# Winery13 CALPELLA DIS N11M-GE1 Schematics

# uFCPGA Mobile Arrandale

# Intel Ibex Peak-M

# 2010-01-13

# REV : A00

*DY : Nopop Component*

*UMA : Pop when schematic is UMA*

*DIS : Pop when schematic is DIS*

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | Cover Page | |
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| Date: Wednesday, January 13, 2010 | Sheet 1 of 88 | |

# Winery CALPELLA Block Diagram

Project code : 91.4EX01.001
Part Number : 48.4EX01.001
PCB P/N : 09288
Revision : A00

## PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Clock Generator
SLG8SP585 7

Nvidia
N11M-GE1(40nm)
80,81,82,83

VRAM(gDDR3)
64Mbx16x4 (512MB) 84,85

VRAM

100MHz/
2.5Gbps

PCIe x 16

Bandwidth
:8GB

Intel CPU
Arrandale
8,9,10,11,12,13,14

DDRIII 1066 Channel A
800/1066MHz

DDR III 1066 Channel B
800/1066MHz

DDRIII 1066 Slot 0 18

DDRIII 1066 Slot 1 19

Power SW
TPS2231R 34

New Card
(FPC Cable to Connect) 34

PCIE x 1 & USB 2.0 x 1

LVDS

RGB CRT

CRT 55

LCD
(Single Chanel) 54

Switchable
74

RGB CRT

LVDS

DMIx4
2.5 GT/s

FDI (UMA)
2.7 GT/s

100MHz
2.5Gbps
PCIE

Intel
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE

20,21,22,23,24,25,26,27,28

PCIE x 1

10/100/1000LOM
RTL8111DL 35

RJ45
CONN

USB 2.0 x 2

PCIE x 1

Mini-Card
WWAN/ WiMAX?

USB 2.0 x 1

Left Side:
USB x 1

(On daughter board)

USB 2.0
480Mbps

USB 2.0 x 1

PCIE x 1

Mini-Card
WLAN 802.11a/b/g/n 64

CardReader
REALTEK
RTS5138
32

(3 in 1)
SD/MMC/MMC+ 33

USB 2.0
480Mbps

USB 2.0 x 1

Right Side:
USB x 1 63

SM Bus
400KHz

Free fall sensor 40

USB 2.0 x 1

Bluetooth 73

CAMERA 73

USB2.0 x 1

Digital Mic Array

USB 2.0 x 1

Biometric 78

LPC Bus
33MHz

Azalia
CODEC
OP AMP
IDT
92HD81UA 30

AZALIA
24MHz

MIC IN

HP OUT

1CH SPEAKER
60

SATA, USB

SATA
3Gbps

SPI

KBC
NUVOTON
NPCE781BA0DX 37

SPI

SM Bus

Thermal & Fan
EMC2102 39,58

Capacity Board 78

Flash ROM
256kB 62

Touch
PAD 68

Int.
KB 68

USB,ESATA
Multi-Port x1 63

ODD
HDD 59

Flash ROM
4MB 62

| CPU DC/DC ISL62883 47,48 | |
|---|---|
| INPUTS | OUTPUTS |
| +PWR_SRC | +VCC_CORE |

| SYSTEM DC/DC RT8205B 46 | |
|---|---|
| INPUTS | OUTPUTS |
| +PWR_SRC | +15V_ALW<br>+3.3V_RTC_LDO<br>+5V_ALW<br>+3.3V_ALW |

| SYSTEM DC/DC TPS51116 50 | |
|---|---|
| INPUTS | OUTPUTS |
| +PWR_SRC | +1.5V_SUS<br>+0.75V_DDR_VTT<br>+V_DDR_REF |

| SYSTEM DC/DC ADP3211 53 | |
|---|---|
| INPUTS | OUTPUTS |
| +PWR_SRC | +CPU_GFXCORE |

| SYSTEM DC/DC TPS51218 86 | |
|---|---|
| INPUTS | OUTPUTS |
| +PWR_SRC | +VCC_GFX_CORE |

| CHARGER BQ24745 45 | |
|---|---|
| INPUTS | OUTPUTS |
| +DC_IN<br>+PBATT | +PWR_SRC |

| SYSTEM DC/DC TPS51218 49 | |
|---|---|
| INPUTS | OUTPUTS |
| +PWR_SRC | +1.05V_VTT |

| LDO APL5930 51 | |
|---|---|
| INPUTS | OUTPUTS |
| +3.3V_ALW | +1.8V_RUN |

| LDO RT9025 51 | |
|---|---|
| INPUTS | OUTPUTS |
| +3.3V_ALW | +1.8V_RUN_GPU |

1st Samsung

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Title: Block Diagram

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

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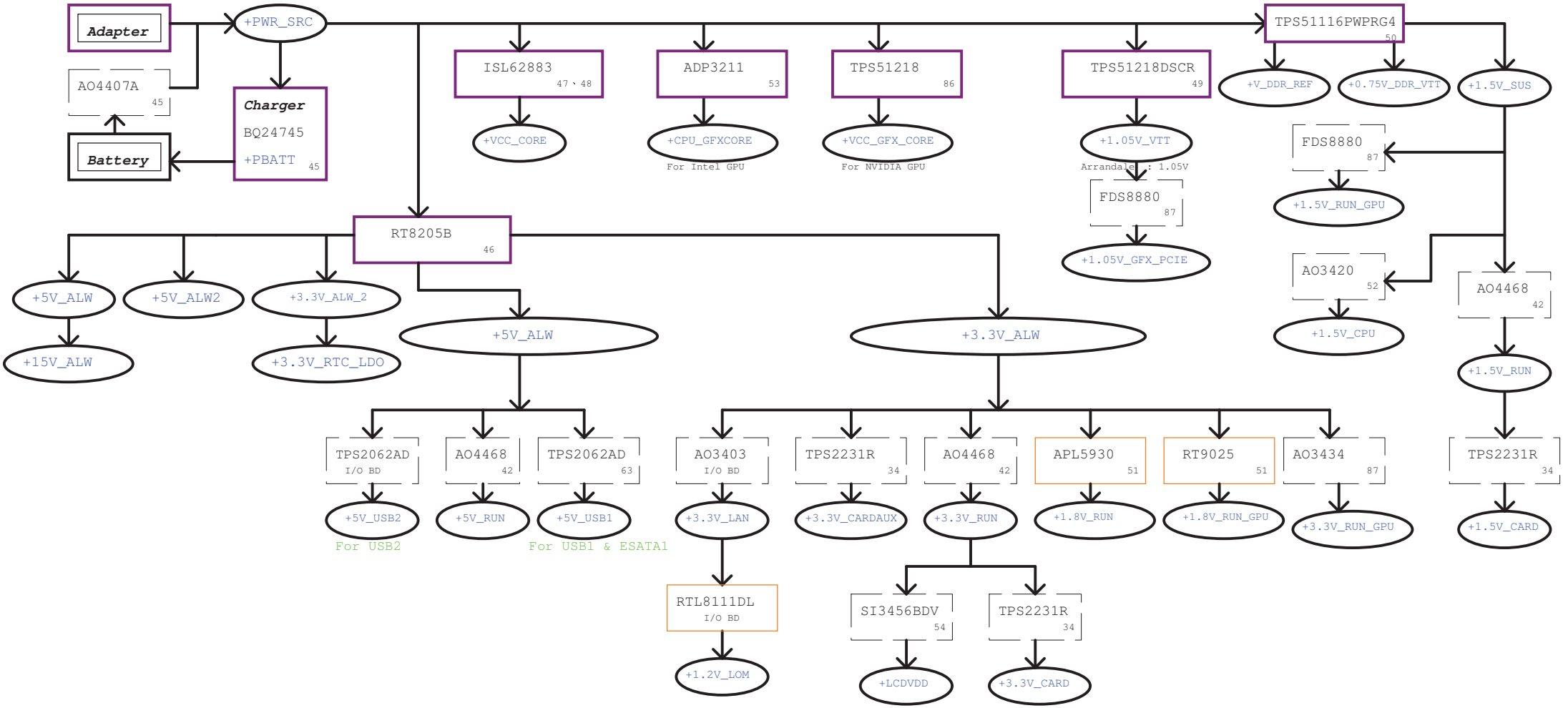


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Title: Power Block Diagram

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

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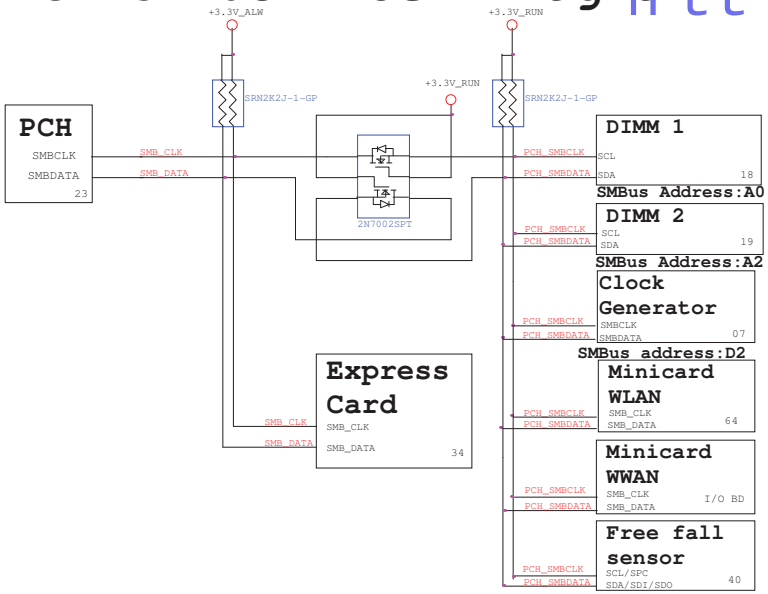
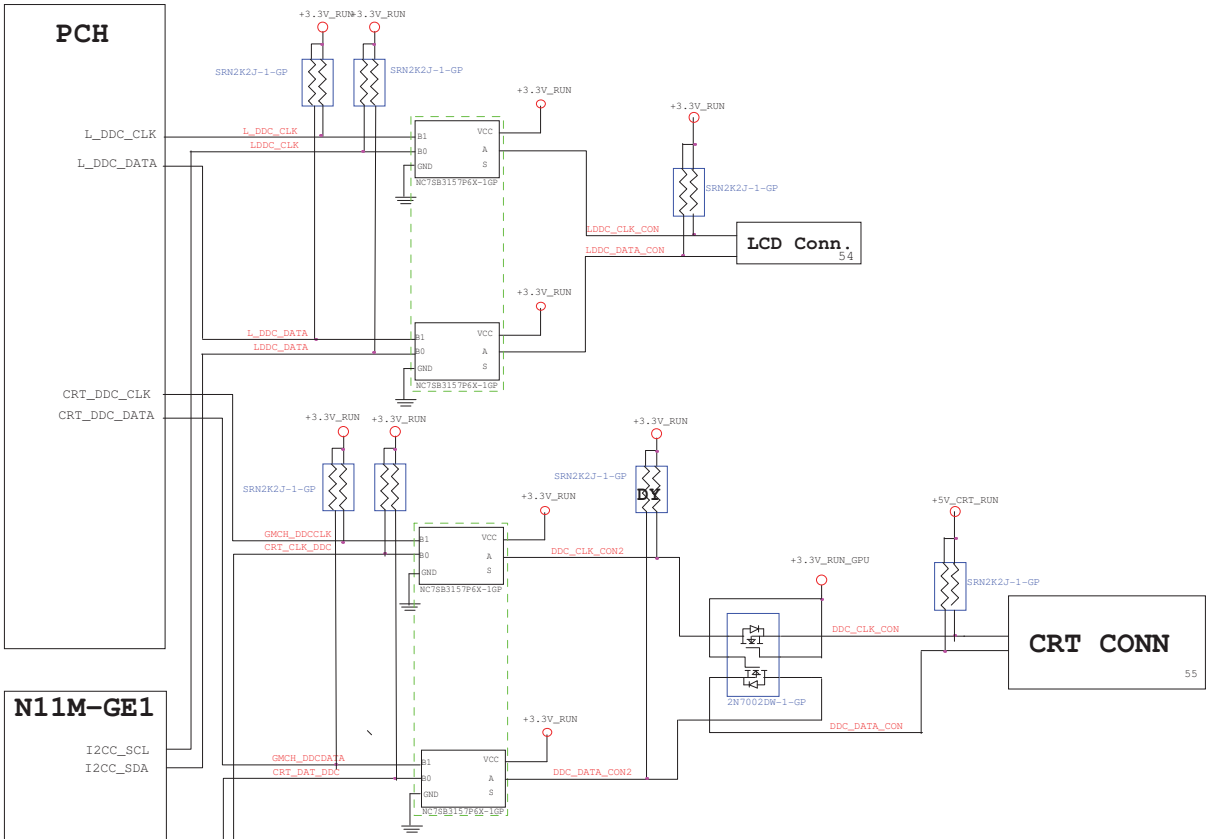
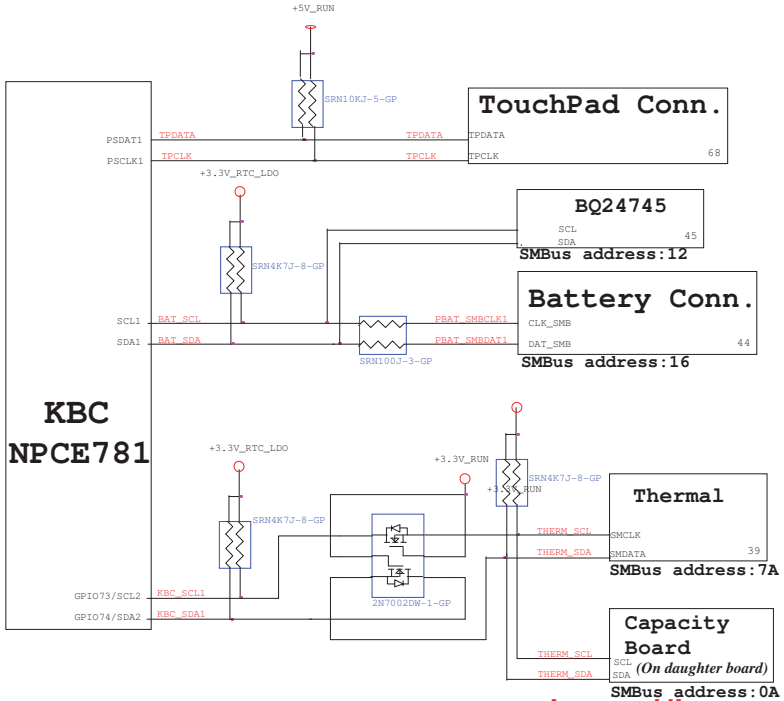
# PCH SMBus Block Diagram




# Switchable Graphic SMBus Block Diagram




# KBC SMBus Block Diagram




Remove HDMI

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Title: SMBUS Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| C | Winery13 MB DIS | A00 |

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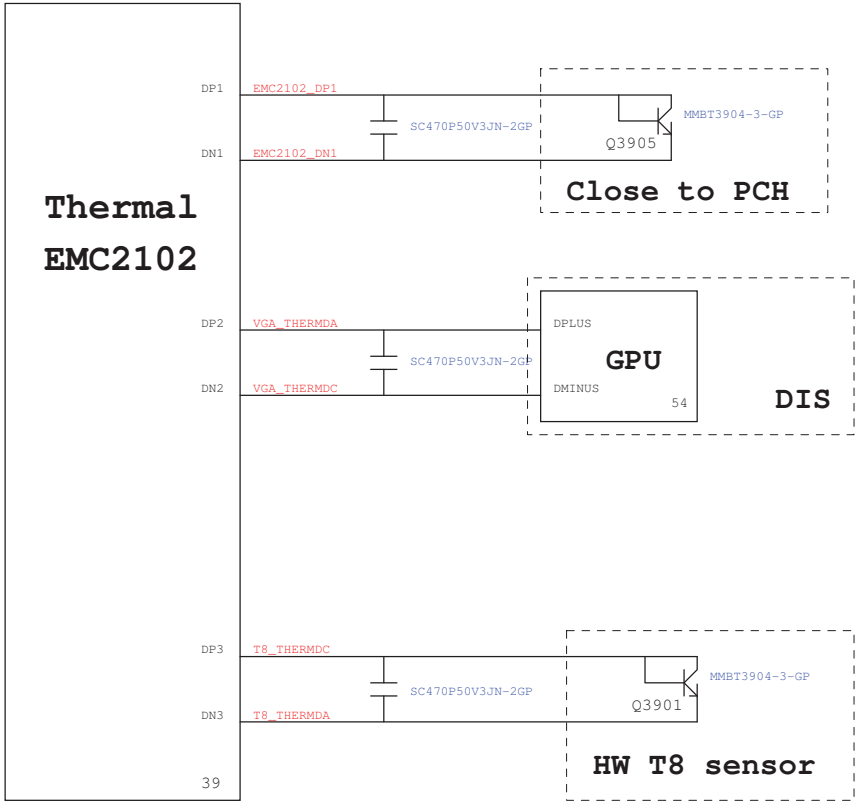
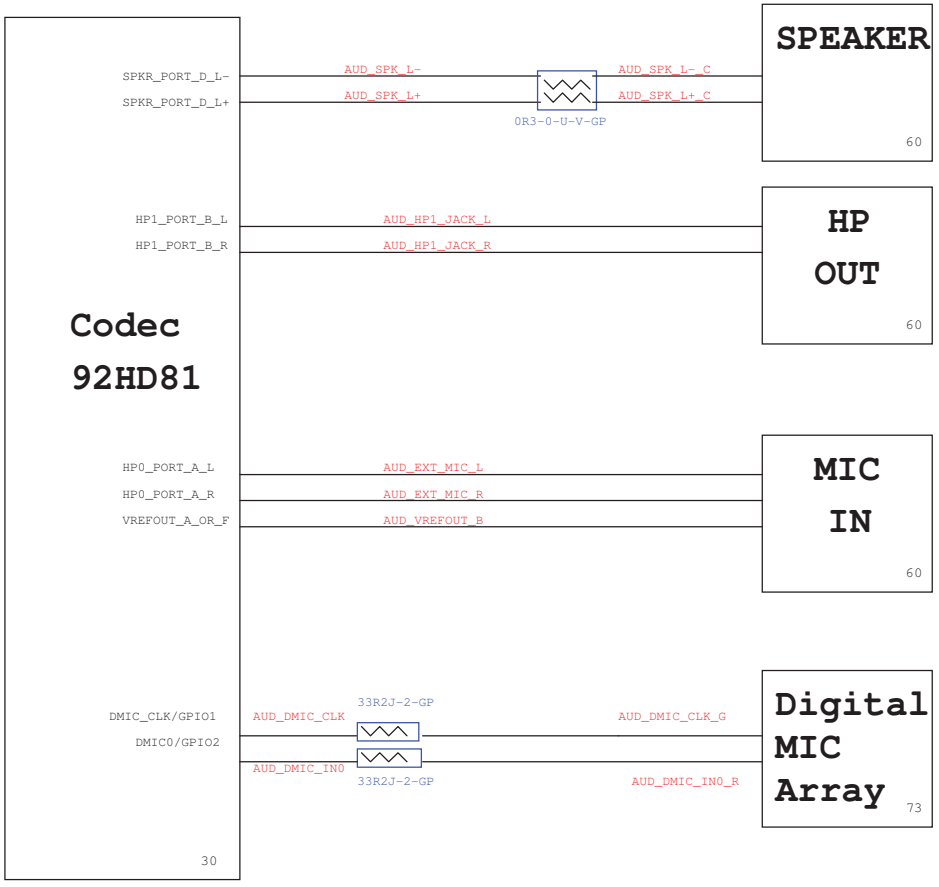
# Thermal Block Diagram




# Audio Block Diagram

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| | | |
|---|---|---|
| Title | Thermal/Audio Block Diagram | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
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## PCH Strapping



| Name | Schematics Notes |
|---|---|
| SPKR | **Reboot option at power-up**<br>**Default Mode:** Internal weak Pull-down.<br>**No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.<br>Intel suggest 1K resistor (Fonseca) |
| INIT3_3V# | Internal pull-up. Leave as "No Connect" |
| GNT3#/ GPIO55 | **Default Mode:** Internal pull-up.<br>**Low (0) = Top Block Swap Mode**<br>Note: Connect to ground with 4.7-kΩ weak pull-down resistor.<br>CRB uses a 1 kΩ; do not stuff resistor. |
| INTVRMEN | **High (1) = Integrated VRM is enabled**<br>**Low (0) = Integrated VRM is disabled**<br>**Note:** CRB uses a 330-kΩ resistor. |
| GNT0#, GNT1# | **Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required.<br>**Boot from PCI:**<br>**Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. |
| GNT2#/ GPIO53 | **Default – Internal pull-up.**<br>**Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops). |
| SPI_MOSI | **Enable Intel Anti-Theft Technology:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br>**Disable Intel Anti-Theft Technology:**Left floating, no pull-down required. |
| NV_ALE | **Enable Intel Anti-Theft Technology:**Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor]<br>**Disable Intel Anti-Theft Technology:**Leave floating (internal pull-down |
| NC_CLE | DMI termination voltage. Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN# /GPIO[33] | **Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.<br>**High (1)-:**Security measure defined in the Flash Descriptor will be enabled.<br>Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently.<br>**Note:**CRB recommends 1-kΩ pull-down for FD Override.<br>There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions. |
| HDA_SDO | Weak internal pull-down. Do not pull high.<br>Sampled at rising edge of RSMRST#. |
| HDA_SYNC | Weak internal pull-down. Do not pull high.<br>Sampled at rising edge of RSMRST#. |
| GPIO15 | **Low (0)-**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality<br>**High (1)-:**Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality<br>**Note:**<br>This is an unmuxed signal.<br>This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low.<br>Sampled at rising edge of RSMRST#.<br>CRB has a 1-kΩ pull-up on this signal to +3.3VA rail. |
| GPIO8 | Weak internal pull-up. Do not pull low.<br>Sampled at rising edge of RSMRST#. |
| GPIO27 | **Default = Do not connect (floating). Internal pull-up.**<br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

## Processor Strapping

Calpella Schematic Checklist Rev1.6

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|---|---|---|---|
| CFG[4] | **Embedded DisplayPort Presence** | **1:** Disabled – No Physical Display Port attached to Embedded DisplayPort.<br>**0:** Enabled – An external Display Port device is connected to the Embedded Display Port. | 1 |
| CFG[3] | **PCI-Express Static Lane Reversal** | **1:** Normal Operation.<br>**0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | 1 |
| CFG[0] | **PCI-Express Configuration Select** | **1:** Single PCI-Express Graphics<br>**0:** Bifurcation enabled | 1 |

## PCIE Routing

| | |
|---|---|
| LANE1 | Card reader |
| LANE2 | MiniCard WLAN |
| LANE3 | LAN |
| LANE4 | MiniCard WWAN |
| LANE5 | New Card |

## USB Table

| USB | |
|---|---|
| Pair | Device |
| 0 | USB1 |
| 1 | USB for ESATA |
| 2 | USB2 |
| 3 | RESERVE |
| 4 | WLAN |
| 5 | WWAN |
| 6 | RESERVED (Not available for HM55) |
| 7 | RESERVED (Not available for HM55) |
| 8 | BlUETOOTH |
| 9 | Card Reader |
| 10 | Biometric |
| 11 | CAMERA |
| 12 | New Card |
| 13 | RESERVED |

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Title: **Table of Content**

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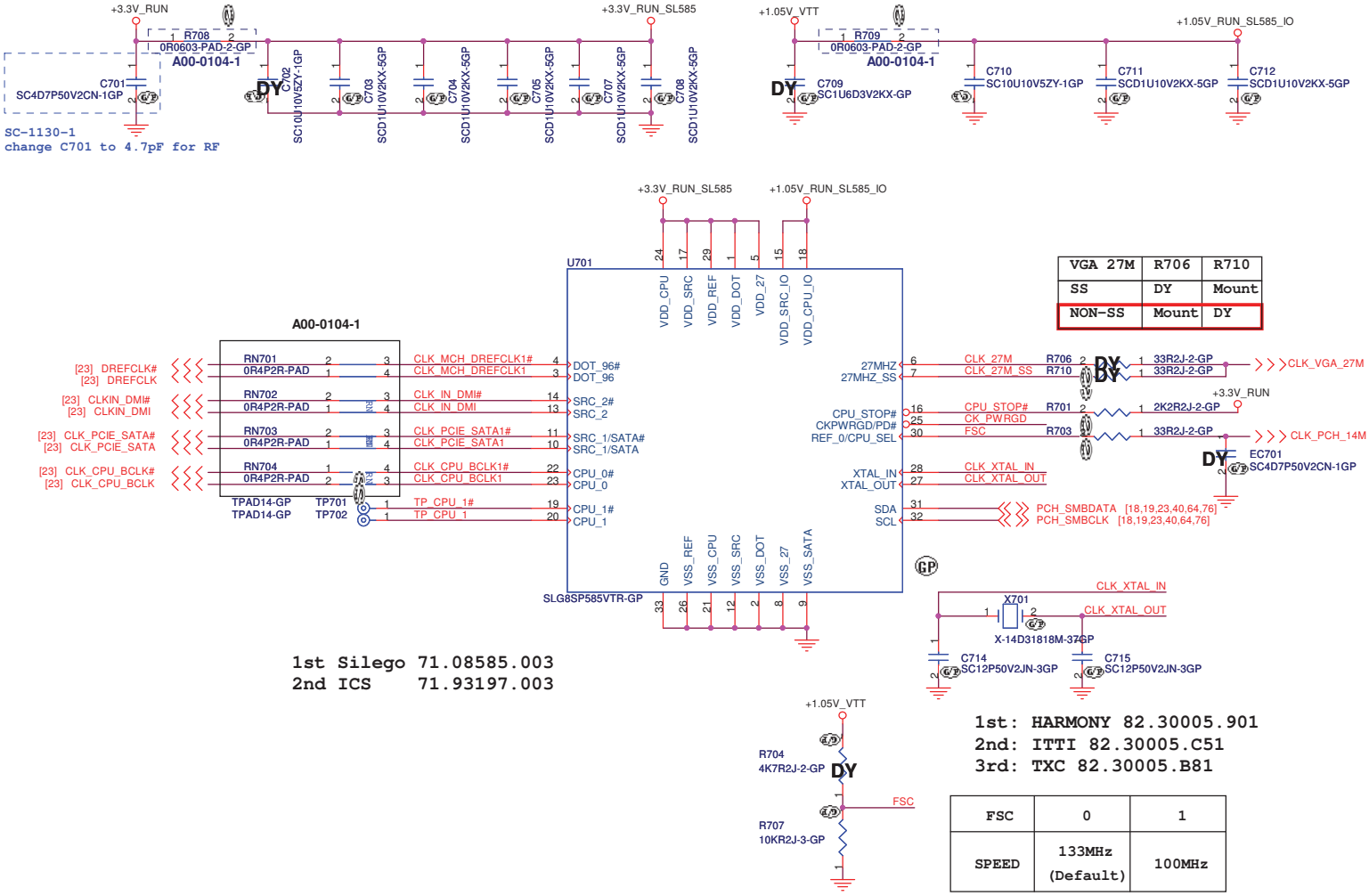
**SSID = Clock GEN**




| VGA 27M | R706 | R710 |
|---|---|---|
| SS | DY | Mount |
| NON-SS | Mount | DY |

1st Silego 71.08585.003
2nd ICS 71.93197.003

1st: HARMONY 82.30005.901
2nd: ITTI 82.30005.C51
3rd: TXC 82.30005.B81

| FSC | 0 | 1 |
|---|---|---|
| SPEED | 133MHz (Default) | 100MHz |

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Title: Clock Generator SLG8SP585

Size | Document Number: Winery13 MB DIS | Rev: A00

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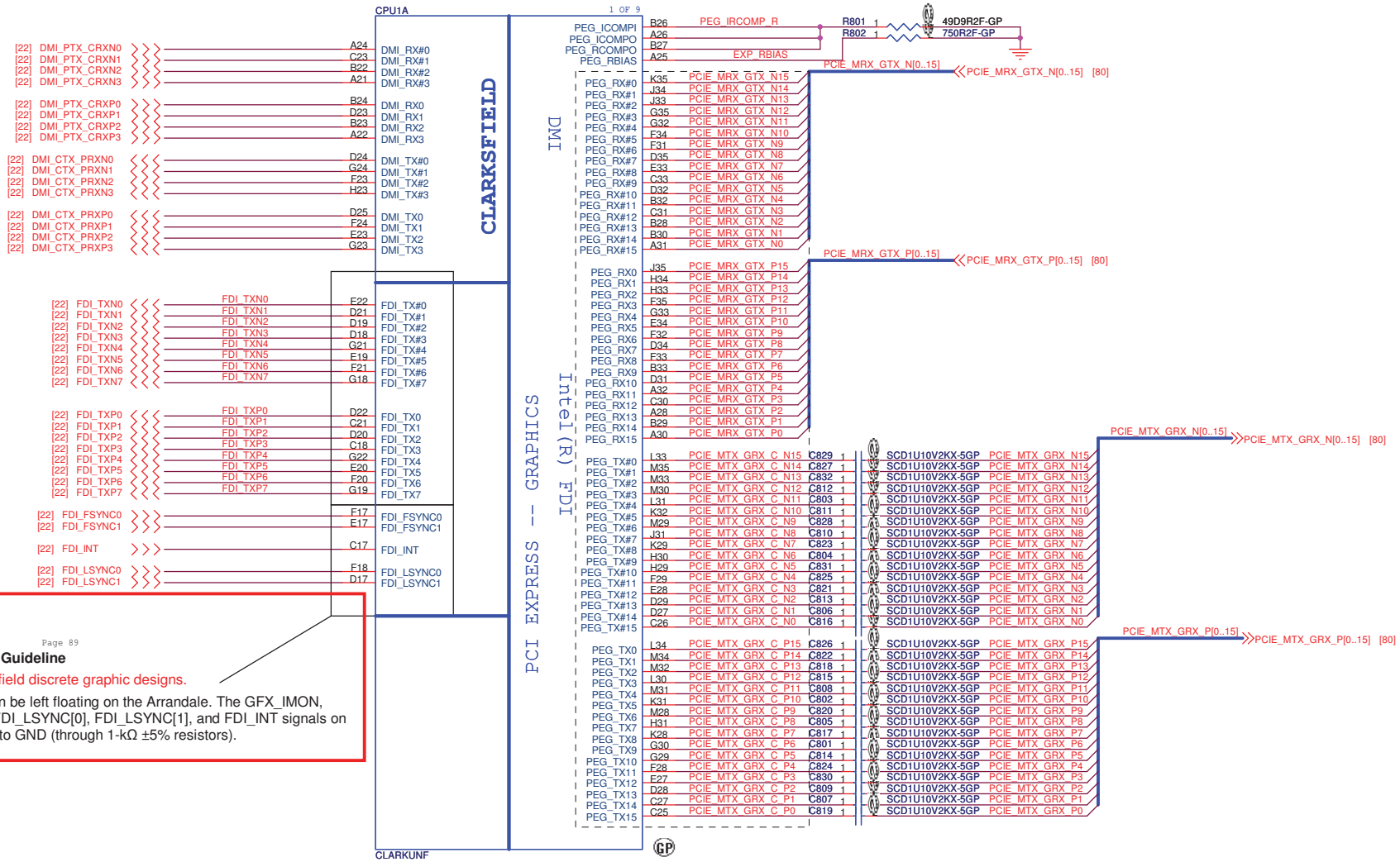
**SSID = CPU**




**Calpella Platform Design Guide**
**Revision 1.6**

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**2.4 Arrandale Graphics Disable Guideline**

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

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Title: CPU (PCIE/DMI/FDI)

Size | Document Number: Winery13 MB DIS | Rev: A00

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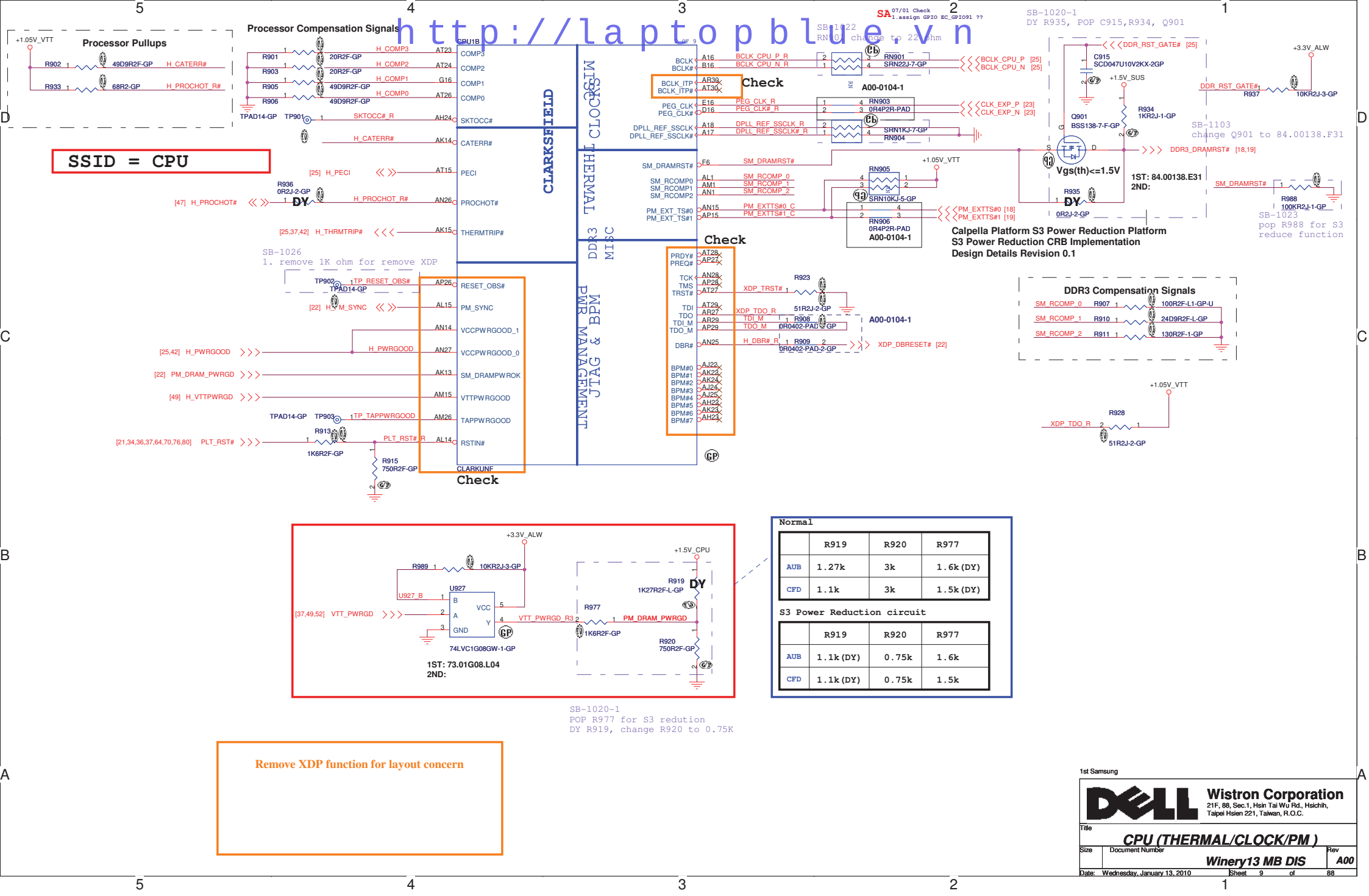


**Normal**

| | R919 | R920 | R977 |
|---|---|---|---|
| AUB | 1.27k | 3k | 1.6k(DY) |
| CFD | 1.1k | 3k | 1.5k(DY) |

**S3 Power Reduction circuit**

| | R919 | R920 | R977 |
|---|---|---|---|
| AUB | 1.1k(DY) | 0.75k | 1.6k |
| CFD | 1.1k(DY) | 0.75k | 1.5k |

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Title: CPU (THERMAL/CLOCK/PM )

Size | Document Number: Winery13 MB DIS | Rev: A00

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SSID = CPU



CPU1C

3 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY A

CLARKUNF

CPU1D

4 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY - B

CLARKUNF

1st Samsung

| | | | |
|---|---|---|---|
| [18] M_A_DQ[63..0] | M_A_DQ0 | A10 | SA_DQ0 |
| | M_A_DQ1 | C10 | SA_DQ1 |
| | M_A_DQ2 | C7 | SA_DQ2 |
| | M_A_DQ3 | A7 | SA_DQ3 |
| | M_A_DQ4 | B10 | SA_DQ4 |
| | M_A_DQ5 | D10 | SA_DQ5 |
| | M_A_DQ6 | E10 | SA_DQ6 |
| | M_A_DQ7 | A8 | SA_DQ7 |
| | M_A_DQ8 | D8 | SA_DQ8 |
| | M_A_DQ9 | F10 | SA_DQ9 |
| | M_A_DQ10 | E6 | SA_DQ10 |
| | M_A_DQ11 | F7 | SA_DQ11 |
| | M_A_DQ12 | E9 | SA_DQ12 |
| | M_A_DQ13 | B7 | SA_DQ13 |
| | M_A_DQ14 | E7 | SA_DQ14 |
| | M_A_DQ15 | C6 | SA_DQ15 |
| | M_A_DQ16 | H10 | SA_DQ16 |
| | M_A_DQ17 | G8 | SA_DQ17 |
| | M_A_DQ18 | K7 | SA_DQ18 |
| | M_A_DQ19 | J8 | SA_DQ19 |
| | M_A_DQ20 | G7 | SA_DQ20 |
| | M_A_DQ21 | G10 | SA_DQ21 |
| | M_A_DQ22 | J7 | SA_DQ22 |
| | M_A_DQ23 | J10 | SA_DQ23 |
| | M_A_DQ24 | L7 | SA_DQ24 |
| | M_A_DQ25 | M6 | SA_DQ25 |
| | M_A_DQ26 | M8 | SA_DQ26 |
| | M_A_DQ27 | L9 | SA_DQ27 |
| | M_A_DQ28 | L6 | SA_DQ28 |
| | M_A_DQ29 | K8 | SA_DQ29 |
| | M_A_DQ30 | N8 | SA_DQ30 |
| | M_A_DQ31 | P9 | SA_DQ31 |
| | M_A_DQ32 | AH5 | SA_DQ32 |
| | M_A_DQ33 | AF5 | SA_DQ33 |
| | M_A_DQ34 | AK6 | SA_DQ34 |
| | M_A_DQ35 | AK7 | SA_DQ35 |
| | M_A_DQ36 | AF6 | SA_DQ36 |
| | M_A_DQ37 | AG5 | SA_DQ37 |
| | M_A_DQ38 | AJ7 | SA_DQ38 |
| | M_A_DQ39 | AJ6 | SA_DQ39 |
| | M_A_DQ40 | AJ10 | SA_DQ40 |
| | M_A_DQ41 | AJ9 | SA_DQ41 |
| | M_A_DQ42 | AL10 | SA_DQ42 |
| | M_A_DQ43 | AK12 | SA_DQ43 |
| | M_A_DQ44 | AK8 | SA_DQ44 |
| | M_A_DQ45 | AL7 | SA_DQ45 |
| | M_A_DQ46 | AK11 | SA_DQ46 |
| | M_A_DQ47 | AL8 | SA_DQ47 |
| | M_A_DQ48 | AN8 | SA_DQ48 |
| | M_A_DQ49 | AM10 | SA_DQ49 |
| | M_A_DQ50 | AR11 | SA_DQ50 |
| | M_A_DQ51 | AL11 | SA_DQ51 |
| | M_A_DQ52 | AM9 | SA_DQ52 |
| | M_A_DQ53 | AN9 | SA_DQ53 |
| | M_A_DQ54 | AT11 | SA_DQ54 |
| | M_A_DQ55 | AP12 | SA_DQ55 |
| | M_A_DQ56 | AM12 | SA_DQ56 |
| | M_A_DQ57 | AN12 | SA_DQ57 |
| | M_A_DQ58 | AM13 | SA_DQ58 |
| | M_A_DQ59 | AT14 | SA_DQ59 |
| | M_A_DQ60 | AT12 | SA_DQ60 |
| | M_A_DQ61 | AL13 | SA_DQ61 |
| | M_A_DQ62 | AR14 | SA_DQ62 |
| | M_A_DQ63 | AP14 | SA_DQ63 |

| | | | |
|---|---|---|---|
| [18] M_A_BS0 | AC3 | SA_BS0 | |
| [18] M_A_BS1 | AB2 | SA_BS1 | |
| [18] M_A_BS2 | U7 | SA_BS2 | |
| [18] M_A_CAS# | AE1 | SA_CAS# | |
| [18] M_A_RAS# | AB3 | SA_RAS# | |
| [18] M_A_WE# | AE9 | SA_WE# | |

| | | | |
|---|---|---|---|
| SA_CK0 | AA6 | M_CLK_DDR0 | [18] |
| SA_CK#0 | AA7 | M_CLK_DDR#0 | [18] |
| SA_CKE0 | P7 | M_CKE0 | [18] |
| SA_CK1 | Y6 | M_CLK_DDR1 | [18] |
| SA_CK#1 | Y5 | M_CLK_DDR#1 | [18] |
| SA_CKE1 | P6 | M_CKE1 | [18] |
| SA_CS#0 | AE2 | M_CS0# | [18] |
| SA_CS#1 | AE8 | M_CS1# | [18] |
| SA_ODT0 | AD8 | M_ODT0 | [18] |
| SA_ODT1 | AF9 | M_ODT1 | [18] |

| | | | |
|---|---|---|---|
| SA_DM0 | B9 | M_A_DM0 | |
| SA_DM1 | D7 | M_A_DM1 | |
| SA_DM2 | H7 | M_A_DM2 | |
| SA_DM3 | M7 | M_A_DM3 | |
| SA_DM4 | AG6 | M_A_DM4 | |
| SA_DM5 | AM7 | M_A_DM5 | |
| SA_DM6 | AN10 | M_A_DM6 | |
| SA_DM7 | AN13 | M_A_DM7 | |

M_A_DM[7..0] [18]

M_A_DQS#[7..0] [18]

M_A_DQS[7..0] [18]

M_A_A[15..0] [18]

| | | |
|---|---|---|
| SA_DQS#0 | C9 | M_A_DQS#0 |
| SA_DQS#1 | F8 | M_A_DQS#1 |
| SA_DQS#2 | J9 | M_A_DQS#2 |
| SA_DQS#3 | N9 | M_A_DQS#3 |
| SA_DQS#4 | AH7 | M_A_DQS#4 |
| SA_DQS#5 | AK9 | M_A_DQS#5 |
| SA_DQS#6 | AP11 | M_A_DQS#6 |
| SA_DQS#7 | AT13 | M_A_DQS#7 |
| SA_DQS0 | C8 | M_A_DQS0 |
| SA_DQS1 | F9 | M_A_DQS1 |
| SA_DQS2 | H9 | M_A_DQS2 |
| SA_DQS3 | M9 | M_A_DQS3 |
| SA_DQS4 | AH8 | M_A_DQS4 |
| SA_DQS5 | AK10 | M_A_DQS5 |
| SA_DQS6 | AN11 | M_A_DQS6 |
| SA_DQS7 | AR13 | M_A_DQS7 |

| | | | |
|---|---|---|---|
| SA_MA0 | Y3 | M_A_A0 | |
| SA_MA1 | W1 | M_A_A1 | |
| SA_MA2 | AA8 | M_A_A2 | |
| SA_MA3 | AA3 | M_A_A3 | |
| SA_MA4 | V1 | M_A_A4 | |
| SA_MA5 | AA9 | M_A_A5 | |
| SA_MA6 | V8 | M_A_A6 | |
| SA_MA7 | T1 | M_A_A7 | |
| SA_MA8 | Y9 | M_A_A8 | |
| SA_MA9 | U6 | M_A_A9 | |
| SA_MA10 | AD4 | M_A_A10 | |
| SA_MA11 | T2 | M_A_A11 | |
| SA_MA12 | U3 | M_A_A12 | |
| SA_MA13 | AG8 | M_A_A13 | |
| SA_MA14 | T3 | M_A_A14 | |
| SA_MA15 | V9 | M_A_A15 | |

[19] M_B_DQ[63..0]

M_B_DQ[63..0]

| | | | |
|---|---|---|---|
| M_B_DQ0 | B5 | SB_DQ0 | |
| M_B_DQ1 | A5 | SB_DQ1 | |
| M_B_DQ2 | C3 | SB_DQ2 | |
| M_B_DQ3 | B3 | SB_DQ3 | |
| M_B_DQ4 | E4 | SB_DQ4 | |
| M_B_DQ5 | A6 | SB_DQ5 | |
| M_B_DQ6 | A4 | SB_DQ6 | |
| M_B_DQ7 | C4 | SB_DQ7 | |
| M_B_DQ8 | D1 | SB_DQ8 | |
| M_B_DQ9 | D2 | SB_DQ9 | |
| M_B_DQ10 | F2 | SB_DQ10 | |
| M_B_DQ11 | F1 | SB_DQ11 | |
| M_B_DQ12 | C2 | SB_DQ12 | |
| M_B_DQ13 | F5 | SB_DQ13 | |
| M_B_DQ14 | F3 | SB_DQ14 | |
| M_B_DQ15 | G4 | SB_DQ15 | |
| M_B_DQ16 | H6 | SB_DQ16 | |
| M_B_DQ17 | G2 | SB_DQ17 | |
| M_B_DQ18 | J6 | SB_DQ18 | |
| M_B_DQ19 | J3 | SB_DQ19 | |
| M_B_DQ20 | G1 | SB_DQ20 | |
| M_B_DQ21 | G5 | SB_DQ21 | |
| M_B_DQ22 | J2 | SB_DQ22 | |
| M_B_DQ23 | J1 | SB_DQ23 | |
| M_B_DQ24 | J5 | SB_DQ24 | |
| M_B_DQ25 | K2 | SB_DQ25 | |
| M_B_DQ26 | L3 | SB_DQ26 | |
| M_B_DQ27 | M1 | SB_DQ27 | |
| M_B_DQ28 | K5 | SB_DQ28 | |
| M_B_DQ29 | K4 | SB_DQ29 | |
| M_B_DQ30 | M4 | SB_DQ30 | |
| M_B_DQ31 | N5 | SB_DQ31 | |
| M_B_DQ32 | AF3 | SB_DQ32 | |
| M_B_DQ33 | AG1 | SB_DQ33 | |
| M_B_DQ34 | AJ3 | SB_DQ34 | |
| M_B_DQ35 | AK1 | SB_DQ35 | |
| M_B_DQ36 | AG4 | SB_DQ36 | |
| M_B_DQ37 | AG3 | SB_DQ37 | |
| M_B_DQ38 | AJ4 | SB_DQ38 | |
| M_B_DQ39 | AH4 | SB_DQ39 | |
| M_B_DQ40 | AK3 | SB_DQ40 | |
| M_B_DQ41 | AK4 | SB_DQ41 | |
| M_B_DQ42 | AM6 | SB_DQ42 | |
| M_B_DQ43 | AN2 | SB_DQ43 | |
| M_B_DQ44 | AK5 | SB_DQ44 | |
| M_B_DQ45 | AK2 | SB_DQ45 | |
| M_B_DQ46 | AM4 | SB_DQ46 | |
| M_B_DQ47 | AM3 | SB_DQ47 | |
| M_B_DQ48 | AP3 | SB_DQ48 | |
| M_B_DQ49 | AN5 | SB_DQ49 | |
| M_B_DQ50 | AT4 | SB_DQ50 | |
| M_B_DQ51 | AN6 | SB_DQ51 | |
| M_B_DQ52 | AN4 | SB_DQ52 | |
| M_B_DQ53 | AN3 | SB_DQ53 | |
| M_B_DQ54 | AT5 | SB_DQ54 | |
| M_B_DQ55 | AT6 | SB_DQ55 | |
| M_B_DQ56 | AN7 | SB_DQ56 | |
| M_B_DQ57 | AP6 | SB_DQ57 | |
| M_B_DQ58 | AP8 | SB_DQ58 | |
| M_B_DQ59 | AT9 | SB_DQ59 | |
| M_B_DQ60 | AT7 | SB_DQ60 | |
| M_B_DQ61 | AP9 | SB_DQ61 | |
| M_B_DQ62 | AR10 | SB_DQ62 | |
| M_B_DQ63 | AT10 | SB_DQ63 | |

| | | | |
|---|---|---|---|
| [19] M_B_BS0 | AB1 | SB_BS0 | |
| [19] M_B_BS1 | W5 | SB_BS1 | |
| [19] M_B_BS2 | R7 | SB_BS2 | |
| [19] M_B_CAS# | AC5 | SB_CAS# | |
| [19] M_B_RAS# | Y7 | SB_RAS# | |
| [19] M_B_WE# | AC6 | SB_WE# | |

| | | | |
|---|---|---|---|
| SB_CK0 | W8 | M_CLK_DDR2 | [19] |
| SB_CK#0 | W9 | M_CLK_DDR#2 | [19] |
| SB_CKE0 | M3 | M_CKE2 | [19] |
| SB_CK1 | V7 | M_CLK_DDR3 | [19] |
| SB_CK#1 | V6 | M_CLK_DDR#3 | [19] |
| SB_CKE1 | M2 | M_CKE3 | [19] |
| SB_CS#0 | AB8 | M_CS2# | [19] |
| SB_CS#1 | AD6 | M_CS3# | [19] |
| SB_ODT0 | AC7 | M_ODT2 | [19] |
| SB_ODT1 | AD1 | M_ODT3 | [19] |

| | | | |
|---|---|---|---|
| SB_DM0 | D4 | M_B_DM0 | |
| SB_DM1 | E1 | M_B_DM1 | |
| SB_DM2 | H3 | M_B_DM2 | |
| SB_DM3 | K1 | M_B_DM3 | |
| SB_DM4 | AH1 | M_B_DM4 | |
| SB_DM5 | AL2 | M_B_DM5 | |
| SB_DM6 | AR4 | M_B_DM6 | |
| SB_DM7 | AT8 | M_B_DM7 | |

M_B_DM[7..0] [19]

M_B_DQS#[7..0] [19]

M_B_DQS[7..0] [19]

M_B_A[15..0] [19]

| | | | |
|---|---|---|---|
| SB_DQS#0 | D5 | M_B_DQS#0 | |
| SB_DQS#1 | F4 | M_B_DQS#1 | |
| SB_DQS#2 | J4 | M_B_DQS#2 | |
| SB_DQS#3 | L4 | M_B_DQS#3 | |
| SB_DQS#4 | AH2 | M_B_DQS#4 | |
| SB_DQS#5 | AL4 | M_B_DQS#5 | |
| SB_DQS#6 | AR5 | M_B_DQS#6 | |
| SB_DQS#7 | AR8 | M_B_DQS#7 | |
| SB_DQS0 | C5 | M_B_DQS0 | |
| SB_DQS1 | E3 | M_B_DQS1 | |
| SB_DQS2 | H4 | M_B_DQS2 | |
| SB_DQS3 | M5 | M_B_DQS3 | |
| SB_DQS4 | AG2 | M_B_DQS4 | |
| SB_DQS5 | AL5 | M_B_DQS5 | |
| SB_DQS6 | AP5 | M_B_DQS6 | |
| SB_DQS7 | AR7 | M_B_DQS7 | |

| | | | |
|---|---|---|---|
| SB_MA0 | U5 | M_B_A0 | |
| SB_MA1 | V2 | M_B_A1 | |
| SB_MA2 | T5 | M_B_A2 | |
| SB_MA3 | V3 | M_B_A3 | |
| SB_MA4 | R1 | M_B_A4 | |
| SB_MA5 | T8 | M_B_A5 | |
| SB_MA6 | R2 | M_B_A6 | |
| SB_MA7 | R6 | M_B_A7 | |
| SB_MA8 | R4 | M_B_A8 | |
| SB_MA9 | R5 | M_B_A9 | |
| SB_MA10 | AB5 | M_B_A10 | |
| SB_MA11 | P3 | M_B_A11 | |
| SB_MA12 | R3 | M_B_A12 | |
| SB_MA13 | AF7 | M_B_A13 | |
| SB_MA14 | P5 | M_B_A14 | |
| SB_MA15 | N1 | M_B_A15 | |

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Title: CPU (DDR)

| Size | Document Number | Rev |
|---|---|---|
| | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 10 of 88

**SSID = CPU**

CFG0

R1101 3KR2F-GP

DY

| PCI-Express Configuration Select | |
|---|---|
| CFG0 | 1:Single PEG<br>0:Bifurcation enabled |

DISBX5%

CFG3

R1102 3KR2F-GP

| CFG3 - PCI-Express Static Lane Reversal | |
|---|---|
| CFG3 | 1 :Normal Operation<br>0 :Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |

DW

07/10 Reversal
1.PCI-Express Static Lane Reversal

CFG4

R1103 3KR2F-GP

DY

| CFG4 - Display Port Presence | |
|---|---|
| CFG4 | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |

**Calpella Platform Design Guide**
**Revision 1.6**

**4.8.3.1 LVDS Switching**

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

**4.8.3.2 eDP Switching**

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

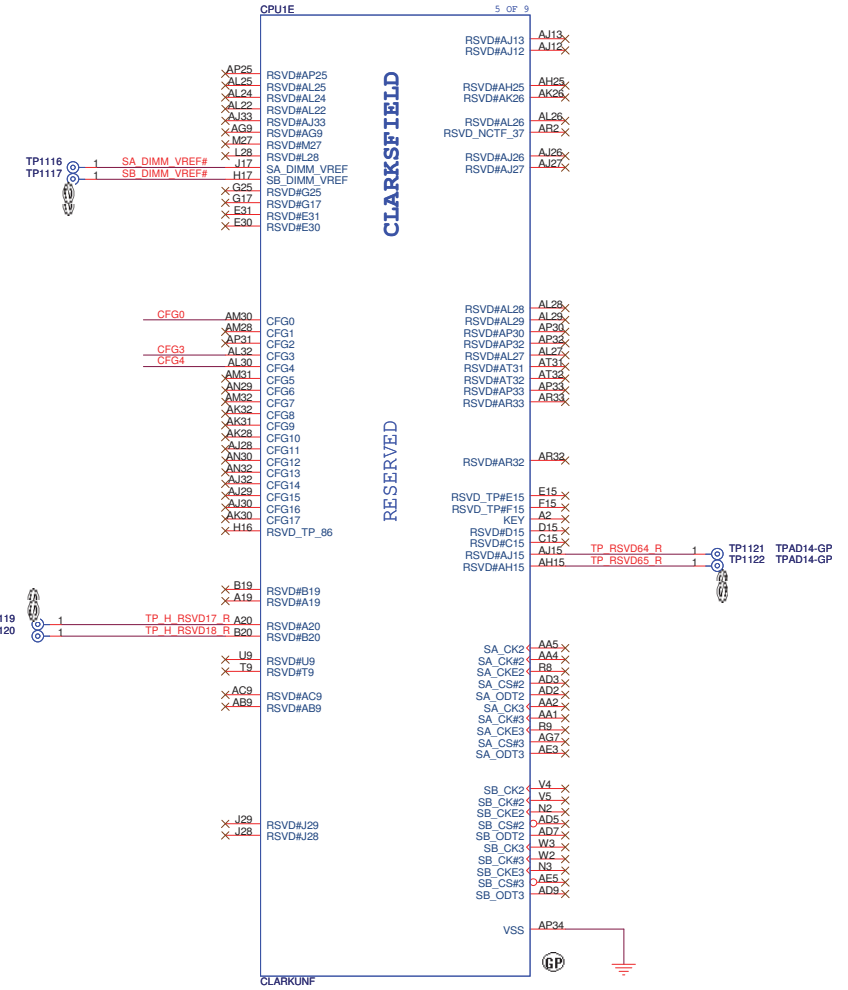
Page 482,486

DW

07/02 Added
1.Added display Switchable strap commentariat

| CFG7(Reserved) - Temporarily used for early Clarksfield samples. | |
|---|---|
| CFG7 | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.<br><br>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality. |

DW30 Only support Arrandale, CFG7 no need pull down

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| Title | | |
|---|---|---|
| CPU (RESERVED) | | |
| Size | Document Number | Rev |
| | Winery13 MB DIS | A00 |
| Date: Wednesday, January 13, 2010 | Sheet 11 of 88 | |

SSID = CPU

PROCESSOR CORE POWER

48A (Arburdale)

18A

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

SA

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

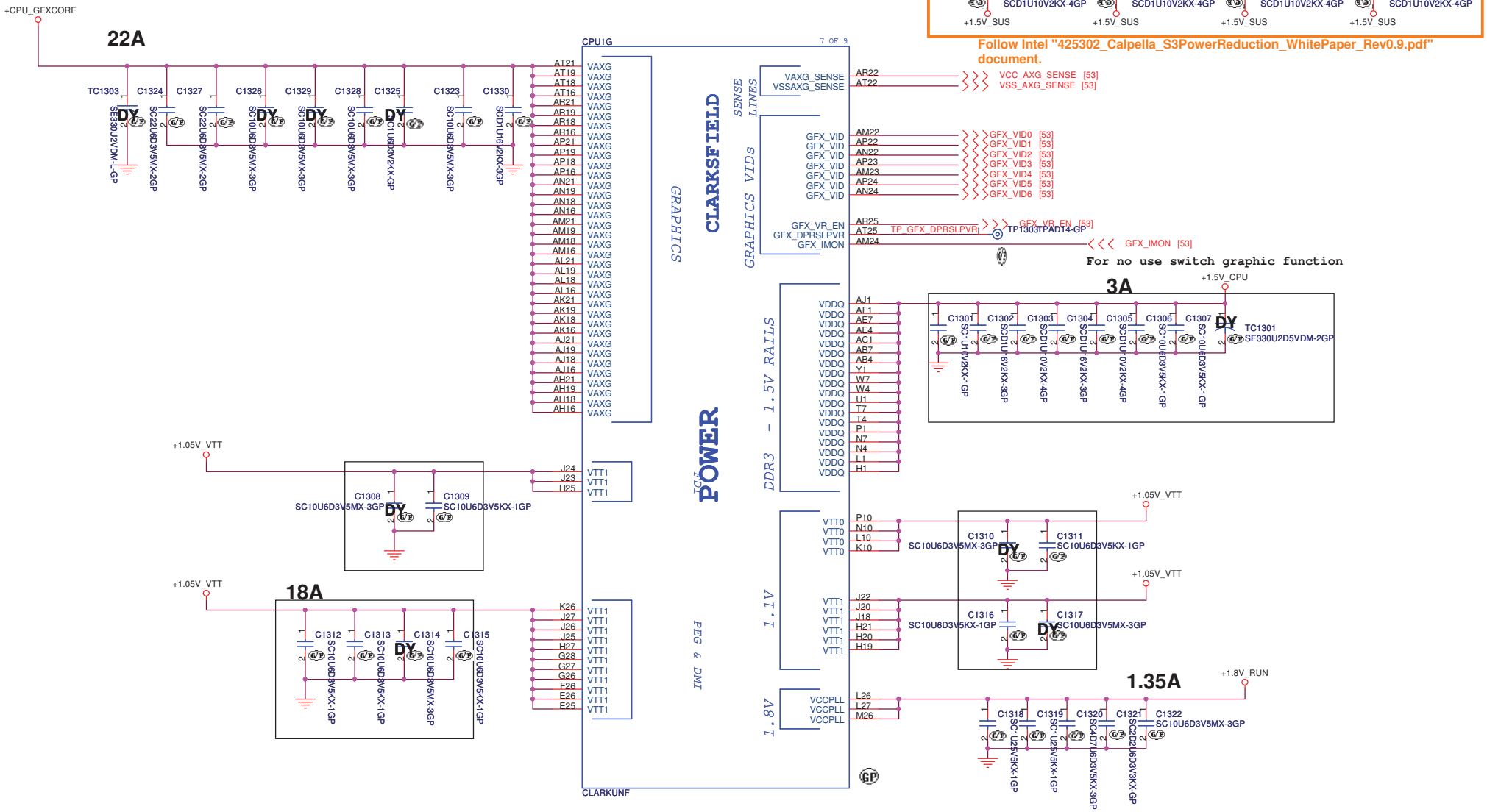
Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V

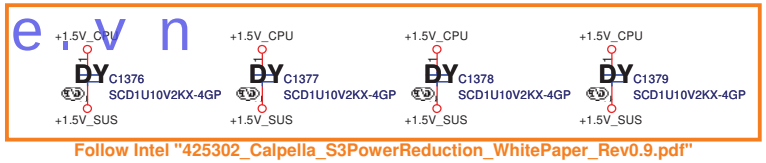
H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SC-1207-1
pop C1243 and change size to 0603 for EMI

| | |
|---|---|
| Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | CPU (VCC_CORE) |
| Size | Document Number: Winery13 MB DIS |
| Rev | A00 |
| Date: Wednesday, January 13, 2010 | Sheet 12 of 88 |

SSID = CPU




Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

1st Samsung

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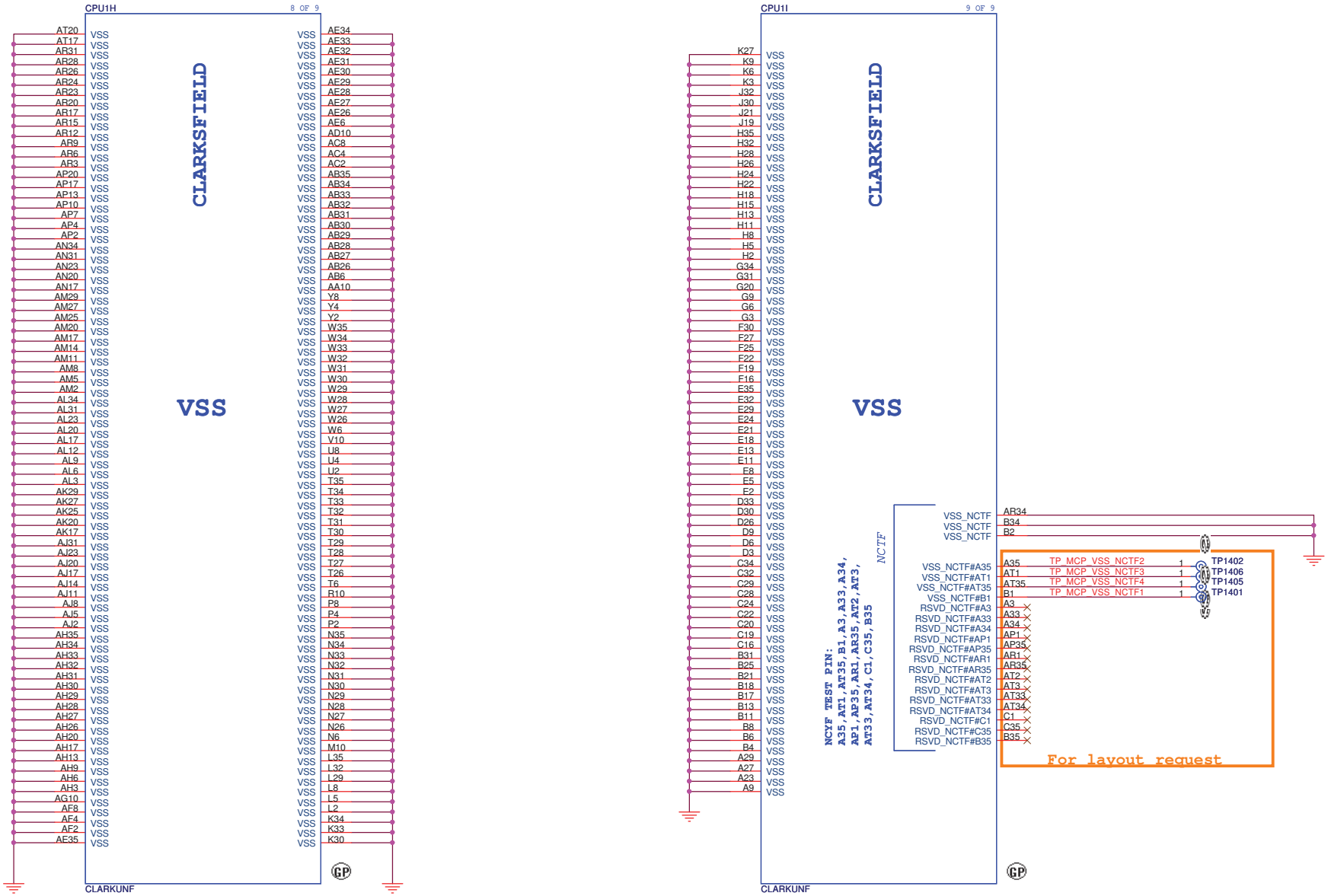
| | | |
|---|---|---|
| Title | CPU (VCC_GFXCORE) | |
| Size | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 13 of 88 | |

SSID = CPU




1st Samsung

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Title: CPU (VSS)

Size | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 14 of 88

(Blanking)

1st Samsung

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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *Winery13 MB DIS* | *A00* |

Date: Wednesday, January 13, 2010 Sheet 15 of 88

(Blanking)

1st Samsung

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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *Winery13 MB DIS* | *A00* |

Date: Wednesday, January 13, 2010 Sheet 16 of 88

(Blank)

1st Samsung

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Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 17 of 88

**SSID = MEMORY**

[10] M_A_DQS#[7..0]
[10] M_A_DQ[63..0]
[10] M_A_DM[7..0]
[10] M_A_DQS[7..0]
[10] M_A_A[15..0]

DM1

[10] M_A_BS2
[10] M_A_BS0
[10] M_A_BS1

M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15 M_A_BS2
M_A_BS0 M_A_BS1
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
M_ODT0 M_ODT1

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF_CA VREF_DQ
RESET#
VTT1 VTT2

NP1 NP2
RAS# WE# CAS#
CS0# CS1#
CKE0 CKE1
CK0 CK0# CK1 CK1#
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL
EVENT#
VDDSPD
SA0 SA1
NC#1 NC#2 NC#/TEST
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VSS

M_A_RAS# [10]
M_A_WE# [10]
M_A_CAS# [10]
M_CS0# [10]
M_CS1# [10]
M_CKE0 [10]
M_CKE1 [10]
M_CLK_DDR0 [10]
M_CLK_DDR#0 [10]
M_CLK_DDR1 [10]
M_CLK_DDR#1 [10]
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
PCH_SMBDATA [7,19,23,40,64,76]
PCH_SMBCLK [7,19,23,40,64,76]
PM_EXTTS#0 [9]
+3.3V_RUN
SA0_DM1
SA1_DM1
+1.5V_SUS

Height 5.2mm

DDR3-204P-25-GP

SMBUS address:A0
R1802 10KR2J-3-GP
R1801 10KR2J-3-GP

DW
07/02 Reserve
1.Added SA0_DM1 pull-up resistor
07/07
2.Reserve pull-hi,lo resistor

C1806 SCD1U10V2KX-5GP
C1807 SC2D2U6D3V3KX-GP DY

Layout Note:
Place near DM1
+1.5V_SUS
C1802 SC10U6D3V5KX-1GP
C1803 SC10U6D3V5KX-1GP
C1804 SC10U6D3V5KX-1GP
C1811 SC10U6D3V5KX-1GP
C1812 SC10U6D3V5KX-1GP
C1816 SC10U6D3V5KX-1GP
C1817 SC10U6D3V5MX-3GP DY

Layout Note:
Put close to VTT1,VTT2.
Layout Note:
Put between two SO-DIMM
+0.75V_DDR_VTT
C1801 SC1U6D3V2KX-1GP DY
C1813 SC1U6D3V2KX-1GP DY
C1814 SC1U6D3V2KX-1GP DY
C1815 SC1U6D3V2KX-1GP DY
C1823 SC10U6D3V5MX-3GP DY

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

+1.5V_SUS
C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875 SCD1U10V3KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

put near connector
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1821 DUMMY-C2
C1819 DUMMY-C2
C1820 DUMMY-C2
C1818 DUMMY-C2

+V_DDR_REF
C1810 SCD1U10V2KX-5GP
C1817 SCD1U10V2KX-5GP
C1809 SC2D2U6D3V3KX-GP DY
+0.75V_DDR_VTT
[9,19] DDR3_DRAMRST#

1st Samsung

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Title: DDRIII-SODIMM SLOT1
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 18 of 88

**SSID = MEMORY**

Change CONN
2009/06/01

[10] M_B_DQS#[7..0]
[10] M_B_DQ[63..0]
[10] M_B_DM[7..0]
[10] M_B_DQS[7..0]
[10] M_B_A[15..0]

DM2

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15
[10] M_B_BS2 M_B_BS2 79 A16/BA2
[10] M_B_BS0 M_B_BS0 109 BA0
[10] M_B_BS1 M_B_BS1 108 BA1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
M_B_DQ23 52 DQ23
M_B_DQ24 57 DQ24
M_B_DQ25 59 DQ25
M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
M_B_DQ32 129 DQ32
M_B_DQ33 131 DQ33
M_B_DQ34 141 DQ34
M_B_DQ35 143 DQ35
M_B_DQ36 130 DQ36
M_B_DQ37 132 DQ37
M_B_DQ38 140 DQ38
M_B_DQ39 142 DQ39
M_B_DQ40 147 DQ40
M_B_DQ41 149 DQ41
M_B_DQ42 157 DQ42
M_B_DQ43 159 DQ43
M_B_DQ44 146 DQ44
M_B_DQ45 148 DQ45
M_B_DQ46 158 DQ46
M_B_DQ47 160 DQ47
M_B_DQ48 163 DQ48
M_B_DQ49 165 DQ49
M_B_DQ50 175 DQ50
M_B_DQ51 177 DQ51
M_B_DQ52 164 DQ52
M_B_DQ53 166 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 181 DQ56
M_B_DQ57 183 DQ57
M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

M_B_DQS#0 10 DQS0#
M_B_DQS#1 27 DQS1#
M_B_DQS#2 45 DQS2#
M_B_DQS#3 62 DQS3#
M_B_DQS#4 135 DQS4#
M_B_DQS#5 152 DQS5#
M_B_DQS#6 169 DQS6#
M_B_DQS#7 186 DQS7#

M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

[10] M_ODT2 M_ODT2 116 ODT0
[10] M_ODT3 M_ODT3 120 ODT1

126 VREF_CA
1 VREF_DQ

[9,18] DDR3_DRAMRST# 30 RESET#

203 VTT1
204 VTT2

NP1 NP1
NP2 NP2

RAS# 110 M_B_RAS# [10]
WE# 113 M_B_WE# [10]
CAS# 115 M_B_CAS# [10]

CS0# 114 M_CS2# [10]
CS1# 121 M_CS3# [10]

CKE0 73 M_CKE2 [10]
CKE1 74 M_CKE3 [10]

CK0 101 M_CLK_DDR2 M_CLK_DDR2 [10]
CK0# 103 M_CLK_DDR#2 M_CLK_DDR#2 [10]

CK1 102 M_CLK_DDR3 M_CLK_DDR3 [10]
CK1# 104 M_CLK_DDR#3 M_CLK_DDR#3 [10]

DM0 11 M_B_DM0
DM1 28 M_B_DM1
DM2 46 M_B_DM2
DM3 63 M_B_DM3
DM4 136 M_B_DM4
DM5 153 M_B_DM5
DM6 170 M_B_DM6
DM7 187 M_B_DM7

SDA 200 PCH_SMBDATA PCH_SMBDATA [7,18,23,40,64,76]
SCL 202 PCH_SMBCLK PCH_SMBCLK [7,18,23,40,64,76]

EVENT# 198 PM_EXTTS#1 [9]

VDDSPD 199

SA0 197 SA0_DM2
SA1 201 SA1_DM2

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206

Height 9.2mm

DDR3-204P-24-GP

+1.5V_SUS

+3.3V_RUN

R1903 10KR2J-3-GP DY
R1904 10KR2J-3-GP
EC1901 SCD1U25V3KX-GP DY
SA1_DM2
SA0_DM2
R1901 10KR2J-3-GP
R1902 10KR2J-3-GP DY

SMBUS address:A4

C1906 SCD1U10V2KX-5GP DY
C1921 SC2D2U6D3V3KX-GP DY

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

Layout Note:
Place near DM2

+1.5V_SUS
C1905 SC10U6D3V5KX-1GP
C1911 SC10U6D3V5KX-1GP
C1913 SC10U6D3V5KX-1GP
C1916 SC1U6D3V5MX-3GP
C1919 SC10U6D3V5KX-1GP
C1920 SC10U6D3V5KX-1GP
TC1903 ST330U2D5VBM-1-GP DY

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT
C1908 SC1U6D3V2KX-GP
C1917 SC1U6D3V2KX-GP
C1918 SC1U6D3V2KX-GP DY
C1909 SC1U6D3V2KX-GP DY

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

+1.5V_SUS
C1976 SCD1U10V2KX-4GP
C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

+V_DDR_REF
C1907 SCD1U10V2KX-5GP
C1910 SCD1U10V2KX-5GP
C1914 SC2D2U6D3V3KX-GP DY

+0.75V_DDR_VTT

put near connector
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
C1901 DUMMY-C2
C1904 DUMMY-C2
C1902 DUMMY-C2
C1903 DUMMY-C2

1st Samsung

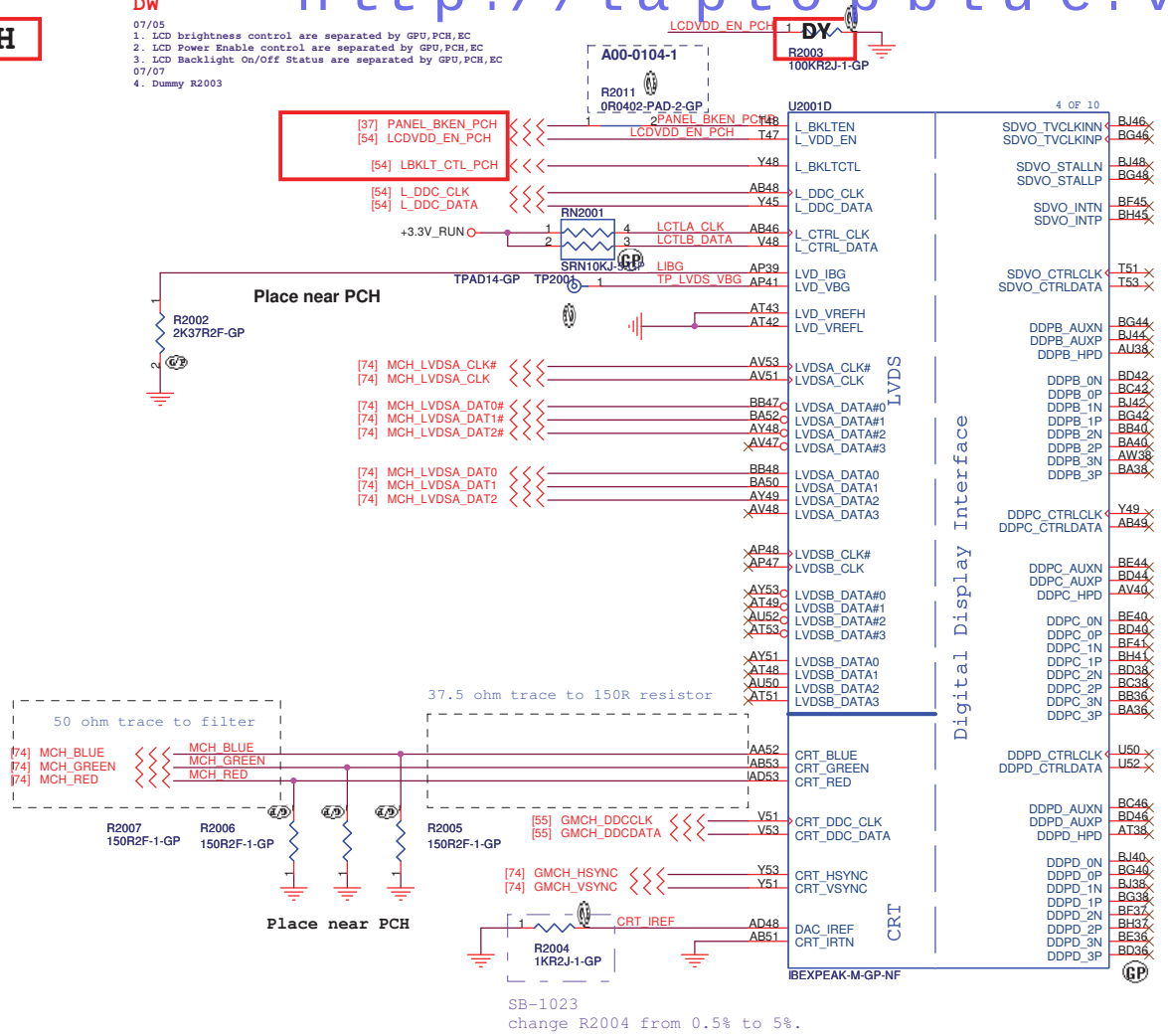
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT2
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 19 of 88

SSID = PCH

DW

07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/07
4. Dummy R2003




SB-1023
change R2004 from 0.5% to 5%.

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

| Size | Document Number | Rev |
|---|---|---|
| | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 20 of 88

SSID = PCH

RN2101 SRN8K2J-2-GP-U
PCI_DEVSEL# PCI_IRDY# PCI_SERR# INT_PIRQC#
DGPU_SELECT# INT_PIRQD# PCI_STOP# INT_PIRQA#
+3.3V_RUN

RN2102 SRN8K2J-2-GP-U
PCI_PERR# PCI_REQ0# PCI_REQ3# PCI_FRAME#
INT_PIRQB# PCI_PLOCK# PCI_REQ1# PCI_TRDY#
+3.3V_RUN

RN2103 SRN10KJ-7GP
DGPU_PWM_SELECT# EDID_SELECT_R# PCH_GPIO4 INT_PIRQE#
+3.3V_RUN

DW
07/02 Added
1. using the single buffers for 4 device with equivalent capability.
2.Rename PCI_PLTRST#

SB-1022
DY U2101; POP R2104
C2101 SCD1U10V2KX-4GP
U2101 74LVC1G08GW-1-GP
[9,34,36,37,64,70,76,80] PLT_RST#
PLTRST# PCH
R2104 0R2J-2-GP

SB-1022
DY U2102; POP R2105
U2102 74LVC1G08GW-1-GP
[54,55] EDID_SELECT#
EDID_SELECT_R#
R2105 0R2J-2-GP
C2112 SC220P50V2KX-3GP

| BOOT BIOS Strap | | |
|---|---|---|
| PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | PCI |
| 1 | 1 | SPI(Default) |

| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

R2109 4K7R2J-2-GP
PCI_GNT3#

U200E IBEXPEAK-M-GP-NF

PCI:
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
C/BE0# C/BE1# C/BE2# C/BE3#
INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD# → PIRQA# PIRQB# PIRQC# PIRQD#
PCI_REQ0# PCI_REQ1# DGPU_SELECT# PCI_REQ3# → REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54
[37,54,74] DGPU_SELECT#
PCI_GNT0# → GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55
TPAD14-GPTP2116
DGPU_PWM_SELECT# PCI_GNT3#
[54] DGPU_PWM_SELECT#
R2121 0R2J-2-GP
[40] HDD_FALL_INT1
[76] WWAN_RF_EN
INT_PIRQE# WWAN_RF_EN PCH_GPIO4 EDID_SELECT_R# → PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
TPAD14-GPTP2108
PCIRST# → PCIRST#
PCI_SERR# PCI_PERR# → SERR# PERR#
PCI_IRDY# PCI_DEVSEL# PCI_FRAME# → IRDY# PAR DEVSEL# FRAME#
PCI_PLOCK# → PLOCK#
PCI_STOP# PCI_TRDY# → STOP# TRDY#
TPAD14-GPTP2115
PCH_PME# → PME#
PLTRST# PCH → PLTRST#
[70] PCLK_FWH
[23] CLK_PCI_FB
[37] PCLK_KBC
[36] PCLK_TPM
R2110 R2108 R2111 R2112 22R2J-2-GP
PCLK_FWH_R CLK_PCI_FB_R PCLK_KBC_R PCLK_TPM_R → CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

NVRAM:
NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0/NV_IO0 NV_DQ1/NV_IO1 NV_DQ2/NV_IO2 NV_DQ3/NV_IO3 NV_DQ4/NV_IO4 NV_DQ5/NV_IO5 NV_DQ6/NV_IO6 NV_DQ7/NV_IO7 NV_DQ8/NV_IO8 NV_DQ9/NV_IO9 NV_DQ10/NV_IO10 NV_DQ11/NV_IO11 NV_DQ12/NV_IO12 NV_DQ13/NV_IO13 NV_DQ14/NV_IO14 NV_DQ15/NV_IO15
NV_ALE NV_CLE
TP_NV_ALE TP_NV_CLE
TP2124 TPAD14-GP TP2125 TPAD14-GP
NV_RCOMP
TP_NV_RCOMP
TP2130 TPAD14-GP
NV_RB#
NV_WR#0_RE# NV_WR#1_RE#
NV_WE#_CK0 NV_WE#_CK1

| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vss when low.<br>Set to Vcc when high.<br>Low = Default |

unused NV_SLE strap

USB:
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
USBRBIAS# USBRBIAS
R2106 22D6R2F-L1-GP
USB_RBIAS_PN
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14
USB_OC#0_1 USB_OC#2_3 USB_OC#4_5 USB_OC#6_7 USB_OC#8_9 USB_OC#10_11 USB_OC#12_13 PCH_OC7#

Port 0 for debug port
USB_PN0 [63] USB_PP0 [63] USB_PN1 [63] USB_PP1 [63] USB_PN2 [76] USB_PP2 [76] TP2122 TP2123 USB_PN4 [64] USB_PP4 [64] USB_PN5 [76] USB_PP5 [76] TP2118 TP2119 TP2120 TP2121 USB_PN8 [73] USB_PP8 [73] USB_PN9 [32] USB_PP9 [32] USB_PN10 [78] USB_PP10 [78] USB_PN11 [73] USB_PP11 [73] USB_PN12 [34] USB_PP12 [34] TP2128 TP2129
TP_USB_PN3 TP_USB_PP3 TP_USB_PN6 TP_USB_PP6 TP_USB_PN7 TP_USB_PP7 TP_USB_PN13 TP_USB_PP13

| USB | |
|---|---|
| Pair | Device |
| 0 | USB1 |
| 1 | USB for ESATA |
| 2 | USB2 |
| 3 | RESERVE |
| 4 | WLAN |
| 5 | WWAN |
| 6 | RESERVED (Not available for HM55) |
| 7 | RESERVED (Not available for HM55) |
| 8 | BlUETOOTH |
| 9 | Card Reader |
| 10 | Biometric |
| 11 | CAMERA |
| 12 | New Card |
| 13 | RESERVED |

USB_OC#0_1 [22,63] USB_OC#2_3 [76]
Pull up in page 22 for layout convenience
SB swap net for layout
Pull up in page 23 for layout convenience

RP2101 SRN10KJ-L3-GP
PCH_OC7# USB_OC#2_3 USB_OC#6_7 USB_OC#4_5
PM_RI# USB_OC#8_9 PEG_B_CLKRQ# USB_OC#10_11
+3.3V_ALW
PM_RI# [22] PEG_B_CLKRQ# [23]
SB swap net for layout

Calpella Platform Design Guide
Revision 1.6

**Table 111. Overcurrent Pin Example Configuration**

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Winery13 MB DIS Rev: A00
Date: Wednesday, January 13, 2010 Sheet 21 of 88

SSID = PCH

U2001C

3 OF 10

DMI

FDI

System Power Management

IBEXPEAK-M-GP-NF

Remove XDP pull-up ?

Option to " Disable " clkrun.
Pulling it down will keep the clks running.

Close to PCH

Pull up in page 23 for layout convenience

SB-31



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 22 of 88

**SSID = PCH**

U2001B — 2 OF 10 — IBEXPEAK-M-GP-NF

PCI-E* Controller Link

PERN1 PERP1 PETN1 PETP1 — WLAN
PERN2 PERP2 PETN2 PETP2 — LAN
PERN3 PERP3 PETN3 PETP3 — WWAN
PERN4 PERP4 PETN4 PETP4 — New Card
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

SMBus

SMBALERT#/GPIO11
SMBCLK — PCH_SMB_CLK [34]
SMBDATA — PCH_SMB_DATA [34]
SML0ALERT#/GPIO60
SML0CLK — SML0_CLK
SML0DATA — SML0_DATA
SML1ALERT#/GPIO74
SML1CLK/GPIO58 — KBC_SCL1 [37]
SML1DATA/GPIO75 — KBC_SDA1 [37]

Remove XDP pull-up

SB-1020

CL_CLK1 — TP2301 TPAD14-GP
CL_DATA1 — TP2302 TPAD14-GP
CL_RST1# — TP2303 TPAD14-GP
+3.3V_ALW — R2304 10KR2J-3-GP

PEG_A_CLKRQ#/GPIO47 — PEG_CLKREQ#

PEG

CLKOUT_PEG_A_N/P — CLK_PCIE_VGA# [80] / CLK_PCIE_VGA [80]
RN2327 0R4P2R-PAD — A00-0104-1
CLKOUT_DMI_N/P — CLK_EXP_N [9] / CLK_EXP_P [9]
CLKOUT_DP_N/CLKOUT_BCLK1_N
CLKOUT_DP_P/CLKOUT_BCLK1_P

From CLK BUFFER

CLKIN_DMI_N/P — CLKIN_DMI# [7] / CLKIN_DMI [7]
CLKIN_BCLK_N/P — CLK_CPU_BCLK# [7] / CLK_CPU_BCLK [7]
CLKIN_DOT_96N/P — DREFCLK# [7] / DREFCLK [7]
CLKIN_SATA_N/CKSSCD_N/P — CLK_PCIE_SATA# [7] / CLK_PCIE_SATA [7]
REFCLK14IN — CLK_PCH_14M [7]
CLKIN_PCILOOPBACK — CLK_PCI_FB [21]
XTAL25_IN / XTAL25_OUT
XCLK_RCOMP — R2306 90D9R2F-1-GP — +1.05V_VTT

Clock Flex

CLKOUTFLEX0/GPIO64 — TP_CLK_OUTFLEX0 — TP2307 TPAD14-GP
CLKOUTFLEX1/GPIO65 — TP_CLK_PCI_LPC — TP2305 TPAD14-GP
CLKOUTFLEX2/GPIO66 — TP_CLK_PCH_REF14 — TP2306 TPAD14-GP
CLKOUTFLEX3/GPIO67 — CLK48M/EDID_SEL — R2307 0R0402-PAD-2-GP — CLK_PCH_48M [32]

CLKOUT_PCIE0N/P
CLKOUT_PCIE1N/P
CLKOUT_PCIE2N/P
CLKOUT_PCIE3N/P
CLKOUT_PCIE4N/P
CLKOUT_PCIE5N/P
CLKOUT_PEG_B_N/P

PCIECLKRQ0/GPIO73
PCIECLKRQ1/GPIO18
PCIECLKRQ2/GPIO20
PCIECLKRQ3/GPIO25
PCIECLKRQ4/GPIO26
PCIECLKRQ5/GPIO44
PEG_B_CLKRQ#/GPIO56

**PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.**
**PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN**

A00-0104-1

RN2311 0R4P2R-PAD — CLK_PCIE_NEW1# / CLK_PCIE_NEW1 — [34] CLK_PCIE_NEW# / [34] CLK_PCIE_NEW
NEWCARD_CLKREQ# — [34] NEWCARD_CLKREQ#
RN2305 0R4P2R-PAD — CLK_PCIE_MINI1_1# / CLK_PCIE_MINI1_1 — [64] CLK_PCIE_MINI1# / [64] CLK_PCIE_MINI1
MINI1_CLKREQ# — [64] MINI1_CLKREQ#
RN2304 0R4P2R-PAD — CLK_PCIE_LAN1# / CLK_PCIE_LAN1 — [76] CLK_PCIE_LAN# / [76] CLK_PCIE_LAN
CLKREQ#_LAN — [76] CLKREQ#_LAN
RN2309 0R4P2R-PAD — CLK_PCIE_MINI2_1# / CLK_PCIE_MINI2_1 — [76] CLK_PCIE_MINI2# / [76] CLK_PCIE_MINI2
MINI2_CLKREQ# — [21] PEG_B_CLKRQ#

Pull up in page 21 for layout convenience

+3.3V_RUN — R2333 10KR2J-3-GP — Q2306_1
Q2306 MMBT3904-7-F-GP — [76] MINI2_CLKREQ_R#
1ST: 84.03904.H11
2ND: 84.03904.L06
R2 — DY — 0R2J-2-GP

+3.3V_ALW — RN2307 SRN10KJ-7GP
PCIECLKRQ5# — USB_OC#12_13 — [21] USB_OC#12_13
CLKREQ#_LAN
MINI2_CLKREQ#

SB
swap net for layout

+3.3V_RUN — RN2308 SRN10KJ-6-GP
NEWCARD_CLKREQ#
KB_DET_R#
GPO_DSM — KB_DET_R# [25] / GPO_DSM [24,76]
MINI1_CLKREQ#

SB-1026
swap net for layout

SB-1023
RN2308 change to 2*1 size

SB-1020
move EDID_SELECT# from GPIO66 to GPIO5

SB-1020

+3.3V_ALW — RN2313 SRN2K2J-1-GP
+3.3V_ALW — RN2302 SRN2K2J-1-GP
PCH_SMB_CLK
PCH_SMB_DATA

+3.3V_RUN — RN2303 SRN2K2J-1-GP
PCH_SMB_DATA — PCH_SMBDATA [7,18,19,40,64,76]
Q2301 DMN66D0LDW-7-GP
1ST: 84.DMN66.03F
2ND: 84.27002.F3F
PCH_SMB_CLK — PCH_SMBCLK [7,18,19,40,64,76]

PEG_CLKREQ#
[25,51] DGPU_1D8V_PGOOD
Q2305 2N7002A-7-GP
1ST: 84.2N702.E31
2ND: 84.2N702.D31

un-stuff 25M X'tal without HDMI/eDP/DP

SC-1125-1
C2313 pop 0 ohm if no use 25MHz XTAL
XTAL25_IN — C2313 0R2J-2-GP
R2380 1MR2J-1-GP — DY
X2301 XTAL25MHZ-67GP — DY
XTAL25_OUT — DY
SB-1104
pop for 25MHz
C2307 SC18P50V2JN-1-GP

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: Document Number: Winery13 MB DIS — Rev: A00
Date: Wednesday, January 13, 2010 — Sheet 23 of 88

SSID = PCH

PCH_RTCX1 — R2401 10MR2J-L-GP — PCH_RTCX2
X2401 X-32D768KHZ-46GP
C2402 SC12P50V2JN-3GP
C2403 SC12P50V2JN-3GP
SB-18

+RTC_CELL — R2402 20KR2J-L-GP — C2401 SC1U6D3V3KX-2GP
+RTC_CELL — R2403 20KR2J-L-GP — C2404 SC1U6D3V3KX-2GP
G2401 GAP-OPEN

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

1st: EPSON 82.30001.861
2nd: QUARTECH 82.30001.A81
3rd: KDS 82.30001.691

DW
07/23 Added
1.Added "ME in Manufacturing Mode" strap
2.Added CardReader_Wake# to sent Card detect signal for PCH . ( Only For JMB380 )

| Flash Descriptor Security Override/ ME Debug Mode | |
|---|---|
| ME_UNLOCK# | This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY. |

DY R2419 1KR2J-1-GP — ME_UNLOCK_R#

NO REBOOT STRAP
+3.3V_RUN — DY R2410 1KR2J-1-GP — SB_SPKR

| No Reboot Strap R23 | |
|---|---|
| HDA_SPKR | Low = Default<br>High = No Reboot |

SB-1026
1. remove R2411 pull high INT_SERIRQ to RN2501.1

DW
07/02 Change
1.Change R2410 to dummy

U2001A — 1 OF 10

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
R2406 1MR2J-1-GP — SM_INTRUDER#
R2404 330KR2F-L-GP — PCH_INTVRMEN

LPC: FWH0/LAD0 D33, FWH1/LAD1 B33, FWH2/LAD2 C32, FWH3/LAD3 A32, FWH4/LFRAME# C34, LDRQ0# A34, LDRQ1#/GPIO23 E34, SERIRQ AB9
LPC_LAD[0..3] [36,37,70] — LPC_LFRAME# [36,37,70] — INT_SERIRQ [25,36,37]

IHDA:
[30] PCH_AZ_CODEC_BITCLK — R2405 33R2J-2-GP — ACZ_BIT_CLK — HDA_BCLK A30
[30] PCH_AZ_CODEC_SYNC — R2407 33R2J-2-GP — ACZ_SYNC_R — HDA_SYNC D29
[30] SB_SPKR — SPKR P1
[30] PCH_AZ_CODEC_RST# — R2408 33R2J-2-GP — ACZ_RST#_R — HDA_RST# C30
[30] PCH_SDIN_CODEC — HDA_SDIN0 G30
HDA_SDIN1 F30
HDA_SDIN2 E32
HDA_SDIN3 F32
[30] PCH_SDOUT_CODEC — R2409 33R2J-2-GP — ACZ_SDATAOUT_R — HDA_SDO B29
[37] ME_UNLOCK# — R2417 0R0402-PAD-2-GP — ME_UNLOCK_R# — HDA_DOCK_EN#/GPIO33 H32
HDA_DOCK_RST#/GPIO13 J30
A00-0104-1

JTAG:
TP2404 PCH_JTAG_TCK — JTAG_TCK M3
TP2405 PCH_JTAG_TMS — JTAG_TMS K3
TP2406 PCH_JTAG_TDI — JTAG_TDI K1
TP2407 PCH_JTAG_TDO — JTAG_TDO J2
TP2408 PCH_JTAG_RST# — TRST# J4

SPI:
[62] PCH_SPI_CLK — R2413 0R2J-2-GP — SPI_CLK_R — SPI_CLK BA2
[62] PCH_SPI_CS0# — R2414 0R2J-2-GP — SPI_CS0_R — SPI_CS0# AV3
SPI_CS1# AY3
[62] PCH_SPI_DO — R2415 0R2J-2-GP — SPI_MOSI_R — SPI_MOSI AY1
[62] PCH_SPI_DI — SPI_MISO AV1
SC-1208-1
change R2413,R2414,R2415 from 15ohm to 0 ohm

SATA:
SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9 — SATA_ITXN0_HRXN0_C C2405 — SATA_ITXP0_HRXP0_C C2406 — SCD01U25V2KX-3GP
SATA_IRXN0_HTXN0_C [59], SATA_IRXP0_HTXP0_C [59], SATA_ITXN0_HRXN0 [59], SATA_ITXP0_HRXP0 [59]
HDD

SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8 — SATA_ITXN1_ORXN1_C C2407 — SATA_ITXP1_ORXP1_C C2408 — SCD01U25V2KX-3GP
SATA_IRXN1_OTXN1_C [59], SATA_IRXP1_OTXP1_C [59], SATA_ITXN1_ORXN1 [59], SATA_ITXP1_ORXP1 [59]
ODD

SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6
SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1

SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5
SATA_IRX_DTX_N4_C [63], SATA_IRX_DTX_P4_C [63], ESATA_ITX_DRX_N4 [63], ESATA_ITX_DRX_P4 [63]
ESATA

SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1

SATAICOMPO AF16, SATAICOMPI AF15 — SATAICOMP — R2412 37D4R2F-GP — +1.05V_VTT
SATALED# T3 — SATA_LED# [66]
SATA0GP/GPIO21 Y9 — GPO_DSM — GPO_DSM [23,76]
SATA1GP/GPIO19 V1 — PCH_GPIO19 — PCH_GPIO19 [25]

IBEXPEAK-M-GP-NF

DW
07/10 assign GPIO
1.assign GPIO GPIO_DSM,Felic_DETECT#

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Document Number: Winery13 MB DIS — Rev: A00
Date: Wednesday, January 13, 2010 — Sheet 24 of 88

SSID = PCH

U2001F

6 OF 10

BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

MISC
GPIO
CPU
NCTF
RSVD

CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROCPWRGD
THRMTRIP#
TP1 … TP24
NC_1 … NC_5
INIT3_3V#
VSS_NCTF_1 … VSS_NCTF_31

IBEXPEAK-M-GP-NF

DW
07/02 Change
1.Change CLK_SATA_OE# to pull-down

07/10 Added
1.Changed PCH GPIO DDR_RST_GATE from GPIO57 to GPIO46 , Bason on design guide
07/23 Added
1.Added Finger Printer Detect Pin, control by PCH
2.Change KB_DET signal from EC to PCH control
3.Change LCD_CBL_DET signal from EC to PCH control

For layout request

A00-0104-1

Placed Within 2" from PCH

SB-32
SB-1023
SB-1026
swap net for layout



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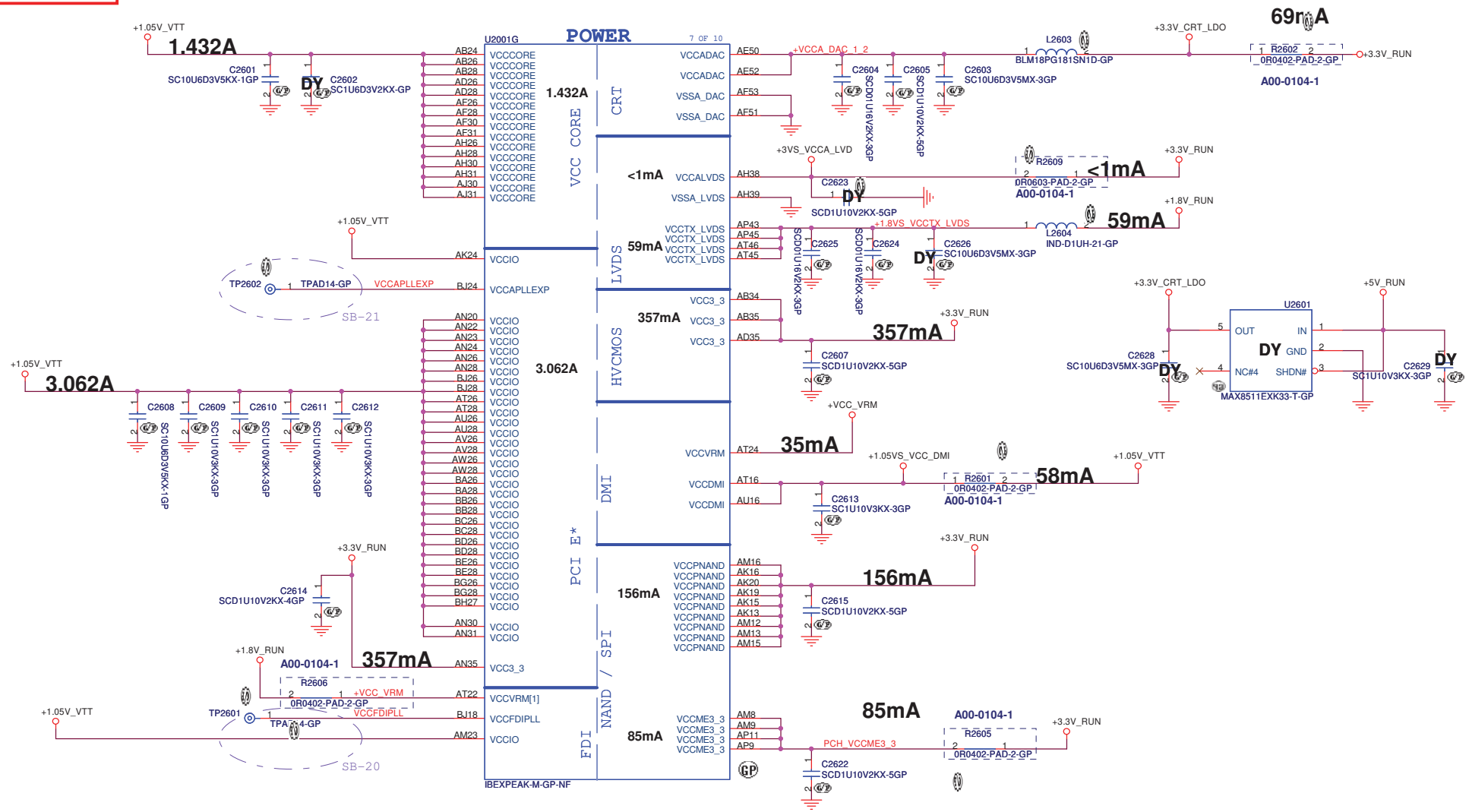
Title: PCH (GPIO/CPU)
Size:
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 25 of 88

SSID = PCH

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| Title | | |
|---|---|---|
| PCH (POWER1) | | |
| Size | Document Number | Rev |
| | Winery13 MB DIS | A00 |
| Date: Wednesday, January 13, 2010 | Sheet 26 of 88 | |

SSID = PCH

POWER

U2001J

SB-15

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK
52mA

AF23 VCCLAN
AF24 VCCLAN
320mA

DCPSUSBYP Y20 DCPSUSBYP
C2707 SCD1U10V2KX-4GP

AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
1.849A

+1.05V_VTT
C2705 SC10U6D3V5KX-1GP
C2708 SC1U6D3V2KX-GP DY
C2704 SC10U6D3V5KX-1GP
C2710 SC1U6D3V2KX-GP DY

SB-17

+1.05V_VTT
L2702 IND-10UH-218-GP
+1.05VS_VCCA_A_DPL
C2734 SC10U6D3V5MX-3GP DY
C2711 SC1U6D3V2KX-GP
L2703 IND-10UH-218-GP
+1.05VS_VCCA_B_DPL
C2735 SC10U6D3V5MX-3GP DY
C2714 SC1U6D3V2KX-GP

+VCCRTCEXT V9 DCPRTC
C2713 SCD1U10V2KX-4GP
+VCC_VRM
AU24 VCCVRM

68mA +1.05VS_VCCA_A_DPL
BB51 VCCADPLLA
BB53 VCCADPLLA
68mA

69mA +1.05VS_VCCA_B_DPL
BD51 VCCADPLLB
BD53 VCCADPLLB
69mA

+1.05V_VTT
C2718 SC1U6D3V2KX-GP
C2719 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO

+VCCSST V12 DCPSST
C2723 SCD1U10V2KX-4GP
+1.05VALW_INT_VCCSUS Y22 DCPSUS
C2724 SCD1U10V2KX-4GP

P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
163mA
+3.3V_ALW
C2726 SCD1U10V2KX-4GP

+3.3V_RUN
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
C2727 SCD1U10V2KX-4GP

+1.05V_VTT
<1mA
C2728 SC10U6D3V5KX-1GP
C2729 SCD1U16V2KX-3GP
C2730 SCD1U16V2KX-3GP
AT18 V_CPU_IO
AU18 V_CPU_IO
<1mA

+RTC_CELL
2mA
A12 VCCRTC 2mA
C2732 SCD1U10V2KX-4GP
C2733 SCD1U10V2KX-4GP
IBEXPEAK-M-GP-NF

USB
163mA
1.849A
Clock and Miscellaneous
PCI/GPIO/LPC
<1mA
V5REF_SUS
<1mA
V5REF
68mA
69mA
PCI/GPIO/LPC
SATA
196mA
CPU
<1mA
RTC
2mA
HDA
6mA

VCCIO V24
VCCIO V26
VCCIO Y24
VCCIO Y26
+1.05V_VTT
C2706 SC1U10V2KX-1GP DY

VCCSUS3_3 V28
VCCSUS3_3 U28
VCCSUS3_3 U26
VCCSUS3_3 U24
VCCSUS3_3 P28
VCCSUS3_3 P26
VCCSUS3_3 N28
VCCSUS3_3 N26
VCCSUS3_3 M28
VCCSUS3_3 M26
VCCSUS3_3 L28
VCCSUS3_3 L26
VCCSUS3_3 J28
VCCSUS3_3 J26
VCCSUS3_3 H28
VCCSUS3_3 H26
VCCSUS3_3 G28
VCCSUS3_3 G26
VCCSUS3_3 F28
VCCSUS3_3 F26
VCCSUS3_3 E28
VCCSUS3_3 E26
VCCSUS3_3 C28
VCCSUS3_3 C26
VCCSUS3_3 B27
VCCSUS3_3 A28
VCCSUS3_3 A26
+3.3V_ALW
C2703 SCD1U10V2KX-4GP

VCCSUS3_3 U23
VCCIO V23
+1.05V_VTT
C2709 SCD1U10V2KX-4GP
+3.3V_ALW

+5VALW_PCH_VCC5REFSUS F24
+3.3V_ALW
D2701 CH751H-40PT-GP
+5V_ALW
R2701 100R2J-2-GP
C2712 SC1U6D3V2KX-GP

DW
07/10 Change resistor Value
1.R2701,R2702 value corrected to 100 Ohms following PDG doc

+5VS_PCH_VCC5REF K49 V5REF
+3.3V_RUN
D2702 CH751H-40PT-GP
+5V_RUN
R2702 100R2J-2-GP
C2715 SC1U6D3V2KX-GP

VCC3_3 J38
VCC3_3 L38
VCC3_3 M36
VCC3_3 N36
VCC3_3 P36
VCC3_3 U35
+3.3V_RUN
C2716 SCD1U10V2KX-4GP

VCC3_3 AD13
+3.3V_RUN
C2717 SCD1U10V2KX-4GP

VCCSATAPLL AK3
VCCSATAPLL AK1
VCCSATAPLL
TP2702 TPAD14-GP
SB-16

VCCIO AH22
VCCVRM AT20
+VCC_VRM
C2725 SC1U6D3V2KX-GP
+1.05V_VTT

VCCIO AH19
VCCIO AD20
VCCIO AF22
VCCIO AD19
VCCIO AF20
VCCIO AF19
VCCIO AH20
VCCIO AB19
VCCIO AB20
VCCIO AB22
VCCIO AD22

VCCME AA34
VCCME Y34
VCCME Y35
VCCME AA35
+1.05V_VTT

VCCSUSHDA L30
6mA
R2707 0R0402-PAD-2-GP
A00-0104-1
+3.3V_ALW
C2731 SC1U6D3V2KX-GP
+3VS_+1.5VS_HDA_IO

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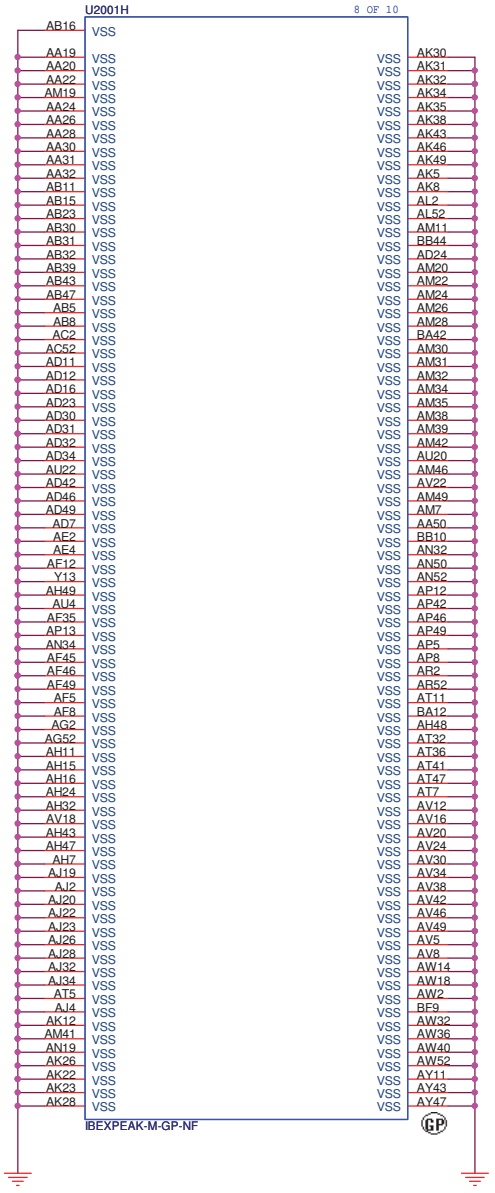
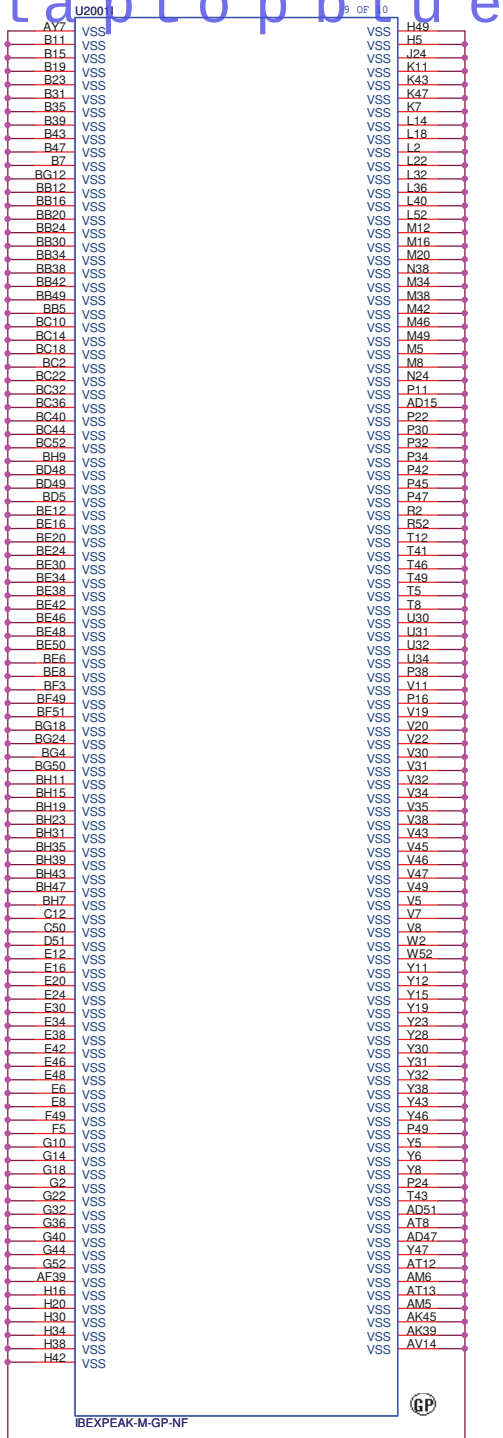
Title: PCH (POWER2)
Size:
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 27 of 88

SSID = PCH

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| Title | | |
|---|---|---|
| PCH (VSS) | | |
| Size | Document Number | Rev |
| | Winery13 MB DIS | A00 |
| Date: Wednesday, January 13, 2010 | Sheet 28 of 88 | |

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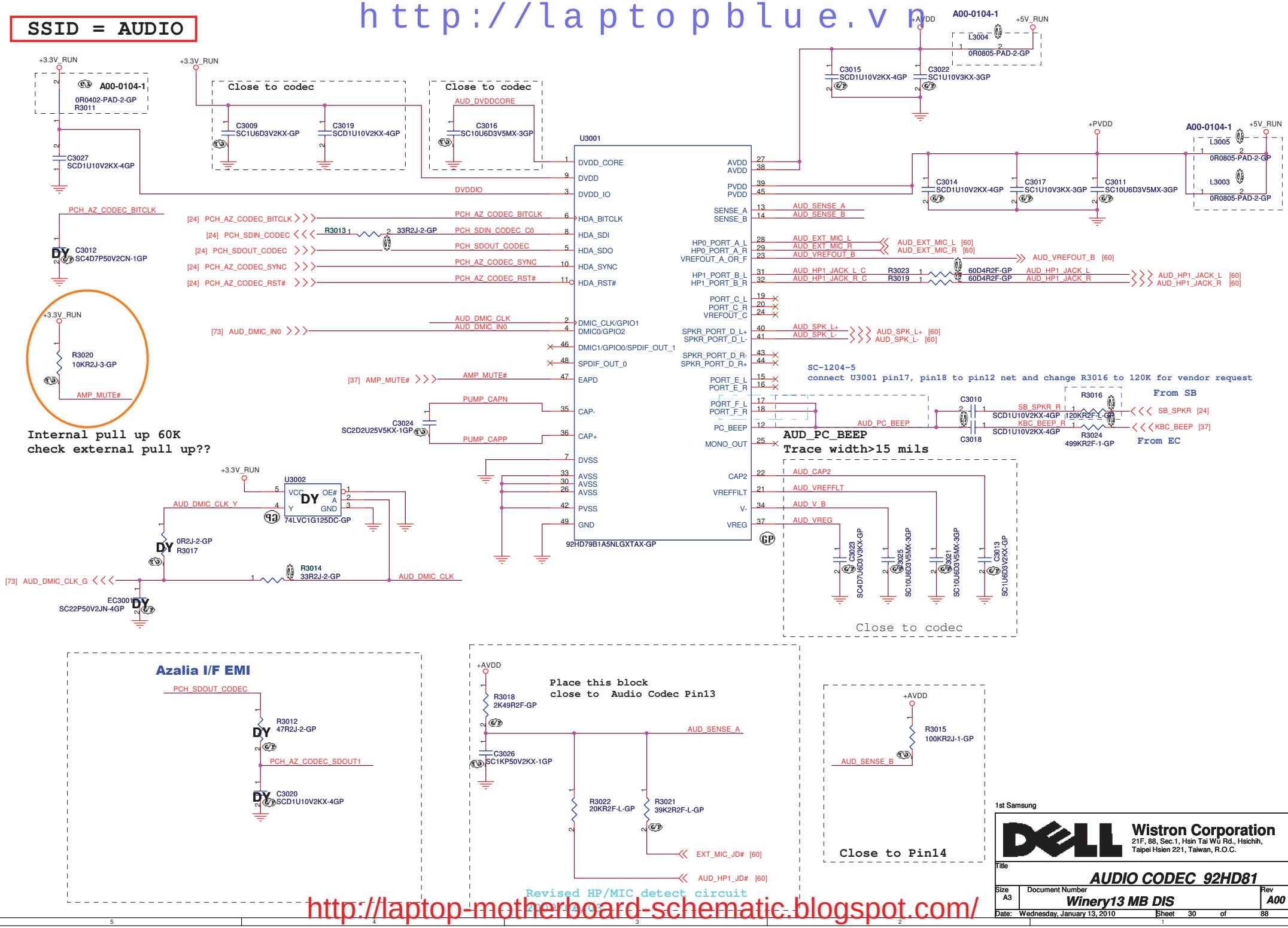
Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 29 of 88

# SSID = AUDIO



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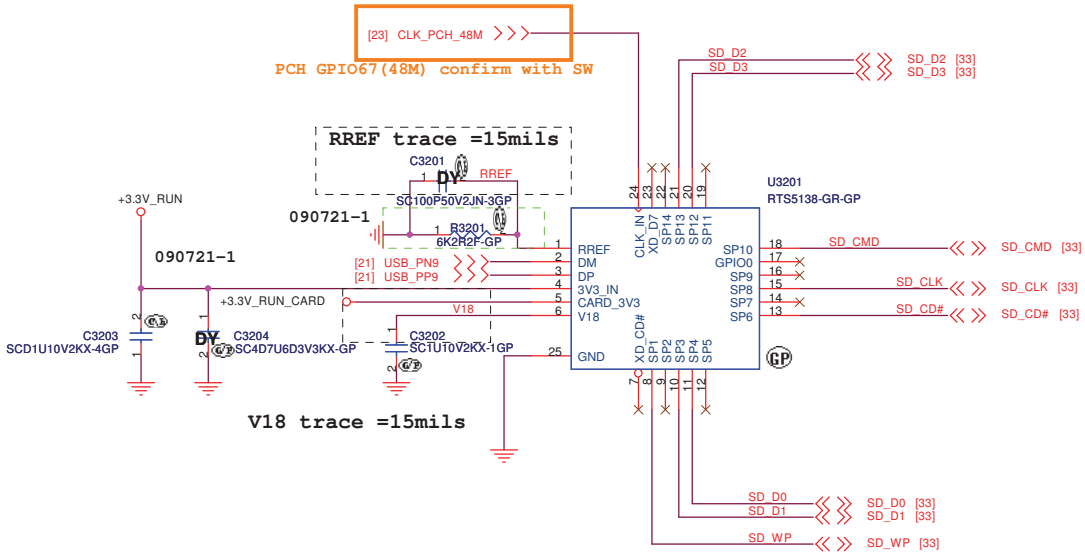
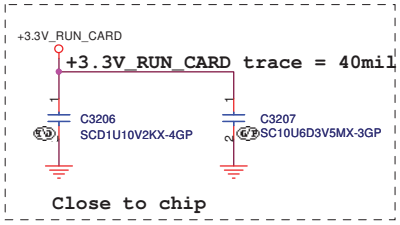
Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 31 of 88

**SSID = SDIO**

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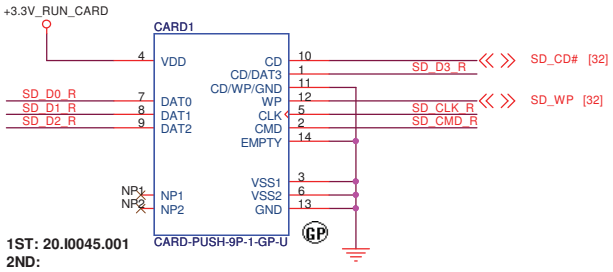
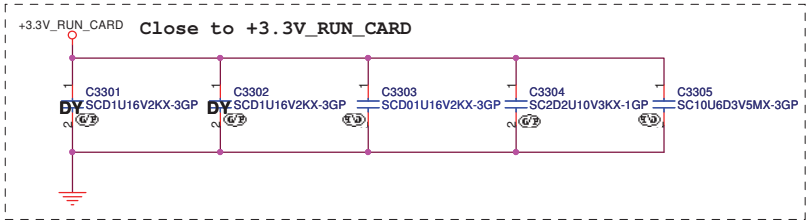
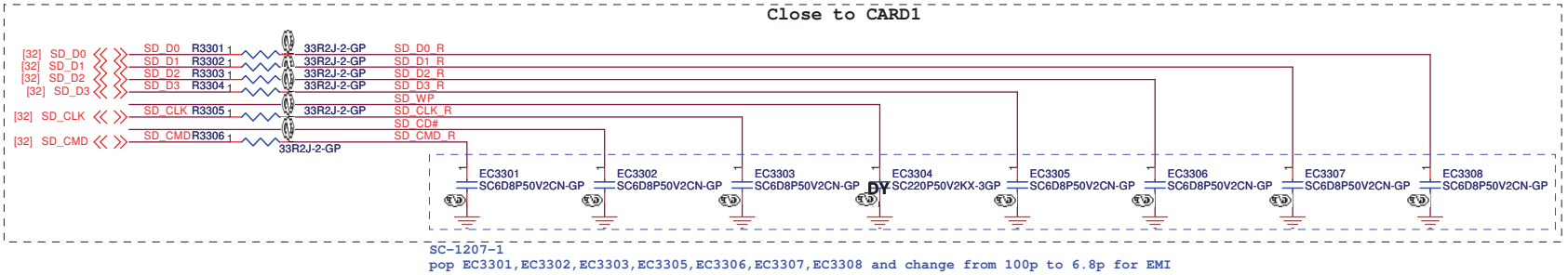
| | | |
|---|---|---|
| Title | CardReader/RTS5138 | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 32 of 88 | |

SSID = SDIO

# SD/MMC/MMC+ Card Reader




SSID = 1394

Remove 1394

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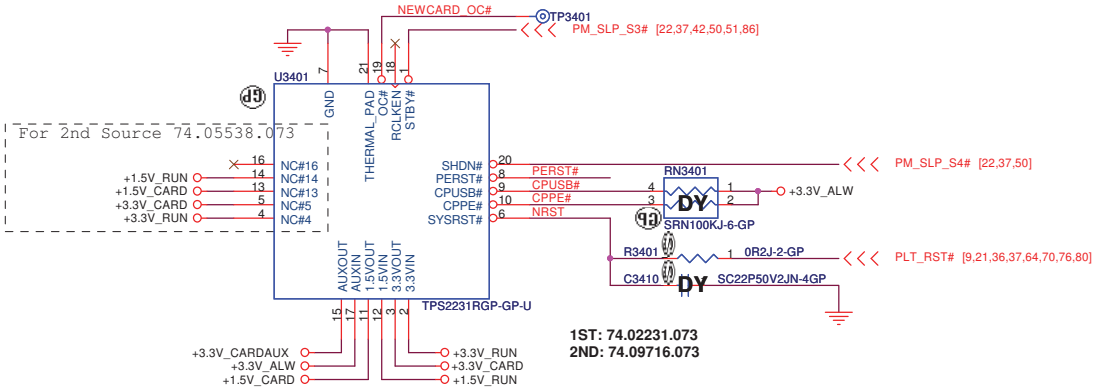
Title: CARD READER CONN

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 33 of 88

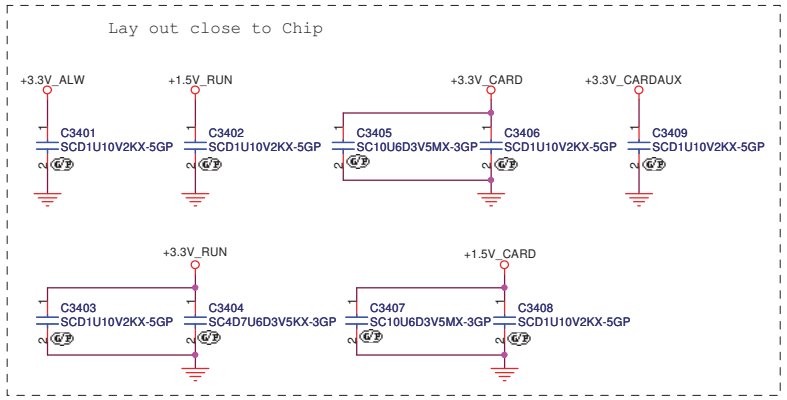
**SSID = ExpressCard**

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

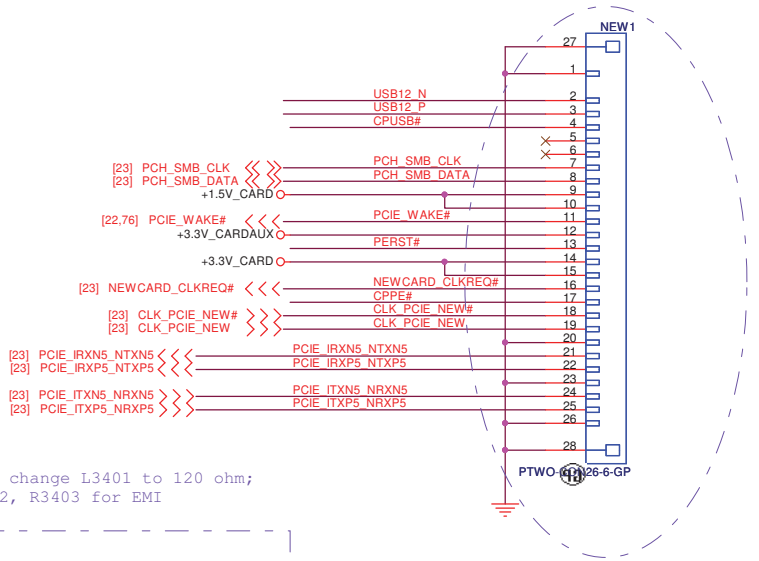



1ST: 74.02231.073
2ND: 74.09716.073

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

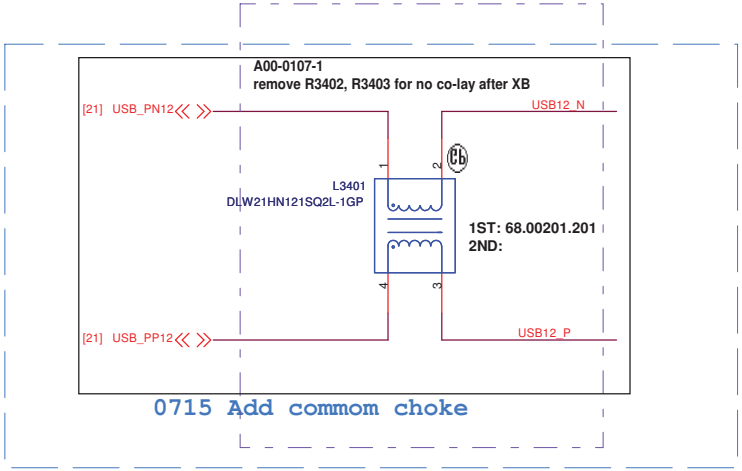



SB-26




1ST: 20.K0370.026
2ND: 20.K0315.026

SB-1021
pop and change L3401 to 120 ohm;
DY R3402, R3403 for EMI

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Title: ExpressCard
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 34 of 88

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Title: *(Reserve)*

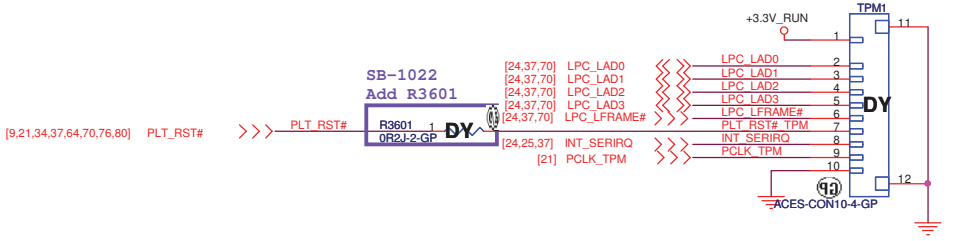
Size: A3 | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 35 of 88

SSID = User.Interface



## TPM board CONN




SC-1125-1
remove TPM AFTP

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| | | |
|---|---|---|
| Title: TPM | | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 36 of 88 | |

SSID = KBC

Put 0.1uf close to VCC-GND pin pair.

| MB VERSION | | |
|---|---|---|
| ID | VER1 | VER0 |
| SA | 0 | 0 |
| SB | 0 | 1 |
| SC | 1 | 0 |
| -1 | 1 | 1 |

KBC CLK EMI

Pull High : Discrete
internal Pull Low for UMA

Pull High : Switch Board
Pull Low : UnSwitch Board

SC-1118-1
change power rail to KBC_PWR

SC-1125-2
add U3703 mux for panel backlight enable signal select

C3710 need place near pin 44.

Add reset IC U3704 to prevent SPI ROM data lost

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Title: KBC Nuvoton NPCE781BA0DX
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 37 of 88

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Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 38 of 88

**SSID = Thermal**

+5V_RUN
25mil
C3910 SC4D7U6D3V5KX-3GP
C3909 SCD1U10V2KX-5GP
+3.3V_RUN
R3907 10KR2J-3-GP
SB-1023
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 [58]
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE [58]
25mil
RN3901 SRN4K7J-8-GP
THERM_SCL [37,78]
THERM_SDA [37,78]

DW
07/10 Del
1. Not reserve S5 power source rail for EMC2102 ??

1. WWAN
1ST: 84.03904.P11
2ND: 84.03904.T11
Q3905 must be near WWAN
C3912 must be near Q3905
CH3904PT-GP Q3905
C3912 SC470P50V2JN-GP
C3914 SC470P50V2JN-GP
C3914 must be near EMC2102

Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. GPU Sensor
[81] VGA_THERMDC
[81] VGA_THERMDA
C3906 SC470P50V2JN-GP
C3906 must be near EMC2102

DW
07/23 Removed
1.Removed SYSTEM Sensor Critical

3. CPU Sensor
Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.
C3901 must be near Q3901
CH3904PT-GP Q3901
C3901 SC470P50V2JN-GP
C3903 SC470P50V2JN-GP
C3903 must be near EMC2102
1ST: 84.03904.P11
2ND: 84.03904.T11
3.HW T8 sensor ( CPU )

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

+3.3V_RUN
R3908 49D9R2F-GP
EMC2102_VDD_3D3
C3905 SCD1U16V2KX-3GP

U3901 EMC2102
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102_DN1
EMC2102_DP1
VGA_THERMDC
VGA_THERMDA
T8_THERMDC
T8_THERMDA
TP_ALERT# TP3903 TPAD14-GP
CLK_32K
EMC2102_CLK_SEL
R3906 10KR2J-3-GP
TP_EM2102_RESET# TP3904 TPAD14-GP
EMC2102-DZK-GP
1ST: 74.02102.A73
2ND: 74.07922.0B3

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
R3903 10KR2J-3-GP
EMC2102_SHDN
R3916 0R2J-2-GP
EMC2102_FAN_mode
R3914 10KR2J-3-GP

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

EMC2102_PWROK
EMC2102_THERMTRIP#
RN3902 SRN10KJ-5-GP
KBC_PWR
R3910 10KR2J-3-GP
R3917 10KR2J-3-GP
Q3903 2N7002A-7-GP
SYS_SHDN#
SHDN
PURE_HW_SHUTDOWN# [37,42]
V_DEGREE
1ST: 84.2N702.E31
2ND: 84.2N702.D31

C3902 SCD1U10V2KX-5GP
R3902 10KR2F-2-GP
C3904 SCD1U10V2KX-5GP
R3904 2K37R2F-GP
TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 86 deg-C.
SC-1204-1

DW
07/28 Removed
1. Removed U3902 AND gate.

*32K suspend clock output*
1ST: 84.2N702.E31
2ND: 84.2N702.D31
Q3902 2N7002A-7-GP
[22] PCH_SUSCLK_2102
CLK_32K_R
R3913 10R2J-2-GP
CLK_32K
C3911 SC4D7P50V2CN-1GP
RUN_POWER_ON [42,52]



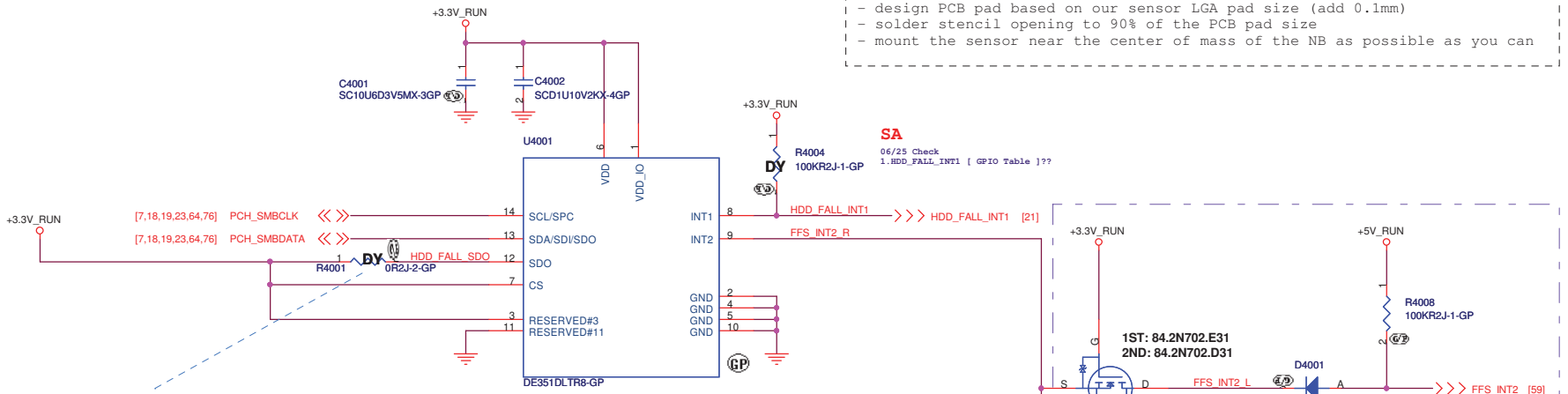
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 39 of 88

# Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can




09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 40 of 88

(Blank)

1st Samsung

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

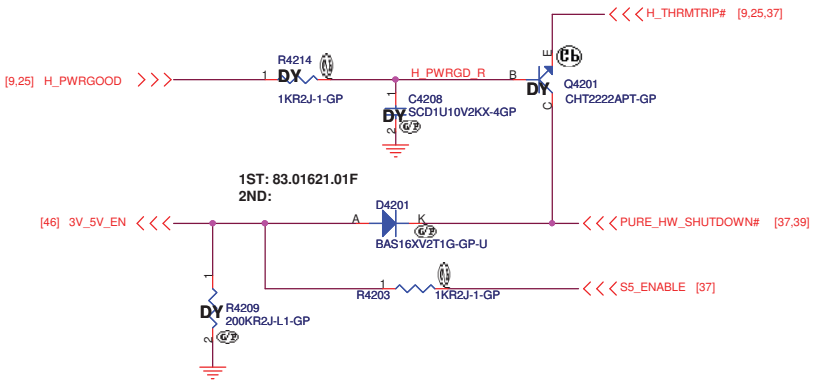
Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

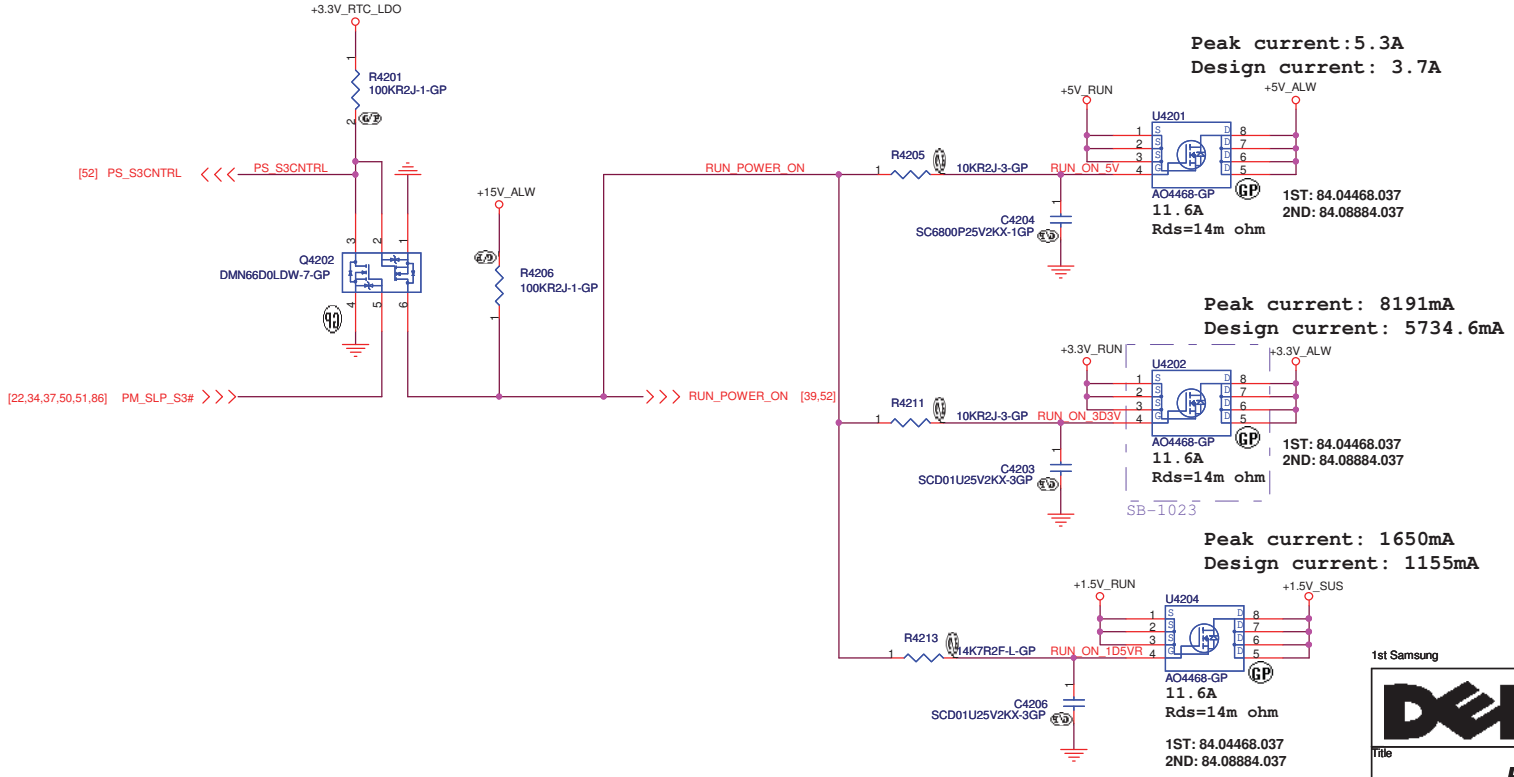
Date: Wednesday, January 13, 2010 | Sheet 41 of 88

SSID = Reset.Suspend



Remove +3.3V_DELAY power rail 2009/05/25




1st Samsung

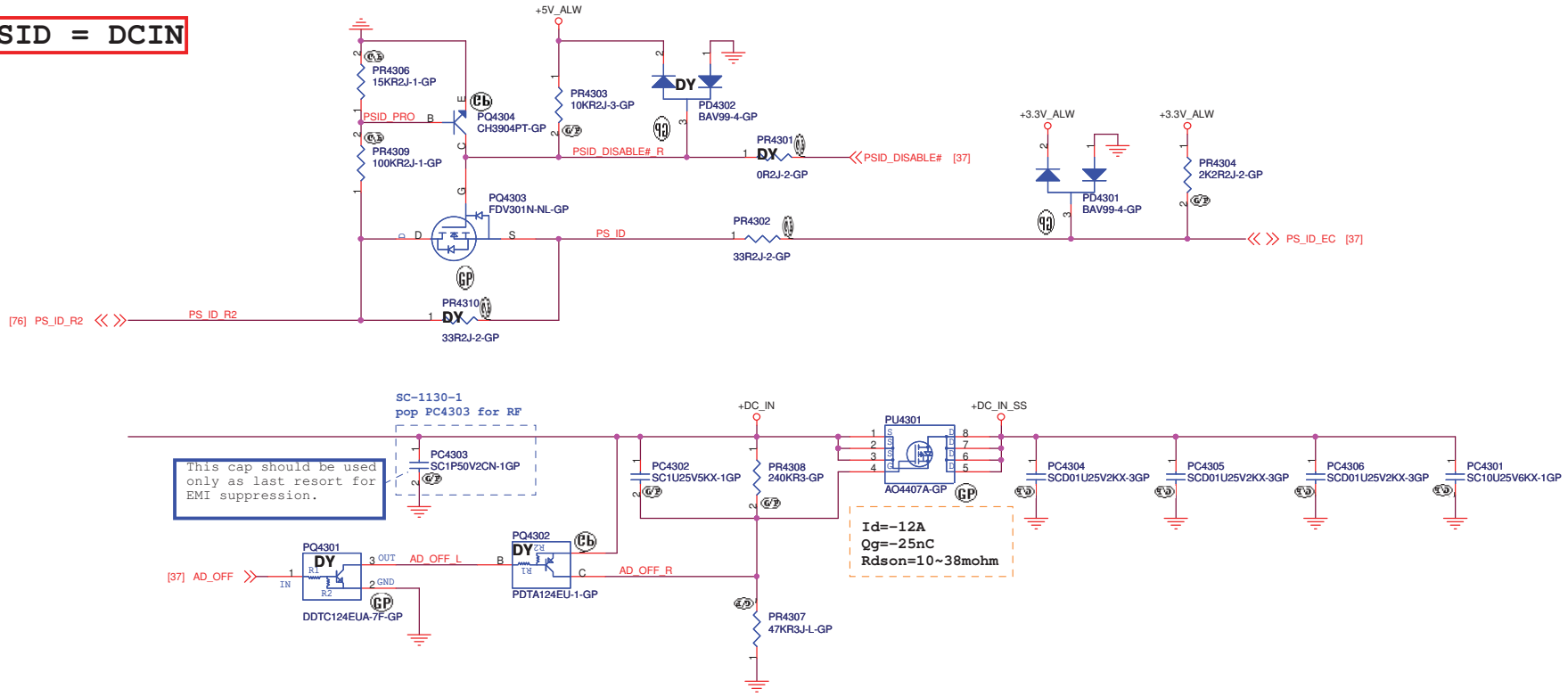
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 42 of 88

**SSID = DCIN**



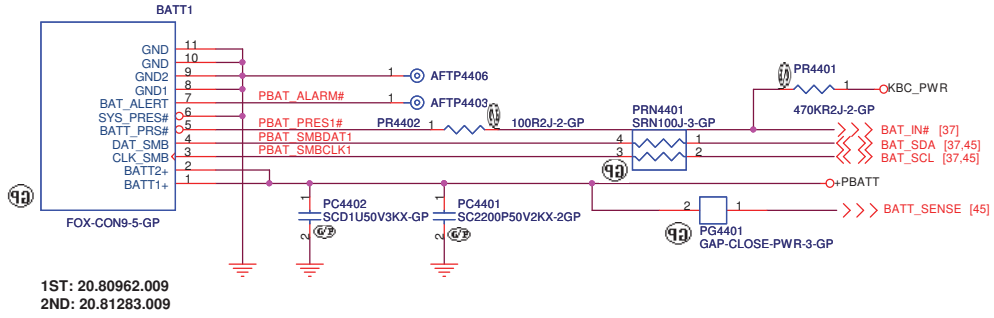

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

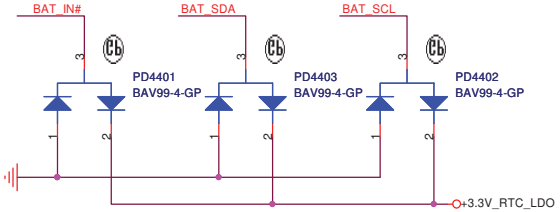
| | | |
|---|---|---|
| Title | DCIN | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 43 of 88 | |

**SSID = BATT**

# Batt Connecter




1ST: 20.80962.009
2ND: 20.81283.009


1st Samsung

Wistron Corporation
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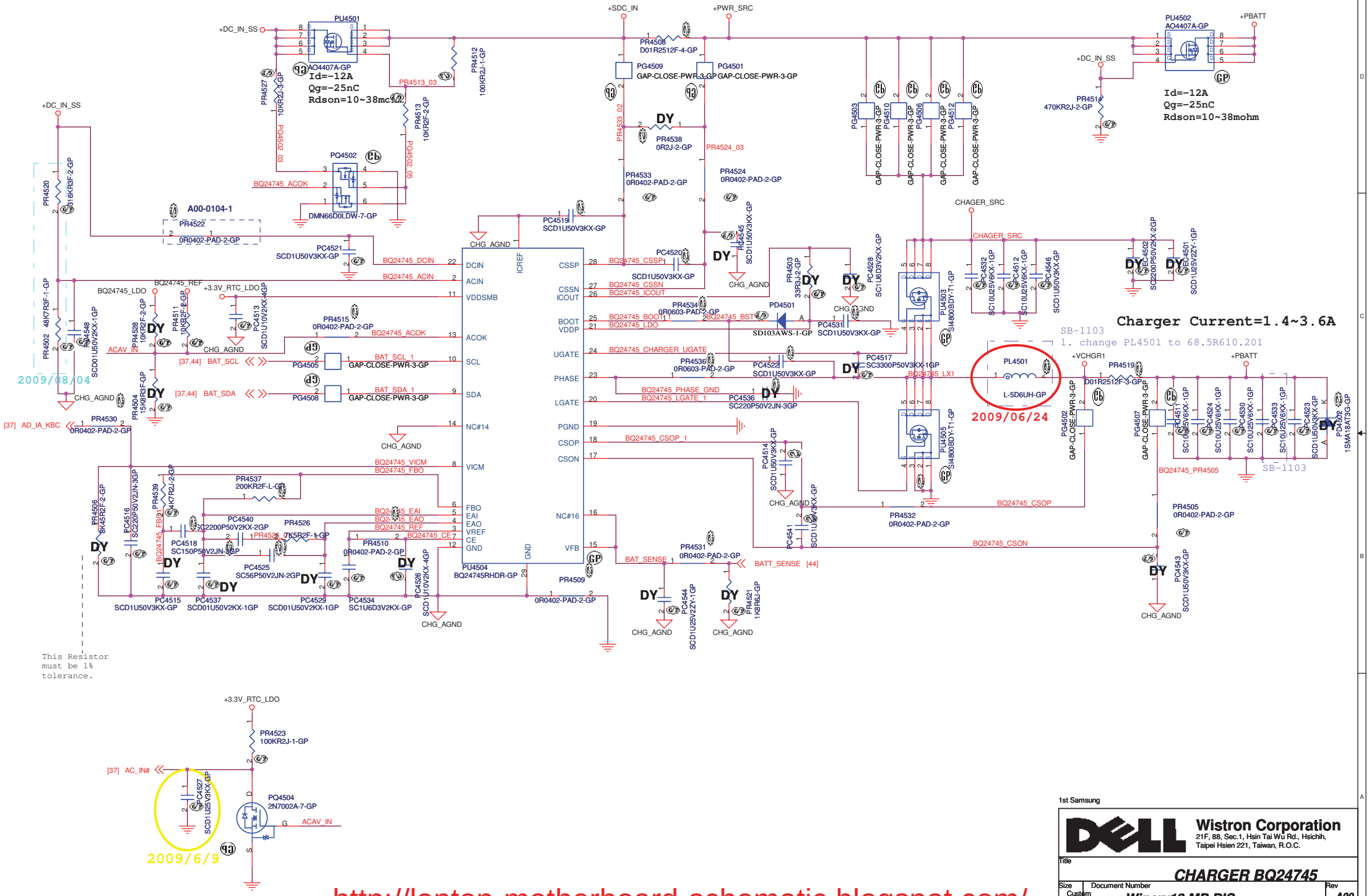
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | Batt Connecter | |
| Size A3 | Document Number Winery13 MB DIS | Rev A00 |
| Date: Wednesday, January 13, 2010 | Sheet 44 of 88 | |

SSID = Charger








1st Samsung

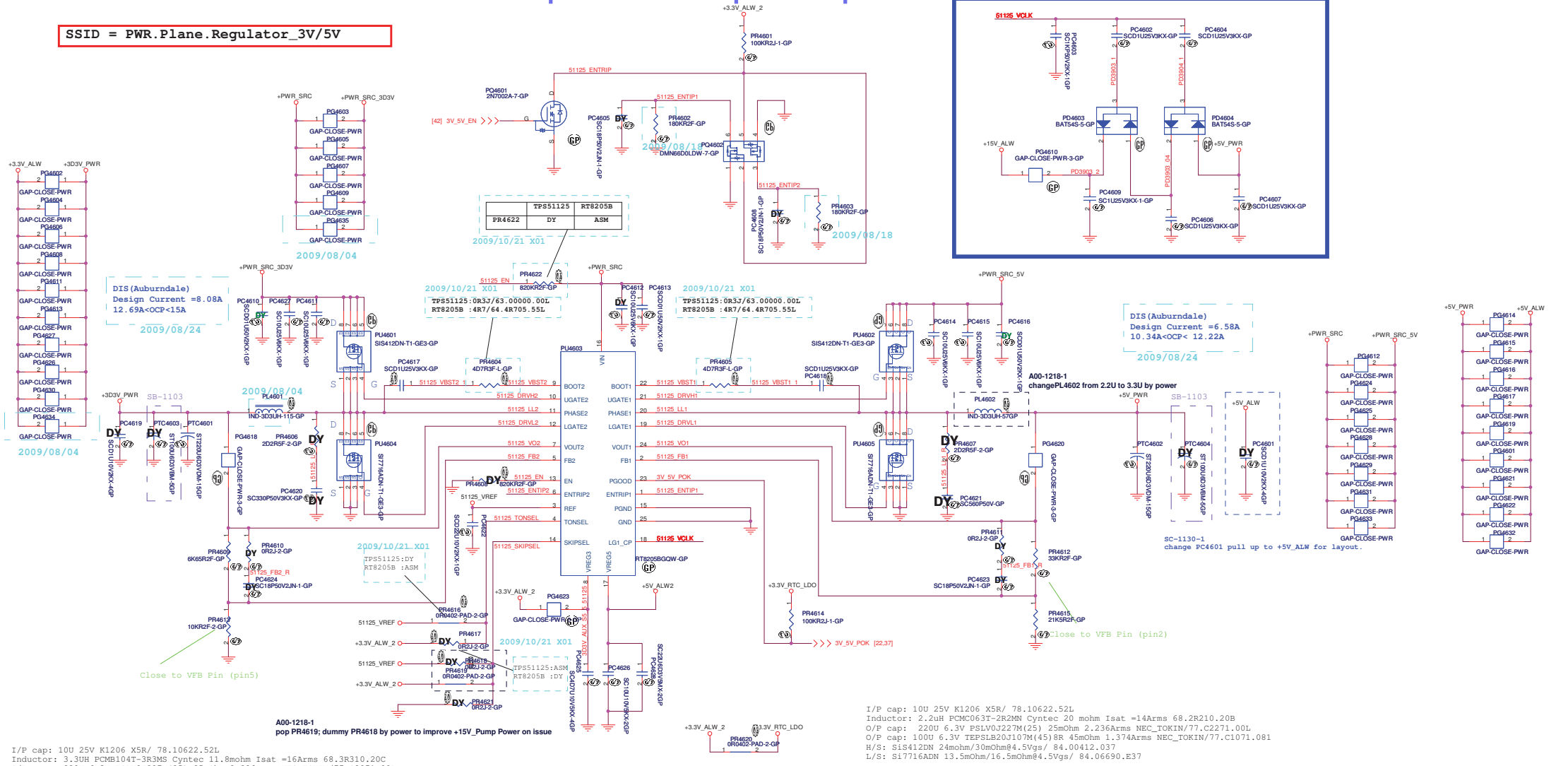
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 45 of 88

SSID = PWR.Plane.Regulator_3V/5V




| TONSEL | CH1 | CH2 |
|---|---|---|
| GND | 200kHz | 265kHz |
| VREF | 245kHz | 305kHz |
| VREG3 | 300kHz | 375kHz |
| VREG5 | 365kHz | 460kHz |

| SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND |
|---|---|---|---|
| Operating Mode | OOA Auto Skip | Auto Skip | PWM only |

| EN0 | Open | 820kΩ to GND | GND |
|---|---|---|---|
| Operating Mode | enable both LDOs, VCLK on and ready to turn on switcher channels | enable both LDOs, VCLK off and ready to turn on switcher channels | disable all circuit |

1st Samsung

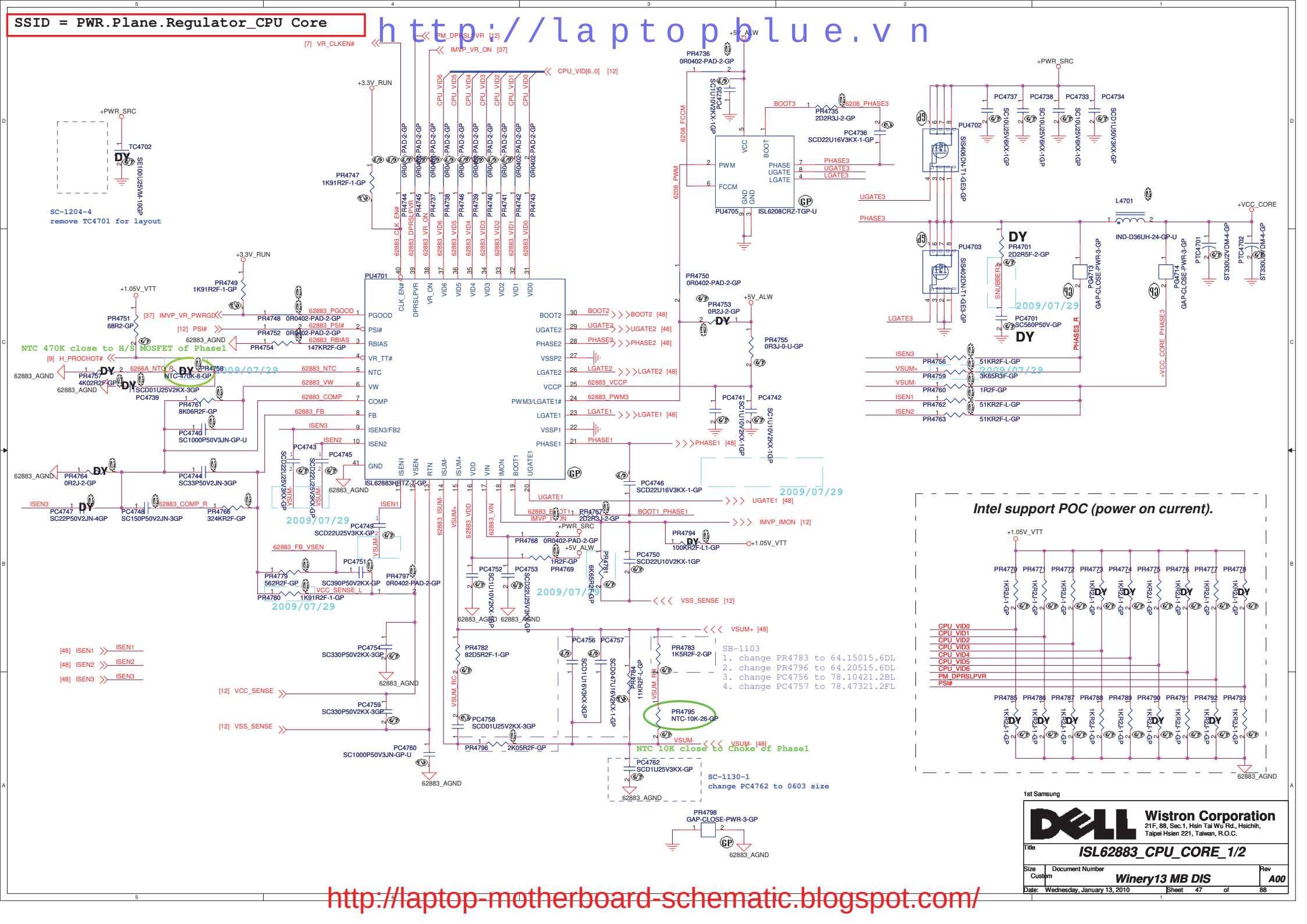
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 46 of 88

SSID = PWR.Plane.Regulator_CPU Core




1st Samsung

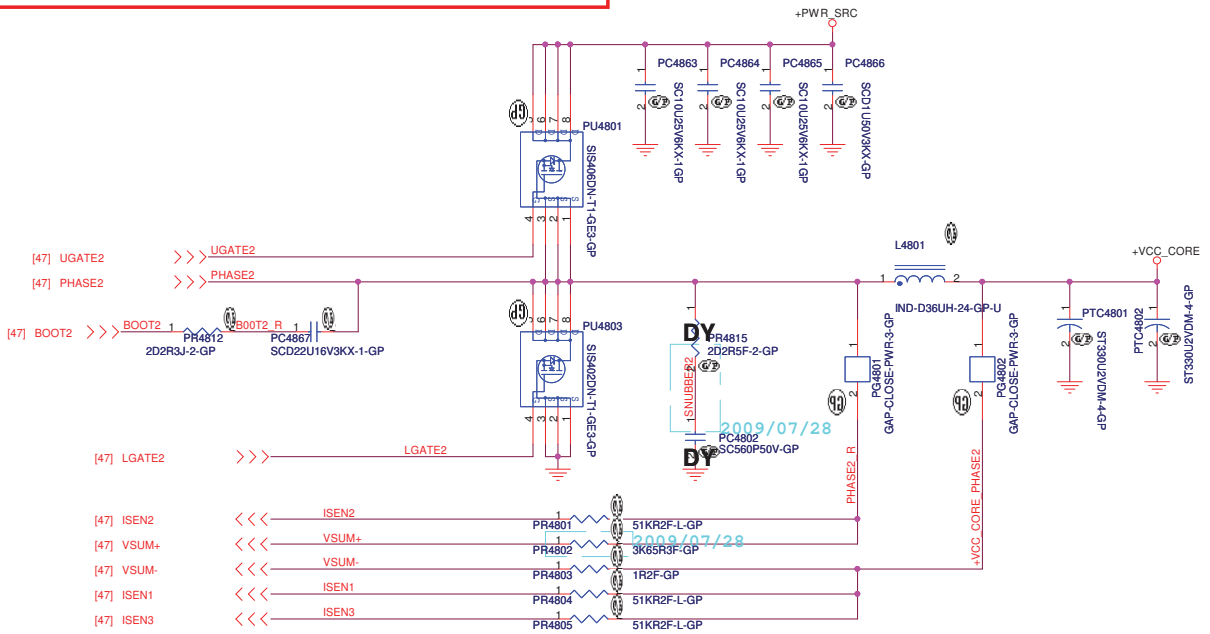
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE_1/2

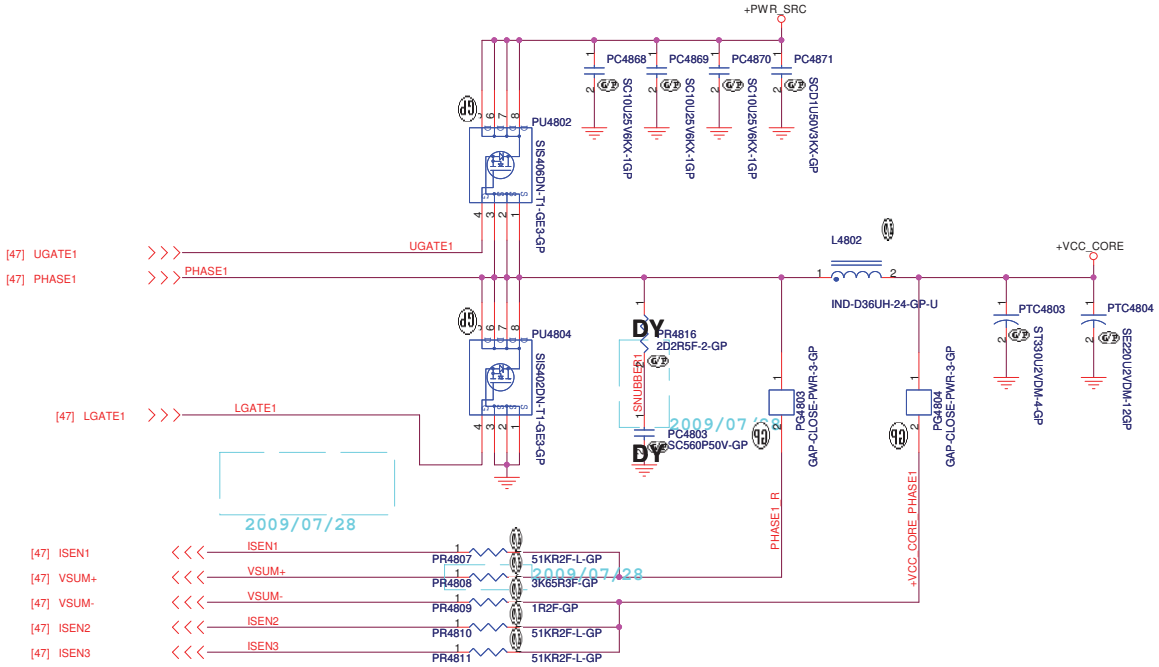
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 47 of 88

SSID = PWR.Plane.Regulator_CPU Core




DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A




I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SiR474DP/ POWERPAK-8/ 10mOhm/12mOhm @4.5Vgs/ 84.00474.037
L/S: Si7170DP/ POWERPAK-8/ 3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037
Freq=300KHz@PER PHASE

1st Samsung

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

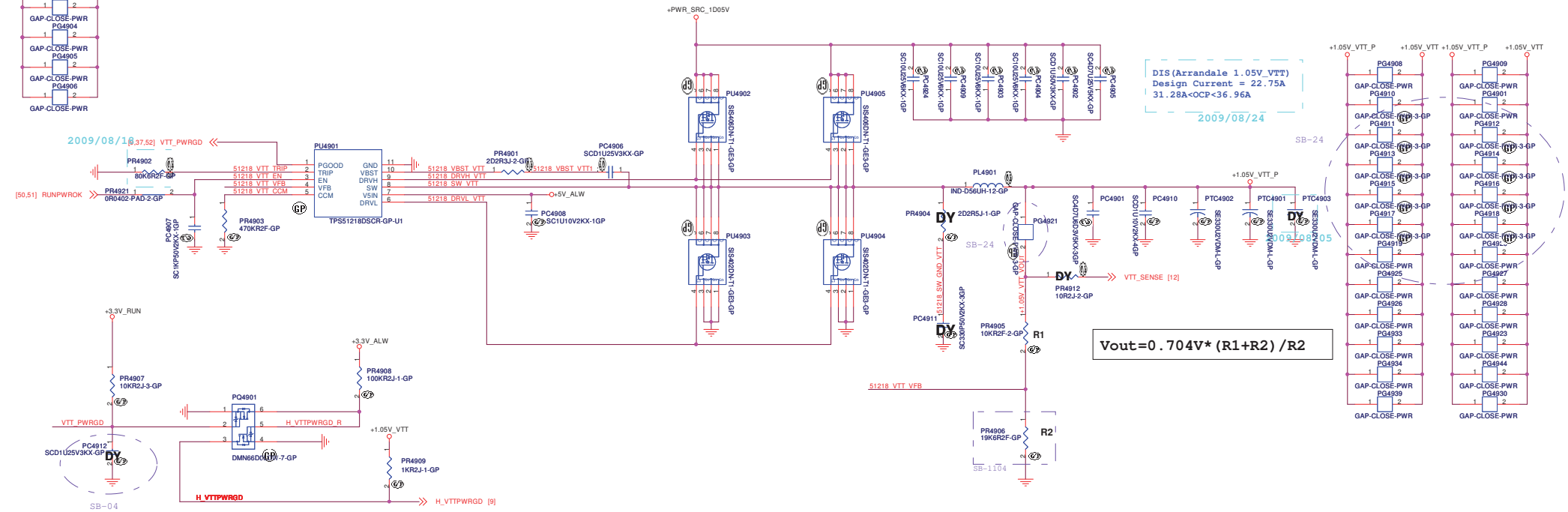
Title: ISL62883_CPU_CORE_2/2

| Size | Document Number | Rev |
|---|---|---|
| Custom | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 48 of 88

SSID = PWR.Plane.Regulator_1D05V_VTT

# TPS51218 for +1.05V_VTT




| Frequency setting |
|---|
| 470K --> 290KHz |
| 200K --> 340KHz |
| 100K --> 380KHz |
| 39K --> 430KHz |

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

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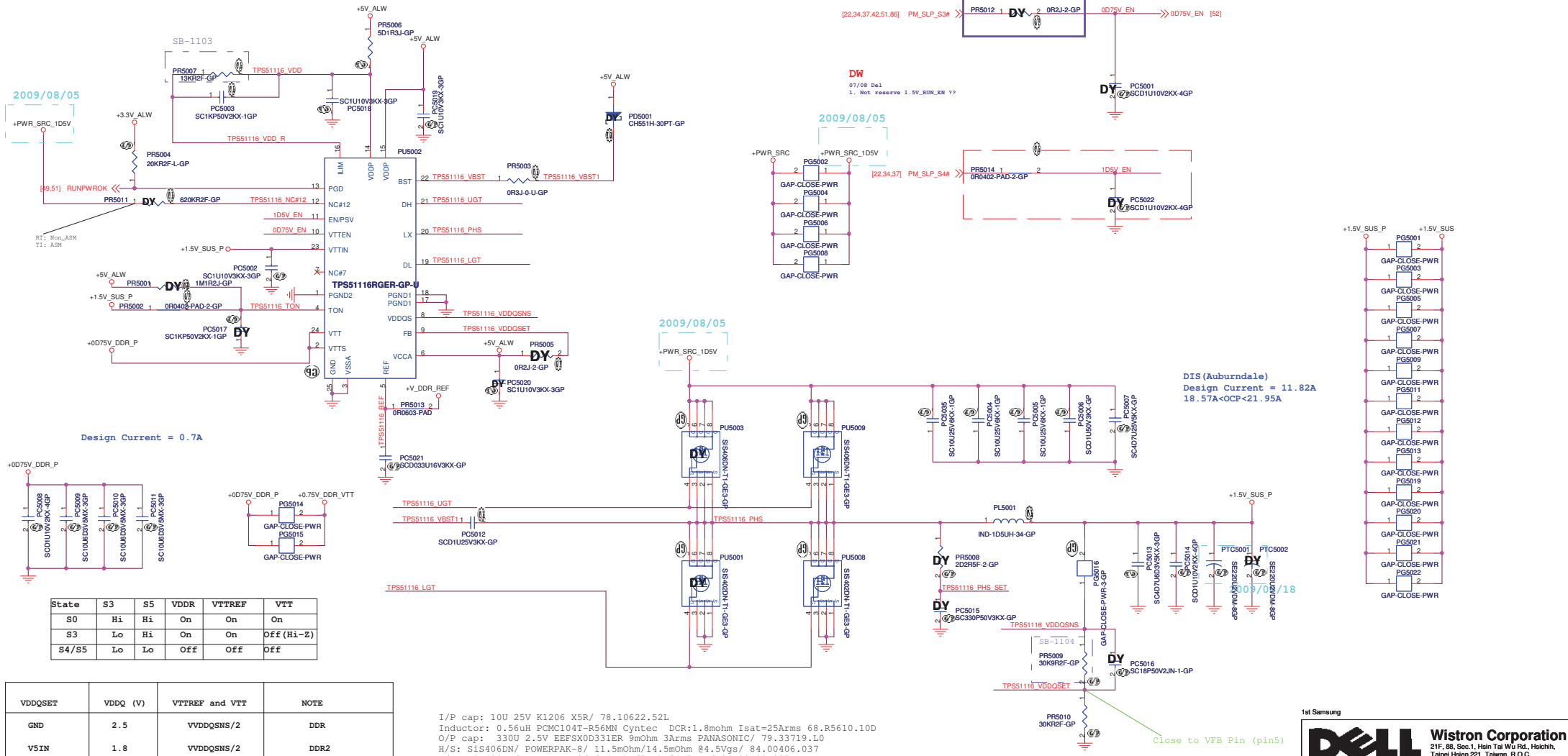
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 49 of 88

SSID = PWR.Plane.Regulator_1D5V/0D75V




| State | S3 | S5 | VDDR | VTTREF | VTT |
|---|---|---|---|---|---|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off(Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |

| VDDQSET | VDDQ (V) | VTTREF and VTT | NOTE |
|---|---|---|---|
| GND | 2.5 | VVDDQSNS/2 | DDR |
| V5IN | 1.8 | VVDDQSNS/2 | DDR2 |
| FB Resistors | Adjustable | VVDDQSNS/2 | 1.5 V < VVDDQ < 3 V |

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
Switching freq-->400KHz

1st Samsung

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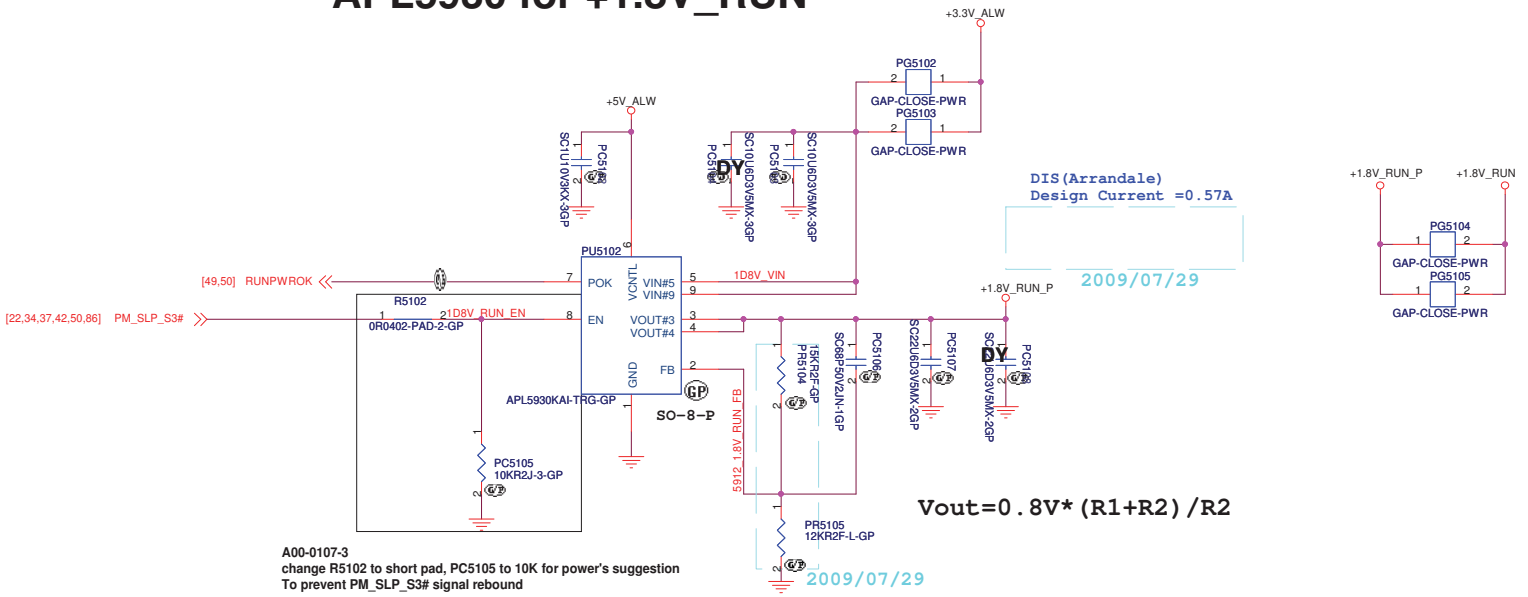
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_SUS
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 50 of 88

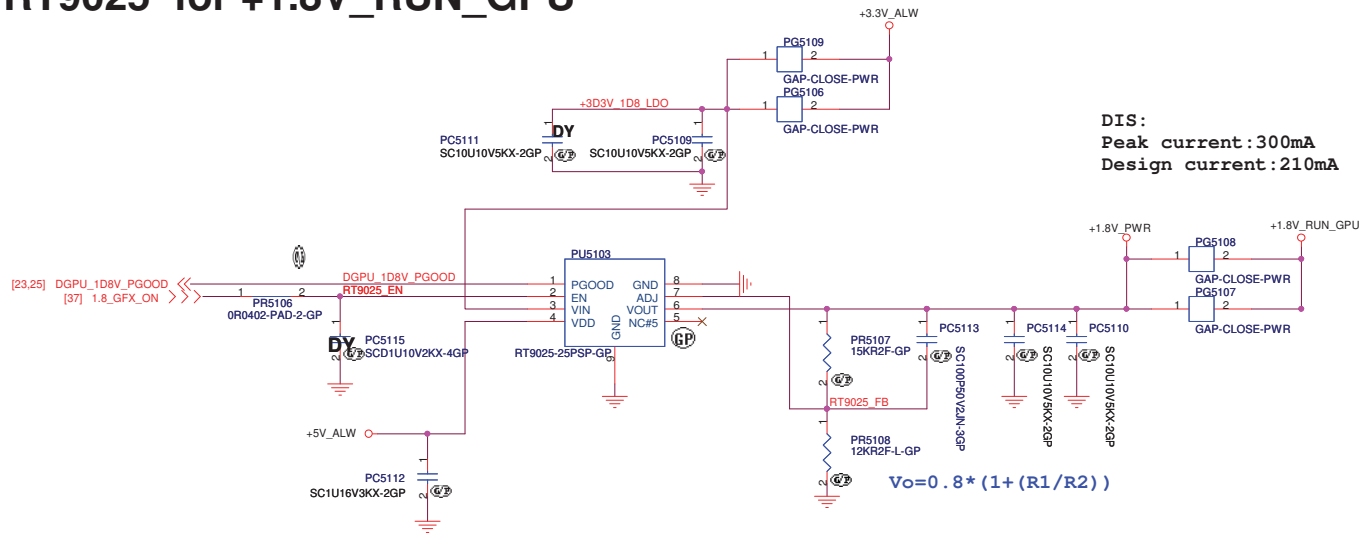
SSID = PWR.Plane.Regulator_1D8V

## APL5930 for +1.8V_RUN




A00-0107-3
change R5102 to short pad, PC5105 to 10K for power's suggestion
To prevent PM_SLP_S3# signal rebound

## RT9025 for +1.8V_RUN_GPU




1st Samsung

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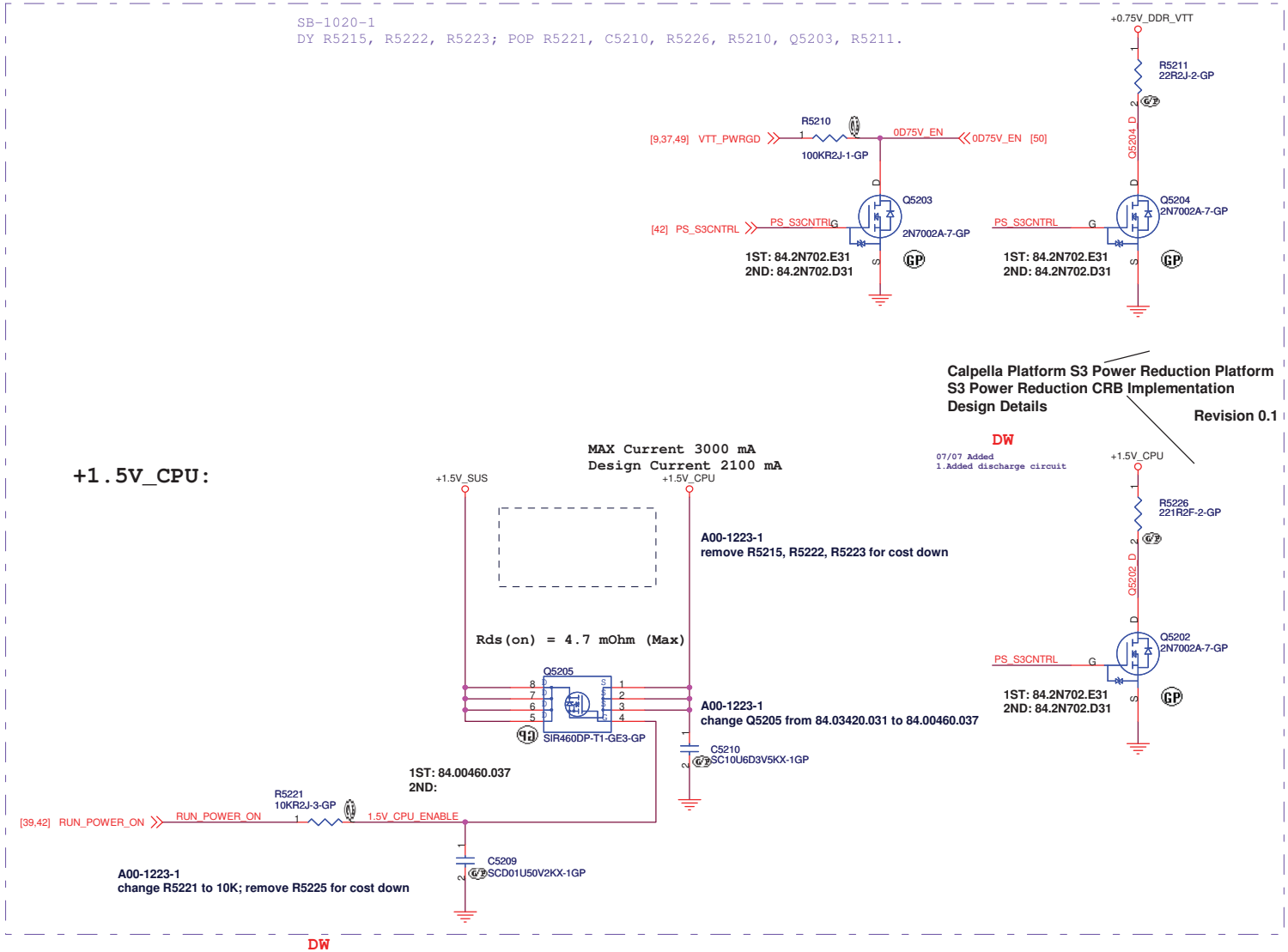
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930/RT9205

| Size | Document Number | Rev |
|---|---|---|
| Custom | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 51 of 88

**SSID = PWR.Plane.Switch_1D5V CPU**

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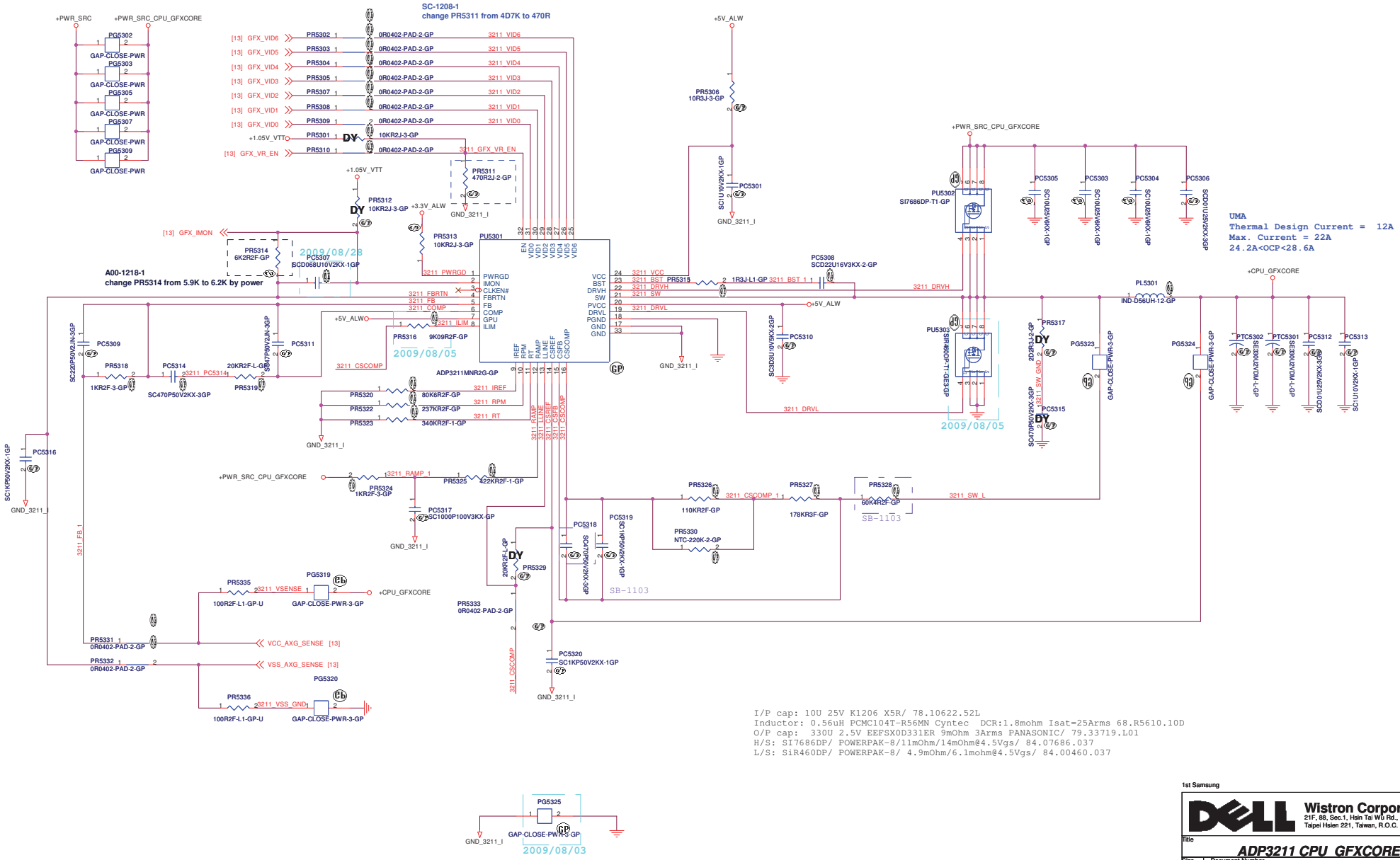
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | DC to DC 1D5V | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 52 of 88 | |

**SSID = CPU.GFX.Regulator**




1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU_GFXCORE

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 53 of 88

SSID = VIDEO

Close PCH

Close GPU

RN5404 SRN2K2J-1-GP

RN5409 SRN2K2J-1-GP

DW
07/07 Added
1.Added LVDS DDC CLK/DAT Pull Hi

[20] L_DDC_DATA
[20] L_DDC_CLK

[81] LDDC_DATA
[81] LDDC_CLK

## UMA/DIS LVDS DDC CLK/DAT select circuit

U5444 NC7SB3157P6X-1GP

[81] LDDC_DATA
[20] L_DDC_DATA

LDDC_DATA_CON
EDID_SELECT#

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

1ST: 73.03157.C0H
2ND: 73.03157.E0J

[21,55] EDID_SELECT#

U5445 NC7SB3157P6X-1GP

[81] LDDC_CLK
[20] L_DDC_CLK

LDDC_CLK_CON
EDID_SELECT#

LDDC_DATA_CON
LDDC_CLK_CON

C5414 SC22P50V2JN-4GP
C5415 SC22P50V2JN-4GP

*EV @ LVDS side*

1ST: 73.03157.C0H
2ND: 73.03157.E0J

## LVDS CONNECTOR

JAE-CON30-DP-U

LCD1

EC5404 SCD1U50V3KX-GP

C5402 SCD1U10V2KX-4GP

R5404 33R2J-2-GP

R5406 100R2J-2-GP
R5413 100R2J-2-GP

R5408 100R2J-2-GP

R5410 10KR2J-3-GP

+3.3V_EEPROM
LCD_BRIGHTNESS
BLON_OUT_R
LCD_TST_L
LDDC_CLK_CON
LDDC_DATA_CON
LCD_DET_G
LCD_CBL_DET#
VGA_TXAOUT0-
VGA_TXAOUT0+
VGA_TXAOUT1-
VGA_TXAOUT1+
VGA_TXAOUT2-
VGA_TXAOUT2+
VGA_TXACLK-
VGA_TXACLK+

SB-06

LCD_CBL_DET# [25]
VGA_TXAOUT0- [74]
VGA_TXAOUT0+ [74]
VGA_TXAOUT1- [74]
VGA_TXAOUT1+ [74]
VGA_TXAOUT2- [74]
VGA_TXAOUT2+ [74]
VGA_TXACLK- [74]
VGA_TXACLK+ [74]

BLON_OUT [37]
LCD_TST [37]

1ST: 20.F1555.030
2ND:

## UMA/DIS LVDS PWM select circuit

R5438 0R2J-2-GP

[37] LBKLT_CTL_EC
[81] LBKLT_CTL_GPU
[20] LBKLT_CTL_PCH

U5448 NC7SB3157P6X-1GP

LCD_BRIGHTNESS
DGPU_PWM_SELECT# [21]

1ST: 73.03157.C0H
2ND: 73.03157.E0J

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

LCD_BRIGHTNESS
LCD_TST

C5402 SC33P50V2JN-3GP
C5401 SC33P50V2JN-3GP

For EMI request

BLON_OUT_R

R5407 10KR2J-3-GP

SSID = Inverter

## INVERTER POWER

1ST: 69.50007.A41
2ND: 69.50007.A31

+PWR_SRC_LCD
+PWR_SRC

F5401 POLYSW-1D1A24V-1-GP

C5401 SC1KP50V2KX-1GP
C5405 SCD1U25V3KX-GP
EC5403 SCD1U25V2ZY-1GP

SC-1207-1
pop EC5403 for EMI

SSID = VIDEO

## LCD POWER

+LCDVDD

C5403 SC10U6D3V5KX-1GP
C5406 SCD1U10V2KX-4GP

SC-1125-2
add mux U5446 to select LCDVDD enable signal

D5409 BAT54C-7-F-GP

ENVDD_M
ENVDD_D
[37] SHBM_LCDTST_EN

A00-1223-1
modify LCD power schematic
remove D5401

1ST: 83.00054.X81
2ND: 83.BAT54.081

R5409 0R2J-2-GP
R5411 49K9R2F-L-GP

U5403 G5285T11U-GP

C5408 SCD1U16V2KX-3GP
C5407 SC1U10V3KX-3GP

1ST: 74.05285.07F
2ND:

SB-1023

DGPU_SELECT# :
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

U5446 NC7SB3157P6X-1GP

[81] LCDVDD_EN_GPU
[20] LCDVDD_EN_PCH

ENVDD_M

DGPU_SELECT# [21,37,74]

1ST: 73.03157.C0H
2ND: 73.03157.E0J

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 54 of 88

**SSID = VIDEO**

A00-1218-1
change R5504, R5505, R5506 from 0R to 33R by EMI

A00-1218-1
change L5501, L5502, L5503 to 0R

[74] M_RED
[74] M_GREEN
[74] M_BLUE

R5504 M_RED_C 33R2J-2-GP
R5505 M_GREEN_C 33R2J-2-GP
R5506 M_BLUE_C 33R2J-2-GP

L5502 0R3J-0-U-GP CRT_R
L5501 0R3J-0-U-GP CRT_G
L5503 0R3J-0-U-GP CRT_B

R5502 150R2F-1-GP
R5501 150R2F-1-GP
R5503 150R2F-1-GP

C5508 SC8P250V2CC-GP
C5501 SC8P250V2CC-GP
C5506 SC8P250V2CC-GP

C5509 SC8P250V2CC-GP
C5507 SC8P250V2CC-GP
C5512 SC8P250V2CC-GP

CRT_R D5501 BAV99-4-GP +3.3V_RUN_GPU
CRT_G D5502 BAV99-4-GP +3.3V_RUN_GPU
CRT_B D5503 BAV99-4-GP +3.3V_RUN_GPU

+5V_CRT_RUN D5504 B0530WS-7-F-GP +5V_RUN
C5510 SCD01U16V2KX-3GP

A00-0104-1
change CRT1 from 20.20431.015 to 20.20401.015

CRT1 VIDEO-15-127-GP-U
AFTP5502

CRT_R
CRT_G
CRT_B
+5V_CRT_RUN
DDC_DATA_CON
JVGA_HS [74]
JVGA_VS [74]
DDC_CLK_CON

1ST: 20.20401.015
2ND: 20.20479.015

C5502 SC33P50V2JN-3GP
C5504 SC33P50V2JN-3GP

**Layout Note:**

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

AFTP5503 +5V_CRT_RUN
AFTP5501 DDC_DATA_CON
AFTP5509 DDC_CLK_CON
AFTP5507 CRT_R
AFTP5506 CRT_G
AFTP5508 CRT_B
AFTP5504 JVGA_HS
AFTP5505 JVGA_VS

**DW**
07/14 Change
1.Change CRT1 CONN PN from 20.20431.015 to 20.20401.015 base on ME emm files.

**DW**
07/07 Change
1.Change CRT DDC CLK/DAT Circuit

Close PCH
+3.3V_RUN
RN5510 SRN2K2J-1-GP
[20] GMCH_DDCDATA
[20] GMCH_DDCCLK

Close GPU
+3.3V_RUN_GPU
RN5511 SRN2K2J-1-GP
[81] CRT_DAT_DDC
[81] CRT_CLK_DDC

**UMA/DIS CRT DDC CLK/DAT select circuit**

U5542 +3.3V_RUN
[81] CRT_DAT_DDC
[20] GMCH_DDCDATA
B0 GND B1 VCC A S
DDC_DATA_CON2
EDID_SELECT#
NC7SB3157P6X-1GP

[21,54] EDID_SELECT#

U5543 +3.3V_RUN
[81] CRT_CLK_DDC
[20] GMCH_DDCCLK
B0 GND B1 VCC A S
DDC_CLK_CON2
EDID_SELECT#
NC7SB3157P6X-1GP

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

+5V_CRT_RUN
RN5513 SRN2K2J-1-GP
DDC_DATA_CON
DDC_CLK_CON
C5519 SC22P50V2JN-4GP
C5520 SC10P50V2JN-4GP

A00-1218-1
change C5520 from 22p to 10p by EMI

*5V @ CRT side*

+3.3V_RUN
Q5517 DMN66D0LDW-7-GP
DDC_DATA_CON2
DDC_DATA_CON
DDC_CLK_CON2
DDC_CLK_CON

<Core Design>

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Title: CRT Connector
Size: A3
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 55 of 88

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Title

*(Reserve)*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *Winery13 MB DIS* | *A00* |

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(Blank)

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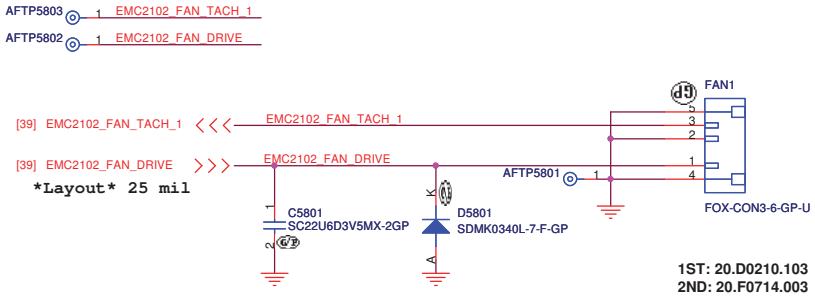
Title: HDMI Connector

| Size | Document Number | Rev |
|---|---|---|
| Custom | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 57 of 88

SSID = Thermal

# Fan Connector

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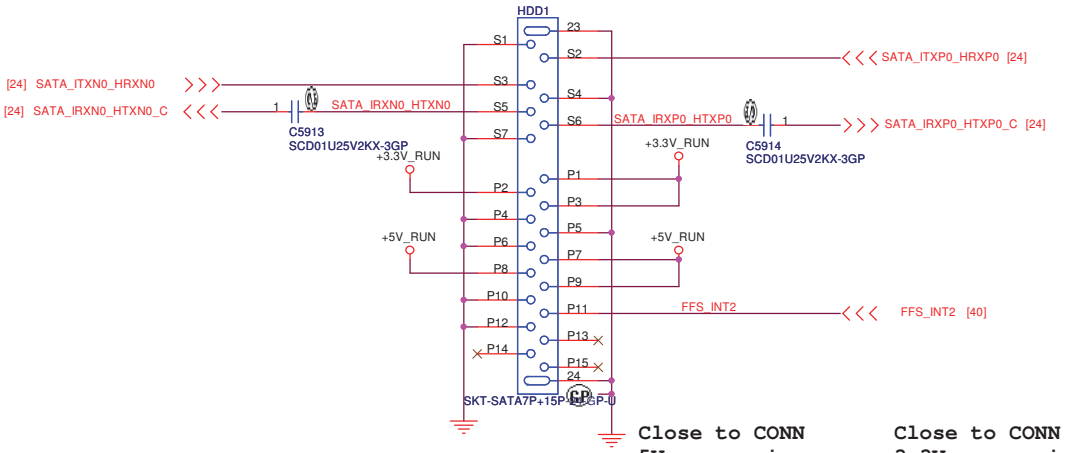
| Title | | |
|---|---|---|
| FAN | | |
| Size: A3 | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 58 of 88 | |

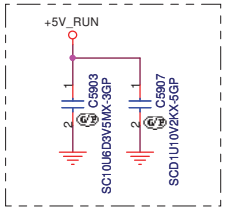
SSID = SATA

# SATA HDD Connector

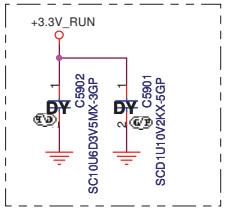



1ST: 22.10300.451
2ND:

Close to CONN
5V power pin



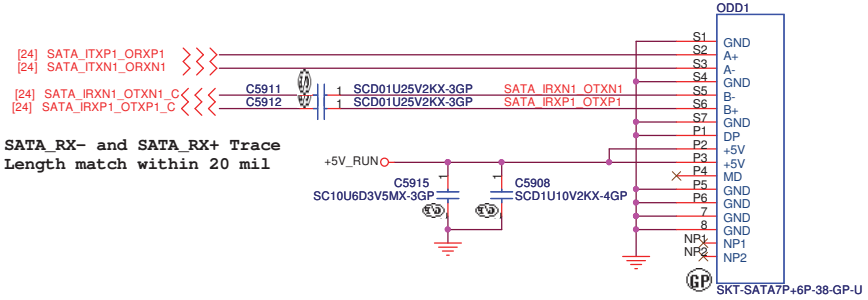

Close to CONN
3.3V power pin




```
SATA HDD Interface comment
*****************************
S1:GND
S2:RX+
S3:RX-
S4:GND
S5:TX-
S6:TX+
S7:GND
*****************************
P1------------ 3.3V
P2------------ 3.3V
P3------------ 3.3V
P4:GND
P5:GND / Dell Detected Pin
P6:GND
P7------------ 5V
P8------------ 5V
P9------------ 5V
P10--- GND
P11:Dell: FFS_INT for supported HDD
P12:GND
P13------------ 12V
P14------------ 12V
P15------------ 12V
*****************************
```

SSID = SATA

# ODD Connector




SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

1ST: 62.10065.531
2ND: 62.10065.D21

1st Samsung

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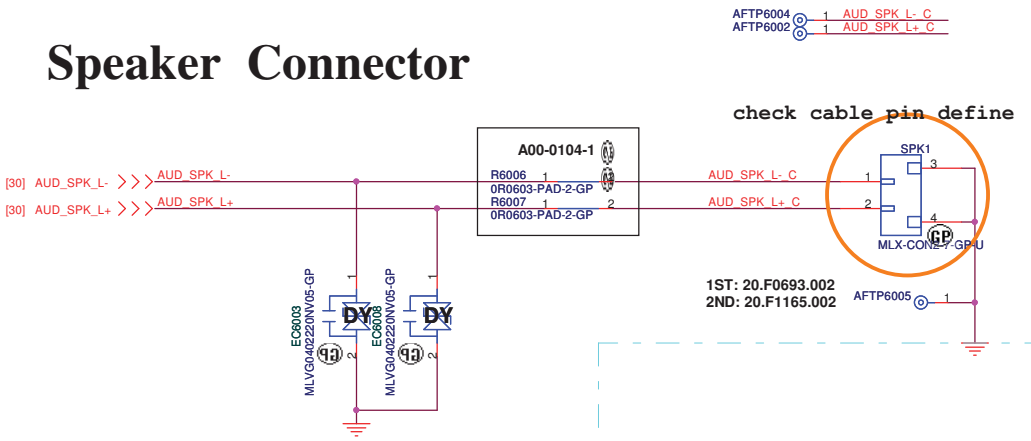
Title: HDD/ODD Connector

| Size | Document Number | Rev |
|---|---|---|
| A3 | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 59 of 88

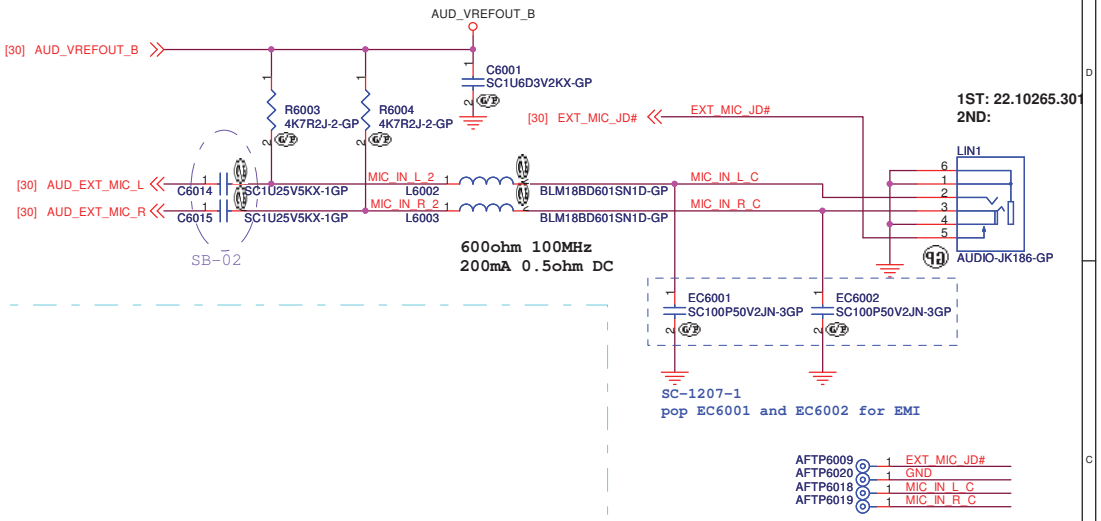
SSID = AUDIO

## Speaker Connector




SSID = AUDIO

## MIC IN

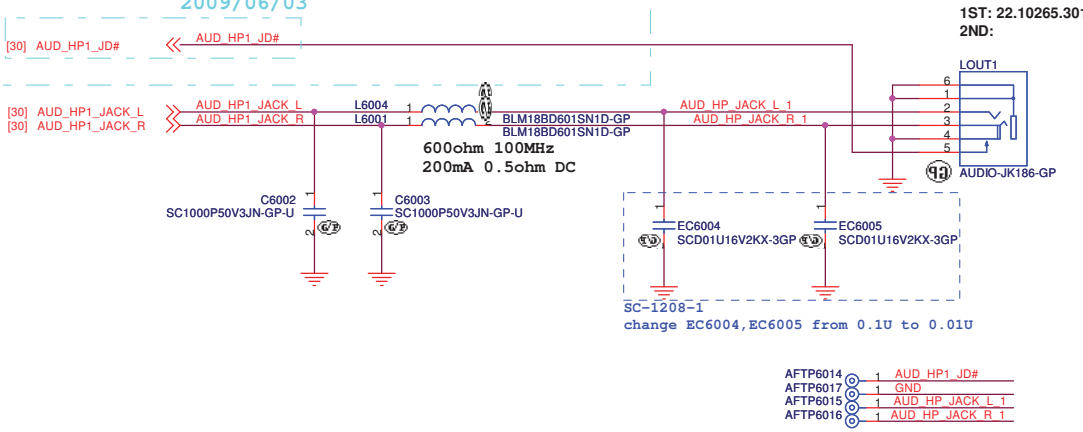



Delete Audio De-pop Circuit
2009/07/24

SSID = AUDIO

## Head Phone

2009/06/03




Added HP circuit 2009/05/26

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Title: SPEAKER/MIC/AUDIO JACK

| Size | Document Number | Rev |
|---|---|---|
| A3 | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 60 of 88

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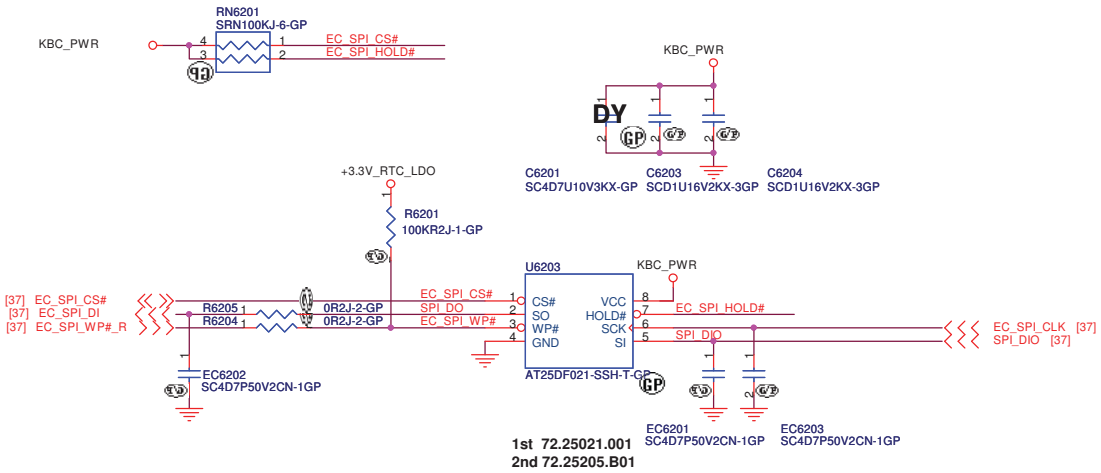
Title: (Reserve)

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

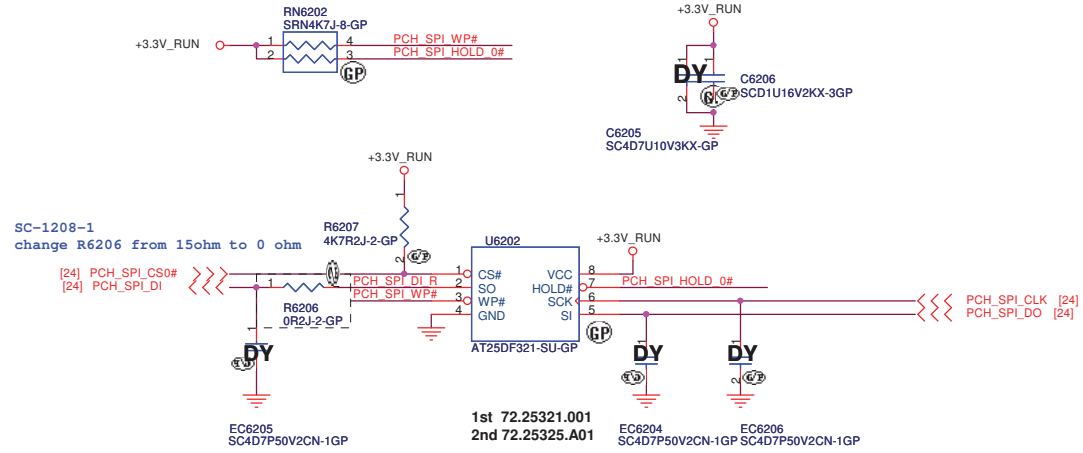
Date: Wednesday, January 13, 2010 | Sheet 61 of 88

SSID = Flash.ROM

## SPI FLASH ROM (2M bits) for KBC

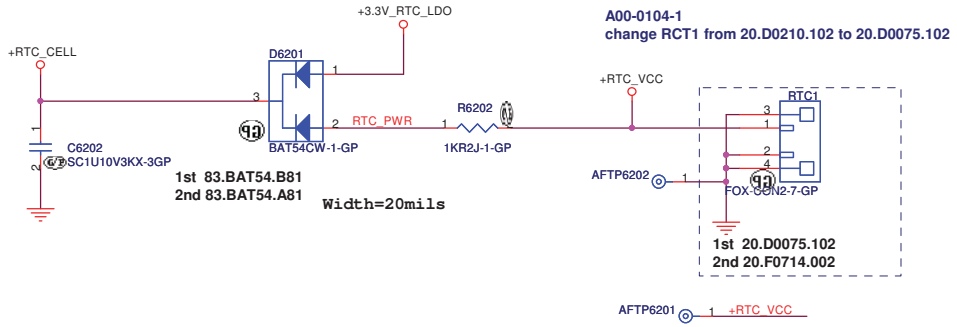



## SPI FLASH ROM (32M bits) for PCH




SSID = RBATT

## RTC Connector

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Title: EEPROM/RTC Connector

| Size | Document Number | Rev |
|---|---|---|
| A3 | Winery13 MB DIS | A00 |

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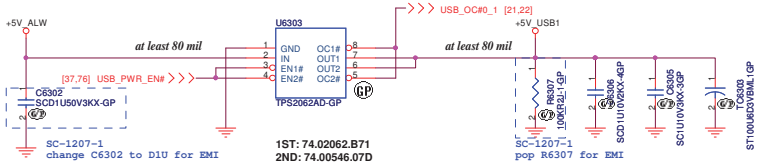
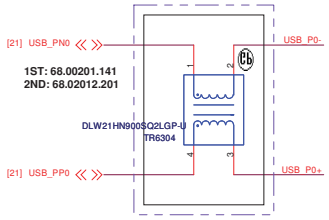
**SSID = USB**

## USB & ESATA Power SW

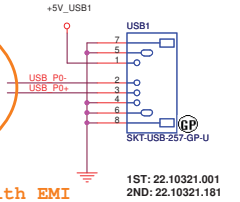



SB-1021
1. pop and change TR6304 to 90 ohm for EMI;
DY R6302, R6308




A00-0106-1
remove R6302, R6308 for no co-lay after XB



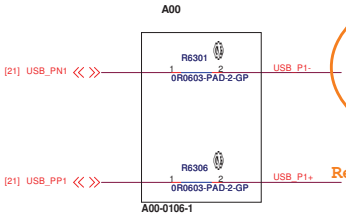





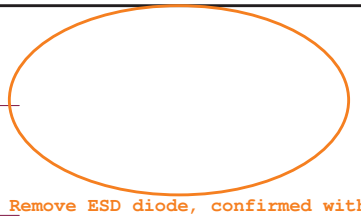
**SSID = ESATA**

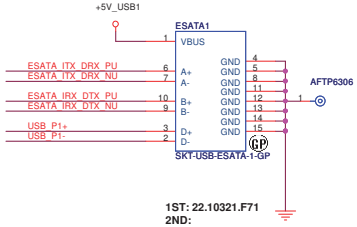
## ESATA Power

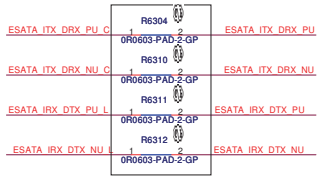
Share one power SW with USB port 1




A00-0106-1
remove TR6301 for no co-lay after XB



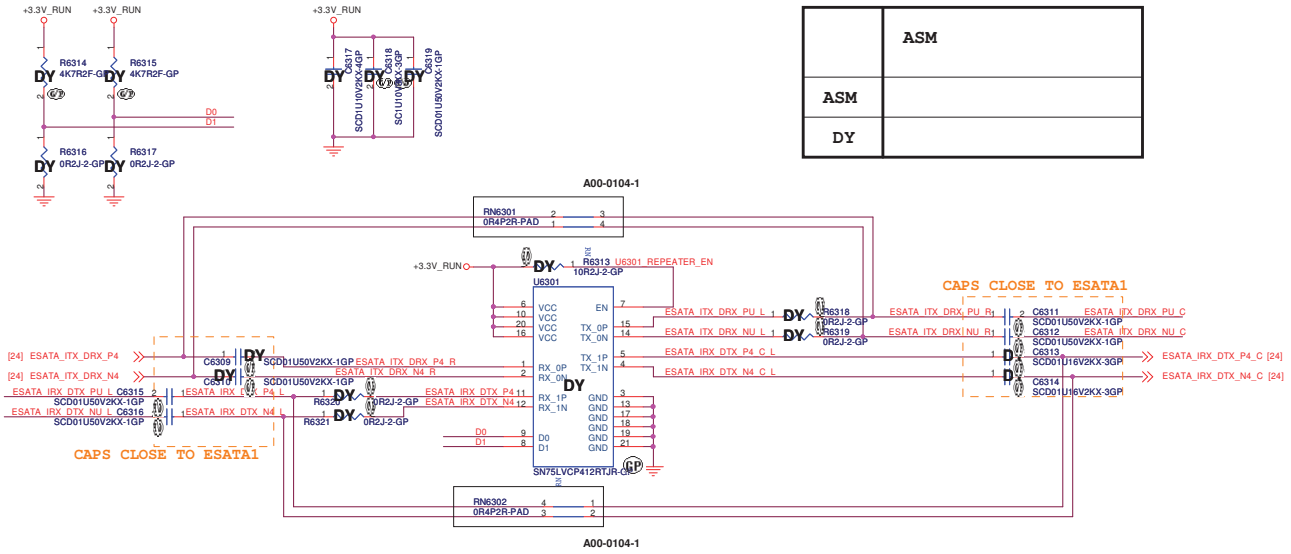




A00-0106-1
remove TR6302, TR6303 for no co-lay after XB




| | ASM |
|---|---|
| ASM | |
| DY | |




A00-0104-1



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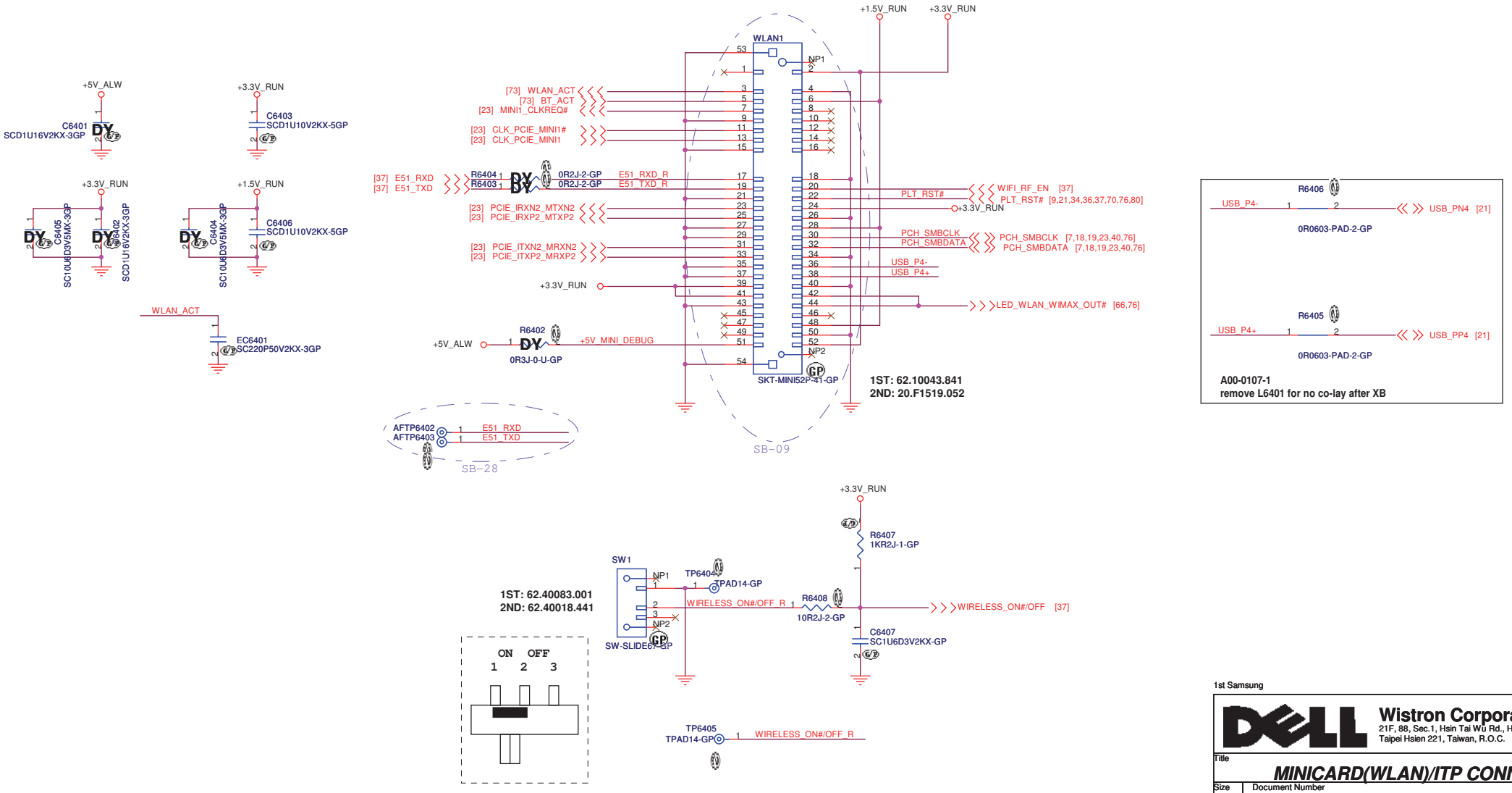
Title: USB/ESATA Port

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 63 of 88

# Mini Card Connector(802.11a/b/g/n)

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Title: MINICARD(WLAN)/ITP CONN

| Size | Document Number | Rev |
|---|---|---|
| A3 | Winery13 MB DIS | A00 |

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1st Samsung

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Title: WWAN Connector

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 65 of 88

**SSID = LED**

### For LED & Capacity board:

| LED Type | Color | Power rail |
|---|---|---|
| BATTERY LED1 | Amber(Multi-color) | ALW |
| SCRL LED | White | ALW |
| CAP LED | White | ALW |
| NUM LED | White | ALW |
| PWR BTN LED | White | ALW |
| SATA ACT LED1 | White | RUN |
| BT ACT LED | White | RUN |
| WLAN/WWAN ACT LED | White | RUN |
| | | |

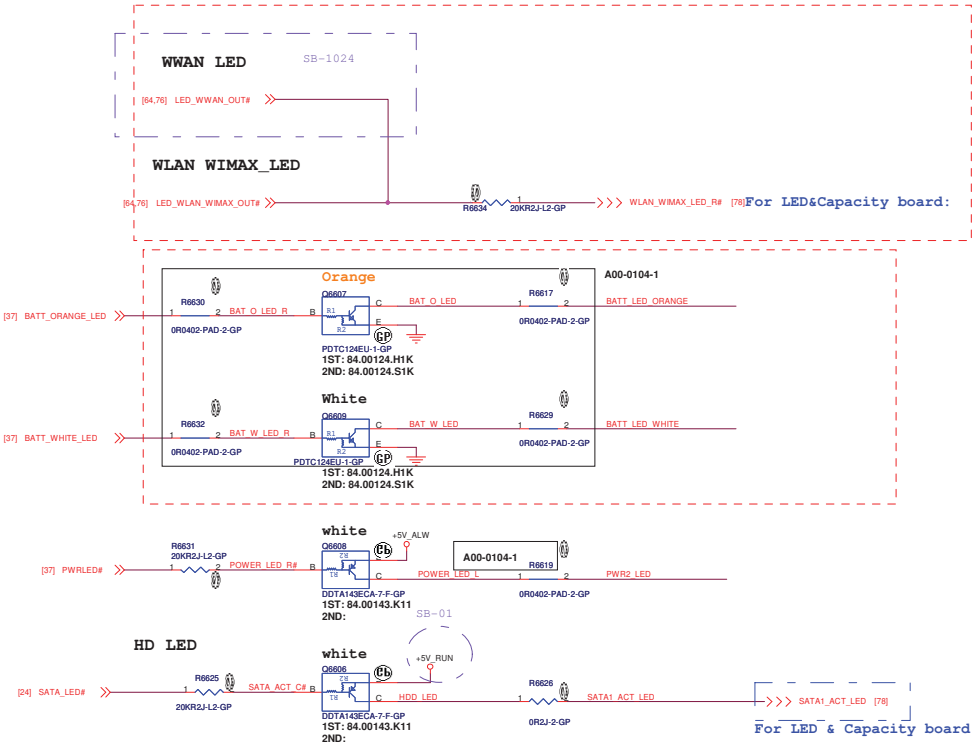
### PWR BTN LED

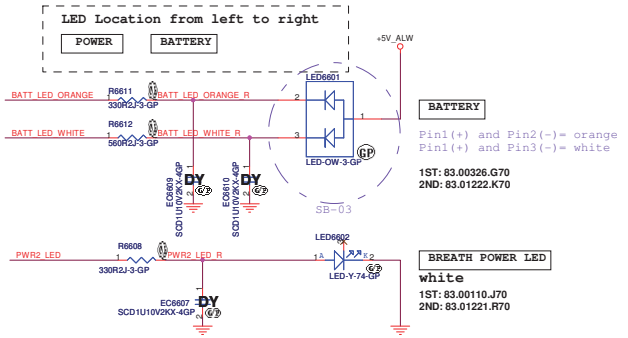

### SCRLK LED


### CAPS LED


### NUM LED


### Bluetooth LED


Remove HDD LED

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Title: LED

| Size | Document Number | Rev |
|---|---|---|
| A2 | Winery13 MB DIS | A00 |

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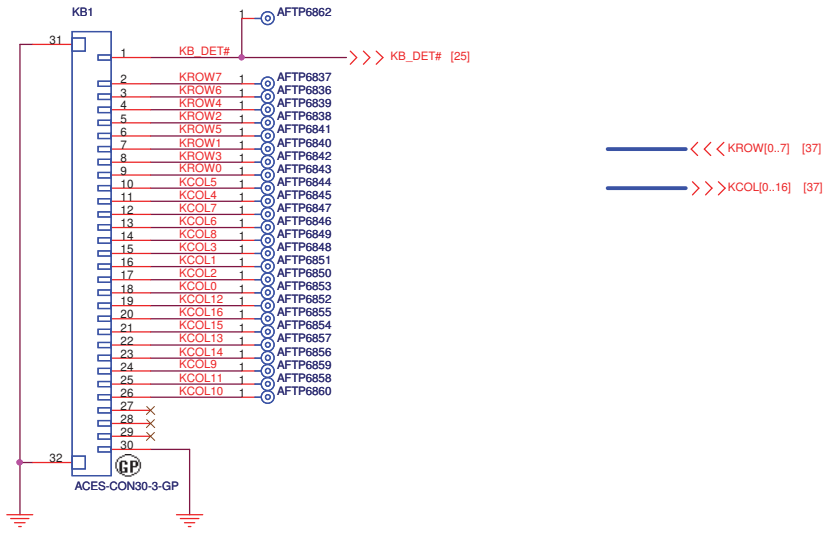
Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 67 of 88

SSID = KBC

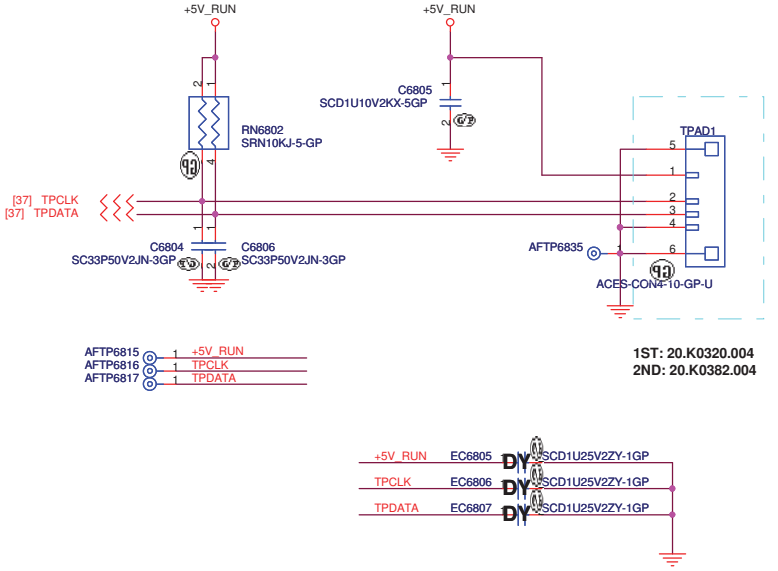
## Internal KeyBoard Connector




1ST: 20.K0421.030
2ND: 20.K0259.030

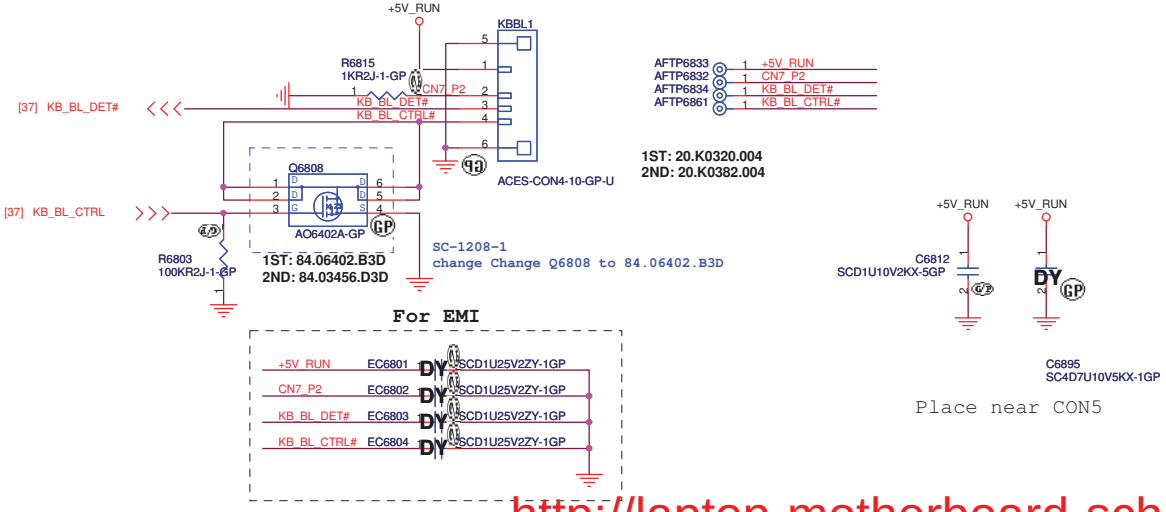
SSID = Touch.Pad

## TouchPad Connector




1ST: 20.K0320.004
2ND: 20.K0382.004

## KB Backlight CONN




1ST: 20.K0320.004
2ND: 20.K0382.004

1ST: 84.06402.B3D
2ND: 84.03456.D3D

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Title: Keyboard/Touch Pad
Size: Custom
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
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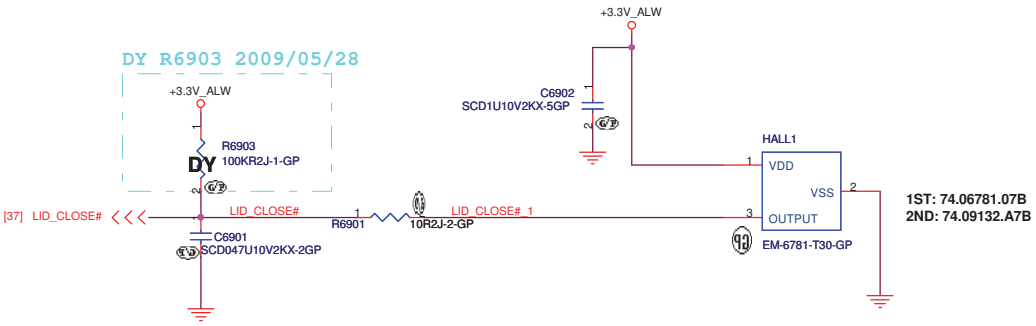
SSID = User.Interface

## Hall Sensor Connector



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Taipei Hsien 221, Taiwan, R.O.C.

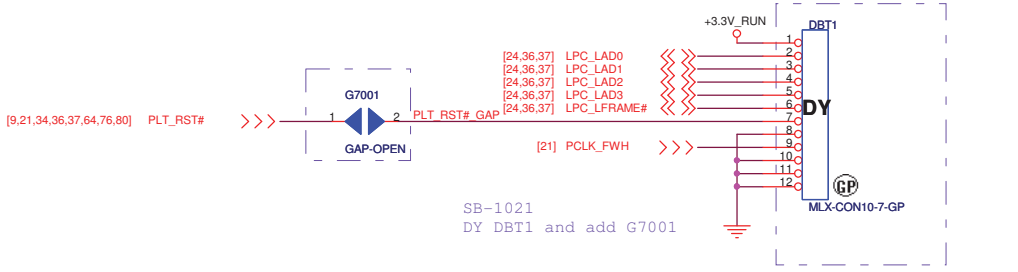
Title: Hall sensor

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 69 of 88

**SSID = DEBUG PORT**

## GOLDEN FINGER FOR DEBUG BOARD




1st Samsung

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| | | |
|---|---|---|
| Title: Debug port | | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 70 of 88 | |

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1st Samsung

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 71 of 88

(Blank)

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Taipei Hsien 221, Taiwan, R.O.C.

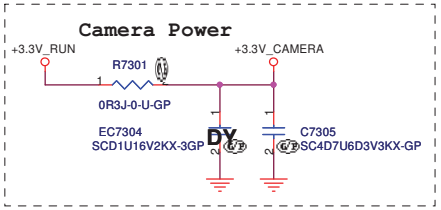
Title: Braidwood

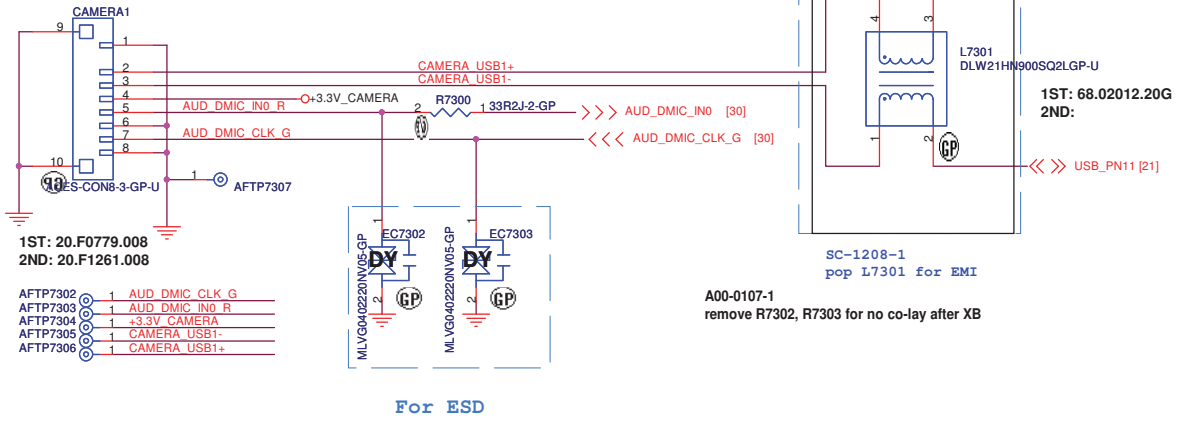
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 72 of 88

SSID = User.Interface

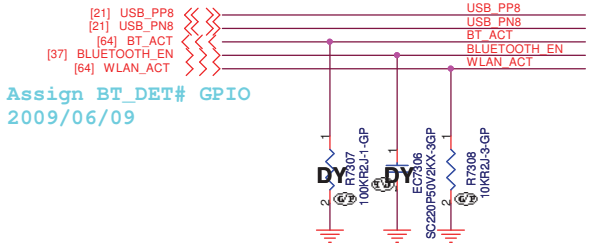
## Camera Connector

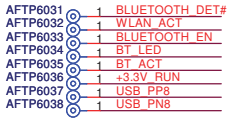


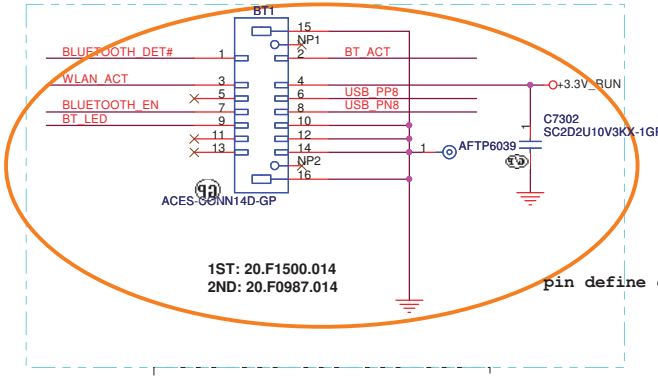



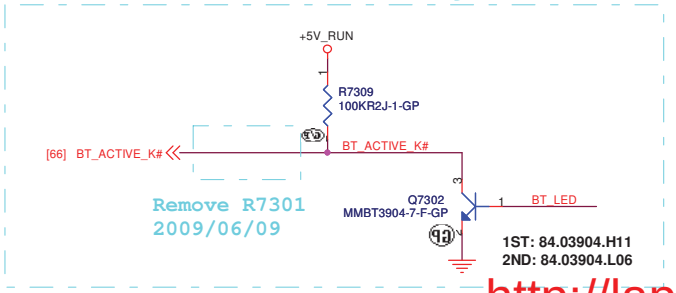

SSID = User.Interface

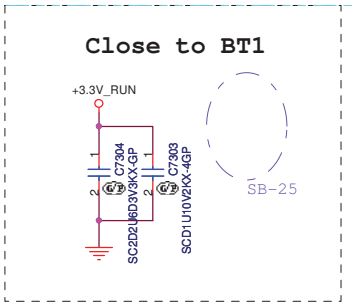
## Bluetooth cable conn.

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

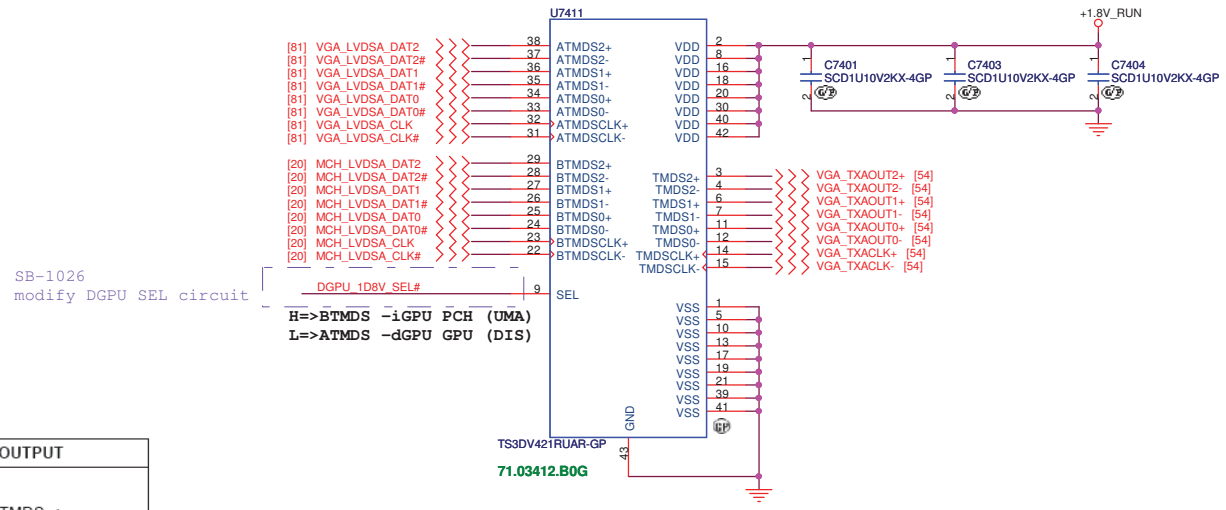
Title: Camera CONN

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 73 of 88

**SSID = VIDEO**

## UMA/DIS LVDS signal select circuit




SB-1026
modify DGPU SEL circuit

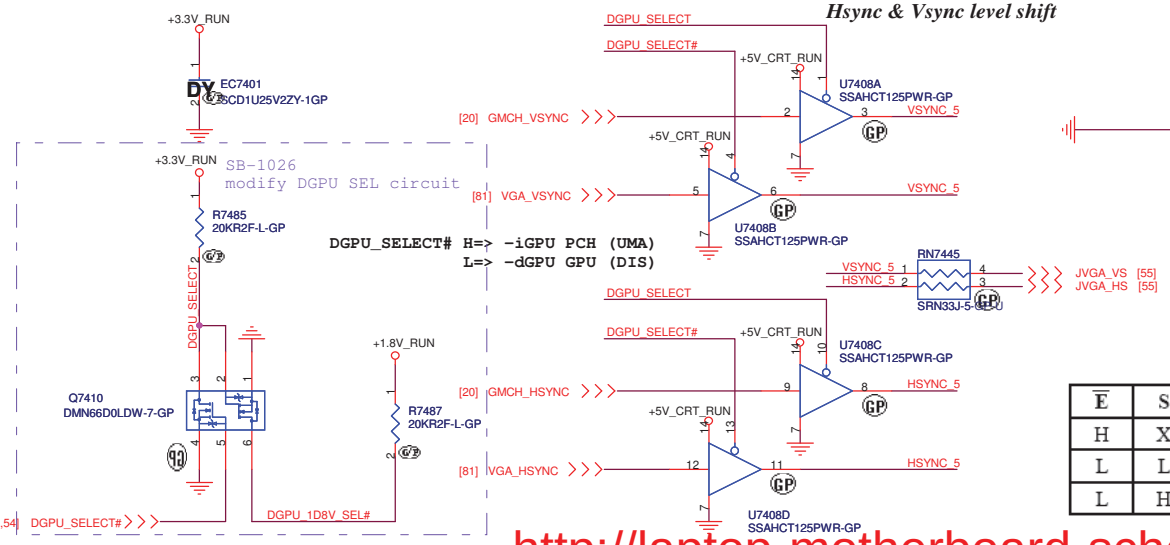
**H=>BTMDS -iGPU PCH (UMA)**
**L=>ATMDS -dGPU GPU (DIS)**

### FUNCTION TABLE

| SEL | FUNCTION | OUTPUT |
|---|---|---|
| L | TMDSn+ = ATMDSn+<br>TMDSn- = ATMDSn-<br>TMDSCLK+ = ATMDSCLK+<br>TMDSCLK- = ATMDSCLK-<br>BTMDSn+ = High Impedance<br>BTMDSn- = High Impedance<br>BTMDSCLK+ = High Impedance<br>BTMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |
| H | TMDSn+ = BTMDSn+<br>TMDSn- = BTMDSn-<br>TMDSCLK+ = BTMDSCLK+<br>TMDSCLK- = BTMDSCLK-<br>ATMDSn+ = High Impedance<br>ATMDSn- = High Impedance<br>ATMDSCLK+ = High Impedance<br>ATMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |

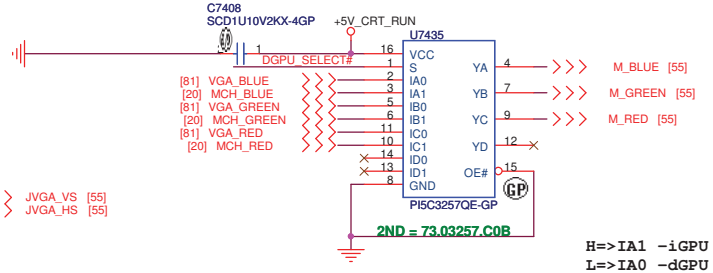
## UMA/DIS CRT Hsync/Vsync select circuit

*Hsync & Vsync level shift*





## UMA/DIS CRT signal select circuit




**H=>IA1 -iGPU PCH (UMA)**
**L=>IA0 -dGPU GPU (DIS)**

| $\overline{E}$ | S | YA | YB | YC | YD | Function |
|---|---|---|---|---|---|---|
| H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Disable |
| L | L | IA0 | IB0 | IC0 | ID0 | S = 0 |
| L | H | IA1 | IB1 | IC1 | ID1 | S = 1 |

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Title: PX Swith-1
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 74 of 88

(Blank)

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Title: (Reserve)

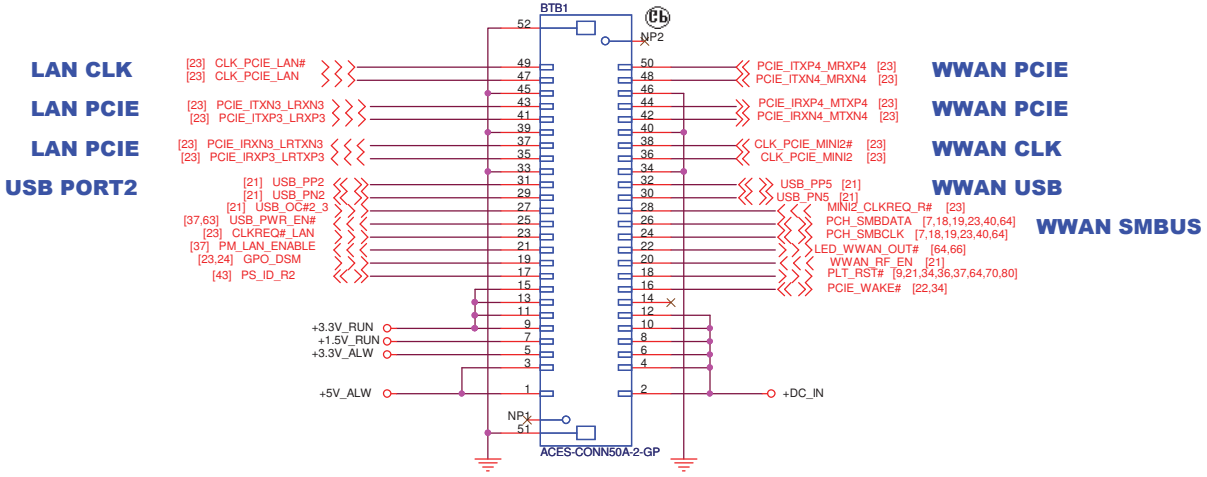
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 75 of 88

# DC_IN baord CON

| | | |
|---|---|---|
| +DC_IN | : | 19.5V/85W |
| +3.3V_RUN | : | 3300mA |
| +5V_ALW | : | 1000mA |
| +1.5V_RUN | : | 500mA |
| +3.3V_ALW | : | 58mA |

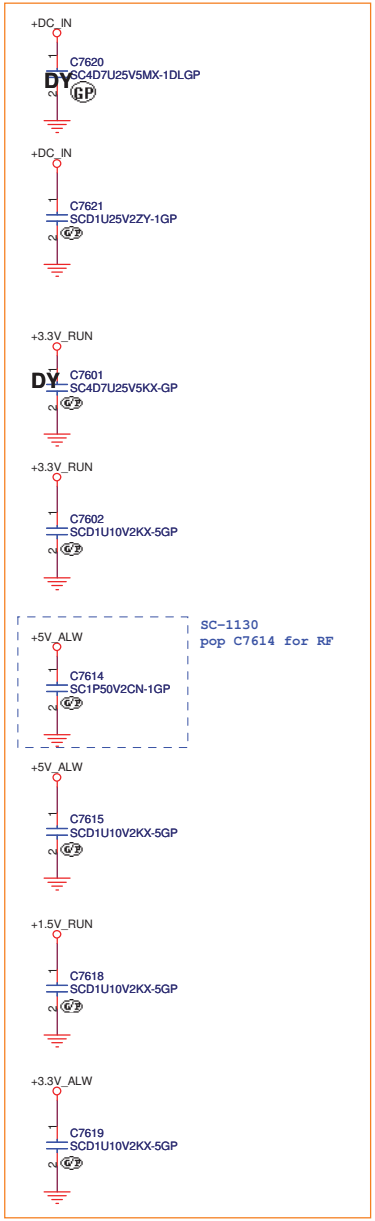
Please reoute 300 mil at least.




Remove AFTP test point
Confirmed with AFTE.

1ST: 20.F1631.050
2ND:

Place near BTB1




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC_IN Board BTB Connector
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 76 of 88

(Blank)

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Title: Audio BD/IO BD CONN

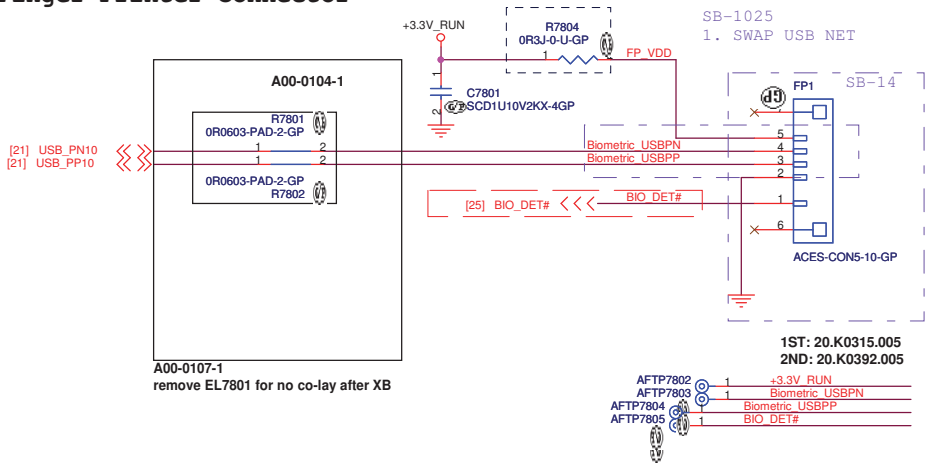
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 77 of 88

**SSID = User.Interface**

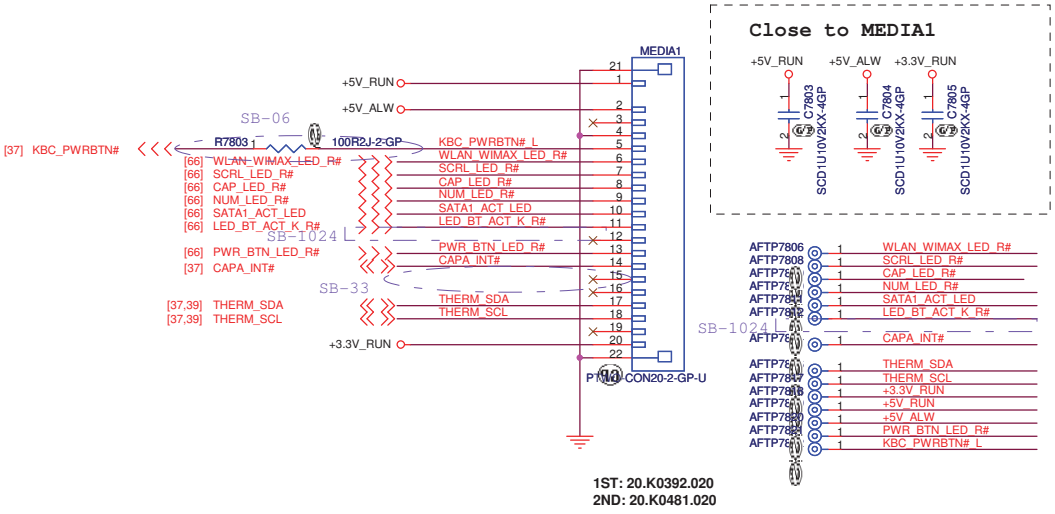
## Finger Printer Connector

A00-1223-1
1. dummy FP1 pin6, pin7 for power pin short to GND when plug in cable issue
2. add damping resister R7804




1ST: 20.K0315.005
2ND: 20.K0392.005

## LED&Capacity board CONN




1ST: 20.K0392.020
2ND: 20.K0481.020

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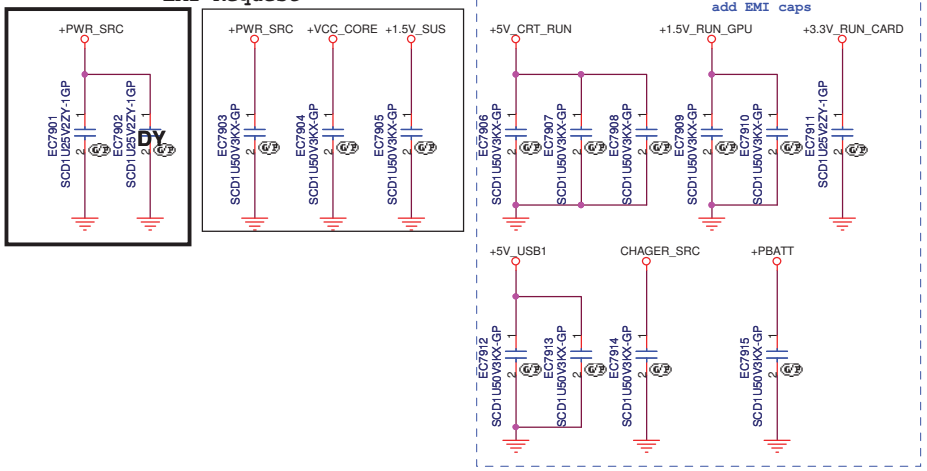
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

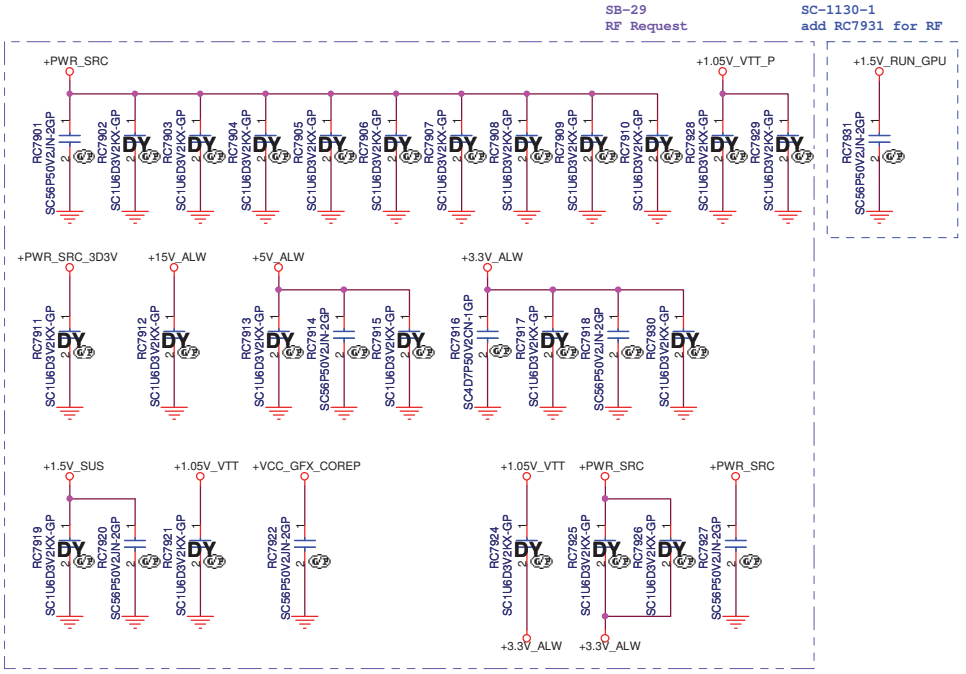
Title: *Finger Printer/Felica/Capacity*
Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*
Date: Wednesday, January 13, 2010 | Sheet 78 of 88

## SSID = EMI

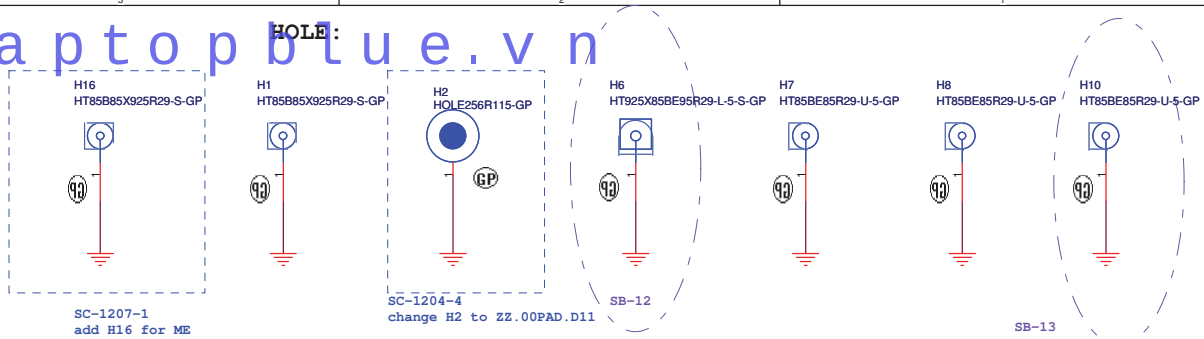
### EMI Request



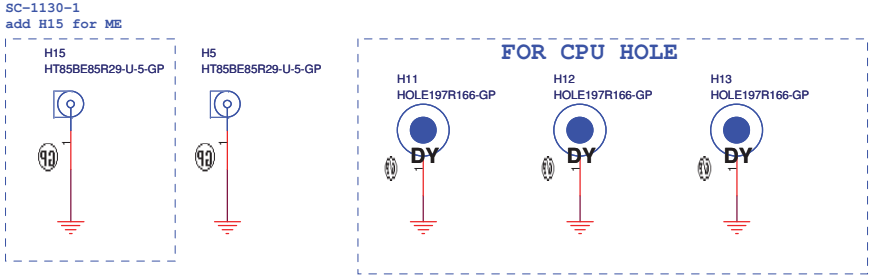

## SSID = RF

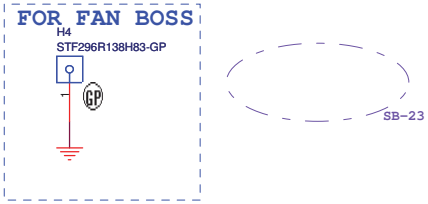


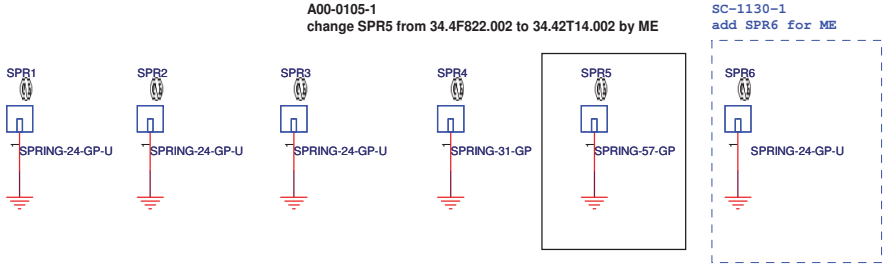

HOLE:




## SSID = Mechanical

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Title: Miscellaneous Components

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 79 of 88

SSID = VIDEO

PCIE_MTX_GRX_P[0..15] PCIE_MTX_GRX_P[0..15] [8]
PCIE_MTX_GRX_N[0..15] PCIE_MTX_GRX_N[0..15] [8]
PCIE_MRX_GTX_P[0..15] PCIE_MRX_GTX_P[0..15] [8]
PCIE_MRX_GTX_N[0..15] PCIE_MRX_GTX_N[0..15] [8]

U8001B 2 OF 7

PCIE_MTX_GRX_P0 AE12 PEX_RX0
PCIE_MTX_GRX_N0 AE12 PEX_RX0#
PCIE_MTX_GRX_P1 AG12 PEX_RX1
PCIE_MTX_GRX_N1 AG13 PEX_RX1#
PCIE_MTX_GRX_P2 AF13 PEX_RX2
PCIE_MTX_GRX_N2 AE13 PEX_RX2#
PCIE_MTX_GRX_P3 AE15 PEX_RX3
PCIE_MTX_GRX_N3 AF15 PEX_RX3#
PCIE_MTX_GRX_P4 AG15 PEX_RX4
PCIE_MTX_GRX_N4 AG16 PEX_RX4#
PCIE_MTX_GRX_P5 AF16 PEX_RX5
PCIE_MTX_GRX_N5 AE16 PEX_RX5#
PCIE_MTX_GRX_P6 AE18 PEX_RX6
PCIE_MTX_GRX_N6 AF18 PEX_RX6#
PCIE_MTX_GRX_P7 AG18 PEX_RX7
PCIE_MTX_GRX_N7 AG19 PEX_RX7#
PCIE_MTX_GRX_P8 AF19 PEX_RX8
PCIE_MTX_GRX_N8 AE19 PEX_RX8#
PCIE_MTX_GRX_P9 AE21 PEX_RX9
PCIE_MTX_GRX_N9 AF21 PEX_RX9#
PCIE_MTX_GRX_P10 AG21 PEX_RX10
PCIE_MTX_GRX_N10 AG22 PEX_RX10#
PCIE_MTX_GRX_P11 AF22 PEX_RX11
PCIE_MTX_GRX_N11 AE22 PEX_RX11#
PCIE_MTX_GRX_P12 AE24 PEX_RX12
PCIE_MTX_GRX_N12 AF24 PEX_RX12#
PCIE_MTX_GRX_P13 AG24 PEX_RX13
PCIE_MTX_GRX_N13 AF25 PEX_RX13#
PCIE_MTX_GRX_P14 AG25 PEX_RX14
PCIE_MTX_GRX_N14 AG26 PEX_RX14#
PCIE_MTX_GRX_P15 AE27 PEX_RX15
PCIE_MTX_GRX_N15 AE27 PEX_RX15#

PEX_TX0 AD10 PCIE_MRX_GTX_C_P0 C8033 2 SCD1U10V2KX-5GP PCIE_MRX_GTX_P0
PEX_TX0# AD11 PCIE_MRX_GTX_C_N0 C8034 SCD1U10V2KX-5GP PCIE_MRX_GTX_N0
PEX_TX1 AD12 PCIE_MRX_GTX_C_P1 C8035 SCD1U10V2KX-5GP PCIE_MRX_GTX_P1
PEX_TX1# AC12 PCIE_MRX_GTX_C_N1 C8036 SCD1U10V2KX-5GP PCIE_MRX_GTX_N1
PEX_TX2 AB11 PCIE_MRX_GTX_C_P2 C8037 SCD1U10V2KX-5GP PCIE_MRX_GTX_P2
PEX_TX2# AB12 PCIE_MRX_GTX_C_N2 C8038 SCD1U10V2KX-5GP PCIE_MRX_GTX_N2
PEX_TX3 AD13 PCIE_MRX_GTX_C_P3 C8039 SCD1U10V2KX-5GP PCIE_MRX_GTX_P3
PEX_TX3# AD14 PCIE_MRX_GTX_C_N3 C8040 SCD1U10V2KX-5GP PCIE_MRX_GTX_N3
PEX_TX4 AD15 PCIE_MRX_GTX_C_P4 C8042 SCD1U10V2KX-5GP PCIE_MRX_GTX_P4
PEX_TX4# AC15 PCIE_MRX_GTX_C_N4 C8043 SCD1U10V2KX-5GP PCIE_MRX_GTX_N4
PEX_TX5 AB14 PCIE_MRX_GTX_C_P5 C8044 SCD1U10V2KX-5GP PCIE_MRX_GTX_P5
PEX_TX5# AB15 PCIE_MRX_GTX_C_N5 C8045 SCD1U10V2KX-5GP PCIE_MRX_GTX_N5
PEX_TX6 AC16 PCIE_MRX_GTX_C_P6 C8047 SCD1U10V2KX-5GP PCIE_MRX_GTX_P6
PEX_TX6# AD16 PCIE_MRX_GTX_C_N6 C8048 SCD1U10V2KX-5GP PCIE_MRX_GTX_N6
PEX_TX7 AD17 PCIE_MRX_GTX_C_P7 C8050 SCD1U10V2KX-5GP PCIE_MRX_GTX_P7
PEX_TX7# AD18 PCIE_MRX_GTX_C_N7 C8051 SCD1U10V2KX-5GP PCIE_MRX_GTX_N7
PEX_TX8 AC18 PCIE_MRX_GTX_C_P8 C8052 SCD1U10V2KX-5GP PCIE_MRX_GTX_P8
PEX_TX8# AB18 PCIE_MRX_GTX_C_N8 C8053 SCD1U10V2KX-5GP PCIE_MRX_GTX_N8
PEX_TX9 AB19 PCIE_MRX_GTX_C_P9 C8054 SCD1U10V2KX-5GP PCIE_MRX_GTX_P9
PEX_TX9# AB20 PCIE_MRX_GTX_C_N9 C8055 SCD1U10V2KX-5GP PCIE_MRX_GTX_N9
PEX_TX10 AD19 PCIE_MRX_GTX_C_P10 C8056 SCD1U10V2KX-5GP PCIE_MRX_GTX_P10
PEX_TX10# AD20 PCIE_MRX_GTX_C_N10 C8057 SCD1U10V2KX-5GP PCIE_MRX_GTX_N10
PEX_TX11 AD21 PCIE_MRX_GTX_C_P11 C8058 SCD1U10V2KX-5GP PCIE_MRX_GTX_P11
PEX_TX11# AC21 PCIE_MRX_GTX_C_N11 C8077 SCD1U10V2KX-5GP PCIE_MRX_GTX_N11
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PEX_TX12# AB22 PCIE_MRX_GTX_C_N12 C8079 SCD1U10V2KX-5GP PCIE_MRX_GTX_N12
PEX_TX13 AC22 PCIE_MRX_GTX_C_P13 C8080 SCD1U10V2KX-5GP PCIE_MRX_GTX_P13
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PEX_TX14# AD24 PCIE_MRX_GTX_C_N14 C8083 SCD1U10V2KX-5GP PCIE_MRX_GTX_N14
PEX_TX15 AE25 PCIE_MRX_GTX_C_P15 C8084 SCD1U10V2KX-5GP PCIE_MRX_GTX_P15
PEX_TX15# AE26 PCIE_MRX_GTX_C_N15 C8085 SCD1U10V2KX-5GP PCIE_MRX_GTX_N15

PEX_IOVDDQ AB13 PEX_IOVDD AC9
PEX_IOVDDQ AB16 PEX_IOVDD AD7
PEX_IOVDDQ AB17 PEX_IOVDD AD8
PEX_IOVDDQ AB7 PEX_IOVDD AE7
PEX_IOVDDQ AB8 PEX_IOVDD AF7
PEX_IOVDDQ AB9 PEX_IOVDD AG7
PEX_IOVDDQ AC13
PEX_IOVDDQ AC7
PEX_IOVDDQ AD6
PEX_IOVDDQ AE6
PEX_IOVDDQ AF6
PEX_IOVDDQ AG6

PEX_REFCLK AB10 CLK_PCIE_VGA CLK_PCIE_VGA [23]
PEX_REFCLK# AC10 CLK_PCIE_VGA# CLK_PCIE_VGA# [23]
PEX_TSTCLK_OUT AF10 PEX_TEST_PLL_CLK_OUT
PEX_TSTCLK_OUT# AE10 PEX_TEST_PLL_CLK_OUT# 200R2F-L-GP DY 1 R8002
PEX_CLKREQ# AE9 PEX_CLKREQ#
PEX_RST# AD9 PEX_RST#
PEX_SVDD_3V3 AG9
PEX_TERMP AG10 PEX_TERMP 1 R8001 2K49R2F-GP
PEX_PLLVDD AF9 +PEX_PLLVDD
PLLVDD K5 +GPU_PLLVDD

GT218-ES-S-A1-GP

+1.05V_GFX_PCIE
SC22U6D3V5MX-2GP C8089
SC10U6D3V5KX-1GP C8074
SC4D7U6D3V3KX-GP C8064
SC1U10V2KX-1GP C8067
SC1U6D3V2KX-GP C8068
Place near GPU

SCD1U16V2KX-3GP C8066
SCD1U16V2KX-3GP C8065
Place under GPU

Revised decoupling C 2009/05/28

Place under GPU
SCD1U16V2KX-3GP C8059
SCD1U16V2KX-3GP C8060
Place near GPU
+1.05V_GFX_PCIE
SC1U6D3V2KX-GP C8063
SC1U6D3V2KX-GP C8062
SC1U10V3KX-3GP C8061
SC10U6D3V5KX-1GP C8073
SC10U6D3V5KX-1GP C8041
Revised decoupling C 2009/05/28

+3.3V_RUN_GPU
R8004 10KR2J-3-GP
Change R8004 resistor value 2009/06/05

+3.3V_RUN_GPU
SCD1U10V2KX-4GP C8049
Place under GPU
Remove 0.01u capacity C8039 2009/05/28

DW
07/10 NO STUFF
1. R8002 made NO STUFF

Change power rail 2009/05/26

+PEX_PLLVDD PEX_PLLVDD = 120mA
SCD1U16V2KX-3GP C8087
SC1U10V2KX-1GP C8070
SC4D7U6D3V3KX-GP C8046
L8011 IND-D1UH-20-GP 100NH 0603 DCR= 0.13 ohm
+1.05V_GFX_PCIE
NV suggestion. Place near GPU
Revised decoupling C 2009/05/28

Place under GPU
+GPU_PLLVDD (Pre pin)
SCD1U16V2KX-3GP C8071
SCD1U16V2KX-3GP C8072
Revised decoupling C 2009/05/28

Place near GPU SB-30
+1.05V_GFX_PCIE
L8005 BLM18SG121TN1D-GP I SP_PLLVDD=45mA
SC1U10V2KX-1GP C8076
SC4D7U6D3V3KX-GP C8075

[25] DGPU_HOLD_RST#
[9,21,34,36,37,64,70,76] PLT_RST#
R8039 0R2J-2-GP
PLT_RST# RC
DY C8086 SC1U6D3V2KX-GP
R8017 100KR2J-1-GP
U8028 74LVC1G08GW-1-GP
+3.3V_RUN
PEX_RST#
R8016 100KR2J-1-GP

DW
07/10 Change
1. Change U8028 from Operating voltage Range 5 to 3 V . Add
2.Added Pull-down resistors on GPU Reset [PEX_REST#] Pin

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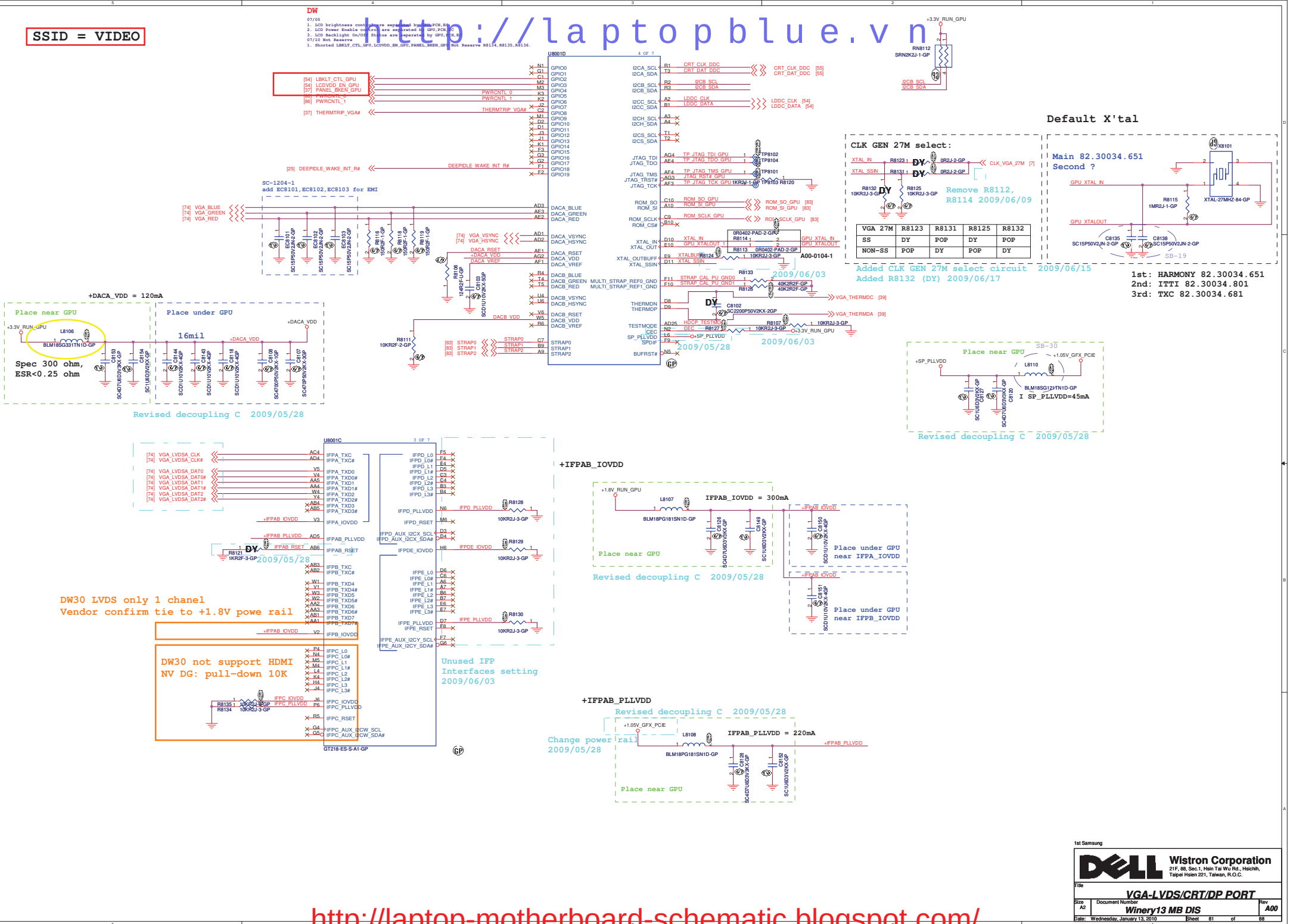
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)
Size: A3 Document Number: Winery13 MB DIS Rev: A00
Date: Wednesday, January 13, 2010 Sheet 80 of 88

SSID = VIDEO

DW
07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/10 Not Reserve
1. Shorted LBKLT_CTL_GPU,LCDVDD_EN_GPU,PANEL_BKEN_GPU Not Reserve R8114,R8135,R8136.

























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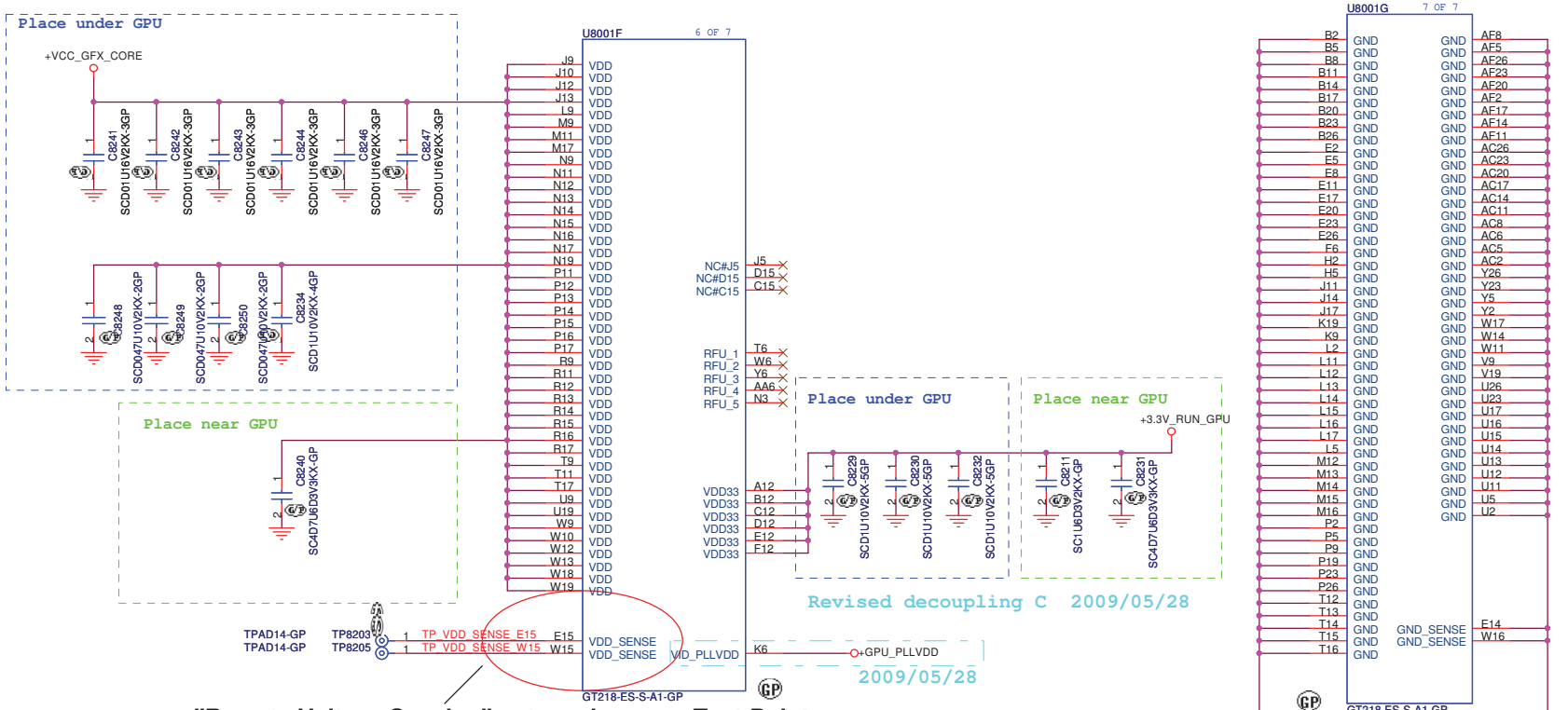
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-LVDS/CRT/DP PORT
Size: A2 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 81 of 88

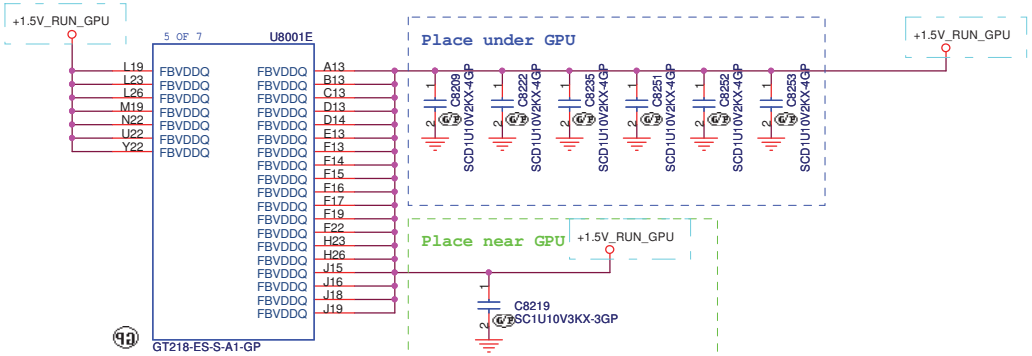
Revised decoupling C 2009/05/28




"Remote Voltage Sensing" not used,reserve Test-Point.

Change FBVDDQ power rail
2009/05/28

FBVDD/Q = 2.24A




Revised decoupling C 2009/05/28



1st Samsung

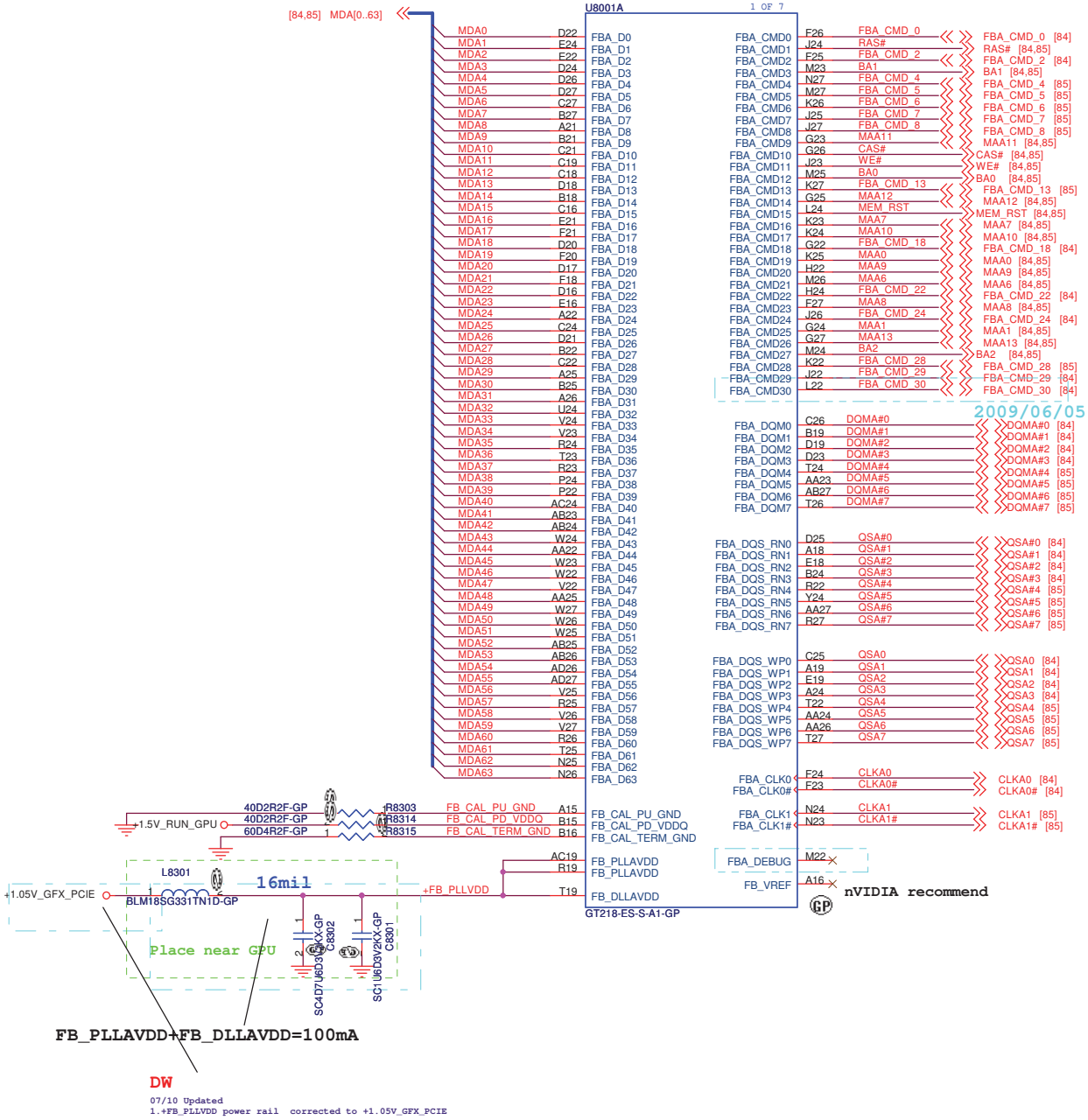
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

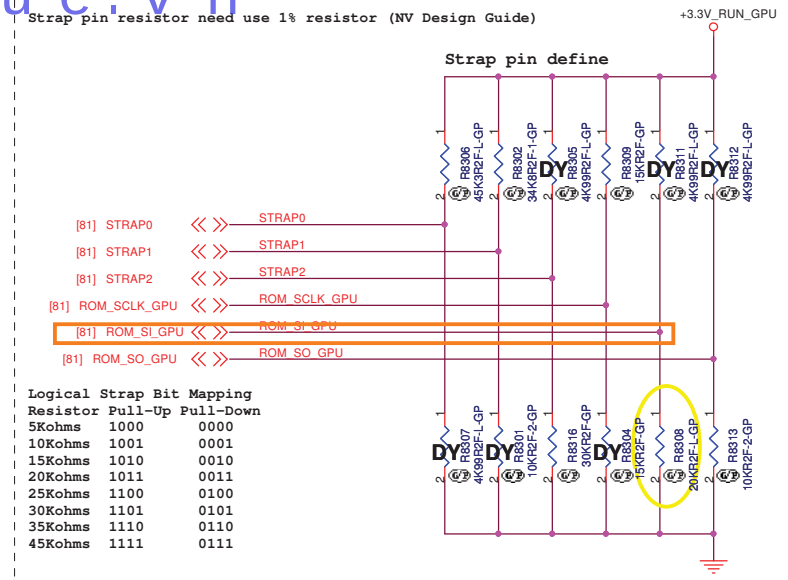
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 82 of 88

**SSID = VIDEO**




Strap pin resistor need use 1% resistor (NV Design Guide)




Logical Strap Bit Mapping

| Resistor | Pull-Up | Pull-Down |
|---|---|---|
| 5Kohms | 1000 | 0000 |
| 10Kohms | 1001 | 0001 |
| 15Kohms | 1010 | 0010 |
| 20Kohms | 1011 | 0011 |
| 25Kohms | 1100 | 0100 |
| 30Kohms | 1101 | 0101 |
| 35Kohms | 1110 | 0110 |
| 45Kohms | 1111 | 0111 |

| Strap0 | | Strap1 | | Strap2 | |
|---|---|---|---|---|---|
| USER_BIT0 | 1 | 3GIO_PADCFG_LUT_ADR0 | 0 | PCI_DEVID_0 | 1 |
| USER_BIT1 | 1 | 3GIO_PADCFG_LUT_ADR1 | 1 | PCI_DEVID_1 | 0 |
| USER_BIT2 | 1 | 3GIO_PADCFG_LUT_ADR2 | 1 | PCI_DEVID_2 | 1 |
| USER_BIT3 | 1 | 3GIO_PADCFG_LUT_ADR3 | 1 | PCI_DEVID_3 | 0 |
| EDID is used | | Reserved | | N11M-GE1 GPU Device ID=0x0A75 | |

| ROM_SI_GPU | | ROM_SO_GPU | | ROM_SCLK_GPU | |
|---|---|---|---|---|---|
| RAM_CFG0 | | VGA_DEVICE | 1 | PEX_PLL_EN_TERM | 0 |
| RAM_CFG1 | | SMB_ALT_ADDR | 0 | SLOT_CLK_CONFIG | 1 |
| RAM_CFG2 | | FB_0_BAR_SIZE | 0 | SUB_VENDOR | 0 |
| RAM_CFG3 | | XCLK_417 | 0 | PCI_DEVID_4 | 1 |

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)
If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K.

| RAM_CFG[3:0] | Config | FB_BUS Width | Definitions |
|---|---|---|---|
| 0000 | | | |
| 0001 | | | |
| 0010 | 64MX16 | DDR3 64Bit | Hynix |
| 0011 | 64MX16 | DDR3 64Bit | Samsung |
| 0100 | | | Default |
| 0101 | | | |
| 0110 | | | |
| 0111 | | | |

| SUB_VENDOR | | XCLK_417 | | PEX_PLL_EN_TERM | |
|---|---|---|---|---|---|
| 0 | No VBIOS ROM | 0 | 277MHz(POR) | 0 | Disable (POR) |
| 1 | BIOS ROM present | 1 | Reserved | 1 | Enable |

| 3GIO_PADCFG | USER[3:0] |
|---|---|
| 0000 | Desktop |
| 1110 | Notebook (POR) |

1111 Use EDID to detect panel settings

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

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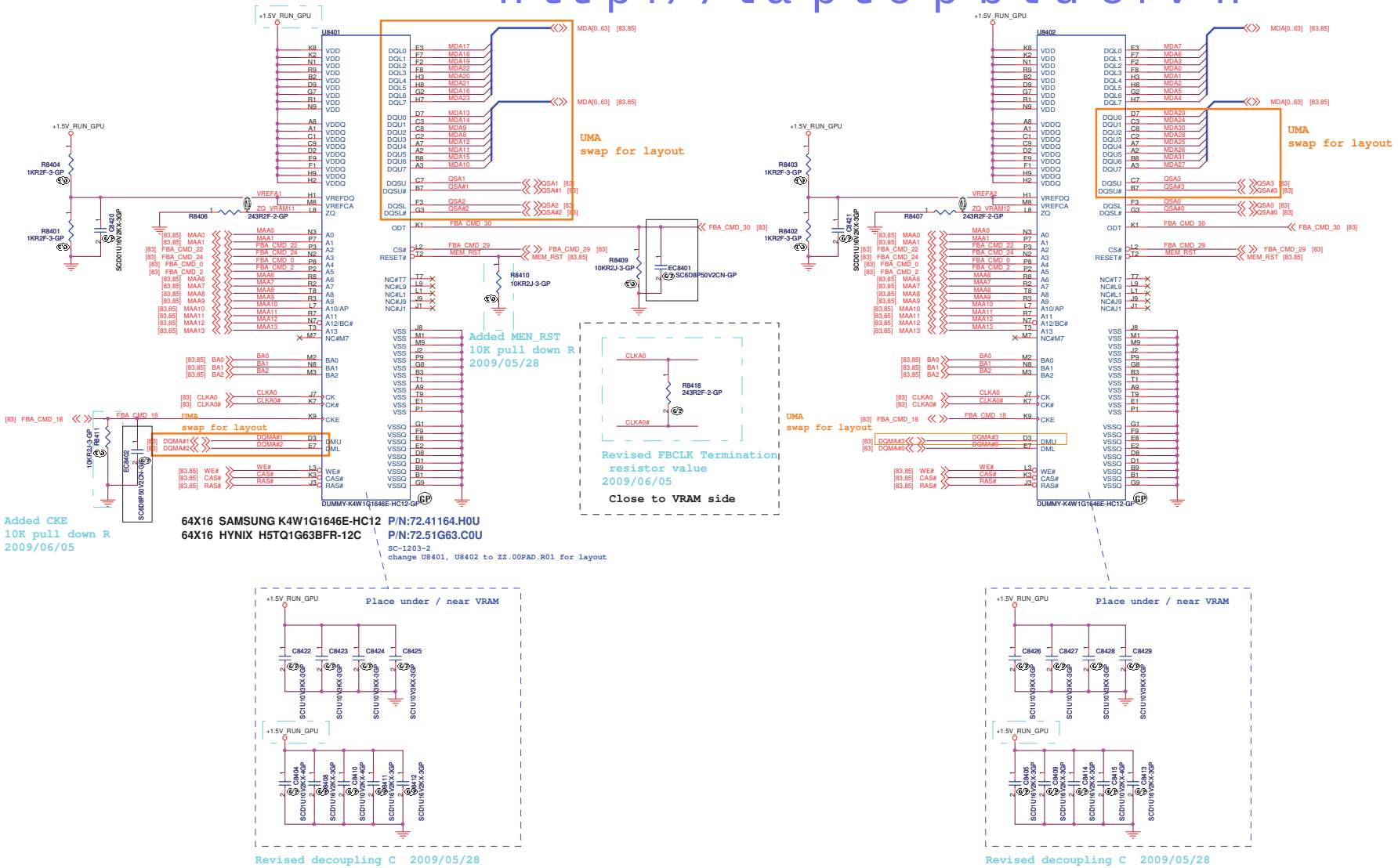
Title: VGA-MEMORY/STRAPS(4/4)
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 83 of 88

SSID = VIDEO



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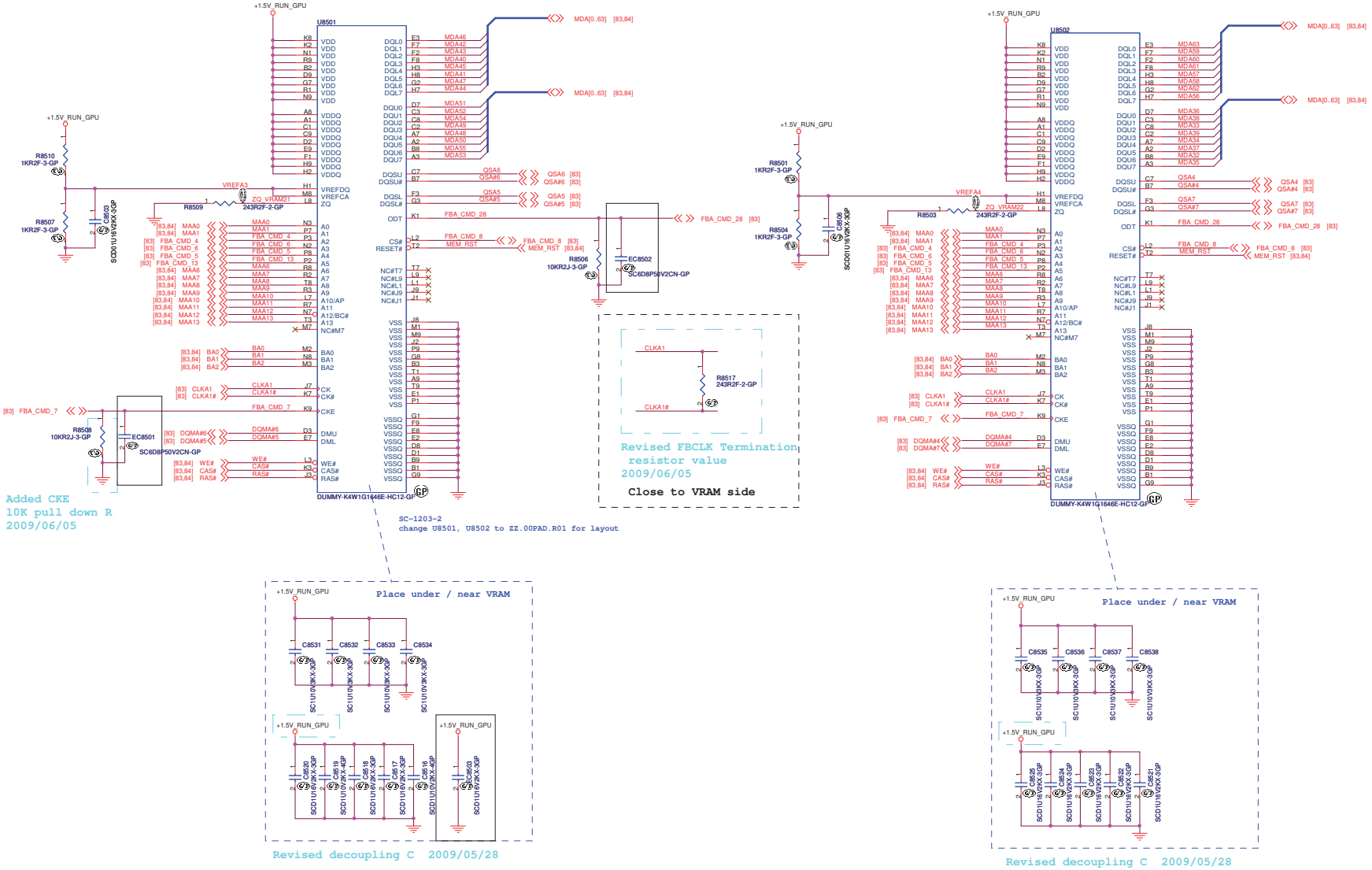
Title: VRAM(1/2)

| Size | Document Number | Rev |
|---|---|---|
| A2 | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 84 of 88

SSID = VIDEO




Added CKE
10K pull down R
2009/06/05

Revised FBCLK Termination
resistor value
2009/06/05
Close to VRAM side

SC-1203-2
change U8501, U8502 to ZZ.00PAD.R01 for layout




Revised decoupling C 2009/05/28




Revised decoupling C 2009/05/28

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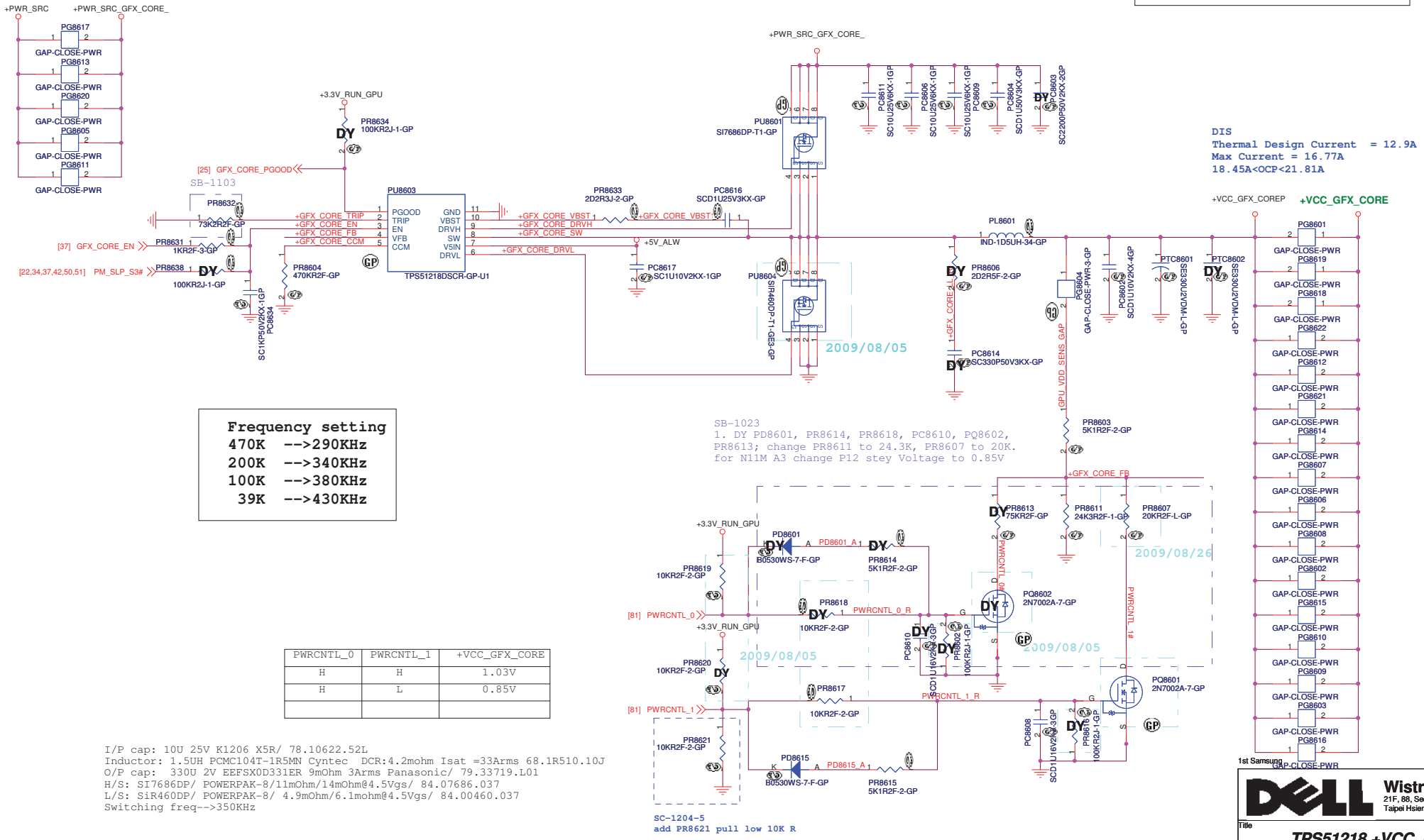
Title: VRAM

| Size | Document Number | Rev |
|---|---|---|
| A2 | Winery13 MB DIS | A00 |

Date: Wednesday, January 13, 2010 Sheet 85 of 88

SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2




**Frequency setting**

| | |
|---|---|
| 470K | -->290KHz |
| 200K | -->340KHz |
| 100K | -->380KHz |
| 39K | -->430KHz |

| PWRCNTL_0 | PWRCNTL_1 | +VCC_GFX_CORE |
|---|---|---|
| H | H | 1.03V |
| H | L | 0.85V |
| | | |

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

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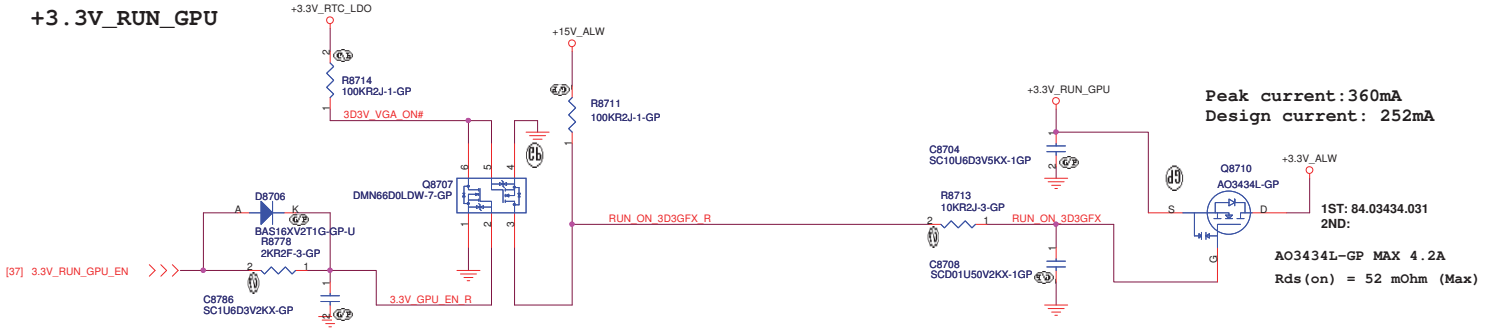
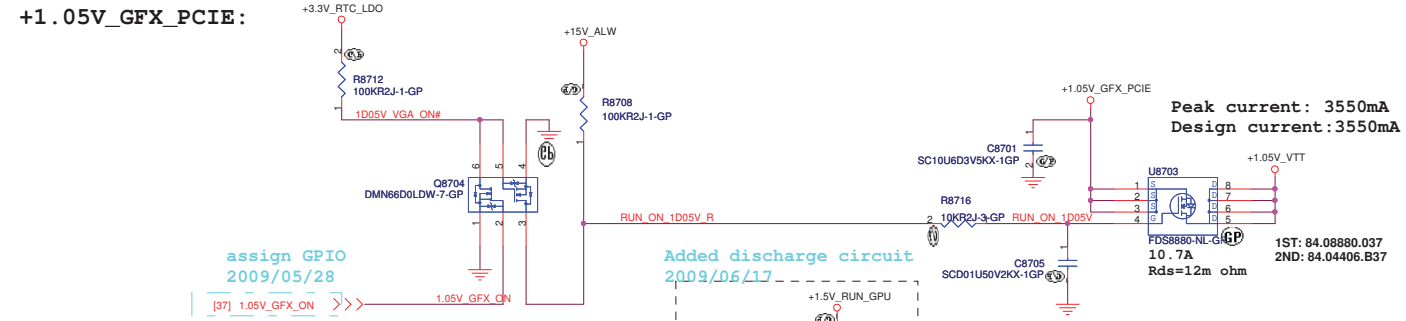
Title: TPS51218 +VCC_GFX_CORE
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 86 of 88

**SSID = VIDEO**

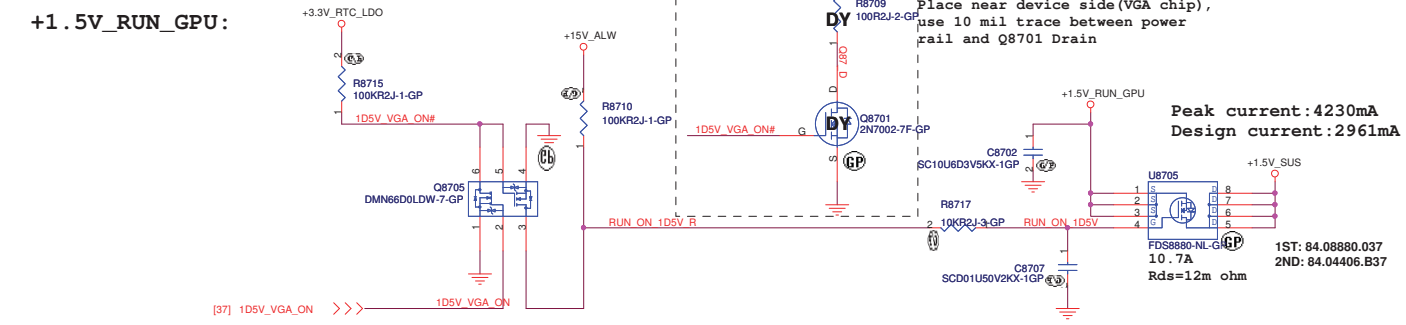
## +3.3V_RUN_GPU




## +1.05V_GFX_PCIE:




## +1.5V_RUN_GPU:

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| | | |
|---|---|---|
| Title: LDO 1.8V | | |
| Size: Custom | Document Number: Winery13 MB DIS | Rev: A00 |
| Date: Wednesday, January 13, 2010 | Sheet 87 of 88 | |

| Item | Page# | Date | Request By | Issue description | Solution Description | Rev. |
|---|---|---|---|---|---|---|
| 01 | 66 | 2009/10/08 | EE | HDD LED light in S5. | Change HDD LED power rail from +5V_ALW to +5V_RUN. | SB |
| 02 | 60 | 2009/10/08 | EE | External MIC NG. | Add caps C6014 C6015. | SB |
| 03 | 66 | 2009/10/08 | EE | Correct battery LED color. | Swap LED6601 pin2 & pin3. | SB |
| 04 | 49 | 2009/10/08 | EE | Improve VTT_PWRGD ramp up signal. | Dummy C4912. | SB |
| 05 | 51 | 2009/10/08 | EE | Fine tune +1.8V_RUN power on sequence behind +3.3V_RUN. | Change PR5102 from 2.2K to 3K and PC5105 from 4700pF to 1uF. | SB |
| 06 | 54,78 | 2009/10/08 | EE | For KBC ESD protect. | Add 100 ohm resistances R5413, R7803. | SB |
| 07 | | | | | | |
| 08 | 30 | 2009/10/08 | EE | | Change CODEC to 92HD79. | SB |
| 09 | 64 | 2009/10/08 | EE | By ME request | Change WLAN1 to 62.10043.841. | SB |
| 10 | | | | | | |
| 11 | 37 | 2009/10/09 | EE | Change board ID. | Dummy R3708 and pop R3701. | SB |
| 12 | 79 | 2009/10/12 | ME | By ME request | Change H6 to ZZ.00PAD.F91 | SB |
| 13 | 79 | 2009/10/12 | ME | By ME request | Change H10 to ZZ.00PAD.D41 | SB |
| 14 | 78 | 2009/10/12 | ME | By ME request | Change FP1 to 20.K0315.005 | SB |
| 15 | 27 | 2009/10/12 | EE | Follow Intel spec | Remove L2701, C2701, C2702; Add TP2701 | SB |
| 16 | 27 | 2009/10/12 | EE | Follow Intel spec | Remove L2704, C2721, C2722; Add TP2702 | SB |
| 17 | 27 | 2009/10/12 | EE | Cost down | Change L2702, L2703 to 68.10050.10Y | SB |
| 18 | 24 | 2009/10/12 | EE | XTAL Load Capacitance as Vendor suggestion | Change C2402, C2403 to 12pF | SB |
| 19 | 81 | 2009/10/12 | EE | XTAL Load Capacitance as Vendor suggestion | Change C8135, C8138 to 15pF | SB |
| 20 | 26 | 2009/10/13 | EE | Follow Intel spec | Remove L2602, C2616; Add TP2601 | SB |
| 21 | 26 | 2009/10/13 | EE | Follow Intel spec | Remove L2601, C2606; Add TP2602 | SB |
| 22 | 37 | 2009/10/13 | EE | Modify 10mW schematic | | SB |
| 23 | 79 | 2009/10/13 | ME | By ME request | Remove H9 (BT BOSS) | SB |
| 24 | 49 | 2009/10/13 | EE | By PSE request | Change pg4910~pg4918 and pg4921 close gap to mask type | SB |
| 25 | 73 | 2009/10/13 | EE | Two AFTP for +3.3V_RUN | Remove AFTP6030 | SB |
| 26 | 34 | 2009/10/14 | ME | By ME request | change NEW1 connector to 20.K0370.026 | SB |
| 27 | 79 | 2009/10/14 | ME | By ME request | change SPR5 to 34.4F822.002 | SB |
| 28 | 64 | 2009/10/14 | EE | By AFTE request | Add AFTP6402, AFTP6403 | SB |
| 29 | 79 | 2009/10/16 | EE | By RF request | Add Cross Moat Caps | SB |
| 30 | 80,81 | 2009/10/16 | EE | Voltage Drop over 3% | change bead value to 120 ohm DCR 0.55 ohm | SB |
| 31 | 22 | 2009/10/16 | EE | RTC data loss | Added 3v/5v S5 power good to control resume reset sequence prevent RTC data loss | SB |
| 32 | 25 | 2009/10/16 | EE | | Swapped Q2515 C,E Pin | SB |
| 33 | 78 | 2009/10/16 | EE | | remove CAPA_RST# from capacity board | SB |
| 34 | 37 | 2009/10/16 | EE | By SW request | Added Switch Baord Detection circuit | SB |

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Title: Change List(1/3)

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| Item | Page# | Date | Request By | Issue description | Solution Description | Rev. |
|---|---|---|---|---|---|---|
| 01 | 37 | 2009/11/18 | EE | Correct R3745 power rail to KBC_PWR | Change R3745 power rail to KBC_PWR | SC |
| 02 | 36 | 2009/11/25 | EE | TPM connector needn't AFTE test point | Remove TPM1 AFTP | SC |
| 03 | 23 | 2009/11/25 | EE | No support HDMI and eDP so needn't pop 25MHz Xtal of PCH. | C2313 pop 0 ohm if no use 25MHz XTAL | SC |
| 04 | 37 | 2009/11/25 | EE | Toggle VGA mode will flicker white screen in hybrid mode. | Add U3703 mux for panel backlight enable signal select | SC |
| 05 | 54 | 2009/11/25 | EE | Toggle VGA mode will flicker white screen in hybrid mode. | Add mux U5446 to select LCDVDD enable signal | SC |
| 06 | 7 | 2009/11/30 | RF | For solve WiMAX noise | Change C701 to 4.7pF for RF | SC |
| 07 | 43 | 2009/11/30 | RF | For solve WiMAX noise | Pop PC4303 for RF | SC |
| 08 | 46 | 2009/11/30 | RF | For solve WiMAX noise | Change PC4601 pull up to +5V_ALW for layout. | SC |
| 09 | 47 | 2009/11/30 | EE | For combine material item | Change PC4762 to 0603 size | SC |
| 10 | 79 | 2009/11/30 | ME | For one hand hold issue, ODD have noise | Add H15 for ME | SC |
| 11 | 79 | 2009/11/30 | RF | For solve WWAN noise | Add RC7931 for RF | SC |
| 12 | 79 | 2009/11/30 | RF | For solve WiMAX noise | Add SPR6 for RF | SC |
| 13 | 55 | 2009/12/04 | EMI | By EMI requirement | Change L5501,L5502,L5503 for EMI | SC |
| 14 | 79 | 2009/12/04 | EMI | By EMI requirement | Add EMI caps | SC |
| 15 | 81 | 2009/12/04 | EMI | By EMI requirement | Add EC8101,EC8102,EC8103 for EMI | SC |
| 16 | 47 | 2009/12/04 | ME | For cosmatic issue when insert 8 cell battery | Remove TC4701 for layout | SC |
| 17 | 79 | 2009/12/04 | ME | For cosmatic issue when insert 8 cell battery | Change H2 to ZZ.00PAD.D11 | SC |
| 18 | 30 | 2009/12/04 | EE | Base on Application Note: IDT 92H81/79 AUX Mode as input of Diagnostic sound. | Connect U3001 pin17, pin18 to pin12 net and change R3016 to 120K for vendor request | SC |
| 19 | 86 | 2009/12/04 | EE | Set PWRCNTL_1 for default low. | Add PR8621 pull low 10K ohm | SC |
| 20 | 12 | 2009/12/07 | EMI | By EMI requirement | Pop C1243 and change size to 0603 for EMI | SC |
| 21 | 33 | 2009/12/07 | EMI | By EMI requirement | Pop C3301, EC3302, EC3303, EC3305, EC3306, EC3307, EC3308 and change from 100p to 6.8p for EMI | SC |
| 22 | 54 | 2009/12/07 | EMI | By EMI requirement | Pop EC5403 for EMI | SC |
| 23 | 60 | 2009/12/07 | EMI | By EMI requirement | Pop EC6001 and EC6002 for EMI | SC |
| 24 | 63 | 2009/12/07 | EMI | By EMI requirement | Pop R6307 for EMI | SC |
| 25 | 79 | 2009/12/07 | ME | For cosmatic issue when insert 8 cell battery | Add H16 for ME | SC |
| 26 | 24 | 2009/12/08 | EE | Base on EA teset result, change to 0 ohm. | Change R2413,R2414,R2415 from 15ohm to 0 ohm | SC |
| 27 | 53 | 2009/12/08 | EE | Base on ARD_Sightings_Report_18 #3622146 | Change PR5311 from 4.7K to 470 ohm | SC |
| 28 | 60 | 2009/12/08 | EE | Audio AP LO THD+N fail | Change EC6004,EC6005 from 0.1U to 0.01U | SC |
| 29 | 62 | 2009/12/08 | EE | Base on EA teset result, change to 0 ohm. | Change R6206 from 15ohm to 0 ohm | SC |
| 30 | 68 | 2009/12/08 | EE | Change PCB Footprint | Change Q6808 to 84.06402.B3D | SC |
| 31 | 73 | 2009/12/08 | EMI | By EMI requirement | Pop L7301 for EMI | SC |

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Title: Change List(2/3)

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

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| Item | Page# | Date | Request By | Issue description | Solution Description | Rev. |
|---|---|---|---|---|---|---|
| 01 | 34 | 2010/01/07 | EE | For no co-lay after XB | remove R3402, R3403 | A00 |
| 02 | 37 | 2010/01/05 | EE | Prevent SPI ROM data lost | Add reset IC U3704 | A00 |
| 03 | 46 | 2009/12/18 | EE | By POWER requirement | changePL4602 from 2.2U to 3.3U | A00 |
| 04 | 46 | 2009/12/18 | EE | TO improve +15V_Pump Power on issue | pop PR4619; dummy PR4618 | A00 |
| 05 | 51 | 2010/01/07 | EE | To prevent PM_SLP_S3# signal rebound | change R5102 to short pad, PC5105 to 10K | A00 |
| 06 | 52 | 2009/12/23 | EE | PREVNET MOS DEMAGE | Change C701 to 4.7pF for RF | A00 |
| 07 | 53 | 2009/12/18 | EE | By POWER requirement | change PR5314 from 5.9K to 6.2K | A00 |
| 08 | 55 | 2009/12/18 | EMI | By EMI requirement | change L5501, L5502, L5503 to 0R | A00 |
| 09 | 55 | 2009/12/18 | EMI | By EMI requirement | change R5504, R5505, R5506 from 0R to 33R | A00 |
| 10 | 55 | 2009/12/18 | EMI | By EMI requirement | change C5520 from 22p to 10p | A00 |
| 11 | 55 | 2010/01/04 | ME | By ME requirement | change CRT1 from 20.20431.015 to 20.20401.015 | A00 |
| 12 | 62 | 2010/01/04 | ME | By ME requirement | change RCT1 from 20.D0210.102 to 20.D0075.102 | A00 |
| 13 | 63 | 2010/01/06 | EE | For no co-lay after XB | remove R6302, R6308,TR6301,TR6302, TR6303 | A00 |
| 14 | 64 | 2010/01/07 | EE | For no co-lay after XB | remove L6401 | A00 |
| 15 | 73 | 2010/01/07 | EE | For no co-lay after XB | remove R7302, R7303 | A00 |
| 16 | 78 | 2009/12/23 | EE | TO PREVENT power pin short to GND when plug in cable | dummy FP1 pin6, pin7 | A00 |
| 17 | 78 | 2009/12/23 | EE | add damping resister R7804 | add R7804 | A00 |
| 18 | 79 | 2010/01/05 | ME | By ME requirement | change SPR5 from 34.4F822.002 to 34.42T14.002 | A00 |

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Title: Change List(3/3)

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 88 of 88