Intel Calpella BIOCK DIAGRAM

Intel Calpella Arrandale UMA

01

POWER

SYSTEM RESET CIRCUIT

BATT CHARGER

AC/BATT CONNECTOR

RUN POWER SW

+3V_S5/+5V_S5

+3V_SUS/+5V_SUS

+5V_RUN/+3V_RUN/+1.8V_RUN

FAN & THERMAL

CLOCK
SLG8SP585VTR
(QFN-32)

POWER

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT

+1.05V_PCH

+1.05V_VTT

CPU VR

DC/DC
+3VPCU/+5VPCU/

CPU
Arrandale 35W
37.5mm X 37.5mm
(rPGA 989)

DDR3-SODIMM1 CHA

DDR3-SODIMM2 CHB

Dual Channel DDR3
1066 1.5V

FDI

DMI X 4

PCH
82801IBM
(HM55)
27mm X 25mm

SATA-ODD

SATA

SATA-HDD

SATA

IHDA

AUDIO/AMP
ALC269

Audio SPK conn

Audio Jacks

LPC

EC
ITE8502

18X8

Keyboard

SPI

FLASH 2Mbyts

SPI

PS/2

FLASH 2Mbyts

Touchpad

HDMI

LVDS

VGA

USB2.0 x 3

PCIEx1

PCIEx1

PCIEx1

PCIEx1

SPI

PS8101

HDMI

Panel Connector

CRT CONN.

USB conn x 3

Card Reader SD MS CARD
RTS5159

GLAN 10/100/1000 LAN
Realtek RTL8111E-GR

MINI-CARD
WLAN

NEW CARD

W83L351YG

MINI-CARD
3G

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PROJECT : FH2

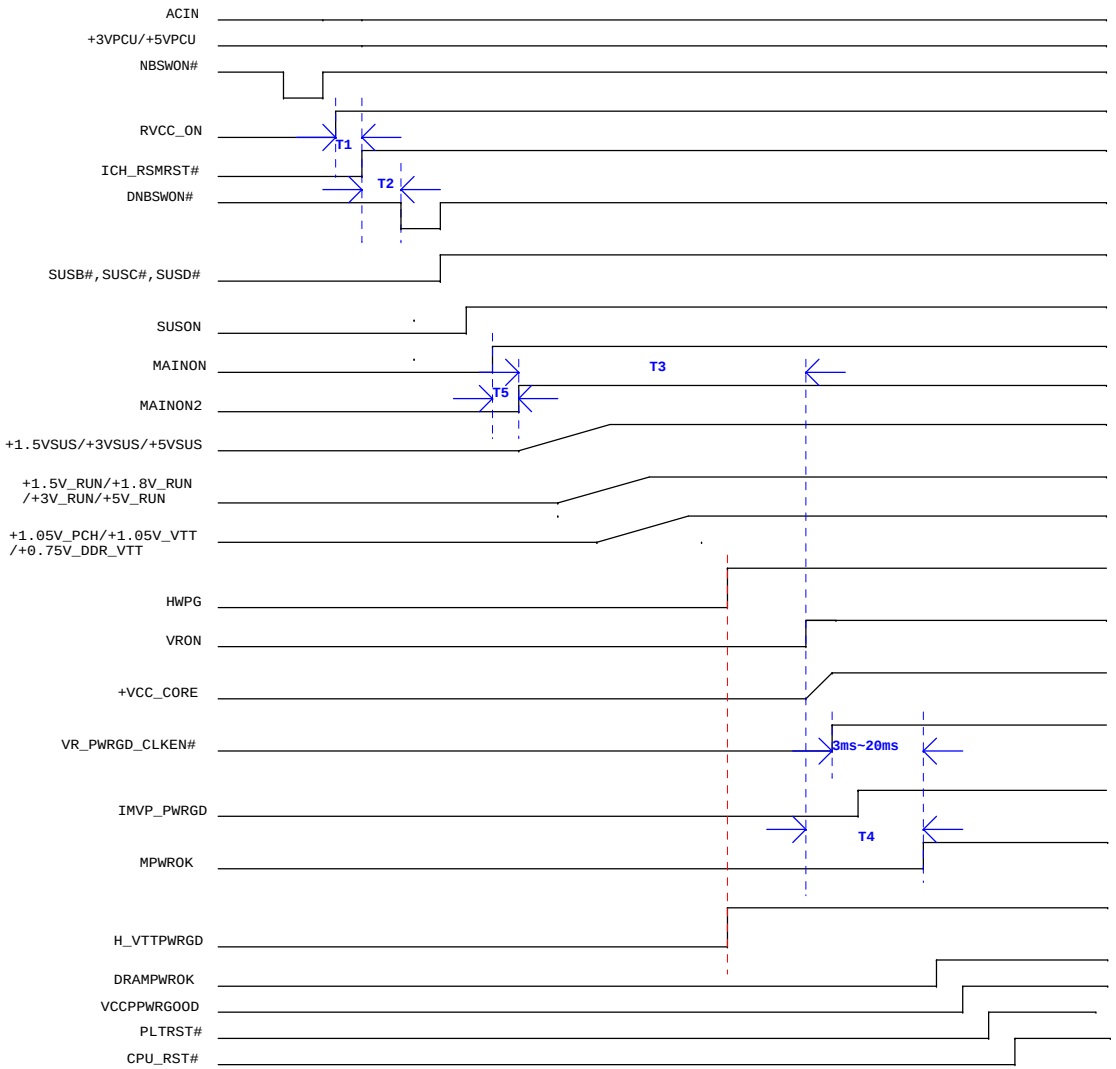
Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, December 21, 2009 Sheet 1 of 38

02

Table of Contents

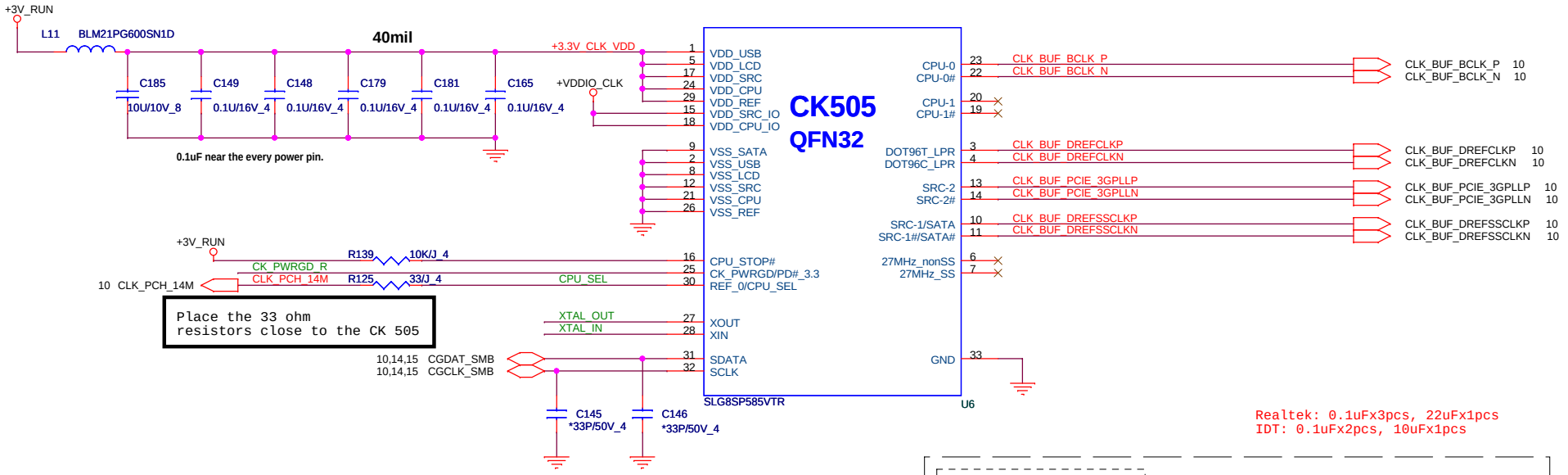
Power Sequence

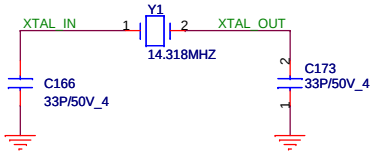


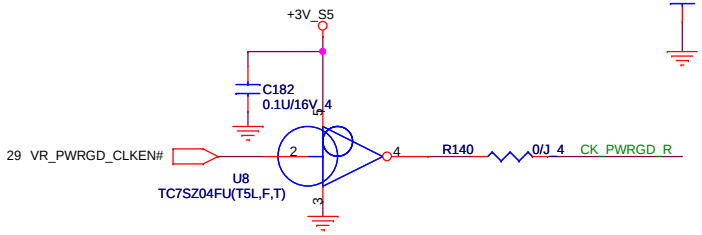
T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to MAINON2 =500us

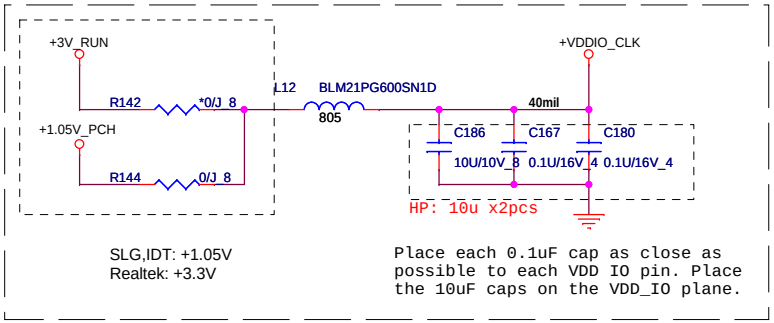
Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	Frontpage	1A
Date: Monday, December 21, 2009	Sheet 2 of 38	

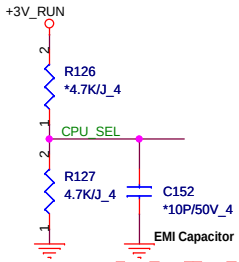








+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

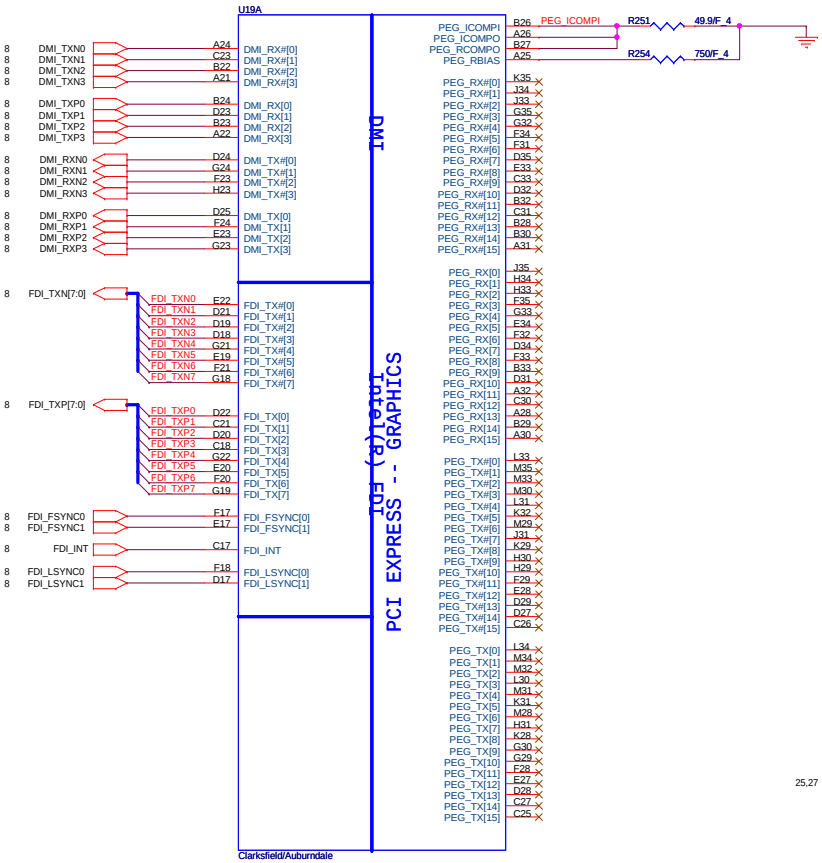


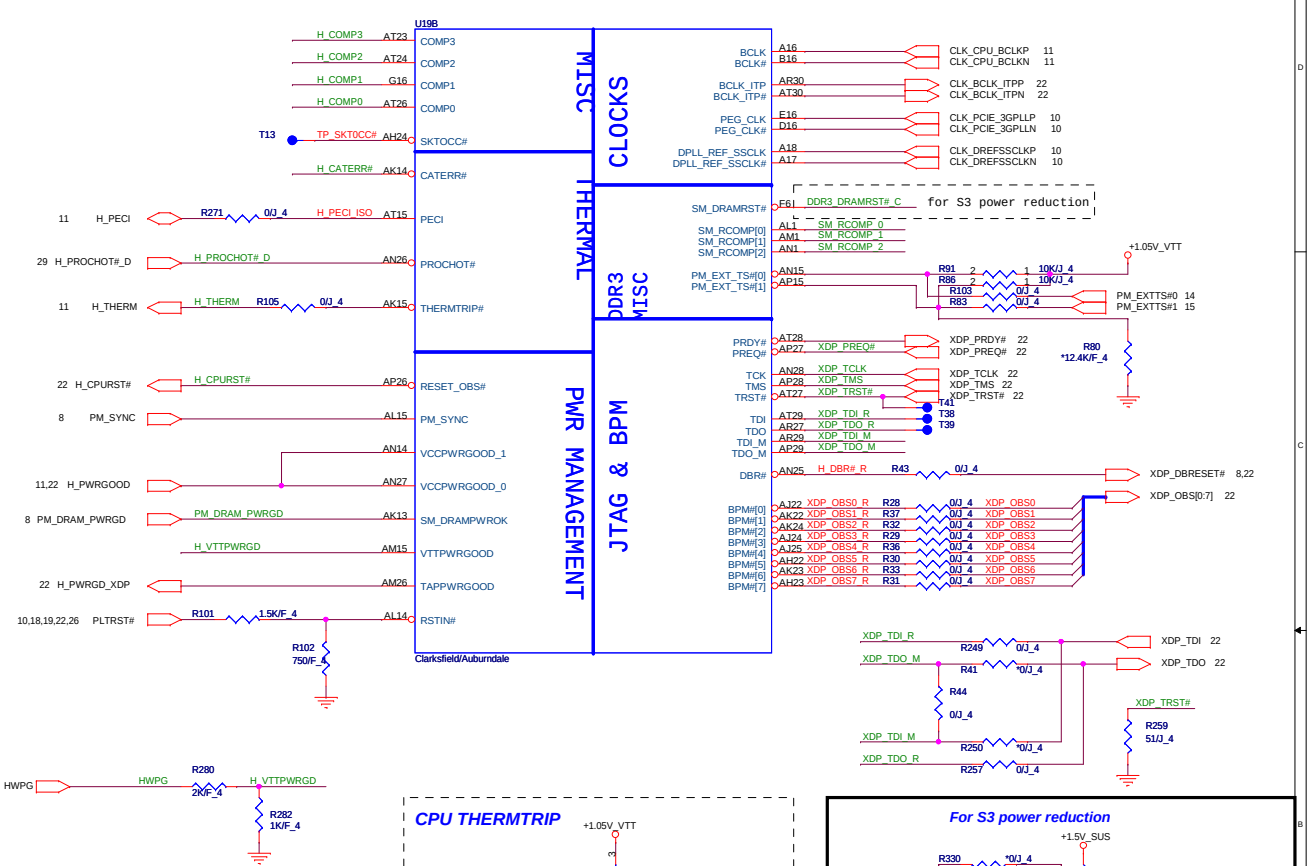
PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

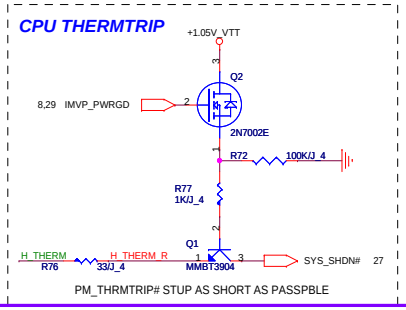
CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

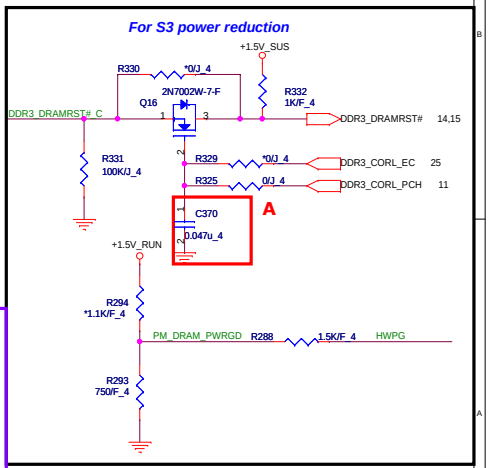
Quanta Computer Inc.
PROJECT : FH2

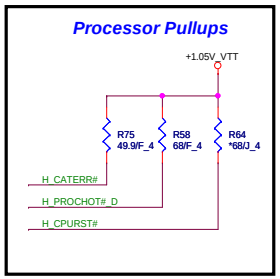
Size	Document Number	Rev
	Clock Generator	1A
Date: Monday, December 21, 2009	Sheet 3 of 38	

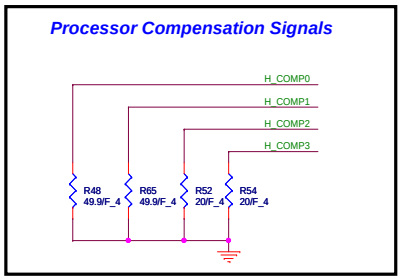


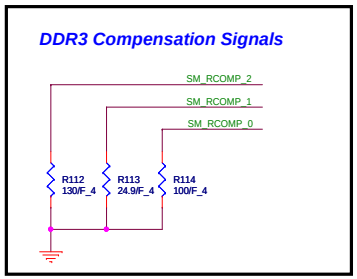


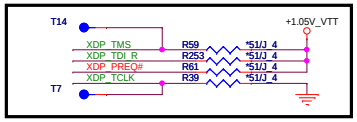


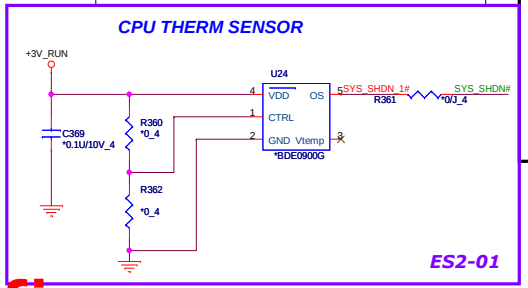










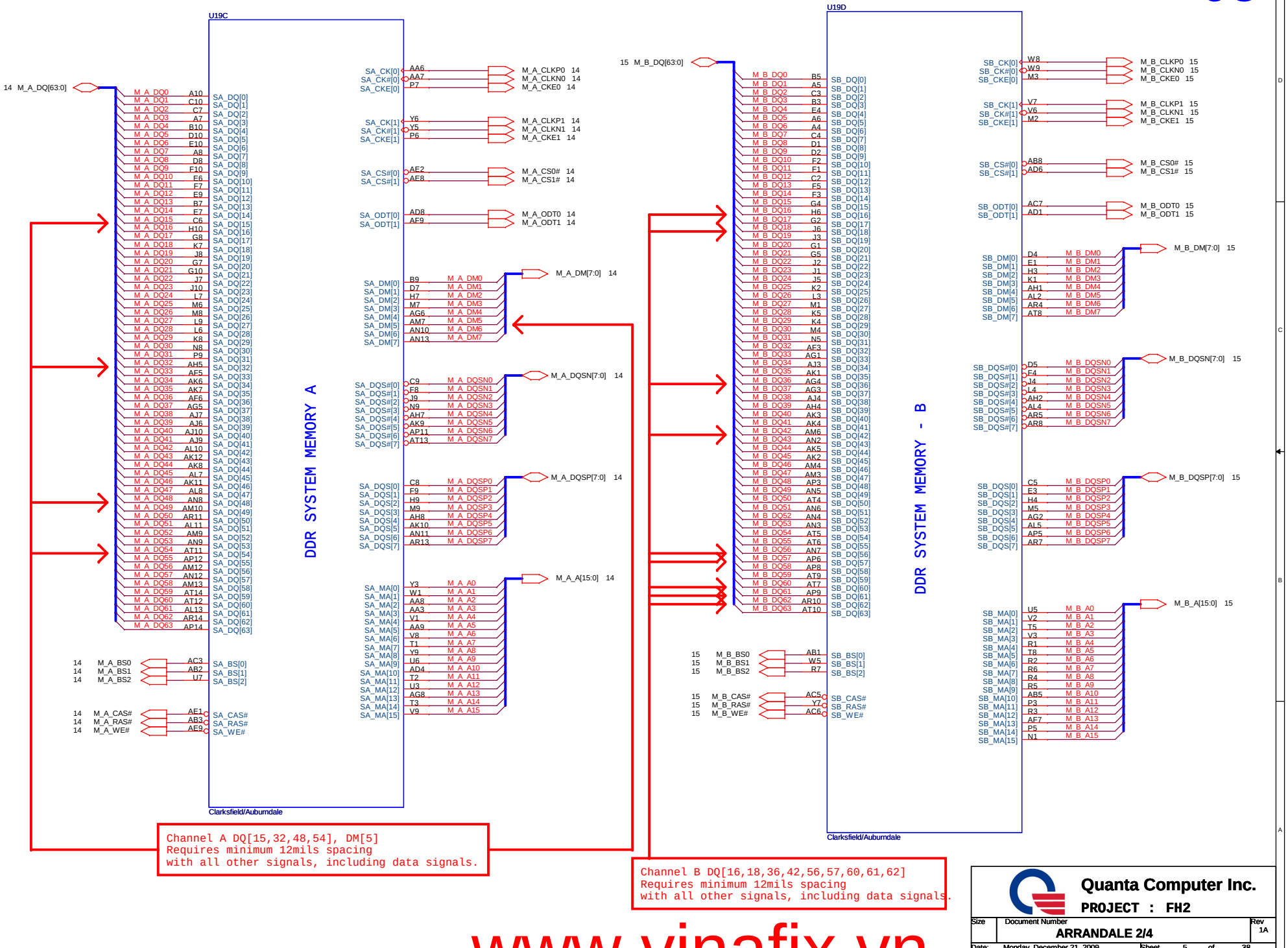


Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	ARRANDALE 1/4	1A
Date: Monday, December 21, 2009	Sheet 4 of 38	

ARRANDALE PROCESSOR (DDR3)

05



Quanta Computer Inc.			
PROJECT : FH2			
Size	Document Number		Rev
	ARRANDALE 2/4		1A
Date: Monday, December 21, 2009		Sheet 5 of 38	

CPU Core Power

ARRANDALE PROCESSOR (GRAPHICS POWER)

+VCC_CORE=4.8 max

+1.05V_VTT=1.8 max

U19F — CPU CORE SUPPLY — 1.1V RAIL POWER

U19G — GRAPHICS POWER — FDI — PEG & DMI — DDR3 - 1.5V RAILS — 1.1V — 1.8V

SENSE LINES — GRAPHICS VIDS

CPU VIDS

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

For S3 power reduction

Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors – caps should be evenly distributed between the connectors

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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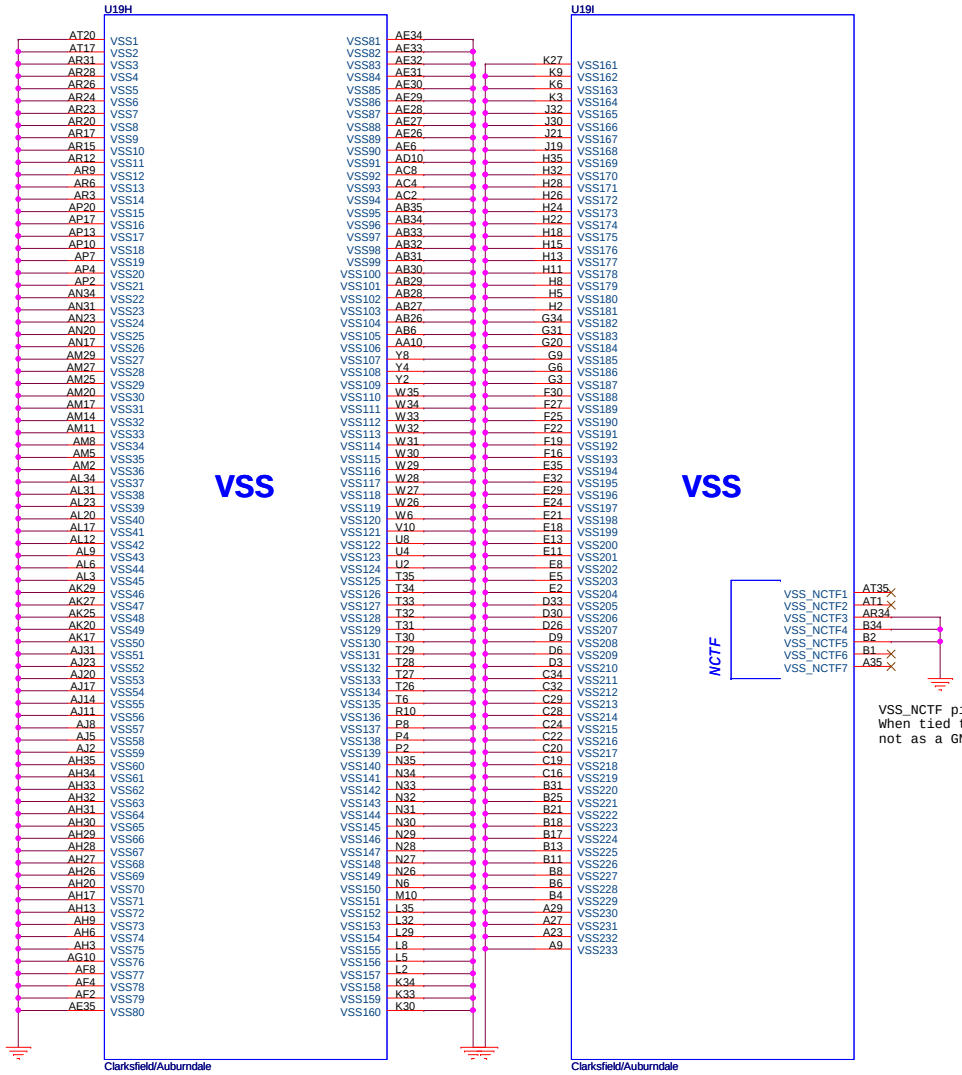
PROJECT : FH2

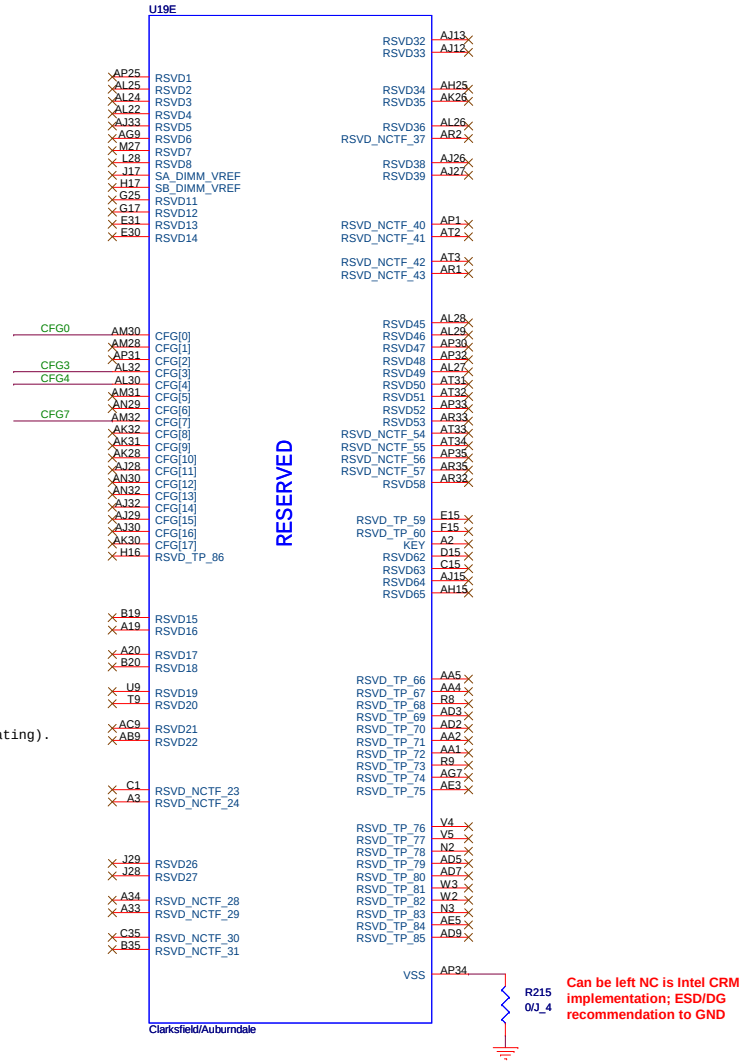
Size	Document Number	Rev
	ARRANDALE 3/4	1A
Date: Monday, December 21, 2009	Sheet 6 of 38	

ARRANDALE PROCESSOR (GND)



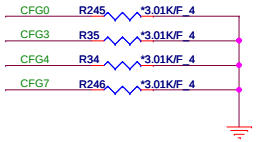
VSS_NCTF pins can be connected to GND or left as NC (floating). When tied to GND they should be routed as trace and not as a GND plane.

ARRANDALE PROCESSOR(RESERVED, CFG)



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



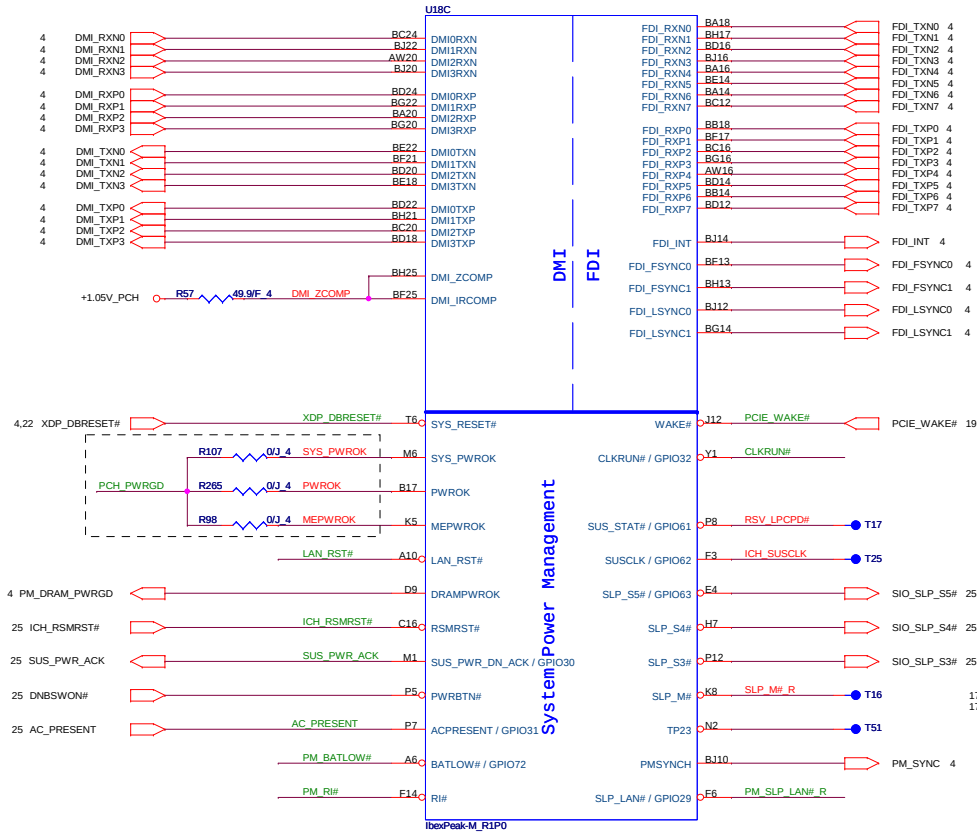
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Quanta Computer Inc.
PROJECT : FH2

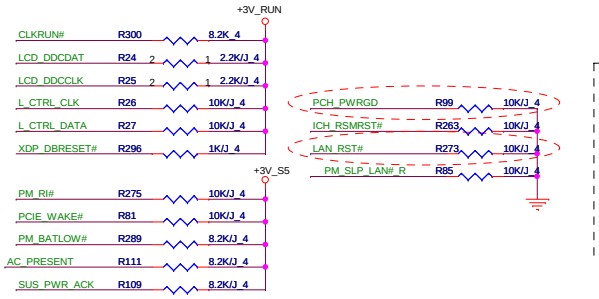
Size	Document Number	Rev
	ARRANDALE 4/4	1A

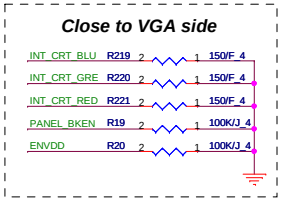
Date: Monday, December 21, 2009 Sheet 7 of 38

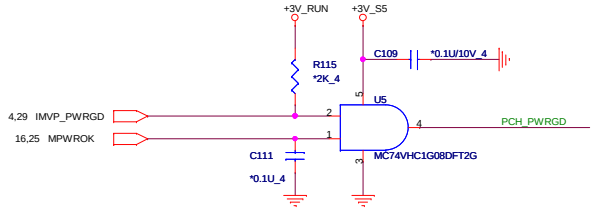
IBEX PEAK-M (DMI,FDI,GPIO)

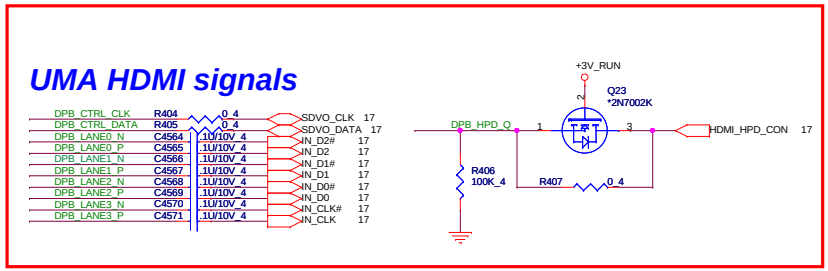


IBEX PEAK-M (LVDS,DDI)







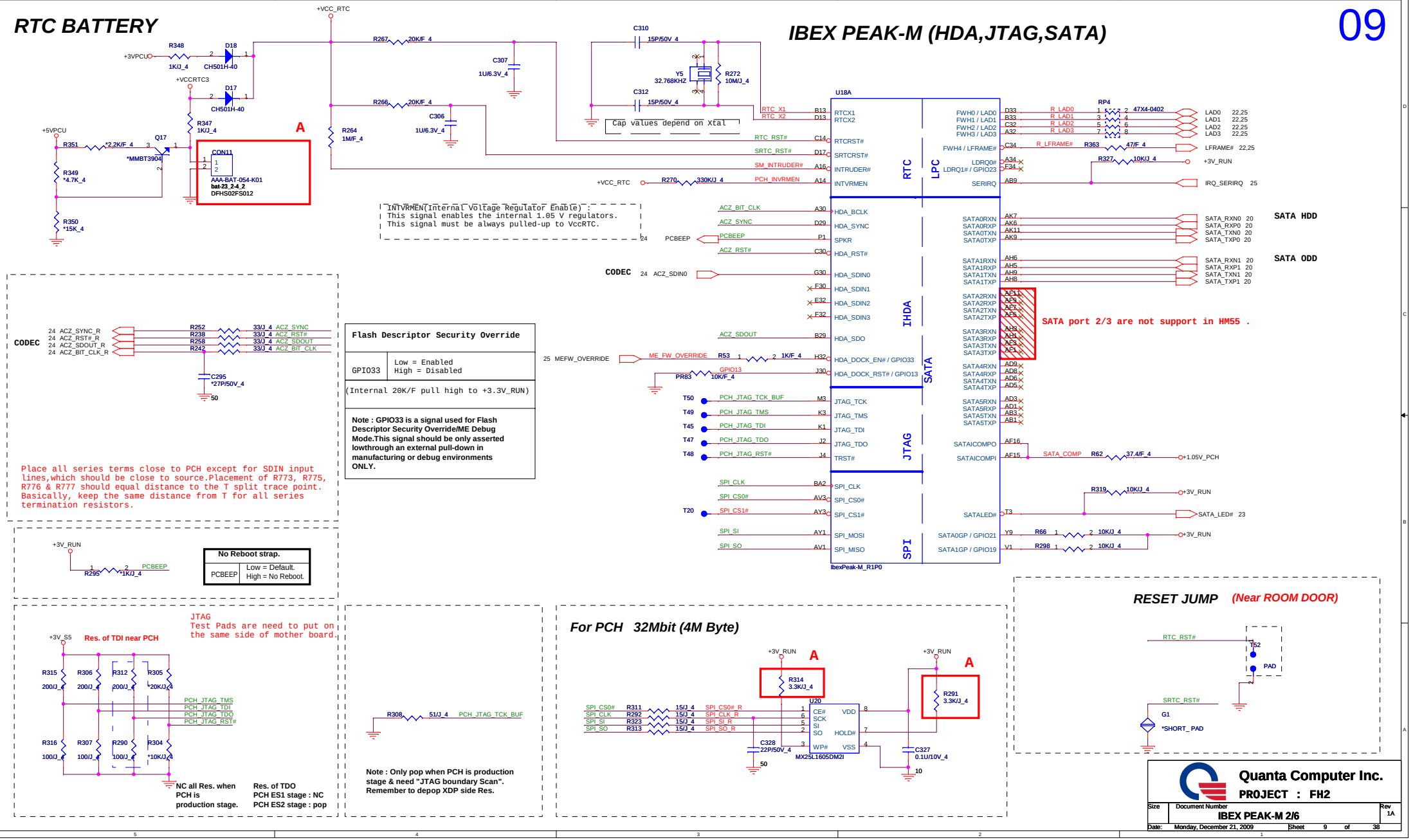


Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: IBEX PEAK-M 1/6	Rev: 1A
Date: Monday, December 21, 2009	Sheet 8 of 38	

RTC BATTERY

IBEX PEAK-M (HDA,JTAG,SATA)

09



Quanta Computer Inc.

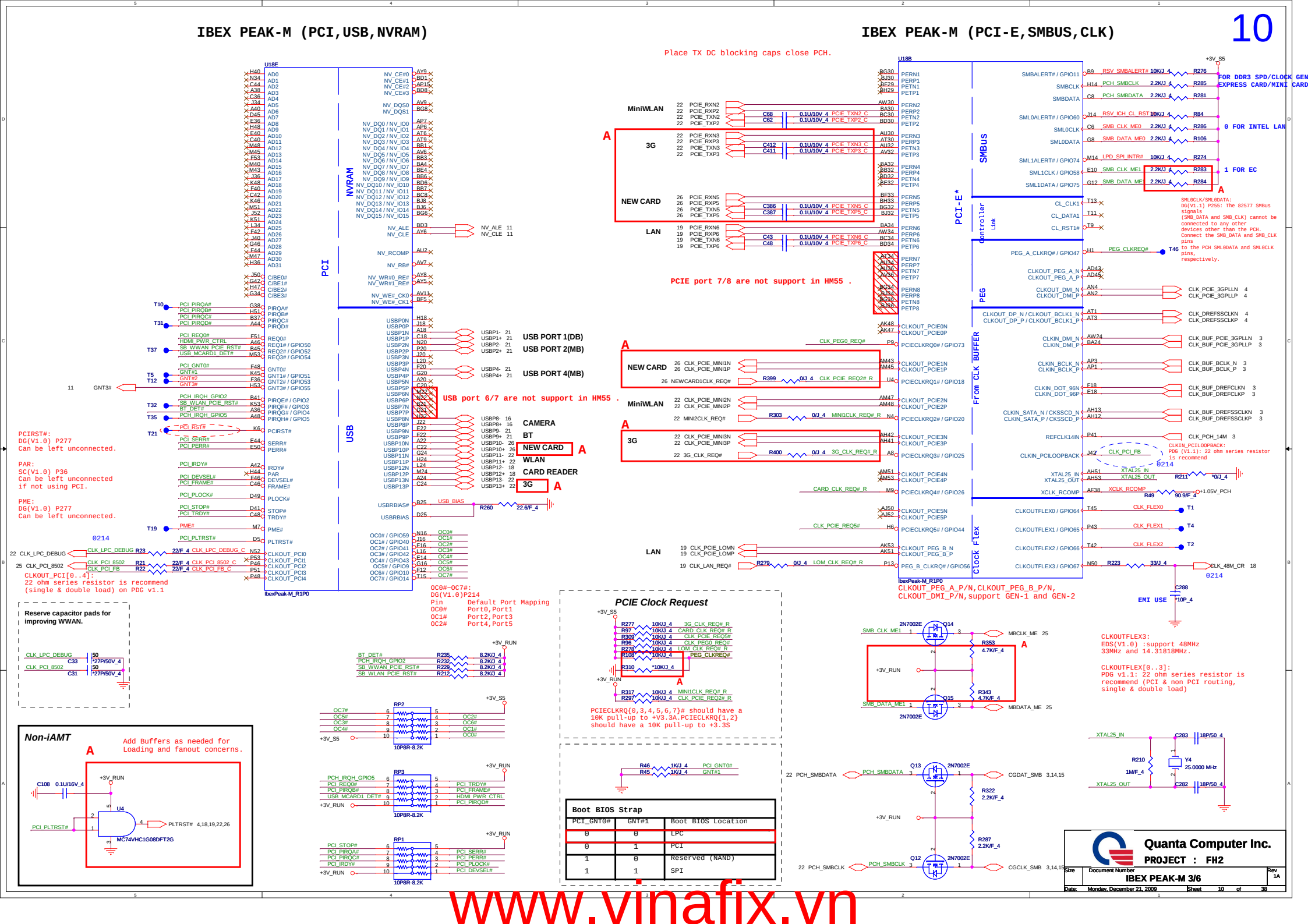
PROJECT : FH2

Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A

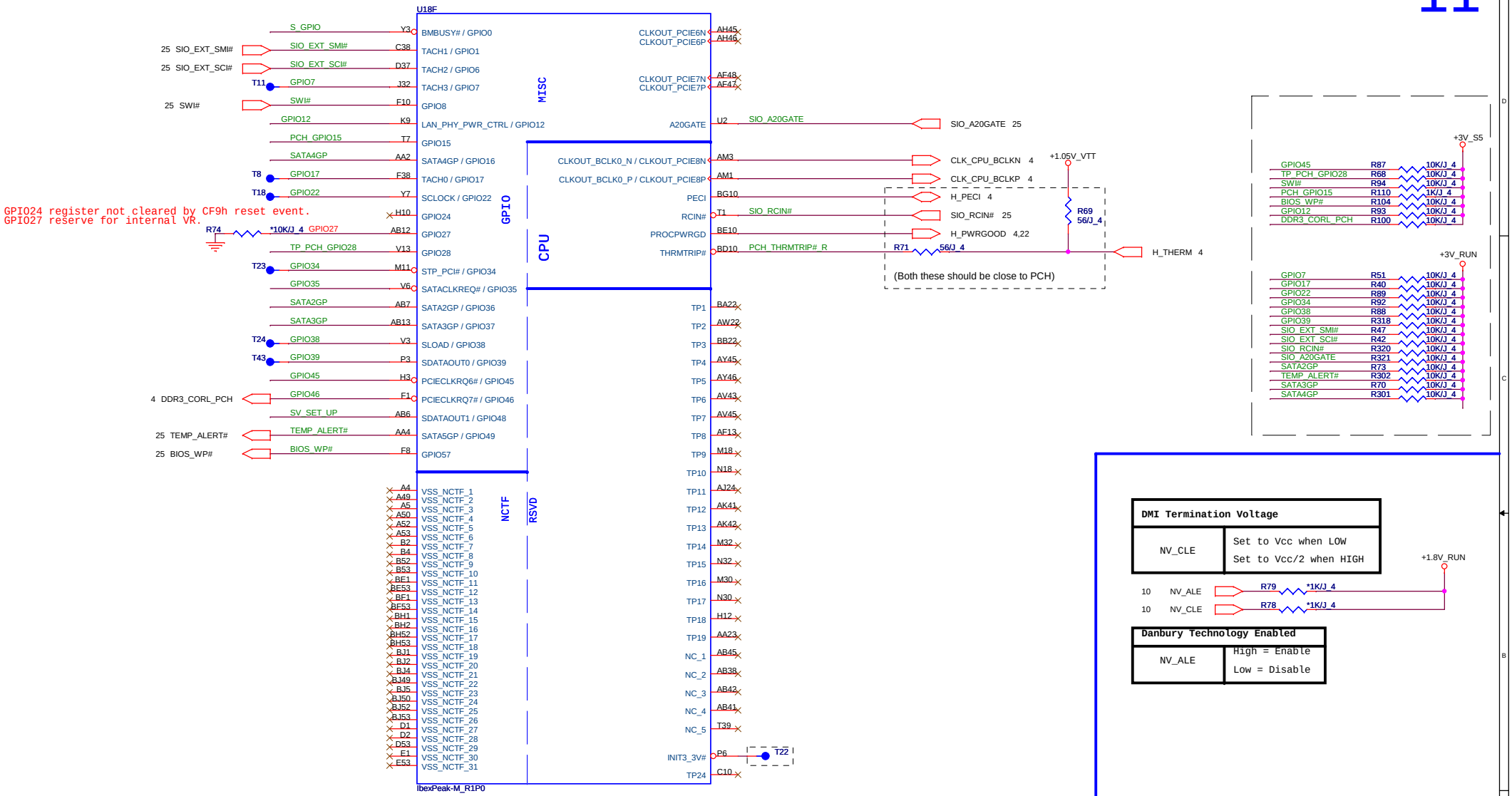
Date: Monday, December 21, 2009 Sheet 9 of 38

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)



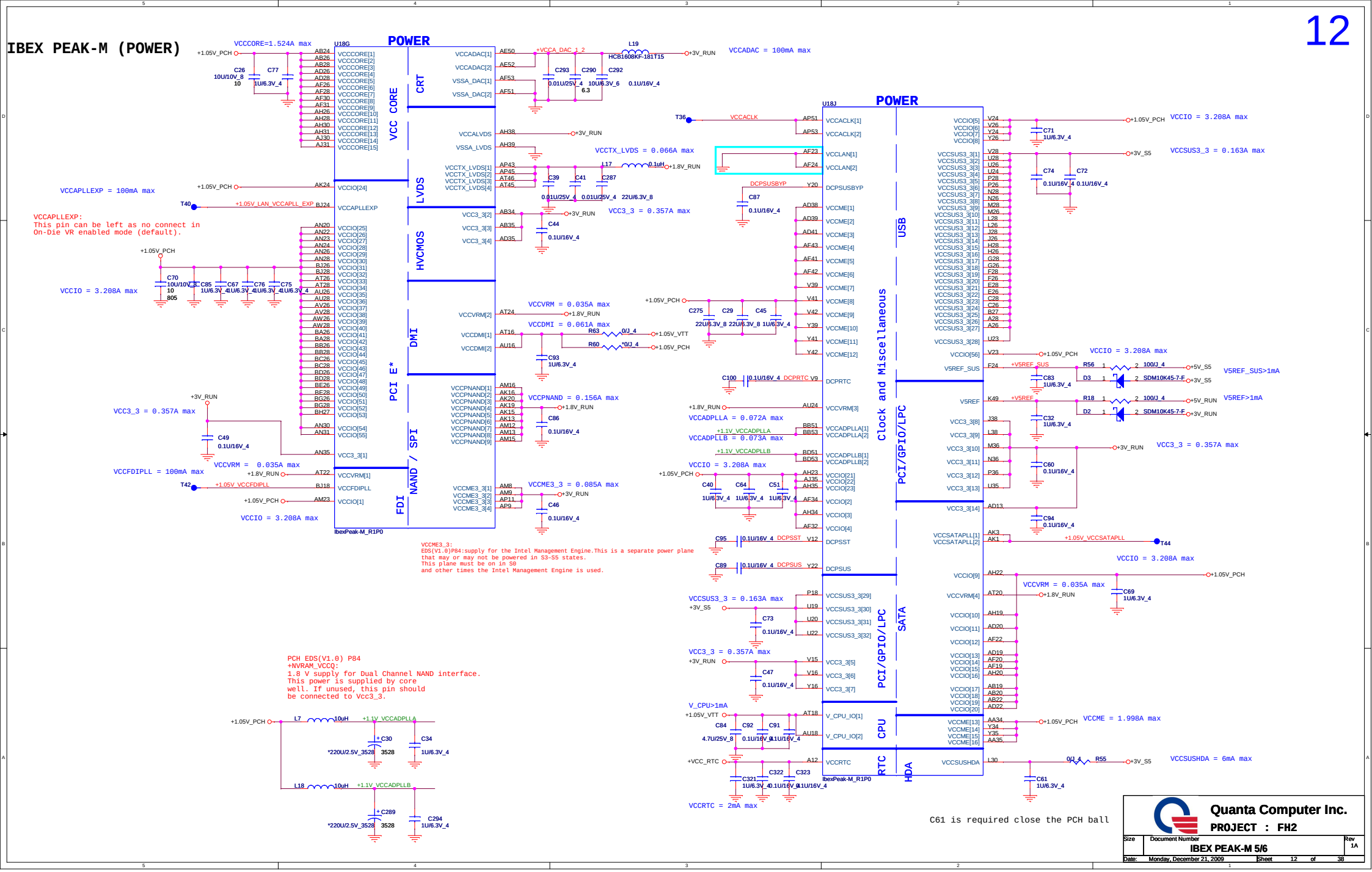
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A
Date: Monday, December 21, 2009	Sheet 11 of 38	

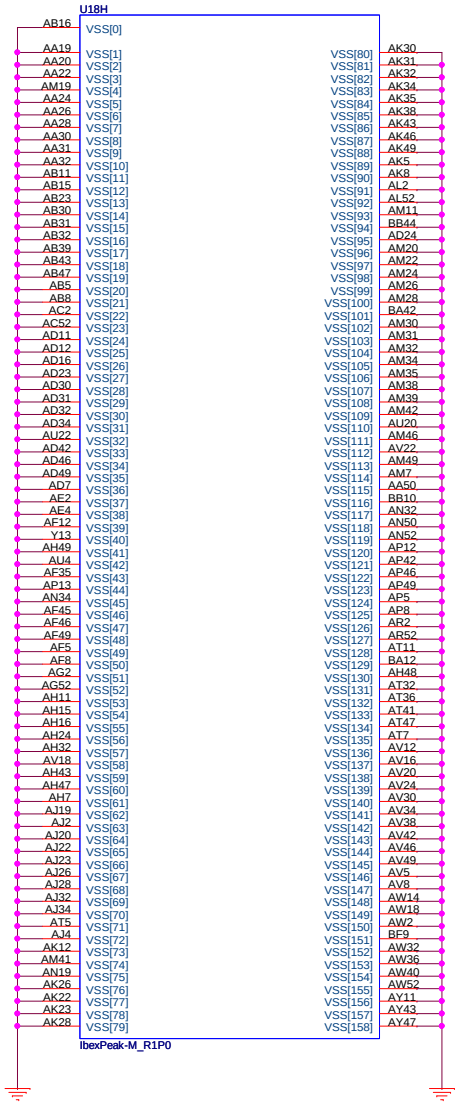
IBEX PEAK-M (POWER)

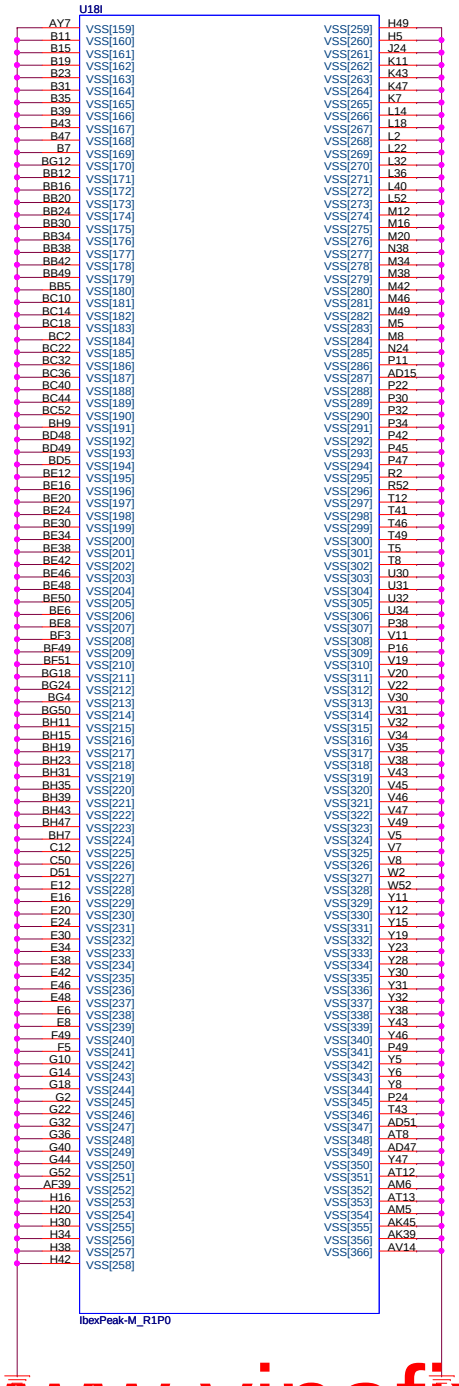


Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	IBEX PEAK-M 5/6	1A
Date: Monday, December 21, 2009	Sheet 12 of 38	

IBEX PEAK-M (GND)

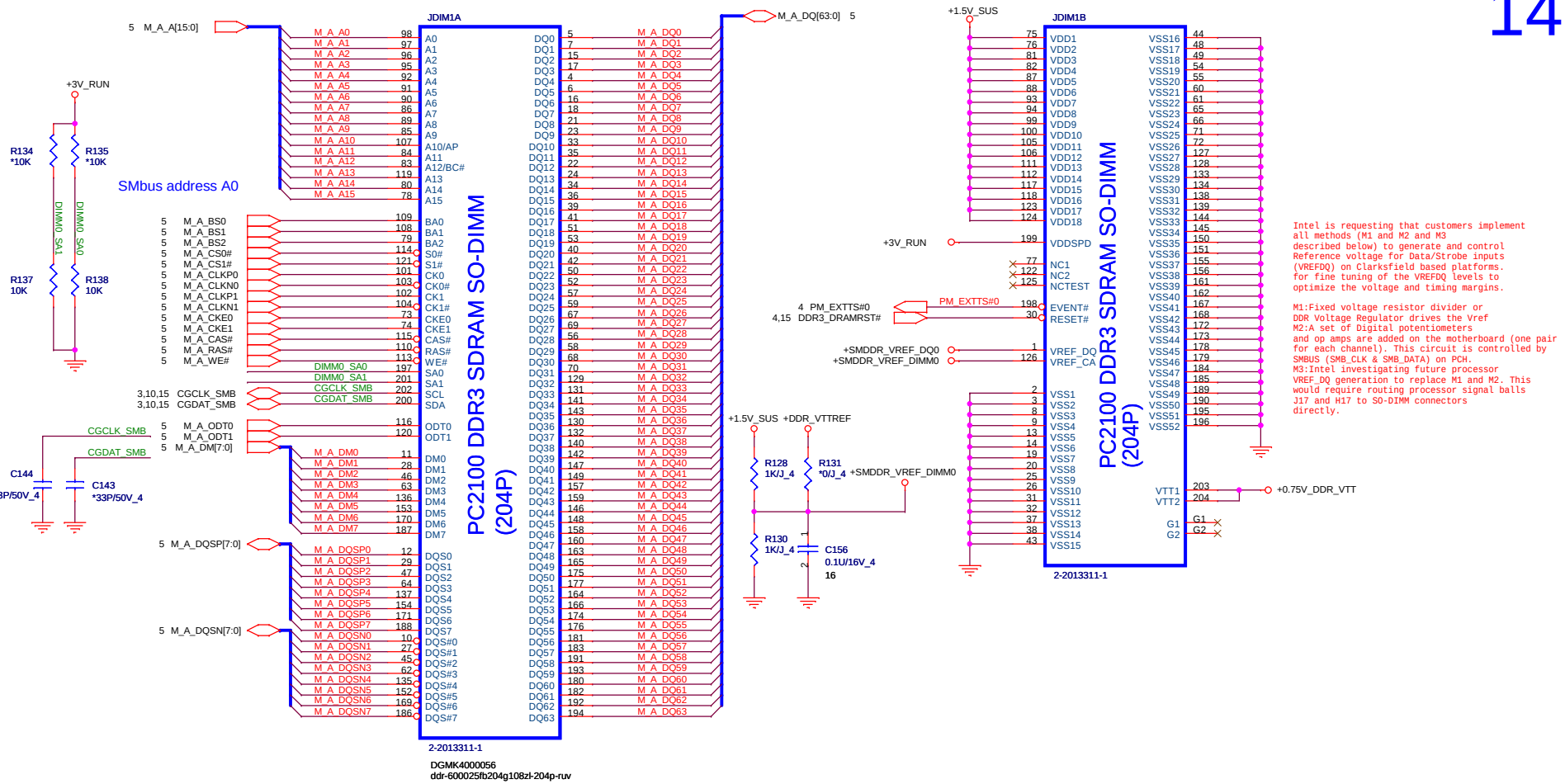




Quanta Computer Inc.

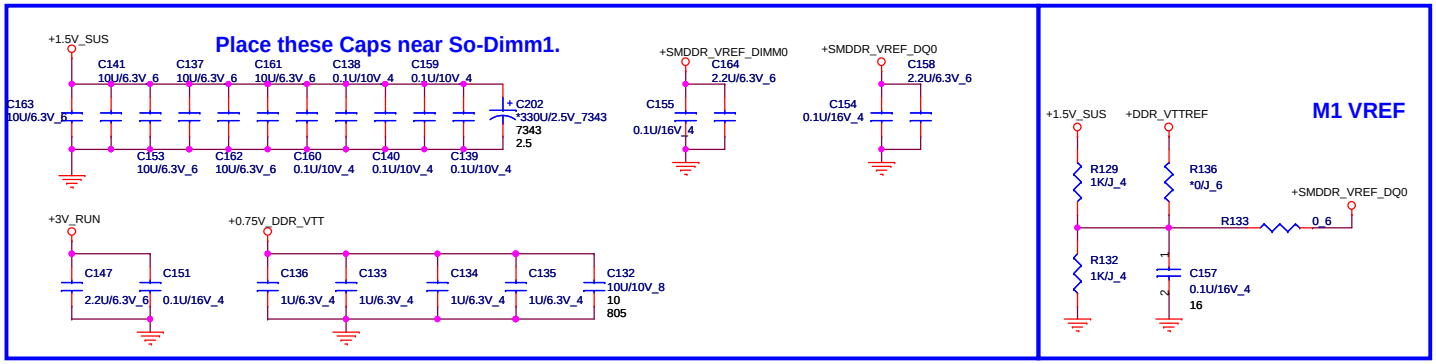
PROJECT : FH2

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
Date:	Monday, December 21, 2009	Sheet 13 of 38



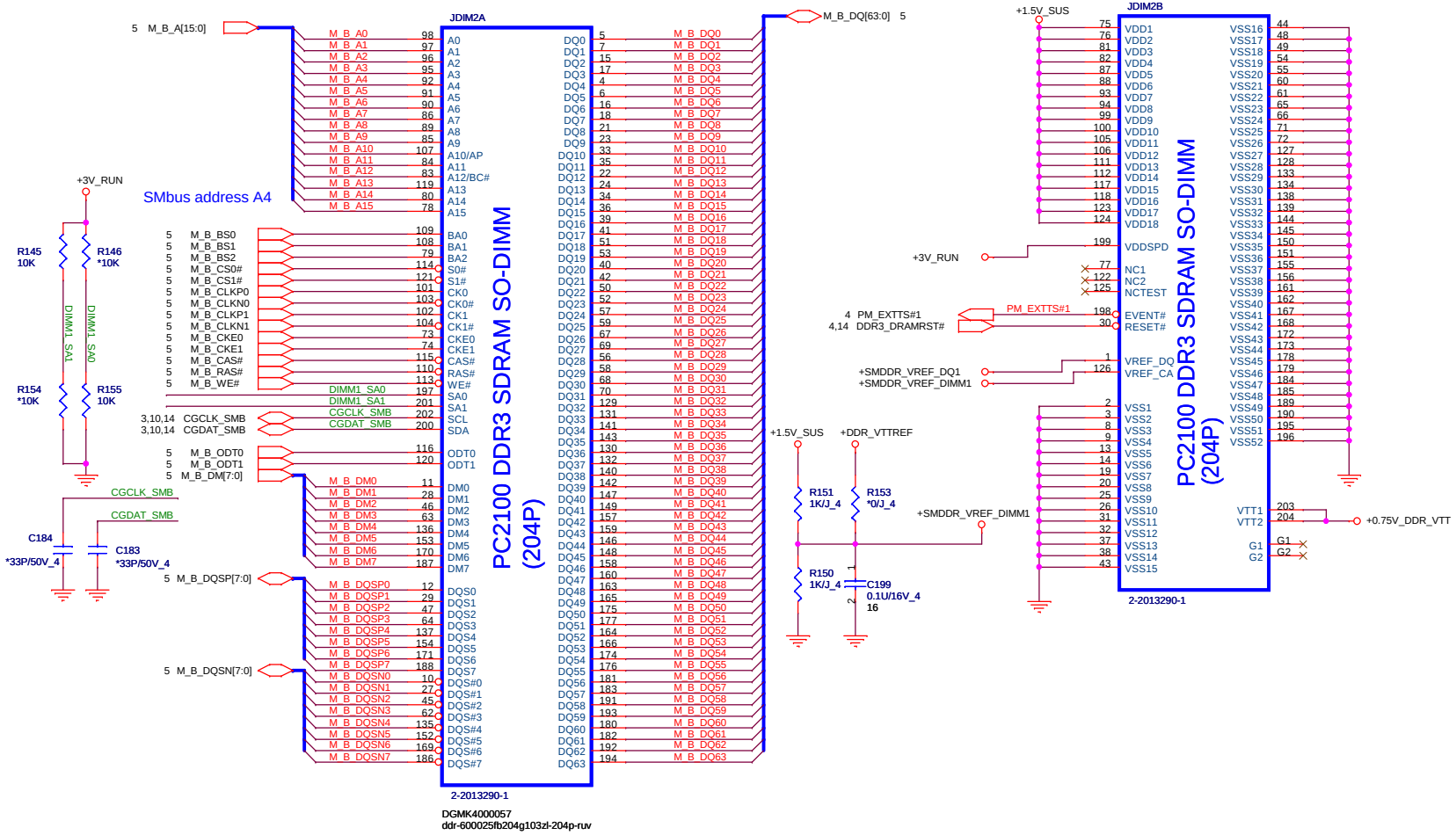
Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

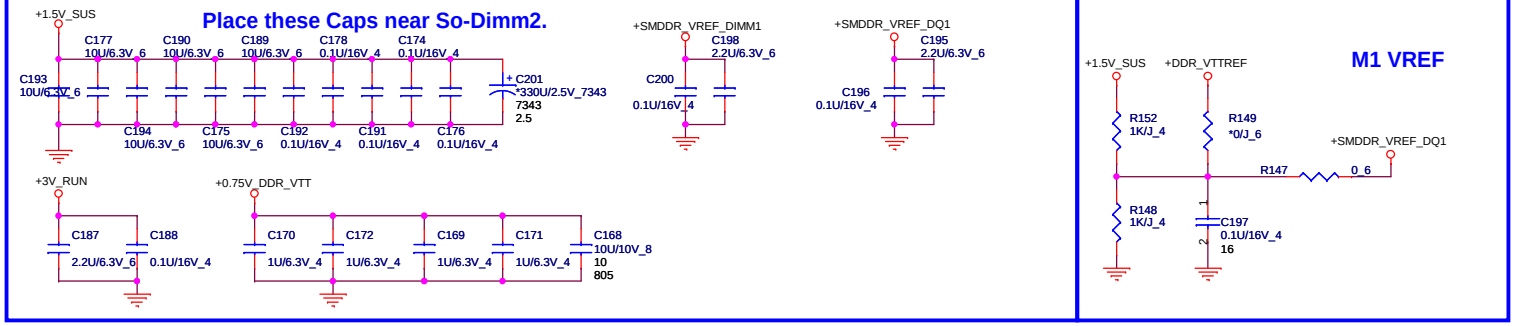
M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.



Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date: Monday, December 21, 2009	Sheet 14 of 38	





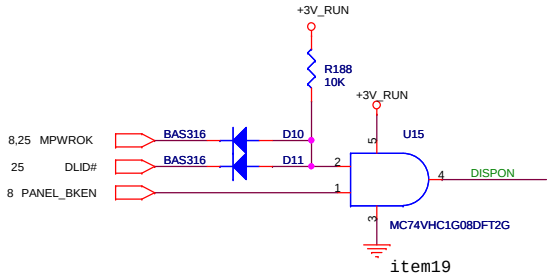
Quanta Computer Inc.

PROJECT : FH2

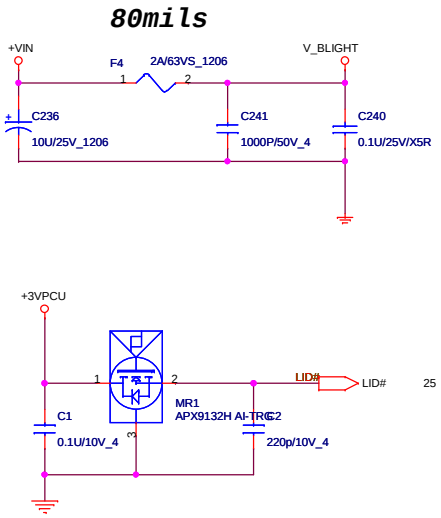
Size	Document Number	Rev
	DDR3 DIMM-2	1A

Date: Monday, December 21, 2009 Sheet 15 of 38

Backlight Control(LDS)

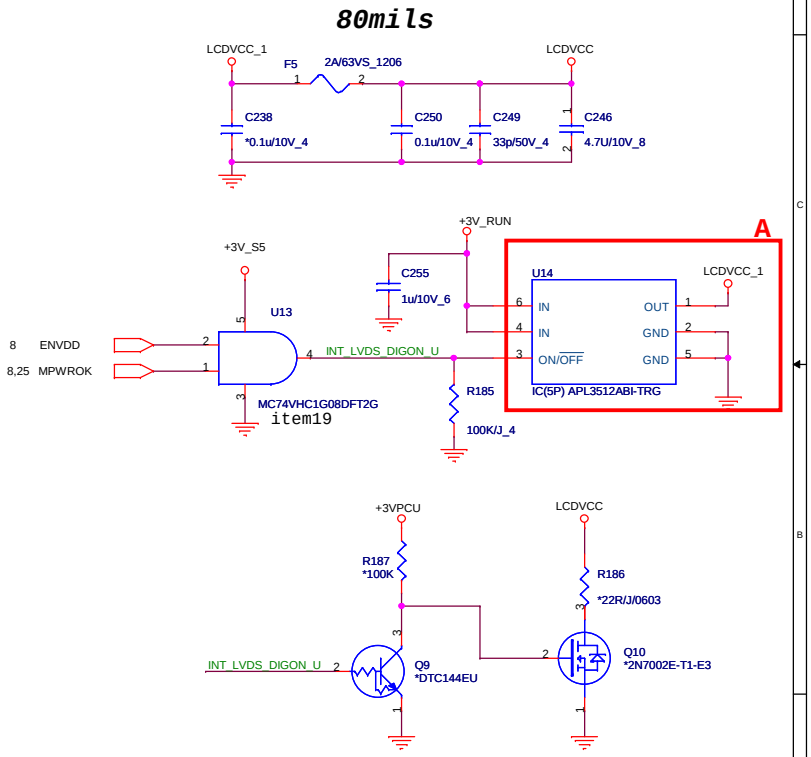


BACKLIGHT POWER

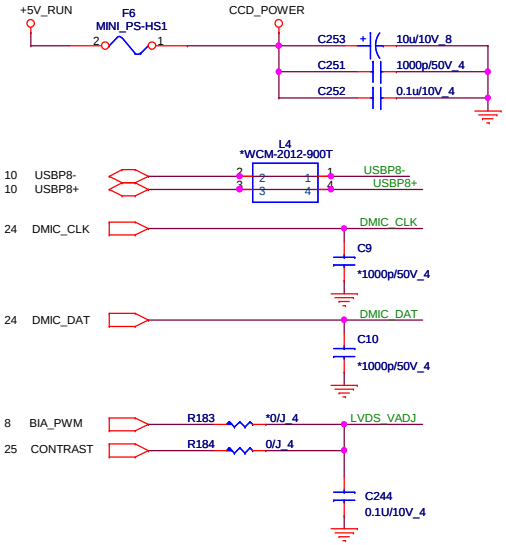


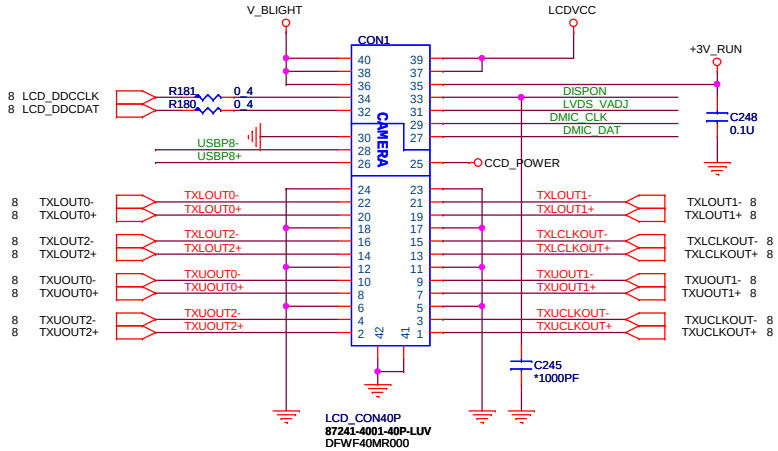
LED Panel POWER SWITCH(LVDS)

16



LVDS/CCD





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PROJECT : FH2

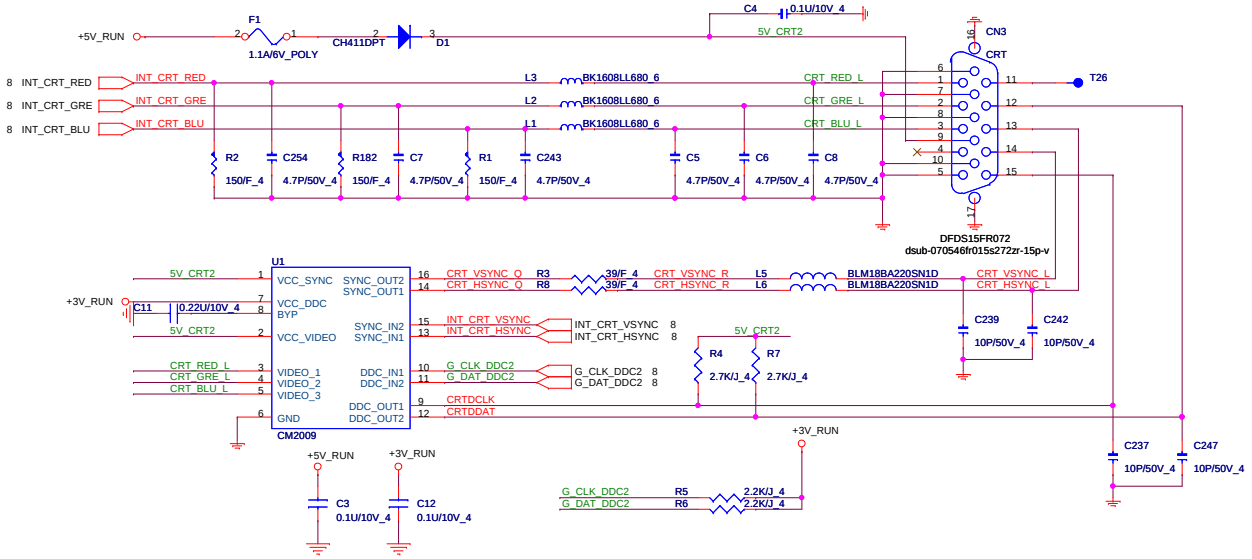
Size	Document Number	Rev
	LCD/LED Panel/CCD	1A
Date: Monday, December 21, 2009	Sheet 16 of 38	

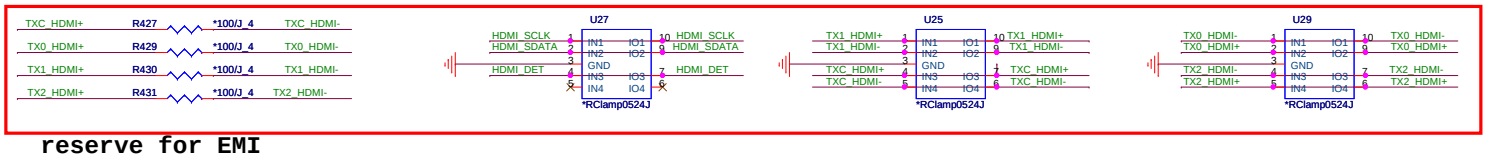
CRT CONN/DDC LEVEL SHIFT

17

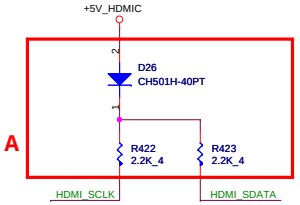
40mils

TBD CN5500 FOOTPRINT





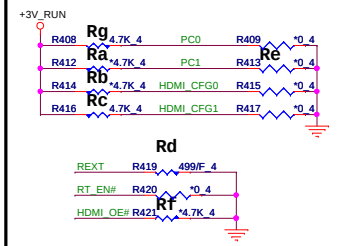
A

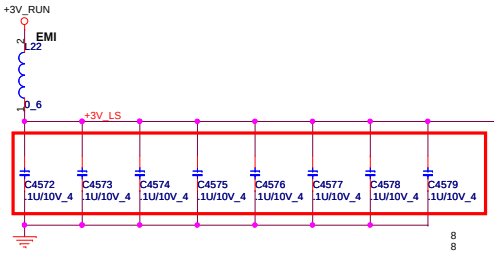


reserve for EMI

Signals		PDT	CHR	PIM
PC1	Ra	NC	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318001
Vendor:PIM P/N:ALP411LS004





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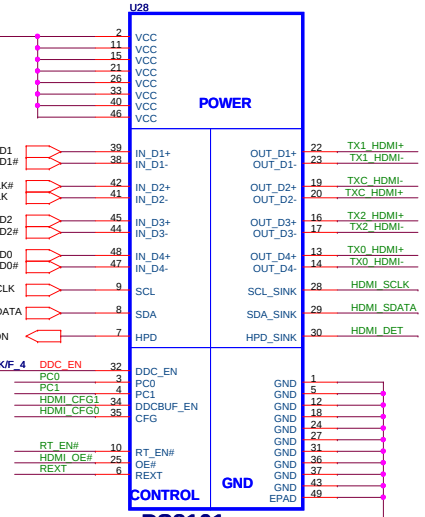
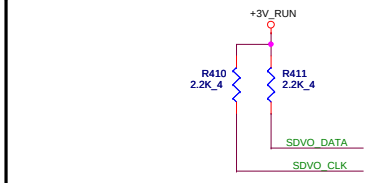
HDMI





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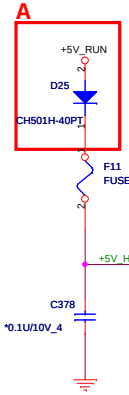
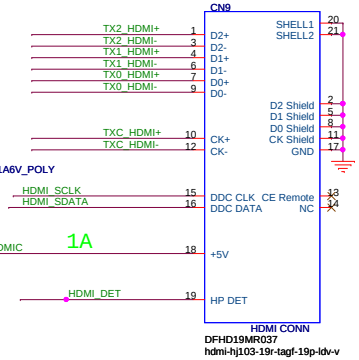




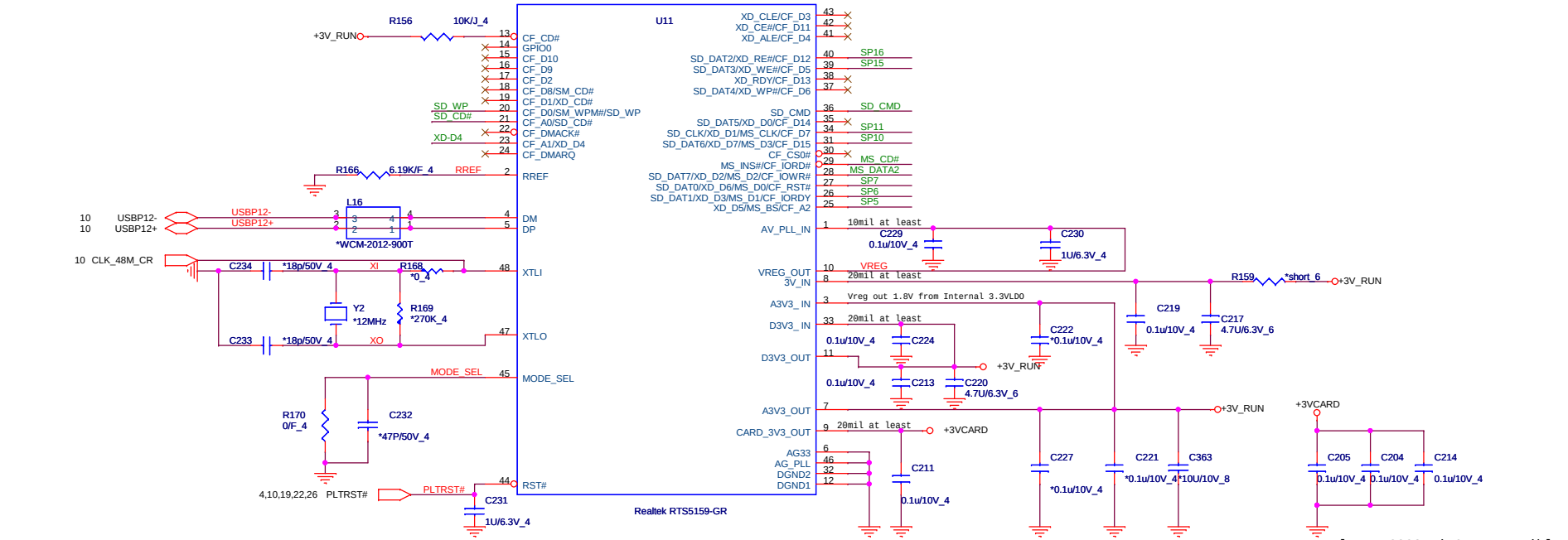
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

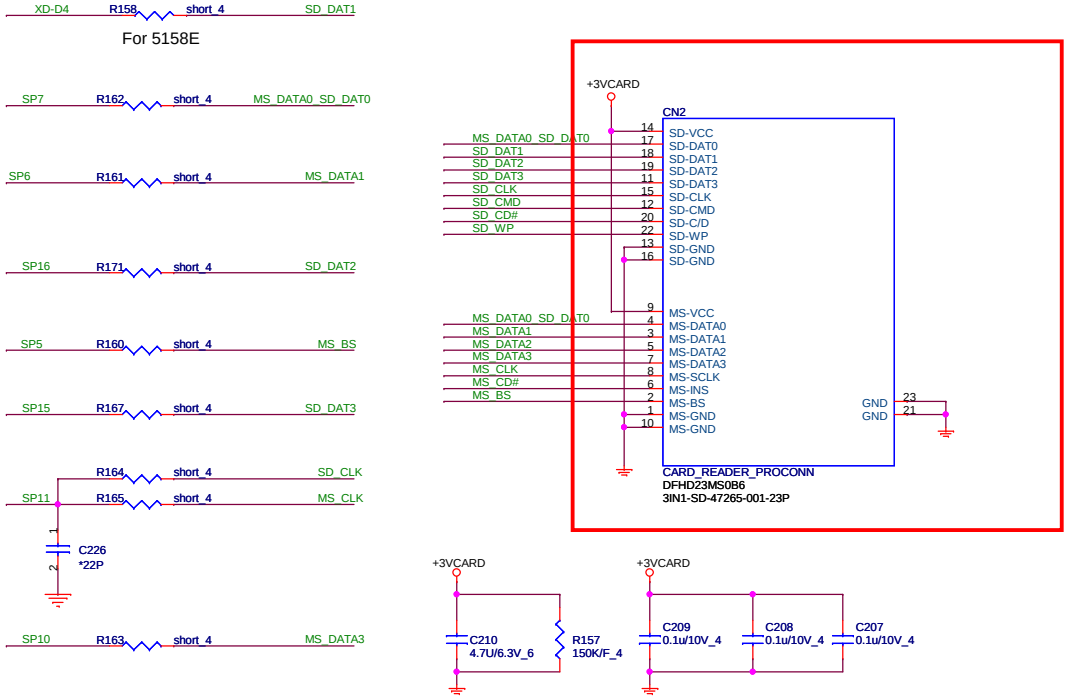
CFG = LOW: LOW-level input voltage: <0.40 V, LOW-level output voltage: 0.60 V
CFG = HIGH: LOW-level input voltage: <0.44 V, LOW-level output voltage: 0.66 V
HDMI_CFG1 = LOW: Passive DDC buffer
HDMI_CFG1 = HIGH: Active DDC buffer

Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	CRT CONN/HDMI	1A
Date: Monday, December 21, 2009	Sheet 17 of 38	

Card Reader

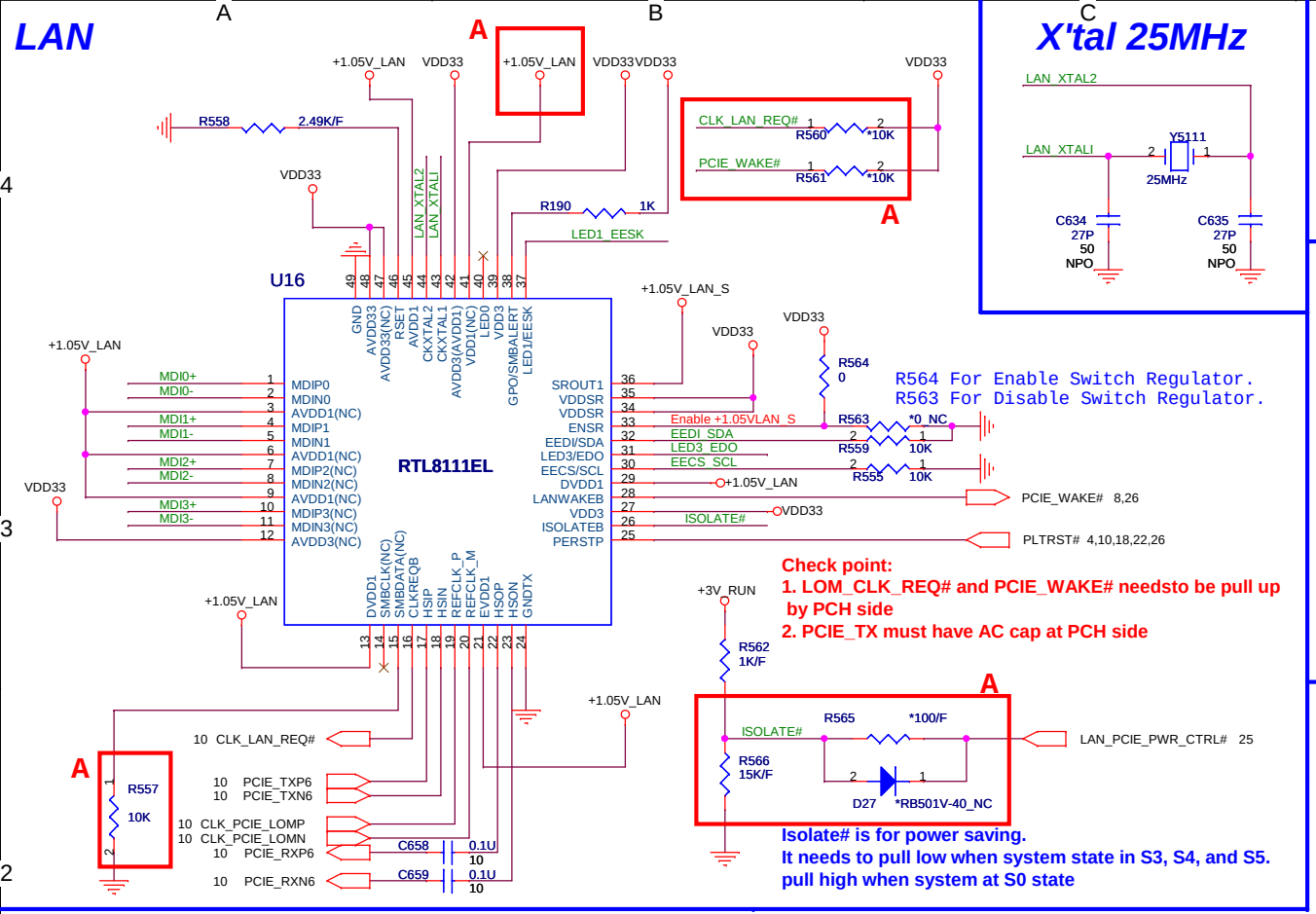




Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	Card Reader RTS5159	1A
Date: Monday, December 21, 2009	Sheet 18 of 38	

LAN



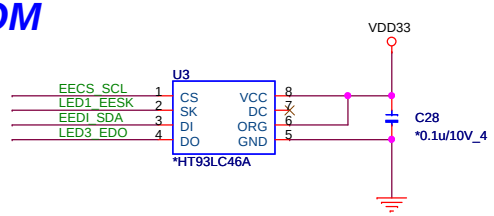
R564 For Enable Switch Regulator.
R563 For Disable Switch Regulator.

Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needsto be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

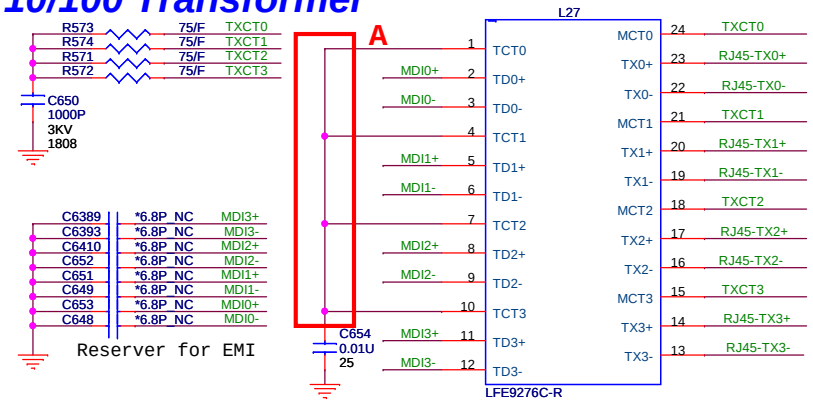
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state

X'tal 25MHz

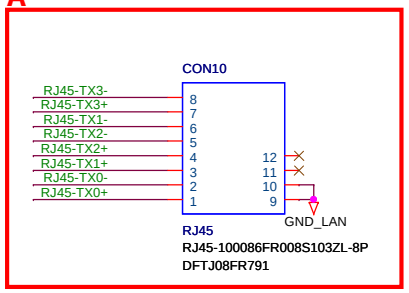
LAN EEPROM

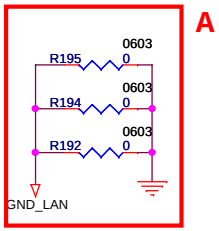


10/100 Transformer

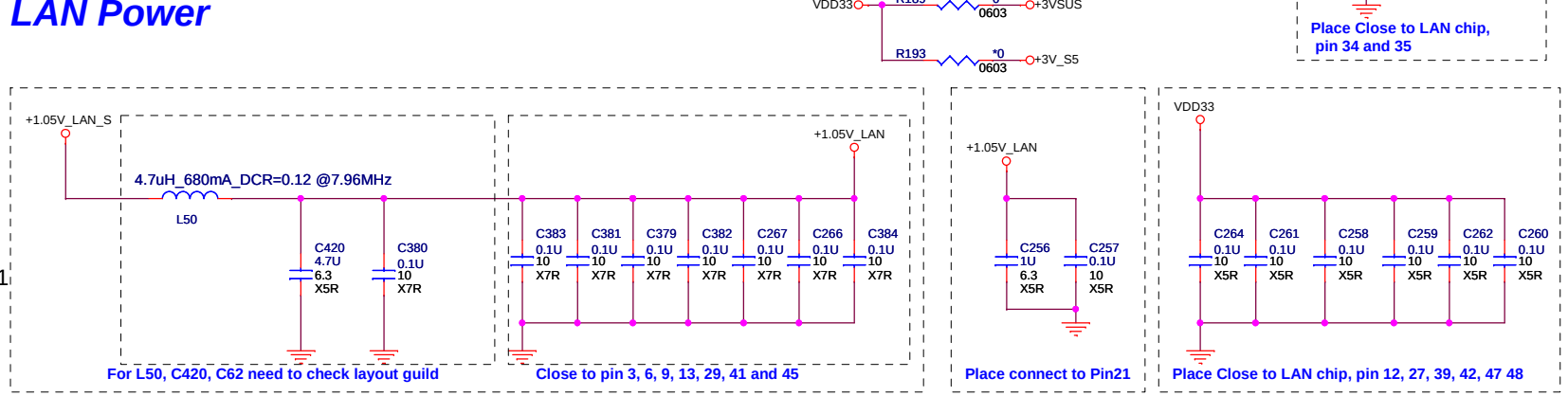


RJ45





LAN Power

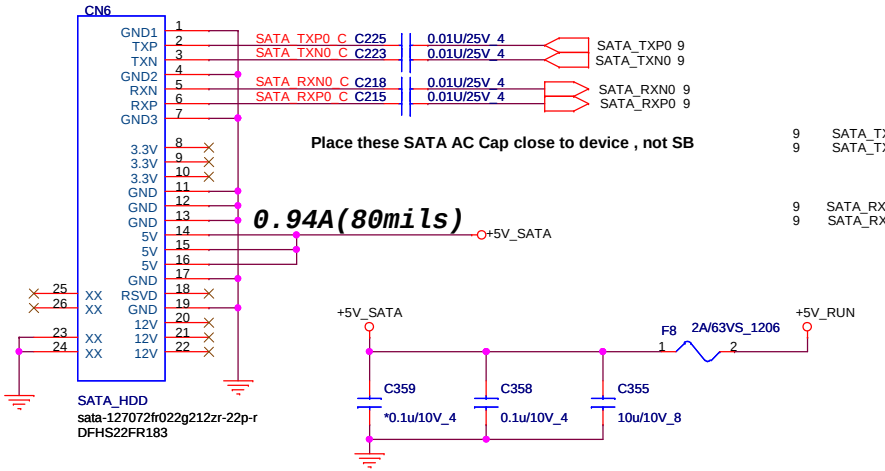


For L50, C420, C62 need to check layout guild
Close to pin 3, 6, 9, 13, 29, 41 and 45
Place connect to Pin21
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48
Place Close to LAN chip, pin 34 and 35

REQ by layout

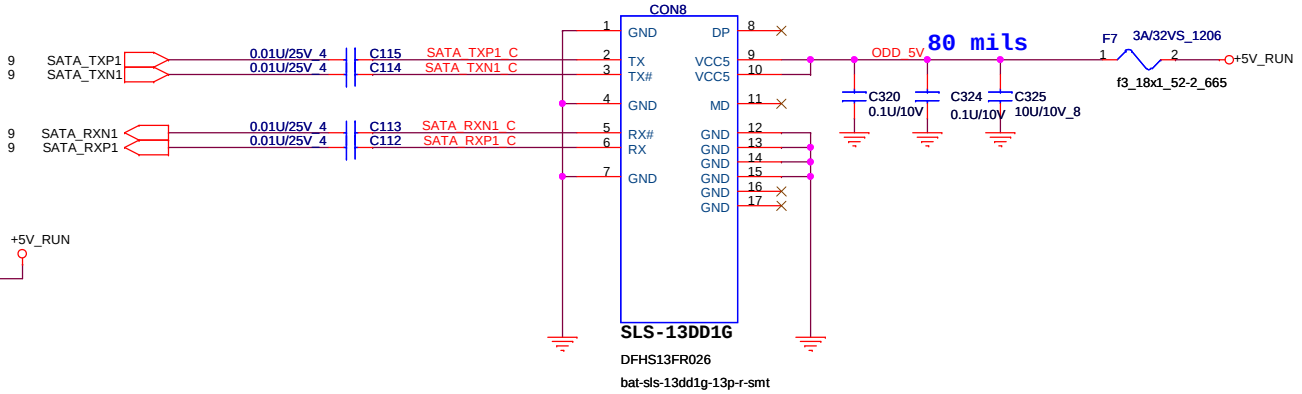
Quanta Computer Inc.	PROJECT : FH2	
Size	Document Number: LAN_RTL8111E-GR/RJ45	Rev 1A
Date: Monday, December 21, 2009	Sheet 19 of 38	

2.5" SATA HDD



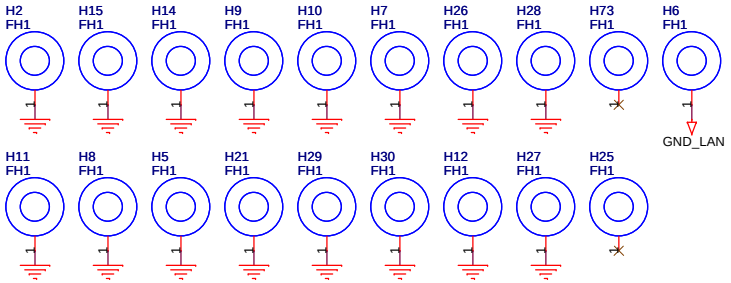
SATA ODD

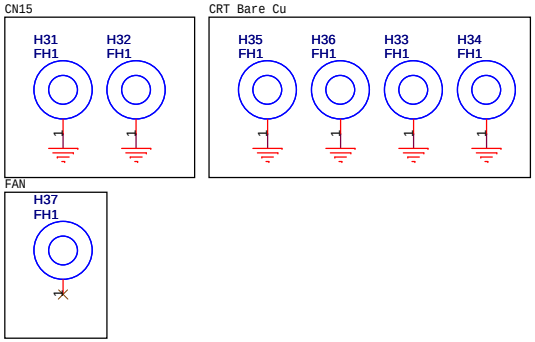
ODD CONN



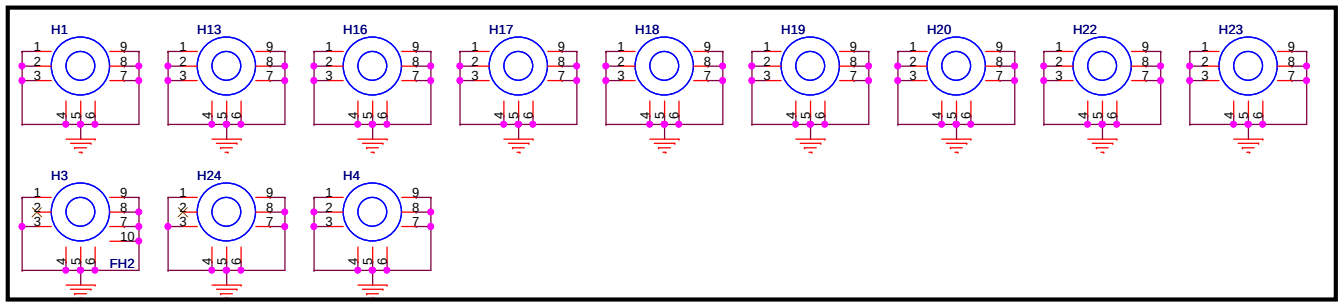
20

Hole

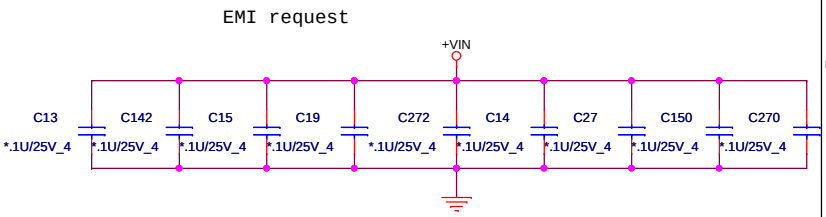




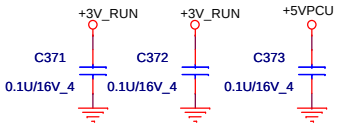
ESD



Decoupling Cap



EMI(Decoupling Cap)



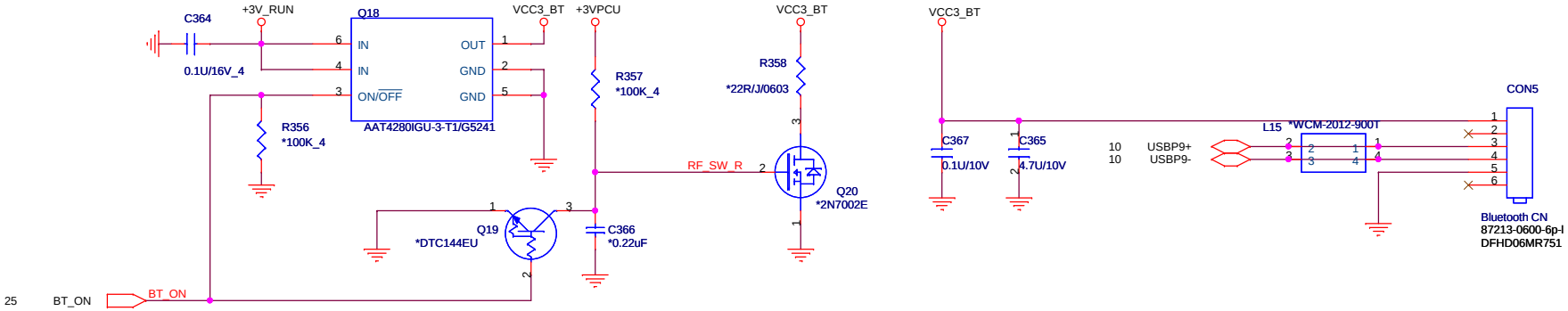
Quanta Computer Inc.

PROJECT : FH2

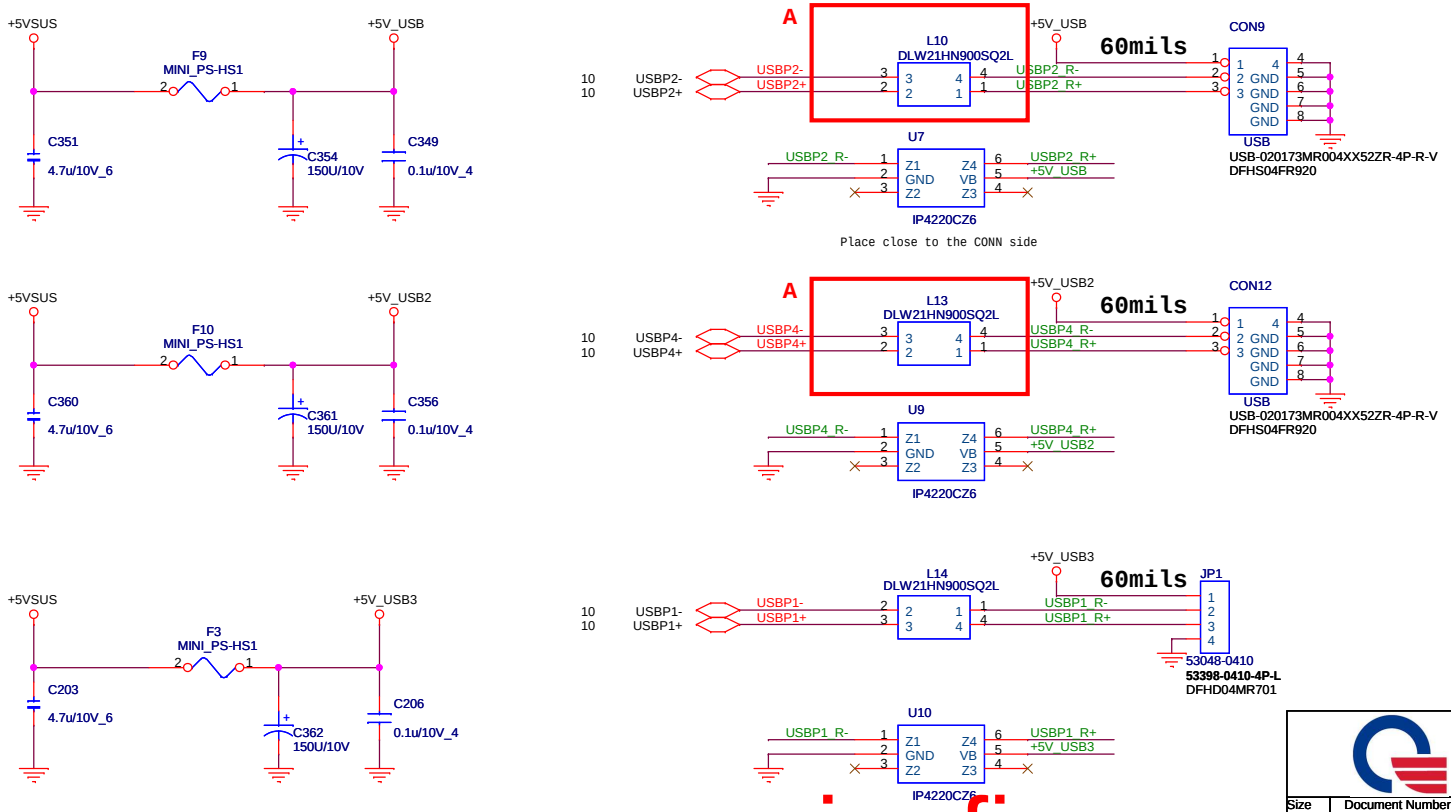
Size	Document Number	Rev
	HDD/ ODD/HOLE	1A

Date: Monday, December 21, 2009 Sheet 20 of 38

BuleTooth (BTM)

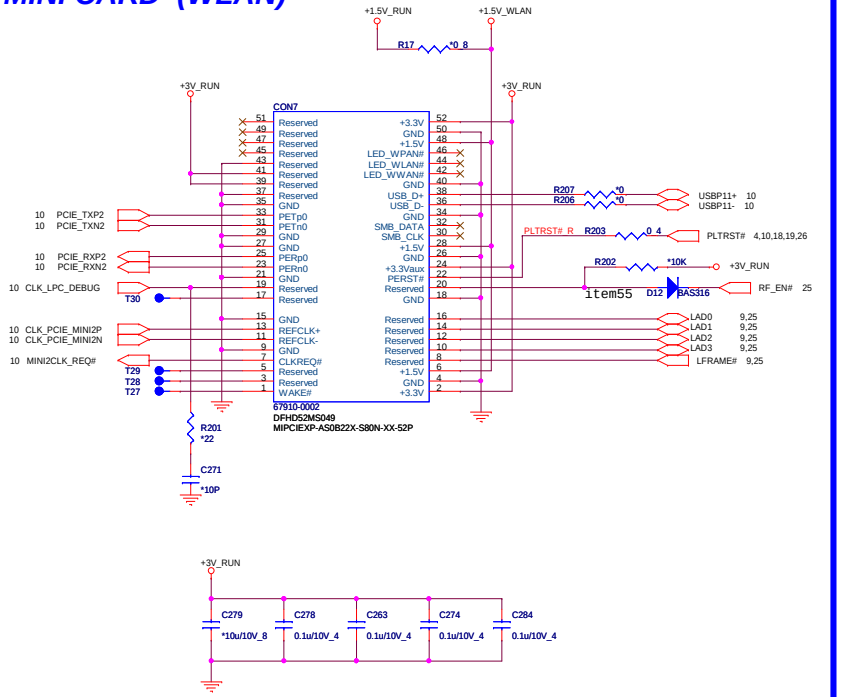


USB Connector

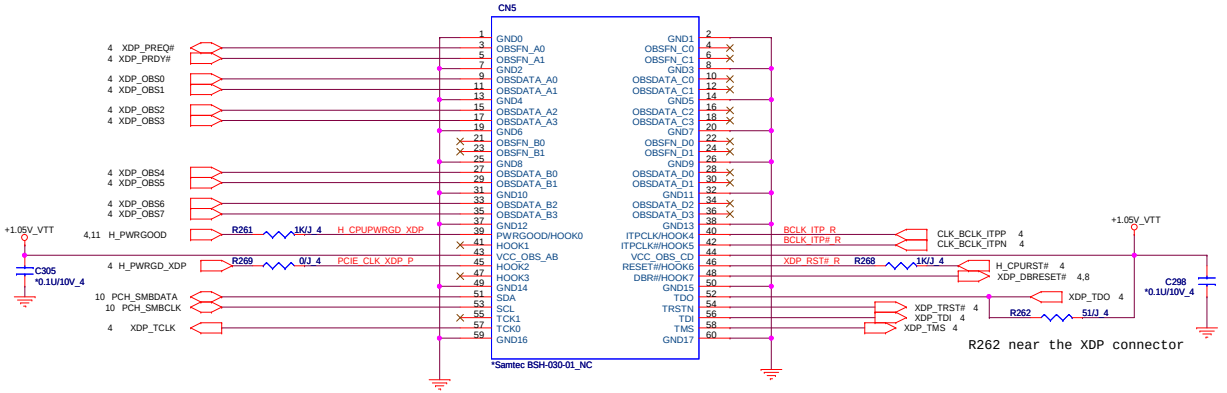


Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: USB/BLUE TOOTH	Rev 1A
Date: Monday, December 21, 2009	Sheet 21 of 38	

MINI CARD (WLAN)

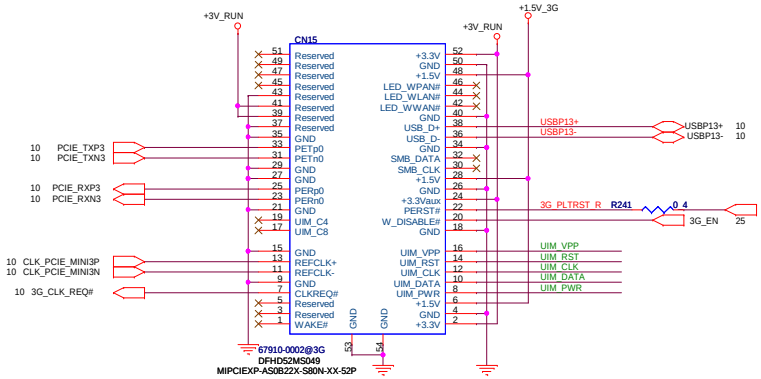


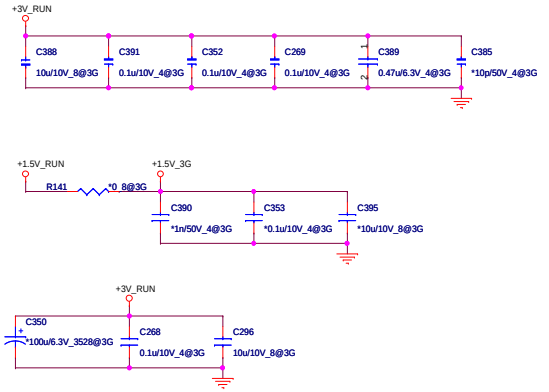
XDP

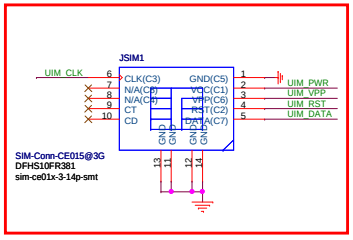


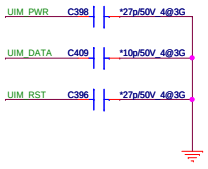
It is for debug. requesst vendeer provide 200 pcs sample.

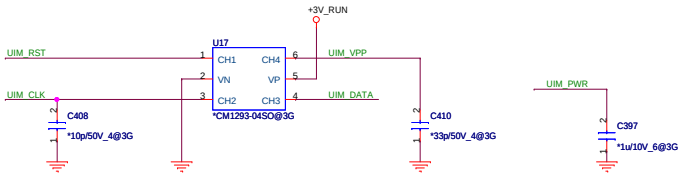
Mini Card2-3G(MNC)







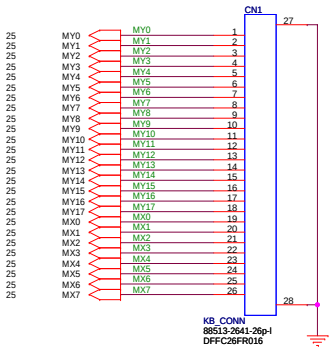




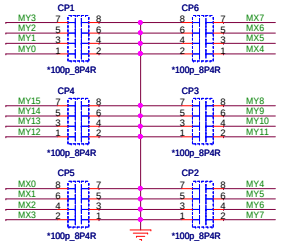
A

Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: MINI CARD(WLAN/3G)/XDP	Rev: 1A
Date: Monday, December 21, 2009	Sheet 22 of 38	

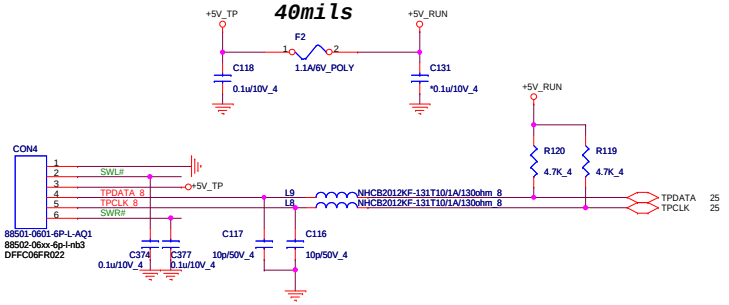
Keyboard(KBC)

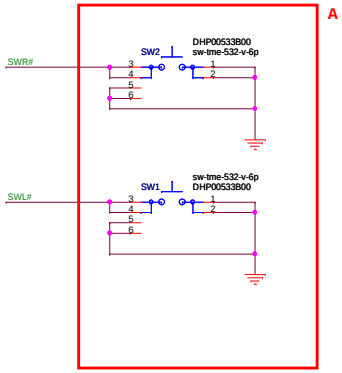


For EMI Reserve Caps for debug

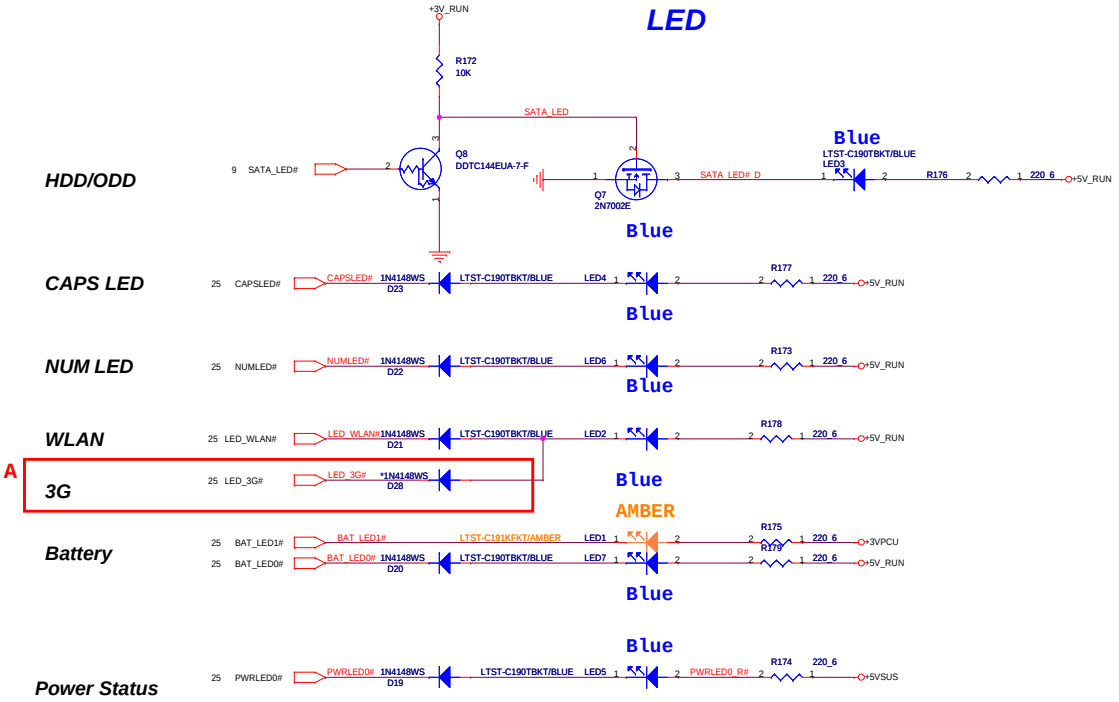


Touch Pad





LED



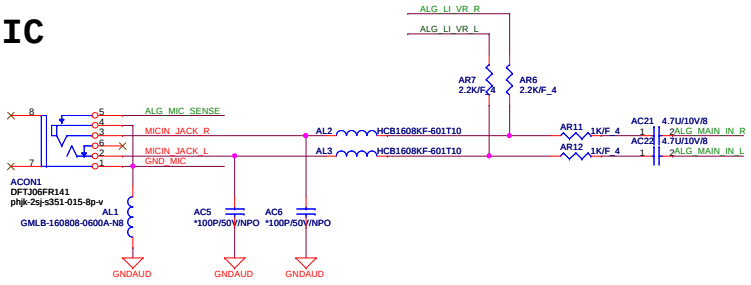
Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	KB/TOUCH PAD/LED	1A

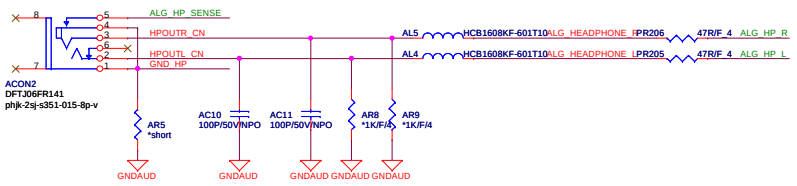
Date: Monday, December 21, 2009 Sheet 23 of 38

Codec ALC269

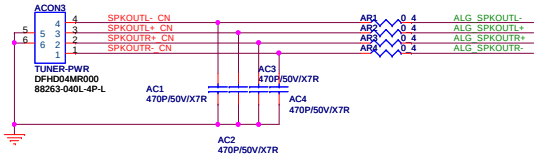
MIC



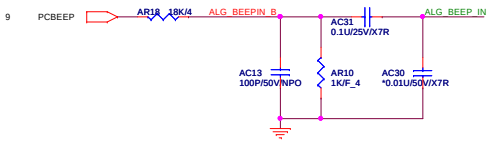
HP



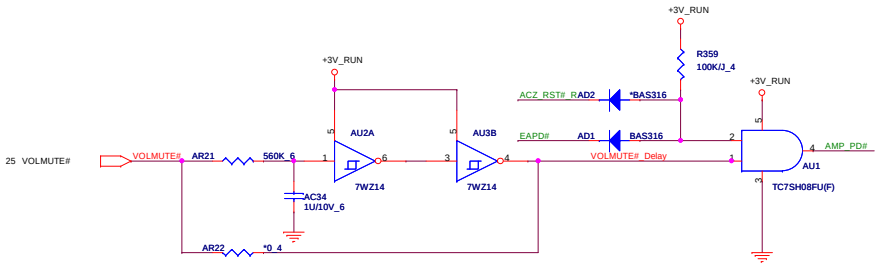
SPKR



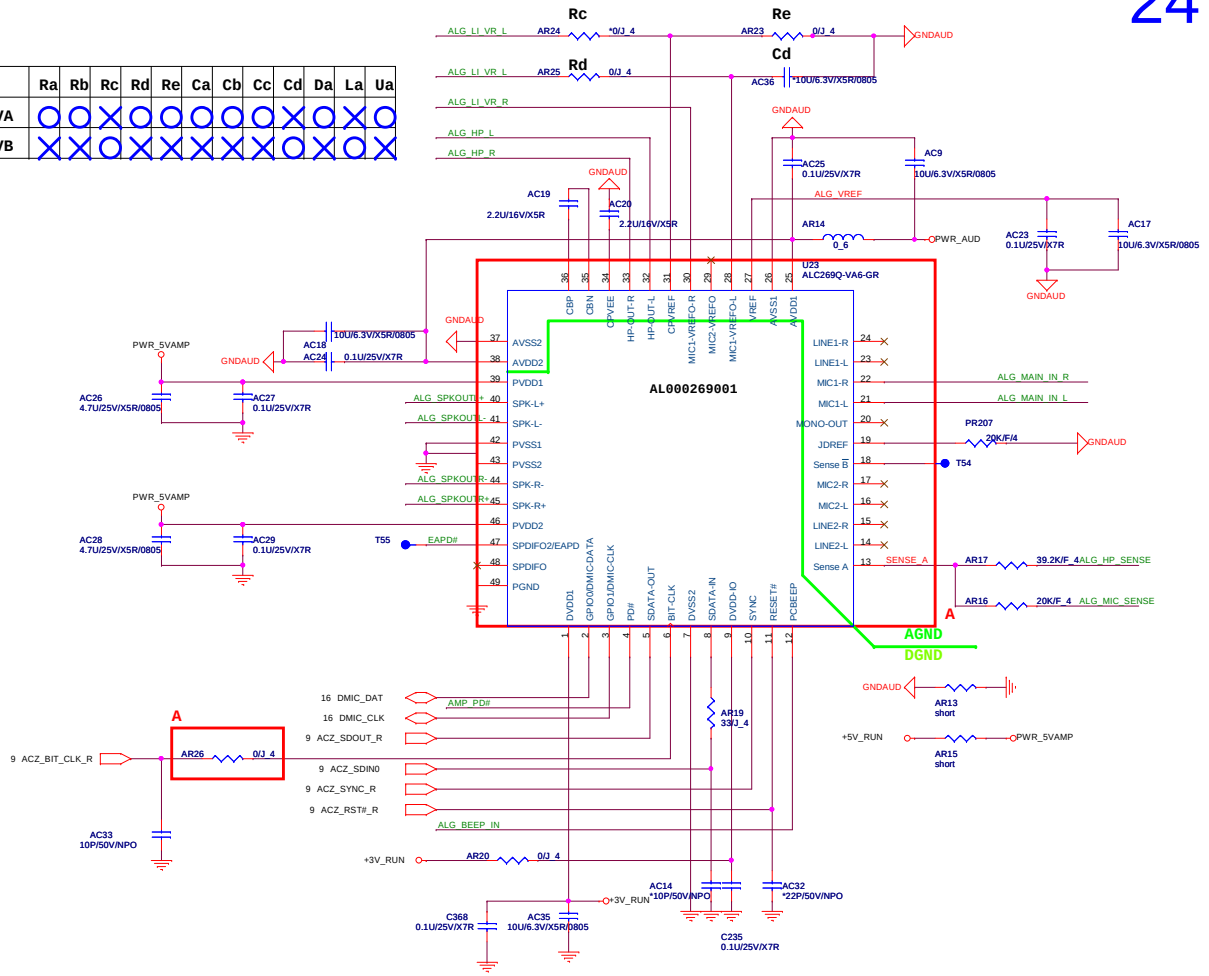
BEEP

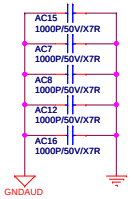


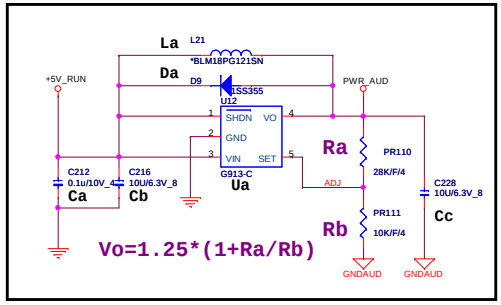
VOLMUTE



U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	O	O	X	O	O	O	O	O	X	O	X	O
ALC269Q-VB	X	X	O	X	X	X	X	X	O	X	O	X







Quanta Computer Inc.
PROJECT : FH2
Size
Document Number
CODEC (ALC269)
Rev 1A
Date: Monday, December 21, 2009
Sheet 24 of 38

EC(KBC)

IT8502

Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

BIOS Write Protect

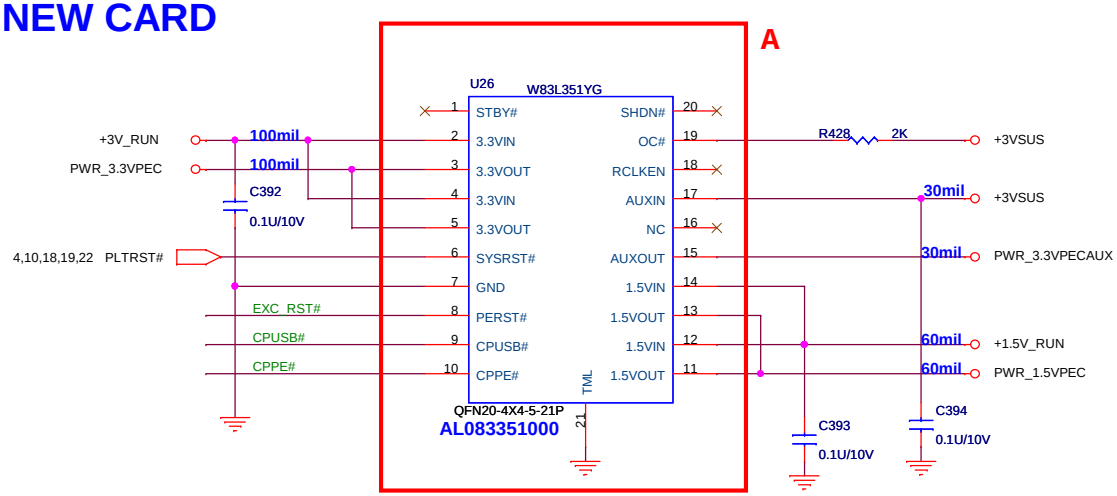
2MB

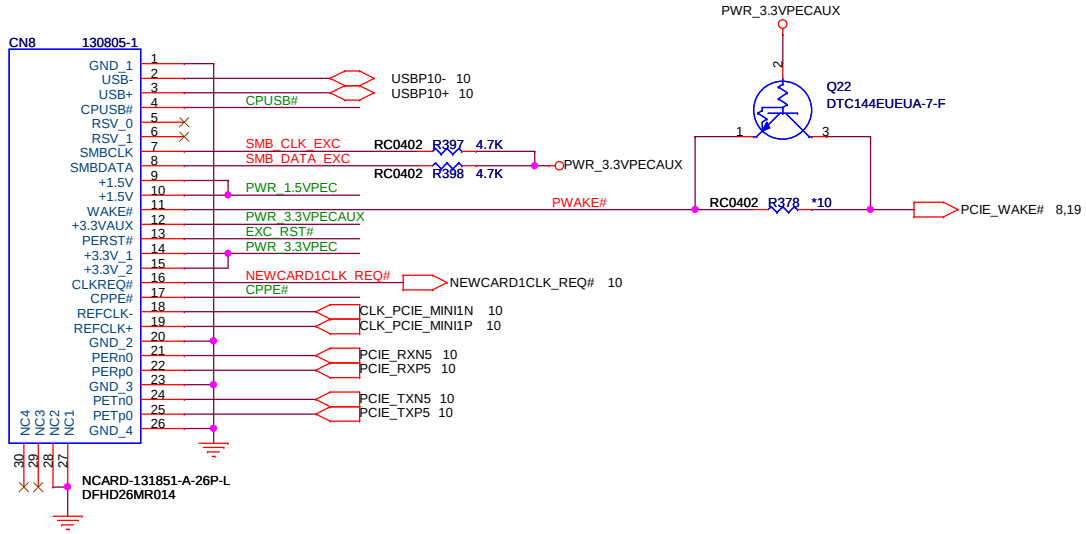
Near ROOM DOOR

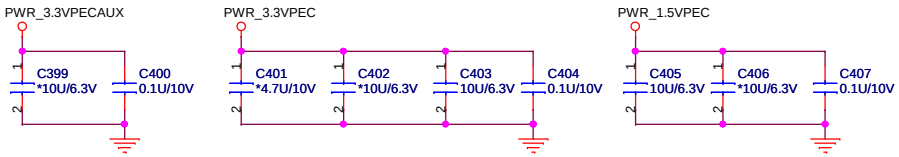
PCB REV	MODEL_ID0	MODEL_ID1
C	LOW	LOW
D	HIGH	LOW
E	LOW	HIGH
F	HIGH	HIGH

Quanta Computer Inc.
PROJECT : FH2
Size | Document Number: EC_ITE8502 | Rev: 1A
Date: Monday, December 21, 2009 | Sheet 25 of 38

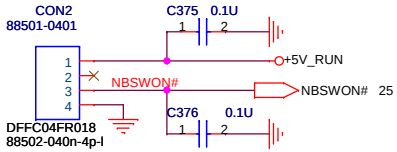
NEW CARD



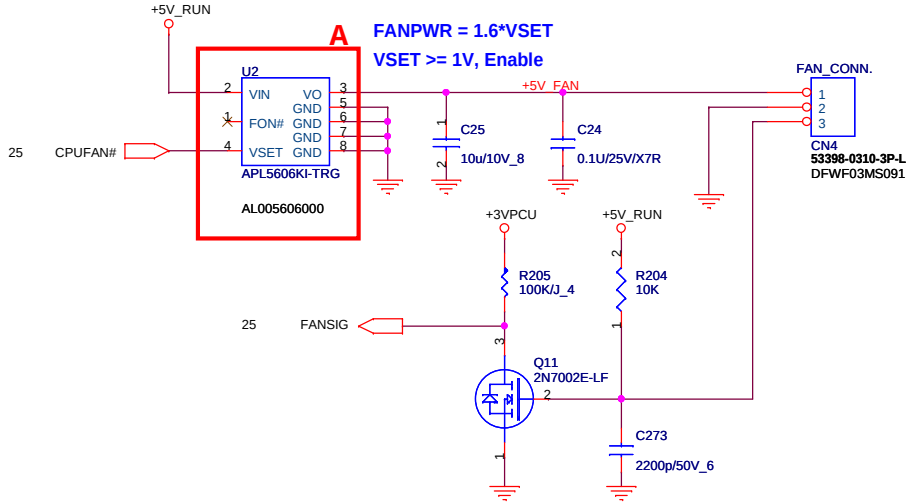




SW BOARD CON



CPU FAN CTRL



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	FAN/SW/NEWCARD	1A

Date: Monday, December 21, 2009 Sheet 26 of 38

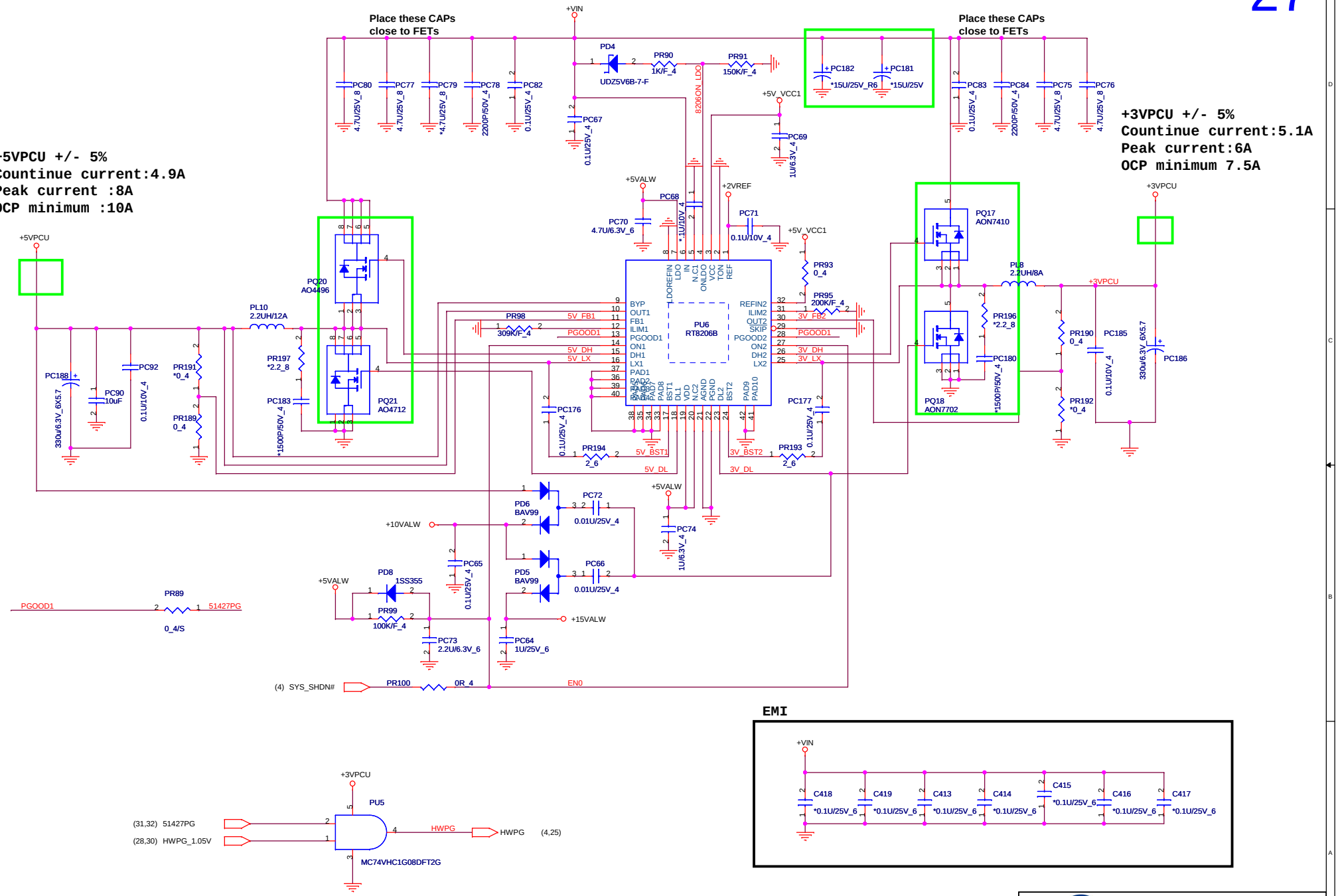
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5VPCU +/- 5%
Countinue current:4.9A
Peak current :8A
OCP minimum :10A

+3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A

Place these CAPs close to FETs

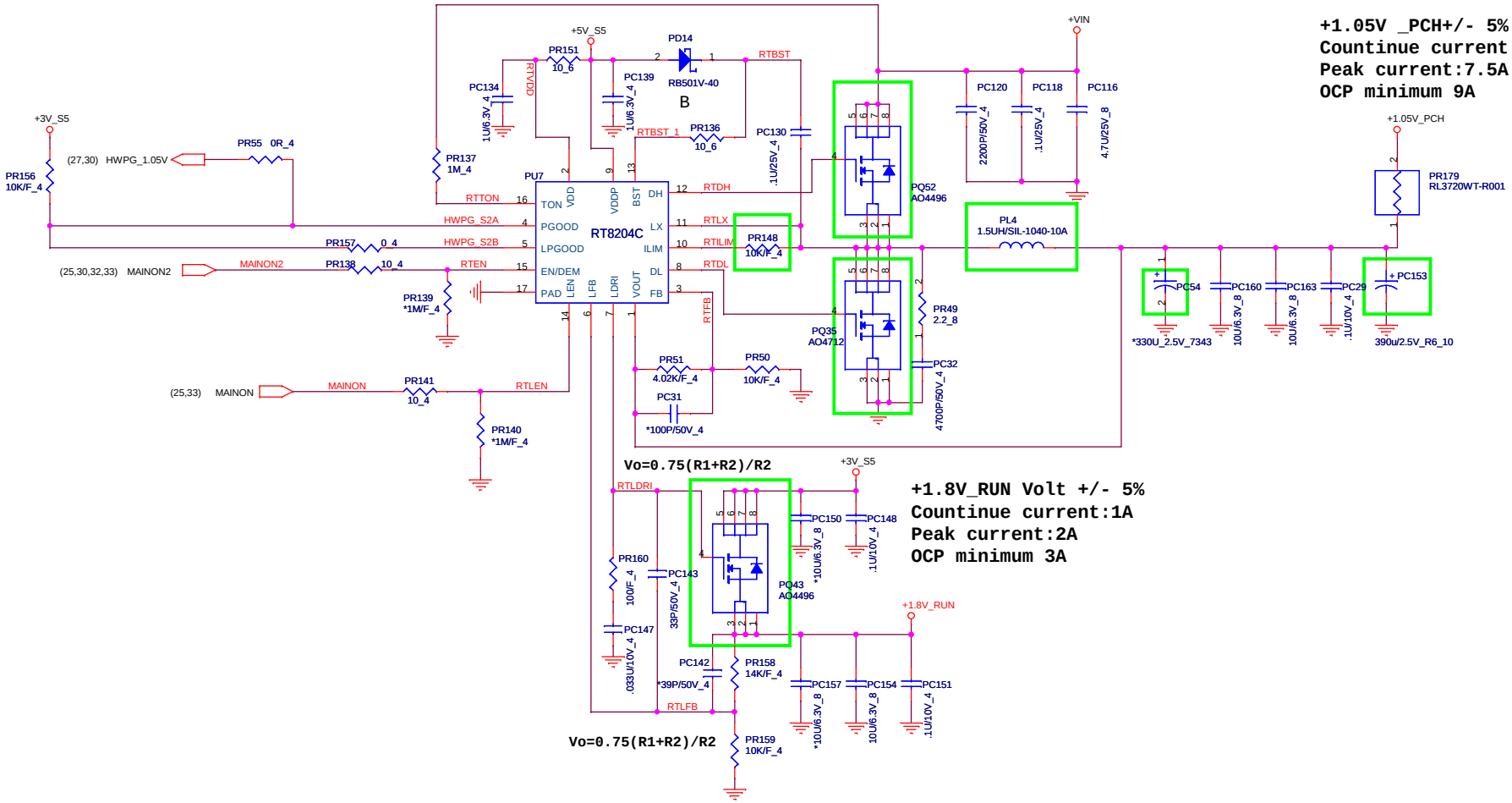
Place these CAPs close to FETs



EMI

Quanta Computer Inc.
PROJECT : FH1

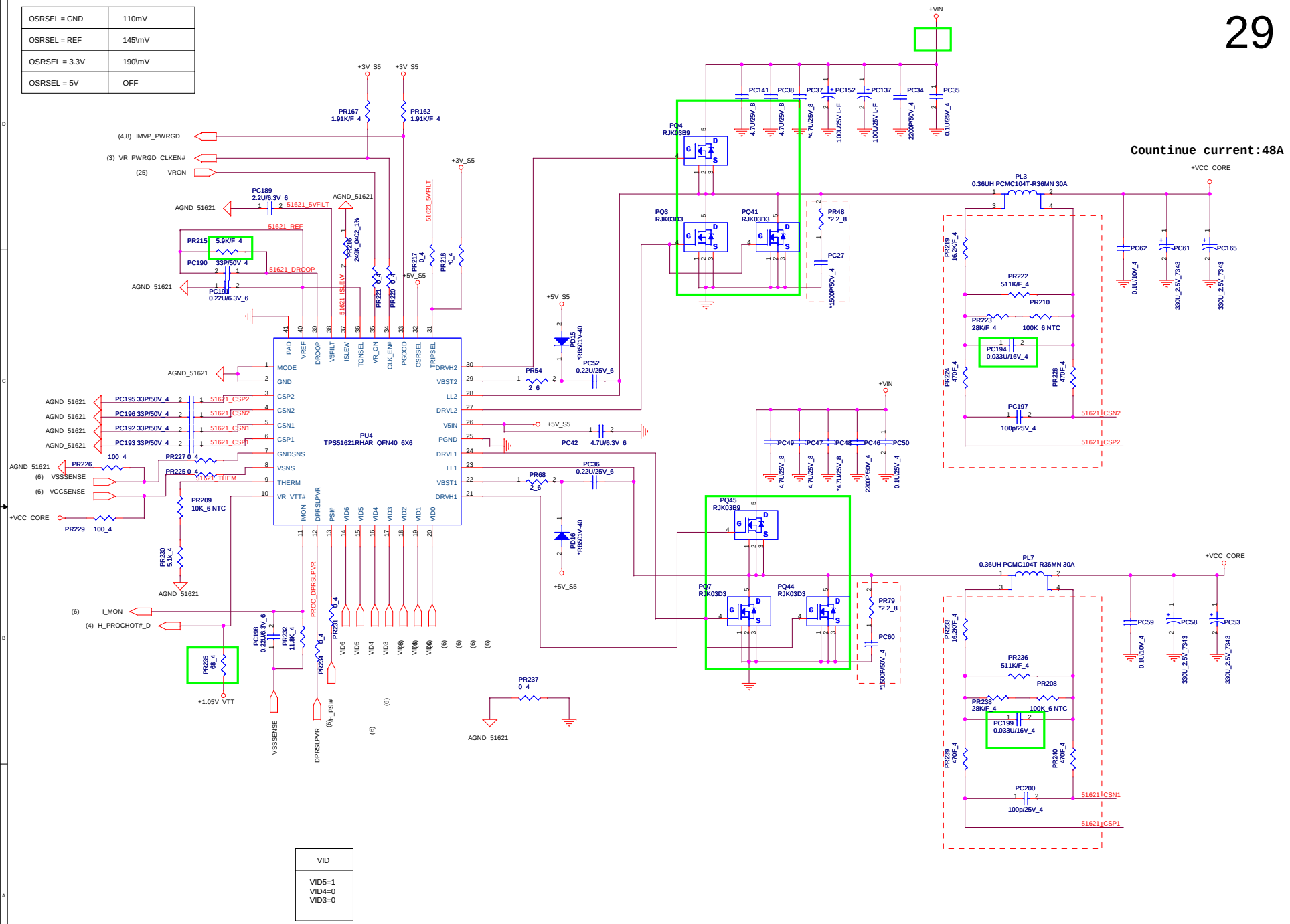
Size	Document Number	Rev
	+5V/+3V (RT8206B)	1A
Date: Monday, December 21, 2009	Sheet 27 of 39	



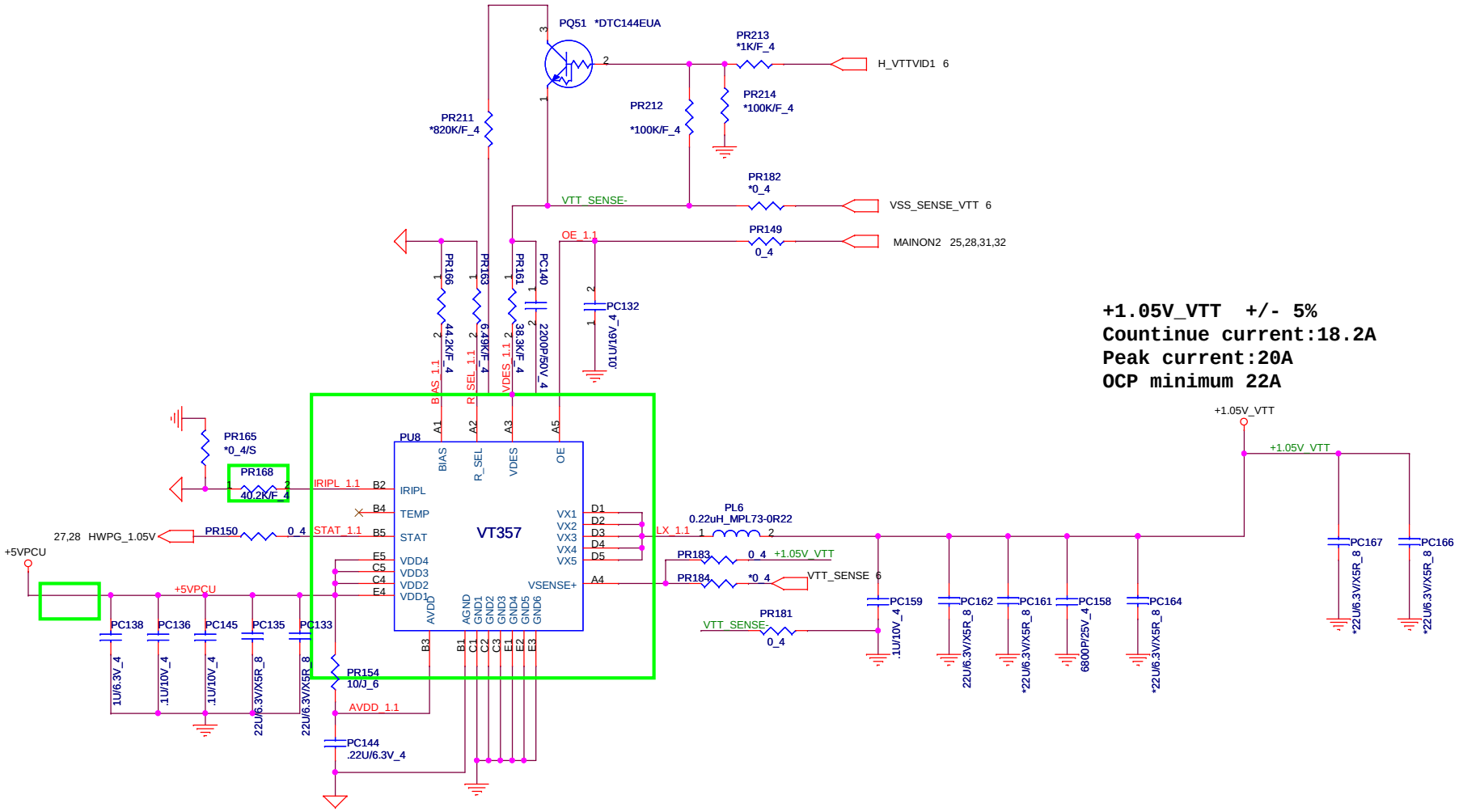
Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: +1.05V/+1.8V (RT8204C)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 28 of 39	

OSRSEL = GND	110mV
OSRSEL = REF	145\mV
OSRSEL = 3.3V	190\mV
OSRSEL = 5V	OFF

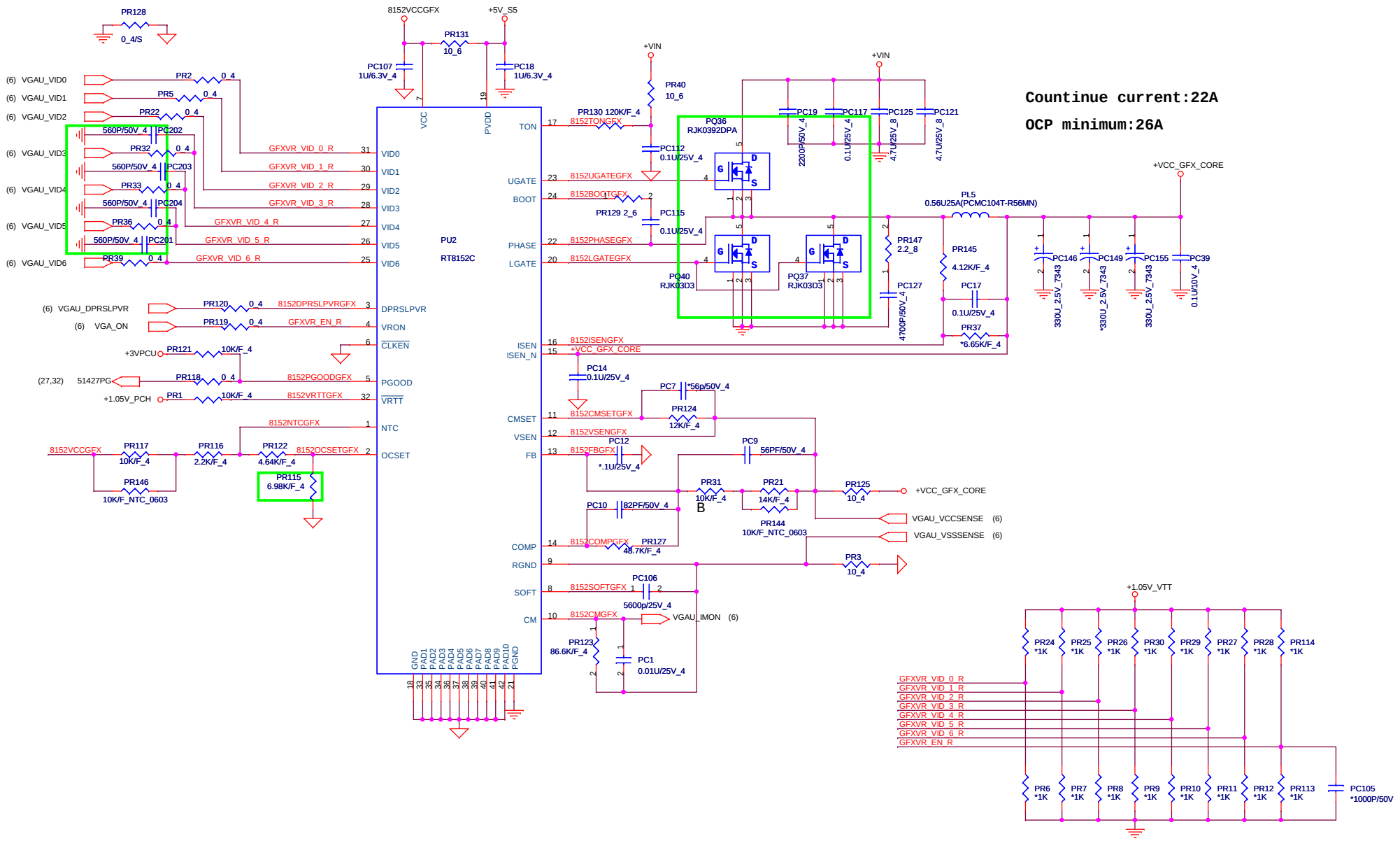
Countinue current:48A



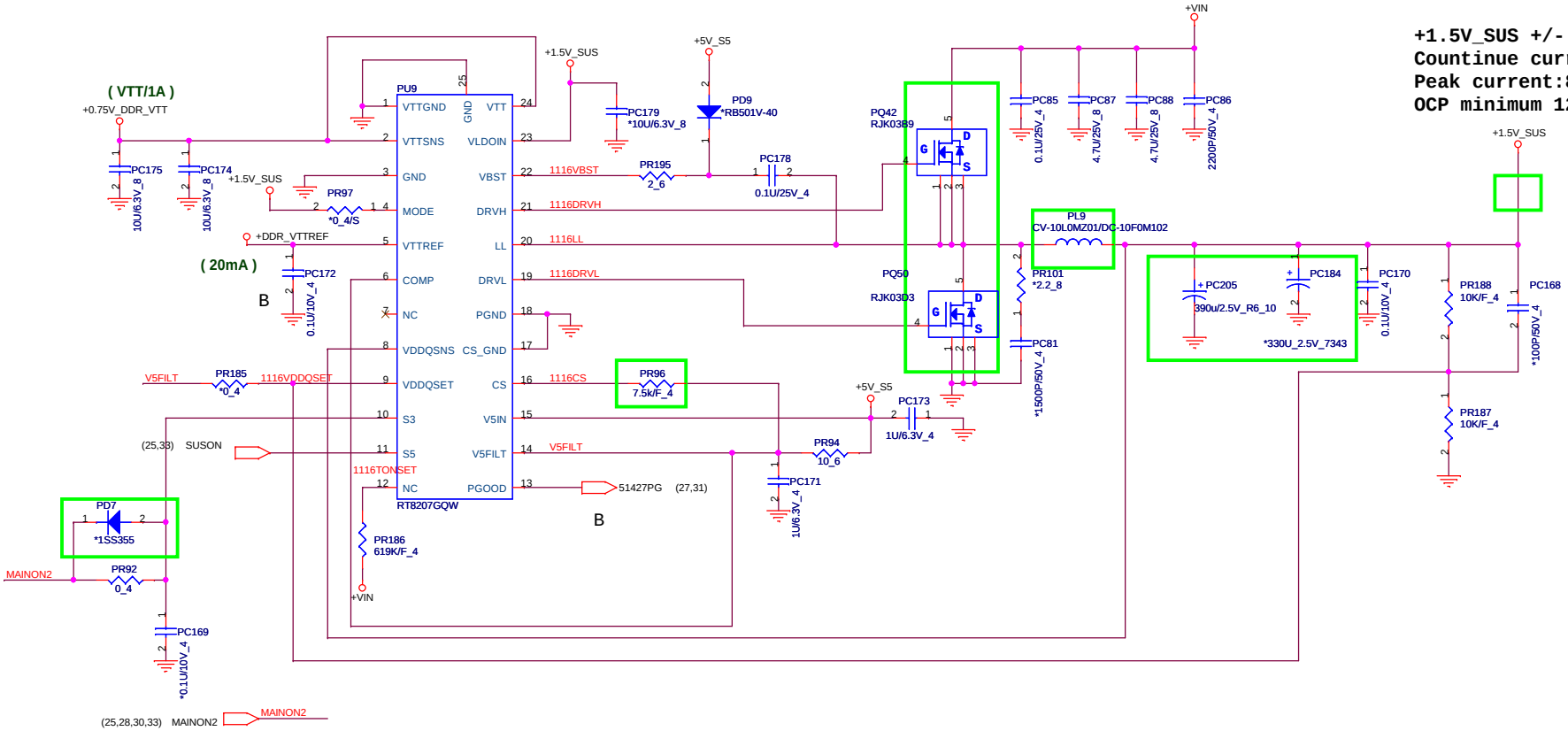
Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	CPU Core (TPS51621)		1A
Date: Monday, December 21, 2009	Sheet 29	of 39	



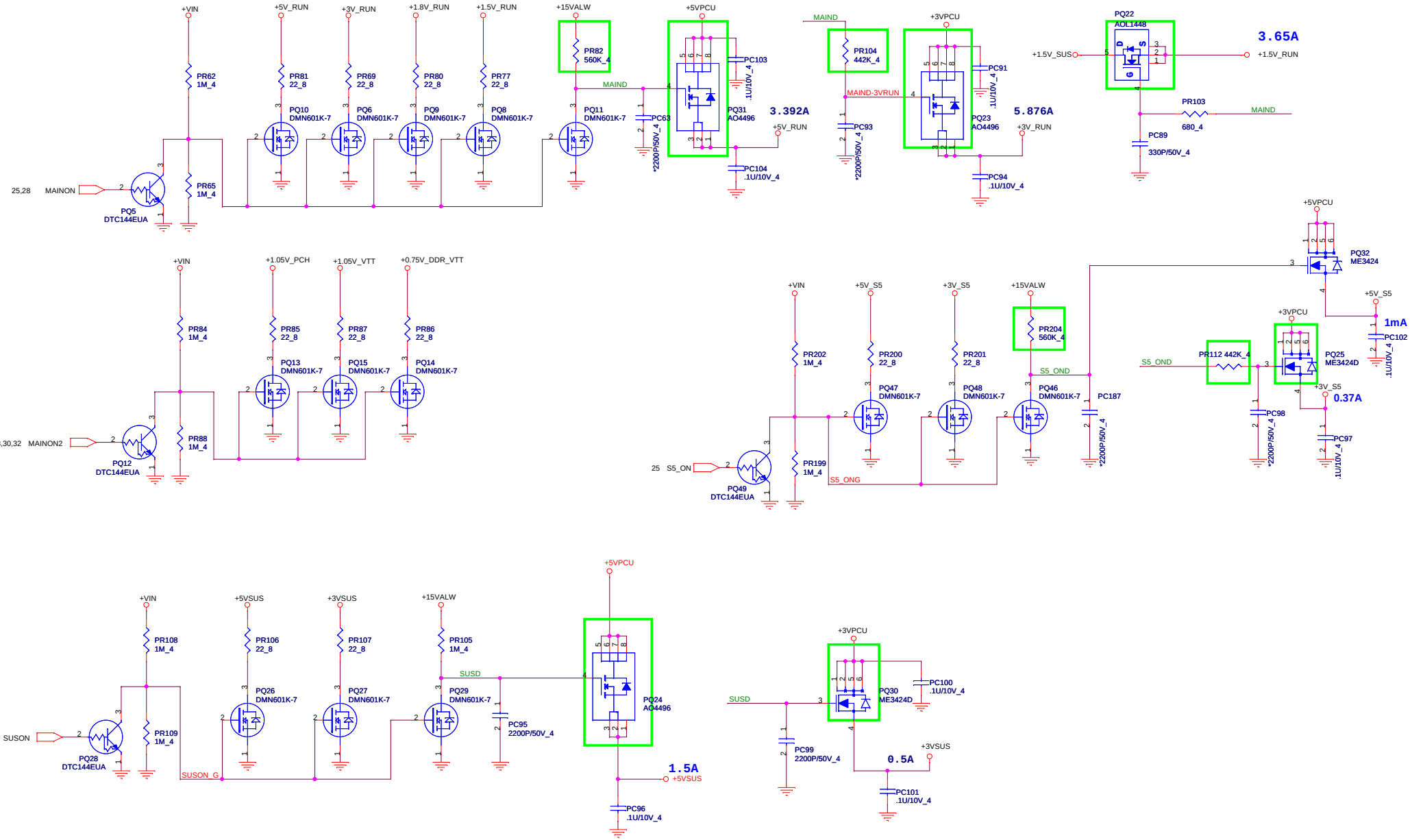
Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number	Rev
	+1.05V_VTT (VT358)	1A
Date: Monday, December 21, 2009	Sheet 30 of 45	



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: UMA GPU CORE (RT8152C)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 31 of 39	

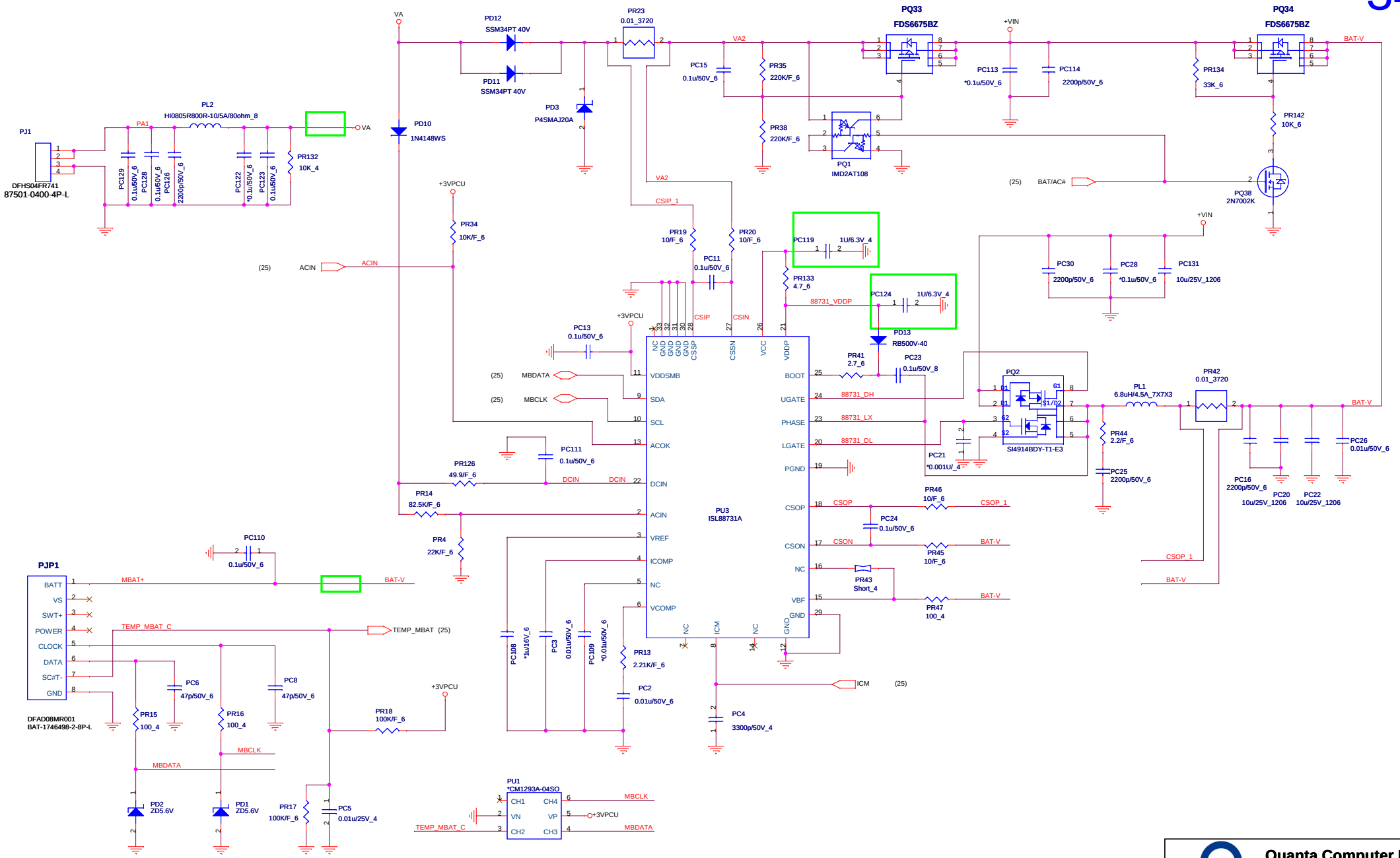


Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 32 of 39	



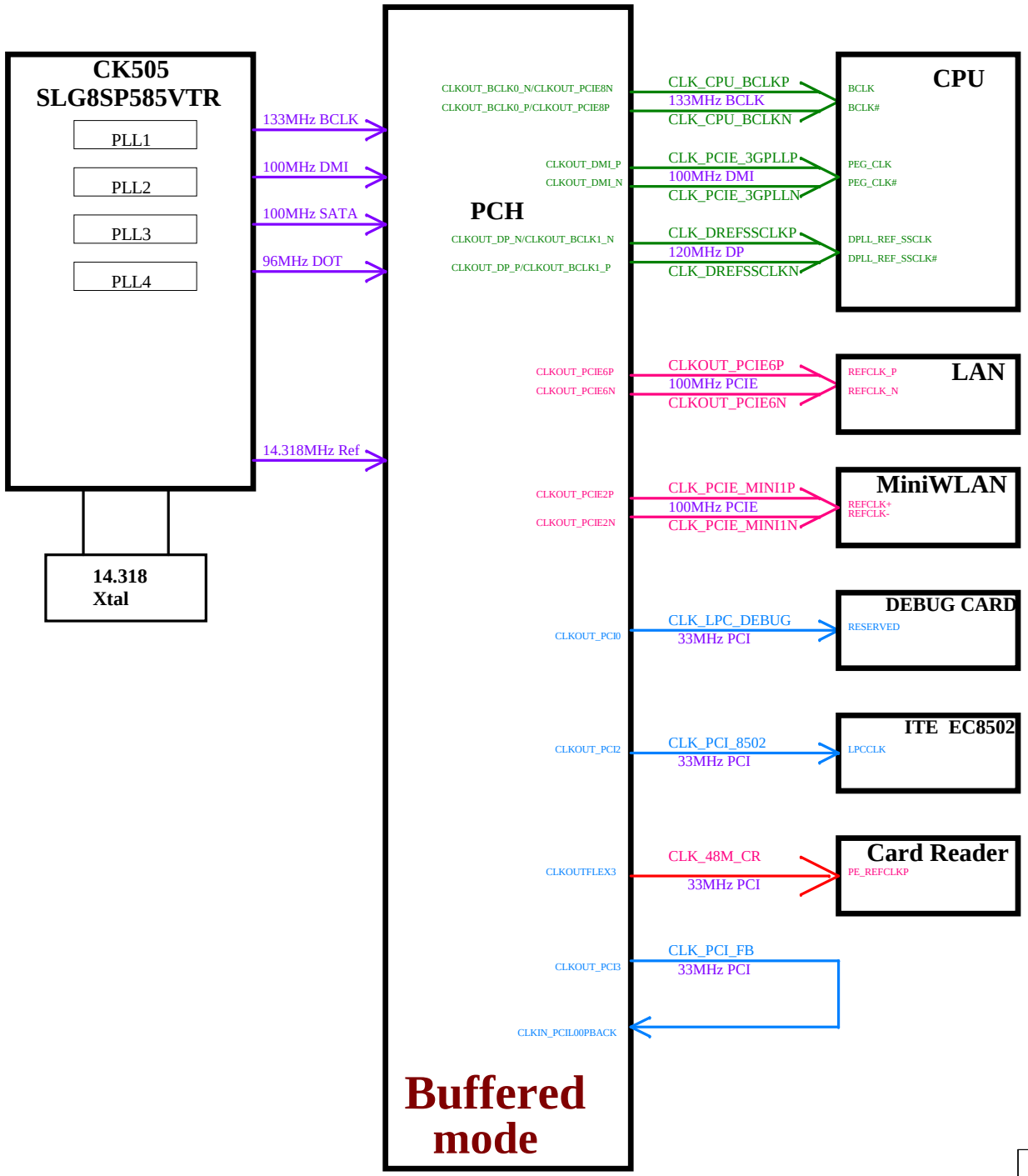
Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	DISCHARGE/3VS5/5VS5/LAN	1A
Date: Monday, December 21, 2009	Sheet 33 of 38	



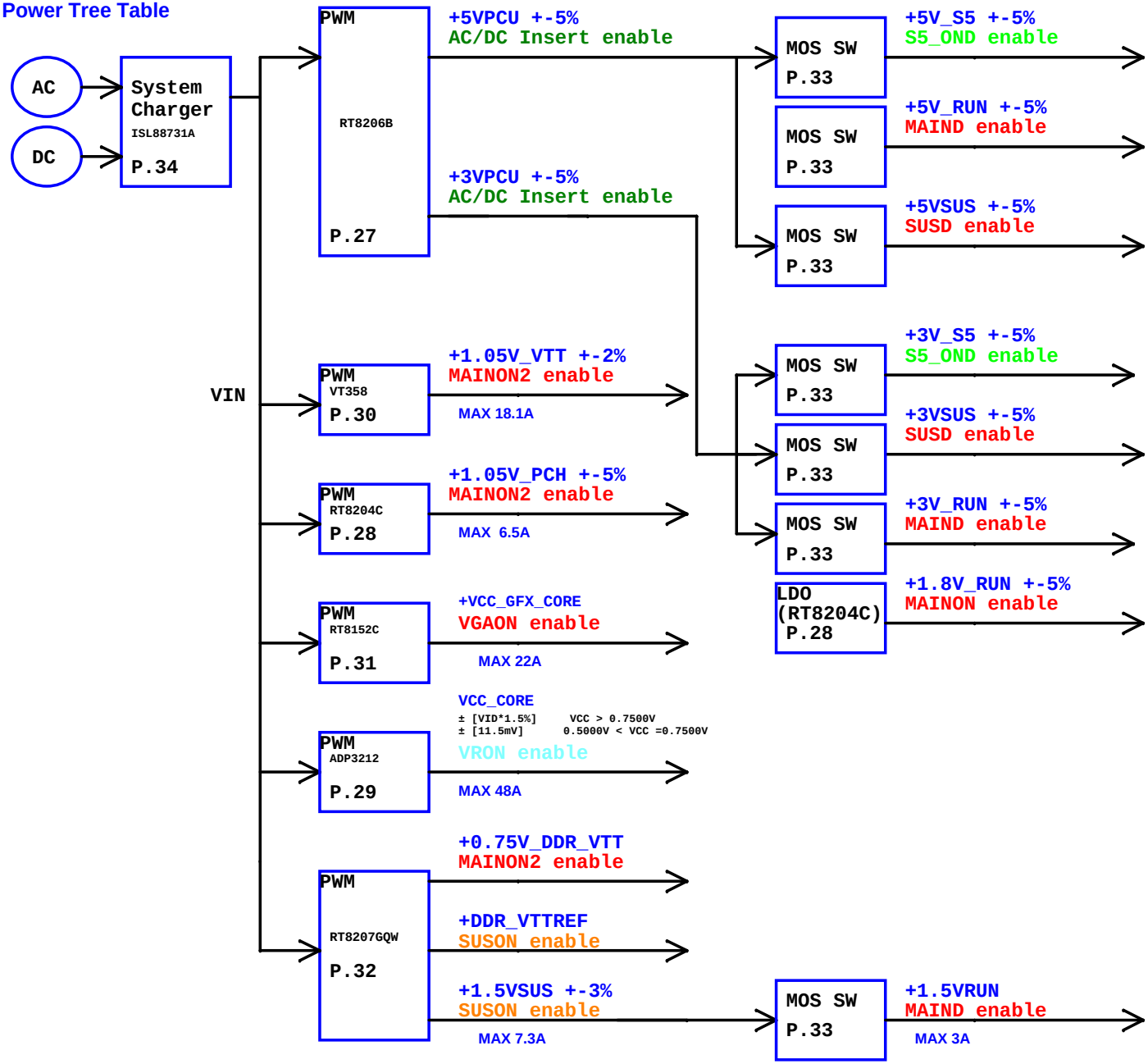
Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	CHARGER (ISL88731)	1A
Date: Monday, December 21, 2009	Sheet 34 of 39	



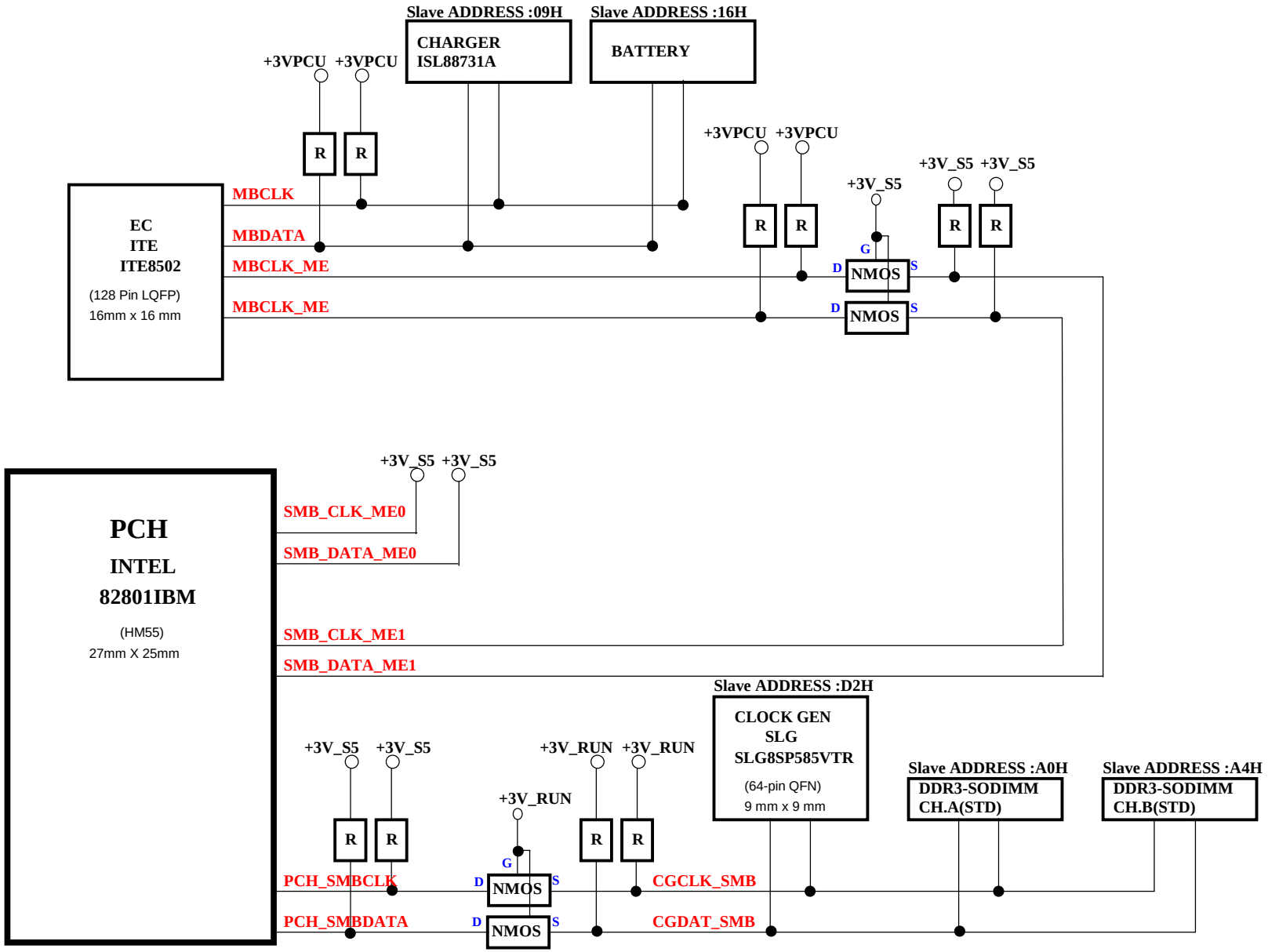
Quanta Computer Inc.
PROJECT : FH2
Clock Distribution
Rev 1A
Monday, December 21, 2009
Sheet 35 of 38

Power Tree Table



Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	Power Tree	1A
Date: Monday, December 21, 2009	Sheet 36 of 38	



Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	SM BUS	1A
Date: Monday, December 21, 2009	Sheet 37 of 38	

CHANGE HISTORY

A

PAGE4 : C370 change to 0.047uF from 1uF

PAGE9 : change R291 and R314 to 3.3K from 10K for intel suggest

PAGE10 : 1.change U4 to MC74VHC1G08DFT2G from TC7SZ32FU(T5L,F,T)
2. R86 non-stuff
3. R283 and R284 change to 2.2K from 6.8K
4. add R353 and R343 4.7K and change SMBus_ME1 pull high to +3VRUN

PAGE11 : change CON11 to battery socket from connector

PAGE 16 : change U14 to IC(5P) APL3512ABI-TRG from G5243AT11U for cost down

PAGE 17 : 1. reserve R427, R429, R430 and R431 for EMI
2. add 1uF C4578,C4579, change C4573, C4574, C4575, C4576 and C4577 to 1uF.
3. change R422 and R423 to 2.2K from 2K.
4. resever U25, U27 and U29 for ESD

PAGE 18 : change CN2 to DFHD23MS0B6

PAGE 19 : 1.mount R562, R565 no stuff for ISOLATE# signal control
2. delete C567, C656 and C655
3. mount R557, delete R576,R191, C567,C656,C655, and reserve R561,R560.
4. delete R585 and R586.
5.add R194, R195 for LAN GND

PAGE 21 : swap L10 and L13 usb signal for layout.

PAGE 22 : 1.change JSIM1 footprint to SIM-CE01X-3-14P-SMT
2. change +3V_3G to +3V_RUN

PAGE 23 : reserve D28 for 3G LED

PAGE 24 : 1. add AR23, AR24, AR25 and AC36 for ALC269-VA and AL269-VB co-layout
2. change U23 footprint to QFN48-7X7-5-49P-SMT
3. add AC26 0 ohm.

PAGE 25 : 1.add T15, T56, T57, T58, T59, T60, T61, T62, T63, T64, T65 and T66 for debug
2. add PCB revsion table
3. mountR365 and R368; non-stuff R367, R366, R369 and R370

PAGE 26 : 1. change U2 to APL5606KI-TRG from G995 for cost down
2. U26 connect Pin4 to +3V_RUN, Pin5 to PWR_3.3VPEC, Pin13 to PWR_1.5VPEC and Pin14 to +1.5V_RUN

PAGE 27 : 1.PL8 changed to choke SMD 5.2UH 5.5A,30% SCDS104R-5R2T-N
2. VIN to GND add C413, C414, C415, C416, C417, C418 and C419 01.uF for EMI
3. PL8 keep original choke (no change)
4. PC181,PC182 non-stuff
5. PQ17 change to AON7410 (BAM74100001)
6. PQ18 change to source AON7702 (BAM77020000)
7. PQ20 change to source AO4496 (BAM44960000)
8. PQ21 change to source AO4712 (BAM47120000)
7.delete PR203,PR102
8.delete PC181, PC182

PAGE 28 : 1.PL4 change to choke coil 1.5UH30%10A (SIL104R-1R5PF) footprint change to choke-etqp4l
2.PC153 change to 390U/2.5V_6X5.8ESR10
3. PL4 change to CHOKE COIL 1.5UH30%10A (SIL104R-1R5PF)
4. PC153 change to 390U/2.5V_6X5.8ESR10
5. delete PC54 BOM
6. PQ35 change to AO4496 (BAM44960000)
7. PQ52 change to source AO4712 (BAM47120000)
8. PQ43 change to source AO4496 (BAM44960000)
9. delete PR179

PAGE 29 : 1.change PR235 to 68ohm from 58 no stuff
2. PR235 change to RES CHIP 68 1/16W +-1 %(0402)
3. PQ4, PQ45 change to RJK03B9DPA (BAM03B90000)
4. PQ3, PQ7, PQ41, PQ44 change to RJK03D3DPA (BAM03D30000)
5. PR215 changed to 5.9K RES CHIP 5.9K 1/16W +-1 %(0402) (CS25902FB10)
6. PC194 and PC199 changed to CAP CHIP 0.033U 16V (+-10%, X7R, 0402)33nF CH3333K1B02
7. Delete PJP0

PAGE 30 : 1.PU8 changed to IC CTRL (25P) VT357FCX-ADJ (CSP-25)
2. PU8 change to IC CTRL (25P) VT357FCX-ADJ (CSP-25)
3. PR168 change to 31.6KF
4.Delete PR180,PJP2
5. PR168 CHANGED TO 40.2K

PAGE 31 : 1.add PC156,PC201,PC202 and PC203 to CAP CHIP 560P 50V(+-10%,X7R,0402)PAL ASN
2. add PC201, PC202, PC203, PC204 560PF
3. PQ36 change to RJK03B9 (BAM03B90000)
4. PQ37, PQ40 change to RJK03D3 (BAM03D30000)

PAGE 32 : 1. change PC184 to 390U/2.5V_6X5.8ESR10
2. PC205=390U/2.5V_6X5.8ESR10.
3. PQ42 change to RJK03B9 (BAM03B90000)
4. PQ50 change to source RJK03D3 (BAM03D30000)
5. delete PC184.
6. add 2nd source PN: DC-10F0M102,(CHOKE 1.0UH +-20% 15A(PCMC104T-1R0MN).
7. delete PD7 BOM
8. delete PR198
9. changed PL9 to DC-33B0M003 CHOKE 3.3UH 11A +-20 %(PCMB104E-3R3MS)

PAGE 33 : 1.PQ24 changed to TRANS MOSFET FDS6690AS (30V,10A)
2. add PQ8 in BOM
3. PQ23, PQ24, PQ31 change to AO4496 (BAM44960000)
4. PQ30, PQ25 change to ME3424D
5. PQ22 CHANGED TO AOL1448 (BAM14480000)
6. PR82 and PR204 CHANGE TO 560K (CS45602FB04)
7. PR104 and PR112 CHANGE TO 442K (CS44422FB00)

PAGE 34 : 1.change PU3 footprint to 'QFN28-5X5-5-33P-smt
2. PC119, PC124 CHANGED TO 0402 TYPE PN: CH5101K9B01
3. delete PF1,PF2

Quanta Computer Inc.
PROJECT : FH2
CHANGE HISTORY