Cover Sheet
02 FM2 DDR3 I/F
03 FM2 PCIE I/F
04 FM2 DISPLAY/MSIC
05 FM2 POWER/GND
06,07 DDR3 DIMM CH-A CH-B
08,09,10,11,12 HUDSON
13 PCIE X16 SLOT & X1 SLOT
14 PCI SLOTs
15 SUPER I/O F71889ED
16 LAN RTL8111E/81105E
17 AUDIO ALC887/VT1708S
18 USB2.0 CONN
19 USB3.0 CONN
20 HDMI CONNECTOR
21 VGA CONNECTOR & FAN
22 LPT/COM/PS2
23 ACPI UPI & SYS POWER
24,25 CPU power
26 CPU_VDD1_2/NB 1.1V/VDDA2.5V
27 DDR POWER
28 ATX & Front Panel
29 BOM OPTION

MS-7721 Ver:3.2

CPU:
AMD FM2

System Chipset:
AMD - Hudson D2 A55 CO-LAY A75

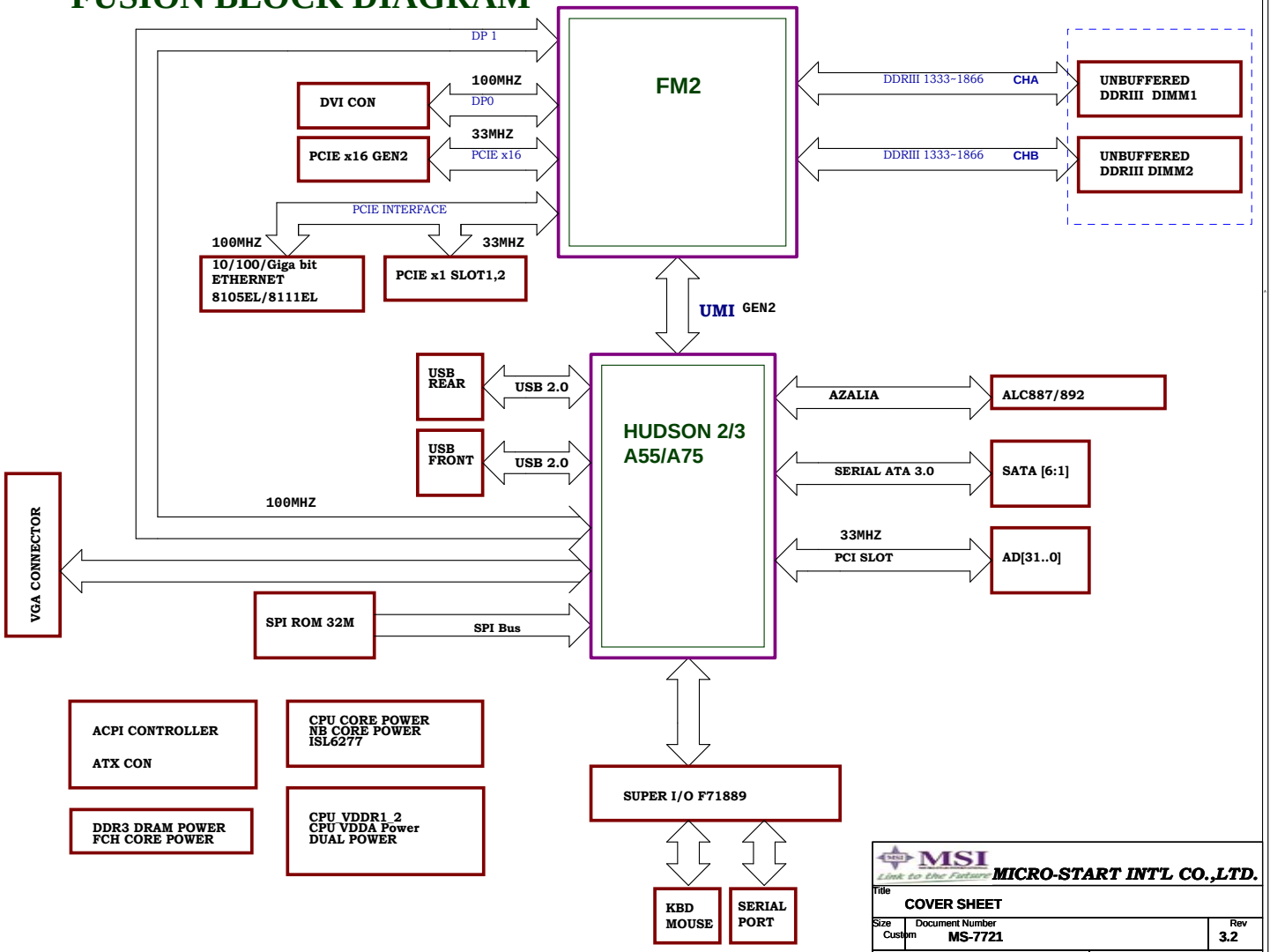
VRM
Controller - ISL62773 3+2

On Board Chipset:
LPC Super I/O --F71889ED
LAN-Realtek 8111E
Azalia CODEC - Realtek ALC887

Main Memory:
DDR III * 2 MAX:16 GB

Expansion Slots:
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Slot * 1

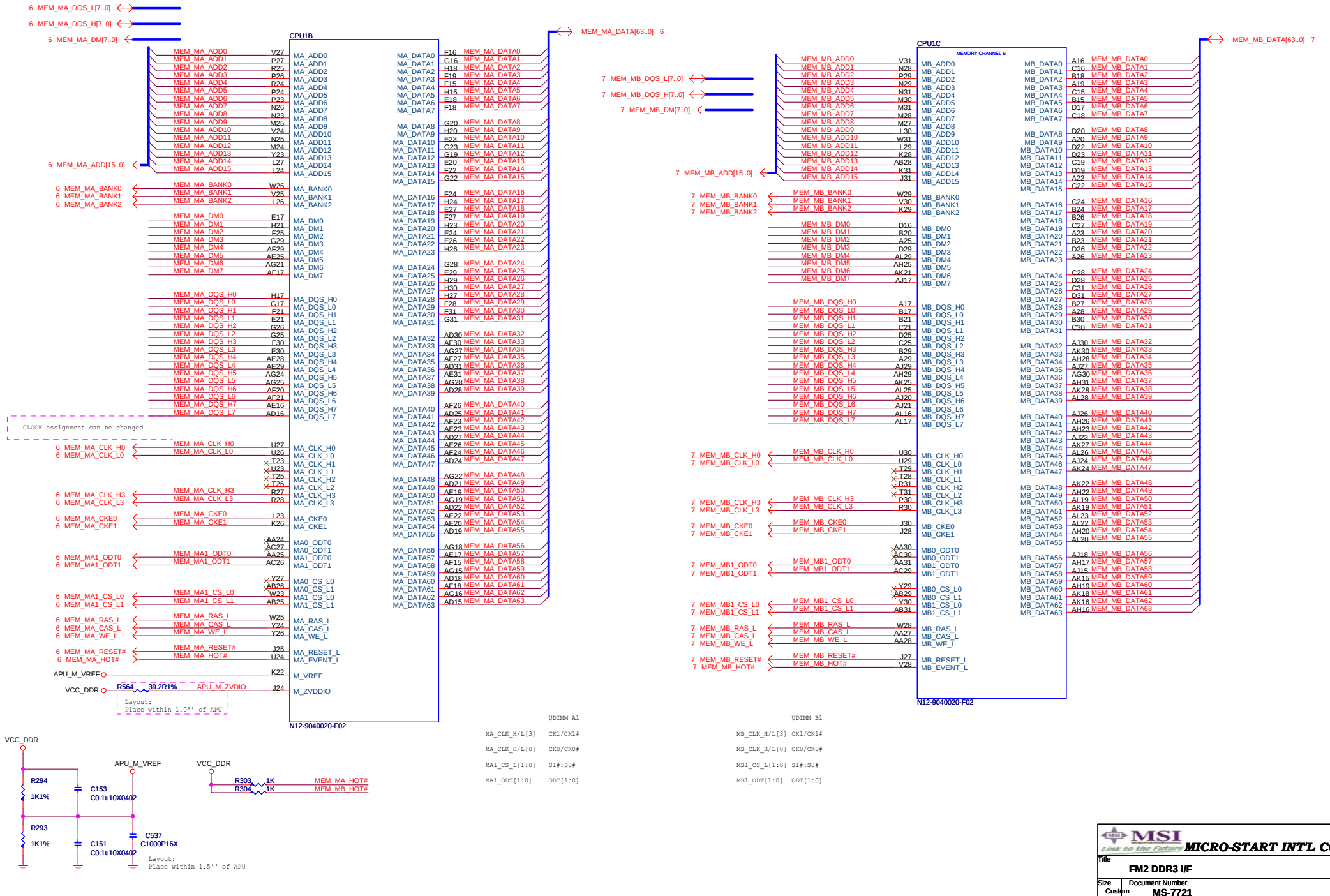
FUSION BLOCK DIAGRAM



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	COVER SHEET	
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 1 of 34	

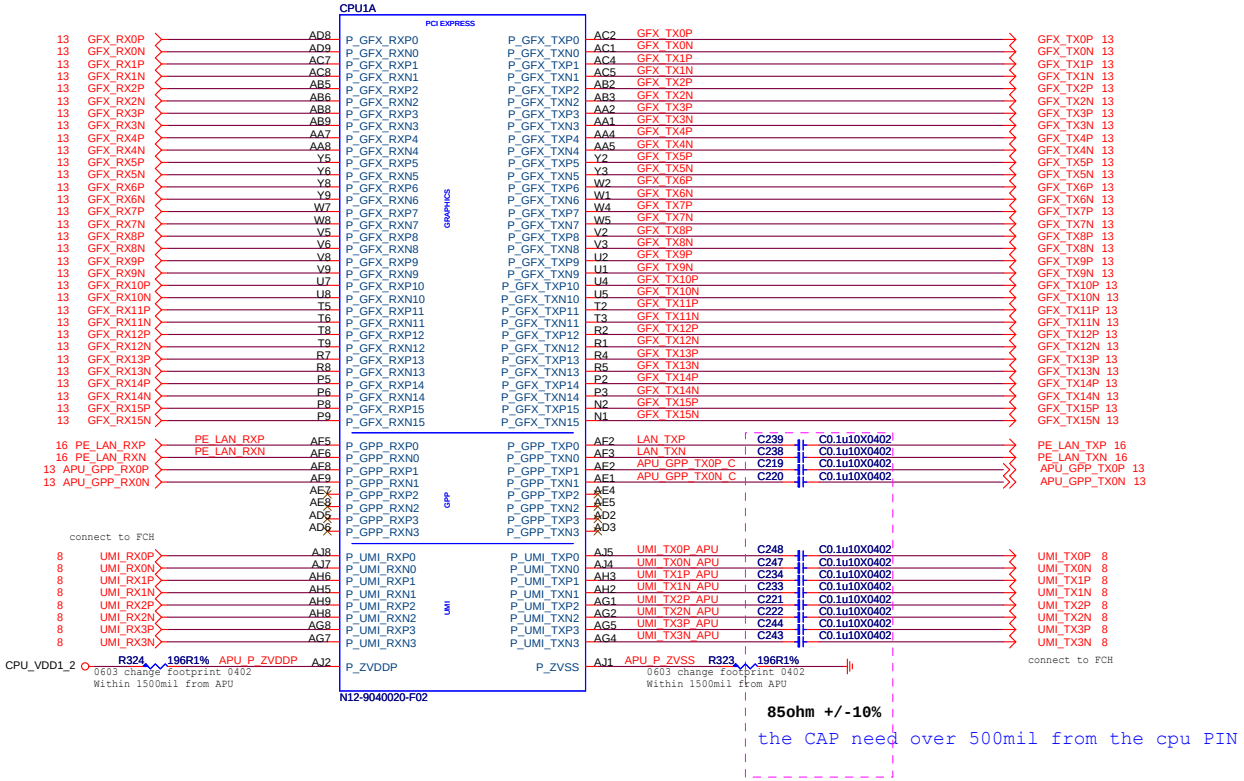
FM2DDR3 I/F



MICRO-START INTL CO.,LTD.

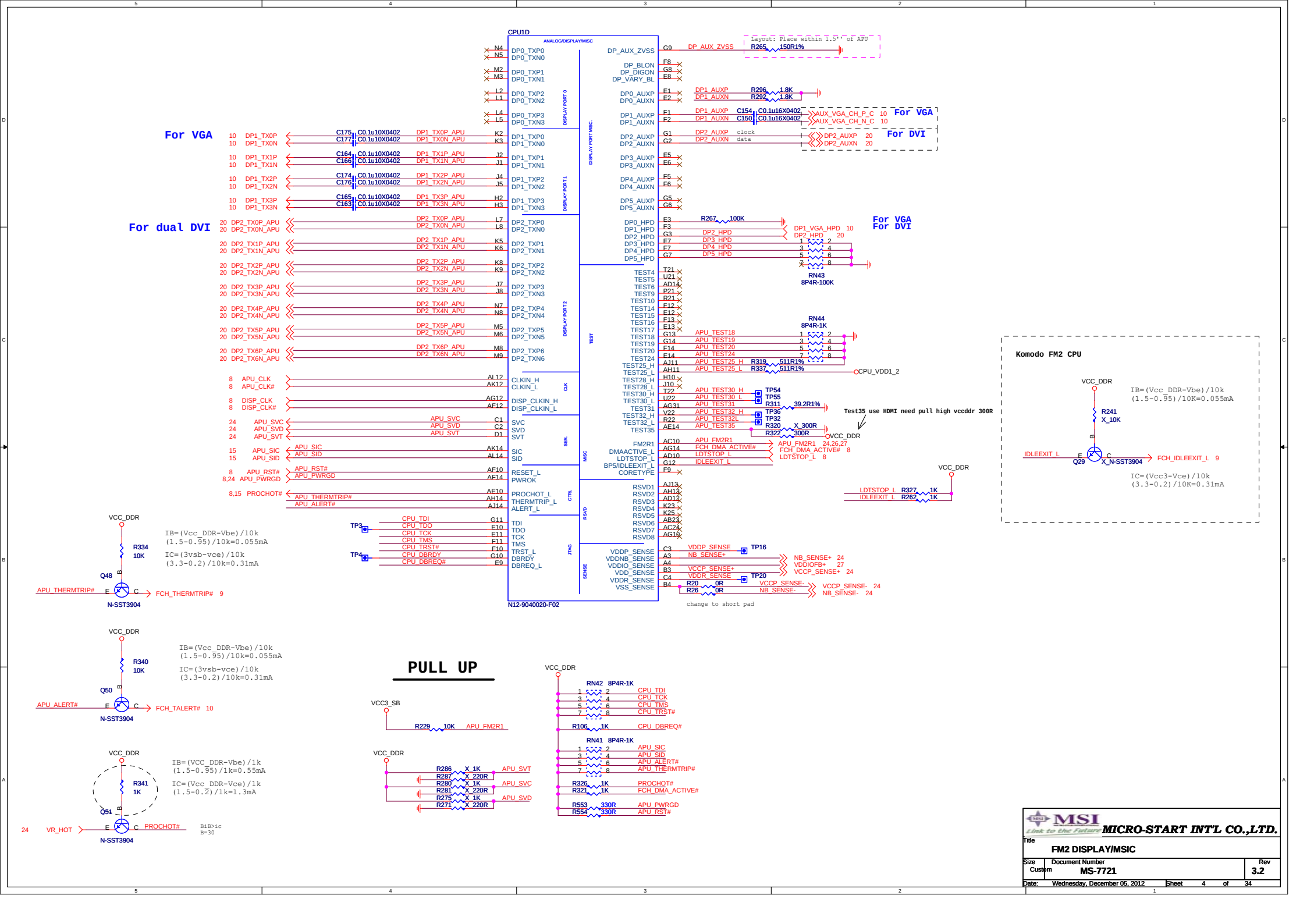
Title	FM2 DDR3 I/F	
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 2 of 34	

FM2 PCIE I/F

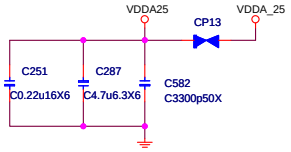


Title	FM2 PCIE I/F
Size	Custom
Document Number	MS-7721
Rev	3.2
Date:	Tuesday, December 04, 2012
Sheet	3 of 34

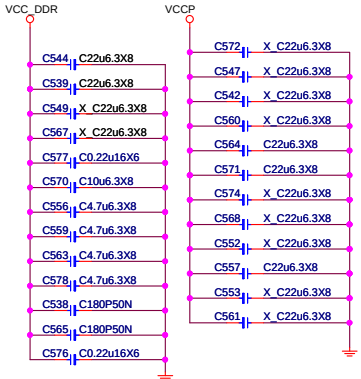
MICRO-START INT'L CO.,LTD.

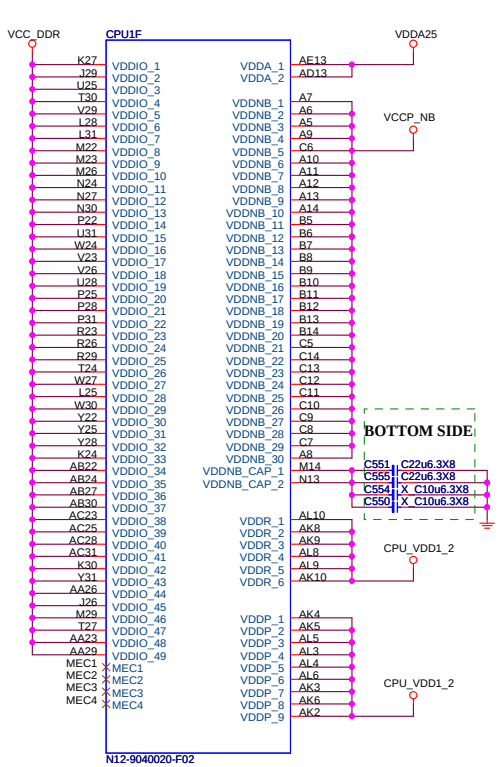

CPU1D
ANALOG/DISPLAY/MISC
DP0_TXP0
DP0_TXN0
DP0_TXP1
DP0_TXN1
DP0_TXP2
DP0_TXN2
DP0_TXP3
DP0_TXN3
DISPLAY PORT 0
DP1_TXP0
DP1_TXN0
DP1_TXP1
DP1_TXN1
DP1_TXP2
DP1_TXN2
DP1_TXP3
DP1_TXN3
DISPLAY PORT 1
DP2_TXP0
DP2_TXN0
DP2_TXP1
DP2_TXN1
DP2_TXP2
DP2_TXN2
DP2_TXP3
DP2_TXN3
DISPLAY PORT 2
DISPLAY PORT MISC.
CLKIN_H
CLKIN_L
DISP_CLKIN_H
DISP_CLKIN_L
CLK
SVC
SVD
SVT
SIC
SID
SER.
RESET_L
PWROK
PROCHOT_L
THERMTRIP_L
ALERT_L
MISC
CTRL
TDI
TDO
TCK
TMS
TRST_L
DBRDY
DBREQ_L
JTAG
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD
VDDP_SENSE
VDDNB_SENSE
VDDIO_SENSE
VDD_SENSE
VDDR_SENSE
VSS_SENSE
SENSE
DP_AUX_ZVSS
DP_BLON
DP_DIGON
DP_VARY_BL
DP0_AUXP
DP0_AUXN
DP1_AUXP
DP1_AUXN
DP2_AUXP
DP2_AUXN
DP3_AUXP
DP3_AUXN
DP4_AUXP
DP4_AUXN
DP5_AUXP
DP5_AUXN
DP0_HPD
DP1_HPD
DP2_HPD
DP3_HPD
DP4_HPD
DP5_HPD
TEST4
TEST5
TEST6
TEST9
TEST10
TEST14
TEST15
TEST16
TEST17
TEST18
TEST19
TEST20
TEST24
TEST25_H
TEST25_L
TEST28_H
TEST28_L
TEST30_H
TEST30_L
TEST31
TEST32_H
TEST32_L
TEST35
TEST
N12-9040020-F02
Layout: Place within 1.5" of APU
DP_AUX_ZVSS
R265 150R1%
DP1_AUXP
DP1_AUXN
R296 1.8K
R292 1.8K
C154 C0.1u16X0402
C150 C0.1u16X0402
AUX_VGA_CH_P_C 10
AUX_VGA_CH_N_C 10
For VGA
For DVI
DP2_AUXP clock
DP2_AUXN data
DP2_AUXP 20
DP2_AUXN 20
For VGA
10 DP1_TX0P
10 DP1_TX0N
C175 C0.1u10X0402
C177 C0.1u10X0402
DP1_TX0P_APU
DP1_TX0N_APU
10 DP1_TX1P
10 DP1_TX1N
C164 C0.1u10X0402
C166 C0.1u10X0402
DP1_TX1P_APU
DP1_TX1N_APU
10 DP1_TX2P
10 DP1_TX2N
C174 C0.1u10X0402
C176 C0.1u10X0402
DP1_TX2P_APU
DP1_TX2N_APU
10 DP1_TX3P
10 DP1_TX3N
C165 C0.1u10X0402
C163 C0.1u10X0402
DP1_TX3P_APU
DP1_TX3N_APU
For dual DVI
20 DP2_TX0P_APU
20 DP2_TX0N_APU
20 DP2_TX1P_APU
20 DP2_TX1N_APU
20 DP2_TX2P_APU
20 DP2_TX2N_APU
20 DP2_TX3P_APU
20 DP2_TX3N_APU
20 DP2_TX4P_APU
20 DP2_TX4N_APU
20 DP2_TX5P_APU
20 DP2_TX5N_APU
20 DP2_TX6P_APU
20 DP2_TX6N_APU
8 APU_CLK
8 APU_CLK#
8 DISP_CLK
8 DISP_CLK#
24 APU_SVC
24 APU_SVD
24 APU_SVT
15 APU_SIC
15 APU_SID
8 APU_RST#
8,24 APU_PWRGD
8,15 PROCHOT#
APU_THERMTRIP#
APU_ALERT#
R267 100K
DP1_VGA_HPD 10
DP2_HPD 20
DP3_HPD
DP4_HPD
DP5_HPD
RN43
8P4R-100K
For VGA
For DVI
RN44
8P4R-1K
APU_TEST18
APU_TEST19
APU_TEST20
APU_TEST24
APU_TEST25_H
APU_TEST25_L
R319 511R1%
R337 511R1%
CPU_VDD1_2
APU_TEST30_H
APU_TEST30_L
APU_TEST31
APU_TEST32_H
APU_TEST32L
APU_TEST35
TP54
TP55
R311 39.2R1%
TP36
TP32
R320 X_300R
R322 300R
Test35 use HDMI need pull high vccddr 300R
VCC_DDR
APU_FM2R1
FCH_DMA_ACTIVE#
LDTSTOP_L
IDLEEXIT_L
APU_FM2R1 24,26,27
FCH_DMA_ACTIVE# 8
LDTSTOP_L 8
Komodo FM2 CPU
VCC_DDR
IB=(Vcc_DDR-Vbe)/10k
(1.5-0.95)/10K=0.055mA
R241
X_10K
IDLEEXIT_L
Q29
X_N-SST3904
FCH_IDLEEXIT_L 9
IC=(Vcc3-Vce)/10k
(3.3-0.2)/10K=0.31mA
LDTSTOP_L R327 1K
IDLEEXIT_L R262 1K
VCC_DDR
R334
10K
Q48
N-SST3904
APU_THERMTRIP#
FCH_THERMTRIP# 9
IB=(Vcc_DDR-Vbe)/10k
(1.5-0.95)/10k=0.055mA
IC=(3vsb-vce)/10k
(3.3-0.2)/10k=0.31mA
TP3
TP4
CPU_TDI
CPU_TDO
CPU_TCK
CPU_TMS
CPU_TRST#
CPU_DBRDY
CPU_DBREQ#
VDDP_SENSE
NB_SENSE+
VCCP_SENSE+
VDDR_SENSE
TP16
TP20
R20 0R
R26 0R
VCCP_SENSE-
NB_SENSE-
NB_SENSE+ 24
VDDIOFB+ 27
VCCP_SENSE+ 24
VCCP_SENSE- 24
NB_SENSE- 24
change to short pad
VCC_DDR
R340
10K
Q50
N-SST3904
APU_ALERT#
FCH_TALERT# 10
IB=(Vcc_DDR-Vbe)/10k
(1.5-0.95)/10k=0.055mA
IC=(3vsb-vce)/10k
(3.3-0.2)/10k=0.31mA
PULL UP
VCC3_SB
R229 10K APU_FM2R1
VCC_DDR
R286 X_1K APU_SVT
R287 X_220R
R280 X_1K APU_SVC
R281 X_220R
R275 X_1K APU_SVD
R271 X_220R
VCC_DDR
RN42 8P4R-1K
CPU_TDI
CPU_TCK
CPU_TMS
CPU_TRST#
R106 1K CPU_DBREQ#
RN41 8P4R-1K
APU_SIC
APU_SID
APU_ALERT#
APU_THERMTRIP#
R326 1K PROCHOT#
R321 1K FCH_DMA_ACTIVE#
R553 330R APU_PWRGD
R554 330R APU_RST#
VCC_DDR
R341
1K
Q51
N-SST3904
24 VR_HOT
PROCHOT#
IB=(VCC_DDR-Vbe)/1k
(1.5-0.95)/1k=0.55mA
IC=(Vcc_DDR-Vce)/1k
(1.5-0.2)/1k=1.3mA
BiB>ic
B=30
MSI
Link to the Future
MICRO-START INTL CO.,LTD.
Title
FM2 DISPLAY/MSIC
Size
Custom
Document Number
MS-7721
Rev
3.2
Date: Wednesday, December 05, 2012
Sheet 4 of 34

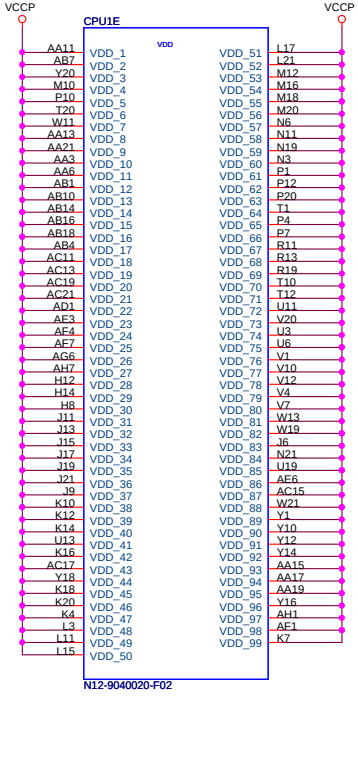
VCC_DDR 5A
VDDA 0.9A
VCCP_NB 41A
CPU_VDD1_2 = VDDR 4A +VDDP 6A
VCCP 60A,90A,110A

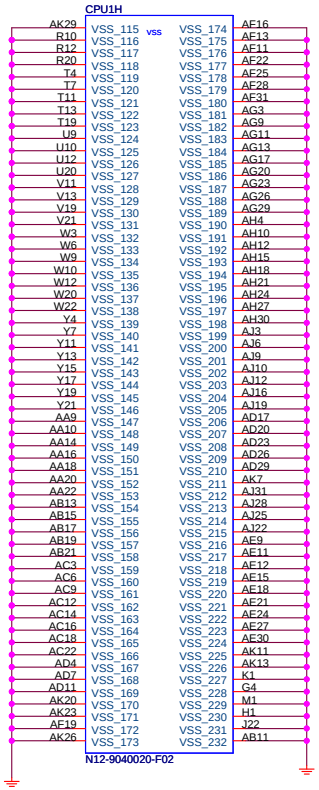


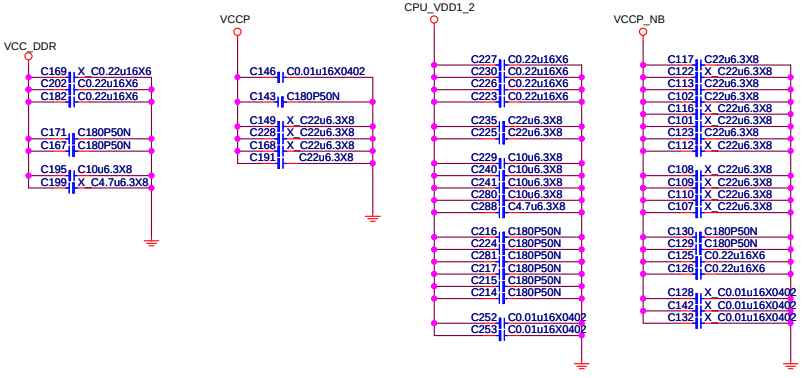
BOTTOM SIDE









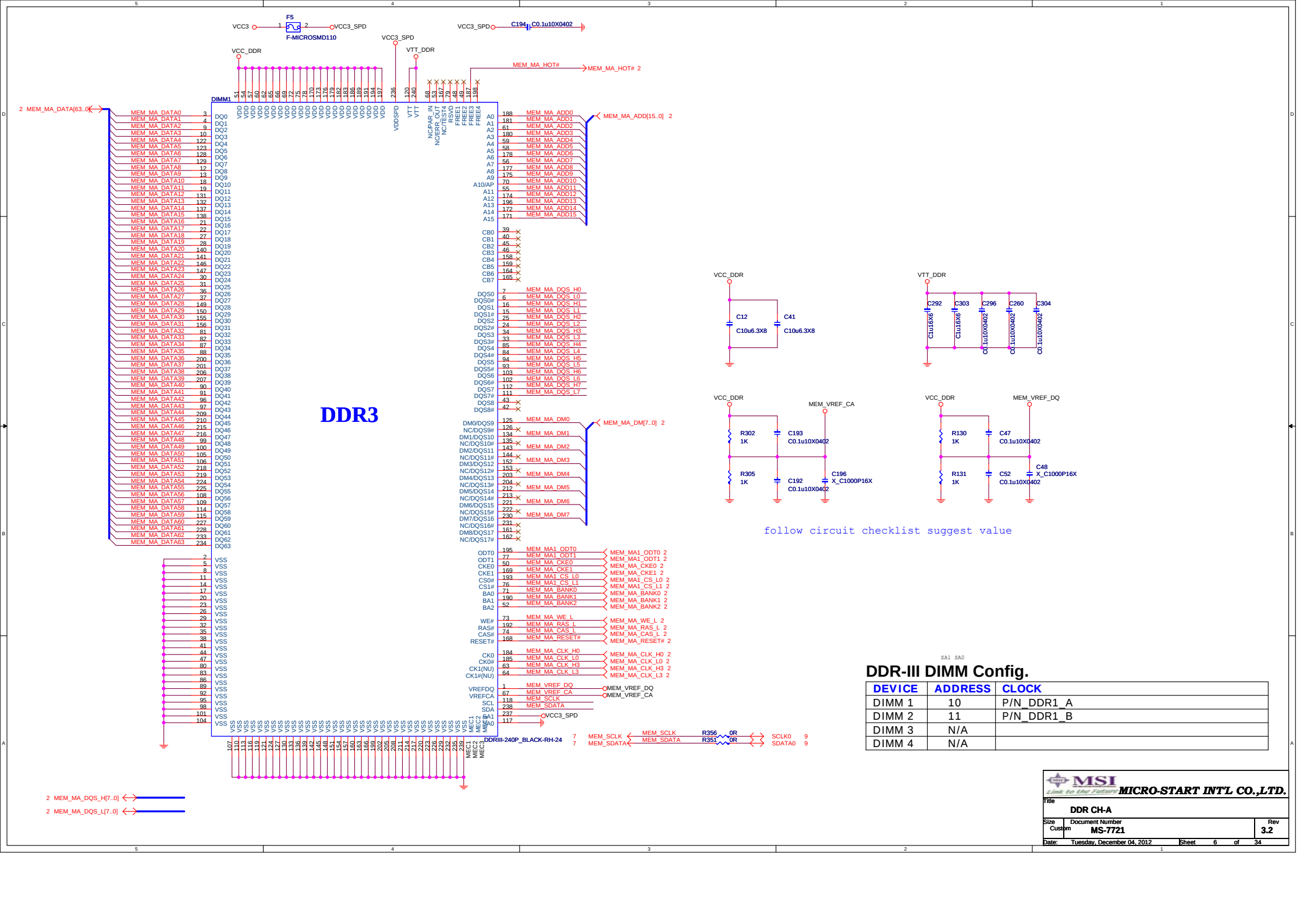


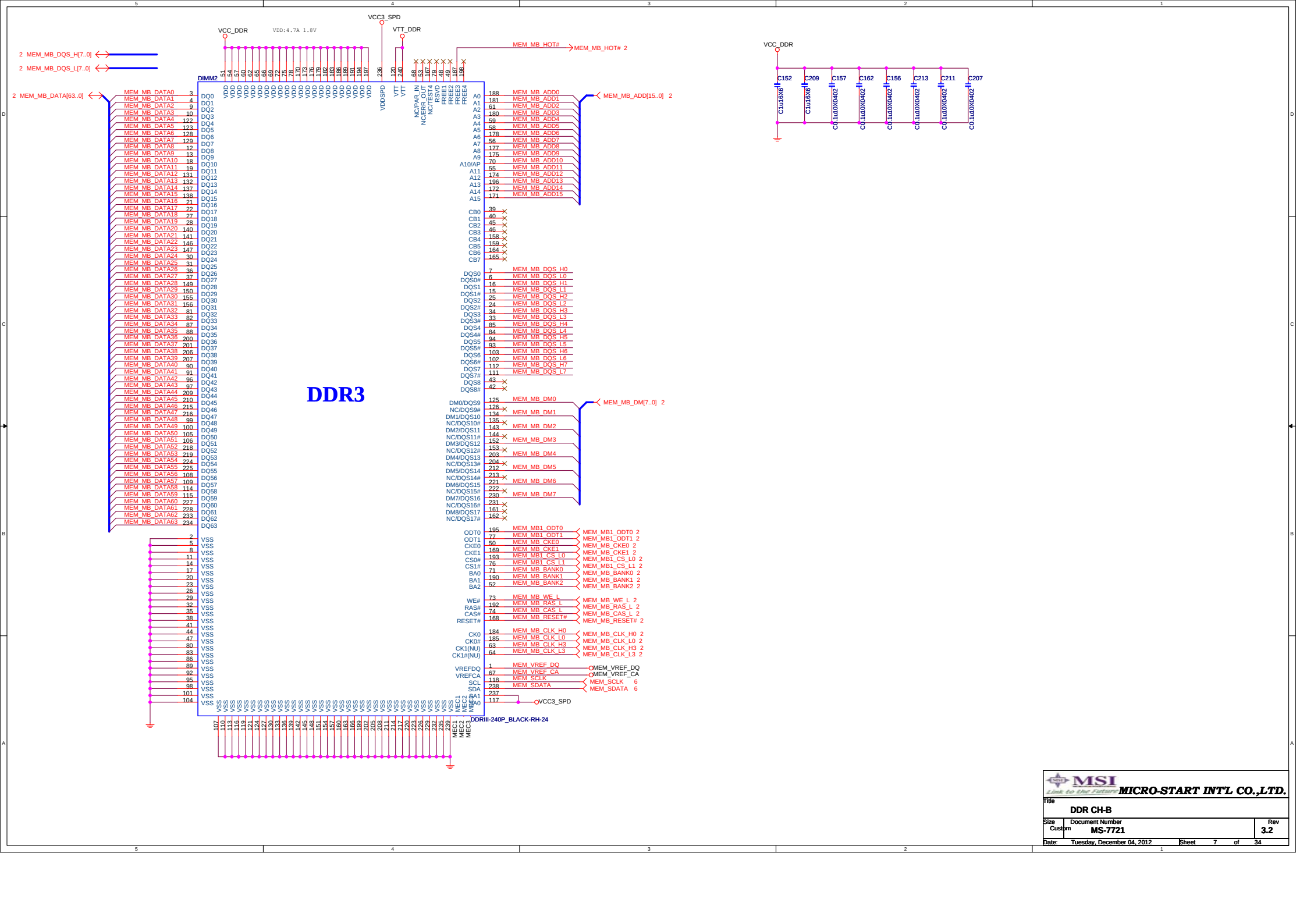
MICRO-START INT'L CO.,LTD.

Title: FM2 POWER&DECOUPLING

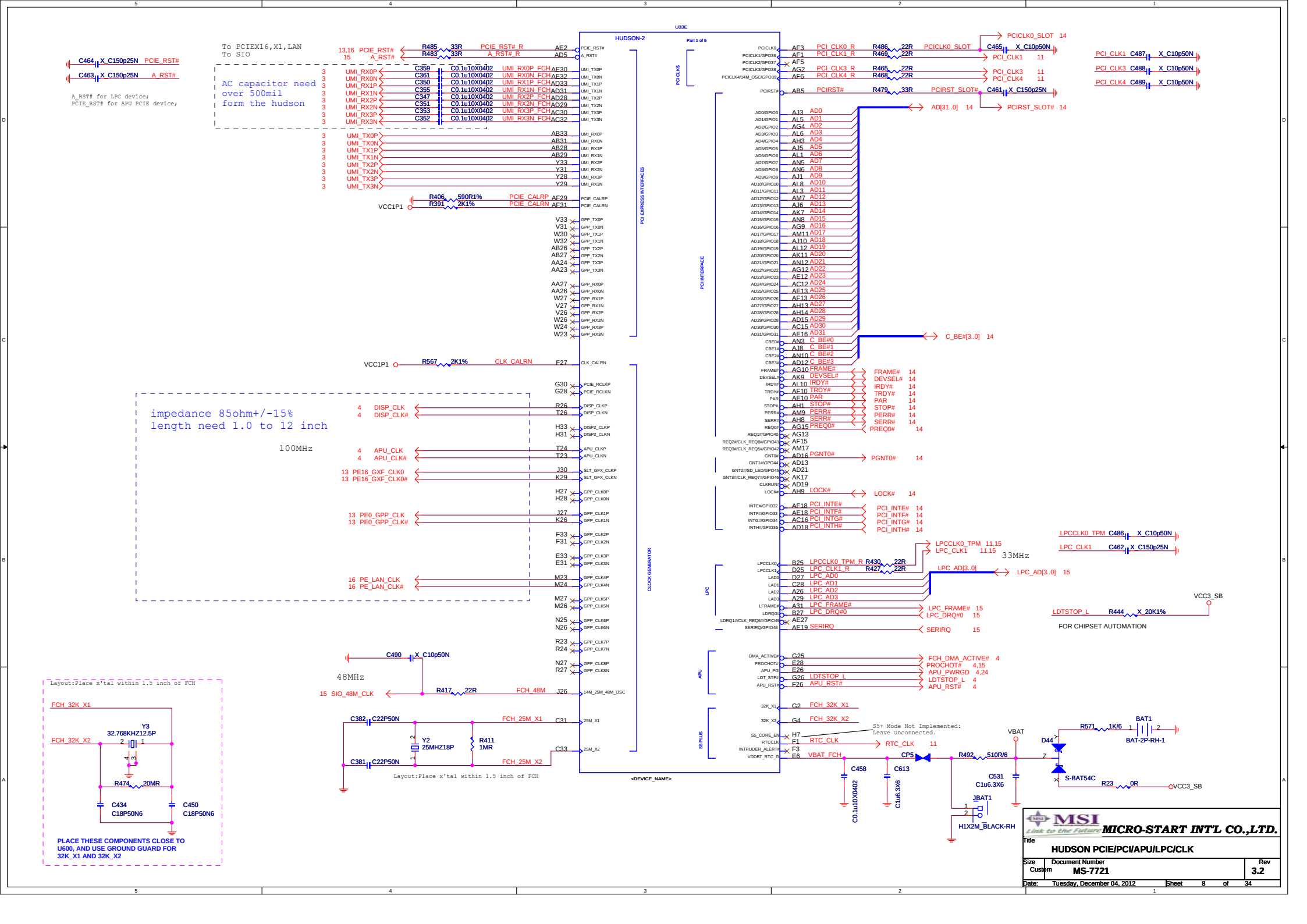
Size	Document Number	Rev
Custom	MS-7721	3.2

Date: Tuesday, December 04, 2012 Sheet 5 of 34

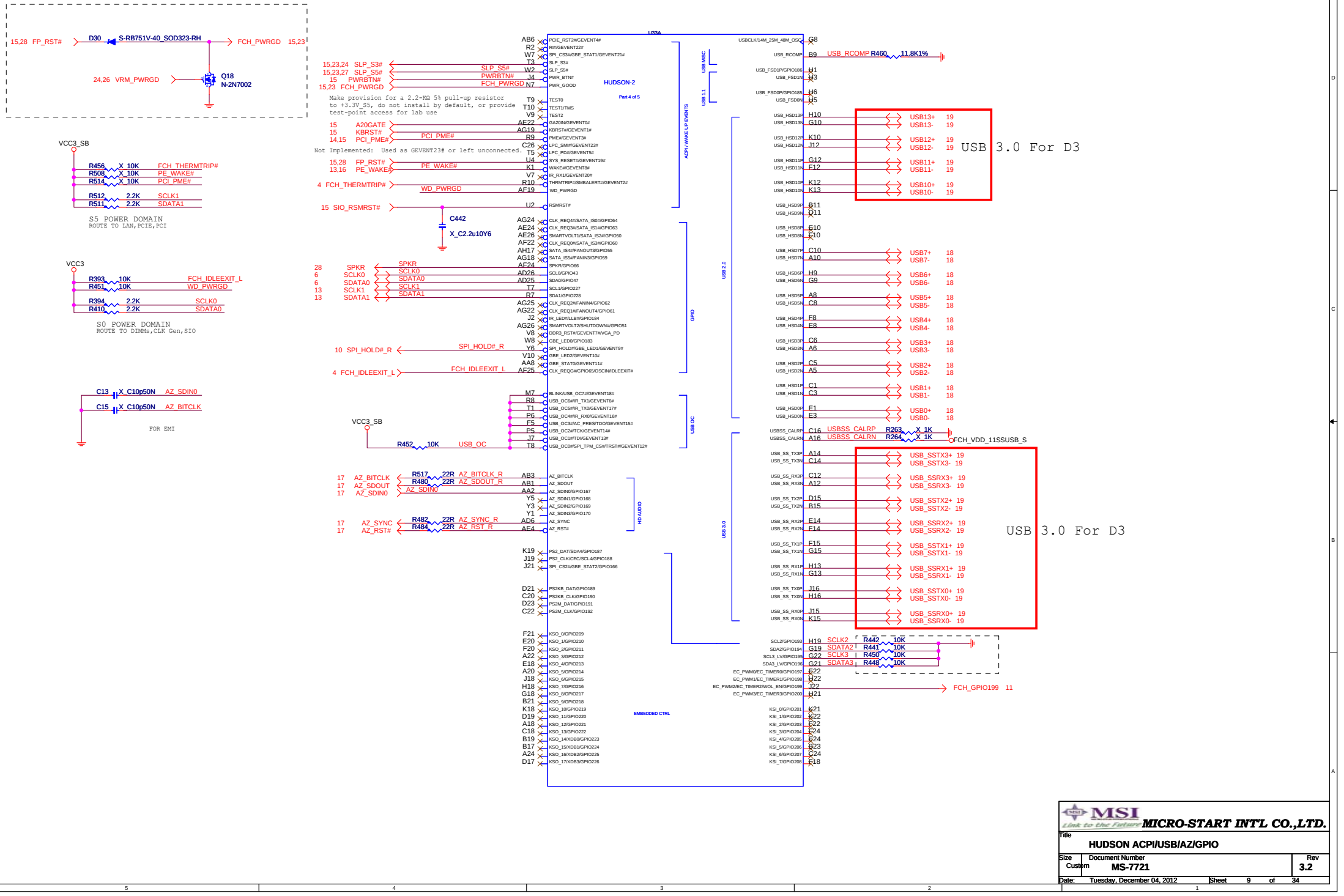

DDR3
DIMM1
DDRIII-240P_BLACK-RH-24
F5
F-MICROSMD110
VCC3
VCC3_SPD
VCC_DDR
VTT_DDR
C194
C0.1u10X0402
MEM_MA_HOT#
MEM_MA_HOT# 2
2 MEM_MA_DATA[63..0]
MEM_MA_ADD[15..0] 2
MEM_MA_DM[7..0] 2
MEM_MA_DQS_H[7..0]
MEM_MA_DQS_L[7..0]
MEM_SCLK
MEM_SDATA
R356 0R
R351 0R
SCLK0
SDATA0
MEM_VREF_DQ
MEM_VREF_CA
MEM_SCLK
MEM_SDATA
VCC3_SPD
C12
C41
C10u6.3X8
C10u6.3X8
C292
C303
C296
C260
C304
C1u16X6
C1u16X6
C0.1u10X0402
C0.1u10X0402
C0.1u10X0402
R302
1K
C193
C0.1u10X0402
R305
1K
C192
C0.1u10X0402
C196
X_C1000P16X
MEM_VREF_CA
R130
1K
C47
C0.1u10X0402
R131
1K
C52
C0.1u10X0402
C48
X_C1000P16X
MEM_VREF_DQ
follow circuit checklist suggest value
SA1 SA0
DDR-III DIMM Config.
DEVICE ADDRESS CLOCK
DIMM 1 10 P/N_DDR1_A
DIMM 2 11 P/N_DDR1_B
DIMM 3 N/A
DIMM 4 N/A
MICRO-START INT'L CO.,LTD.
Title
DDR CH-A
Size Custom
Document Number MS-7721
Rev 3.2
Date: Tuesday, December 04, 2012
Sheet 6 of 34

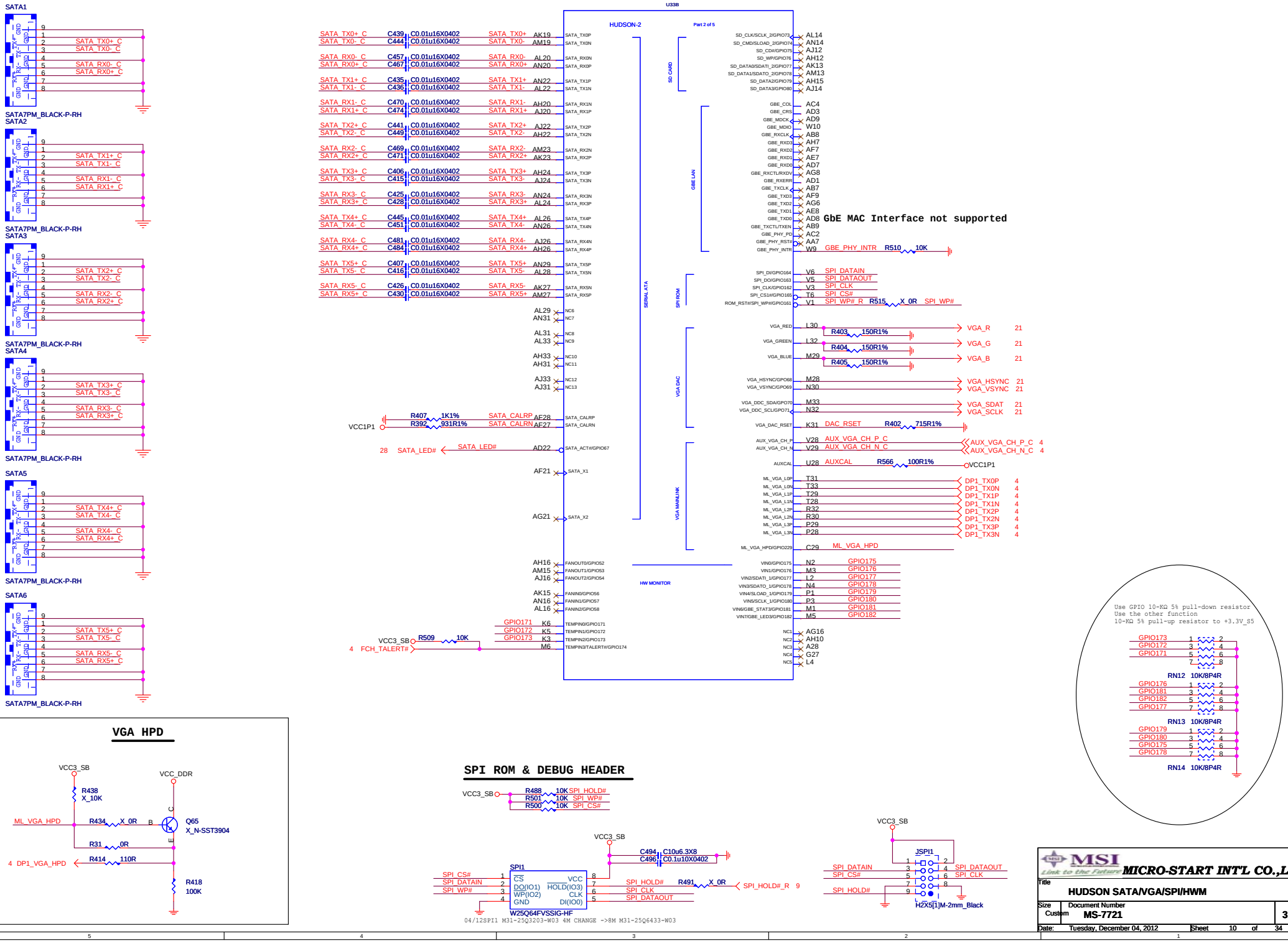


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title: DDR CH-B			
Size: Custom	Document Number: MS-7721		Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 7 of 34		

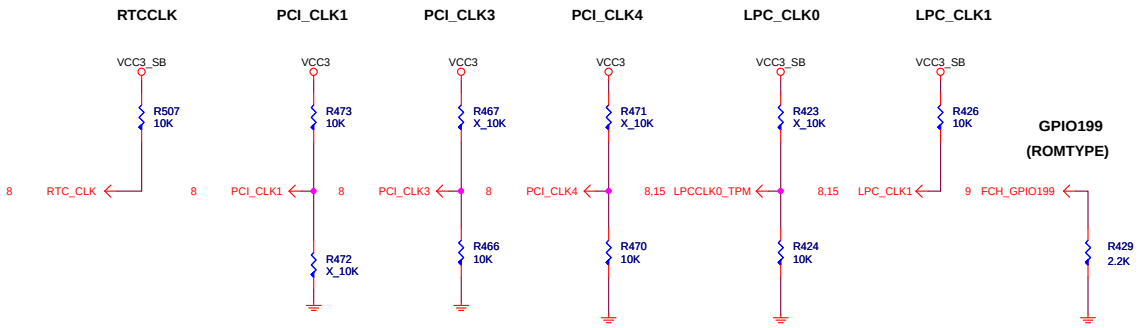

U33E
HUDSON-2
Part 1 of 5
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
SS PLUS
PCI CLKS
<DEVICE_NAME>
To PCIEX16,X1,LAN
To SIO
AC capacitor need over 500mil form the hudson
A_RST# for LPC device;
PCIE_RST# for APU PCIE device;
impedance 85ohm+/-15%
length need 1.0 to 12 inch
100MHz
33MHz
48MHz
FOR CHIPSET AUTOMATION
S5+ Mode Not Implemented: Leave unconnected.
Layout:Place x'tal within 1.5 inch of FCH
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
MICRO-START INT'L CO.,LTD.
HUDSON PCIE/PCI/APU/LPC/CLK
Custom
MS-7721
3.2
Tuesday, December 04, 2012
Sheet 8 of 34

HUDSON ACPI/USB/AZ/GPIO



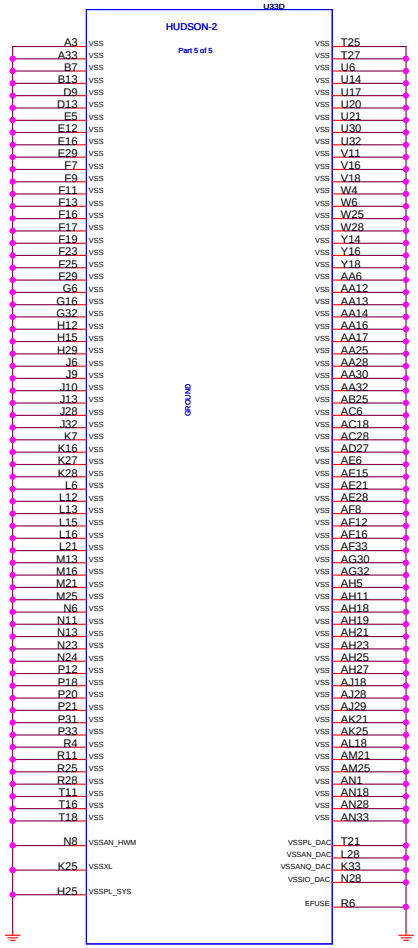

SATA1
SATA7PM_BLACK-P-RH
SATA2
SATA7PM_BLACK-P-RH
SATA3
SATA7PM_BLACK-P-RH
SATA4
SATA7PM_BLACK-P-RH
SATA5
SATA7PM_BLACK-P-RH
SATA6
SATA7PM_BLACK-P-RH
U33B
HUDSON-2
Part 2 of 5
SERIAL ATA
SD CARD
GBE LAN
SPI ROM
VGA DAC
VGA HANDLINK
HW MONITOR
GbE MAC Interface not supported
GBE_PHY_INTR
SPI_DATAIN
SPI_DATAOUT
SPI_CLK
SPI_CS#
SPI_WP#
VGA_R
VGA_G
VGA_B
VGA_HSYNC
VGA_VSYNC
VGA_SDAT
VGA_SCLK
DAC_RSET
AUX_VGA_CH_P_C
AUX_VGA_CH_N_C
AUXCAL
ML_VGA_HPD
SATA_LED#
SATA_CALRP
SATA_CALRN
FCH_TALERT#
Use GPIO 10-KΩ 5% pull-down resistor
Use the other function
10-KΩ 5% pull-up resistor to +3.3V_S5
RN12 10K/8P4R
RN13 10K/8P4R
RN14 10K/8P4R
VGA HPD
SPI ROM & DEBUG HEADER
W25Q64FVSSIG-HF
04/12SPI1 M31-25Q3203-W03 4M CHANGE ->8M M31-25Q6433-W03
H2X5[1]M-2mm_Black
MICRO-START INT'L CO.,LTD.
HUDSON SATA/VGA/SPI/HWM
MS-7721
3.2
Tuesday, December 04, 2012
Sheet 10 of 34

FCH REQUIRED STRAPS



	S5+ Mode RTCCLK	PCIeR GEN PCI_CLK1	Debug Strap PCI_CLK3	CLK GEN PCI_CLK4	IMC Enable LPC_CLK0	CLKGEN Enable LPC_CLK1	GPIO199 (ROMTYPE)
PULL HIGH	S5 Plus MODE DISABLED DEFAULT	PCIe interface at Gen2 DEFAULT	Enable Debug Straps	Reserved	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 Plus MODE ENABLED	FORCE PCIe at Gen1	Disable Debug Straps DEFAULT	APU_CLK/DISP_CLK Required setting DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT

this pin is not used in external clock mode
(needed only for integrated clock)



Layout:
VSSXL,VSSPL_SYS,VSSAN_HWM,VSSIO_DAC,
VSSAN_DAC, VSSANQ_DAC,VSSPL_DAC
are connected to VSS through dedicated vias.

FCH DEBUG STRAPS

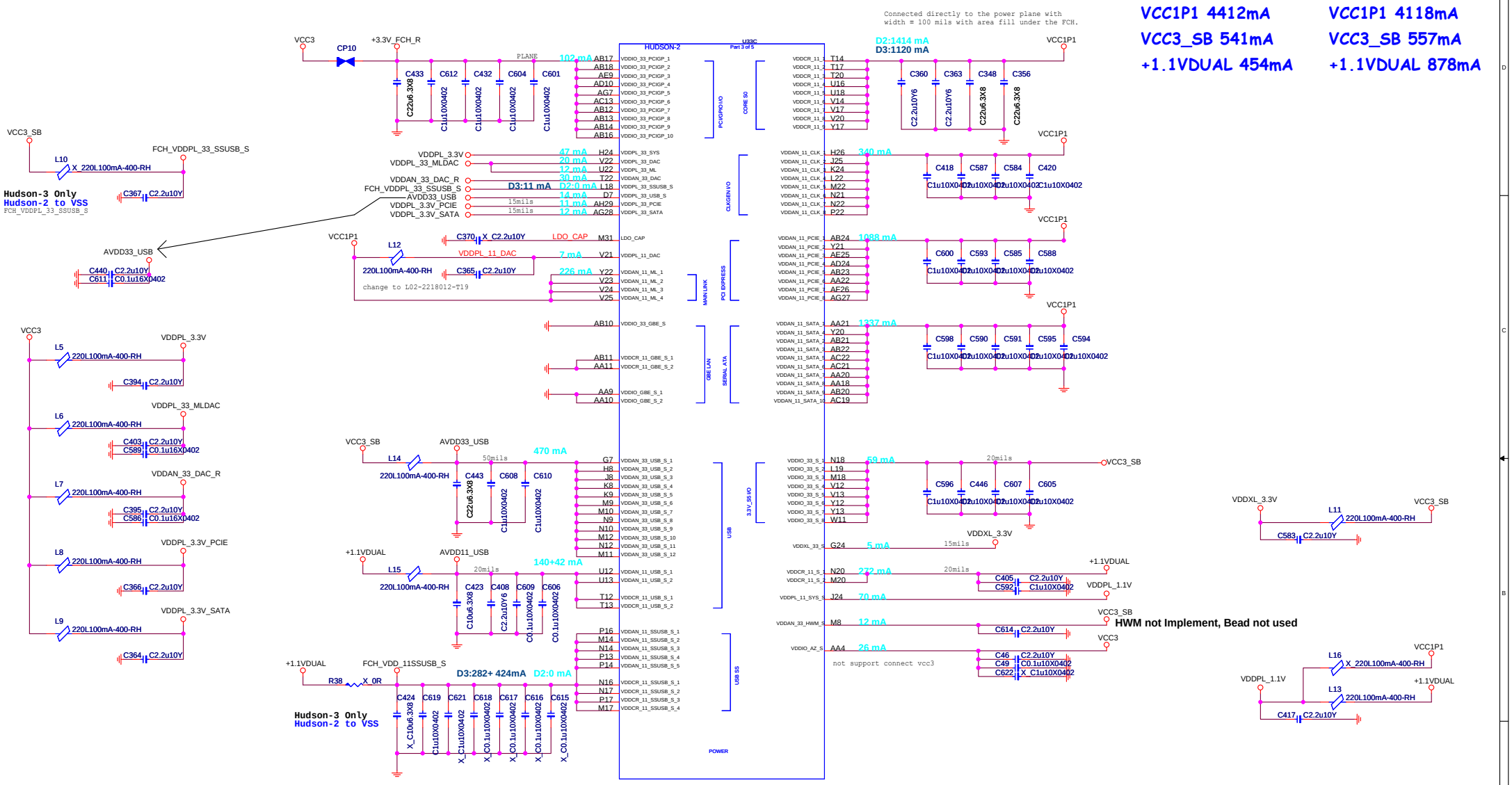
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT		normal REFCLK termination DEFAULT	Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock		inverted REFCLK termination	Enable loading settings for UMI/PLL/misc from I2C ROM	Boot from PCI bus

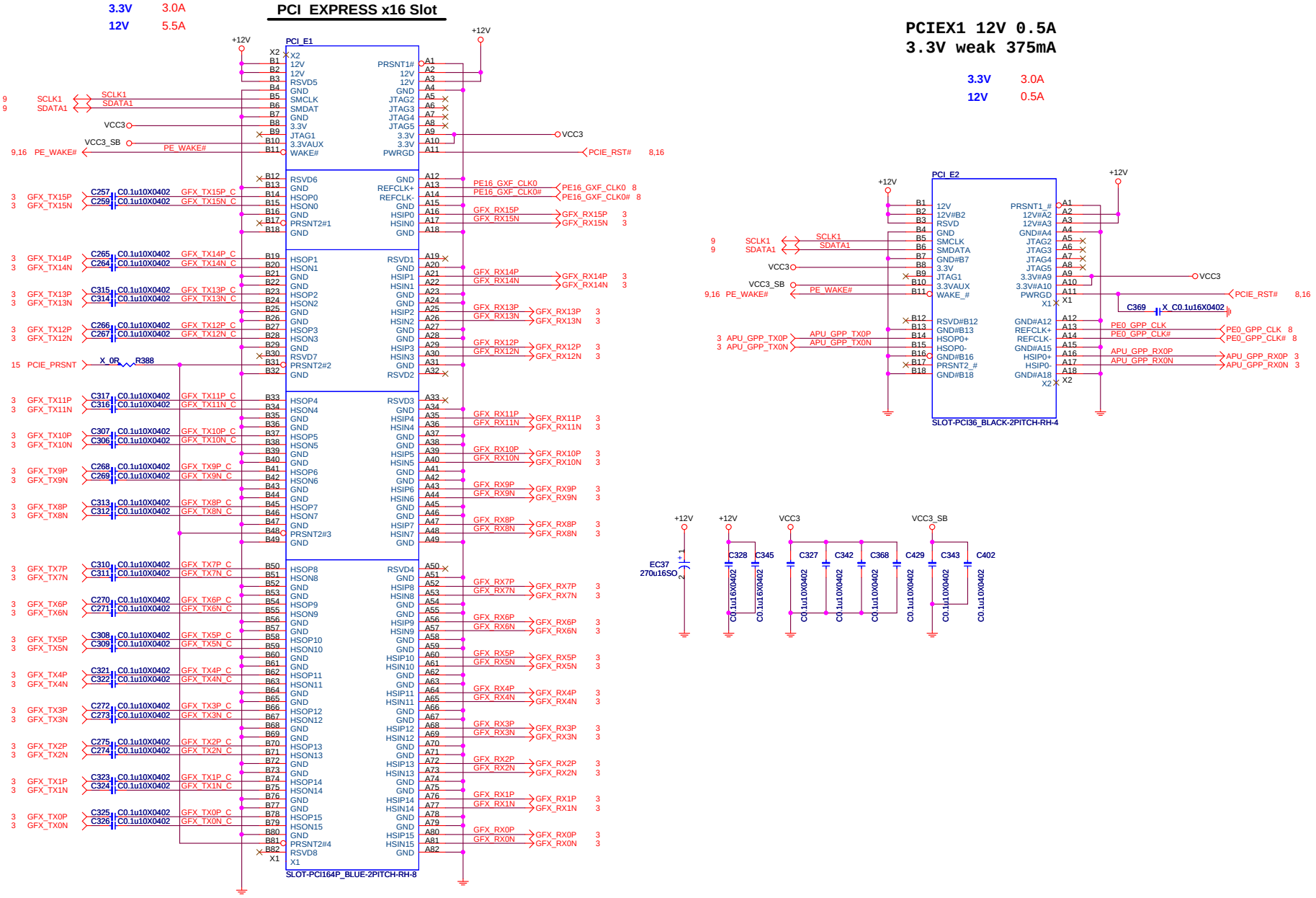
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: HUDSON STRAPS

Size: Custom | Document Number: MS-7721 | Rev: 3.2

Date: Tuesday, December 04, 2012 | Sheet 11 of 34


D2
VCC3 265mA
VCC1P1 4412mA
VCC3_SB 541mA
+1.1VDUAL 454mA
D3
VCC3 260mA
VCC1P1 4118mA
VCC3_SB 557mA
+1.1VDUAL 878mA
Connected directly to the power plane with width = 100 mils with area fill under the FCH.
HUDSON-2
U33C
Part 3 of 5
D2:1414 mA
D3:1120 mA
D3:11 mA
D2:0 mA
D3:282+ 424mA
D2:0 mA
HWM not Implement, Bead not used
Hudson-3 Only
Hudson-2 to VSS
FCH_VDDPL_33_SSUSB_S
change to L02-2218012-T19
not support connect vcc3
POWER
MICRO-START INT'L CO.,LTD.
HUDSON POWER&DECOUPLING
MS-7721
3.2
Tuesday, December 04, 2012
Sheet 12 of 34



MSI MICRO-START INT'L CO.,LTD.

Title: PCI EXPRESS X16

Size	Document Number	Rev
Custom	MS-7721	3.2

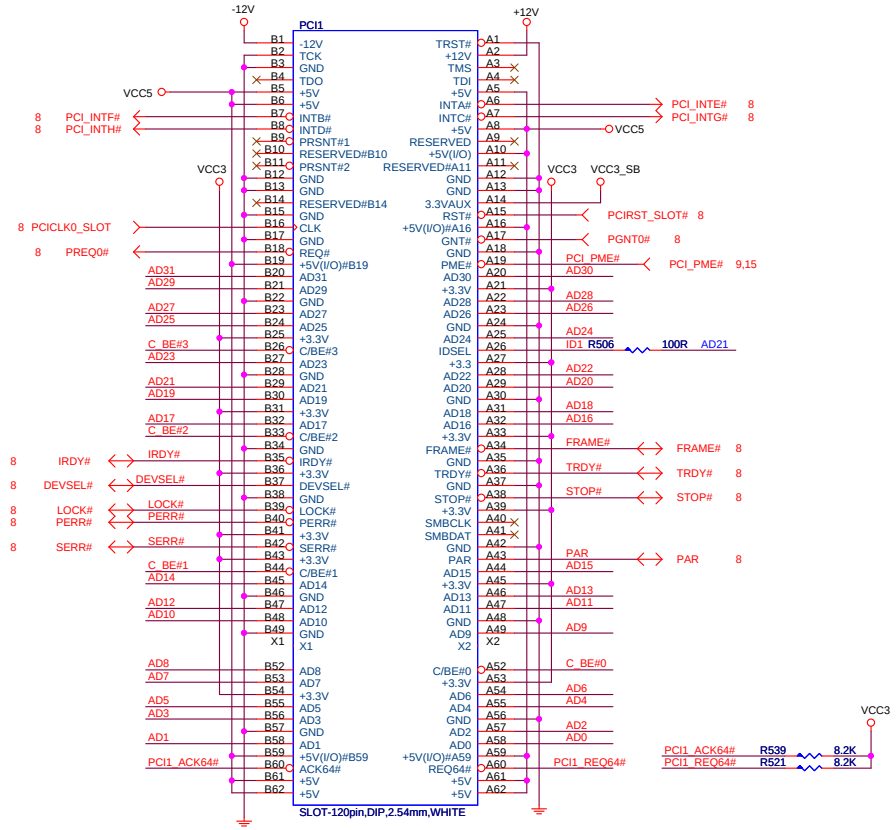
Date: Tuesday, December 04, 2012 Sheet 13 of 34

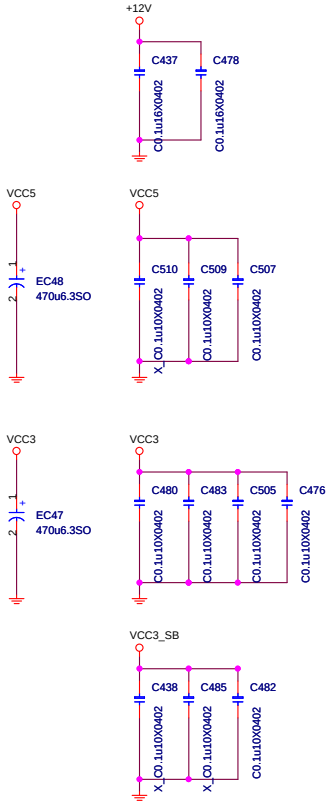
3.3V	7.6A
5V	5.0A
12V	0.5A

AD[31..0] 8

C_BE#[3..0] 8

PCI SLOT 1 (PCI VER: 2.2 COMPLY)





IDSEL = AD21

MASTER = PCI_REQ#0
PCI_GNT#0

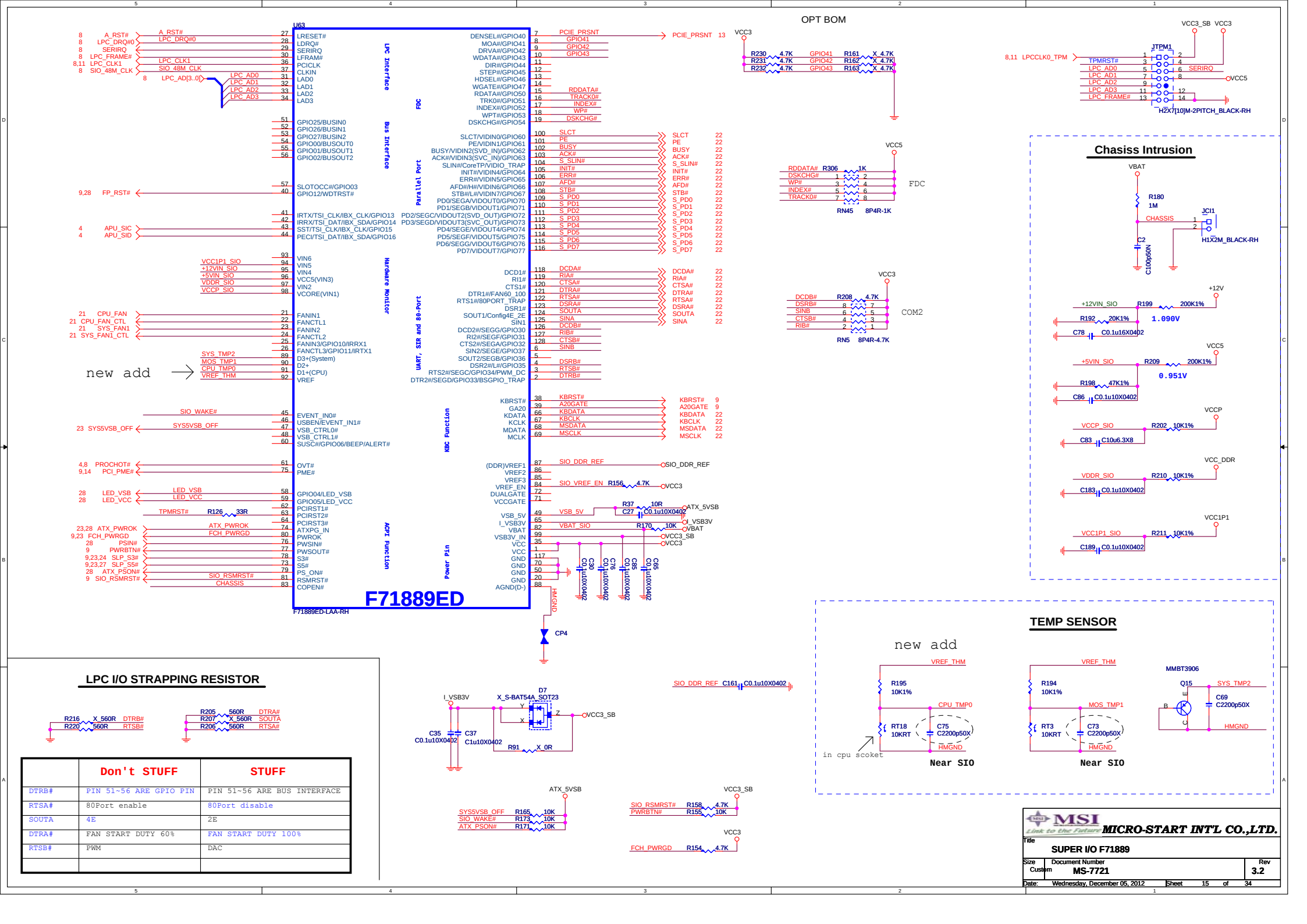
PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PREQ#0 PGNT#0	AD21	CLK_33M_PCH_PCI (ICS113)

MICRO-START INT'L CO.,LTD.

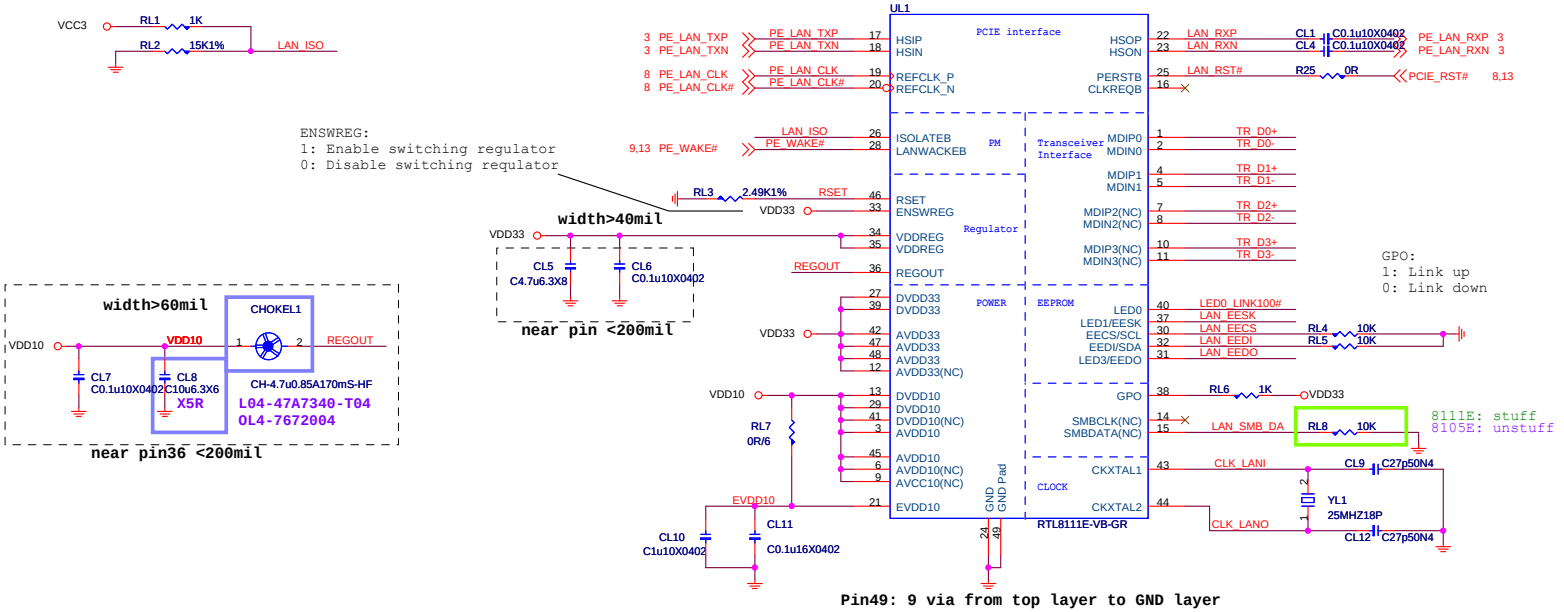
Title: PCI/PCIE X1 SLOTs		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 14 of 34	



LPC I/O STRAPPING RESISTOR

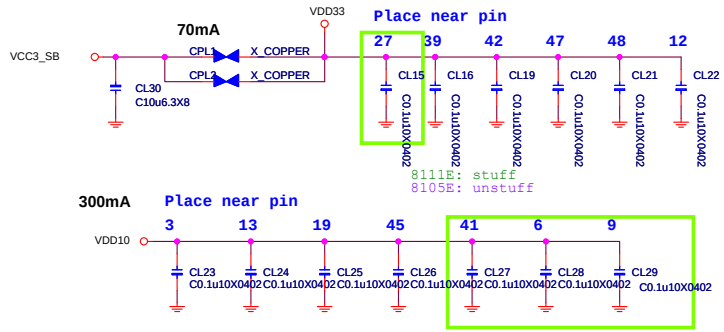
	Don't STUFF	STUFF
DTRB#	PIN 51~56 ARE GPIO PIN	PIN 51~56 ARE BUS INTERFACE
RTSA#	80Port enable	80Port disable
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
RTSB#	PWM	DAC

RTL8111E/8105E

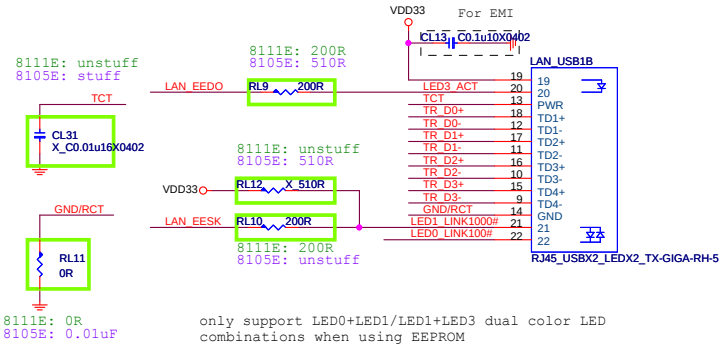


Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

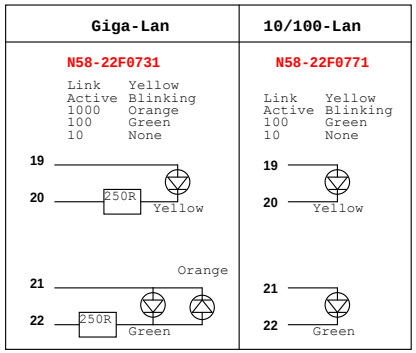
3.3v Power on rise time : 1~100ms.



LAN Connector



only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

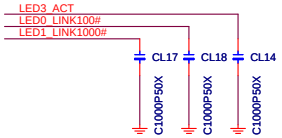


8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



MICRO-START INTL CO.,LTD.

Title: LAN-RTL8111E/8105E.		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 16 of 34	

ALC887-VD
VT1708S CE

11mA
Closed Codec

VCC3

CA1 C10u6.3X6
CA2 C0.1u10X0402

Closed Codec
CA3 closed PIN25
CA4 closed PIN38

VOUT
CA3
CA4 C22u6.3X8

用SMD CAP 手動量測會FAIL在THD+N
用EL-CAP or SOLID cap,才會pass

UA1

9 AZ_SDOUT
9 AZ_SDIN0
9 AZ_SYNC
9 AZ_RST#
9 AZ_BITCLK

RA6 22R SDIN0

47 EPAD/SPDIF-IN
48 SPDIF-OUT
5 SDATA-OUT
8 SDATA-IN
10 SYNC
11 RESET#
6 BCLK
DVDD DVDD-IO
LDO-OUT1 LDO-OUT2

FRONT-R 36 A_LOUT_R ECA2 100u16SO LOUT_R
FRONT-L 35 A_LOUT_L ECA1 100u16SO LOUT_L
SURR-R 41
SURR-L 39
CENTER 43
LFE 44
SIDE-R 46
SIDE-L 45

need use X5R

2 GPIO0/DMIC-CLK/SPDIF-OUT2
3 REGREF
CA9 C10u6.3X6
SENSE_A 13 Sense A
SENSE_B 34 Sense B

LINE1-R 24 A_LINE_IN_R CA7 C4.7u6.3X8 LINE_IN_R
LINE1-L 23 A_LINE_IN_L CA8 C4.7u6.3X8 LINE_IN_L
LINE2-R 15 A_LINE2_R ECA3 100u16SO LINE2_R
LINE2-L 14 A_LINE2_L ECA4 100u16SO LINE2_L

MIC1_V_R 32 MIC1-VREFO-R
MIC2_VREFO 30 MIC2-VREFO
MIC1_V_L 28 MIC1-VREFO-L
37 PIN37-VREFO
29 LDO-IN
LINE2_VREFO 31 LINE2-VREFO
27 VREF
VCAP 33 Sense C
JDREF 40 JDREF

MIC1-R 22 A_MIC1_R CA10 C4.7u6.3X8 MIC1_R
MIC1-L 21 A_MIC1_L CA11 C4.7u6.3X8 MIC1_L
MIC2-R 17 A_MIC2_R CA14 C4.7u6.3X8 MIC2_R
MIC2-L 16 A_MIC2_L CA15 C4.7u6.3X8 MIC2_L

CD-R 20
CD-GND 19
CD-L 18

12 BEEP
GPIO1/DMIC-DATA
DVSS
AVSS1 AVSS2

ALC887-VD2-CG-HF

need use X5R

45.8mA
LDOVDD
VREF_AUDIO
CA16 X_C0.1u16X0402
CA18 C10u6.3X6
CA17 X_C100p50N
RA13 20K1%
Reserve for 1708
Closed Codec

C647.C649 close to Pin27

EL 100u (C94-1012511-N07)

4.7k change to 2.2k,Microphone recording the effect better

LIN_OUT
AUDIO1B
LOUT_R RA1 75R LOUT_RA
LOUT_L RA2 75R LOUT_LA
FRONT_JD
JACK-AUDIOX3F_PK/GR/BU-RH-6

100pF Cap can change to
TVS by PM request.

LOUT_LA CA5 ESD-SFI0402
LOUT_RA CA6 ESD-SFI0402
LOUT_LA RA3 22K
LOUT_RA RA4 22K

LIN_IN
AUDIO1A
LINE_IN_R RA5 75R LINE_IN_RA
LINE_IN_L RA7 75R LINE_IN_LA
LINE1_JD
JACK-AUDIOX3F_PK/GR/BU-RH-6

LINE_IN_LA CA32 C100p50N
LINE_IN_RA CA33 C100p50N

MIC1
AUDIO1C
MIC1_V_L RA9 2.2K MIC1_LA
MIC1_V_R RA10 2.2K MIC1_RA
MIC1_R RA11 75R MIC1_RA
MIC1_L RA12 75R MIC1_LA
MIC1_JD
JACK-AUDIOX3F_PK/GR/BU-RH-6

MIC1_RA CA12 C100p50N
MIC1_LA CA13 C100p50N

VCAP
CA19 X_C0.1u16X0402
CA20 X_C10u6.3X6

887:Remove
1708:Stuff
Closed Codec

EMI
CA21 X_C0.1u16X0402
CA22 X_C1000P16X

CPA1 X_COPPER
CPA2 X_COPPER

D LIN_IN
E LIN_OUT
F MIC1
N54-13F0271-K06

When connected in series capacitor polarity,
the required resistance to ground

F_LINE2_L RA14 22K
F_LINE2_R RA15 22K

RNA2
8P4R-75R
MIC2_R F_MIC2_R
MIC2_L F_MIC2_L
LINE2_L F_LINE2_L
LINE2_R F_LINE2_R

DA1
LINE2_VREFO
S-BAT54A_SOT23
MIC2_VREFO
S-BAT54A_SOT23
DA2

RNA1
8P4R-4.7K

F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
Close to Jack

N31-2051411-H06
JAUD1
MIC GND
MICPWR PRESENCE#
FLINE OUTR LINE NEXT R
HPON
FLINE OUTL LINE NEXT L
H2X5[8]M_BLACK-RH

MIC2_JD
LINE2_JD

RA19 47R
CA30 C1000P16X

CA27 ESD-SFI0402
CA28 ESD-SFI0402
CA29 ESD-SFI0402
CA31 ESD-SFI0402

RA20 39.2K1%
RA21 20K1%

Varister --> cap for cost down
Close to Front panel
For HDA/AC97 front cable.

SENSE_A
RA16 5.1K1% FRONT_JD
RA17 10K1% LINE1_JD
RA18 20K1% MIC1_JD
CA23 X_C100p50N
Closed Codec
SENSE_B
CA26 X_C100p50N

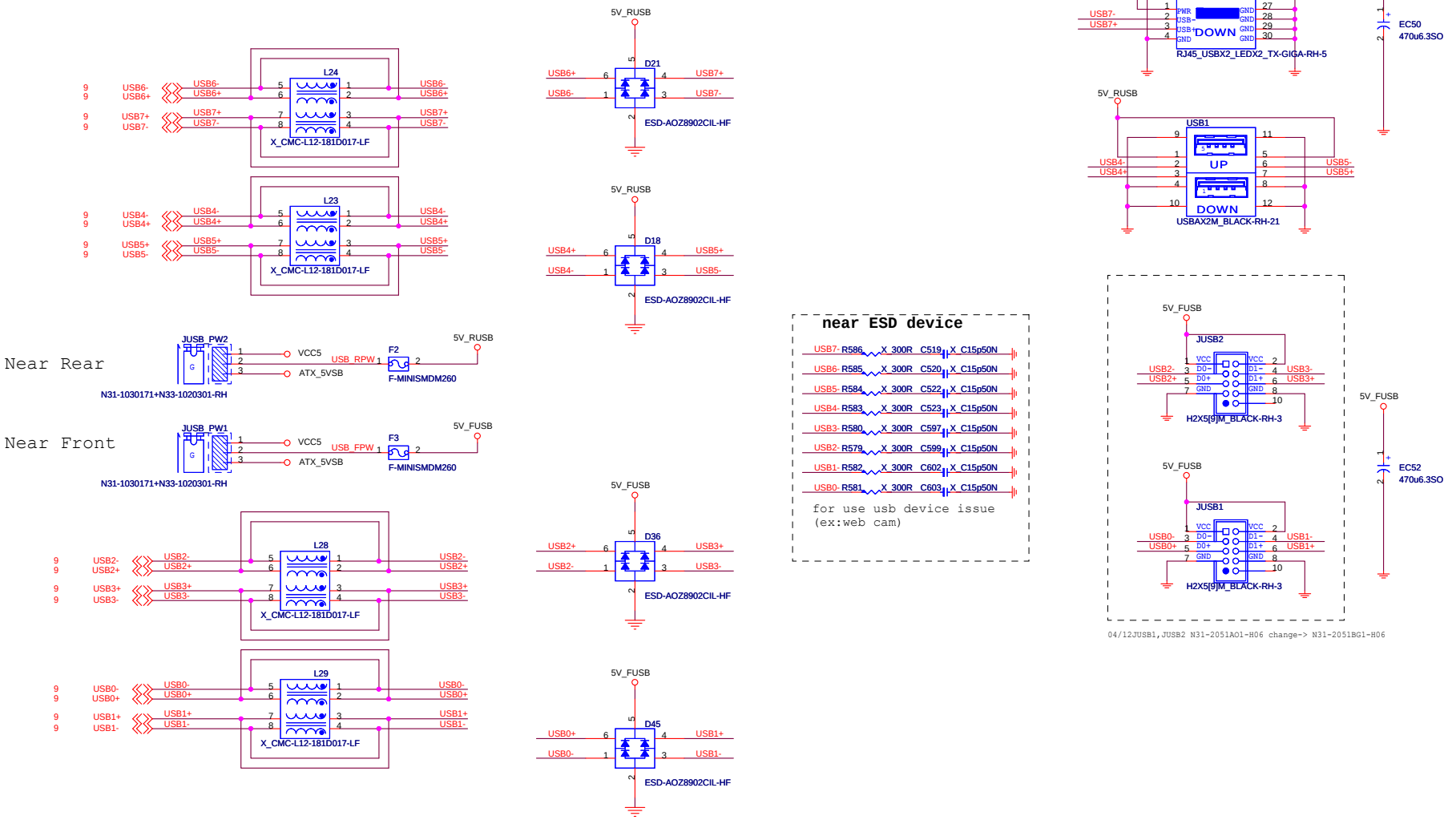
ATX_5VSB
LA1 0R/8
LDOVDD
DA3 X_TVS
CA24 C0.1u10X0402
CA25 C10u6.3X6

C659,C669 close to L35

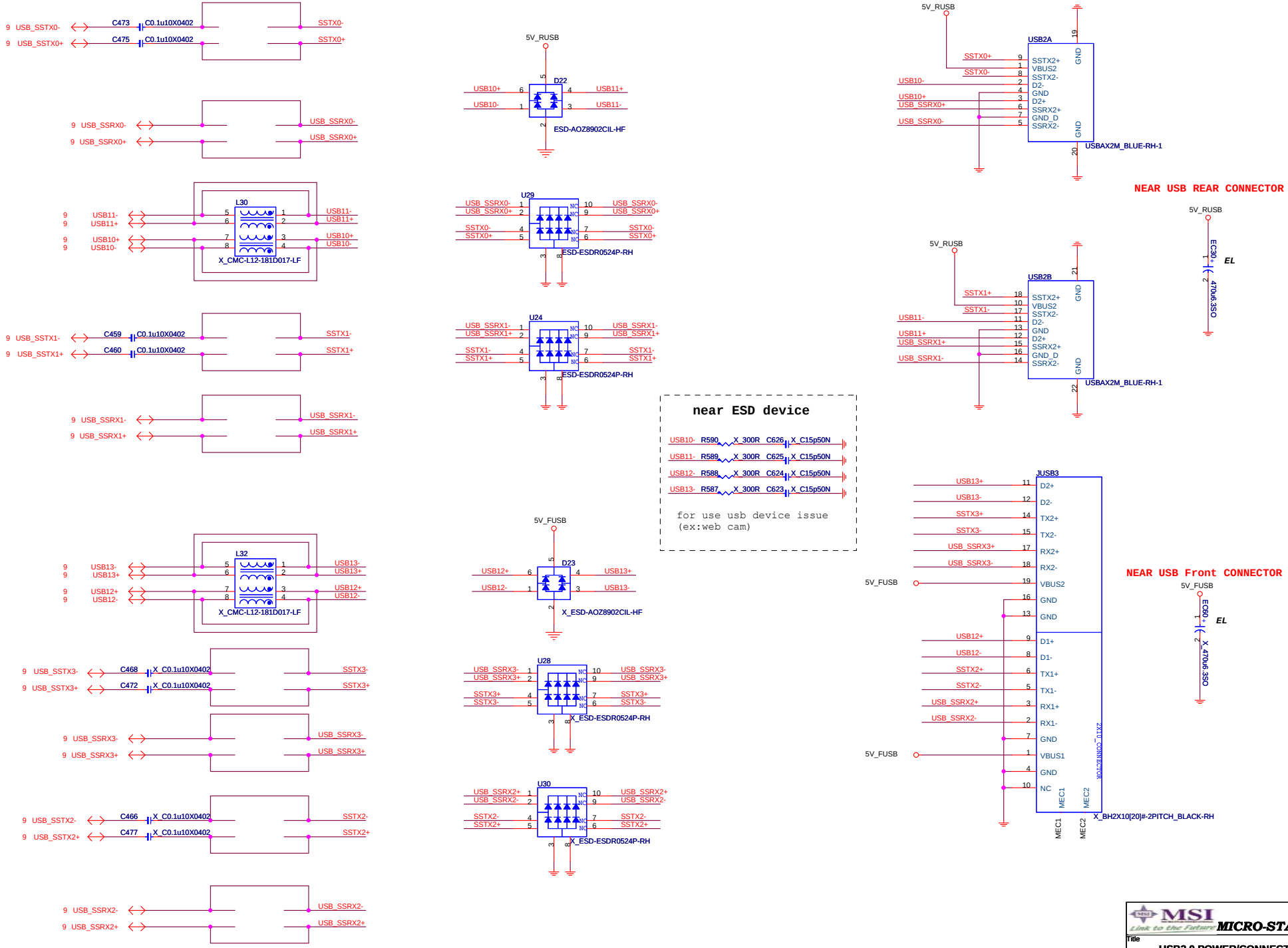
0402 300pF varistor
DOG-2950500-SI0
DOG-3010510-I05

MICRO-START INT'L CO.,LTD.

Title	HUDSON SATA/VGA/SPI/HWM	
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 17 of 34	



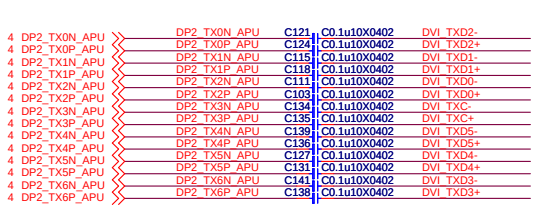
MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title	USB2.0 POWER/CONNECTORS	
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 18 of 34	

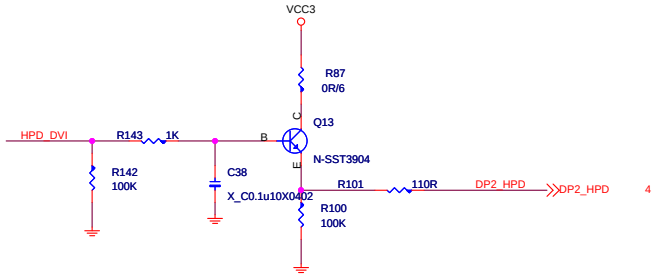


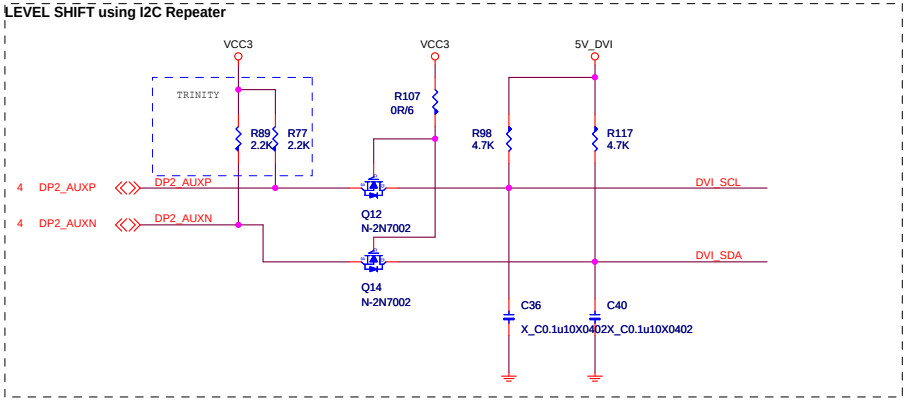
MICRO-START INT'L CO.,LTD.

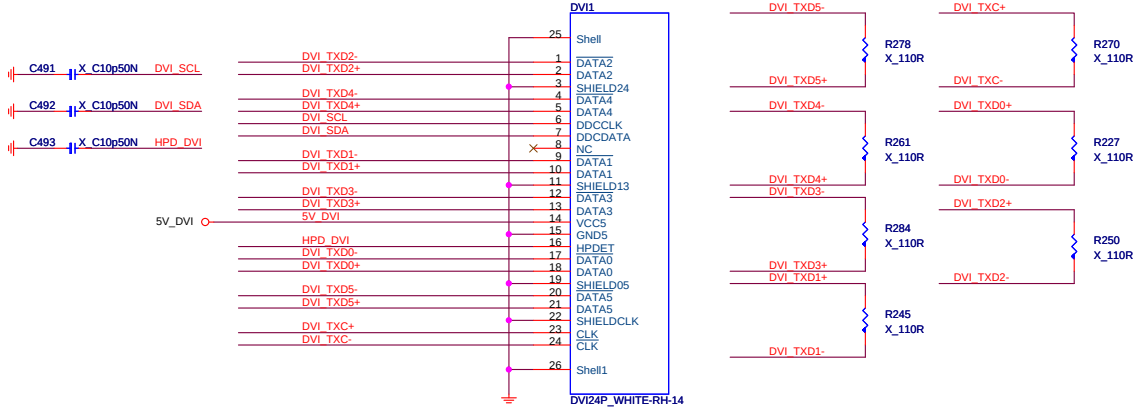
Title	USB3.0 POWER/CONNECTORS	
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 19 of 34	

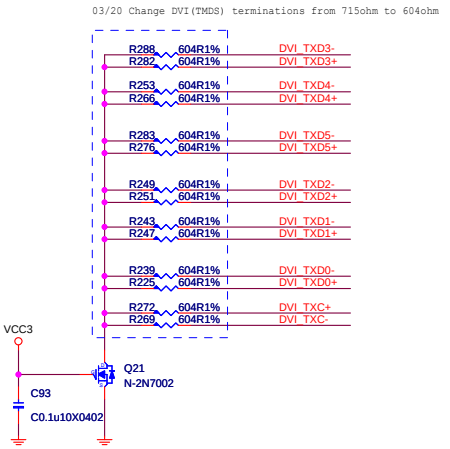
DVI CONNECTOR

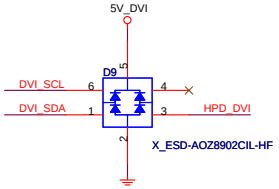


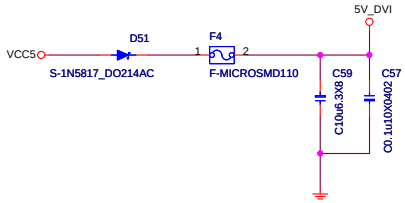








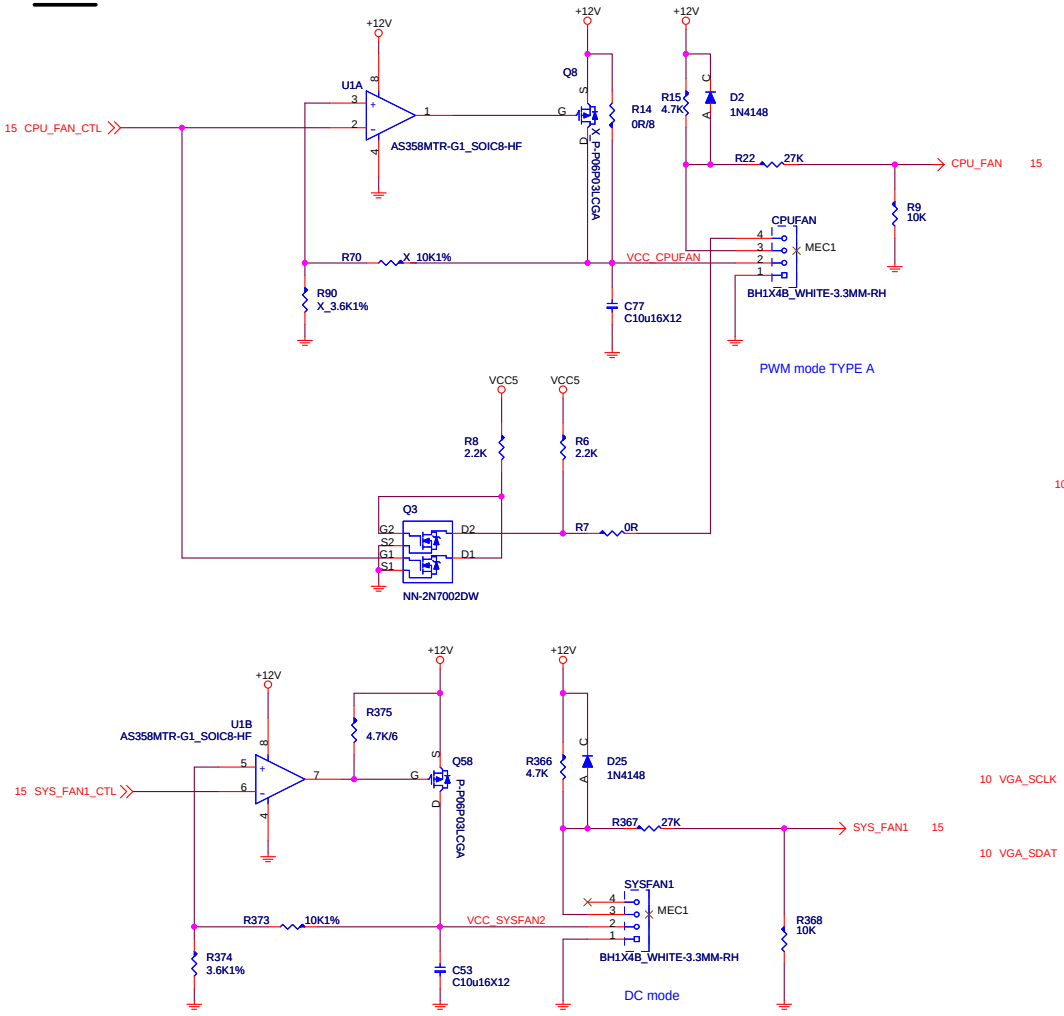


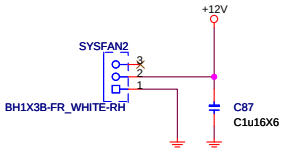


MSI Link to the Future MICRO-START INT'L CO.,LTD.

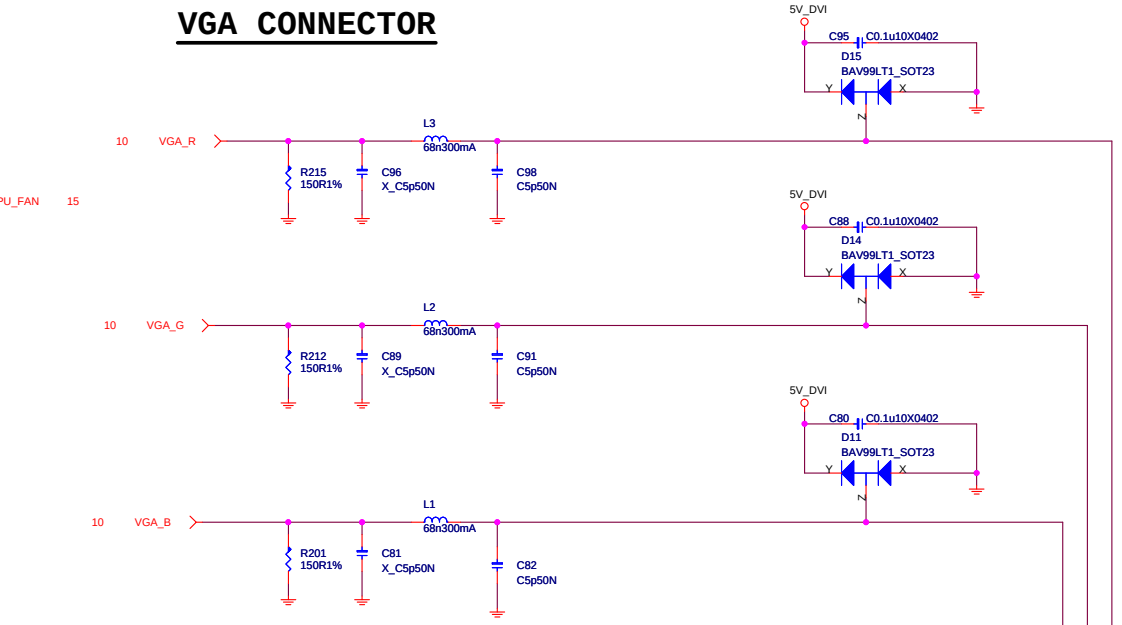
Title: DVI/HDMI SWITCH		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 20 of 34	

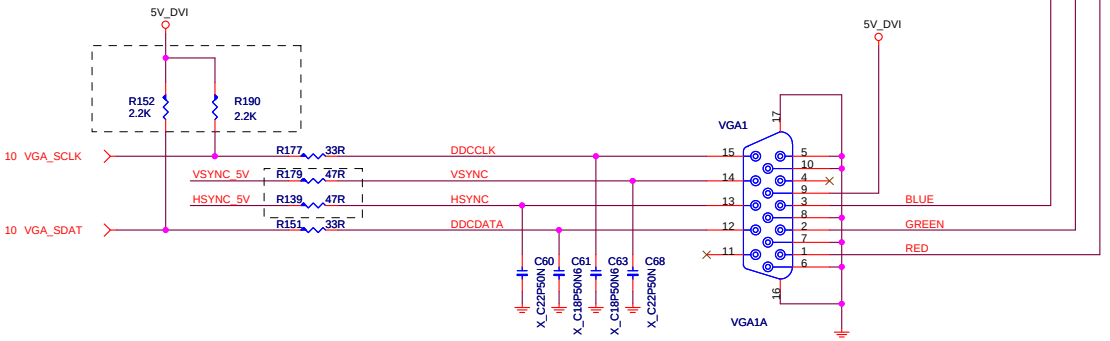
FAN

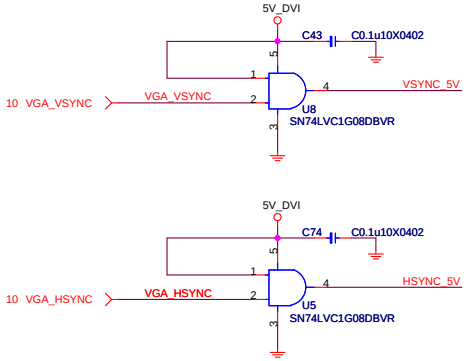


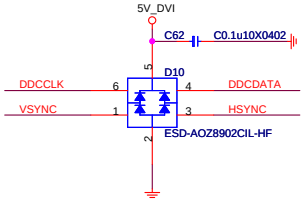


VGA CONNECTOR





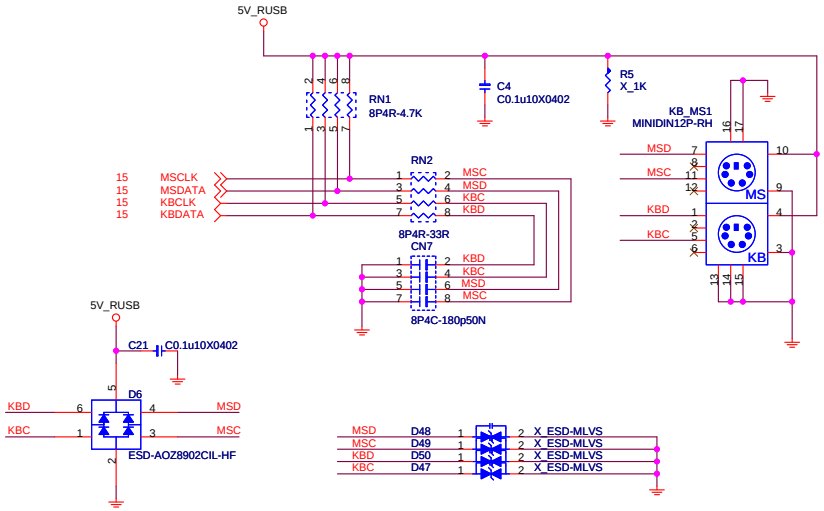




MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: DVI & VGA CONN.		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 21 of 34	

PS2 Connect

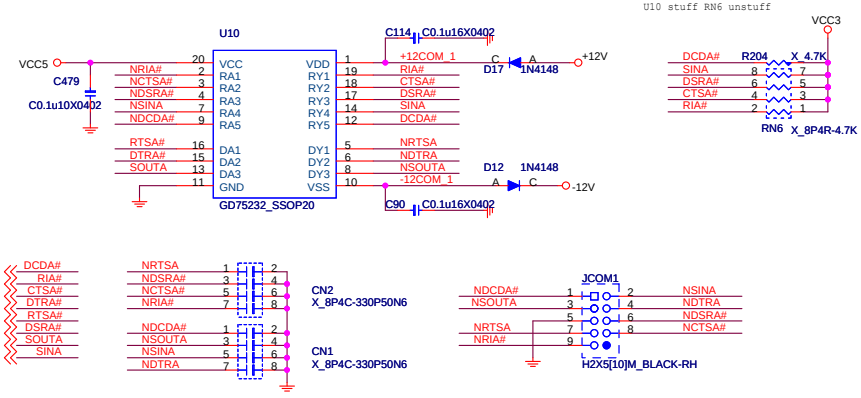


TVS P/N:
D0G-0200529-A68
D0G-0422013-N47
D0G-15A0509-N47
D0G-0422003-P03
D0G-0422003-N47

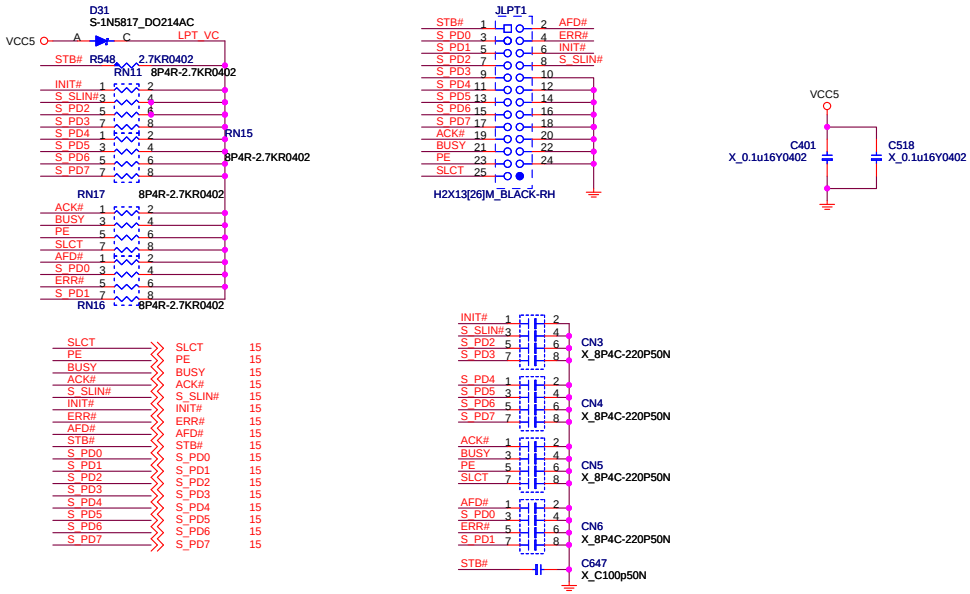
Varistor:
D0G-3010510-I05
D0G-2950500-SI0

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

SERIAL PORT 1



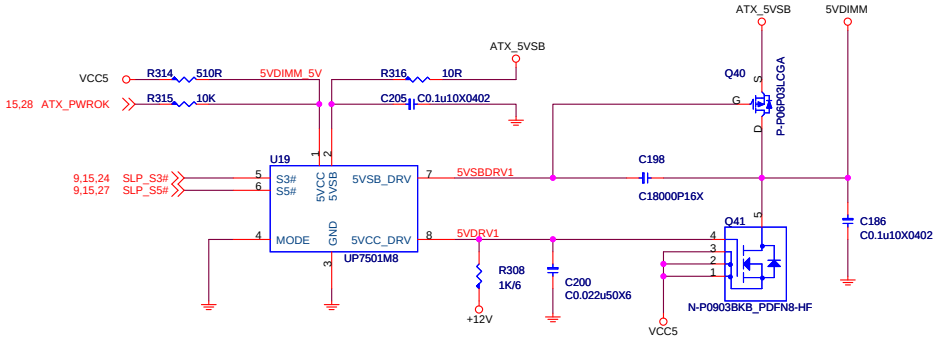
PARALLAL PORT



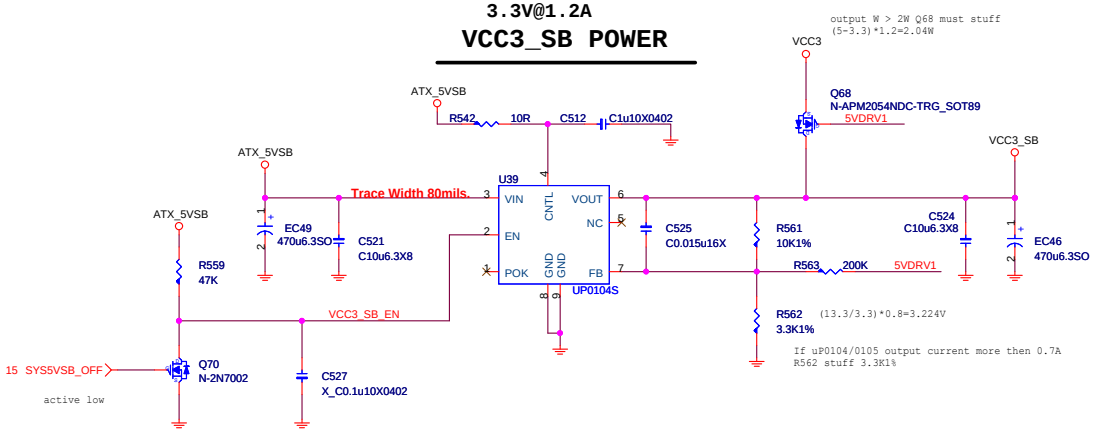
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	COM/LPT	
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 22 of 34	

5VDIMM FOR DDR



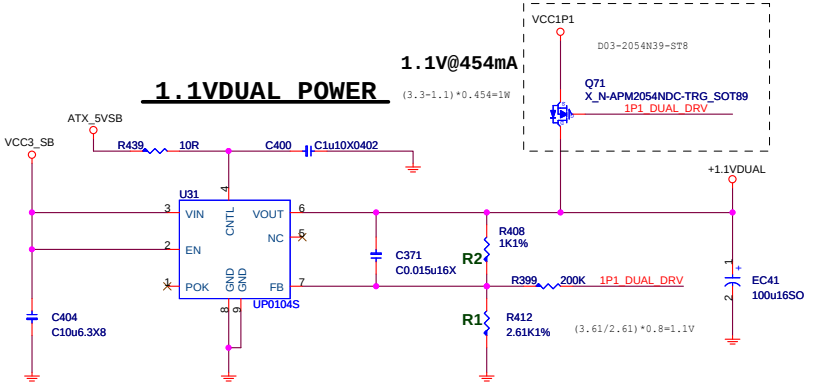
3.3V@1.2A
VCC3_SB POWER



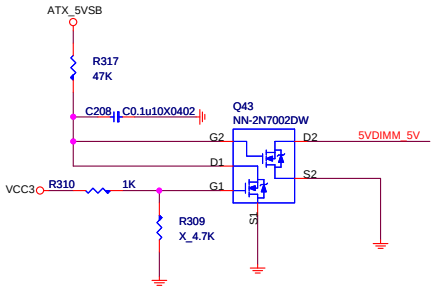
1.1VDUAL POWER

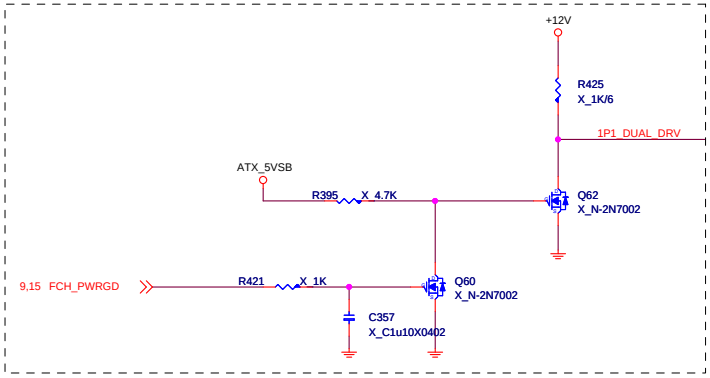
1.1V@454mA

(3.3-1.1)*0.454=1W



For special PSU sequence





MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: ACPI UPI & SYS POWER		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 23 of 34	

Note:

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VID Override Circuit

design check

APU_PG:
from FCH to APU & UP1640
PU 330R to VCC_DDR

Add TWO GND VIA in 9PIN

ISL6208BCRZ

ISL62773HRZ_QFN48-HF

BOTTOM PAD
CONNECT TO GND
Through 8 VIAs

Power soulation
R523 -> 680 ohm (OCP)
R527 -> 412 ohm (OCP_NB)
R705 -> 4.02K ohm (loadline)
R546 -> 4.02K ohm (NB_loadline)

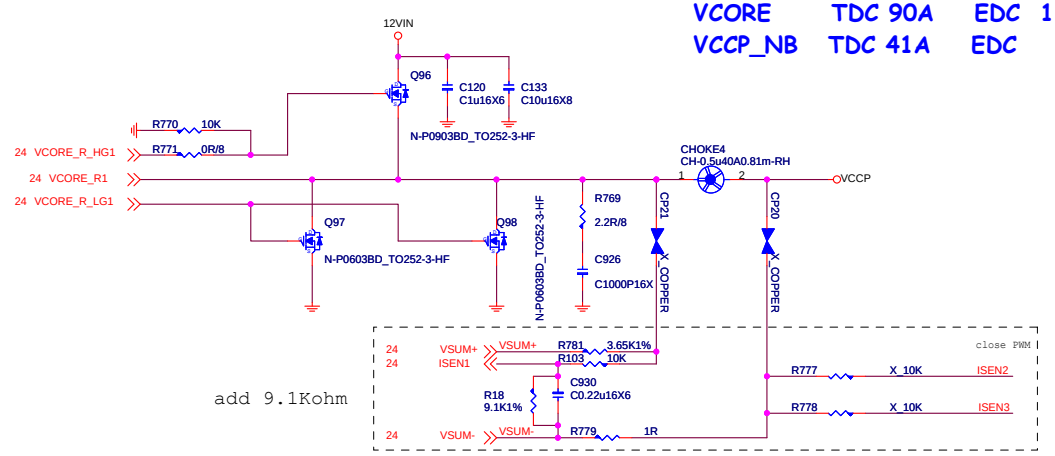
CLOSE Q96

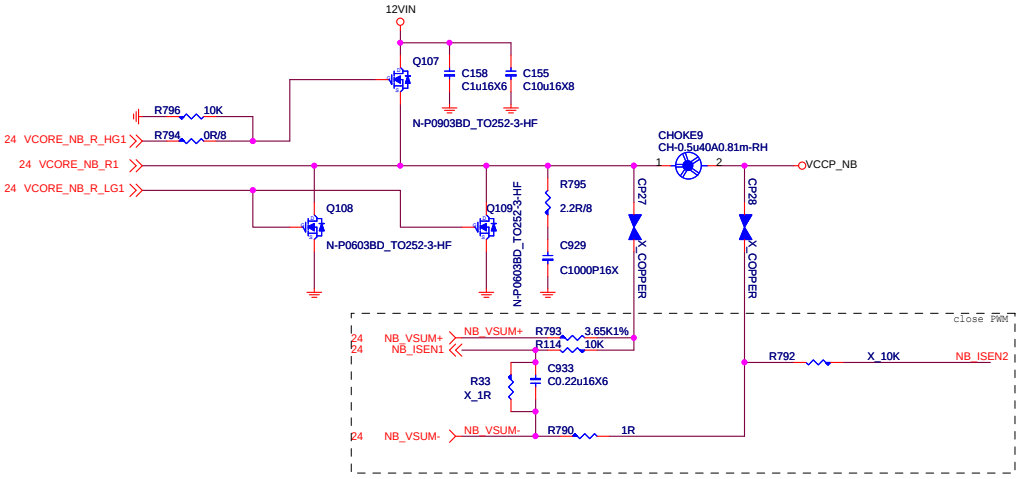
CLOSE Q107

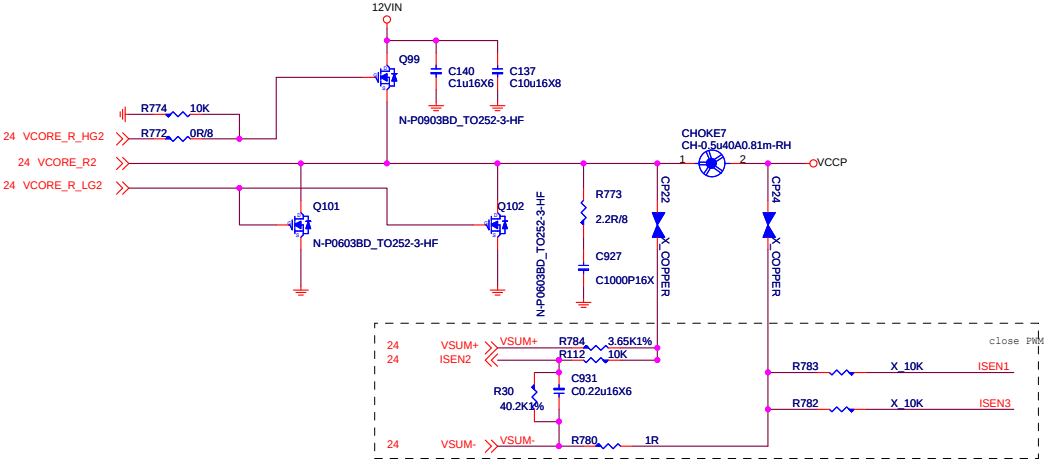
12*(3/12.1)=2.975V
>1V

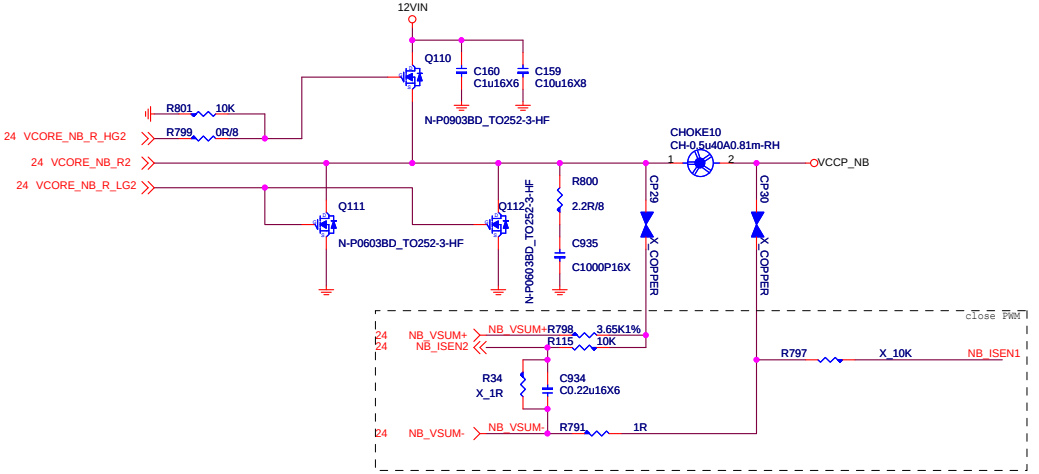
MSI MICRO-START INT'L CO.,LTD.		
Title: UP1640 3+2 Phase		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 24 of 34	

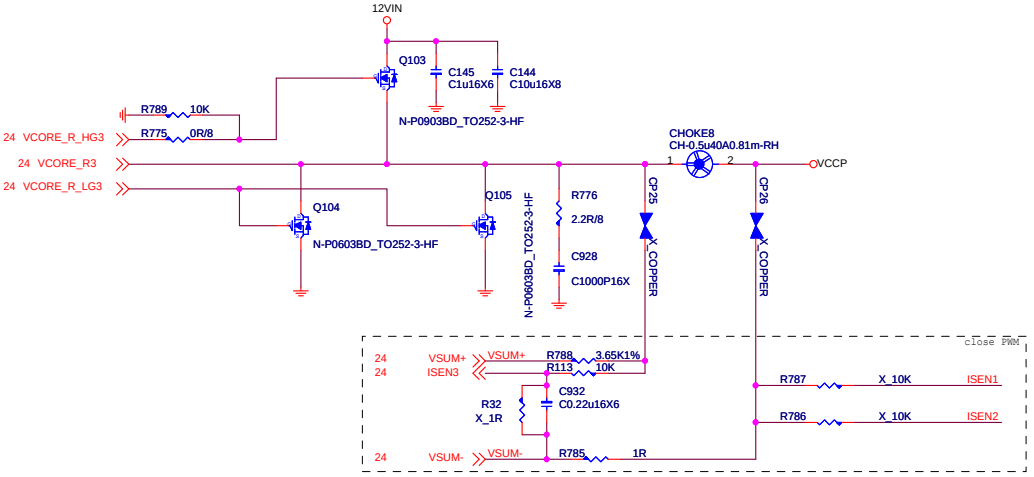
VCORE TDC 90A EDC 120A
VCCP_NB TDC 41A EDC 60A

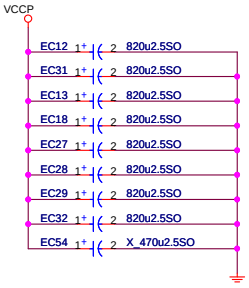


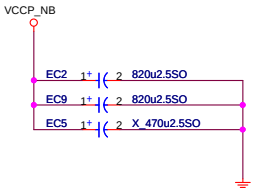












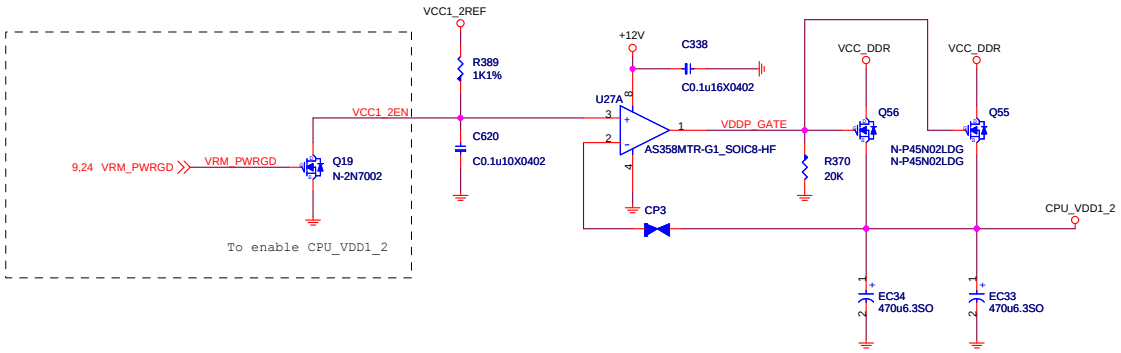
MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: APU Power		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 25 of 34	

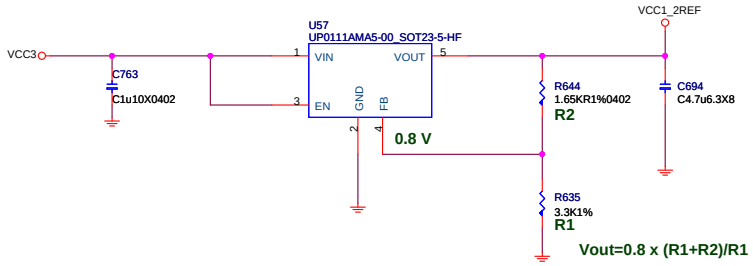
CPU_VDD1_2 POWER

1.2 V@ VDDP 6A + VDDR 4A

CPU_VDD1_2 10A

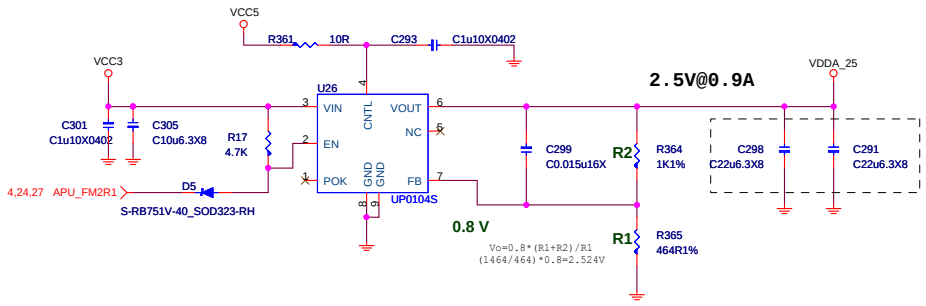


VCC1_2REF



CPU VDDA_25 POWER

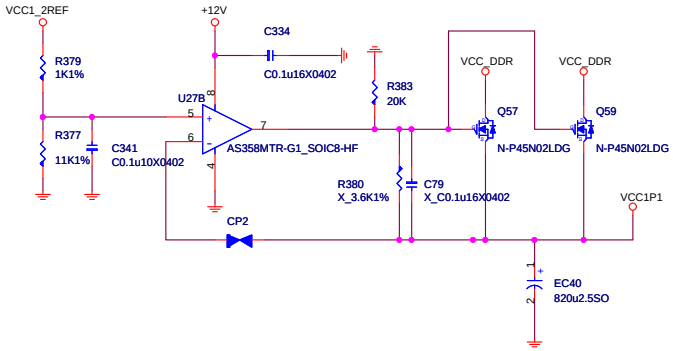
VDDA_25 0.9A



VCC1P1 POWER

VCC1P1 4.4A

1.1V@4.4A

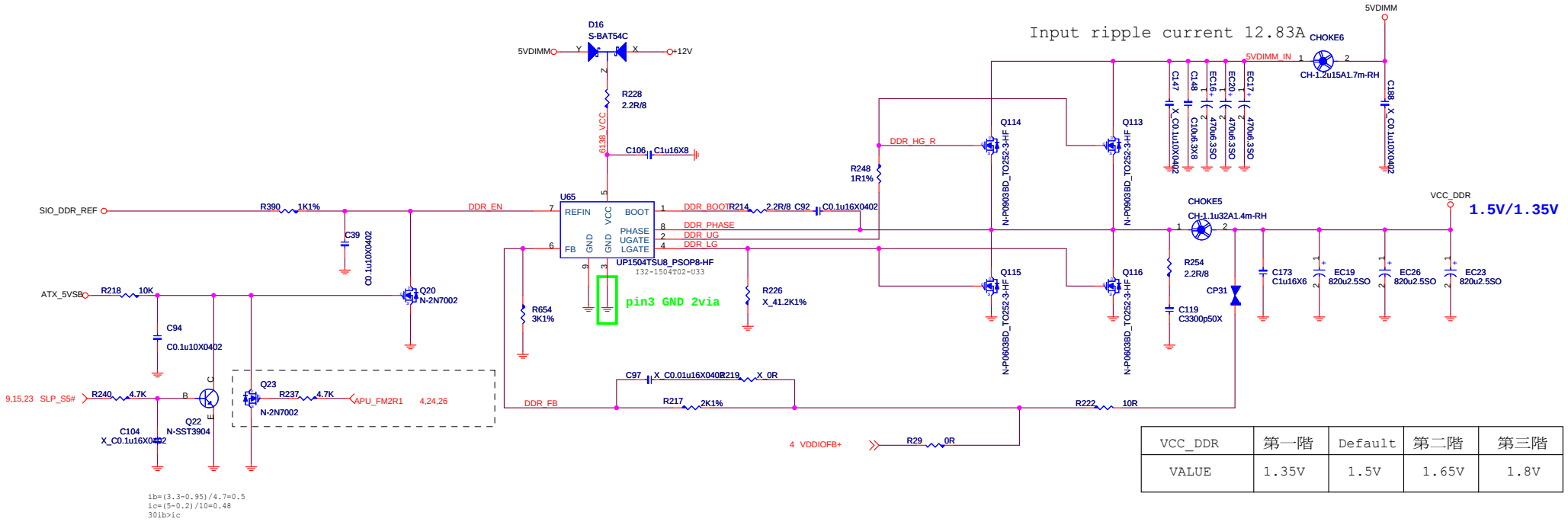


MICRO-START INTL CO.,LTD.

Title: FCH CORE Power		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 26 of 34	

DDR III 1.5V POWER

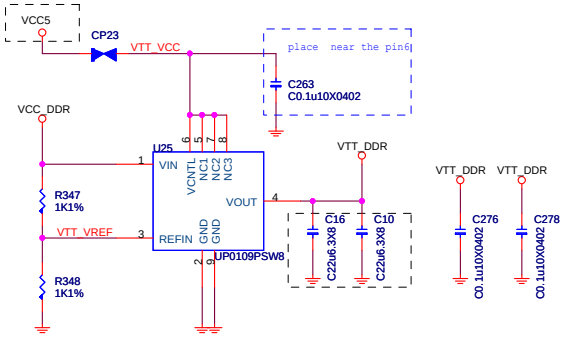
VCC_DDR 13.5A+14.4A=27.9A



VCC_DDR	第一階	Default	第二階	第三階
VALUE	1.35V	1.5V	1.65V	1.8V

VTT_DDR 1A

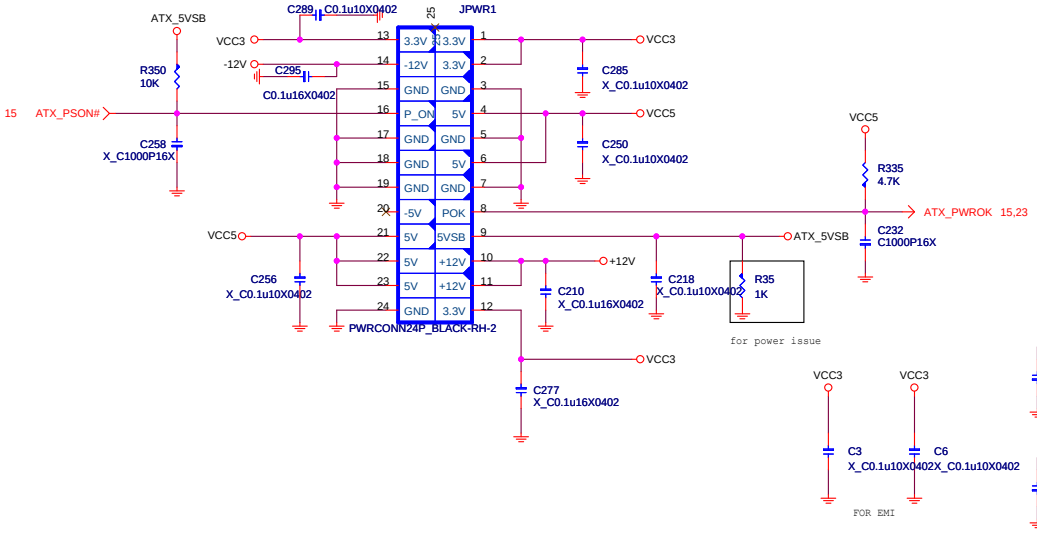
0.75V@1A VTT_DDR POWER

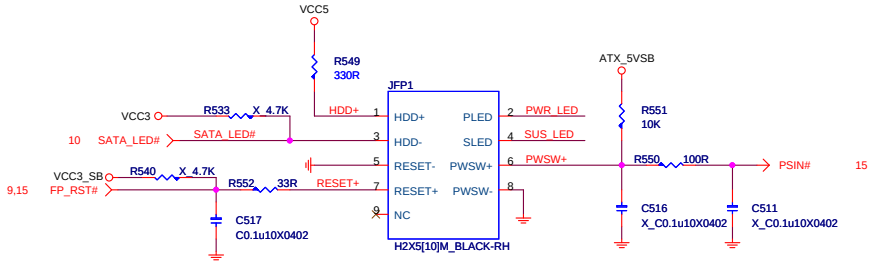


MICRO-START INT'L CO.,LTD.

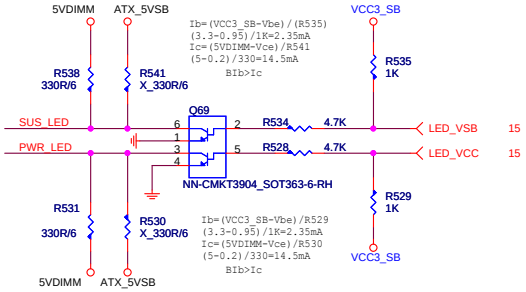
Title	DDR Power		
Size: Custom	Document Number: MS-7721		Rev: 3.2
Date: Tuesday, December 04, 2012		Sheet 27 of 34	

ATX CONNECTOR

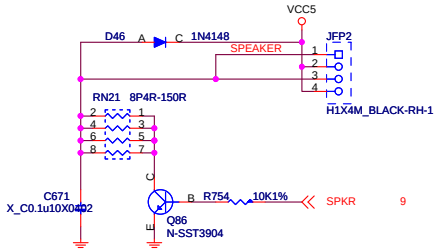




LED (for Fintek 71889)



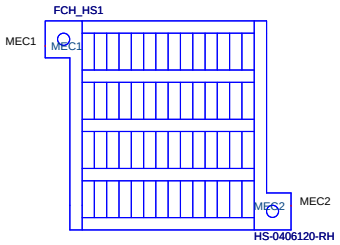
BUZZER

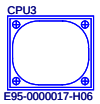


MICRO-START INT'L CO.,LTD.

Title: ATX & FRONT PANEL		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Tuesday, December 04, 2012	Sheet 28 of 34	

HEAT SINK





USBII
USB2.0
X_USBAX2M_BLACK-RH-20

Hudson-3
D2
X_AMD-218-0755111-A14-RH

Hudson-4
D2
X_AMD-218-0755117-A14-RH

R
0 ohm
X_0R

SATAIII
SATA3
X_SATA7P_WHITE-P-RH

R1
0 ohm
X_0R

MANUAL PART

AVL:
D06-0100161-F52
D06-0100101-K26

PK0-0772132-G37,精成,23,寶安恩斯邁廠(MSIS)
PK0-0772132-E48,競華,23,寶安恩斯邁廠(MSIS)

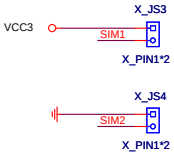
MK1
G51-M1SPD32-Q13

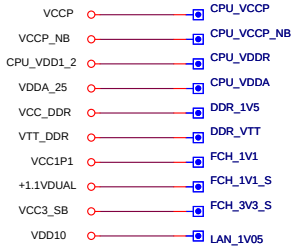
UEFI1
G51-M1SPXXA-A09

MK2
X_G51-M1SPD33-Q13

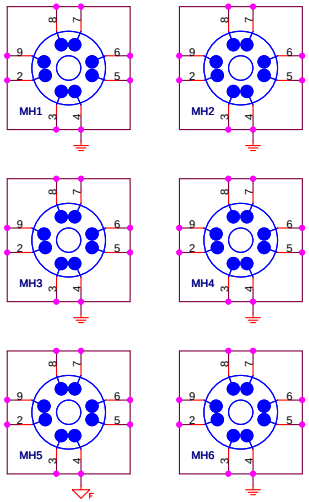
MK3
X_G51-M1SPD48-Q13

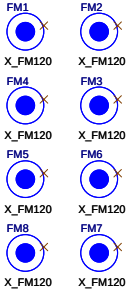
Simulation





Optics Orientation Holes





MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: BOM OPTION		
Size: Custom	Document Number: MS-7721	Rev: 3.2
Date: Thursday, December 06, 2012	Sheet 29 of 34	