

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

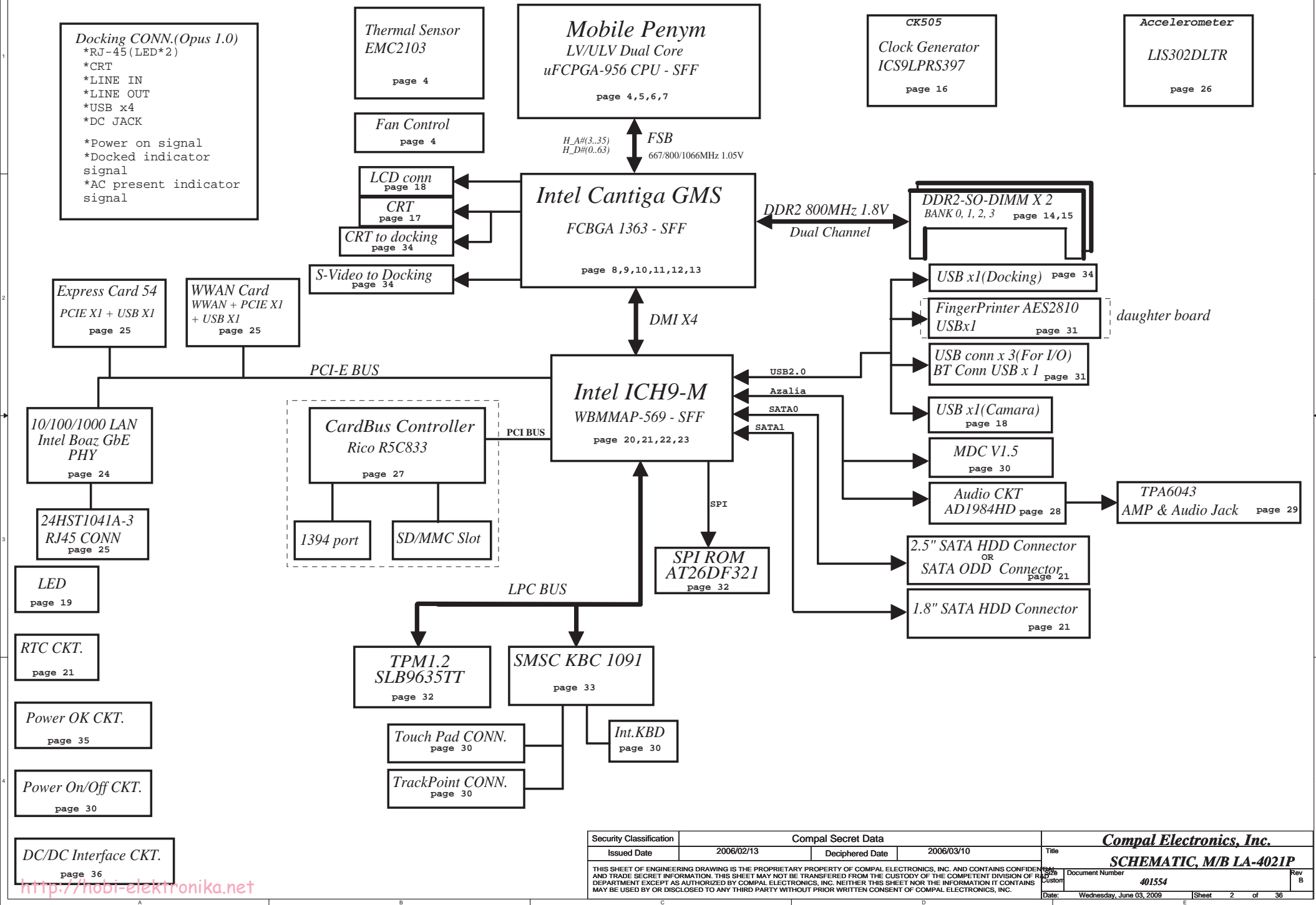
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	產出日期	
	解密日期	

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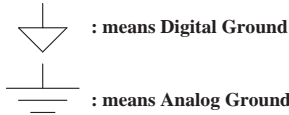


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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

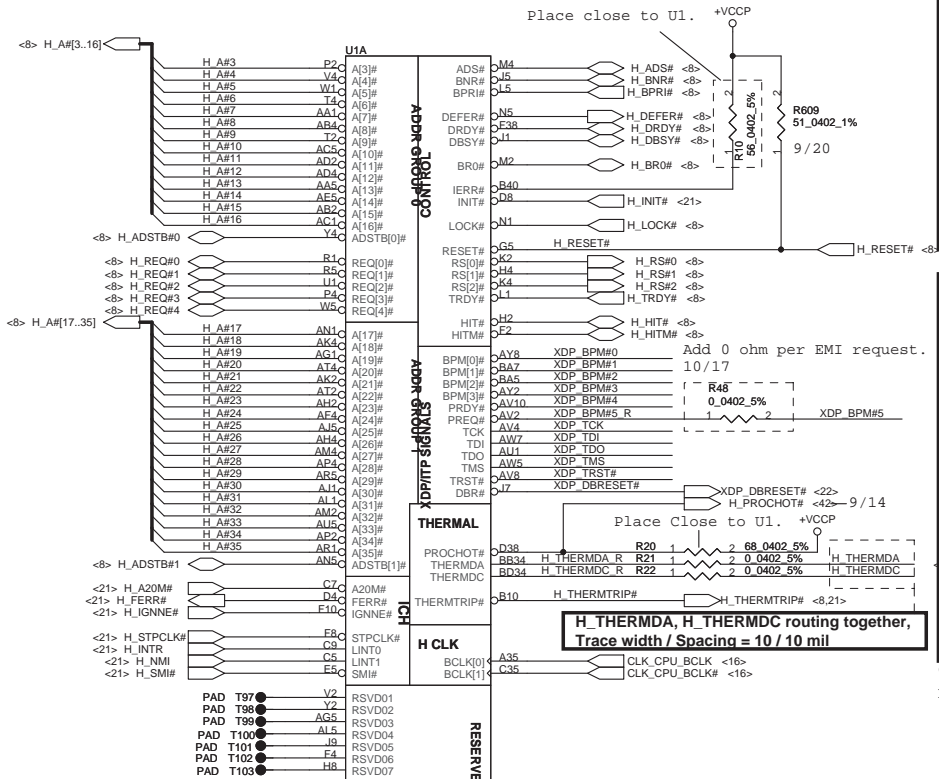
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

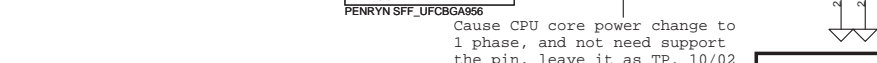
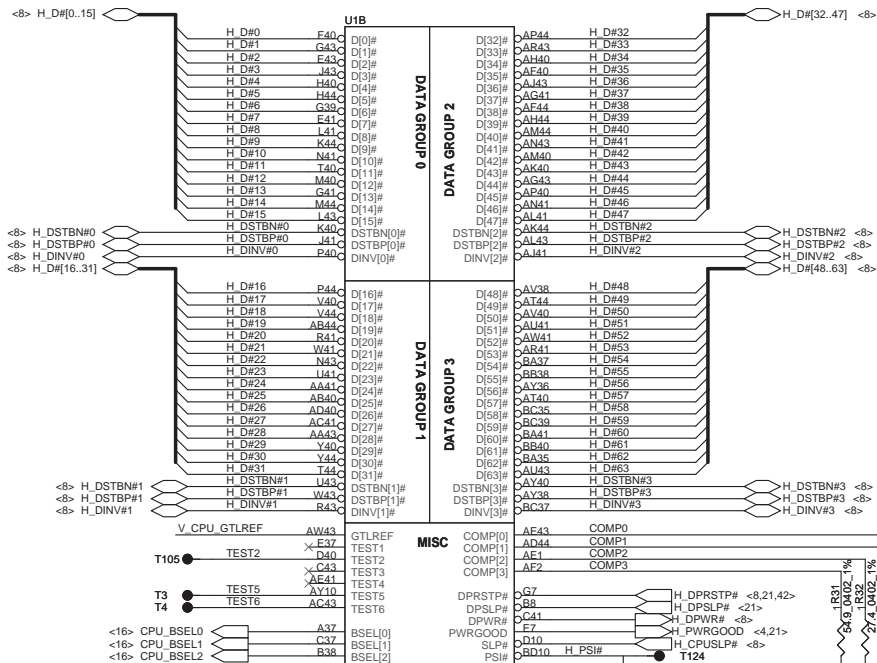
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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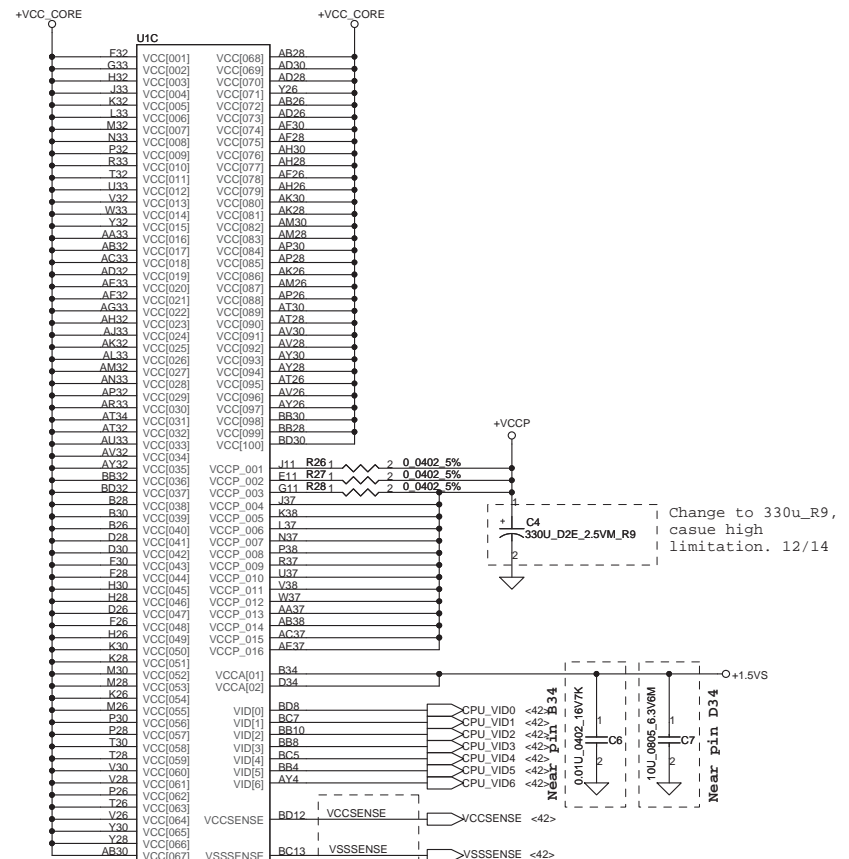


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TFS

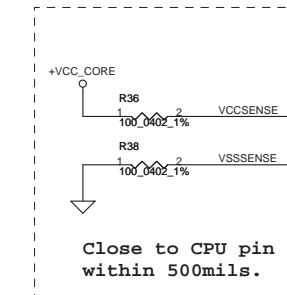
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

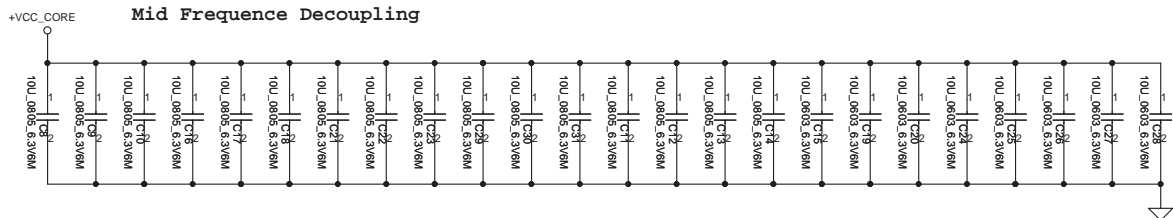


Close to CPU pin AW43 within 500mils.

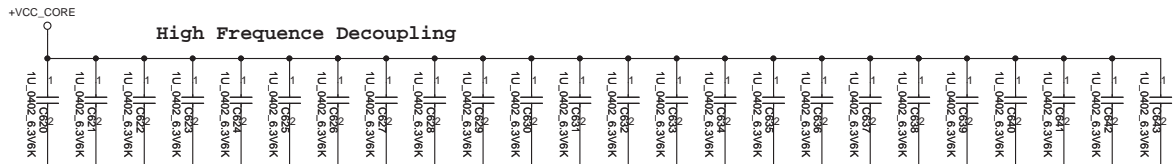
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UID			U1E		
B42	VSS[001]	VSS[082]	G25	VSS_164	VSS_280
F44	VSS[002]	VSS[083]	G23	VSS_165	VSS_281
D44	VSS[003]	VSS[084]	G21	VSS_166	VSS_282
D42	VSS[004]	VSS[085]	J25	VSS_167	VSS_283
F42	VSS[005]	VSS[086]	J23	VSS_168	VSS_284
H42	VSS[006]	VSS[087]	J21	VSS_169	VSS_285
K42	VSS[007]	VSS[088]	L26	VSS_170	VSS_286
M42	VSS[008]	VSS[089]	L23	VSS_171	VSS_287
P42	VSS[009]	VSS[090]	L21	VSS_172	VSS_288
T42	VSS[010]	VSS[091]	N25	VSS_173	VSS_289
Y42	VSS[011]	VSS[092]	N23	VSS_174	VSS_290
AB42	VSS[012]	VSS[093]	N21	VSS_175	VSS_291
AD42	VSS[013]	VSS[094]	R25	VSS_176	VSS_292
AF42	VSS[014]	VSS[095]	R23	VSS_177	VSS_293
AK42	VSS[015]	VSS[096]	R21	VSS_178	VSS_294
AM42	VSS[016]	VSS[097]	U25	VSS_179	VSS_295
AP42	VSS[017]	VSS[098]	U23	VSS_180	VSS_296
AR42	VSS[018]	VSS[099]	U21	VSS_181	VSS_297
AV44	VSS[019]	VSS[100]	W25	VSS_182	VSS_298
AV44	VSS[020]	VSS[101]	W23	VSS_183	VSS_299
AT42	VSS[021]	VSS[102]	W21	VSS_184	VSS_300
AV42	VSS[022]	VSS[103]	G31	AA25	VSS_301
AV42	VSS[023]	VSS[104]	J29	AA23	VSS_302
BA43	VSS[024]	VSS[105]	L29	AC25	VSS_303
BB42	VSS[025]	VSS[106]	L27	AC23	VSS_304
C39	VSS[026]	VSS[107]	N29	AE21	VSS_305
F39	VSS[027]	VSS[108]	N27	AE23	VSS_306
G37	VSS[028]	VSS[109]	J31	AG25	VSS_307
H38	VSS[029]	VSS[110]	J29	AG23	VSS_308
I39	VSS[030]	VSS[111]	L31	AG21	VSS_309
L39	VSS[031]	VSS[112]	N31	AG25	VSS_310
M38	VSS[032]	VSS[113]	R27	AG23	VSS_311
N39	VSS[033]	VSS[114]	R25	AG21	VSS_312
R39	VSS[034]	VSS[115]	U29	AJ25	VSS_313
T38	VSS[035]	VSS[116]	U27	AJ23	VSS_314
U39	VSS[036]	VSS[117]	U25	AJ21	VSS_315
W39	VSS[037]	VSS[118]	W29	AL25	VSS_316
Y38	VSS[038]	VSS[119]	W27	AL23	VSS_317
AA39	VSS[039]	VSS[120]	W25	AL21	VSS_318
AC39	VSS[040]	VSS[121]	AA25	AN25	VSS_319
AD38	VSS[041]	VSS[122]	AA27	AN23	VSS_320
AE39	VSS[042]	VSS[123]	AA29	AR25	VSS_321
AG39	VSS[043]	VSS[124]	AC27	AR23	VSS_322
AH38	VSS[044]	VSS[125]	AC29	AR21	VSS_323
AJ39	VSS[045]	VSS[126]	AC31	AU25	VSS_324
AL39	VSS[046]	VSS[127]	AE29	AU23	VSS_325
AM38	VSS[047]	VSS[128]	AE27	AU21	VSS_326
AN39	VSS[048]	VSS[129]	AG29	AW25	VSS_327
AR39	VSS[049]	VSS[130]	AG27	AW23	VSS_328
AS37	VSS[050]	VSS[131]	AJ29	AW21	VSS_329
AT38	VSS[051]	VSS[132]	AJ27	BA25	VSS_330
AU39	VSS[052]	VSS[133]	AE31	BA23	VSS_331
AW39	VSS[053]	VSS[134]	AG31	BA21	VSS_332
AX39	VSS[054]	VSS[135]	AE33	BA25	VSS_333
AY39	VSS[055]	VSS[136]	AJ31	BC25	VSS_334
BA39	VSS[056]	VSS[137]	AL29	BC23	VSS_335
BB41	VSS[057]	VSS[138]	AL27	BC21	VSS_336
BD40	VSS[058]	VSS[139]	AN29	C17	VSS_337
BD38	VSS[059]	VSS[140]	AN27	C19	VSS_338
R36	VSS[060]	VSS[141]	AN25	C17	VSS_339
H34	VSS[061]	VSS[142]	AN23	F17	VSS_340
D36	VSS[062]	VSS[143]	AN21	F19	VSS_341
K34	VSS[063]	VSS[144]	AR29	G19	VSS_342
M34	VSS[064]	VSS[145]	AR27	G17	VSS_343
M36	VSS[065]	VSS[146]	AR25	G15	VSS_344
P34	VSS[066]	VSS[147]	AW29	L17	VSS_345
T34	VSS[067]	VSS[148]	AW27	L19	VSS_346
V34	VSS[068]	VSS[149]	AW25	N19	VSS_347
T36	VSS[069]	VSS[150]	AW23	N17	VSS_348
Y34	VSS[070]	VSS[151]	AW21	R19	VSS_349
AB34	VSS[071]	VSS[152]	BA29	R17	VSS_350
AD34	VSS[072]	VSS[153]	BA27	U19	VSS_351
AE34	VSS[073]	VSS[154]	BA25	U17	VSS_352
AF34	VSS[074]	VSS[155]	BC29	W19	VSS_353
AH34	VSS[075]	VSS[156]	BC27	W17	VSS_354
AK34	VSS[076]	VSS[157]	BA31	W15	VSS_355
AM34	VSS[077]	VSS[158]	BC31	AA19	VSS_356
AP34	VSS[078]	VSS[159]	C21	AA17	VSS_357
	VSS[079]	VSS[160]	C23	AC19	VSS_358
	VSS[080]	VSS[161]	C25	AC17	VSS_359
	VSS[081]	VSS[162]	E25	AE19	VSS_360
		VSS[163]	E23	AE17	VSS_361
			E21	AG19	VSS_362
				AG17	VSS_363
				AJ19	VSS_364
				AJ17	VSS_365
				AN19	VSS_366
				AN17	VSS_367
				AR19	VSS_368
				AR17	VSS_369
				AU19	VSS_370
				AU17	VSS_371
				AW19	VSS_372
				AW17	VSS_373
				BA19	VSS_374
				BA17	VSS_375
				BC19	VSS_376
				BC17	VSS_377
				C11	VSS_378
				C15	VSS_379
				E15	VSS_380
				H10	VSS_381
				M12	VSS_382
				J15	VSS_383
				L15	VSS_384
				N15	VSS_385
				M10	VSS_386
				T12	VSS_387
				R15	VSS_388
				U15	VSS_389
				W15	VSS_390
				T10	VSS_391
				Y12	VSS_392
				AD12	VSS_393
					VSS_394
					VSS_395

Mid Frequency Decoupling



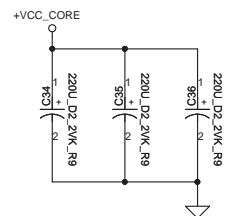
High Frequency Decoupling



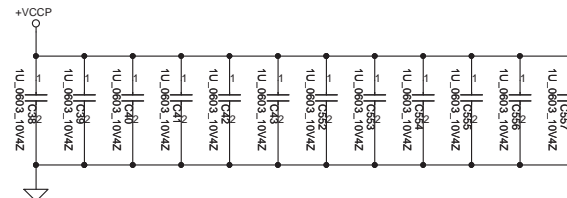
6/14 :Replace 12pcs 10uF_0805 to 24 pcs 1uF_0402 for CPU transient fail issue.

ESR <= 1.5m ohm

Near CPU CORE regulator



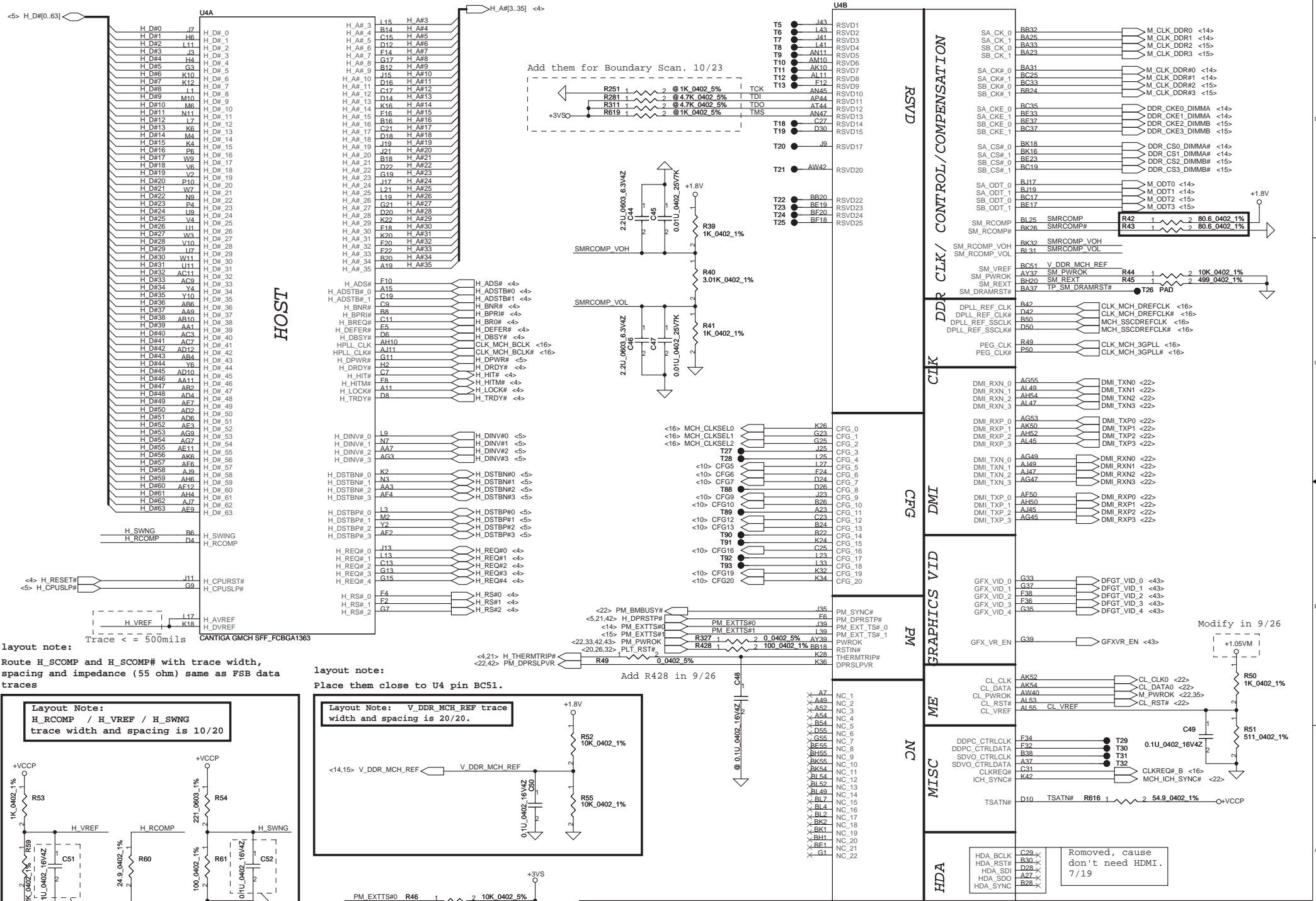
Del C37 to improve power plan. 6/14

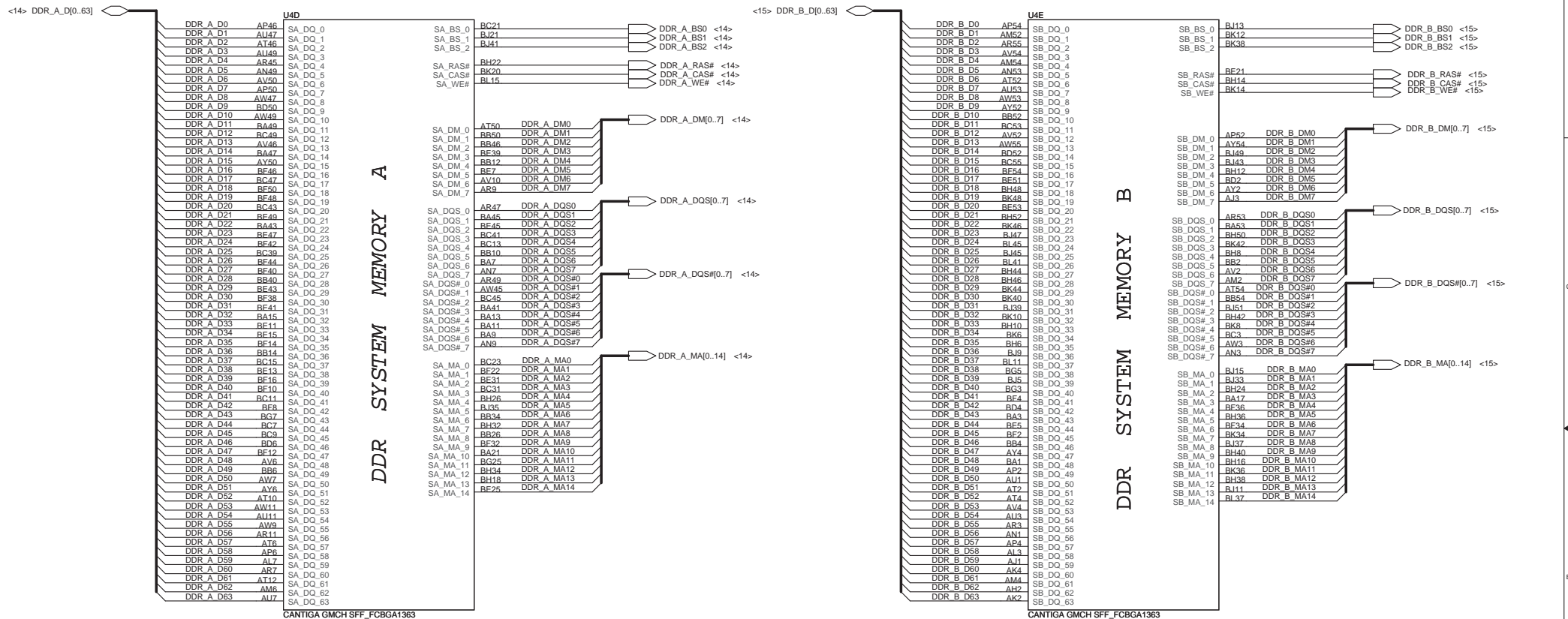


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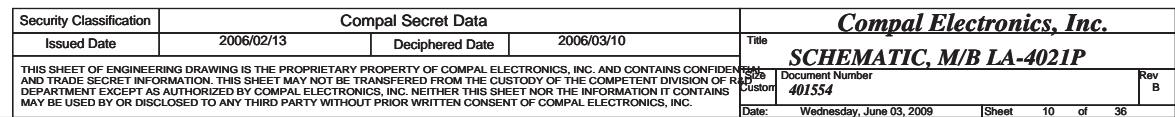
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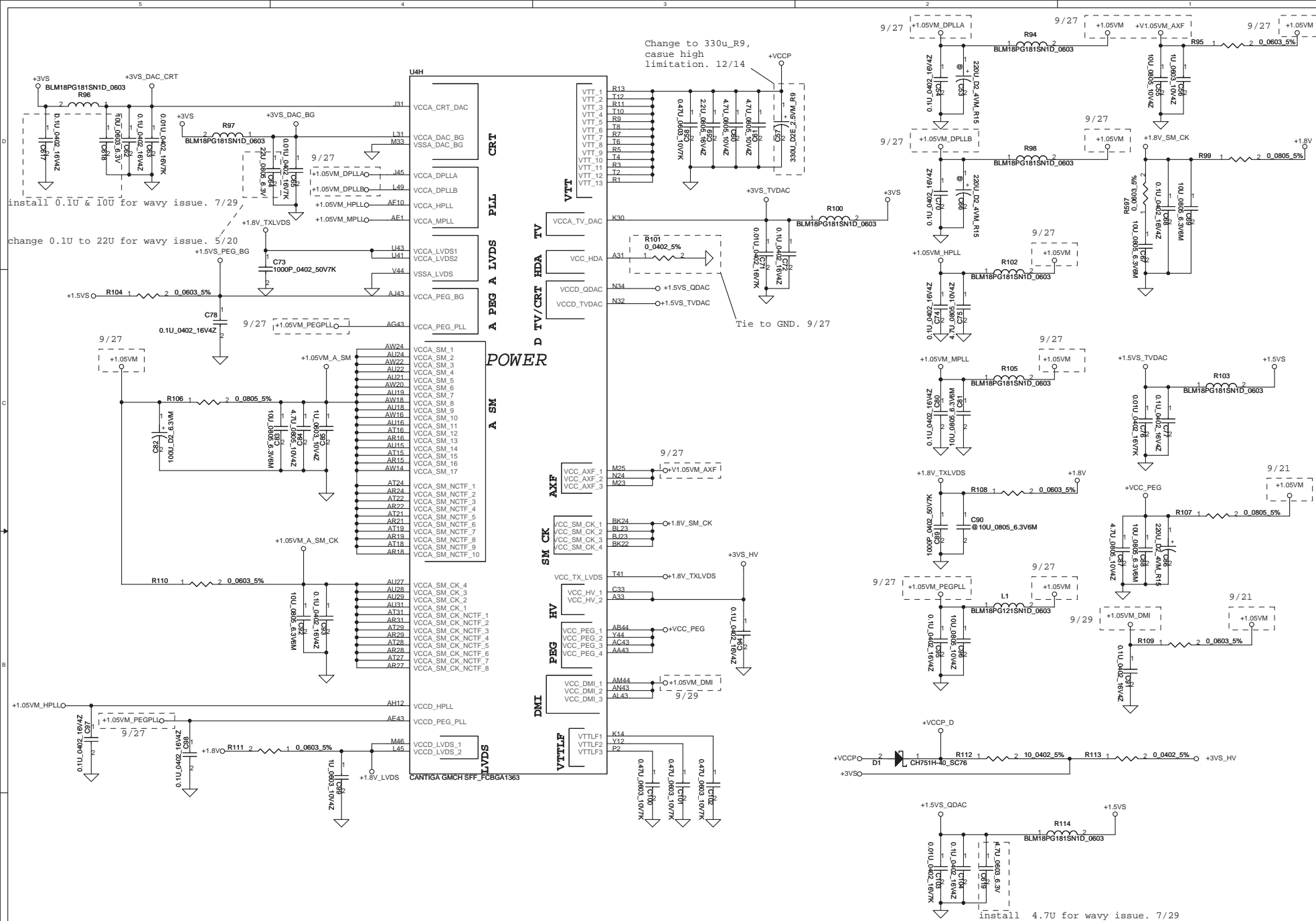
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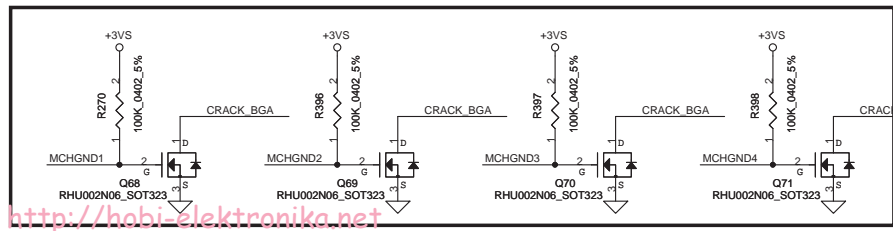
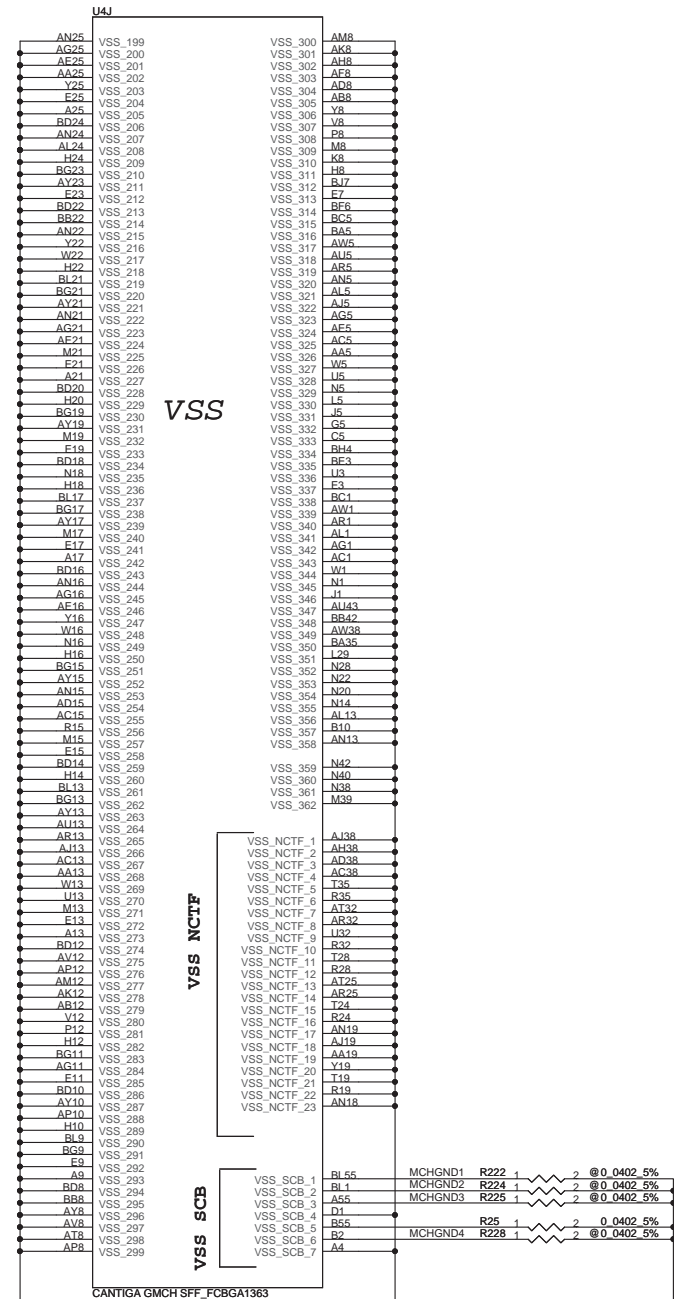
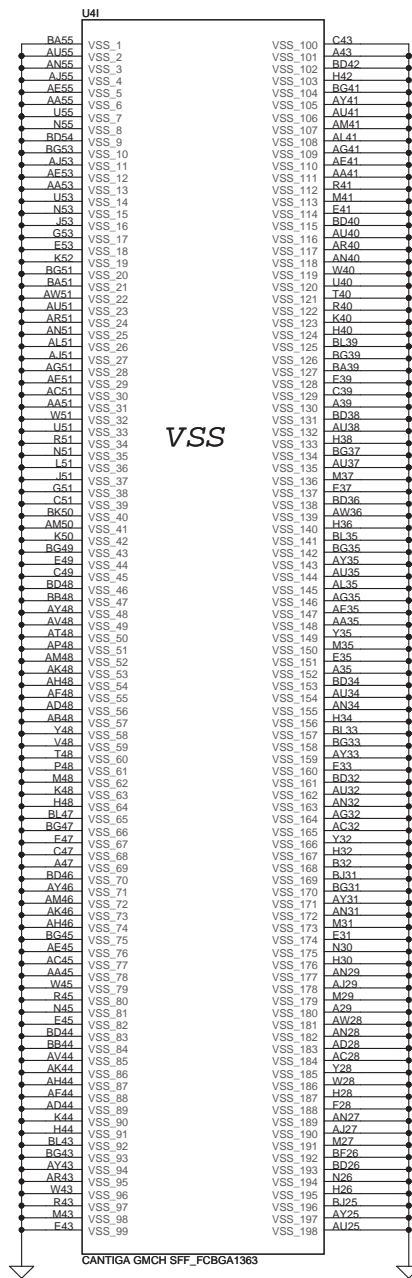


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<9> DDR_A_DQS#[0..7]

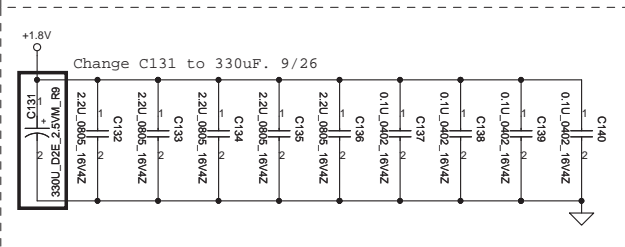
<9> DDR_A_D[0..63]

<9> DDR_A_DM[0..7]

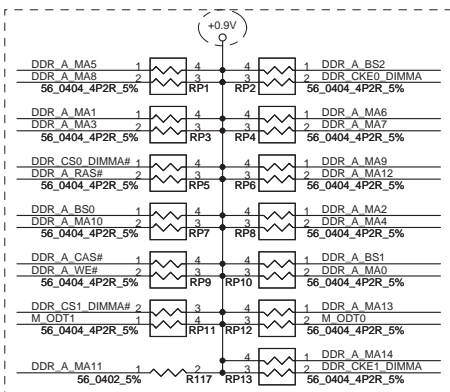
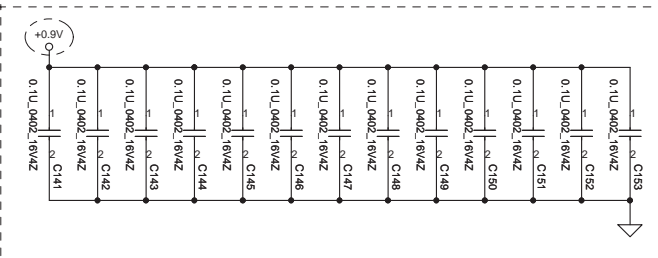
<9> DDR_A_DQS[0..7]

<9> DDR_A_MA[0..14]

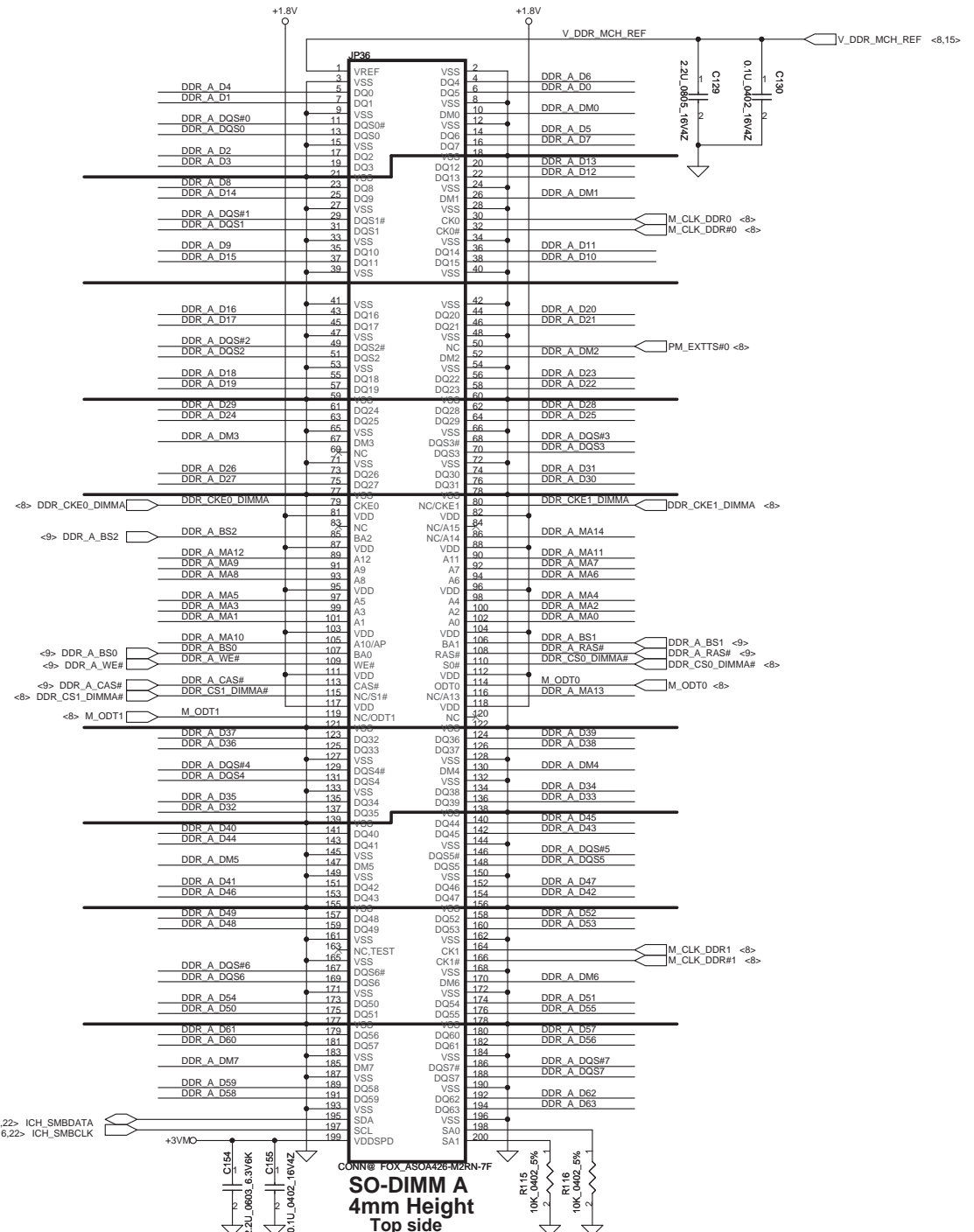
Layout Note:
Place near JP36



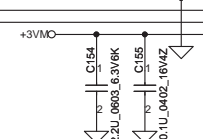
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



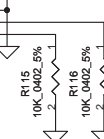
Layout Note:
Place these resistor
closely JP9, all
trace length Max=1.5"



<15,16,22> ICH_SMBDATA
<15,16,22> ICH_SMBCLK



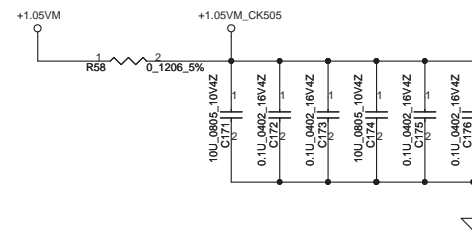
CONN FOX_ASO428-M2RN-7F
SO-DIMM A
4mm Height
Top side



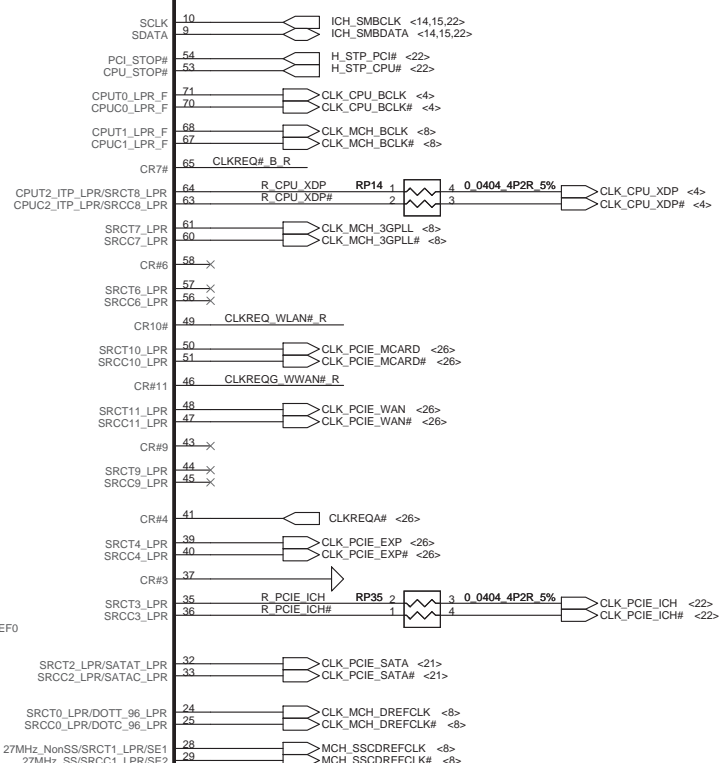
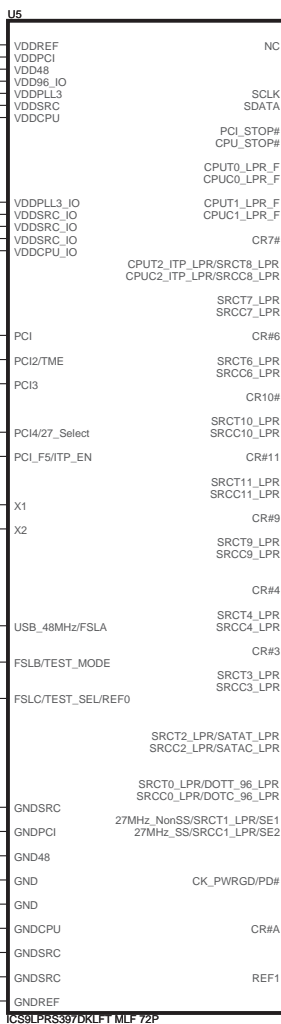
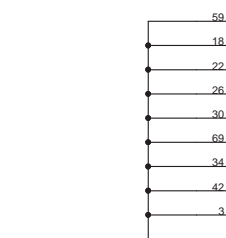
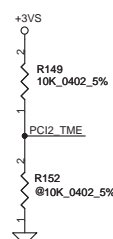
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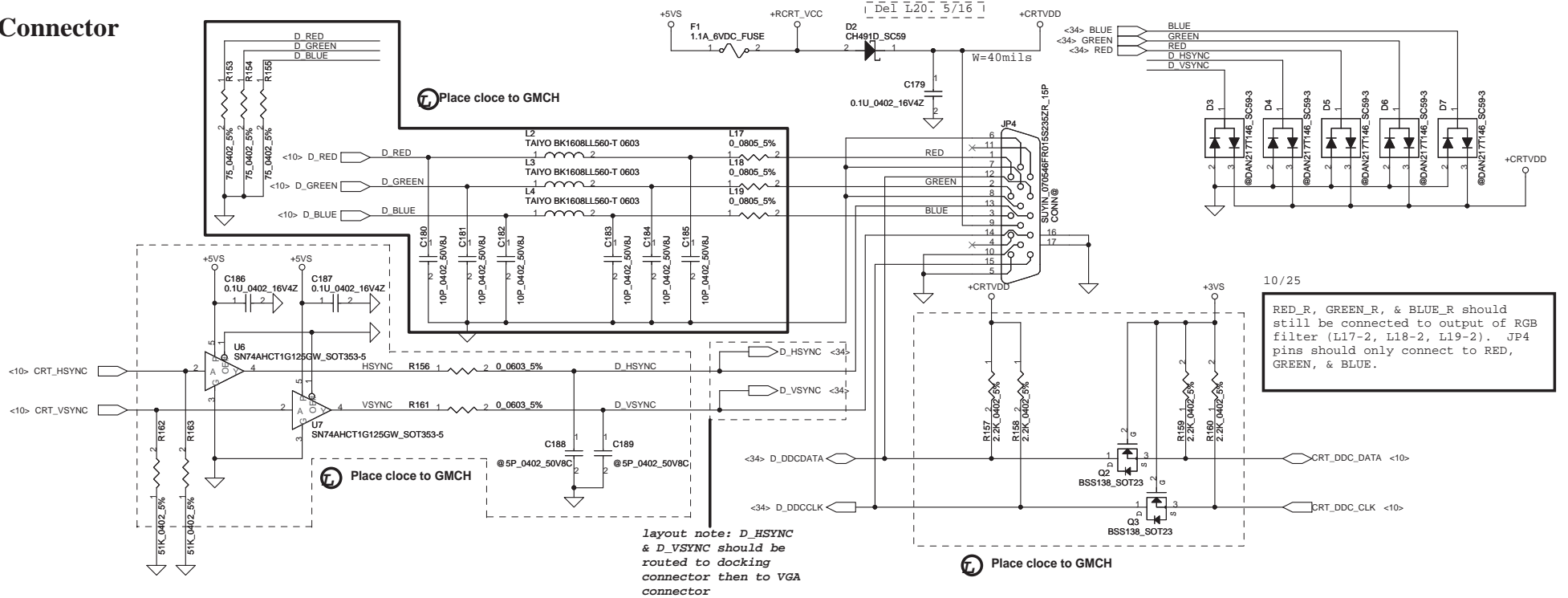


Mount C157 & C166 tp solve
WWAN noise issue. 1/23

[illegible]

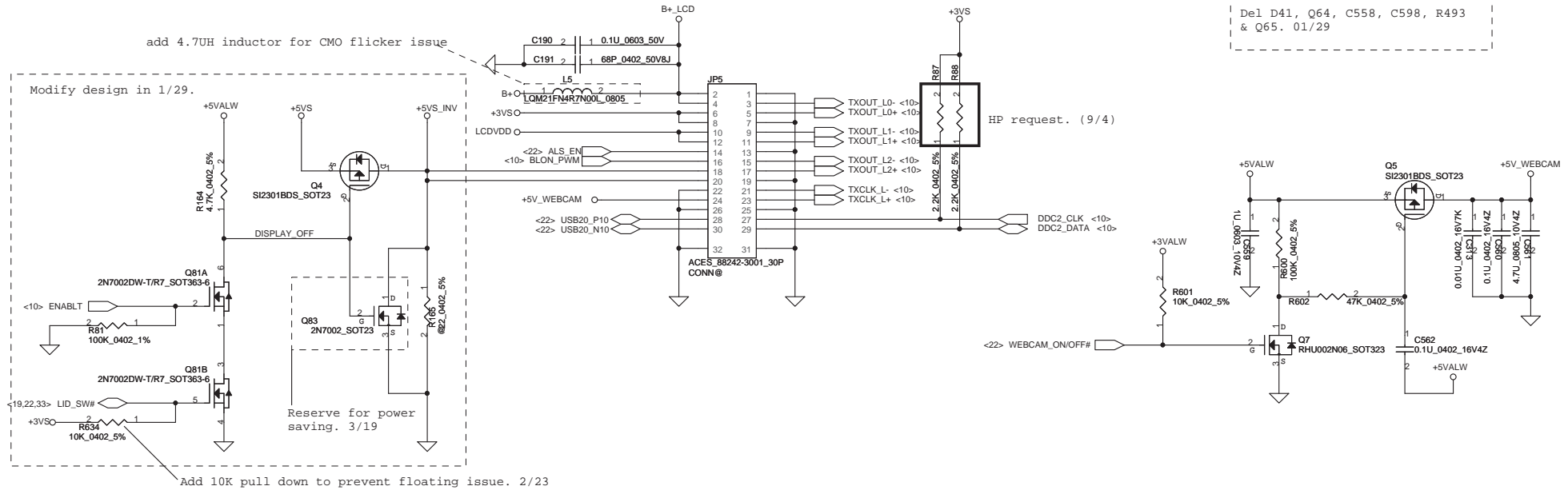
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CRT Connector

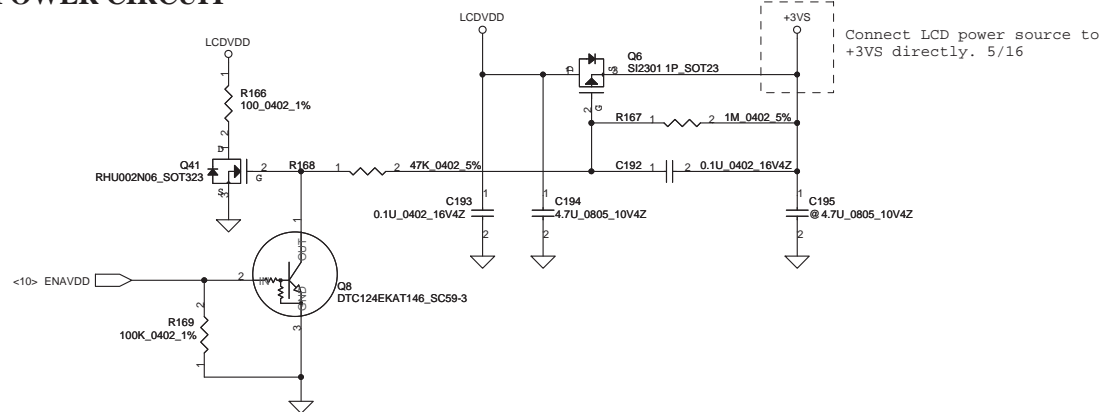


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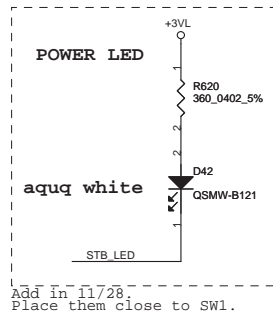
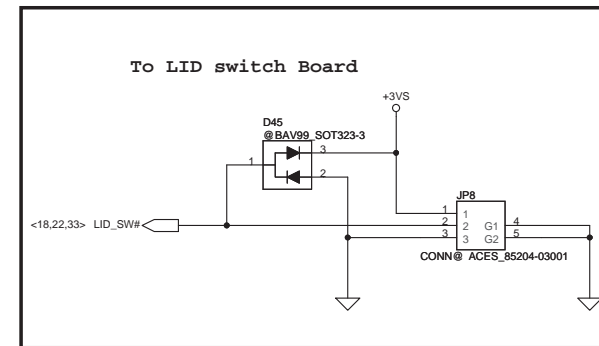
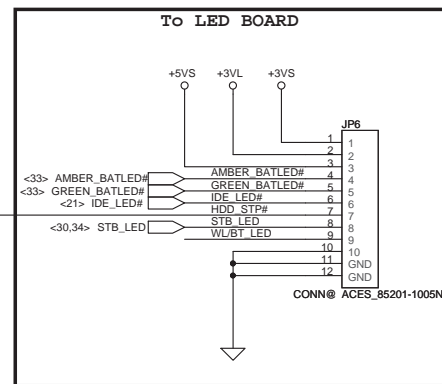
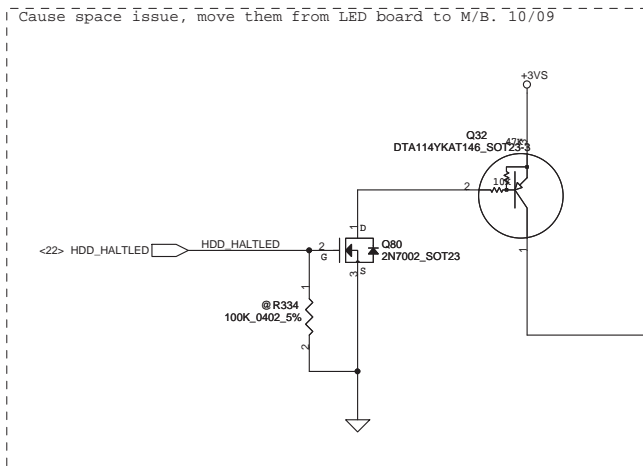
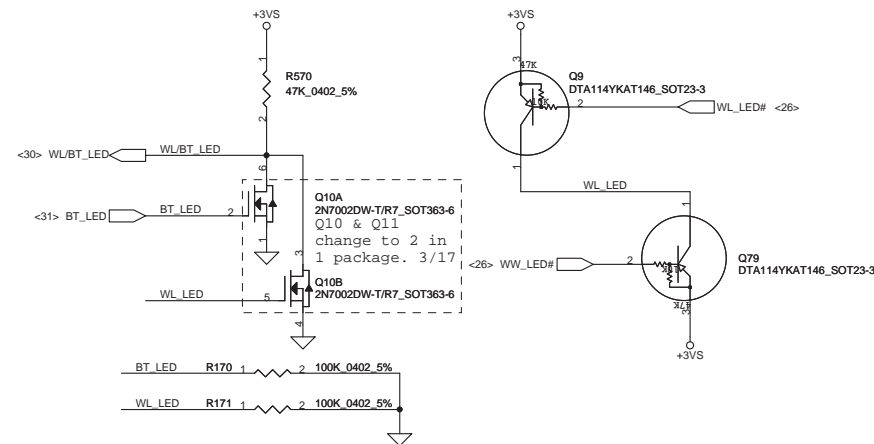
LCD/PANEL BD. CONN.



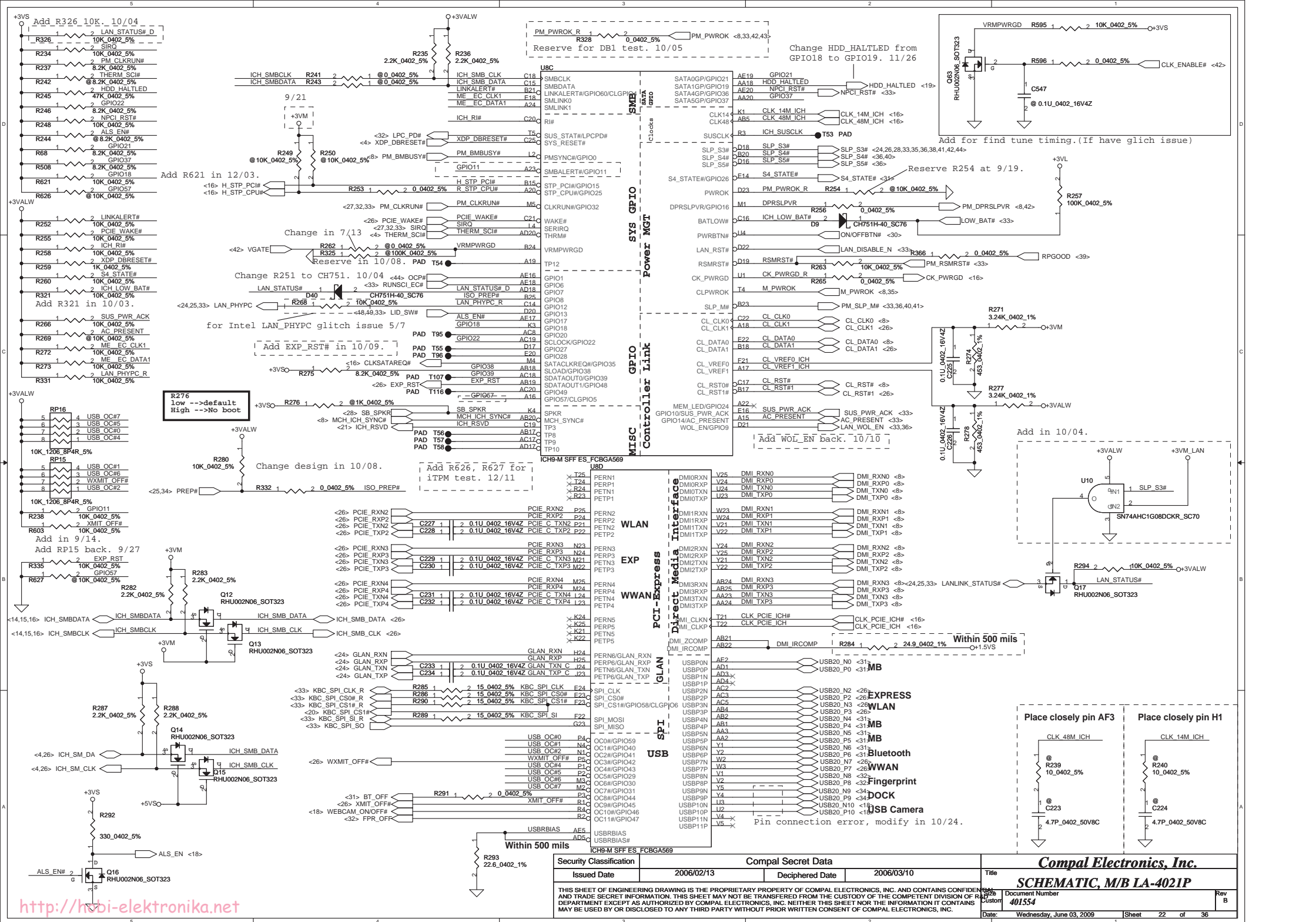
LCD POWER CIRCUIT



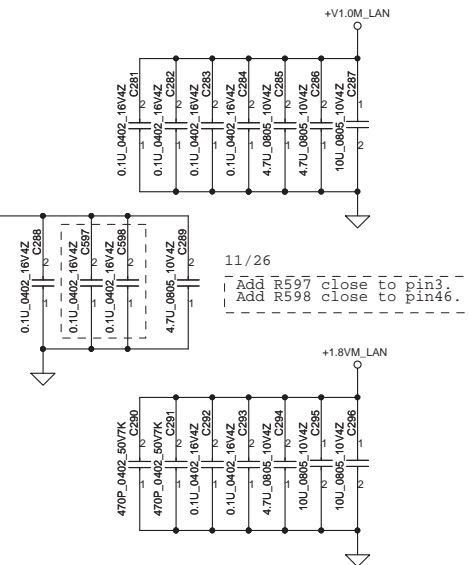
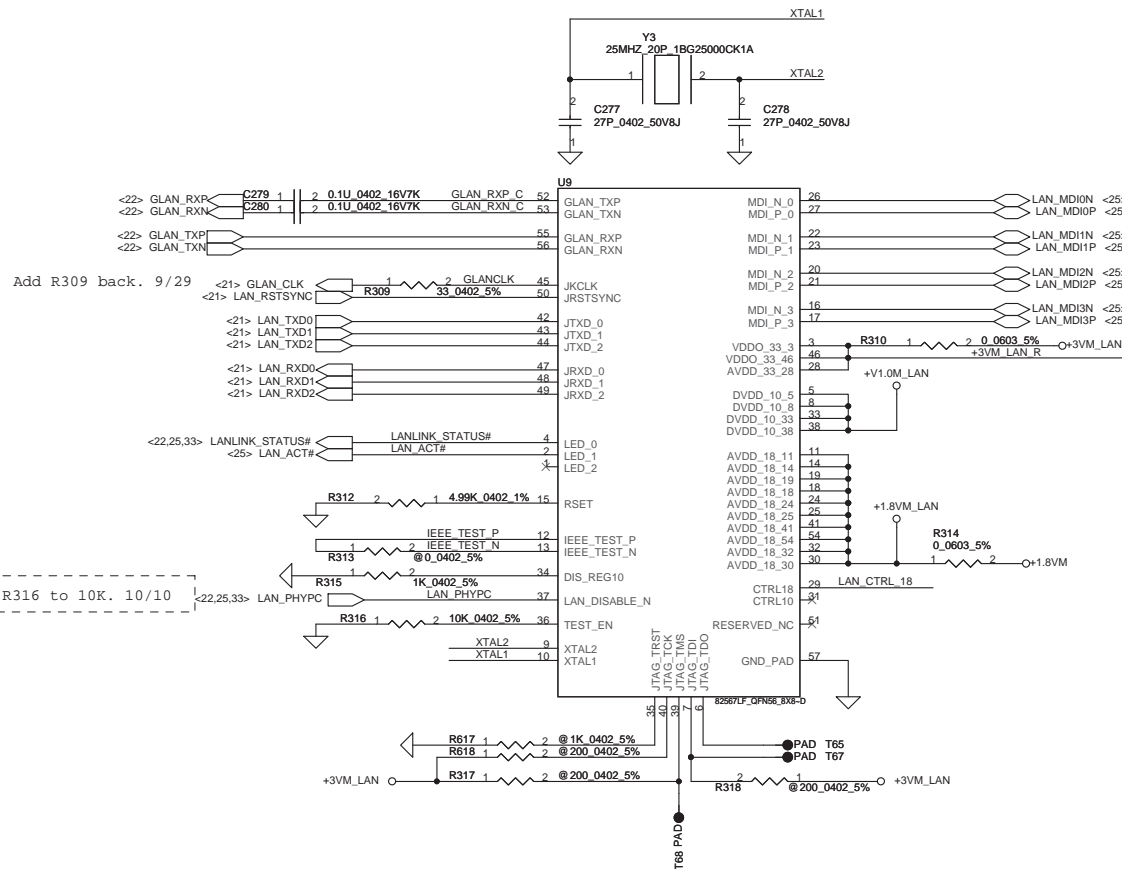
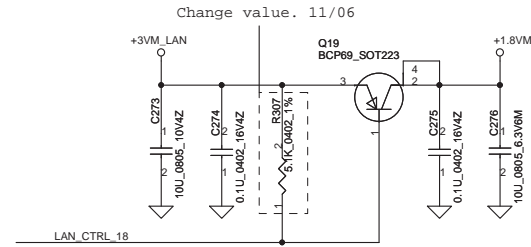
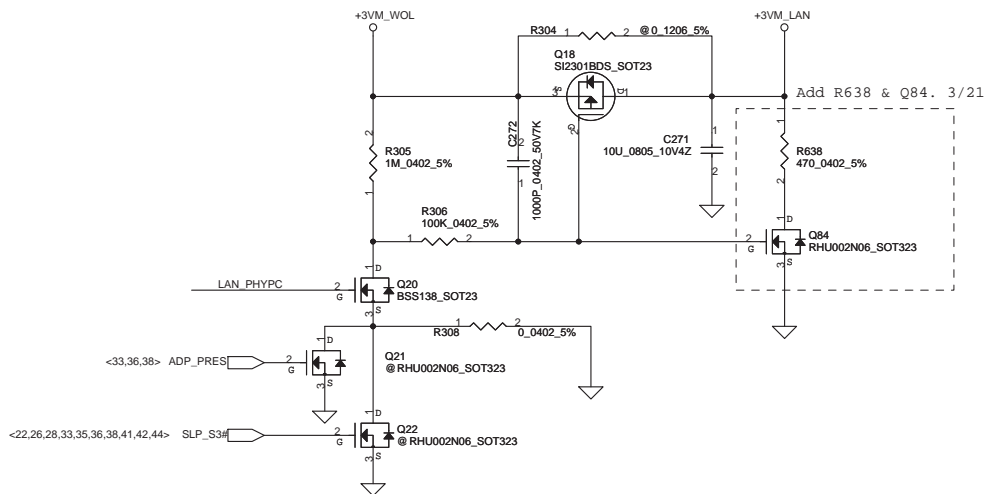
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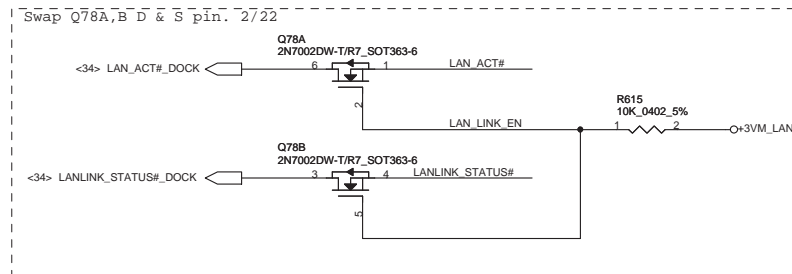




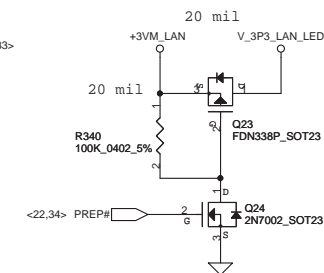
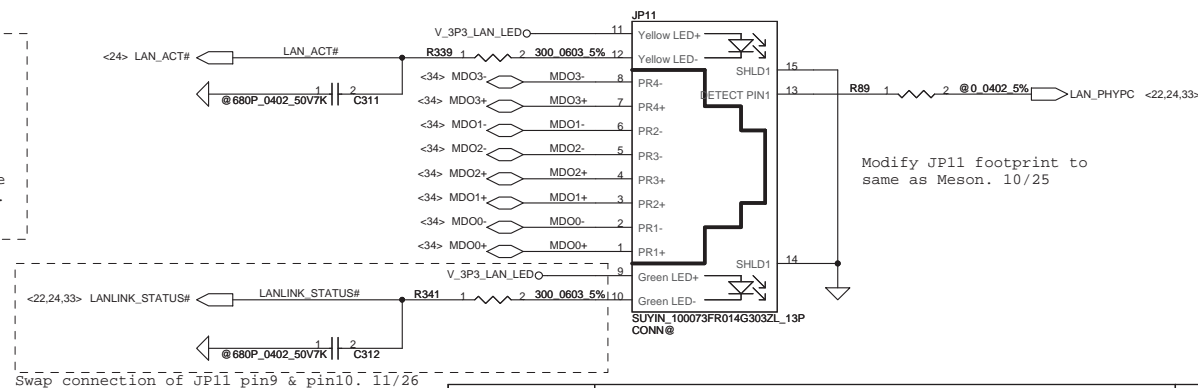
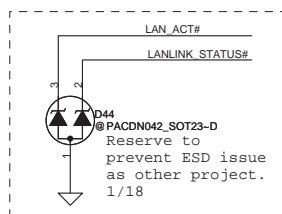
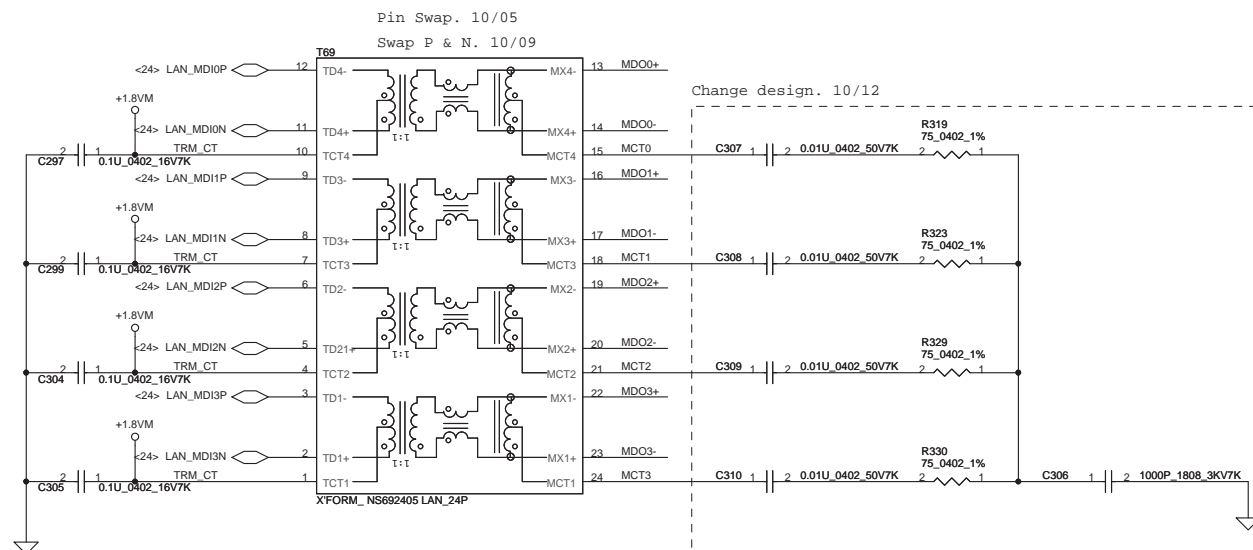
Change R315 to 1K and R316 to 10K. 10/10

11/26
Add R597 close to pin3.
Add R598 close to pin46.

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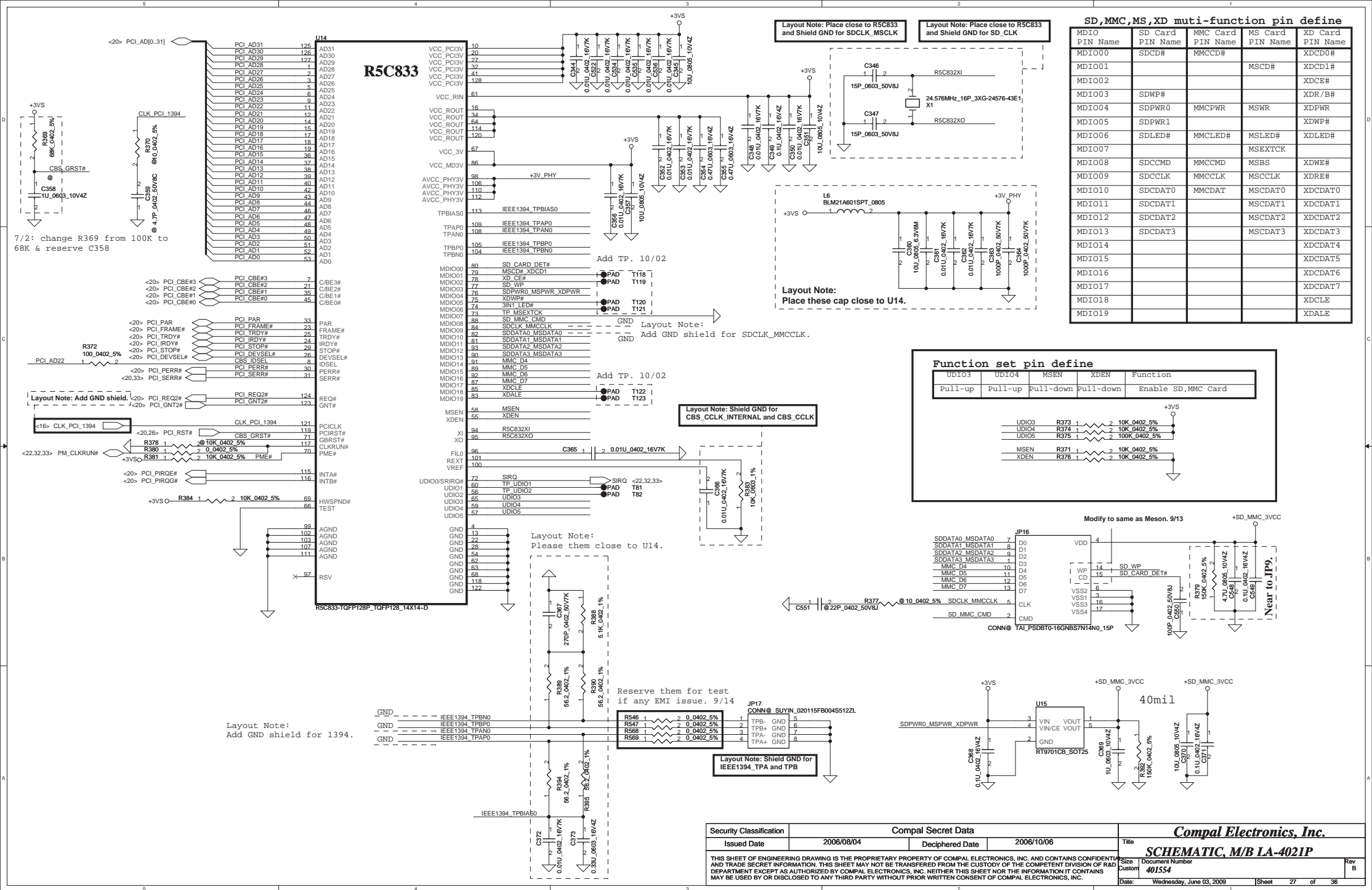
Delete all termination cause they are already inside BOAZMAN. 9/28



Swap connection of JP11 pin9 & pin10. 11/26

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AMP. FOR INTERNAL SPEAKER

	GAIN1	GAIN0
10dB	0	0
12dB	0	1
15.6dB	1	0
21.6dB	1	1



SWITCH BOARD.

The schematic diagram illustrates the internal wiring of a switch board. It features a central 12-pin connector labeled JP23. The connections are as follows:

- Pin 1:** +3V (connected to +3V_L)
- Pin 2:** +3V (connected to +3V_L)
- Pin 3:** CAP (connected to CAP_RST_EC)
- Pin 4:** RST (connected to CAP_RST_EC)
- Pin 5:** EC (connected to CAP_RST_EC)
- Pin 6:** WU/BT (connected to WU/BT_LED)
- Pin 7:** LED (connected to WU/BT_LED)
- Pin 8:** I2C_CLK (connected to I2C_CLK)
- Pin 9:** I2C_DAT (connected to I2C_DAT)
- Pin 10:** I2C_INT (connected to I2C_INT)
- Pin 11:** STB_LED (connected to STB_LED)
- Pin 12:** GND1 (connected to GND2)

Additional components and connections include:

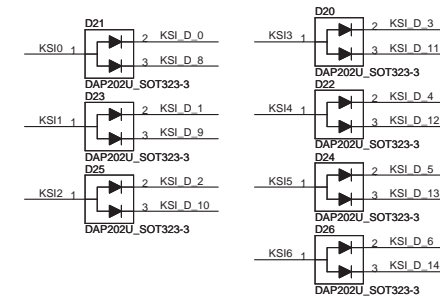
- Resistors:** R466 (5.1K 0402 5%) and R467 (5.1K 0402 5%) are connected between +3V_L and the I2C lines. R468 (10K 0402 5%) is connected between I2C_INT and ground.
- LEDs:** D47 and D49 are PACDN042_SOT23-D LEDs connected to the WU/BT_LED and STB_LED lines, respectively.
- Connectors:** I2C_CLK, I2C_DAT, I2C_INT, CAP_RST_EC, WU/BT_LED, and STB_LED are external connectors.

MDC 1.5 Conn.

The MDC 1.5 Conn. section includes the JP24 connector (CONN# ACES_88025-120L_12P) and the JP26 connector (CONN# ACES_85204-02001_2P). It shows the connection of various signals to the AC97 controller (U37) and the AC97 codec (U38). The JP24 connector is connected to the AC97 controller (U37) and the AC97 codec (U38). The JP26 connector is connected to the AC97 controller (U37) and the AC97 codec (U38). The AC97 controller (U37) is connected to the AC97 codec (U38) via the AC97_SDO, AC97_SYNC, AC97_SDI, and AC97_BITCLK signals. The AC97 controller (U37) is also connected to the AC97 codec (U38) via the AC97_RST# and MODEM_DISABLE# signals. The AC97 controller (U37) is connected to the AC97 codec (U38) via the AC97_SDO, AC97_SYNC, AC97_SDI, and AC97_BITCLK signals. The AC97 controller (U37) is also connected to the AC97 codec (U38) via the AC97_RST# and MODEM_DISABLE# signals.

RJ-11 Conn.

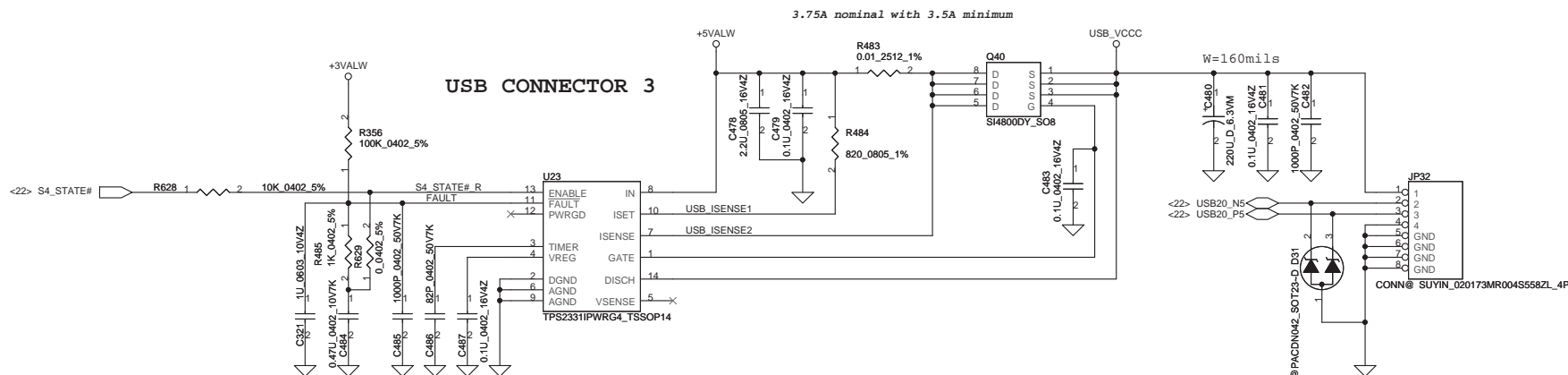
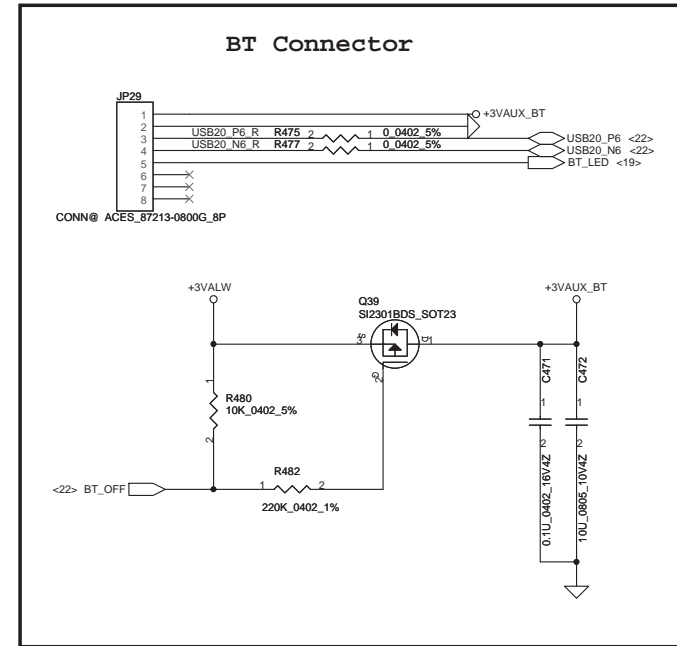
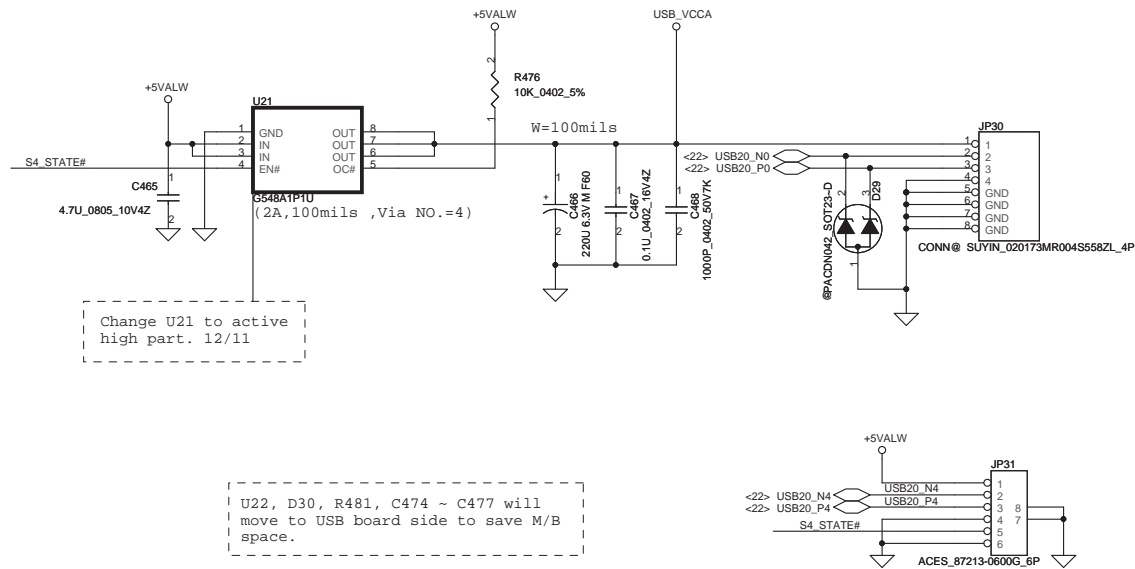
The RJ-11 Conn. section includes the JP25 connector (CONN# ACES_88266-02001) and the JP26 connector (CONN# ACES_85204-02001_2P). It shows the connection of the RJ-11 signals to the AC97 controller (U37) and the AC97 codec (U38). The JP25 connector is connected to the AC97 controller (U37) and the AC97 codec (U38). The JP26 connector is connected to the AC97 controller (U37) and the AC97 codec (U38). The AC97 controller (U37) is connected to the AC97 codec (U38) via the RJ-11 signals. The AC97 controller (U37) is also connected to the AC97 codec (U38) via the RJ-11 signals.

[illegible][illegible]

TrackPoint CONN. T/P BOARD.

The diagram illustrates the electrical connections for the TrackPoint connector and the T/P board. It shows the JP27 connector on the left, which is connected to the ACES_87151-0807G connector. The JP28 connector on the right is connected to the ACES_87151-04051_4P connector. The JP28 connector is also connected to the D39 connector, which is a UESD3.3DTS5 SOT-723. The diagram includes power supply connections for +5V and ground, and a 0.1U_0402_16V4Z capacitor. Signal lines for SP_CLK, SP_DATA, TP_CLK, and TP_DATA are shown.

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Change for S11 to prevent USB power short to GND cause system shutdown. 0130

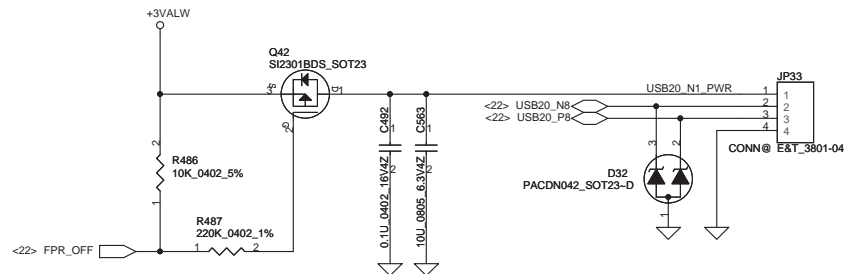
Change C486 from 2200pF to 680pF.
Change C321 from 1000pF to 1uF.
Change R356 from 10K to 100K.
Change C484 from 1000pF to 0.47uF.
Change R484 from 1K to 820.

Currently power USB will not enable after OCP, so add R629 make it enable after OCP free.

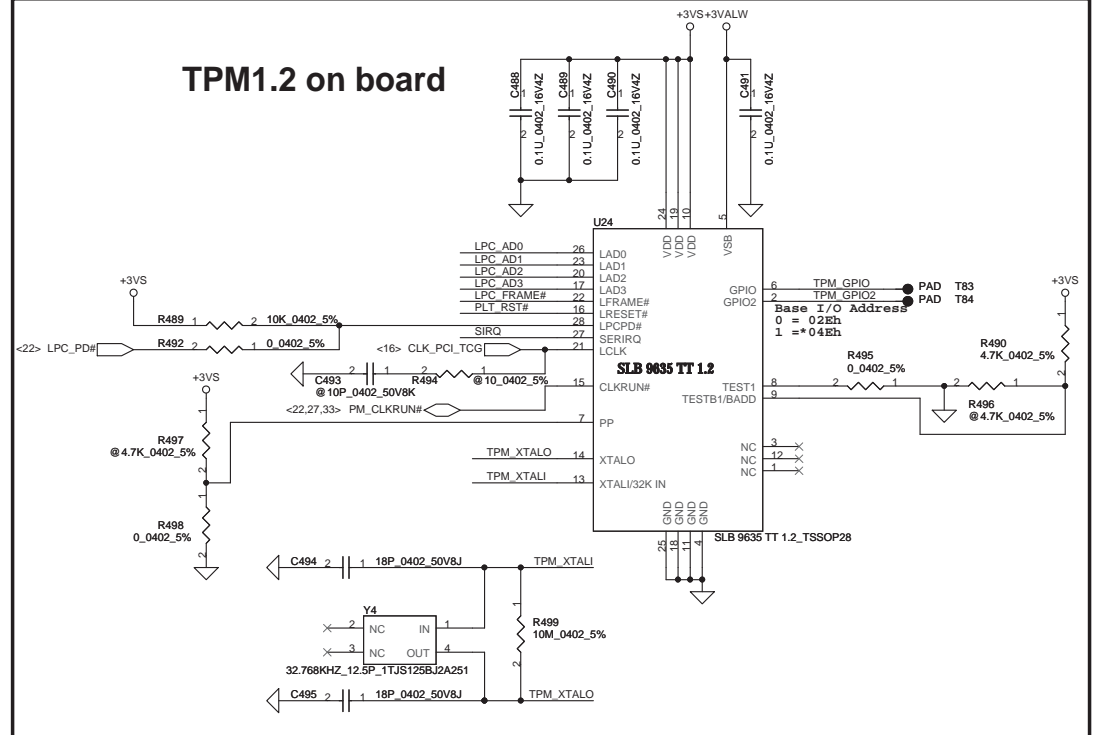
<http://hobi-elektronika.net>

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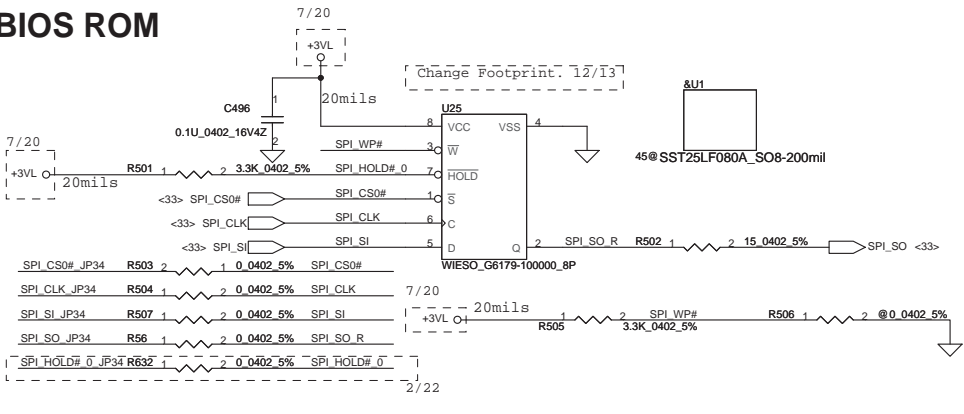
Finger printer



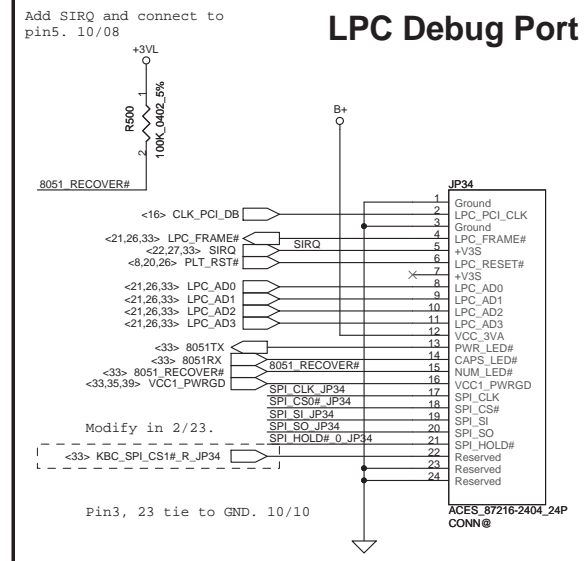
TPM1.2 on board



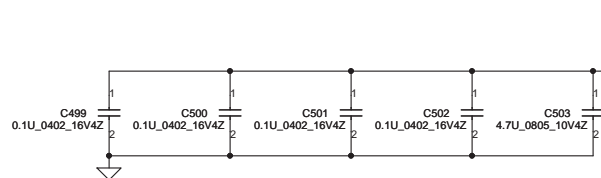
BIOS ROM



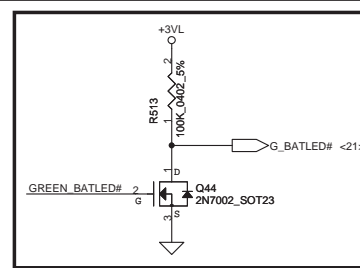
LPC Debug Port



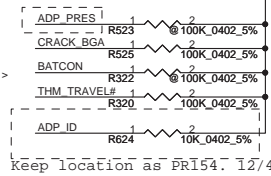
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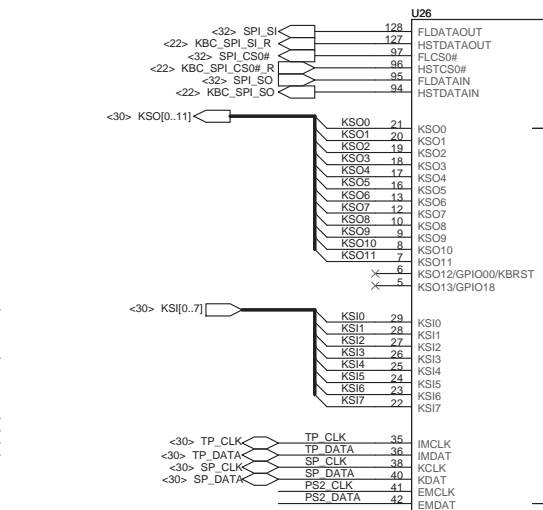
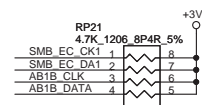
Del BATSEL_A# pin since only one battery. 10/18



Del D35 & @523 for power saving. 0130



Add in 12/3.



Keyboard/Mouse Interface

SMSC_1091-NU_TQFP-128P

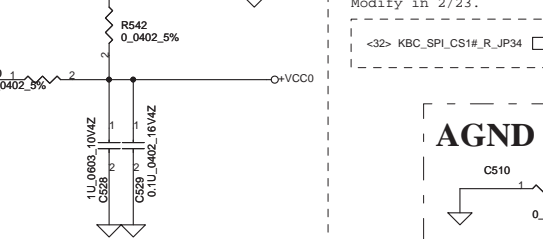
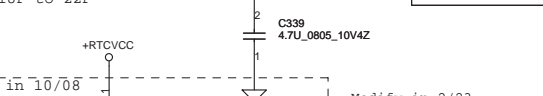
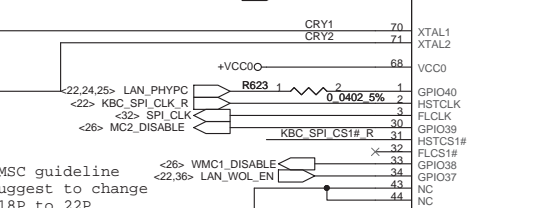
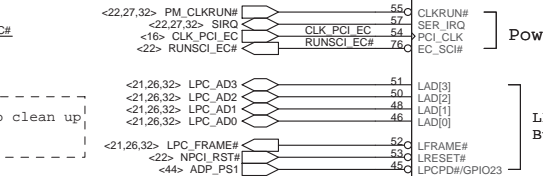
General Purpose I/O Interface

Access Bus Interface

Power Mgmt/SIRQ

LPC Bus

Miscellaneous

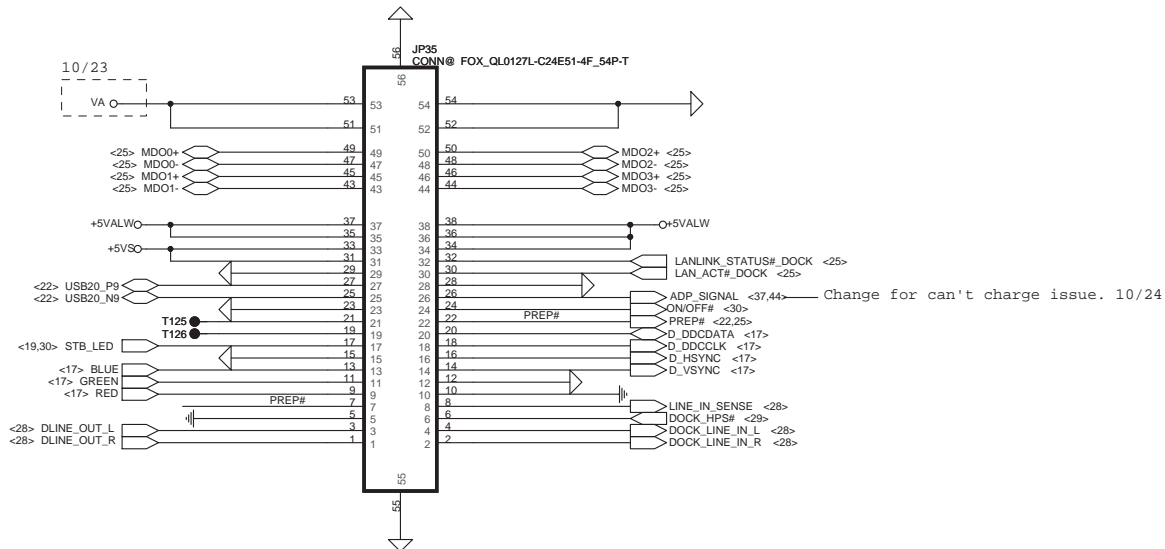
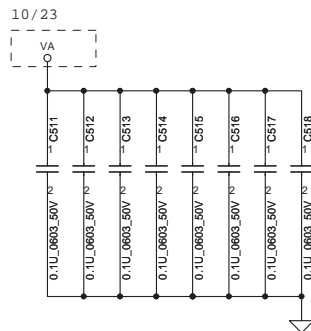


AGND FILTER

SMSC guideline suggest to change 0.1u to 0 ohm

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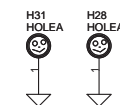
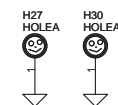
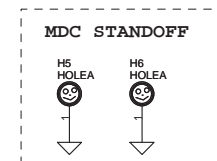
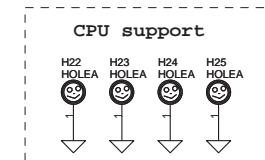
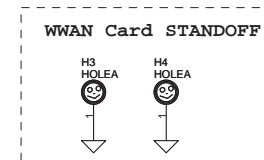
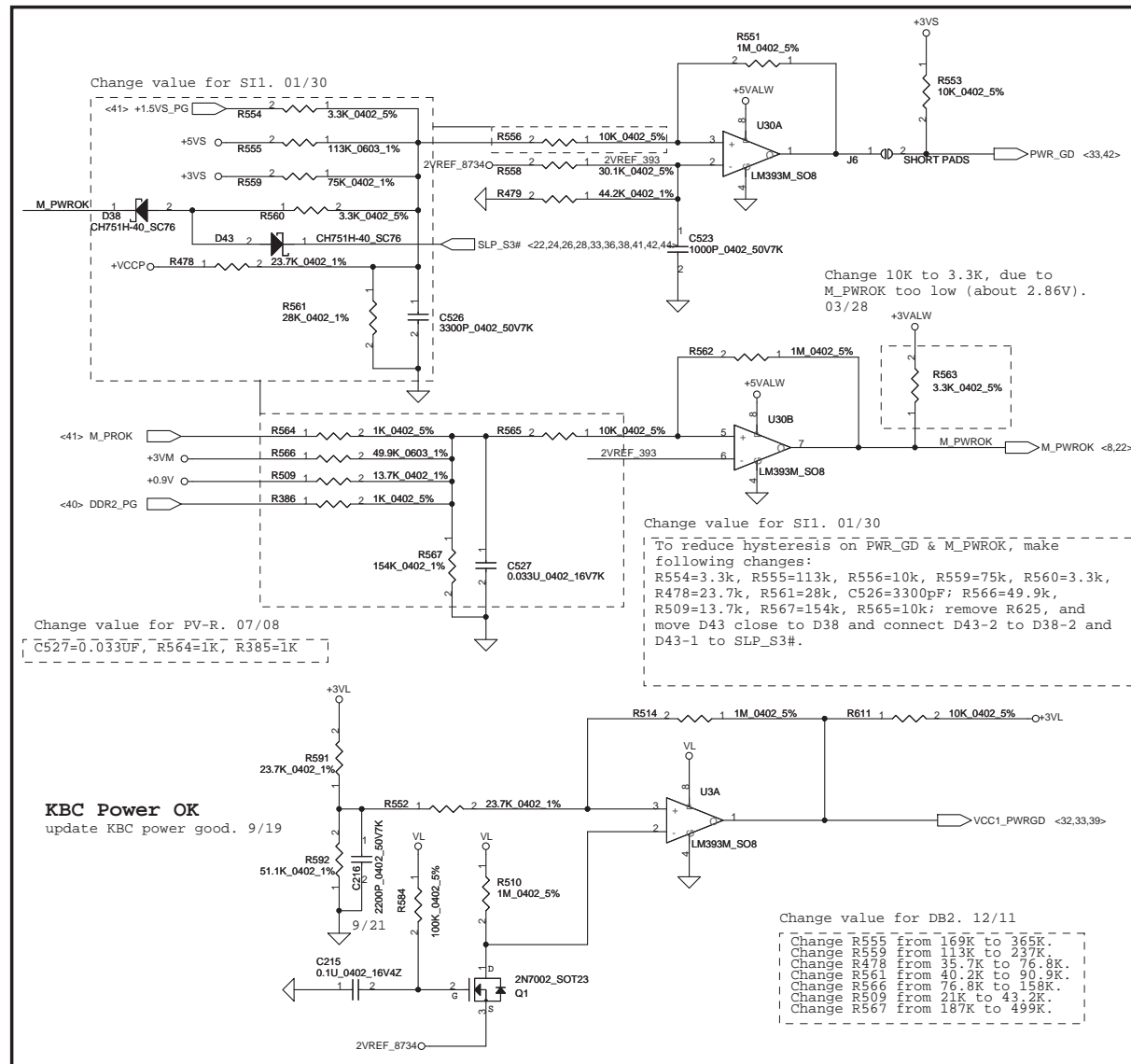
DOCKING CONNECT



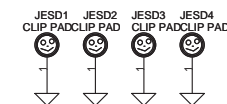
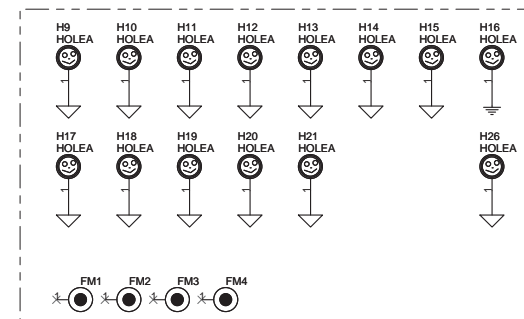
Delete:

1. L21 ~ L23
2. C605 ~ C610.
3. R635 ~ R637.
4. U27 ~ U29
5. C519 ~ C521.
6. R548 ~ R550.

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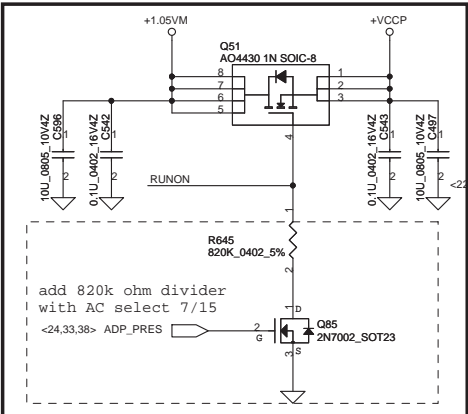
Del H1, H7 & H8. 1/18



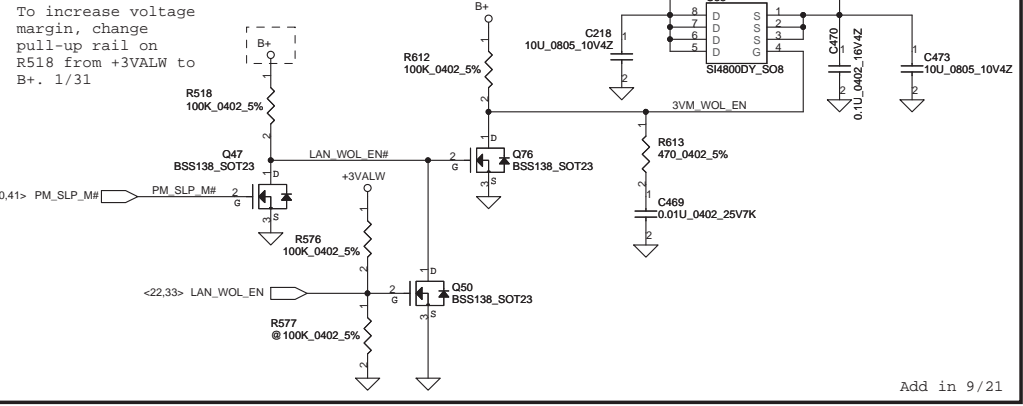
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Modify at 7/31 after discuss with power team.

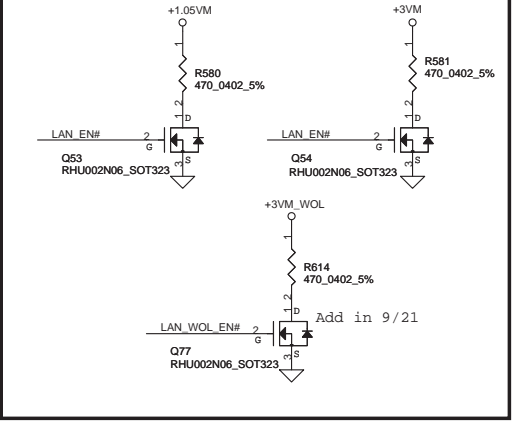
+1.05VM to +VCCP Transfer



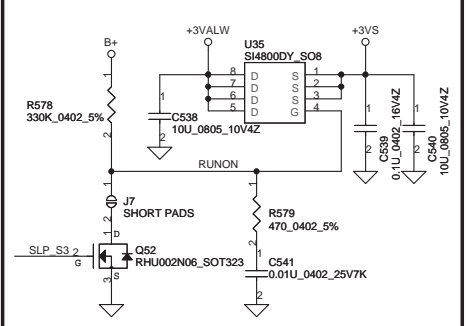
+3VALW to +3VM_WOL Transfer



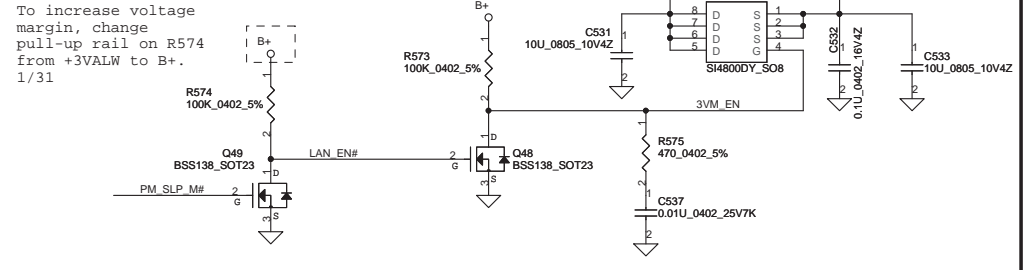
Discharge circuit-2 for V-M



+3VALW to +3VS Transfer

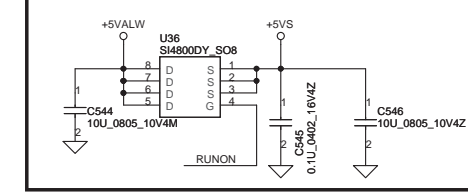


+3VALW to +3VM Transfer

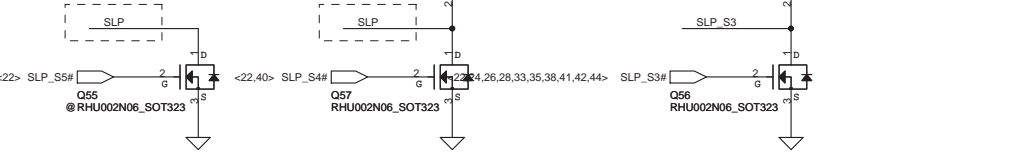


SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

+5VALW to +5VS Transfer



Design Change at 9/14.



Discharge circuit-1

