Mockingbird-N/V/L 14/15_CML & Hellcat14/15_CML UMA Schematic

2019/12/09

REV : SC

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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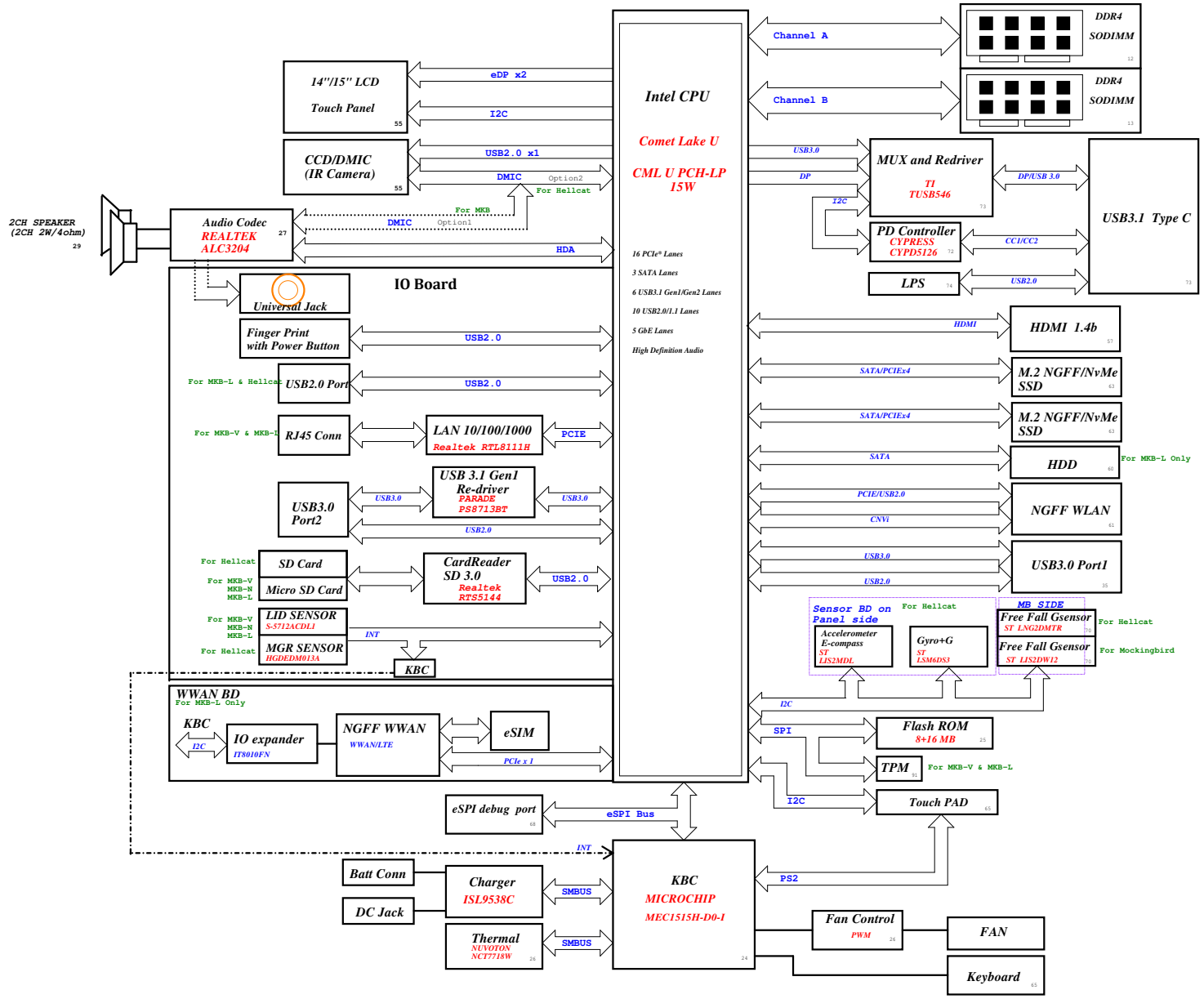
Title	Cover Page	
Size A4	Document Number Mockingbird_CML	Rev SC
Date: Monday, December 09, 2019	Sheet 1 of 105	

Mockingbird N/V/L/HellCat CML Block Diagram



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Title: Block Diagram

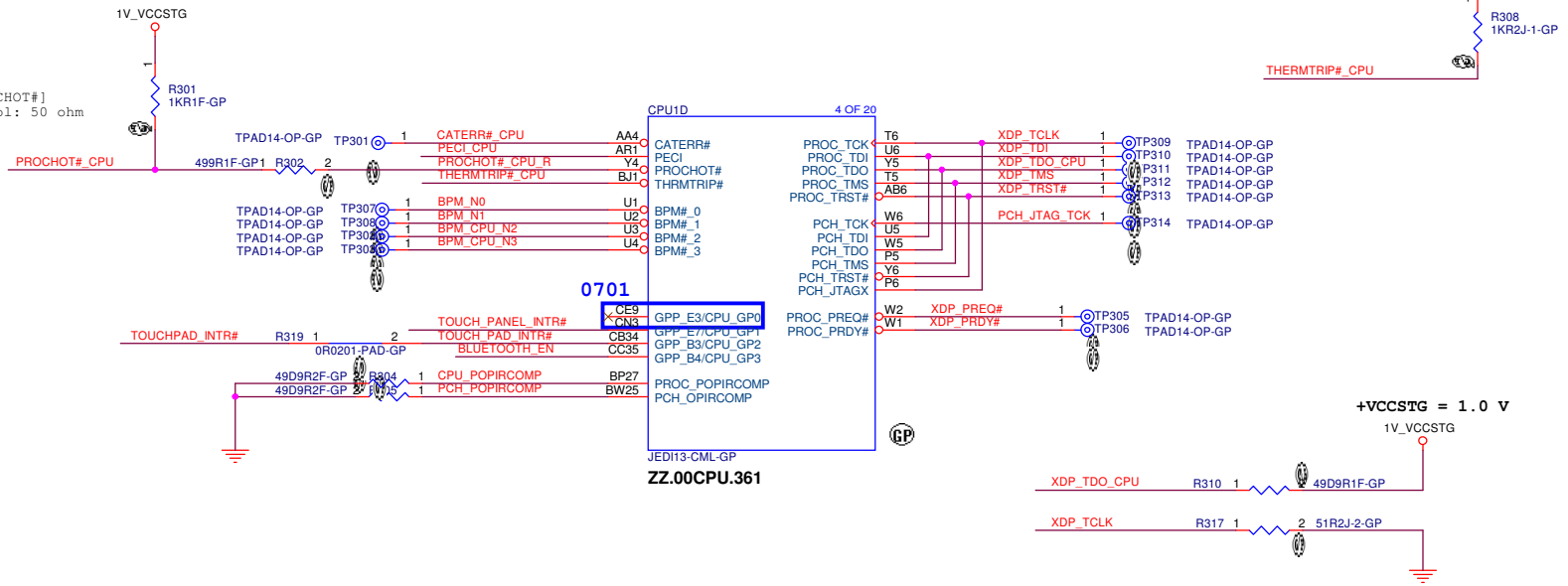
Size: Custom | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 2 of 105

SSID = CPU

24 PECI_CPU
24,44,46 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TOUCHPAD_INTR#
61 BLUETOOTH_EN

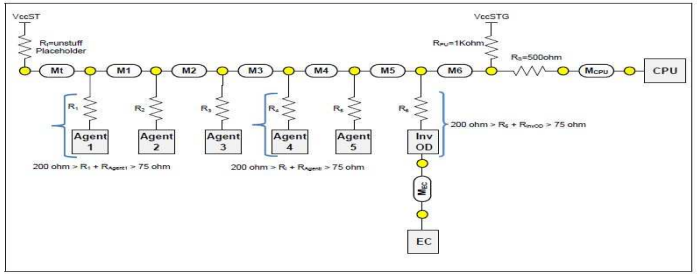
[PECI] and [PROCHOT#]
Impedance control: 50 ohm



ZZ.00CPU.361

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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Title: CPU (THML/JTAG)

Size	Document Number	Rev
A3	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 3 of 105

SSID = CPU

DP to HDMI2.0

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3

57 HDMI_HPD_CPU

57 HDMI_SCL_CPU
57 HDMI_SDA_CPU

DP for Type-C Mux

73 DP2_DDI_TX_N0
73 DP2_DDI_TX_P0
73 DP2_DDI_TX_N1
73 DP2_DDI_TX_P1
73 DP2_DDI_TX_N2
73 DP2_DDI_TX_P2
73 DP2_DDI_TX_N3
73 DP2_DDI_TX_P3

73 DP2_AUX_CPU_P
73 DP2_AUX_CPU_N

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU

72,73 DP1_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

55 IR_CAM_DET#

1.65GT Length 6.5" (3VIA)

DP to HDMI1.4b

DP for Type-C Mux

3D3V_S0
RN401
HDMI_SCL_CPU
HDMI_SDA_CPU
SRN2K2J-1-GP

3D3V_S0
SRN2K2J-1-GP
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK
RN403
10KR2J-3-GP
R407
IR_CAM_DET#
10KR2J-3-GP
R408
CAM_SHUTTER#

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

Helicat

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

CPU1A
1 OF 20

HDMI_DDI_TX_N2 AL5
HDMI_DDI_TX_P2 AL6
HDMI_DDI_TX_N1 AJ5
HDMI_DDI_TX_P1 AJ6
HDMI_DDI_TX_N0 AF6
HDMI_DDI_TX_P0 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6
DDI1_TXN_0
DDI1_TXP_0
DDI1_TXN_1
DDI1_TXP_1
DDI1_TXN_2
DDI1_TXP_2
DDI1_TXN_3
DDI1_TXP_3

DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2
DDI2_TXN_0
DDI2_TXP_0
DDI2_TXN_1
DDI2_TXP_1
DDI2_TXN_2
DDI2_TXP_2
DDI2_TXN_3
DDI2_TXP_3

EDP_TXN_0 AG4
EDP_TXP_0 AG3
EDP_TXN_1 AG2
EDP_TXP_1 AG1
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1
eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_TX_CPU_N1
eDP_TX_CPU_P1

Length 2"-10" (2VIA)
Cable Length 4"-15"

EDP_AUX_N AH4
EDP_AUX_P AH3
eDP_AUX_CPU_N
eDP_AUX_CPU_P

Length 10" (3VIA)

DISP_UTILS AM7

DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4
DDI2_AUX_P AD3
DDI3_AUX_N AG7
DDI3_AUX_P AG6
DP2_AUX_CPU_N
DP2_AUX_CPU_P

TYPE-C MUX

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7
HDMI_HPD_CPU
DP1_HPD_CPU_R
SIO_EXT_SMI#
PI_CAM_DET#
eDP_HPD_CPU

EDP_BKLTEN CK11
EDP_VDDEN CG11
EDP_BKLTCTL CH11
L_BKLT_EN
EDP_VDD_EN
L_BKLT_CTRL

1V_VCCIO
R401
24D9R2F-L-GP
eDP_RCOMP_CPU AM6
DISP_RCOMP

HDMI_SCL_CPU CC8
HDMI_SDA_CPU CC9
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA

CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

TPAD14-OP-GP TP402
CAM_SHUTTER# CP4
GPP_E23 CN4
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA

GPP_H17_STRAP CR26 CP26
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA

JEDI13-CML-GP

ZZ.00CPU.361

3D3V_S0
SIO_EXT_SMI# R402 10KR2J-3-GP

Add RTC Gen 9 reset circuit_20170814 leakage issue

3D3V_S5_PCH
R406 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R405 10KR2J-3-GP
RTC_RST
Q401
DP1_HPD_CPU_R
DP1_HPD_CPU
CPU_DP_HPD_P
RTC_RST
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

RTC Gen 9 reset circuit_20170814

DP1_HPD_CPU_R
R403 100KR2J-1-GP

DP for Type-C Mux

<Core Design>

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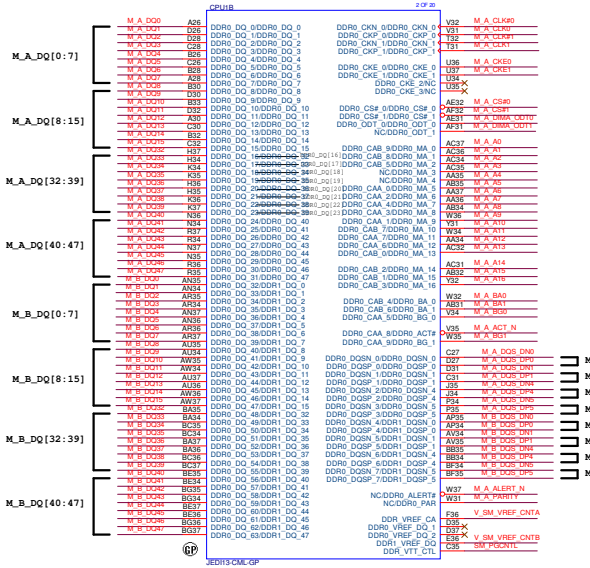
Title: CPU (DDI/EDP/TBT/TPC/)

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

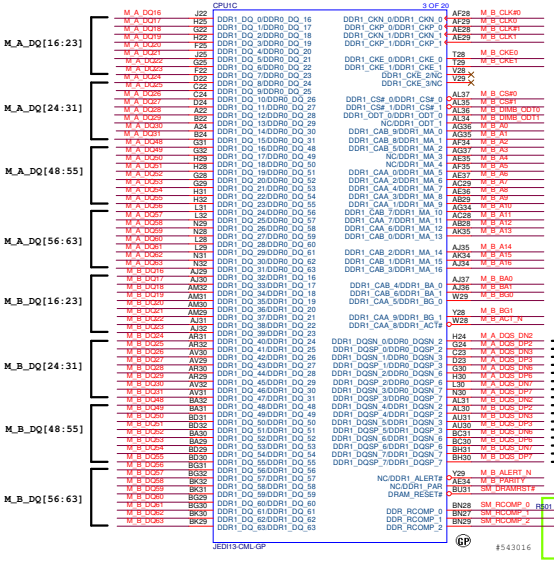
Date: Monday, December 09, 2019 | Sheet 4 of 105

SSID = CPU

DDR4 ball type: Non Interleaved Type



ZZ.00CPU.361



#543016

Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

SC-20191202

0614 Layout HT

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

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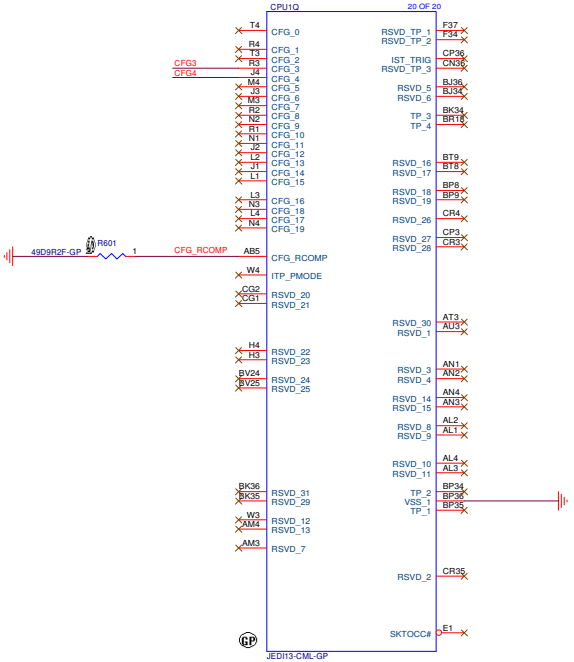
Title: CPU (DDR)
Size: Custom | Document Number: Mockingbird_CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 5 of 105

SSID = CPU

15 CFG3
15 CFG4



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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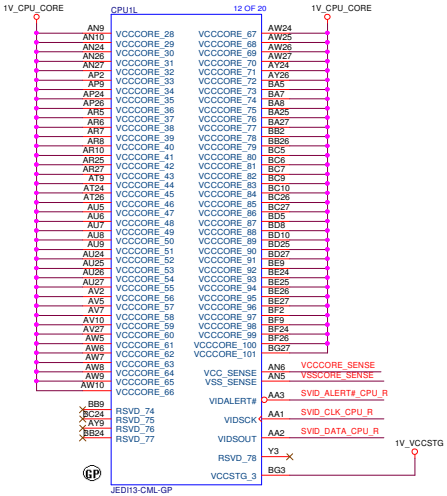
Title: CPU (CFG/IST)
Size: A2 | Document Number: Mockingbird_CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 6 of 105

SSID = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

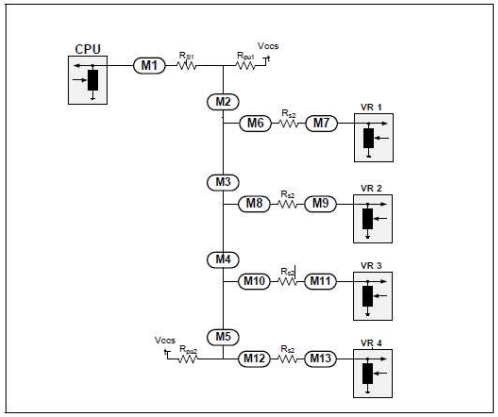


Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

Topology Guidelines	
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

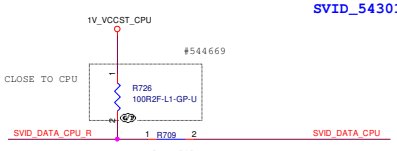
. Routing Illustration for SVID Topology



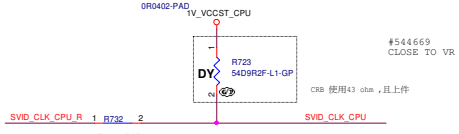
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

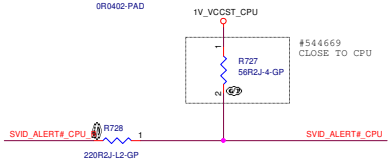
SVID DATA

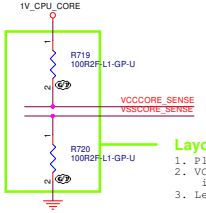


SVID CLOCK



SVID ALERT





Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title: CPU (VCCIN/VID)

Size	Document Number	Rev
A2	Mockingbird_CML	SC

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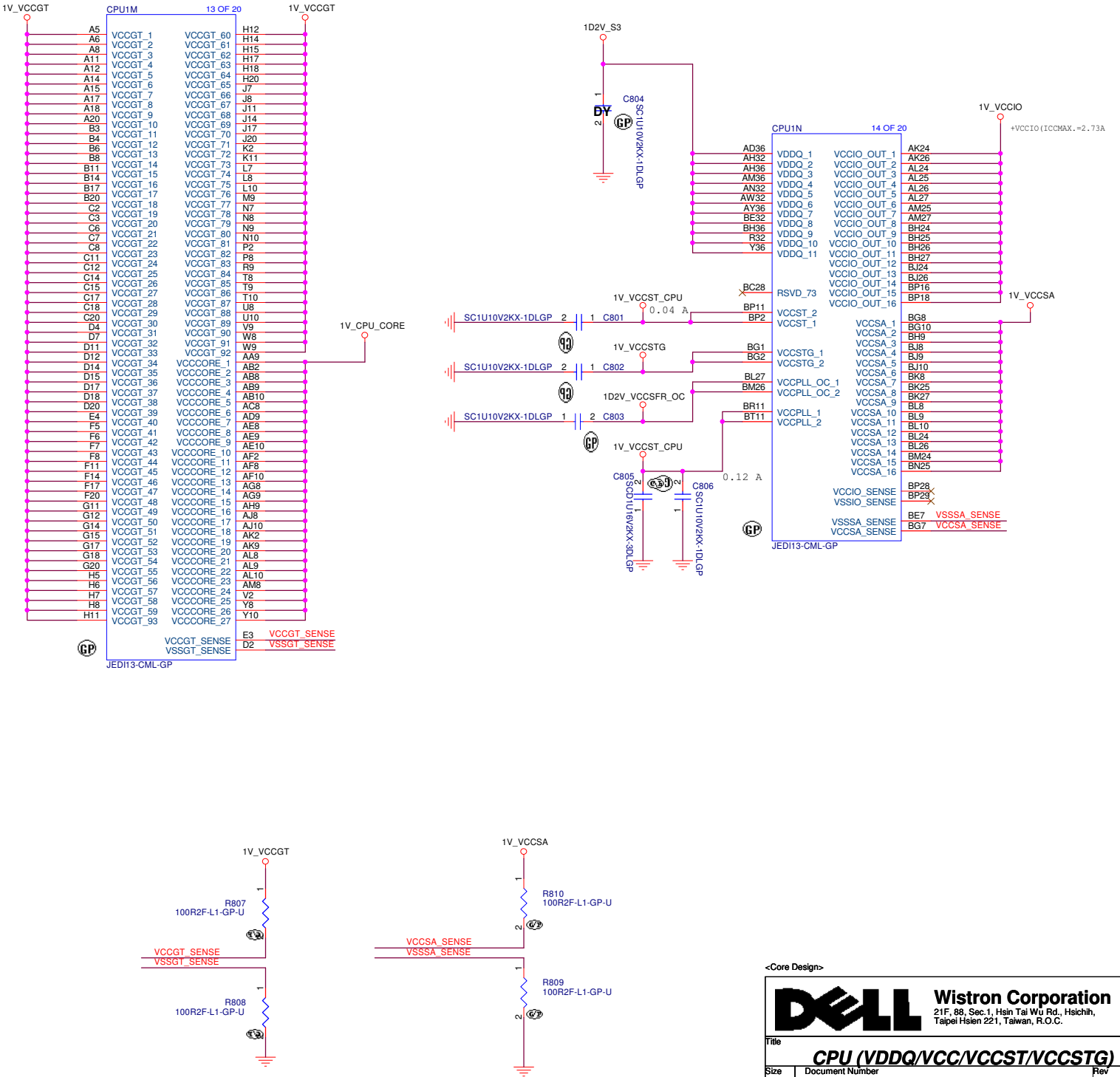
SSID = CPU

46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE



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Title: CPU (VDDQ/VCC/VCCST/VCCSTG)

Size: A3 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 8 of 105

(Blanking)

<Core Design>

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Title: CPU (RSVD)

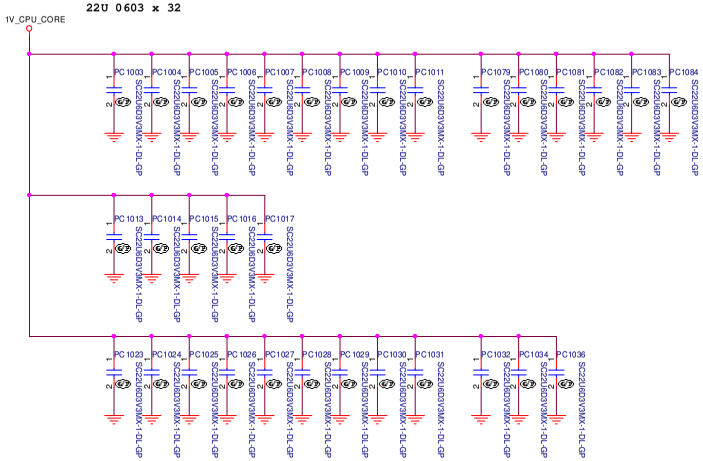
Size: A3 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 9 of 105

SSID = CPU

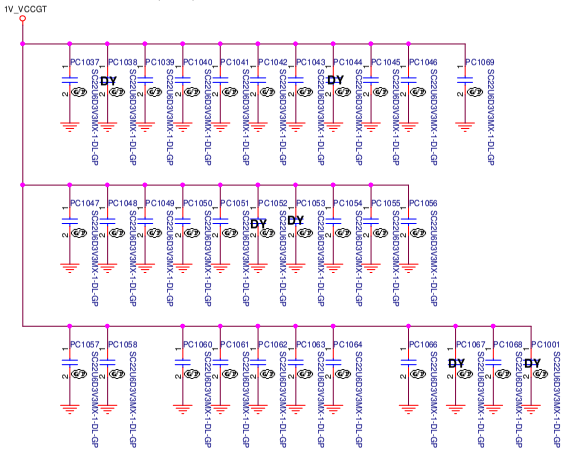
1V_CPU_CORE

22U 0603 x 32



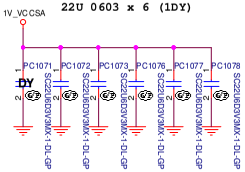
VCCGT

22U 0603 x 32 (6 DY)



VCCSA

22U 0603 x 6 (1DY)



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
V_{CCCORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
V_{CCGT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{CCCORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{CCGT}	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
V_{CCSA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
V_{CCIO}	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
V_{CCPLL_OC}	1x 1uF 0402		Do not merge V_{CCPLL}, V_{CCPLL_OC} and V_{CCST} to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
V_{CCPLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
V_{CCST}	1x 1uF 0402		
V_{CCSTG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(CORE Power Cap1)

Size	Document Number	Rev
A2	Mockingbird_CML	SC

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SSID = CPU

PCH DERIVED RAILS

1D05V_S5

C1112 SC10U6D3V3MX-DL-GP

3D3V_S5_PCH — R1103 — 3D3V_VCCPRIM

0R0603-PAD

1D8V_S5 — R1104 — 1D8V_VCCPRIM

0R0603-PAD

1V_VCCIO

+VCCIO(ICCMAX.=2.73A)

C1133 C1134 SC10U6D3V3MX-DL-GP

1D05V_S5

C1128 C1129 SC10U6D3V3MX-DL-GP

U-line 23e 28W
IccMax current-10ms max = 34 A

UNSLICED GT

1V_VCCGT

C1102 C1103 C1104 C1105 C1106 C1107 DY SC1U10W2KX-1DLGP

VCCIO

1V_VCCIO

+VCCIO(ICCMAX.=2.73A)

C1108 C1109 C1110 C1111 DY SC1U10W2KX-1DLGP

+VCCMPHYGTAON_1P0(ICCMAX.=2.12A)

1D05V_S5

C1114 SC1U10V2KX-1DLGP

1D05V_S5

C1116 C1117 SC1U10V2KX-1DLGP

1D05V_S5

C1118 SC10U6D3V3MX-DL-GP C1119 SC1U10V2KX-1DLGP

1D05V_S5

C1121 SC1U10V2KX-1DLGP

1D2V_S3

C1136 C1137 C1138 SC10U6D3V3MX-DL-GP C1139 C1140 C1141 C1142 SCD1U16V2KX-3DLGP

C1131 DY SC22U6D3V3MX-1DL-GP C1130 SC10U6D3V3MX-DL-GP

FC1102 DY SC22U6D3V2MX-DL-GP

FC1103 DY SC22U6D3V2MX-DL-GP

Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

<Core Design>

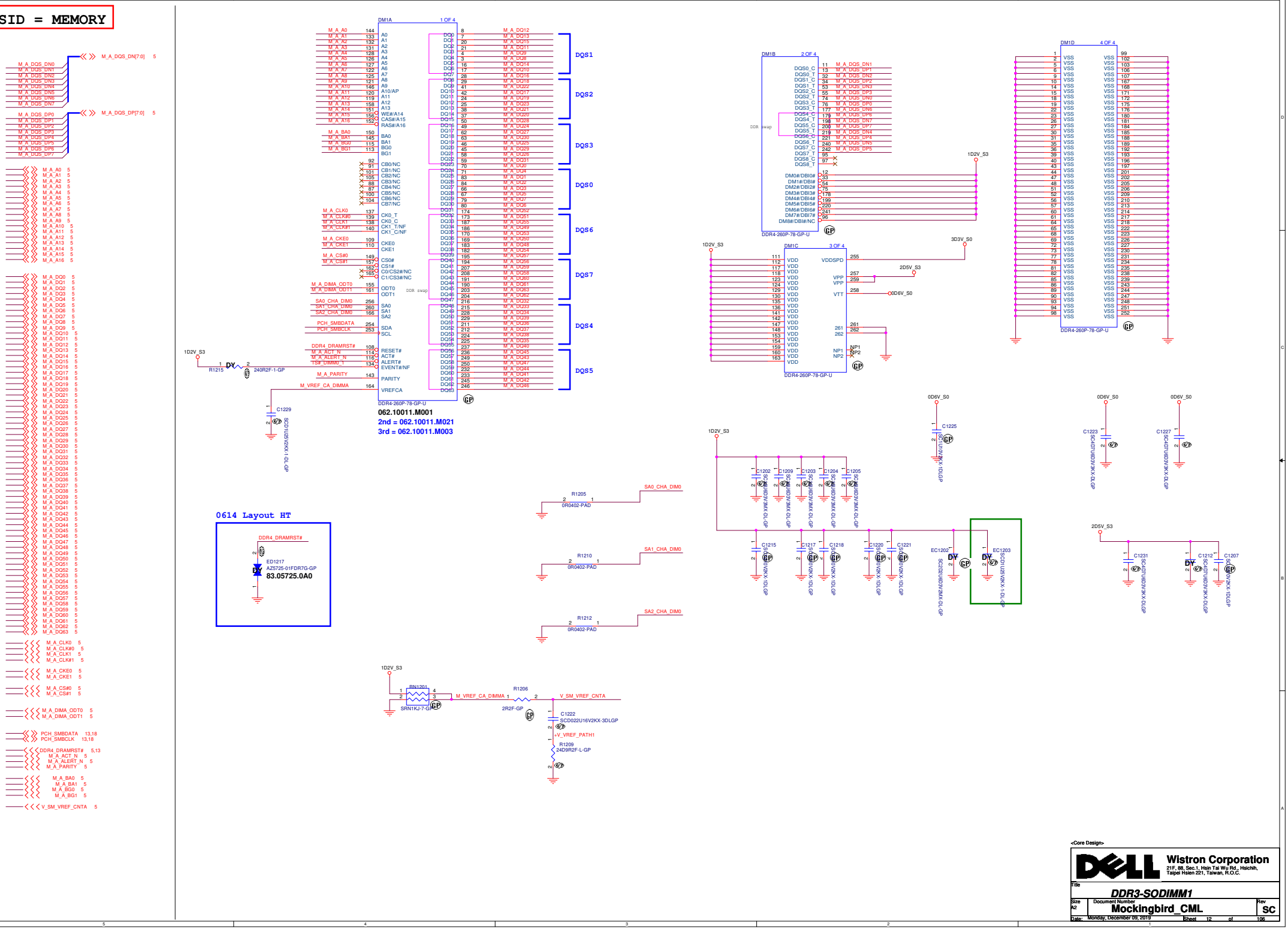
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)

Size: A3 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 11 of 105

SSID = MEMORY



<Core Design>

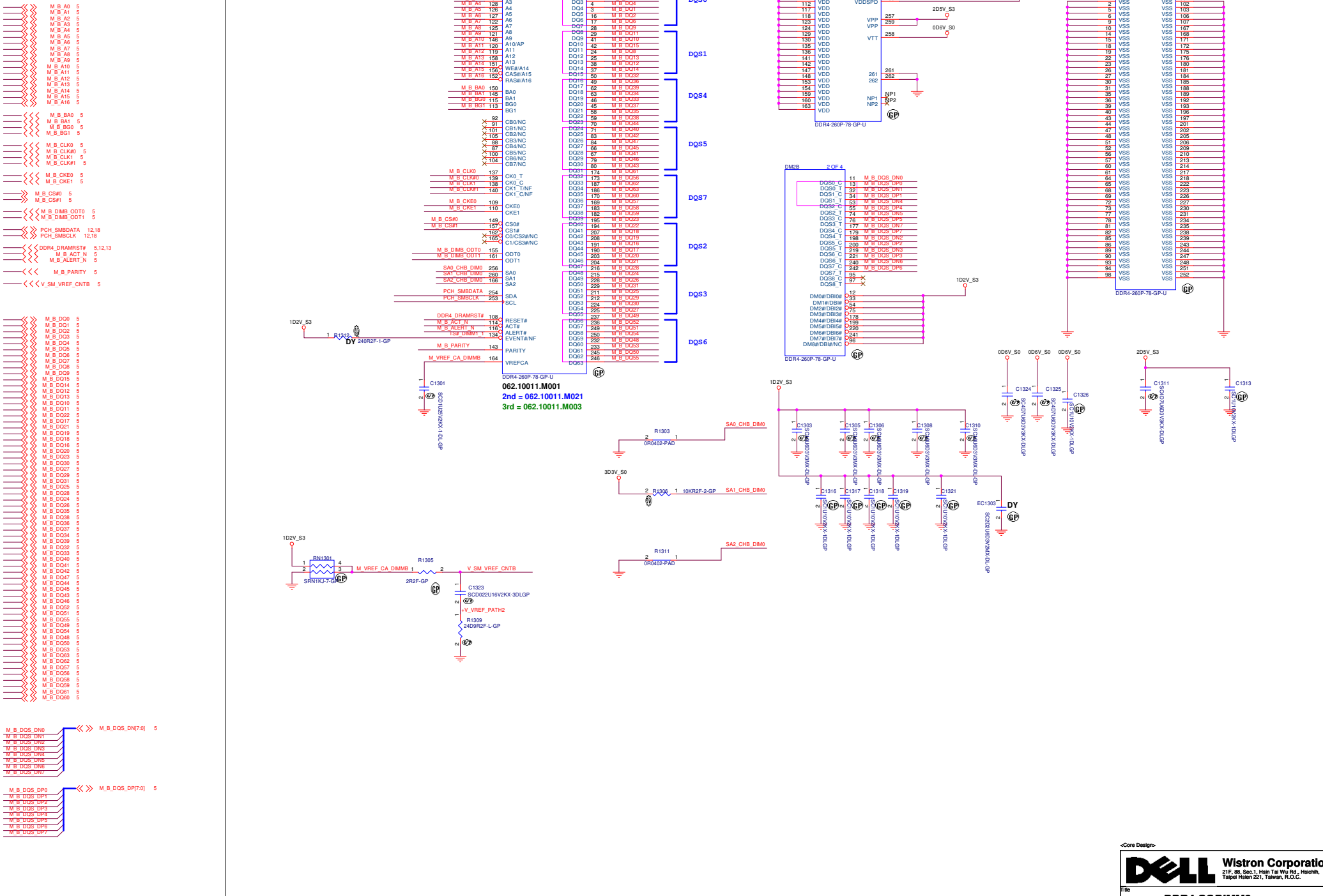
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 12 of 106

SSID = MEMORY



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR4-SODIMM2*

Size	Document Number	Rev
A2	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 13 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

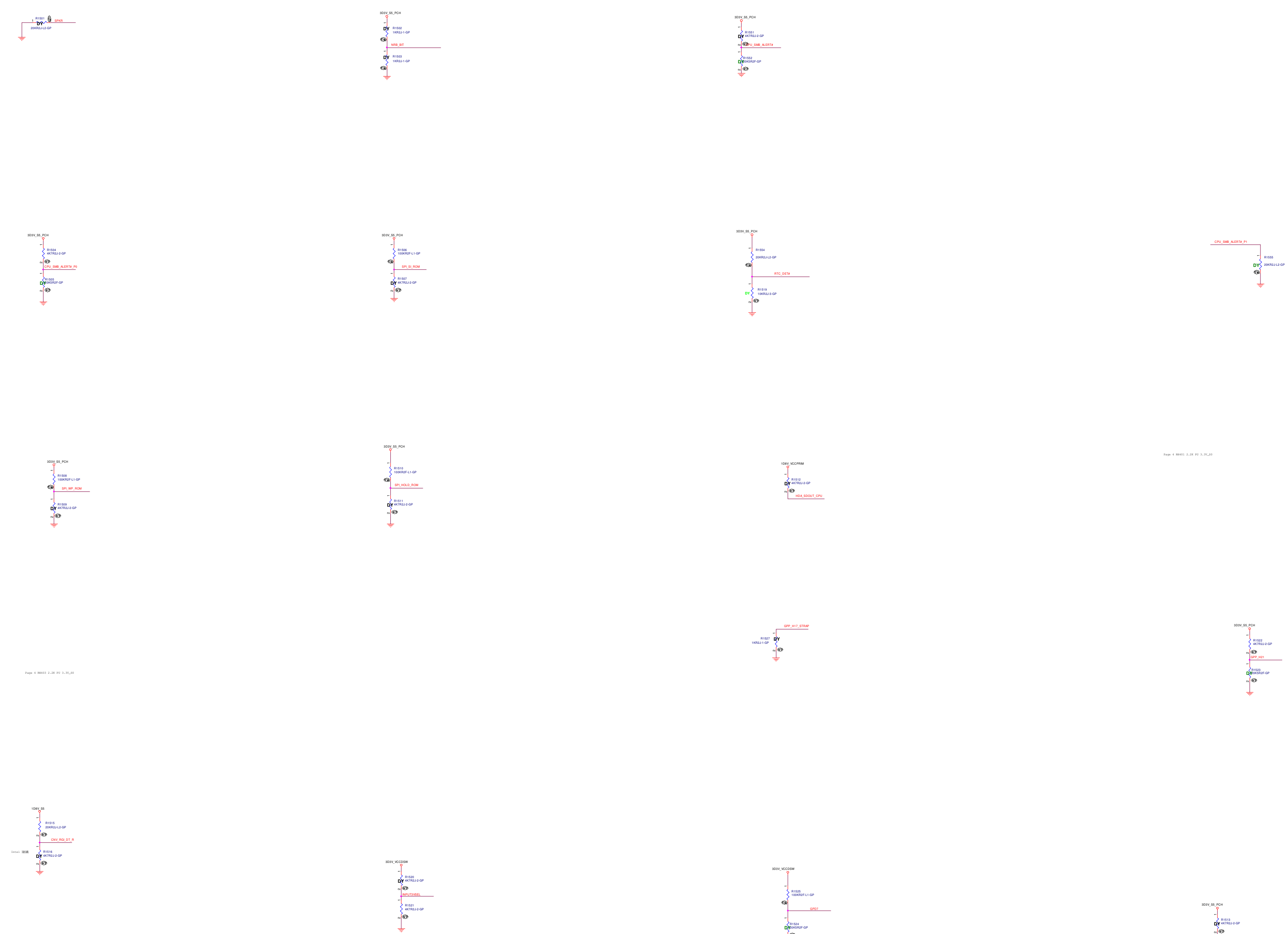
Title
DDR (RSVD) (DDR4-CHA1)

Size	Document Number	Rev
A4	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 14 of 105

SSID = CPU

19,27 SPKR
18,24,25,91 SPI_SI_ROM
18 CPU_SMB_ALERT#
18 CPU_SMB_ALERT#_P0
18,24,25 SPI_WP_ROM
18,24,25 SPI_HOLD_ROM
20 NRB_BIT
6 CFG4
6 CFG3
20,61 CNV_RGI_DT_R
19 HDA_SDOUT_CPU
21 GPP_H23
17 INPUT3VSEL
18 CPU_SMB_ALERT#_P1
21 GPP_H21
21 GPD7
20,25 RTC_DET#
4 GPP_H17_STRAP



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

PCH strap pin:

CFG3 — R1517 1KR2J-1-GP DY

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

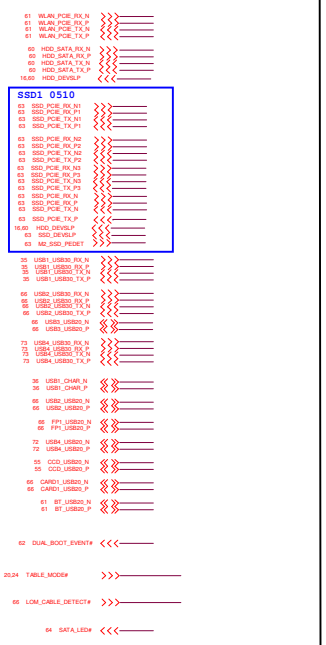
CFG4 — R1518 1KR2J-1-GP

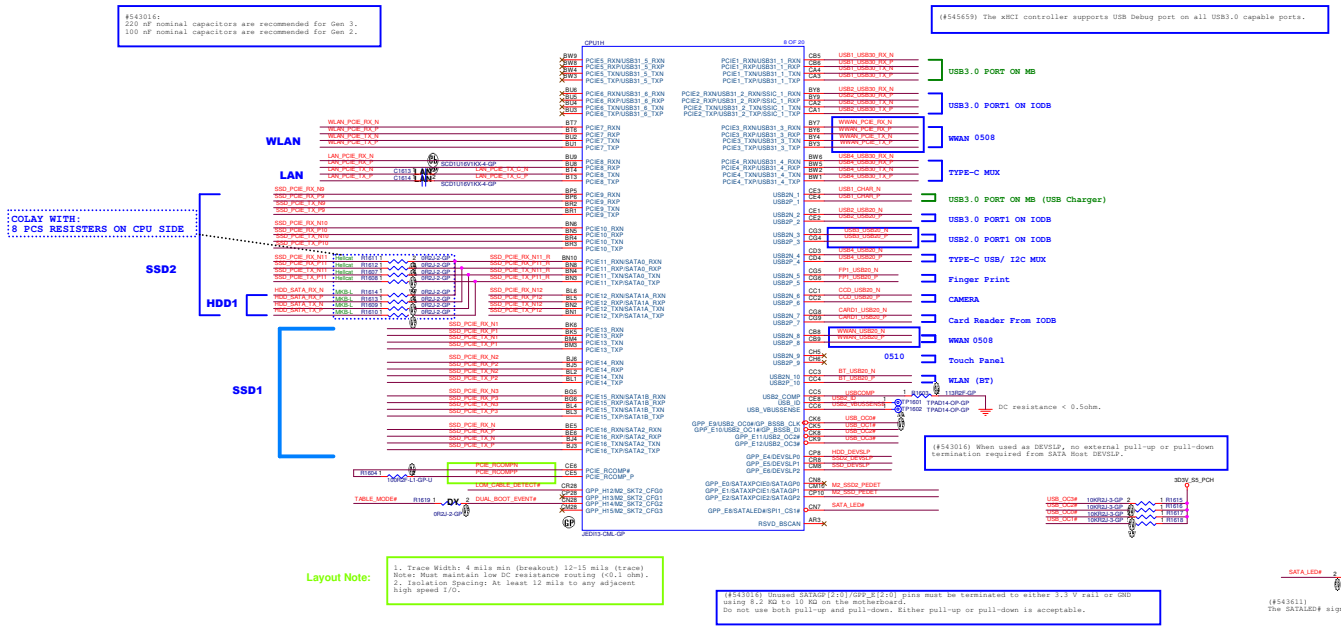
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (STRAP)	
Size A0	Document Number Mockingbird_CML	Rev SC
Date: Monday, December 09, 2019	Sheet 15 of 105	

SSID = CPU





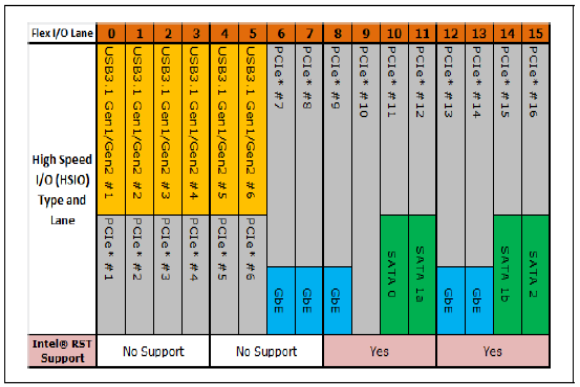


Table 1-3. PCH HSIO Detail

SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/ Base-U	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	PCIe*	PCIe*	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	SATA 0/ PCIe*	SATA 1A/ PCIe*	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*	PCIe*
Premium-U	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*/ SATA 1B	PCIe*/ SATA 2
Premium-Y	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	Not Available	Not Available

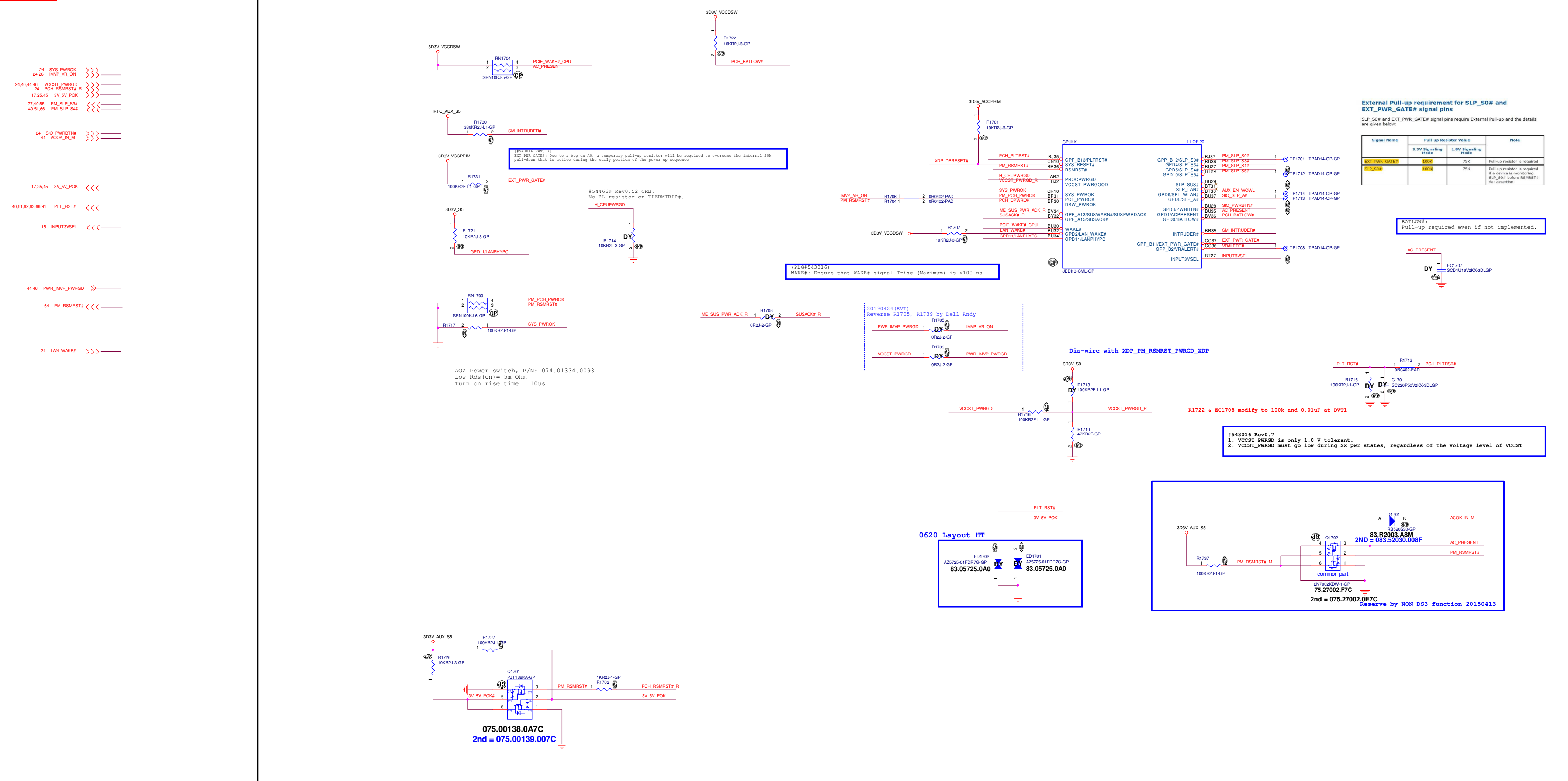
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP6	RP7	RP5		RP12	RP11	RP9		RP15	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

	ROCKY	Rogue
USB_OC0#	TYPEC PD	NC
USB_OC1#	Power share	USB3.0 Power
USB_OC2#	USB3.0 Power	NC
USB_OC3#	USB2.0 Power	TYPEC PD

SSID = CPU



24 SYS_PWROK
24,26 IMVP_VR_ON
24,40,44,46 VCCST_PWRGD
24 PCH_RSMRST#_R
17,25,45 3V_5V_POK
27,40,55 PM_SLP_S3#
40,51,66 PM_SLP_S4#
24 SIO_PWRBTN#
44 ACOK_IN_M
17,25,45 3V_5V_POK
40,61,62,63,66,91 PLT_RST#
15 INPUT3VSEL
44,46 PWR_IMVP_PWRGD
64 PM_RSMRST#
24 LAN_WAKE#
3D3V_VCCDSW
RN1704
SRN10KJ-5-GP
PCIE_WAKE#_CPU
AC_PRESENT
R1722
10KR2J-3-GP
PCH_BATLOW#
RTC_AUX_S5
R1730
330KR2J-L1-GP
SM_INTRUDER#
3D3V_VCCPRIM
R1731
100KR2F-L1-GP
EXT_PWR_GATE#
#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.
H_CPUPWRGD
R1714
10KR2J-3-GP
3D3V_S5
R1721
10KR2J-3-GP
GPD11/LANPHYPC
RN1703
SRN100KJ-6-GP
PM_PCH_PWROK
PM_RSMRST#
R1717
100KR2J-1-GP
SYS_PWROK
AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us
R1701
10KR2J-3-GP
XDP_DBRESET#
IMVP_VR_ON
PM_RSMRST#
R1706
R1704
0R0402-PAD
R1707
10KR2J-3-GP
ME_SUS_PWR_ACK_R
R1708
0R2J-2-GP
SUSACK#_R
(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.
20190424(EVT)
Reverse R1705, R1739 by Dell Andy
R1705
PWR_IMVP_PWRGD
IMVP_VR_ON
R1739
VCCST_PWRGD
PWR_IMVP_PWRGD
CPU1K
11 OF 20
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SPL_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL
JEDI13-CML-GP
TP1701 TPAD14-OP-GP
TP1712 TPAD14-OP-GP
TP1714 TPAD14-OP-GP
TP1713 TPAD14-OP-GP
TP1708 TPAD14-OP-GP
AUX_EN_WOWL
VRALERT#
Dis-wire with XDP_PM_RSMRST_PWRGD_XDP
3D3V_S0
R1718
100KR2F-L1-GP
R1716
100KR2F-L1-GP
VCCST_PWRGD_R
R1719
47KR2F-GP
R1722 & EC1708 modify to 100k and 0.01uF at DVT1
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
AC_PRESENT
EC1707
SCD1U16V2KX-3DLGP
PLT_RST#
R1713
0R0402-PAD
PCH_PLTRST#
R1715
100KR2J-1-GP
C1701
SC220P50V2KX-3DLGP
0620 Layout HT
PLT_RST#
3V_5V_POK
ED1702
AZ5725-01FDR7G-GP
83.05725.0A0
ED1701
AZ5725-01FDR7G-GP
83.05725.0A0
3D3V_AUX_S5
D1701
RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
ACOK_IN_M
AC_PRESENT
PM_RSMRST#
R1737
100KR2J-1-GP
PM_RSMRST#_M
Q1702
common part
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
Reserve by NON DS3 function 20150413
3D3V_AUX_S5
R1727
100KR2J-1-GP
R1726
10KR2J-3-GP
Q1701
PJT138KA-GP
PM_RSMRST#
1KR2J-1-GP
R1702
PCH_RSMRST#_R
3V_5V_POK#
3V_5V_POK
075.00138.0A7C
2nd = 075.00139.007C

External Pull-up requirement for SLP_S0# and EXT_PWR_GATE# signal pins

SLP_S0# and EXT_PWR_GATE# signal pins require External Pull-up and the details are given below:

Signal Name	Pull-up Resister Value		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
EXT_PWR_GATE#	100K	75K	Pull-up resistor is required
SLP_S0#	100K	75K	Pull-up resistor is required if a device is monitoring SLP_S0# before RSMRST# de- assertion

BATLOW#:
Pull-up required even if not implemented.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH_(PMU)	
Size A1	Document Number Mockingbird_CML	Rev SC
Date: Monday, December 09, 2019	Sheet 17 of 105	

SSID = CPU

WWAN 0508

0510

For eSPI

WLAN

SSD2 SATA

SSD1

WWAN 0508

2nd = 075.27002.0E7C

2nd = 082.30003.0591

2nd = 082.30006.0571

FC1801 close to EC1803

Layout: Place at the open door area.

<Core Design>

Wistron Corporation

CPU (SPI/ESPI/SMBS/XTAL/CLK)

Mockingbird_CML

SSID = CPU

15,27 SPKR
27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
98 ME_FWP_SW
27 HDA_SDOUT_CODEC
65 KB_LED_BL_DET

15 HDA_SDOUT_CPU

55 DMIC_PCH_CLK
55 DMIC_PCH_DATA

61 BT_PCMFRM_CRF_RST_N
61 BT_PCMOUT_CLKREQ0

62 WWAN_GPIO_PERST#

55 TOUCH_PANEL_DET#

CPU1G 7 OF 20

HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST_N_CPU 1 BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
KB_LED_BL_DET CK23 GPP_D23/I2S_MCLK
BL37 I2S1_SFRM/SNDW2_CLK
BL34 I2S1_TXD/SNDW2_DATA

GPP_G0/SD_CMD CH36 WWAN_GPIO_PERST#
GPP_G1/SD_DATA0 CL35
GPP_G2/SD_DATA1 CM36
GPP_G3/SD_DATA2 CN35
GPP_G4/SD_DATA3 CH35
GPP_G5/SD_CD# CK36
GPP_G6/SD_CLK CK34
GPP_G7/SD_WP

TPAD14-OP-GP TP1903

BT_PCMFRM_CRF_RST_N 1 R1924 33R2J-2-GP BT_PCMFRM_CRF_RST_N_R CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
BT_PCMOUT_CLKREQ0 1 R1923 33R2J-2-GP BT_PCMOUT_CLKREQ0_R CH29 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
TOUCH_PANEL_DET# CH30 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
DMIC_PCH_CLK CP24 GPP_D19/DMIC_CLK0/SNDW4_CLK
DMIC_PCH_DATA CN24 GPP_D20/DMIC_DATA0/SNDW4_DATA
TPM_ID CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA
SPKR CF35 GPP_B14/SPKR

GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7 BW36
GPP_A16/SD_1P8_SEL BY37
SD_1P8_RCOMP CK33
SD_3P3_RCOMP CM34

SD_RCOMP R1901 1 2.200R2F-L-GP

JEDI13-CML-GP

Bucky DMIC I2C from Codec IC

3D3V_S5 R1925 10KR2J-3-GP TOUCH_PANEL_DET#

3D3V_S5 R1910 10KR2J-3-GP fwTPM TPM_ID
R1911 10KR2J-3-GP TPM

EC1901 1 DY 2 HDA_BITCLK_CODEC
SC10P50V2JN-4DLGP

HDA_SYNC_CODEC R1908 1 2 0R0402-PAD HDA_SYNC_CPU

R1920~R1921 need to close for merge prepare

HDA_BITCLK_CODEC R1920 1 0R0402-PAD HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 33R2J-2-GP HDA_SDOUT_CPU

ME_FWP_SW R1909 1 1KR2J-1-GP

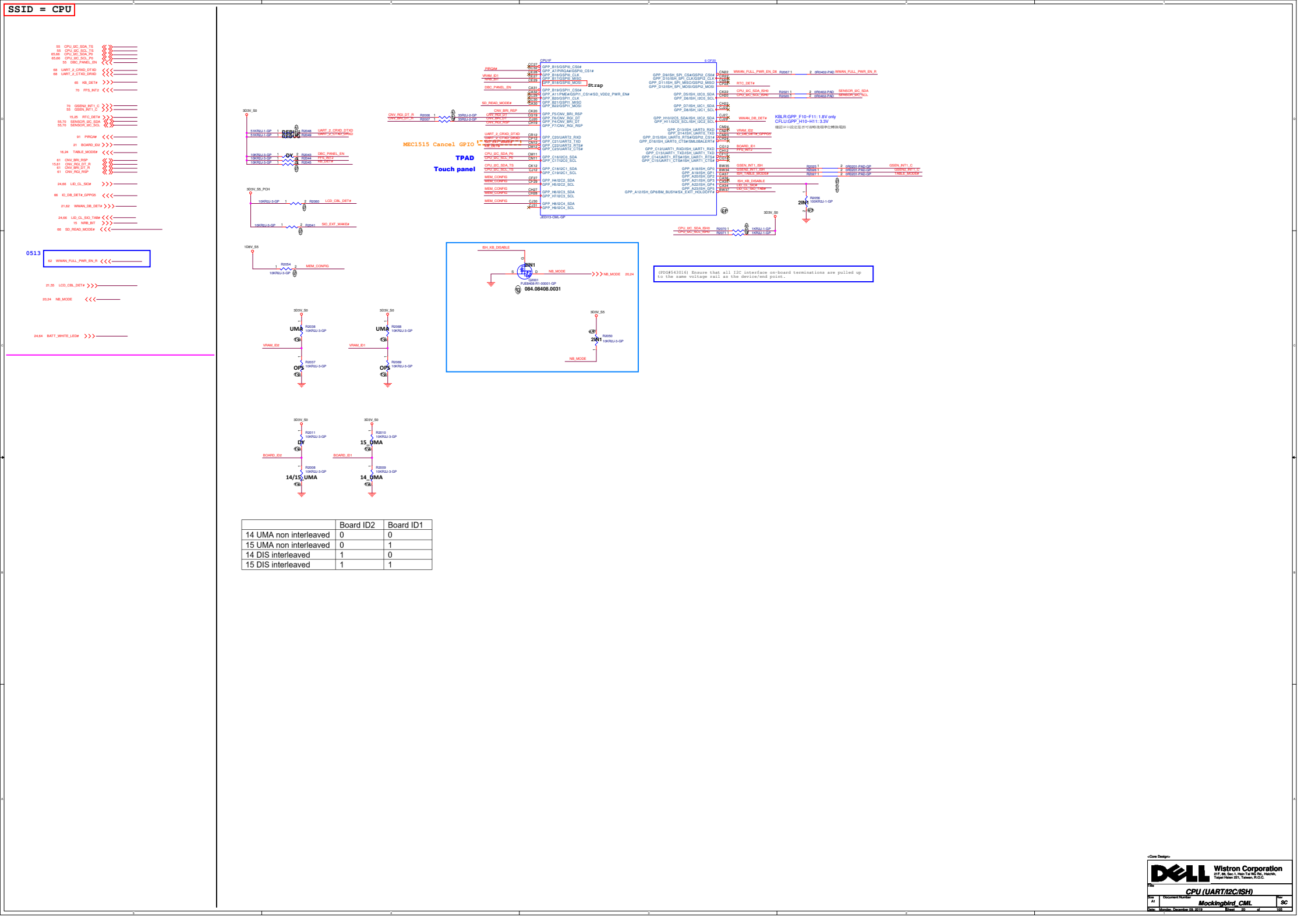
HDA_SDOUT_CODEC
EC1903 1 DY 2
SC33P50V2JN-3DLGP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2 | Document Number: Mockingbird_CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 19 of 105

SSID = CPU



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

	Board ID2	Board ID1
14 UMA non interleaved	0	0
15 UMA non interleaved	0	1
14 DIS interleaved	1	0
15 DIS interleaved	1	1

<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: A1 | Document Number: Mockingbird_CML | Rev: SC

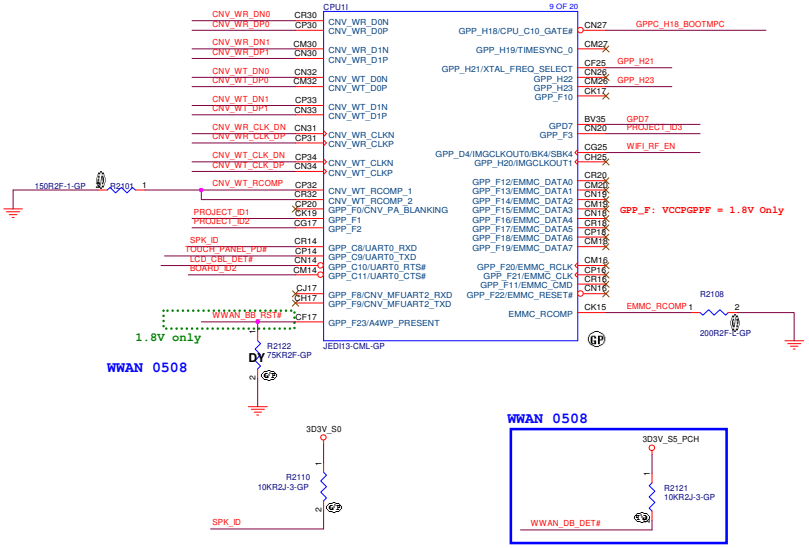
Date: Monday, December 09, 2019 | Sheet 20 of 155

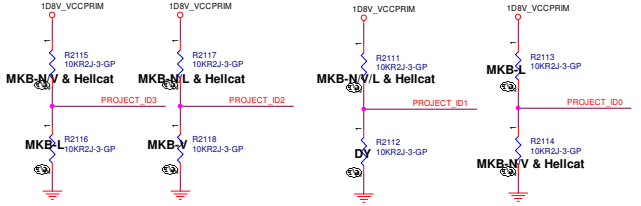
SSID = CPU

40 GPPC_H18_BOOTMPC
61 WIFI_RF_EN
55 TOUCH_PANEL_PD#
20 BOARD_ID2
15 GPP_H23
15 GPP_H21

61 CNV_WT_CLK_DN
61 CNV_WT_CLK_DP
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WR_CLK_DN
61 CNV_WR_CLK_DP
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1

18 PROJECT_ID0
15 GPD7
62 WWAN_BB_RST#
20,62 WWAN_DB_DET#
20,55 LCD_CBL_DET#
29 SPK_ID





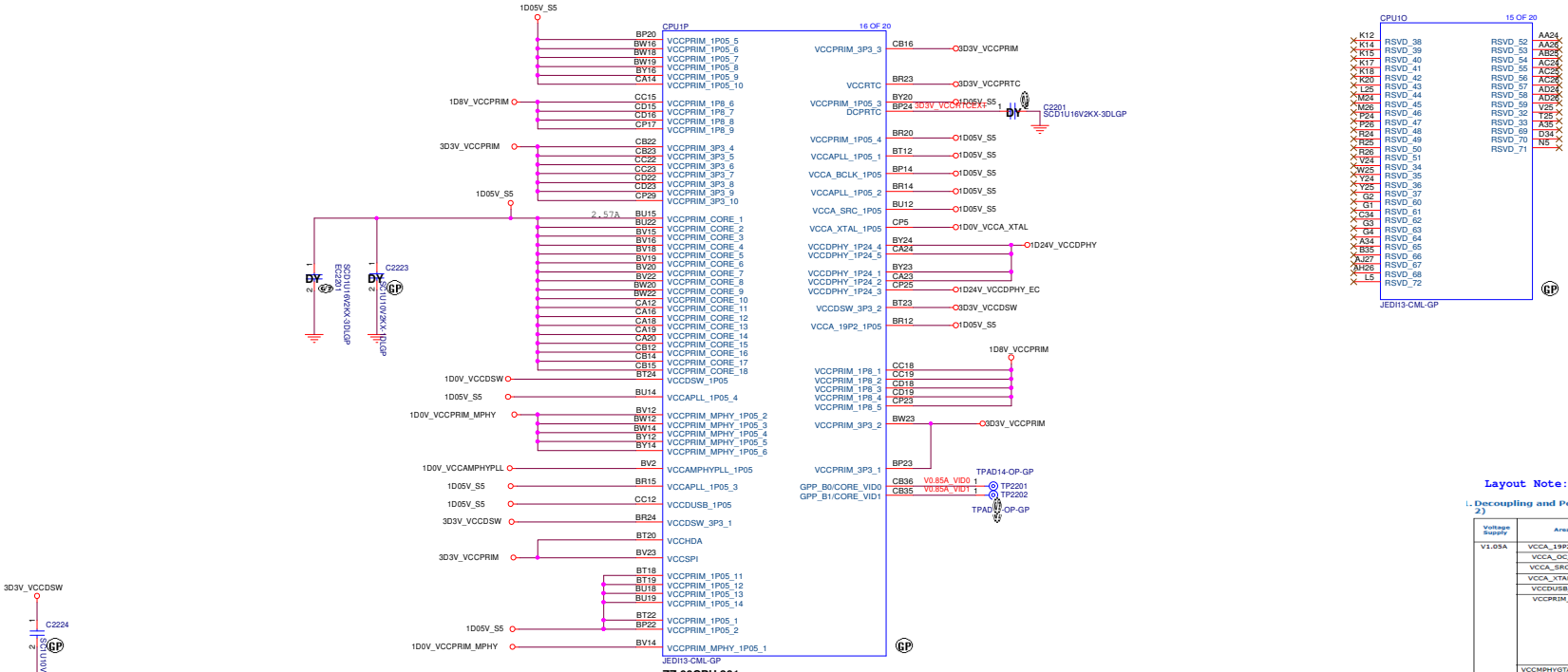
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude (Reseved)
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Series
		01	7000 Series
		00	N/A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVI)
Size: A2 | Document Number: Mockingbird_CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 21 of 105

SSID = CPU



Layout Note:

1. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC12	-	-	-	-	
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, BP20, BW16, BW18, BW19, BV16, CA14, BR20, BY20, BT16, BT19, BU18, BU19	1uF	0402	1	E	BP20
	VCCMPHYGTAON_1P05	BV12, BW12, BW14, BV12, BY14, BV14	22uF	0603	1	E	BV12
	VCCAMPHYPLL_1P05	BV2	1uF	0402	1	E	BV2
V1.0A / V0.85A	VCCPRIM_CORE	BU15, BU22, BV13, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV18, Note 1
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23,CC15, CD15, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP29,BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DSW	VCCDSW_GPIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BY23, CA23, CP25, BY24, CA24	4.7uF	0402	1	E	CP25

Notes:
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, refer to "Loop Inductance Reduction Decoupling".
5. Refer to Electromagnetic Interference chapter for recommended placement
6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.

<Core Design>

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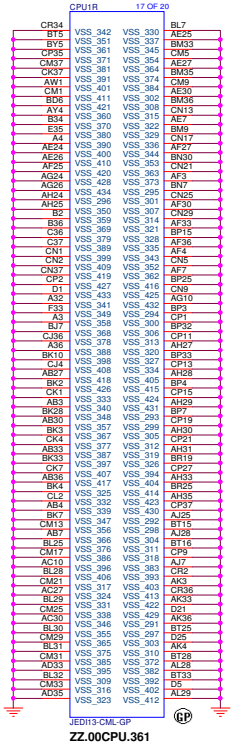
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

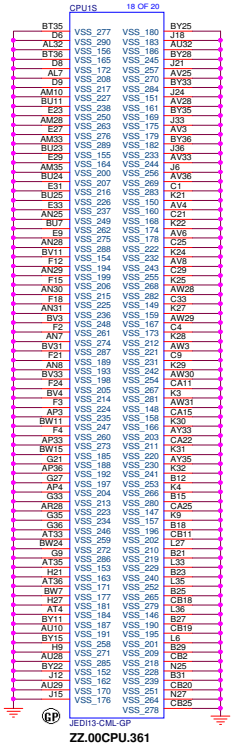
Size	Document Number	Rev
A2	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 22 of 105

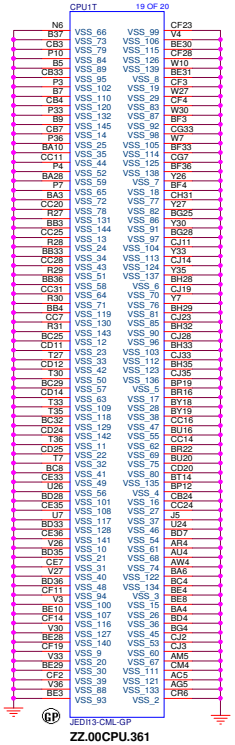
SSID = CPU



ZZ.00CPU.361



ZZ.00CPU.361



ZZ.00CPU.361

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

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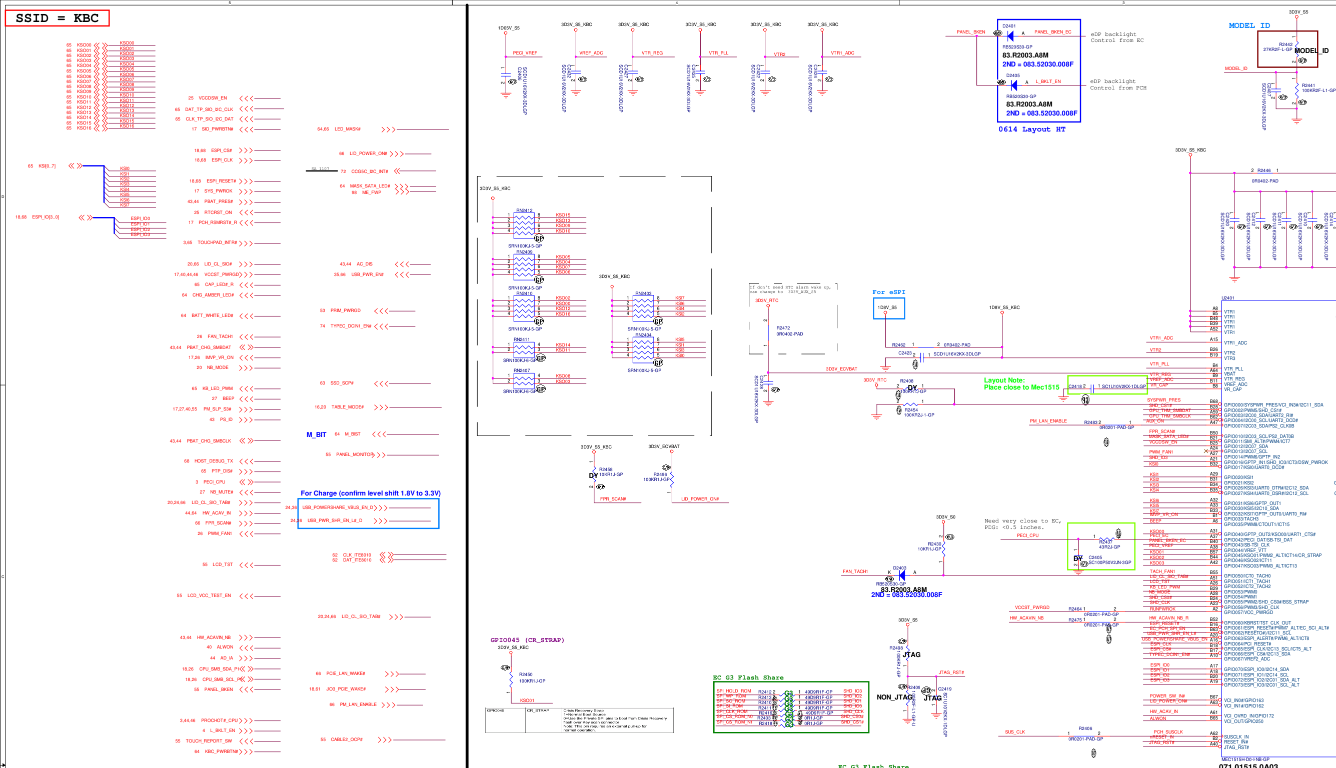
Title: PCH_(VSS)

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 23 of 105



#	Hellcat	MockingBird	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	14" UMA	N5 14"/15" UMA	100.0K	10.0K	3
2	13" Upsell UMA	V5 14"/15" UMA	100.0K	17.8K	2.801
3	13" MS/15" MS UMA	L 14"/15" UMA (CML & KBL-R)	100.0K	27.0K	2.598
4	17" CS UMA		100.0K	37.4K	2.402
5	15" Upsell UMA	N5 14"/15" DIS	100.0K	49.9K	2.201
6	17" 2in1 UMA	V5 14"/15" DIS	100.0K	64.9K	2.001
7	14"/15" MS DIS	L 14"/15" DIS (CML)	100.0K	82.5K	1.808
8	17" CS DIS		100.0K	107K	1.594
9	15" Upsell DIS		100.0K	154K	1.299
10	17" 2in1 DIS		100.0K	200K	1.1

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

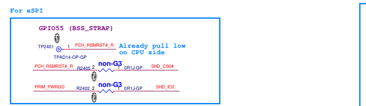


TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNote 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/ICT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

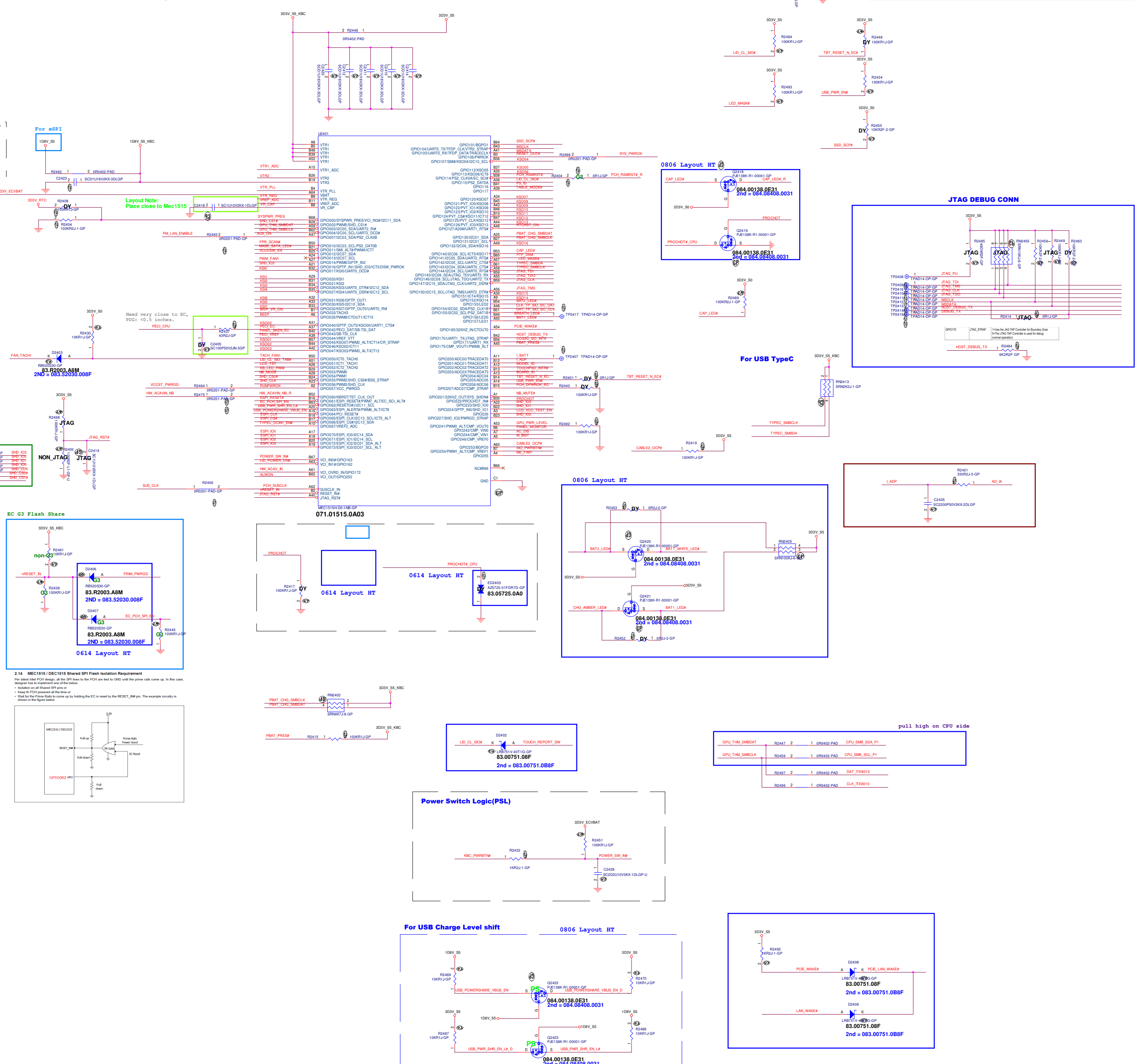
2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI CS0# is detected high while RSMRST# is low.



Vader15"/17" CML

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE285PA0DX

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 24 of 106

SSID = SPI Flash

Socket for 16M

SKT251 — SKT-G6179HT0321-001-GP — 62.10089.011

Layout : SKT251 and U2503 co-lay

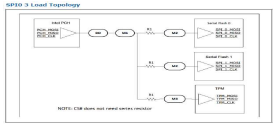
U2501 — 8M — W25Q64JVSSIQ-GP
072.25Q64.0H01
2nd = 072.25647.000D
3rd = 072.02564.0H01

U2503 — 16M — W25Q128JVSIQ-GP
072.25128.0B51
2nd = 072.25128.0D61
3rd = 072.25128.0F0D

Dual SPI0 Devices + TPM Topology Guidelines

The CFL PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device. The system can be configured with 1 SPI0 Flash and 1 TPM device.

SPI0 3 Load Topology



Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, mils	
				Segment	Total	Segment	Total

Notes:
1. R1 Resistor should be 15 ohm for 1.8V and 33 ohm for 3.3V. SPI0_I/O2 and SPI0_I/O3 connection to be pulled up with 1k ohm on R2 resistor.
2. 5 number of vias can be allowed.
3. Reference plane should be Continuous Ground Plane only allowed.
4. This topology relates to SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO and SPI0_CLK
5. Design guideline support up to 50MHz.

SSID = RTC

0614 Layout HT

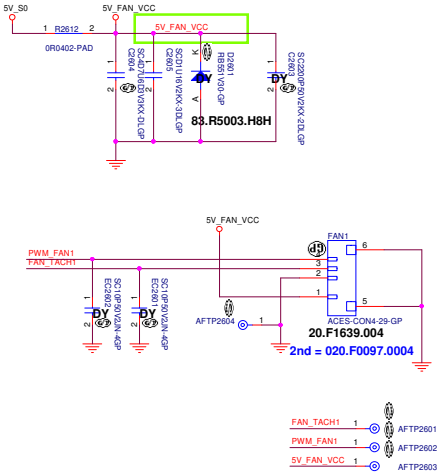
0614 Layout HT

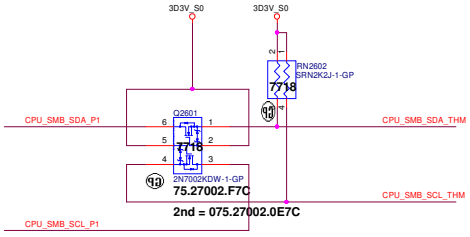
0614 Layout HT

SSID = Thermal Sensor

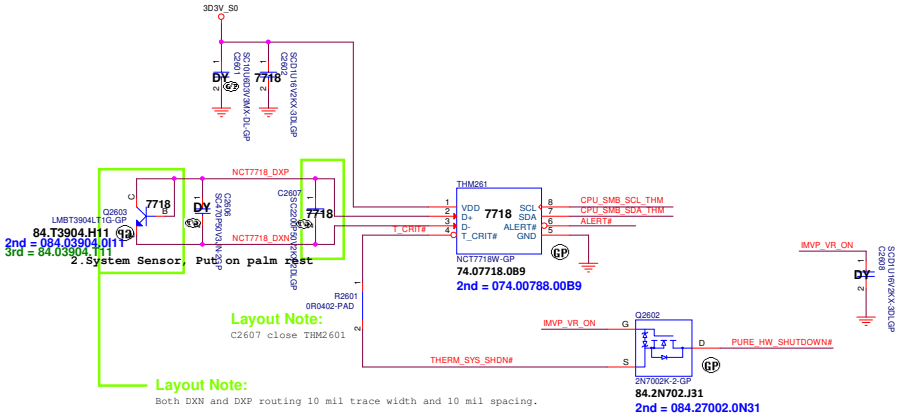
PWM FAN1

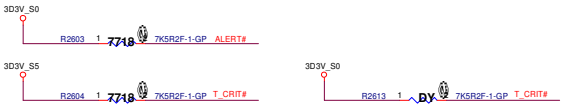
Layout Note:
Signal Routing Guideline:
Trace width = 15mil





18,24 CPU_SMB_SDA_P1
18,24 CPU_SMB_SCL_P1
17,24 IMVP_VR_ON
40 PURE_HW_SHUTDOWN#
24 PWM_FAN1
24 FAN_TACH1





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

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Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: Mockingbird_CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 28 of 105

SSID = Audio

19 HDA_SDIN0_CPU
19 HDA_SDOUT_CODEC
19 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC

29 AUD_SPK_R+
29 AUD_SPK_R-
29 AUD_SPK_L+
29 AUD_SPK_L-

24 NB_Mute#
15,19 SPKR
24 BEEP
66 AUD_SENSE
29 LINE1_VREFO
29 MIC2_VREFO
29 AUD_HP1_JACK_L
29 AUD_HP1_JACK_R
29 LINE1_L
29 LINE1_R

29,66 AUD_SLEEVE
29,66 AUD_RING
55 DMIC_SCL_CODEC
55 DMIC_SDA_CODEC
17,40,55 PM_SLP_S3#

Audio Codec Chip ALC3204

Analog
Digital
>2A
moat
ALC3204
071.03204.0003
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power
DVDD must >= DVDD_IO
Azalia I/F EMI
150mA
084.03413.0031
2nd = 084.02301.0031
084.00138.0E31
2nd = 084.08408.0031
75.00054.A7D
2nd = 75.00054.T7D
SC-20191202
Tied at point only under Codec or near the Codec
Place close to Pin 20
place close to pin8
For RTC Gen9 reset circuit change power rail. 20170921

<Core Design>

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Title: Audio Codec ALC3204
Size: A2
Document Number: Mockingbird_CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 27 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

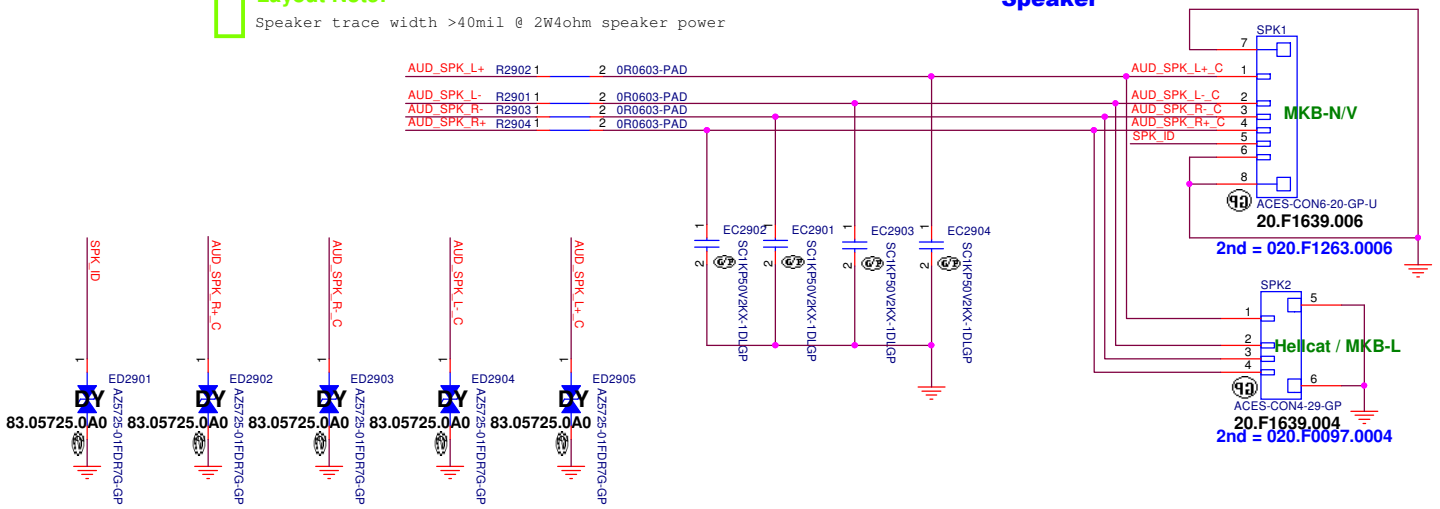
Size	Document Number	Rev
A4	*Mockingbird_CML*	*SC*

Date: Monday, December 09, 2019 Sheet 28 of 105

SSID = Audio

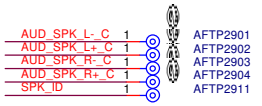
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: FG
0: Veci



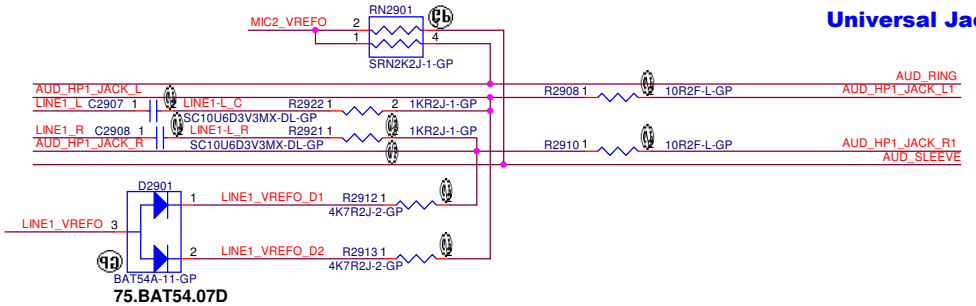
27 AUD_SPK_R+
27 AUD_SPK_R-
27 AUD_SPK_L-
27 AUD_SPK_L+

21 SPK_ID

From Codec

27 MIC2_VREFO
27,29,66 AUD_RING
27 AUD_HP1_JACK_L
27 LINE1_L
27 LINE1_R
27 AUD_HP1_JACK_R
27,29,66 AUD_SLEEVE
27 LINE1_VREFO

Universal Jack (Moved to I/O Board)



To IO Board

27,29,66 AUD_RING
66 AUD_HP1_JACK_L1
66 AUD_HP1_JACK_R1
27,29,66 AUD_SLEEVE

<Core Design>

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Title: Audio IO

Size	Document Number	Rev
A3	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 29 of 105

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<Core Design>

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Title

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Size	Document Number	Rev
A4	**Mockingbird_CML**	**SC**

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<Core Design>

Wistron Corporation
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Title
LAN RTL8106

Size	Document Number	Rev
Custom	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 31 of 105

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size: A3 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 32 of 105

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5170

Size	Document Number	Rev
A4	***Mockingbird_CML***	***SC***

Date: Monday, December 09, 2019 Sheet 33 of 105

<Core Design>

Wistron Corporation
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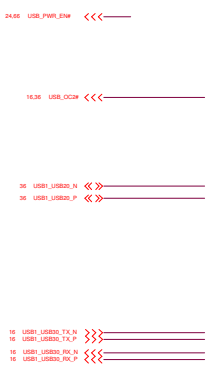
Taipei Hsien 221, Taiwan, R.O.C.

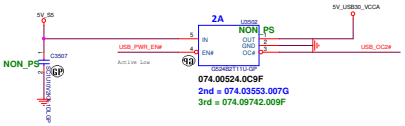
Title: USB2.0 CONN

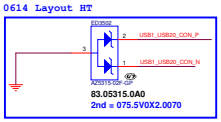
Size	Document Number	Rev
	Mockingbird_CML	SC

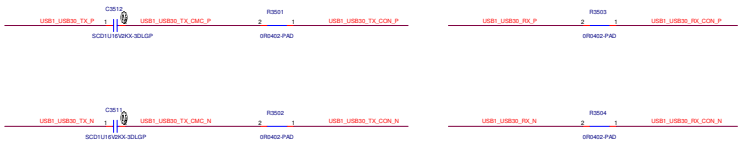
Date: Monday, December 09, 2019 Sheet 34 of 105

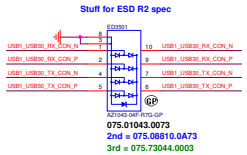
SSID = USB3.0 Port1

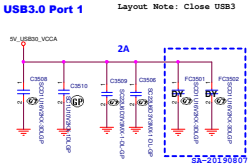


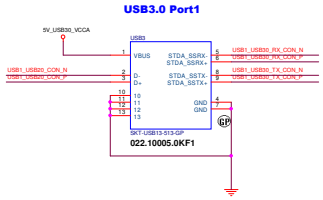












Main Func = USB3.0 Port2

<Core Design>

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File:

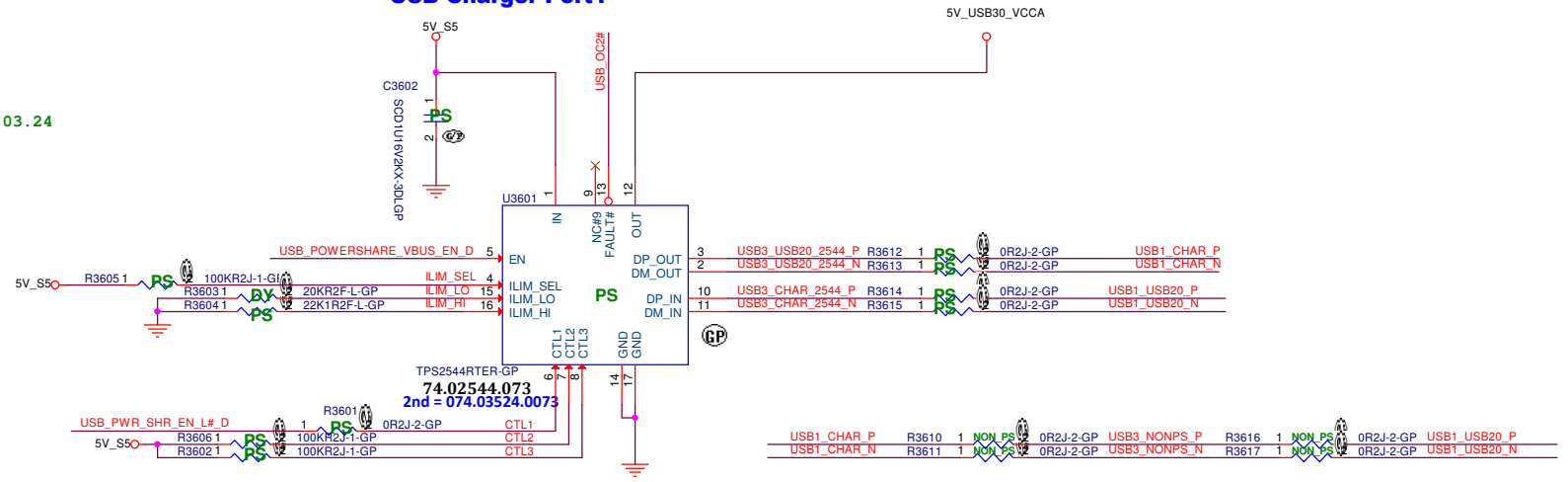
USB3.0 CONN

Size	Document Number	Rev
A1	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 35 of 155

SSID = USB Charger

USB Charger Port1



2018.03.24

16 USB1_CHAR_P
16 USB1_CHAR_N

35 USB1_USB20_N
35 USB1_USB20_P

24 USB_POWERSHARE_VBUS_EN_D
24 USB_PWR_SHR_EN_L#_D

16,35 USB_OC2#

Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_typ}\,(mA) = \frac{50{,}500}{(R_{ILIM\_XX}\,(k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

BOLT 15 32bit 0822

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Charger

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 36 of 105

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<Core Design>

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Title

USB3.0 PORT

Size	Document Number	Rev
A4	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 37 of 105

(Blanking)

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A4	Mockingbird_CML	SC

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<Core Design>

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Title
(RSVD)

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SSID = Power Plane & Sequence

5V_S0 & 3D3V_S0

17,27,55 PM_SLP_S3#

HW_SHUTDOWN

45 3V_5V_EN

26 PURE_HW_SHUTDOWN#

24 ALWON

POWER GOOD

51 1D2V_VTT_PWRGD

VCCIO & VCCSTG

21 GPPC_H18_BOOTMPC

17,24,44,46 VCCST_PWRGD

17,61,62,63,66,91 PLT_RST#

VCCST_CPU

17,51,56 PM_SLP_S4#

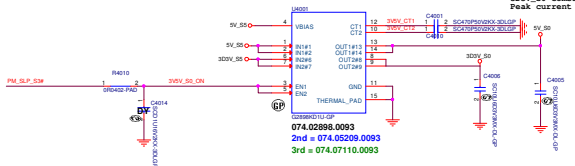
ROSA Run Power

5V_S0

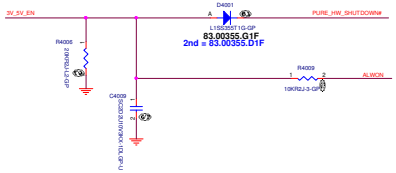
5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A



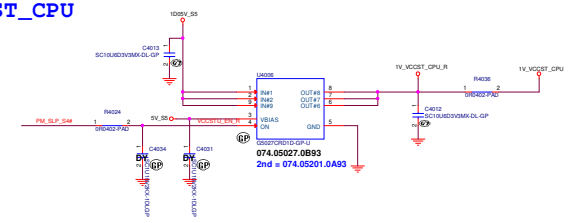
ROSA Run Power



MANAGEMENT RAIL POWER GENERATION

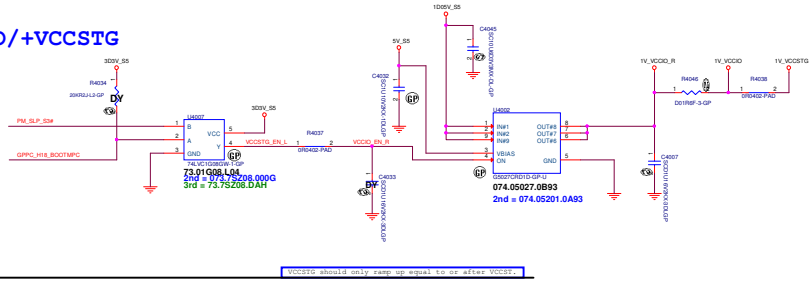
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST_CPU



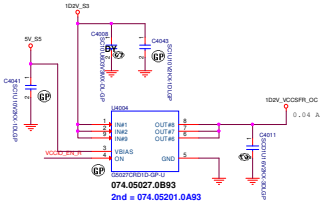
Power Good

+VCCIO/+VCCSTG

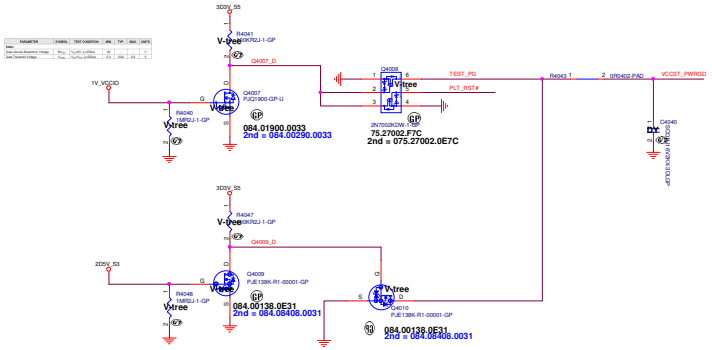


VCCSTG should only ramp up equal to or after VCCST.

1D2V_VCCSFR_OC



V-tree_VCCIO



<Core Design>

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Title: Power Plane Enable

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<Core Design>

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Title
Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	***Mockingbird_CML***	*SC*

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(Blanking)

<Core Design>

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A4	Mockingbird_CML	SC

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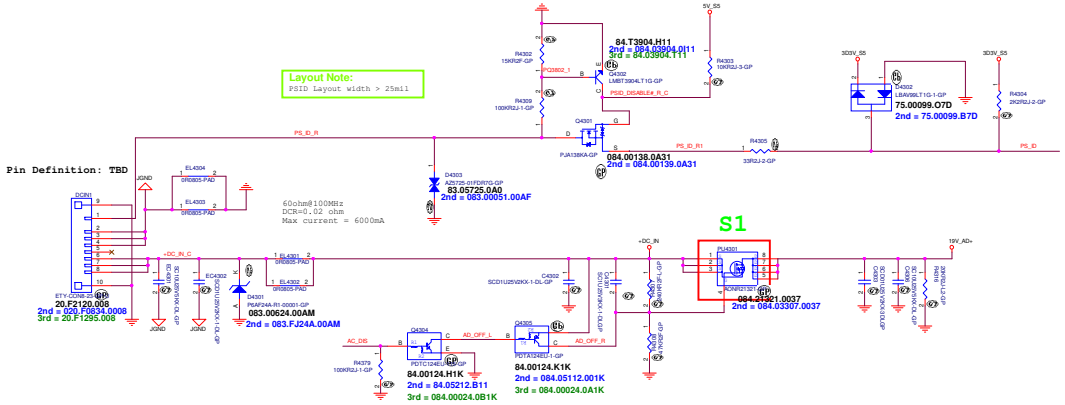
SSID = ADT Input

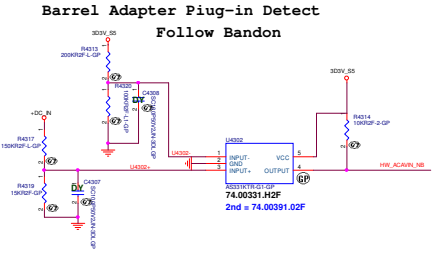
24.44 AC_DIS

24 PS_ID

24.44 HW_ACAVIN_NB

89 +DC_IN_C



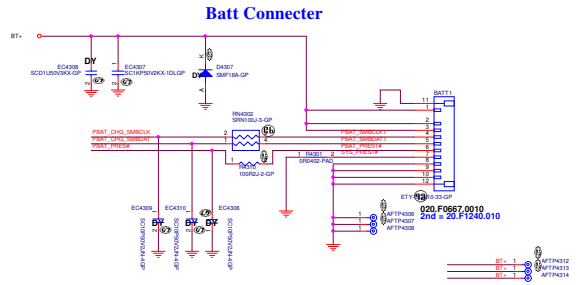


24.44 PBAT_CHG_SMBCLK

24.44 PBAT_CHG_SMBDAT

24.44 PBAT_PRES#

SSID = M-BAT Input



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Title: DCIN

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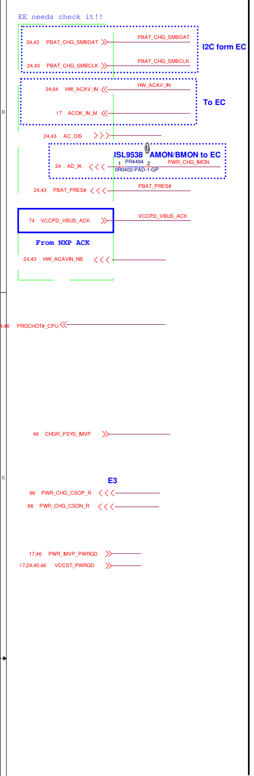
SSID = Charger

ISL9538C For Charger

OFFPAGE



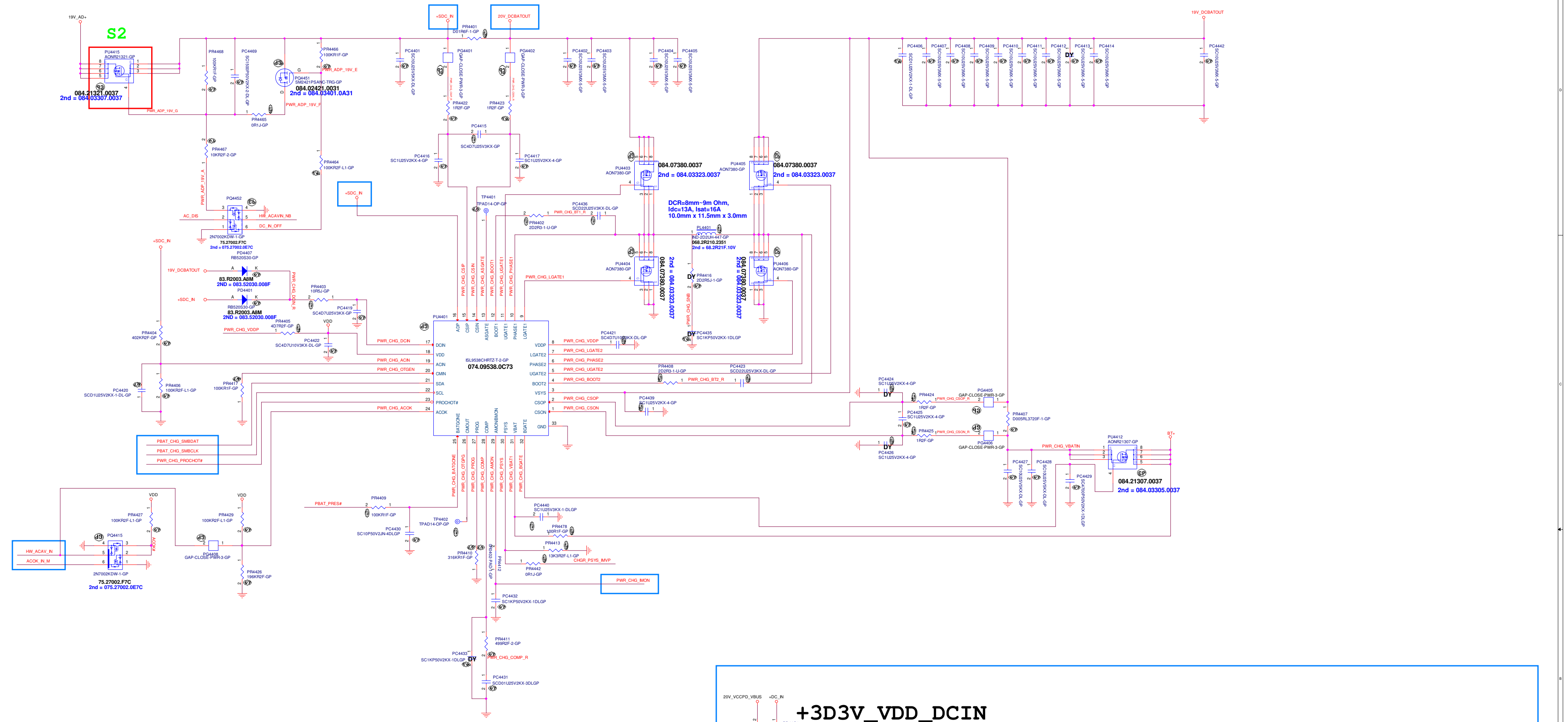
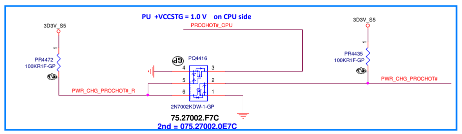
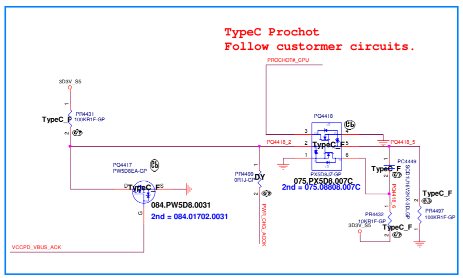
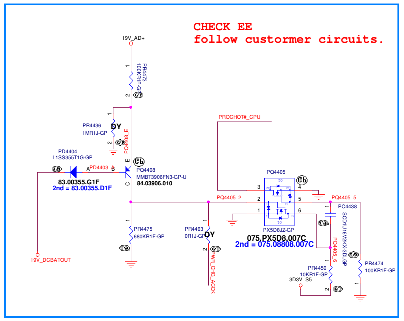


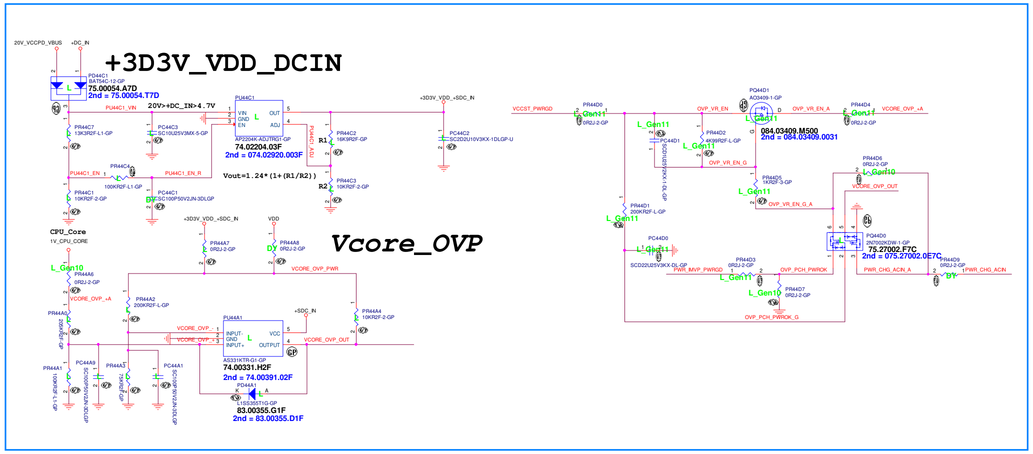
TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476









Jedi15"/17" CML

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Title: Power (Charger_ISL9538)

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

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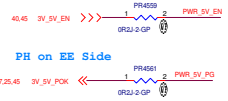
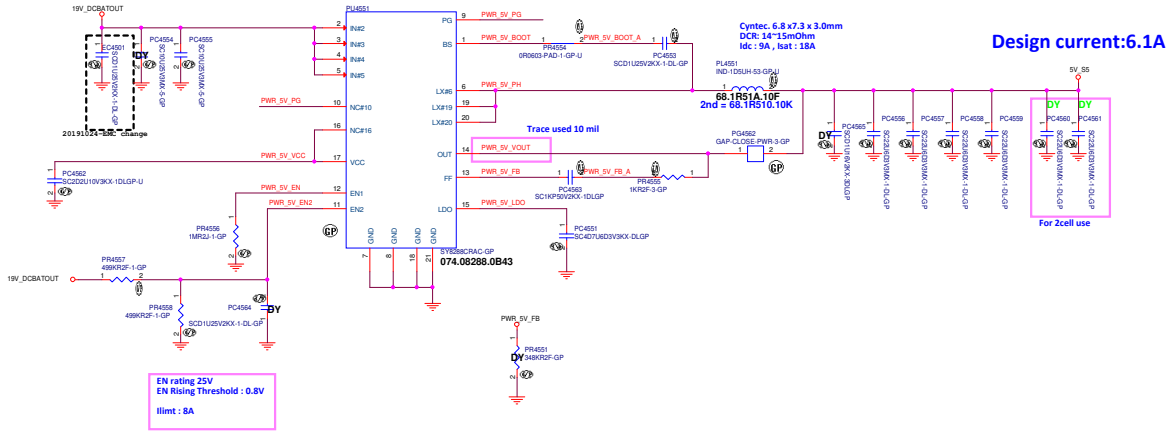
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP



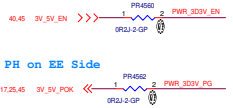
SY8288C For 5V

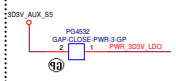


SSID = PWR.Plane.Regulator_3D3V

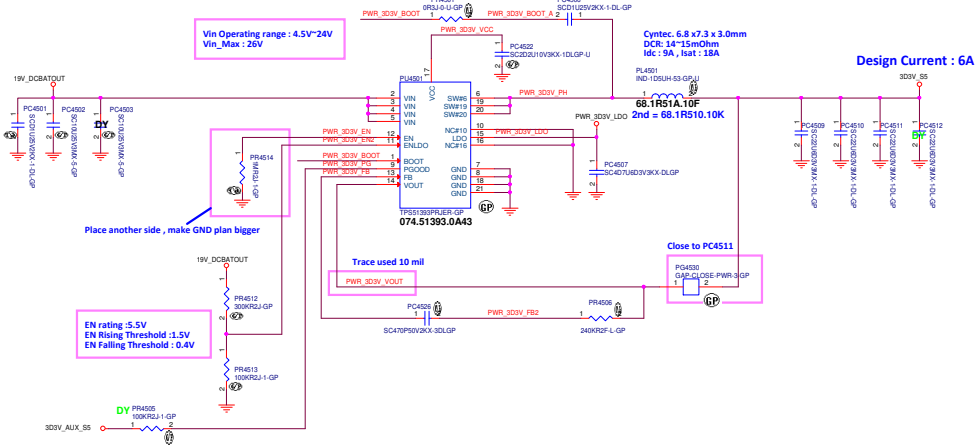
OFFPAGE-Signal

OFFPAGE-GAP





TPS51393 For 3D3V



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Title: POWER (8288_5V/51393_3D3V)

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SSID = CPU_CORE

OFFPAGE

PH on CPU side

3,24,44 PROCHOT#_CPU

7 SVID_ALERT#_CPU

7 SVID_CLK_CPU

7 SVID_DATA_CPU

17,44 PWR_IMVP_PWRGD

17,24,40,44 VCCST_PWRGD

For VCCGT Sense

8 VSSGT_SENSE

8 VCCGT_SENSE

For Vcore Sense

7 VCCORE_SENSE

7 VSSCORE_SENSE

For Vccsa Sense

8 VSSSA_SENSE

8 VCCSA_SENSE

EE side Link
SVID Pull High V

1V_VCCST_CPU — PC4601 GAP-CLOSE_PWR-2-GP — PWR_CORE_VCCST

47 PWR_VCORE_PWMB

47 PWR_VCORE_ISUMN

47 PWR_VCORE_ISUMP

47 PWR_VCORE_FCCM#

47 PWR_VCORE_PWMA

48 PWR_VCCGT_PWM

48 PWR_VCCGT_FCCM#

48 PWR_VCCGT_ISUMN

48 PWR_VCCGT_ISUMP

50 PWR_VCCSA_ISUMP

50 PWR_VCCSA_ISUMN

50 PWR_VCCSA_PWM

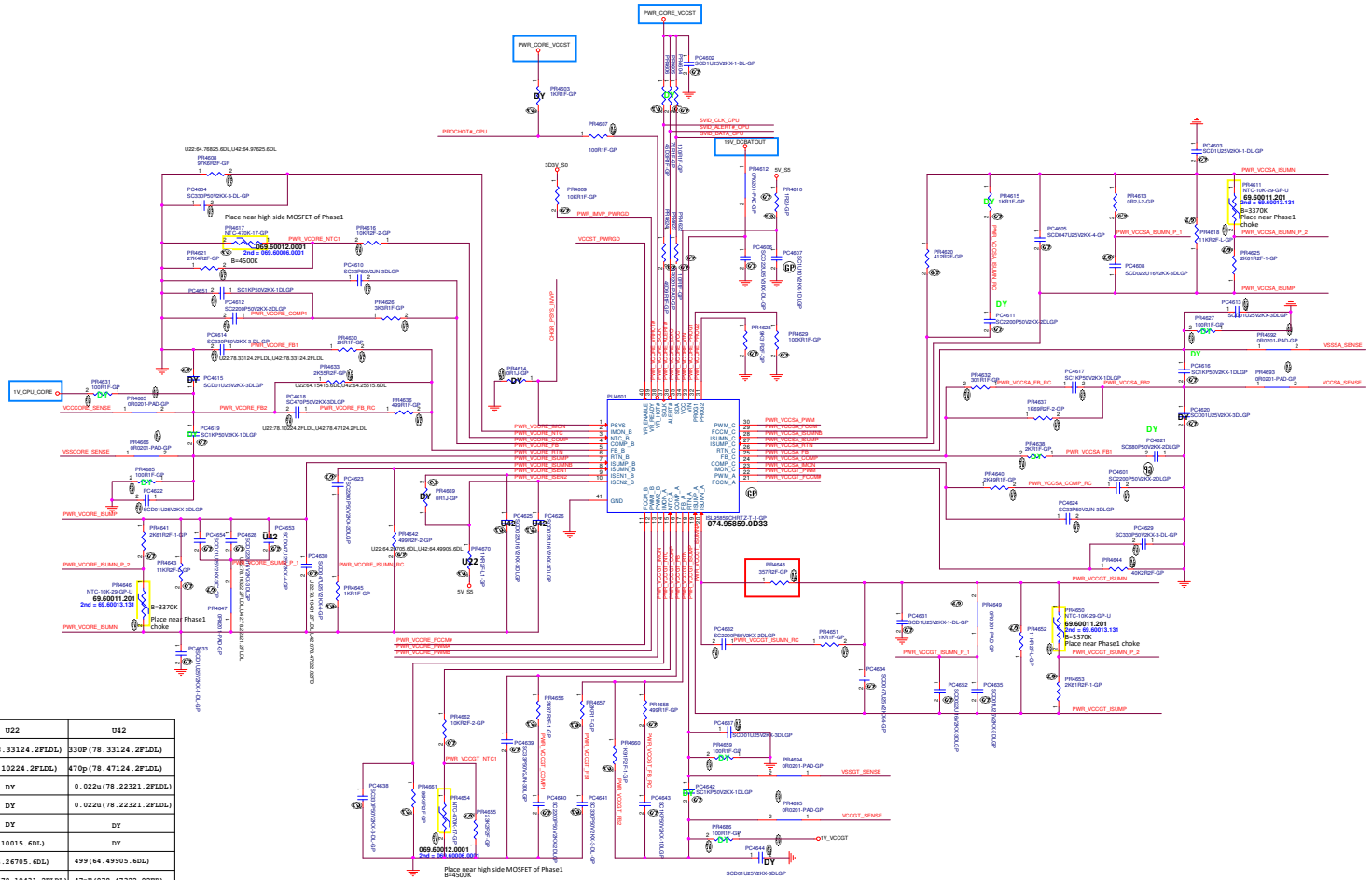
50 PWR_VCCSA_FCCM

47 PWR_VCORE_ISEN1

47 PWR_VCORE_ISEN2

44 CHGR_PSYS_IMVP

ISL95859C For CPUCORE



	U22	U42
PC4614	330P(78.33124.2FLDL)	330P(78.33124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4670	1K(64.10015.6DL)	DY
PR4642	267(64.26705.6DL)	499(64.49905.6DL)
PC4630	0.1uF(78.10431.2FLDL)	47nF(078.47322.02FD)
PC4628	0.01uF(78.10322.2FLDL)	22nF(78.22321.2FLDL)
PC4654	DY	0.01uF(78.10322.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
PR4608	76.8K(64.76825.6DL)	97.6K (64.97625.6DL)

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File: POWER (95859_CPUCORE(1/3))

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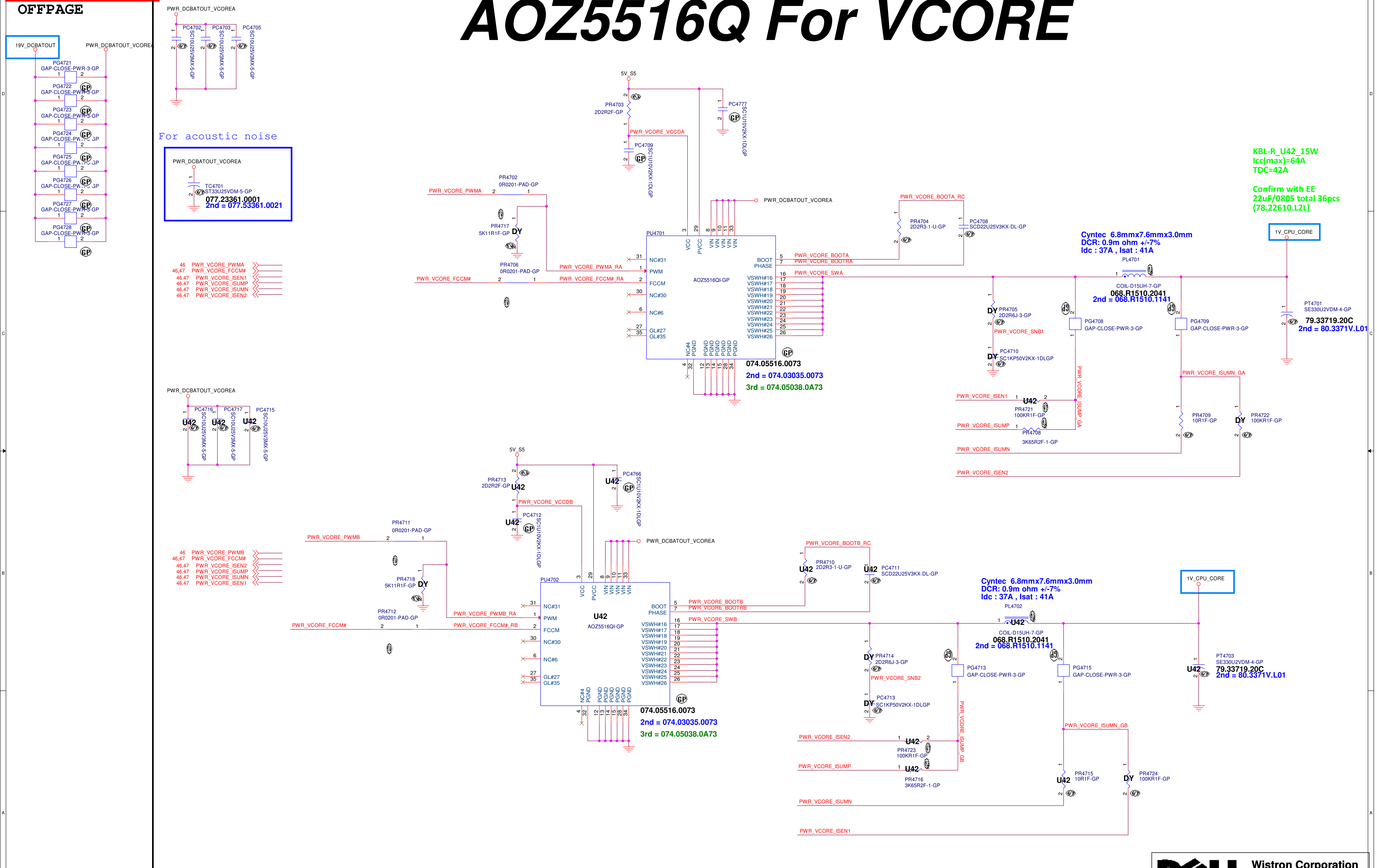
SSID = CPU_CORE

OFFPAGE

AOZ5516Q For VCORE



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Title	POWER (5038_CPU_VCORE(2/3))
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SSID = CPU_CORE

AOZ5516Q For VCCGT

Offpage-Signal

19V_DCBATOUT

PWR_DCBATOUT_VCCGT

PG4801 GAP-CLOSE-PWR-3-GP

PG4802 GAP-CLOSE-PWR-3-GP

PG4803 GAP-CLOSE-PWR-3-GP

PG4804 GAP-CLOSE-PWR-3-GP

For acoustic noise

PC4802 SC10U25V3MX-5-GP

PC4803 SC10U25V3MX-5-GP

PC4804 SC10U25V3MX-5-GP

PWR_DCBATOUT_VCCGT

TC4801 ST33U25VDM-5-GP

077.23361.0001

2nd = 077.53361.0021

5V_S5

46 PWR_VCCGT_PWM

46 PWR_VCCGT_FCCM#

46 PWR_VCCGT_ISUMP

46 PWR_VCCGT_ISUMN

PR4804 2D2R2F-GP

PC4866 SC1U10V2KX-1DLGP

PWR_VCCGT_VCC_R

PC4808 SC1U10V2KX-1DLGP

PR4802 0R0201-PAD-GP

PWR_VCCGT_PWM

PR4812 5K11R1F-GP DY

PR4806 0R0201-PAD-GP

PWR_VCCGT_FCCM#

PWR_VCCGT_PWM_R

PWR_VCCGT_FCCM#_R

PU4801

AOZ5516QI-GP

VCC PVCC VIN VIN VIN VIN VIN

NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35

BOOT PHASE

VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26

NC#4 PGND PGND PGND PGND PGND PGND

074.05516.0073

2nd = 074.03035.0073

3rd = 074.05038.0A73

PWR_VCCGT_BOOT

PWR_VCCGT_BOOTR

PWR_VCCGT_SW

PWR_VCCGT_BOOT_RC

PR4805 2D2R3-1-U-GP

PC4807 SCD22U25V3KX-DL-GP

PR4803 2D2R6J-3-GP DY

PWR_VCCGT_SNB

PC4806 SC1KP50V2KX-1DLGP DY

PR4808 3K65R2F-1-GP

PWR_VCCGT_ISUMP

PWR_VCCGT_ISUMP_G

PWR_VCCGT_ISUMN

PWR_VCCGT_ISUMN_G

PR4801 0R0201-PAD-GP

PL4801

COIL-D15UH-7-GP

068.R1510.2041

2nd = 068.R1510.1141

Cyntec 6.8mmx7.6mmx3.0mm

DCR: 0.9m ohm +/-7%

Idc : 37A , Isat : 41A

PG4807 GAP-CLOSE-PWR-3-GP

PG4808 GAP-CLOSE-PWR-3-GP

1V_VCCGT

PANASONIC

ESR: 9 mohm

PT4801 SE330U2VDM-4-GP

79.33719.20C

2nd = 80.3371V.L01

KBL_U22_15W

Icc(max)=31A

TDC=21A

Confirm with EE

22uF/0805 total 33pcs

(78.22610.L2L)

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Title: POWER (5038_CPU_VCORE(3/3))

Size: A3 | Document Number: Mockingbird_CML | Rev: SC

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RSVD

<Core Design>

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Title: POWER (CPU_VCCGTS_RSVD)

Size	Document Number	Rev
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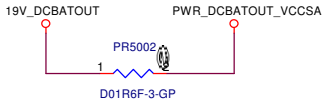
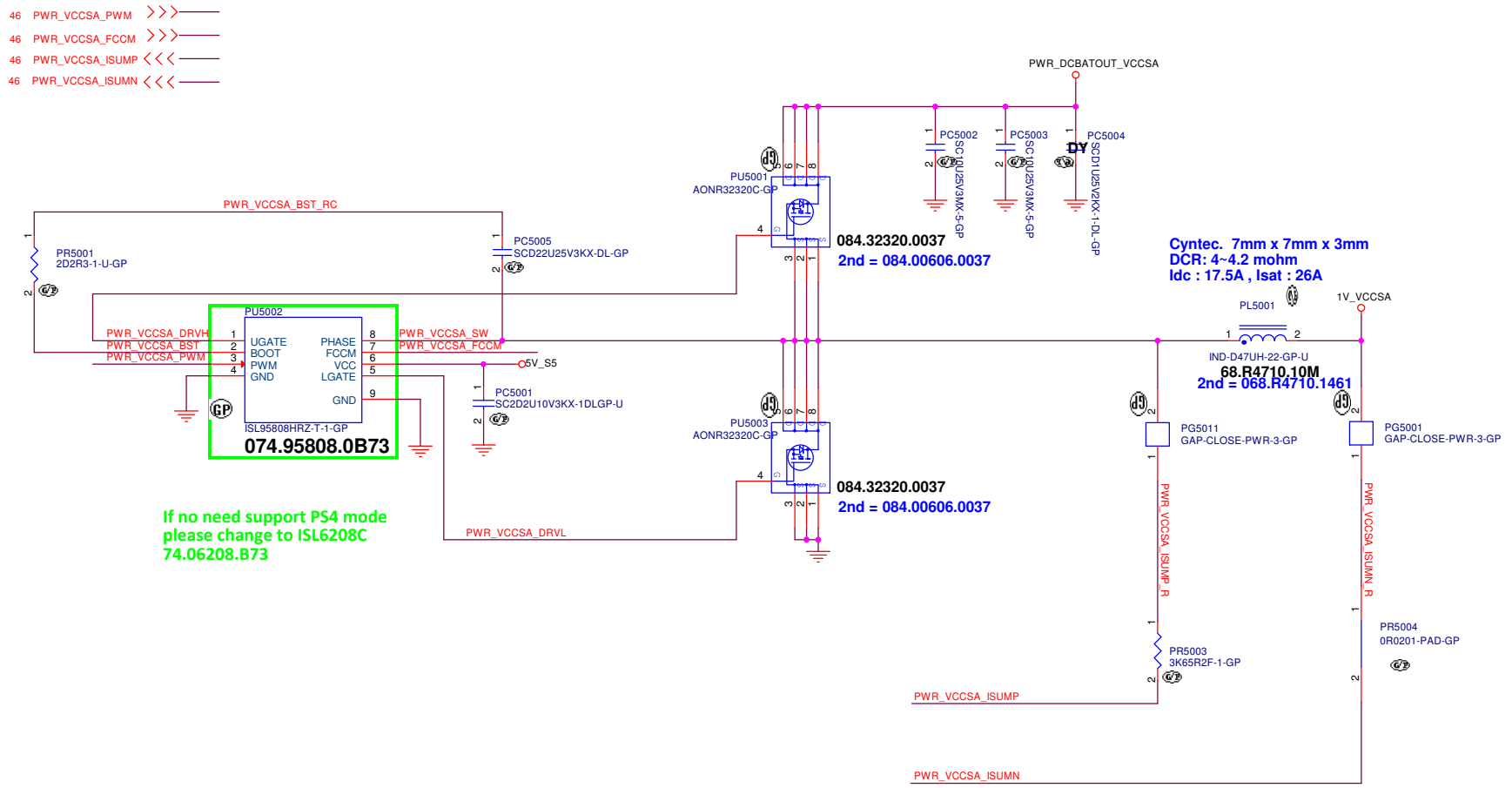
Main Func = CPU_CORE

ISL95808 For VCCSA

OFFPAGE





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Title: POWER (ISL95808_VCCSA)

Size	Document Number	Rev
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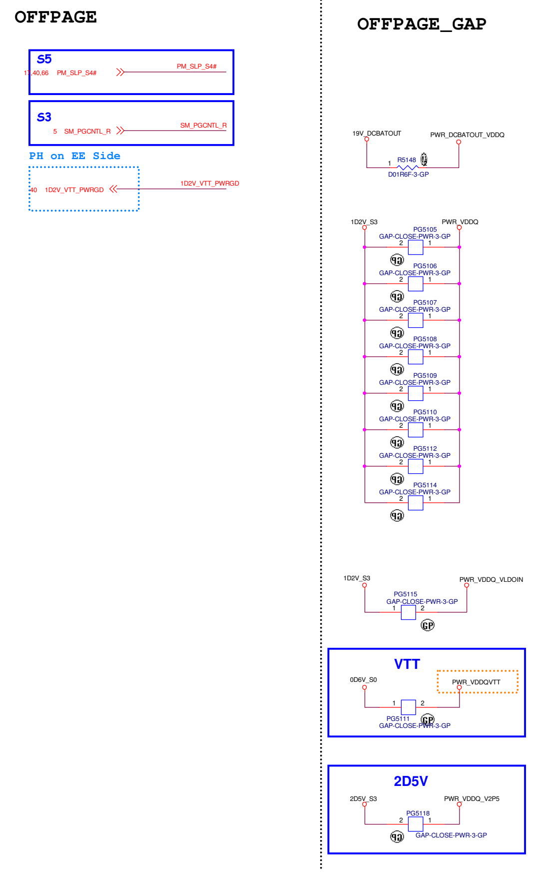
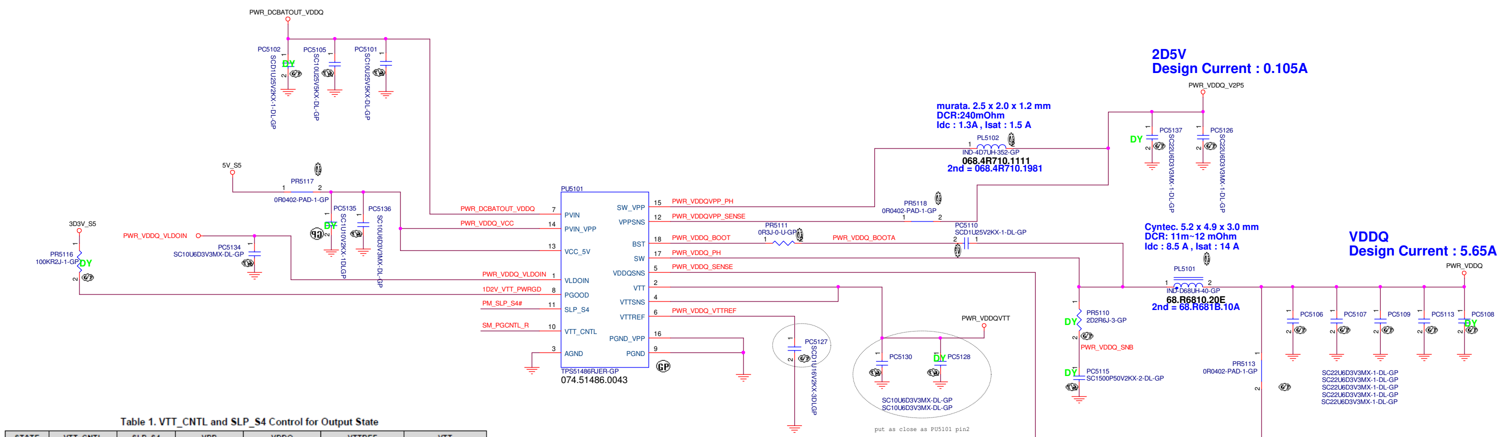
SSID = PWR.Plane.Regulator_1D2V/0D6V



OFFPAGE
S5
PM_SLP_S4#
S3
SM_PGCNTL_R
PH on EE Side
1D2V_VTT_PWRGD
OFFPAGE_GAP
19V_DCBATOUT
PWR_DCBATOUT_VDDQ
R5148
D01R6F-3-GP
1D2V_S3
PWR_VDDQ
PG5105
PG5106
PG5107
PG5108
PG5109
PG5110
PG5112
PG5114
GAP-CLOSE-PWR-3-GP
PG5115
PWR_VDDQ_VLDOIN
VTT
0D6V_S0
PWR_VDDQVTT
PG5111
2D5V
2D5V_S3
PWR_VDDQ_V2P5
PG5118



PWR_DCBATOUT_VDDQ
PC5102
PC5105
PC5101
5V_S5
PR5117
0R0402-PAD-1-GP
3D3V_S5
PWR_VDDQ_VLDOIN
PC5134
SC10U6D3V3MX-DL-GP
PR5116
100KR2J-1-GP
PC5135
PC5136
PU5101
PVIN
PVIN_VPP
VCC_5V
VLDOIN
PGOOD
SLP_S4
VTT_CNTL
AGND
SW_VPP
VPPSNS
BST
SW
VDDQSNS
VTT
VTTSNS
VTTREF
PGND_VPP
PGND
TPS51486RJER-GP
074.51486.0043
PWR_VDDQ_VCC
1D2V_VTT_PWRGD
PM_SLP_S4#
SM_PGCNTL_R
PWR_VDDQVPP_PH
PWR_VDDQVPP_SENSE
PWR_VDDQ_BOOT
PWR_VDDQ_BOOTA
PWR_VDDQ_PH
PWR_VDDQ_SENSE
PWR_VDDQ_VTTREF
murata. 2.5 x 2.0 x 1.2 mm
DCR:240mOhm
Idc : 1.3A , Isat : 1.5 A
PL5102
068.4R710.1111
2nd = 068.4R710.1981
PR5118
PR5111
PC5110
2D5V
Design Current : 0.105A
PWR_VDDQ_V2P5
PC5137
PC5126
Cyntec. 5.2 x 4.9 x 3.0 mm
DCR: 11m~12 mOhm
Idc : 8.5 A , Isat : 14 A
PL5101
68.R6810.20E
2nd = 68.R681B.10A
VDDQ
Design Current : 5.65A
PWR_VDDQ
PR5110
PWR_VDDQ_SNB
PC5115
PR5113
PC5106
PC5107
PC5109
PC5113
PC5108
PWR_VDDQVTT
PC5127
PC5130
PC5128
put as close as PU5101 pin6
put as close as PU5101 pin2

VTT
Icc(max)=0.6A
Design Current=0.42A

Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	051_POWER (TPS51486R_VDDQ/VTT)	
Size: Custom	Document Number: MockingBird CML	Rev: SC
Date: Monday, December 09, 2019	Sheet 51 of 106	

SSID = PWR.Plane.Regulator_1D0V

TPS51397 For 1D05V

OFFPAGE-Signal

SC-20191202

25,53 3V_5V_DSW_OK — PR5210 150KR2J-GP — PWR_1D05V_EN

fine tune power sequence

OFFPAGE-GAP

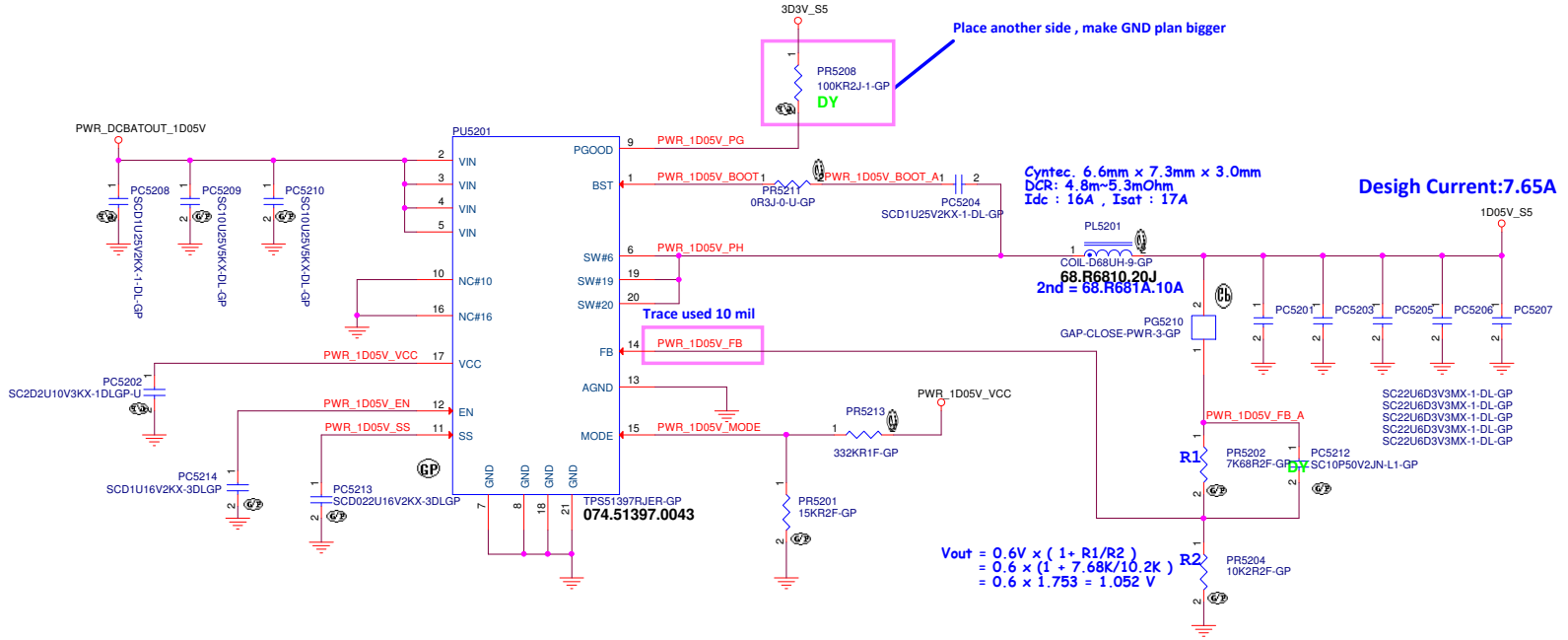
PWR_DCBATOUT_1D05V

19V_DCBATOUT

PG5201 GAP-CLOSE-PWR-3-GP

PG5202 GAP-CLOSE-PWR-3-GP

PG5203 GAP-CLOSE-PWR-3-GP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

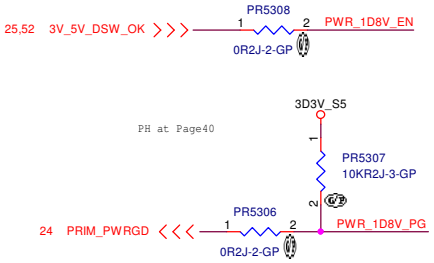
Title: POWER (TPS51397_1D05V)

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 52 of 105

SSID = 1D8V

OFFPAGE



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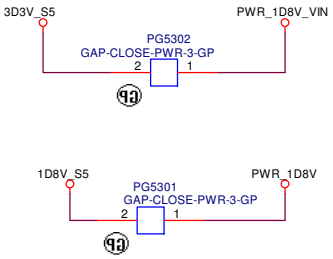
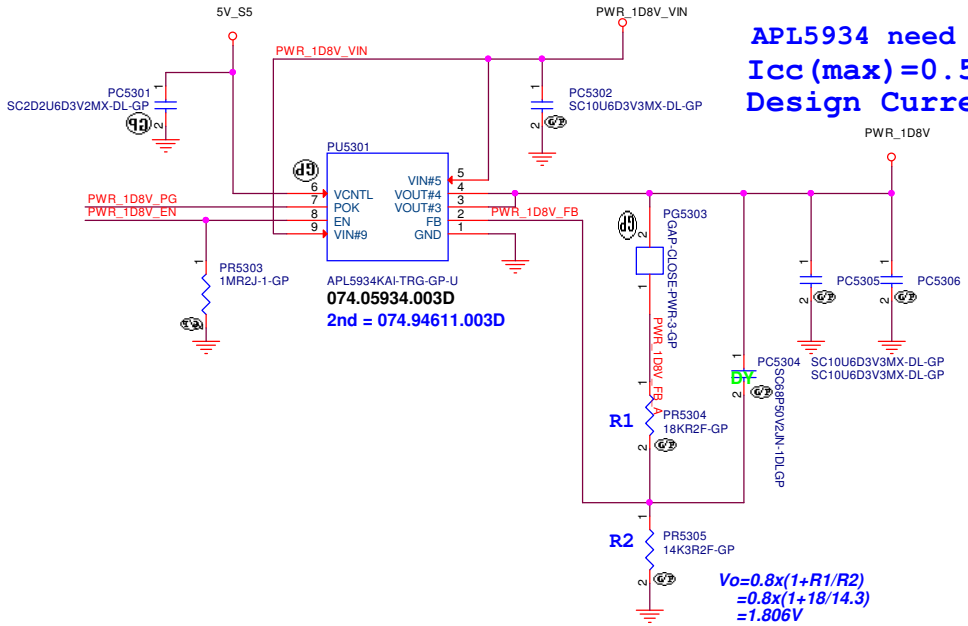


APL5934 for 1D8V



APL5934 need <1.8W
Icc(max)=0.585A
Design Current=0.41A

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (APL5934_1D8V)	
Size: A3	Document Number: Mockingbird_CML 53	Rev: SC
Date: Monday, December 09, 2019	Sheet of	

<Core Design>

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Title

054_LDO-V1D8V&2D5V

Size	Document Number	Rev
A3	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 54 of 105

SSID = LCD

Main Func = Touch panel

Main Func = CAMERA

INVERTER POWER

Hinge up cable protection

Near LCD1 connector

PANEL_PWRGD CIRCUIT

Touch Panel

CCD& CAM

Sensor Board

Display

eDP

Brightness

EC (BIST MODE)

IR LED POWER

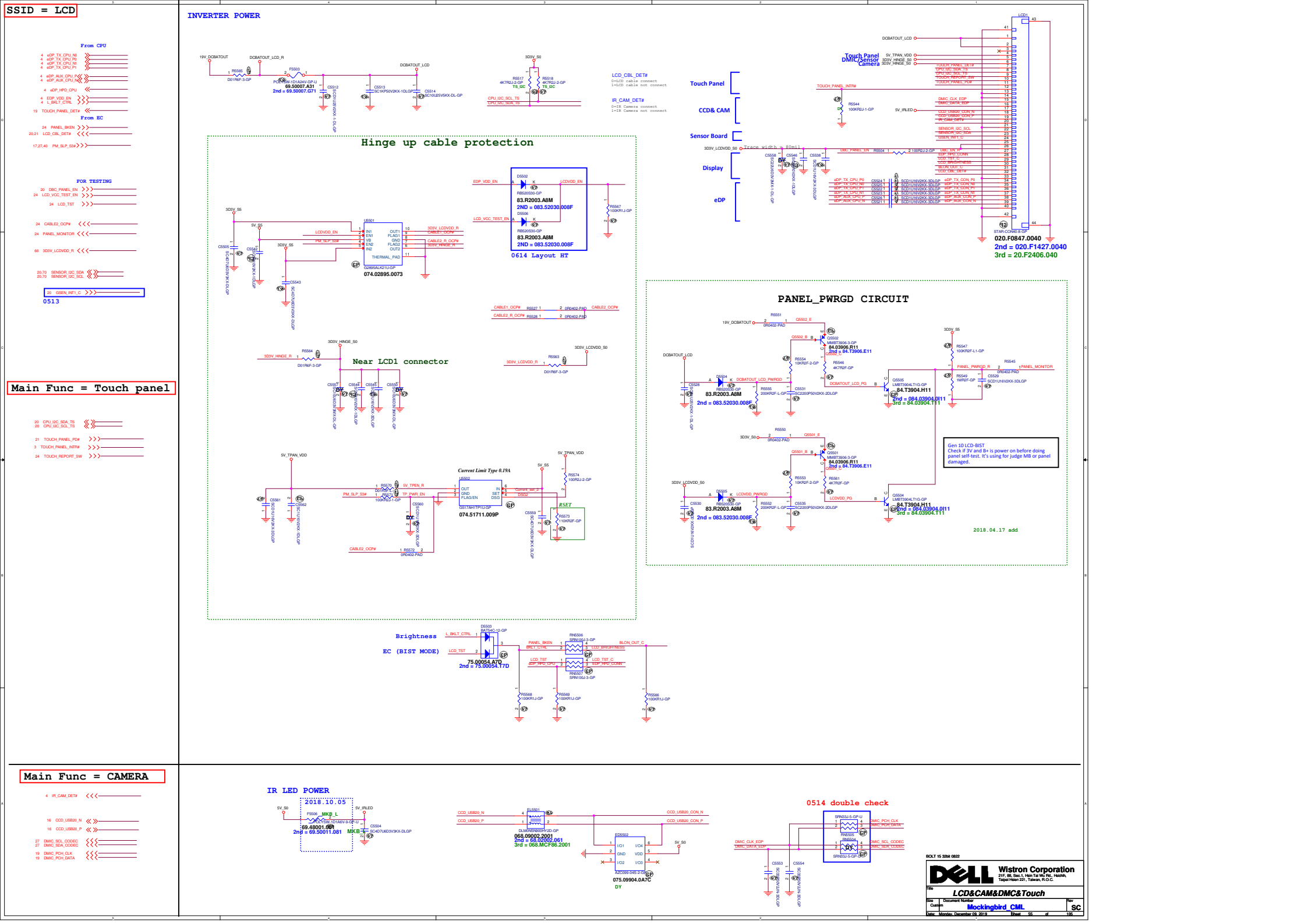
0513

0614 Layout HT

0514 double check

2018.04.17 add

Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT(Reserved)

Size: A3 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 56 of 105

SSID = HDMI Level Shifter/Connector

4 HDMI_DDI_TX_N0
4 HDMI_DDI_TX_P0
4 HDMI_DDI_TX_N1
4 HDMI_DDI_TX_P1
4 HDMI_DDI_TX_N2
4 HDMI_DDI_TX_P2
4 HDMI_DDI_TX_N3
4 HDMI_DDI_TX_P3

4 HDMI_SCL_CPU
4 HDMI_SDA_CPU
4 HDMI_HPD_CPU

HDMI_DDI_TX_N3 C5701 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_P3 C5704 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_N0 C5705 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_P0 C5703 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_N1 C5707 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_P1 C5706 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_N2 C5708 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_P2 C5709 1 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P2

SA-20190722

5V_S0
R5705 1 470R1F-GP
R5759 1 470R1F-GP
R5773 1 470R1F-GP
R5774 1 470R1F-GP
R5775 1 470R1F-GP
R5776 1 470R1F-GP
R5777 1 470R1F-GP
R5778 1 470R1F-GP
Q5701 PJE138K-R1-00001-GP
HDMI_PLL_GND
084.00138.0E31
2nd = 084.08408.0031

5V_S0
D5701 RB520S30-GP
D5702 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
83.R2003.A8M
2ND = 083.52030.008F

0614 Layout HT

HDMI_SCL_R
HDMI_SDA_R
RN5702 SRN2K2J-1-GP
3D3V_S0
Q5702
HDMI_SCL_CPU
HDMI_SCL_CON
HDMI_SDA_CPU
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
HDMI_SDA_CON

HDMI_DDI_TX_CON_N0
ER5701 180R2J-1-GP
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1
ER5702 180R2J-1-GP
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2
ER5703 180R2J-1-GP
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N3
ER5704 180R2J-1-GP
HDMI_DDI_TX_CON_P3

5V_S0
F5701
5V_HDMI
POLYSW-1D1A6V-9-GP-U
69.48001.081
2ND = 69.50011.081

HDMI CONN

5V_HDMI
SCD1U16V2KX-3DLGP C5702
HDMI1
+5V_POWER
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND
HDMI_SCL_CON
HDMI_SDA_CON
SKT-HDMI23-211-GP
022.10025.0421
2nd = 022.10025.0411
3rd = 022.10025.0401

3D3V_S0
HDMI_HPD_B R5710 1 150KR2F-L-GP HDMI_DET_CON
Q5703 LMBT3904LT1G-GP
84.T3904.H11
2nd = 084.03904.0I11
3rd = 84.03904.111
HDMI_HPD_CPU R5712 1 0R0402-PAD HDMI_HPD_E
R5709 100KR2J-1-GP
R5711 200KR2F-L-GP

EMI Request:

HDMI_DDI_TX_CON_P0 ED5704 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N0 ED5705 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_P1 ED5706 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N1 ED5707 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_P2 ED5708 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N2 ED5709 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_P3 ED5710 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DDI_TX_CON_N3 ED5711 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_DET_CON ED5712 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_SCL_CON ED5713 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF
HDMI_SDA_CON ED5714 PESD5V0H1BSFYL-GP-U 083.5V0H1.00AF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: Custom
Document Number: Mockingbird_CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 57 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	*Mockingbird_CML*	*SC*

Date: Monday, December 09, 2019 Sheet 58 of 105

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	*Mockingbird_CML*	*SC*

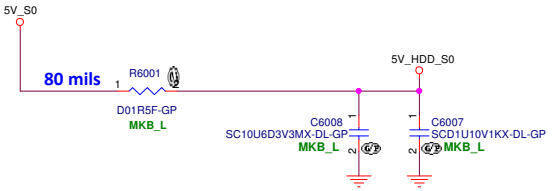
Date: Monday, December 09, 2019 Sheet 59 of 105

SSID = HDD

HDD

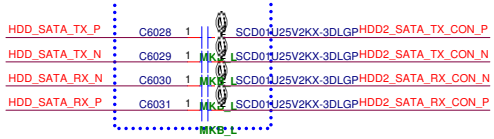
70 FFS_INT2_Q
16 HDD_DEVSLP
16 HDD_SATA_TX_P
16 HDD_SATA_TX_N
16 HDD_SATA_RX_P
16 HDD_SATA_RX_N
18 HDD_DET#

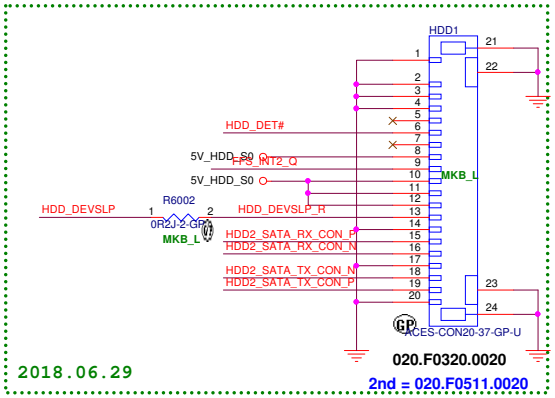
HDD POWER



SATA HDD Connector

COLAY WITH:R1611/R1612/R1607/R1608





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF_HDD/ODD

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 60 of 105

SSID = WLAN

PCIE

16 WLAN_PCIE_TX_N
16 WLAN_PCIE_TX_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P

PCIE_CLK

18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
18 WLAN_CLKREQ_CPU_N

USB2.0

16 BT_USB20_P
16 BT_USB20_N

Single end

3 BLUETOOTH_EN
21 WIFI_RF_EN
17,40,62,63,66,91 PLT_RST#
18,24 SUS_CLK

Debug

24,68 HOST_DEBUG_TX

Power EN (Madesimo)

19 BT_PCMOUT_CLKREQ0
19 BT_PCMFRM_CRF_RST_N

21 CNV_WT_DN0
21 CNV_WT_DP0
21 CNV_WT_DN1
21 CNV_WT_DP1
21 CNV_WT_CLK_DN
21 CNV_WT_CLK_DP

21 CNV_WR_DN0
21 CNV_WR_DP0
21 CNV_WR_DN1
21 CNV_WR_DP1
21 CNV_WR_CLK_DN
21 CNV_WR_CLK_DP

15,20 CNV_RGI_DT_R
20 CNV_BRI_DT_R

20 CNV_BRI_RSP
20 CNV_RGI_RSP

18 JIO3_PCIE_WAKE#
18 CLKIN_XTAL_LCP_R

3D3V_S5 → R6140 D01R5F-GP → 3D3V_WLAN

1.1A

C6110 SCD1U16V2KX-3DLGP
C6106 SC10U6D3V3MX-DL-GP
C6109 SCD1U16V2KX-3DLGP

AFTE14P-GP AFTP6101 — 1 3D3V_WLAN
AFTE14P-GP AFTP6105 — 1 WLAN_CLKREQ_CPU_N
AFTE14P-GP AFTP6106 — 1 WIFI_RF_EN_R
AFTE14P-GP AFTP6107 — 1 BLUETOOTH_EN_R
AFTE14P-GP AFTP6108 — 1 PLT_RST#
AFTE14P-GP AFTP6109 — 1 BT_USB20_CON_N
AFTE14P-GP AFTP6110 — 1 BT_USB20_CON_P
AFTE14P-GP AFTP6102 — 1 JIO3_PCIE_WAKE#

3D3V_WLAN → R6141 10KR2J-3-GP DY → WIFI_RF_EN → R6114 0R2J-2-GP DY → WIFI_RF_EN_R

3D3V_WLAN → R6142 10KR2J-3-GP DY → BLUETOOTH_EN → R6113 0R2J-2-GP DY → BLUETOOTH_EN_R

WLAN1 — NGFF_KEY_E_75P — SKT-NGFF75P-164-GP

76	76	77	77
74	3_3VAUX	75	GND
72	3_3VAUX	73	RESERVED#73
70	RESERVED#70	71	RESERVED#71
68	RESERVED#68	69	GND
66	RESERVED#66	67	RESERVED#67/2ND_LANE_PERN1
64	GPIO0_NFC_RESET#/MGPIO7	65	RESERVED#65/2ND_LANE_PERP1
62	NFC_I2C_IRQ/MGPIO5	63	GND
60	NFC_I2C_SM_CLK	61	RESERVED#61/2ND_LANE_PETN1
58	NFC_I2C_SM_DATA	59	RESERVED#59/2ND_LANE_PETP1
56	W_DISABLE#1	57	GND
54	RESERVED#54/W_DISABLE#2	55	PEWAKE0#
52	PERST0#	53	CLKREQ0#
50	SUSCLK_32KHZ	51	GND
48	COEX1	49	REFCLKN0
46	COEX2	47	REFCLKP0
44	COEX3	45	GND
42	CLINK_CLK	43	PERN0
40	CLINK_DATA	41	PERP0
38	CLINK_RESET	39	GND
36	UART_CTS	37	PETN0
34	UART_RTS	35	PETP0
32	UART_TX	33	GND
22	UART_RX	23	SDIO_RESET
20	UART_WAKE	21	SDIO_WAKE
18	GND	19	SDIO_DAT3
16	LED#2	17	SDIO_DAT2
14	PCM_OUT	15	SDIO_DAT1
12	PCM_IN	13	SDIO_DAT0
10	PCM_SYNC	11	SDIO_CMD
8	PCM_CLK	9	SDIO_CLK
6	LED#1	7	GND
4	3_3VAUX	5	USB_D-
2	3_3VAUX	3	USB_D+
NP2	NP2	1	GND
		NP1	NP1

3D3V_WLAN → R6106 10KR2J-3-GP → CLKIN_XTAL_LCP_R
WIFI_RF_EN_R
BLUETOOTH_EN_R
PLT_RST#
SUS_CLK → R6135 33R2J-2-GP → SUSCLK_WLAN
CNV_RGI_RSP → R6109 22R2J-2-GP → CNV_RGI_RSP_R → CNV_RGI_DT_R
CNV_BRI_RSP → R6118 22R2J-2-GP → CNV_BRI_RSP_R
BT_PCMOUT_CLKREQ0
BT_PCMFRM_CRF_RST_N
3D3V_WLAN → R6134 75KR2F-GP, R6133 71K5R2F-1-GP

WLAN_PCIE_TX_CON_N → C6107 SCD1U16V2KX-3DLGP → WLAN_PCIE_TX_N
WLAN_PCIE_TX_CON_P → C6108 SCD1U16V2KX-3DLGP → WLAN_PCIE_TX_P

062.10003.0B11
2nd = 062.10007.0371
3rd = 062.10007.0511

BT_USB20_CON_P — R6111 0R0402-PAD — BT_USB20_P
BT_USB20_CON_N — R6110 0R0402-PAD — BT_USB20_N

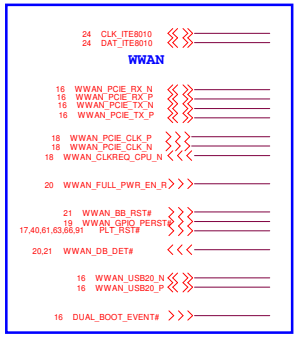
1D8V_S5 → R6115 20KR2J-L2-GP → CNV_BRI_DT_R

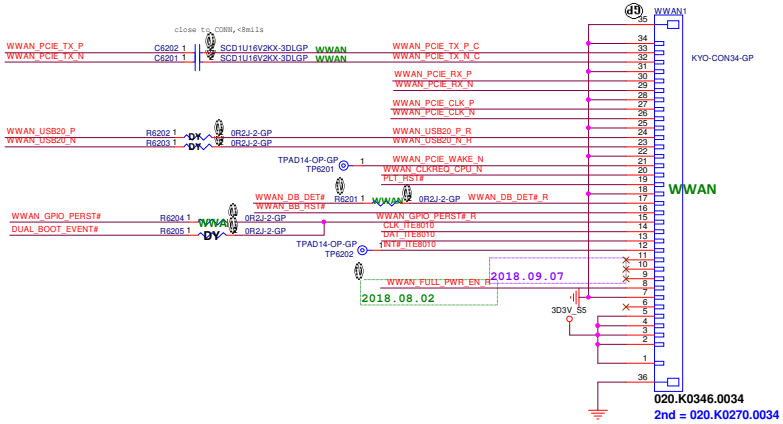
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN
Size: A3
Document Number: Mockingbird_CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 61 of 105

SSID = WWAN





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

Size	Document Number	Rev
A2	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 62 of 105

SSID = M.2 SSD

18 SSD_CLKREQ_CPU_N
17,40,61,62,63,66,91 PLT_RST#
16 SSD_DEVSLP
18 SSD_CLK_CPU_P
18 SSD_CLK_CPU_N
16 SSD_PCIE_TX_P
16 SSD_PCIE_TX_N
16 SSD_PCIE_RX_N
16 SSD_PCIE_RX_P
16 SSD_PCIE_TX_P3
16 SSD_PCIE_TX_N3
16 SSD_PCIE_RX_P3
16 SSD_PCIE_RX_N3
16 SSD_PCIE_TX_P2
16 SSD_PCIE_TX_N2
16 SSD_PCIE_RX_P2
16 SSD_PCIE_RX_N2
16 SSD_PCIE_TX_P1
16 SSD_PCIE_TX_N1
16 SSD_PCIE_RX_P1
16 SSD_PCIE_RX_N1
16 M2_SSD_PEDET
64 M2_PCIE_LED#
24 SSD_SCP#

SSD M.2 CONN

SSD1
SKT-NGFF75P-224-GP
062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21

PCIE:1 SATA:0

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-12.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

M.2 SSD2

16 SSD_PCIE_TX_P9
16 SSD_PCIE_TX_N9
16 SSD_PCIE_RX_N9
16 SSD_PCIE_RX_P9
16 SSD_PCIE_TX_P10
16 SSD_PCIE_TX_N10
16 SSD_PCIE_RX_P10
16 SSD_PCIE_RX_N10
16 SSD_PCIE_TX_P11
16 SSD_PCIE_TX_N11
16 SSD_PCIE_RX_P11
16 SSD_PCIE_RX_N11
16 SSD_PCIE_TX_P12
16 SSD_PCIE_TX_N12
16 SSD_PCIE_RX_P12
16 SSD_PCIE_RX_N12
18 SSD_CLK_CPU_P_3
18 SSD_CLK_CPU_N_3
18 CLK_PCIE_NVME_REQ3#
17,40,61,62,63,66,91 PLT_RST#
16 SSD2_DEVSLP
16 M2_SSD2_PEDET

SSD M.2 CONN

SSD2
SKT-NGFF75P-224-GP
062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21

0618 For Layout

PCIE:1 SATA:0

<Core Design>

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: mSATA		
Size: A2	Document Number: Mockingbird_CML	Rev: SC
Date: Monday, December 09, 2019	Sheet 63 of 105	

SSID = Power BTN

24 KBC_PWRBTN#

66 KBC_PWRBTN#_R

Power button

KBC_PWRBTN#_R

ED6401 AZ5725-01FDR7G-GP

DY 83.05725.0A0

0614 Layout HT

KBC_PWRBTN# R6419 0R0402-PAD KBC_PWRBTN#_R

EC6403 DY SC1KR50V2KX-1DLGP

G6401 GAP-OPEN

G6402 GAP-OPEN

Layout note:
G6401 place to buttom
G6402 place to top

SSID = Battery LED

Low actived from KBC GPIO

24,66 LED_MASK#

24 CHG_AMBER_LED#

24 BATT_WHITE_LED#

R6408 0R0402-PAD

Q6410 PJE8408-R1-00001-GP

DY 084.08408.0031

CHG_AMBER_LED# CHG_AMBER_LED#_Q

LED_MASK#

Q6411 PJE8408-R1-00001-GP

DY 084.08408.0031

BATT_WHITE_LED#_Q BATT_WHITE_LED#

R6409 0R0402-PAD

0806 Layout HT

0614 Layout HT

Q6403 LDTA144VLT1G-GP

084.00144.0B11

2nd = 84.00144.P11

5V_S5

AMBER_LED_BAT

R6407 499R2F-2-GP

DY EC6402 SCD1U25V2KX-1-DL-GP

BAT_AMBER

LED1 MKB_L LED-YW-5-GP

083.1212A.0070

2nd = 083.00327.0070

Battery LED1 (AMBER_LED)

0614 Layout HT

Q6404 LDTA144VLT1G-GP

084.00144.0B11

2nd = 84.00144.P11

WHITE_LED_BAT

R6406 549R2F-GP

DY EC6404 SCD1U25V2KX-1-DL-GP

BAT_WHITE

LED2 MKB_NV/HELLCAT LED-YW-5-GP

083.1212A.0070

2nd = 083.00327.0070

Battery LED2 (WHITE_LED)

SSID = HDD LED

24 MASK_SATA_LED#

16 SATA_LED#

63 M2_PCIE_LED#

SATA HDD LED
LOW actived from PCH GPIO

3D3V_S0

R6411 10KR2J-3-GP

DY R6415 10KR2J-3-GP

MASK_SATA_LED#

1D8V_S0

R6403 10KR2J-3-GP

Vth(max)=1V

Q6409 PJA138KA-GP

084.00138.0A31

2nd = 084.00139.0A31

BATT_WHITE_LED#

0614 Layout HT

D6401 RB520S30-GP

SATA_LED# SATA_LED#_D

83.R2003.A8M

2ND = 083.52030.008F

D6402 RB520S30-GP

M2_PCIE_LED#

83.R2003.A8M

2ND = 083.52030.008F

SSID = M-BIST

17 PM_RSMRST#

24 M_BIST

24,44 HW_ACAV_IN

PM_RSMRST# R6418 0R2J-2-GP RSMRST#_R

3D3V_S5

R6414 330KR2F-L-GP

DY R6404 2MR2F-GP

M_BIST

HW_ACAV_IN D6403 RB520S30-GP

83.R2003.A8M

2nd = 083.52030.008F

C6405 SC1U10V2KX-1DLGP

Q6408 LMBT3904LT1G-GP

84.T3904.H11

2nd = 084.03904.0I11

3rd = 84.03904.T11

Q6407_B

KBC_PWRBTN#

Q6407 PDTA124EU-1-GP

CHG_AMBER_LED#_Q

Q6407_C

84.00124.K1K

2nd = 084.05112.001K

3rd = 084.00024.0A1K

R6413 150R2J-L1-GP-U

BOLT 15 32bit 0822

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 64 of 105

SSID = KB

0513

24 CAP_LED#_R

20 KB_DET#

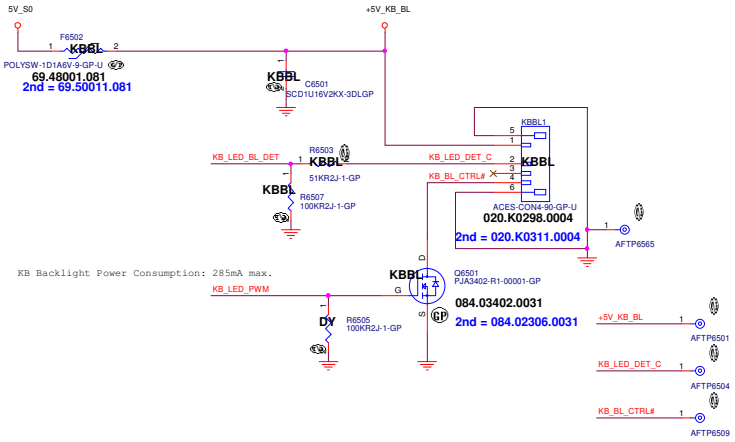
19 KB_LED_BL_DET

24 KB_LED_PWM

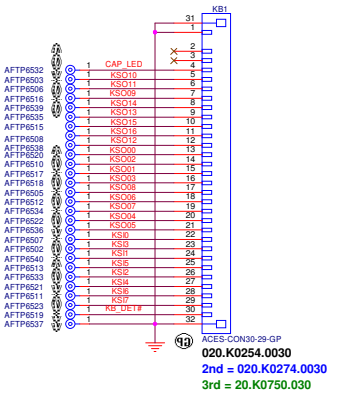
24 KSO00 KSO01 KSO02 KSO03 KSO04 KSO05 KSO06 KSO07 KSO08 KSO09 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16

24 KSI[0..7] KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

Keyboard Backlight (Reserved)

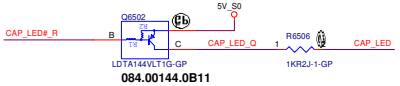


Internal Keyboard Connector



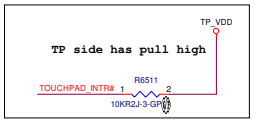
CAP LED Control

LOW actived from KBC GPIO



SSID = TPAD

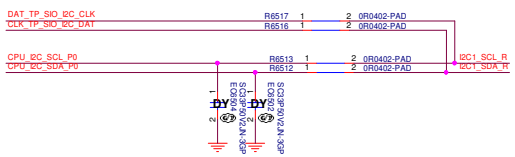
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Support PTP

PS2

I2C



0513

52 CLK_TP_SIO_I2C_DAT

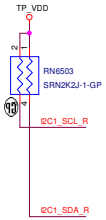
54 DAT_TP_SIO_I2C_CLK

20,66 CPU_I2C_SCL_P0

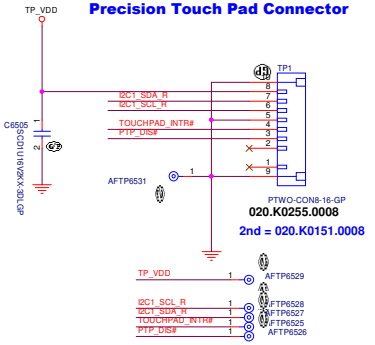
20,66 CPU_I2C_SDA_P0

3,24 TOUCHPAD_INTR#

24 PTP_DIS#



Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 65 of 105

SSID = IO Connector

Pin define by follow layout routing

IO DET

20 IO_DB_DET#_GPPG5

AUDIO

27,29 AUD_RING
27,29 AUD_SLEEVE
29 AUD_HP1_JACK_L1
29 AUD_HP1_JACK_R1
27 AUD_SENSE

CRD

16 CARD1_USB20_N
16 CARD1_USB20_P
20 SD_READ_MODE#

USB3.0

PORT1

16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P
16 USB2_USB20_N
16 USB2_USB20_P

USB CONTROL

16 USB_OC1#
24,35 USB_PWR_EN#

LAN

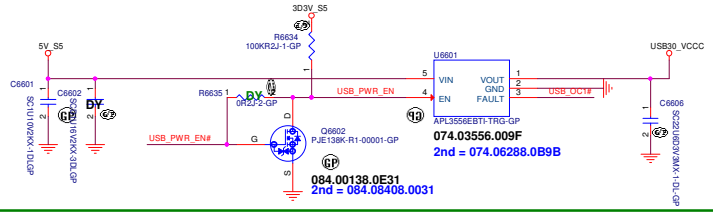
16 LAN_PCIE_RX_N
16 LAN_PCIE_RX_P
16 LAN_PCIE_TX_N
16 LAN_PCIE_TX_P
18 LAN_CLK_CPU_N
18 LAN_CLK_CPU_P
18 LAN_CLKREQ_CPU_N
24 PM_LAN_ENABLE
24 PCIE_LAN_WAKE#
16 LOM_CABLE_DETECT#

FP

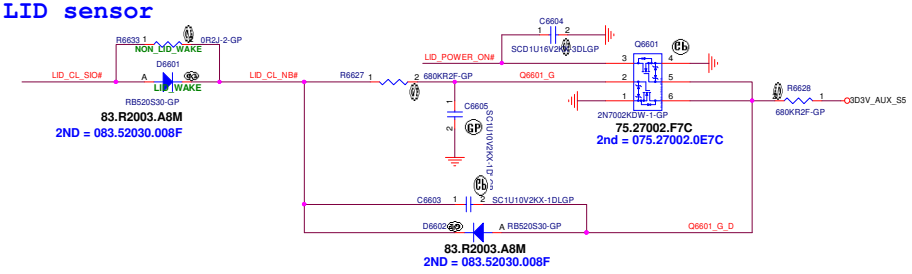
16 FP1_USB20_N
16 FP1_USB20_P
24 FPR_SCAN#
64 KBC_PWRBTN#_R
17,40,51 PM_SLP_S4#

20,24 LID_CL_SIO#
24 LID_POWER_ON#
20,24 LID_CL_SIO_TAB#
17,40,61,62,63,91 PLT_RST#
24,64 LED_MASK#
20,65 CPU_I2C_SCL_P0
20,65 CPU_I2C_SDA_P0
44 PWR_CHG_CSOP_R
44 PWR_CHG_CSON_R
55 3D3V_LCDVDD_R

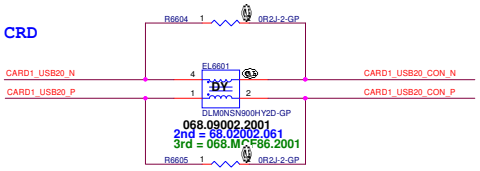
USB2.0 Power



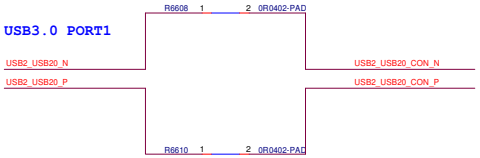
LID sensor



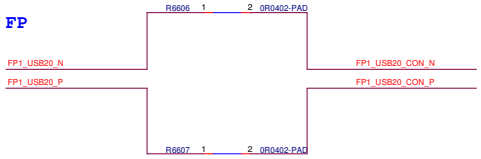
CRD



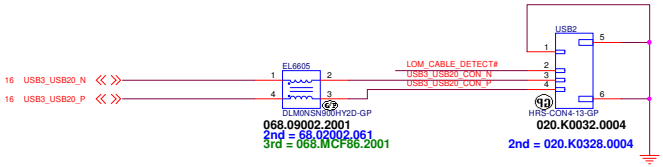
USB3.0 PORT1



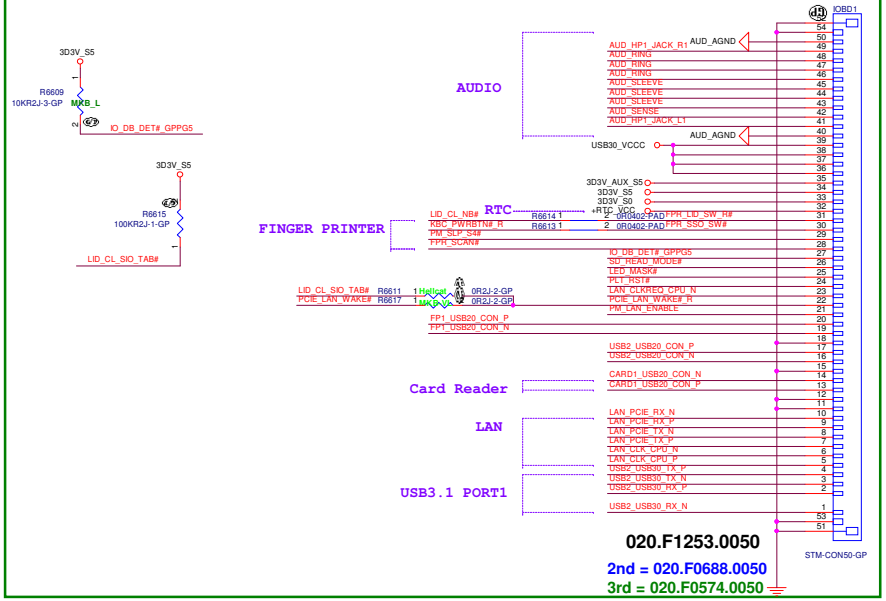
FP



USB2.0 PORT

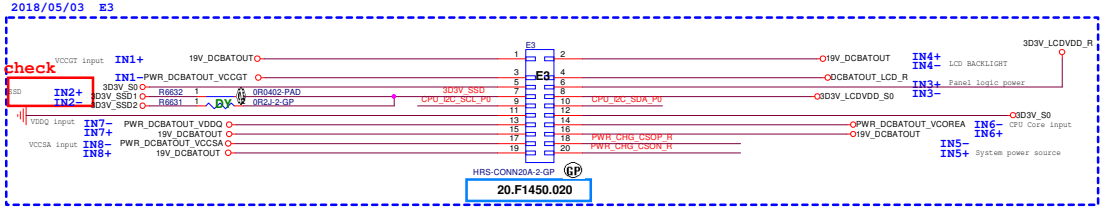


I/O Board Connector



2018/05/03 E3

0514 double check



BOLT 15 32bit 0822

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: Custom
Document Number: Mockingbird_CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 66 of 105

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Mockingbird_CML* | Rev: *SC*

Date: Monday, December 09, 2019 | Sheet 67 of 105

SSID = Debug

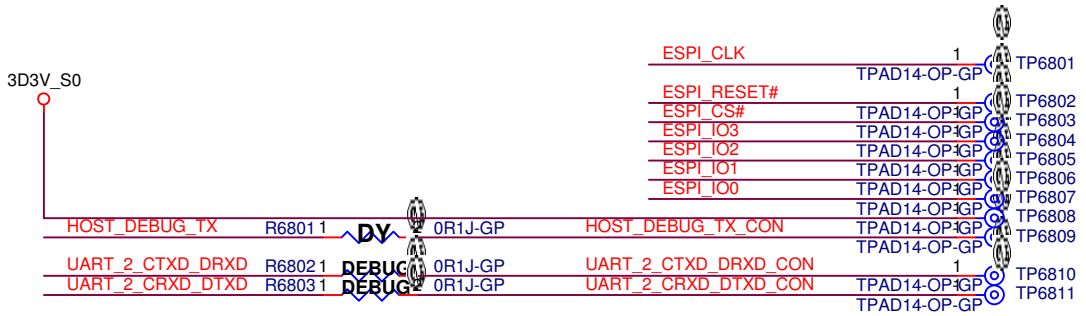
ESPI

18,24 ESPI_CLK
18,24 ESPI_RESET#
18,24 ESPI_CS#
18,24 ESPI_IO[3..0]
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0

UART

24 HOST_DEBUG_TX
20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

ESPI Debug Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Mockingbird_CML***	SC

Date: Monday, December 09, 2019 Sheet 68 of 105

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Mockingbird_CML***	***SC***

Date: Monday, December 09, 2019 Sheet 69 of 105

SSID = Free Fall sensor

Mantis Accelerometer for adaptive thermal and HDD protection

20 GSEN2_INT1_C

20,55 SENSOR_I2C_SCL

20,55 SENSOR_I2C_SDA

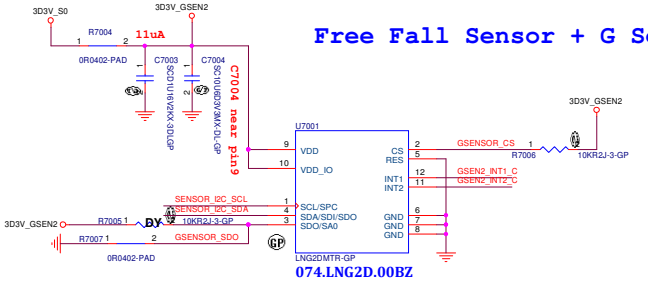
18 FFS_INT1

20 FFS_INT2

60 FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor

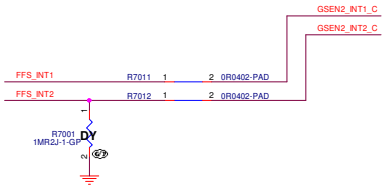


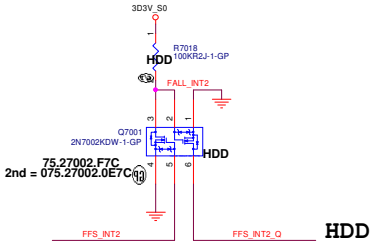
074.LNG2D.00BZ

Hellcat & MKB-L(8bit) :074.LNG2D.00BZ
MKB-N/V(12bit) :074.LIS2D.M002

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can





Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 70 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

Size	Document Number	Rev
A4	Mockingbird_CML	SC

Date: Monday, December 09, 2019 Sheet 71 of 105

SSID =TypeC

74 PD_VBUS_C_CTRL1

EC

24 TYPEC_SMBDA
24 TYPEC_SMBCLK
74 VBUS_P_CTRL
24 CCG5C_I2C_INT#

0513

MUX TUSB546

73 I2C_DATA_PD
73 I2C_CLK_PD
4,73 DP1_HPD_CPU

73 CCG5_SBU1
73 CCG5_SBU2

74 NX5P3363_FO

TYPE-C CONNECTOR

73 USB1_CC1
73 USB1_CC2
73 TOP_MUX_P_L
73 TOP_MUX_N_L
73 BOT_MUX_P_L
73 BOT_MUX_N_L
73 USB1_SBU1
73 USB1_SBU2

PCH

16 USB4_USB20_P
16 USB4_USB20_N

From System

3D3V_S5 → D7202 SBA0520Q-R1-00001-GP-U → VCC3PD_1

083.00520.0F8F

2nd = 083.05S40.001F

For debattery

3D3V_S5 → D7203 SBA0520Q-R1-00001-GP-U → VCC3PD → R7210 0R0402-PAD → VDDD

083.00520.0F8F

2nd = 083.05S40.001F

Power

VDDD: C7203 SCD1U16V2KX-3DLGP, C7204 SCD1U16V2KX-3DLGP, C7207 SC1U10V3KX-1DLGP

VCC3PD_1: C7210 SCD1U16V2KX-3DLGP, C7212 SC1U10V3KX-1DLGP

VDDD → RN7202 SRN2K2J-1-GP (I2C_CLK_PD, I2C_DATA_PD)

3D3V_S5 → R7215 2K2R2J-2-GP → CCG5C_I2C_INT#

MOD ID Settings

VDDD → R7201 51KR2J-1-GP → CCG5_MOD_ID1 → R7213 150KR2J-GP

MOD ID Settings

VDDD → R7212 100KR2J-1-GP (DY) → CCG5_MOD_ID2 → R7214 100KR2J-1-GP

VDDD → R7219 (DY) → CCG5_SWD_CLK/CCG5_I2C_CFG_EC → R7220 (DY)

VCC3PD_1 → R7217 100KR2J-1-GP; R7223 100KR1J-GP → PD_VBUS_C_CTRL1, VBUS_P_CTRL_C → Q7201 2N7002KDW-1-GP → PD_VBUS_C_CTRL1_C, VBUS_P_CTRL; R7218 100KR2J-1-GP; R7222 100KR2J-1-GP

75.27002.F7C

2nd = 075.27002.0E7C

U7201 CYPD5126-40LQXIT-16-GP

071.05126.0S03

VDDD: 31 VDDD, 32 VDDIO, 8 V5V

VCC3PD_1: 19 VSYS, SCD1U16V2KX-3DLGP 2 — 1 C7218 PD_VCCD, 33 VCCD

5V_S5 → 8 V5V

20V_VCCPD_VBUS → 22 VBUS

1, 40 CSP, CSN

CCG5C_I2C_INT#, TYPEC_SMBCLK, TYPEC_SMBDA → 15 I2C_INT_EC, 17 I2C_SCL_SCB1_EC, 16 I2C_SDA_SCB1_EC

CCG5_MOD_ID2, I2C_CLK_PD, I2C_DATA_PD → 5 I2C_INT_AR, 4 I2C_SCL_SCB2_AR, 3 I2C_SDA_SCB2_AR

CCG5_MOD_ID1, CCG5_LM → 21 SCL3/VSEL_1, 20 SDA3/VSEL_2

NX5P3363_FO, CCG5_PROCHOT# → 13 UV_OCP_TRIP/SCL_4, 14 OVP_TRIP/SDA_4

CCG5_SWD_CLK/CCG5_I2C_CFG_EC → 2 SWD_CLK/I2C_CFG, CCG5_SWD_ID → 6 SWD_IO/AR_RST

3D3V_S5 → R7225 1 (DY) 10KR2J-3-GP → R7226 1 (DY) 10KR2J-3-GP

R7216 2 — 1 NX5P3363_FO 10KR2J-3-GP

R7224 1 — 0R2J-2-GP

11 VBUS_P_CTRL, 12 VBUS_C_CTRL

9 CC1, 7 CC2 → C7221 1 SC390P50V2KX-1-GP, C7220 1 SC390P50V2KX-1-GP

23 DPLUS_SYS, 24 DMINUS_SYS → USB4_USB20_P, USB4_USB20_N

29 UART_TX, 30 UART_RX → TYPEC_SMBCLK, TYPEC_SMBDA

28 DPLUS_TOP, 27 DMINUS_TOP → TOP_MUX_P_L, TOP_MUX_N_L

26 DPLUS_BOT, 25 DMINUS_BOT → BOT_MUX_P_L, BOT_MUX_N_L

35 SBU1, 34 SBU2 → USB1_SBU1, USB1_SBU2

36 AUX_P, 37 AUX_N → CCG5_SBU1, CCG5_SBU2

38 LSTX, 39 LSRX

10 XRES#, 18 HPD → PD_XRES, CPU_DP_HPD_MUX — R7208 1 — 2 0R0402-PAD → DP1_HPD_CPU

41 GND

VDDD → R7207 10KR2F-2-GP (DY) → DP1_HPD_CPU → R7209 100KR2J-1-GP

PD_XRES → R7221 4K7R2J-2-GP → VDDD

C7219 SCD1U16V2KX-3DLGP (DY)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB PD(CYPD5126)

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 72 of 105

SSID = TYPEC MUX

DisplayPort Source

- 4 DP2_DDI_TX_P0
- 4 DP2_DDI_TX_N0
- 4 DP2_DDI_TX_P1
- 4 DP2_DDI_TX_N1
- 4 DP2_DDI_TX_P2
- 4 DP2_DDI_TX_N2
- 4 DP2_DDI_TX_P3
- 4 DP2_DDI_TX_N3

USB HOST

- 16 USB4_USB30_RX_P
- 16 USB4_USB30_RX_N
- 16 USB4_USB30_TX_P
- 16 USB4_USB30_TX_N

DisplayPort AUX

- 4 DP2_AUX_CPU_P
- 4 DP2_AUX_CPU_N

MUX I2C

- 72 I2C_CLK_PD
- 72 I2C_DATA_PD

DisplayPort HPD

- 4,72 DP1_HPD_CPU

I2C/USB MUX

- 72 CCG5_SBU1
- 72 CCG5_SBU2

TypeC CC

- 72 USB1_SBU1
- 72 USB1_SBU2
- 72 USB1_CC1
- 72 USB1_CC2
- 72 TOP_MUX_P_L
- 72 TOP_MUX_N_L
- 72 BOT_MUX_P_L
- 72 BOT_MUX_N_L

For displayport function at dead battery condition

3D3V_SS — R73031 2 0R0402-PAD — 3D3V_MUX

Slave address : 0X44

U7301 TUSB546-DCIRNQR-1-GP

071.00546.M001

DisplayPort Source

USB HOST

FLIP PIN	CTL0 PIN NAME	CTL1 PIN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

DCI		Non-DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode if unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

3A

20V_VCCPD_VBUS

USB1 — SKT-USB28-1-GP

062.10009.0681

2nd = 062.10009.M045

R7308 2MR2F-GP — R7309 2MR2F-GP

ED7302 — AZ1043-04F.R7G-GP

075.01043.0073

2nd = 075.08810.0A73

3rd = 075.73044.0003

ED7301 — AZ1043-04F.R7G-GP

075.01043.0073

2nd = 075.08810.0A73

3rd = 075.73044.0003

0614 Layout HT

ED7304 — AZ5315-02F-GP

83.05315.0A0

2nd = 075.5V0X2.0070

ED7305 — AZ5315-02F-GP

83.05315.0A0

2nd = 075.5V0X2.0070

ED7306 — AZ5315-02F-GP

83.05315.0A0

2nd = 075.5V0X2.0070

ED7307 — AZ5315-02F-GP

83.05315.0A0

2nd = 075.5V0X2.0070

EL7301 — DLM0NSN900HY2D-GP

068.09002.2001

2nd = 68.02002.061

3rd = 068.MCF86.2001

EL7302 — DLM0NSN900HY2D-GP

068.09002.2001

2nd = 68.02002.061

3rd = 068.MCF86.2001

<Core Design>

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Title: USB Type-C&MUX(TUSB546)

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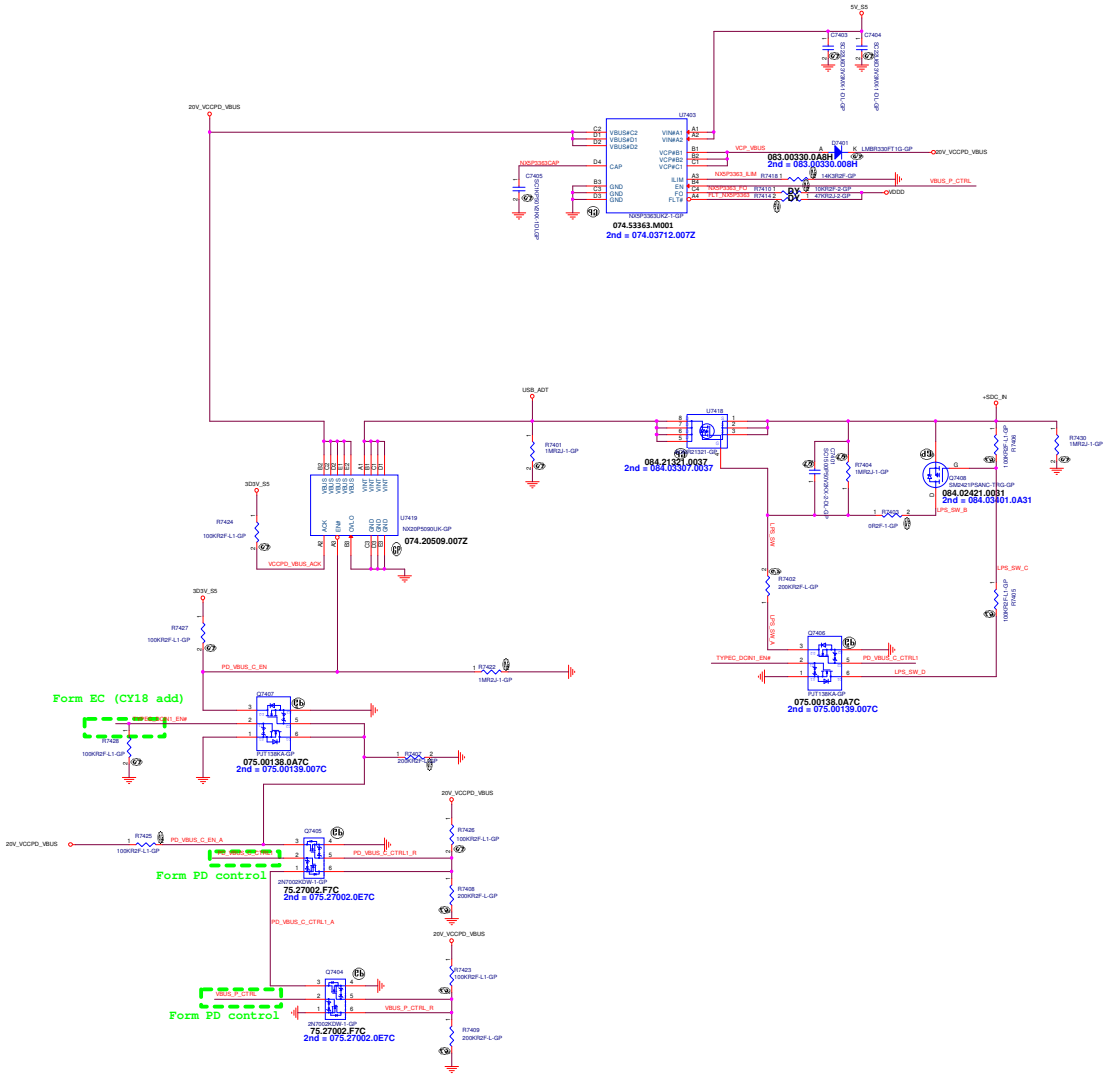
SSID = LPS

72 PD_VBUS_C_CTRL1
72 VBUS_P_CTRL
24 TYPEC_DCIN1_EN#
44 VCCPD_VBUS_ACK
72 NX5P3363_FO



<Core Design>

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Title: GPU(2/5)DIGITALOUT

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Title: *Reserved*

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Title
GPU(1/5)PEG

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<Core Design>

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Title: GPU(2/5)DIGITALOUT

Size: A2 | Document Number: Mockingbird_CML | Rev: SC

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<Core Design>

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Title: GPU(3/5)VRAM I/F

Size	Document Number	Rev
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Date: Monday, October 01, 2012 Sheet 79 of 105

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File: GPU(4/5)GPIO/STRAP

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

Date: Monday, December 02, 2013 | Sheet 79 of 100

<Core Design>

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Title: *GPU(5/5)PWR/GND*

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

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Title

GPU-VRAM1,2 (1/4)

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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Title

GPU-VRAM5,6 (3/4)

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Title

GPU-VRAM7,8 (4/4)

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File: GPU (RT8816A_VGA)

Size	Document Number	Rev
A1	Mockingbird_CML	SC

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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DISCRETE VGA POWER		
Size A0	Document Number Mockingbird_CML		Rev SC
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Title

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Title

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SSID = UnusedParts

H1 HOLE256R142-1-GP — ZZ.PAD01.V91

H5 HOLE335R178-GP — ZZ.00PAD.7F1

HS1 STF237R113H91-GP — 434.0HH0K.0001

CPU SKREW HOLE

H16 HOLE276R150-GP — ZZ.00PAD.H91
H17 HOLE276R150-GP — ZZ.00PAD.H91
H18 HOLE276R150-GP — ZZ.00PAD.H91
H19 HOLE276R150-GP — ZZ.00PAD.H91

H2 HOLE — ZZ.0HOLE.XXX
H3 HOLE — ZZ.0HOLE.XXX
H4 HOLE — ZZ.0HOLE.XXX

TYPEC SKREW HOLE

H14 HOLE256R142-1-GP — ZZ.PAD01.V91
H15 HOLE256R142-1-GP — ZZ.PAD01.V91

SSID = EMI Capacitors

Mind the voltage rating of the caps.

19V_DCBATOUT
1D2V_S3
3D3V_S0
PWR_DCBATOUT_VCOREA
PWR_DCBATOUT_VCCGT
5V_S0
5V_S5
20V_DCBATOUT
+SDC_IN
1V_CPU_CORE
1V_VCCGT
1V_VCCSA
PWR_DCBATOUT_VDDQ

20191024-EMC change

優先放在PC4705旁邊
或相對PC4705的Top層

優先放在PC4717旁邊
或相對PC4717的Top層

優先放在PC4804旁邊
或相對PC4804的Top層

SSID = RF Capacitors

Mind the voltage rating of the caps.

3D3V_S5 — 0.1uF 0402 x 5 — SA-20190807
5V_S5 — 0.1uF 0402 x 5 — SA-20190807
19V_DCBATOUT — 0.1uF 0402 x 10 — SA-20190807
1D05V_S5 — 0.1uF 0402 x 10 — SA-20190807
3D3V_S0 — SA-20190807
5V_S0 — SA-20190807

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Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: Mockingbird CML | Rev: SC
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Title

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SSID = TPM

17,40,61,62,63,66 PLT_RST#

18,24,25 SPI_CLK_ROM
15,18,24,25 SPI_SI_ROM
18,24,25 SPI_SO_ROM
18 SPI_CS_ROM_N2

20 PIRQA#

18 TPM_SPI_IRQ#

3D3V_S5 R9149 0R2J-2-GP
DY ST_TPM
3D3V_S0 R9150 TPM 0R2J-2-GP 3D3V_TPM

3D3V_TPM
TPM C9109 SC10U6D3V3MX-DL-GP
TPM C9112 SCD1U16V2KX-3DLGP
TPM C9113 SCD1U16V2KX-3DLGP

3D3V_S5_PCH
R9148 10KR2J-3-GP TPM SPI_CS2#_IC

3D3V_TPM
R9151 10KR2J-3-GP TPM
R9124 DY 0R2J-2-GP TPM_SPI_IRQ#
SPI_IRQ#_TPM2 R9123 TPM 0R2J-2-GP PIRQA#

3D3V_TPM 5mA
TPM C9104 SCD1U16V2KX-3DLGP

3D3V_S5 40mA
TPM C9106 SC10U6D3V3MX-DL-GP
TPM C9108 SCD1U16V2KX-3DLGP

SPI_SI_ROM R9133 TPM 15R1F-GP SPI_SI_ROM_TPM
SPI_SO_ROM R9132 TPM 15R1F-GP SPI_SO_ROM_TPM
SPI_CS_ROM_N2 R9130 TPM 0R1J-GP SPI_CS2#_IC
SPI_CLK_ROM R9138 TPM 15R1F-GP SPI_CLK_ROM_TPM

Close to U2501

U9101

8	VHIO	SDA/GPIO0	29 TPM_GPIO0 1 TP9101
22	VHIO	SCL/GPIO1	30 TPM_GPIO1 1 TP9102
1	VSB	PIRQ#/GPIO2	18 SPI_IRQ#_TPM2
		GPIO3	6 TPM_GPIO3 1 TP9103
		GPIO4	13 TPM_GPIO4 R9118 1 DY 2 2K2R1F-GP SPI_CS_ROM_N2
		PP/GPIO6	4 TPM_GPIO6_PP 1 TP9104
21	MOSI/GPIO7		
24	MISO		
20	SCS#/GPIO5		
19	SCLK		
PLT_RST# 17	PLTRST#		
16	GND		
23	GND		
33	GND		
U9101_2_GND 2	NC#2		
3	NC#3		
5	NC#5		

NC#7 7, NC#9 9, NC#10 10, NC#11 11, NC#12 12, NC#14 14, NC#15 15, NC#25 25, NC#26 26, NC#27 27, NC#28 28, NC#31 31, NC#32 32

TPM

R9152 0R1J-GP DY ST_TPM

NPCT750JABYX-GP
071.00750.0E03

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Title	INT IO (TPM)	
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Title: *Finger Print*

Size: A3 | Document Number: *Mockingbird_CML* | Rev: *SC*

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Title: *(Reserved)*

Size: A3 | Document Number: *Mockingbird_CML* | Rev: *SC*

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Title: *(Reserved)*

Size: A3 | Document Number: *Mockingbird_CML* | Rev: *SC*

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Size: A3 | Document Number: *Mockingbird_CML* | Rev: *SC*

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Title

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Size	Document Number	Rev
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Title

LVDS_Switch

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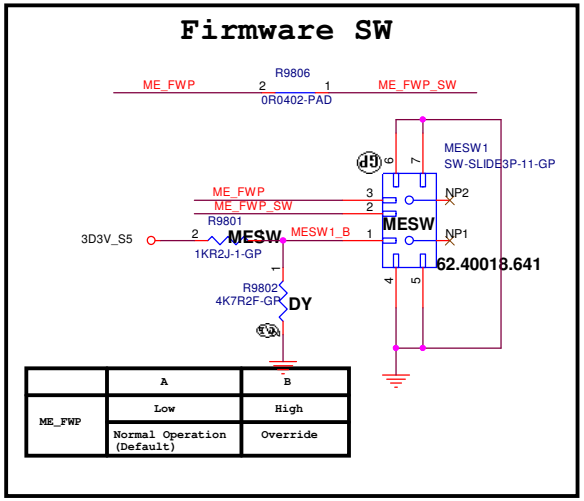
Main Func = Firmware SW

19 ME_FWP_SW
24 ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

<Core Design>

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Title: CRT_Switch

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<Core Design>

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Title

Debug (XDP debug)

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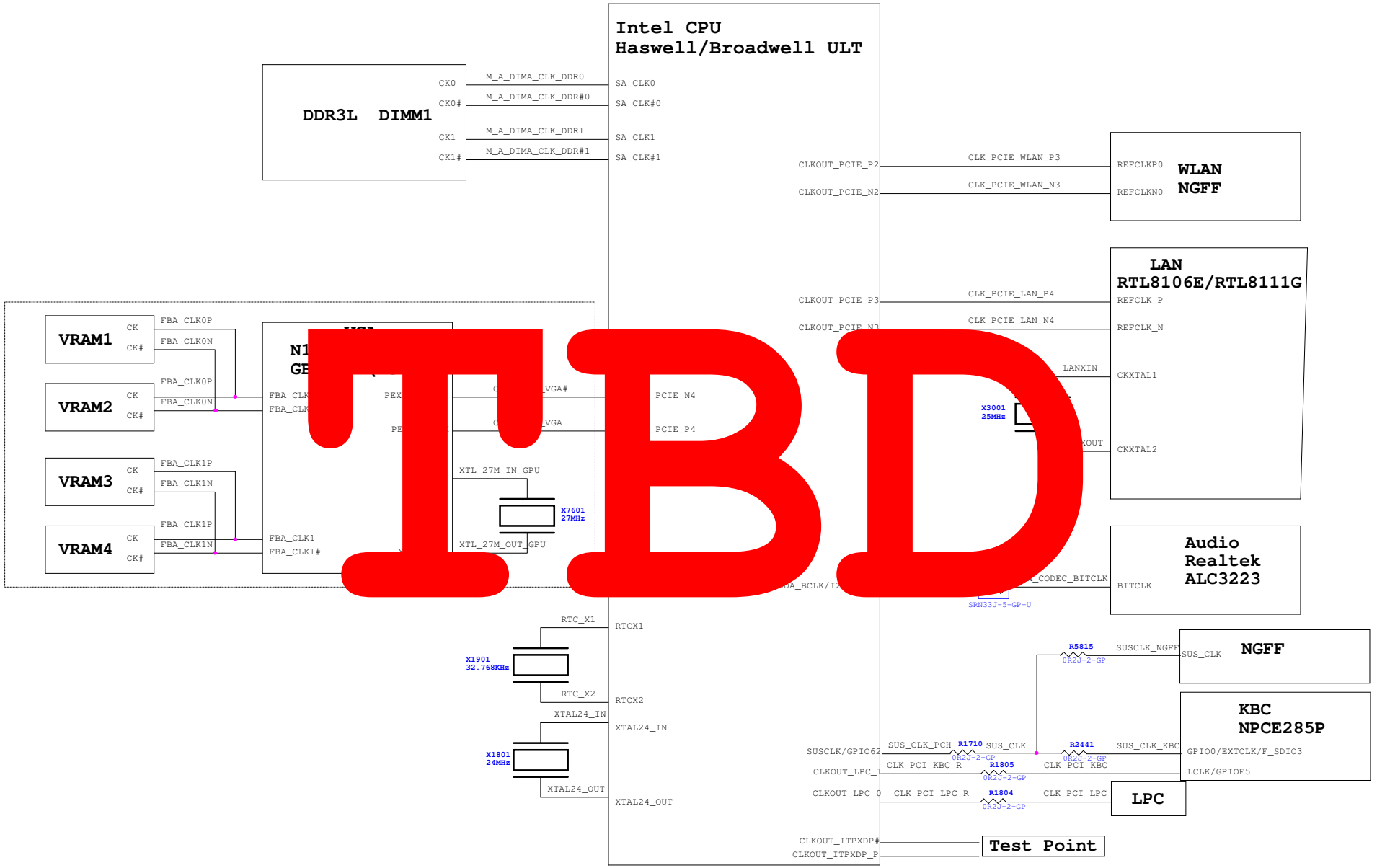
CLK Block Diagram



<Core Design>
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Title	CLK Block Diagram	
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Title: Change History

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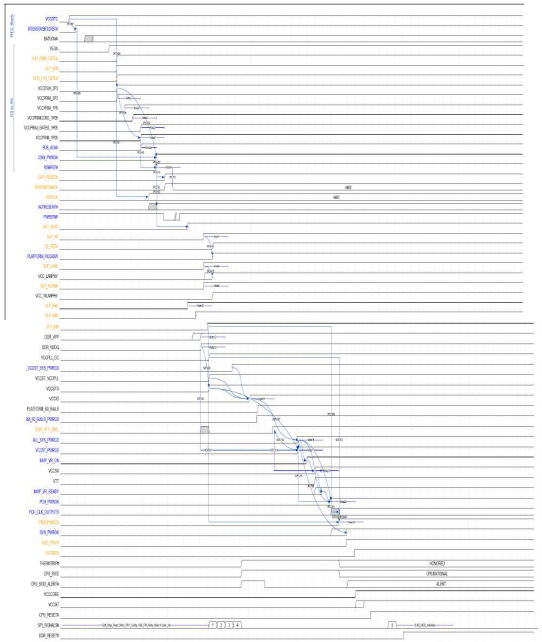
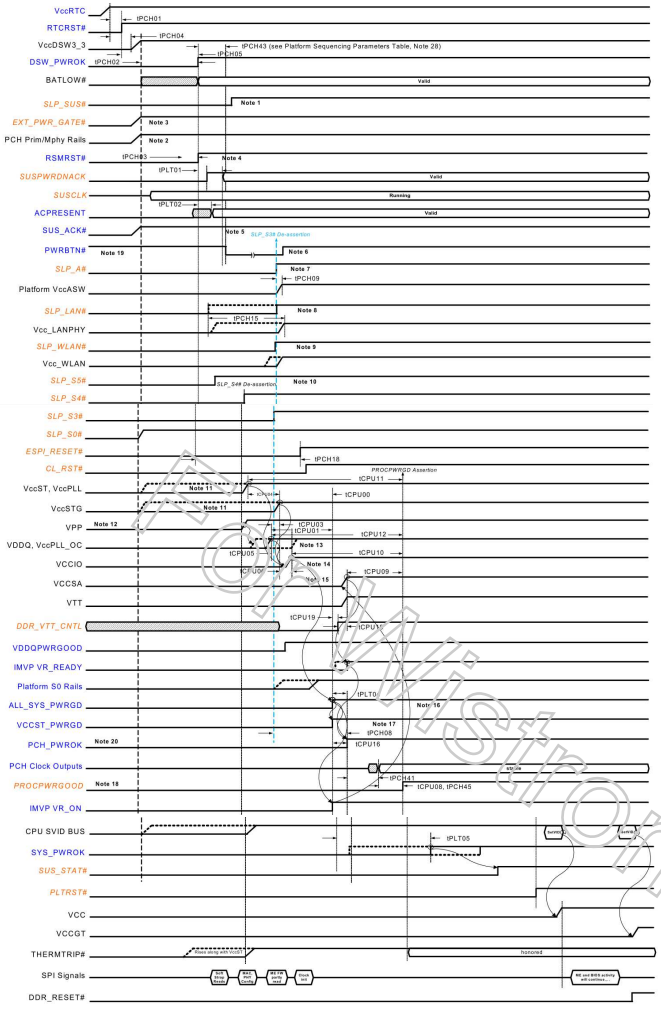
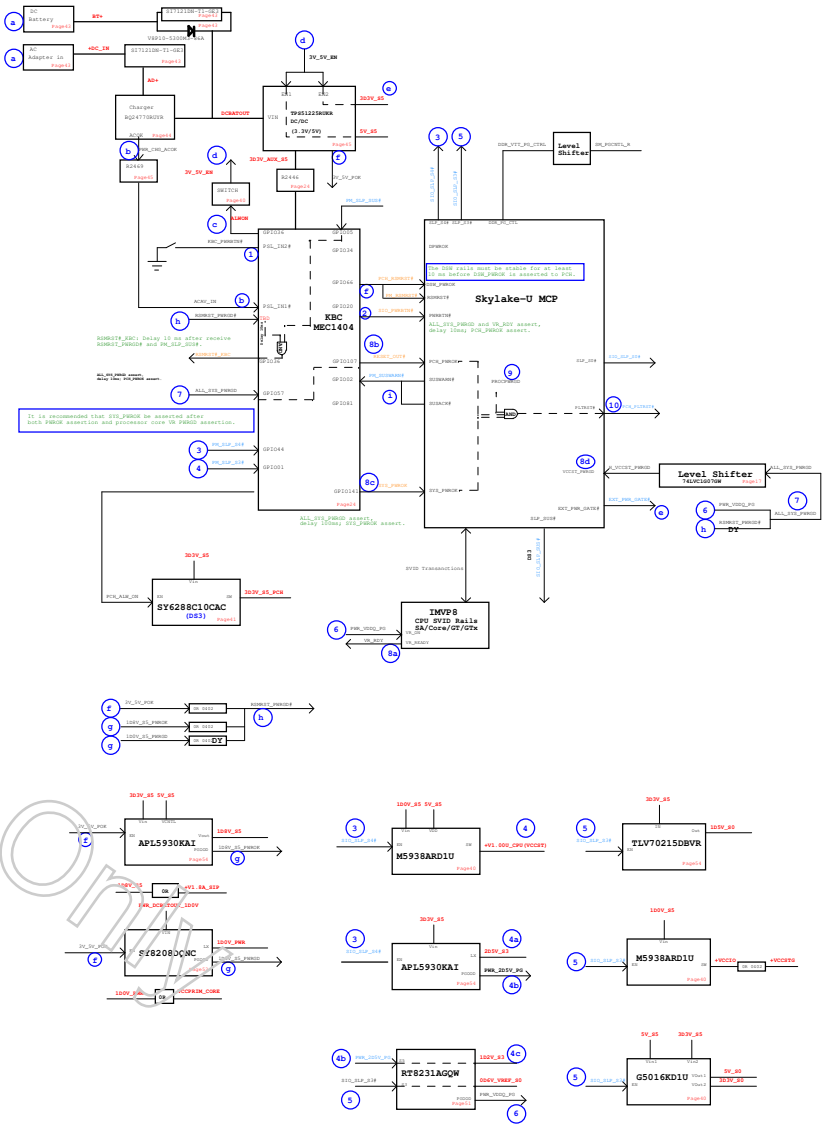
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



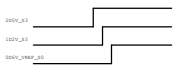
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



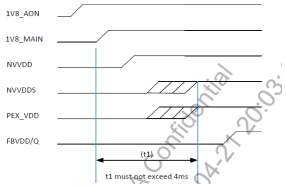
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



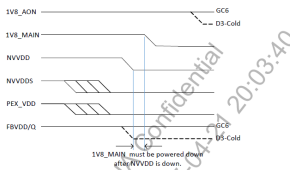
For DDR4 power sequence



NV N17S GPU Power ON sequence



NV N17S GPU Power Down sequence



a → b → c → d → e → f → g → h → i

1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 8a → 8b → 9 → 10

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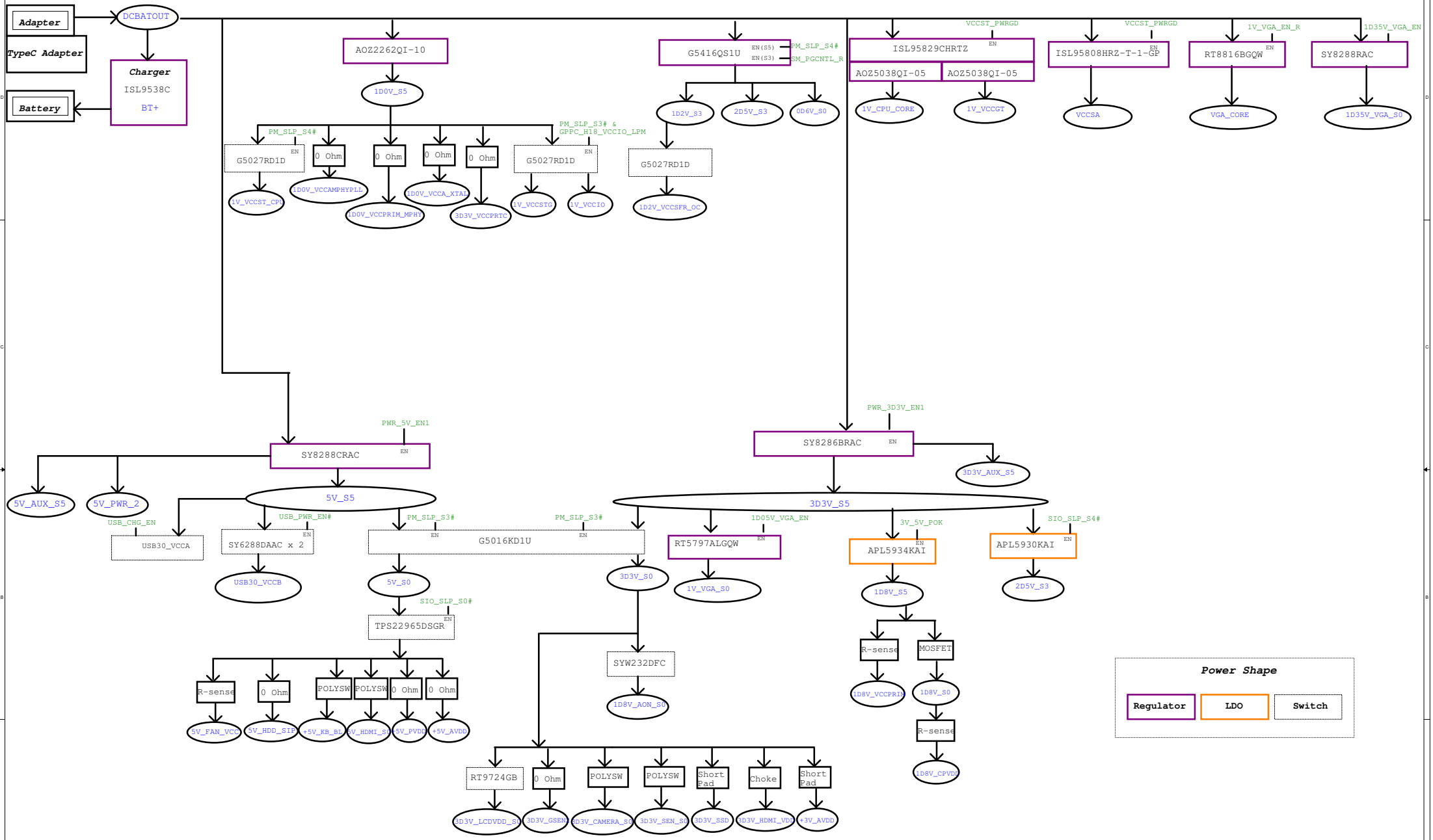
Power Sequence

Mockingbird_CML



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Title: Power Block Diagram

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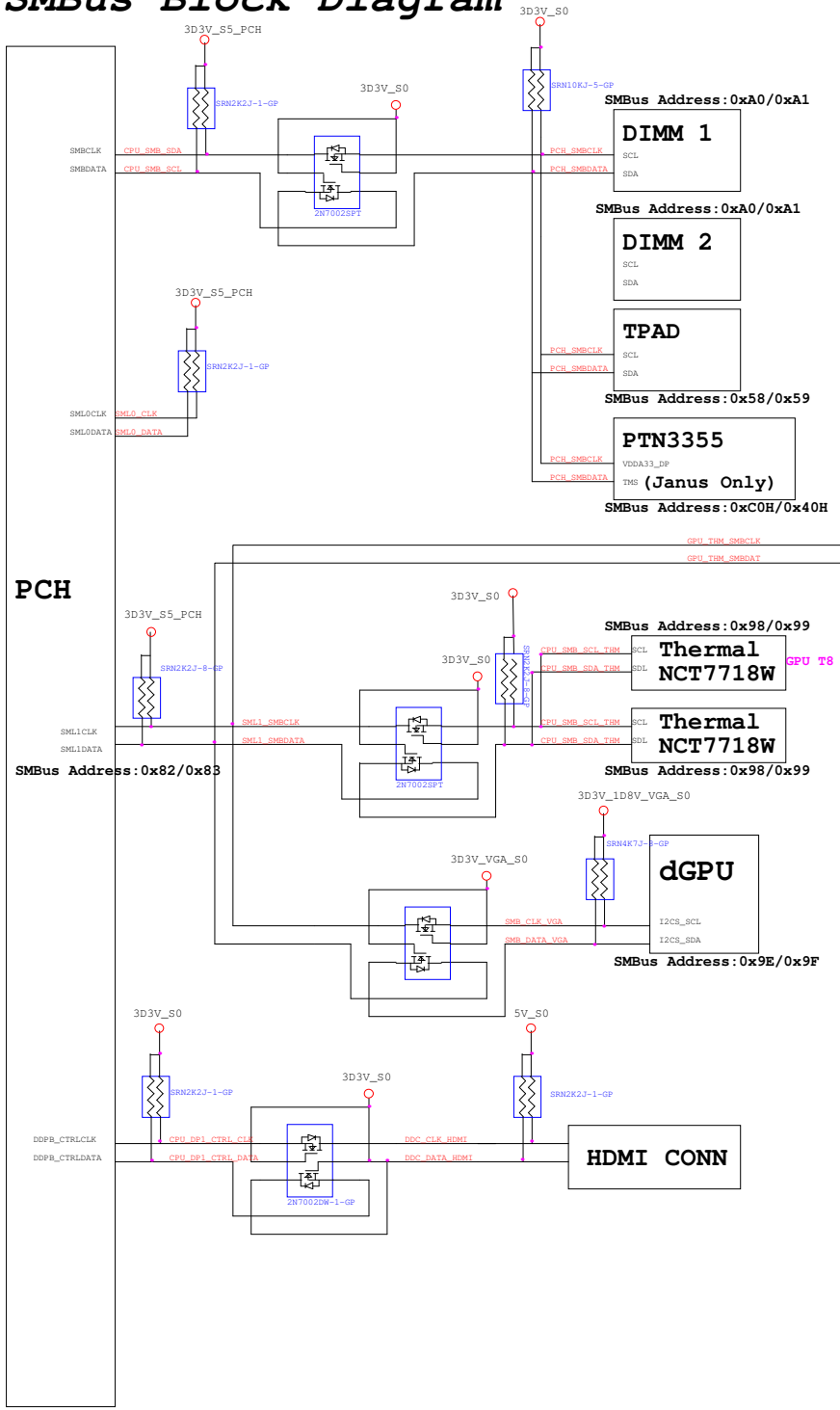
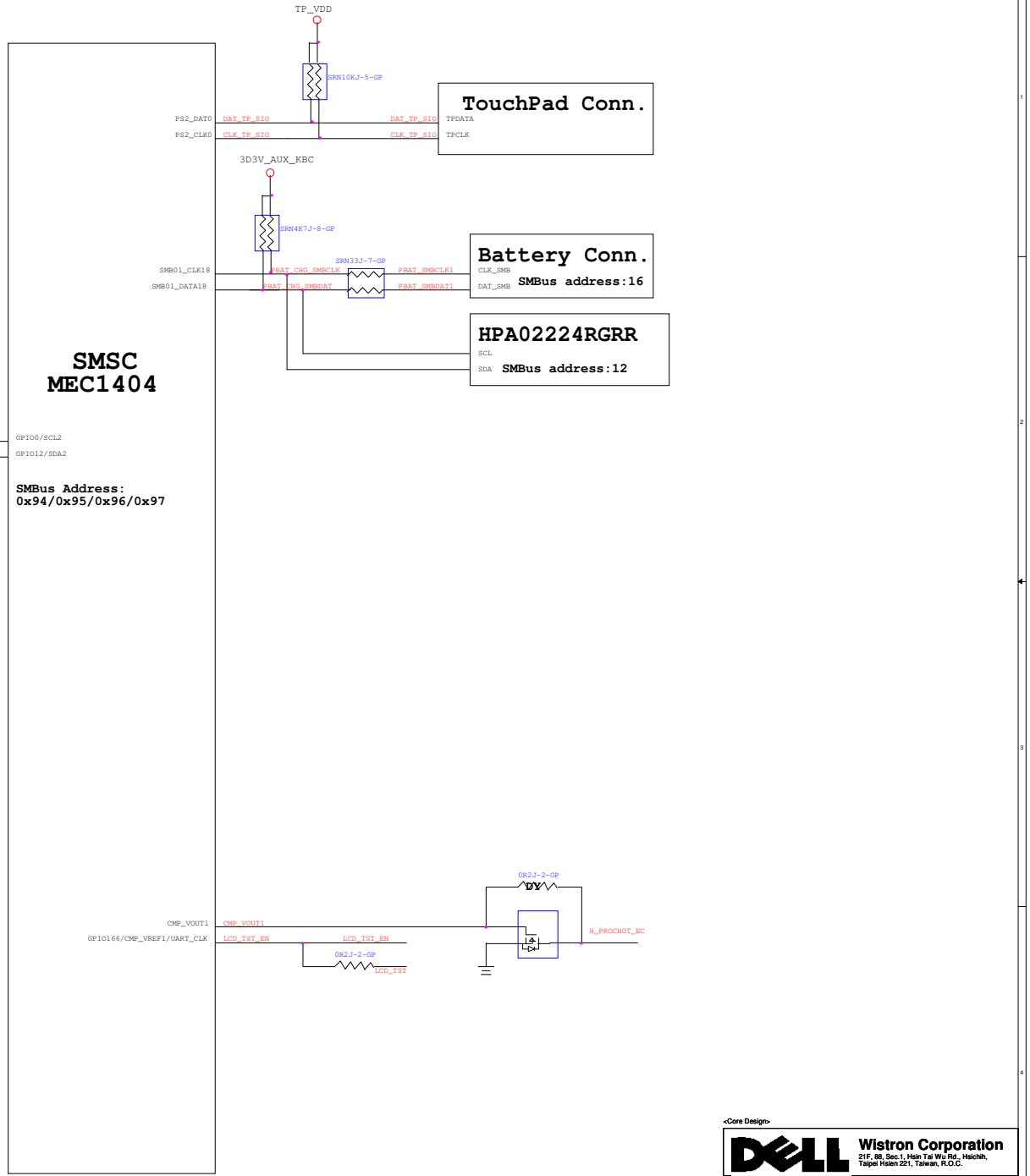
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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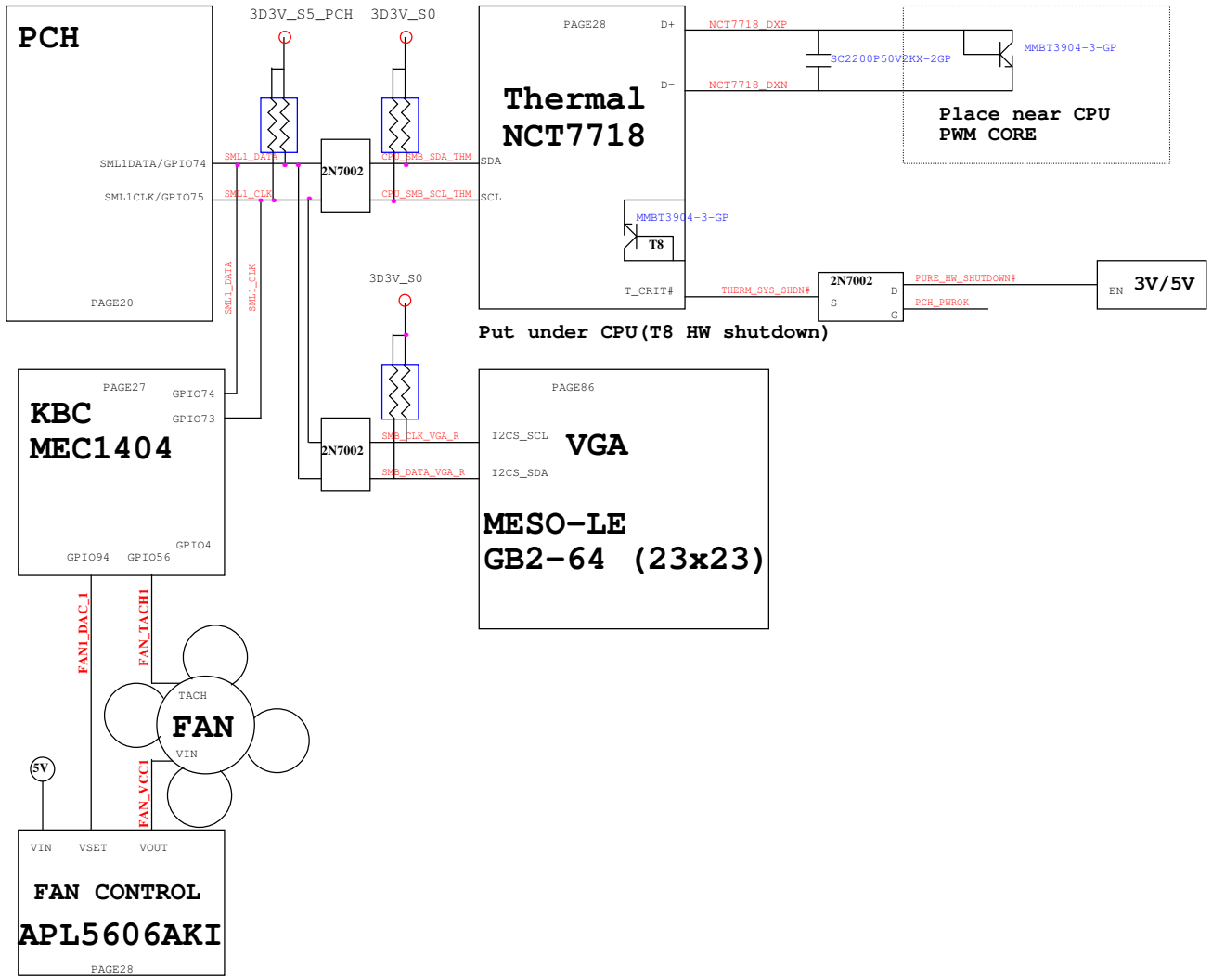
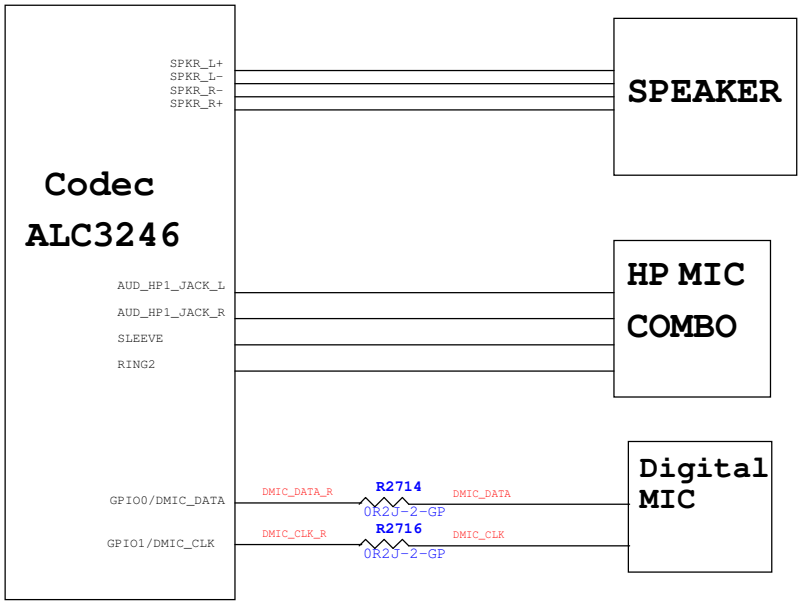
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Mockingbird_CML | Rev: SC

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