MS-7687 Version :1.0

CPU :

INTEL Sandy Bridge Processor

System Chipset :

INTEL Cougar Point Chipset

On Board Chipset :

VRM 12 -- NCP6151S52
Gigabit LAN -- RTL8111E-VB-GR-RH
HDA Codec -- Realtek ALC662
Super I/O -- SIO-NCT6776F
SPI Flash 32Mb

Main Memory :

2 Channel DDR III * 2(Max 8GB)

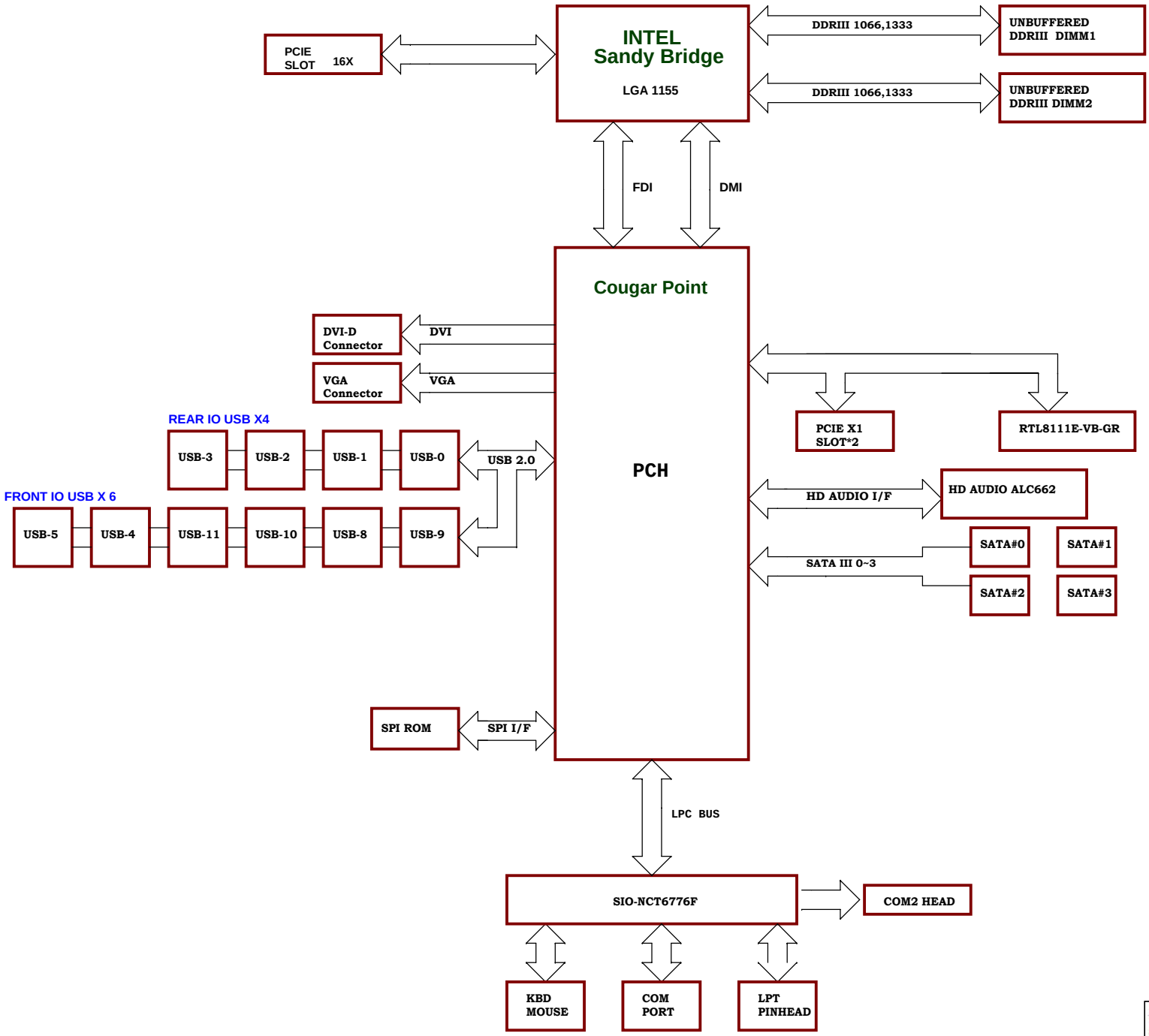
Expansion Slot :

PCI Express x16 Slot * 1
PCI Express x1 Slot * 2

lenovo

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Cover Sheet		
Size	Document Number: Lenovo IH61M	Rev: 1.0
Date: Wednesday, February 23, 2011	Sheet 1 of 33	

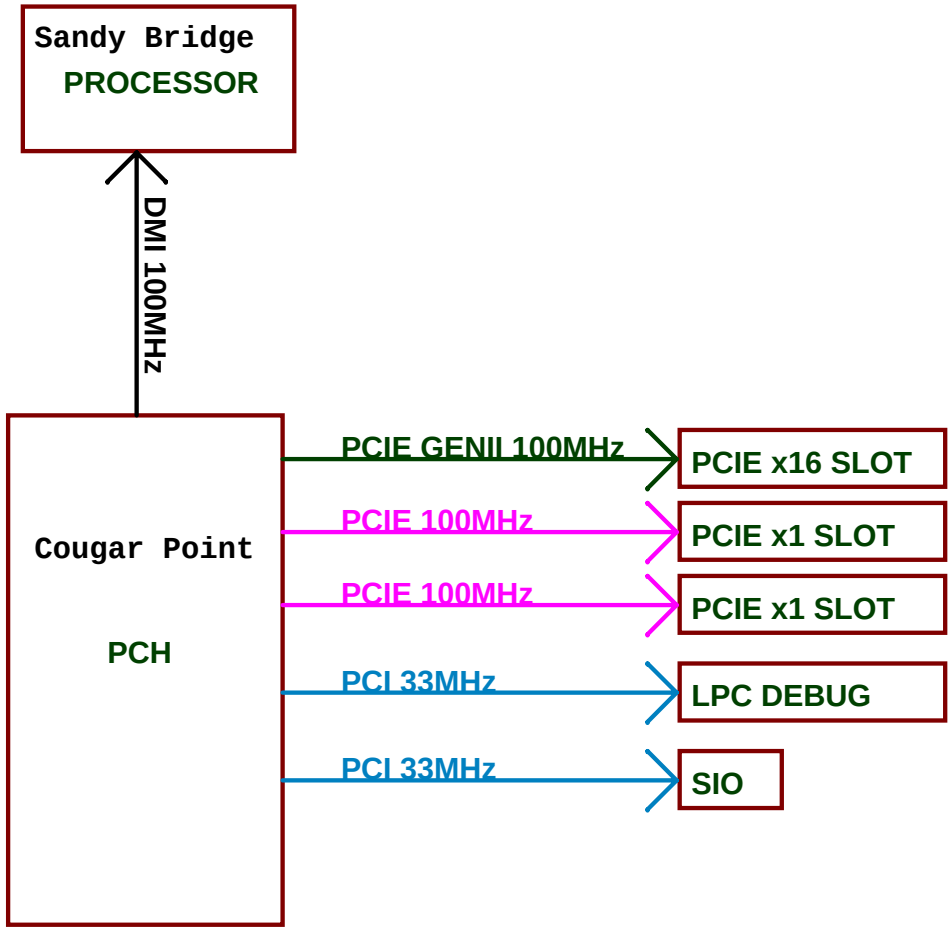


MSI MICRO-START INT'L CO.,LTD.

Title: Block Diagram

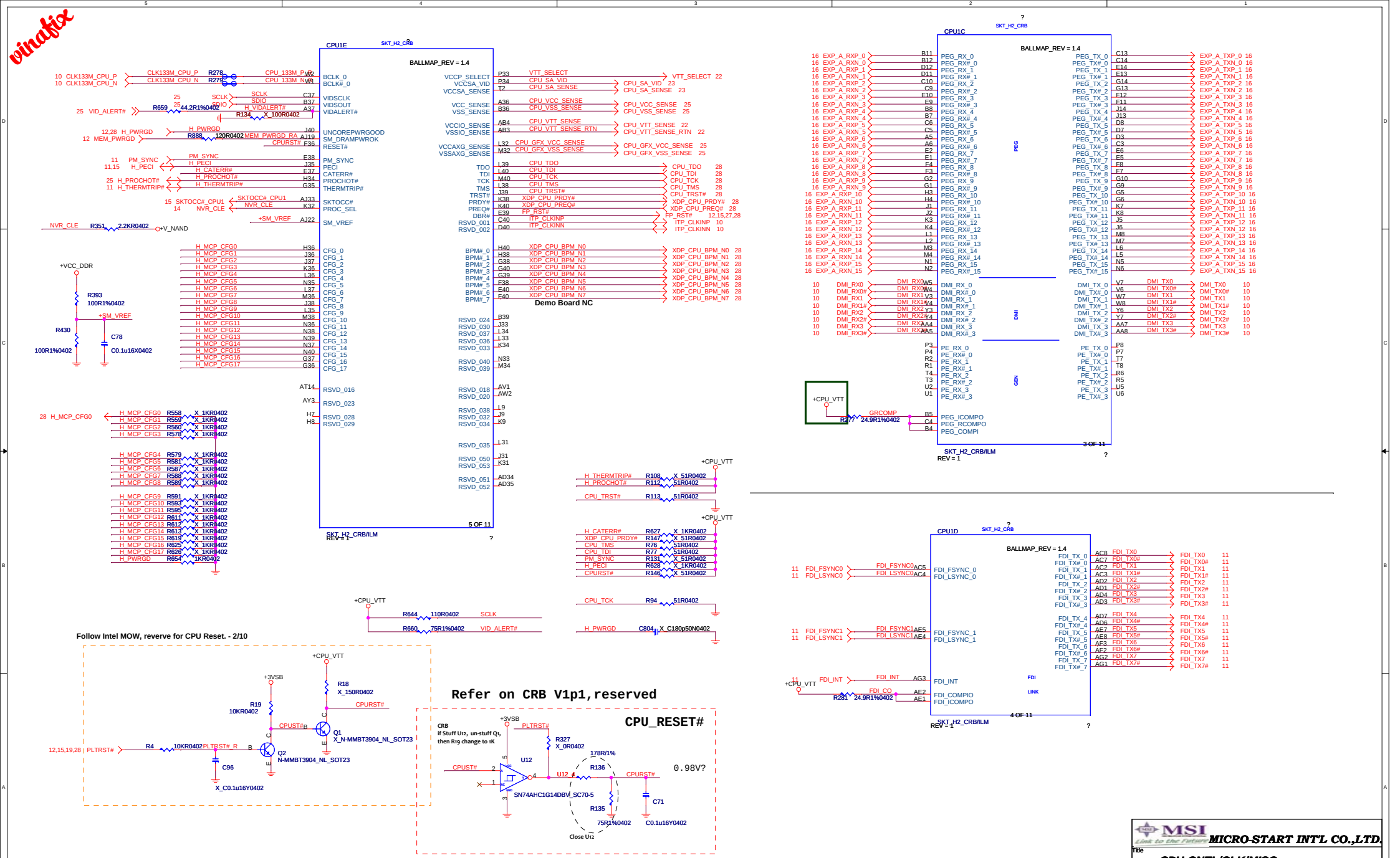
Size	Document Number	Rev
	Lenovo IH61M	1.0

Date: Wednesday, February 23, 2011 Sheet 2 of 33



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Clock MAP		
Size	Document Number: Lenovo IH61M	Rev: 1.0
Date: Wednesday, February 23, 2011	Sheet 3 of 33	

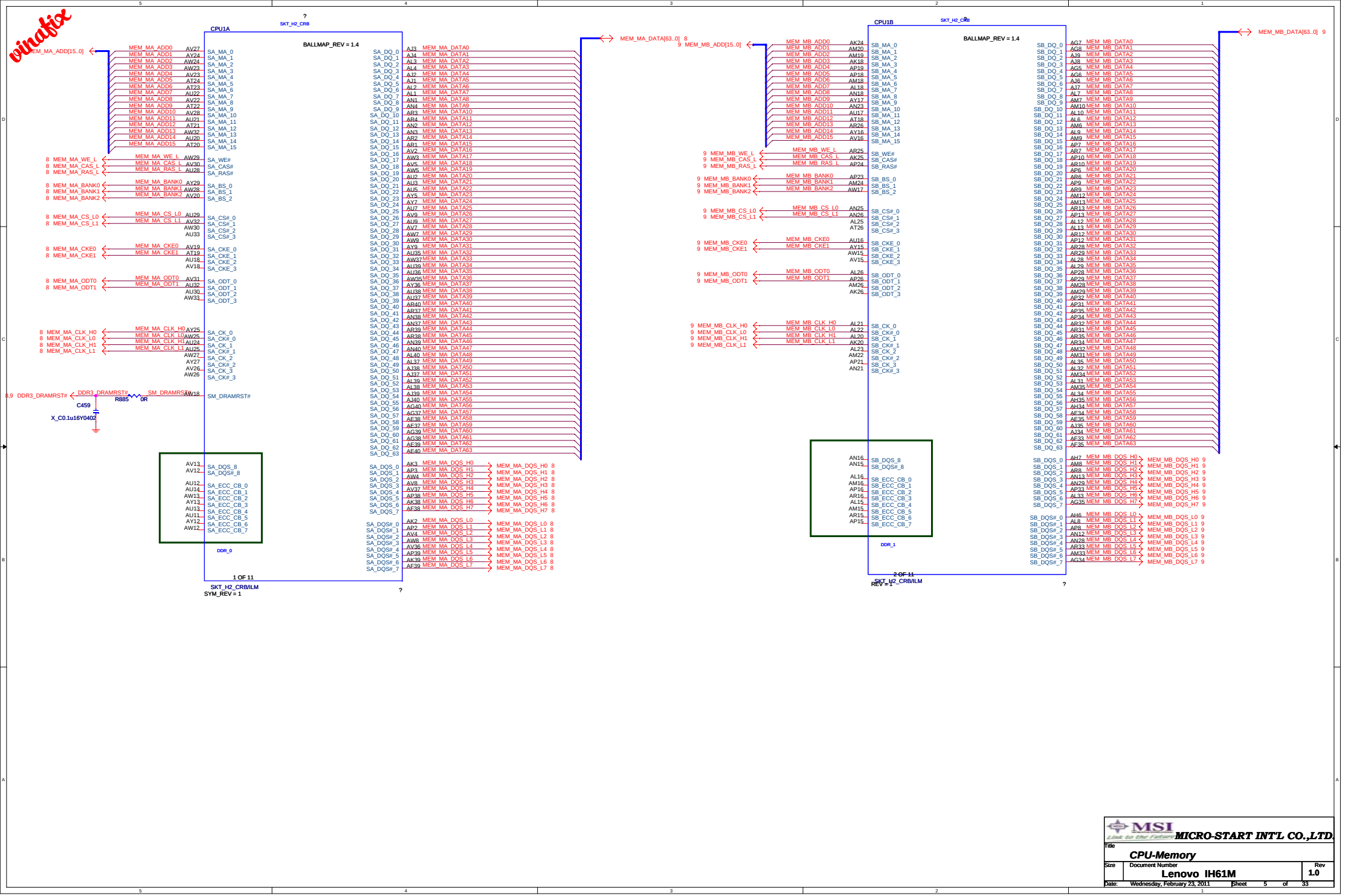


MSI MICRO-STAR INT'L CO.,LTD.

Title: CPU-CNTL/CLK/MISC

Size: | Document Number: Lenovo IH61M | Rev: 1.0

Date: Wednesday, February 23, 2011 | Sheet 4 of 33



CPU1F SKT_H2_CRB 2
BALLMAP_REV = 1.4
6 OF 11
SKT_H2_CRB/ILM
REV = 1

CPU1H SKT_H2_CRB 2
BALLMAP_REV = 1.4
8 OF 11
SKT_H2_CRB/ILM
REV = 1

CPU1G SKT_H2_CRB 2
BALLMAP_REV = 1.4
7 OF 11
SKT_H2_CRB/ILM
REV = 1

+VCCP
+CPU_VTT
+VCC_DDR
+CPU_GFX
+VCC_SA
+VCC1_8
1A
POWER

+1.5V_DDR3-Decoupling

+VCC_DDR
C199 C22u6.3X50805
C191 X_C22u6.3X50805
C200 C22u6.3X50805
CPU SOCKET CAVITY CAPS

+CPU_VTT Decoupling

+CPU_VTT
C136 C22u6.3X50805
C137 C22u6.3X50805
C152 C22u6.3X50805
C153 C22u6.3X50805
C477 C4.7u6.3X50805
C474 X_C4.7u6.3X50805
+CPU_VTT
C192 X_C22u6.3X50805
C181 X_C22u6.3X50805
C180 X_C22u6.3X50805
C169 X_C22u6.3X50805
C168 X_C22u6.3X50805
C475 C4.7u6.3X50805
CPU SOCKET CAVITY CAPS

+CPU_VCCP-Decoupling

+VCCP
C472 X_C22u6.3X50805
C471 C22u6.3X50805
C470 C22u6.3X50805
C468 X_C22u6.3X50805
C469 C22u6.3X50805
+VCCP
C135 C22u6.3X50805
C179 X_C22u6.3X50805
C178 X_C22u6.3X50805
C177 X_C22u6.3X50805
C176 X_C22u6.3X50805
+VCCP
C151 C22u6.3X50805
C167 C22u6.3X50805
C166 C22u6.3X50805
C165 C22u6.3X50805
C164 C22u6.3X50805
+VCCP
C150 C22u6.3X50805
C149 C22u6.3X50805
C148 X_C22u6.3X50805
C134 C22u6.3X50805
C133 C22u6.3X50805
C132 C22u6.3X50805
PLACE ALL 08056 CAPS INSIDE CPU SOCKET CAVITY

+VCC1_8
C658 C10u6.3X50805-RH-3
C478 C22u6.3X50805

+VCCP
C173 C22u6.3X50805
C155 C22u6.3X50805
C127 C22u6.3X50805
C120 C22u6.3X50805
C105 C22u6.3X50805

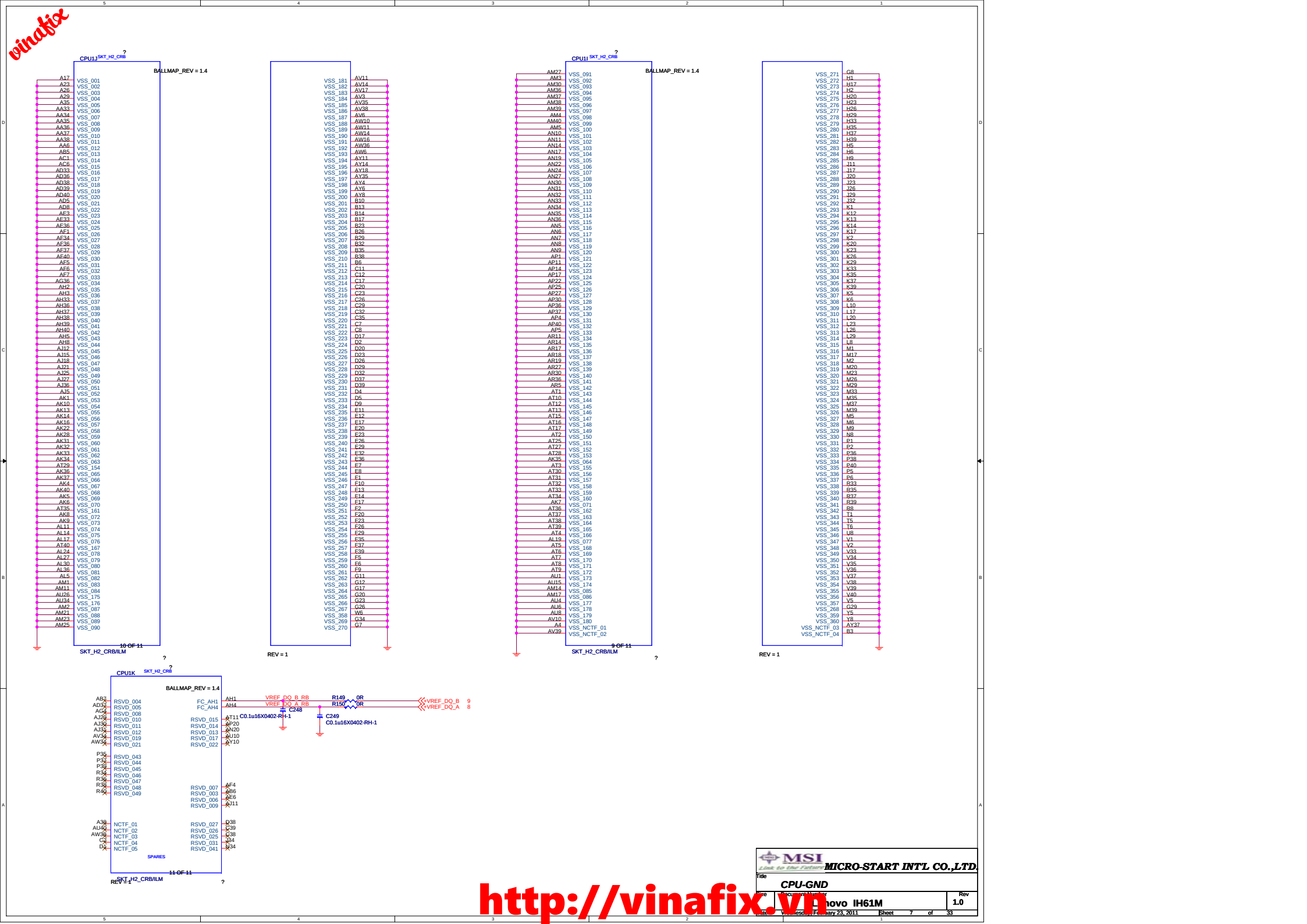
+CPU_GFX Decoupling

+CPU_GFX
C188 22uF/6.3V/X5R/0805
C198 22uF/6.3V/X5R/0805
C189 22uF/6.3V/X5R/0805
C231 22uF/6.3V/X5R/0805
+CPU_GFX
C194 22uF/6.3V/X5R/0805
C476 22uF/6.3V/X5R/0805
C473 22uF/6.3V/X5R/0805

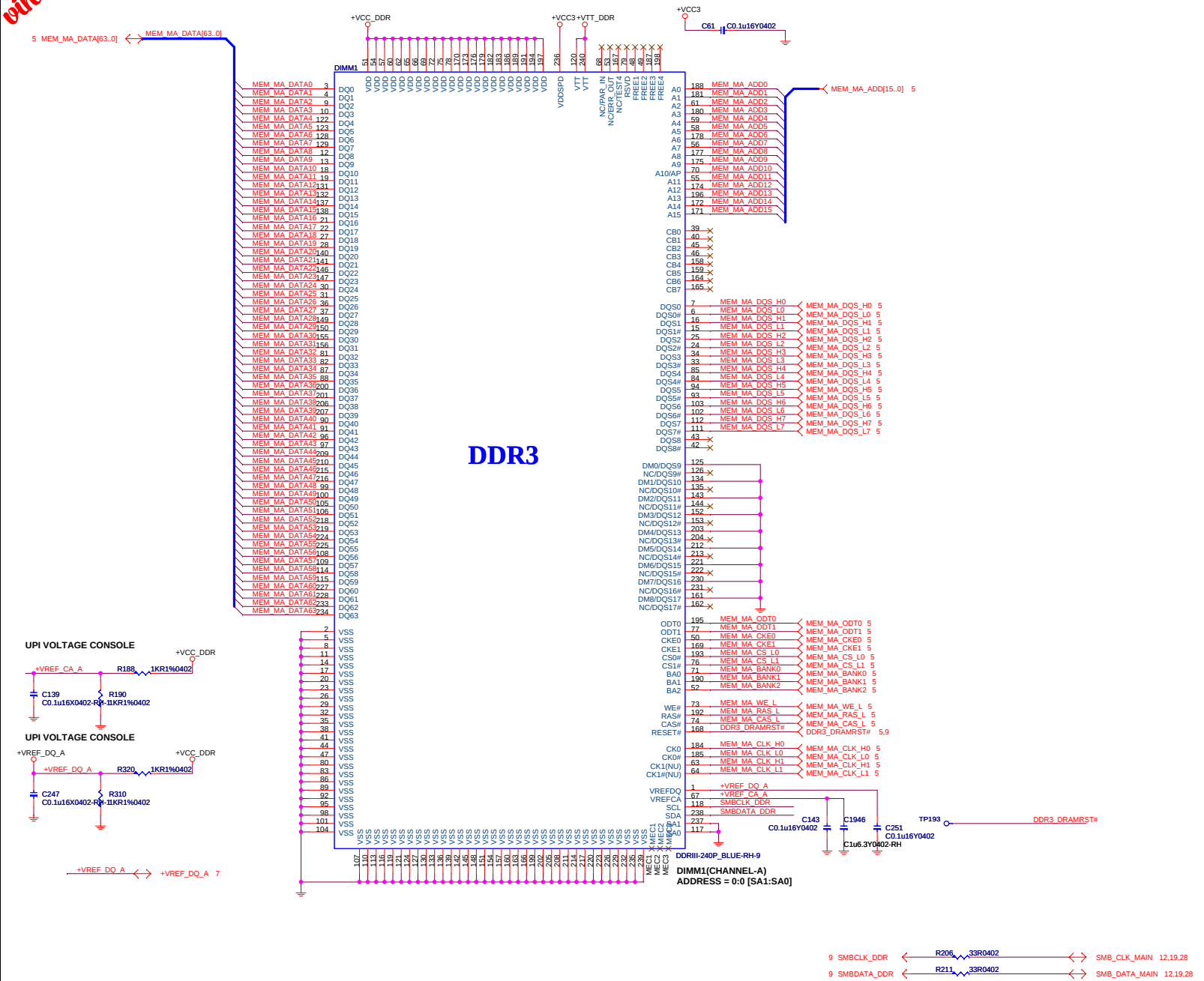
+VCC_SA
C661 C10u6.3X50805-RH-3

TP130 +VCCP
TP134 +CPU_VTT
TP131 +CPU_GFX
TP132 +VCC_DDR
TP133 +VCC1_8
TP135 +VCC_SA

MSI MICRO-START INT'L CO.,LTD.
Title: CPU-Power
Size | Document Number: Lenovo IH61M | Rev: 1.0
Date: Wednesday, February 23, 2011 | Sheet 6 of 33



DDRIII DIMM_A1



MSI MICRO-START INT'L CO.,LTD.			
Title: DDR3 Chanel-A DIMM1			
Size	Document Number: Lenovo IH61M		Rev: 1.0
Date: Wednesday, February 23, 2011	Sheet 8 of 33		

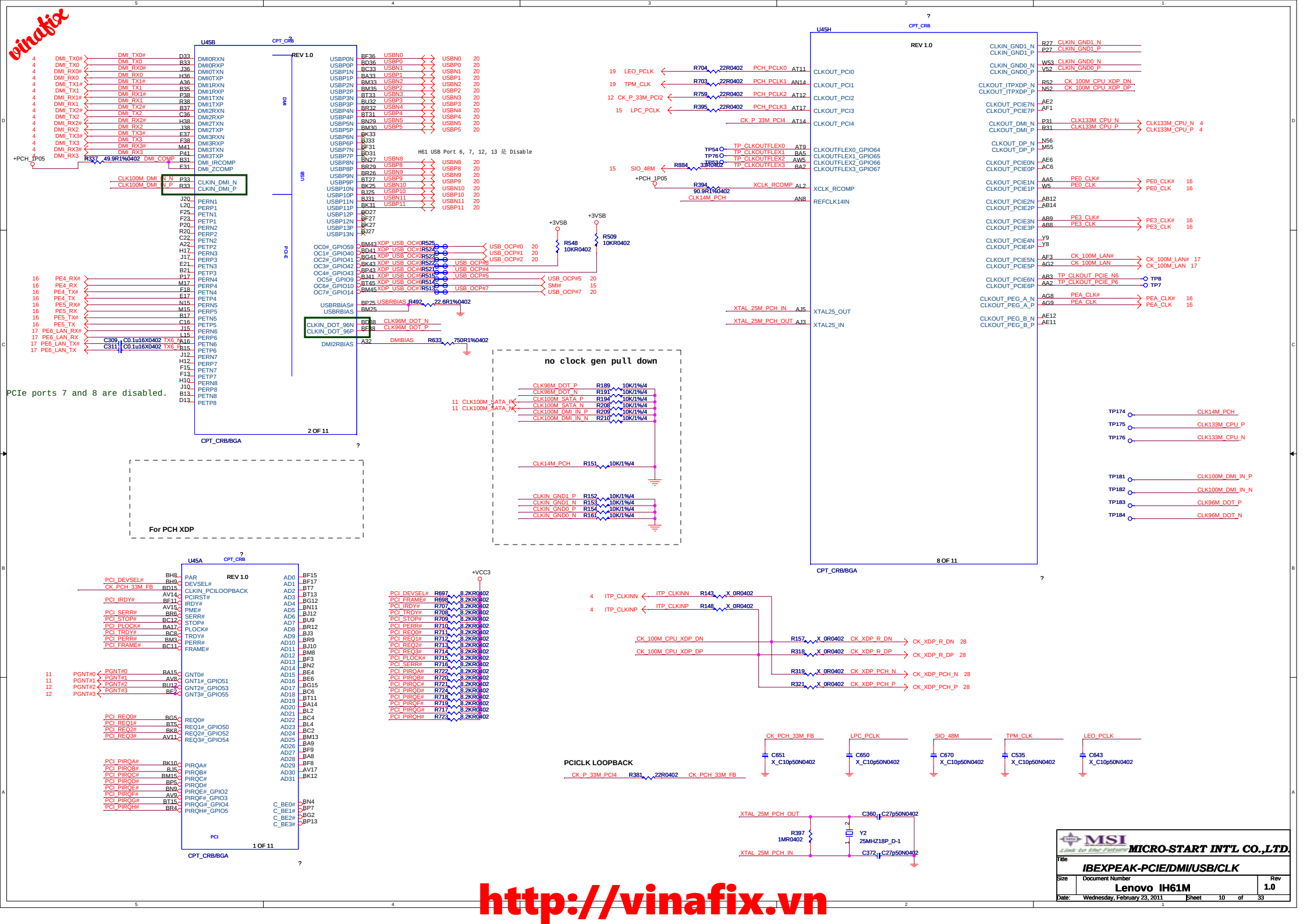
DDRIII DIMM_B1

DDR3

DIMM3(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

Title	DDR3 Chanel-B DIMM2
Size	Document Number: Lenovo IH61M
Rev	1.0
Date:	Wednesday, February 23, 2011
Sheet	9 of 33

MSI Link to the Future MICRO-START INT'L CO.,LTD.


U45B
CPT_CRB
REV 1.0
DMI_TX0#
DMI_TX0
DMI_RX0#
DMI_RX0
DMI_TX1#
DMI_TX1
DMI_RX1#
DMI_RX1
DMI_TX2#
DMI_TX2
DMI_RX2#
DMI_RX2
DMI_TX3#
DMI_TX3
DMI_RX3#
DMI_RX3
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_IRCOMP
DMI_ZCOMP
+PCH_1P05
R337 49.9R1%0402
DMI_COMP
CLK100M_DMI_N_N
CLK100M_DMI_N_P
CLKIN_DMI_N
CLKIN_DMI_P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
DMI
PCIE
USB
2 OF 11
CPT_CRB/BGA
PE4_RX#
PE4_RX
PE4_TX#
PE4_TX
PE5_RX#
PE5_RX
PE5_TX#
PE5_TX
PE6_LAN_RX#
PE6_LAN_RX
PE6_LAN_TX#
PE6_LAN_TX
C309 C0.1u16X0402 TX6_N
C311 C0.1u16X0402 TX6_P
PCIe ports 7 and 8 are disabled.
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P
USBN0
USBP0
USBN1
USBP1
USBN2
USBP2
USBN3
USBP3
USBN4
USBP4
USBN5
USBP5
USBN8
USBP8
USBN9
USBP9
USBN10
USBP10
USBN11
USBP11
H61 USB Port 6, 7, 12, 13 是 Disable
OC0#_GPIO59
OC1#_GPIO40
OC2#_GPIO41
OC3#_GPIO42
OC4#_GPIO43
OC5#_GPIO9
OC6#_GPIO10
OC7#_GPIO14
XDP_USB_OC#0
XDP_USB_OC#1
XDP_USB_OC#2
XDP_USB_OC#3
XDP_USB_OC#4
XDP_USB_OC#5
XDP_USB_OC#6
XDP_USB_OC#7
R525
R524
R523
R522
R521
R515
R514
R513
USB_OCP#0
USB_OCP#1
USB_OCP#2
USB_OCP#3
USB_OCP#4
USB_OCP#5
USB_OCP#7
SMI#
+3VSB
R548 10KR0402
R509 10KR0402
USBRBIAS#
USBRBIAS
R492 22.6R1%0402
CLKIN_DOT_96N
CLKIN_DOT_96P
CLK96M_DOT_N
CLK96M_DOT_P
DMI2RBIAS
DMIBIAS
R633 750R1%0402
no clock gen pull down
CLK96M_DOT_P
CLK96M_DOT_N
CLK100M_SATA_P
CLK100M_SATA_N
CLK100M_DMI_IN_P
CLK100M_DMI_IN_N
CLK14M_PCH
CLKIN_GND1_P
CLKIN_GND1_N
CLKIN_GND0_N
CLKIN_GND0_P
R189 10K/1%/4
R191 10K/1%/4
R194 10K/1%/4
R208 10K/1%/4
R209 10K/1%/4
R210 10K/1%/4
R151 10K/1%/4
R152 10K/1%/4
R153 10K/1%/4
R154 10K/1%/4
R161 10K/1%/4
For PCH XDP
U45A
CPT_CRB
REV 1.0
PAR
DEVSEL#
CLKIN_PCILOOPBACK
PCIRST#
IRDY#
PME#
SERR#
STOP#
PLOCK#
TRDY#
PERR#
FRAME#
PCI_DEVSEL#
CK_PCH_33M_FB
PCI_IRDY#
PCI_SERR#
PCI_STOP#
PCI_PLOCK#
PCI_TRDY#
PCI_PERR#
PCI_FRAME#
PGNT#0
PGNT#1
PGNT#2
PGNT#3
GNT0#
GNT1#_GPIO51
GNT2#_GPIO53
GNT3#_GPIO55
PCI_REQ0#
PCI_REQ1#
PCI_REQ2#
PCI_REQ3#
REQ0#
REQ1#_GPIO50
REQ2#_GPIO52
REQ3#_GPIO54
PCI_PIRQA#
PCI_PIRQB#
PCI_PIRQC#
PCI_PIRQD#
PCI_PIRQE#
PCI_PIRQF#
PCI_PIRQG#
PCI_PIRQH#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#_GPIO2
PIRQF#_GPIO3
PIRQG#_GPIO4
PIRQH#_GPIO5
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
C_BE0#
C_BE1#
C_BE2#
C_BE3#
PCI
1 OF 11
CPT_CRB/BGA
+VCC3
PCI_DEVSEL# R697 8.2KR0402
PCI_FRAME# R698 8.2KR0402
PCI_IRDY# R707 8.2KR0402
PCI_TRDY# R708 8.2KR0402
PCI_STOP# R709 8.2KR0402
PCI_PERR# R710 8.2KR0402
PCI_REQ0# R711 8.2KR0402
PCI_REQ1# R712 8.2KR0402
PCI_REQ2# R713 8.2KR0402
PCI_REQ3# R714 8.2KR0402
PCI_PLOCK# R715 8.2KR0402
PCI_SERR# R716 8.2KR0402
PCI_PIRQA# R722 8.2KR0402
PCI_PIRQB# R720 8.2KR0402
PCI_PIRQC# R721 8.2KR0402
PCI_PIRQD# R724 8.2KR0402
PCI_PIRQE# R718 8.2KR0402
PCI_PIRQF# R719 8.2KR0402
PCI_PIRQG# R717 8.2KR0402
PCI_PIRQH# R723 8.2KR0402
PCICLK LOOPBACK
CK_P_33M_PCI4 R381 22R0402 CK_PCH_33M_FB
U45H
CPT_CRB
REV 1.0
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
LEO_PCLK
TPM_CLK
CK_P_33M_PCI2
LPC_PCLK
PCH_PCLK0
PCH_PCLK1
PCH_PCLK2
PCH_PCLK3
R704 22R0402
R703 22R0402
R759 22R0402
R395 22R0402
TP_CLKOUTFLEX0
TP_CLKOUTFLEX1
TP_CLKOUTFLEX2
TP_CLKOUTFLEX3
CLKOUTFLEX0_GPIO64
CLKOUTFLEX1_GPIO65
CLKOUTFLEX2_GPIO66
CLKOUTFLEX3_GPIO67
SIO_48M
R884 33R0402
XCLK_RCOMP
R394 90.9R1%0402
CLK14M_PCH
REFCLK14IN
XTAL_25M_PCH_IN
XTAL_25M_PCH_OUT
XTAL25_OUT
XTAL25_IN
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_GND0_N
CLKIN_GND0_P
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLK133M_CPU_N
CLK133M_CPU_P
PE0_CLK#
PE0_CLK
PE3_CLK#
PE3_CLK
CK_100M_LAN#
CK_100M_LAN
TP_CLKOUT_PCIE_N6
TP_CLKOUT_PCIE_P6
PEA_CLK#
PEA_CLK
8 OF 11
CPT_CRB/BGA
TP174 CLK14M_PCH
TP175 CLK133M_CPU_P
TP176 CLK133M_CPU_N
TP181 CLK100M_DMI_IN_P
TP182 CLK100M_DMI_IN_N
TP183 CLK96M_DOT_P
TP184 CLK96M_DOT_N
ITP_CLKINN
ITP_CLKINP
R143 X_0R0402
R148 X_0R0402
CK_100M_CPU_XDP_DN
CK_100M_CPU_XDP_DP
R157 X_0R0402 CK_XDP_R_DN
R318 X_0R0402 CK_XDP_R_DP
R319 X_0R0402 CK_XDP_PCH_N
R321 X_0R0402 CK_XDP_PCH_P
C651 X_C10p50N0402
C650 X_C10p50N0402
C670 X_C10p50N0402
C535 X_C10p50N0402
C643 X_C10p50N0402
XTAL_25M_PCH_OUT
XTAL_25M_PCH_IN
R397 1MR0402
Y2 25MHZ18P_D-1
C360 C27p50N0402
C372 C27p50N0402
MSI
MICRO-START INT'L CO.,LTD.
Title
IBEXPEAK-PCIE/DMI/USB/CLK
Size
Document Number
Lenovo IH61M
Rev
1.0
Date: Wednesday, February 23, 2011
Sheet 10 of 33
http://vinafix.vn

SATA ports 2 and 3 are disabled.

ROUTE TRACE LENGTH NO LONGER THAN 450 MILS TO RESISTOR

have an internal weak pull-up -
Default destination is SPI

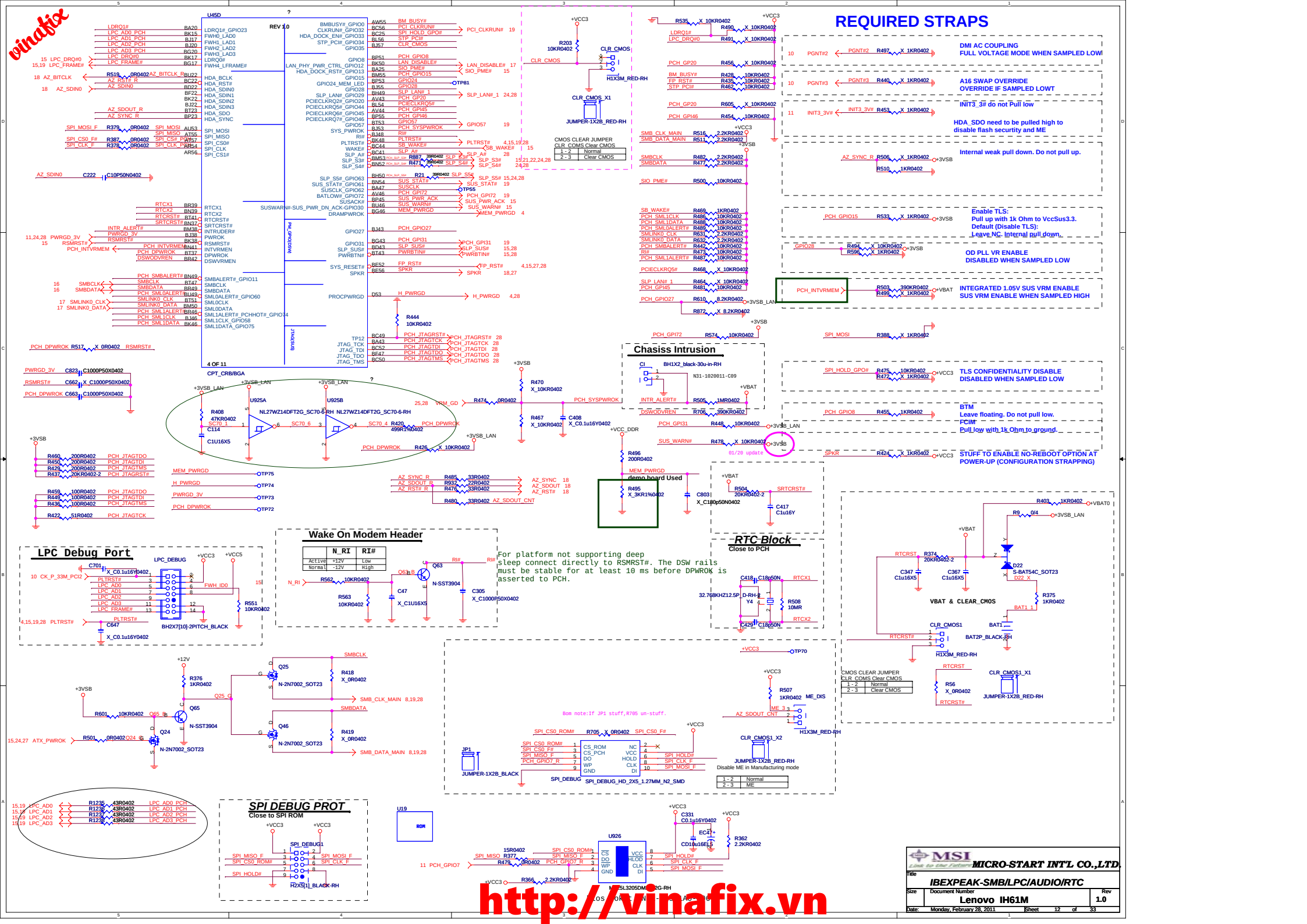
Intel Update

BOOT DEVICE	GNT1#	SATA1GP_ GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

VGA DACSET RESISTORS CLOSE TO MCH(500 MILS TO MCH BALLS)

Title	IBEXPEAK-SATA/HOST/FAN/GPIO
Size	Document Number: Lenovo IH61M
Rev	1.0
Date:	Wednesday, February 23, 2011
Sheet	11 of 33

MSI MICRO-START INT'L CO.,LTD.


REQUIRED STRAPS
DMI AC COUPLING
FULL VOLTAGE MODE WHEN SAMPLED LOW
A16 SWAP OVERRIDE
OVERRIDE IF SAMPLED LOWT
INIT3_3# do not Pull low
HDA_SDO need to be pulled high to disable flash securtity and ME
Internal weak pull down. Do not pull up.
Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.
OD PLL VR ENABLE
DISABLED WHEN SAMPLED LOW
INTEGRATED 1.05V SUS VRM ENABLE
SUS VRM ENABLE WHEN SAMPLED HIGH
TLS CONFIDENTIALITY DISABLE
DISABLED WHEN SAMPLED LOW
BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING)
Chasis Intrusion
Wake On Modem Header
RTC Block
Close to PCH
LPC Debug Port
SPI DEBUG PROT
Close to SPI ROM
VBAT & CLEAR_CMOS
CPT_CRB/BGA
4 OF 11
REV 1.0
demo board Used
For platform not supporting deep sleep connect directly to RSMRST#. The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.
CMOS CLEAR JUMPER
Normal
Clear CMOS
Disable ME in Manufacturing mode
MSI
MICRO-STAR INT'L CO.,LTD.
IBEXPEAK-SMB/LPC/AUDIO/RTC
Lenovo IH61M
1.0
Monday, February 28, 2011
Sheet 12 of 33
http://vinafix.vn

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

DMI PLL FILTER

SATA PLL FILTER

5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore,they can satisfy the requirement.

Near ball AF1

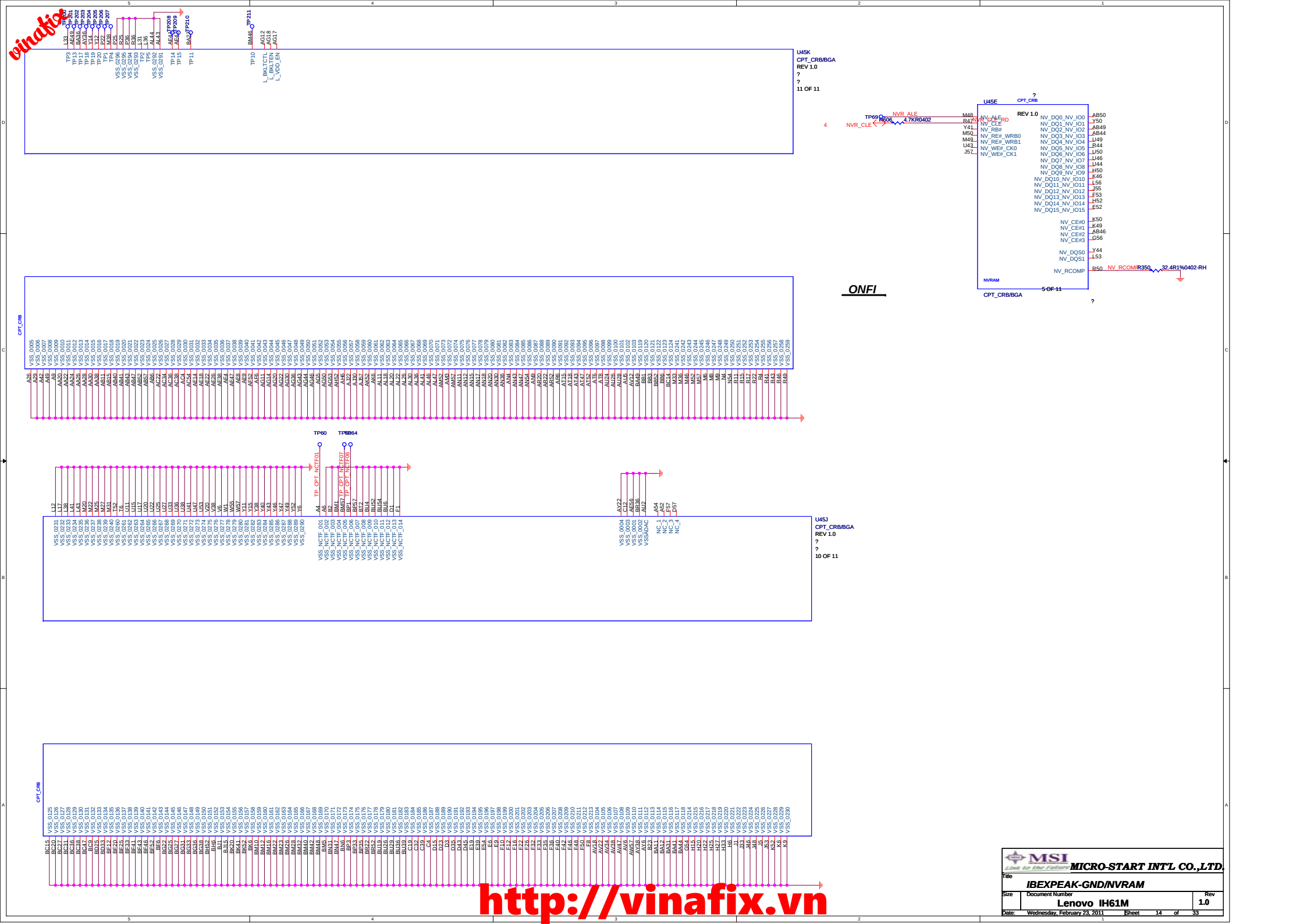
PCH decoupling cap

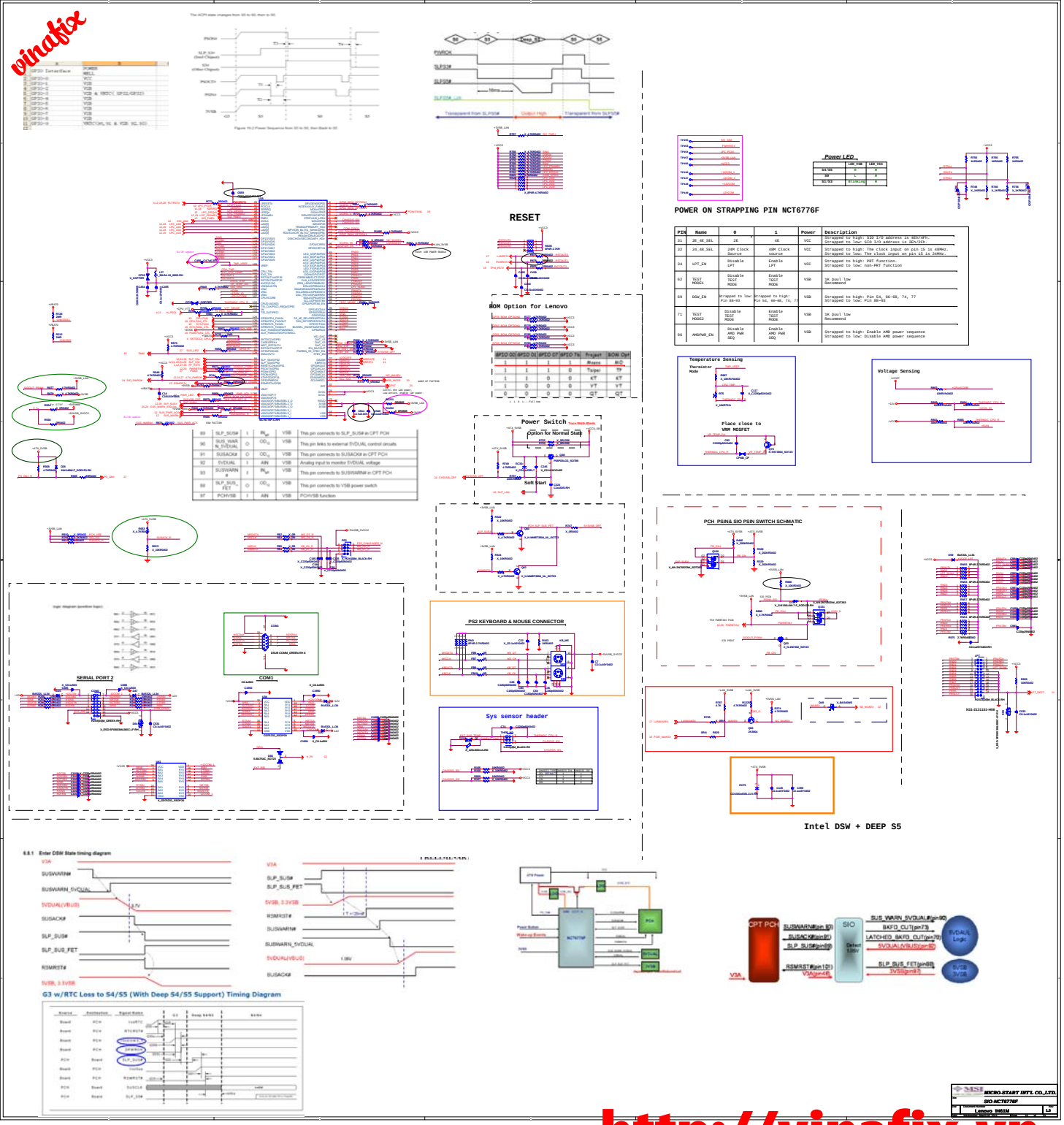
bottom side

bottom side

Title	IBEXPEAK-POWER
Size	Document Number: Lenovo IH61M
Rev	1.0
Date:	Wednesday, February 23, 2011
Sheet	13 of 33

MSI MICRO-START INT'L CO.,LTD.


U45K
CPT_CRB/BGA
REV 1.0
11 OF 11
U45E
CPT_CRB
REV 1.0
NVRAM
5 OF 11
CPT_CRB/BGA
NVR_ALE
NVR_CLE
R606 4.7KR0402
R350 32.4R1%0402-RH
NV_RCOMP
ONFI
U45J
CPT_CRB/BGA
REV 1.0
10 OF 11
TP60
TP61
TP_CPT_NCTF01
TP_CPT_NCTF07
TP_CPT_NCTF06
http://vinafix.vn
MICRO-START INT'L CO.,LTD.
IBEXPEAK-GND/NVRAM
Lenovo IH61M
1.0
Wednesday, February 23, 2011
14 of 33



RESET

BOM Option for Lenovo

Power Switch

Option for Normal State

Soft Start

PS2 KEYBOARD & MOUSE CONNECTOR

Sys sensor header

SERIAL PORT 2

COM1

Temperature Sensing

Thermistor Mode

Place close to VRM MOSFET

Voltage Sensing

PCH_PSIN& SIO PSIN SWITCH SCHMATIC

Intel DSW + DEEP S5

POWER ON STRAPPING PIN NCT6776F

PIN	Name	0	1	Power	Description
31	2E_4E_SEL	2E	4E	VCC	Strapped to high: SIO I/O address is 4E0/4F0. Strapped to low: SIO I/O address is 2E0/2F0.
32	24_48_SEL	24M Clock Source	48M Clock source	VCC	Strapped to high: The clock input on pin 1G is 48Mhz. Strapped to low: The clock input on pin 1G is 24Mhz.
34	LPT_EN	Disable LPT	Enable LPT	VCC	Strapped to high: PRT Function. Strapped to low: non-PRT function
62	TEST MODE1	Disable TEST MODE	Enable TEST MODE	VSB	1K pull low Recommend
69	DSW_EN	Strapped to low: Pin 69~93	Strapped to high: Pin 54, 66~68, 74, 77 Strapped to low: Pin 80~88	VSB	Strapped to high: Pin 54, 66~68, 74, 77 Strapped to low: Pin 80~88
71	TEST MODE2	Disable TEST MODE	Enable TEST MODE	VSB	1K pull low Recommend
96	AMDPWR_EN	Disable AMD PWR SEQ	Enable AMD PWR SEQ	VSB	Strapped to high: Enable AMD power sequence Strapped to low: Disable AMD power sequence

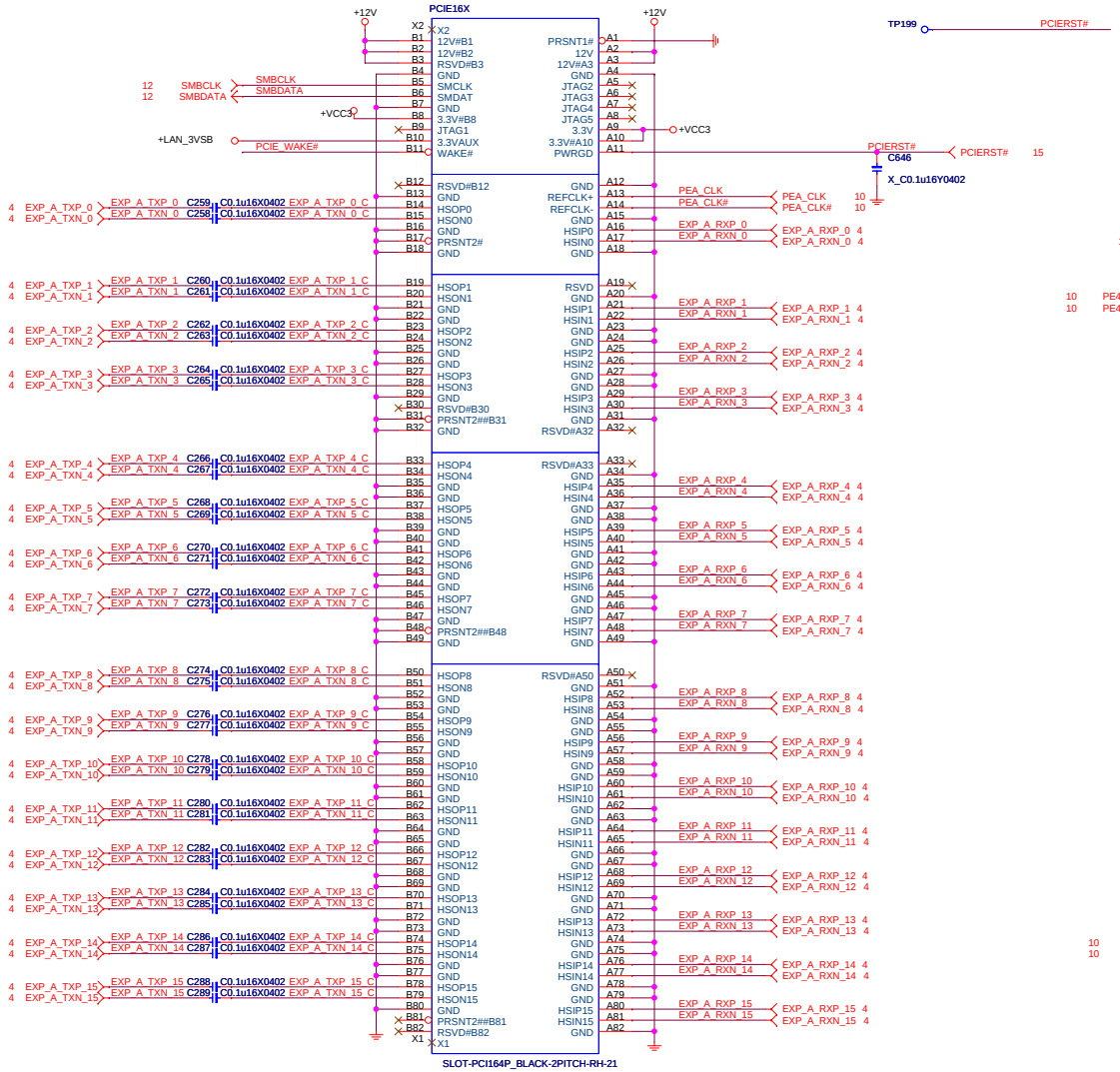
Power LED		
	LED_VSB	LED_VCC
S4/S5	H	H
S0	L	H
S1/S3	0.5Hz/1Hz	H

89	SLP_SUS#	I	IN_{ST}	VSB	This pin connects to SLP_SUS# in CPT PCH
90	SUS_WAR N_5VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits.
91	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
92	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
93	SUSWARN #_3VDUAL	I	IN_{ST}	VSB	This pin connects to SUSWARN# in CPT PCH
88	SLP_SUS_ FET	O	OD_{12}	VSB	This pin connects to VSB power switch
97	PCHVSB	I	AIN	VSB	PCHVSB function

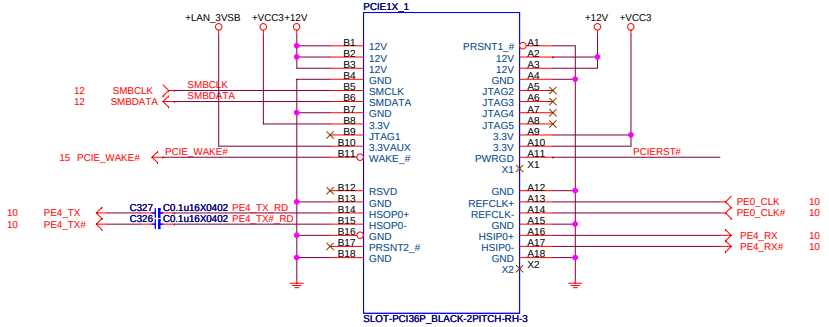
G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram

MSI	MICRO-START INT'L CO.,LTD.
	SIO-NCT6776F
	Lenovo B481M

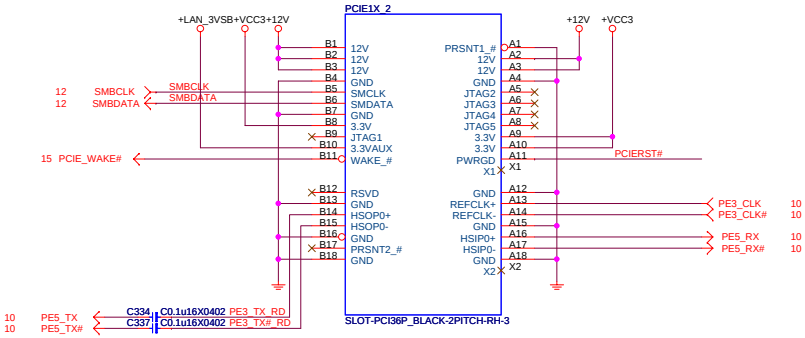
PCI EXPRESS X16 SLOT

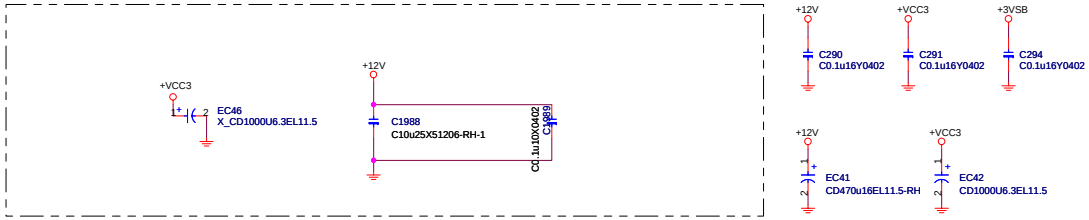


PCI EXPRESS x1-PORT



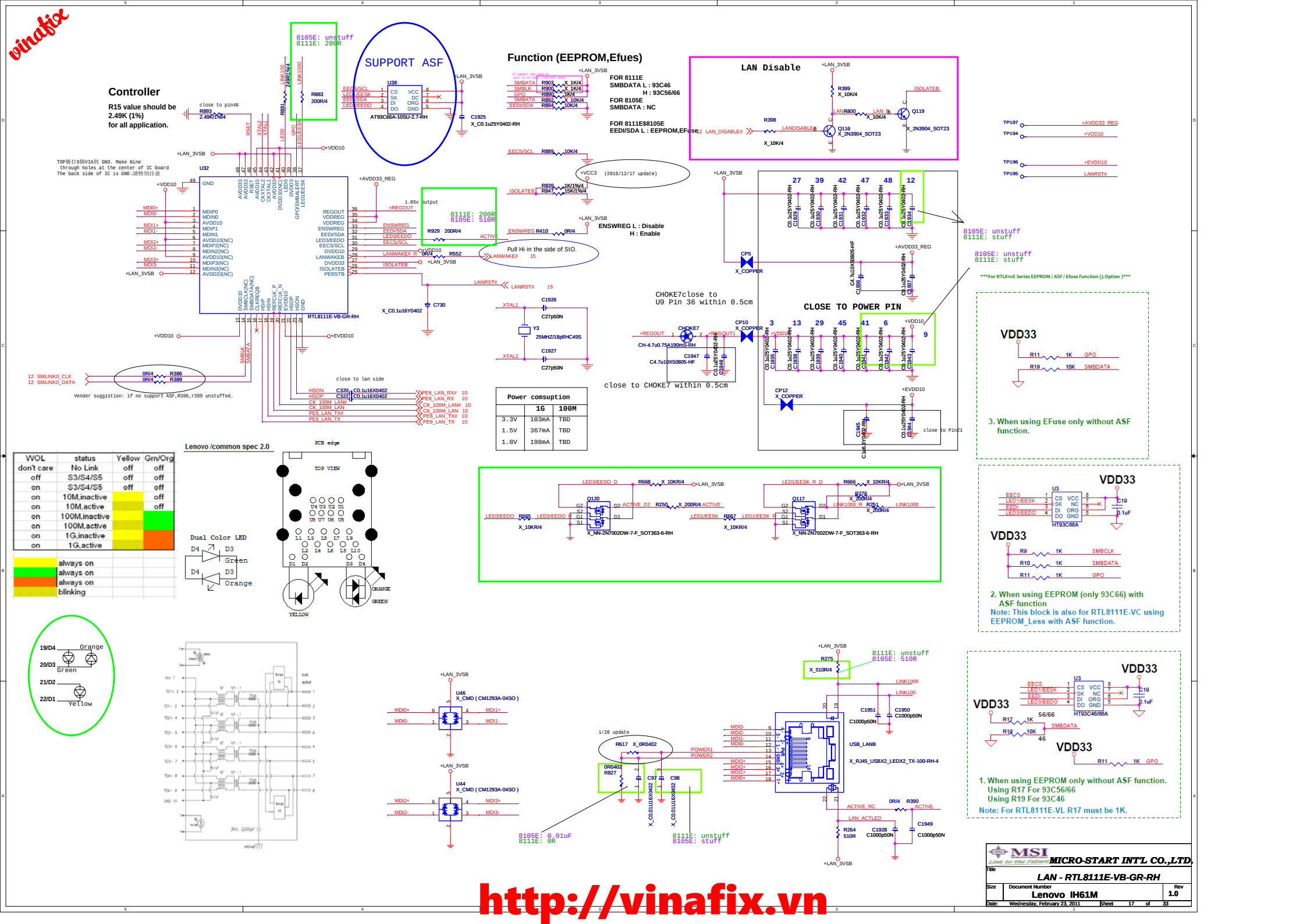
PCI EXPRESS x1-PORT





MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

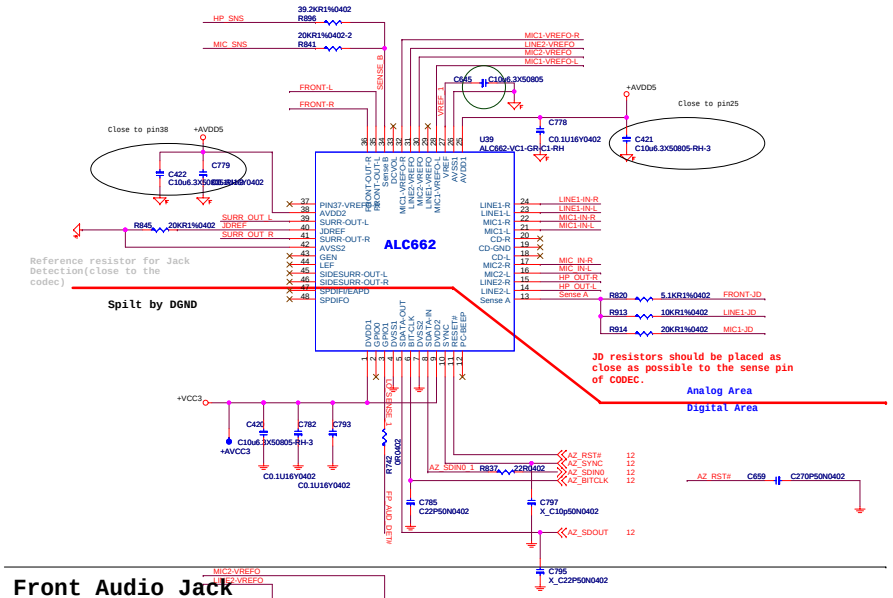
Title	PCIE x16&x1	
Size	Document Number: Lenovo IH61M	Rev: 1.0
Date: Wednesday, February 23, 2011	Sheet 16 of 33	



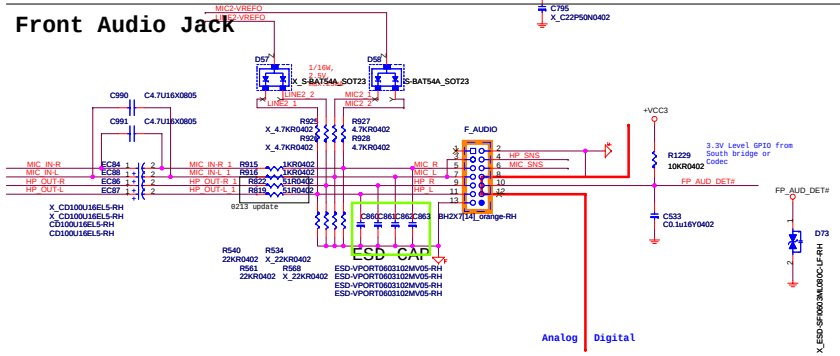
WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

Audio Codec ALC662

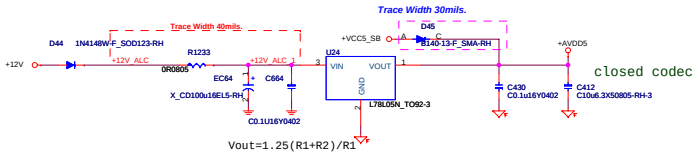
JD resistors and front microphone input cap. should be placed as close as possible to the sense pin of CODEC.



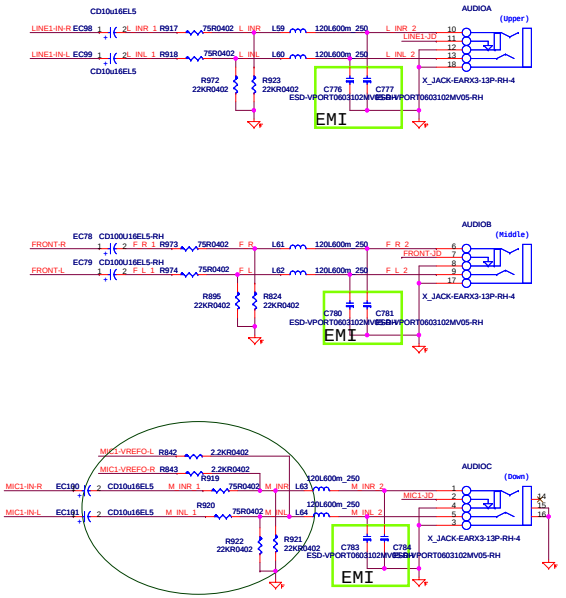
Front Audio Jack



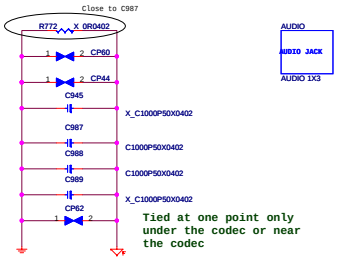
AUDIO CODE REGULATORS

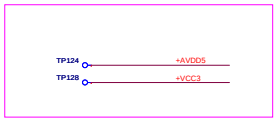


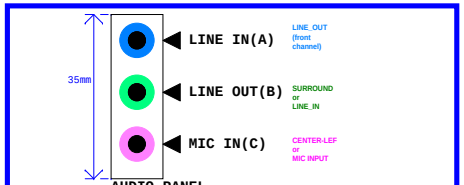
Rear Phone Jack



CD IN





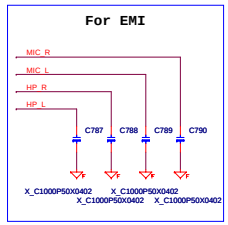


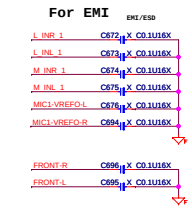
AUDIO PANEL
AUDIO1

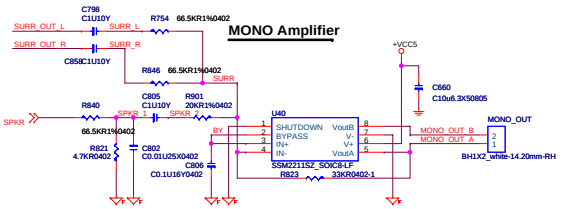
ALC888(DD) Desktop Configuation (5.1 Channel Solution For Lenovo NOVO) (3 Jacks at rear panel , 2 jacks at front panel)

Pin Assignment	Location	Re-tasking
LINE1 (pin-23/24)	Rear Panel	line input
FRONT(pin-35/36)	Rear Panel	AMP output
MIC1 (pin-21/22)	Rear Panel	MIC input
SURR (pin-39/41)	Rear RCA Jack	Line output
CEN/LFE (pin-43/44)	N/A	Line output
SIDE-SURR (pin-45/46)	N/A	Line output
LINE2 (pin-14/15)	Front Panel	AMP output
FMIC (pin-16/17)	Front Panel	Stereo MIC input

EMI







MSI MICRO-START INT'L CO.,LTD.

Title: Azalia Codec - ALC662

Size	Document Number	Rev
Custom	Lenovo IH61M	1.0

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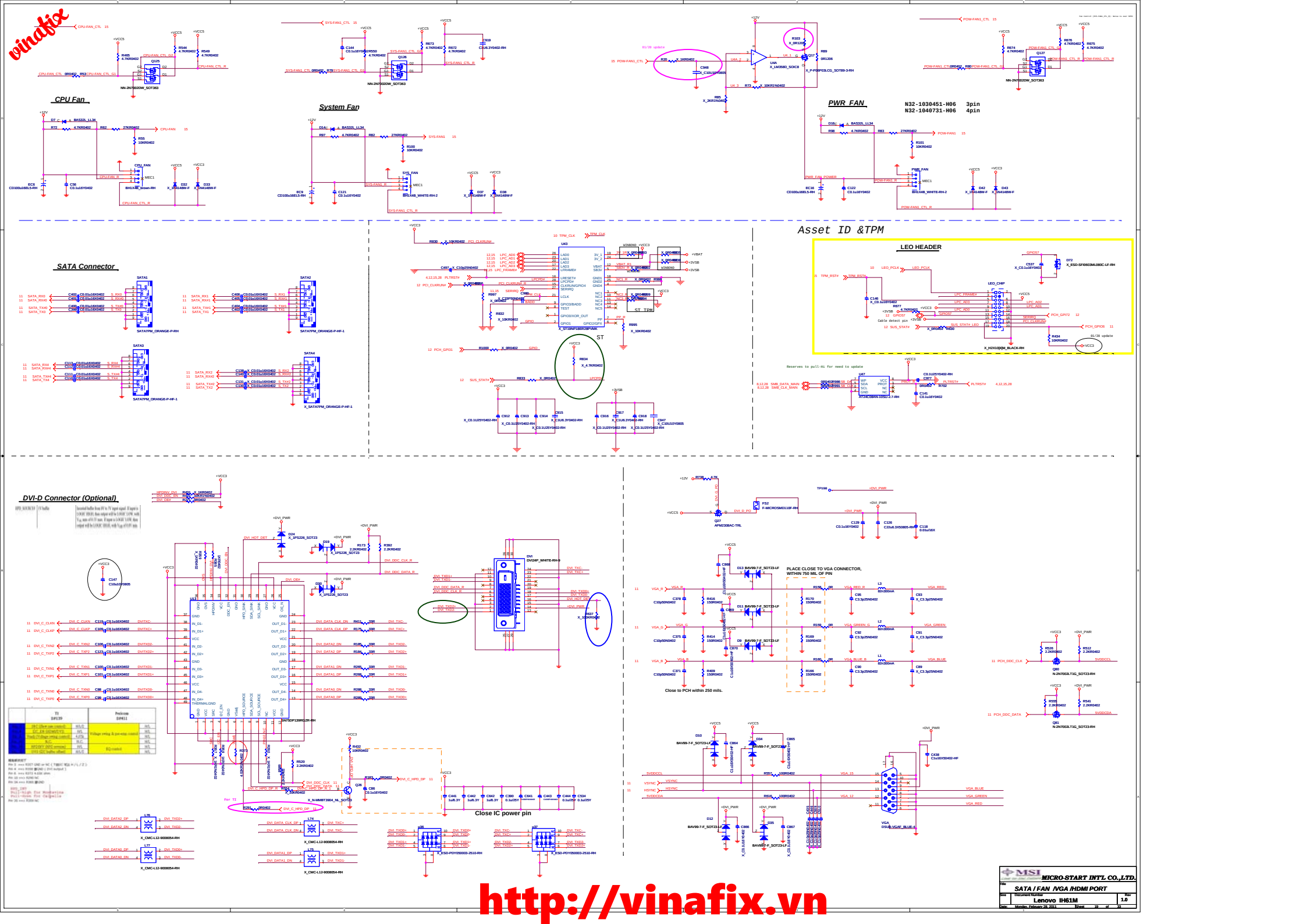


Front Panel and Rear I/O USB Connector

Rear USB Connnector For USB Port 0 / 1

6.5A

+VCC5 +VCC5_SB

C235 C0.1u16Y0402

C123 C0.1u16Y0402

U16 UP7536AMA8_SOT23-8-HF

21,24 USB_EN#
10 USB_OCP#1
15 USB_MODE

C228 C0.1u16Y0402

EC36 CD1000U6.3EL11.5

+5VUSB_SVCC1

R226 X_0R SBD3+
R225 X_0R SBD3-
R228 X_0R SBD2+
R227 X_0R SBD2-

L8 INPAQ (MCM2012B900GBE)
L9 INPAQ (MCM2012B900GBE)

USBP3 USBN3 USBP2 USBN2

D21 ESD-AOZ8902CIL-HF

C433 X_C.01u16X0402

+5VUSB_SVCC1

X_C0.1u16Y0402 C432

USB_LANA UP DOWN

X_RJ45_USBX2_LEDX2_TX-100-RH-4

Rear USB Connnector For USB Port 2 / 3

+VCC5 +VCC5_SB

C183 C0.1u16Y0402

C725 C0.1u16Y0402

U11 UP7536AMA8_SOT23-8-HF

21,24 USB_EN#
10 USB_OCP#5
15 USB_MODE

C182 C0.1u16Y0402

EC30 CD1000U6.3EL11.5

+5VUSB_SVCC2

D27 ESD-AOZ8902CIL-HF

C450 X_C.01u16X0402

R230 X_0R SBD9+
R229 X_0R SBD9-
R232 X_0R SBD8+
R231 X_0R SBD8-

USBP9 USBN9 USBP8 USBN8

L25 L22 INPAQ (MCM2012B900GBE)

C436 X_C0.1u16Y0402

USB UP DOWN USBAX2M_BLACK-RH

+3VSB_LAN +3VSB

R129 X_4.7KR0402
R130 4.7KR0402

USB_MODE

R128 X_4.7KR0402

15,24 SUS_WARN_5VDUAL

EN_Q49

Q49 X_N-MMBT3904_NL_SOT23

12,24,28 SLP_S4#

R331 0R

FUSB_G3 FUSB_G2 FUSB_G1

X_ESD-SFI0603ML080C-LF-RH D63 D62 D61

+VCC5 EC74 .CD1000U6.3EL11.5

+5VUSB_SVCC4 R266 27KR0402 R267 51KR0402 USB_OCP#0
+5VUSB_SVCC1 R202 27KR0402 R199 51KR0402 USB_OCP#1
+5VUSB_SVCC5 R594 27KR0402 R586 51KR0402 USB_OCP#2
+5VUSB_SVCC2 R590 27KR0402 R582 51KR0402 USB_OCP#5

Lenovo Consumer MB common spec V0 2:
Must reserve ESD protection diode on USB front header 5V_Dual power.

+5VUSB_SVCC1 +5VUSB_SVCC2 +5VUSB_SVCC3 +5VUSB_SVCC4 +5VUSB_SVCC5

D54 D55 D56 D52 D53

X_ESD-SFI0603ML080C-LF-RH

Front Panel USB Connnector For USB Port 6 / 7

+VCC5 +VCC5_SB

C458 C0.1u16Y0402

C366 C0.1u16Y0402

U30 UP7536AMA8_SOT23-8-HF

21,24 USB_EN#
10 USB_OCP#0
15 USB_MODE

C467 C0.1u16Y0402

EC54 CD1000U6.3EL11.5

+5VUSB_SVCC4

L21 L24 INPAQ (MCM2012B900GBE)

USBP1 USBN1 USBP0 USBN0

D28 X_ESD-AOZ8902CIL-HF

C448 X_C.01u16X0402

R234 X_0R SBD1+
R233 X_0R SBD1-
R293 X_0R SBD0+
R235 X_0R SBD0-

C665 C0.1U16Y0402

F_USB1 H2X6[11]M_YELLOW-RH

C530 C0.1u16Y0402

FUSB_G1

EMI

Front Panel USB Connnector For USB Port 8 / 9

+VCC5 +VCC5_SB

C462 C0.1u16Y0402

C724 C0.1u16Y0402

U29 UP7536AMA8_SOT23-8-HF

21,24 USB_EN#
10 USB_OCP#2
15 USB_MODE

C466 C0.1u16Y0402

EC58 CD1000U6.3EL11.5

+5VUSB_SVCC5

L23 L26 INPAQ (MCM2012B900GBE)

USBP5 USBN5 USBP4 USBN4

D29 X_ESD-AOZ8902CIL-HF

C449 X_C.01u16X0402

R295 X_0R SBD5+
R294 X_0R SBD5-
R304 X_0R SBD4+
R302 X_0R SBD4-

C668 C0.1U16Y0402

F_USB2 H2X6[11]M_YELLOW-RH

C457 C0.1u16Y0402

FUSB_G2

EMI

Front Panel USB Connnector For USB Port 10 / 11

+VCC5 +VCC5_SB

C447 X_C0.1u16Y0402

C721 C0.1u16Y0402

U27 X_UP7536AMA8_SOT23-8-HF

21,24 USB_EN#
10 USB_OCP#7
15 USB_MODE

C463 X_C0.1u16Y0402

EC59 X_CD1000U6.3EL11.5

+5VUSB_SVCC3

L29 L28 X_INPAQ (MCM2012B900GBE)

USBP10 USBN10 USBP11 USBN11

D46 X_ESD-AOZ8902CIL-HF

C451 X_C.01u16X0402

R306 X_0R SBD10+
R305 X_0R SBD10-
R311 X_0R SBD11+
R309 X_0R SBD11-

C671 X_C0.1U16Y0402

F_USB3 X_H2X6[11]M_YELLOW-RH

C453 C0.1u16Y0402

FUSB_G3

EMI

+5VUSB_SVCC3 R584 X_27KR0402 R583 51KR0402 USB_OCP#7

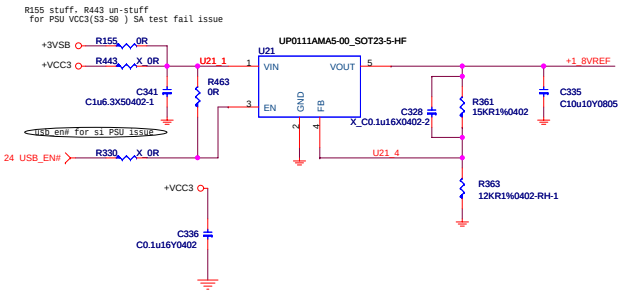
MSI MICRO-START INT'L CO.,LTD.

Title: Front / Rear USB Connectors

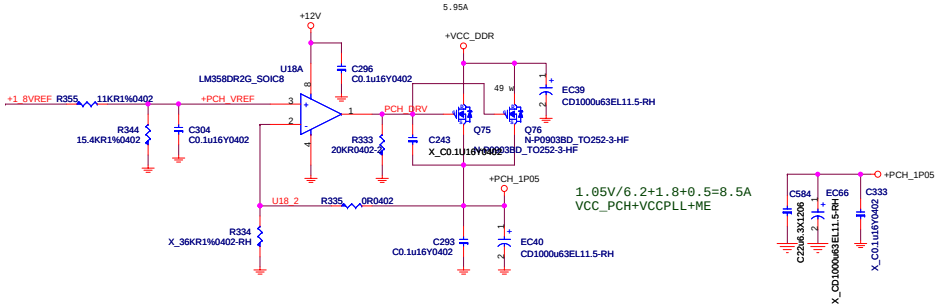
Size | Document Number: Lenovo IH61M | Rev: 1.0

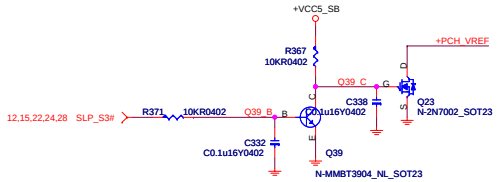
Date: Wednesday, February 23, 2011 | Sheet 20 of 33

1.8V Reference Power

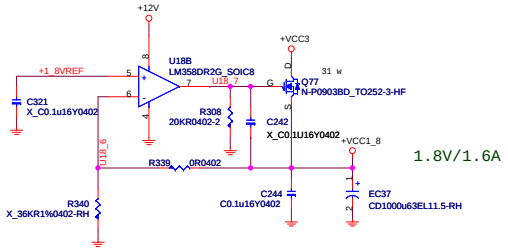


PCH Core Power





1.8V VSFR



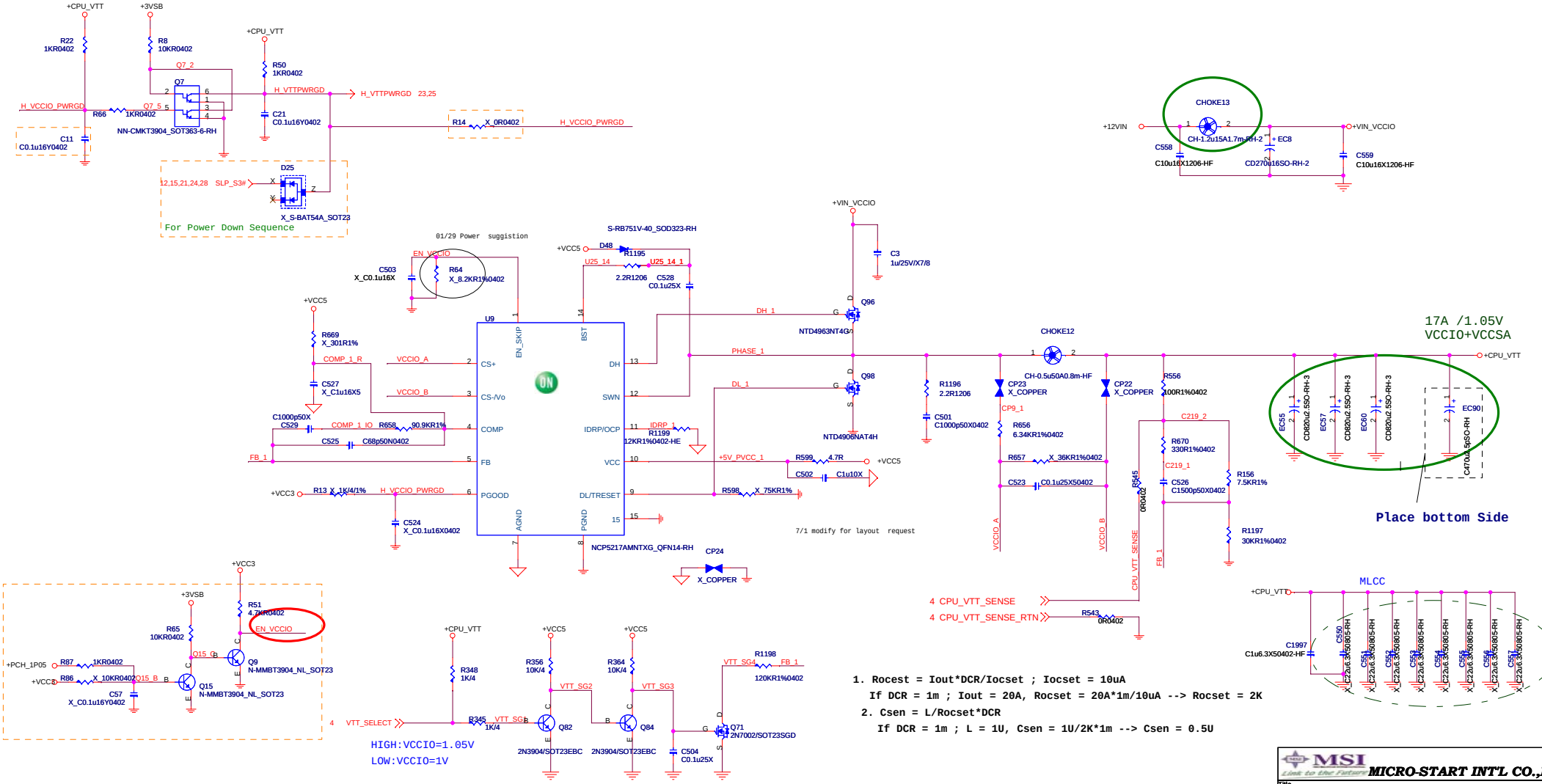
MSI MICRO-START INT'L CO.,LTD.

Title: PCH & ME Core Power

Size | Document Number: Lenovo IH61M | Rev: 1.0

Date: Wednesday, March 02, 2011 | Sheet 21 of 33

CPU VTT Power
1.1V - 30A - 29W



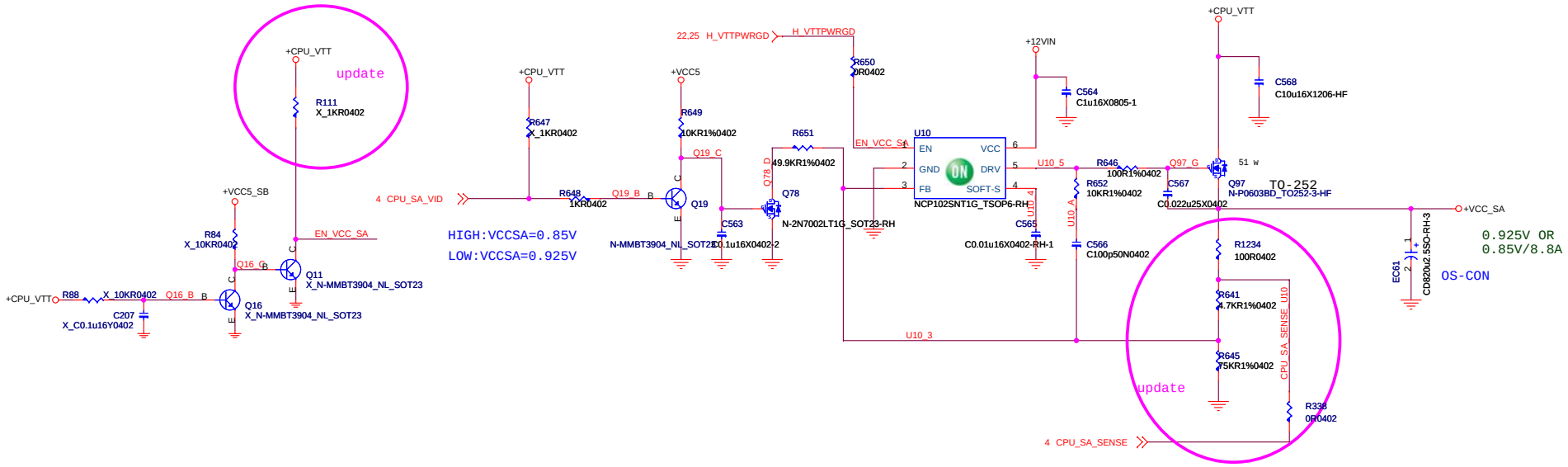
1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 1m ; Iout = 20A, Rocest = 20A*1m/10uA --> Rocset = 2K
2. Csen = L/Rocset*DCR
   If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title	CPU VTT VR	
Size	Document Number: Lenovo IH61M	Rev: 1.0
Date: Monday, February 28, 2011	Sheet 22 of 33	

VCCSA

1.05V/8.8A



MSI — Link to the Future — MICRO-START INT'L CO.,LTD.

Title	CPU VCC_SA	
Size	Document Number: Lenovo IH61M	Rev: 1.0
Date: Wednesday, February 23, 2011	Sheet 23 of 33	

DDRIII Regulator Power Source

5V - 5.8A - 29W

5.085A
VDDQ+VTT++PCH_1P05

4.5+6.5+5.95=16.95A
VDDQ+VTT++PCH_1P05

Vout = 0.8[(R249(GND)+R246)/R249]

For EMI

Control S5 +1.05_ME ON/OFF

Table 1 5VDUAL Output Truth Table

S5#	S3#	MODE	5VDUAL	Remarks
↑	↑	X	5VCC	S0/S1/S2 (Active)
↑	0	X	5VSB	S3
0	X	↑	5VSB	S4/S5
0	X	0	Shutdown	S4/S5

Note that when MODE = L, the 5VDUAL output can only be enabled by 5VCC and 12VCC POR (refer to the related sections for detail).

DDRIII Termination Power

1A

DDRIII I/O power decoulping caps.

Deep Mode WOL LAN Power CTRL Circuit

Update- 2009.9.3

Original LAN Power Source

LOW FOR LAN_POWER OK

3.3V Standby Power

0.8A

3.3V - 0.95A - 3.1W

The current come form +Vcc5_sb,please check layout

EMI CAPs

Title	DDR Power
Size	Document Number: Lenovo IH61M
Rev	1.0
Date:	Wednesday, February 23, 2011
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MICRO-START INT'L CO.,LTD.

CPU CRORE : OCP Min=134A , OCP Max=168A , OVP=DAC+175mV
GFX CRORE : OCP Min=42A , OCP Max=52.5A , OVP=DAC+175mV

VOLTAGE REGULATOR MODULE (VRD12)

update
C114 change to 470K resistor

Level Shift

PWM ADDRESS

RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE

RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

3PHASE OPTION

FOR NCP6151 AUTO PHASE SHED SETTING

FOR NCP6131 IMAX

PWM ADDRESS

VCORE IMAX SET AT 120A

VCORE VBOOT SET AT 0V

V_GT IMAX SET AT 35A

MSI MICRO-START INT'L CO.,LTD.

Title: NCP6151S52MNR2G_QFN52-RH

Size: | Document Number: Lenovo IH61M | Rev: 1.0

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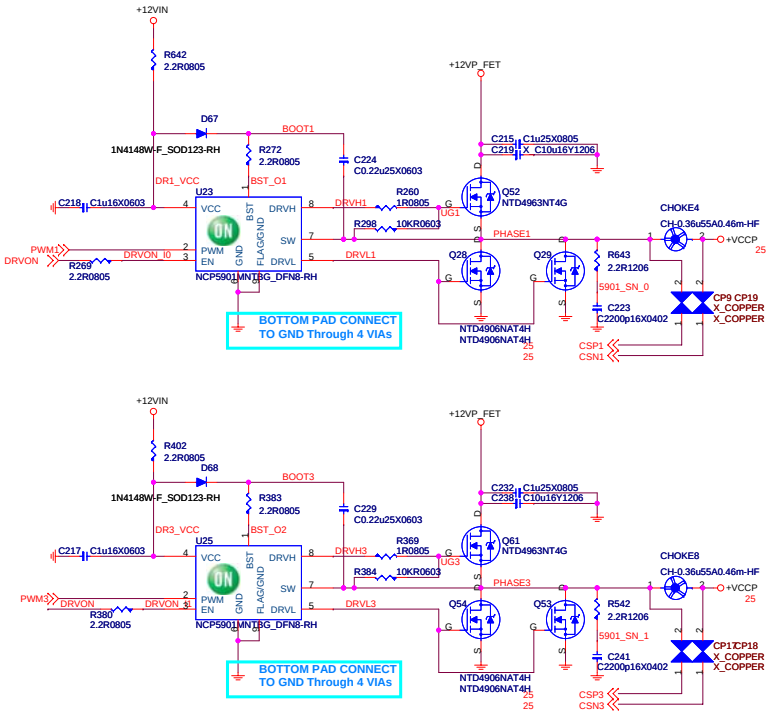
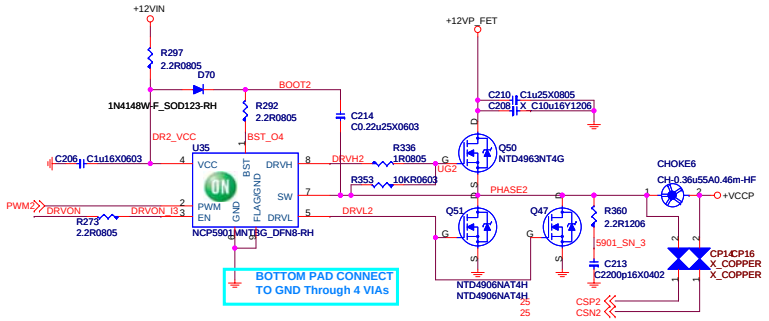
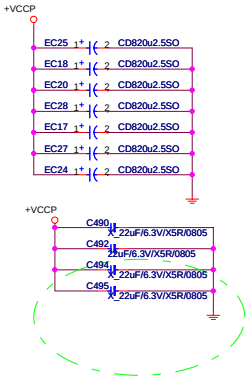
+CPU_VCCP

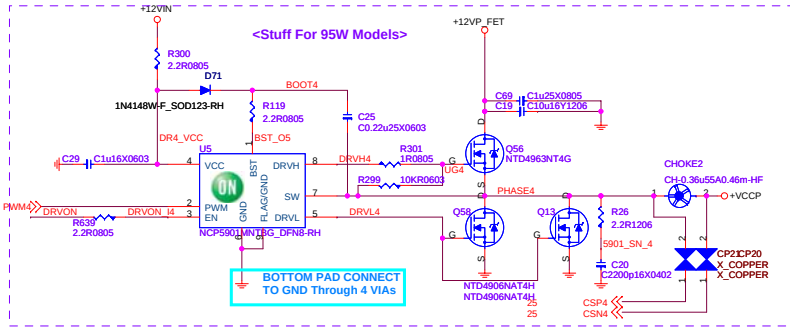




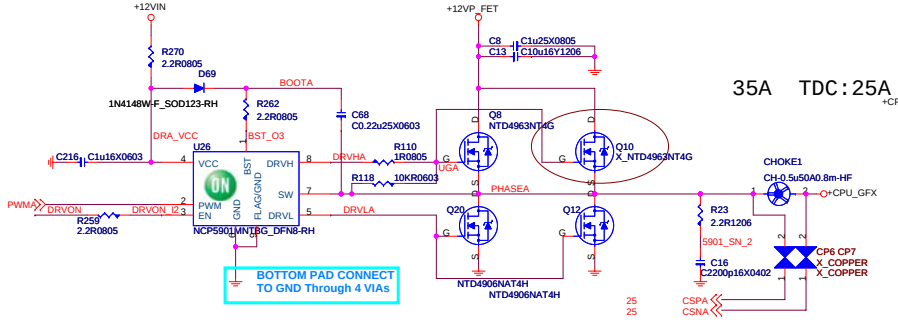
112A TDC:85A

+CPU_VCCP Output Caps

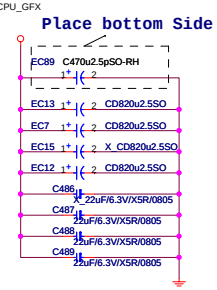




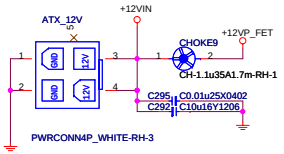
+CPU_GFX

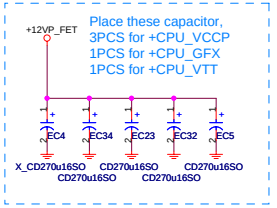


35A TDC:25A



ATX12V Power Connector

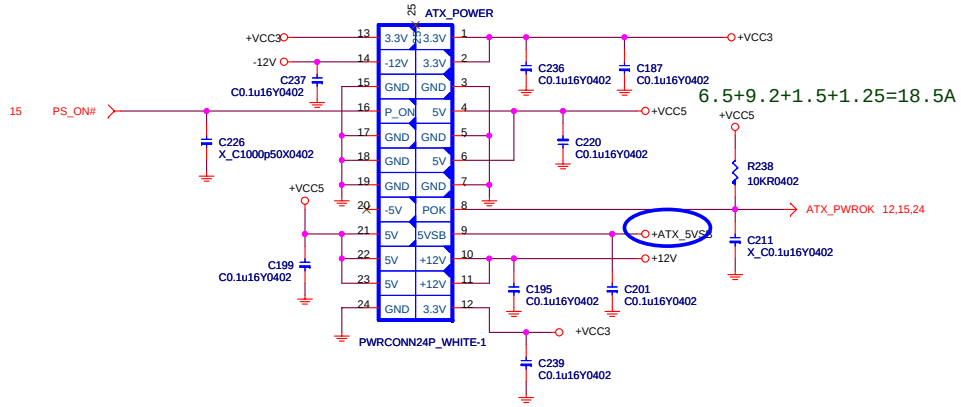


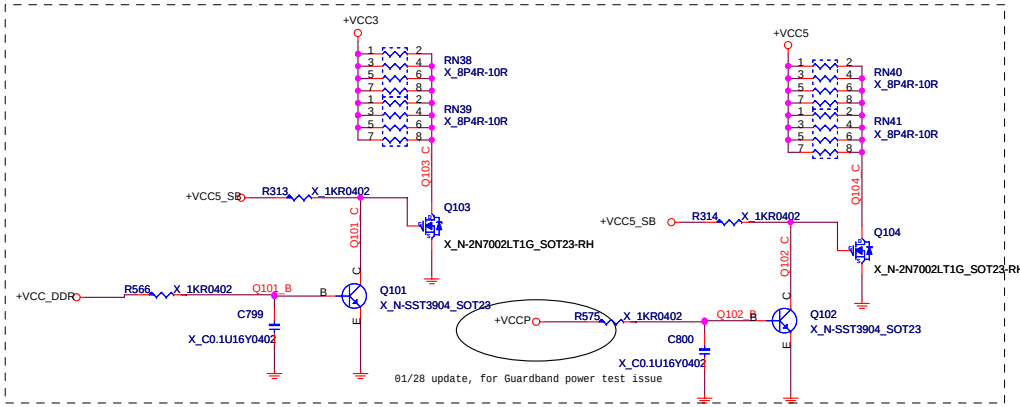


MSI Link to the Future	MICRO-START INTL CO.,LTD.	
Title	VCORE & VGFX POWER	
Size	Document Number: Lenovo IH61M	Rev: 1.0
Date: Wednesday, February 23, 2011	Sheet 26 of 33	

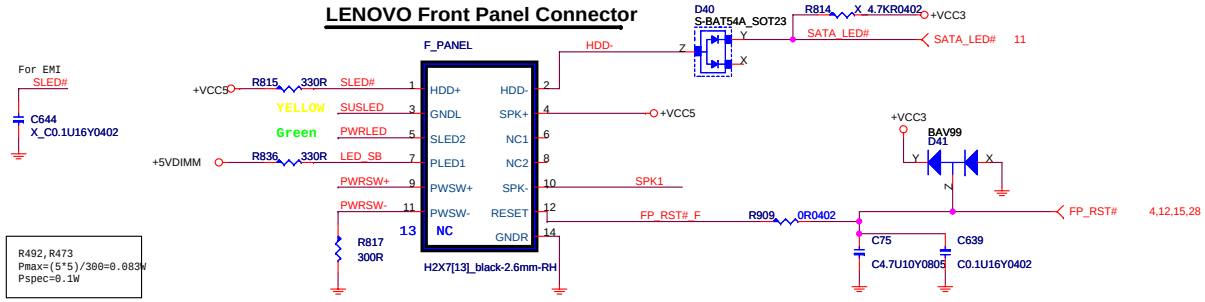
ATX Power Connector / Front Panel / LED

24 Pin ATX Power Connector

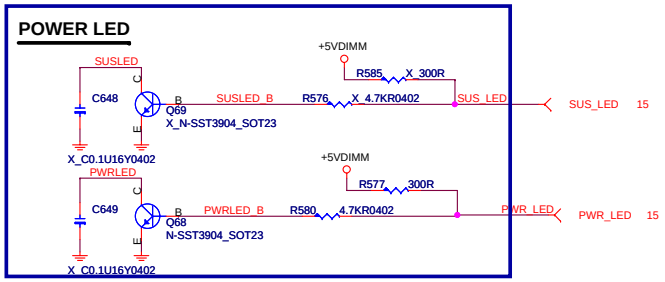




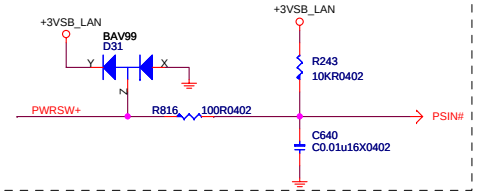
LENOVO Front Panel Connector



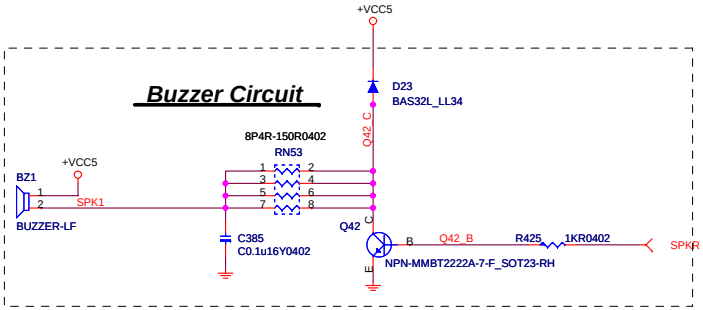
POWER LED

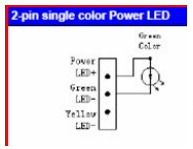


POWER BUTTON



Buzzer Circuit





HD (IDE Hard Disk Active LED)	Pin 1:LED anode(+) Pin 8:LED cathode(-)
(Power LED)	Pin 3:LED cathode(-) (green) Pin 2:LED cathode(-) (yellow)
Power Switch	Open:Normal Operation Close:Power on /Off

LED Status (Dual color LED)	
System State	Dual Color POWER LED State
S0	Steady Green
S1	Green Blinking (frequency is under 1Hz)
S3	Steady Yellow
S4/S5	Off
Default S5 in lose power .	Note series resistor is 330Ω

MICRO-START INT'L CO.,LTD.

Title		
ATX Connector / Front Panel / LED		
Size	Document Number: Lenovo IH61M	Rev: 1.0
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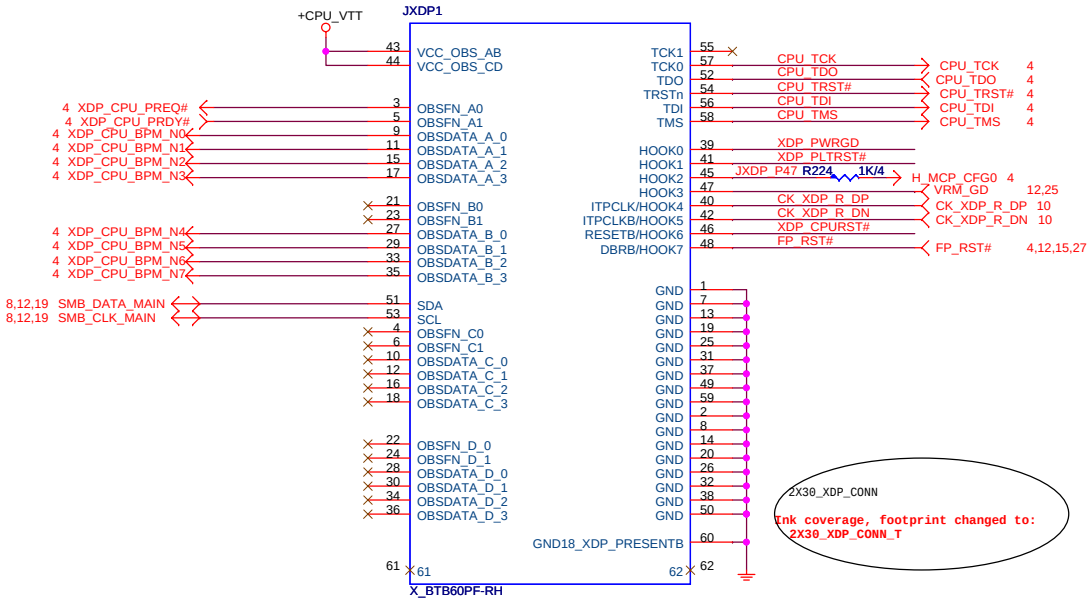
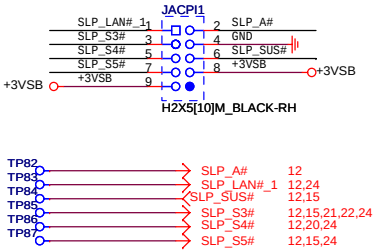
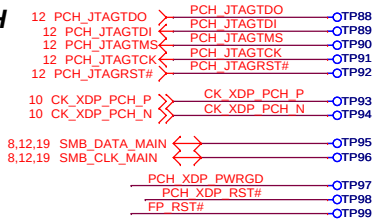
Reserve debug port 5020 for CPU

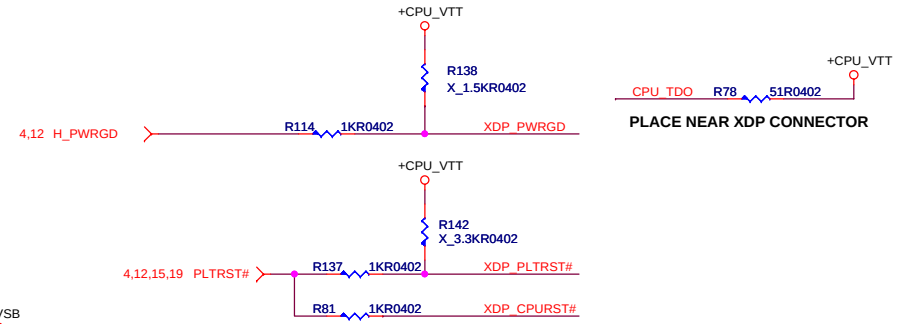


For INTEL TEST

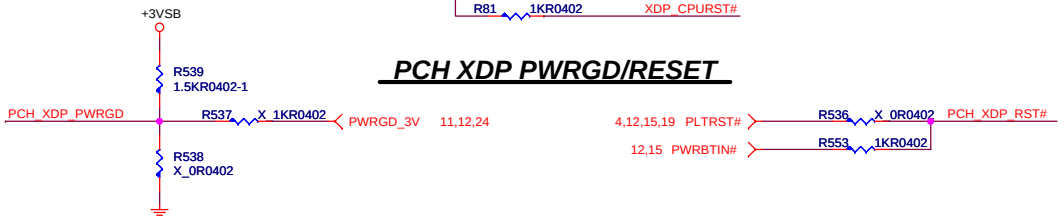


Reserve debug port 5020 for PCH

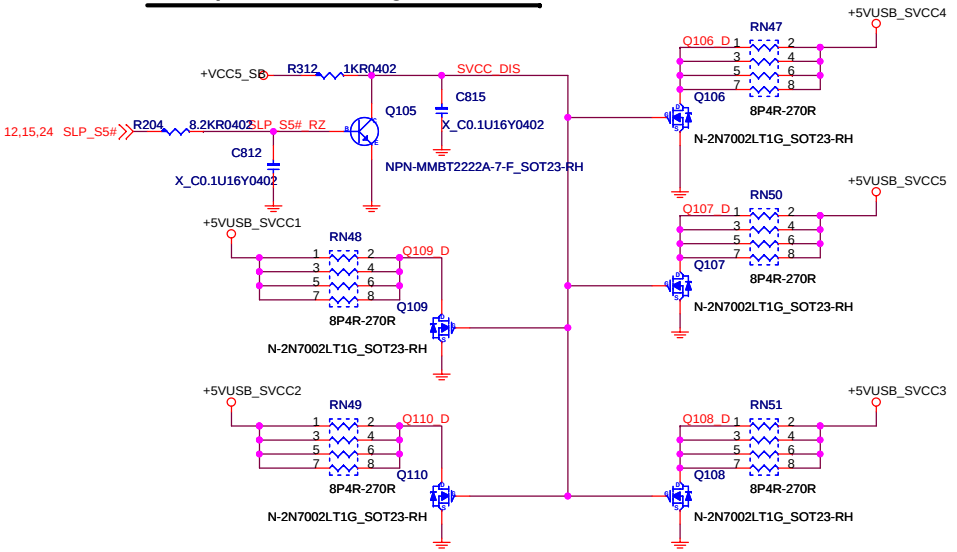




PCH XDP PWRGD/RESET



USB power discharge circuit



MSI MICRO-START INT'L CO.,LTD.

Title: USB PW-Discharge/BIOS_WP

Size	Document Number	Rev
	Lenovo IH61M	1.0

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Manual Parts

PCB1

P30-0768710-E36
PCB

P30-0768710-E36

XU1_X2

X_CPU RETENTION BACKPLATE

U3_X1

MEC1 MEC1

MEC2 MEC2

HS_31X31_1

XU1_X1

CPU SOCKET

+VCC5 +3VSB_LAN +VCC5_SB

C0.1u16Y0402 G732 C0.1u16Y0402 G733 C0.1u16Y0402 G734 C0.1u16Y0402 G735

+LAN_3VSB

C0.1u16Y0402 G736

U3_X1_1 卡钩

U3_X1_2 卡钩

VBAT-S1

BAT-BCR2032P-RH

USB_LAN

AUDIO CONN

RJ45_USBX2

Simulation

SIP2 SIM2 X_PIN1*2

+VCC3 SIP1 SIM1 X_PIN1*2

+CPU_GFX +VCC5 +5VDIMM +VCC3 +12V +PCH_1P05 +PCH_1P05 +3VSB +12VP_FET

C0.1u16Y0402 G729 C0.1u16Y0402 G699 C0.1u16Y0402C700 C0.1u16Y0402 G703 C0.1u16Y0402 C702 C0.1u16Y0402 G704 C0.1u16Y0402 G705 C0.1u16Y0402 G706 C707 C0.1u16Y0402 C708 C709 C0.1u16Y0402 C711 C0.1u16Y0402 C710

+12VIN +CPU_VTT +VCC_SA +VCC1_8 +VCC5_SB +ATX_5VSB +3VSB_LAN

C712 C0.1u16Y0402 C713 C714 C0.1u16Y0402 C716 C0.1u16Y0402 C715 C0.1u16Y0402 G717 C0.1u16Y0402 G718 C0.1u16Y0402 G726 C0.1u16Y0402 G727 C0.1u16Y0402 G728 C0.1u16Y0402 G722 C0.1u16Y0402 G719 C0.1u16Y0402 G720

PCB Mounting Holes

Mounting Holes

MH7 MH1 MH8 MH2 MH5 MH4 X_MH001

Optics Orientation Holes

Optical Fiducial Marks-120

FM12 FM16 FM15 FM9 FM2 FM11 FM13 FM1 X_FM

+VCC3 +VCC3 +VCC3 +VCC3

C681 C0.1u16Y0402 C682 C0.1u16Y0402 C683 C0.1u16Y0402 C684 C0.1u16Y0402

+VCC1_8 C0.1u16Y0402 G731

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Manual Parts & Option Parts

Size | Document Number: Lenovo IH61M | Rev: 1.0

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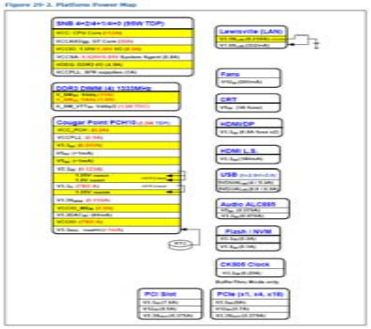

ATX POWER 2X24pin

+5V | +3.3V | +ATX_5VSB | +12V

ATX 2X2pin

+12V

MOSFET-p

+VCC5_SB

+3VSB 0.9A

+3VSB_LAN

DVI-D&VGA +DVI_PWR 1A

NCP6151S52MNR2G +NCP5901MNTBG
VCCP VRD12
4-Phase Switch

ISL95870BRUZ
CPU VTT
1.1V Switch

NCP5901MNTBG +NCP5901MNTBG
GFX Power
GFX Switch

Linear
VCC1_8
Linear 1.5A

UP7501
5VDIMM
5V PWM

NCP1587DR2G
VCC_DDR
1.5V Switch 17A

Linear
PCH Core Power
1.05V Linear 8.5A

UP7533 X5
USB Power
5V

UP7711
VTT_DDR
0.75V Linear 0.75A

LGA1155-CPU	
V Core	- 112A
1.05V CPU VTT	- 8.5A
1.5V VCC_DDR	- 4.5A
VCC_GFX	- 35A
VCC_1.8V VCCPLL (<0.8A)	- <0.8A
VCC_SA 0.925V/0.85V	- 8.8A

Cougar point PCH(5.5W TDP)	
1.05V Core:	- 6.7A
VCCCORE,VCCIO,VCCDMI,VccAPLLEXP, VccSATAPALL,VccADPLLA,VccADPLLB	
V1.8 S0:VCCVRM,VCCPNAND	35mA
3.3V Vcc3_3	357mA
V5 s0: V5REF	1mA
V5 s0: V5REF_SUS	1mA
VccSus3_3 3.3V VccHDA	123mA
VTT:V_CPU_IO	1mA
1.05V VCCME:VCCME,VCCLAN,	1800mA
3.3V VccSusHDA	6mA
VCCRTC	2mA

LAN 8111e	
+VDD10	- 300mA
3.3v	- 70mA

PCI Express x16 slot		
+12V		- 5.5 A
+3.3Vaux	(wake)	- 375mA
+3.3Vaux	(no wake)	- 20mA
+3.3V		- 3.0A

PCI Express x 1 slot		
+12V		- 0.5 A
+3.3Vaux	(wake)	- 375mA
+3.3Vaux	(no wake)	- 20mA
+3.3V		- 3.0A

PCI Express x 1 slot		
+12V		- 0.5 A
+3.3Vaux	(wake)	- 375mA
+3.3Vaux	(no wake)	- 20mA
+3.3V		- 3.0A

AUDIO ALC662	
+12V	- 0.07 A
+3.3V	- 0.07A

FAN	
+12V	- 0.6A

PS2		
+5V	(S0,S1)	- 345mA
+5V	(S3)	- 2.0mA

USB x10		
+5V	(S0,S1)	- 5.0A
+5V	(S3)	- 20mA

DDRIII x2 & TERMINATOR	
1.5V VCC_DDR(S0,S1)	-2.75A*2=5.5A
0.75V VTT_DDR	- 1A

3V Battery

MSI MICRO-START INTL CO.,LTD

Title: Power comsumption

Size | Document Number: Lenovo IH61M | Rev: 1.0

Date: Wednesday, February 23, 2011 Sheet 30 of 33

Table 2-27. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled low

Table 2-27. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT3# / GPIO55	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (Cougar Point inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high
GNT1#/ GPIO51/	Boot BIOS Strap bit 1 BBS1	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination:** 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GBE LAN. **NOTE:** PCI Boot BIOS destination is not supported on Mobile

Table 2-27. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
SATA1GP/ GPIO19	Boot BIOS Strap bit 0 BBS0	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination:** 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. **NOTE:** PCI Boot BIOS destination is not supported on mobile.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. **NOTE:** The internal pull-up is disabled after PLTRST# deasserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.

Table 2-27. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Port B Detected	Rising edge of PWROK	When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled high when strap is sampled.

NOTE: See Section 3.1 for full details on pull-up/pull-down resistors.

Table 2-27. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of RSMRST#	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. **NOTE:** The weak internal pull-down is disabled after PLTRST# deasserts. **NOTE:** Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel® Management Engine after chipset bringup and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	This signal has a weak internal pull-up. **NOTE:** The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. **NOTE:** The weak internal pull-down is disabled after RSMRST# deasserts. **NOTE:** A strong pull-up may be needed for GPIO functionality **NOTE:** This signal must be pulled up to support Intel RPAT and Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.

Title: History			
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PCH

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BMBUSY#	I/O	Core	3.3V	GPI	BM_BUSY#
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	NC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	NC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[9]	OC5#	I/O	Resume	3.3V	Native	USB_OCP#5
GPIO[10]	OC6#	I/O	Resume	3.3V	Native	USB_OCP#6
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	GPI	NC
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	OC7#	I/O	Resume	3.3V	Native	USB_OCP#7
GPIO[15]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[16]	SATA4GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	NC
GPIO[18]	PCIECLKRQ1#	I/O	Core	3.3V	Native	Pull-Hi
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[20]	PCIECLKRQ2#	I/O	Core	3.3V	Native	Pull-Hi
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	NC
GPIO[24]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[25]	PCIECLKRQ3#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[26]	PCIECLKRQ4#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[27]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[28]	unmuxed	I/O	Resume	3.3V	GPO	USB_MODE
GPIO[29]	SLP_LAN#	I/O	Resume	3.3V	GPI	NC
GPIO[30]	SUS_PWR_DN_ACK	I/O	Resume	3.3V	GPI	Pull-Hi
GPIO[31]	ACPRESENT	I/O	Resume	3.3V	GPI	Pull-Hi
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	NC
GPIO[34]	STP_PCI#	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	NC
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	USB_OCP#[1:4]
GPIO[44]	PCIECLKRQ5#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[45]	PCIECLKRQ6#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[46]	PCIECLKRQ7#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[47]	PEG_A_CLKRQ#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	NC
GPIO[49]	SATA5GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ#1
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT#1
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ#2
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT#2
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ#3
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT#3
GPIO[56]	PEG_B_CLKRQ#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[57]	unmuxed	I/O	Resume	3.3V	GPI	USB_DET1
GPIO[58]	SML1CLK	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	USB_OCP#0
GPIO[60]	SML0ALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[61]	SUS_STAT#	I/O	Resume	3.3V	Native	USB_DET2
GPIO[62]	SUSCLK	I/O	Resume	3.3V	Native	NC
GPIO[63]	SLP_S5#	I/O	Resume	3.3V	Native	SLP_S5#
GPIO[64:67]	CLKOUTFLEX	I/O	Core	3.3V	Native	NC
GPIO[72]	unmuxed	I/O	Resume	3.3V	Native	USB_DET3
GPIO[73]	PCIECLKRQ0#	I/O	Resume	3.3V	Native	PCIECLKRQ0#
GPIO[74]	SML1ALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[75]	SML1DATA	I/O	Resume	3.3V	Native	Pull-Hi

SIO(6776F)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[5:0]	UNUSED		
GPIO6	SKTOCC#	INPUT	
GPIO7	UNUSED		
GPIO10	BOARD_ID1		
GPIO11	BOARD_ID0		
GPIO12	LOW_PWR		
GPIO13	UNUSED		
GPIO14	UNUSED		
GPIO15	LED_VSB	OUTPUT	
GPIO16	LED_VCC	OUTPUT	
GPIO17	PAS_DET#	INPUT	
GPIO20	PLTRST_BUS1#	OUTPUT	PCI RESET BUFFER1
GPIO21	PLTRST_BUS2#	OUTPUT	PCI RESET BUFFER2
GPIO22	UNUSED		
GPIO23	UNUSED		
GPIO24	ATX_PWROK	INPUT	ATX POWER OK INPUT
GPIO26	PSIN#	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	SIO_PWROK	OUTPUT	RESERVE FOR PWRGD_3V
GPIO33	RSMRST#	OUTPUT	
GPIO40	UNUSED		
GPIO41	DVI_C_HPD_DP		
GPIO42	FP_AUD_DET#	INPUT	FRONT AUDIO CABLE DETECTION
GPIO43	UNUSED		

DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	00	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 2	10	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

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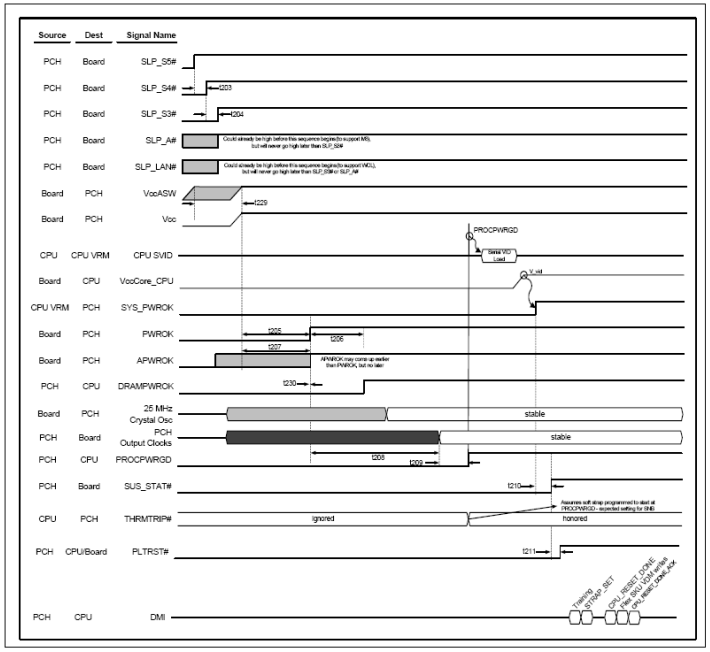
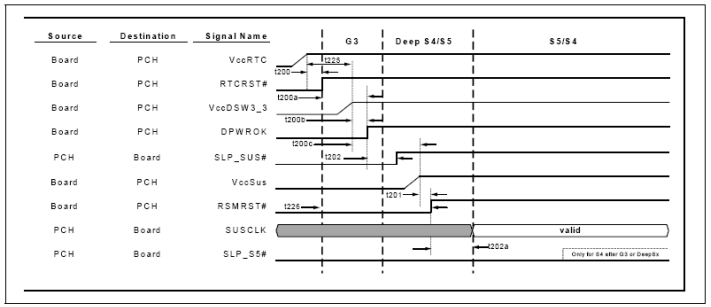
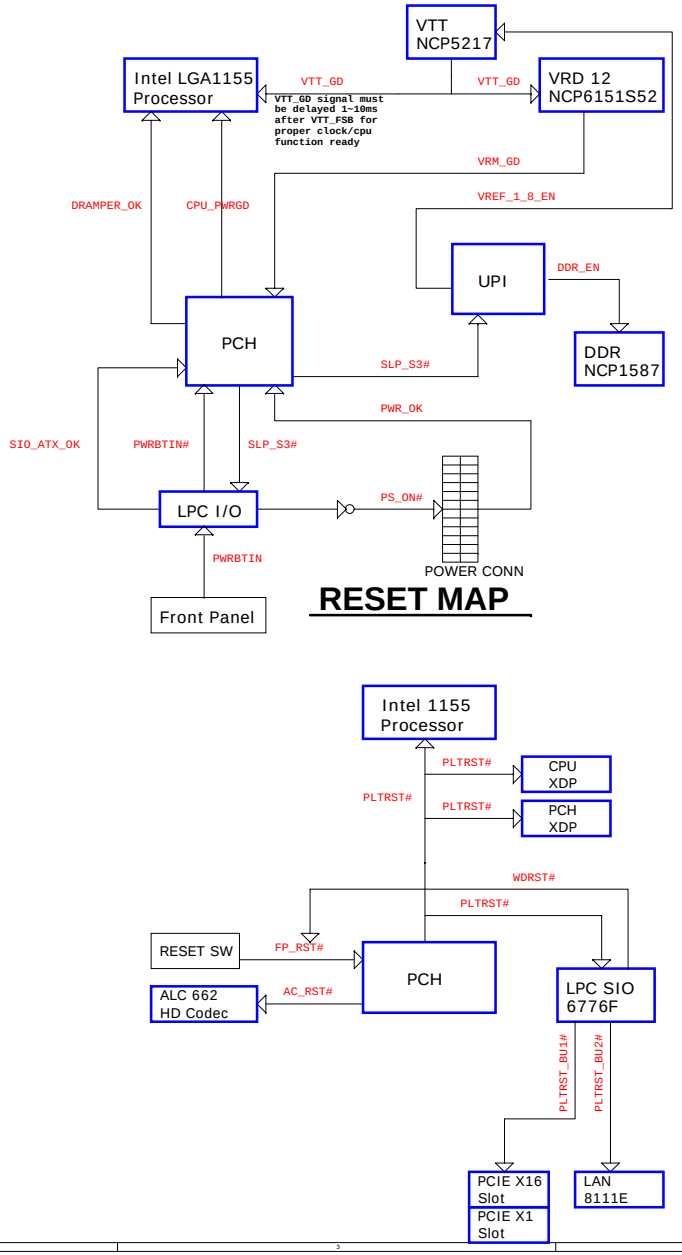
PWROK MAP

S5 to S0 Timing Diagram



G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram





RESET MAP

12V
5V
3.3V
5VDRV1
VCC_1_8REF
PCH_1_8
PCH_Core(1.05V)
CPU_VTT
DDR_EN
VCC_DDR
CPU_VTT_PWG
CPU_VCCP
VRM_PWG
ATX_POK(SIO_ATX_POK)
PL_RST
PCI_RST

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Title	Reset & PWROK map	
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