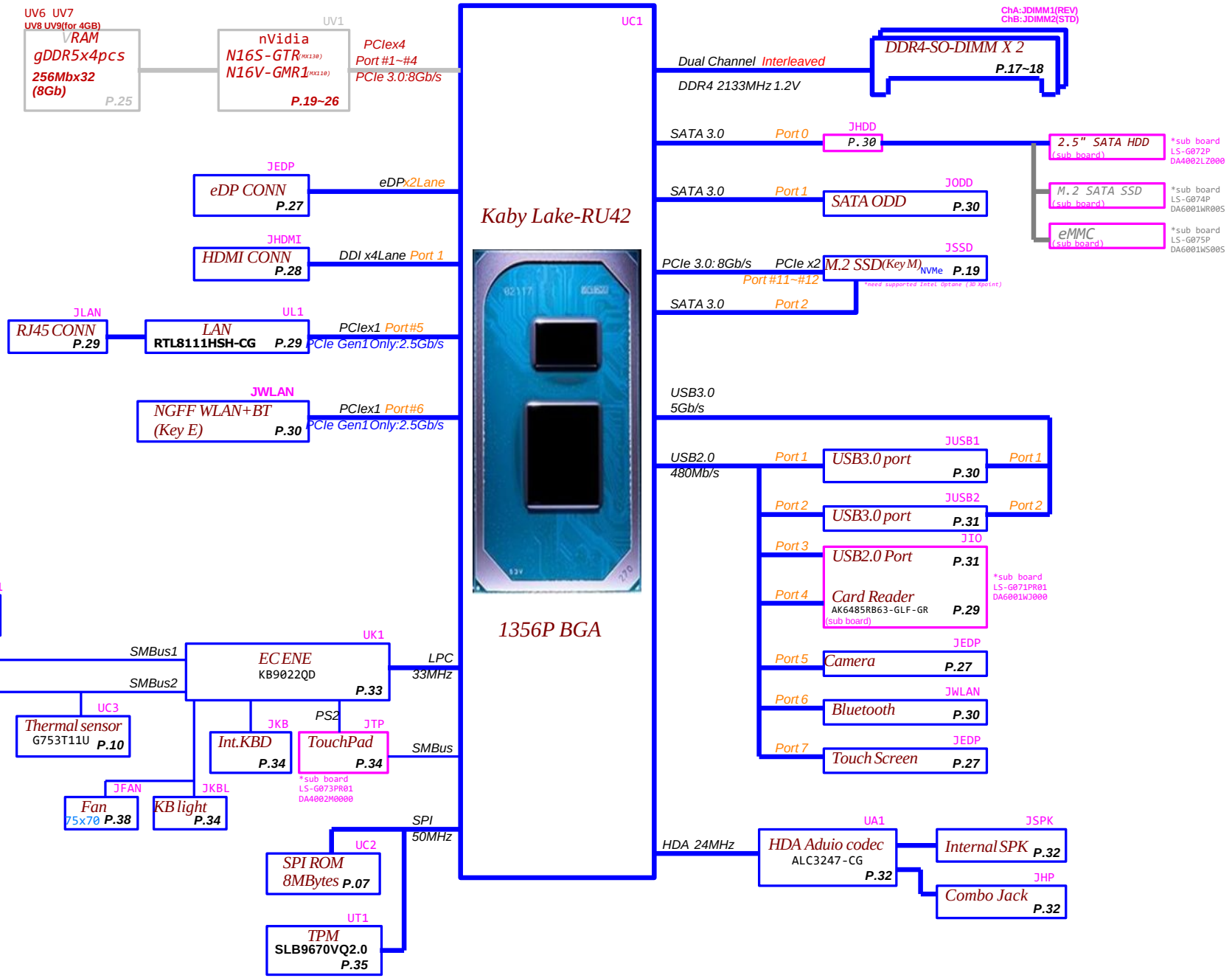
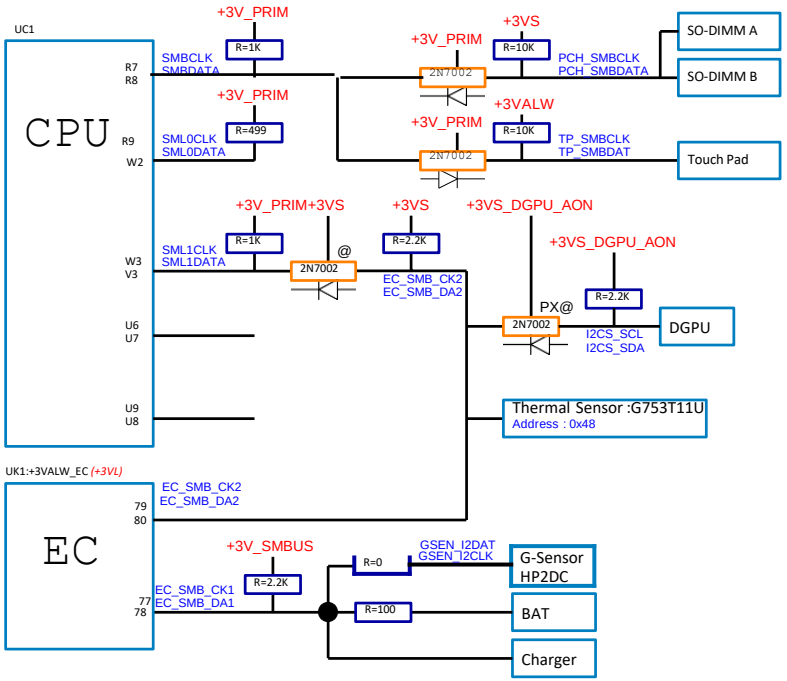


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date 2018/08/24	Title: Block Diagrams

Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L)		Rev: v0.3
Date: Monday, January 08, 2018	Sheet 2	of 59	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/15	Deciphered Date 2019/12/15	Title: Notes List
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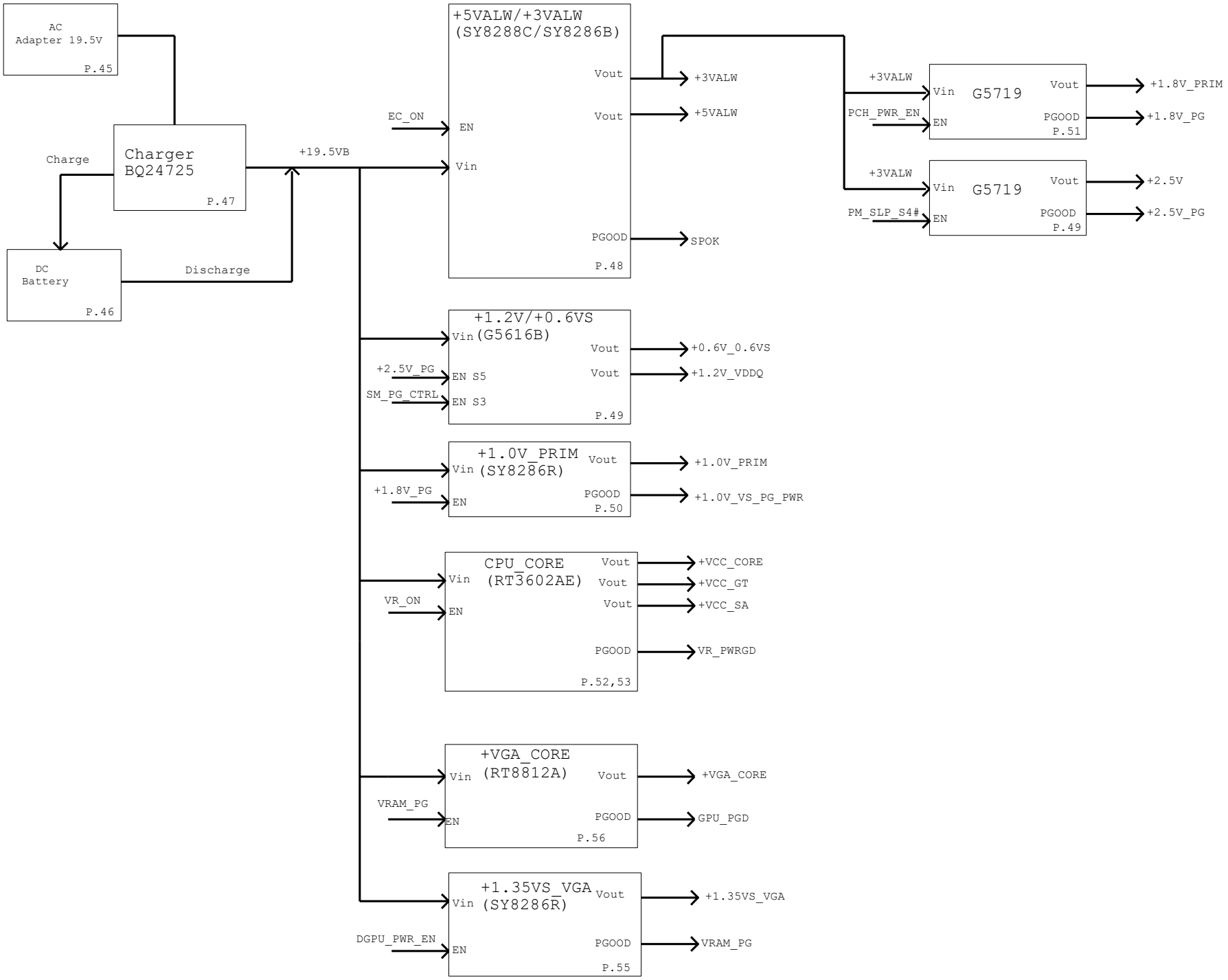
			Date: Friday, January 05, 2018; Sheet 3 of 99



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

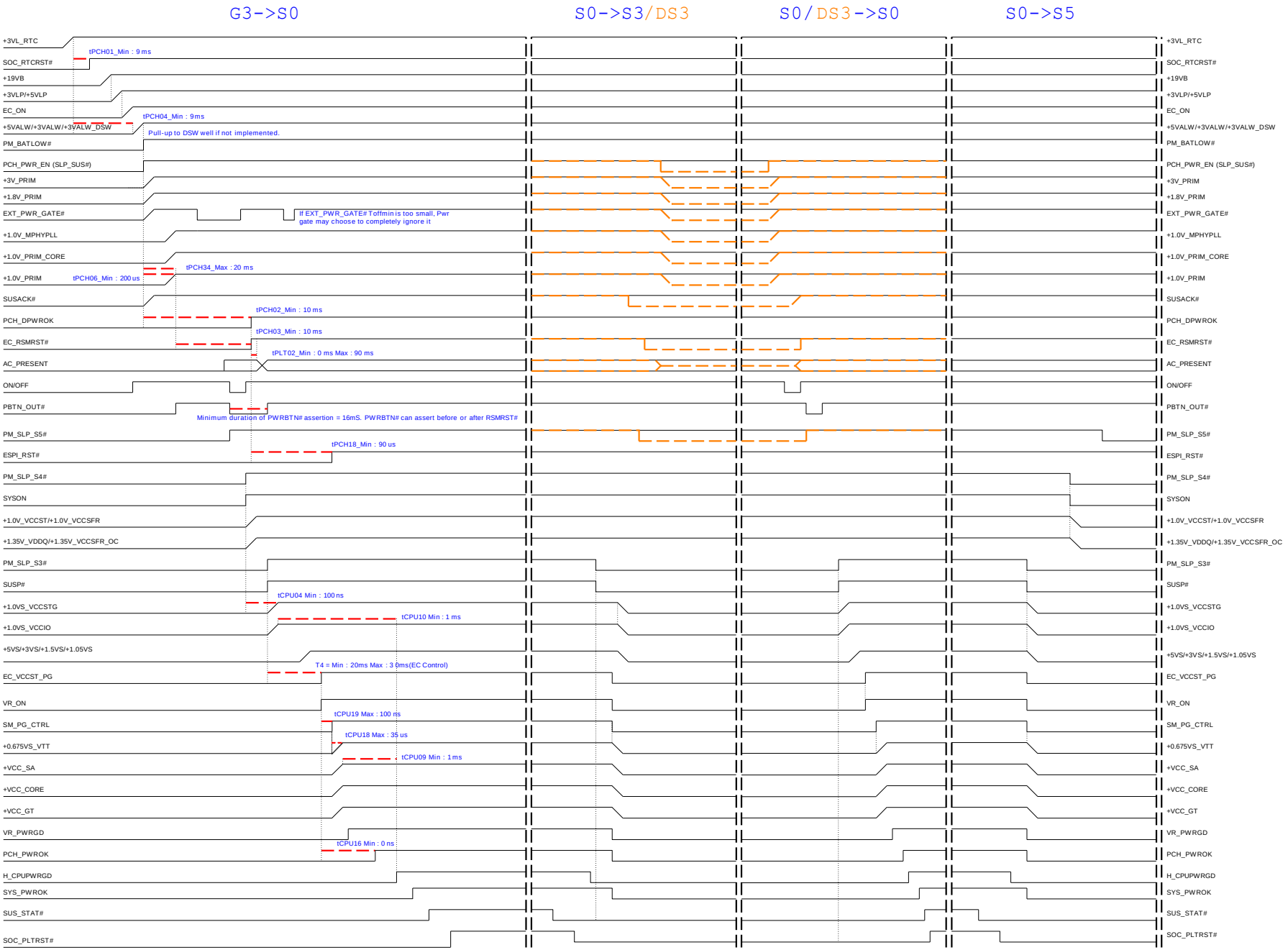
Compal Electronics, Inc.

Title: *Power Block Diagram*

Size: | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 58 of 59

[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: HW Reserve

Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L)		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 4 of 59		

SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

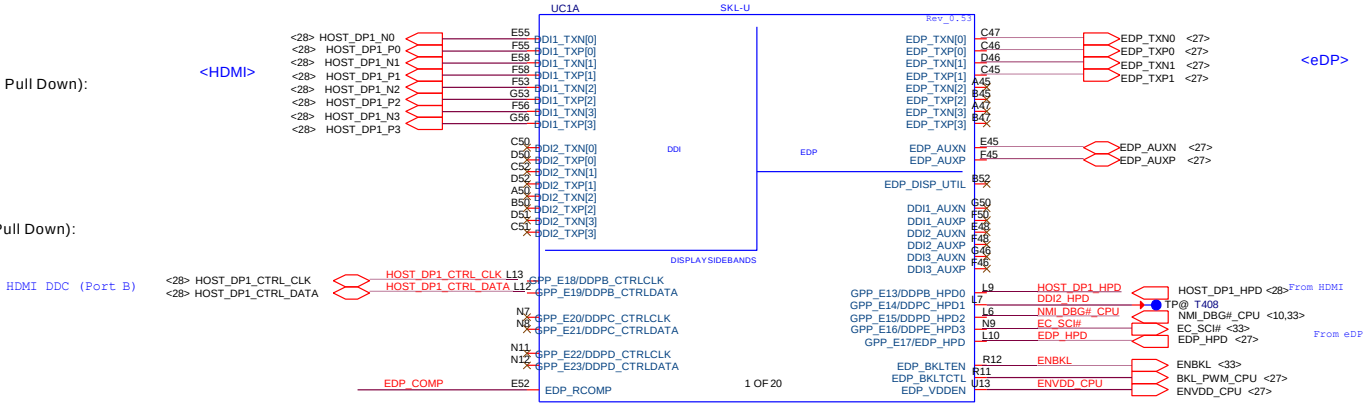
1 = Port B is detected.

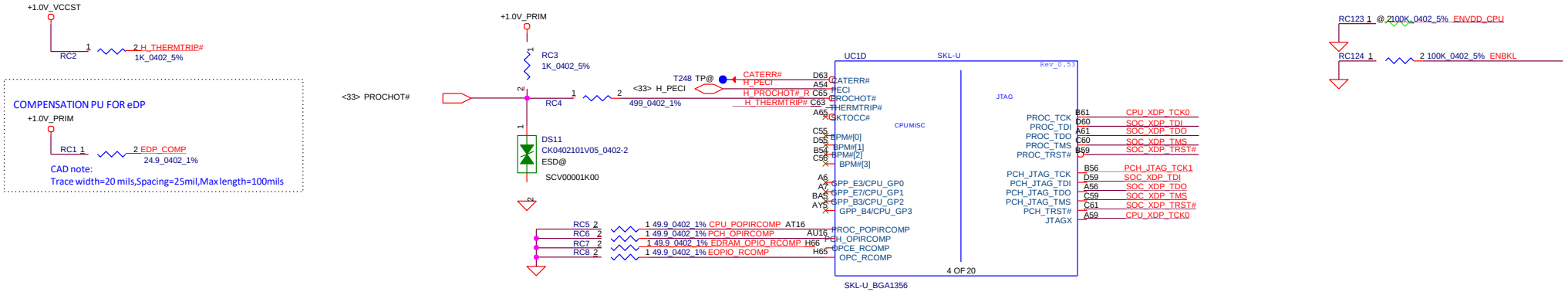
SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.





XDP CONN

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

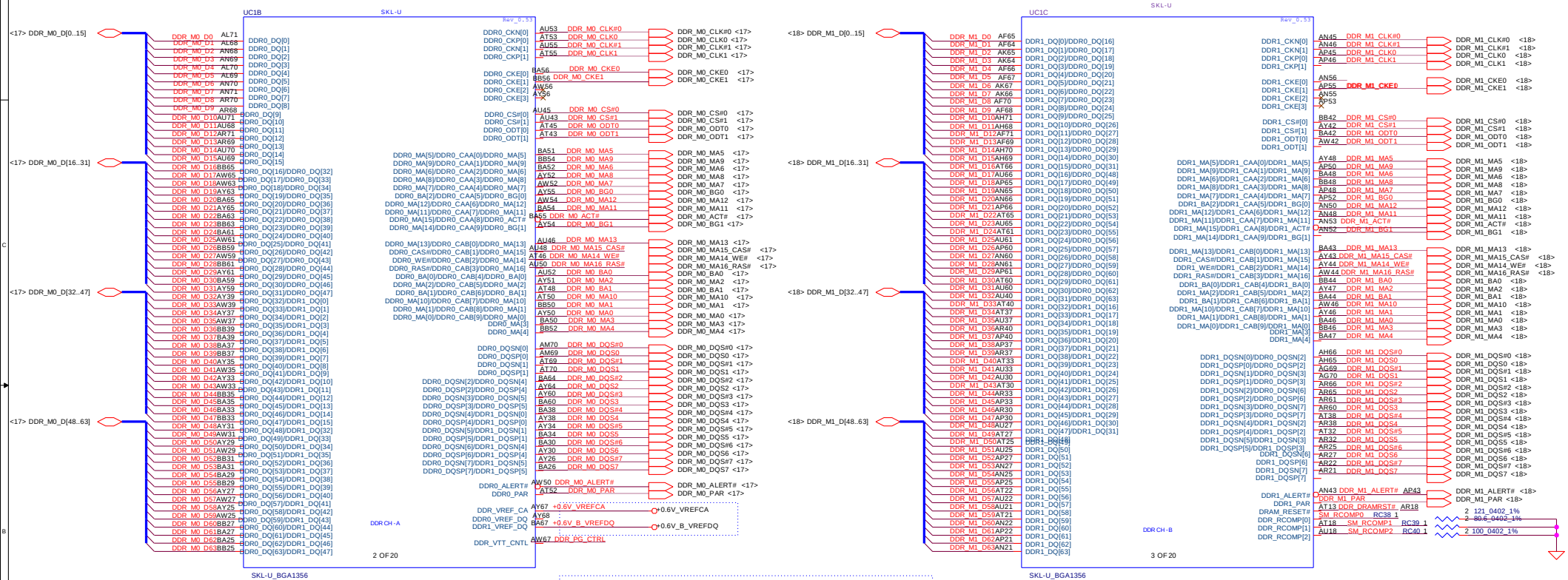
Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

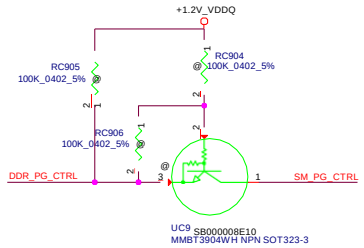
Date: Friday, January 05, 2018 | Sheet 5 of 59

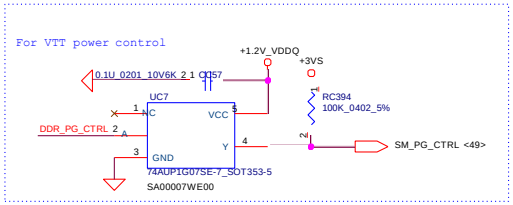
Interleaved Memory

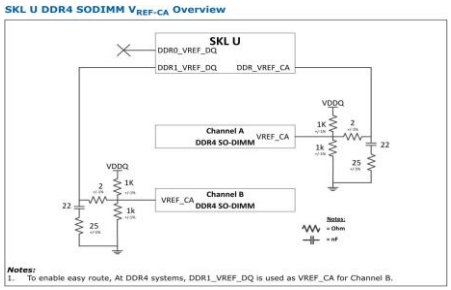
Interleaved Memory

<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)









Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.			
Title: SKL-U(2/12)DDRIII			
Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L)		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 6	of 59	

SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E SKL-U

SPI-FLASH

<35> HOST_SPI_0_SO
<35> HOST_SPI_0_SI
<35> HOST_SPI_0_CS2#

HOST_SPI_0_CLK AV2 SPI0_CLK
HOST_SPI_0_SO AW3 SPI0_MISO
HOST_SPI_0_SI AV3 SPI0_MOSI
HOST_SPI_0_SIO2 AW2 SPI0_IO2
HOST_SPI_0_SIO3 AU4 SPI0_IO3
HOST_SPI_0_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
HOST_SPI_0_CS2# AU1 SPI0_CS2#

SPI-TOUCH

M2 GPP_D1/SPI1_CLK
M4 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

CLINK

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

SMBUS, SMLINK

GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 SMBALERT# TP@ T239

GPP_C3/SML0CLK R9 SML0CLK
GPP_C4/SML0DATA W2 SML0DATA
GPP_C5/SML0ALERT# W1 SML0ALERT#

GPP_C6/SML1CLK W3 SML1CLK
GPP_C7/SML1DATA V3 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 1 2 SML1ALERT#
RC902 @ 0_0201_5% TP@ T234

LPC

GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0 <33>
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1 <33>
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2 <33>
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3 <33>
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# <33>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT# TP@ T2402

<33> EC_KBRST# EC_KBRST# AW13 GPP_A0/RCIN#
To TPM <33,35> SERIRQ SERIRQ AY11 GPP_A6/SERIRQ
LPC Mode

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI0 RC387 1 2 22_0402_5% CLK_PCI_LPC <33>
GPP_A10/CLKOUT_LPC1 AY9
GPP_A8/CLKRUN# AW11 PM_CLKRUN PM_CLKRUN# <33>
CC182 22P 50V J NPO 0402 EMI@

5 OF 20

SKL-U_BGA1356

SMB
(Link to XDP, DDR, TP)

SML1
(Link to EC,DGPU, LAN, Thermal Sensor)

SML0ALERT# RC218 1K_0402_1%

+3V_PRIM
SML1ALERT# RC903 2 @ 1 150K_0402_1%
SML0ALERT# RC360 2 @ 1 10K_0402_5%
+3VS
SMBALERT# 8 1
EC_KBRST# 7 2
6 3
5 4
RPC19 10K_0804_8P4R_5%
To EC

SPI ROM (8MByte Only)

Go SPI ROM UC2 Source From

RPH11
HOST_SPI_0_CS0#_R 1 8 EC_SPI_CS0#
HOST_SPI_0_CS0#_R 2 7 HOST_SPI_0_CS0#
HOST_SPI_0_SO_R 3 6 EC_SPI_SO
HOST_SPI_0_SO_R 4 5 HOST_SPI_0_SO
15_0804_8P4R_5%
EC_SPI_CS0# <33>
EC_SPI_SO <33>

RPH12
HOST_SPI_0_HOLD# 1 8 HOST_SPI_0_SIO3
HOST_SPI_0_SI_R 2 7 HOST_SPI_0_SI
HOST_SPI_0_SI_R 3 6 EC_SPI_SI
4 5
15_0804_8P4R_5%
EC_SPI_SI <33>

HOST_SPI_0_WP# 2 RC388 1 HOST_SPI_0_SIO2 15_0402_5%

+3V_SPI
CC8 1 2 0.1U_0201_10V6K

UC2
HOST_SPI_0_CS0#_R 1 CS# VCC 8 HOST_SPI_0_HOLD#
HOST_SPI_0_SO_R 2 DO(IO1) HOLD#(IO3) 7 HOST_SPI_0_CLK_R
HOST_SPI_0_WP# 3 WP#(IO2) CLK 6 HOST_SPI_0_SI_R
4 GND DI(IO0) 5
XM25QH64AHIG SOP 8P
SA0000B8300 SPI ROM Part:
ACES_91960-0084L_8P-T
Main:SA0000B8300, S IC FL 64M XM25QH64AHIG SOP 8P(XMC)
2nd: SA000039A40, S IC FL 64M W25Q64JVSSIQ SOIC 8P SPI ROM(Winbond)
3th: SA000085L00, S IC FL 64M MX25L6473FM2I-08G SOP 8P(MXIC)
Use socket footprint

+3VS
RC216 10K_0402_5% RC215 10K_0402_5%
QC1A SMBCLK 6 1 PCH_SMBCLK <17,18>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
QC1B SMBDATA 3 4 PCH_SMBDATA <17,18>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00

+3VS
<DB> Un-pop QC2 for new 0x90 thermal sensor
SML1CLK 6 QC2A 1 EC_SMB_CK2 <10,33>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
SML1DATA 3 QC2B 4 EC_SMB_DA2 <10,33>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00

+3V_PRIM
SML0CLK RC49 1 2 499_0402_1%
SML0DATA RC50 1 2 499_0402_1%
RPC7
SML1CLK 1 8
SML1DATA 2 7
SMBCLK 3 6
SMBDATA 4 5
1K_0804_8P4R_5%

+3V_SPI
HOST_SPI_0_SIO2 RC3901 @ 2 1K_0402_1%
HOST_SPI_0_SIO3 RC3911 @ 2 1K_0402_1%
HOST_SPI_0_CS0#_R 1 @ 2 RC357 1K_0402_5%

+3V_PRIM +3VALW
RC81 10K_0402_5% RC82 10K_0402_5%
SB00001FF00
SMBCLK 1 QC7A 6 TP_SMBCLK <34>
L2N7002SDW1T1G 2N SC88-6
SMBDATA 4 QC7B 3 TP_SMBDATA <34>
SB00001FF00
L2N7002SDW1T1G 2N SC88-6

HOST_SPI_0_SIO3 RC51 1 ES@ 2 1K_0402_1%
From WW36 MOW for SKL-U ES sample

+3VS_PGPPA
PM_CLKRUN# RC107 1 2 8.2K_0402_5%
SERIRQ RC122 1 2 8.2K_0402_5%

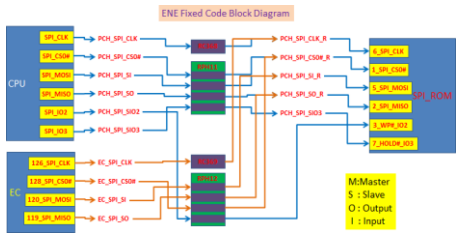
Follow 543016_SKL_U_Y_PDG_0_9

CLK Source CPU

Go SPI ROM UC2&EC

HOST_SPI_0_CLK 2 RC368 15_0402_5% EMI@ 1 HOST_SPI_0_CLK_R HOST_SPI_0_CLK_R <33,35>
CC9 10P_0402_50V8J @EMI@

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P MXIC SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M M25Q064A13ESEC0F SO8W 8P



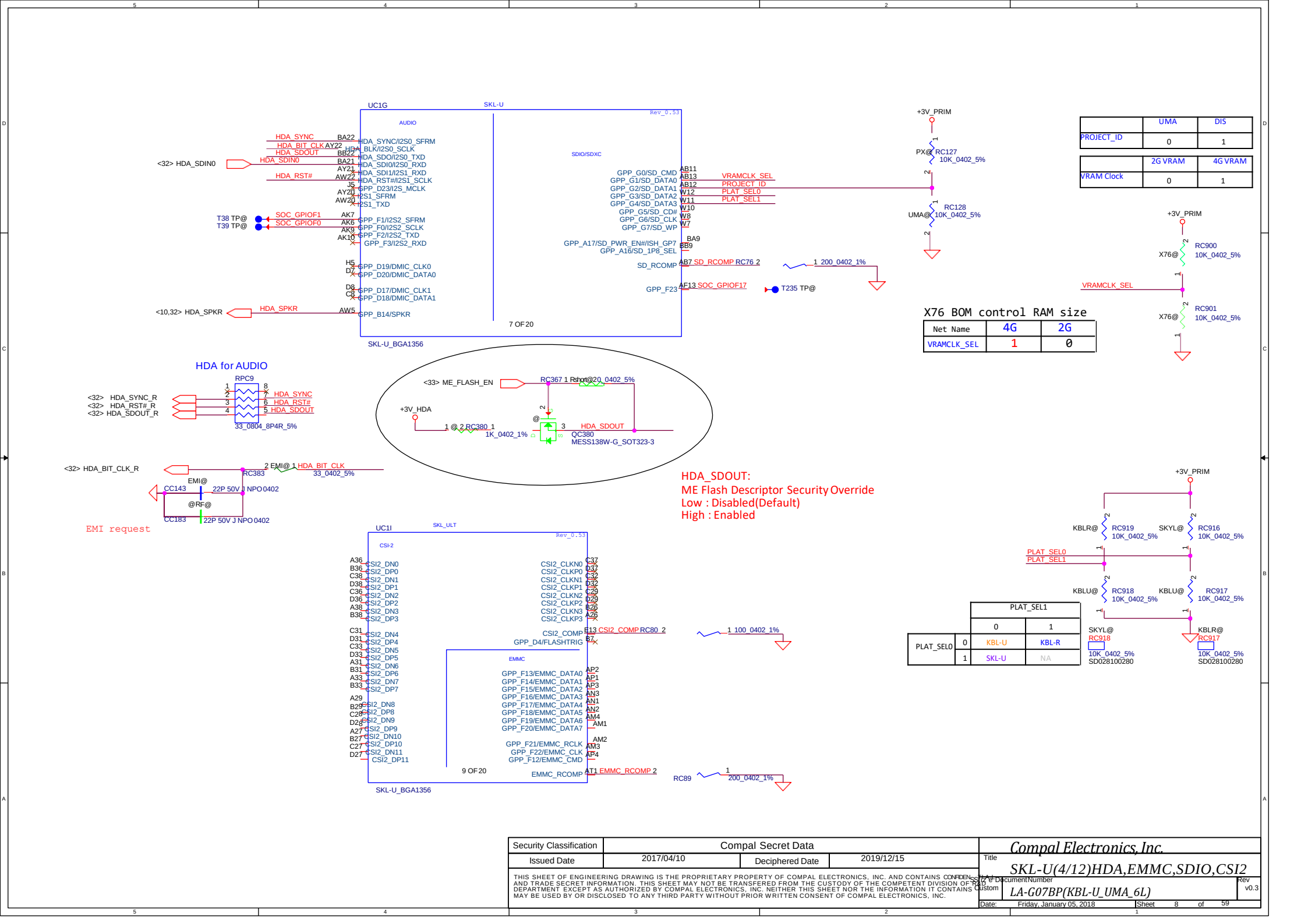
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 7 of 59



	UMA	DIS
PROJECT_ID	0	1

	2G VRAM	4G VRAM
VRAM Clock	0	1

X76 BOM control RAM size

Net Name	4G	2G
VRAMCLK_SEL	1	0

PLAT_SEL0	PLAT_SEL1 = 0	PLAT_SEL1 = 1
0	KBL-U	KBL-R
1	SKL-U	NA

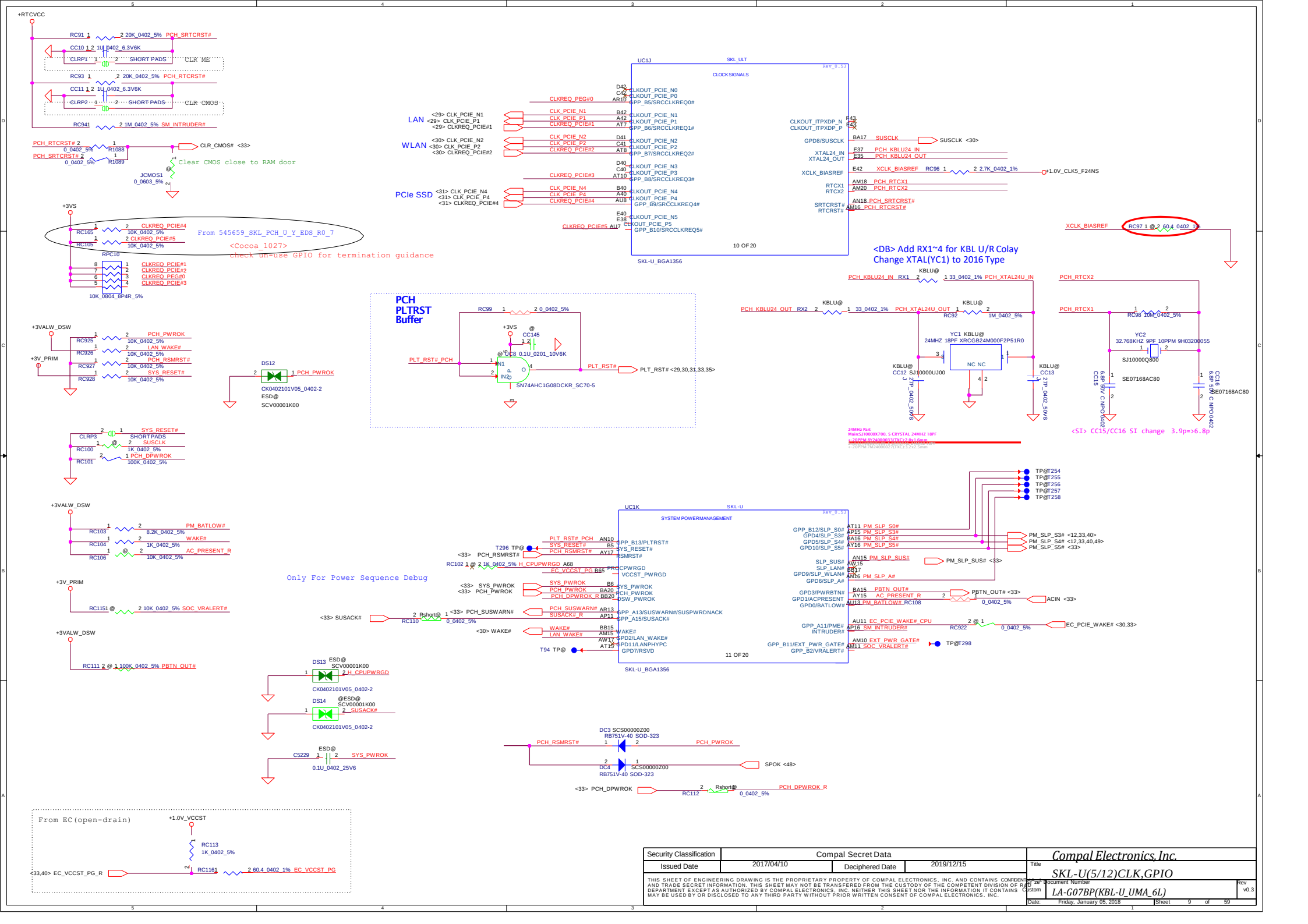
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

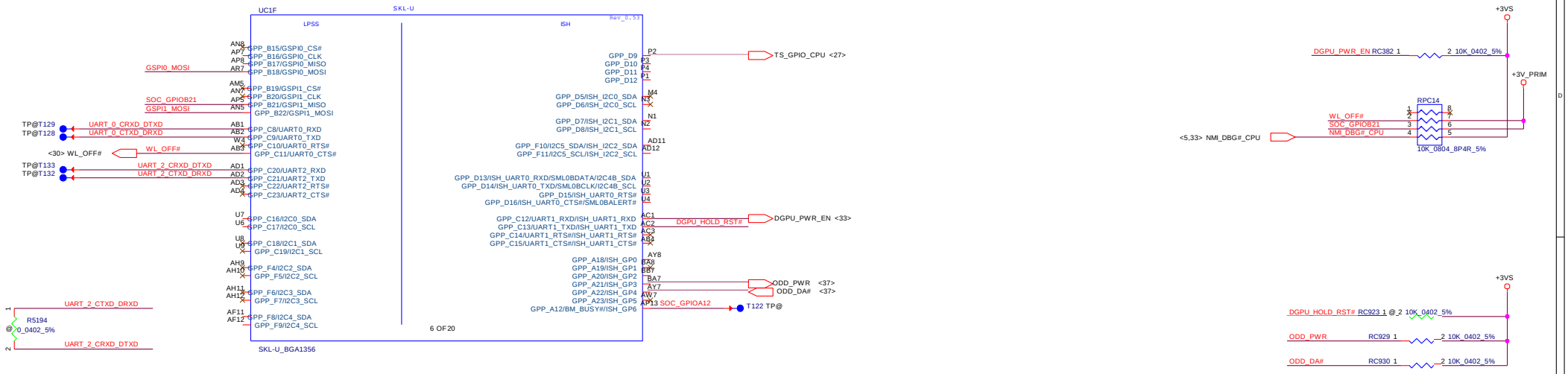
Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 8 of 59



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.			
Title: SKL-U(5/12)CLK,GPIO			
Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L)		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 9 of 59		



Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

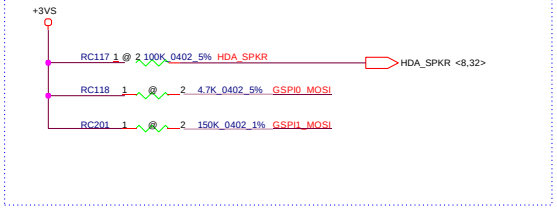
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

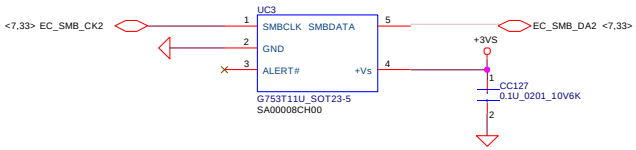
1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR

Address : 0x48



<DB> Change Thermal Sensor IC

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 10 of 59

UC1H

SKL-U

Rev_0.53

PCIE/USB3/SATA

SSIC /USB3

USB2

8 OF 20

SKL-U_BGA1356

LAN

WLAN

HDD

ODD

M.2 SSD

USB2.0/USB3.0

USB2.0/USB3.0

USB2.0/USB3.0

USB2.0

Card Reader

Camera

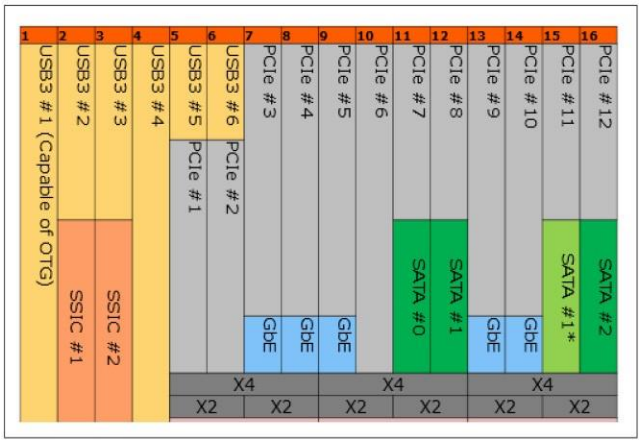
BT

TS

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
						Cycle Router #2				Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3		RP5				RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5				RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6			RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

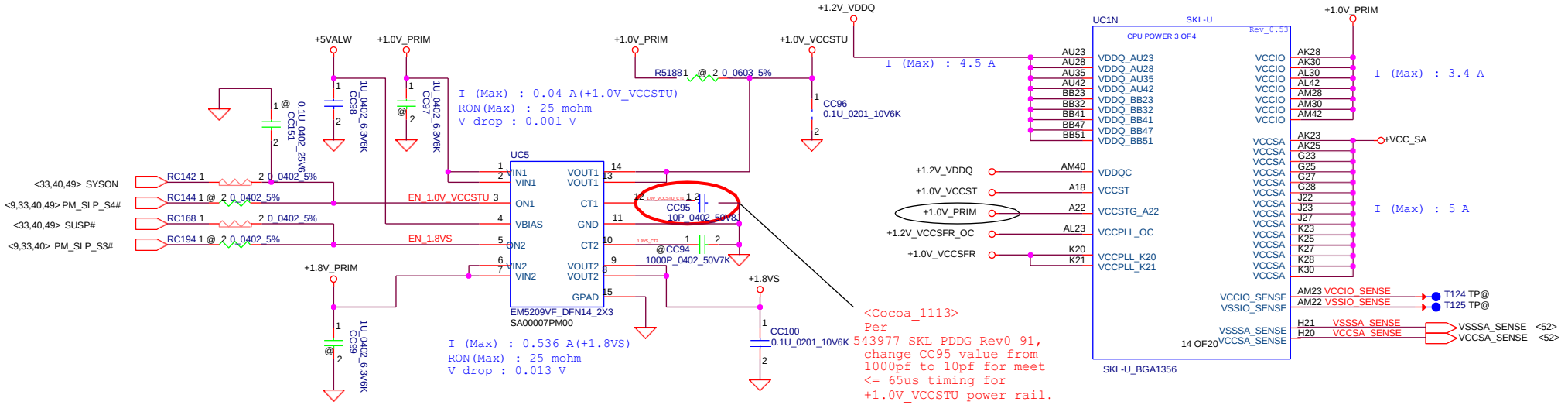
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

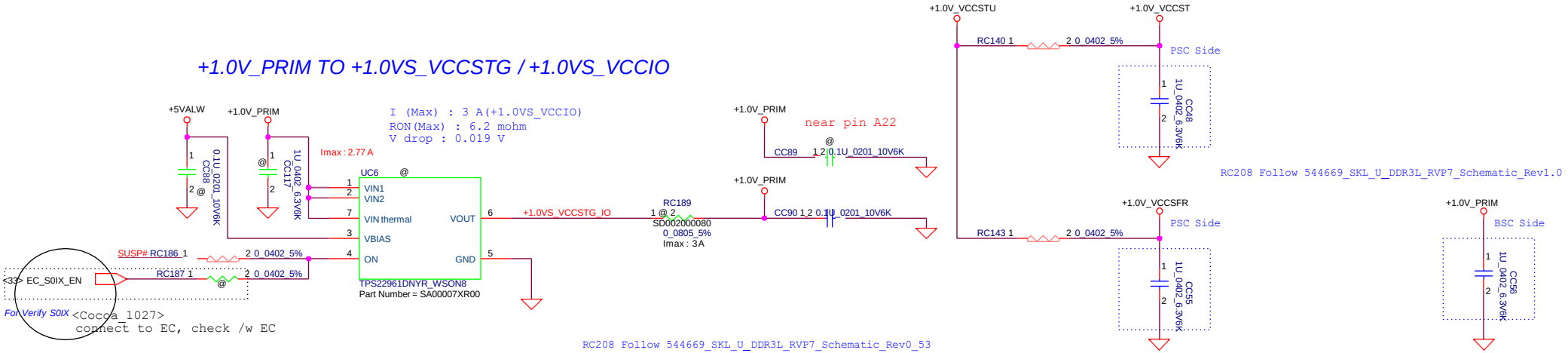
Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

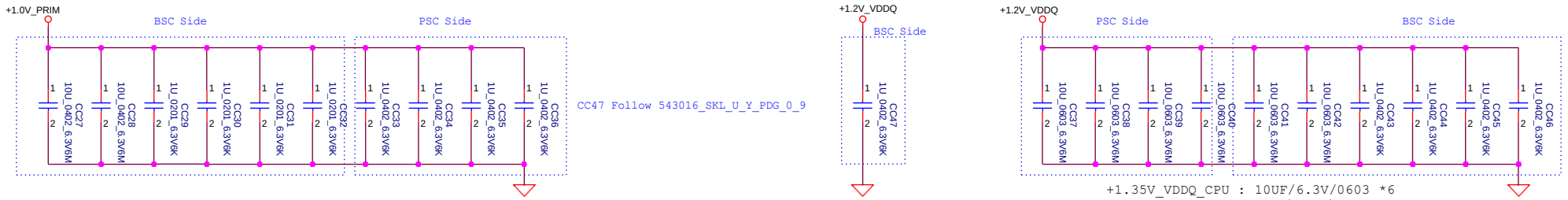
Date: Friday, January 05, 2018 | Sheet 11 of 59

+1.0V_PRIM TO +1.0V_VCCSTU



+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO





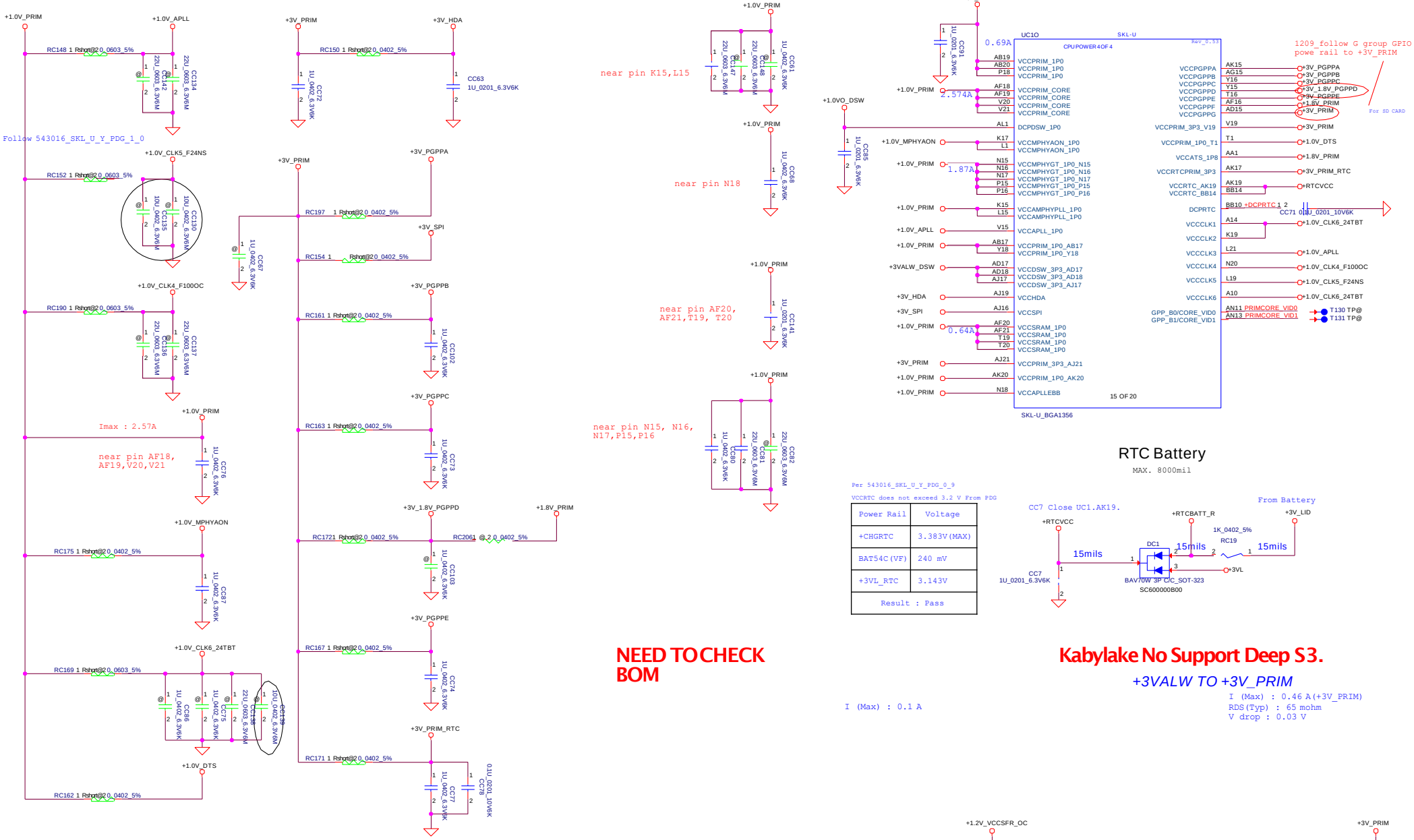
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 12 of 59



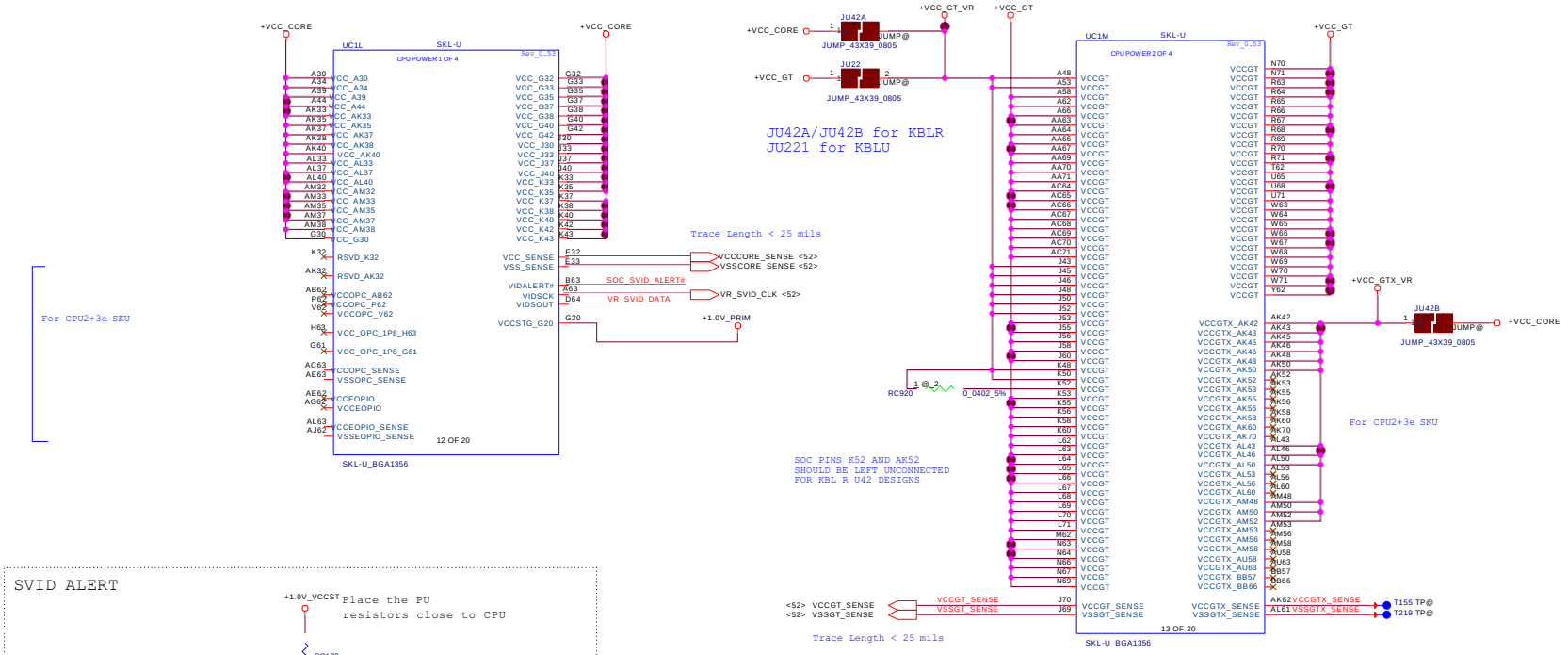
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

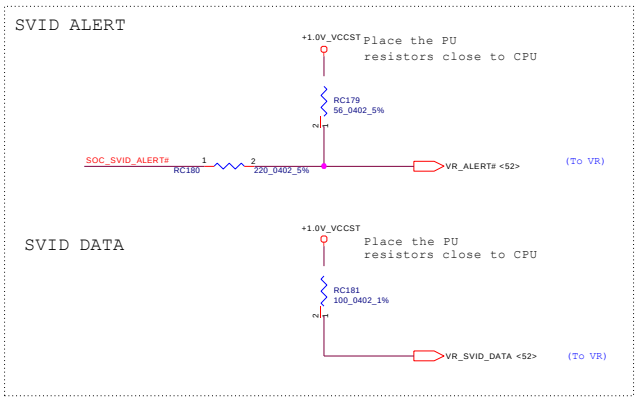
Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 13 of 59





Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.

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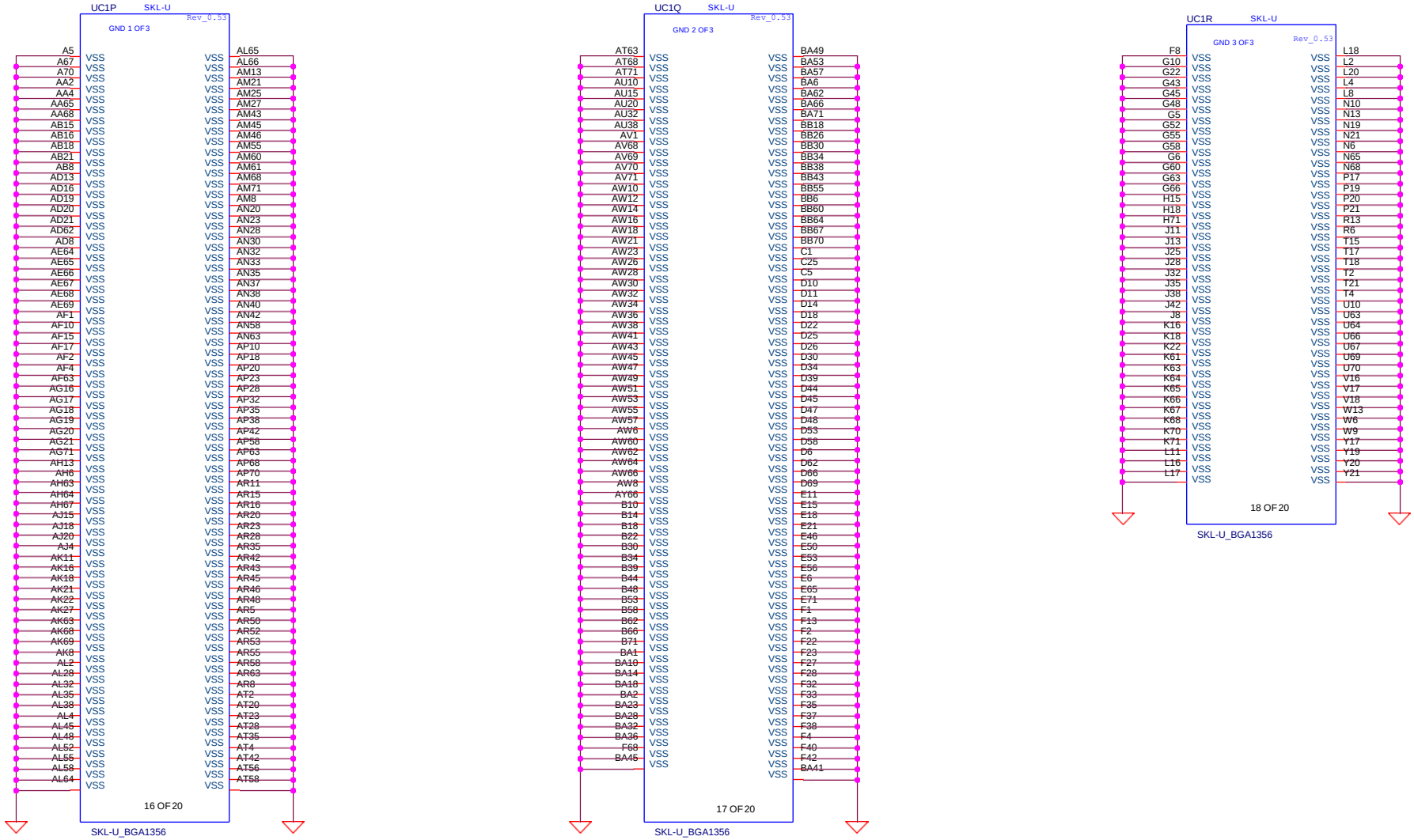
Issued Date	2017/04/10	Deciphered Date 2019/12/15	Title: SKL-U(10/12)Power,SVID
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDEN AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R& DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: D, Custom; Document Number: LA-G07BP(KBL-U_UMA_6L); Rev: v0.3
			Date: Friday, January 05, 2018; Sheet 14 of 59



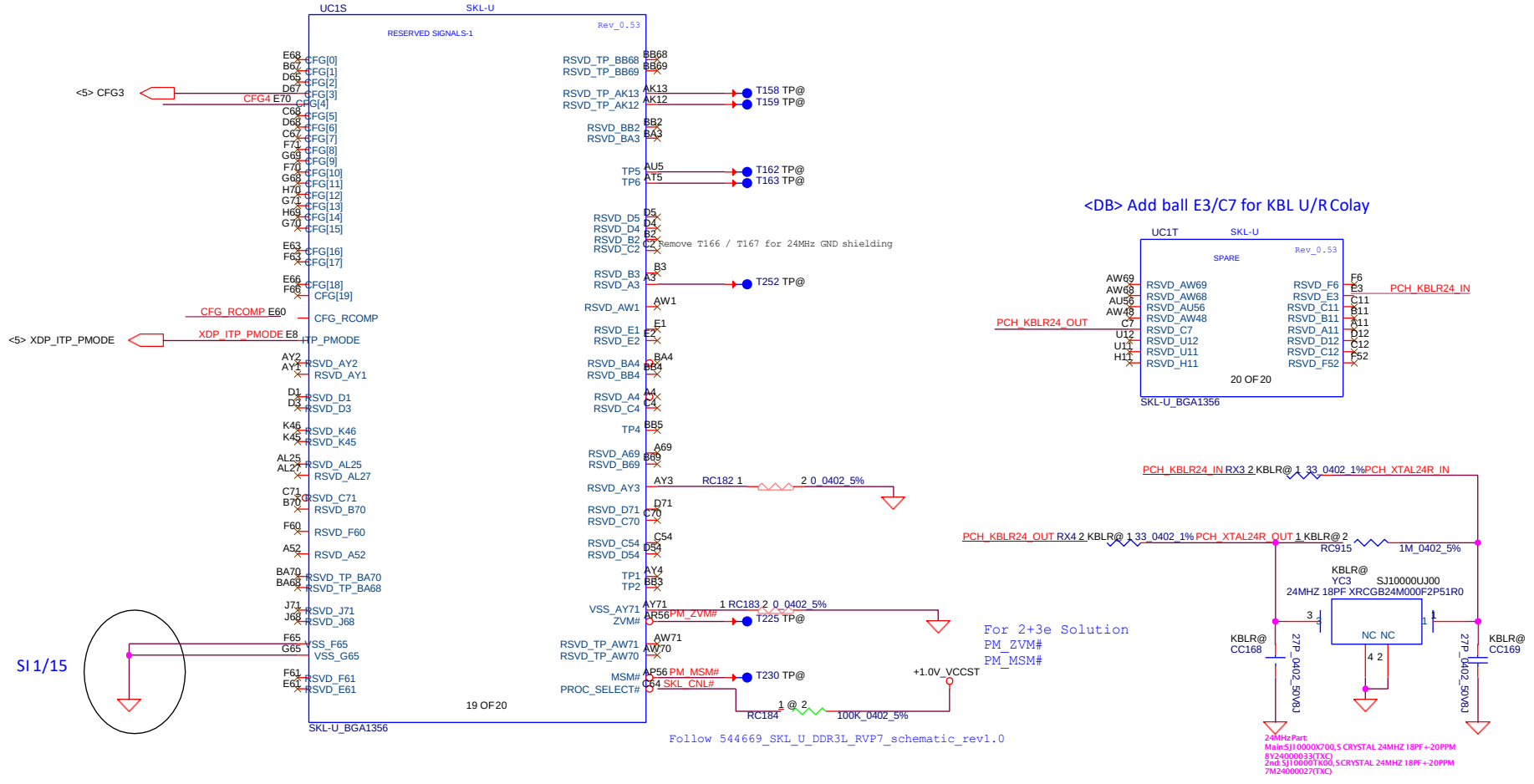
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

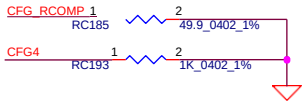
Compal Electronics, Inc.

Title: SKL-U(11/12)GND

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 15 of 59





Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.			
Title: SKL-U(12/12)RSVD			
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Date: Friday, January 05, 2018	Sheet 16 of 59		

CHANNEL-A

REVERSE TYPE

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
PLACE THE CAP near JDIMM1. 164

Layout Note:
Place near JDIMM1

PLACE NEAR TO PIN

PLACE NEAR TO SODIMM

Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

9/8 Modify

For ECC DIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: P18-DDRIV_CHA: DIMM0

Size: C | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

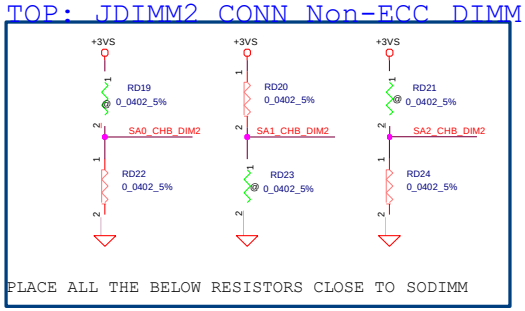
Date: Friday, January 05, 2018 | Sheet 17 of 59

CHANNEL-B

Interleaved Memory

STD (5.2 mm)

TOP: JDIMM2 CONN Non-ECC DIMM

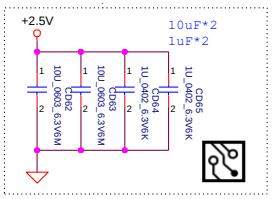


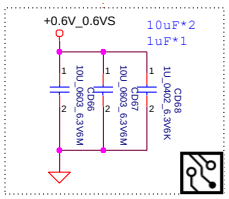
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

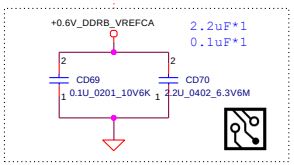
Layout Note:
Place near JDIMM2.257,259

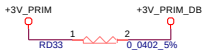
Layout Note:
Place near JDIMM2.258



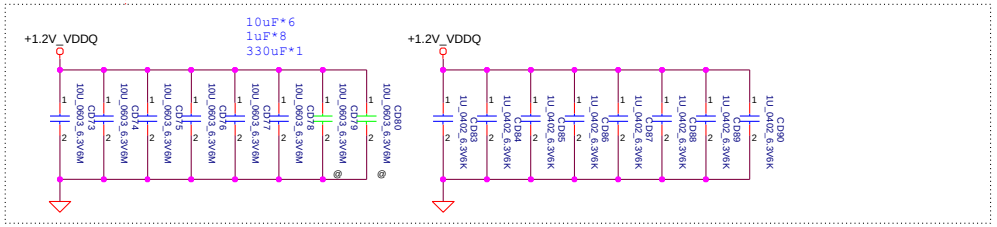


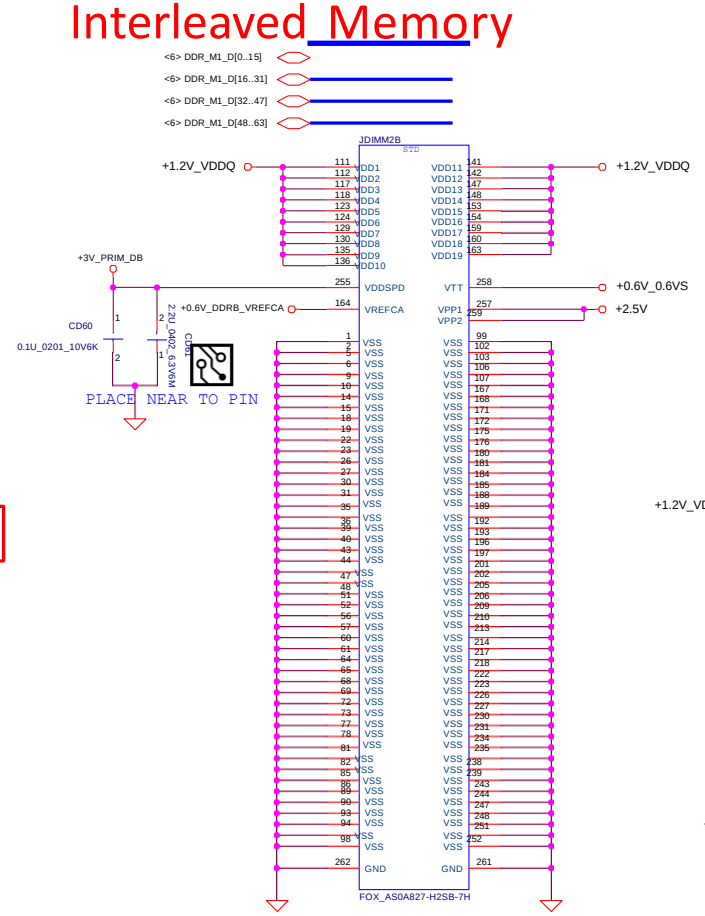
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



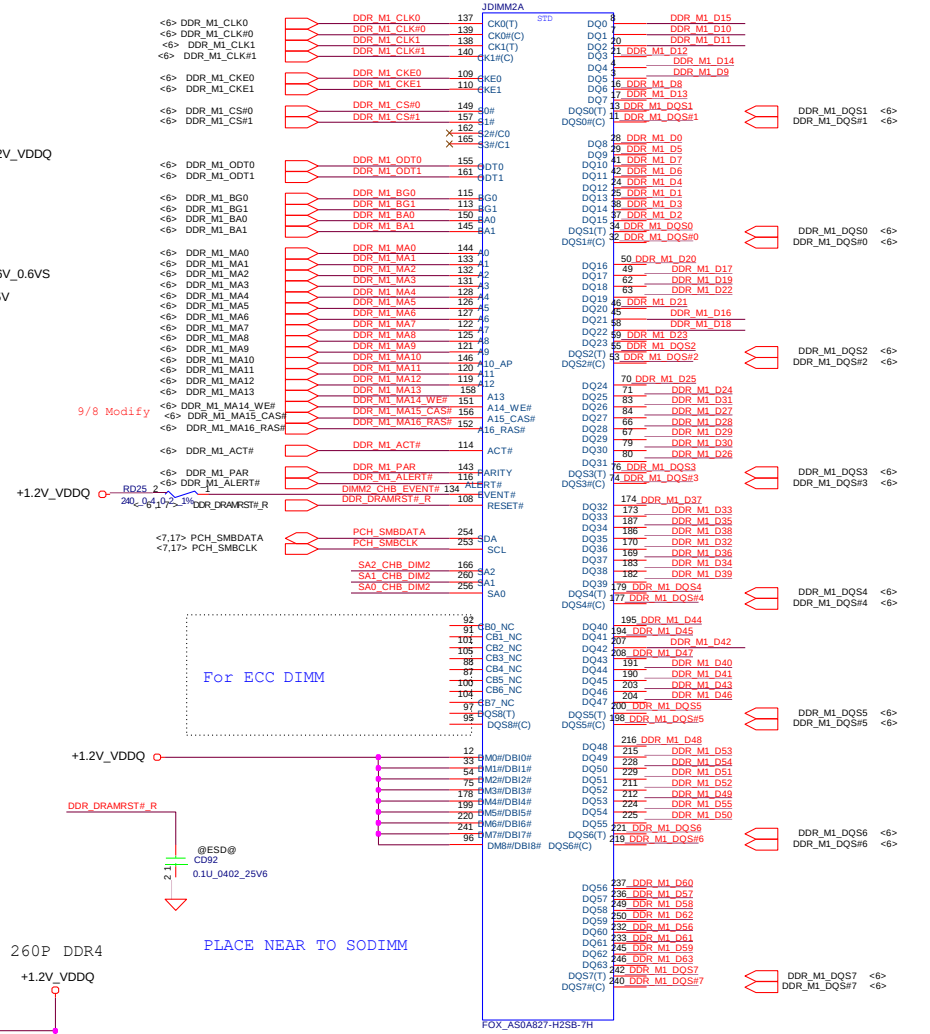


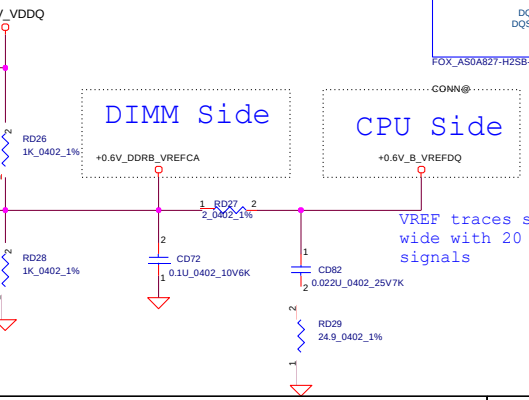
Layout Note:
Place near JDIMM2





Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4





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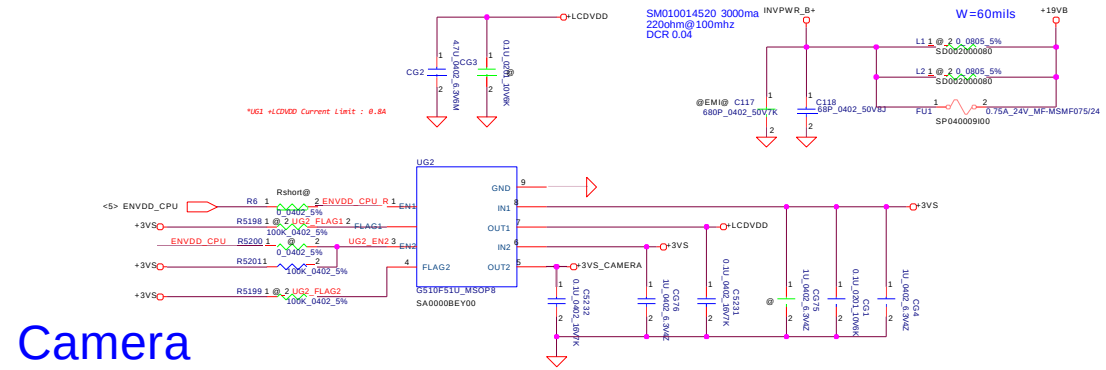
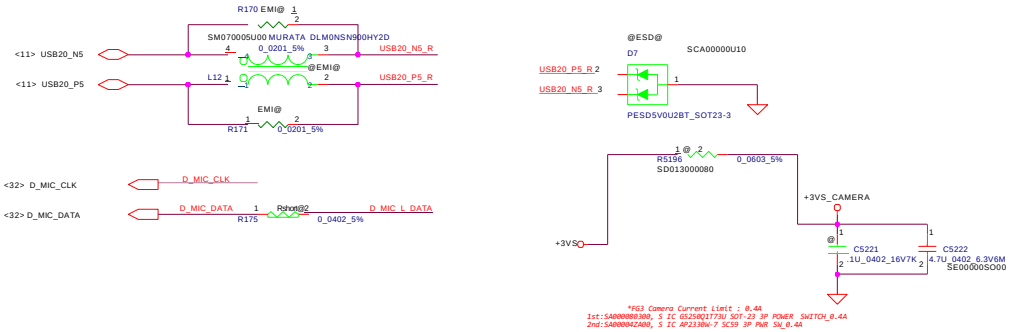
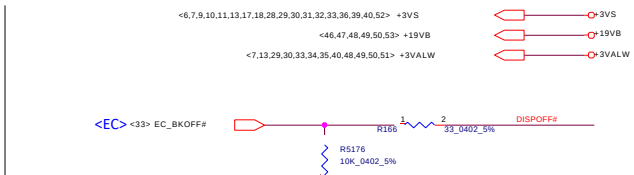
Issued Date	2017/04/10	Deciphered Date 2019/12/15	Title: P19-DDRIV_CHB: DIMM0
			Size: Document Number: LA-G07BP(KBL-U_UMA_6L) Rev: v0.3
			Date: Friday, January 05, 2018 Sheet 18 of 59

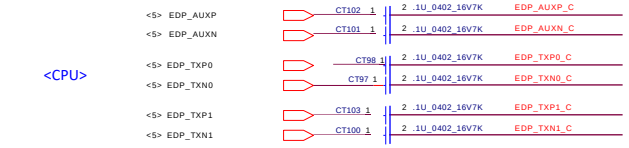
eDP Power

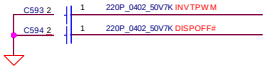


Camera

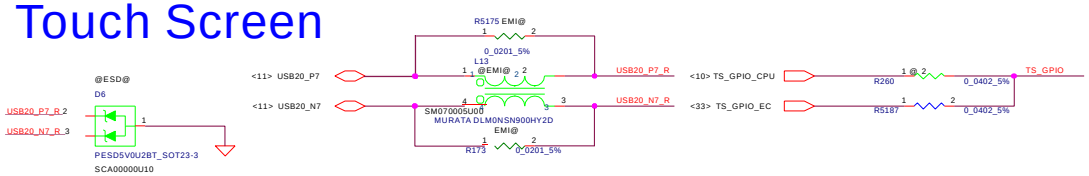




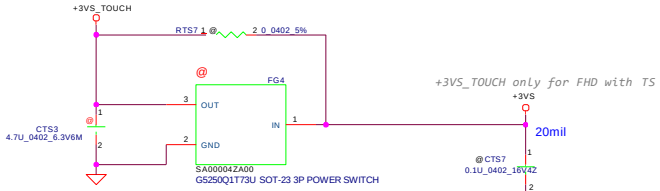


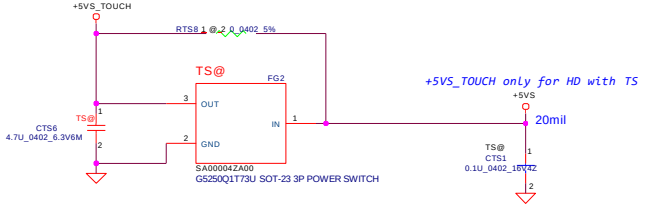


Touch Screen

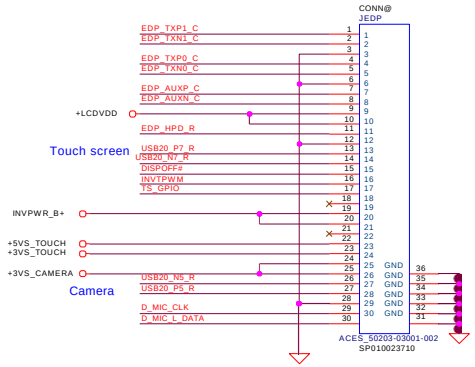


Touch Screen Power Selection:





eDP



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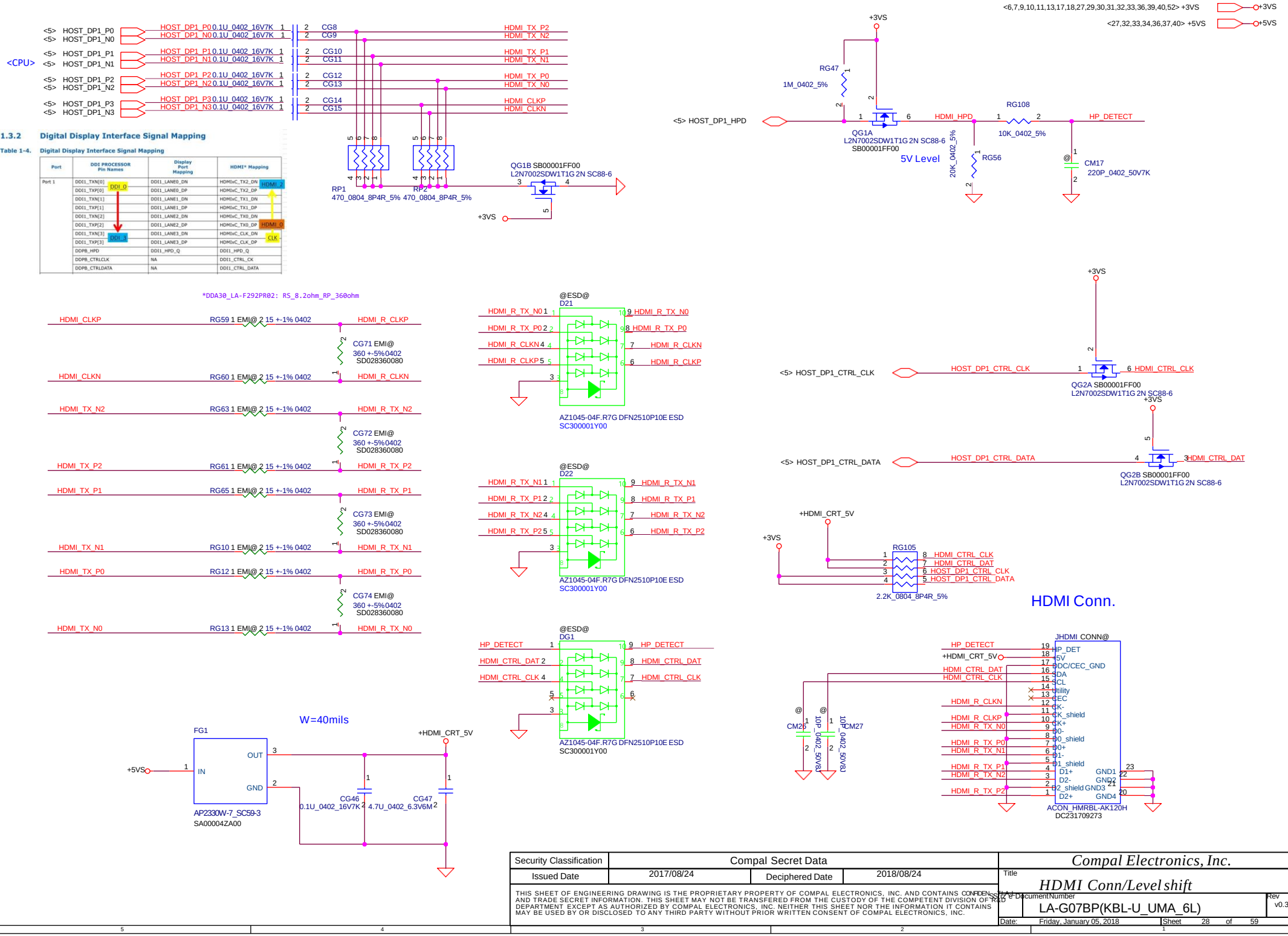
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: eDP CONN/Camera/TS

Size: D | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 27 of 59



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Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: HDMI Conn/Level shift

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Date: Friday, January 05, 2018 | Sheet 28 of 59

+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

CL8, CL23 closeLL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin22.
CL11, CL27 close UL1 Pin30.

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32

CL10& CL16 close to UL1: Pin 23

(SA000084T00) RTL8111HSH-CG Giga

powe rail need tocheck

powe rail need tocheck

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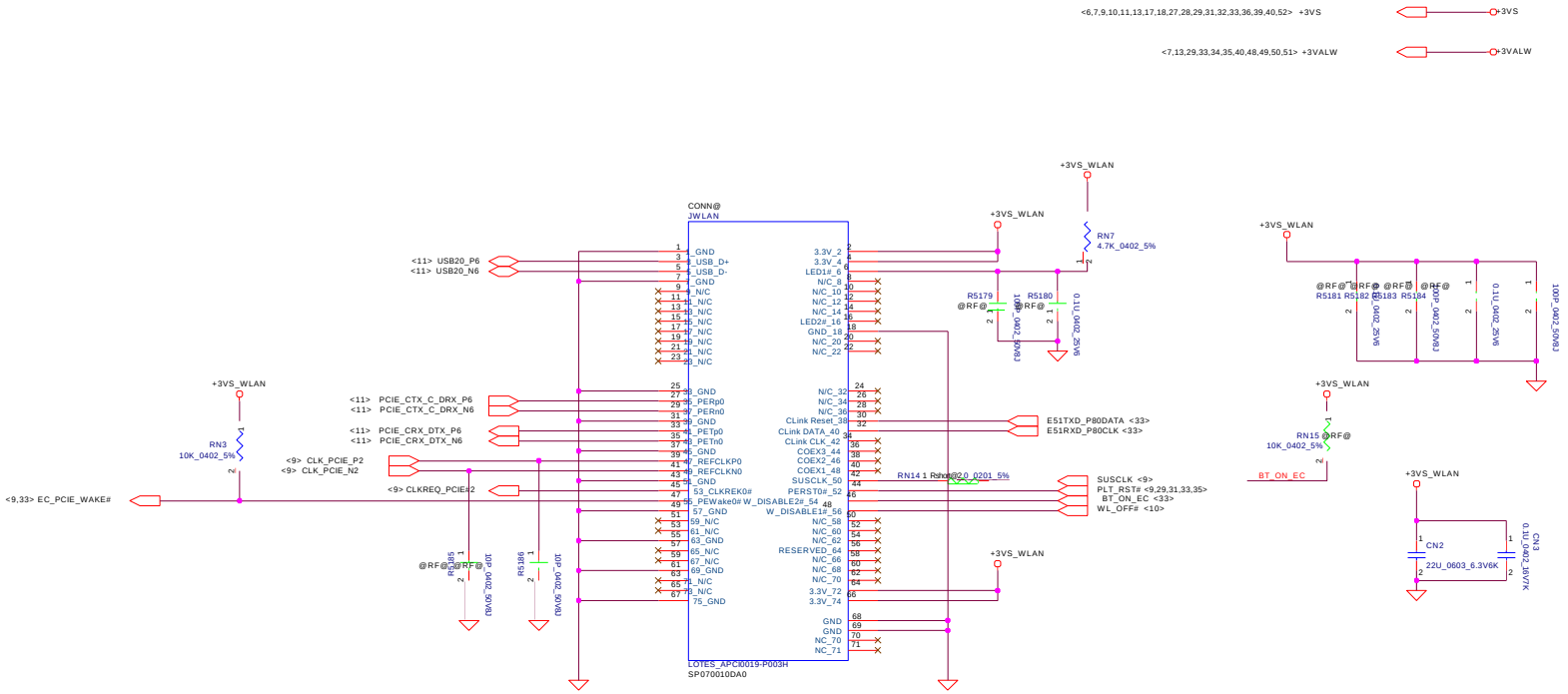
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: LAN 8111

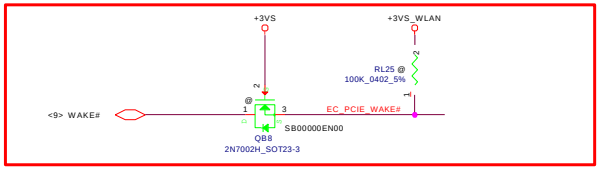
Size: C | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

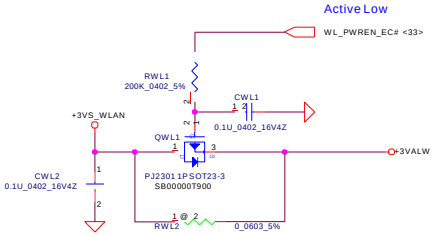
Date: Friday, January 05, 2018 | Sheet 29 of 59



NGFF and WLAN

Unpop QB8 and RL25 for not support OBFF





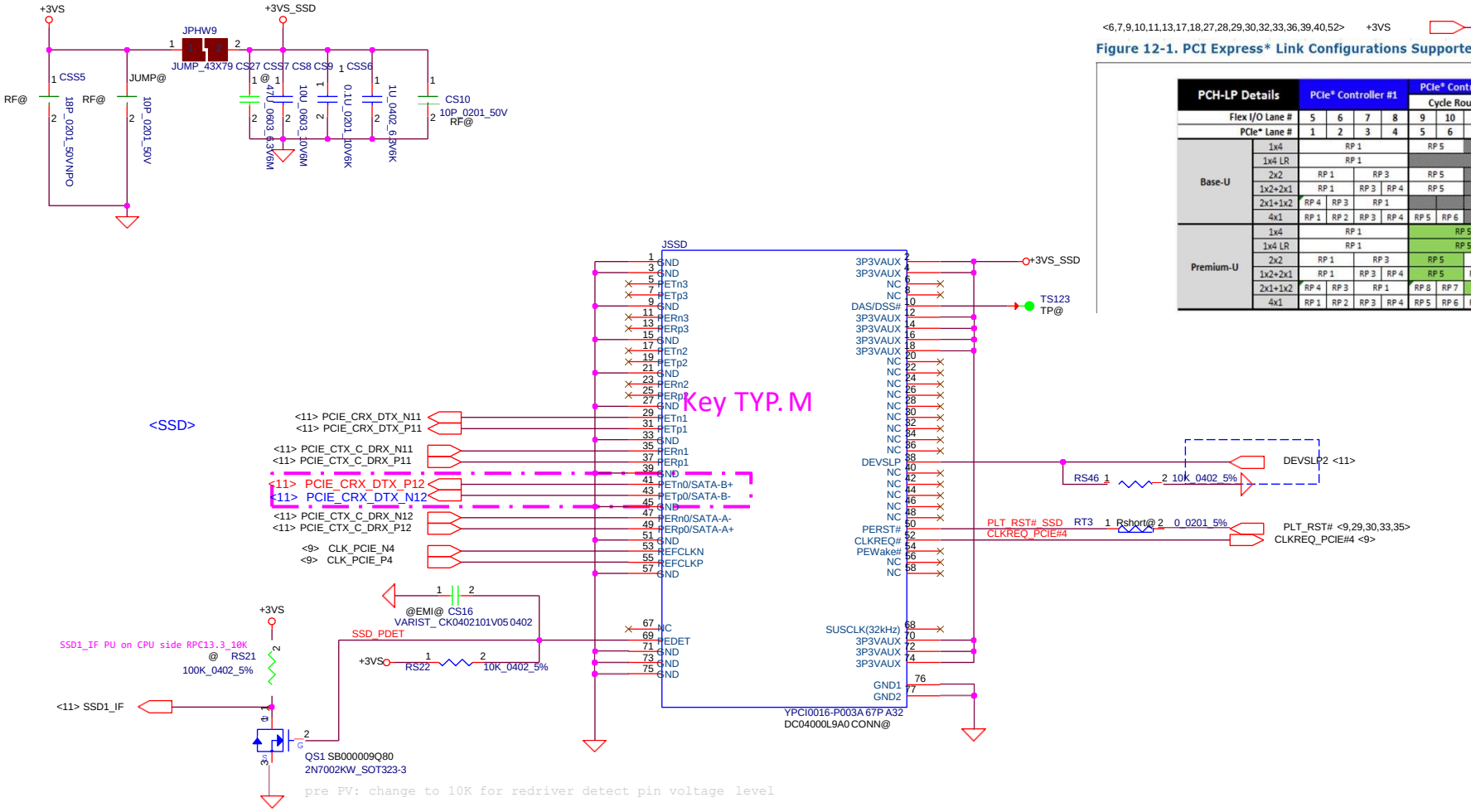
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: WLAN-BT

Size: C | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 30 of 59



<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52> +3VS +3VS

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2 Cycle Router #2				PCIe* Controller #3 Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1						RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH	
41	PETn0	PCIe TX	42 N/C
43	PETp0	PCIe TX	44 N/C
45	GND	Return current path	46 N/C
47	PERn0	PCIe Rx	48 N/C
49	PERp0	PCIe Rx	50 PERST#
51	GND	Return current path	52 CLKREQ#

39	GND	Return Current Path	40
41	TXP	Transmitter Differential Signal Pair	42
43	TXN	Transmitter Differential Signal Pair	44
45	GND	Return Current Path	46
47	RXN	Receiver Differential Signal Pair	48
49	RXP	Receiver Differential Signal Pair	50
51	GND	Return Current Path	52

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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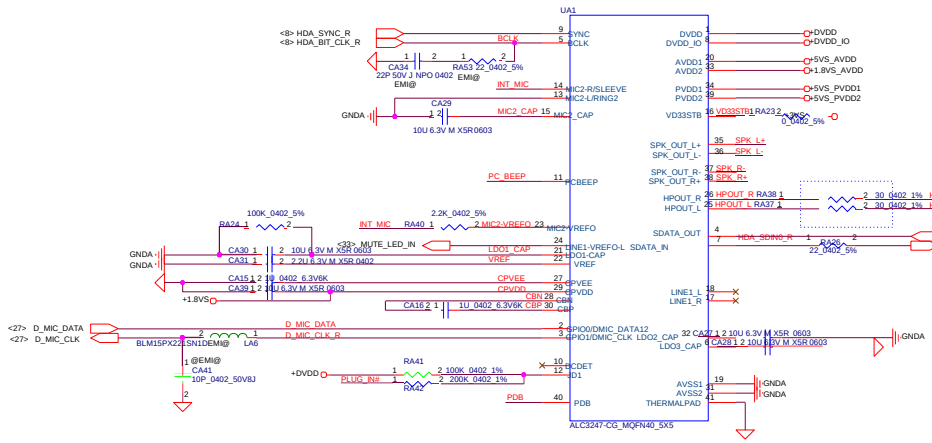
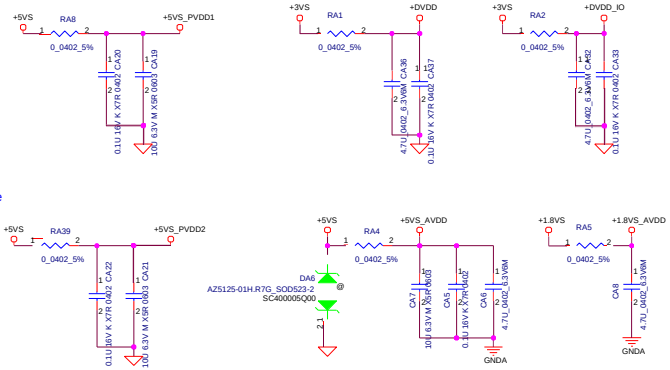
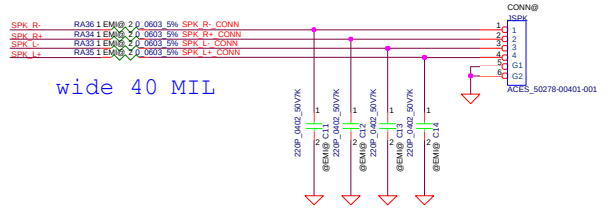
Issued Date	2017/08/24 Deciphered Date 2018/08/24	Title: *M.2 SSD*
		Size: A4 Document Number: LA-G07BP(KBL-U_UMA_6L) Rev: v0.3
		Date: Friday, January 05, 2018 Sheet 31 of 59

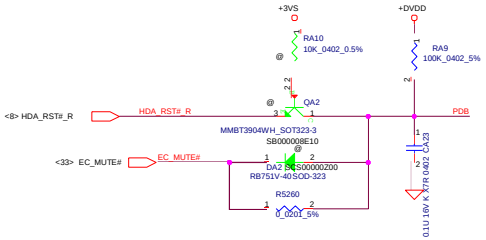




Internal SPK



wide 40 MIL

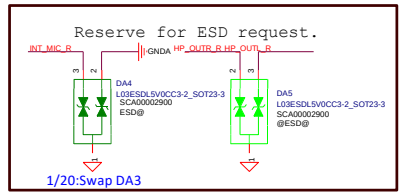


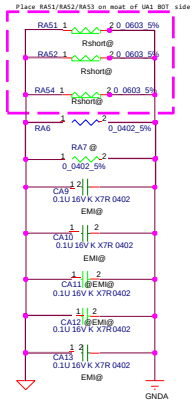
PC Beep

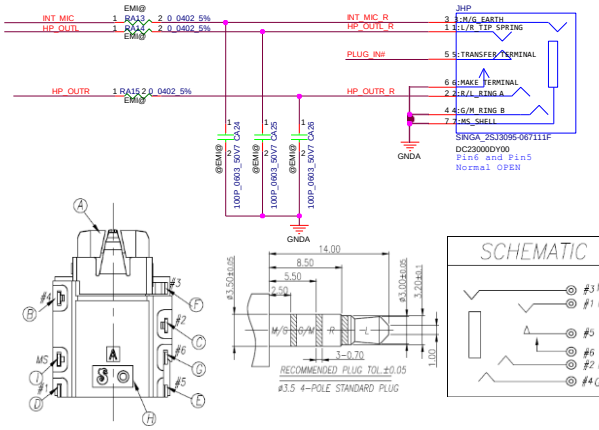
EC Beep <33> EC_BEEP#

SB Beep <8,10> HDA_SPKR

Close to Codec pin34







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Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.	
Title	AUDIO ALC3258-CG
Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L) Rev: V3.0
Date: Friday, January 05, 2018	Sheet 32 of 59

EC Board ID (UMA, DIS, phase) control table

RK4	KBL-U				KBL-R			
	DB	SI	PV	MV	DB	SI	PV	MV
UMA	15K	27K	43K	75K	130K	200K	270K	430K
DIS	20K	33K	56K	100K	160K	240K	330K	560K

Reserve EC_CLR_CMOS for clear CMOS

U_DB_UMA_15kohm:SD034150280,5 RES 1/16W 15K+-1% 0402
U_DB_ DIS_20kohm:SD034200280,5 RES 1/16W 20K +-1% 0402 (2016-03-04 :Confirm intel platform not support EC Clear CMOS function)
U_SI_UMA_27kohm:SD034270280,5 RES 1/16W 27K +-1% 0402 (2017-10-05 : 2018OPP Add EC Clear CMOS function)
U_SI_ DIS_33kohm:SD034330280,5 RES 1/16W 33K +-1% 0402
U_PV_UMA_43kohm:SD034430280, 5 RES 1/16W 43K +-1% 0402
U_PV_ DIS_56kohm:SD034560280, 5 RES 1/16W 56K +-1% 0402
U_MV_UMA_75kohm:SD034750280,5 RES 1/16W 75K +-1% 0402
U_MV_ DIS_100kohm:SD034100380,5 RES 1/16W 100K+-1% 0402
R_DB_UMA_130kohm:SD034130380,5 RES 1/16W 130K+-1% 0402
R_DB_ DIS_160kohm:SD034160380,5 RES 1/16W 160K +-1% 0402
R_SI_UMA_200kohm:SD034200380, 5 RES 1/16W 200K +-1% 0402
R_SI_ DIS_240kohm:SD000001880,5 RES 1/16W 240K +-1% 0402
R_PV_UMA_270kohm:SD000000G280, 5 RES 1/16W 270K +-1% 0402
R_PV_ DIS_330kohm:SD034330380, 5 RES 1/16W 330K +-1% 0402

RK106 2 0 0402 5% CLR_CMOS# <9>
EC_CLR_CMOS — Q51 2N7002K_SOT23-3 SB00000EN00
R483 10K_0402_5%

PC & MISC

T2403 TP@ TOUCH_ON
EC_KBRST# <7>
SERIRQ <7,35>
LPC_FRAME# <7>
LPC_AD3 <7>
LPC_AD2 <7>
LPC_AD1 <7>
LPC_AD0 <7>
CLK_PCI_LPC <7>
PLT_RST# <9,19,29,30,31,35>
EC_RST#
EC_SCI# <5>
PM_CLKRUN# <7>
EC_PCIE_WAKE# <9,30>
PM_CLKRUN# R RK10 0 0402 5%
RK6 0 0402 5%

PWM Output

EC_VCCST_PG/GPIO0F — EC_VCCST_PG_R — EC_VCCST_PG_R <9,40>
BEEP#/GPIO10 — EC_BEEP# <32>
FAN_PWM1 — EC_FAN_PWM1 <36>
CLR_CMOS
AC_OFF/GPIO13

AD Input

VCIN1_BATT_TEMP/AD0/GPIO38 — B/I# — B/I# <46>
VCIN1_BATT_DROP/AD1/GPIO39 — ADP_I — ADP_I <45,47>
ADP_I/AD2/GPIO3A
AD_BID/AD3/GPIO3B — BOARD_ID
AD4/GPIO42 — ADP_ID — ADP_ID <45>
AD5/GPIO43 — EC_PME# — EC_PME <29>
R5178 1 2 0 0201 5%

DA Output

DA0/GPIO3C — KBL_ON# <34>
EN_DFAN1/DA1/GPIO3D — NMI_DBG# — VR_PWRGD — VR_PWRGD <52>
DA2/GPIO3E — EC_MUTE# — EC_MUTE# <32>
DA3/GPIO3F

PS2 Interface

EC_MUTE#/PSCLK1/GPIO4A — VR_ON — VR_ON <40,52>
USB_EN#/PSDAT1/GPIO4B — LAN_PWR_EN <29>
PSCLK2/GPIO4C — TP_CLK — TP_CLK <34>
PSDAT2/GPIO4D — TP_DATA — TP_DATA <34>
TP_CLK/GPIO4E
TP_DATA/GPIO4F

Int. K/B Matrix

<34> KSI[0..7]
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
<34> KSO[0..17]
KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16 KSO17

SPI Device Interface

ENBKL/GPXIOA00 — ENBKL — ENBKL <5>
WOL_EN/GPXIOA01 — ME_FLASH_EN — WL_PWREN_EC# <30>
ME_EN/GPXIOA02 — VCIN0_PH — ME_FLASH_EN <8>
VCIN0_PH1/GPXIOD00 — VCIN0_PH <45>

SPI Flash ROM

MISO/GPIO5B — EC_SPI_SO <7>
MOSI/GPIO5C — EC_SPI_SI <7>
SPICLK/GPIO58 — EC_SPI_CLK
SPICS#/GPIO5A — EC_SPI_CS0# <7>

GPIO

EC_CIR_RX/AD6/GPIO40 — TS_GPIO_EC <27>
SYS_PWROK/AD7/GPIO41 — SYS_PWROK — SYS_PWROK <9>
GPIO50 — EC_S0IX_EN — EC_S0IX_EN <12>
BATT_CHG_LED#/GPIO52 — BAT_CHG_LED — BAT_CHG_LED <45>
CAPS_LED#/GPIO53 — CAP_LOCK# — CAP_LOCK# <34>
PWR_LED#/GPIO54 — PWR_LED# — PWR_LED# <39>
BATT_LOW_LED#/GPIO55 — SYSON — ACIN <9>
SYSON/GPIO56 — BT_ON_EC — SYSON <12,40,49>
VR_ON/GPIO57 — PCH_DPWROK — BT_ON_EC <30>
DPWROK_EC/GPIO59 — PCH_DPWROK <9>

SM Bus

EC_SMB_CK1/GPIO44 <46,47>
EC_SMB_DA1/GPIO45 <46,47>
EC_SMB_CK2/GPIO46 <7,10,22>
EC_SMB_DA2/GPIO47 <7,10,22>
RK15 1 2 0 0402 5% EC_SMB_CK2_R
RK16 1 2 0 0402 5% EC_SMB_DA2_R

GPIO GPO

PM_SLP_S3#/GPIO04 <9,12,40>
PM_SLP_S5# <9>
SUSACK# <9>
PM_SLP_SUS# <9>
PCH_SUSWARN# <9>
GPIO07
GPIO08
GPIO0A
GPIO0B
GPIO0C
AC_PRESENT/GPIO0D
PWM2/GPIO11
FAN_SPEED1/GPIO14
FANFB1/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
PCH_PWROK/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A

EC_RSMRST#/GPXIOA03 — PCH_RSMRST# — PCH_RSMRST# <9>
GPXIOA04 — USB_ON# — USB_ON# <38,39>
VCIN1_ADP_PROCHOT/GPXIOA05 — VCIN1_PH — VCIN1_PH <45>
VCOUT1_PROCHOT#/GPXIOA06 — H_PROCHOT#_EC
VCOUT0_MAIN_PWR_ON/GPXIOA07 — MAINPWON — MAINPWON <48>
BKOFF#/GPXIOA08 — EC_BKOFF# — EC_BKOFF# <27>
GPXIOA09 — RK25 1 2 0 0402 5% — DGPU_PWR_EN <10,24>
PCH_PWR_EN/GPXIOA10 — PCH_PWR_EN — PCH_PWR_EN <40,51>
PWR_VCCST_PG/GPXIOA11 — +1.0VS_PG — +1.0VS_PG <50>

GPI

VCIN1_AC_IN/GPXIOD01 — VCIN1_AC_IN_R — EC_ON — EC_ON <39,48>
ALW_PWR_EN EC_ON/GPXIOD02 — ON/OFF# — ON/OFF# <39>
ON/OFF#/GPXIOD03 — LID_SW# — LID_SW# <39>
LID_SW#/GPXIOD04 — SUSP# — SUSP# <12,40,49>
SUSP#/GPXIOD05 — VCIN1_AC_IN
GPXIOD06
PECI/GPXIOD07 — EC_PECI RK17 1 2 43 0402 1% — H_PECI <5>
V18R/VCC_IO2 — +V18R — +3VALW_EC
CK8 4.7U_0402_6.3V6M

<32> MUTE_LED_IN — MUTE_LED_IN
<36> FAN_SPEED1 — FAN_SPEED1
VCIN1_ACOK_R
<30> E51TXD_P80DATA — E51TXD_P80DATA
<30> E51RXD_P80CLK — E51RXD_P80CLK
<9> PCH_PWROK — PCH_PWROK
<45> AC_LED# — AC_LED#
<34> MUTE_LED_OUT
<9> PBTN_OUT# — PBTN_OUT#
<9,12,40,49> PM_SLP_S4# — PM_SLP_S4#

KB9022QD_LQFP128_14X14
SA000075S30

Power Rails

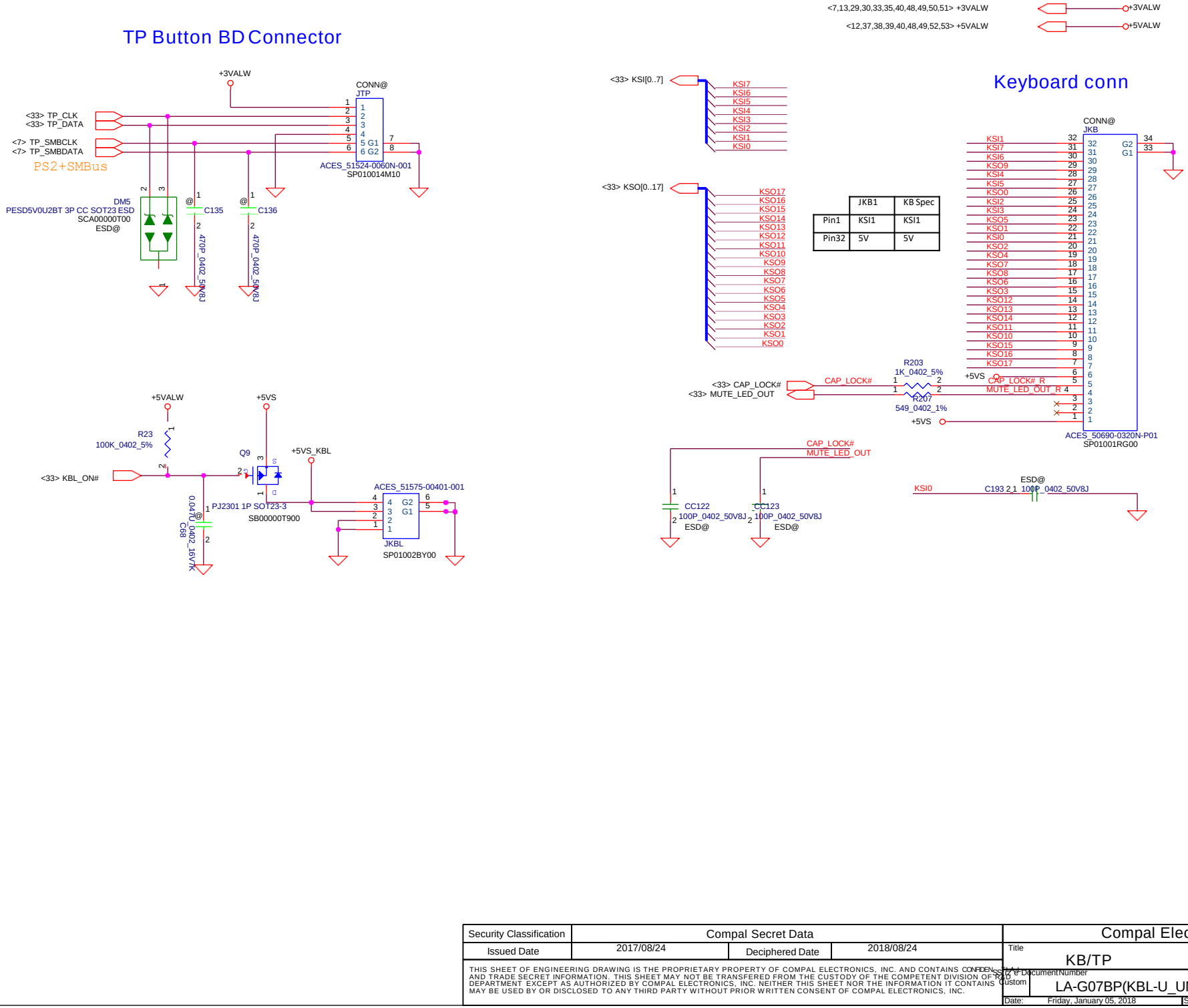
+3VL — RK1 0_0603_5% — CK1 0.1U_0201_10V6K — CK2 0.1U_0201_10V6K
+3VALW_EC — +3VALW_EC
LK1 SM01000Q500 S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402 — +EC_VCCA
CK3 0.1U_0201_10V6K — ECAGND
+3V_EC_VDD — 1 RK3 2 0_0402_5%
+3V_LID
RK2 100K_0402_1% — BOARD_ID
U_PX@ RK4 56K +-1% 0402 SD034560280
U_UMA@ RK4 43K +-1% 0402 SD034430280
R_PX@ RK4 330K +-1% 0402 SD034330380
R_UMA@ RK4 270K +-1% 0402 SD00000G280
ESD@ CK4 0.1U_0402_25V6 — PLT_RST#
+3VALW_EC @ RK7 2 1 330K_0402_5% — EC_RST# — @ CK5 1 2 0.1U_0402_16V7K
CLK_PCI_LPC — CK9 22P 50V J NPO 0402 EMI@ — RK109 22_0402_5% EMI@
EC_SCI# — 1 @ 2 PM_CLKRUN# R RK10 0 0402 5% — RK6 0 0402 5%
<47> VCIN1_ACOK — 1 @ 2 VCIN1_ACOK_R R4958 0_0402_5%
1 2 VCIN1_AC_IN_R R5094 0_0402_5%
VCIN1_AC_IN 1 @ 2 VCIN1_AC_IN_R R4960 0_0402_5%
For Solve tPCH04(Min 9ms) Sequence Timing
+5VS — RK28 2 1 MUTE_LED_OUT 100K_0402_5%
RK26 2 1 E51TXD_P80DATA 100K_0402_5%
RK20 1 @ 2 PCH_PWROK 100K_0402_5%
RK108 1 2 MUTE_LED_IN 10K_0402_5%
+3VALW_EC — RK21 10K_0402_5% — NMI_DBG# — DK2 SCS00000Z00 RB751V-40 SOD-323 — NMI_DBG#_CPU <5,10>
20mil
LK2 SM01000Q500 TAI-TECH HCB1005KF-221T15 0402 — ECAGND — ECAGND <45>

Power Rails

<52> VR_HOT# — VR_HOT# RK8 1 2 0 0402 5% — PROCHOT# <5>
H_PROCHOT#_EC 2 — @QK1 2N7002_SOT23-3 SB00000EN00
RK91 2 0 0402 5%
TP_CLK RK12 1 2 4.7K_0402_5% — +3VALW
TP_DATA RK13 1 2 4.7K_0402_5%
+3VL — RP12 8 7 6 5 1 2 3 4 — PLT_RST# EC_ON PCH_PWR_EN — 100K_0804_8P4R_5%
PBTN_OUT# R295 1 @ 2 1K_0402_5%
EC_CLR_CMOS 1 @ 2 RK107 10K_0402_5%
+3VALW_EC — LID_SW# RK18 2 @ 1 47K_0402_5%
+3V_SMBUS — +3VS — RP11 8 7 6 5 1 2 3 4 — EC_SMB_CK1 EC_SMB_DA1 EC_SMB_CK2 EC_SMB_DA2 — 2.2K_0804_8P4R_5%
EC_SCI# RK14 2 1 10K_0402_5%
SYSON RK23 1 @ 2 100K_0402_5%
SUSP# RK27 1 2 100K_0402_5%
EC_SPI_CLK RC369 1 EMI@ 2 HOST_SPI_0_CLK_R 15_0402_5% — HOST_SPI_0_CLK_R <7,35>
CC128 RC369 place near ECSide
CC144 22P 50V J NPO 0402 @EMI@
EMI request

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.
Title: EC ENE-KB9022
Size: Custom
Document Number: LA-G07BP(KBL-U_UMA_6L)
Rev: v0.3
Date: Tuesday, January 09, 2018
Sheet 33 of 59



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: KB/TP

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

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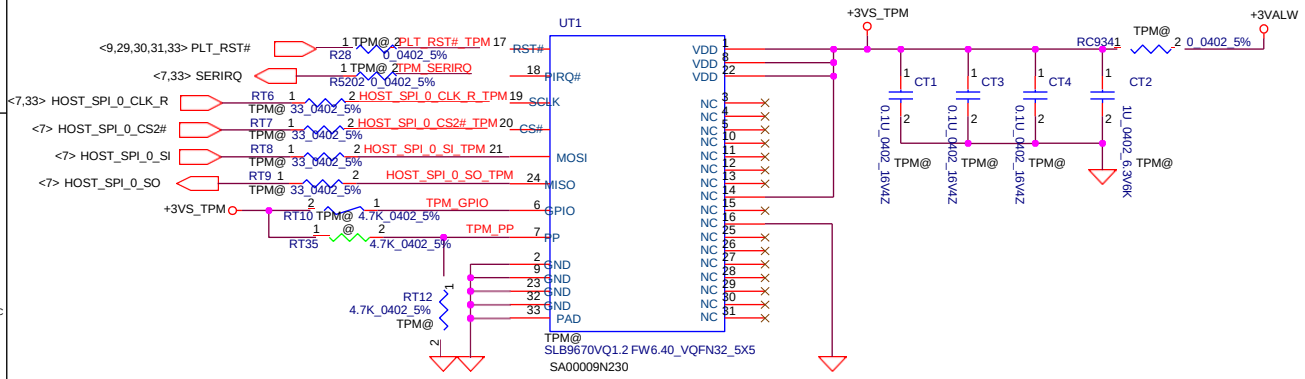
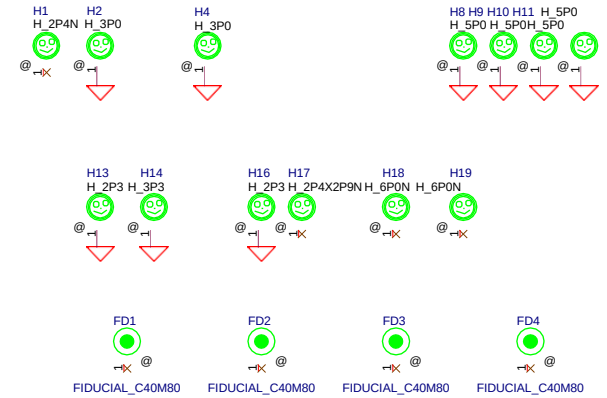
+3VALW +3VALW <7,13,29,30,33,34,40,48,49,50,51>

TPM2.0



Screw Hole

CPU



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: TPM/Screw

Size: A3 | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

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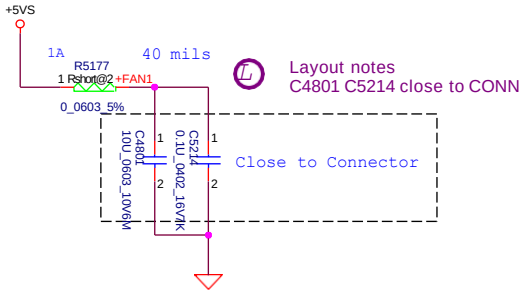

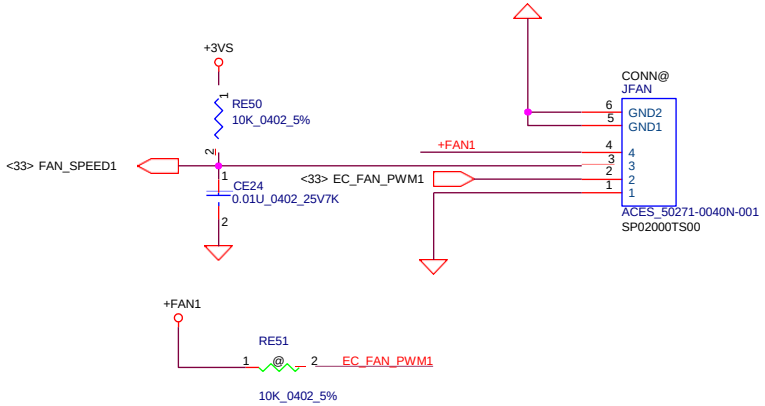

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date	2018/08/24
Title	FAN		
Size	Document Number		Rev
Custom	LA-G07BP(KBL-U_UMA_6L)		v0.3
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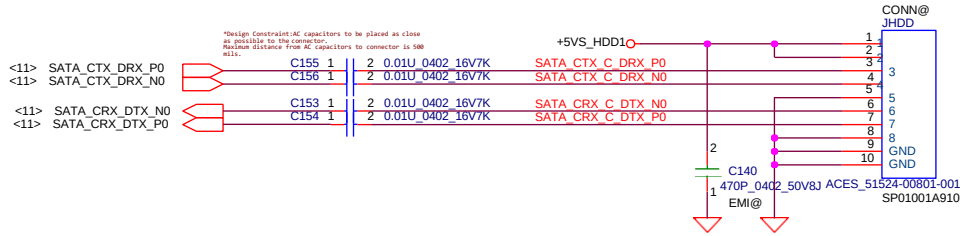
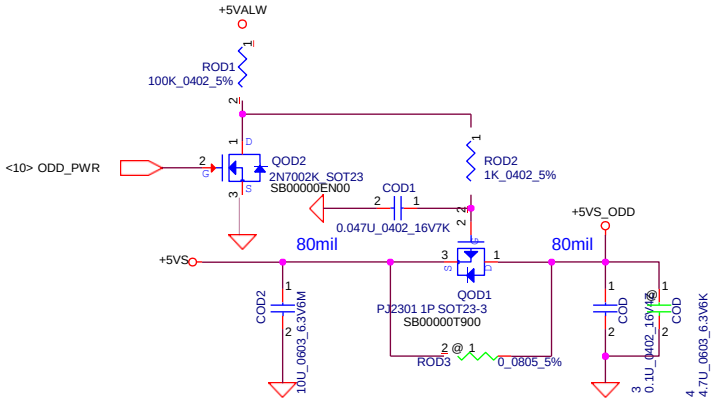
2.5" SATA HDD

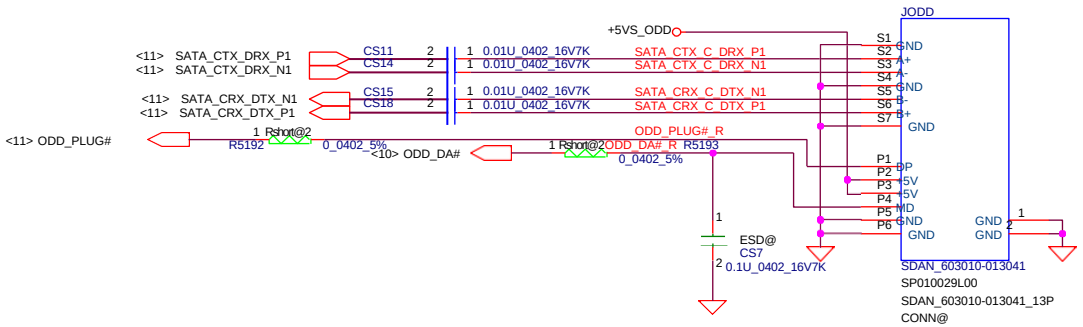
<27,28,32,33,34,36,40> +5VS
<12,34,38,39,40,48,49,52,53> +5VALW
<7,13,29,30,33,34,35,40,48,49,50,51> +3VALW

<PV> change short pad



SATA ODD





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date	2018/08/24
Title	HDD/ODD Conn		
Size	Document Number		Rev
Custom	LA-G07BP(KBL-U_UMA_6L)		v0.3
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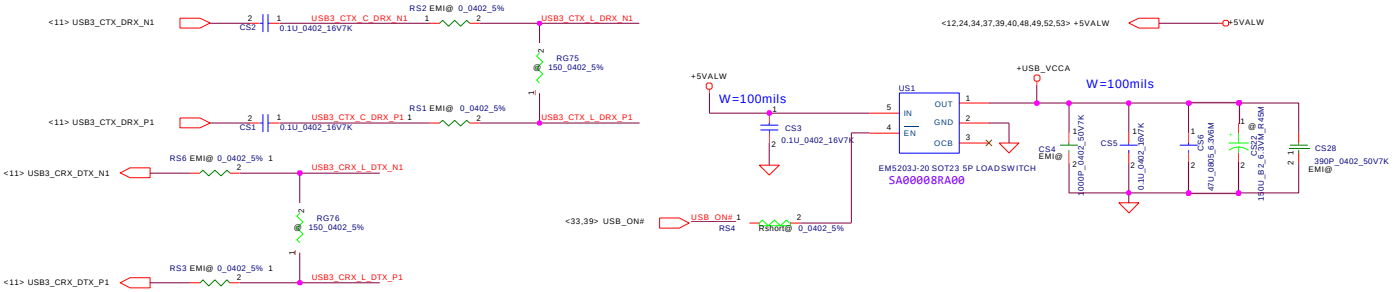
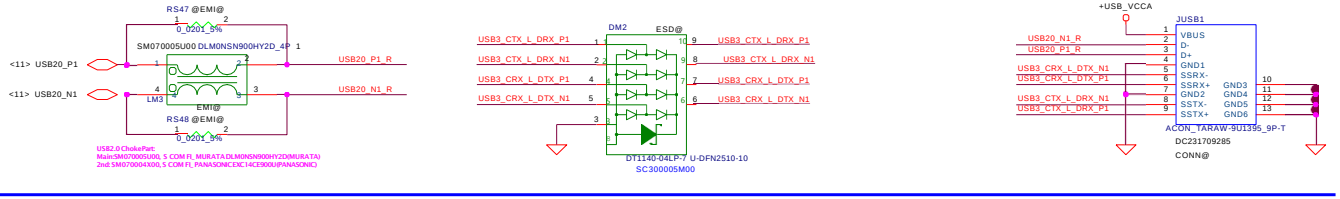
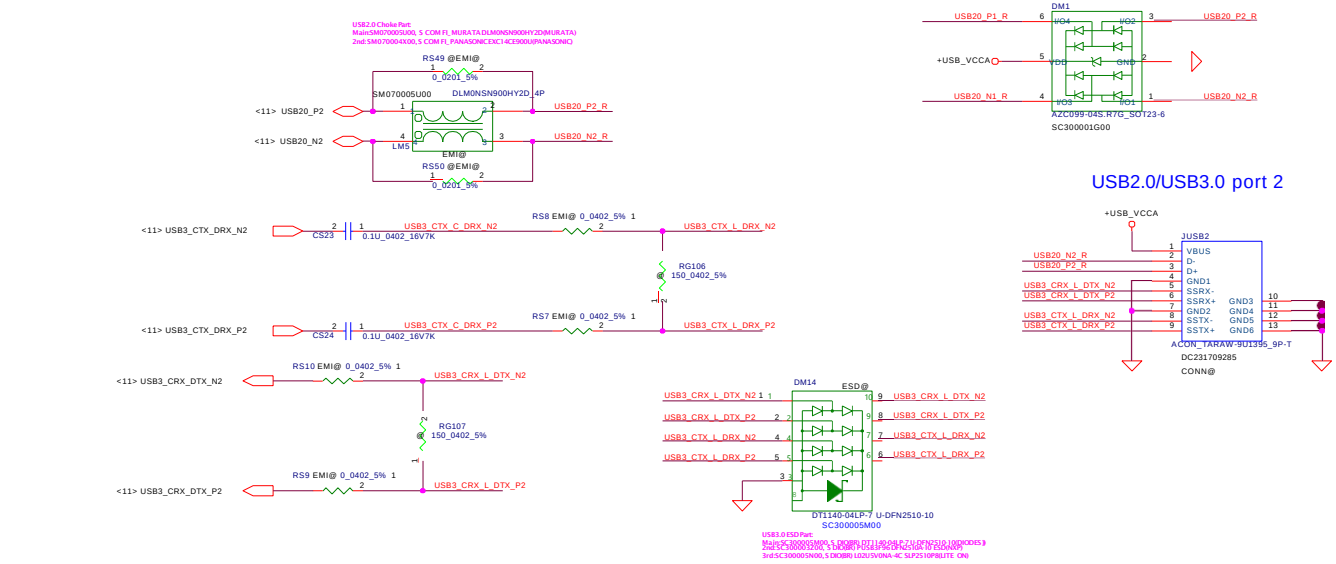


USB2.0/USB3.0 port 1





USB2.0/USB3.0 port 2

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.	
Title	USB 3.0/2.0 conn
Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L)
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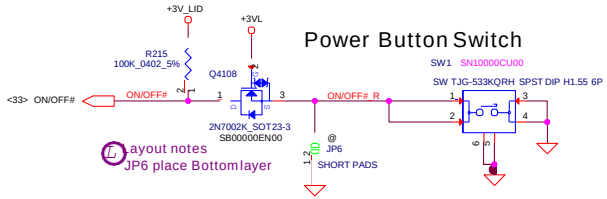
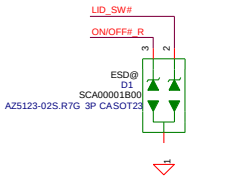
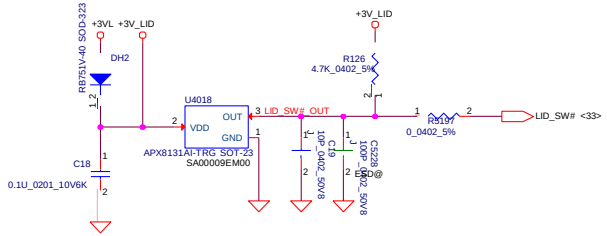
Power Button Switch

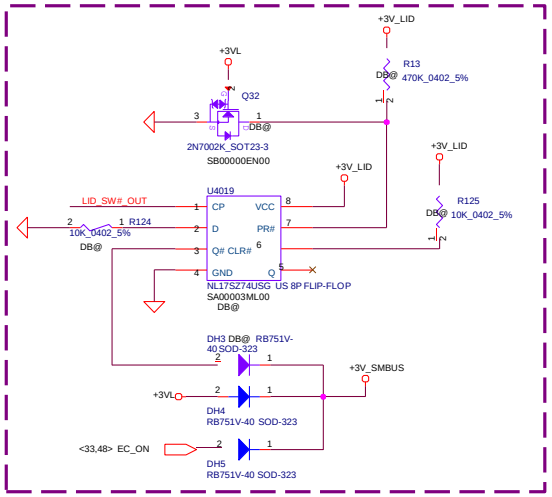


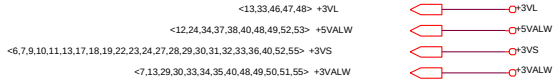
ESD Diode



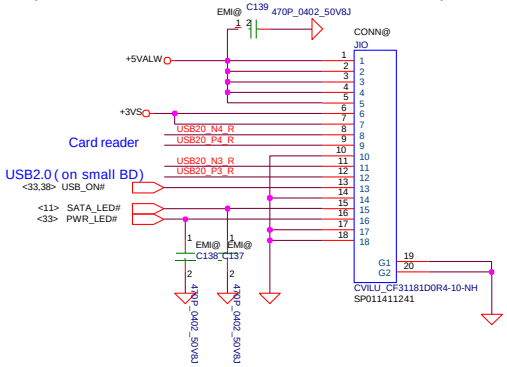
Lid Switch (Hall Effect Sensor)

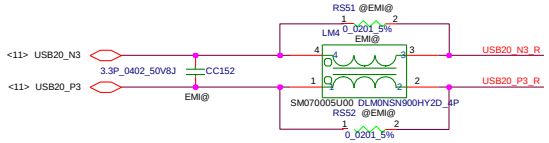


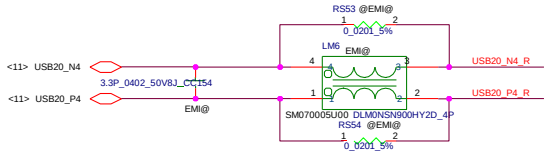




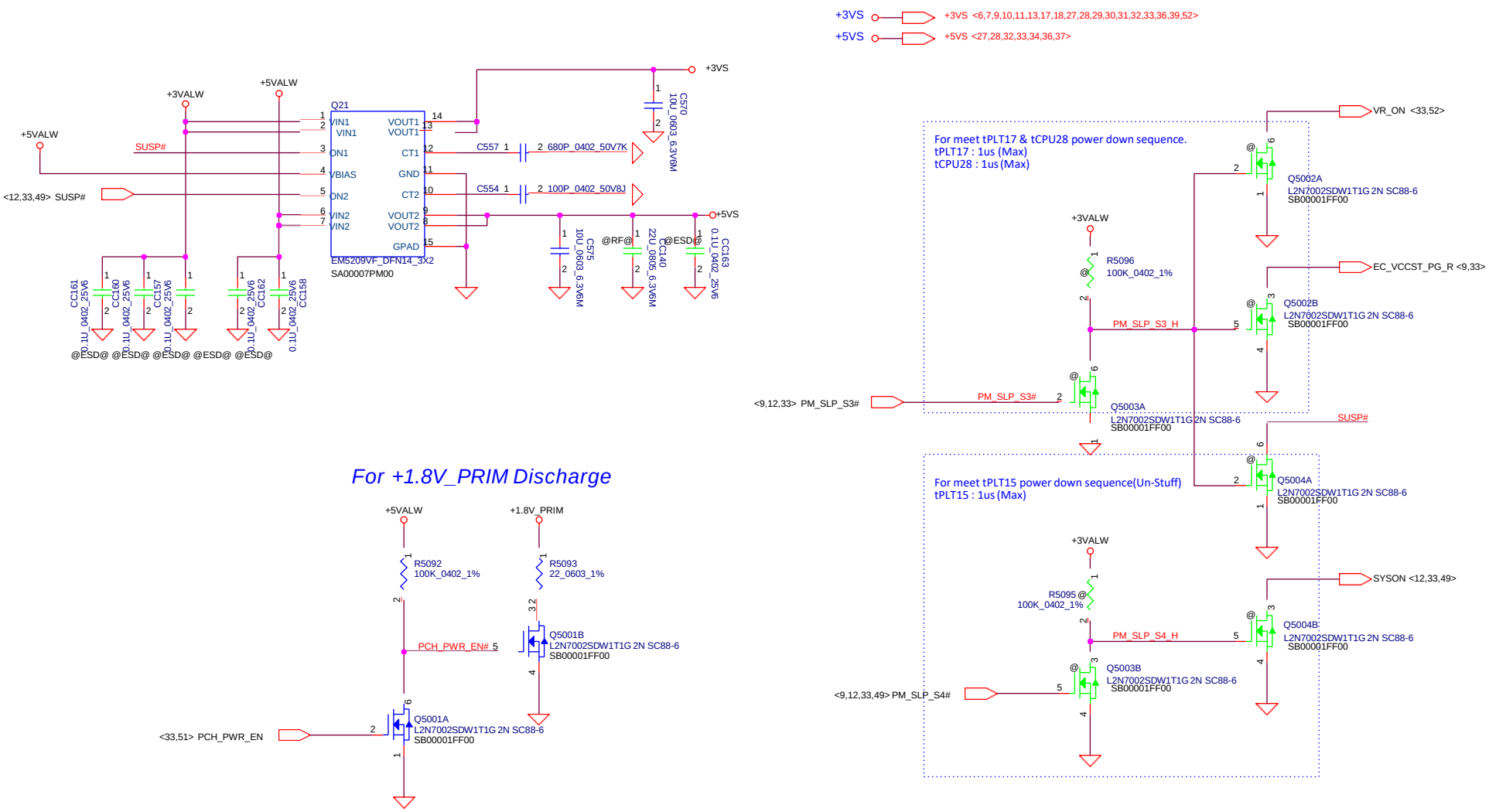
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date	2018/08/24
Title	IO CON		
Size: Custom	Document Number: LA-G07BP(KBL-U_UMA_6L)		Rev: v0.3
Date: Tuesday, January 09, 2018	Sheet 39 of 59		



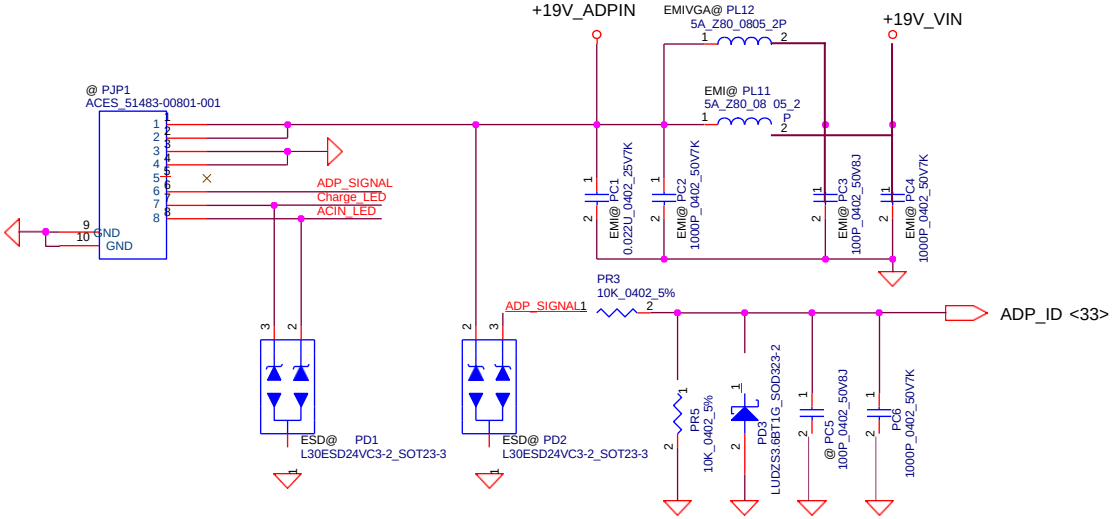
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

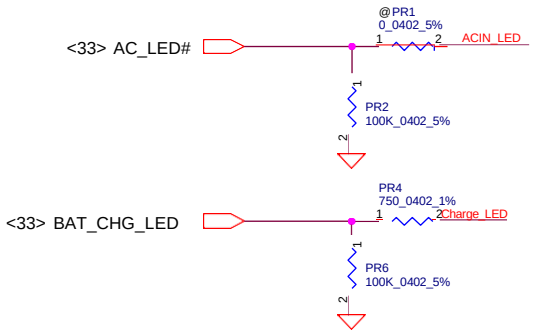
Compal Electronics, Inc.

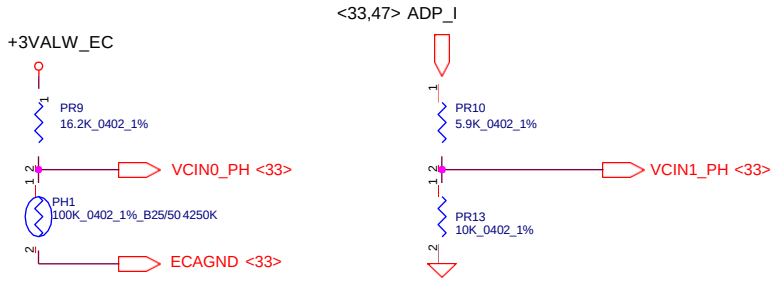
Title: DC Interface

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

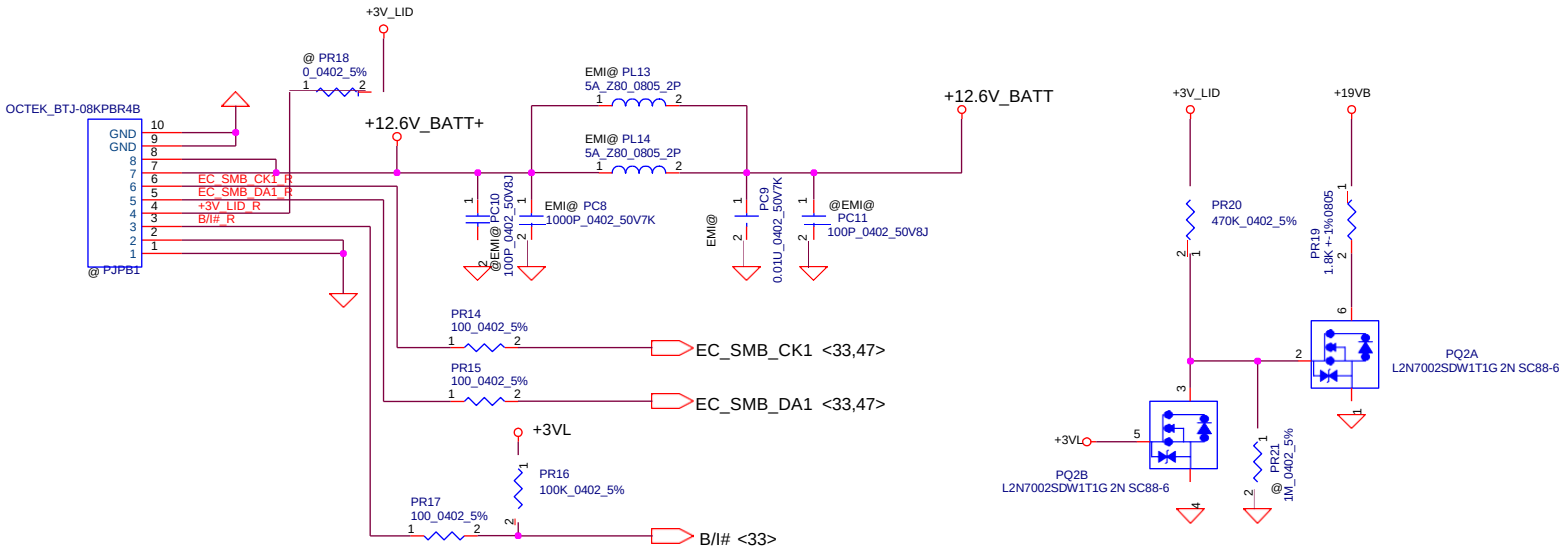
Date: Friday, January 05, 2018 | Sheet 40 of 59





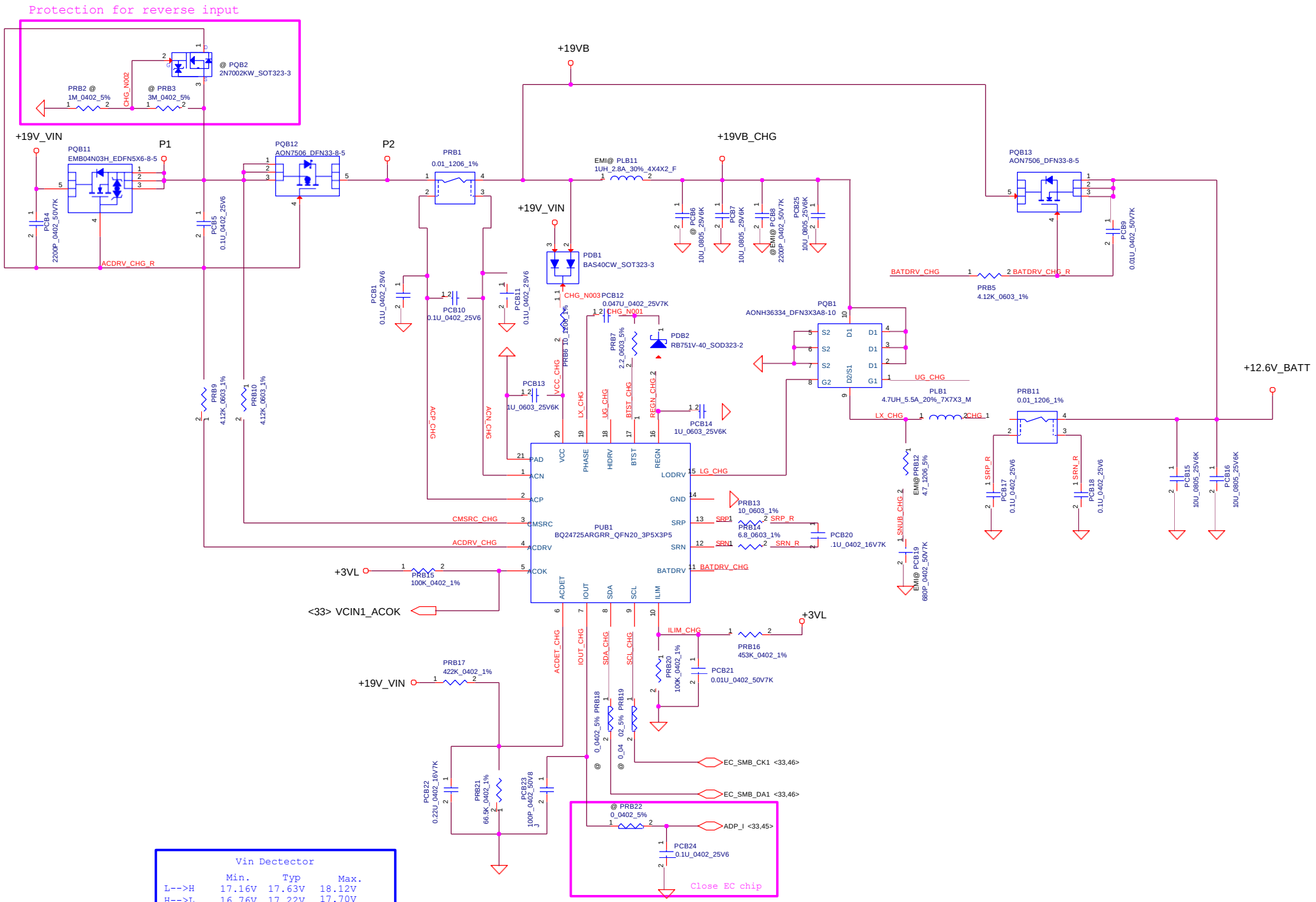


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	DC Conn		
Size	Document Number		Rev
	LA-G07BP(KBL-U_UMA_6L)		v0.3
Date:	Friday, January 05, 2018	Sheet 45	of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	*BATT Conn*		
Size	Document Number		Rev
	LA-G07BP(KBL-U_UMA_6L)		v0.3
Date:	Friday, January 05, 2018	Sheet	46 of 59



Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.02
= 2.291 A

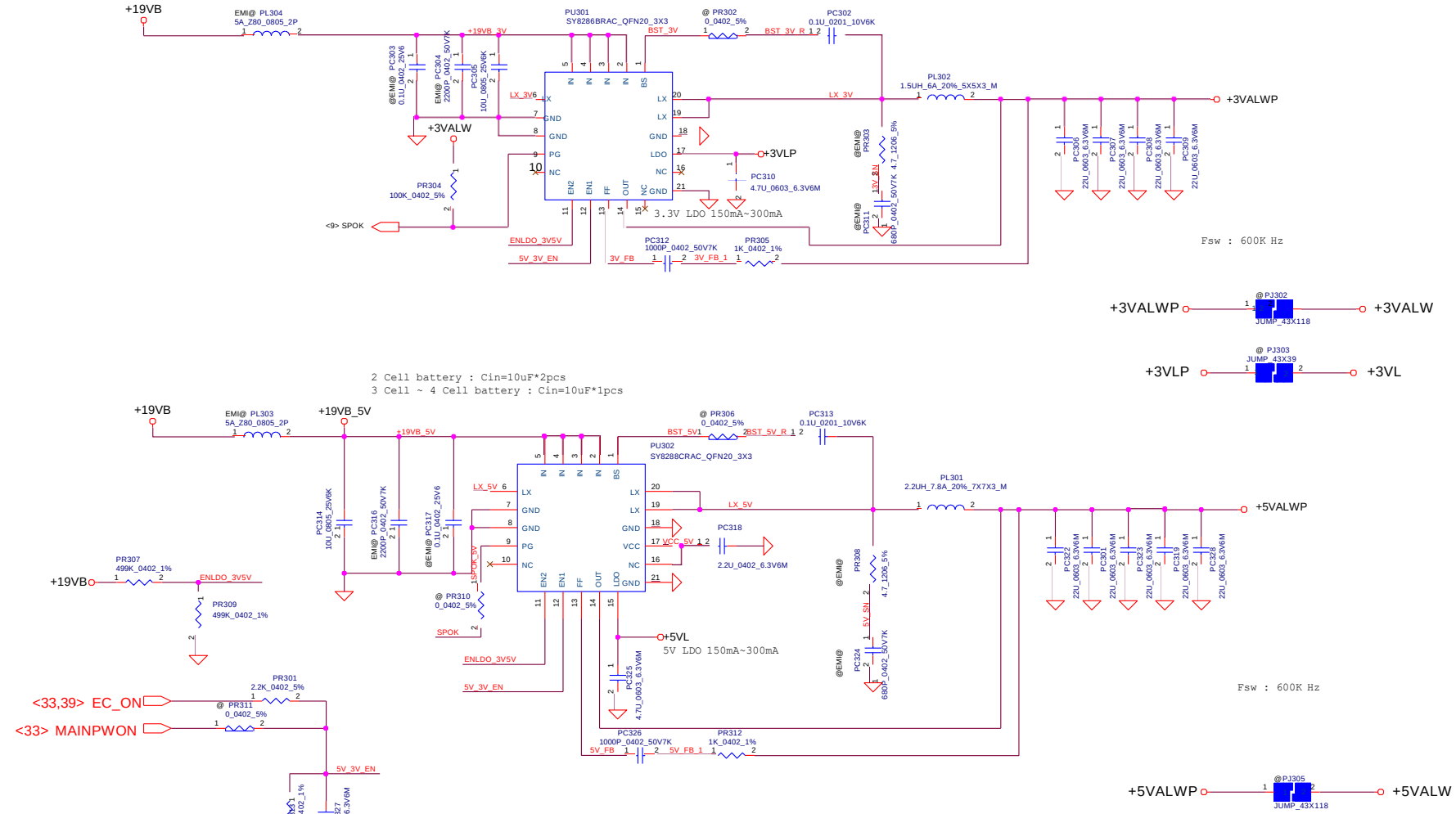
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: CHARGER

Size: C | Document Number | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 47 of 59



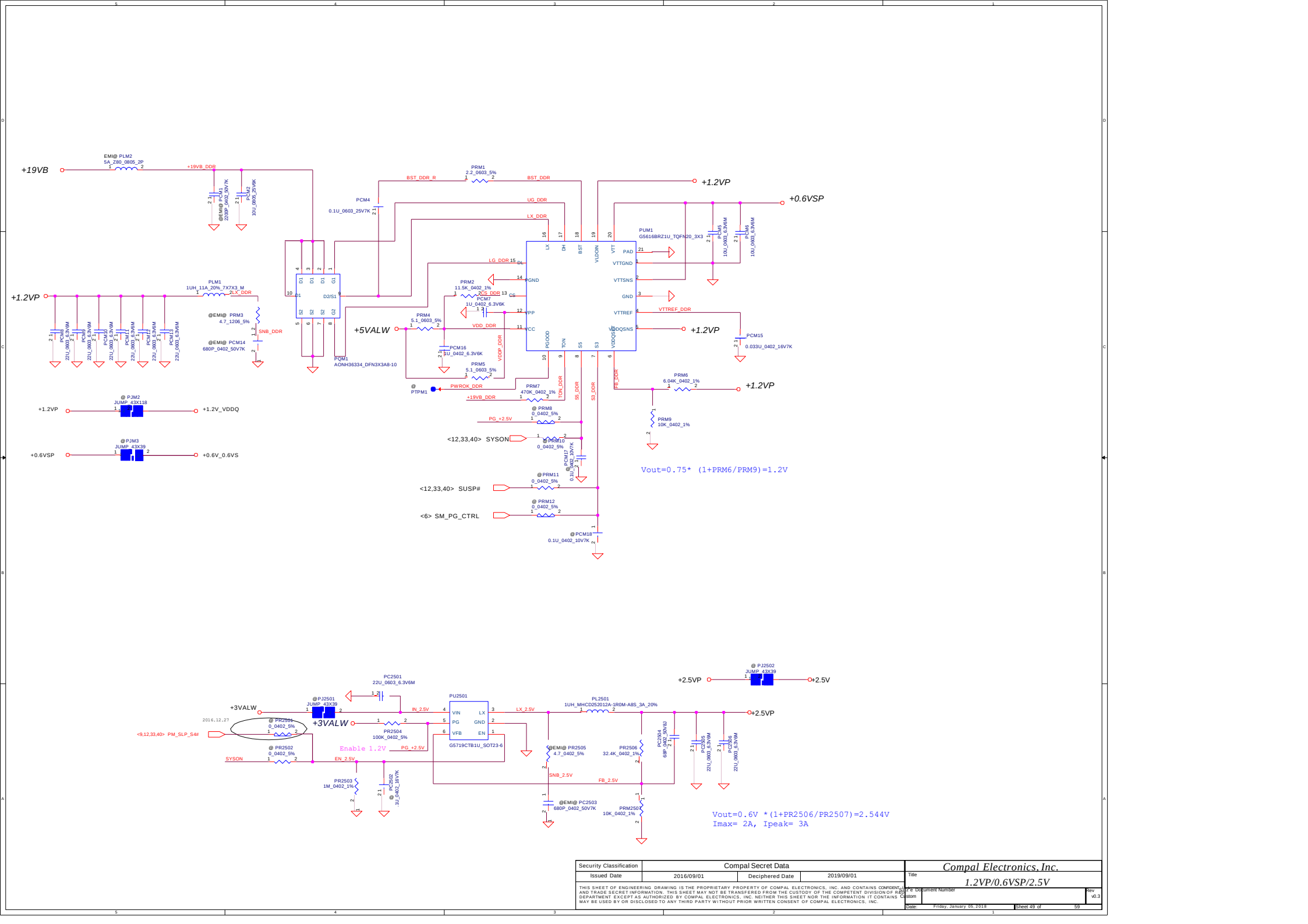
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: LA-G07BP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet: 48 of 59



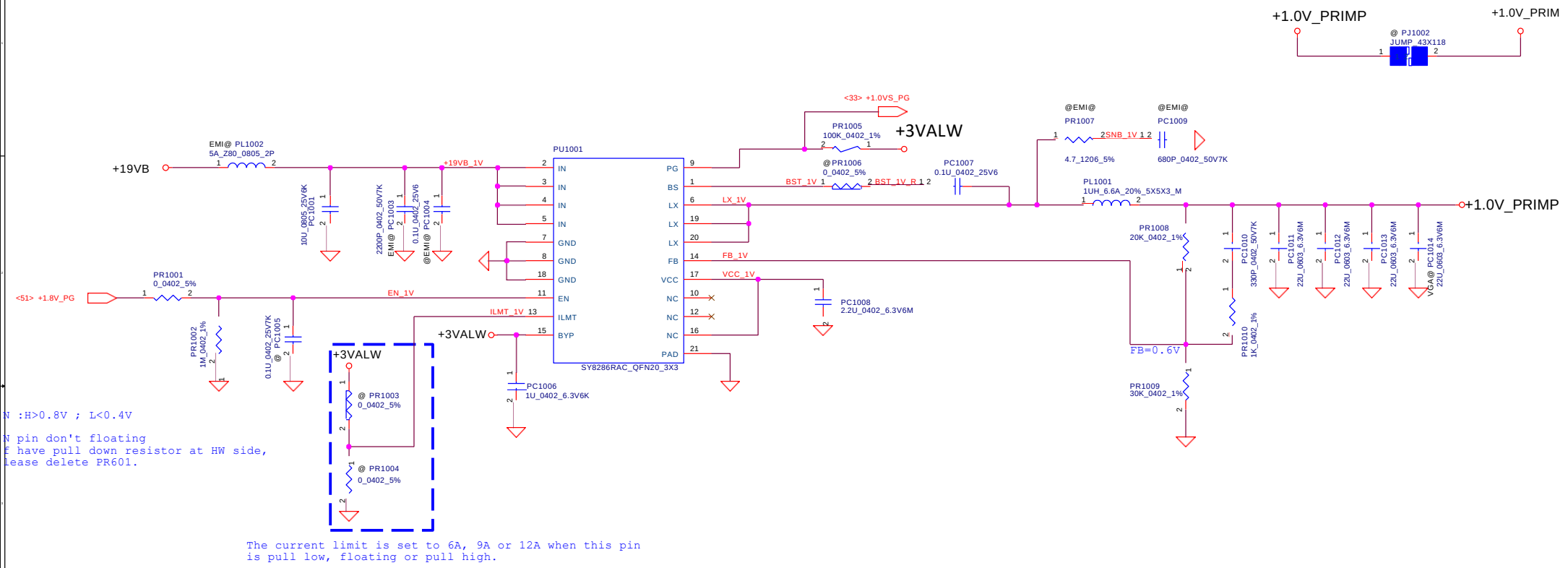
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5V

Size: C | Document Number: Custom | Rev: V0.3

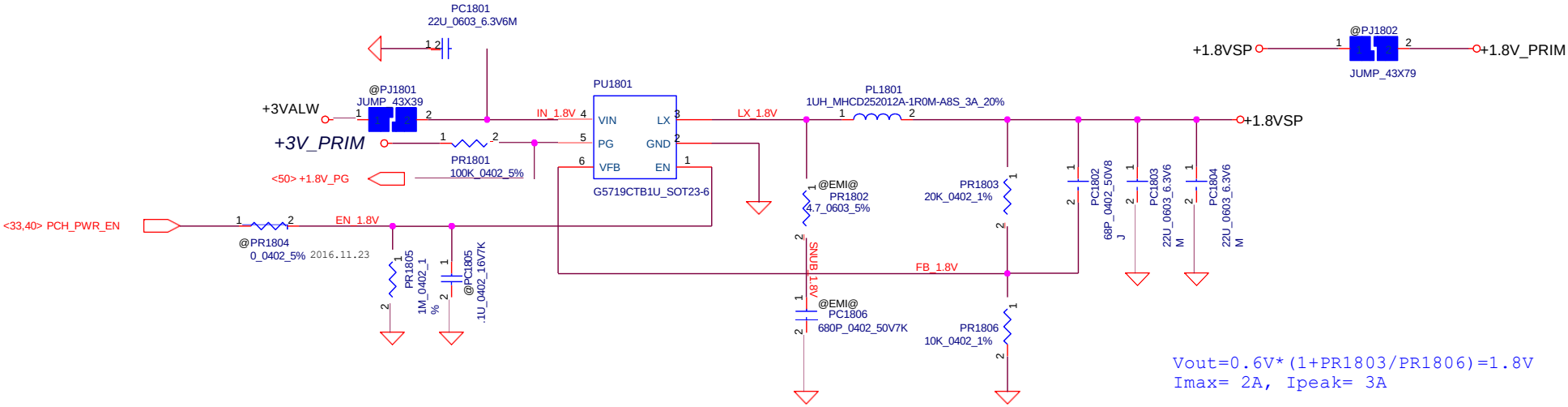
Date: Friday, January 05, 2018 | Sheet 49 of 59



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

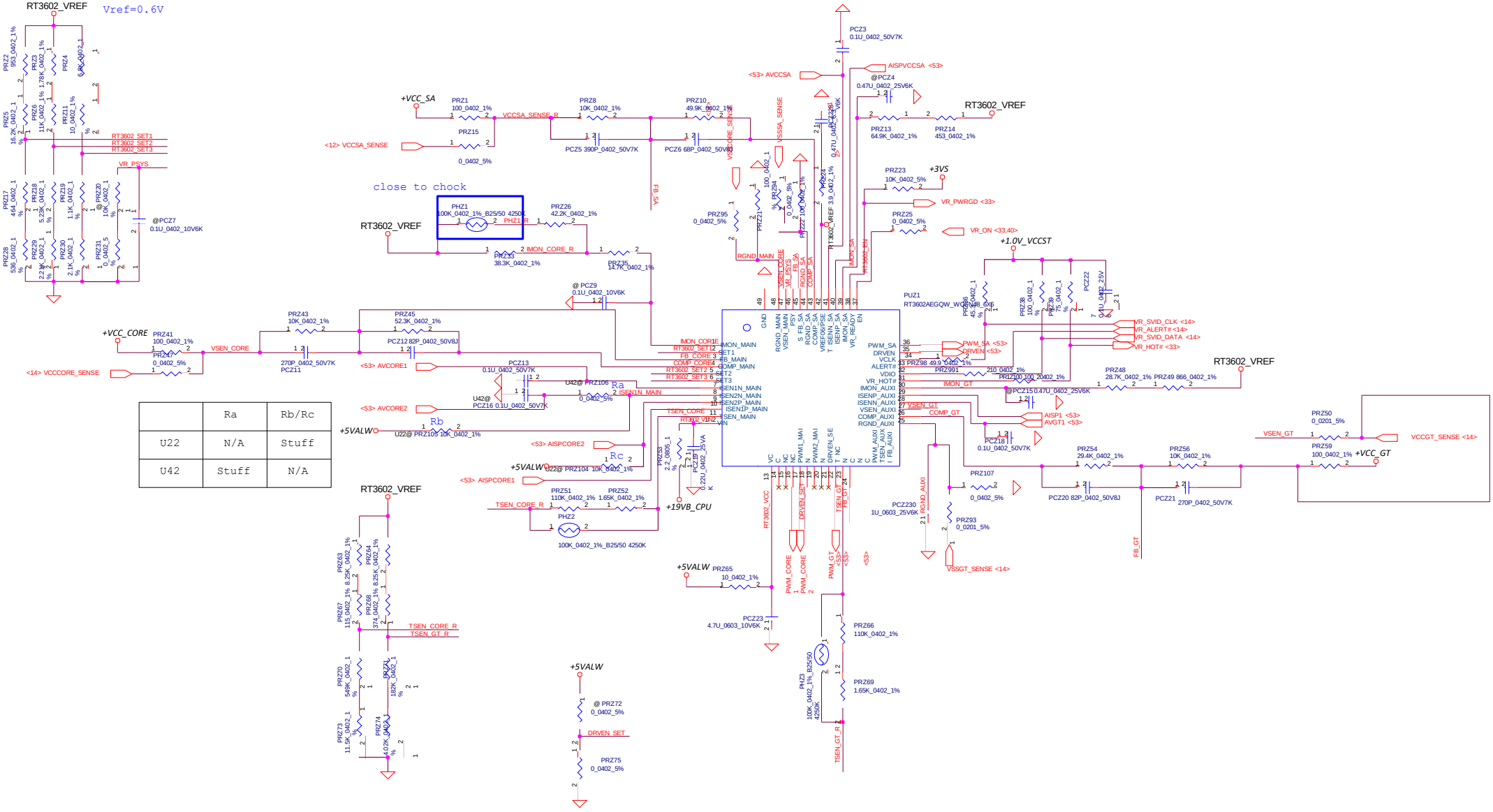
Title: 1.0V_PRIM

Size: Custom	Document Number	Rev: v0.3
Date: Friday, January 05, 2018	Sheet 50 of 59	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	1.8V_PRIM		
Size	B	Document Number	LA-G07BP(KBL-U_UMA_6L) Rev v0.3
Date:		Sheet 51 of 59	



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

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Title: CPU_CORE
Size: C
Document Number: LA-G07BP(KBL-U_UMA_6L)
Rev: V0.3
Date: Friday, January 05, 2018
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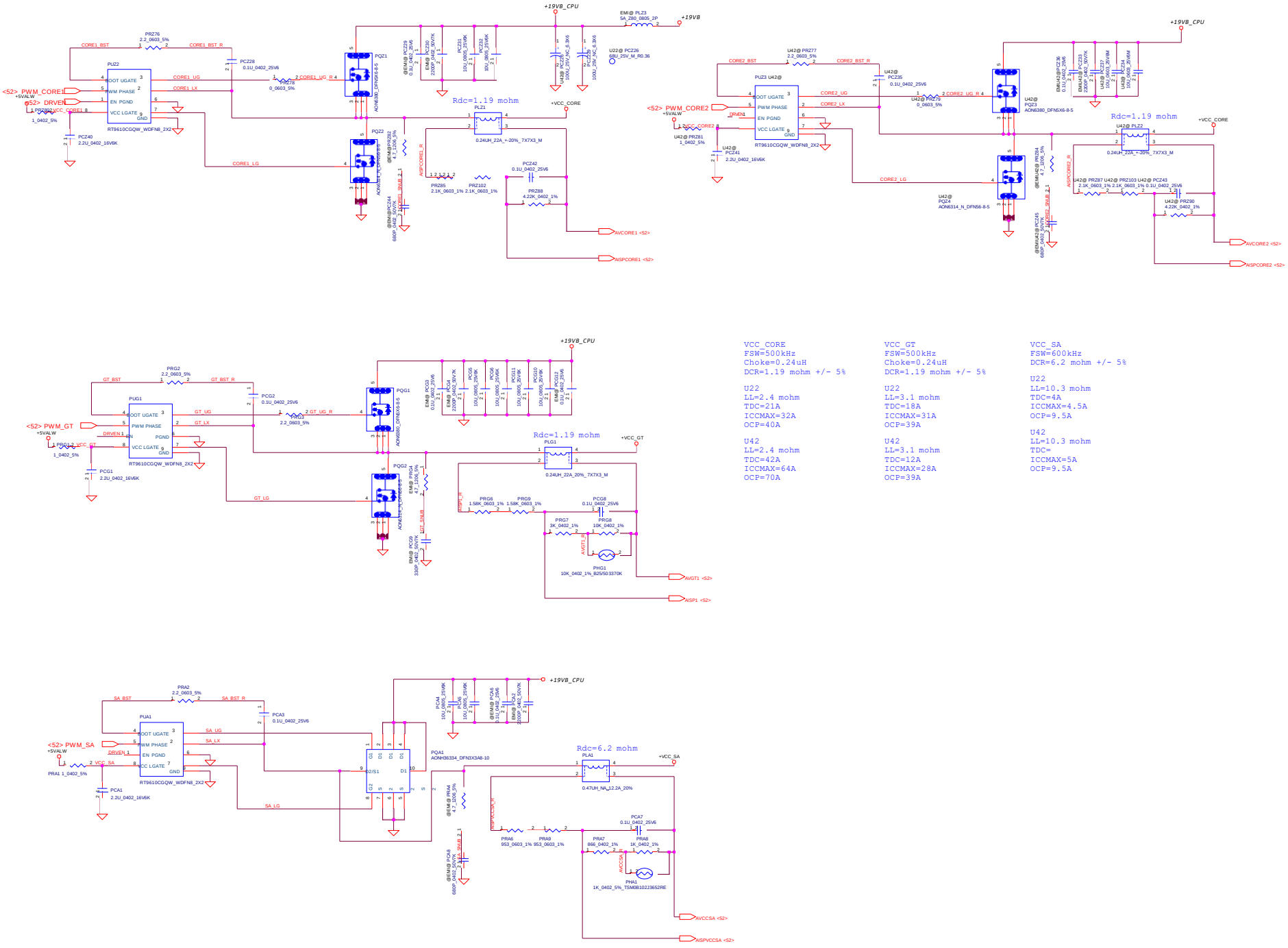

VCC_CORE
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=5A
OCP=9.5A

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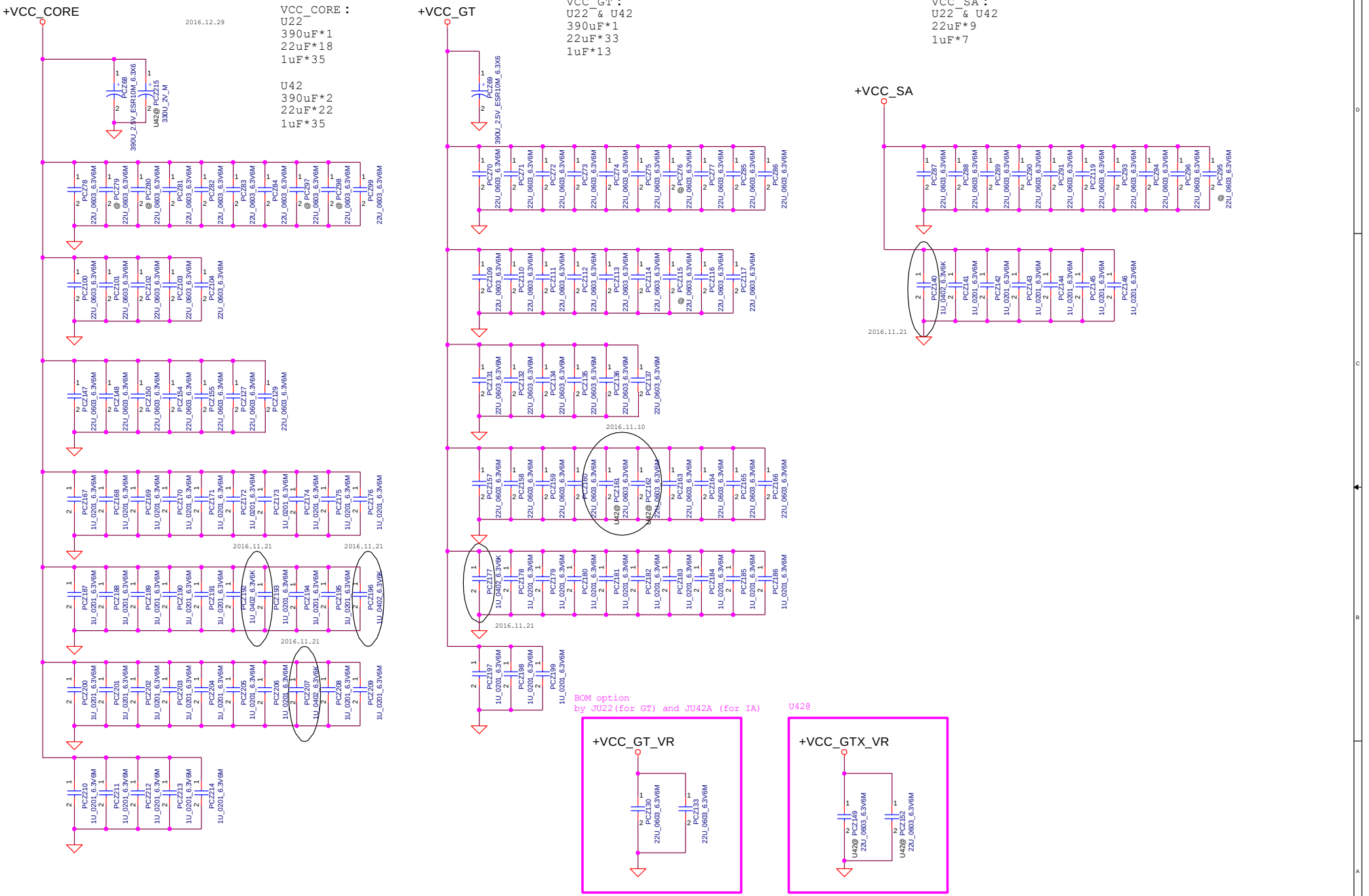
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	CPU Power stage		
Size	Document Number		Rev
	LA-G07BP(KBL-U_UMA_6L)		X0.3
Date: Friday, January 05, 2018		Sheet 93 of 99	



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *PROCESSOR DECOUPLING*

Size: E-e Document Number: LA-G07BP(KBL-U_UMA_6L) Rev: v0.3

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

BOM Structure Table (1/2)

Function	*Stuff*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

i3_7100U_R1@ / i3_7100U_R3@ — UC1 — i3_7100U — SA0000A38H0 / SA0000A38J0 — S IC FJ8067702739738 SR343 H0 2.4G BGA

U_i5_7200U_SR342@ / i5_7200U_R3@ — UC1 — U_SI i5-7200U_SR342 H0 2.5G — SA0000A37H0 — S IC FJ8067702739739 SR342 H0 2.5G BGA

U_i7_7500U_SR341@ / i7_7500U_R3@ — UC1 — U_SI i7-7500U_SR341 H0 2.7G — SA0000A34F0 — S IC FJ8067702739740 SR341 H0 2.7G BGA

R_i5_8250U_QNEF@ / i5_8250U_R3@ — UC1 — R_SI i5_8250U_QNEF Y0 1.6G — SA0000AWB10 — S IC FJ8067703282221 SR3LA Y0 1.6G FCBGA

R_i7_8550U_SR3LC@ / i7_8550U_R3@ — UC1 — R_SI i7-8550U_SR3LC Y0 1.8G — SA000AWC20 — S IC FJ8067703281816 SR3LC Y0 1.8G FCBGA

MX110@ / MX130@ — UV1 — N16V-GMR1-S-A2 — SA00009IT00 — S IC N16V-GMR1-S-A2 BGA595P

UV1 — N16S-GTR-S-A2 — SA00009FP00 — S IC N16S-GTR-S-A2 BGA 595PGPU

ZZZ — 2G Micron — M2G_R1@ X7674032L01 / M2G_R3@ X7674032L06

ZZZ — 4G Micron — M4G_R1@ X7674032L26 / M4G_R3@ X7674032L29

ZZZ — 2G Hynix — H2G_R1@ X7674032L04 / H2G_R3@ X7674032L07

ZZZ — 4G Hynix — H4G_R1@ X7674032L25 / H4G_R3@ X7674032L28

ZZZ — 2G Samsung — S2G_R1@ X7674032L05 / S2G_R3@ X7674032L08

ZZZ — 4G Samsung — S4G_R1@ X7674032L27 / S4G_R3@ X7674032L30

45@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

RO0000003HM

R_i3_7020U_QN96@ — UC1 — R_SI_i3_7020U_QN96 Y0 2.3G — SA0008LD00 — S IC A32 FJ8067703282620 QN96 Y0 2.3G

R_i3_8130U_QP8K@ — UC1 — R_SI_i3-8130U_QP8K Y0 2.2G — SA0008KN10 — S IC A32 FJ8067703282227 QP8K Y0 2.2G

R_i7_8550U_QNBF@ — UC1 — R_SI_i7_8550U_QNBF Y0 1.8G — SA000AWC10 — S IC A32 FJ8067703281816 QNBF Y0 1.8G

U_i3_7020U_QNZU@ — UC1 — U_SI_i3-7020U_QNZU H0 2.3G — SA0008LH00 — S IC A32 FJ8067702739769 QNZU H0 2.3G

<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR_1/IR_2 Camera
6	IR_2 Camera
7	Card Reader
8	X
9	X
10	X

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0		DESTINATION		CLK
1				1	USB3.0 Type-C		X
2				2	USB3.0 Type-C		X
3				3	USB2.0/USB3.0		X
4				4	USB2.0/USB3.0		X
5	1			5	GPU(DIS only)		CLK0
6	2			6	GPU(DIS only)		
7	3				GPU(DIS only)		
8	4				GPU(DIS only)		
9	5				LAN		CLK1
10	6				WLAN		CLK2
11	7	0			HDD		X
12	8	1a			ODD		CLK3
13	9				X		X
14	10				X		X
15	11	1b*			NVMe x2	X	CLK4
16	12	2				SATA SSD	X

DAX — KBLU-2G — KBLU_2G@ — DA6001WM000 — PCB 29M LA-G07BP REV0 MB 3 PCB 29L LA-G07CP REV0 MB 3

DAX — KBLR-2G — KBLR_2G@ — DA6001WR000

DAX — KBLU-4G — KBLU_4G@ — DA8001EH000

DAX — KBLR-4G — KBLR_4G@ — DA8001EI000

ZZZ — DAZ_U2G — DAZ_U2G@ — DAZ23T00600

ZZZ — DAZ_R2G — DAZ_R2G@ — DAZ23T00500

ZZZ — DAZ_U4G — DAZ_U4G@ — DAZ23T00600

ZZZ — DAZ_R4G — DAZ_R4G@ — DAZ23T00500

DAX — KBLU-UMA — KBLU_UMA@ — DA6001YA000 — PCB 29M LA-G07BP REV0 M/B 3 PCB 29L LA-G07BP REV0 M/B 3

DAX — KBLR-UMA — KBLR_UMA@ — DA6001YB000

ZZZ — EMC for EE — X4E@ — X4EABB32L01 — SMT EMC FOR EE AG07C EPK50

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