Compal Confidential

V15 /DH5VF
V17 /DH7VF
Vx15/DH53F
Vx17/DH73F

MB Schematic Document

Intel CoffeeLake H
Nvidia N17P-G0/G1

LA-F951P

Rev:1A

2018.02.22

Security Classification	Compal Secret Data		
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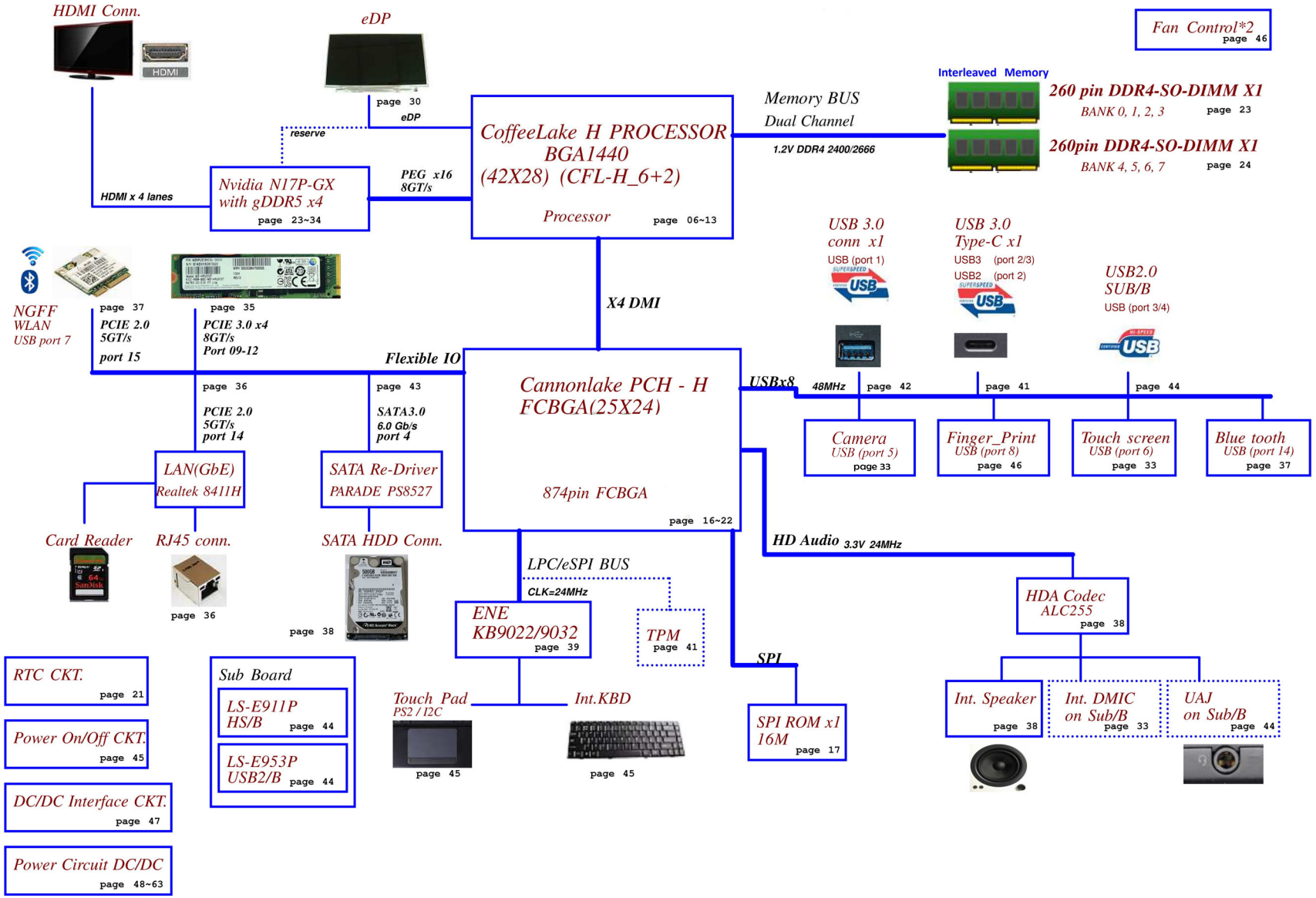
Title: *Cover Sheet*

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 1 of 67



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Title	Block Diagrams		
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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VS)	N17P-GX (VGA)	0x9E		
	EC			
	CC controller 179F			
	TMS			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
VRAM BOM Select	X76@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
USB charger	CHG@
non USB charger	NCHG@
G-Sensor	GSEN@
Thermal sensor	TMS@
for SW debug board	UART@
Intel CNVi (reserve)	CNVI@
Finger Print	FP@
FinerPrint(with PBA)	PBA@
USB Type-C CC controller	TYPEC@
EMI/ESD requirement	EMC@
EMI/ESD require reserve	XEMC@
FP ESD requirement	FPEMC@
28P keyboard connector	V15@
32P keyboard connector	VX15@
SATA HDD W REDRIVER	SATARD@
SATA HDD WO REDRIVER	SATANRD@
NV N17P-G0(1050)	G0@
NV N17P-G1(1050TI)	G1@
i5 CPU	i5@
i7 CPU	i7@
ALC 255 Codec	255@
ALC 256 Codec	256@
Codec LDO mode	LDO@
Codec Switch mode	SWR@

State

SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	HIGH	HIGH	HIGH	ON	ON	ON	ON
RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+1.8VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table

43 Level	Description	BOM Structure
Vx15,Sienta		
431AB1BOL60	SMT MB AF951 DH53F I5QP89 PG1 4G 32HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G1@/VX15@/SATANRD@
431AB1BOL61	SMT MB AF951 DH53F I7QP86 PG1 4G 32HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G1@/VX17@/SATANRD@
431AB1BOL66	SMT MB AF951 DH53F I78750 PG1 4G 32HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/VX15@/SATANRD@
V15, Vx15-Freed		
431AB1BOL62	SMT MB AF951 DH53F I5QP89 PG0 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G0@/V15@/SATANRD@/FP@
431AB1BOL63	SMT MB AF951 DH53F I78750 PG0 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G0@/V15@/SATANRD@/FP@
431AB1BOL64	SMT MB AF951 DH53F I5QP89 PG1 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G1@/V15@/SATANRD@/FP@
431AB1BOL65	SMT MB AF951 DH53F I78750 PG1 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATANRD@/FP@
V17		
431AB1BOL65	SMT MB AF951 DH7VF I5QP89 PG0 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G0@/V15@/SATARD@/FP@
431AB1BOL65	SMT MB AF951 DH7VF I78750 PG0 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G0@/V15@/SATARD@/FP@
431AB1BOL65	SMT MB AF951 DH7VF I5QP89 PG1 4G 28HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I5@/G1@/V15@/SATARD@/FP@
431AB1BOL65	SMT MB AF951 DH7VF I78750 PG1 4G 32HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATARD@/FP@
VX17		
431AB1BOL08	SMT MB AF951 DH7VF I5QP89 PG1 4G 32HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATARD@/FP@
431AB1BOL09	SMT MB AF951 DH7VF I78750 PG1 4G 32HDMI	255@/CHG@/CMC@/CNVI@/LDO@/IOAC@/TYPEC@/VGA@/QNDQ@/I7@/G1@/V15@/SATARD@/FP@

X76730BOL51 SAMSUNG1280
X76730BOL52 HYNLX1280
X76730BOL53 SAMSUNG2560
X76730BOL54 HYNIX2560
X76730BOL55 MICRON2560

BOARD ID Table

	V series		Vx series	
	Board ID	PCB Revision	Board ID	PCB Revision
15"	0	0.1	10	0.1
	1	0.2	11	0.2
	2	1.0	12	1.0
	3	1.A	13	1.A
	4		14	
17"	5	1.0	15	1.0
	6		16	
	7		17	
	8		18	
	9		19	

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Title: Notes List
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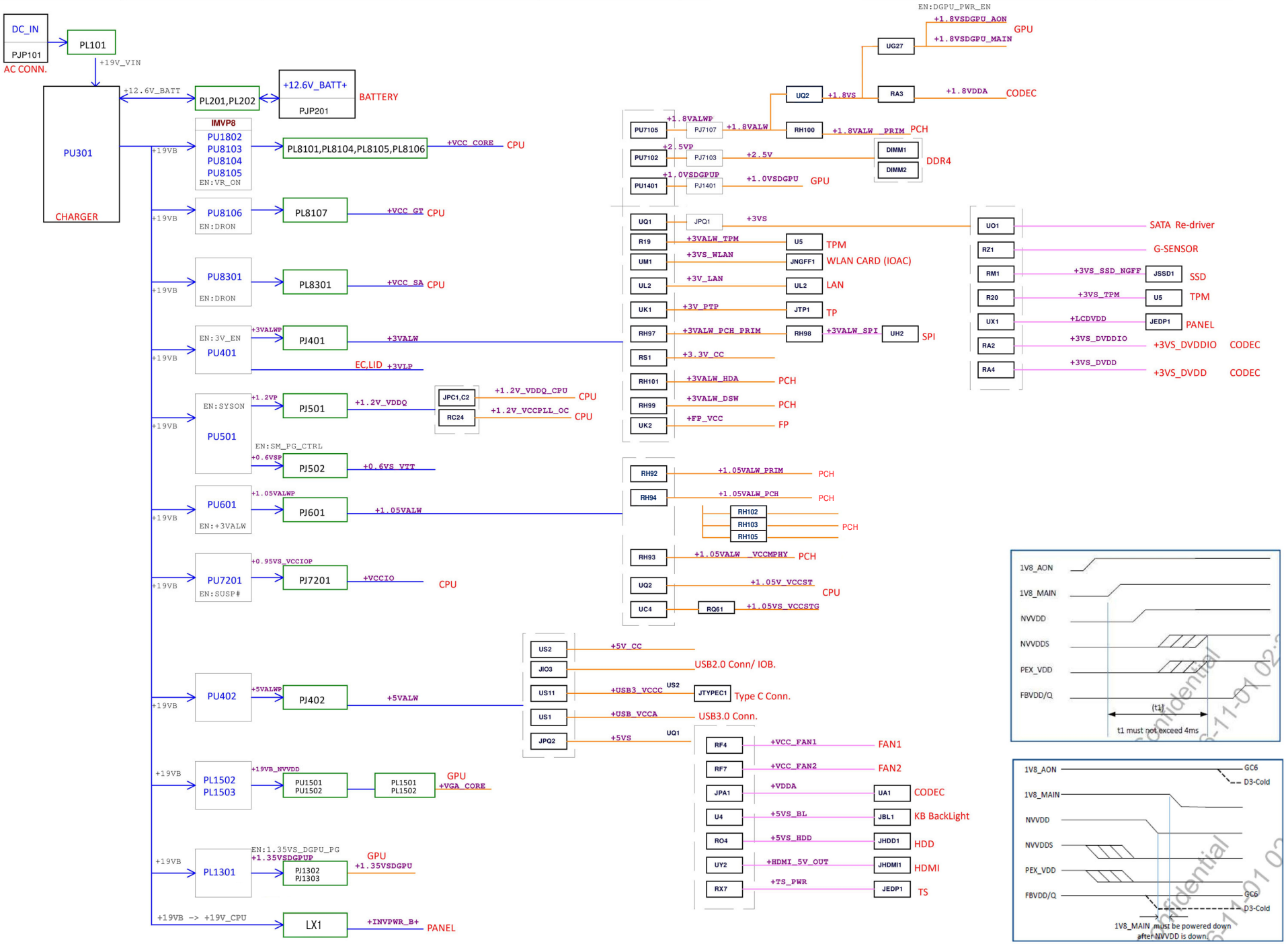

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Title	Power Map		
Size	Document Number		Rev
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DH5VF_EVT Power Sequence AC mode

BIOS ver: V0.02W1
EC: ver: V002AT04

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Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

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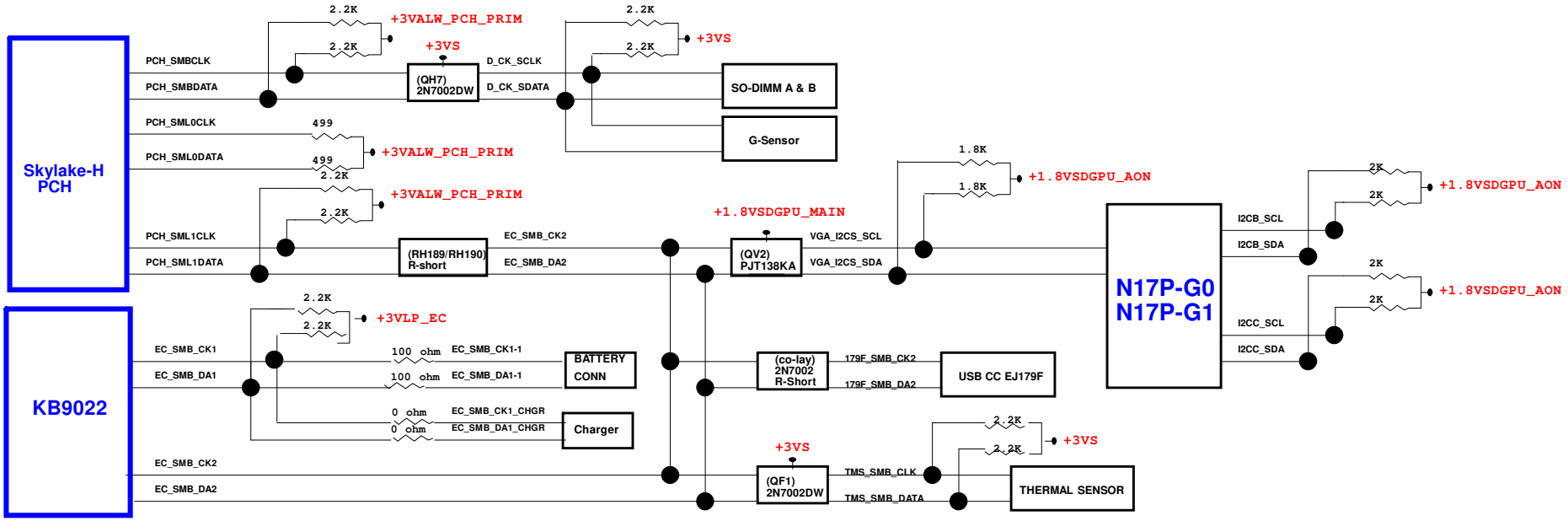

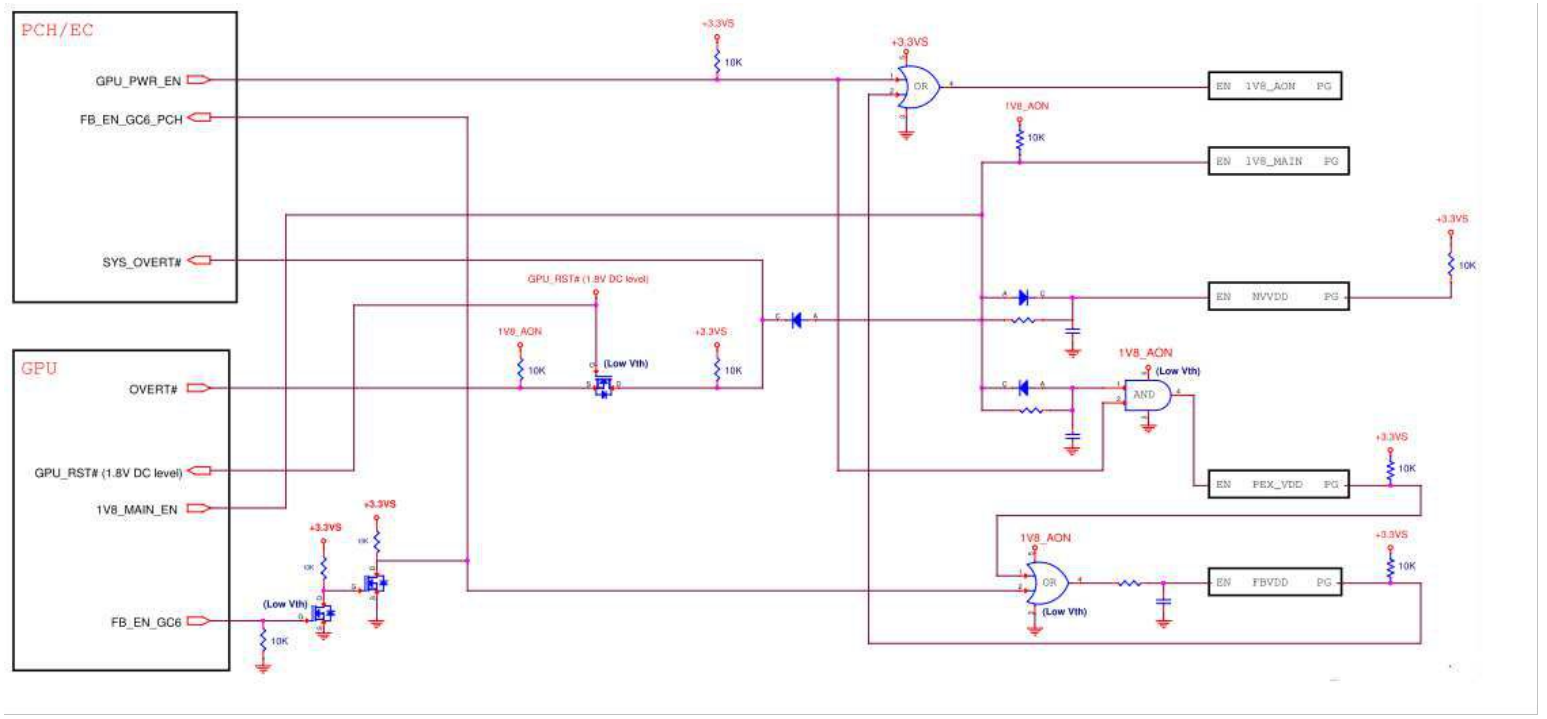

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Compal Electronics, Inc.			
Title	N17E-GDDR5_D		
Size	Document Number		Rev
	DH5VF M/B LA-F591PR01		1.0
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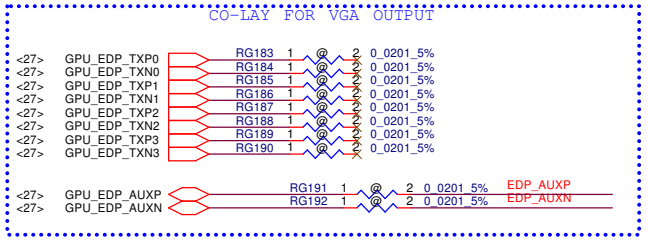

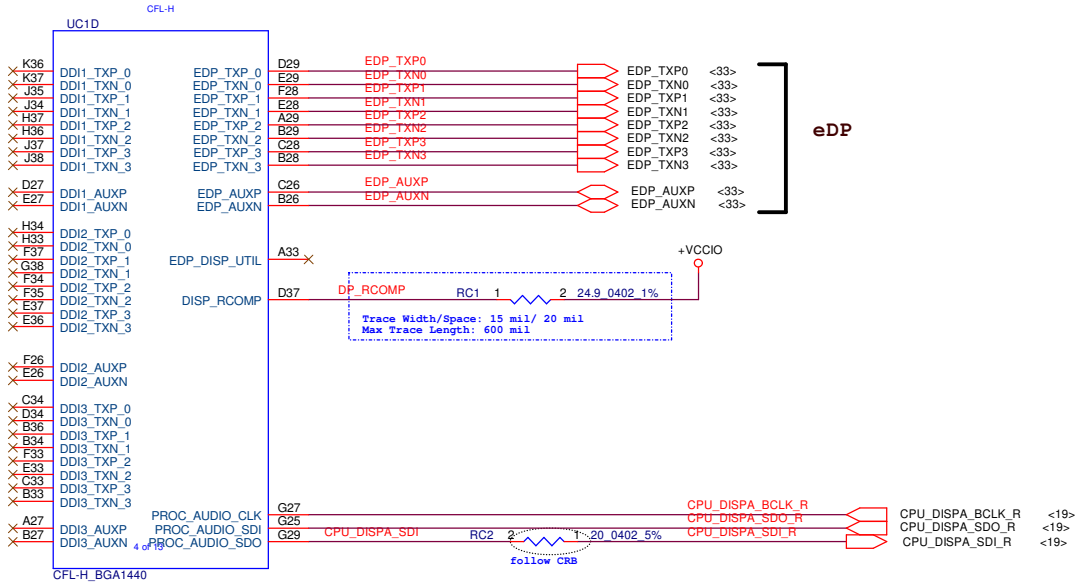

Coffee Lake-H CPU SKU

UC1 — I5@ — CFL-H 2.3G BGA — SA0000BPJ40

UC1 — I7@ — CFL-H 2.2G BGA — SA0000BPZ40

Cannon Lake PCH SKU

UH1 — QNDQ@ — CNP-H_BGA874 — SA0000BVP10

NV N17P SKU

UV1 — G0@ — N17P-G0-A1 — SA0000A0540

UV1 — G1@ — N17P-G1-A1 — SA0000A0660

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Title: CFL-H(1/8)DDI/eDP

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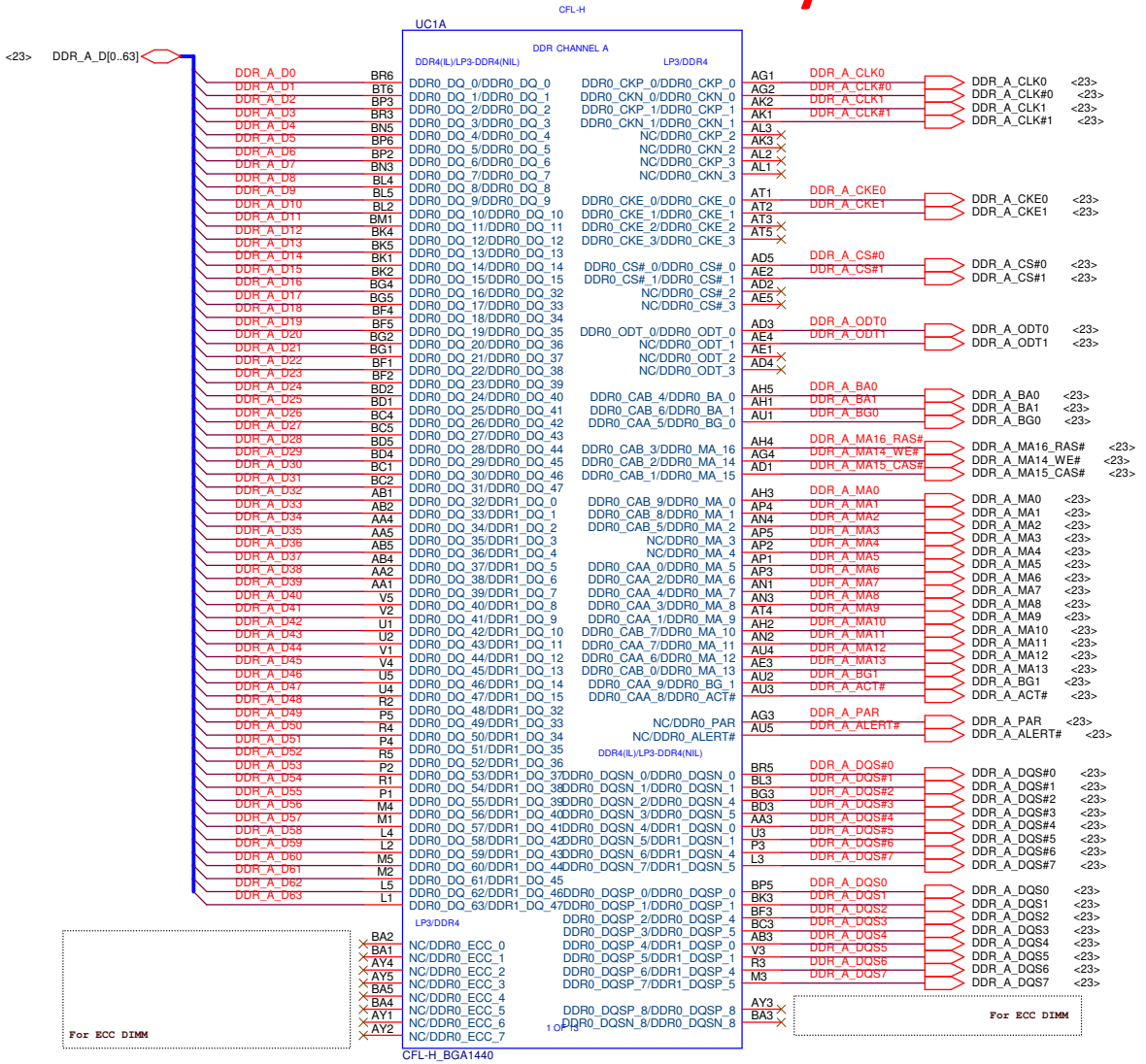
CHANNEL-A

Interleaved Memory



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Title: CFL-H(2/8)DIMMA			
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
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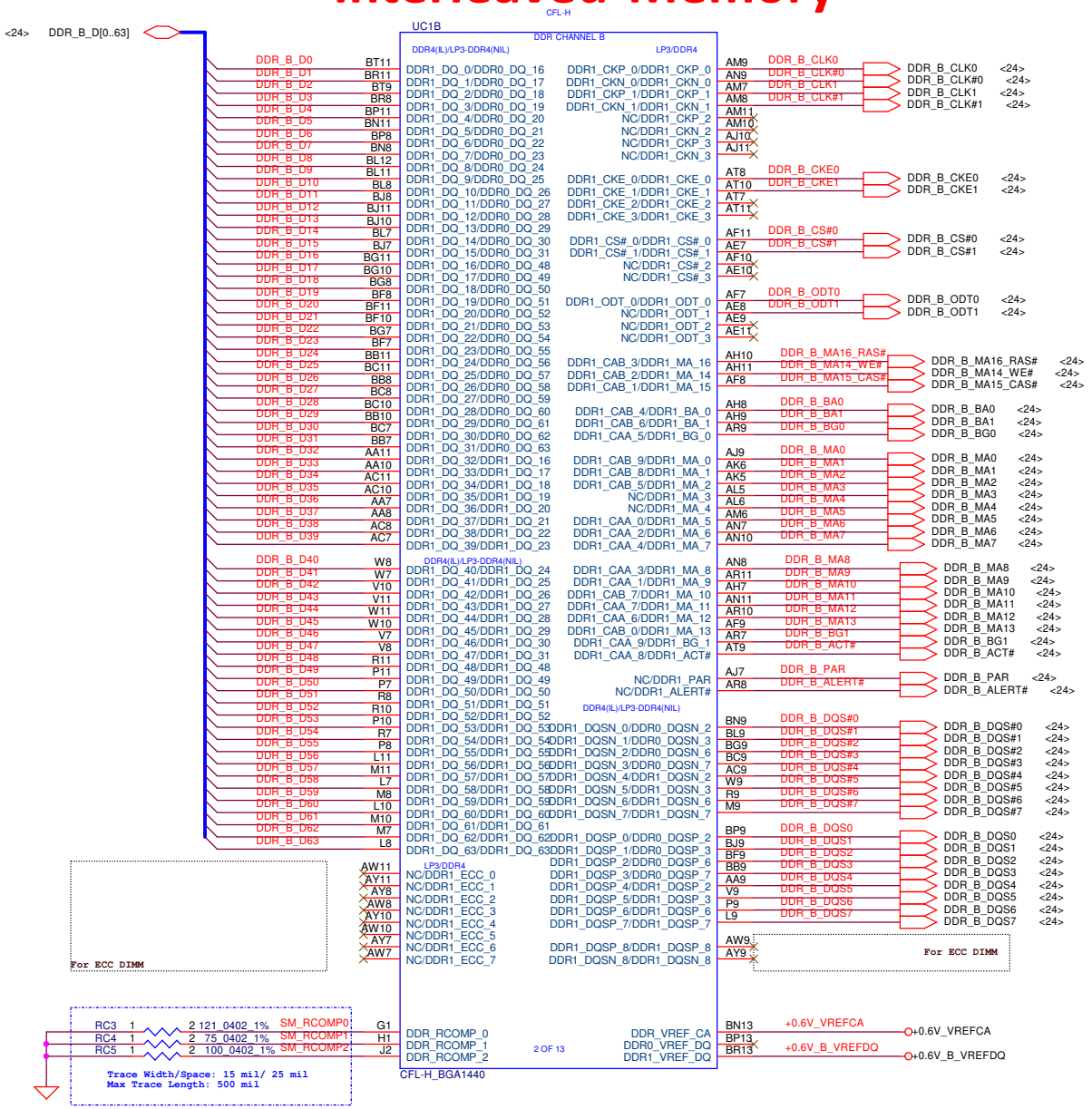
CHANNEL-B

Interleaved Memory



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Compal Electronics, Inc.			
Title	CFL-H(3/8)DIMMB		
Size	Document Number		Rev
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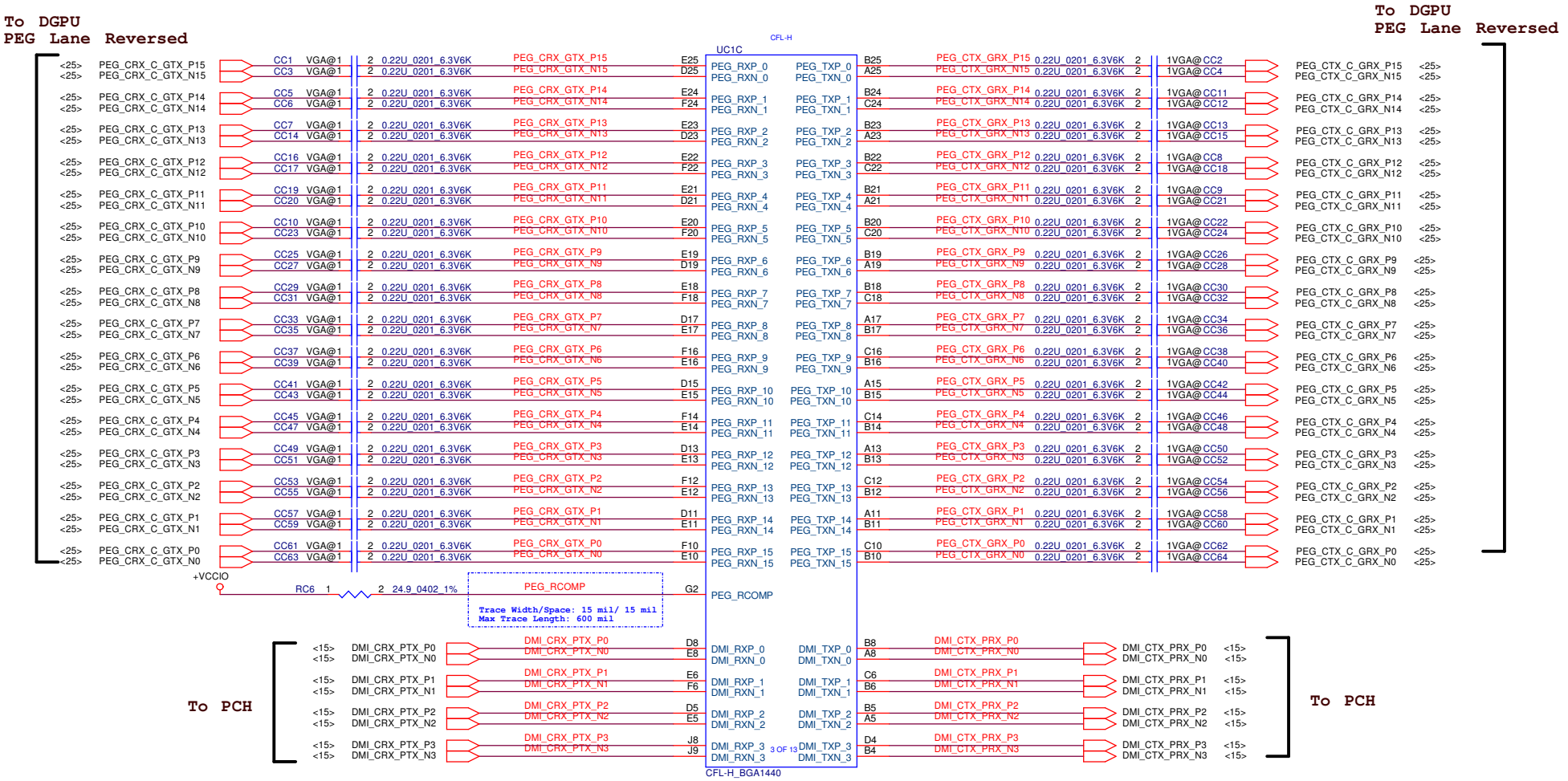
PEG&DMI



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: PEG/DMI			
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
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571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

UC1E
CFL-H
CFL-H_BGA1440
5 OF 13

PCH_CPU_BCLK_P / PCH_CPU_BCLK_N → BCLKP / BCLKN
PCH_CPU_PCIBCLK_P / PCH_CPU_PCIBCLK_N → PCI_BCLKP / PCI_BCLKN
PCH_CPU_24M_CLK_P / PCH_CPU_24M_CLK_N → CLK24P / CLK24N
CPU_SVID_ALERT# / CPU_SVID_CLK / CPU_SVID_DAT → VIDALERT# / VIDSCK / VIDSOUT
H_PROCHOT#_R → PROCHOT#
DDR_PG_CTRL → DDR_VTT_CNTL
EC_VCCST_PG → VCCST_PWRGD
H_CPUPWRGD → PROCPWRGD
H_PLTRST_CPU# → RESET#
H_PM_SYNC_R → PM_SYNC
H_PM_DOWN → PM_DOWN
H_PECI → PECI
PCH_THERMTRIP#_R → THERMTRIP#
SKTOCC# → SKTOCC#
CATERR# → CATERR#
PROC_SELECT# → ZVM# / MSM#
RSVD1 / RSVD2

CFG_0 BN25 CFG0
CFG_1 BN27
CFG_2 BN26 CFG2
CFG_3 BN28
CFG_4 BR20 CFG4
CFG_5 BM20 CFG5
CFG_6 BT20 CFG6
CFG_7 BP20 CFG7
CFG_8 BR23
CFG_9 BR22
CFG_10 BT23
CFG_11 BT22
CFG_12 BM19
CFG_13 BR19
CFG_14 BP19
CFG_15 BT19
CFG_17 BN23
CFG_16 BP23
CFG_19 BR22
CFG_18 BN22

CFG0 RC7 1 @ 2 1K_0402_5%
CFG2 RC8 1 2 1K_0402_5%
CFG4 RC9 1 2 1K_0402_5%
CFG5 RC10 1 @ 2 1K_0402_5%
CFG6 RC11 1 @ 2 1K_0402_5%
CFG7 RC12 1 @ 2 1K_0402_5%

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
* 0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
* 0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
* 11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

Sensitive
Sensitive

BPM#_0 BR27 XDP_BPM#0 → TC1 TP@
BPM#_1 BT27 XDP_BPM#1 → TC2 TP@
BPM#_2 BM31 XDP_BPM#2 → TC3 TP@
BPM#_3 BT30 XDP_BPM#3 → TC4 TP@

PROC_TDO BT28 CPU_XDP_TDO → CPU_XDP_TDO <19>
PROC_TDI BL32 CPU_XDP_TDI → CPU_XDP_TDI <19>
PROC_TMS BP28 CPU_XDP_TMS → CPU_XDP_TMS <19>
PROC_TCK BR28 CPU_XDP_TCK0 → CPU_XDP_TCK0 <19>
To be confirm
PROC_TRST# BP30 CPU_XDP_TRST# → CPU_XDP_TRST# <22>
PROC_PREQ# BL30 XDP_PREQ# → TC19 TP@
PROC_PRDY# BP27 XDP_PRDY# → TC20 TP@

CFG_RCOMP BT25 — CFG_RCOMP 1 RC18 2 49.9_0402_1%
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

XDP_PREQ# → XDP_PREQ# <22>
XDP_PRDY# → XDP_PRDY# <22>

<19> H_CPUPWRGD
<18> H_PLTRST_CPU#
<18> H_PM_SYNC_R
<18,39> H_PECI
<18> PCH_THERMTRIP#_R
RC17 1 @ 2 0_0402_5%
TP@ TC5 SKTOCC#
TP@ TC6 CATERR#

PROC_SELECT# should be unconnected on CFL processor
EDS1.2 8/21

XEMC@ 0.1U_0402_10V6K 1 2 CC65 H_CPUPWRGD
EMC@ 1000P_0402_50V7K 1 2 CC66 H_PROCHOT#_R
XEMC@ 0.1U_0402_10V6K 1 2 CC67 H_THERMTRIP#
EMC@ 1000P_0402_50V7K 1 2 CC68 EC_VCCST_PG
Near CPU side
follow 1050 Request 8/21

+1.05V_VCCST
RH1 1 2 1K_0402_5% H_THERMTRIP#

+1.2V_VDDQ
UC3 74AUP1G07GW_TSSOP5 (NC, A, GND, VCC, Y)
DDR_PG_CTRL
CC69 0.1U_0402_10V6K
SM_PG_CTRL
+3VS
RC23 330K_0402_5%
SM_PG_CTRL <52>
PU 330K follow CRB 8/21

+1.05VS_VCCSTG
Place to CPU side
RC76 2 CMC@ 1 51_0402_5% CPU_XDP_TMS
RC77 2 CMC@ 1 51_0402_5% CPU_XDP_TDI
RC78 2 CMC@ 1 51_0402_5% CPU_XDP_TDO
Place to CPU side
RC79 2 CMC@ 1 51_0402_5% CPU_XDP_TCK0
RC80 2 @ 1 51_0402_5% PCH_JTAG_TCK1
RC81 2 @ 1 51_0402_5% CPU_XDP_TRST#
PCH_JTAG_TCK1 <19>

+1.05VS_VCCSTG
RC21 1K_0402_5%
<39,50> H_PROCHOT#
RC14 1 2 499_0402_1% H_PROCHOT#_R
+1.05V_VCCST
RC22 1K_0402_5%
<39,47> EC_VCCST_PG_R
RC151 2 60.4_0402_1% EC_VCCST_PG
<18> H_PM_DOWN_R
RC16 1 2 20_0402_5% H_PM_DOWN
RH2 13_0402_5%

SVID
+1.05V_VCCST
RC19 56_0402_1%
RC20 100_0402_1%
<56,57> CPU_SVID_ALERT#_R
RC13 1 2 220_0402_5% CPU_SVID_ALERT#
<56,57> CPU_SVID_DAT
CPU_SVID_DAT

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Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0
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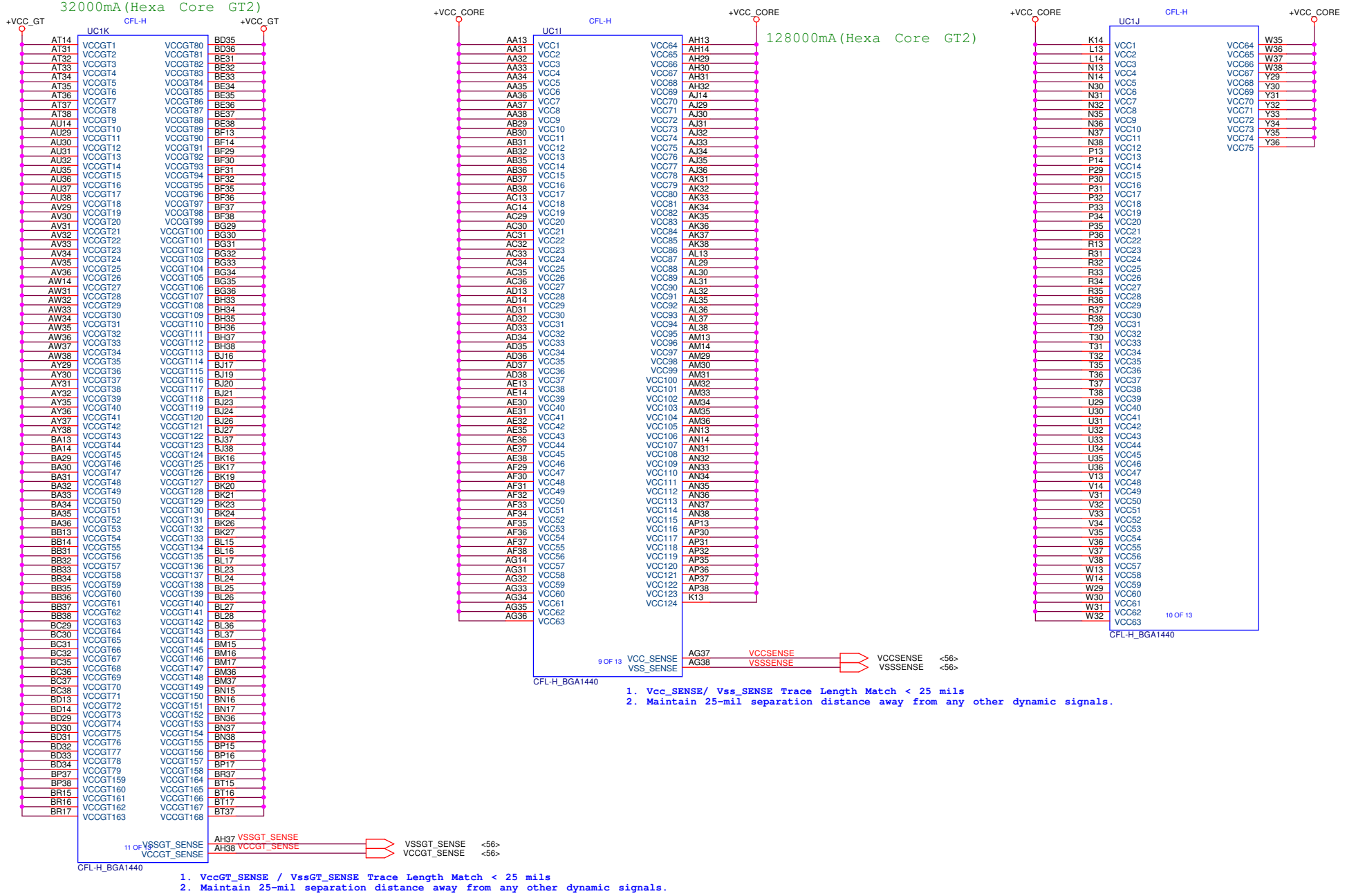
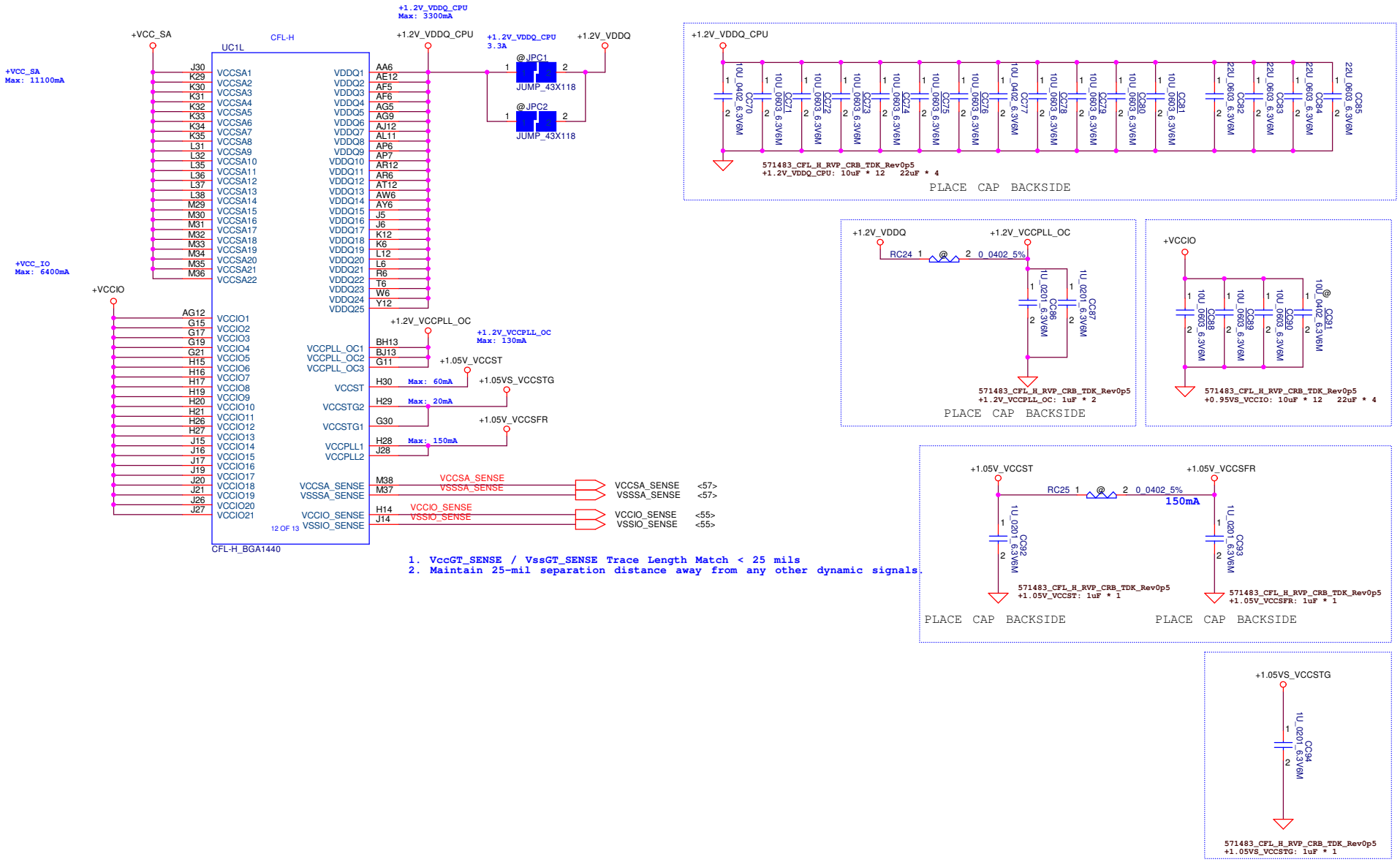


Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title: CFL-H(6/8)VCC CORE/GT			
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
Date: Thursday, February 22, 2018	Sheet 12 of 67		



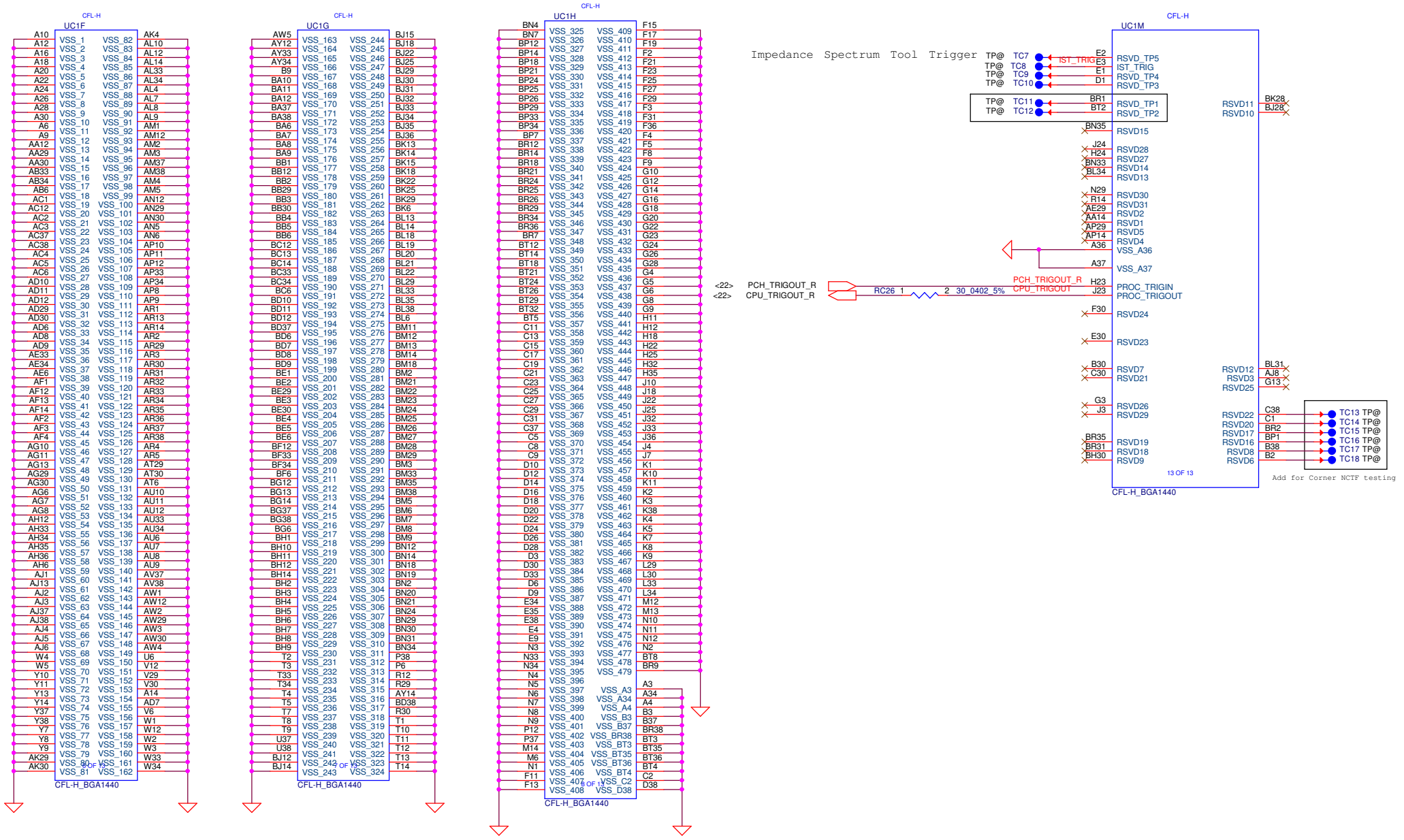
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

Date: Thursday, February 22, 2018 Sheet 13 of 67



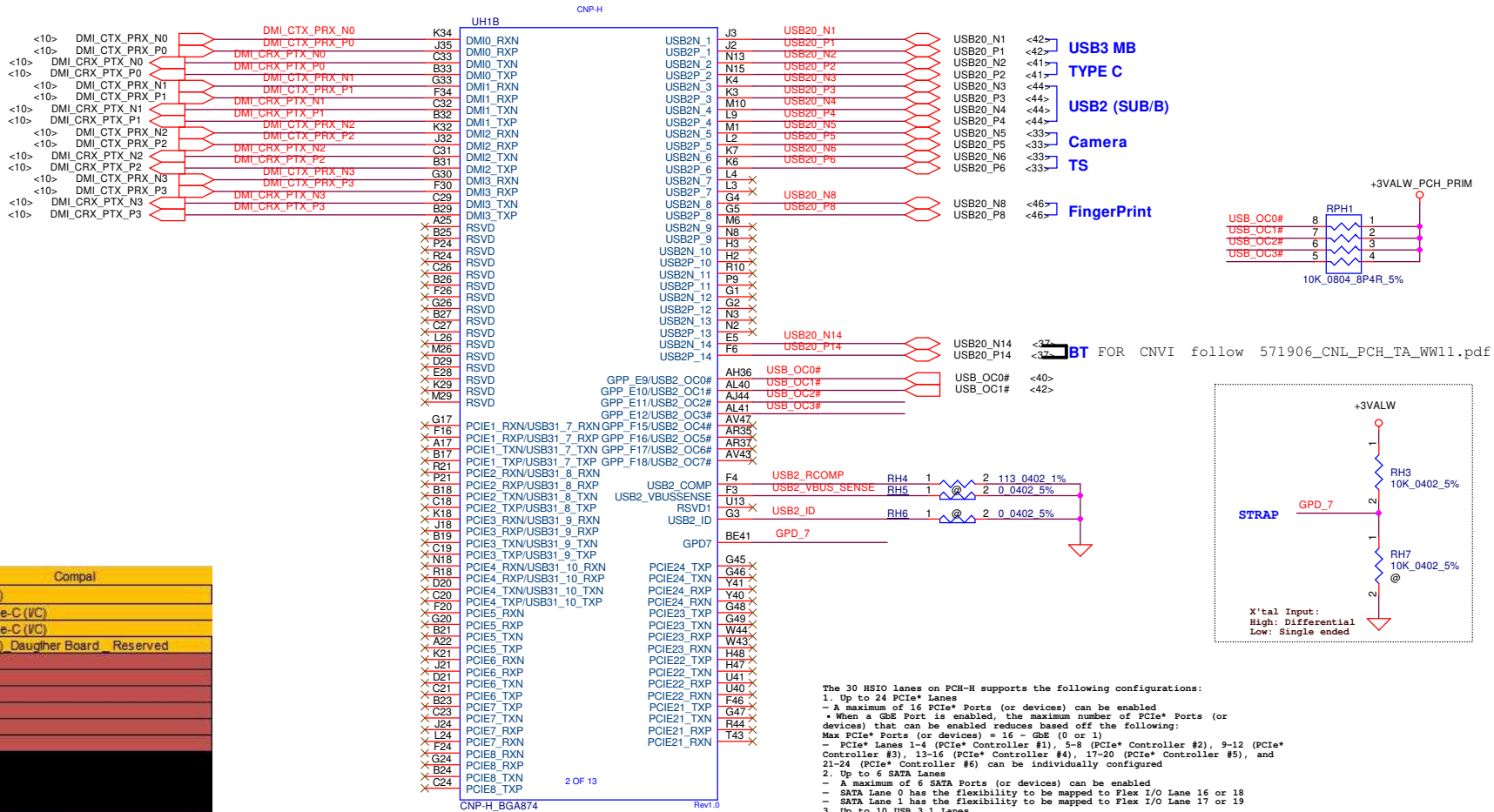
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: CFL-H(8/8)GND/RSVD

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

Date: Thursday, February 22, 2018 Sheet 14 of 67



	CFL-H (HM370)		Compal
Lane0	USB3.1 Port1		USB 3 (I/O)
Lane1	USB3.1 Port2		USB 3 Type-C (I/C)
Lane2	USB3.1 Port3		USB 3 Type-C (I/C)
Lane3	USB3.1 Port4		USB 3 (I/O)_Daugther Board _Reserved
Lane4	USB3.1 Port5		
Lane5	USB3.1 Port6		
Lane6	USB3.1 Port7	PCIe Port1	
Lane7	USB3.1 Port8	PCIe Port2	
Lane8	USB3.1 Port9	PCIe Port3	
Lane9	USB3.1 Port10	PCIe Port4	
Lane10		PCIe Port5	
Lane11		PCIe Port6	
Lane12		PCIe Port7	
Lane13		PCIe Port8	
Lane14		PCIe Port9	M.2 SSD#1 (PCIe x4)
Lane15		PCIe Port10	M.2 SSD#1 (PCIe x4)
Lane16	SATA3 Port0	PCIe Port11	M.2 SSD#1 (PCIe x4)
Lane17	SATA3 Port1	PCIe Port12	M.2 SSD#1 (PCIe x4)
Lane18	SATA3 Port0*	PCIe Port13	
Lane19	SATA3 Port1*	PCIe Port14	LAN+CR
Lane20	SATA3 Port2	PCIe Port15	WIFI
Lane21	SATA3 Port3	PCIe Port16	
Lane22	SATA3 Port4	PCIe Port17	HDD
Lane23	SATA3 Port5	PCIe Port18	
Lane24		PCIe Port19	
Lane25		PCIe Port20	
Lane26		PCIe Port21	
Lane27		PCIe Port22	
Lane28		PCIe Port23	
Lane29		PCIe Port24	
	USB2 Port1		USB 3 (I/O)
	USB2 Port2		USB 3 Type-C (I/C)
	USB2 Port3		USB 2 (I/O)
	USB2 Port4		USB 2 (I/O)
	USB2 Port5		CCD
	USB2 Port6		TS
	USB2 Port7		
	USB2 Port8		FP
	USB2 Port9		
	USB2 Port10		
	USB2 Port11		
	USB2 Port12		
	USB2 Port13		
	USB2 Port14		BT

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configuratiom , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE		SATA 0a	GbE	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5						
																		SATA 1a												
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

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Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

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PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT — RH11 EMC@ 33_0402_1% — XTAL_24M_PCH_OUT_R

XTAL_24M_PCH_IN — RH8 1M_0402_5% — RH9 EMC@ 33_0402_1% — XTAL_24M_PCH_IN_R

YH1 24MHZ_18PF_XRCGB24M000F2P51R0 (NC NC)

C5H 33P_0402_50V8J — C6H 18P_0402_50V8J

PCH_RTCX1 — RH12 10M_0402_5% — PCH_RTCX2

YH2 32.768KHZ_9PF_X1A000141000200

C7H 10P_0402_50V8J — C8H 10P_0402_50V8J

Trace Space: 15 mil
Max Trace Length: 1000 mil

use same part w C5MMH

+3VS — RPH2 10K_0804_8P4R_5%

LAN_CLKREQ# — VGA_CLKREQ# <25>
WLAN_CLKREQ#
SSD_CLKREQ#

remove TP as C5PRH

UH1G CNP-H CNP-H_BGA874 Rev1.0 7 OF 13

<11> PCH_CPU_24M_CLK_P
<11> PCH_CPU_24M_CLK_N
PCH_CPU_24M_CLK_P — D7
PCH_CPU_24M_CLK_N — C6
CLKOUT_CPUNSSC_P — CLKOUT_ITPXDP# — Y3 — TP@ TH2
CLKOUT_CPUNSSC# — CLKOUT_ITPXDP_P — Y4 — TP@ TH3

<11> PCH_CPU_BCLK_P
<11> PCH_CPU_BCLK_N
PCH_CPU_BCLK_P — B8
PCH_CPU_BCLK_N — C8
CLKOUT_CPUBCLK_P CLKOUT_CPUPCIBCLK# — B6 PCH_CPU_PCIBCLK_N — PCH_CPU_PCIBCLK_N <11>
CLKOUT_CPUBCLK# CLKOUT_CPUPCIBCLK_P — A6 PCH_CPU_PCIBCLK_P — PCH_CPU_PCIBCLK_P <11>

XTAL_24M_PCH_OUT_R — U9
XTAL_24M_PCH_IN_R — U10
XTAL_OUT
XTAL_IN
CLKOUT_PCIE_N0 — AJ6 CLK_PEG_VGA# — CLK_PEG_VGA# <25>
CLKOUT_PCIE_P0 — AJ7 CLK_PEG_VGA — CLK_PEG_VGA <25> — DGPU

RH10 1 2 60.4_0402_1% — XCLK_BIASREF — T3
XCLK_BIASREF (PDG)
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil
8/24
CLKOUT_PCIE_N1 — AH9 CLK_PCIE_LAN# — CLK_PCIE_LAN# <36>
CLKOUT_PCIE_P1 — AH10 CLK_PCIE_LAN — CLK_PCIE_LAN <36> — GLAN

PCH_RTCX1 — BA49
PCH_RTCX2 — BA48
RTCX1
RTCX2
CLKOUT_PCIE_N2 — AE14 CLK_PCIE_WLAN# — CLK_PCIE_WLAN# <37>
CLKOUT_PCIE_P2 — AE15 CLK_PCIE_WLAN — CLK_PCIE_WLAN <37> — NGFF WL+BT(KEY E)

VGA_CLKREQ# — BF31
<36> LAN_CLKREQ# — LAN_CLKREQ# — BE31
<37> WLAN_CLKREQ# — WLAN_CLKREQ# — AR32
<35> SSD_CLKREQ# — SSD_CLKREQ# — BB30
CLKOUT_PCIE_N3 — AE6 CLK_PCIE_NGFF# — CLK_PCIE_NGFF# <35>
CLKOUT_PCIE_P3 — AE7 CLK_PCIE_NGFF — CLK_PCIE_NGFF <35> — M2 SSD

GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4# — BA30
GPP_B10/SRCCLKREQ5# — AN29
GPP_H0/SRCCLKREQ6# — AE47
GPP_H1/SRCCLKREQ7# — AC48
GPP_H2/SRCCLKREQ8# — AE41
GPP_H3/SRCCLKREQ9# — AF48
GPP_H4/SRCCLKREQ10# — AC41
GPP_H5/SRCCLKREQ11# — AC39
GPP_H6/SRCCLKREQ12# — AE39
GPP_H7/SRCCLKREQ13# — AB48
GPP_H8/SRCCLKREQ14# — AC44
GPP_H9/SRCCLKREQ15# — AC43

remove no use srcclkreq

CLKOUT_PCIE_N4 — AC2
CLKOUT_PCIE_P4 — AC3
CLKOUT_PCIE_N5 — AB2
CLKOUT_PCIE_P5 — AB3
CLKOUT_PCIE_N6 — W4
CLKOUT_PCIE_P6 — W3
CLKOUT_PCIE_N7 — W7
CLKOUT_PCIE_P7 — W6
CLKOUT_PCIE_N8 — AC14
CLKOUT_PCIE_P8 — AC15
CLKOUT_PCIE_N9 — U2
CLKOUT_PCIE_P9 — U3
CLKOUT_PCIE_N10 — AC9
CLKOUT_PCIE_P10 — AC11
CLKOUT_PCIE_N11 — AE9
CLKOUT_PCIE_P11 — AE11
CLKOUT_PCIE_N12 — AC7
CLKOUT_PCIE_P12 — AC6
CLKOUT_PCIE_N15 — V2
CLKOUT_PCIE_P15 — V3
CLKOUT_PCIE_N14 — T2
CLKOUT_PCIE_P14 — T1
CLKOUT_PCIE_N13 — AA1
CLKOUT_PCIE_P13 — Y2

CLKIN_XTAL — R6 — REFCLK_CNV — REFCLK_CNV <37>
RH14 10K_0402_5%

remove SD signal from PCH

UH1M CNP-H CNP-H_BGA874 Rev1.0 13 OF 13

GPP_G0/SD_CMD — AW13
GPP_G1/SD_DATA0 — BE9
GPP_G2/SD_DATA1 — BF8
GPP_G3/SD_DATA2 — BF9
GPP_G4/SD_DATA3 — BG8
GPP_G5/SD_CD# — BE8
GPP_G6/SD_CLK — BD8
GPP_G7/SD_WP — AV13

GPP_I11/M2_SKT2_CFG0 — AP3
GPP_I12/M2_SKT2_CFG1 — AP2
GPP_I13/M2_SKT2_CFG2 — AN4
GPP_I14/M2_SKT2_CFG3 — AM7
3.3V
1.8V

remove CPU_C10_GATE#

GPP_J0/CNV_PA_BLANKING — AV6
GPP_J1/CPU_C10_GATE# — AY3
GPP_J11/A4WP_PRESENT — AR13
GPP_J10 — AV7
GPP_J_2 — AW3
GPP_J_3 — AT10
GPP_J4/CNV_BRI_DT/UART0B_RTS# — AV4
GPP_J5/CNV_BRI_RSP/UART0B_RXD — AY2
GPP_J6/CNV_RGI_DT/UART0B_TXD — BA4
GPP_J7/CNV_RGI_RSP/UART0B_CTS# — AV3
GPP_J8/CNV_MFUART2_RXD — AW2
GPP_J9/CNV_MFUART2_TXD — AU9

<37> CNV_BRI_PTX_DRX — CNV_BRI_PTX_DRX
<37> CNV_BRI_PRX_DTX — CNV_BRI_PRX_DTX
<37> CNV_RGI_PTX_DRX — CNV_RGI_PTX_DRX
<37> CNV_RGI_PRX_DTX — CNV_RGI_PRX_DTX
GPP_J9

CNV_WR_CLKN — BD4 CLK_CNV_PRX_DTX_N — CLK_CNV_PRX_DTX_N <37>
CNV_WR_CLKP — BE3 CLK_CNV_PRX_DTX_P — CLK_CNV_PRX_DTX_P <37>
CNV_WR_D0N — BB3 CNV_PRX_DTX_N0 — CNV_PRX_DTX_N0 <37>
CNV_WR_D0P — BB4 CNV_PRX_DTX_P0 — CNV_PRX_DTX_P0 <37>
CNV_WR_D1N — BA3 CNV_PRX_DTX_N1 — CNV_PRX_DTX_N1 <37>
CNV_WR_D1P — BA2 CNV_PRX_DTX_P1 — CNV_PRX_DTX_P1 <37>
CNV_WT_CLKN — BC5 CLK_CNV_PTX_DRX_N — CLK_CNV_PTX_DRX_N <37>
CNV_WT_CLKP — BB6 CLK_CNV_PTX_DRX_P — CLK_CNV_PTX_DRX_P <37>
CNV_WT_D0N — BE6 CNV_PTX_DRX_N0 — CNV_PTX_DRX_N0 <37>
CNV_WT_D0P — BD7 CNV_PTX_DRX_P0 — CNV_PTX_DRX_P0 <37>
CNV_WT_D1N — BG6 CNV_PTX_DRX_N1 — CNV_PTX_DRX_N1 <37>
CNV_WT_D1P — BF6 CNV_PTX_DRX_P1 — CNV_PTX_DRX_P1 <37>
CNV_WT_RCOMP — BA1 CNV_WT_RCOMP — RH16 1 2 150_0402_1%
PCIE_RCOMPN — B12 PCIE_RCOMPN — RH17 1 2 100_0402_1%
PCIE_RCOMPP — A13 PCIE_RCOMPP
SD_RCOMP_1P8 — BE5 SD_RCOMP_1P8 — RH18 1 2 200_0402_1%
SD_RCOMP_3P3 — BE4 SD_RCOMP_3P3 — RH19 1 2 200_0402_1%
SD_1P8_RCOMP — BD1
SD_3P3_RCOMP — BE1
GPPJ_RCOMP_1P81 — BE2 GPPJ_RCOMP_1P8 — RH20 1 2 200_0402_1%
GPPJ_RCOMP_1P82
GPPJ_RCOMP_1P83
RSVD2 — Y35
RSVD3 — Y36
RSVD1 — BC1
TP — AL35 — TP@ TH4
#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

checked CRB

+1.8VALW_PRIM — RH1811 CNVI@ 20K_0402_1% — CNV_BRI_PRX_DTX
RH1821 CNVI@ 20K_0402_1% — CNV_RGI_PRX_DTX

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

For DDX03 R02

XTAL Frequency Select

+1.8VALW_PRIM — RH15 1 2 4.7K_0402_5% — CNV_BRI_PTX_DRX — STRAP

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

VCCPSPI Select

+1.8VALW_PRIM — RH21 1 @ 2 4.7K_0402_5% — GPP_J9 — STRAP

The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

M.2 CNV Mode Select

+1.8VALW_PRIM — RH22 2 1 10K_0402_5% — CNV_RGI_PTX_DRX — STRAP
RH23 2 @ 1 10K_0402_5%

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

Pulled down by CRF CNVi RGI_DT pin

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI/SD

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

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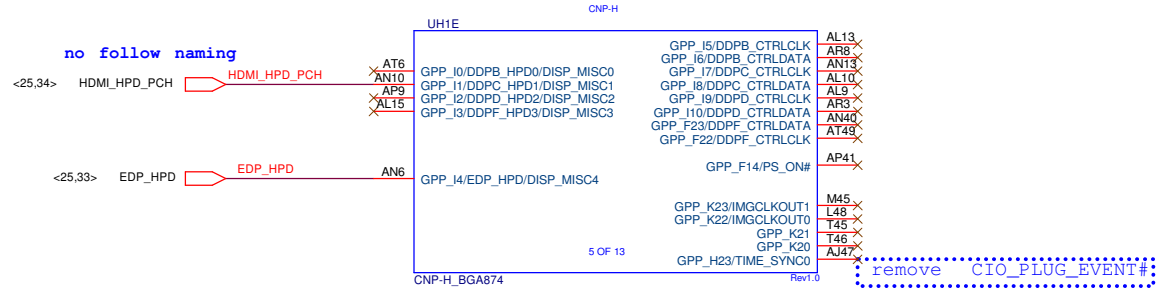
no follow naming

can remove if no use DP
08/18

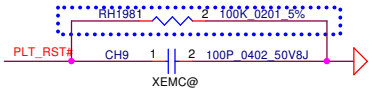
remove PCH DP SCLK/SDATA

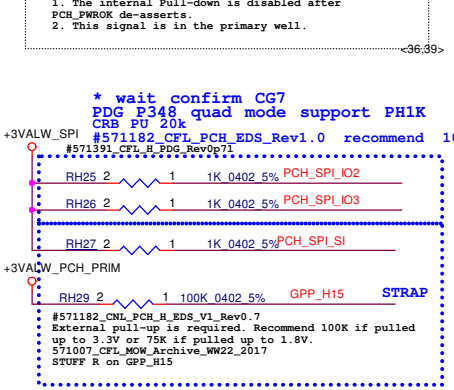
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.



remove CIO_PLUG_EVENT#

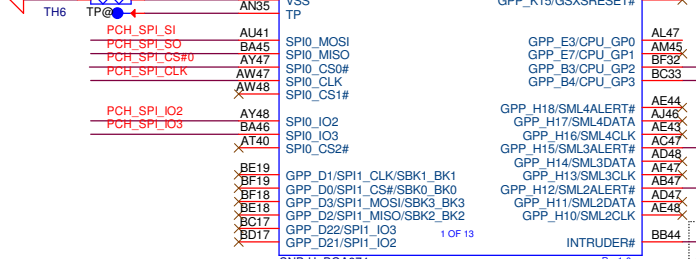
intel critical net recommend



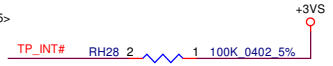


intel critical net recommend

CRB connect GND

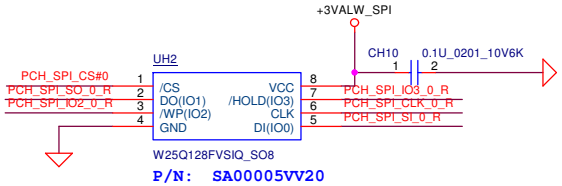


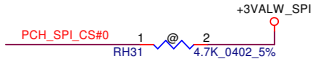
GPIO Serial Expander (GSX) is the capability provided by the PCH to expand the GPIOs on a platform that needs more GPIOs than the ones provided by the PCH.

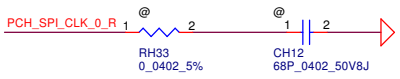


RVP: 330K
A 1 M pull-up is used on the customer reference board (CRB). This is needed to reduce leakage from Coin Cell Battery in G3 state.

SPI ROM (16MByte)

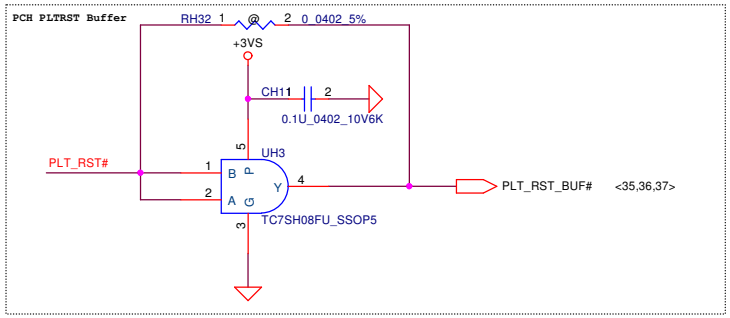






sch checklist 0.7
1 device 15 ohm / 2 device 33 ohm

note : 1050 Use 8M rom



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PCH(3/8)DDC/SPI

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

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#571391_CFL_H_PDG_Rev0p5
• eSPI clock and eSPI data mismatched: <500 mils.
• eSPI clock and eSPI chip select mismatched: <500 mils.
• eSPI signal maximum 9 Vias
* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.

USB3 MB
USB3 Type C
USB3 SUB
USB3 Type C
USB3 SUB
LPC Bus
check straps
LPC : +3.3V
1A modify
M.2 SSD PCIE L3
M.2 SSD PCIE L2
NGFF
WL+BT(KEY E)
M.2 SSD PCIE L1
HDD
GLAN
M.2 SSD PCIE L0
M.2 SSD PCIE/SATA select pin
For Intel CLINK

	GPP_F13 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

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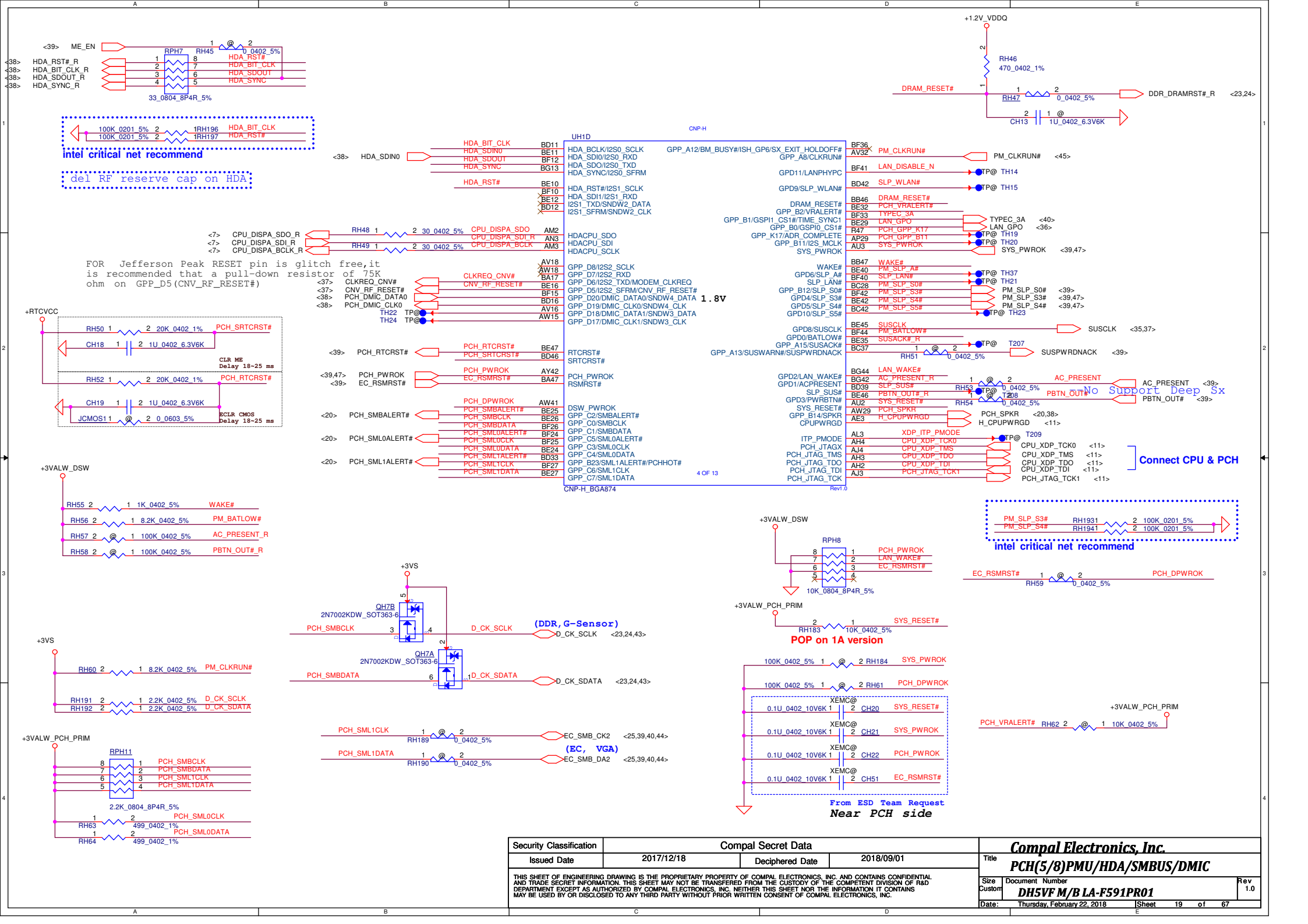

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: PCH(5/8)PMU/HDA/SMBUS/DMIC

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

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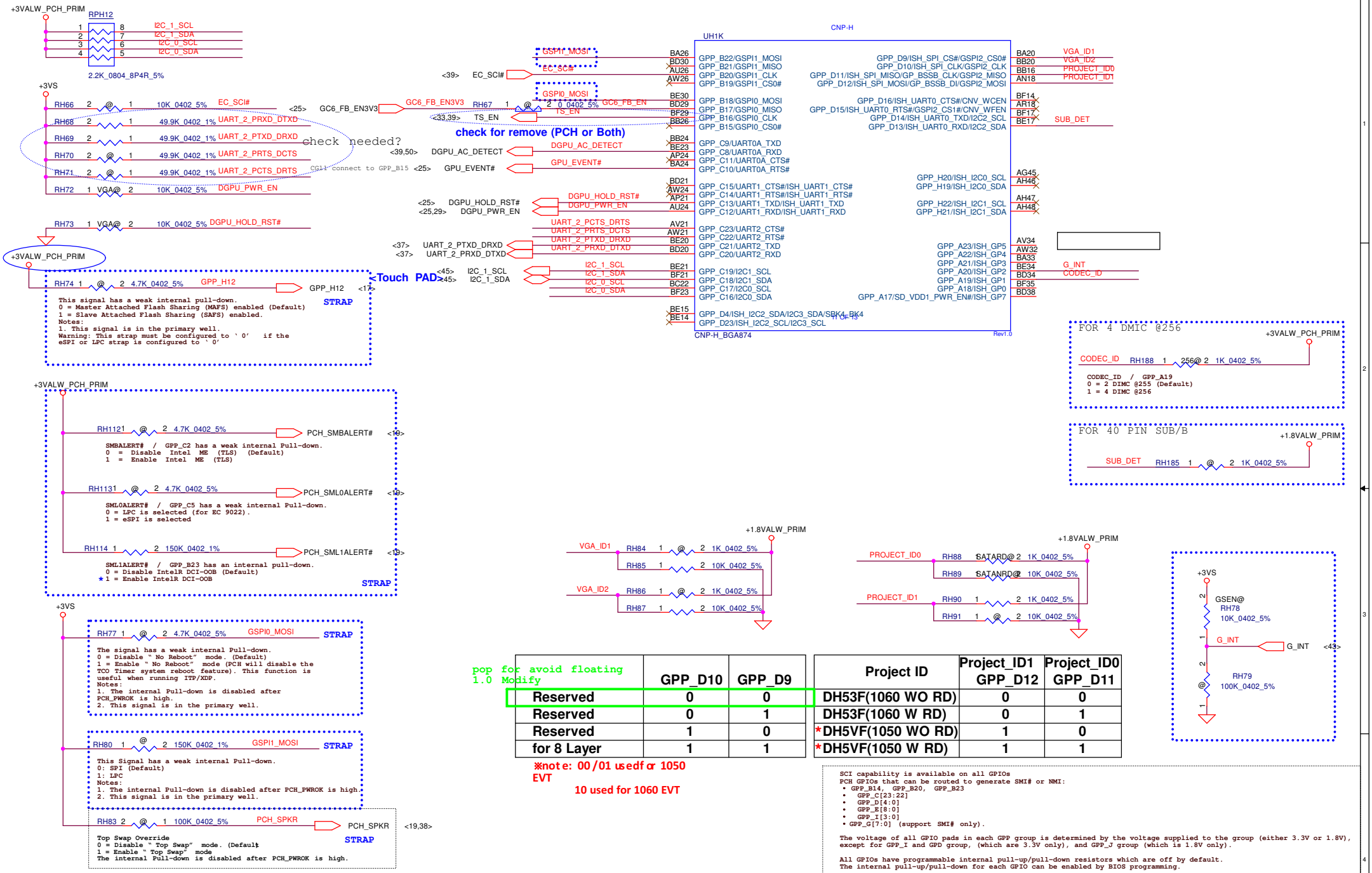

pop for avoid floating
1.0 Modify

GPP_D10	GPP_D9
Reserved	0	0
Reserved	0	1
Reserved	1	0
for 8 Layer	1	1

※note: 00/01 usedfor 1050 EVT
10 used for 1060 EVT

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
DH53F(1060 WO RD)	0	0
DH53F(1060 W RD)	0	1
*DH5VF(1050 WO RD)	1	0
*DH5VF(1050 W RD)	1	1

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0]
- GPP_I[3:0]
- GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPD group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

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GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V * 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

3-5MM FROM PACKAGE EDGE

pop for intel sensitive net (1.0)

place near VCCDUSB FOR W22/W23

1-3MM FROM PACKAGE VCCPRIM_MPHY W31

1-3MM FROM PACKAGE EDGE

pop for intel sensitive net (1.0)

1-5MM FROM PACKAGE EDGE FOR VCCAPLL C1/C2

1-3MM FROM PACKAGE EDGE FOR VCCA_BCLK V19

1-5MM FROM PACKAGE EDGE FOR VCCAPLL B1/B2/B3

1-3MM FROM PACKAGE EDGE

LC filter colse to pin

1uF 1-3MM FROM PACKAGE EDGE

change to 10k

reserve filter folloe CRB 8/21

change to 0_0603 (1.0)

1-3MM FROM PACKAGE FOR PGPPEF AE35/AE37

1-3MM FROM PACKAGE FOR PGPPHK AC35/AC36

1-3MM FROM PACKAGE FOR VCCPRIM AY8/BB7

reserve for cnd issue (1.0)

near AG19/AG20

CONN@ SP02000RO00

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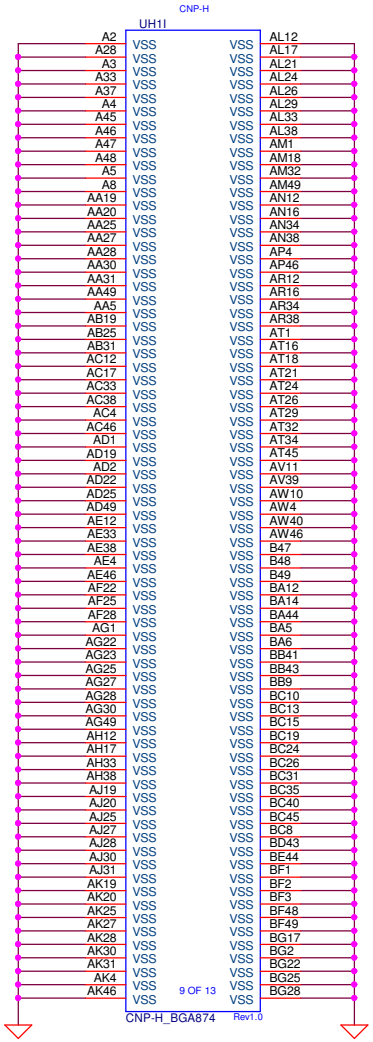
Issued Date	2017/12/18	Deciphered Date	2018/09/01

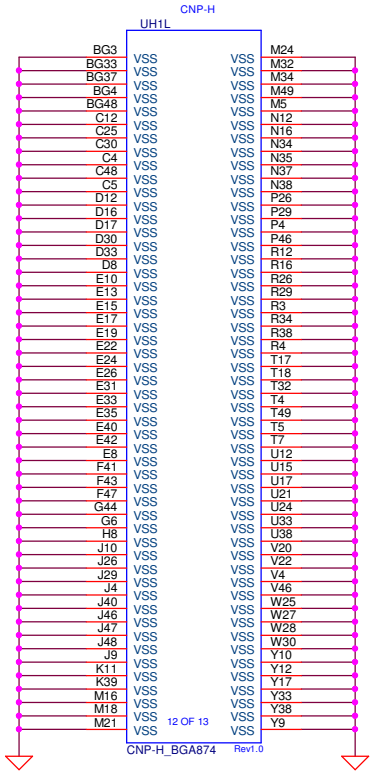
Compal Electronics, Inc.

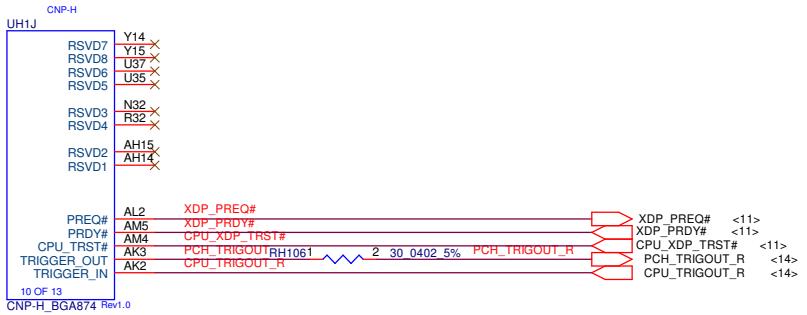
Title: PCH(7/8)Power

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 21 of 67







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Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

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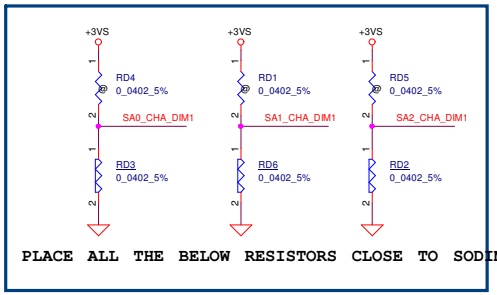
CHANNEL-A

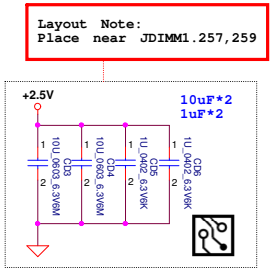
BOT REVERSE TYPE (4 mm)

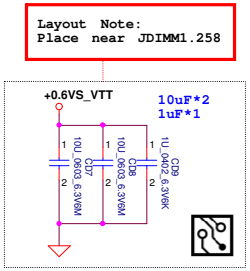
Interleaved Memory

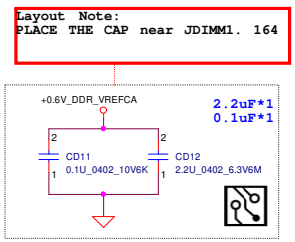
TOP: JDIMM1 CONN Non-ECC DIMM

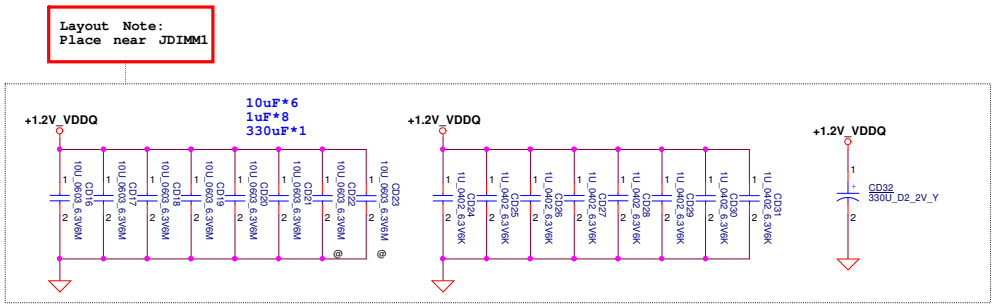


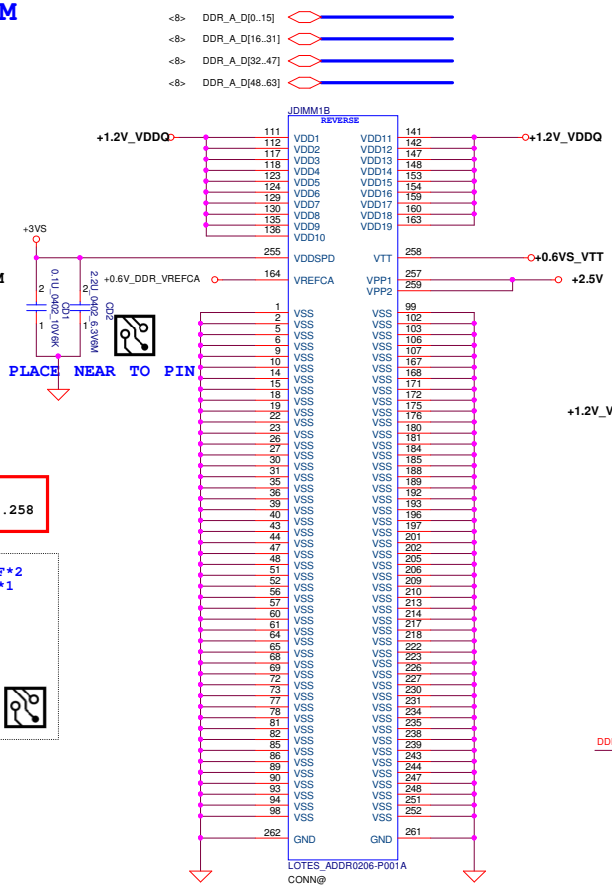
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

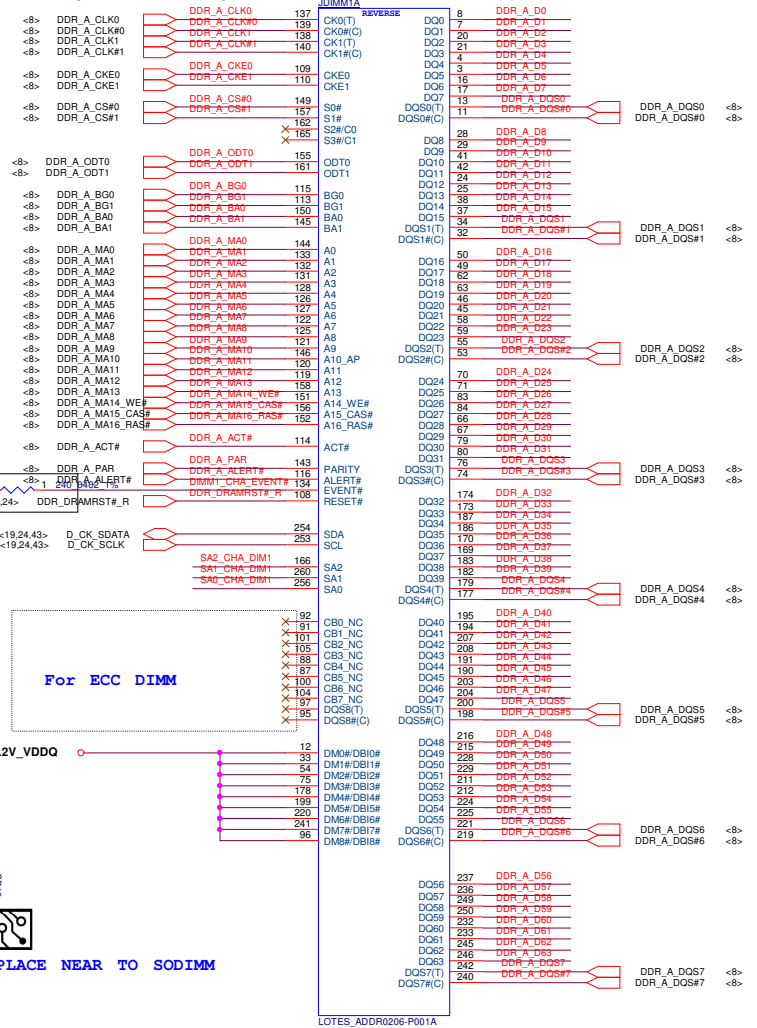




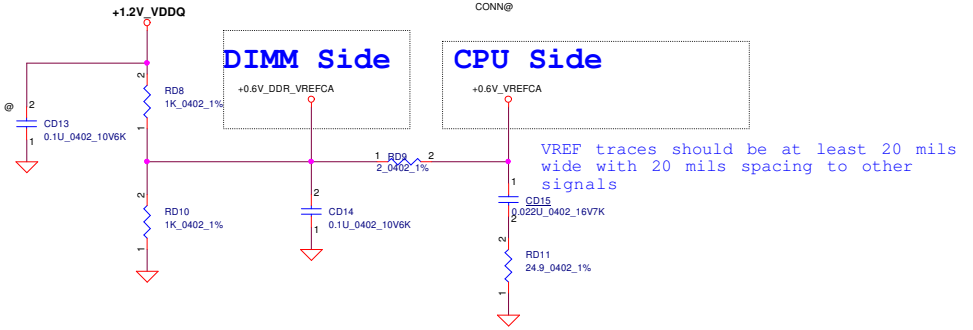








Part Number:SP07001FYH0
Part Value:S SOCKET FOX_AS0A826-H4RB-7H 260P DDR4



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Compal Electronics, Inc.

Title: **DDRIV_CHA: DIMM0**

Size	Document Number	Rev
	DH5VF M/B LA-F591PR01	1.0

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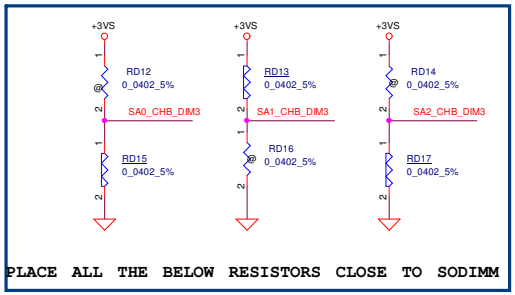
CHANNEL-B

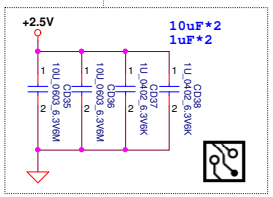
TOP: JDIMM3 CONN Non-ECC DIMM



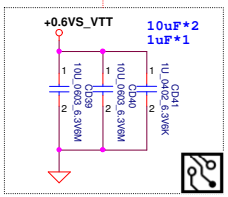
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

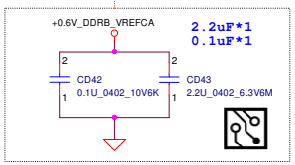
Layout Note:
Place near JDIMM3.257,259



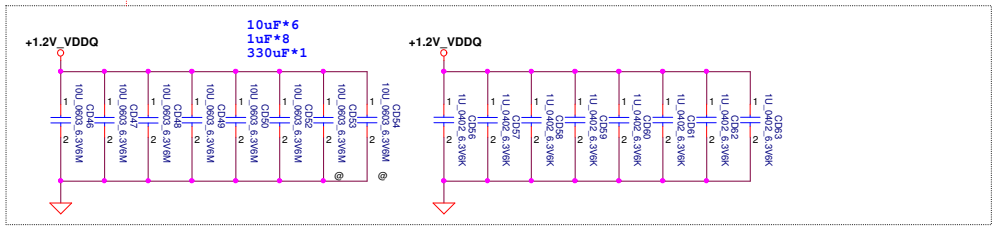
Layout Note:
Place near JDIMM3.258



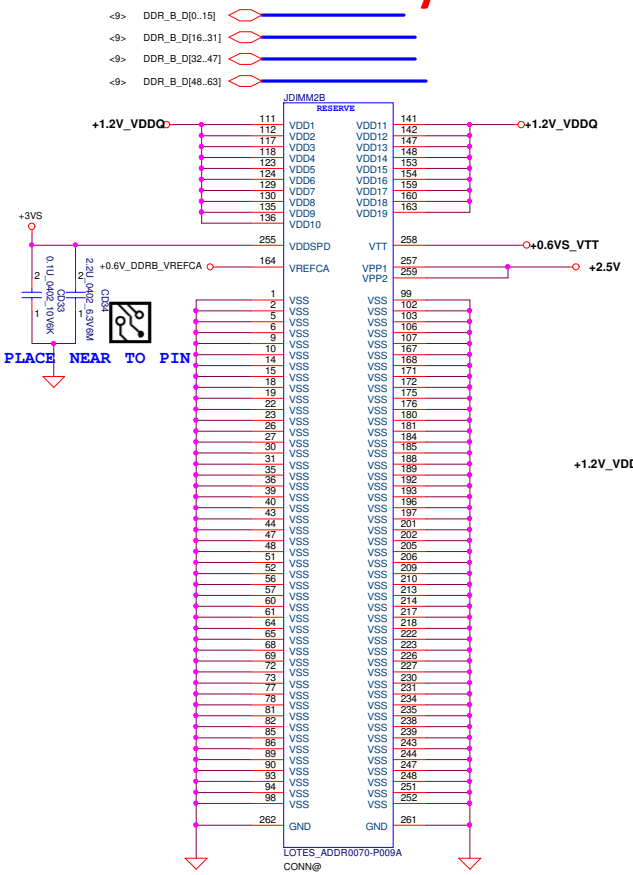
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3



Layout Note:
Place near JDIMM3

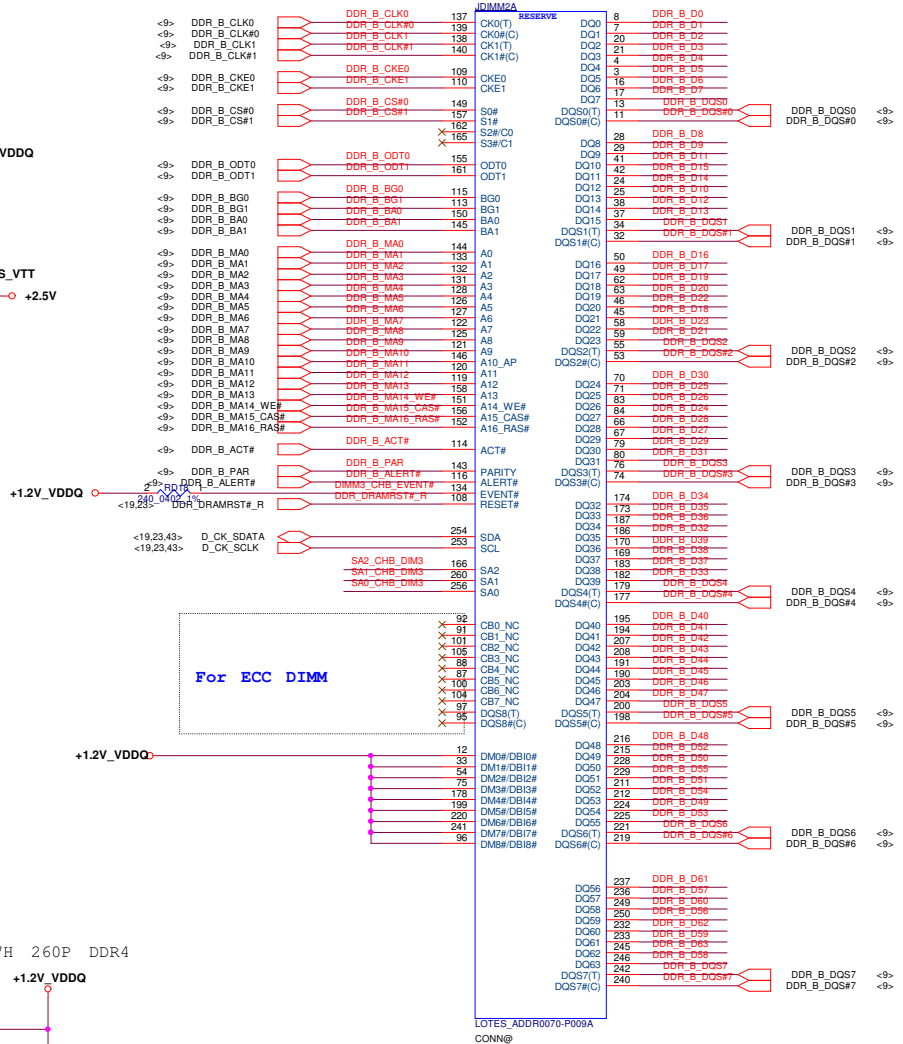


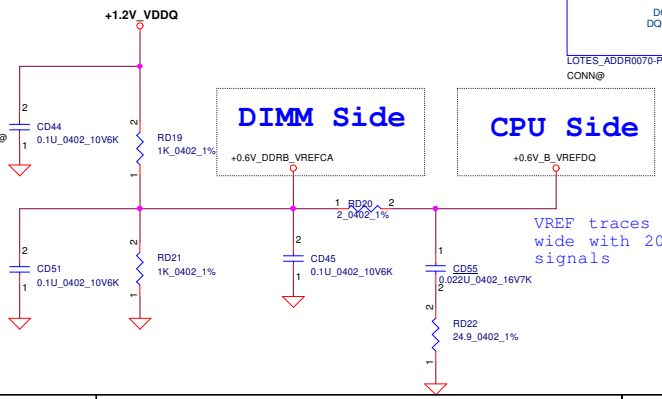
Interleaved Memory



Part Number:SP07001CEA0
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4

BOT STD (4 mm)





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size	Document Number	Rev
	DH5VF M/B LA-F591PR01	1.0

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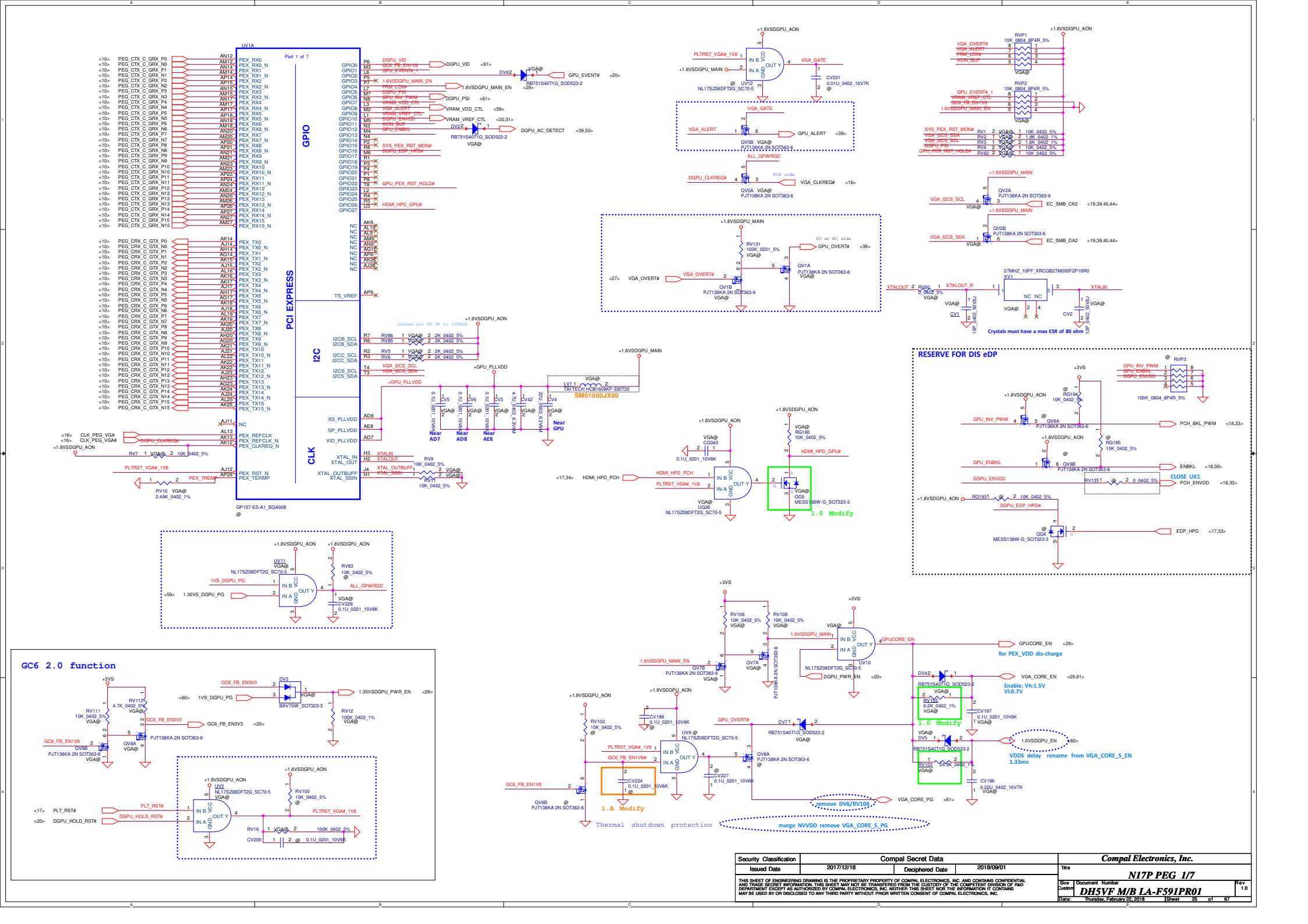

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Compal Electronics, Inc.			
Title: N17P PEG 1/7			
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
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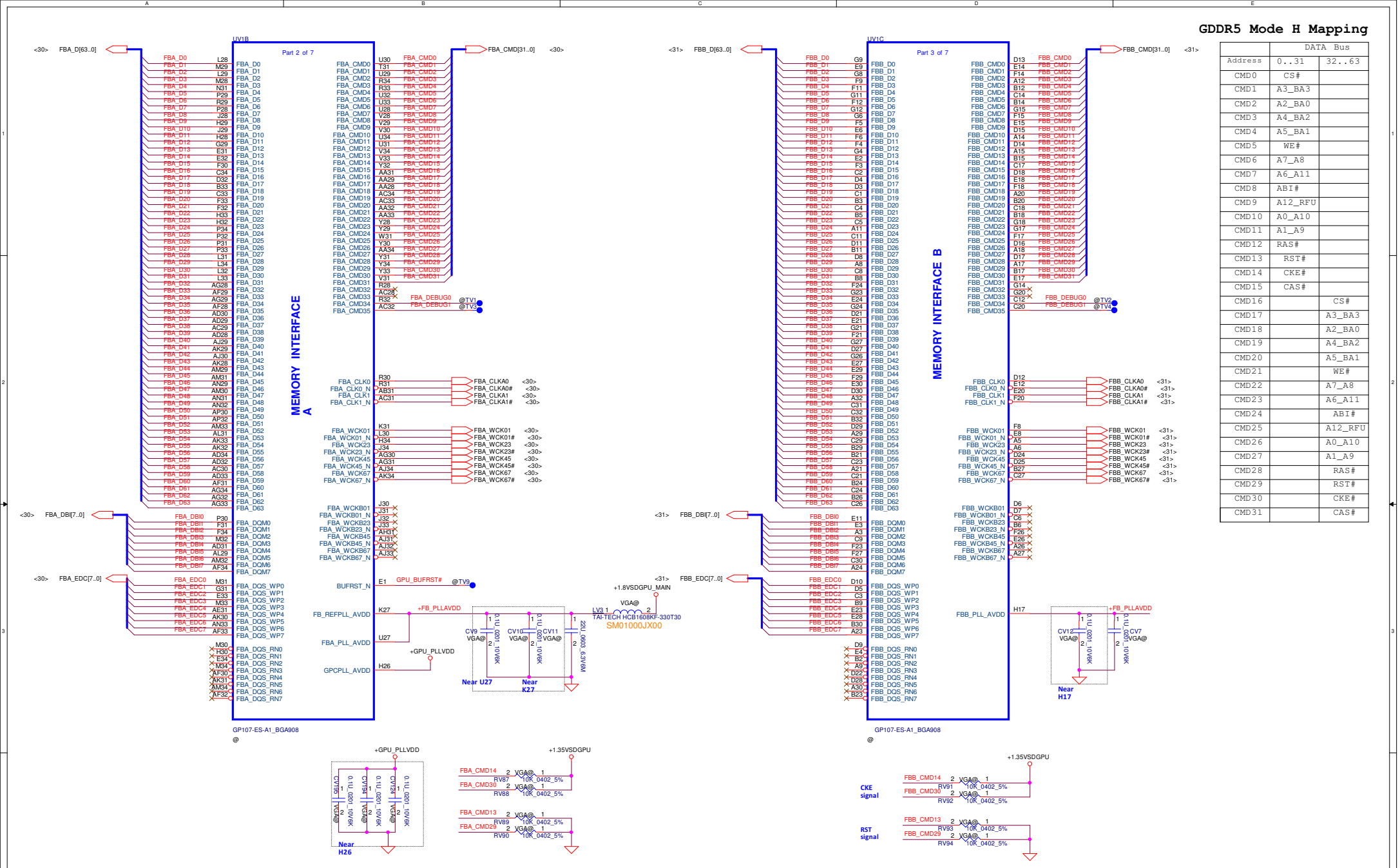

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

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Compal Electronics, Inc.

Title: **N17P VRAM 2/7**

Size: Custom | Document Number: **DH5VF M/B LA-F591PR01** | Rev: 1.0

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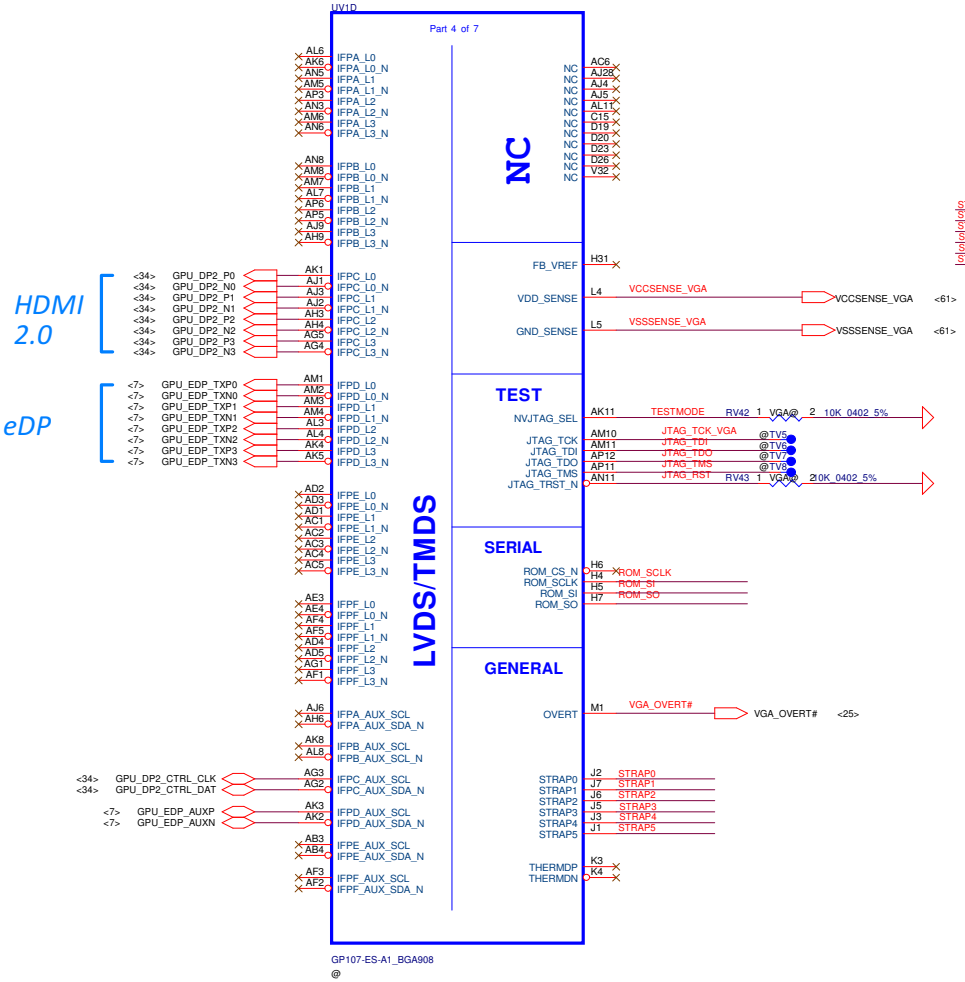

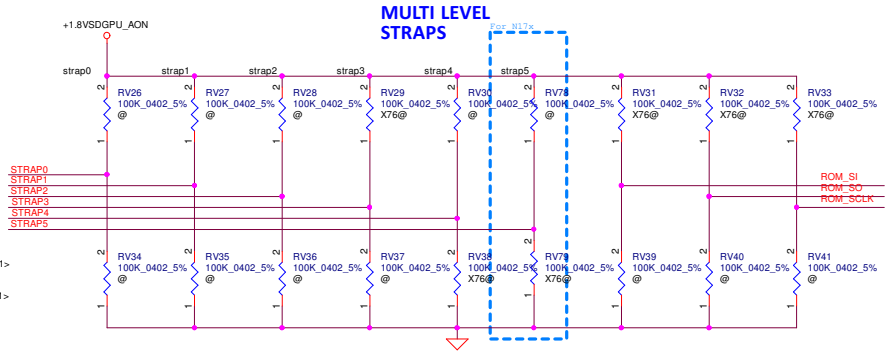

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325F3-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325F3-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

HDMI audio output

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Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title	N17P STRAP 3/7		
Size	Document Number		Rev
Custom	DH5VF M/B LA-F591PR01		1.0
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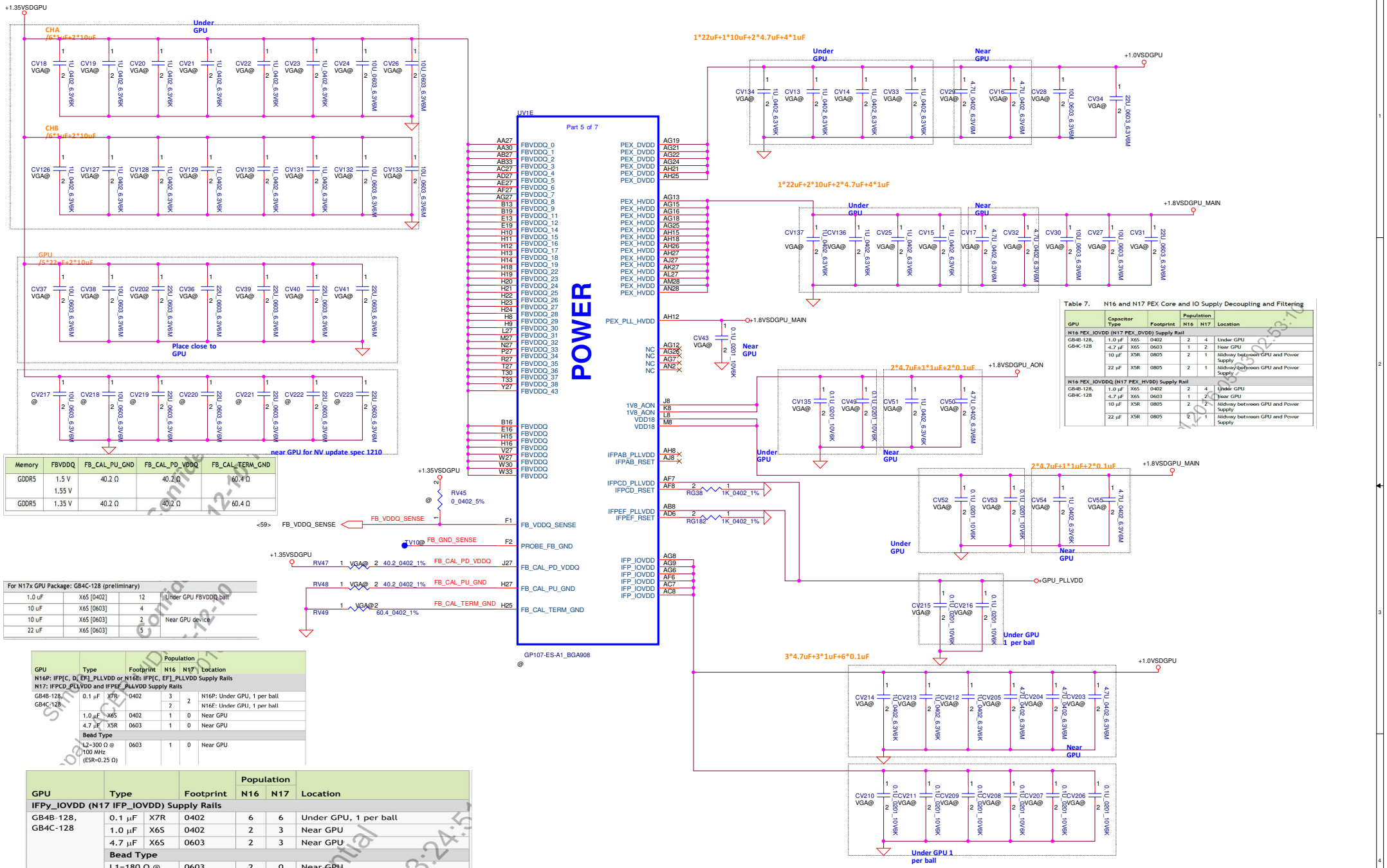

Table 7. N16 and N17 PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S 0402	2	4	Under GPU
	4.7 µF	X6S 0603	1	2	Near GPU
	10 µF	X5R 0805	2	1	Midway between GPU and Power Supply
	22 µF	X5R 0805	2	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S 0402	2	4	Under GPU
	4.7 µF	X6S 0603	1	2	Near GPU
	10 µF	X5R 0805	2	2	Midway between GPU and Power Supply
	22 µF	X5R 0805	2	1	Midway between GPU and Power Supply

Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDDR5	1.5 V 1.55 V	40.2 Ω	40.2 Ω	60.4 Ω
GDDR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω

For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	

GPU	Type	Footprint	Population N16	Population N17	Location
N16P: IFP[C, D, EF]_PLLVDD or N16E: IFP[C, EF]_PLLVDD Supply Rails N17: IFPCD_PLLVDD and IFPEF_PLLVDD Supply Rails					
GB4B-128, GB4C-128	0.1 µF X7R	0402	3	2	N16P: Under GPU, 1 per ball
			2		N16E: Under GPU, 1 per ball
	1.0 µF X6S	0402	1	0	Near GPU
	4.7 µF X5R	0603	1	0	Near GPU
	Bead Type				
	L2=300 Ω @ 100 MHz (ESR=0.25 Ω)	0603	1	0	Near GPU

GPU	Type	Footprint	Population N16	Population N17	Location
IFPy_IOVDD (N17 IFP_IOVDD) Supply Rails					
GB4B-128, GB4C-128	0.1 µF X7R	0402	6	6	Under GPU, 1 per ball
	1.0 µF X6S	0402	2	3	Near GPU
	4.7 µF X6S	0603	2	3	Near GPU
	Bead Type				
	L1=180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	2	0	Near GPU

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Issued Date	2017/12/18	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title: N17P POWER 4/7

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 28 of 67

N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2

UV1G
Part 7 of 7
POWER
GP107-ES-A1_BGA908
@

+VGA_CORE
VDD_1 VDD_4 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_14 VDD_15 VDD_17 VDD_18 VDD_20 VDD_21 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_31 VDD_34 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41 VDD_42 VDD_44 VDD_45 VDD_47 VDD_48 VDD_49 VDD_51 VDD_52 VDD_53 VDD_54 VDD_55 VDD_56 VDD_58 VDD_59 VDD_60 VDD_62 VDD_63 VDD_65 VDD_66 VDD_67 VDD_68 VDD_69 VDD_70 VDD_71

VDDS_SENSE
GNDS_SENSE
U1
U2
NVVDD & NVVDDS merge
confirm NV nc or not

XVDD

+1.35VSDGPU
+5VS
RV115 100K_0402_5% VGA@
VGA@ RV116 20_0402_5%
+1.35VSDGPU_R
1.35VSDGPU_PWR_EN#
<25,59> 1.35VSDGPU_PWR_EN
QV11B 2N7002KDW_SOT363-6 VGA@
QV11A 2N7002KDW_SOT363-6 VGA@

+VGA_CORE
+5VS
RV117 100K_0402_5% VGA@
VGA@ RV118 20_0402_5%
+VGA_CORE_R
NVVDD_EN#
<25,61> VGA_CORE_EN
QV10B 2N7002KDW_SOT363-6 VGA@
QV10A 2N7002KDW_SOT363-6 VGA@

UV1F
Part 6 of 7
GND
GP107-ES-A1_BGA908
@

GND_0 GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99
GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140 GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169 GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198 GND_199 GND_OPT GND_OPT

+1.8V_AON/+1.8V_MAIN

DV2
+1.8VALW
1V8_AON_EN
+1.8VSDGPU_AON
RG1791 10K_0402_5%
<25> 1.8VSDGPU_MAIN_EN
+5VALW
CG337 0.1U_0201_10V6K VGA@
UG27
VIN1 VIN1 ON1 VBIAS ON2 VIN2 VIN2
VOUT1 VOUT1 CT1 GND CT2 VOUT2 VOUT2 GPAD
EM5209VF_DFN14_2X3 VGA@
CG335 220P_0402_50V8J
CG336 220P_0402_50V8J
+1.8VSDGPU_MAIN
CG334 10U_0603_6.3V6M
CG338 10U_0603_6.3V6M
CG339 22U_0603_6.3V6M

+1.0VSDGPU
+5VS
VGA@ R214 100K_0402_5%
VGA@ R39 20_0402_5%
GPUCORE_EN#
Q17A VGA@ 2N7002KDW_SOT363-6
<25> GPUCORE_EN
Q17B 2N7002KDW_SOT363-6 VGA@

remove NVDDS discharge

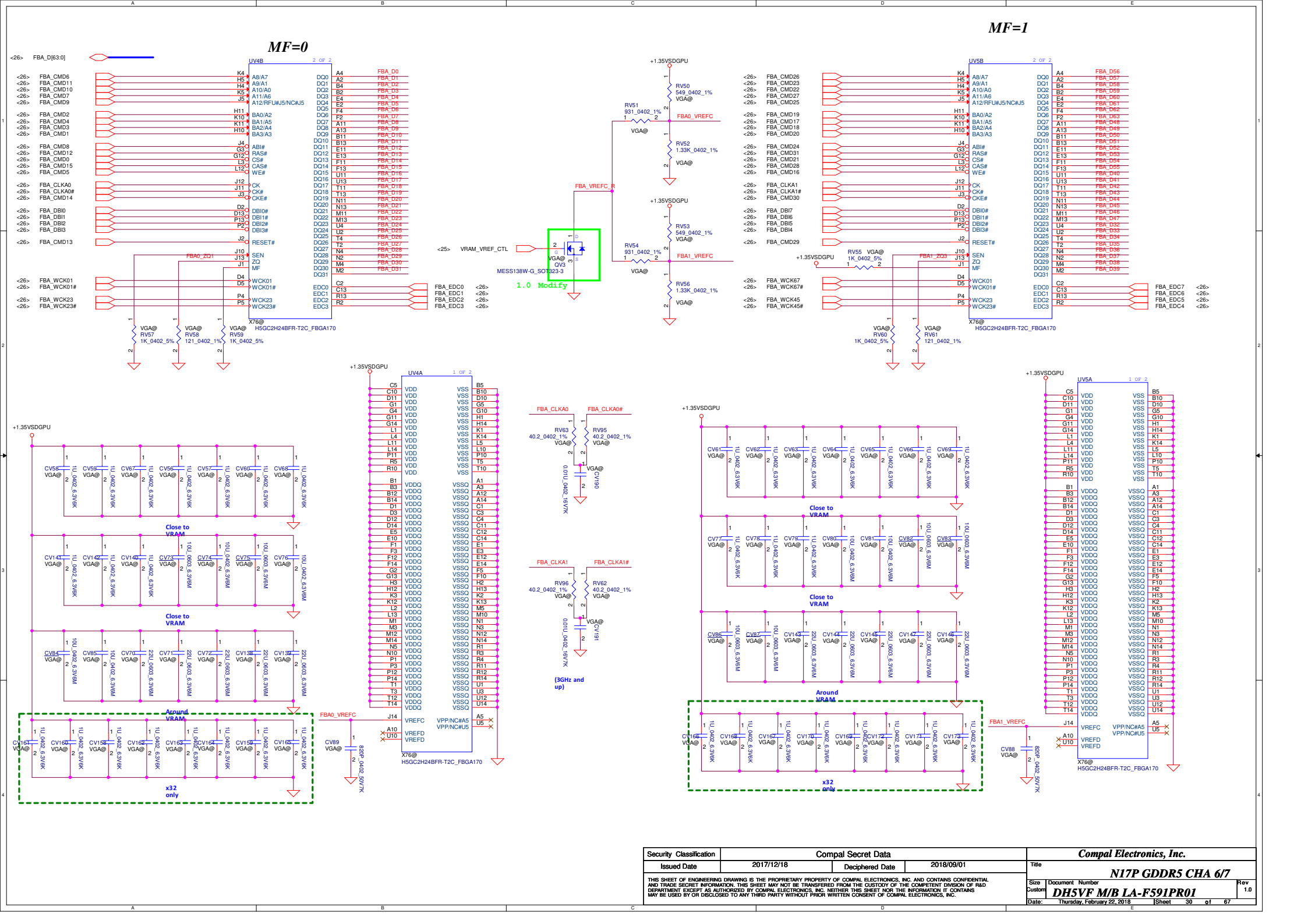
For Power down sequence

<20> DGPU_PWR_EN
DV1 RB751S40T1G_SOD523-2 VGA@
1V8_AON_EN
RY22 49.9K_0402_5% VGA@
CV35 0.1U_0201_10V6K VGA@

1.0 Modify

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.
Title: N17P POWER & GND 5/7
Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0
Date: Thursday, February 22, 2018 | Sheet 29 of 67



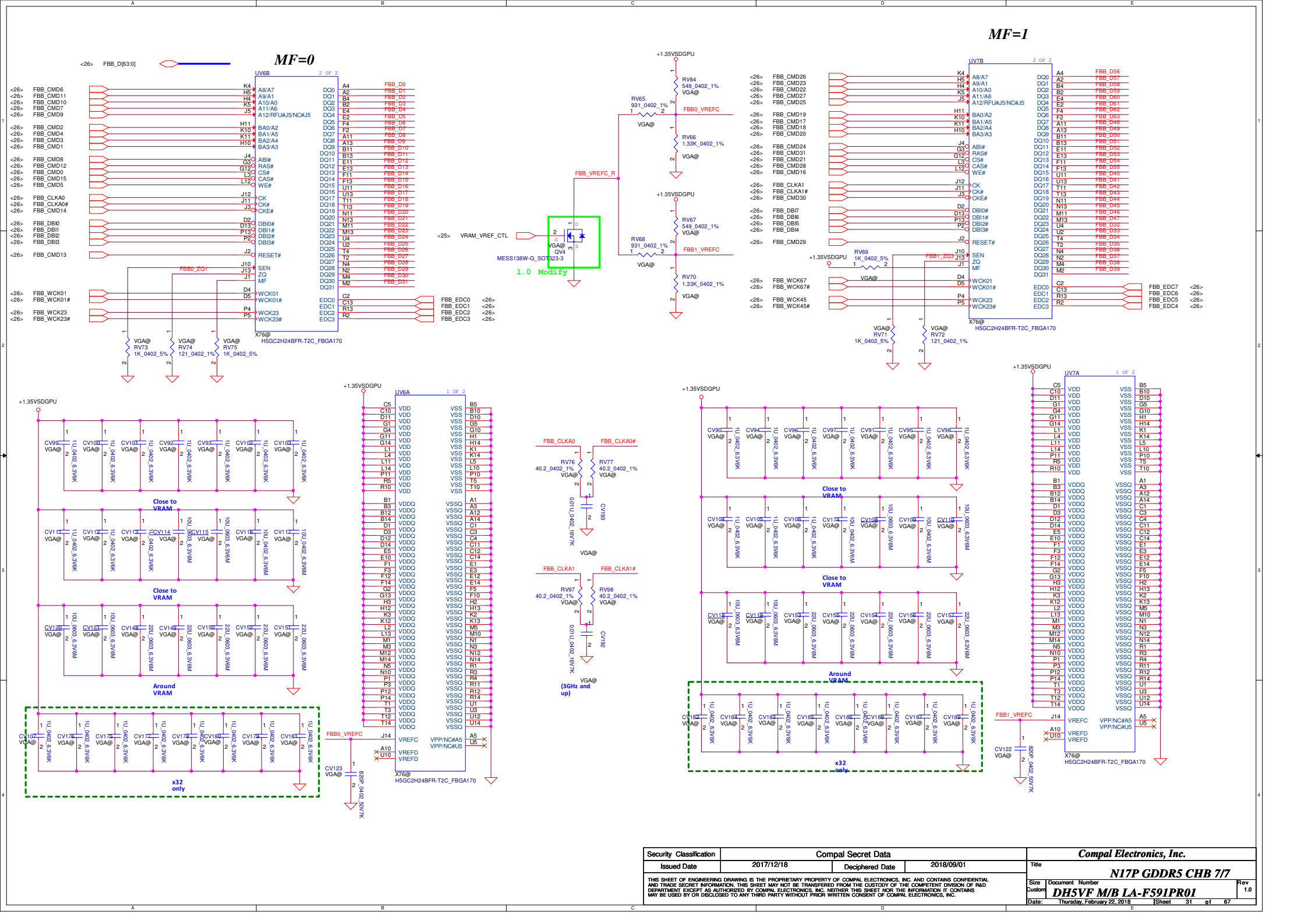
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: **N17P GDDR5 CHA 6/7**

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

Date: Thursday, February 22, 2018 | Sheet 30 of 67


MF=0
MF=1
UV6B
UV7B
UV6A
UV7A
X76@ H5GC2H24BFR-T2C_FBGA170
MESS138W-G_SOT323-3
1.0 Modify
Close to VRAM
Around VRAM
x32 only
(3GHz and up)
Security Classification
Compal Secret Data
Issued Date
2017/12/18
Deciphered Date
2018/09/01
Compal Electronics, Inc.
N17P GDDR5 CHB 7/7
DH5VF M/B LA-F591PR01
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remove GPAK circuit for improve HDMI layout (1.0)

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: **N17P G-Pak sequence 8/8**

Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

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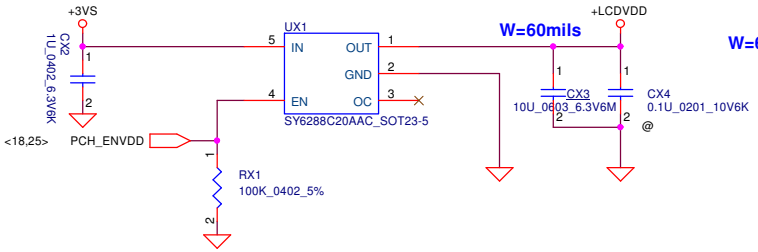
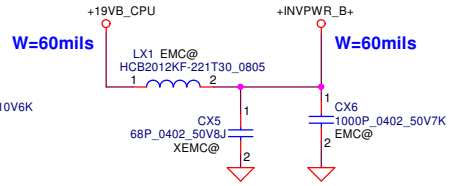
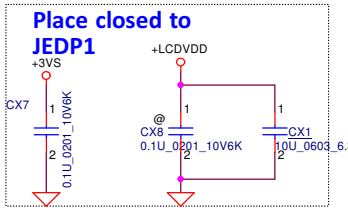
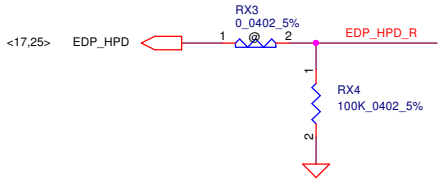
LCD POWER CIRCUIT

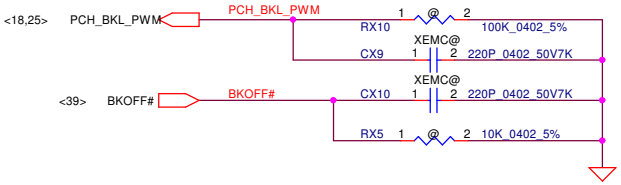


SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04

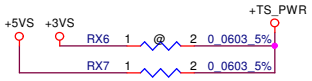




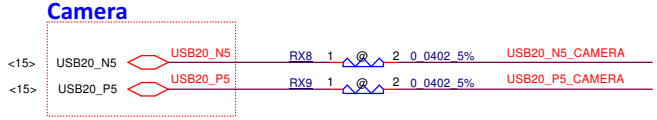


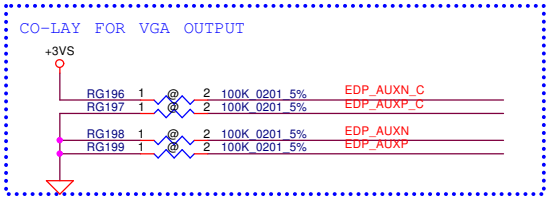


USB Touch Screen

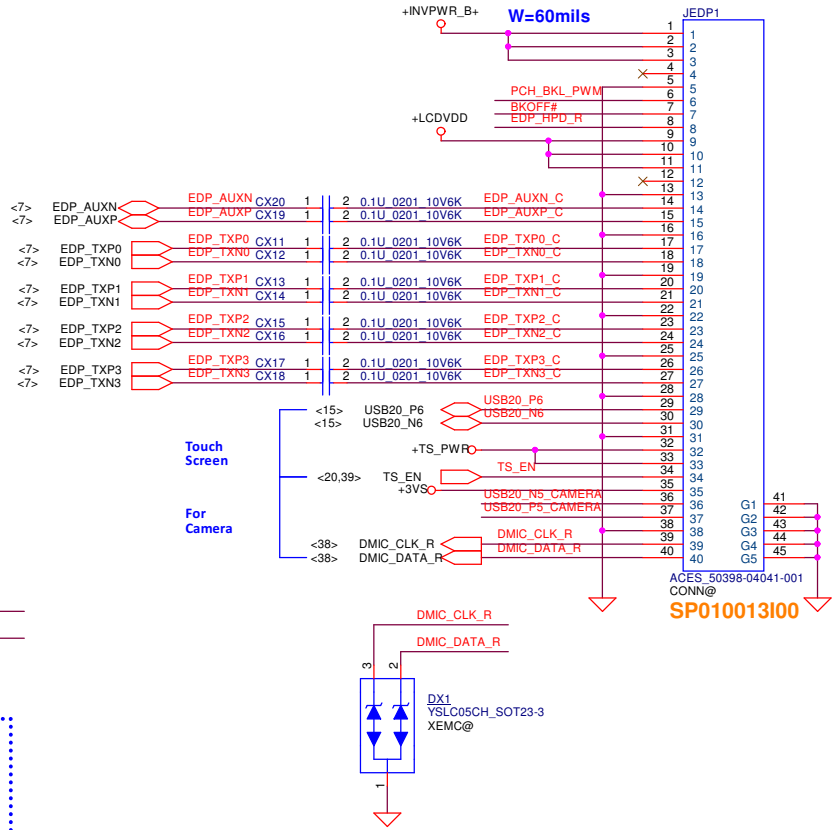


Camera





LED PANEL Conn.



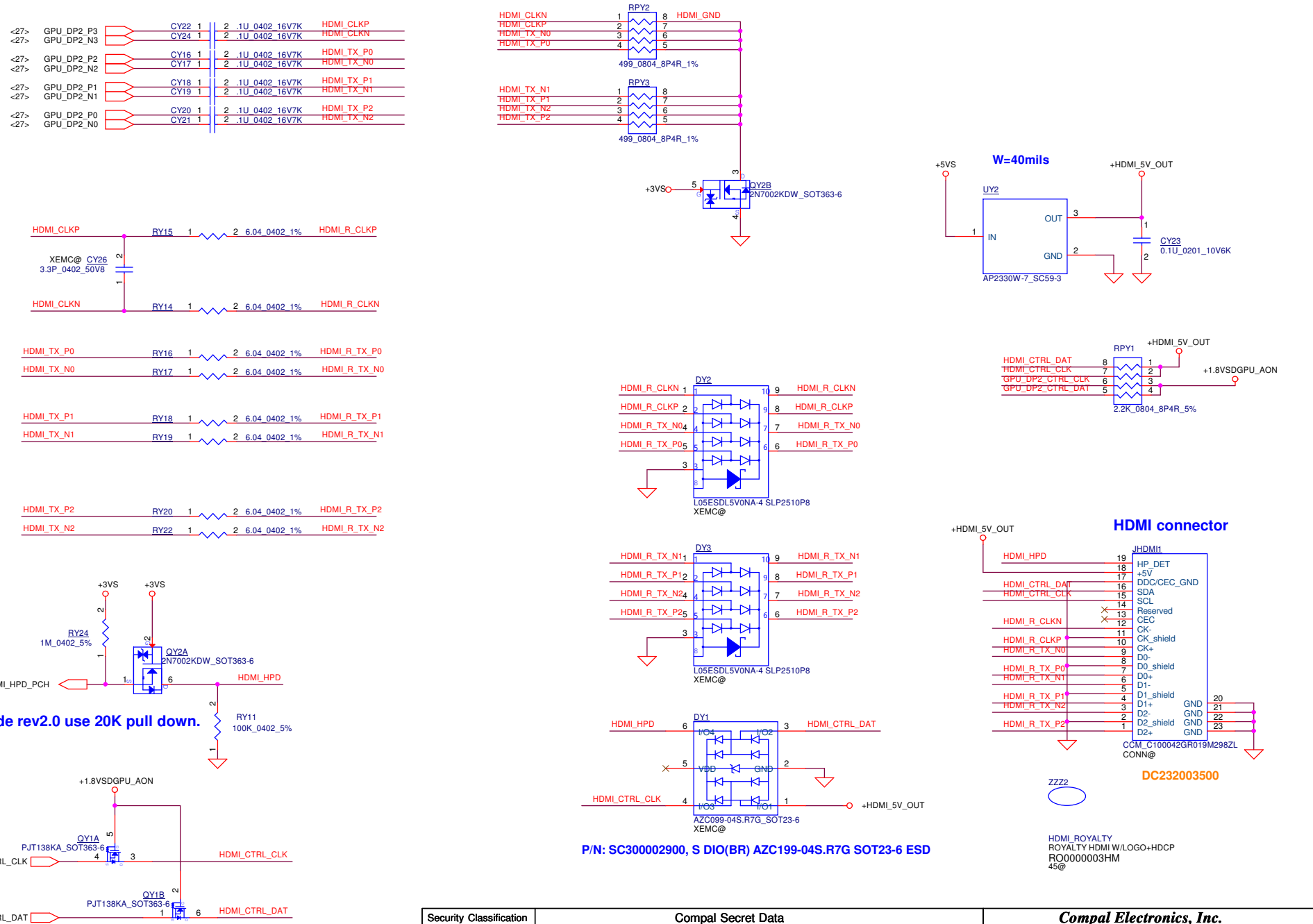
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: eDP CONN.

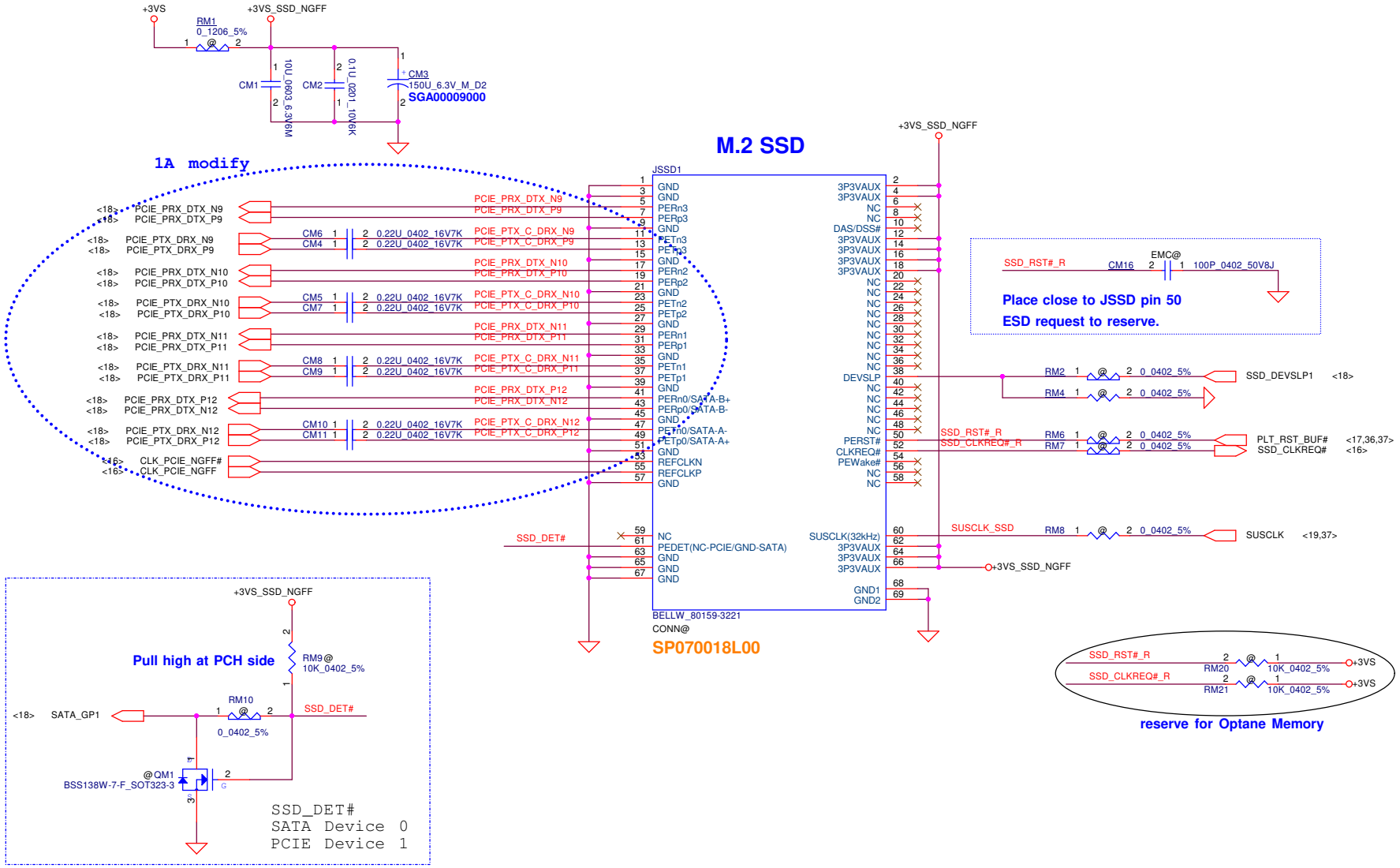
Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

Date: Thursday, February 22, 2018 Sheet 33 of 67



Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title	HDMI CONN.		
Size	Document Number		Rev
Custom	DH5VF M/B LA-F591PR01		1.0
Date:	Thursday, February 22, 2018	Sheet	34 of 67



Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

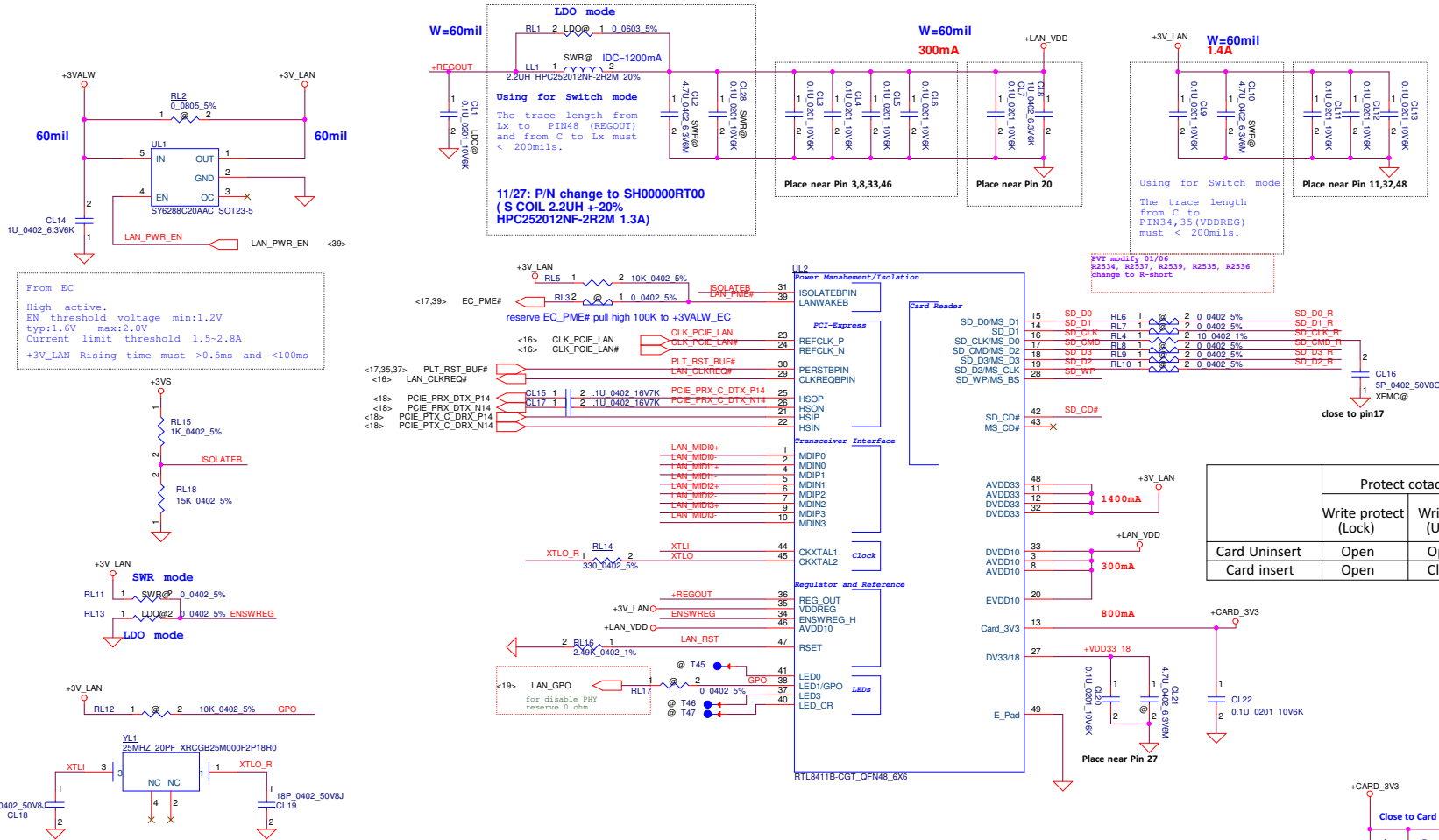
Compal Electronics, Inc.

Title: mSATA-SSD

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 35 of 67

LAN-RTL8411B

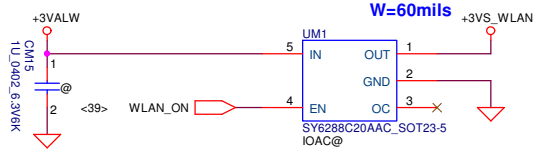


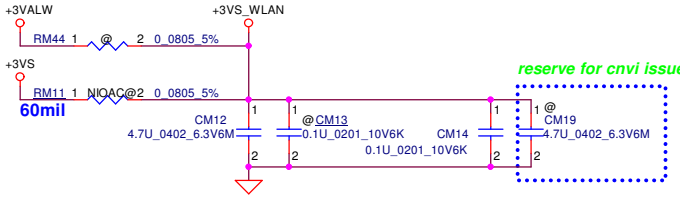
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

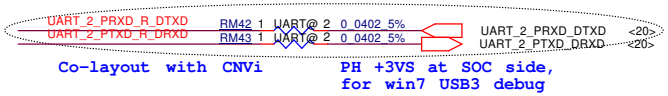
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title	LAN RTL8411H		
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
Date: Thursday, February 22, 2018	Sheet 36 of 67		

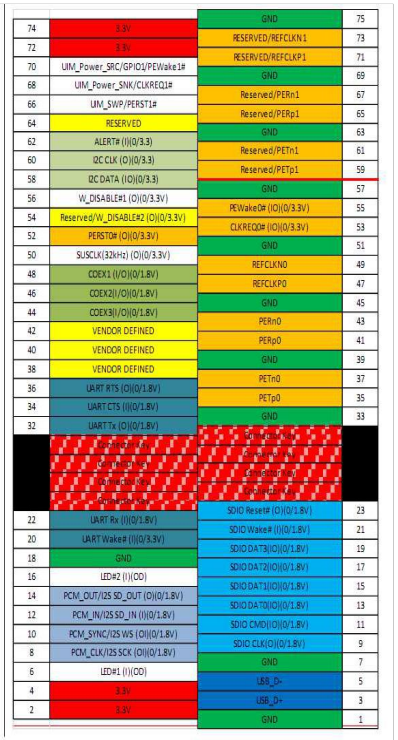
Wireless LAN



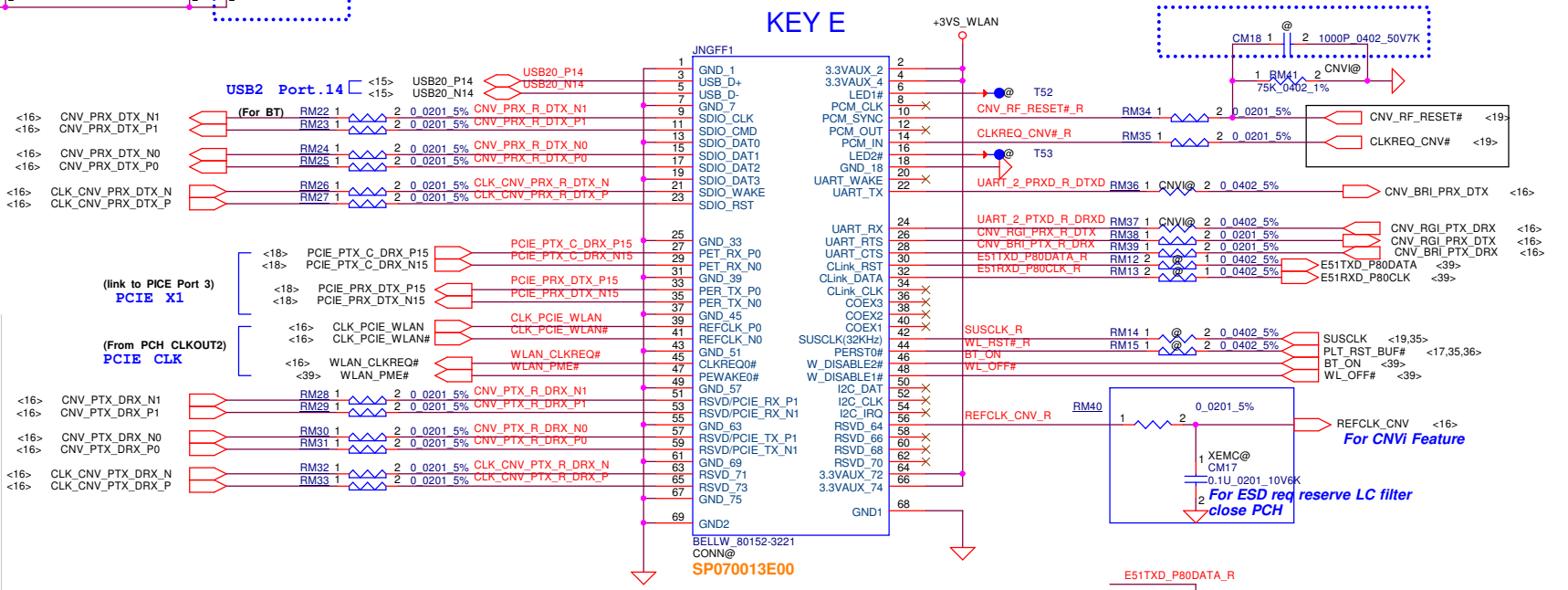




NGFF WL+BT (KEY E)



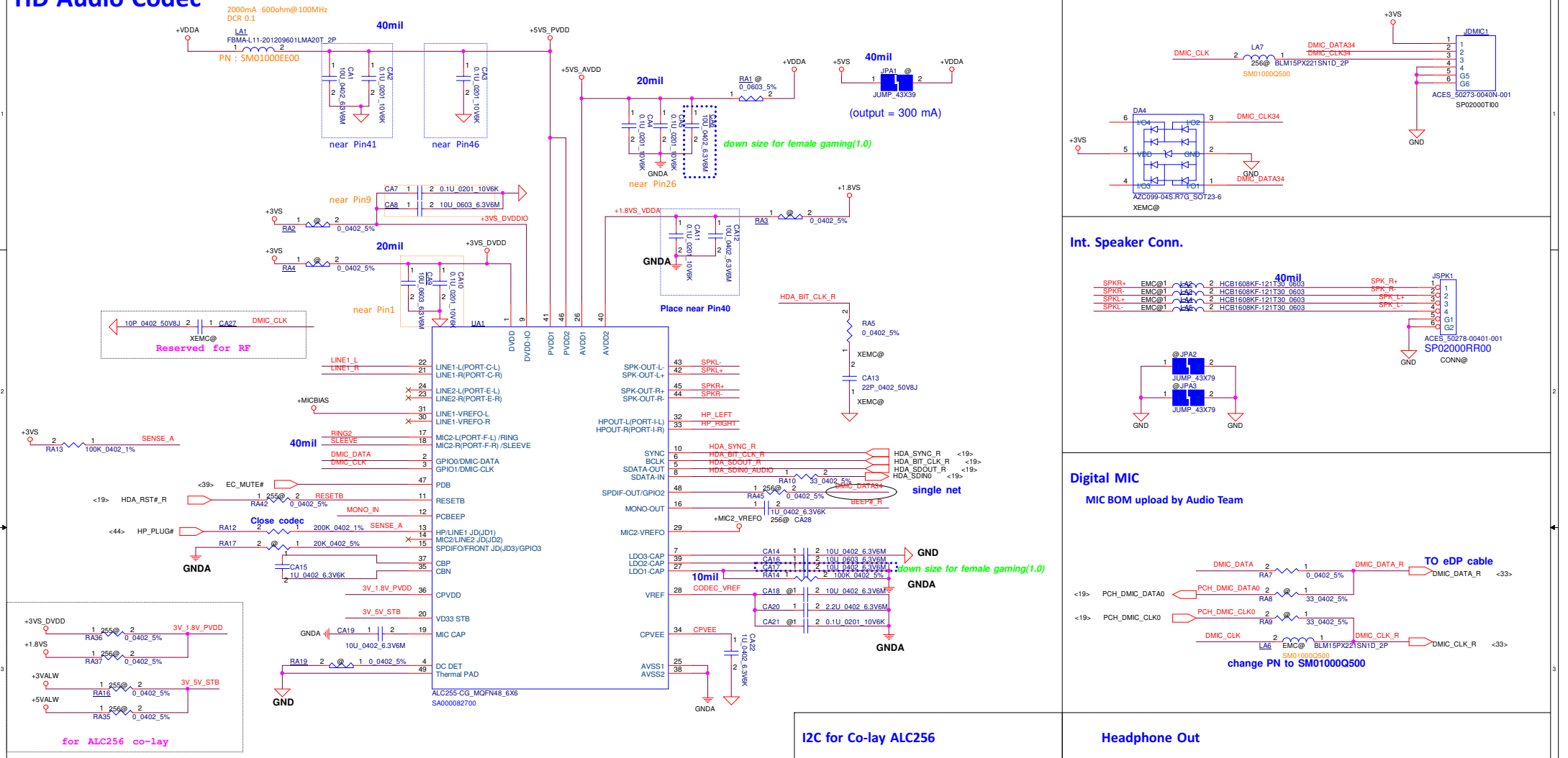
KEY E



Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title: M.2 Key E (WLAN)			
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
Date: Thursday, February 22, 2018	Sheet 37 of 67		

HD Audio Codec



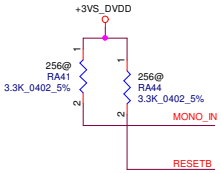
DMIC3 Conn. (support on 256)

Int. Speaker Conn.

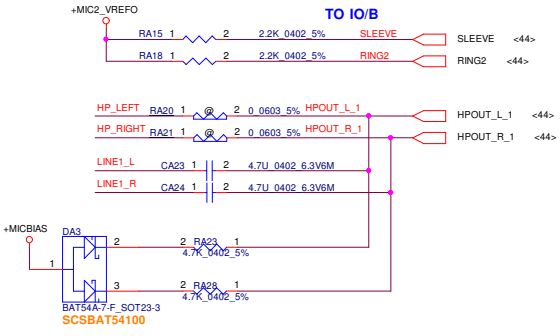
Digital MIC

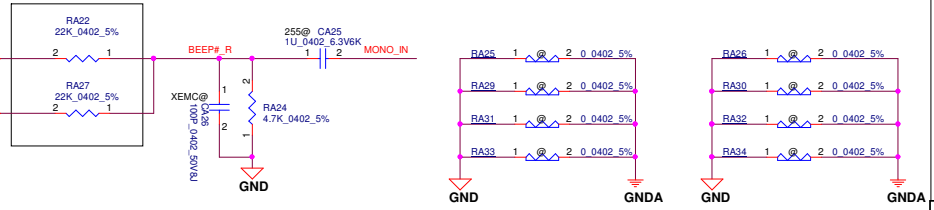
MIC BOM upload by Audio Team

I2C for Co-lay ALC256



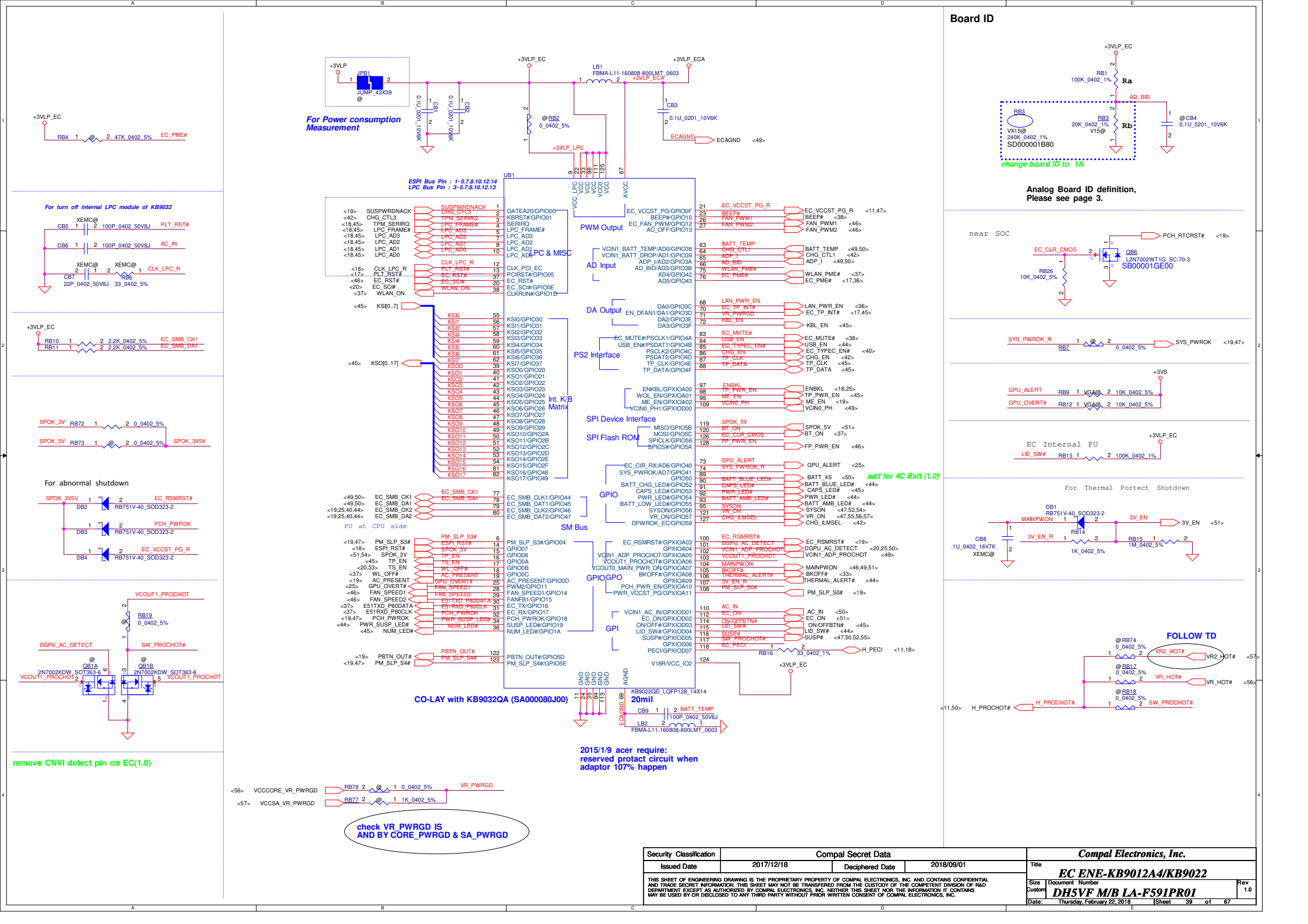
Headphone Out





Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.			
Title: HD Audio Codec ALC255			
Size: Custom	Document Number: DH5VF M/B LA-F591PR01		Rev: 1.0
Date: Thursday, February 22, 2018	Sheet 38 of 67		



Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

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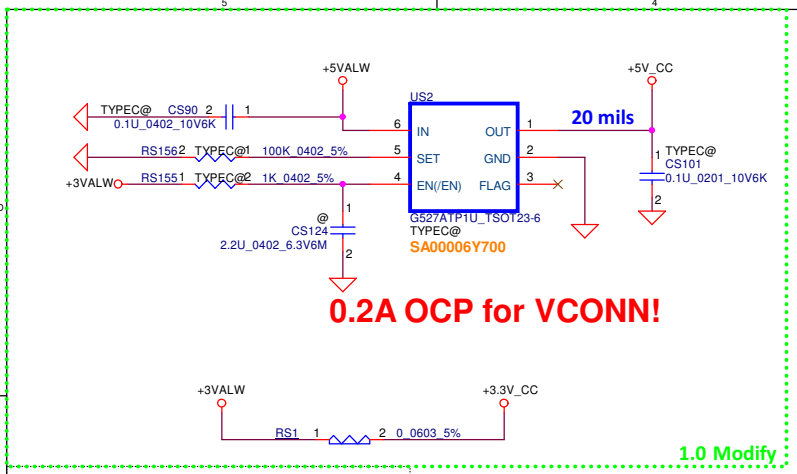
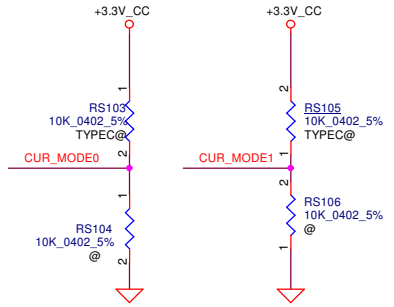
Compal Electronics, Inc.

Title: **EC ENE-KB9012A4/KB9022**

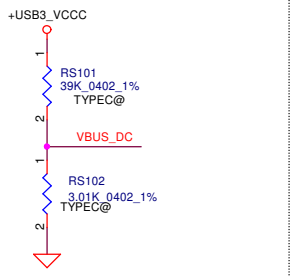
Size: Custom | Document Number: **DH5VF M/B LA-F591PR01** | Rev: 1.0

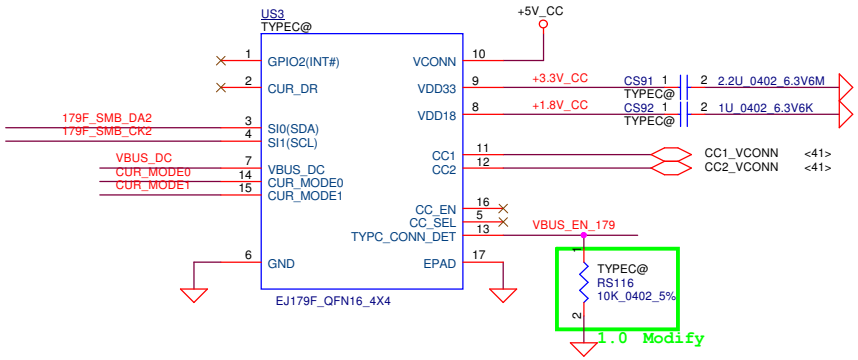
Date: Thursday, February 22, 2018 | Sheet 39 of 67

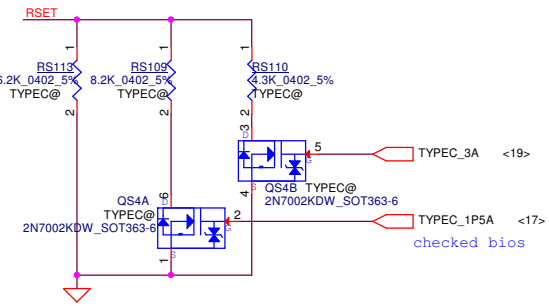




Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current







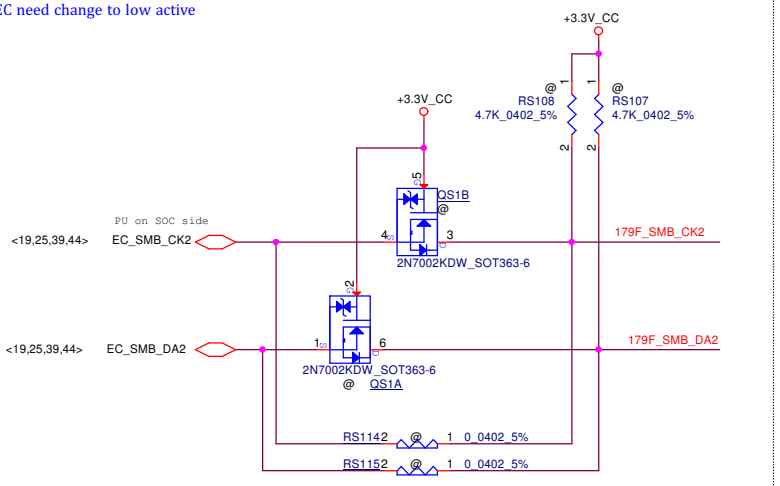
G518 MOS Current Limit				
GPP_B1 (TYPEC_3A)	GPP_B4 (TYPEC_1P5A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

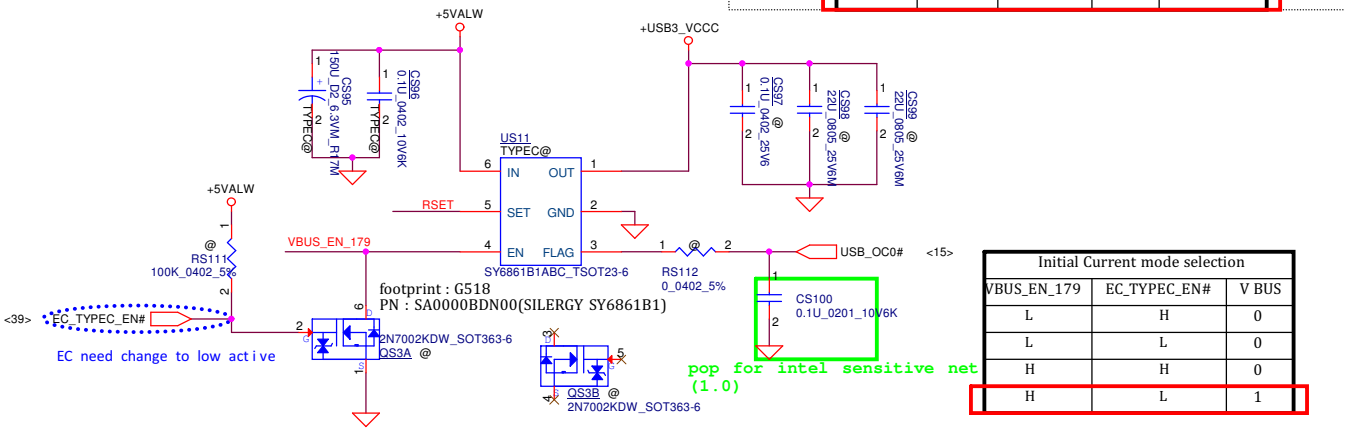
Remove INT#,
platform doesn't monitor it

CC_SEL
report CC1 or CC2 is connection

CC_EN
power path control "low active"

EC need change to low active

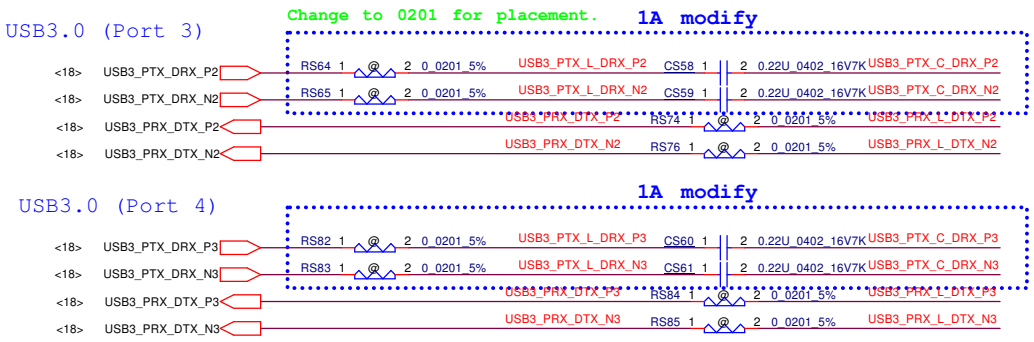


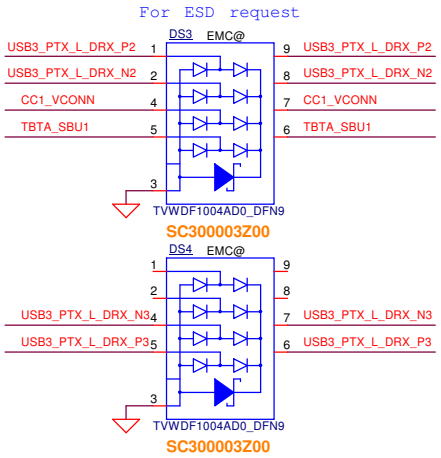


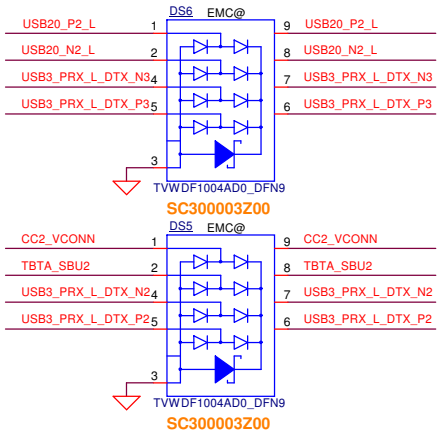
Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

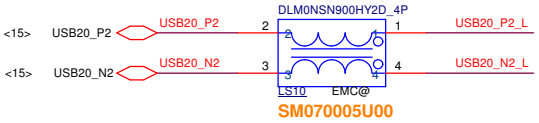
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

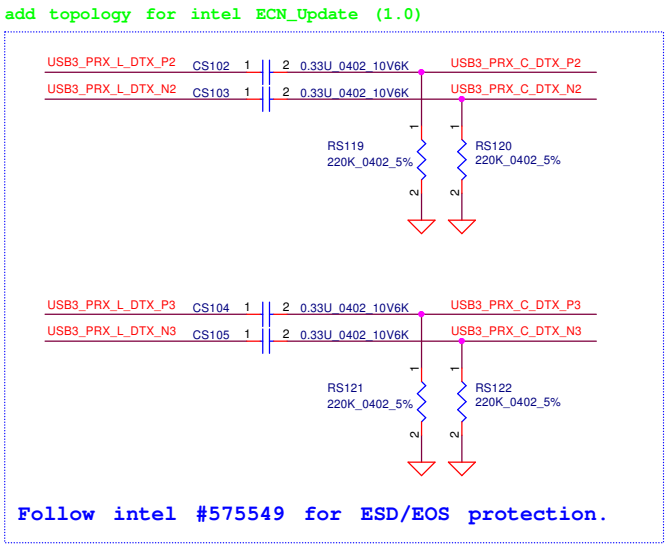
Compal Electronics, Inc.	
Title	CC+USB TYPE C
Size: Custom	Document Number: DH5VF M/B LA-F591PR01
Rev	1.0
Date: Thursday, February 22, 2018	Sheet 40 of 67

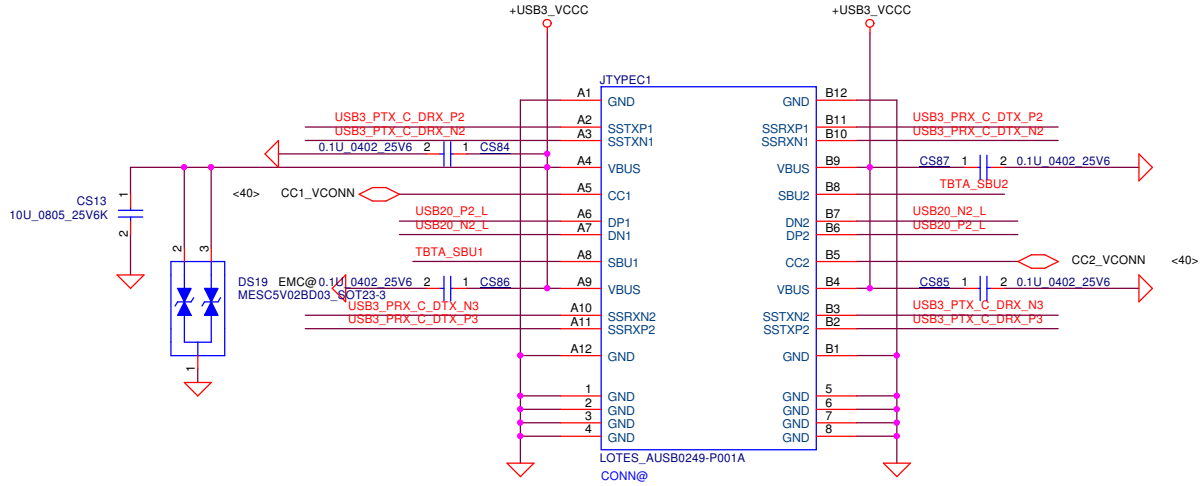












CC1_VCONN & CC2_VCONN need 20mil trace width.

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

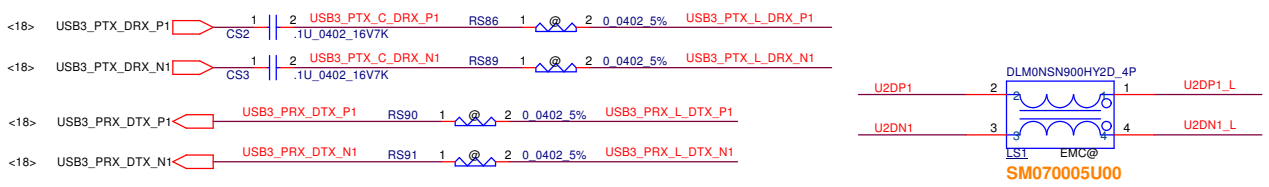
Compal Electronics, Inc.

Title: CC+USB TYPE C

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

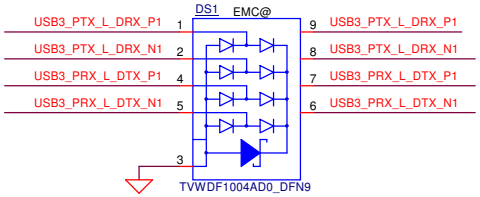
Date: Thursday, February 22, 2018 | Sheet 41 of 67

USB3.0 /2.0 CMC

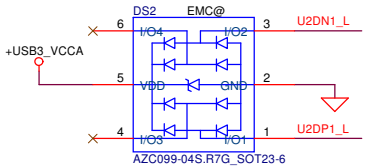


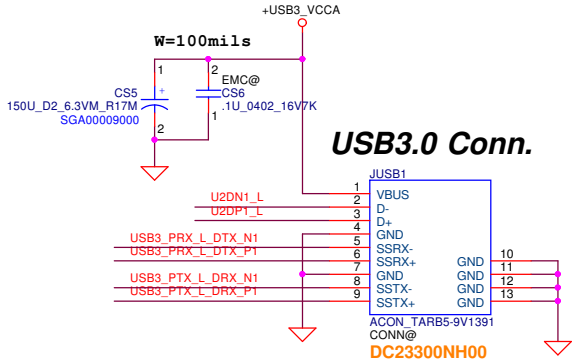
SM070005U00

ESD request



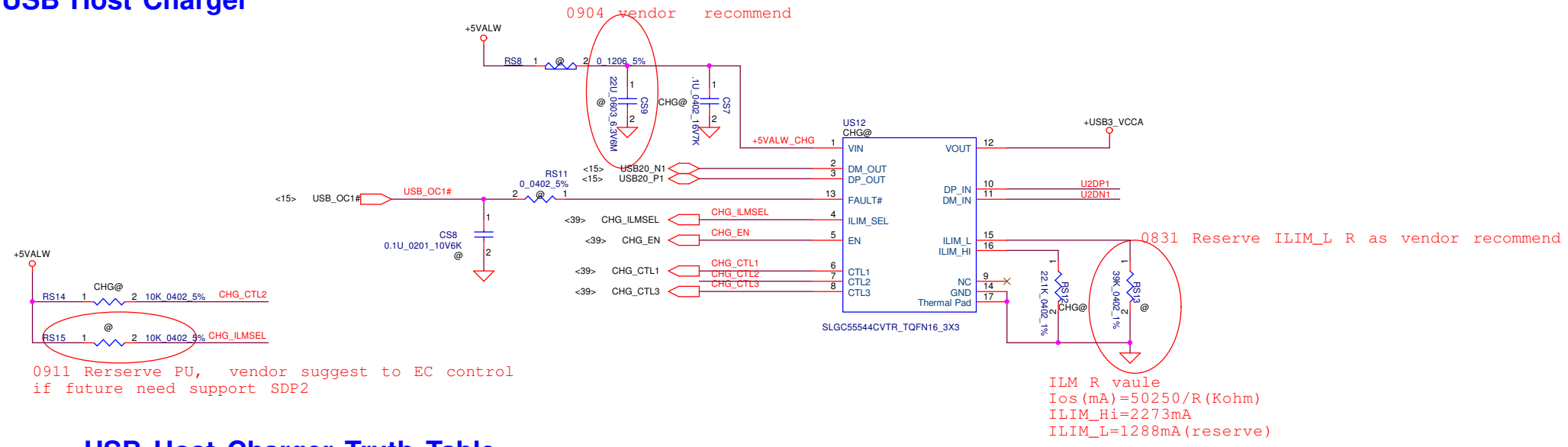
SC300003Z00





DC23300NH00

USB Host Charger



SLGC55544CVTR_TQFN16_3X3

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

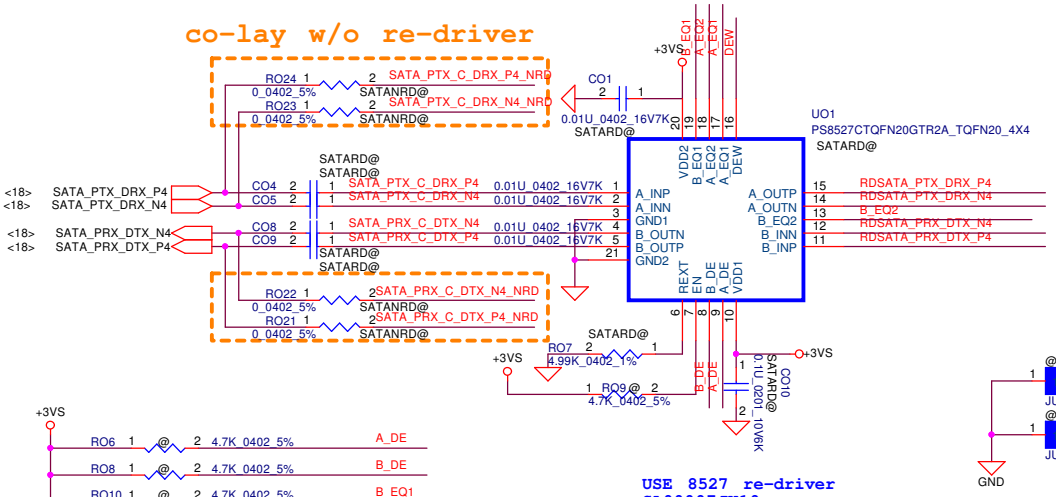
Compal Electronics, Inc.

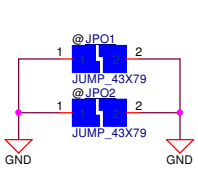
Title: USB3.0 Conn/USB Charger

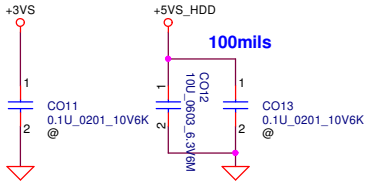
Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

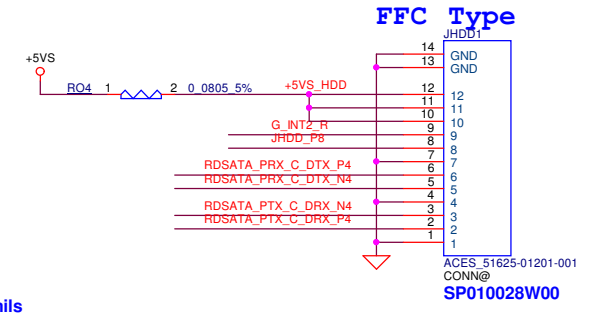
Date: Thursday, February 22, 2018 | Sheet 42 of 67

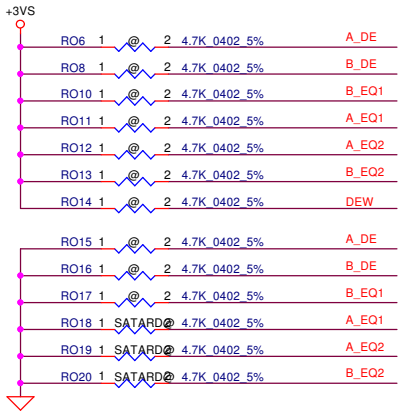
SATA Re-Driver and cable HDD Conn.











Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.

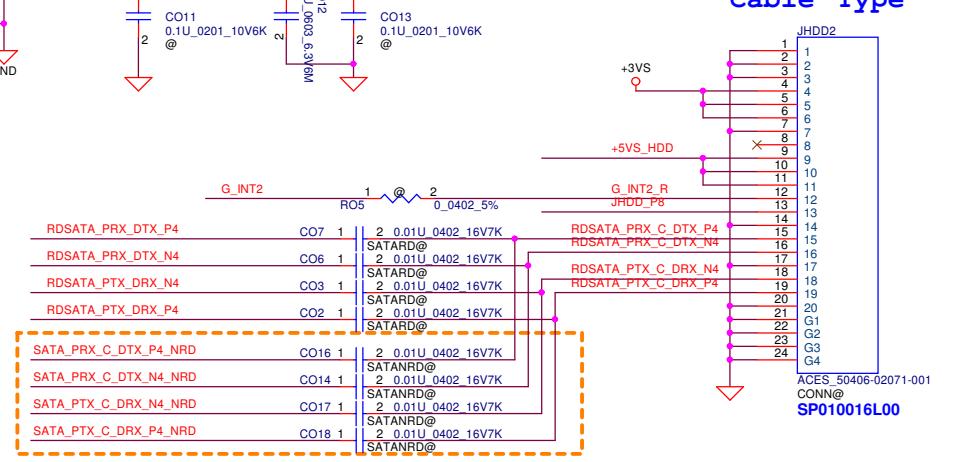
Internally tied to VDD/2 (M status).

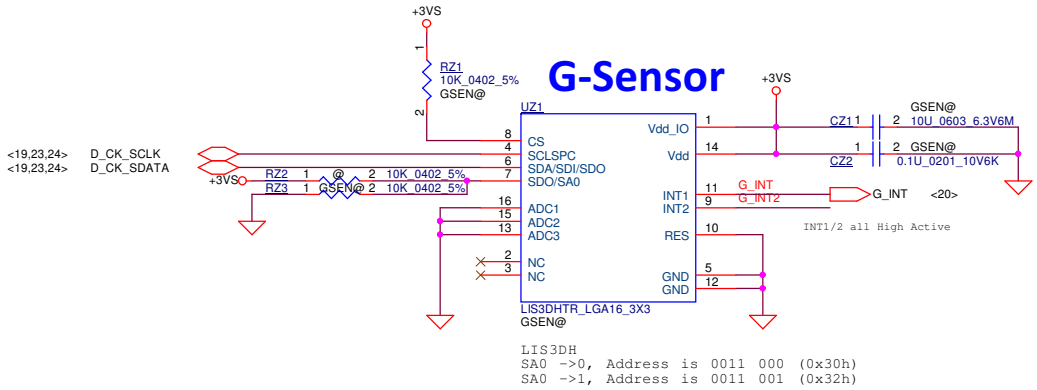
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB





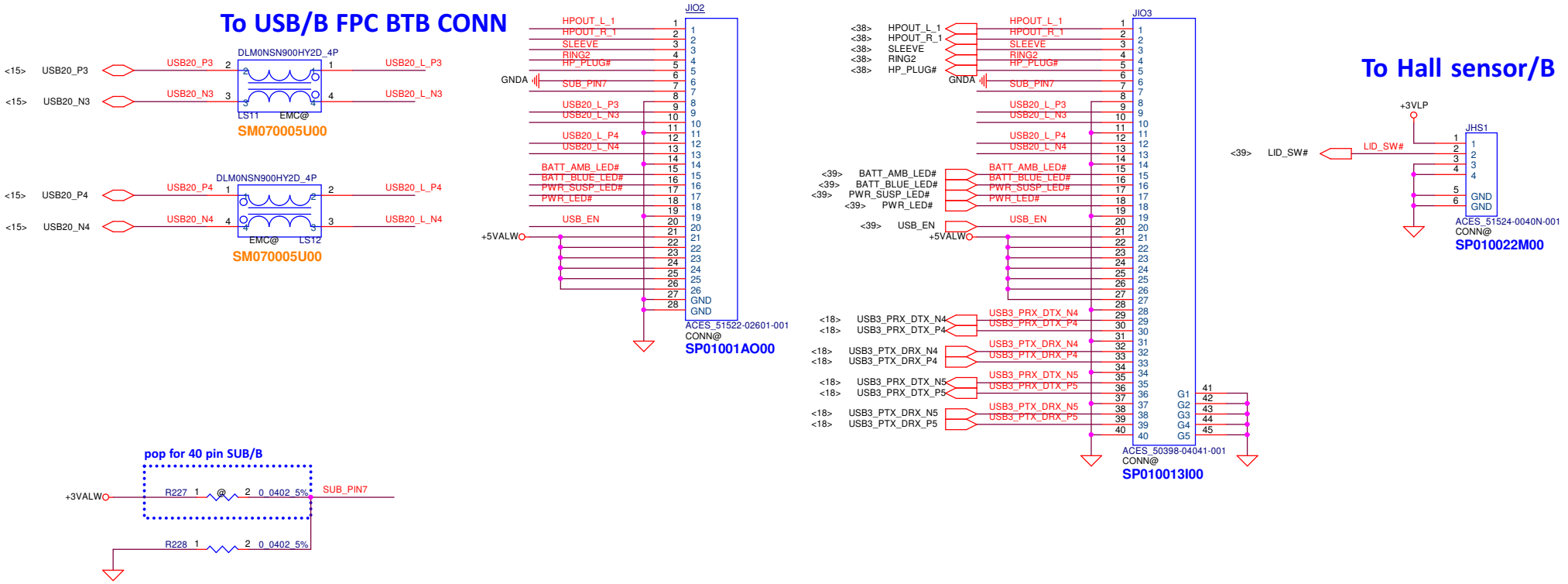
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

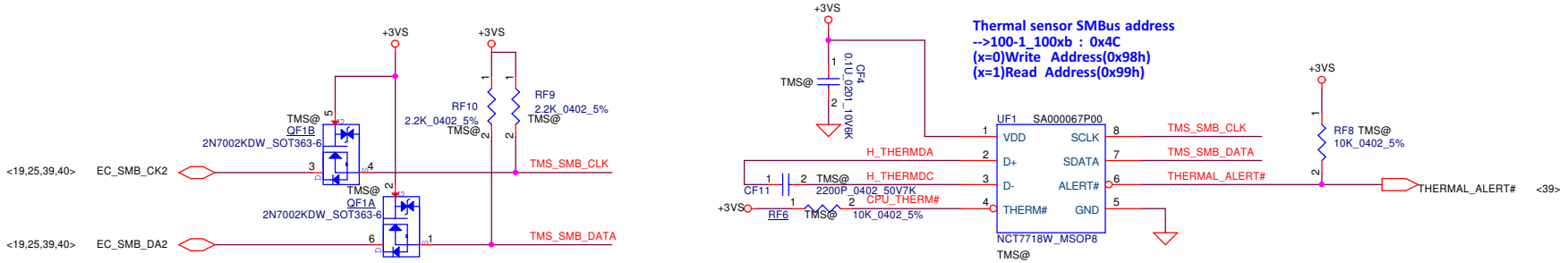
Title: HDD/ Re-Driver/ G-sensor

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 43 of 67



THERMAL SENSOR



Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: FUN/B & LED/B

Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

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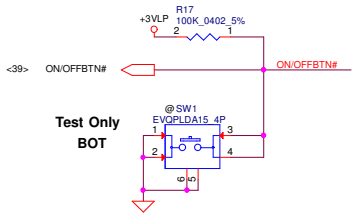
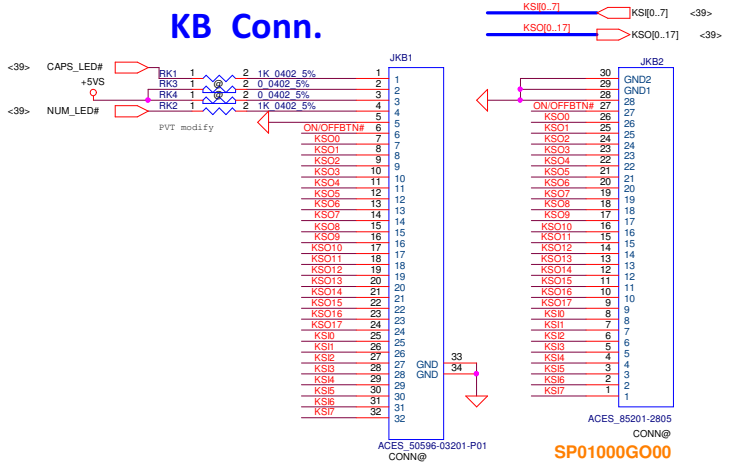
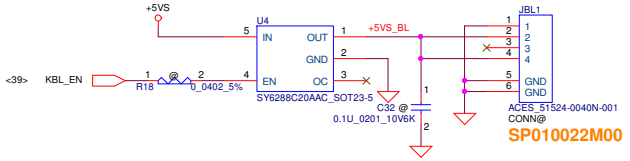
ON/OFF BTN



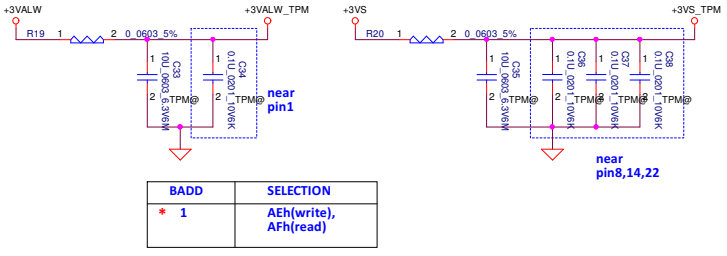
KB Conn.



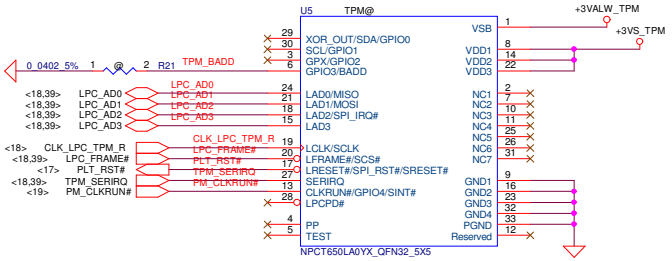
KB BackLight



TPM



BADD	SELECTION
* 1	AEh(write), AFh(read)



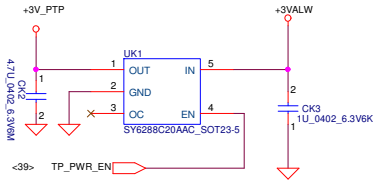
SERIRQ PH 10K to +3VS at PCH side

CLKRUN# PH 10K to +3VS at PCH side

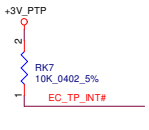
LPCPD# had internal PH

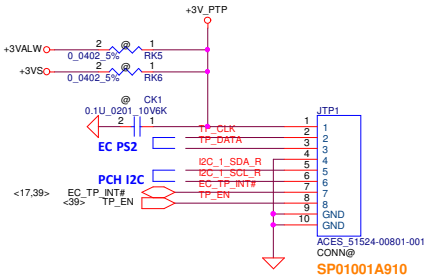
P/N:SA00008ELC0 (S IC NPCT650ABBYX QFN 32P TPM2.0 FW 1.3.1.0)

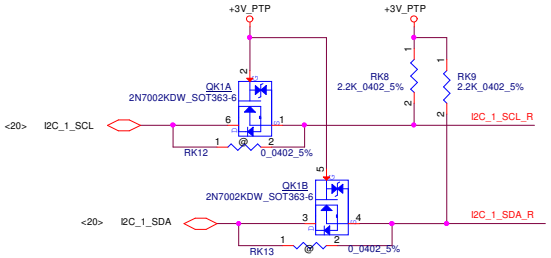
Touch Pad

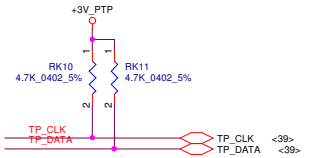


TP_PWR_EN follow SYSON behavior



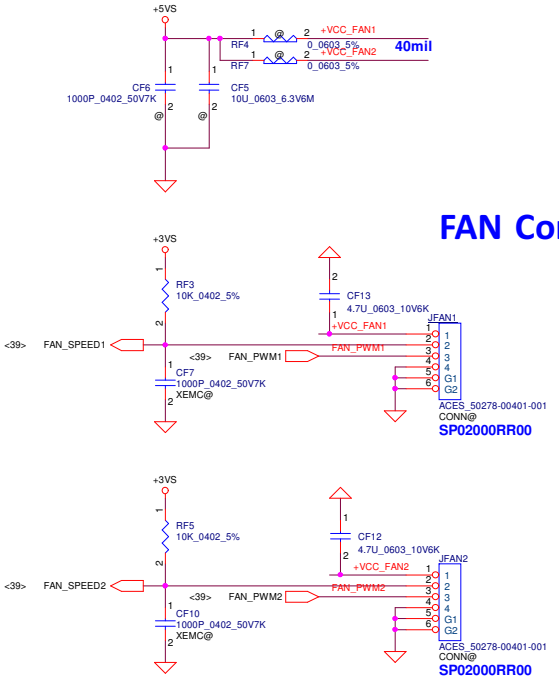


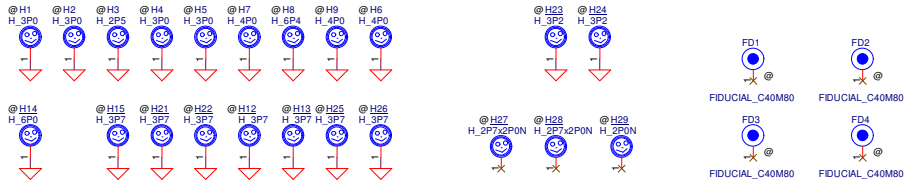


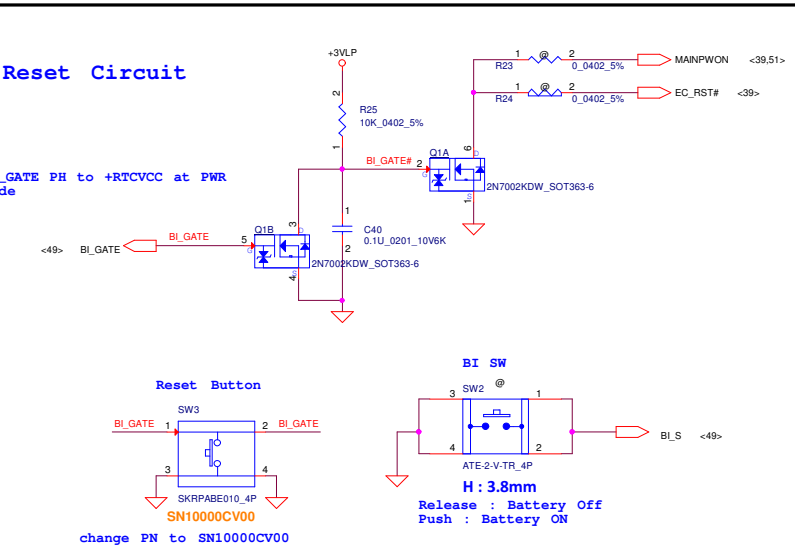


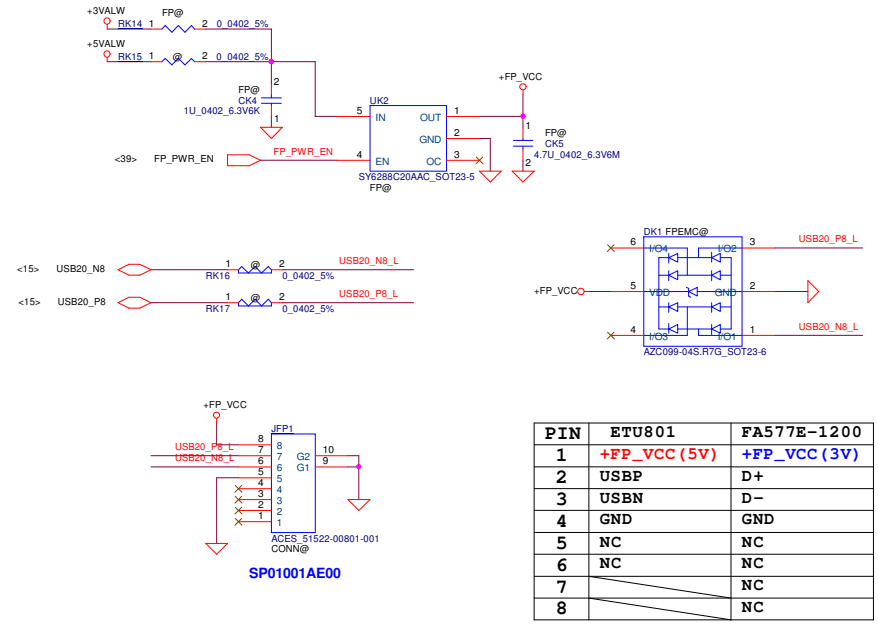
Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.	
Title	KB & TP & TPM Connector
Size / Document Number	DH5VF M/B LA-F591PR01
Rev	1.0
Date: Thursday, February 22, 2018	Sheet 45 of 67









PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

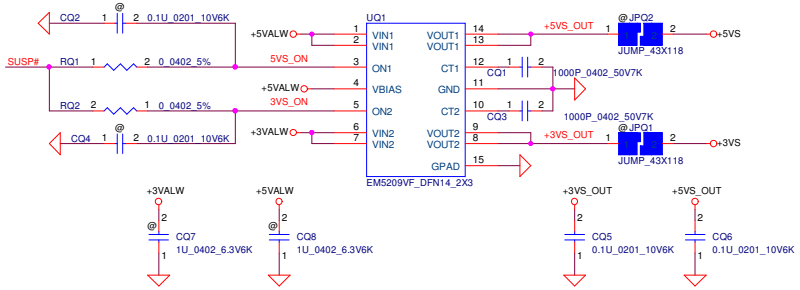
Compal Electronics, Inc.

Title: FAN & FP & Screw Hole

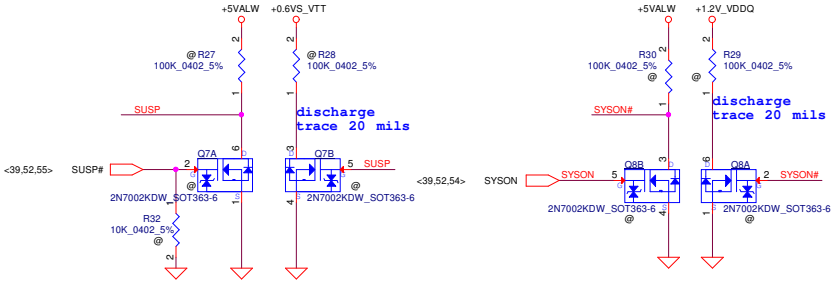
Size: Custom | Document Number: DH5VF M/B LA-F591PR01 | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 46 of 67

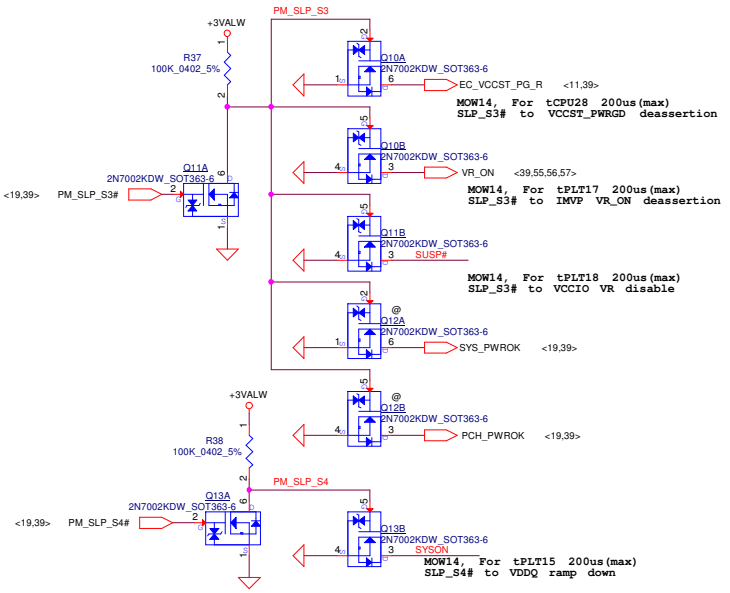
System DC inferface



Place CQ7 close UQ1 pin 1&2
Place CQ8 close UQ1 pin 6&7

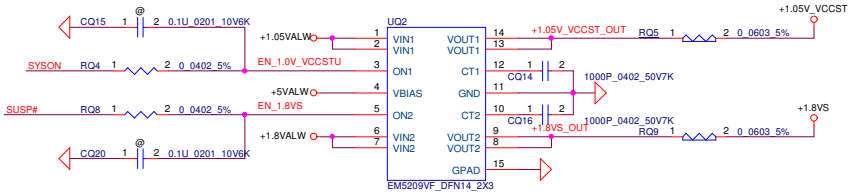


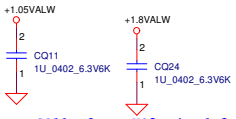
For Power ON/Off Sequence



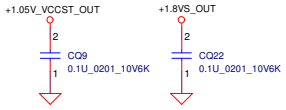
P/N: SB00000EO00 footprint use SB00000ZU00

+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS

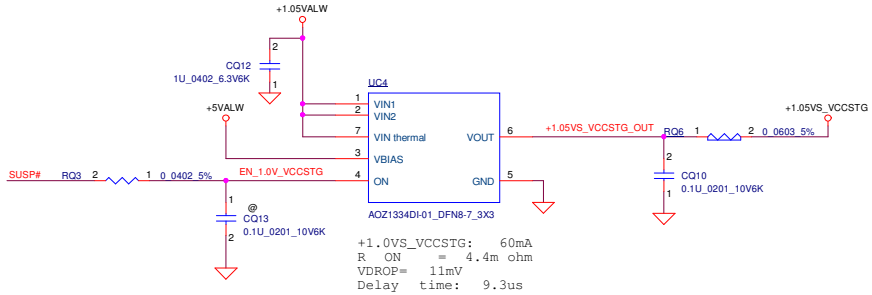




Place CQ11 close UQ2 pin 1&2
Place CQ24 close UQ2 pin 6&7



+1.05VALW TO +1.05VS_VCCSTG



+1.0VS_VCCSTG: 60mA
R ON = 4.4m ohm
VDROP= 11mV
Delay time: 9.3us

Security Classification	Compal Secret Data		
Issued Date	2017/12/18	Deciphered Date	2018/09/01

Compal Electronics, Inc.

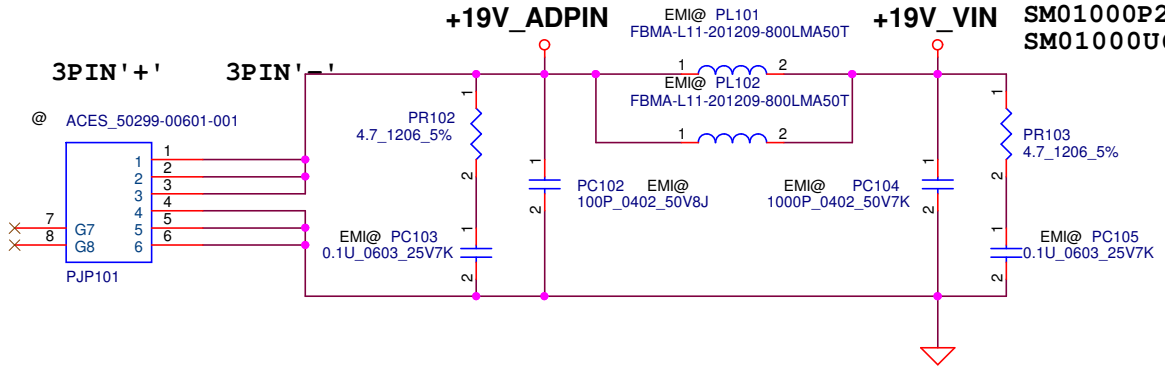
Title: DC Interface

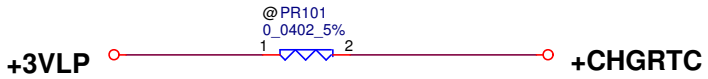
Size	Document Number	Rev
Custom	DH5VF M/B LA-F591PR01	1.0

Date: Thursday, February 22, 2018 Sheet 47 of 67

change PL101 PL102 from SM01000P200 to comm part SM01000U600

20160216 3PIN'+' 3PIN'-'





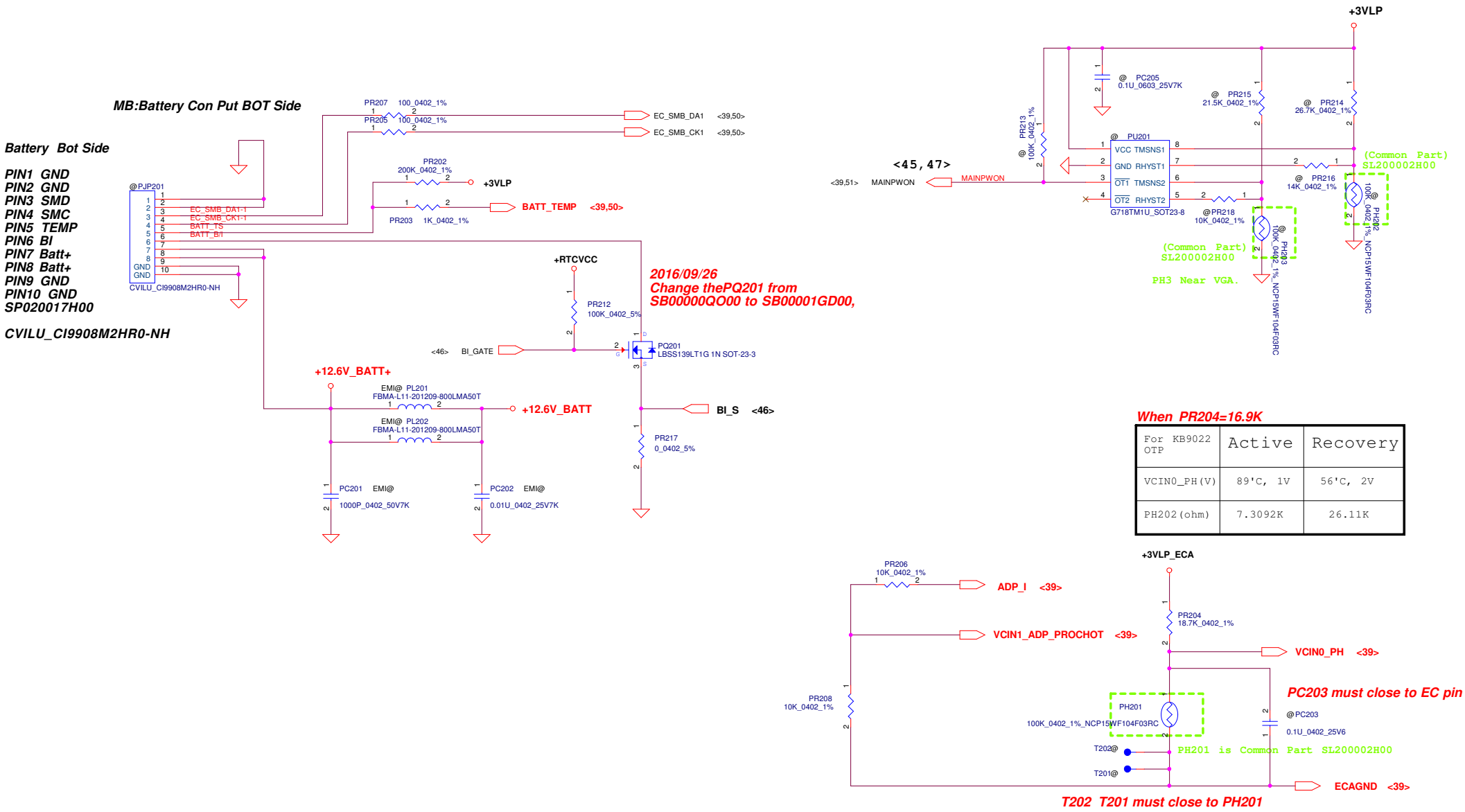
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DCIN

Size: Custom | Document Number: C5MMH M/B LAE911P | Rev: 0.1

Date: Thursday, February 22, 2018 | Sheet 48 of 67



Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 0.1

Date: Thursday, February 22, 2018 | Sheet 49 of 67

Module model information

ISL95520_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 L2N7002WT1G_SC70-3

PR301 1M_0402_1%

PR302 3M_0402_5%

Need check the SOA for inrush

+19V_VIN

PQ310 EMB04N03H_EDFN5X6-8-5

+19V_P1

PQ311 AON7380_DFN3X3-8-5

+19V_P2

PR303 0.005_1206_1%

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

EMI@ PL704 FBMA-L11-201209-800LMA50T

@PJP1 JUMP_43X118

Co-lay jump and ISN choke.

+19VB

+19VB_CHG

PC302 10U_0805_25V6K

PC303 10U_0805_25V6K

PC305 EMI@ 0.1U_0402_25V6

PC304 EMI@ 2200P_0402_25V7K

PC324 EMI@ 0.1U_0402_25V6

@PC322 1000P_0402_25V

CSIP_CHG_R

CSIN_CHG_R

PR304 @ 0_0402_5%

PR305 2_0402_5%

PC306 0.1U_0402_25V6

PR306 499K_0402_1%

PR307 4.02K_0402_1%

PR308 4.02K_0402_1%

Range:2V~3.5V
20*49.9/(392+49.9)=2.55V

PR310 66.5K_0402_1%

PC301 2200P_0402_50V7K

support Turbo boost : 2200P
no support Turbo boost : 0.1u

PQ312 AON7380_DFN3X3-8-5

PR309 100_0402_1%

+12.6V_BATT

CMSRC_CHG

ASGATE_CHG

PC307 0.22U_0603_25V7K

@PC308 0.1U_0402_25V7K

CSIP_CHG

CSIN_CHG

OPCN_CHG

OPCP_CHG

VBAT_CHG

BGATE_CHG

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 1
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W

Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 2
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x (VAD P x IAD P + VBA T x IBA T)
K_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.

adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

PR311 100K_0402_1%

VDD_CHG

ACIN_CHG

<39> AC_IN

PR313 158K_0402_1%

<39,49> EC_SMB_DA1

<39,49> EC_SMB_CK1

<11,39> H_PROCHOT#

<39> ADP_I

@PR314 0_0402_5%

@PR316 0_0402_5%

@PR317 0_0402_5%

PR318 8K_0402_1%

PR321 24K_0402_1%

EC_SMB_DA1_R

EC_SMB_CK1_R

AMON_ISL95520

BMON_ISL95520

Close to EC.

PU301 ISL88739AHRZ-T_QFN32_4X4

ACIN ACOK SDA SCL PROCHOT# AMON BMON NC AGND PROG COMP CCLIM FSET BATGONE CSON CSOP ACLIM

BOOT UGATE PHASE LGATE VDDP VDD DCIN NTC

BST_CHG UG_CHG LX_CHG LG_CHG VDDP_CHG VDD_CHG

PC309 0.47U_0402_16V4Z

PR312 0_0603_5%

PQ305 AON7506_DFN33-8-5

PQ306 AON7506_DFN33-8-5

Choke 4.7uH SH00000YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)

PL301 4.7UH_PCMB063T-4R7MS_8A_20%

+17.4V_BATT_CHG

PR315 0.01_1206_1%

+12.6V_BATT

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

PC310 10U_0805_25V6K

PC311 10U_0805_25V6K

PC312 10U_0805_25V6K

PR319 4.7_0402_5%

PC313 1U_0201_6.3V6K

PC314 1U_0201_6.3V6K

PR320 4.7_1206_5%

EMI@ PC315 680P_0402_50V7K

PR323 100K_0402_1%

PR324 10_1206_5%

PC318 1U_0603_25V6

PD1 S SCH DIO BAS40CW SOT-323

VF = 0.38V

+19V_VIN

+12.6V_BATT

PC316 0.1U_0402_25V6

PC317 0.1U_0402_25V6

Close to EC.

Follow adapter and battery wattage in Vsys current source.
Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

PR322 @ 0_0402_5%

VDD=5V

VDD_CHG

PR325 10K_0402_1%

CCLIM_CHG

ACLIM_CHG

PROG_CHG

COMP_CHG

FSET_CHG

CSOP_CHG

CSOP_CHG_R

CSON_CHG

CSON_CHG_R

PR328 200K_0402_1%

PR329 200K_0402_1%

PR330 2_0402_5%

PC319 0.1U_0402_25V6

@PR334 0_0402_5%

PR333=0 ohm, Fs=500KHZ ~ +/- 15%

@ PR331 76.8K_0402_1%

PR335 150K_0402_1%

@ PC320 560P_0402_50V7K

PR332 100_0402_1%

PC321 0.015U_0402_25V7K

@PR333 0_0402_5%

BATT_TEMP <39,49>

BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

+3VS

@VGA@ PR340 10K_0402_1%

@VGA@ PR341 10K_0402_1%

@ PQ309 L2N7002WT1G_SC70-3

AC_IN

PR336 135W@

PR337 75K_0402_1%

OCCP setting

Hybrid boost power mode
Cell = 4s

<20,25,39> DGPU_AC_DETECT

@VGA@ PQ314 RUM001L02_VMT3

@VGA@ PQ313B 2N7002KDW_SOT363-6

@VGA@ PQ313A 2N7002KDW_SOT363-6

H_PROCHOT#

AC_IN

ICClimit : 7.73A
Delta I : 1.44A
IC charge current :6.48A

Battery current limimed by CCLim ~ 3.89A.
Adapter current limimed by ACLim ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ).
CC_LIM = VccLIM / 64 x Rs2
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ).
CC_LIM = VccLIM / 32 x Rs2
AC_LIM = Vac_LIM / 32 x Rs1

For 4S per cell 4.35V battery

ACIN_CHG

4S_BATT@ PR338 2M_0402_1%

4S_BATT@ PR339 100K_0402_1%

4S_BATT@ PQ315 LTC015EUBF38TL_UMT3F

<39> BATT_4S

4S_BATT@ PQ316 L2N7002WT1G_SC70-3

<39,52,55> SUSP#

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

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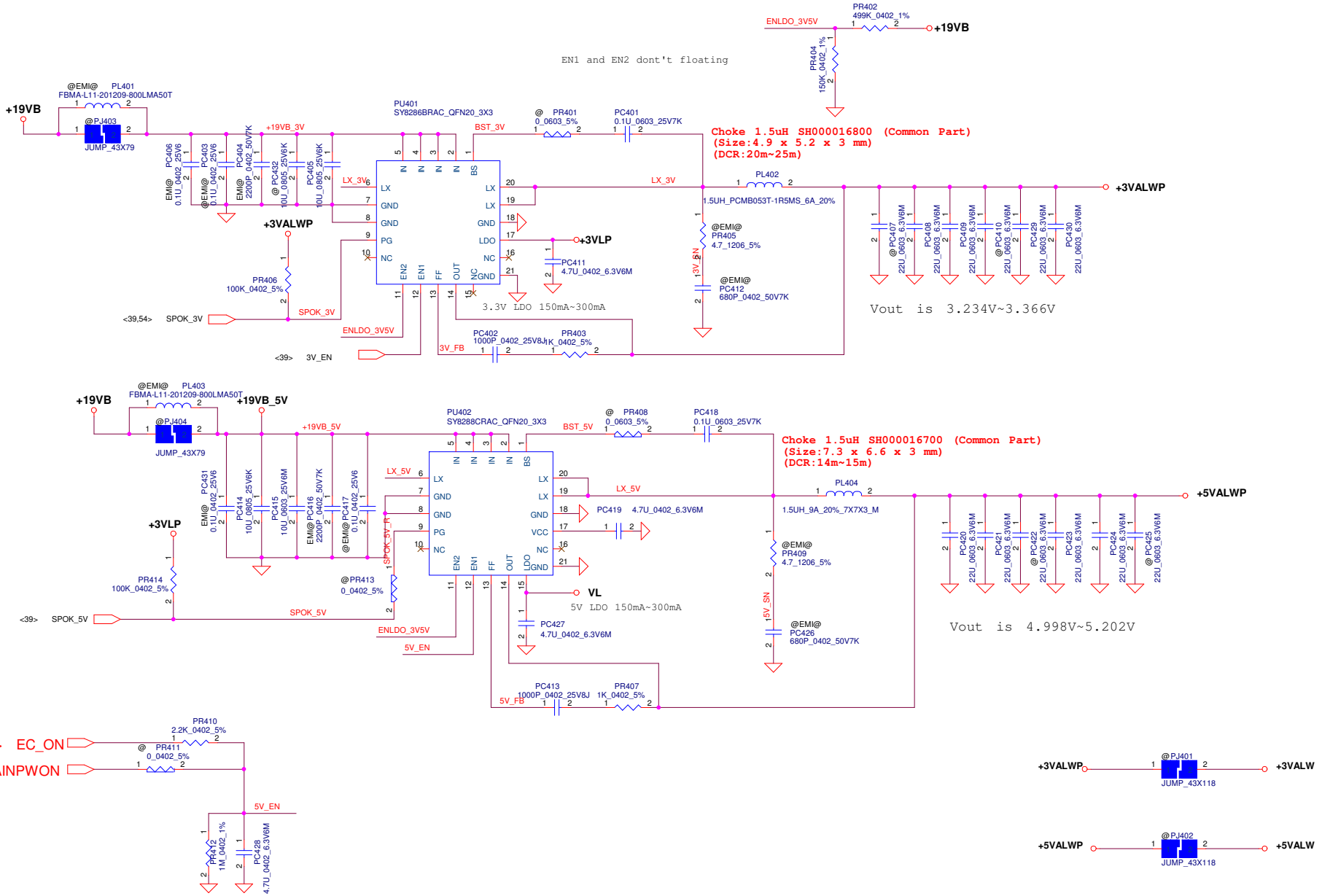
Compal Electronics, Inc.

Title: PWR_CHARGER

Size: Document Number: Rev: 0.1

Date: Thursday, February 22, 2018 Sheet 50 of 67



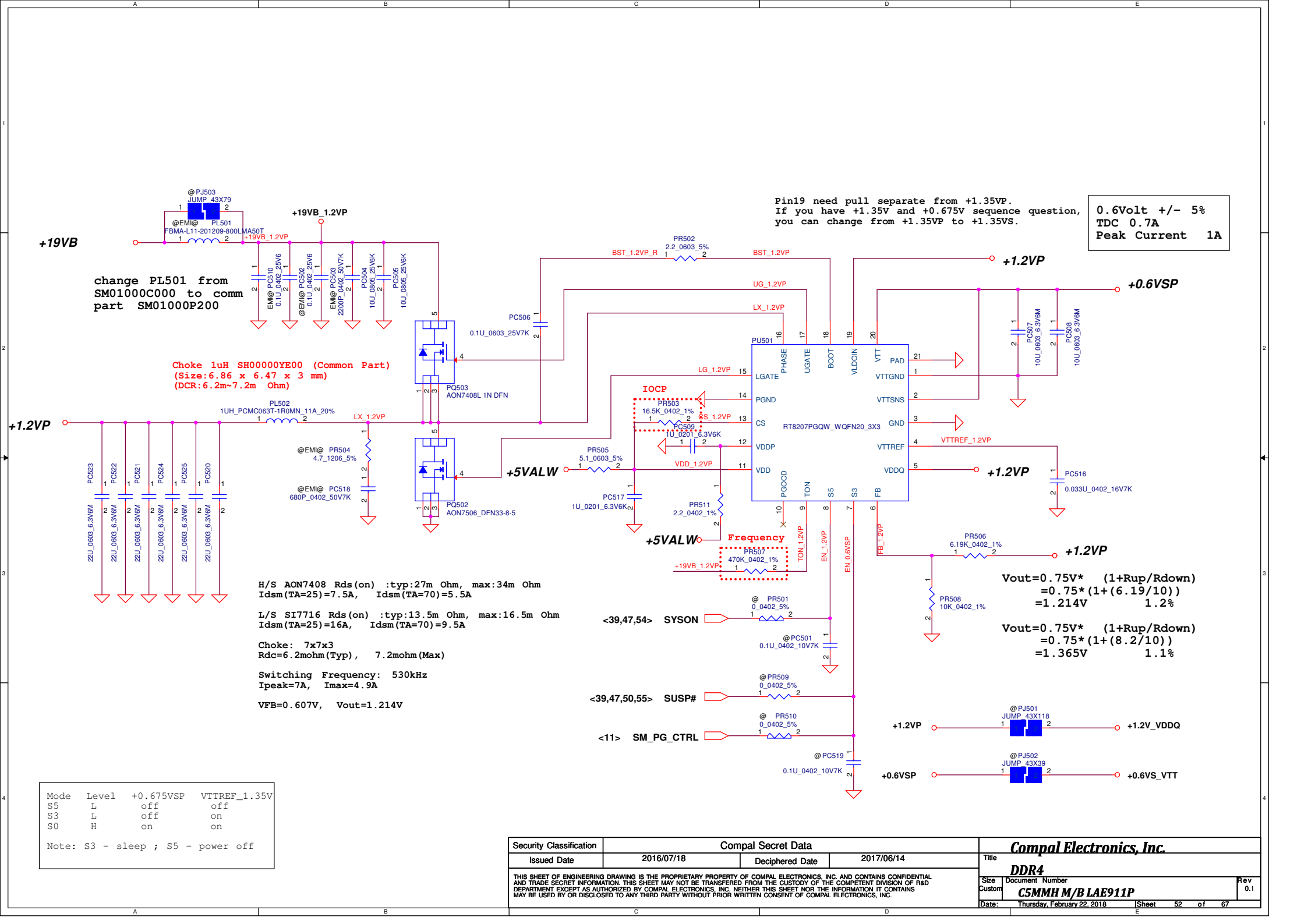
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	C5MMH M/B LAE911P	0.1

Date: Thursday, February 22, 2018 | Sheet 51 of 67



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

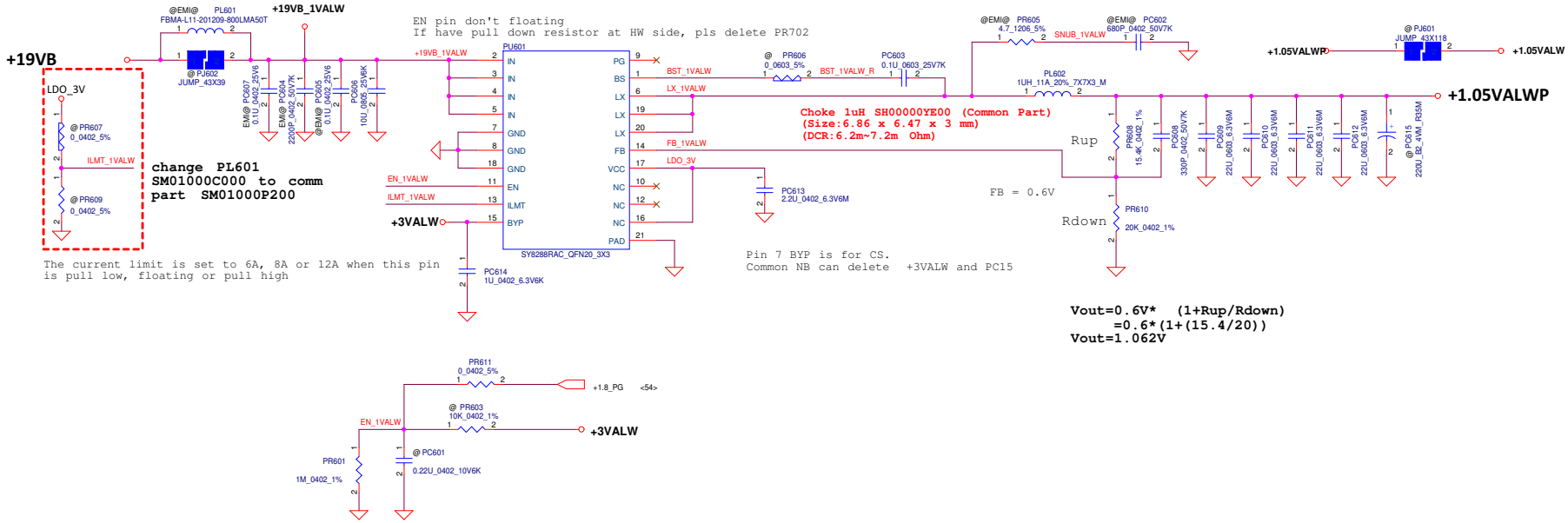
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DDR4

Size: Custom | Document Number: C5MMH M/B LAE911P | Rev: 0.1

Date: Thursday, February 22, 2018 | Sheet 52 of 67



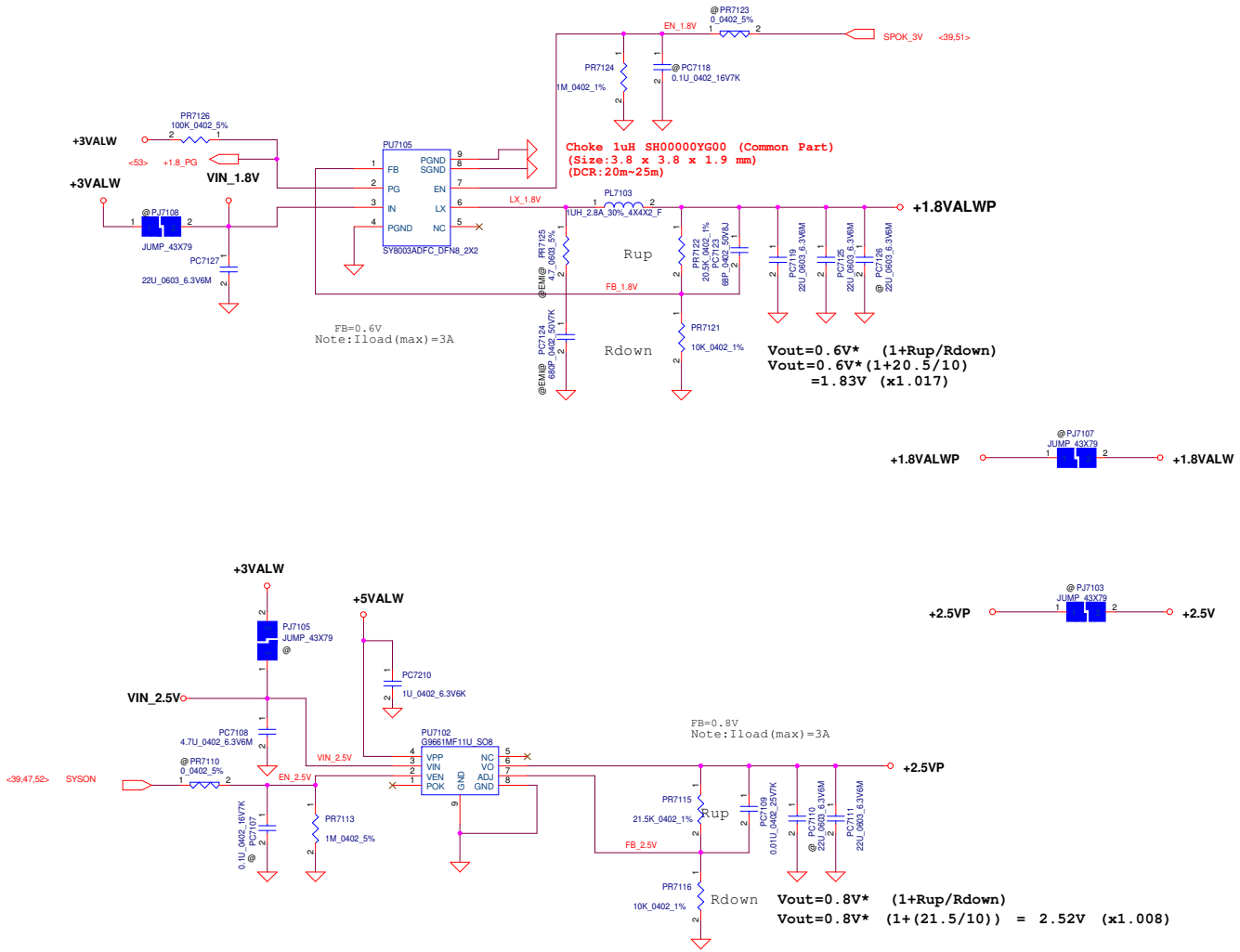
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 1V

Size	Document Number	Rev
C	C5MMH M/B LAE911P	0.1

Date: Thursday, February 22, 2018 Sheet 53 of 67



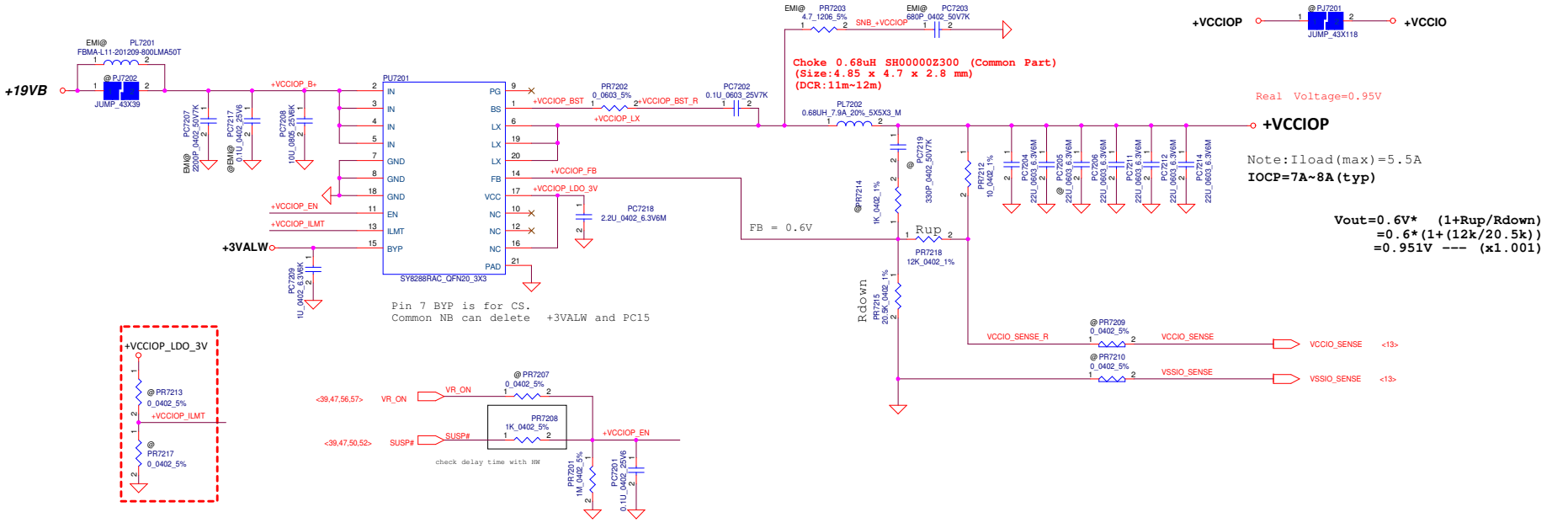
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: **1.5VS/2.5V**

Size	Document Number	Rev
C	C5MMH M/B LAE911P	0.1

Date: Thursday, February 22, 2018 Sheet 54 of 67



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: C5MMH M/B LAE911P

Size	Document Number	Rev
C	1.0VS_VCCIO	0.1

Date: Thursday, February 22, 2018 Sheet 55 of 67

90A for ICCMAX=2.2V 76A for ICCMAX=2.2V

Fs=400k, LL=1.8m for Core
Fs=400k, LL=2.1m for GT
SET1 ICCMAX=128A, OCP=120%, DVIDT=35.7mV.
SET2 Ramp=133%, DVIDW=9us, QRT=25mV, QRW=44%
SET3 Zero LL disable, VR address Core=0, GT=1.
SETA1 ICCMAX=32A, OCP=120%, DVIDT=60mV.
SETA2 Ramp=133%, DVIDW=9us, QRT=25mV, QRW=44%
Core offset function disable, GT offset function disable, PSYS disable.

RT3607CE

GND

Reserved for RF Team Request

ENABLE
Upper Threshold > 0.8V
Lower Threshold < 0.3V

confirm with power sequence, it need behind +5VS.

PR94and PR98 pull high resistor are pop at the end of VR SVID.
Other VR is unpop.

H/S AON6380 Rds(on) :typ:8.2mOhm, max:10.5mOhm
Idsm(TA=25)=22A, Idsm(TA=70)=17.5A

L/S AON6314 Rds(on) :typ:2.8mOhm, max:3.5mOhm
Idsm(TA=25)=37A, Idsm(TA=70)=30A

Ta=70=>Id=17.5A
Rdson=8.2-10.5 mohm

Ta=70=>Id=30A
Rdson=2.8-3.5 mohm

Choke 0.15uH SH00000X700
(Size:6.59 x 6.6 x 3.0 mm)
(DCR:0.9m +-7%)

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

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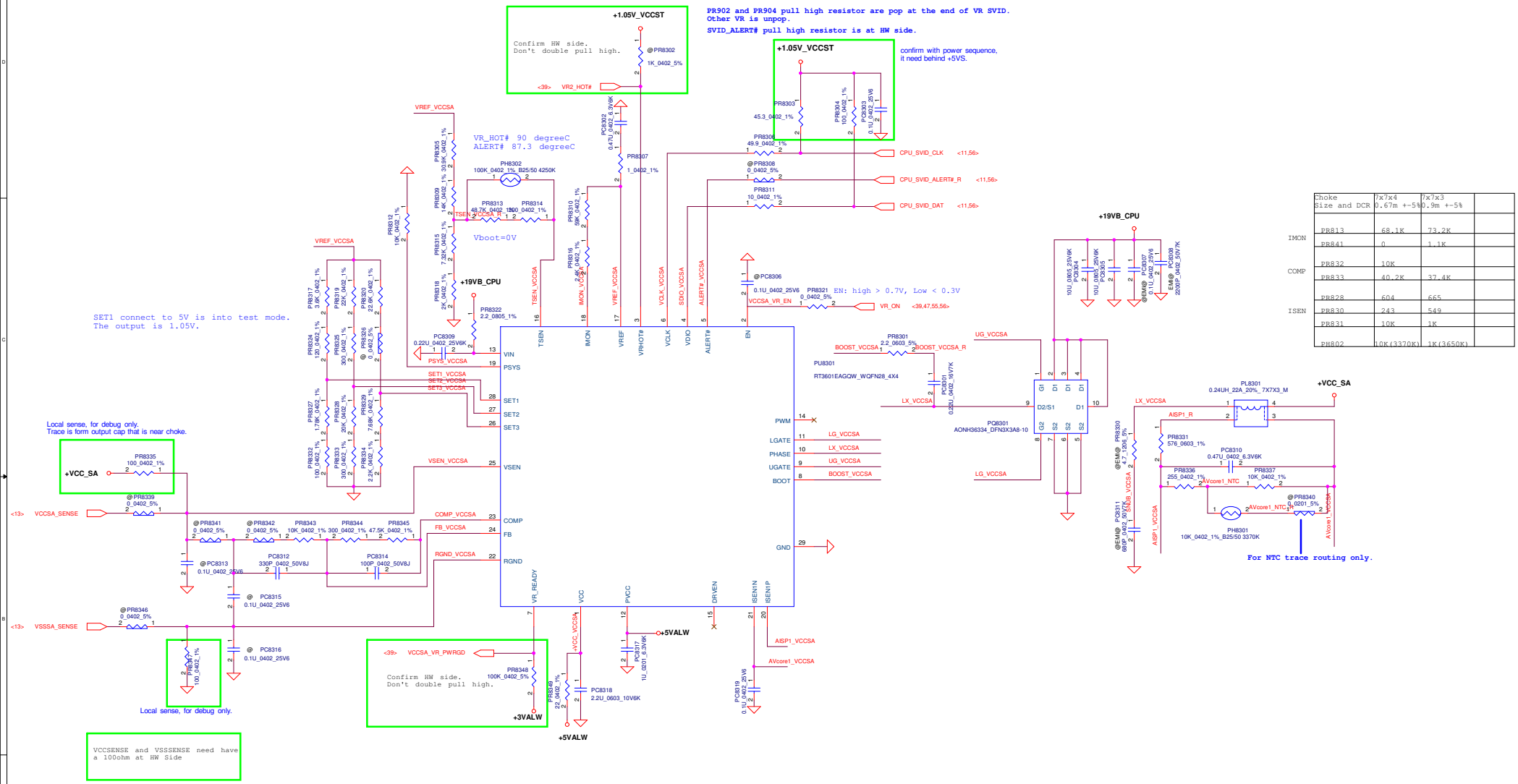
Title	RT3607CE		
Size	Document Number		Rev
Custom			0.1
Date: Thursday, February 22, 2018	Sheet 56 of 67		

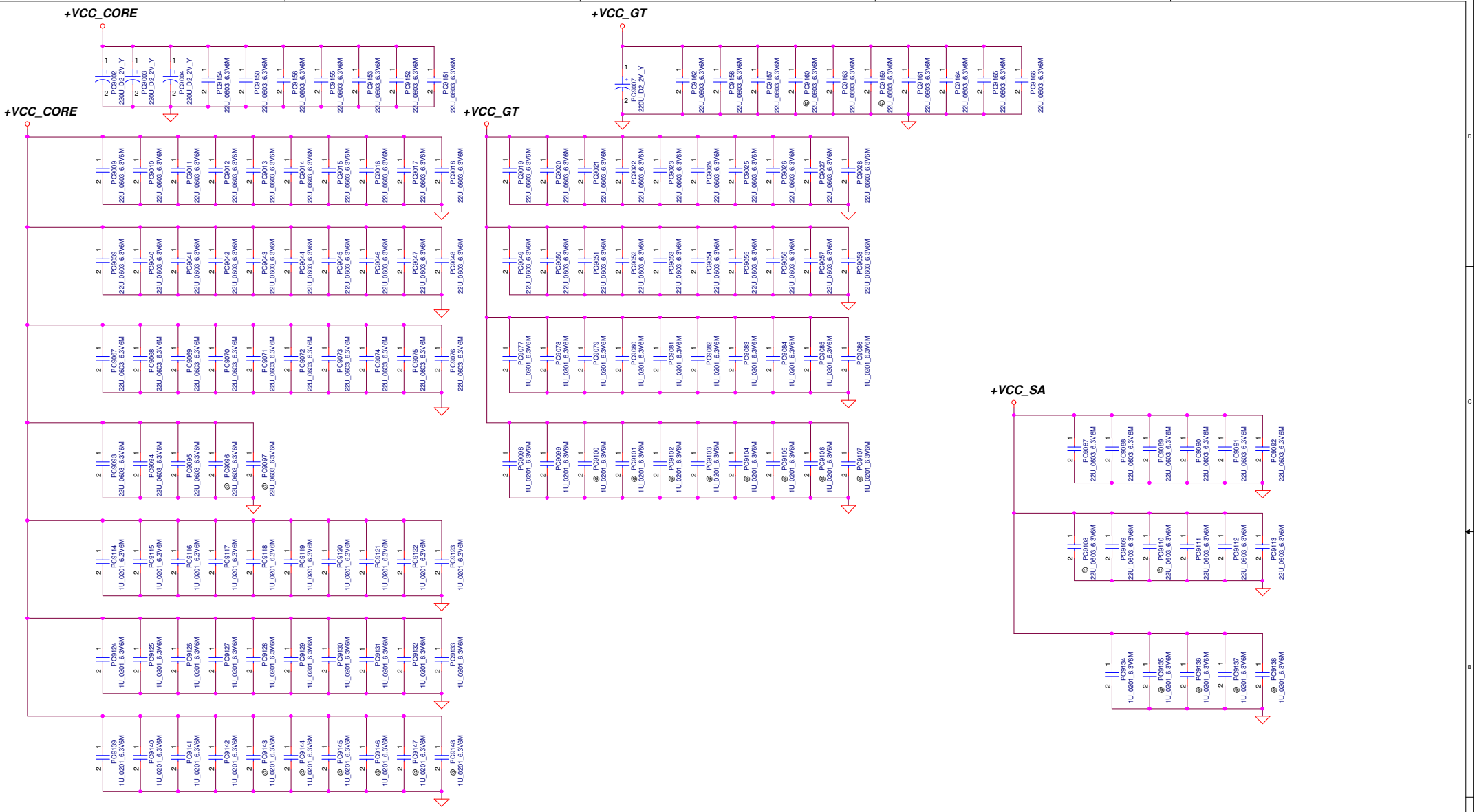


Choke Size and DCR	7x7x4 0.67m +-5%	7x7x3 0.9m +-5%	
IMON PR813	68.1K	73.2K	
IMON PR841	0	1.1K	
COMP PR832	10K		
COMP PR833	40.2K	37.4K	
ISEN PR828	604	665	
ISEN PR830	243	549	
ISEN PR831	10K	1K	
PH802	10K(3370K)	1K(3650K)	

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Title: RT3601EA VCC_SA

Size: Custom	Document Number	Rev: 0.1
Date: Thursday, February 22, 2018	Sheet 57 of 67	



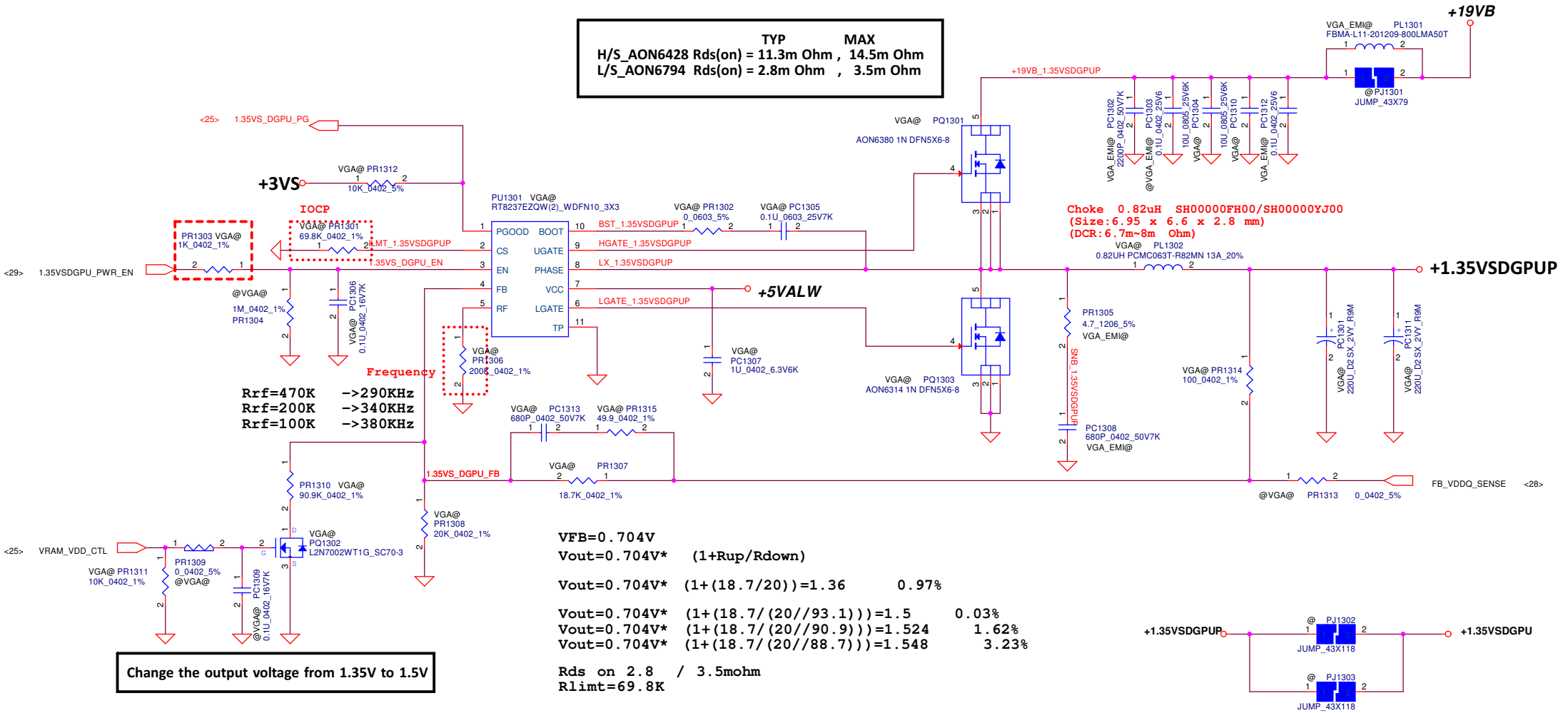
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: C5MMH M/B LAE911P

Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 22, 2018 | Sheet 58 of 67



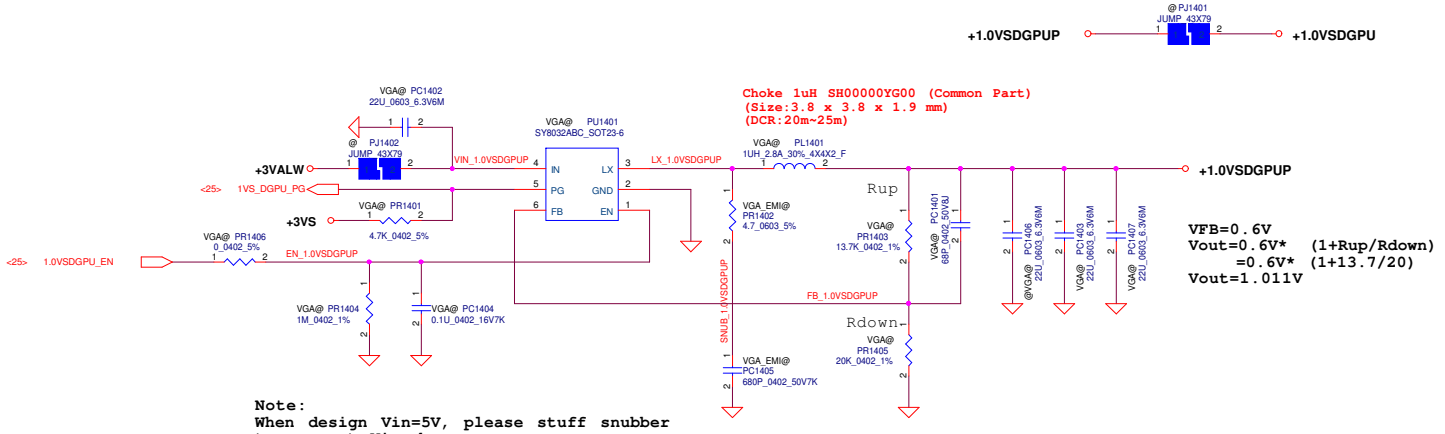
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: VRAM

Size	Document Number	Rev
A3	C5MMH M/B LAE911P	0.1

Date: Thursday, February 22, 2018 Sheet 59 of 67

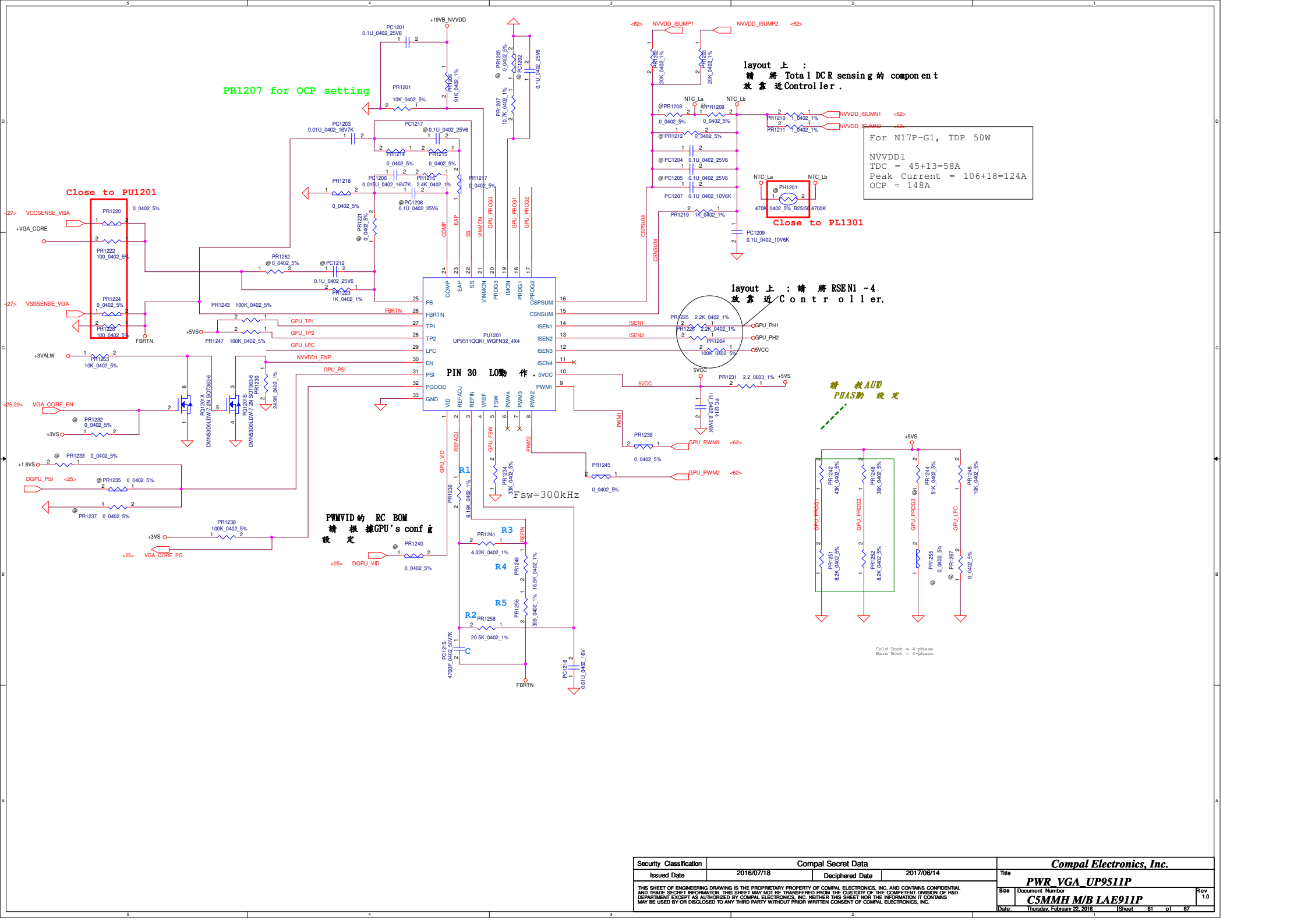


Compal Electronics, Inc.

Title: 1.05VSDGPU

Size	Document Number	Rev
C	C5MMH M/B LAE911P	0.1

Date: Thursday, February 22, 2018 Sheet 60 of 67



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

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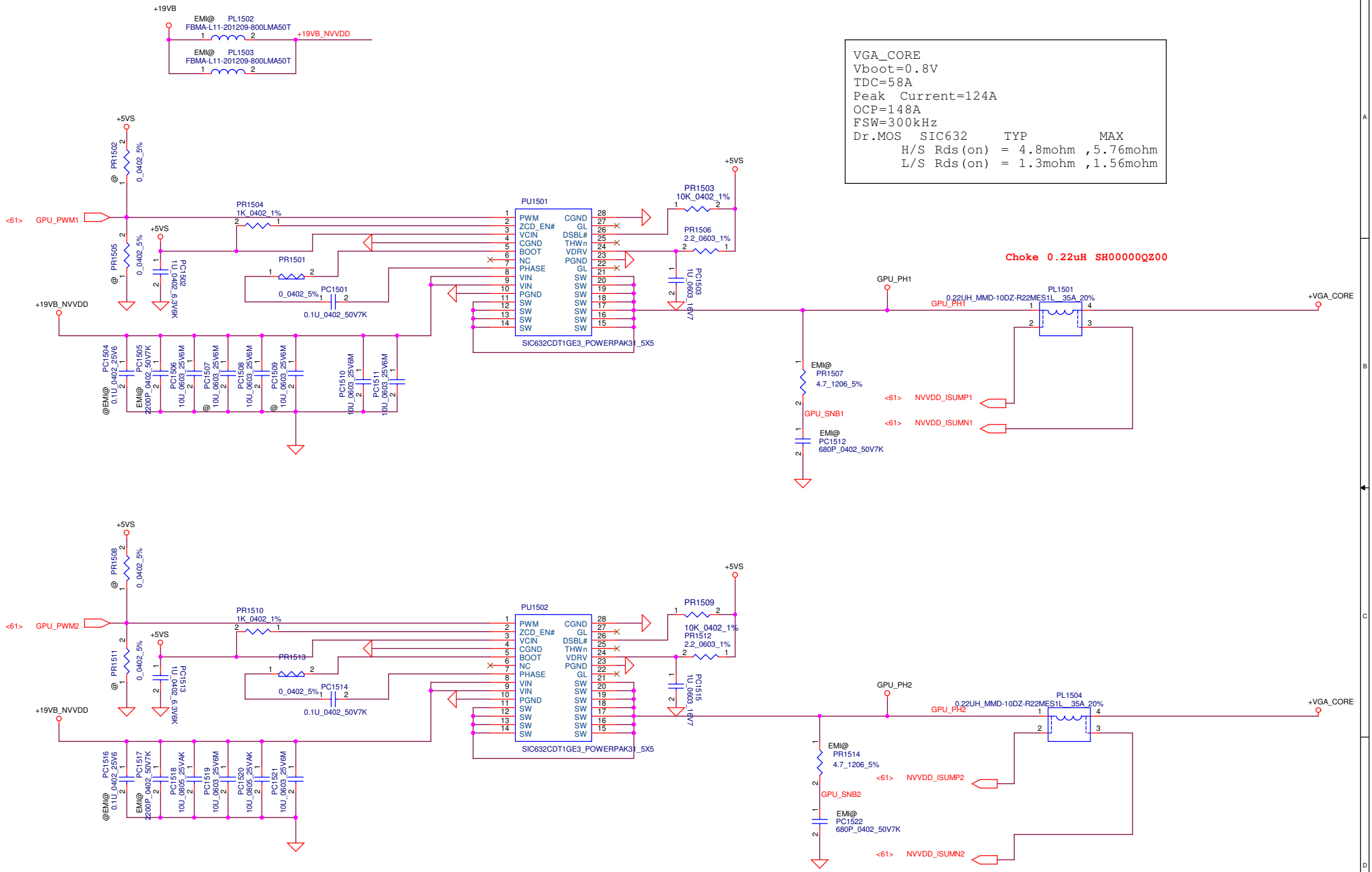
Compal Electronics, Inc.

Title: PWR_VGA_UP9511P

Size: | Document Number: C5MMH M/B LAE911P | Rev: 1.0

Date: Thursday, February 22, 2018 | Sheet 61 of 67



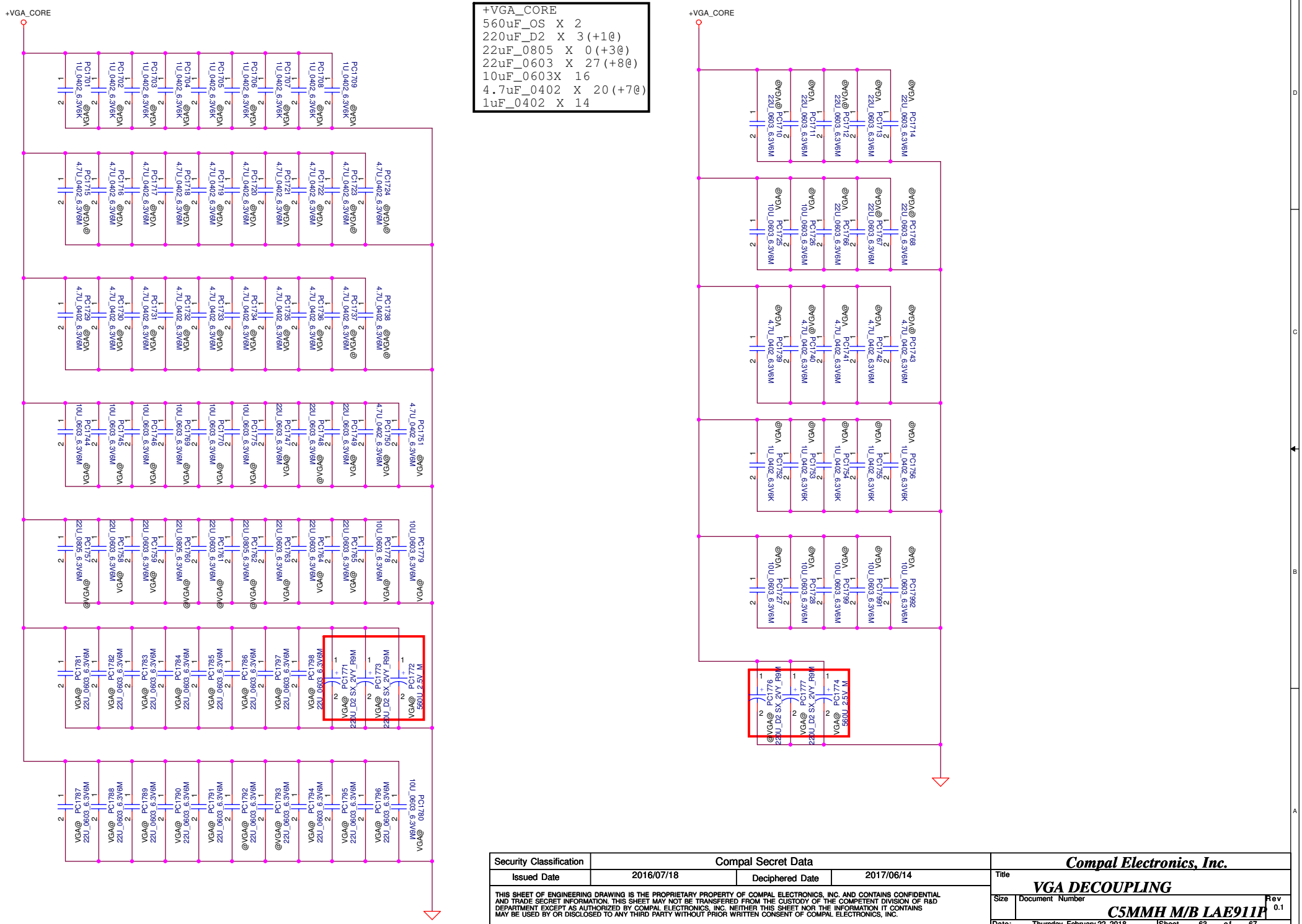
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	C5MMH M/B LAE911P	1.0

Date: Thursday, February 22, 2018 Sheet 62 of 67



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: **VGA DECOUPLING**

Size | Document Number: **C5MMH M/B LAE911P** | Rev: 0.1

Date: Thursday, February 22, 2018 | Sheet 63 of 67

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Solution Change	0.2	50	Change the PQ310 from AON6366E (SB00001D800) to EMB04N03H (SB00001C500). Change the PQ311,PQ312 from AON6366E (SB00001D800) to AON7380 (SB00001GM00). Change the PC302,PC303,PC310、PC311、PC312 from 10U_0603_25V (SE00000X200) to 10U_0805_25V (SE00000QK00). Delete the PC323 10U_0603_25V (SE00000X200).	10/13	A2
02	Design Update	Solution Change	0.2	53	Change the PR603 (10K_0402_1%, SD034100280) from pop to un-pop.	10/13	A2
03	Design Update	Solution Change	0.2	54	Change the PR7126 (100K_0402_5%, SD028100380) from un-pop to pop. Change the PR7126.2 net from +3VS to +3VALW.	10/13	A2
04	Design Update	Solution Change	0.2	63	Change the PC1748,PC1761、PC1770、PC1772、PC1767、PC1768 (22U_0603_6.3V, SE00000M000) from pop to un-pop.	10/13	A2
05	Design Update	Down size for SNB MLCC	0.2	50、59、62	Change the PC315,PC1308,PC1512、PC1512 from 680P_50V_K_X7R_0603 (SE025681K80) to 680P_50V_K_X7R_0402 (SE074681K80).	10/13	A2
06	Design Update	Solution Change	0.2	59	Change the PQ1302 from 2N7002KW (SB000009Q80) to L2N7002WT1G (SB00000ST00).	10/13	A2
07	Design Update	Down size for MLCC	0.2	59	Change the PC1307 from 1U_6.3V_M_X5R_0603 (SE107105M80) to 1U_6.3V_K_X5R_0402 (SE000000K80).	10/13	A2
08	Design Update	Down size for EMI MLCC	0.2	48	Change the PC102 from 100P_50V_J_NPO_0603 (SE024101J80) to 100P_50V_J_NPO_0402 (SE071101J80). Change the PC104 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80).	10/13	A2
09	Design Update	Down size for MLCC	0.2	63	Change the PC1747,PC1759,PC1749、PC1758、PC1764、PC1766、PC1768 from 22U_6.3V_M_X5R_0805(SE000000I10) to 22U_6.3V_M_X5R_0603 (SE00000M000).	10/13	A2
10	Design Update	Solution Change	0.2	56	Change the PH8103,PH8104 from 150K_5%_0402_B25/50_4500K (SL200002K00) to 220K_5%_0402_B25/50_4700K (SL200002I00). Change the PR8109,PR8110 from 8.87K_0402_1%(SD034887180) to 8.66K_0402_1%(SD034866180). Change the PR8118,PR8119 from 931K_0402_1%(SD034931280) to 57.6K_0402_1%(SD034576280).	10/23	A2
11	雷雕區	Down size for Jump	0.2	53	Change the PJ602 from 43X79 to 43X39.	10/23	A2
12	Design Update	Solution Change	0.2	56、57	Change the PC8113,PC8124,PC8310、PC8359、PC8118 from 0.47U_16V_Z_Y5V_0402 (SE000002F80) to 0.47U_6.3V_K_X5R_0402 (SE124474K80). Change the PC8310 from 0.47U_25V_K_X5R_0402 (SE00000WA00) to 0.47U_6.3V_K_X5R_0402 (SE124474K80).	10/25	A2
13	Design Update	Solution Change	0.2	58	Add the location PC9164,PC9165,PC9166 and pop, 22U_6.3V_M_X5R_0603 (SE00000M000)	10/26	A2
14	Design Update	CPU transient test result	0.2	56、57、58	Change the PR8114 from 6.81K_0402_1% (SD034681180) to 5.76K_0402_1% (SD034576180). Change the PR8113 from 2.49K_0402_1% (SD034249180) to 1.8K_0402_1% (SD00000R580). Change the PR8117 from 560K_0402_1% (SD034560380) to 442K_0402_1% (SD034442300). Change the PR8116 from 510K_0402_1% (SD00000RK80) to 402K_0402_1% (SD034402380). Change the PR8141 from 100_0402_1% (SD034100080) to 8.2K_0402_1% (SD000004100). Change the PR8149 from 1.05K_0402_1% (SD00000J480) to 3.16K_0402_1% (SD000006580). Change the PR8176 from 20K_0402_1% (SD034200280) to 16.9K_0402_1% (SD034169280). Change the PR8310 from 63.4K_0402_1% (SD03463K280) to 59K_0402_1% (SD034590280). Change the PR8319 from 24.9K_0402_1% (SD034249280) to 22K_0402_1% (SD034220280). Change the PR8325 from 0_0402_5% (SD028000080) to 300_0402_1% (SD034300080). Change the PR8328 from 22K_0402_1% (SD034220280) to 20K_0402_1% (SD034200280). Change the PR8333 from 680_0402_1% (SD034680080) to 300_0402_1% (SD034300080). Change the PC8312 from 270P_0402_50V7K (SE074271K80) to 330P_0402_50V8J (SE000006I80). Change the PR8331 from 470_0603_1% (SD014470080) to 576_0603_1% (SD014576080). Change the PR8336 from 42.2_0402_1% (SD00000ZN00) to 255_0402_1% (SD034255080). Change the PR8134 from 121K_0402_1% (SD034121380) to 13.3K_0402_1% (SD034133280). Change the PR8138 from 49.9K_0402_1% (SD034499280) to 26.7K_0402_1% (SD034267280). Change the PR8147 from 3.32K_0402_1% (SD034332180) to 768_0402_1% (SD00000TT80). Change the PC9110,PC9108 from 22U_0603_6.3V6M (SE00000M000) to un-pop Change the PC9112,PC9113 from un-pop to 22U_0603_6.3V6M (SE00000M000). Change the PC8126 from 330P_0402_25V8J (SE00000FD80) to 330P_0402_50V8J (SE000006I80). Change the PR8173 from 0_0603_5% (SD013000080) to 10_0603_1% (SD014100A80). Change the PC8137 from 330P_0402_25V8J (SE00000FD80) to 270P_0402_50V7K (SE074271K80). Change the PC9159,PC9160 from 22U_0603_6.3V6M (SE00000M000) to un-pop Change the PC9057,PC9058 from un-pop to 22U_0603_6.3V6M (SE00000M000).	10/27	A2
15	Design Update	Power sequence	0.2	59、60	Change the PR1303 from 10K_0402_1% (SD034100280) to 1K_0402_1% (SD034100180). Change the PR1401 from 10K_0402_5% (SD028100280) to 4.7K_0402_5% (SD028470180).	11/02	A2
16	Design Update	Solution Change	0.2	61	Change the PU1201 from UP9511P (SA00009SW00) to UP9511Q (SA0000BK300). Change the PR1243,PR1247 from 10K_0402_5%(SD028100280) to 100K_0402_5%(SD028100380).	11/08	A2
17	Design Update	Solution Change	0.2	52、56、57	Change the PC8317,PC509,PC517 from 1U_0402_10V6K(SE00000QL10) to 1U_0201_6.3V6K (SE00000YB00). Change the PC8112,PC8115,PC8132、PC8139、PC8157、PC8161 from 1U_0402_25V6K (SE00001QV00) to 1U_0201_6.3V6K (SE00000YB00).	11/08	A2
18	Design Update	Solution Change	0.2	50、56	Change the PR340,PQ314,PQ312、PQ313、PR327,PR307、PQ308 from pop to un-pop. Change the PR326 from un-pop to 0_0603_5% (SD013000080) Change the PR310 from 51.1K_0402_1% (SD034511280) to 52.3K_0402_1% (SD034523280) Change the PC8147 from 10U_0805_25V_X5R (SE00000QK00) to un-pop	11/14	A2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
19	Design Update	Solution Change	1.0	50	Change the PC313 PC314 from 1U_16V_X5R_0402(SE00000OU00) to 1U_63V_X5R_0201(SE00000YB00).	12/15	C
20	Design Update	Solution Change	1.0	50、55 56、57	Change the PR304 PR314 PR316、PR332、PR334、PR8111、PR8120、PR8128 PR8139 PR8142、PR8143、PR8153、PR8154、PR8155 PR8165 PR8170、PR8175、PR8190、PR8129、PR8163、PR8184 PR8198 PR8204、PR8208、PR8226、PR8339、PR8341 PR8342 PR8346、PR8347、PR333 from 0_0402_5%(SD028000080) to R-short	12/15	C
21	Design Update	Solution Change	1.0	50	Change the PC305 PC324 from 01U_0402_25V7K(SE00000W210) to 01U_0402_25V6(SE00000G880).	12/18	C
22	Design Update	Solution Change	1.0	56	Change the PC8101 PC8122 PC8155、PC8150、PC8158 from 0.1U_0603_50V7K(SE025104K80) to 0.1U 25V K X7R 0603 (SE042104K80).	12/18	C
23	Design Update	SW2 un-pop	1.0	49	Change the PR217 from un-pop to 0_0402_5%(SD028000080).	12/18	C
24	Design Update	Solution Change	1.0	50	Change the PR326 PR7202 from 0_0603_5%(SD013000080) to R-short	12/18	C
25	Design Update	Solution Change	1.0	56	Add PC8116 PC8118 33U_D1_25V M_R6 M(SGA0000A400), and un-pop	12/19	C
26	Design Update	4S_BATT	1.0	50	Delete location PR326 PR327 PQ307、PQ308 Add location PR338->2M_0402_1%(SD034200480) PR339->100K_0402_1%(SD034100380) Add location PQ315->LTC015EUBFS8TL(SB000011K00) PQ316->2N7002K W1 N SOT323-3(SB00000ST00)	12/20	C
27	Design Update	Solution Change	1.0	50	Change the PC309 from 0.22U_0603_25V(SE000005Z80) to 0.47U_0402_16V(SE000002F80).	12/21	C
28	Design Update	ACIN_CHG	1.0	50	Change the PR306 from 392K_0402_1%(SD034392380) to 499K_0402_1%(SD034499380). Change the PR310 from 52.3K_0402_1%(SD034523280) to 66.5K_0402_1%(SD034665280).	12/25	C
29	Design Update	Power sequence	1.0	60	Change the PR1406 from 10K_0402_1%(SD034100280) to 0_0402_5%(SD028000080).	12/27	C
30	Design Update	3valw interfere	1.0	55、59	Change the Jump PJ7202 PJ1301 from short to open Change the bead PL7201 PL1301 from un-pop to pop 0805_5A(SM01000U600). Change the PR7203 from un-pop to pop 4.7_1206_5% (SD001470B80) Change the PC7203 from un-pop to pop 680pF_0402_50V (SE074681K80)	01/10	C
31	Design Update	Solution Change	1.A	55	Change the PR7202 from R-short to 0_0603_5%(SD013000080).	01/12	C

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	29	Design Update	9/27	power source optimization	DGPU1.8V power source change to 1.8VALW	A2	0.2
2	39	Design Update	9/27	version upgrade	Change board ID to DVT (V15_ID1/VX15_ID11)	A2	0.2
3	37	Design Update	10/17	CNVI power request	Add RM44 for +3VALW to +3VS_WLAN	A2	0.2
4		Design Update	10/19	0 ohm part count reduce	RH186/RH47/RH103/RH105/RH97/RH98/RH99/RH100/ RD3/RD6/RD2/RD15/RD13/RD17/RM22/RM23/RM24/ RM25/RM26/RM27/RM28/RM29/RM30/RM31/RM32/ RM33/RM34/RM35/RM38/RM39/RM40/RS1/RS8/RS16/ R19/R20/RQ5/RQ9/RQ6	A2	0.2
5	41,42	Design Update	10/19	USB common voltage footprint update	LS1/LS10 change footprint to "MURAT_DLM0NSN900HY2D_4P"	A2	0.2
6		Design Update	10/24	for cost, change 10uF_0402 to 0603	CV75, Cv83, CV86, Cc88, CV87, Cv83, Cv73, Cv82,Cv108, Cv119, Cv118, Cv110, Cv120, Cv121, Cv114, Cv115 , CC75, Cc73, Cc80, CC74,CC76, CC78, CC79, CX1 CX3, CA6, CA8, CA9, CA16, CA17, CC71, CC72, CC81, CC89, CC90,	A2	0.2
7	44	Design Update	10/25	USB CMC move to M/B	add L11/ L12 for USB2.0 CMC	A2	0.2
8	39	Design Update	10/26	CNVI device detact issue	add PU 100K RB78 for CNVI card detect reserved RB79 PD 0ohm for CNVI card detect EC add PIN89 GPIO50 as CNVI_DET# add PIN 19 CNVI_DET#	A2	0.2
9	38	Design Update	10/26	for reserve 4 dmic	Change JDMIC1 to 4pin : SP02000TI00	A2	0.2
10	43	Design Update	11/02	SATA HDD redriver EQ tuning	UNPOP RO17 for redriver EQ	A2	0.2
11	25	Design Update	11/02	NV vga sequence tuning	change RV105 to 8.2K (vga_core_en) RV12 change to 100k_1% (1.35VSDGPU_PWR_EN) RV113 change to 4.7k_5% PR1303 change to 1k PR1401 change to 4.7k	A2	0.2
12	43	Design Update	11/06	co-lay no HDD re-driver circuit	add CO14/CO16~18/RO21~24 for no re-driver.	A2	0.2
13	45	Design Update	11/13	for factory request, don't include SW1 in bom	unpop SW1 and control by SMT memo	A2	0.2
14	40	Design Update	11/13	replace level shift by 0 ohm on Type-C circuit	unpop QS1/RS107/RS108 POP RS114/RS115	A2	0.2
15		Design Update	11/13	fine tune crystal frequency	24Mhz Keep 33 18 /1M 25Mhz Keep 10 18 /330 27Mhz CV1 change to 15PF (15 12 /0) 32.768Khz change CH7/CH8 to 10PF (10 10 /10M)	A2	0.2
16		Design Update	12/14	0 OHM change to R-short	change RC17/RH5/RH6/RH94/RH96/RV125/RM2/RB19/RB76/RO4 /RS114/RS115 to R-short	PVT	1.0
17	18	Design Update	12/14	peci issue, can't get system temperature	UNPOP RH41	PVT	1.0
18	46	Design Update	12/14		unpop SW2(BI SW)	PVT	1.0
19	39	Design Update	12/16		channge board ID to ver1.0 (V series 15k/ vx series 200k)	PVT	1.0
20	40	Design Update	12/18	change typeC VCONN sol to G527	add RS116 on VBUS_EN_179 change US2 to SA00006Y700, add RS156/RS155/CS101/CS124	PVT	1.0

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
21	37	Design Update	12/18	BT lost issue	reserve RM45 for pull up BT_ON to +3VS_WLAN	PVT	1.0
22	25	Design Update	12/20	vga sequence tuning	change RV105 to 6.2k / RV103 to 24.9k	PVT	1.0
23	21	Design Update	12/20	intel sensitive net	pop CH29 & CH34	PVT	1.0
24	45	Design Update	12/21	intel ECN_Update	Change RS64,RS65,RS74,RS76,RS82~RS85 to 0201 size. Add CS102~CS105,RS119~RS122.	PVT	1.0
25	37 21	Design Update	12/22	CNVI lost issue	reserve CM18 on CNV_RF_RESET# add CH52 0.1U on +1.8VALW_PRIM	PVT	1.0
26	37 21	Design Update	12/26	CNVI lost issue	reserve CM19 4.7uF on +3VS_WLAN reserve CH53_10uF on +1.8VALW_PRIM change RH100 R-short to 0_0603	PVT	1.0
27	38	Design Update	12/26	charmeleon down z-high on wi-fi card area	change CA6/CA17 to 0402 package	PVT	1.0
28	32	Design Update	12/26	improve HDMI layout	remove GPAK circuit for improve HDMI layout del U18/CV225/RV126/RV125/CG341/CG342	PVT	1.0
29	18, 35	Design Update	01/11	improve optone layout for HM370	change PCIE port from 17-20 to 12-9 change from SSD_DEVSLP4 to SSD_DEVSLP1 change from SATA_GP4 to SATA_GP1	PVT	1A
30	18	Design Update	01/11		HDD port change to SATA0B	PVT	1A
31	32	Design Update	01/11		JTYPEC1.A2/A3/B2/B3 change to NET NAME	PVT	1A
32	7	Design Update	02/22	change PN for MP chip	UC1/UH1/UV1/ change to MP part number	PVT	1A
33	19	Design Update	02/22	PVT memo improve	POP RH183 Remove CQ7/CQ8	PVT	1A

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