LLA-1 17833 Gemini Lake Schematics

PCB P/N: 17833

REV : -1M

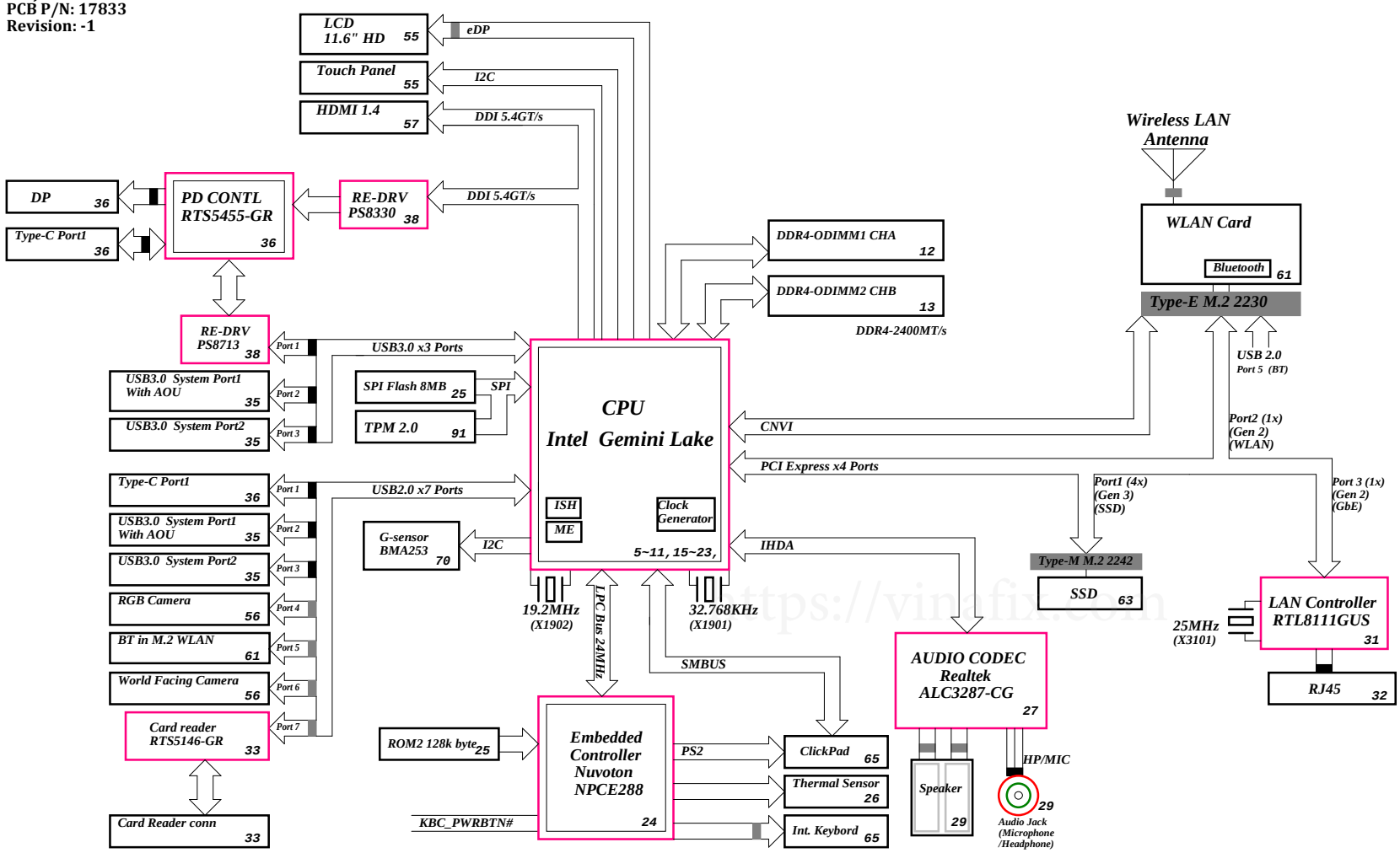
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***		
Size: A4	Document Number: **Leia**	Rev: **-1M**
Date: Thursday, December 28, 2017	Sheet 1 of 104	

Gemini Lake Board Block Diagram

Project code: 4PD0DA010001
PCB P/N: 17833
Revision: -1



CHARGER BQ25700ARSNR 44	
INPUTS	OUTPUTS
19V_DCBATOUT	BT+

SYSTEM DC/DC TPS51225BRUKR 45	
INPUTS	OUTPUTS
19V_DCBATOUT	5V_S5 3D3V_S5

CPU PMIC BD2671 46	
INPUTS	OUTPUTS
19V_DCBATOUT	1D8V_S5 1D2V_S5 1D05V_S0

SYSTEM DC/DC BD2671 47	
INPUTS	OUTPUTS
5V_S5	1V_CPU_VCGI

DDR4 BD2671 50	
INPUTS	OUTPUTS
5V_S5	1D2V_S3

DDR4 PMIC BD2671 51	
INPUTS	OUTPUTS
3D3V_S5	2D5V_S3

SYSTEM Load switch G2898KD1U 40	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0

PCB Layer Stackup

L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND/VCC
L6:Bottom

IOBD

PWR Board
- Power Button — KBC_PWRBTN#

SENSOR Board
- Hall sensor
- G-sensor BMA253 — I2C

WIFI Board
- WIFI LED*3

Active Pen 66 — Power (3.3V)

External Connector/Socket
Internal Connector/Socket
Internal Switch

<Variant Name>

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Title: Block Diagram
Size: A2 | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 2 of 104

SSID = CPU

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***CPU (Reserved)***

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 3 of 104

SSID = CPU

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (Reserved)***

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 4 of 104

SSID = CPU

CPU1A — 1 OF 13 — DDR4_LP3_LP4 — DDR0

CPU1B — 2 OF 13 — DDR4_LP3_LP4 — DDR1

GEMINI-LAKE-GP

SB 0619 ODT0 (pin BB39) del

SB 0619 ODT0 (pin BC8) del

SB 0619 DY

DY

Del off page and add TP

#567247 #82 Figure 5-1 system memory resistive compensation

Vinafix.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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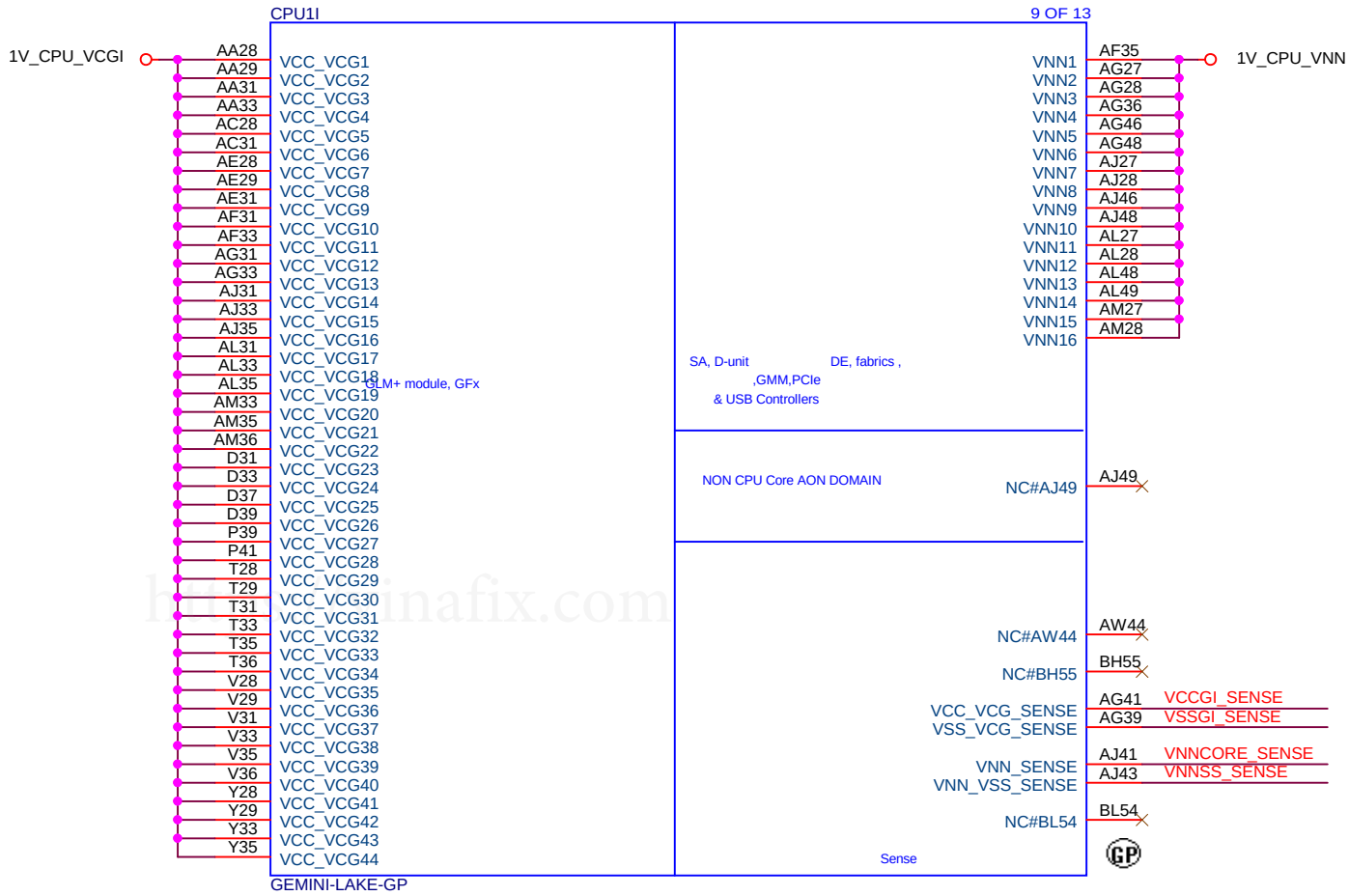
Title: CPU (DDR)

Size: Custom | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 5 of 104

SSID = CPU PDG P54

47 VSSGI_SENSE
47 VCCGI_SENSE
50 VNNCORE_SENSE
50 VNNSS_SENSE



<Variant Name>

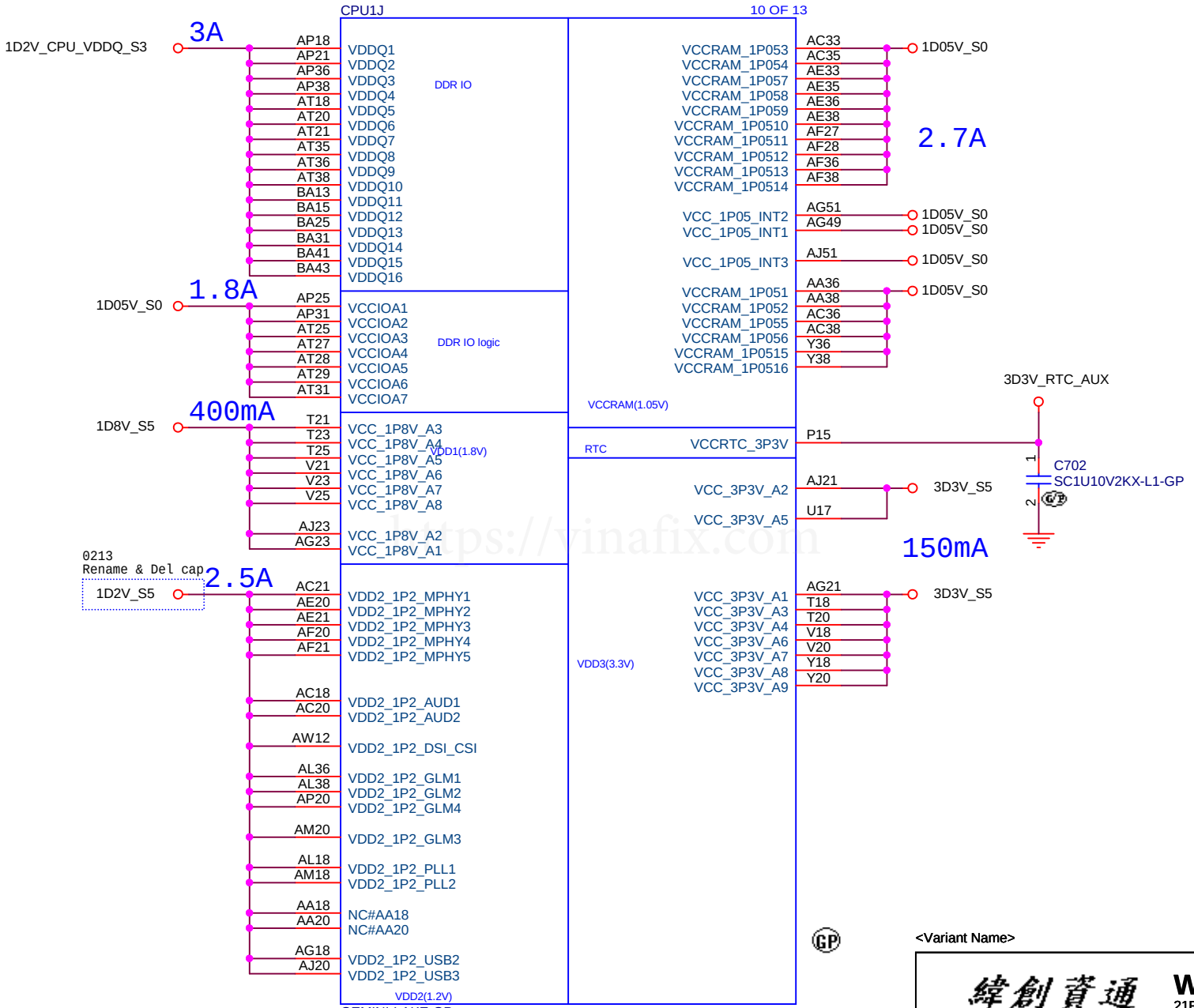
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VCCGI/VNN/Others)***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 6 of 104

SSID = CPU



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VDDQ/VCCIO/Others)**

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 7 of 104

SSID = CPU

DP

38 DDI0_TX_P0
38 DDI0_TX_N0
38 DDI0_TX_P1
38 DDI0_TX_N1
38 DDI0_TX_P2
38 DDI0_TX_N2
38 DDI0_TX_P3
38 DDI0_TX_N3
38 DDI0_AUX_CPU_N
38 DDI0_AUX_CPU_P
38 DDI0_HPD_CPU

HDMI

57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_DET_CPU

EDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
24 eDP_BLEN_CPU
55 eDP_VDDEN_CPU
55 eDP_HPD_CPU
55 eDP_BLCTRL_CPU

99 GPIO43_DSI_TE2
15 GPIO42_FLASH_OVR
24 ME_UNLOCK

CPU1C — 3 OF 13

DP
DDI0_TX_P0 AH1
DDI0_TX_N0 AH3
DDI0_TX_P1 AE2
DDI0_TX_N1 AE3
DDI0_TX_P2 AJ2
DDI0_TX_N2 AJ3
DDI0_TX_P3 AG2
DDI0_TX_N3 AG3
DDI0_AUX_CPU_P AC12
DDI0_AUX_CPU_N AC10
DDI0_HPD_CPU C39
B43
C43
DDI0_TXP_0
DDI0_TXN_0
DDI0_TXP_1
DDI0_TXN_1
DDI0_TXP_2
DDI0_TXN_2
DDI0_TXP_3
DDI0_TXN_3
DDI0_AUXP
DDI0_AUXN
HV_DDI0_HPD
DDI0_DDC_SCL
DDI0_DDC_SDA
DDI0/DDI_B
3D3V_S5
R808 10KR2J-L-GP
ver1.2 0518

HDMI
HDMI_DDI_TX_P0 AA2
HDMI_DDI_TX_N0 AA3
HDMI_DDI_TX_P1 Y3
HDMI_DDI_TX_N1 Y1
HDMI_DDI_TX_P2 AD1
HDMI_DDI_TX_N2 AD3
HDMI_DDI_TX_P3 AC2
HDMI_DDI_TX_N3 AC3
HDMI_SCL_CPU C42
HDMI_SDA_CPU A42
HDMI_DET_CPU C38
AC7
AC5
DDI1_TXP_0
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
DDI1_AUXP
DDI1_AUXN
DDI1_DDC_SCL
DDI1_DDC_SDA
HV_DDI1_HPD
DDI1/DDI_C
3D3V_S0
R809 10KR2J-L-GP
RN802 SRN10KJ-L-GP

EDP
eDP_TX_CPU_P0 AE12
eDP_TX_CPU_N0 AE13
eDP_TX_CPU_P1 AC15
eDP_TX_CPU_N1 AC17
AE10
AE8
AE5
AE7
eDP_AUX_CPU_P W17
eDP_AUX_CPU_N W15
eDP_HPD_CPU# B39
eDP_BLCTRL_CPU_E B41
eDP_BLEN_CPU C40
eDP_VDDEN_CPU_E C41
EDP_RCOMP_P AA5
EDP_RCOMP_N AA7
EDP_TXP_0
EDP_TXN_0
EDP_TXP_1
EDP_TXN_1
EDP_TXP_2
EDP_TXN_2
EDP_TXP_3
EDP_TXN_3
EDP_AUXP
EDP_AUXN
HV_DDI2_HPD
PNL0_BKLCTL
PNL0_BKLTEN
PNL0_VDDEN
EDP_RCOMP_P
EDP_RCOMP#
eDP/DDI_A
R801 100R2F-L-GP-U
1D8V_S0
3D3V_S0
R807 DY R814
eDP_HPD_CPU
Q802 PJA138KA-GP
084.00138.0A31
100KR2J-4-GP
eDP_HPD_CPU#
SC 0713 reserved 3D3V

R812 2K2R2F-GP
R813 2K2R2F-GP
eDP_BLCTRL_CPU_B
eDP_BLCTRL_CPU
eDP_BLCTRL_CPU_E
Q803 LMBT3904LT1G-GP
84.T3904.H11
R815 DY 0R2J-2-GP
SD 0904
R812/R813 change to 64.22015.6DL

R816 2K2R2F-GP
R817 2K2R2F-GP
eDP_VDDEN_CPU_B
eDP_VDDEN_CPU
eDP_VDDEN_CPU_E
Q804 LMBT3904LT1G-GP
84.T3904.H11
R818 DY 0R2J-2-GP
SD 0904
R816/R817 change to 64.22015.6DL

MDSI
MDSI_A_CLKP AL2
MDSI_A_CLKN AM3
MDSI_C_CLKP AG13
MDSI_C_CLKN AG12
MDSI_A_DP_0 AN5
MDSI_A_DN_0 AN7
MDSI_A_DP_1 AJ15
MDSI_A_DN_1 AJ17
MDSI_A_DP_2 AJ7
MDSI_A_DN_2 AJ5
MDSI_A_DP_3 AJ10
MDSI_A_DN_3 AJ12
MDSI_C_DP_0 AG15
MDSI_C_DN_0 AG17
MDSI_C_DP_1 AG8
MDSI_C_DN_1 AG10
MDSI_C_DP_2 AG7
MDSI_C_DN_2 AG5
MDSI_C_DP_3 AE15
MDSI_C_DN_3 AE17
MIPI_I2C_SCL R53
MIPI_I2C_SDA R54
0214 change net name
0214 Adding R811
0216 Adding GPIO 43
GPIO_43 MDSI_C_TE T53 GPIO43_DSI_TE2
GPIO_42 MDSI_A_TE T55 GPIO42_FLASH_OVR
R811 1 2 ME_UNLOCK 0R0402-PAD-1-GP
MDSI_RCOMP AL5
R810 150R2F-4-L-GP
Layout Notes:
layout W/S=10/15mil,
length <1000mil.

GEMINI-LAKE-GP

EDP_TXP[3:0]	O	V1P05	Transmit Signals for eDP*
EDP_TXN[3:0]	O	V1P05	Transmit Complement Signals for eDP*
EDP_AUXP	I/O	V1P05	Display Port Auxiliary Channel for eDP*
EDP_AUXN	I/O	V1P05	Display Port Auxiliary Channel Complement for eDP*
EDP_RCOMP_P/N	I/O	V1P05	This signal is used for pre-driver slew rate compensation.
PNL[0,1]_BKLTCTL	O	V1P8/V3P3	Panel Backlight Brightness Control (for eDP*/MDSI)
PNL[0,1]_BKLTEN	O	V1P8/V3P3	Panel Backlight Enable (for eDP*/MDSI)
PNL[0,1]_VDDEN1	O	V1P8/V3P3	Panel Power Enable (for eDP*/MDSI)
DDI[2:0]_HPD	I	V1P8/V3P3	Digital Display Interface Hot-Plug Detect *Notes:* 1. These are muxed signals and need to be enabled through GPIO programming 2. DDI2 is a dedicated eDP* port. 3. A logic inversion circuit with a mandatory pull up resistor is required on the platform
Note:	I/O Voltage is controlled by Soft Straps. Refer to 'Gemini Lake SoC SPI and Signed Master Image Profile (SMIP) Programming Guide' Rev0.6. (CDI# 571036)		

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CPU (DDI/EDP/MDSI)
Size: Custom | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 8 of 104

SSID = CPU

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (MCSI/Camera)

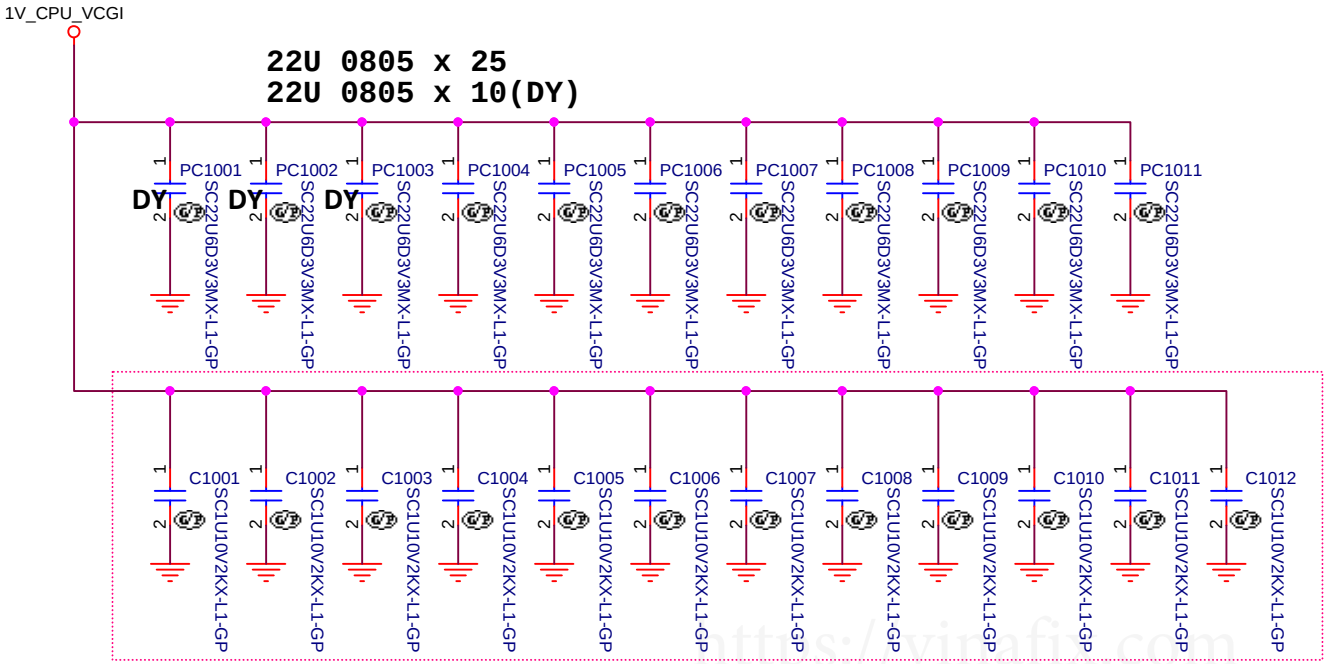
Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 9 of 104

SSID = CPU

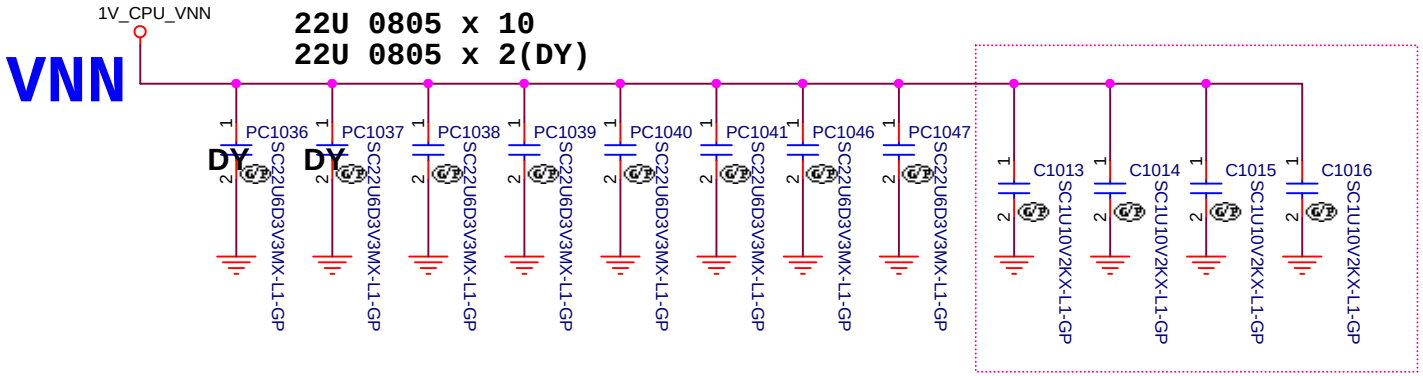
VCCGI

IccMax = 21 A



Vinafix.com

VNN



<Variant Name>

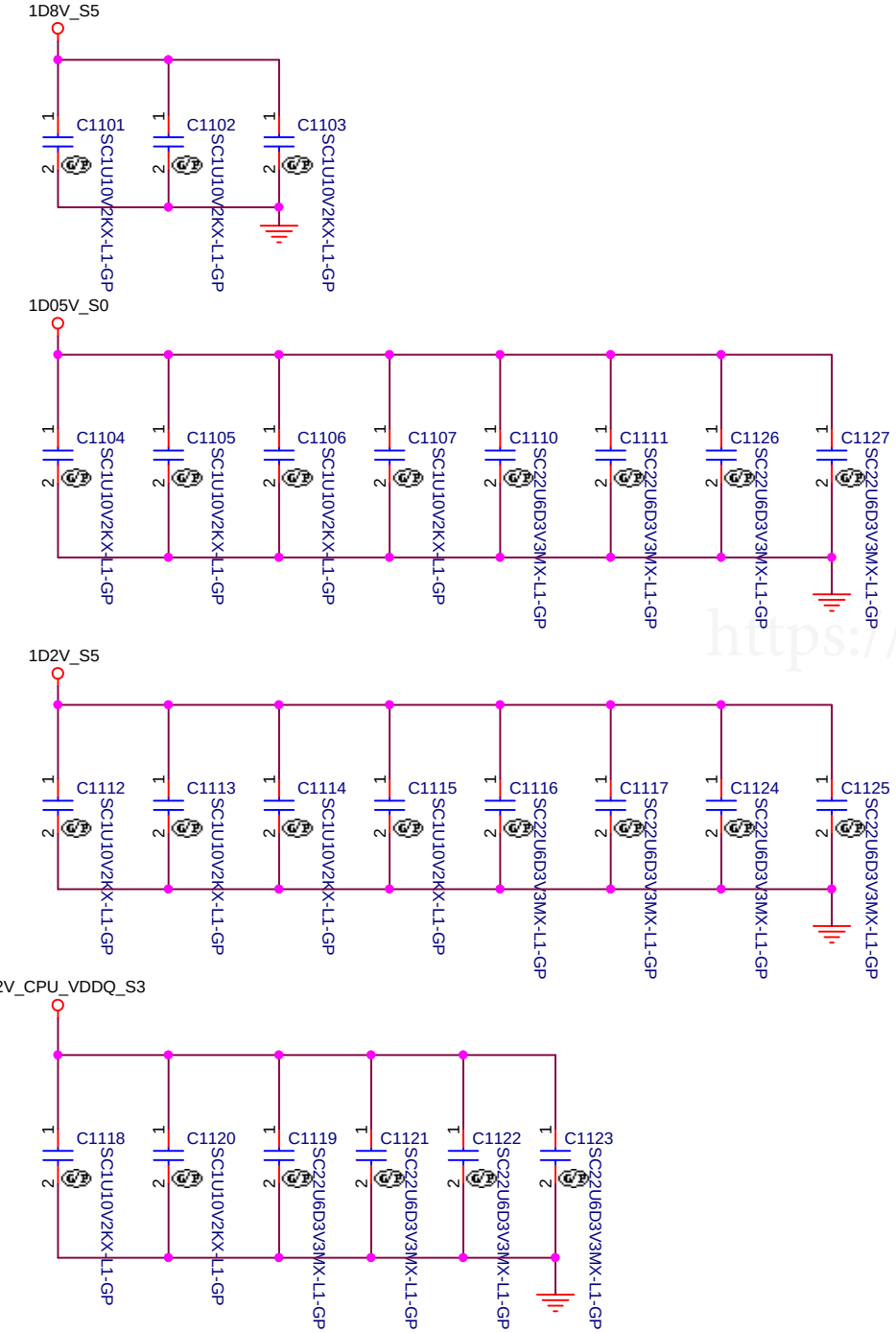
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 10 of 104

SSID = CPU



System Rail Name	Power Balls [GND]	Max L from Ball to nearest BSC [0402-1uF]			Max L from Ball to nearest ESC [0402 - 1uF]			Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF]			Max L / R from Ball to VR Bulk [330uF_9mOhm]		
		Back Side Cap	BSC (nH)	Total (nH)	Top Side Edge Cap	ESC (nH)	Total (nH)	Top Side MLCC	MLCC (nH)	Total (nH)	Top Side Bulk	Bulk (nH)	(mΩ)
VCC_1P8V_A	V21,T25,V25,T23,V23,T21 [Y27,Y25,Y23,Y21,T27,V27,P21] AJ23,AG23[AJ25, AG25]	C417 C438 BSC_USB	1.36 0.714 1.29	0.673									
VCCIOA	AT27,AT28,AT29,AT25,AP31,AT31,AP25 [AM29,AP27,AP28,AP28,AP33,AT33,AP23,AT23,AU28,AM31]	C429 C418	0.475 0.475	0.426	C202 C203	3.72 4.10	3.6	C601 C602	5.12 4.78	4.537			
VDDQ	AP36,AT36,AP38,AT38,AT35,AT18,AP18,AP21,AT20,AT21,BA43,BA41,BA31,BA13,BA15,BA25 [AV39,AR39,AP35,AM38,AT33,AP33,AT23,AR17,AP23,AM23,AM21,AY43,AV33,BC31,AV23,AV17,AV41,AY41,BC25,AY13,AY15]	C412 C428	0.475 0.523	0.223				*C816 *C817 *C820 *C821	2.06 4.10 1.62 3.30	0.496			
VCCRAM_1P05	AC35,AE35,AE38,AE36,AF28,AF27,AF38,AF36,AC33,AE33 [AE27,AF29,AF40,AG38,AJ38,AC29,AA35,AG35,AJ36,AF25]	C424	0.712					C608	2.89				
VCCRAM_1P05_IO	AA36,AA38,Y36,Y38,AC38,AC36 [V38,W39,AF40,W41,T38,AA35]	C405	0.989					C609	3.62				
VDD2_1P24_GLM	AP20,AL38,AL36 [AM21,AR17,AJ38, AJ36]	C415	0.619		C219	1.78		C610 C611	2.10 2.09	1.978			
VDD2_1P24_AUD_ISH_PLL	AM18,AL18 [AJ18, AL17]	C435	0.791					#C823 #C824	1.88 1.88	1.75			
VDD2_1P24_USB2	AJ20,AG18 [AG20, AJ18]	C433	0.747		C217	1.723		C623	2.13				
VDD2_1P24_MPHY	AC21,AE20,AE21,AF20,AF21 [AG20,AF18,AE18,AA23,AC23,AE23,AF23,AA21]	C442	0.667		C218	1.6		C624	2.08				
VDD2_1P24_DSI_CSI	AW12[AW10]							C625	2.22				

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: **CPU (Power CAP2)**

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 11 of 104

DDR4 CHA

SB 0619 49.9->240 ohm

SB 0619 chagne to 34.8 ohm

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

swap for SA layout

072.40512.0A0U

DIMM_CHA_VREFDQ

DDR4 (CHA) On Board RAM Power Decouple Cap For RAM1,RAM2,RAM3,RAM4

VDDQ/VDD 1uF(0402) x 16

VDDQ/VDD 10uF(0603) x 5

VTT 1uF(0402) x 8

VTT 10uF(0603) x 2

VPP 1uF(0402) x 8

VPP 10uF x3

EMI

SC 0710
EC1205 / EC1204 / EC1201 / EC1206 / EC1202 / EC1203 ASM for EMI issue

5-13. DDR4 Memory Down (Double-T) Decoupling Recommendation

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 Memory Down 1x16 (4 device) Each channel	VDD/VDDQ	4 Per DRAM as close as possible to the VDD pins of DRAM	32x 1μF (0402)	2
		Distribute evenly across domain, close by Drams	10x 10μF (0603)	
	Vpp	2 as near each x16 DRAM device as possible	16x 1μF (0402)	2
		Distribute evenly across domain, close by Drams	5x 10μF (0603)	2
	VTT	2 as near each x16 DRAM device as possible	16x 1μF (0402)	2
		Distribute evenly across domain, close by Drams	4x 10μF (0603)	2

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be dependent on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.

<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: DDR (DDR4-DOWN1_CHA)
Size: A1 | Document Number: Leia | Rev: -1M
Date: Thursday, December 26, 2017 | Sheet 12 of 108

DDR4 CHB

SD 0904
Property change from ODIMM to CHB

SB 0619 49.9->240 ohm

SB 0619 chagne to 34.8 ohm

SB 0619 ODT0 PD

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

swap for SA layout

072.40512.0A0U
CHB

DIMM_CHB_VREFDQ

DDR4 (CHB) On Board RAM Power Decouple Cap For RAM5,RAM6,RAM7,RAM8

SD 0904
CHB CAP remove ODIMM property

VDDQ/VDD 1uF(0402) x 16

VDDQ/VDD 10uF(0603) x 5

VTT 1uF(0402) x 8

VTT 10uF(0603) x 2

VPP 1uF(0402) x 8

VPP 10uF x3

5-13. DDR4 Memory Down (Double-T) Decoupling Recommendation

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 Memory Down 1x16 (4 device) Each channel	VDD/VDDQ	4 Per DRAM as close as possible to the VDD pins of DRAM	32x 1uF (0402)	2
		Distribute evenly across domain, close by Drams	10x 10uF (0603)	
	Vpp	2 as near each x16 DRAM device as possible	16x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	5x 10µF (0603)	2
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	4x 10µF (0603)	2

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be dependent on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.

<Variant Name>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-DOWN2_CHB)
Size: Custom
Document Number: Leia
Rev: -1M
Date: Thursday, December 26, 2017
Sheet 13 of 106

SSID = CPU

Blanking

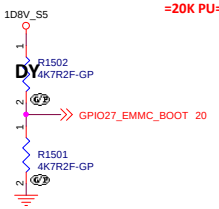
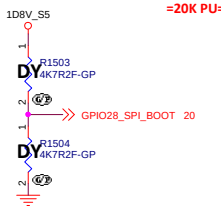
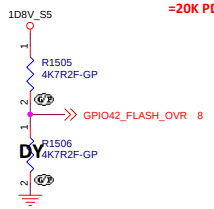
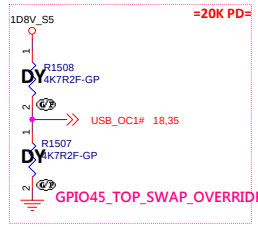
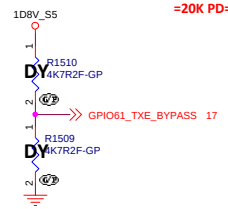
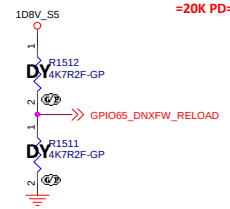
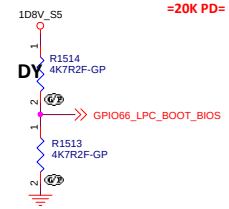
<Variant Name>

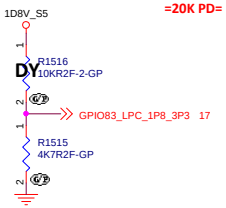
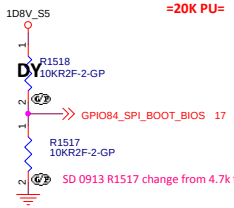
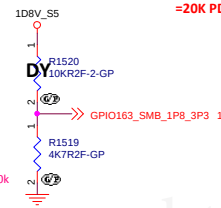
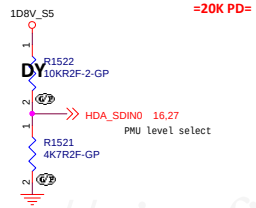
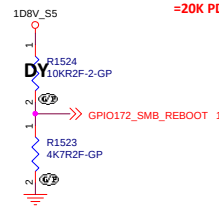
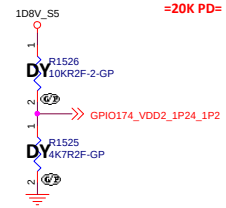
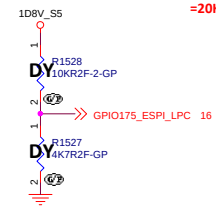
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)SODIMM3_SODIMM4	
Size A4	Document Number Leia	Rev -1M
Date: Thursday, December 28, 2017	Sheet 14 of 104	

HW STRAP

SB 0619 follow rosa

GPIO	GPIO_27	GPIO_28	GPIO_42	GPIO_45	GPIO_61	GPIO_65	GPIO_66
Schematic							
High	Enable =default=	Enable =default=	Override =Normal=	Enable =debug=	Enable	Force	Boot form LPC
Low	Disable	Disable	No Override	Disable =default=	Disable =default=	Not Force =default=	Not form LPC =default=

GPIO	GPIO_83	GPIO_84	GPIO_163	GPIO_168	GPIO_172	GPIO_174	GPIO_175
Schematic							
High	Buffer set 1.8v	Disable boot from SPI	1.8v	1.8v	Enable	1.24v	eSPI mode
Low	Buffer set 3.3v =default=	Enable boot from SPI =default=	3.3v =default=	3.3v =default=	Disable =default=	1.20v =default=	LPC mode =default=

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable ***Note:*** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Notes:*** 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) ***Note:*** The board should strap this low and do not use otherwise
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_163	AVS_I2S1_WS_SYNC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(STRAP)**

Size: Custom | Document Number: Leia | Rev: -1

Date: Thursday, December 28, 2017 | Sheet 15 of 104

SSID = PCH

SPI ROM

25,91 SPI_SI_ROM
25,91 SPI_SO_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
25 SPI_CS_CPU_N0
25,91 SPI_CLK_ROM

EMMC

63 EMMC_RCLK
63 EMMC_CLK
63 EMMC_D0
63 EMMC_D1
63 EMMC_D2
63 EMMC_D3
63 EMMC_D4
63 EMMC_D5
63 EMMC_D6
63 EMMC_D7
63 EMMC_CMD
63 EMMC_RST#

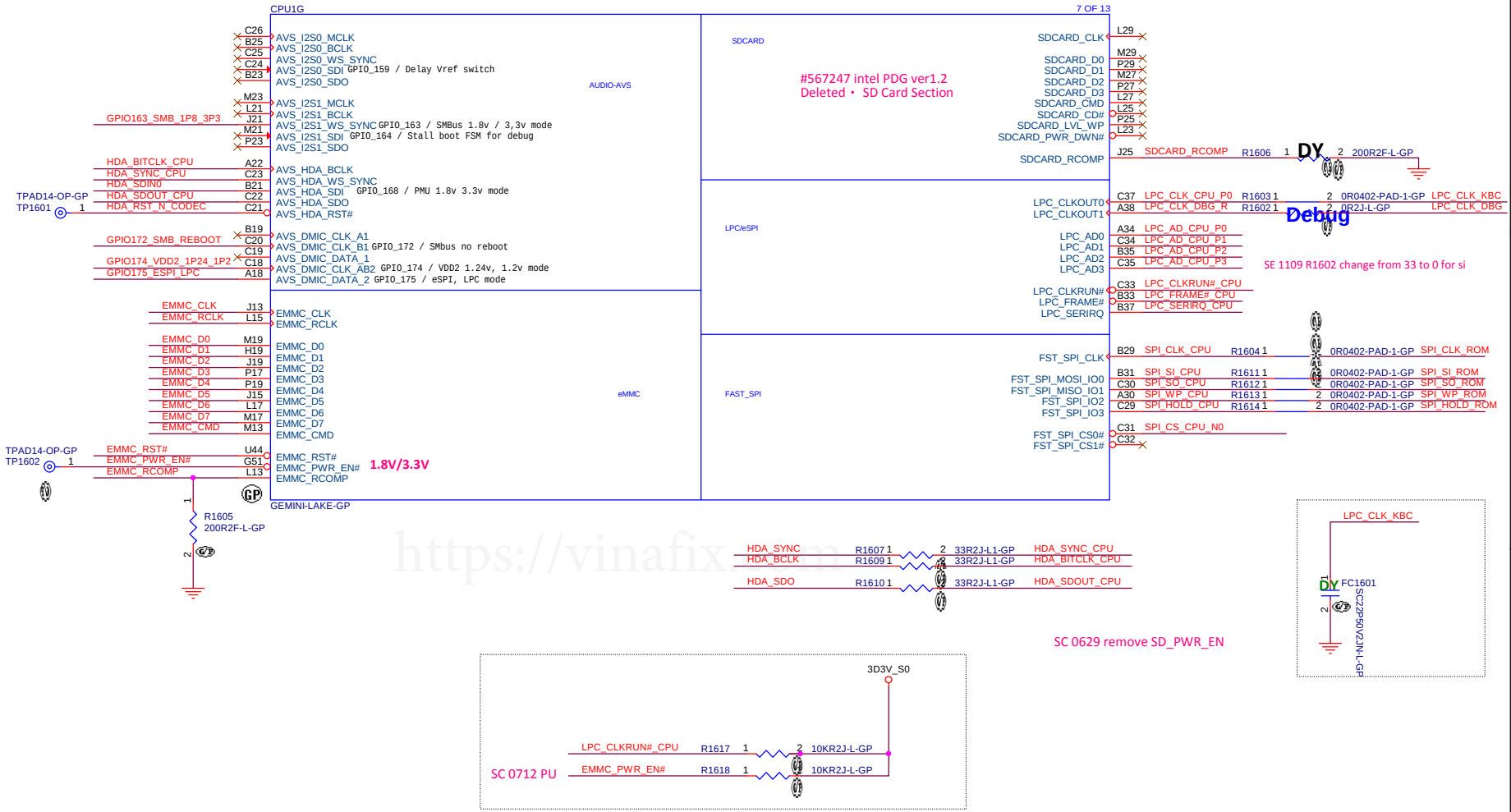
SC 0712
remove EMMC_PWR_EN#

STRAP

15 GPIO163_SMB_1P8_3P3
15 GPIO172_SMB_REBOOT
15 GPIO174_VDD2_1P24_1P2
15 GPIO175_ESPI_LPC

OTHER

24 LPC_CLKRUN#_CPU
24,68 LPC_FRAME#_CPU
24 LPC_SERIRQ_CPU
24 LPC_CLK_KBC
68 LPC_CLK_DBG
24,68 LPC_AD_CPU_P3
24,68 LPC_AD_CPU_P2
24,68 LPC_AD_CPU_P1
24,68 LPC_AD_CPU_P0
27 HDA_SYNC
27 HDA_BCLK
27 HDA_SDO
15,27 HDA_SDIN0



2.8 eMMC* Signals

Table 2-8. Gemini Lake eMMC* Interface Signals

Signal Name	Dir.	I/O Voltage	Description
EMMC_CLK	O	V1P8	eMMC* Clock
EMMC_D[7:0]	I/O	V1P8	**eMMC Port Data bits 0 to 7:** Bi-directional port used to transfer data to and from eMMC* device.
EMMC_CMD	I/O	V1P8	**eMMC Port Command:** This signal is used for card initialization and transfer of commands.
EMMC_RST_N	O	V1P8	**eMMC Reset:** This signal is used to Reset the eMMC* Card ***Note:*** This signal is unused until further update.
EMMC_PWR_N	O	V1P8/V3P3	**eMMC Power Enable:** This signal is used to power cycle the eMMC* Card
EMMC_RCLK	I	V1P8	**eMMC Return Clock:** Return Clock/Data Strobe signal
EMMC_RCOMP	I	V1P8	**eMMC RCOMP:** This signal is used for pre-driver slew rate compensation.
Note:	I/O Voltage is controlled by Hardware Strap(GPIO_168)		

<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AVS/EMMC/SD/LPC/ESPI)
Size: A3 | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 16 of 104

SSID = CPU

Touch panel
55 CPU_I2C_SDA_TS
55 CPU_I2C_SCL_TS

Touch pad/ Reserved PD
36,65,99 CPU_SMB_SCL
36,65,99 CPU_SMB_SDA

G sensor
56,70 CPU_I2C_SCL_P5
56,70 CPU_I2C_SDA_P5

CNVi
61 CNVI_WGR_CLK_P
61 CNVI_WGR_CLK_N
61 CNVI_WGR_DATA_P0
61 CNVI_WGR_DATA_N0
61 CNVI_WGR_DATA_P1
61 CNVI_WGR_DATA_N1
61 CNVI_WT_CLK_P
61 CNVI_WT_CLK_N
61 CNVI_WT_DATA_P0
61 CNVI_WT_DATA_N0
61 CNVI_WT_DATA_P1
61 CNVI_WT_DATA_N1
61 CLKIN_XTAL_LCP
61 XTAL_CLKREQ
61 CNV_BRI_RSP
61 CNV_RGI_RSP
61 CNV_BRI_DT
61 CNV_RGI_DT
61 CNV_RF_RESET#

TPM
91,99 XDP_BOOT_HALT

15 GPIO83_LPC_1P8_3P3
15 GPIO84_SPI_BOOT_BIOS
15 GPIO61_TXE_BYPASS
15 GPIO65_DNXFW_RELOAD
15 GPIO66_LPC_BOOT_BIOS
99 XDP_UART_TXD
99 XDP_UART_RXD

CPU1F
6 OF 13
GEMINI-LAKE-GP
LPSS_I2C
LPSS_SPI
LPSS SMBus
LPSS_UART
CNVi

SC 0630 reserved
Reserved Touch panel
3.3v
1.8V Touch panel
3.3v G sensor
3.3v Touch pad/ Reserved PD
3.3V / 1.8V
DY

CNVi RX for wifi
CNVi TX for wifi
from module
for BT
RF rest to CNVi Module
CNVi Companion RF M.2 module

SD 0911
CPU1F.J29 change from CLKIN_XTAL_LCP to CLKIN_XTAL_LCP_R

SC0628 #567247 p336

SIO_SPI_0_FS1	0	Chip Select 2	Fast SPI Chip select 2 (For TPM)

SD 0913 CPU1F.L37 add R1711 to GND
SD 0913 CPU1F.P33 add R1712 to 1.8v_s5
SD 0913 CPU1F.P37 add R1713 to GND
SD 0913 CPU1F.L54 add R1714 to GND

Close to CPU
SD 0911
add EC1701/ER1701/EL1701/ED1701 for CLKIN_XTAL_LCP (intel suggetion)

-1M 1228 DY ED1701
DY-EMC
075.09904.0A7C

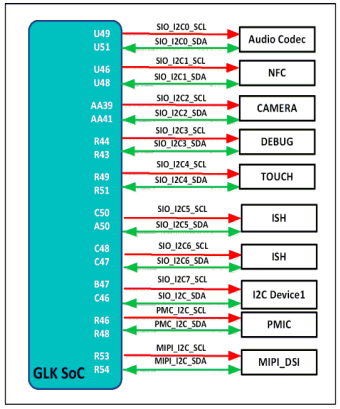
-1M 1211
1. add R1715 between CNV_BRI_RSP & 1D8V_S5
2. add R1716 between CNV_RGI_RSP & 1D8V_S5

For Touch Panel
075.00138.0A7C
75.27002.F7C

SD 0907
Add R1707 /R1710 ,and PU 3D3V_s0

SD 0907
R1705 /R1706 change symbol (4.7K),and DY

Figure 24-1. I²C Interface Topology



To configure the I²C ports, follow the pin muxing options listed out in the Gemini Lake SoC – External Design Specification (EDS).

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (I2C/SMB/SPI/UART/CNVI)
Size: A2 | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 17 of 104

SSID = PCH

USB3.0 port1(AOU)

35 USB1_USB30_TX_P
35 USB1_USB30_TX_N
35 USB1_USB30_RX_P
35 USB1_USB30_RX_N

USB3.0 port2

35 USB2_USB30_TX_P
35 USB2_USB30_TX_N
35 USB2_USB30_RX_P
35 USB2_USB30_RX_N

TypeC

38 USB0_USB30_TX_P
38 USB0_USB30_TX_N
38 USB0_USB30_RX_P
38 USB0_USB30_RX_N

LAN

31 LAN_PCIE_TX_P
31 LAN_PCIE_TX_N
31 LAN_PCIE_RX_P
31 LAN_PCIE_RX_N
31 LAN_CLK_CPU_P
31 LAN_CLK_CPU_N
31 LAN_CLKREQ_CPU_N
31 LAN_WAKE#

WLAN

61 WLAN_PCIE_TX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_RX_N
61 WLAN_CLK_CPU
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N
61 WLAN_WAKE#

M.2 PCIe SSD

63 SSD_CLK_CPU_P
63 SSD_CLK_CPU_N
63 SSD_CLKREQ_CPU_N
63 SSD_PCIE_TX_P0
63 SSD_PCIE_TX_N0
63 SSD_PCIE_RX_P0
63 SSD_PCIE_RX_N0

63 SSD_PCIE_TX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_RX_N1

63 SSD_PCIE_TX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_RX_N2

63 SSD_PCIE_TX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_RX_N3

BT

61 BT_USB20_P
61 BT_USB20_N

RGB camera

56 USB4_USB20_P
56 USB4_USB20_N

World facing camera

56 USB6_USB20_P
56 USB6_USB20_N

Caed reader

33 USB7_USB20_N
33 USB7_USB20_P

USB2.0 Port2

35 USB2_USB20_P
35 USB2_USB20_N

USB3.0 Port1

35 USB1_USB20_P
35 USB1_USB20_N

TypeC

36 USB0_USB20_P
36 USB0_USB20_N

35 USB_OC0#
15,35 USB_OC1#

Layout Notes:
Layout W/S=8/15, length <1000mil

CPU1D — 4 OF 13

R1803 1 — 56R2F-1-GP — 2 PCIE_REF_CLK_RCOMP L10 → PCIE_REF_CLK_RCOMP

PCIe

WLAN
WLAN_CLK_CPU N7 → PCIE_CLKOUT1P
WLAN_CLK_CPU_N N5 → PCIE_CLKOUT1N

LAN
LAN_CLK_CPU_P R7 → PCIE_CLKOUT2P
LAN_CLK_CPU_N R5 → PCIE_CLKOUT2N

SSD_CLK_CPU_P N8 → PCIE_CLKOUT3P
SSD_CLK_CPU_N N10 → PCIE_CLKOUT3N

R12 → PCIE_CLKOUT0P
R10 → PCIE_CLKOUT0N

M.2 PCIe SSD
SSD_PCIE_TX_P0 E2 / SSD_PCIE_TX_N0 F2 → PCIE_P0_TXP / PCIE_P0_TXN
SSD_PCIE_RX_P0 G7 / SSD_PCIE_RX_N0 H6 → PCIE_P0_RXP / PCIE_P0_RXN
SSD_PCIE_TX_P1 A7 / SSD_PCIE_TX_N1 C7 → PCIE_P1_TXP / PCIE_P1_TXN
SSD_PCIE_RX_P1 D4 / SSD_PCIE_RX_N1 E5 → PCIE_P1_RXP / PCIE_P1_RXN
SSD_PCIE_TX_P2 C9 / SSD_PCIE_TX_N2 B9 → PCIE_P2_TXP / PCIE_P2_TXN
SSD_PCIE_RX_P2 E7 / SSD_PCIE_RX_N2 F6 → PCIE_P2_RXP / PCIE_P2_RXN

PDG ver 1.2

PCIE_CLKREQ0# PCIE_CLKREQ1# PCIE_CLKREQ2# PCIE_CLKREQ3#
PCIE_WAKE0# PCIE_WAKE1# PCIE_WAKE2# PCIE_WAKE3#
3.3V / 1.8V

TPAD14-OP-GP TP1802 — WLAN_CLKREQ_CPU_N — R1815 0R0402-PAD-1-GP — WLAN_CLKREQ_CPU_N_R C45
LAN_CLKREQ_CPU_N — R1816 0R0402-PAD-1-GP — LAN_CLKREQ_CPU_N_R B45
SSD_CLKREQ_CPU_N — R1818 0R0402-PAD-1-GP — SSD_CLKREQ_CPU_N_R C44
CARD_CLKREQ_CPU_N A46

TPAD14-OP-GP TP1803 — WLAN_WAKE# — R1802 0R0402-PAD-1-GP — PCIE_WAKE1_CPU D47
LAN_WAKE# — R1807 0R0402-PAD-1-GP — PCIE_WAKE2_CPU F45
TPAD14-OP-GP TP1804 — PCIE_WAKE3_CPU D50
PCIE_WAKE0_CPU F47

SATA
J3 SATA_P0_TXP / J2 SATA_P0_TXN
J7 SATA_P0_RXP / J5 SATA_P0_RXN

SATA/USB3
SATA_P1_USB3_P5_TXP / SATA_P1_USB3_P5_TXN
SATA_P1_USB3_P5_RXP / SATA_P1_USB3_P5_RXN

USB3
USB3_P0_TXP / USB3_P0_TXN
USB3_P0_RXP / USB3_P0_RXN
USB3_P1_TXP / USB3_P1_TXN
USB3_P1_RXP / USB3_P1_RXN

PCIe/USB3
PCIE_P3_USB3_P4_TXP / PCIE_P3_USB3_P4_TXN
PCIE_P3_USB3_P4_RXP / PCIE_P3_USB3_P4_RXN
PCIE_P4_USB3_P3_TXP / PCIE_P4_USB3_P3_TXN
PCIE_P4_USB3_P3_RXP / PCIE_P4_USB3_P3_RXN
PCIE_P5_USB3_P2_TXP / PCIE_P5_USB3_P2_TXN
PCIE_P5_USB3_P2_RXP / PCIE_P5_USB3_P2_RXN

SSIC
NC#AA10 / NC#AA8
NC#W13 / NC#W12
NC#U15

USB2
USB2_DP0 U7 / USB2_DN0 U5
USB2_DP1 N2 / USB2_DN1 N3
USB2_DP2 L2 / USB2_DN2 L3
USB2_DP3 R13 / USB2_DN3 R15
USB2_DP4 M1 / USB2_DN4 M3
USB2_DP5 R2 / USB2_DN5 R3
USB2_DP6 P1 / USB2_DN6 P3
USB2_DP7 U8 / USB2_DN7 U10
USB2_RCOMP U12 — R1805 1 — 2 113R2F-GP

USB2_OTG_ID V1
USB2_VBUS_SNS V3
GPIO_44 / HVM — USB2_OC0# U54
GPIO_45 / Top swap overrided — USB2_OC1# U53
USB_OTG 1 — TP1801 TPAD14-GP — R1804 1 — 2 0R0402-PAD-1-GP

PCIE2_USB3_SATA3_RCOMP# C5 / PCIE2_USB3_SATA3_RCOMP_P C6
PCIE_OBSN_CPU / PCIE_OBSP_CPU — R1801 1 — 2 100R2F-L1-GP-U
Layout Notes:
Diff Layout X-Y-Z=4.5-5.5-20, length<1000mil

GEMINI-LAKE-GP

USB3.0 port2
USB0_USB30_TX_P B15 / USB0_USB30_TX_N C15
USB0_USB30_RX_P F15 / USB0_USB30_RX_N D15
TypeC
USB1_USB30_TX_P C14 / USB1_USB30_TX_N A14
USB1_USB30_RX_P J11 / USB1_USB30_RX_N H11
USB3.0 port1(AOU)
SSD_PCIE_TX_P3 C10 / SSD_PCIE_TX_N3 A10
SSD_PCIE_RX_P3 H9 / SSD_PCIE_RX_N3 F9
M.2 PCIe SSD
WLAN_PCIE_TX_P C11 / WLAN_PCIE_TX_N B11
WLAN_PCIE_RX_P D11 / WLAN_PCIE_RX_N F11
WLAN
LAN_PCIE_TX_P B13 / LAN_PCIE_TX_N C13
LAN_PCIE_RX_P F13 / LAN_PCIE_RX_N D13
LAN
USB2_DP0 U7 / USB2_DN0 U5 — USB0_USB20_P N2 / USB0_USB20_N N3 — TypeC
USB2_DP1 N2 / USB2_DN1 N3 — USB1_USB20_P L2 / USB1_USB20_N L3 — USB3.0 Port1(AOU)
USB2_DP2 L2 / USB2_DN2 L3 — USB2_USB20_P R13 / USB2_USB20_N R15 — USB3.0 Port2
USB2_DP3 R13 / USB2_DN3 R15 — USB4_USB20_P M1 / USB4_USB20_N M3 — RGB Camera
USB2_DP4 M1 / USB2_DN4 M3 — BT_USB20_P R2 / BT_USB20_N R3 — WLAN Combo(Bluetooth)
USB2_DP5 R2 / USB2_DN5 R3 — USB6_USB20_P P1 / USB6_USB20_N P3 — World facing Camera
USB2_DP6 P1 / USB2_DN6 P3 — USB7_USB20_P U8 / USB7_USB20_N U10 — Card Reader
USB2_DP7 U8 / USB2_DN7 U10

SC 0713
R1809+ R1811 PU 100k for cnvi req

3D3V_S0
R1809 1 — 2 100KR2F-L1-GP — WLAN_CLKREQ_CPU_N_R
R1810 1 — 2 10KR2F-L1-GP — SSD_CLKREQ_CPU_N_R
SC0717 GP
R1811 1 — DY — 2 100KR2F-L1-GP — PCIE_WAKE1_CPU
R1812 1 — DY — 2 10KR2F-L1-GP — PCIE_WAKE2_CPU
SC0731 DY

1D8V_S5
R1808 1 — 2 10KR2F-L1-GP — USB_OC0#
R1806 1 — 2 10KR2F-L1-GP — USB_OC1#

3D3V_LAN_S5
R1817 1 — 2 10KR2F-L1-GP — LAN_CLKREQ_CPU_N_R
SC 0630

10.10 USB 2.0 Disabling and Termination Guidelines

If a USB port(s) is not implemented on the platform:

- USB_DP [6:0] and the USB_DN[6:0]signals can be left unconnected
- USB2_RCOMP Should be connected to 113Ohm 1% resistor Pull down to ground
- When the platform does not use the USB2_OTG_ID, USB2_VBUS_SNS, and USB2_OC0/1_N pins:
  - USB2_OTG_ID and USB2_OC[x]_N pins can be left unconnected.
  - USB2_VBUS_SNS needs to be connected to GND.
- The USB2_OTG_ID pin has an internal 100kohm pull up and the USB2_OC[0:1]_N pins have an internal 20k pull up, so an external pull up is not required. However, if customers are concerned on platform EMI, it is recommended to use external 10k pull up resistor to V1P8A

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB3/USB2)
Size: A3 | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 18 of 104

SSID = PCH

APS debug port

1.8v

CPU1H

8 OF 13

GEMINI-LAKE-GP

0526

Signal Name	Dir.	I/O Voltage	Description
PROCHOT_N	I/O, OD	V1P8	**Processor Hot:** asserted when the processor die temperature has reached its maximum operating temperature.

all S0 power rail ok
(PCH_PWROK delay 1D05V_S0 between 5~100ms)
and SYS_PWROK for discrete power solution

0213 Del Audio off-page
0215 Del 3V_5V_PWRGD off-page
0217 Del SML1_DATA/SML1_CLK
0220 Del AC_PRESENT

0516

0601

0516

0518

32.768 kHz

X1901 (32.768 kHz)

Vendor PN	Wisrton PN	C1903	C1904
EPSON EP.FC-135R 32.768K12.5+-20	082.30003.0191	18pF	18pF
NDK EXS00A-MU00503	082.30003.0221	18pF	18pF
TXC 9H03200042	082.30003.0231	18pF	18pF

19.2 MHz

-1 1221
R1906&R1907 change from shortpad to 0 ohm

X1902 (19.2 MHz)

Vendor PN	Wisrton PN	C1906	C1907
TXC 7V19200001	082.30001.0171	15pF	15pF
HARMONY X3G019200DC1H-HU	082.30001.0181	15pF	15pF

<Variant Name>

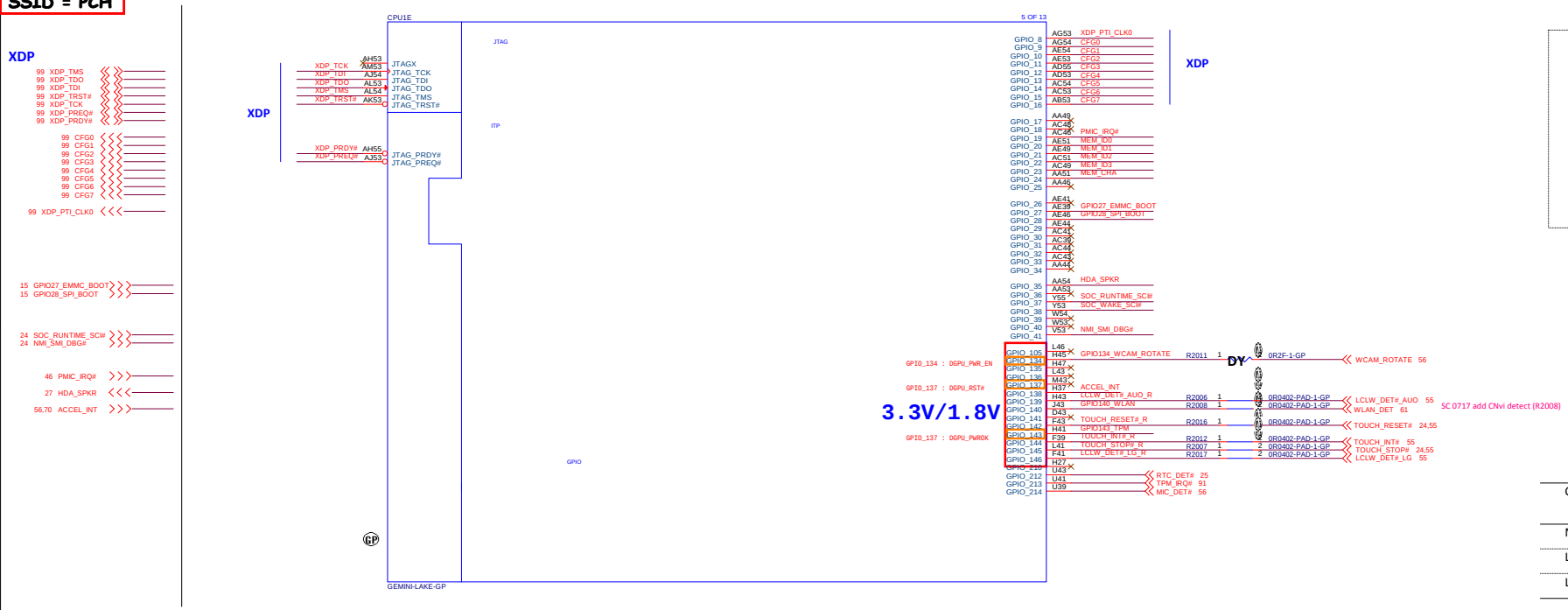
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

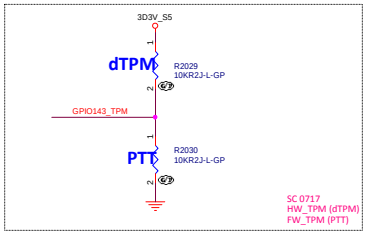
Title: CPU (PMU/PMC/SVID/RTC/MISC)

Size: A2 | Document Number: Leia | Rev: -1M

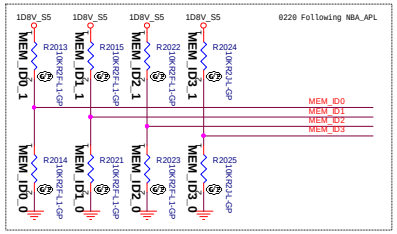
Date: Thursday, December 28, 2017 | Sheet 19 of 104

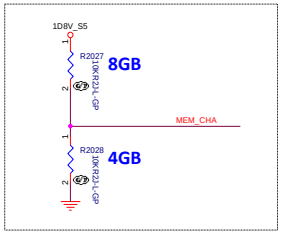
SSID = PCH

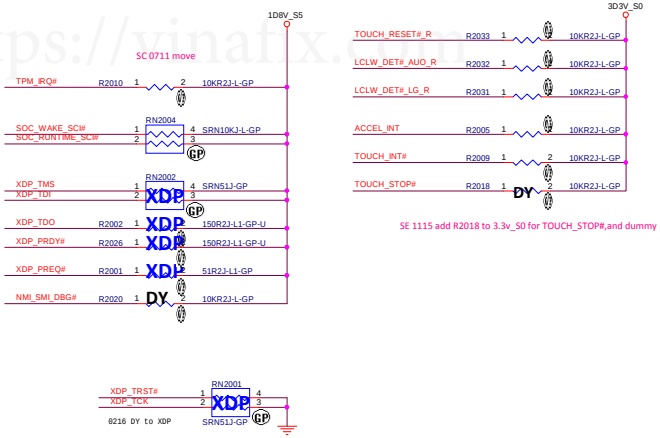




ClamShell Panel	LCLW_DET#_AUO (GPIO_139)	LCLW_DET#_LG (GPIO_146)
NON TOUCH	HIGH	HIGH
LCLW: AUO	LOW	HIGH
LCLW: LG	HIGH	LOW







LCD CONN.		
ClamShell	PIN 20	PIN 21
NON TOUCH	HIGH	HIGH
LCLW: AUO	LOW	HIGH
LCLW: LG	HIGH	LOW

GPIO22	GPIO21	GPIO20	GPIO19					
MD_ID3	MD_ID2	MD_ID1	MD_ID0	Vendor PN	Wisrton PN	Vendor	Density
0	0	0	0	H5AN8G6NAFR-UHC	SM30L08875	HYNIX	8GB
0	0	0	1	MT40A512M16JY-083E:B	SM30L08877	MICRON	8GB
0	0	1	0	K4A8G165WC-BCRC	SM30N71798	SAMSUNG	8GB
0	0	1	1	H5AN8G6NAFR-UHC	SM30L08875	HYNIX	4GB
0	1	0	0	MT40A512M16JY-083E:B	SM30L08877	MICRON	4GB
0	1	0	1	K4A8G165WC-BCRC	SM30N71798	SAMSUNG	4GB

0=L ,1=H

SC 0626

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO/JTAG/ITP)

Size: A2 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 20 of 104

SSID = CPU

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (Reserved)*

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 21 of 104

SSID = CPU

Blanking

<Variant Name>

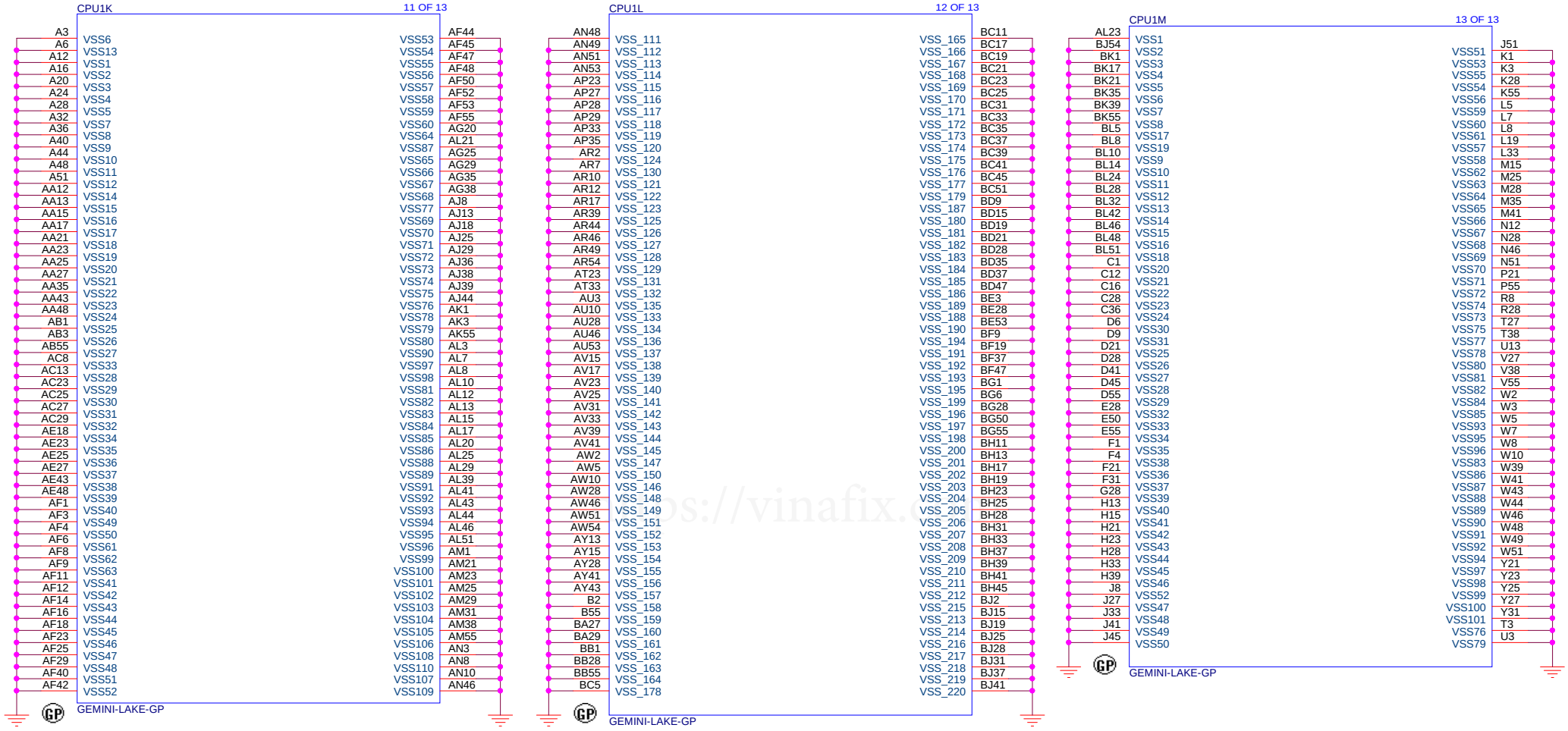
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Reserved)

Size: A4 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 22 of 104

SSID = CPU



<Variant Name>

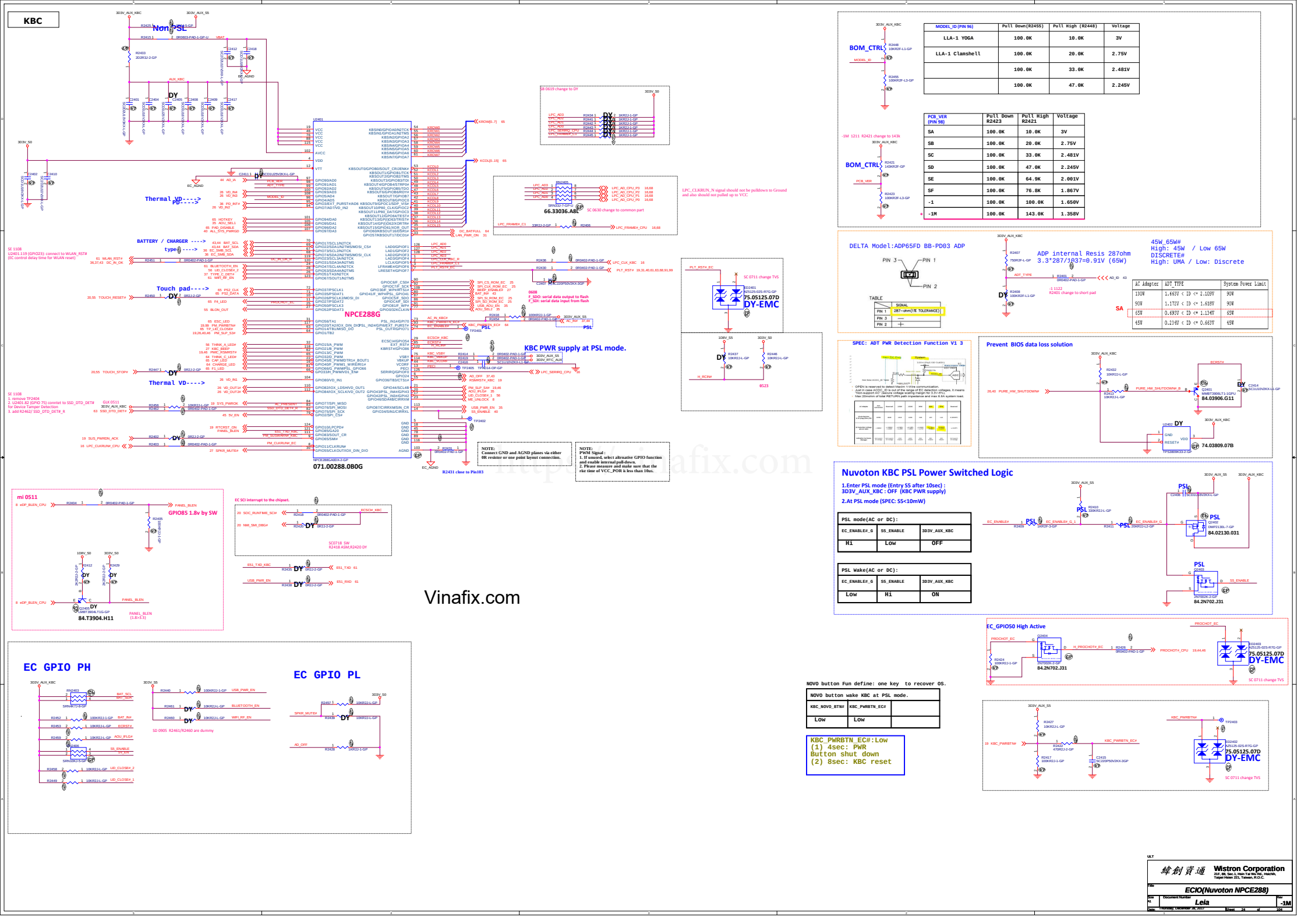
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VSS**

Size	Document Number	Rev
Custom	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 23 of 104

KBC



U2401
NPCE288G
071.00288.0B0G

Vinafix.com

BOM_CTRL

MODEL_ID (PIN 96)	Pull Down(R2455)	Pull High (R2448)	Voltage
LLA-1 YOGA	100.0K	10.0K	3V
LLA-1 Clamshell	100.0K	20.0K	2.75V
	100.0K	33.0K	2.481V
	100.0K	47.0K	2.245V

BOM_CTRL

PCB_VER (PIN 98)	Pull Down R2423	Pull High R2421	Voltage
SA	100.0K	10.0K	3V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.481V
SD	100.0K	47.0K	2.245V
SE	100.0K	64.9K	2.001V
SF	100.0K	76.8K	1.867V
-1	100.0K	100.0K	1.650V
-1M	100.0K	143.0K	1.358V

DELTA Model:ADP65FD BB-PD03 ADP

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.105V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.214V < ID <= 0.663V	45W

SA

SPEC: ADT PWR Detection Function V1 3

Prevent BIOS data loss solution

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

EC_GPIOS0 High Active

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

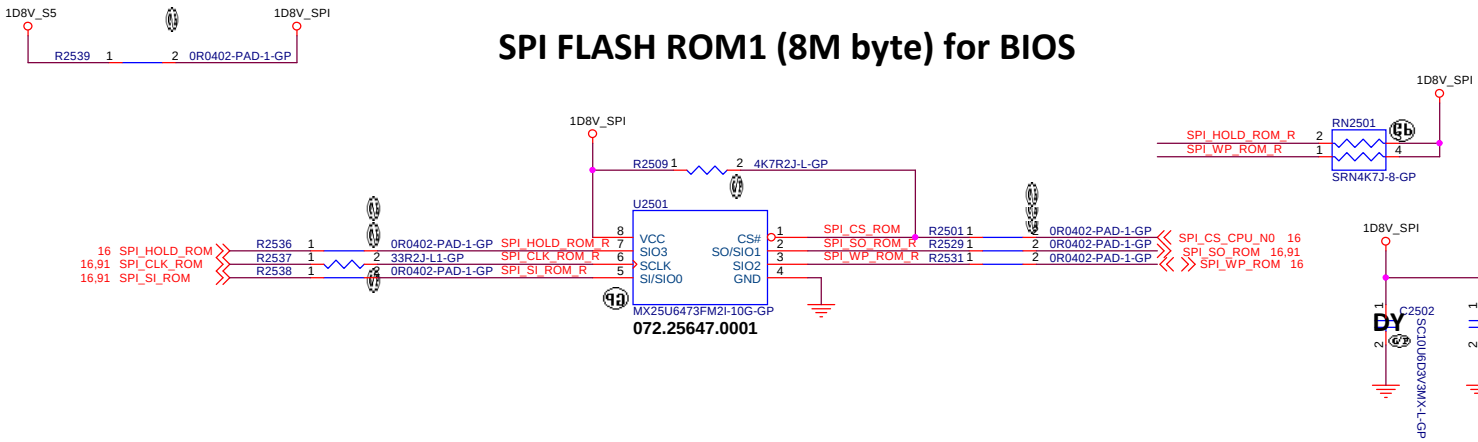
EC GPIO PH

EC GPIO PL

Wistron Corporation	緯創資通
Title	ECIO(Nuvoton NPCE288)
Size: A1	Document Number: Leia
Rev: -1M
Date: Thursday, December 28, 2017	Sheet 24 of 35

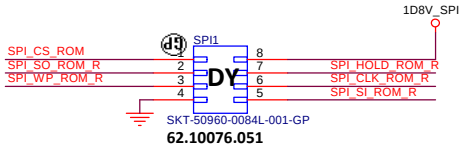
Flash.ROM/RBAT

SPI FLASH ROM1 (8M byte) for BIOS



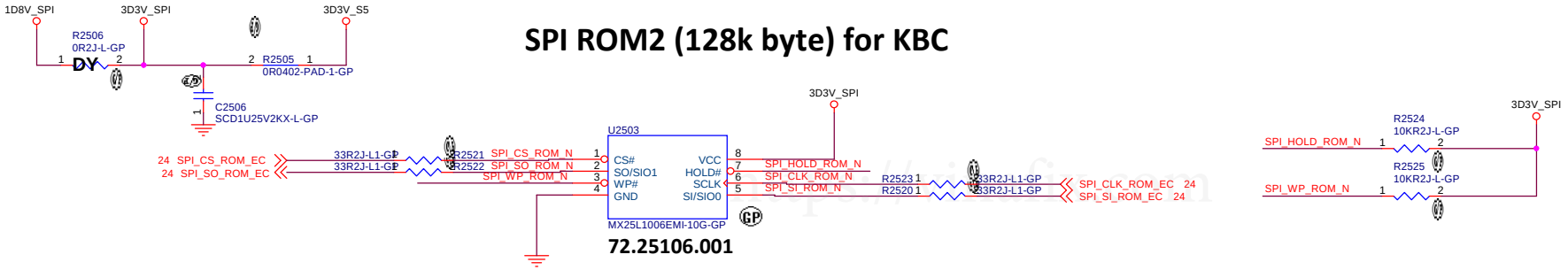
LKL-1

Co-Layout Design on U2501
SPI ROM Socket (SPI1)

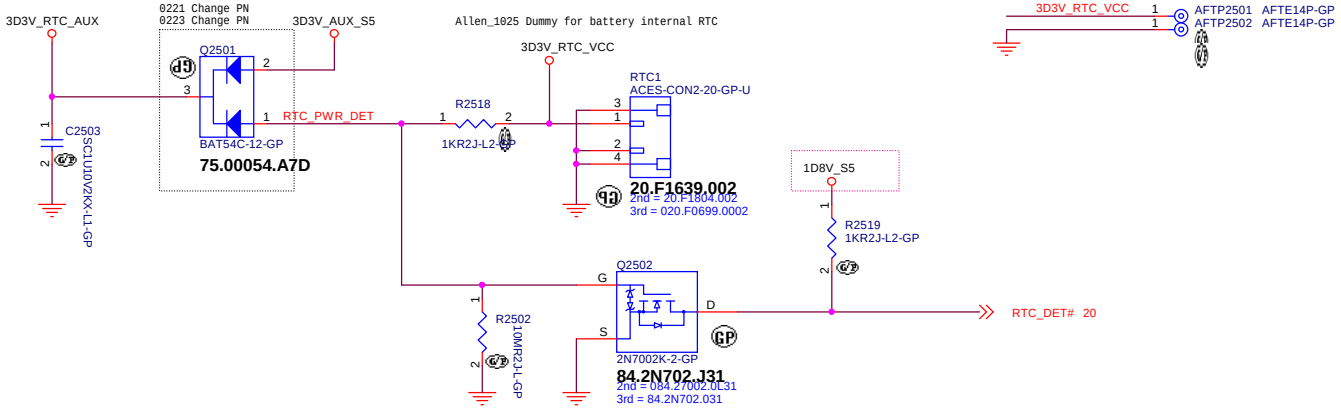


only EVT ASM

SPI ROM2 (128k byte) for KBC



RTC conn.



Co-Layout Design on U2503
FEROM Socket (SPI2)

SC 0711 remove socket on SPI2

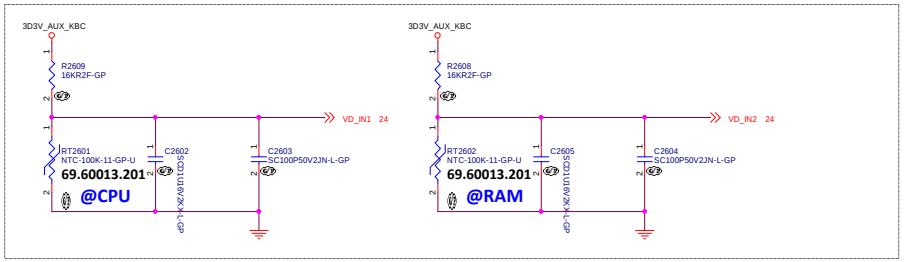
only EVT ASM

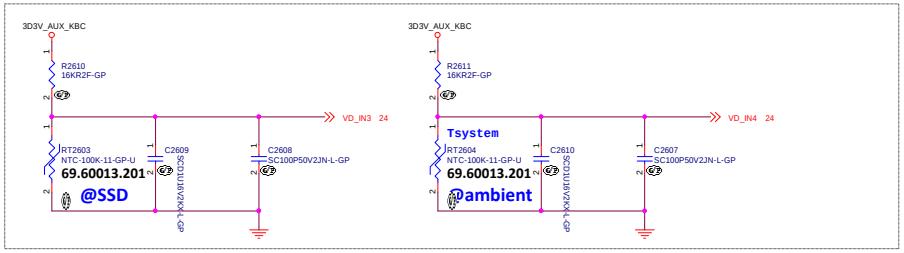
ULT

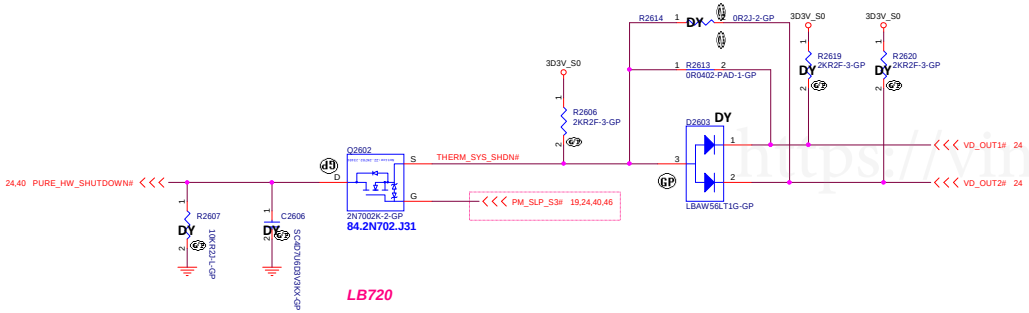
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Flash/RTC**		
Size: A3	Document Number: **Leia**	Rev: **-1M**
Date: Thursday, December 28, 2017	Sheet 25 of 104	

Thermal

SC 0717 change from 3D3V_AUX_S5 to 3D3V_AUX_KBC



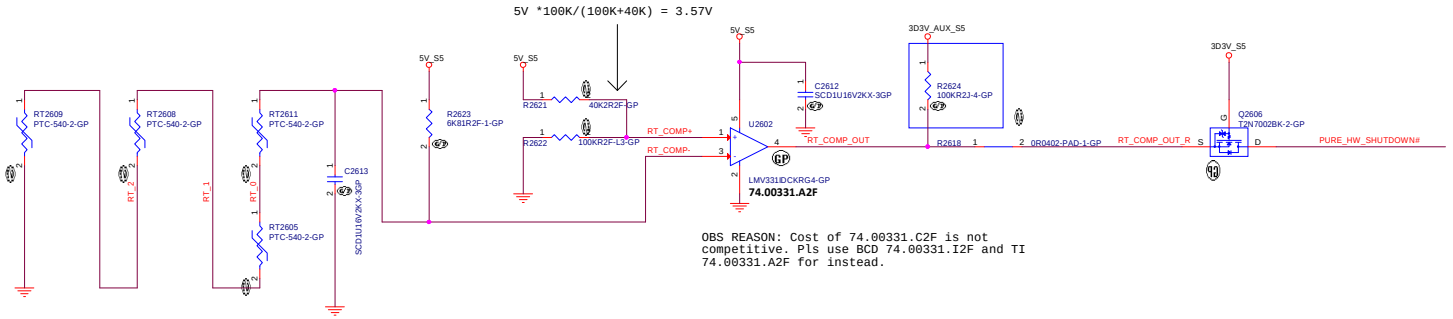




SE 1106 add PTC Logic SCH from LLA-1.5,but remove 3 PTC

PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

ULT

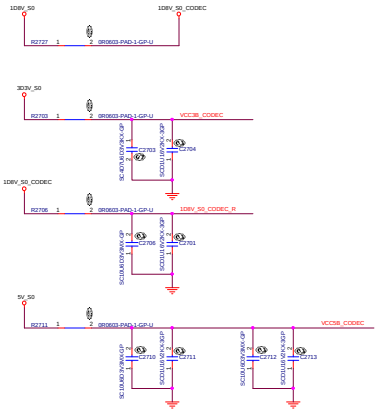
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

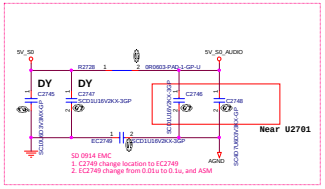
Title: INT IO (Thermal/Fan)

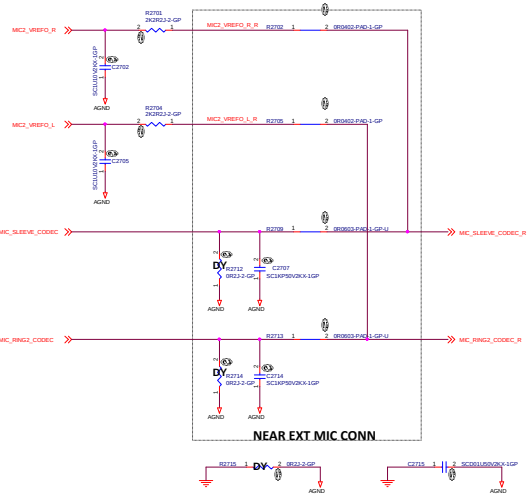
Size: A2 | Document Number: Leia | Rev: -1M

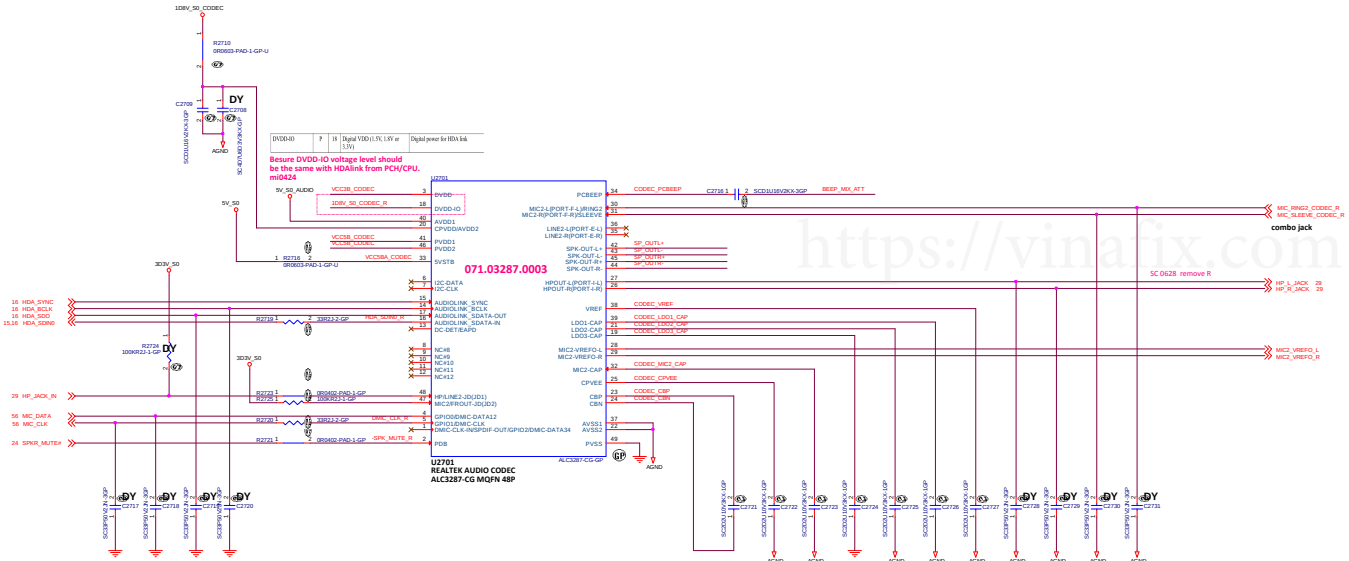
Date: Thursday, December 28, 2017 | Sheet 26 of 104

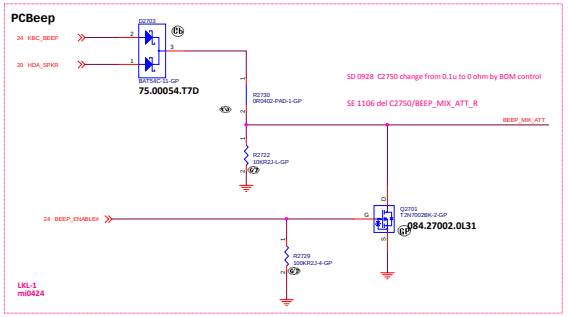
AUDIO

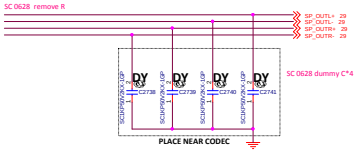












Wistron Corporation			
Audio (Codec ALC3287)			
Size: A1	Document Number: Leia		Rev: -1M
Date: Thursday, December 28, 2017	Sheet 27 of 104		

Blanking

Vinafix.com

ULT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

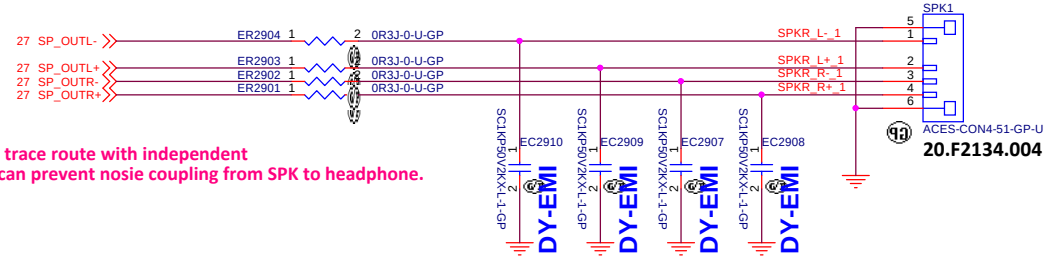
Title: ***(Reserved) Audio AMP***

Size	Document Number	Rev
A4	***Leia***	**-1M**

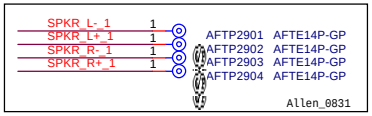
Date: Thursday, December 28, 2017 Sheet 28 of 104

Speaker/Audio CONN

Speaker CONN



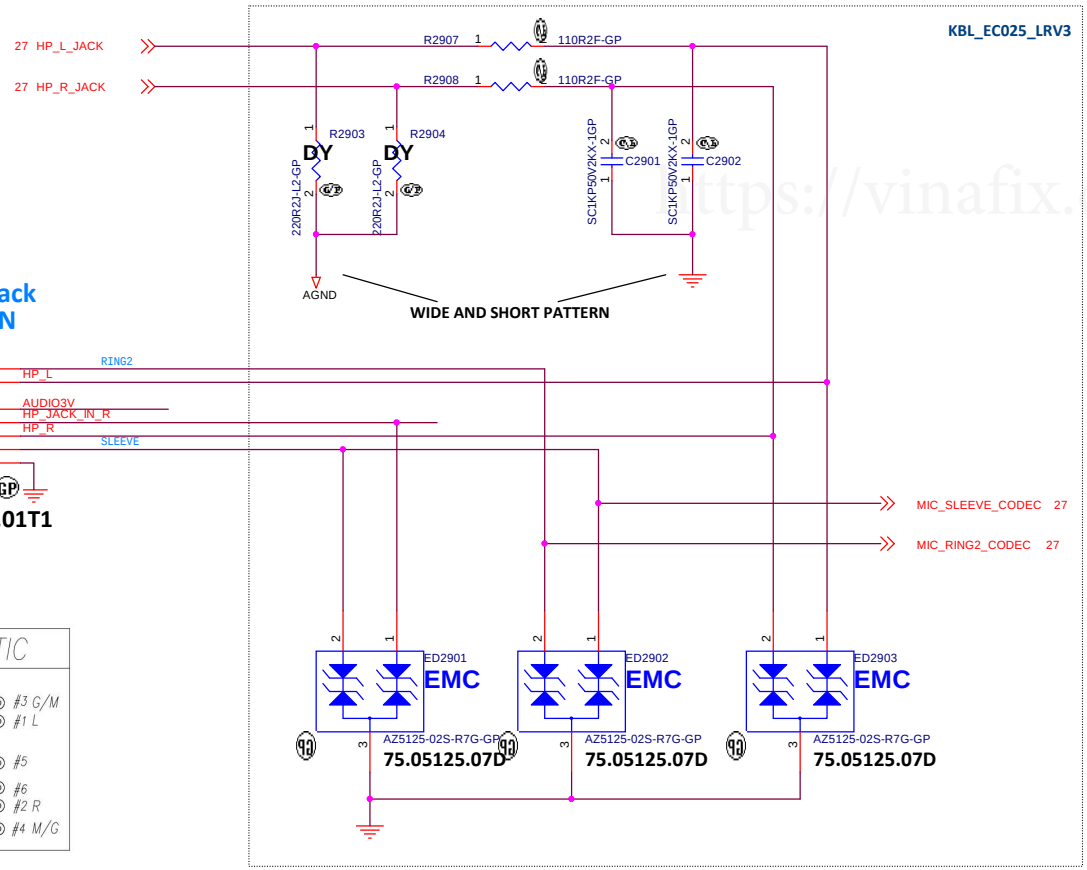
vendor,
If can, SPK trace route with independent
FPC cable can prevent nosie coupling from SPK to headphone.



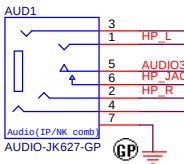
Audio_Combo_Jack

-1 1128
R2907,R2908 chnage to 110 ohm

NEAR AUDIO1 CONN

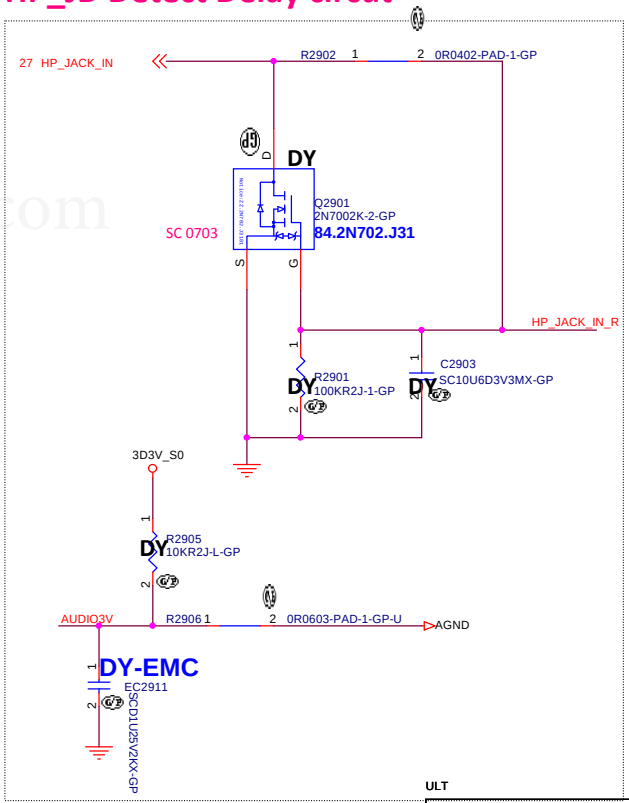


Headphone Jack
AUDIO CONN



022.10002.01T1

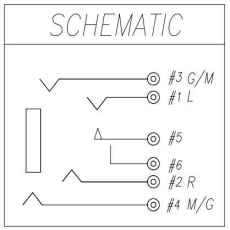
HP_JD Detect Delay circut



ULT

SE 1109
ED2901.2 connect to MIC_SLEEVE_CODEC

SCHEMATIC



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (HP/SPK/MIC Jack)		
Size: A3	Document Number: Leia	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 29 of 104	

SSID = LOM

Blanking

ULT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

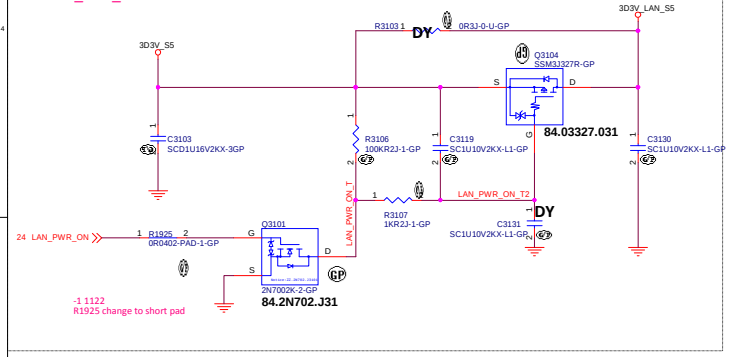
Title: ***(Reserved)***

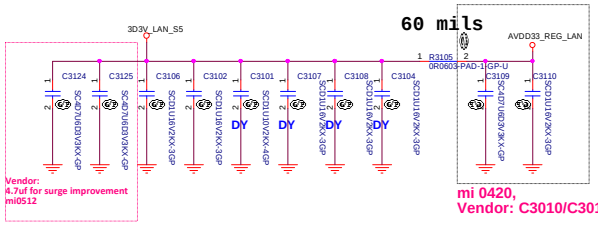
Size	Document Number	Rev
A4	***Leia***	**-1M**

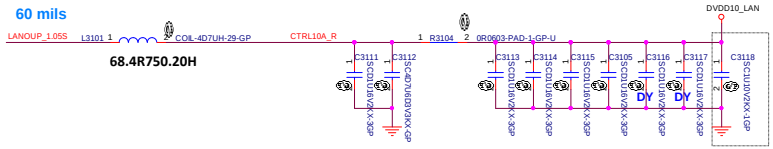
Date: Thursday, December 28, 2017 Sheet 30 of 104

LAN

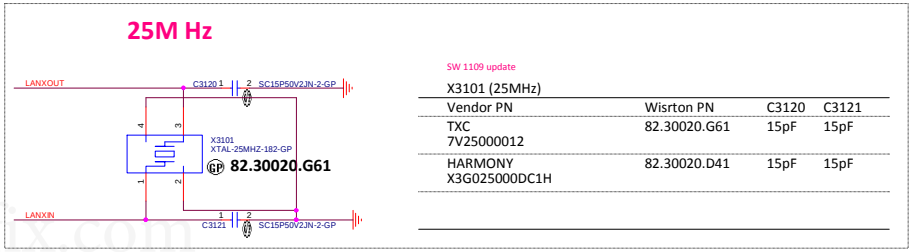
0517
3D3V_LAN_S5







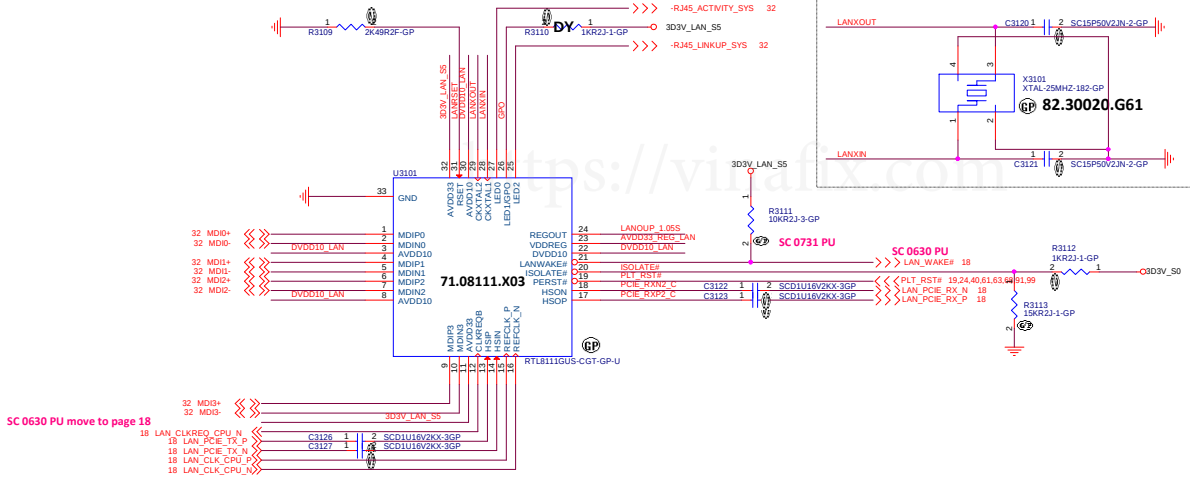
mi 0420,
Vendor: C3010/C3011 layout close to pin23



SW 1109 update

X3101 (25MHz)

Vendor PN	Wisrton PN	C3120	C3121
TXC 7V25000012	82.30020.G61	15pF	15pF
HARMONY X3G025000DC1H	82.30020.D41	15pF	15pF



ULT

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

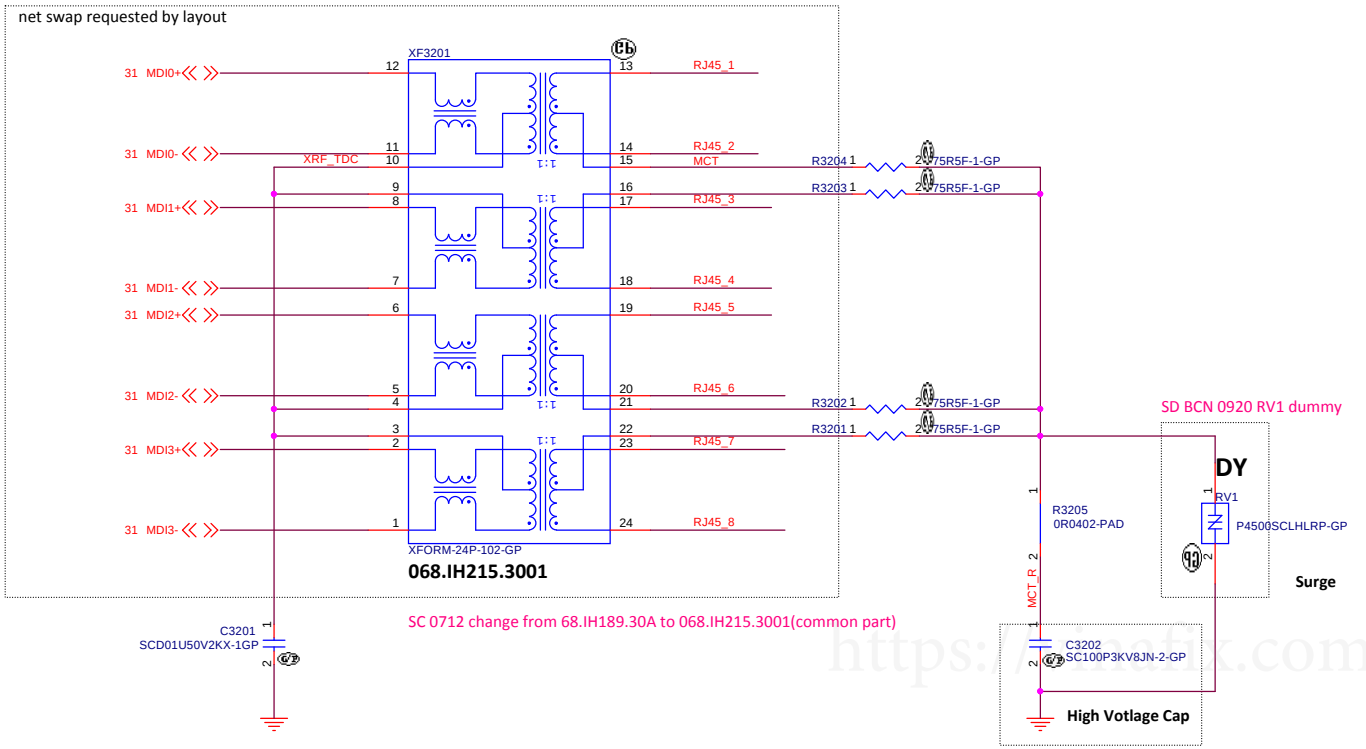
Title: **LAN_RTL8111GUS**

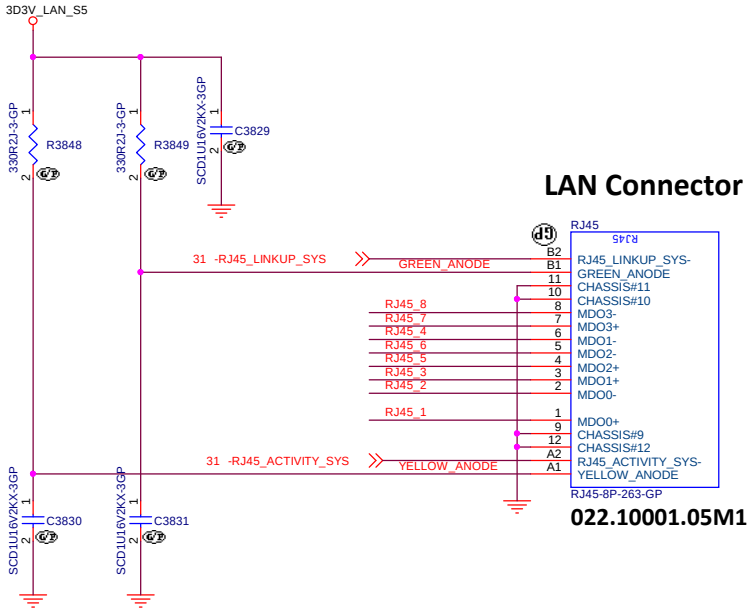
Size: A2 | Document Number: **Leia** | Rev: **-1M**

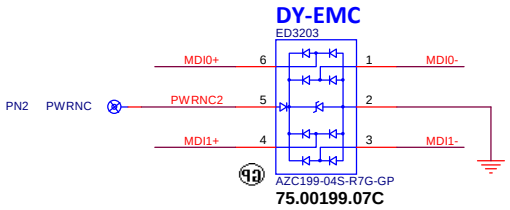
Date: Thursday, December 28, 2017 | Sheet 31 of 104

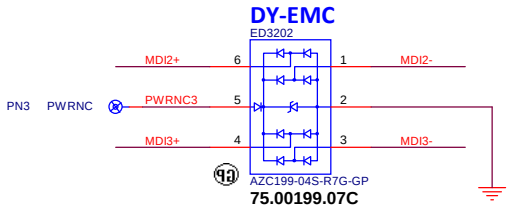
LAN CONN

10/100M/1000M Lan Transformer









ULT

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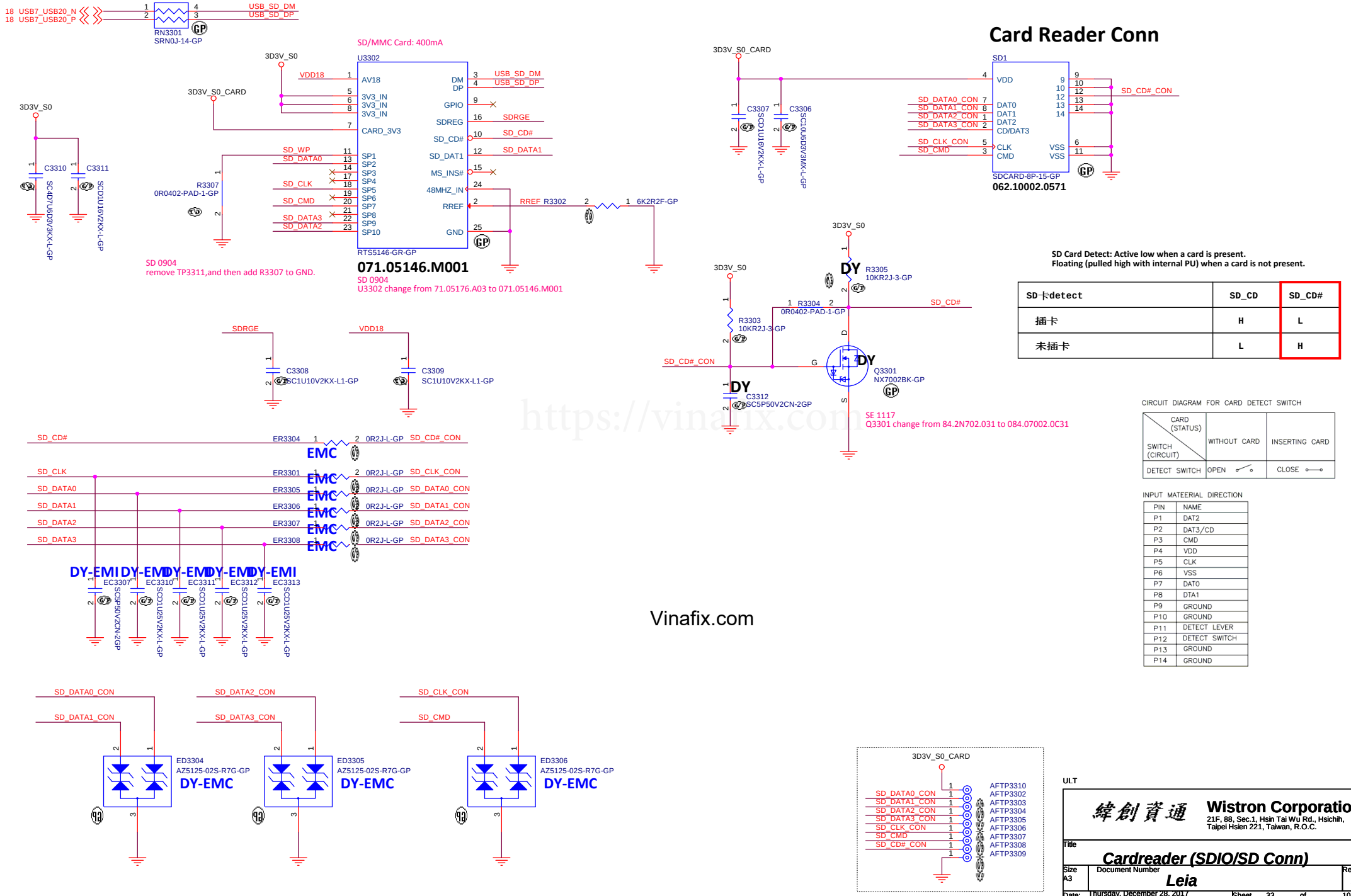
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RJ45+Transformer***

Size	Document Number	Rev
A3	***Leia***	-1M

Date: Thursday, December 28, 2017 Sheet 32 of 104

Card Reader



SSID = USB

Blanking

ULT

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Taipei Hsien 221, Taiwan, R.O.C.

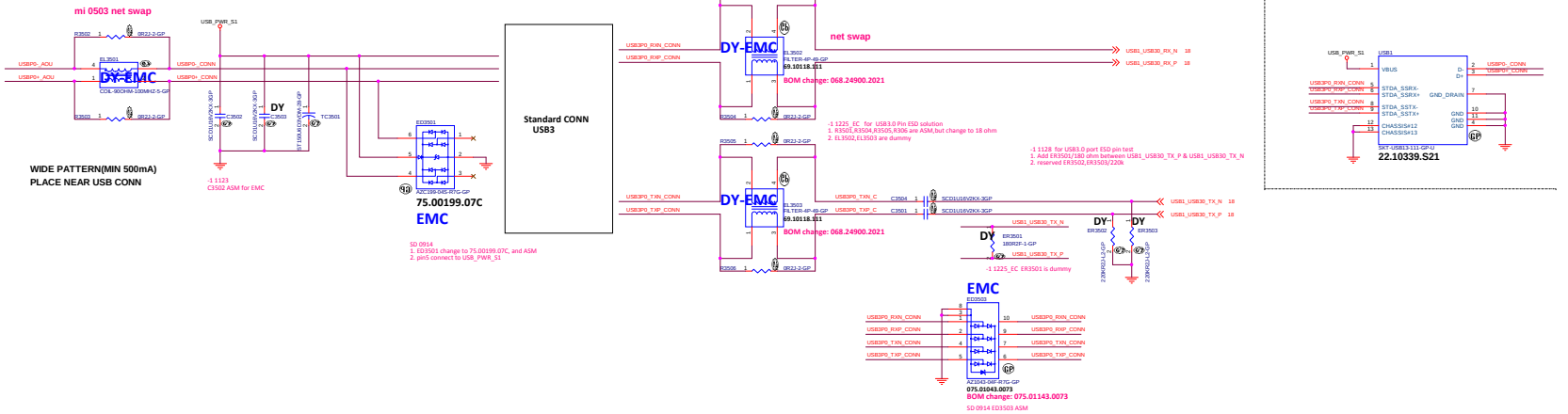
Title: USB 2.0 CONN

Size: A4 | Document Number: Leia | Rev: -1M

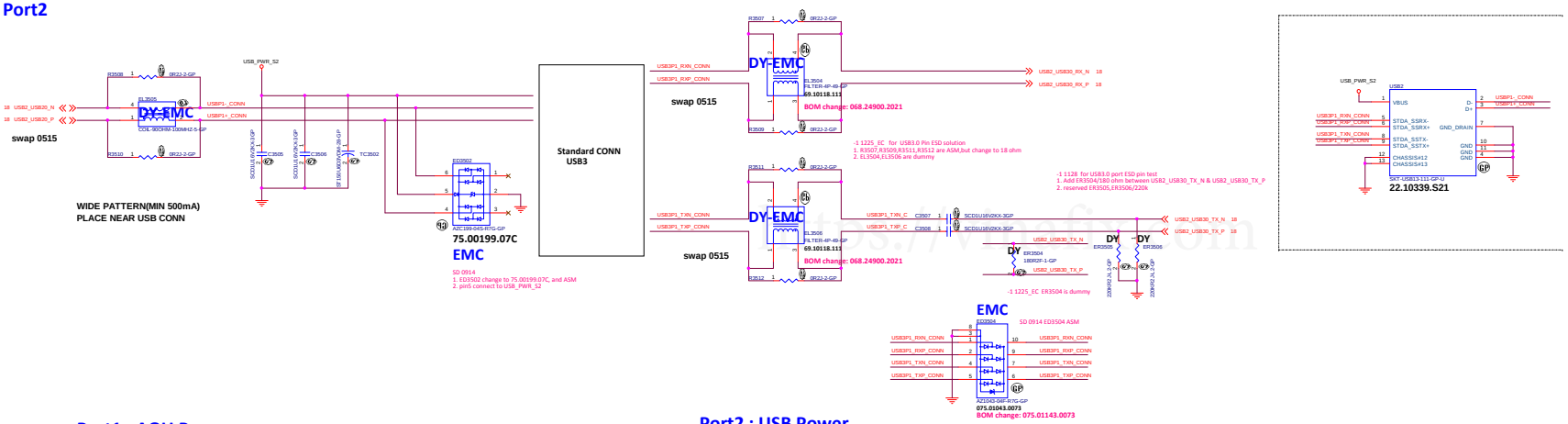
Date: Thursday, December 28, 2017 | Sheet 34 of 104

SSID = USB

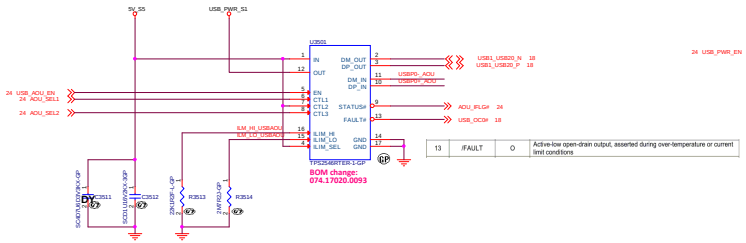
Port1(AOU)



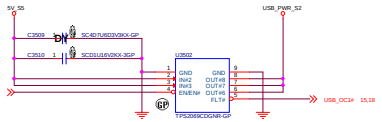
Port2



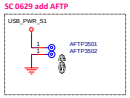
Port1 : AOU Power



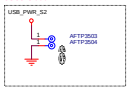
Port2 : USB Power



SC 0629 add AFTP



SC 0629 add AFTP



ULT	緯創資通 Wistron Corporation	
Title	USB (USB3.0 Conn)	
Size A1	Document Number Leia	Rev -1M
Date: Thursday, December 26, 2017	Sheet 35 of 39	

SSID = USB

>> PD

DUMMY-SYMBOL

BOM control: 071.05455.0003 /RTS5455-GR

BOM Control: SL50M27768AA

DY-EMC

EMC

SCA0L72570AA

75.27002.F7C

74.02204.03F

75.00199.07C

075.01043.0073

075.8S300.0073

SC 0629 add AFTP

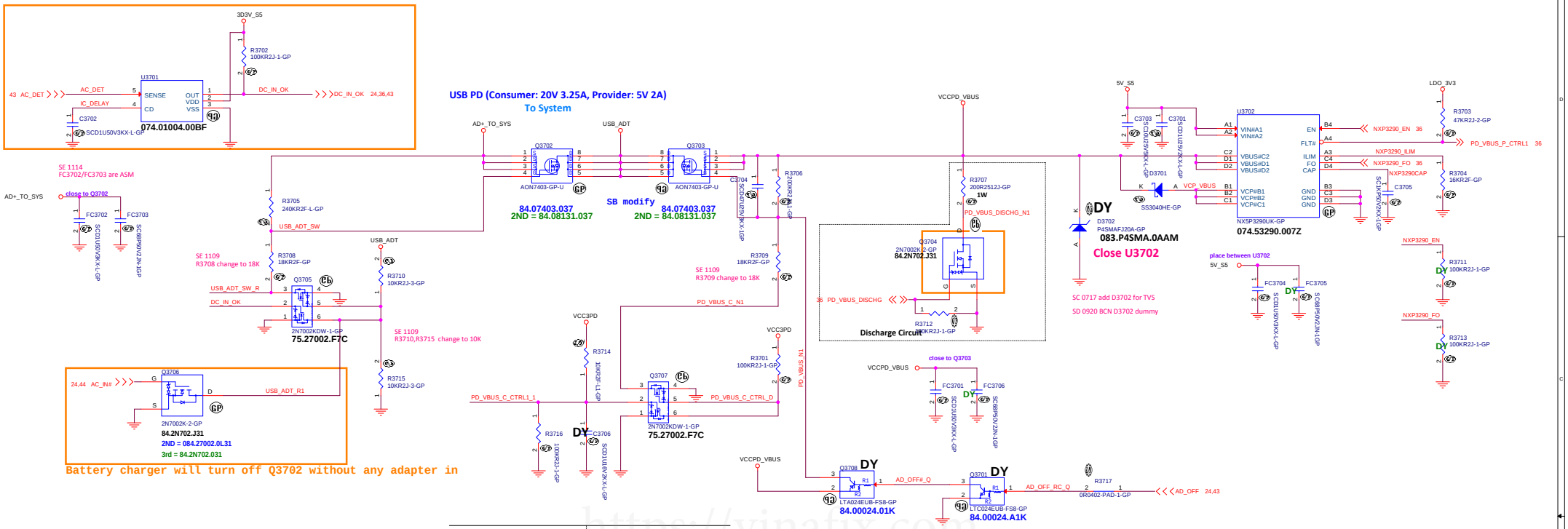
Wistron Corporation

Title: USB Type-C

Size: A1 | Document Number: Leia | Rev: -1

Date: Thursday, December 26, 2017 | Sheet 36 of 106

SSID = USB type C



	R3718	R3719	R3714	R3716	C3704
AC control	DY	ASM	DY	DY	DY
PD control	ASM	DY	ASM	ASM	ASM

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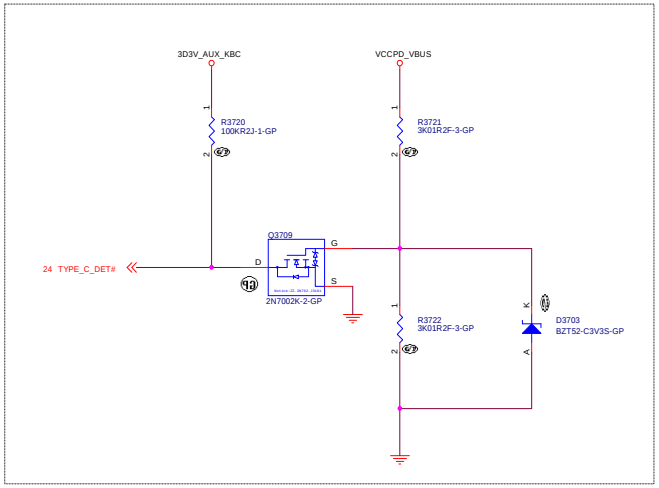

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	QA802	OFF	
					QA803	OFF	
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	QA802	ON	Control by Charger *DC_IN_OK*
					QA803	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	QA802	OFF	
					QA803	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High (Realtek fine tune)	QA802	OFF	Control by Charger *ACOK_IN_M*
					QA803	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

ULT

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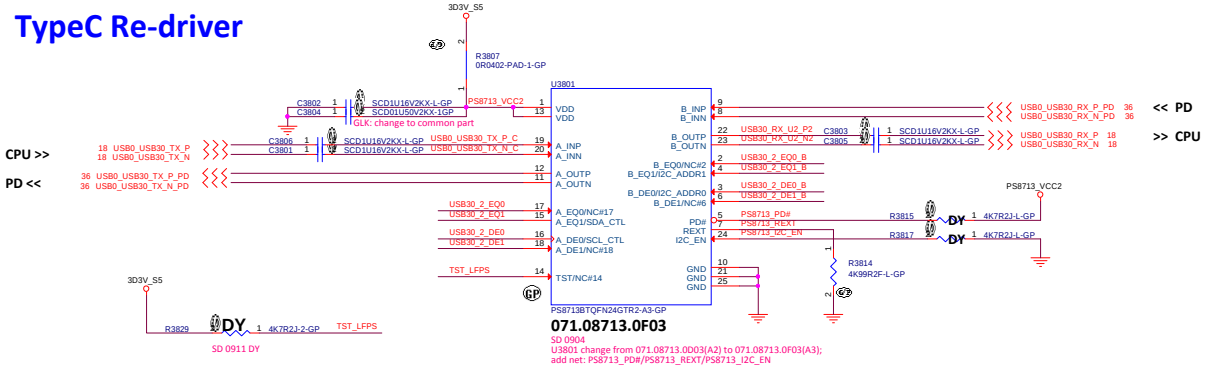
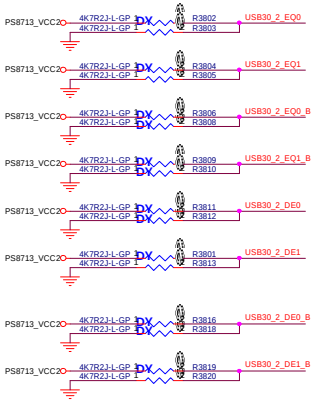
Title: **PD controll**

Size: A2 | Document Number: **Leia** | Rev: **-1M**

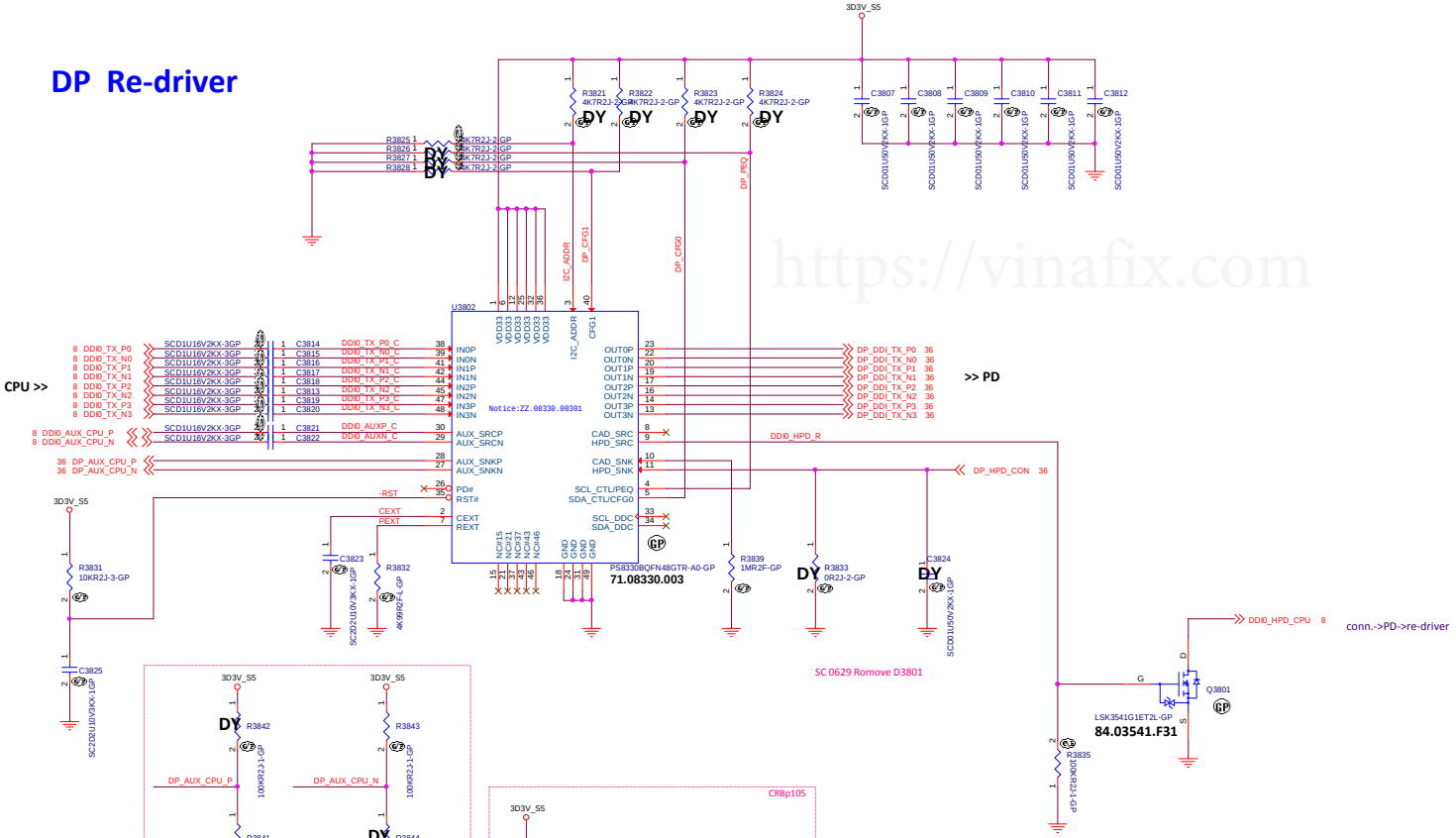
Date: Thursday, December 28, 2017 | Sheet 37 of 104

TypeC Re-driver





DP Re-driver



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Title: **Type-C Redriver**

Size	Document Number	Rev
A2	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 38 of 104

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ULT

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Title	***(Reserved)***
Size: A4	Document Number: ***Leia***
Rev: **-1M**	
Date: Thursday, December 28, 2017	Sheet 39 of 104

SSID = Reset.Suspend

Power Sequence

ALL_SYS_PWRGD

PMIC_PWRGD — R4006 1 — 2 — ALL_SYS_PWRGD
0R0402-PAD — Allen_0996

To EC

19,46 PMIC_PWRGD
24 ALL_SYS_PWRGD

0216 Adding off-page
0221 Rename net
0309 Del 5V_S5_EN

45 3V_S5_EN

24 S5_ENABLE
24,26 PURE_HW_SHUTDOWN#
19,46 PMIC_THERMTRIP#
19,24,31,61,63,68,91,99 PLT_RST#
19,24,26,46 PM_SLP_S3#

SC 0629 del

To 3V/ 5V Power IC S5 ENABLE

PMIC_THERMTRIP#
PLT_RST# — R4001 1K8R2-GP — H_PWRGD_R — Q4002 Allen_0901 LMBT3904LT1G-GP 84.T3904.H11 2nd = 84.T3904.L11 3rd = 84.T3904.K11
R4002 2K2R2J-L1-GP
PLACE CLOSE TO PCH1
0221 Change PN
D4001 RB551V30-GP 83.R5003.H8H
3V_S5_EN — PURE_HW_SHUTDOWN#
0221 Rename Net
0309 Del 5V_S5_EN
R4004 2KR2F-L1-GP — S5_ENABLE

RUN Power

5V_S0/3D3V_S0

5V_S5 — C4007 SC10U6D3V3MX-L-GP — C4006 SC1U10V2KX-L1-GP
3D3V_S5 — C4008 SC10U6D3V3MX-L-GP — C4009 SC1U10V2KX-L1-GP
PM_SLP_S3# — R4003 — 3V_5V_S0_EN
0R0402-PAD — Allen_0105 short pad — C4051 SC1U10V2KX-L-GP

U4001 G2898KD1U-GP
VBIAS, IN1#1, IN1#2, IN2#6, IN2#7, EN1, EN2, CT1, CT2, OUT1#13, OUT1#14, OUT2#8, OUT2#9, GND, THERMAL_PAD

SW_5V_S0_CT — C4004 SC470P50V2KX-L-GP
SW_3D3V_S0_CT — C4001 SC1KP50V2KX-L-1-GP
5V_SYS_OUT
3V_SYS_OUT
3.5A
3A
C4011 SC2D1U10V2KX-L-GP
C4010 SC2D1U10V2KX-L-GP

5V_SYS_OUT — PG4001 GAP-CLOSE-PWR-6-GP
PG4002 GAP-CLOSE-PWR-6-GP
PG4003 GAP-CLOSE-PWR-6-GP
PG4004 GAP-CLOSE-PWR-6-GP
5V_S0

3V_SYS_OUT — PG4005 GAP-CLOSE-PWR-6-GP
PG4006 GAP-CLOSE-PWR-6-GP
PG4007 GAP-CLOSE-PWR-6-GP
3D3V_S0

1D8V_S0

1D8V_S5 — C4014 SC10U6D3V3MX-L-GP — C4015 SC1U10V2KX-L1-GP
5V_S5
3D3V_S0 — R4059 — 1D8V_S0_EN
0R0402-PAD

U4002 G2898KD1U-GP
VBIAS, IN1#1, IN1#2, IN2#6, IN2#7, EN1, EN2, CT1, CT2, OUT1#13, OUT1#14, OUT2#8, OUT2#9, GND, THERMAL_PAD

SW_1D8V_S0_CT — C4012 SC470P50V2KX-L-GP
SW_CARD_CT — C4013 SC470P50V2KX-L-GP
1D8V_S0
0.5A
SC 0629 del 3D3V_S0_CARD
C4016 SC2D1U10V2KX-L-GP

Discharge circuit

3D3V_AUX_S5 — R4056 100KR2J-4-GP — 3D3V_S5_EN_DCG
Q4001 2N7002KDW-1-GP 75.27002.F7C
0221 Rename Net
3V_S5_EN
3D3V_S5_DISCHG — R4048 1KR2J-GP — 3D3V_S5
0221 Change PN

-1M 1212 add Discharge circuit to fine tune the t31 down sequence
-1M 1218_8CN
dummy Q4003,Q4004, R4005,R4007,R4008,R4009,R4010

1D05V_S0
PM_SLP_S3# — R4008 1KR2F-L1-GP — R4007 6D8R5J-GP — size 0805
Q4003 2N7002KDW-GP 75.27002.F7C
3D3V_S5 — R4005 10KR2F-2-GP
R4009 1KR2F-L1-GP — R4010 6D8R5J-GP — size 0805
Q4004 2N7002KDW-GP 75.27002.F7C

ULT

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Title: Sequence (Power Plane EN)
Size: A2 | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 40 of 104

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Title	*(Reserved)DS3*
Size A4	Document Number *Leia*
Rev	-1M
Date: Thursday, December 28, 2017	Sheet 41 of 104

<Core Design>

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Wistron Corporation
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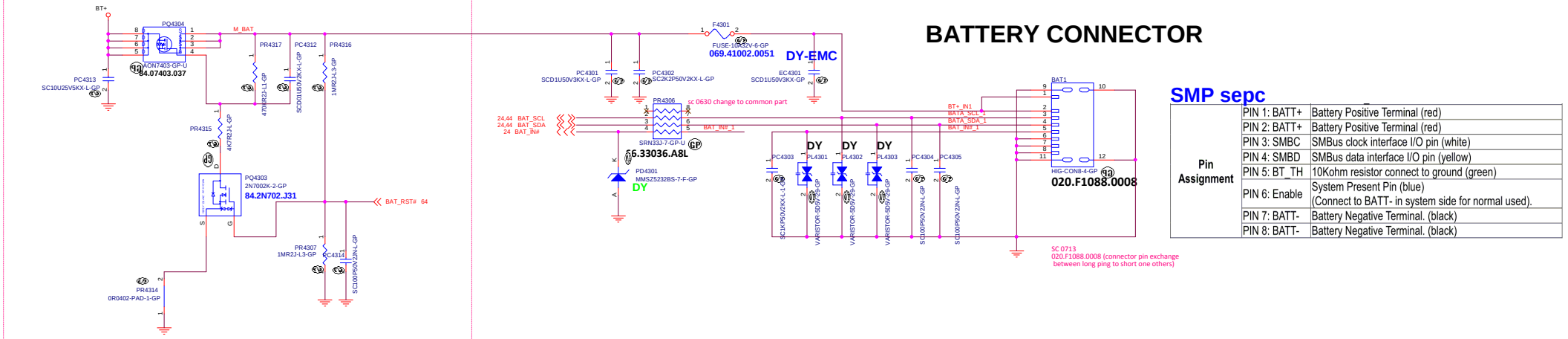
Title: ***Reserved***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 42 of 104

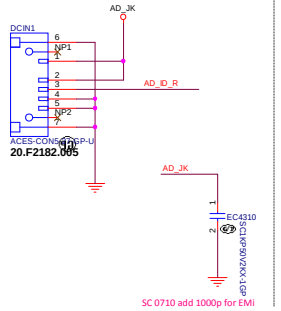
BATTERY CONNECTOR



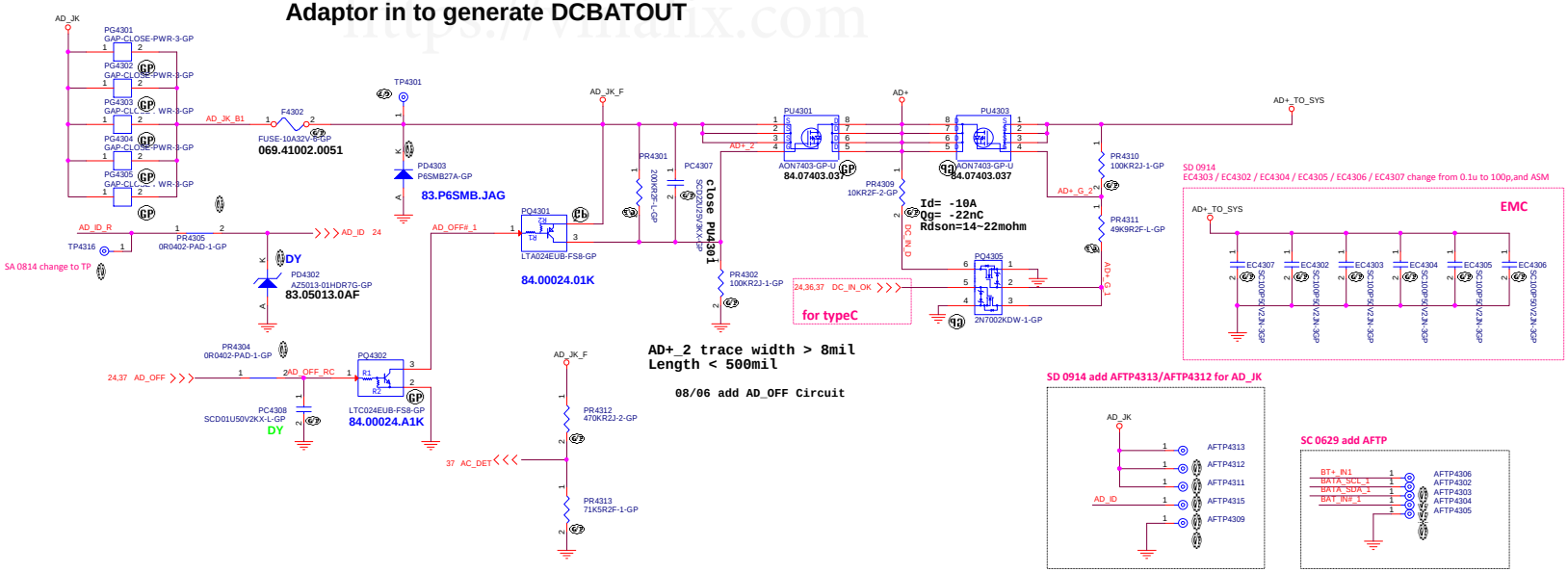
SMP sepc

Pin Assignment	PIN 1: BATT+	Battery Positive Terminal (red)
	PIN 2: BATT+	Battery Positive Terminal (red)
	PIN 3: SMBC	SMBus clock interface I/O pin (white)
	PIN 4: SMBD	SMBus data interface I/O pin (yellow)
	PIN 5: BT_TH	10Kohm resistor connect to ground (green)
	PIN 6: Enable	System Present Pin (blue) (Connect to BATT- in system side for normal used).
	PIN 7: BATT-	Battery Negative Terminal. (black)
	PIN 8: BATT-	Battery Negative Terminal. (black)

DC Jack



Adaptor in to generate DCBATOUT



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<Variant Name>

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Title: DCIN & BATT CONN

Size: A2 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 43 of 104

OFFPAGE

24,43 BAT_SCL — PR4406 0R0402-PAD-1-GP — PWR_CHG_SCL
24,43 BAT_SDA — PR4411 0R0402-PAD-1-GP — PWR_CHG_SDA
24 AD_IA — PR4418 0R0402-PAD-1-GP — PWR_CHG_IADPT
39,24,46 PROCHOT#_CPU — PR4427 0R0402-PAD-1-GP — PWR_CHG_PROCHOT#
24,37 AC_IN# — PR4429 0R0402-PAD-1-GP — PWR_AC_IN#

delete P_SYS and PR4429
0425

	V(ILIM)	PR7325
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	74K ohm	1200KHz
1.5uH	86K ohm	1200KHz
2.2UH	100K Ohm	800KHZ

# of CELL	VCELL_PRES	PR7314
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

2.2uH DCR=18-20mohm, Idc=8A, Isat=14A 6.8*6.4*3mm

SE 1114 add PC4442,PC4443 for AD+_TO_SYS

sc 0630 change to common part

84.2N702.J31
2nd = 84.2N702.W31
3rd = 84.2N702.031

0505 buyer: 7"

<Core Design>
Wistron Corporation
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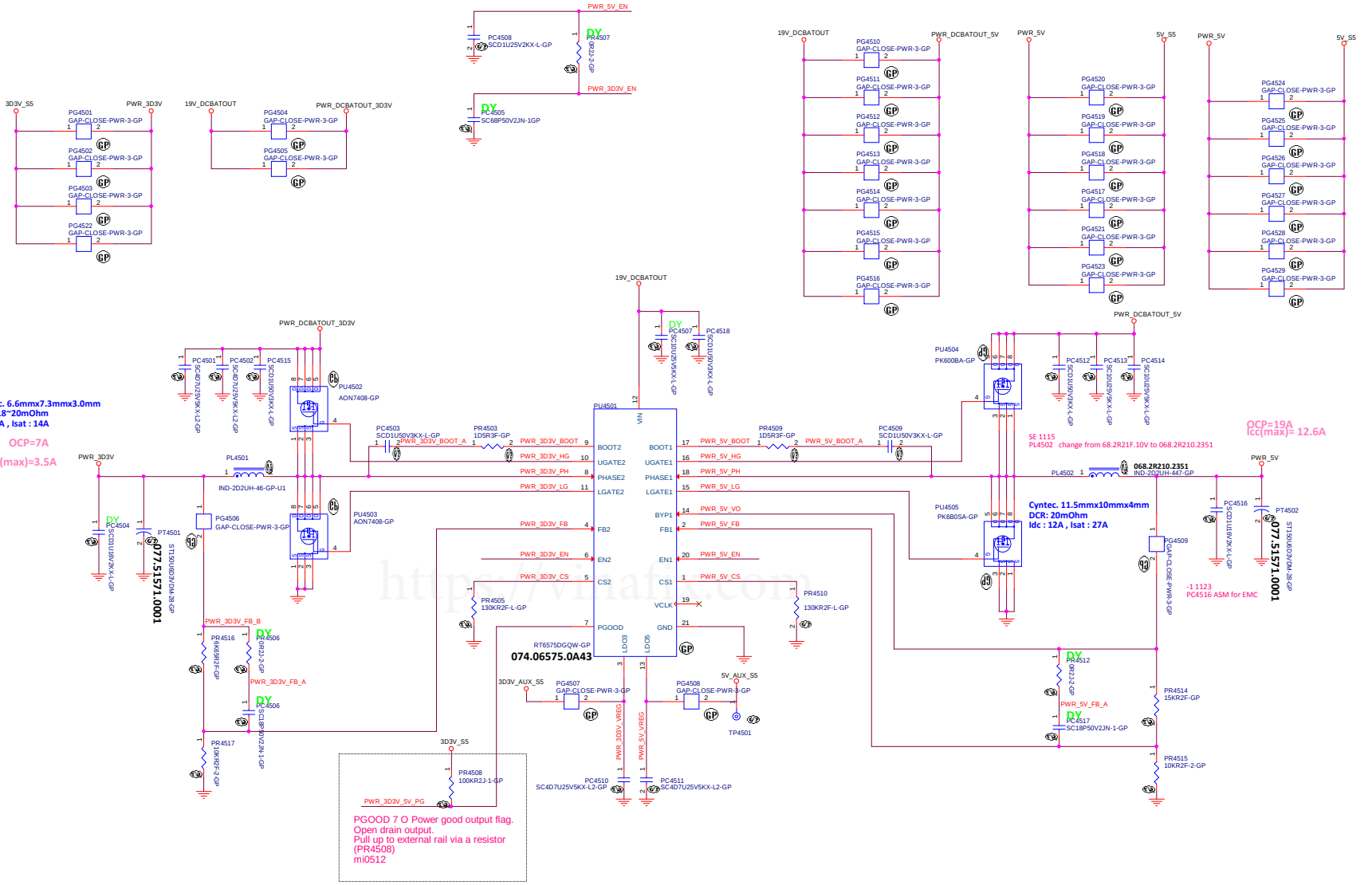
Title: CHARGER_BQ25700ARSNR
Size: Custom | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 44 of 104

OFFPAGE

24 5V_EN — PR4501 0R0402-PAD-1-GP — PWR_5V_EN

40 3V_S5_EN — PR4506 0R0402-PAD-1-GP — PWR_3D3V_EN

3V_5V_PWRGD — PR4523 0R0402-PAD-1-GP — PWR_3D3V_5V_PG



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	5V/3D3V
Size A2	Document Number Leia
Rev	-1M
Date: Thursday, December 28, 2017	Sheet 45 of 104

OFFPAGE

19 PMIC_I2C_SCL — PR4609 0R0402-PAD-1-GP — PWR_CLK
19 PMIC_I2C_SDA — PR4615 0R0402-PAD-1-GP — PWR_DATA
19,36,45 3V_5V_PWRGD — PR4616 0R0402-PAD-1-GP — PWR_PMIC_EN
19 PM_SLP_S0# — PR4617 0R0402-PAD-1-GP — PWR_SLP_S0_B
19,24,26,40 PM_SLP_S3# — PR4618 0R0402-PAD-1-GP — PWR_SLP_S3_B
19,24 PM_SLP_S4# — PR4619 0R0402-PAD-1-GP — PWR_SLP_S4_B
19,24 PMIC_RSMRST# — PR4620 0R0402-PAD-1-GP — PWR_RSMEST_B
19,40 PMIC_PWRGD — PR4621 0R0402-PAD-1-GP — PWR_PCH_PWROK
19,40 PMIC_THERMTRIP# — PR4622 0R0402-PAD-1-GP — PWR_THERMTRIP_B
19,24,44 PROCHOT#_CPU — PR4623 0R0402-PAD-1-GP — PWR_PROCHOT_B
20 PMIC_IRQ# — PR4624 0R0402-PAD-1-GP — PWR_IRQ_B

Gemini Lake PMIC and SoC Signal Connections

Gemini Lake PMIC Pin	Gemini Lake SoC Pin Name	SoC Pin	SoC Pin Type	Voltage Rail
IRQ#	TBD	TBD	Input	1.8V (SoC internal)
THERMTRIP#	THERMTRIP_N	J53	Output	1.8V (SoC internal)
PROCHOT#	PROCHOT_N	J54	Input	1.8V (SoC internal)
SLP_S4#	PMU_SLP_S4_N	J49	Output	1.8V (SoC internal)
SLP_S3#	PMU_SLP_S3_N	D51	Output	1.8V (SoC internal)
SLP_S0#	PMU_SLP_S0_N	C52	Output	1.8V (SoC internal)
PCH_PWROK	SoC_PWROK	D25	Input	External PU 20K to V3P3A and PD 100K to GND
RSMRST#	RSM_RST_N	F27	Input	External PU 20K to V3P3A and PD 100K to GND
DATA	PMIC_I2C_SDA	TBD	Input/ Output	1.8V (SoC internal)
CLK	PMIC_I2C_SCL	TBD	Output	1.8V (SoC internal)

0601

Main Func = CPU_CORE

I2C, Other signals

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19V_DCBATOUT — PG4613 GAP-CLOSE-PWR-3-GP — PC4602 SC1U50V3KX-GP
1D8V_S5 — PG4601 GAP-CLOSE-PWR-3-GP

Need EE Check

PR4601 1KR2F-L1-GP DY — PR4602 1KR2F-L1-GP DY — PC4601 SC1U10V2KX-L1-GP

0601

SD 0904 PR4627 DY

EE

3D3V_S5 — PR4625 1KR2F-L1-GP — PR4626 1KR2F-L1-GP DY — PR4628 1KR2F-L1-GP DY — PR4627 10KR2F-L3-GP — 1D8V_S5

0526

PU4601E BD2671MWV-E2-GP

PWR_VSYS	57	VSYS	
PWR_VDD_1VP8A	29	VDD_V1P8A	
PWR_CLK	37	CLK	
PWR_DATA	36	DATA	
PWR_PMIC_EN	33	PMIC_EN	
PWR_SLP_S0_B	20	SLP_S0_B	
PWR_SLP_S3_B	21	SLP_S3_B	
PWR_SLP_S4_B	22	SLP_S4_B	
PWR_RSMEST_B	19	RSMRST_B	
PWR_PCH_PWROK	18	PCH_PWROK	
PWR_THERMTRIP_B	34	THERMTRIP_B	
PWR_PROCHOT_B	35	PROCHOT_B	
PWR_IRQ_B	38	IRQ#	

5_0F_5

VSYS_V5A_0	31	PWR_VSYS_V5A_0	PR4603 20R2J-3-GP — PC4603 SC4D7U6D3V3KX-L-GP — PG4614 GAP-CLOSE-PWR-3-GP — 5V_S5
VSYS_V5A_1	4	PWR_VSYS_V5A_1	PC4604 SC4D7U6D3V3KX-L-GP — PG4616 GAP-CLOSE-PWR-3-GP — 5V_S5
VSYS_V5A_2	50	PWR_VSYS_V5A_2	PC4615 SC4D7U6D3V3KX-L-GP — PG4615 GAP-CLOSE-PWR-3-GP — 5V_S5
LDO15	30	PWR_PMIC_LDO1D5V	PC4605 SC4D7U6D3V3KX-L-GP
EXTMODE	32	PWR_EXTMODE	PR4631 0R2J-2-GP DY
TEST0	39	PWR_TEST0	PR4608 100KR2F-L3-GP
DDR_SEL0	2	PWR_EXTMODE0	
DDR_SEL1	12	PWR_EXTMODE1	
DDR_SEL2	17	PWR_EXTMODE2	
GND0	28		
GND1	46		
GND2	64		
PGND	69		

DDR4

PR4604 0R0402-PAD-1-GP — PR4605 0R0402-PAD-1-GP — PR4632 0R2J-2-GP DY

DDR4

PR4630 0R0402-PAD-1-GP — PR4606 0R2J-2-GP DY — PR4607 0R2J-2-GP DY — PR4633 0R0402-PAD-1-GP

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

<Variant Name>

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Title: 5V/3D3V
Size: Custom | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 46 of 104

OFFPAGE

PR4723 0R0402-PAD-1-GP
6 VCCGI_SENSE — PWR_VCCGI_FBPC

PR4724 0R0402-PAD-1-GP
6 VSSGI_SENSE — PWR_VCCGI_FBNB

Main Func = CPU_CORE

BUCK2[VCCGI]:1.0V_21A

19V_DCBATOUT, PWR_DCBATOUT_VCORE

PG4701 GAP-CLOSE-PWR-3-GP
PG4702 GAP-CLOSE-PWR-3-GP
PG4703 GAP-CLOSE-PWR-3-GP
PG4704 GAP-CLOSE-PWR-3-GP
PG4705 GAP-CLOSE-PWR-3-GP
PG4706 GAP-CLOSE-PWR-3-GP

MOSFET GATE Driver

5V_S5
PC4705 SC4D7U6D3V3KX-L-GP
PR4701 0R0402-PAD-1-GP
PC4716 SC1U10V2KX-L1-GP

PU4701 BD9515NUXE2-GP-U
PVCC, PWM, EN, PAD PGND, BOOT, HG, SW, LG
PWR_VCCGI_PVCC, PWR_VCCGI_PWM_1, PWR_VCCGI_BOOT, PWR_VCCGI_HG, PWR_VCCGI_PH, PWR_VCCGI_LG

PC4711 SCD47U25V3KX-1GP
PR4720 0R0805-PAD-1-GP-U
PR4721 10KR2J-3-GP
PWR_VCCGI_HG_A

PU4702 075.07321.0073 FDMS3600-02-RJK0215-COLAY-GP

0510 requested by Dante

PWR_DCBATOUT_VCORE
PC4702 SC100U25V5KX-1-GP
PC4703 SC100U25V5KX-1-GP
PC4701 SC100U25V5KX-1-GP
PC4704 SC100U25V5KX-1-GP

PU4601A 1 OF 5 — BD26711MWV-E2-GP
VCCGI_PWM, VCCGI_DRVEN, VCCGI_CSP, VCCGI_CSN, VCCGI_VOS, VCCGI_FBP, VCCGI_FBN
PWR_VCCGI_PWM, PWR_VCCGI_DRVEN, PWR_VCCGI_CSP, PWR_VCCGI_CSN, PWR_VCCGI_VOS, PWR_VCCGI_FBP, PWR_VCCGI_FBN

PR4702 0R0402-PAD-1-GP

SE 1115
PL4701 change from 68.R2210.10N to 68.R2210.20E

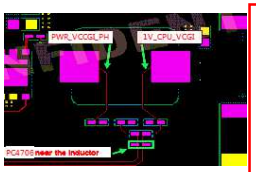
PL4701 68.R2210.20E COIL-D22UH-3-GP

ICCMAX=21A
TDC=18A

close choke
VCCGI :1D0V_21A
1V_CPU_VCGI
PC4718 SC470U2V3MX-L-GP
PT4701 SE330U2VDM-4-GP

TOKO 10 X 11.15 X 4 mm
DCR: 0.64 +-7% m ohm
Idc :32A , Isat : 32A

PR4707 1K5R2F-2-GP
PR4708 3K01R2F-3-GP
PR4719 NTC-10K-27-GP-U
PR4709 7K5R2F-1-GP
close choke



PWR_VCCGI_PH
Panasonic 7.3 * 4.3 * 1.9 mm
ESR: 9 m ohm
PR4722 2D2R5F-2-GP
22uF_6.3V_0805 *8pcs
DY*2pcs
PWR_VCCGI_SNUB
PC4715 SC1KP50V2KX-L-1-GP

PC4717 SC56P50V2JN-2GP
PR4710 0R0402-PAD-1-GP
PWR_VCCGI_CSPA

close PMIC
PC4714 SCD047U25V2KX-GP
close choke
PC4706 SCD22U25V3KX-GP
SC 0718
PC4706 change from 78.22422.2BLDL to 78.22422.2BL

PR4711 681R2F-GP

PC4707 SCD1U25V2KX-L-GP
DY

close PMIC
PC4710 SCD047U25V2KX-GP
PR4716 0R0402-PAD-1-GP

PR4712 4K3R3F-GP
DY
PC4712 SC470P50V2KX-L-GP
-1M 1228 power team: DY PC4712
PR4713 0R0402-PAD-1-GP
PC4713 SC1U10V2KX-L1-GP
PR4715 0R0402-PAD-1-GP
DY
PC4736 SCD1U25V2KX-L-GP

PWR_VCCGI_FBPA, PWR_VCCGI_FBPB, PWR_VCCGI_FBNA

PG4707 GAP-CLOSE-PWR-3-GP — PWR_VCCGI_FBPC
PG4708 GAP-CLOSE-PWR-3-GP — PWR_VCCGI_FBNB

EE
1V_CPU_VCGI
PR4717 SRN100J-3-GP
66.10136.04L
sc 0630 change to common part

<Variant Name>

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Title	5V/3D3V
Size A2	Document Number: Leia
Rev	-1M
Date: Thursday, December 28, 2017	Sheet 47 of 104

<Variant Name>

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Title: ***5V/3D3V***

Size: Custom | Document Number: **Leia** | Rev: **-1M**

Date: Thursday, December 28, 2017 | Sheet 48 of 104

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<Variant Name>

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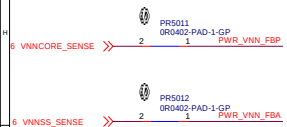
Title ***Reserved***

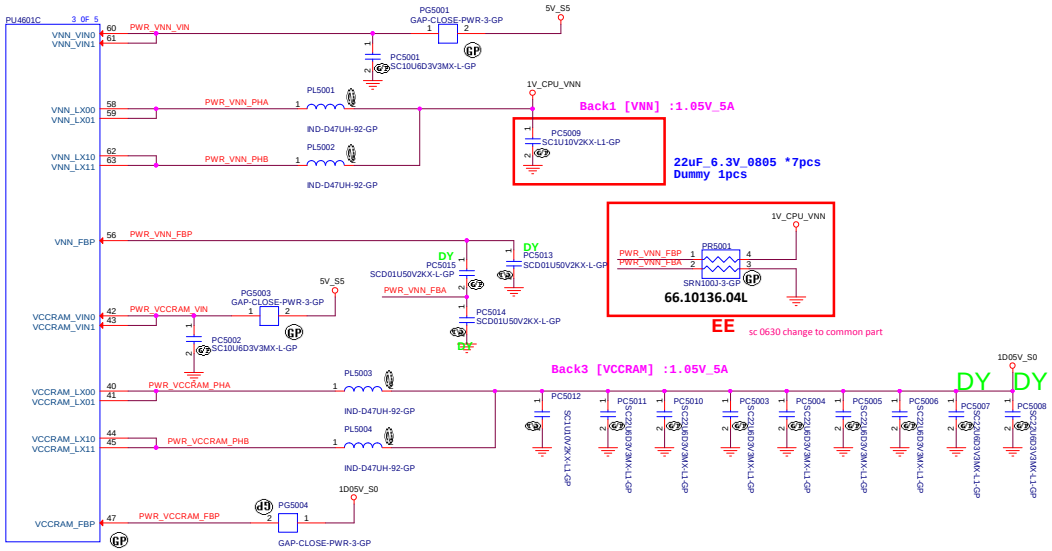
Size	Document Number	Rev
A4	**Leia**	**-1M**

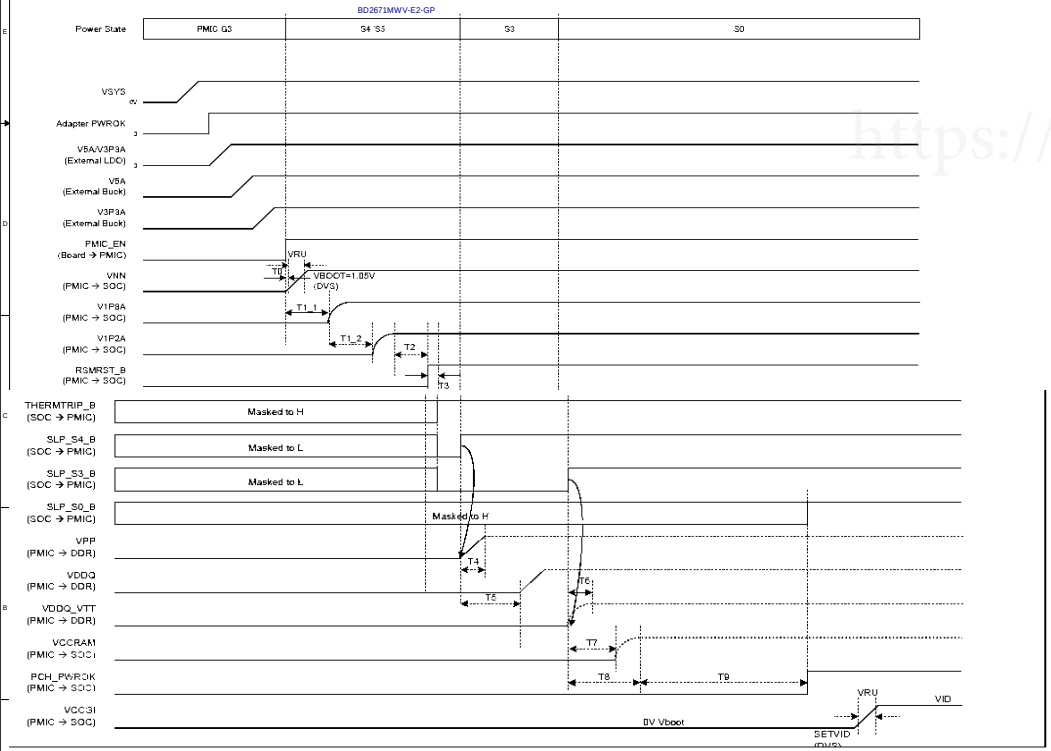
Date: Thursday, December 28, 2017 Sheet 49 of 104

OFFPAGE

VNN[BUCK1], VCCRAM[BUCK3]







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Title	5V/3D3V
Size: A2	Document Number: Leia
Rev	-1M
Date: Thursday, December 28, 2017	Sheet 50 of 104

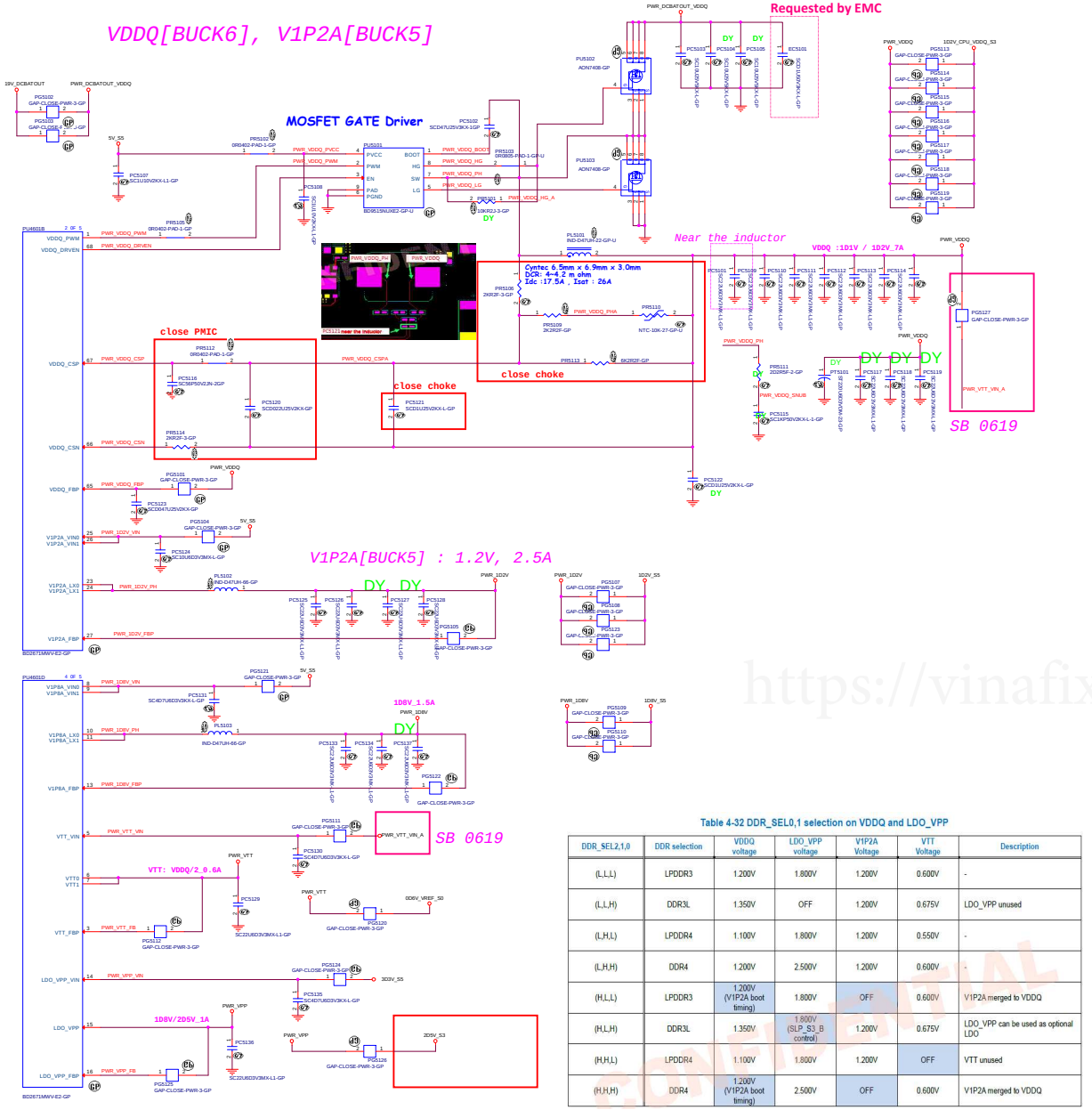

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

<Variant Name>

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Title: 5V/3D3V

Size: A1 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 51 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***5V/3D3V***

Size	Document Number	Rev
Custom	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 52 of 104

<Variant Name>

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Title: ***5V/3D3V***

Size	Document Number	Rev
A3	**Leia** Vinafix.com	**-1M**
Date: Thursday, December 28, 2017	Sheet 53 of 104	

Blanking

<Variant Name>

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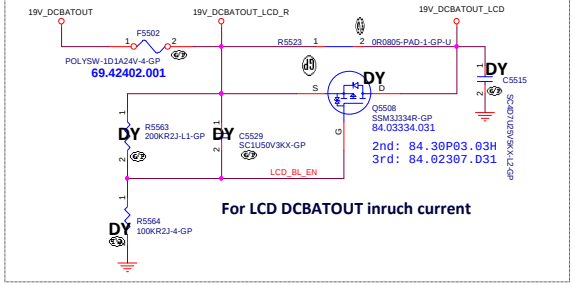
Title: ***(Reserved)1D8V***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 54 of 104

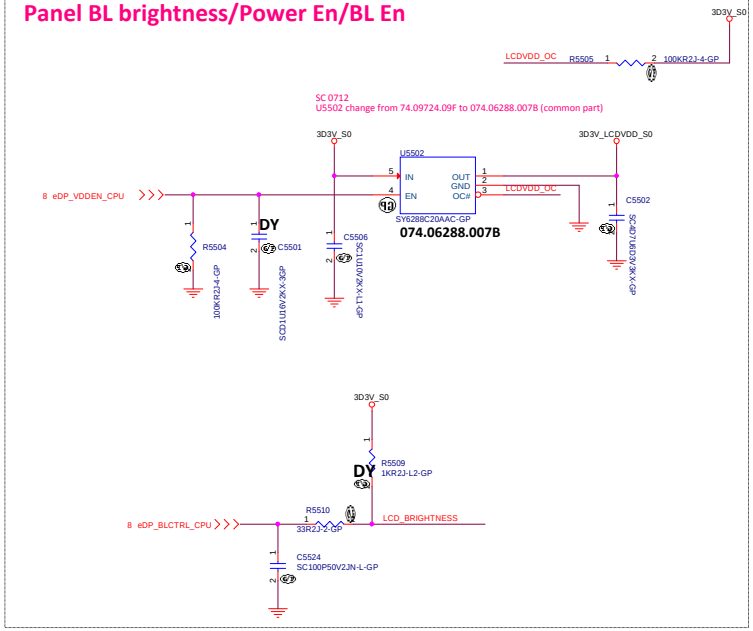
LCD+TOUCH

LCD Backlight Power



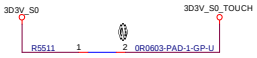
For LCD DCBATOUT inruch current

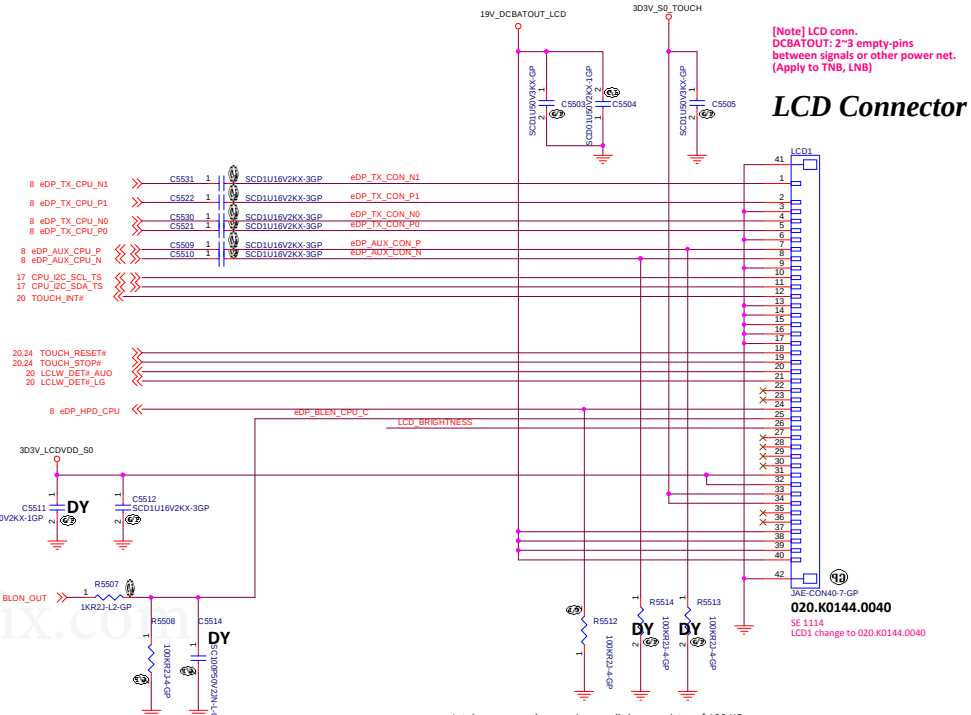
Panel BL brightness/Power En/BL En



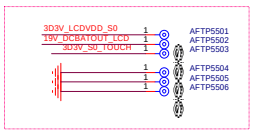
SD 0911 add

LCD CONN.		
ClamShell	PIN 20	PIN 21
NON TOUCH	HIGH	HIGH
LCLW: AUO	LOW	HIGH
LCLW: LG	HIGH	LOW





SC 0630 add AFTP



ULT

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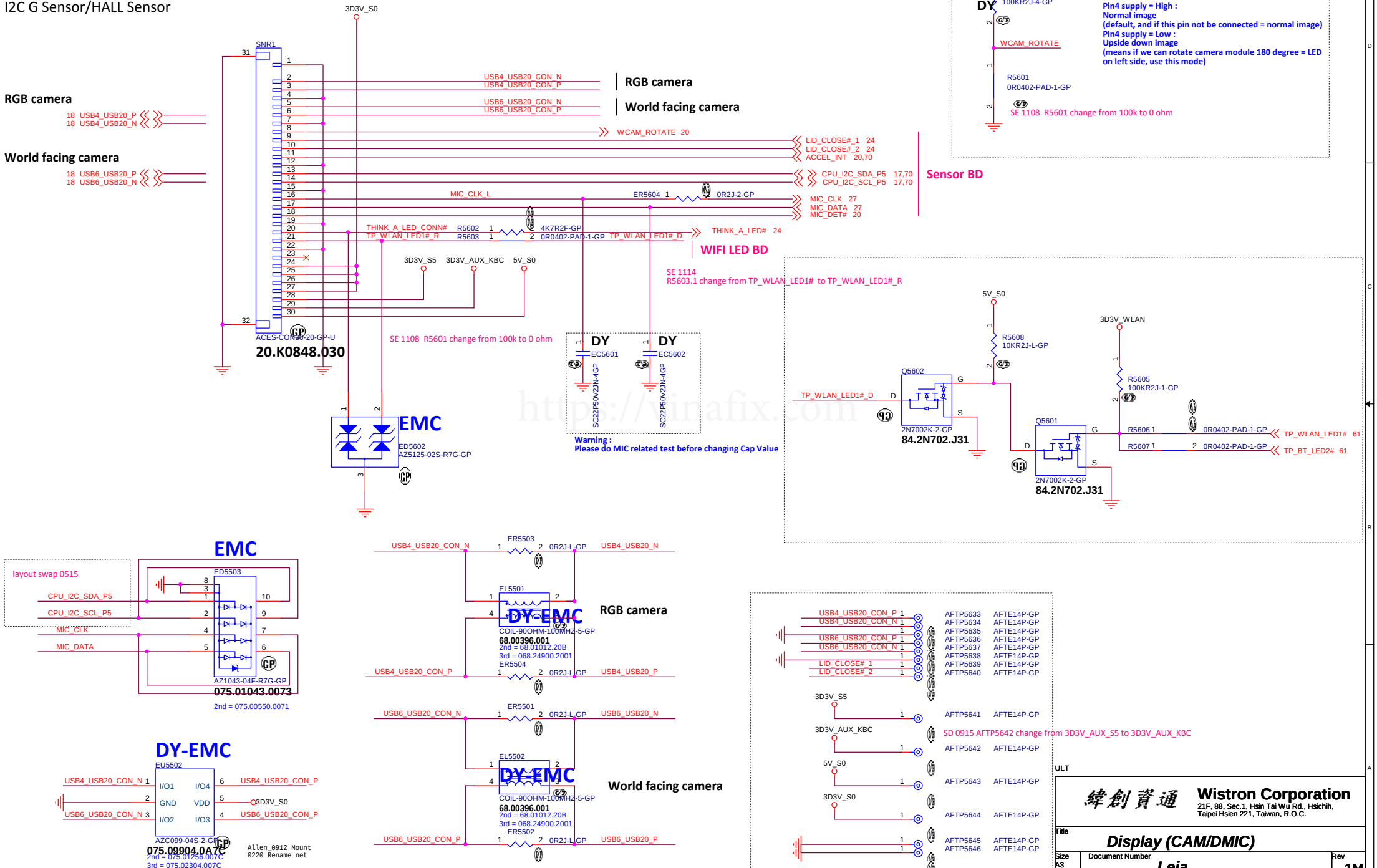
Title: Display (LCD/TOUCH)

Size	Document Number	Rev
A2	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 55 of 104

Camera Conn.

RGB/World Facing Camera with MIC
I2C G Sensor/HALL Sensor



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Title: Display (CAM/DMIC)

Size	Document Number	Rev
A3	Leia	-1M

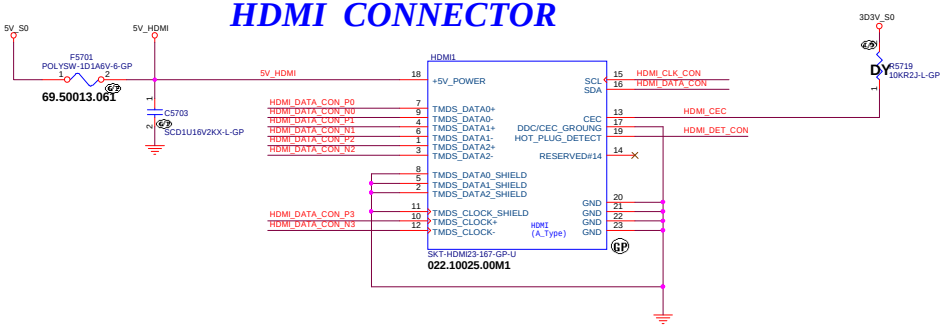
Date: Thursday, December 28, 2017 Sheet 56 of 104

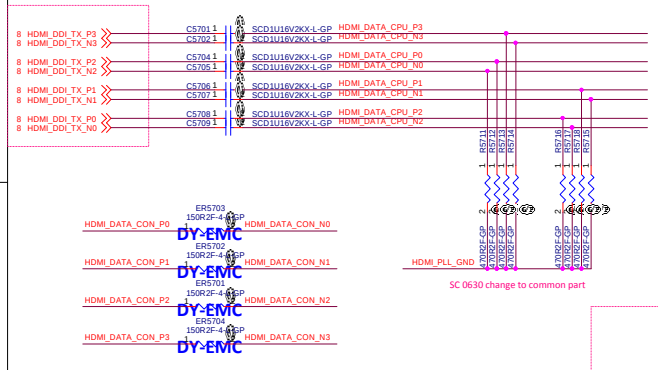
HDMI

HDMI Passive Level Shifter

Close to HDMI Connector

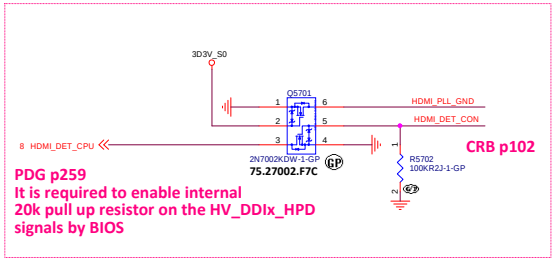
HDMI CONNECTOR



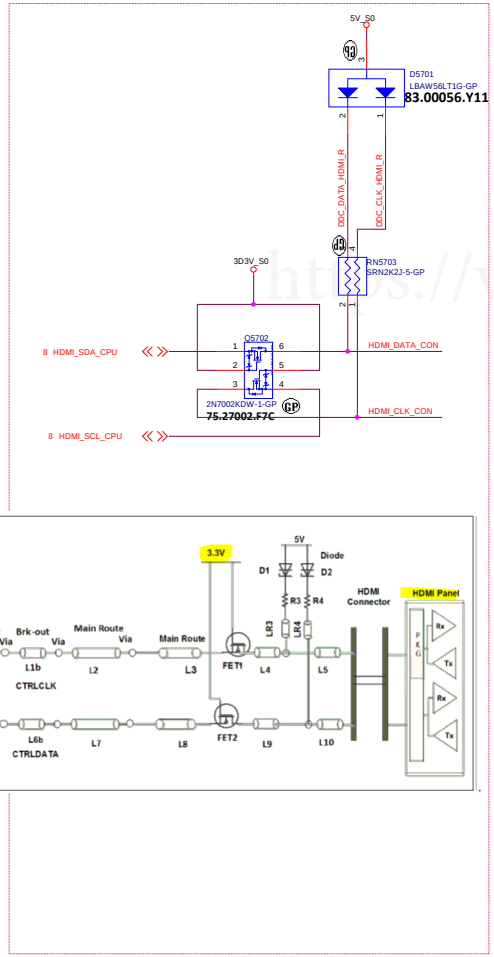


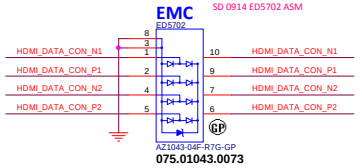
SC 0630 change to common part

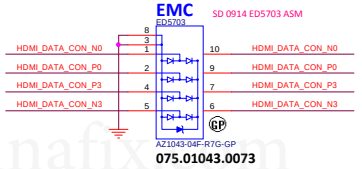
Vinafix.com

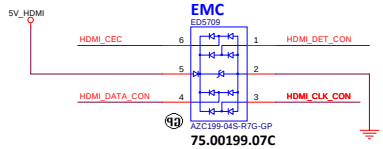


PDG p259
It is required to enable internal
20k pull up resistor on the HV_DDIx_HPD
signals by BIOS



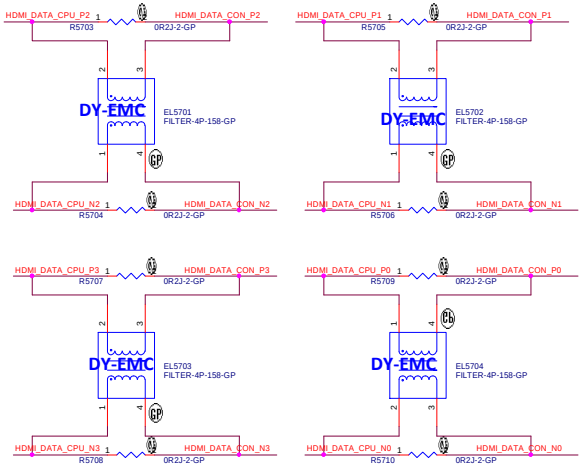


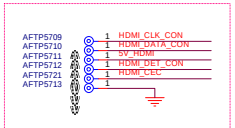




SD 0911
ED5709 change from 075.09904.0A7C to 75.00199.07C

*SD 0914
ED5709 ASM, and pin 5 conect to 5V_HDMI





ULT

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Title: Display (HDMI)

Size: A2 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 57 of 104

SSID = Display Port

Blanking

ULT

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Title: ***Display Port***

Size	Document Number	Rev
A4	***Leia***	**-1M**

Date: Thursday, December 28, 2017 Sheet 58 of 104

SSID = DVI

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ULT

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Title: *DVI*		
Size: A4	Document Number: *Leia*	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 59 of 104	

SSID = SATA

ULT

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Title: ***INT IO (HDD/ODD)***

Size	Document Number	Rev
A4	***Leia***	**-1M**

Date: Thursday, December 28, 2017 Sheet 60 of 104

WLAN(CNVi)

-1M 1212
1. CNV_BRI_RSP&CNV_RGI_RSP move to page 17
2. R6127.1 chnage to CNV_BRI_DT & PU 1D8V_S5, dummy
3. R6128.1 change to CNV_RGI_DT & PU 1D8V_S5

9560_Jefferson: 2A

3D3V_S0 R6103 1 WLAN 0R5J-5-GP 3D3V_WLAN
3D3V_S0 R6105 1 WLAN 0R5J-5-GP 3D3V_WLAN
3D3V_S5 R6104 1 CNVi 0R5J-5-GP
3D3V_S5 R6106 1 CNVi 0R5J-5-GP

J5 WLAN1 NGFF_KEY_E_75P

NP1		NP2	
	NP1		NP2
1	GND	2	3_3VAUX
3	USB_D+	4	3_3VAUX
5	USB_D-	6	LED#1
7	GND	8	PCM_CLK
9	SDIO_CLK	10	PCM_SYNC
11	SDIO_CMD	12	PCM_IN
13	SDIO_DAT0	14	PCM_OUT
15	SDIO_DAT1	16	LED#2
17	SDIO_DAT2	18	GND
19	SDIO_DAT3	20	UART_WAKE
21	SDIO_WAKE	22	UART_RX
23	SDIO_RESET		
33	GND	32	UART_TX
35	PETP0	34	UART_RTS
37	PETN0	36	UART_CTS
39	GND	38	CLINK_RESET
41	PERP0	40	CLINK_DATA
43	PERN0	42	CLINK_CLK
45	GND	44	COEX3
47	REFCLKP0	46	COEX2
49	REFCLKN0	48	COEX1
51	GND	50	SUSCLK_32KHZ
53	CLKREQ0#	52	PERST0#
55	PEWAKE0#	54	W_DISABLE
57	GND	56	RESERVED#54/W_DISABLE#2
59	RESERVED#59/2ND_LANE_PETP1	58	W_DISABLE#1
61	RESERVED#61/2ND_LANE_PETN1	60	NFC_I2C_SM_DATA
63	GND	62	NFC_I2C_SM_CLK
65	RESERVED#65/2ND_LANE_PERP1	64	NFC_I2C_IRQ/MGPIO5
67	RESERVED#67/2ND_LANE_PERN1	66	GPIO0_NFC_RESET#/MGPIO7
69	GND	68	RESERVED#66
71	RESERVED#71	70	RESERVED#68
73	RESERVED#73	72	RESERVED#70
75	GND	74	3_3VAUX
77	77	76	3_3VAUX

SKT-NGFF75P-70-GP-U1
062.10003.0401
BOM control: 62.10043.M71

DUMMY-SYMBOL

18 BT_USB20_P
18 BT_USB20_N
17 CNVI_WGR_DATA_N1
17 CNVI_WGR_DATA_P1
17 CNVI_WGR_DATA_N0
17 CNVI_WGR_DATA_P0
17 CNVI_WGR_CLK_N
17 CNVI_WGR_CLK_P
18 WLAN_PCIE_TX_P
18 WLAN_PCIE_TX_N
SCD1U16V2KX-L-GP2 1C6111 WLAN_PCIE_TX_CON_P
SCD1U16V2KX-L-GP2 1C6110 WLAN_PCIE_TX_CON_N
18 WLAN_PCIE_RX_P
18 WLAN_PCIE_RX_N
18 WLAN_CLK_CPU
18 WLAN_CLK_CPU_N
PEG_CLKREQ5_WLAN#
18 WLAN_WAKE#
17 CNVI_WT_DATA_N1
17 CNVI_WT_DATA_P1
17 CNVI_WT_DATA_N0
17 CNVI_WT_DATA_P0
17 CNVI_WT_CLK_N
17 CNVI_WT_CLK_P

3D3V_WLAN
C6102 SCD1U16V2KX-3GP
C6103 SC1U10V2KX-1GP
C6104 SC10U6D3V3MX-GP
DY

CNV_RF_RESET#_R R6120 2 1 0R0402-PAD-1-GP CNV_RF_RESET# 17
WLAN_DET_R R6134 1 2 0R0402-PAD-1-GP WLAN_DET 20 CNV_BRI_RSP 17
TP_WLAN_LED1# 56
XTAL_CLKREQ 17
TP_BT_LED2# 56
CNV_RGI_DT 17
CNV_RGI_RSP 17
CNV_BRI_DT 17
E51_RXD_R R6118 DY 1 0R2J-2-GP E51_RXD 24
E51_TXD_R R6121 DY 1 0R2J-2-GP E51_TXD 24
PM_SUSCLK 19
PERST0# W_DISABLE R6122 2 1 0R0402-PAD-1-GP BLUETOOTH_EN 24
WIFI_RF_EN_CON R6124 2 1 1KR2J-L2-GP WIFI_RF_EN 24
CLKIN_XTAL_LCP 17

1D8V_S5
CNV_BRI_DT R6127 1 DY 2 20KR2J-L2-GP
CNV_RGI_DT R6128 1 DY 2 20KR2J-L2-GP
3D3V_WLAN
BLUETOOTH_EN R6129 1 100KR2J-1-GP
WIFI_RF_EN R6130 1 100KR2J-1-GP
XTAL_CLKREQ R6126 75KR2F-GP
CNV_RF_RESET#_R R6125 75KR2F-GP
PERST0# DY R6131 75KR2F-GP

SC 0713
pin 52 PD 100k ????

3D3V_S0 R6136 10KR2J-L-GP DY
R6123 DY 1 0R2J-2-GP PLT_RST# 19,24,31,40,63,68,91,99
R6135 DY 1 0R2J-2-GP WLAN_RST# 24

SE 1108
1. add R6135 for WLAN_RST#, and DY
2. add R6136 to 3.3V_S0 for PU,and DY

Vinafix.com

3D3V_WLAN Q6102 LTC015TEBFS8TL-GP 84.00015.B1H DY
PEG_CLKREQ5_WLAN# R6109 1 2 0R0402-PAD-1-GP WLAN_CLKREQ_CPU_N 18

3D3V_WLAN
R6110 1 2 100KR2F-L1-GP WLAN_WAKE# SC0717
R6111 1 DY 2 100KR2F-L1-GP WLAN_CLKREQ_CPU_N

SD 0913 add R6111/100k ,and PU 3D3V_WLAN for WLAN_CLKREQ_CPU_N,but DY it

SC 0717
WLAN_DET_R R6132 100KR2J-1-GP
Q6101 DY 2N7002K-2GP 84.2N702.J31
2nd = 084.27002.0L31
3rd = 84.2N702.031
3D3V_WLAN_S0_EN
3D3V_S0 R6133 10KR2J-L-GP DY

E51_TXD R6102 2KR2J-1-GP DY
C6113 SC1U10V2KX-L1-GP

3D3V_S5
C6105 SC10U6D3V3MX-L-GP DY
C6106 SC1U10V2KX-L1-GP DY
3D3V_S0
C6107 SC10U6D3V3MX-L-GP DY
C6108 SC1U10V2KX-L1-GP DY

5V_S5
SC 0717
U6101 DY
VBIAS
IN1#1 IN1#2 IN2#6 IN2#7
EN1 EN2
CT1 CT2
OUT1#13 OUT1#14 OUT2#8 OUT2#9
GND
THERMAL_PAD
G2898KD1U-GP
074.02898.0093
2nd = 074.22976.0091
WLAN_DET
3D3V_WLAN_S0_EN
SW_WLAN_S5_CT C6114 DY 2 SC470P50V2KX-L-GP
SW_WLAN_S0_CT C6115 DY 1 SC1KP50V2KX-L-1-GP
3D3V_WLAN
3.5A
C6116 SCD1U16V2KX-L-GP DY
C6117 SCD1U16V2KX-L-GP DY
ULT

BT_USB20_N
BT_USB20_P
ED6101 DY-EMC
I/O1 I/O2 I/O3 I/O4
AZC099-04S-2-GP
075.09904.0A7C
0418 LKL
3D3V_WLAN

3D3V_WLAN
AFTP6101
AFTP6103

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Title	INT IO (WLAN M.2)	
Size A3	Document Number Leia	Rev -1M
Date: Thursday, December 28, 2017	Sheet 61 of 104	

SSID = WWAN

Blanking

ULT

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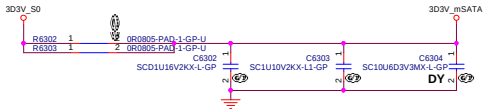
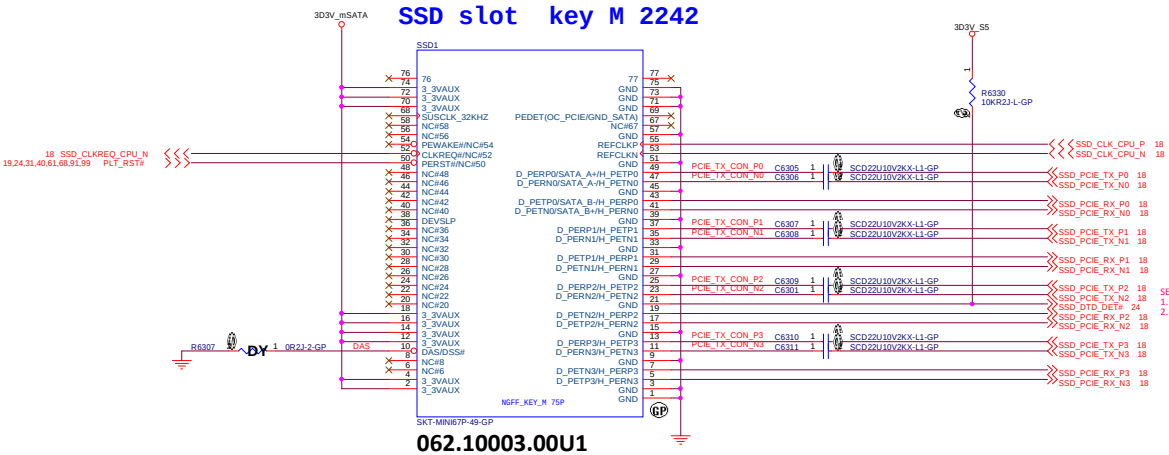
Title: ***WWAN***		
Size: A4	Document Number: ***Leia***	Rev: **-1M**
Date: Thursday, December 28, 2017	Sheet 62 of 104	

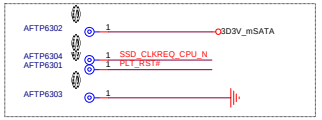
M.2 SSD



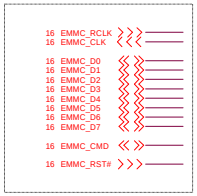


062.10003.00U1

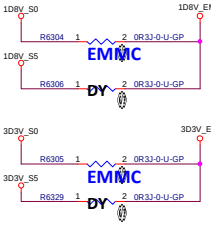
SE 1108
1. Remove GND on SSD1.21, and connect to SSD_DTD_DET# for Device Tamper Detection
2. add R6330 to 3.3V_S5 for SSD_DTD_DET#

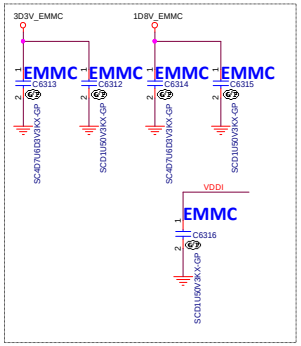


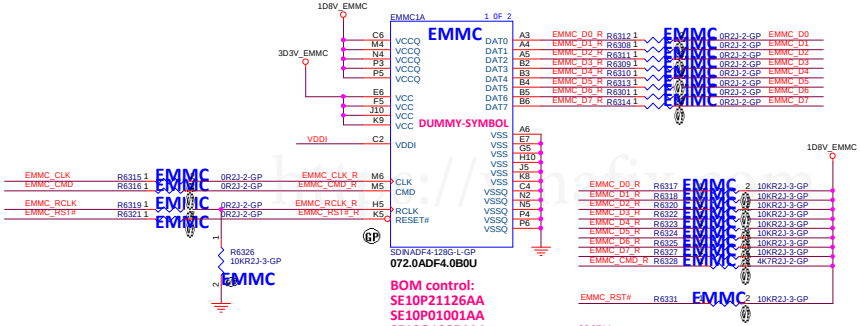
eMMC



SC 0712 remove U6301 load switch add 0ohm

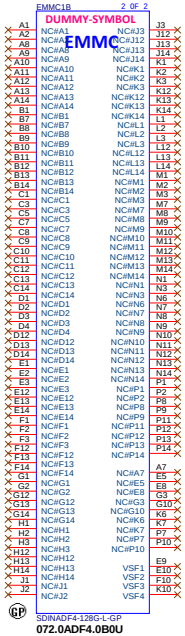






BOM control:
SE10P21126AA
SE10P01001AA
SE10Q12854AA
SE10P17869AA

SC 0711
Connected to EMMC RESET Pin with Pull up Resistor



mi 0418
follow INAND 7232 16-128GB data sheet

EMMC (colay)

Vendor	Vendor PN	Wisrton PN	
SANDISK	SDINADF4-128-1001K	SE10P21126AA IC EMMC 128GB SDINADF4-128-1001K BGA153P	FVT SKU#1_CS
SAMSUNG	KLMCG4JETD-B041	SE10P01001AA IC EMMC 64GB KLMCG4JETD-B041 FBGA153P	FVT SKU#3_CS
SAMSUNG	KLMDG4UCTA-B041	SE10Q12854AA IC EMMC 128GB KLMDG4UCTA-B041 FBGA153P	FVT SKU#5_YG
SANDISK	SDINADF4-64G-1001K	SE10P17869AA IC EMMC 64GB SDINADF4-64G-1001K FBGA153P	FVTSKU#6_YG

ULT

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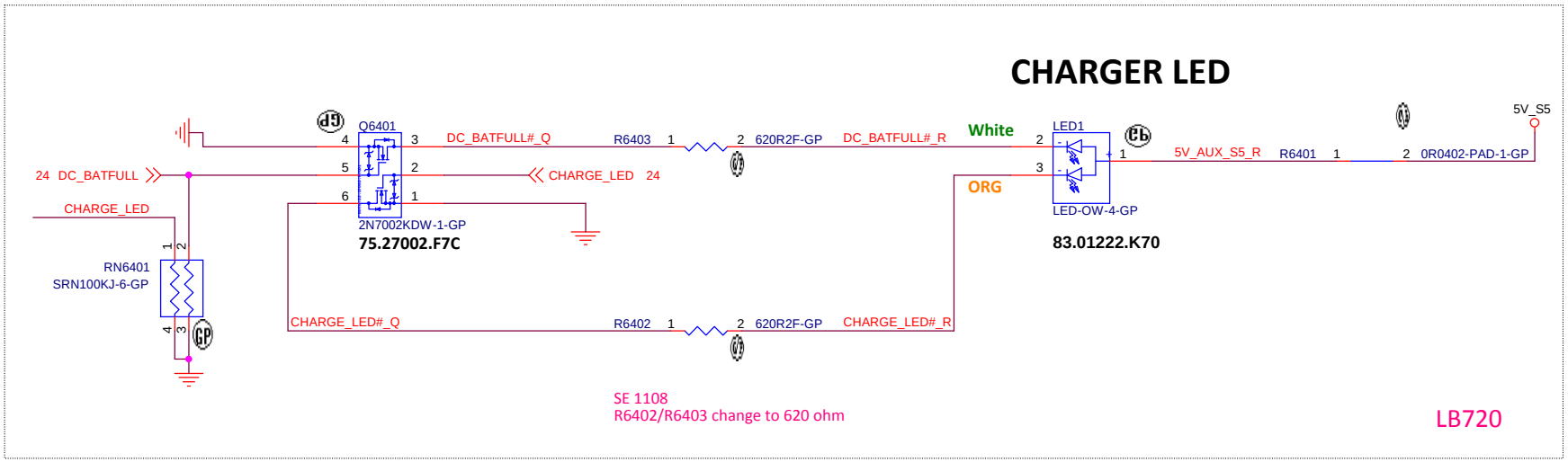
Title: **INT IO (SSD M.2/ eMMC)**

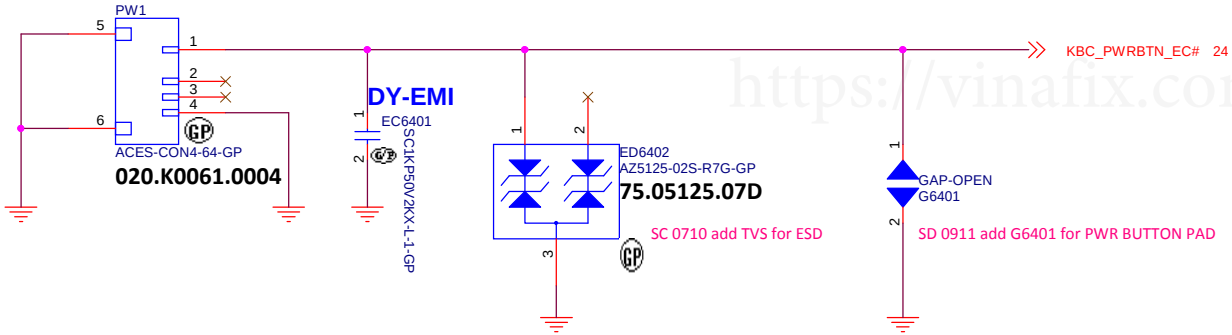
Size	Document Number	Rev
A2	Leia	-1M

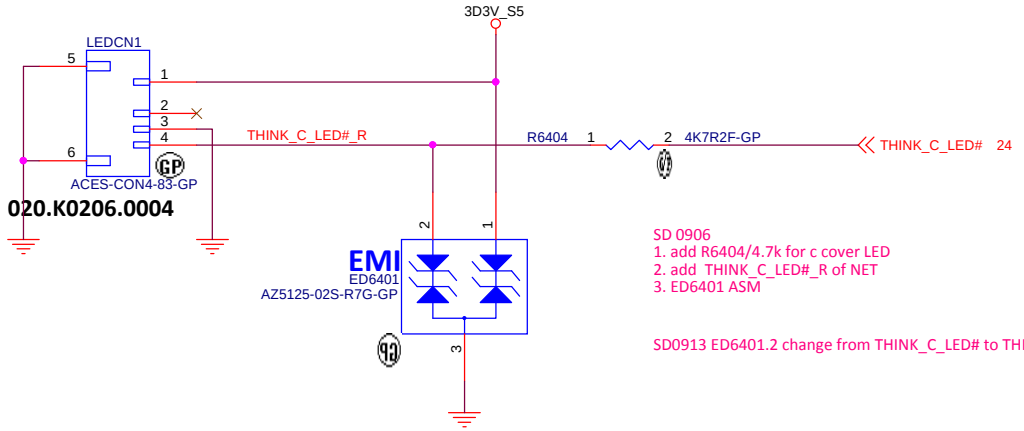
Date: Thursday, December 28, 2017 Sheet 63 of 104

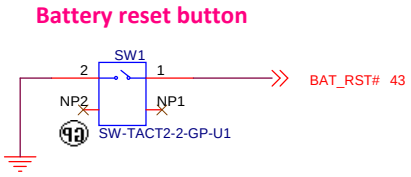
LED / PWRBTN

CHARGER LED

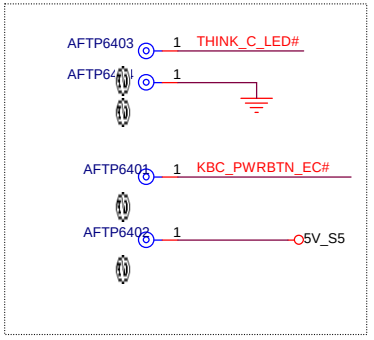








SD 0914 AFTP6403 change from CHARGE_LED to THINK_C_LED#_R



ULT

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Title: LED Board/Power Button		
Size: Custom	Document Number: Leia	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 64 of 104	

KB / TOUCH PAD

24 KROW[0..7]
24 KCOL[0..15]

24 HOTKEY

SC 0710 change to 100 ohm

24 ESC_LED — Q6501 — R6504 100KR2J-1-GP — 2N7002K-2-GP — 84.2N702.J31 — ESC_LED_D — R6512 — 100R2F-L1-GP-U — LED1

24 F1_LED — Q6502 — R6507 100KR2J-1-GP — 2N7002K-2-GP — 84.2N702.J31 — F1_LED_D — R6513 — 100R2F-L1-GP-U — LED2

24 F4_LED — Q6503 — R6508 100KR2J-1-GP — 2N7002K-2-GP — 84.2N702.J31 — F4_LED_D — R6515 — 100R2F-L1-GP-U — LED3

24 CAP_LED — Q6504 — R6509 100KR2J-1-GP — 2N7002K-2-GP — 84.2N702.J31 — CAP_LED_D — R6516 — 100R2F-L1-GP-U — LED4

LB720

SC 0626

KEYBOARD CONN

KB1 — HRS-CON32-8-GP

KROW3 KROW7 KROW6 KCOL14 KROW4 KROW1 KCOL0 KROW2 KROW0 KCOL4 KCOL2 KROW5 KCOL1 KCOL3 KCOL6 KCOL7 KCOL5 KCOL15 KCOL13 KCOL9 KCOL12 KCOL10 KCOL8 KCOL11 LED1 LED2 LED3 HOTKEY LED4

3D3V_S0

EC6502 EC6503 EC6504 EC6505 EC6506 EC6507 EC6508 EC6509 EC6510 EC6511 EC6512 EC6513 EC6514 EC6515 EC6516 EC6517 EC6518 EC6519 EC6520 EC6521 EC6522 EC6523 EC6524 EC6525 EC6526 — DY-EMI — SRN4P50V2KX-3GP

020.K0333.0032

Assign	Purpose
VCC	VCC 3V For LED
LED1	LED For Esc
LED2	LED For F1
LED3	LED For F4
LED4	LED For CapsLK

SC 0627

Sense (S1 ~ S8) / **Drive (D1 ~ D16)**

	SENSE 0	SENSE 1	SENSE 2	SENSE 3	SENSE 4	SENSE 5	SENSE 6	SENSE 7	HOT KEY
DRV0	1	2	17	16	31	110	46	131	
DRV1	112	3	18	30	32	45	47		
DRV2	113	4	19	114	33	115	48		
DRV3	6	5	20	21	34	35	49	50	
DRV4	7	8	23	22	37	36	52	51	
DRV5	13	9	24	28	38	117	53	56	
DRV6	119	10	25	118	39	132	54	133	
DRV7	12	11	26	27	40	41	42	55	
DRV8	120	121	14	15	29	116	43	61	
DRV9	75	123	104	Win				89	
DRV10	76	122	EZ3	EZ2	EZ4	EZ1		84	
DRV11	85	86	130	129	App		INB	INF	
DRV12	80	81	128	127		83	126	79	
DRV13		124	125			60		62	
DRV14				44			57		
DRV15	58						64		
DRV16	105	96	100	95	91	90	101	106	
DRV17	93	103	102	97	98	92	108	99	
GND									Fn

This matrix has some unnecessary mappings (e.g. 125, EZ#, etc.) due to universal use purpose.

Membrane Pin

Pin #	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	NC

0523

TOUCH PAD CONN

3D3V_S0 — R6505 10KR2J-L-GP — R6503 0R0402-PAD-1-GP — RN6501 SRN4K7J-8-GP

mi0505
24 PAD_DISABLE
24 PS2_DATA
24 PS2_CLK
24 TP_LID_CLOSE#
17,36,99 CPU_SMB_SDA
17,36,99 CPU_SMB_SCL

CLICK1 — FUSEVCC3B — AFTP6510 AFTP6511 — HRS-CON12-8-GP

20.K0824.012

Lid close	
L	Dis touchpad
H	EN touchpad

75.05125.07D
2nd = 075.05011.007D
3rd = 075.52215.007D

ED6501 ED6502 — AZ5125-02S-R7G-GP

EMC DY-EMC

ULT

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Title: INT IO (KB/TP)
Size: A2 | Document Number: Leia | Rev: -1M
Date: Thursday, December 28, 2017 | Sheet 65 of 104

Active PEN Charger

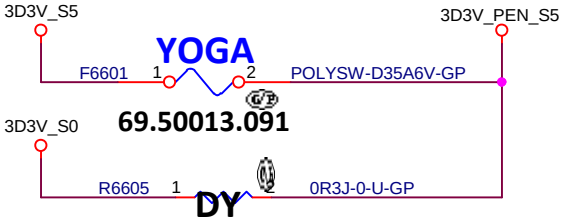
SC 0711 change location

SC 0719 remove pen function

SC 0727 add pen function

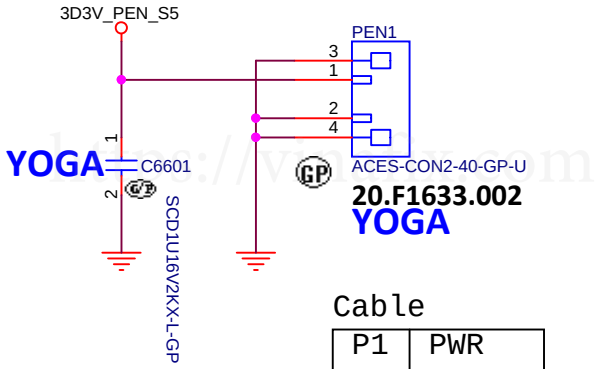
SD 0907
1. remove PEN_DCT#/SW2/TP6611
2. PEN1 change from 020.F0111.0004 to 20.F1633.002
3. remove R6602/Q6601/C6602 /R6601/C6603/EC6601/R6630/R66293
4. Pen Power rail chamge from 3D3V_S0 to 3D3V_PEN_S5

SD 0914
R6606 change to F6601



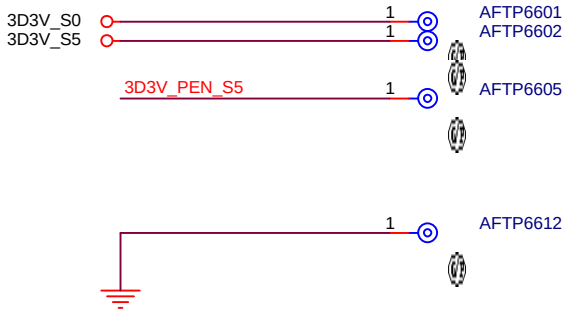
Max Current = 200(mA)

PEN Charger CONN



Cable

P1	PWR
P2	GND



ULT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: IO Board Connector		
Size: A4	Document Number: Leia	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 66 of 104	

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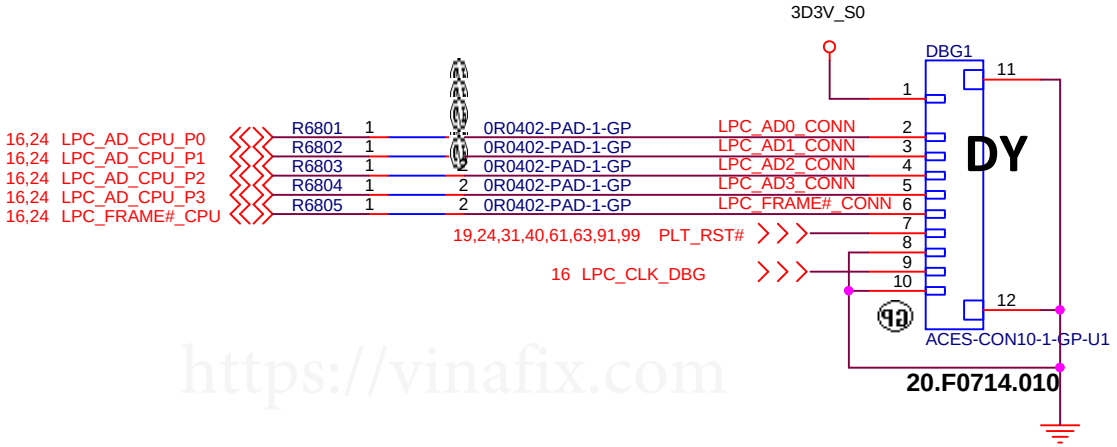
ULT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Sensor (Hall-Sensor)***
Size: A4	Document Number: ***Leia***
Rev: **-1M**	
Date: Thursday, December 28, 2017	Sheet 67 of 104

Debug CONN

SC 0627 remove DBG1 conn



ULT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Debug (LPC conn)*		
Size: A4	Document Number: *Leia*	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 68 of 104	

SSID = Sensor

Blanking

ULT

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Taipei Hsien 221, Taiwan, R.O.C.

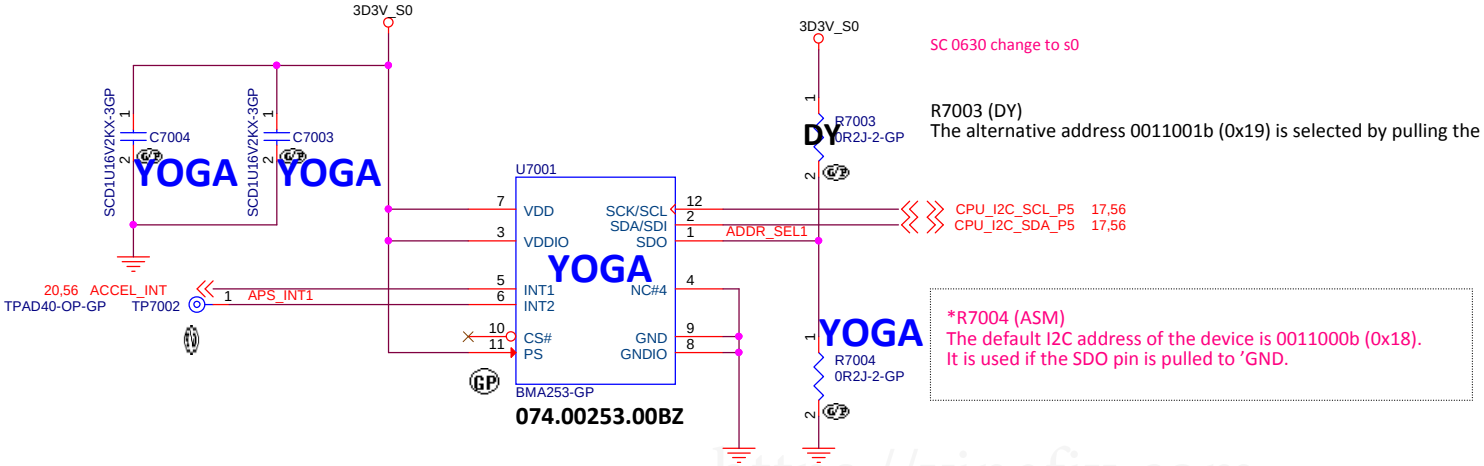
Title: E-compass/GYRO

Size: A4 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 69 of 104

G Sensor

Angle Calculation (I2C)



R7003 (DY)
The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V DDIO '.

*R7004 (ASM)
The default I2C address of the device is 0011000b (0x18).
It is used if the SDO pin is pulled to 'GND.

BOMcontrol
074.00253.00BZ -> 074.00253.M001

ULT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Sensor (G-sensor BMA253)*		
Size: Custom	Document Number: *Leia*	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 70 of 104	

Blanking

<Variant Name>

緯創資通 Wistron Corporation
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Title

Thunderbolt (1/5)

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 71 of 104

Blanking

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (2/5)

Size	Document Number		Rev
A4	**Leia**	teknisi indonesia	**-1M**
Date: Thursday, December 28, 2017		Sheet 72 of 104	

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Thunderbolt (3/5)***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 73 of 104	

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 74 of 104

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Thunderbolt (5/5)***
Size: A4	Document Number: **Leia**
Rev: **-1M**	
Date: Thursday, December 28, 2017	Sheet 75 of 104

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU (1/5) PEG***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 76 of 104	

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU (2/5) DIGITAL***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 77 of 104	

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU (3/5) VRAM***
Size: A4	Document Number: **Leia**
Rev: **-1M**	
Date: Thursday, December 28, 2017	Sheet 78 of 104

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU (4/5) GPIO***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 79 of 104	

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (5/5) PWR/GND***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 80 of 104

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM1,2 (1/4)***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 81 of 104	

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM3,4 (2/4)***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 82 of 104	

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VRAM5,6 (3/4)***	
Size: A4	Document Number: **Leia**	Rev: **-1M**
Date: Thursday, December 28, 2017	Sheet 83 of 104	

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VRAM7,8 (4/4)*		
Size: A4	Document Number: Leia	Rev: -1M
Date: Thursday, December 28, 2017	Sheet 84 of 104	

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VGA_CORE***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 85 of 104	

Blanking

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DISCRETE VGAPOWER***
Size: A4	Document Number: **Leia**
Rev: **-1M**	
Date: Thursday, December 28, 2017	Sheet 86 of 104

Blanking

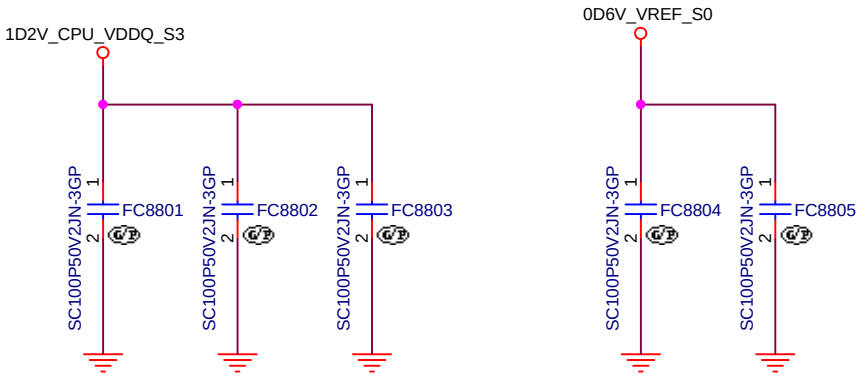
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserve)***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 87 of 104



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS (RF)***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 88 of 104

SPR1
SPRING-63-GP

SPR2
SPRING-63-GP

EMI Clip

H2
HOLE170X130R138X99-GP
ZZ.SCREW.S91

H3
HOLE233R142-GP-U1
ZZ.00PAD.5S1

H4
HOLE233R142-GP-U1
ZZ.00PAD.5S1

H5
HOLE233R142-GP-U1
ZZ.00PAD.5S1

H6
HOLE233R142-GP-U1
ZZ.00PAD.5S1

HS2
STFT237B142R113H47-GP
434.0DA01.0001

H23
HT6BE75R26-U-45-GP
ZZ.00PAD.EH1

H12
HOLE237R103-GP
ZZ.00PAD.EJ1

H13
HT85B95X975R29-S-GP
ZZ.00PAD.D71

H17
HT85B95X975R29-S-GP
ZZ.00PAD.D71

SC 0626

H19
HT85B95X975R29-S-GP
ZZ.00PAD.D71

SC 0623

H22
HOLE315R95-GP
ZZ.00PAD.911

ZZ.00PAD.D71 for thermal modify screw punch design
0428

SC 0628 remove H24 H25

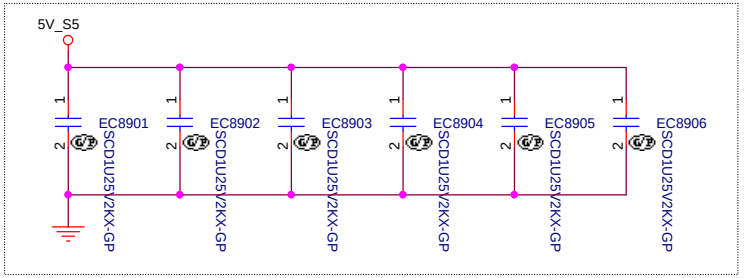
layout modify footprint&P/N

H14
HOLE315R95-GP
ZZ.0LEIA.0KB

H15
HOLE315R95-GP
ZZ.0LEIA.0KB

H16
HOLE315R95-GP
ZZ.0LEIA.0KB

0519



-1 1123
EC8901,EC8902,EC8903,EC8904,EC8905,EC8906 are ASM

ULT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS (ME/EMI Caps)***

Size: Custom | Document Number: ***Leia*** | Rev: **-1M**

Date: Thursday, December 28, 2017 | Sheet 89 of 104

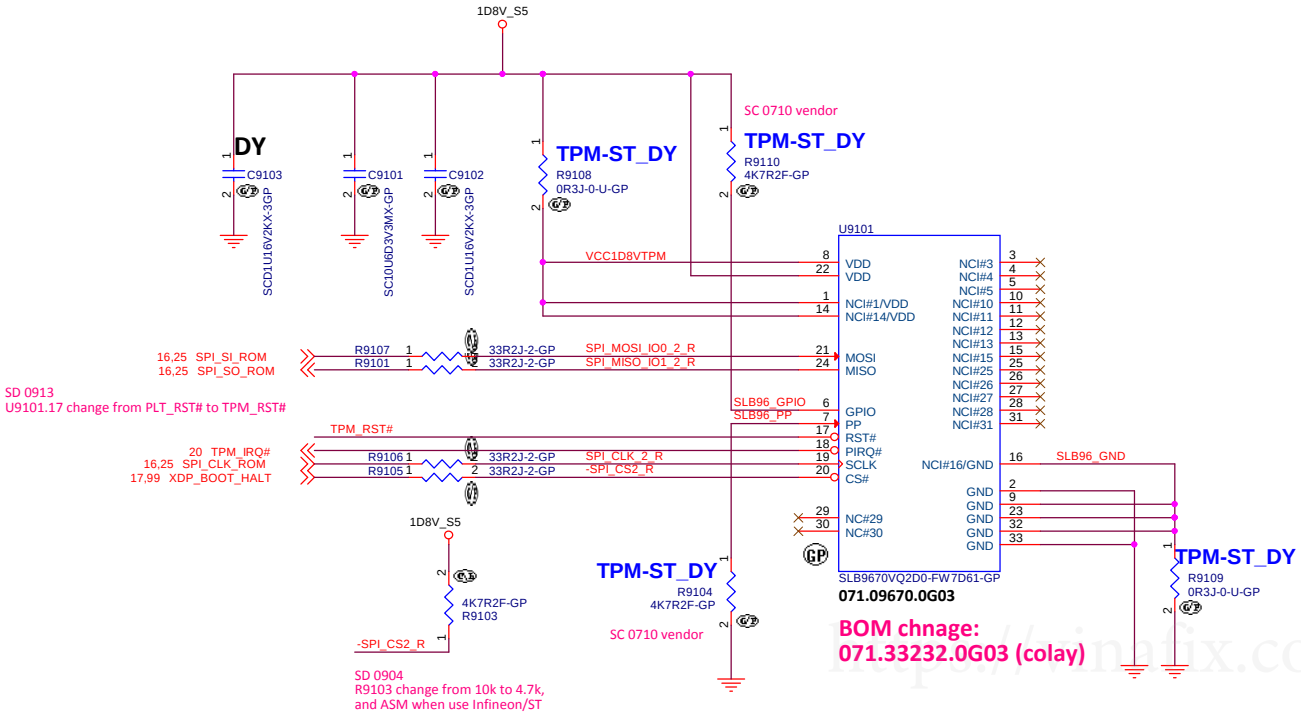
Blanking

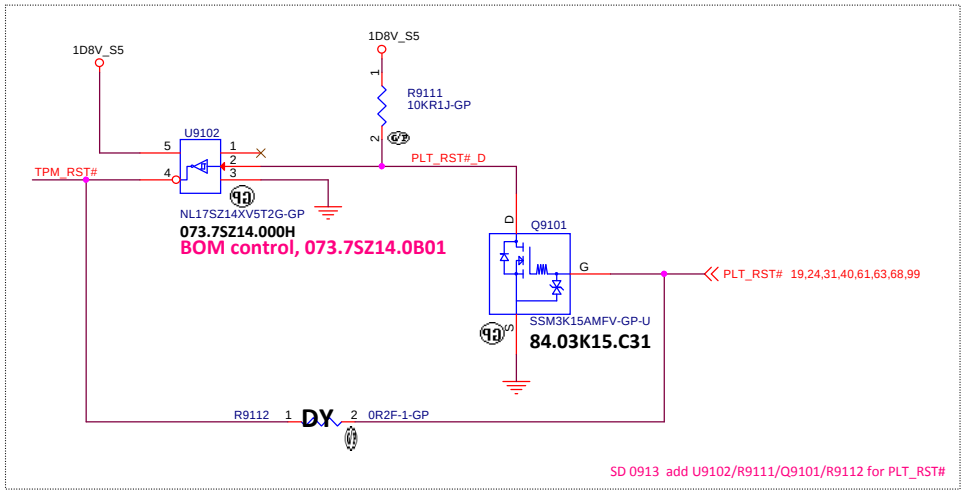
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***NFC***	
Size A4	Document Number **Leia**	Rev **-1M**
Date: Thursday, December 28, 2017	Sheet 90 of 104	

TPM 2.0





TABLE

Pin No	Infineon SLB9670VQ2.0 FW7.61	ST ST33HTPH2E32AHB4
1	VDD	NC
2	GND	GND
3	NCI	NC
4	NCI	NC
5	NCI	NC
6	GPIO	GPIO
7	PP	PP
8	VDD	NC
9	GND	NC
10	NCI	NC
11	NCI	NC
12	NCI	NC
13	NCI	NC
14	VDD	NC
15	NCI	NC
16	GND	NC
17	RST#	SPI_RST#
18	PIRQ#	SPI_PIRQ#
19	SCLK	SPI_CLK
20	CS#	SPI_CS#
21	MOSI	MOSI
22	VDD	VPS
23	GND	NC
24	MISO	MISO
25	NCI	NC
26	NCI	NC
27	NCI	NC
28	NCI	NC
29	NC	NC
30	NC	NC
31	NCI	NC
32	GND	NC

-1 1123 update

U9101 (colay)

Vendor	Vendor PN	Wisrton PN
Infineon	SLB9670VQ2.0 FW7.63	071.09670.0H03 (not MP) IC TPM SLB9670VQ2.0 FW7.63 VQFN 32P
ST	ST33HTPH2E32AHB4	071.33232.0G03 /SL80L81401AE IC TPM2.0 ST33HTPH2E32AHB4 VQFN 32P

SC 0713
071.33232.0G03 FW has fixed a missing message problem under Windows OS that existed in 071.33232.0E03.

ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM 2.0

Size: A3 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 91 of 104

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Print***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 92 of 104

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Express Card***

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 93 of 104

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Smart Card Socket***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 94 of 104

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SW GFX eDP

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 95 of 104

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Bottom Docking

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 96 of 104

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN***

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 97 of 104

Blanking

<Variant Name>

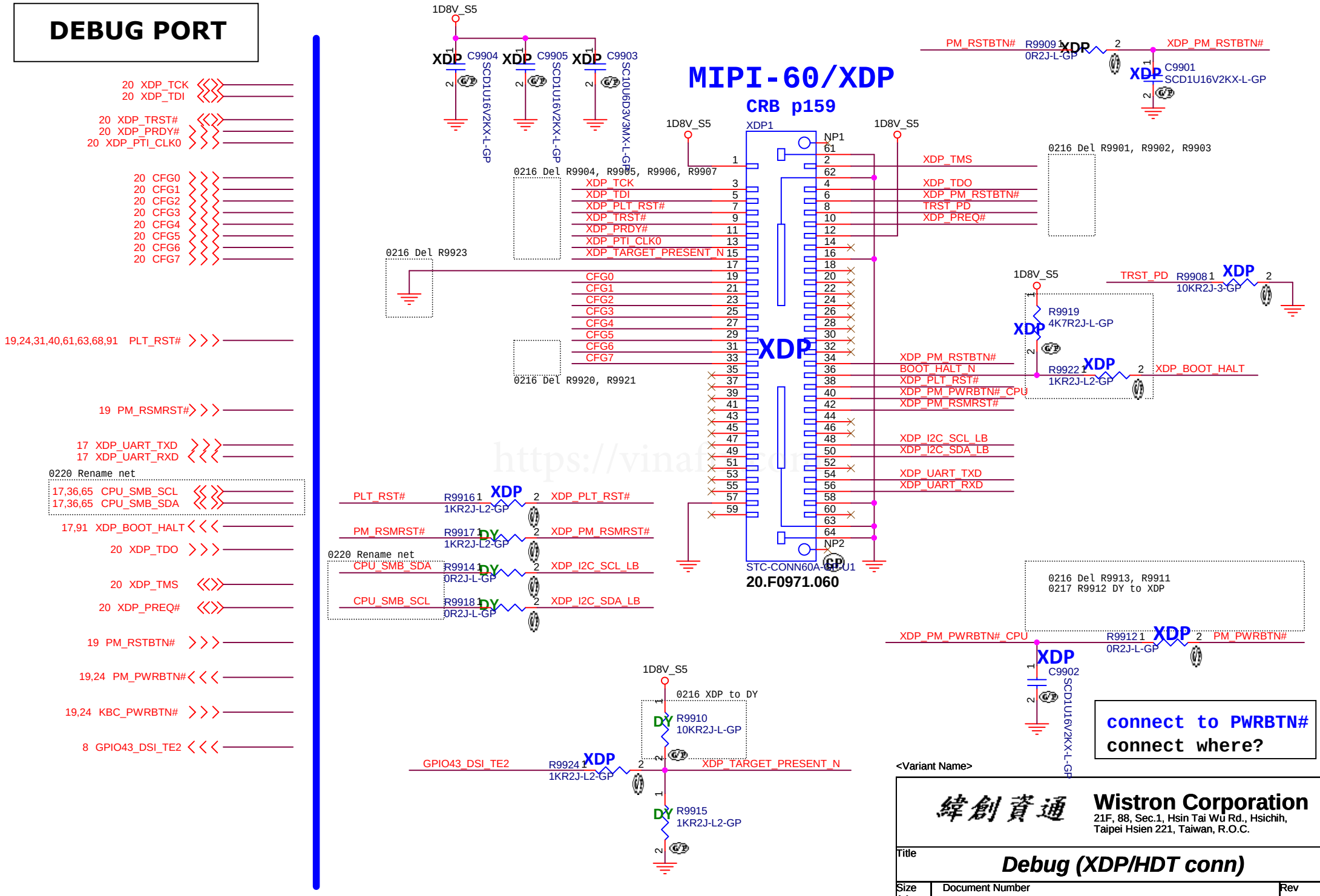
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LAN SWITCH

Size	Document Number	Rev
A4	**Leia**	**-1M**

Date: Thursday, December 28, 2017 Sheet 98 of 104

DEBUG PORT



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Debug (XDP/HDT conn)	
Size A4	Document Number Leia	Rev -1
Date: Thursday, December 28, 2017	Sheet 99 of 104	

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Table of Content*

Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 100 of 104

Blanking

<Variant Name>

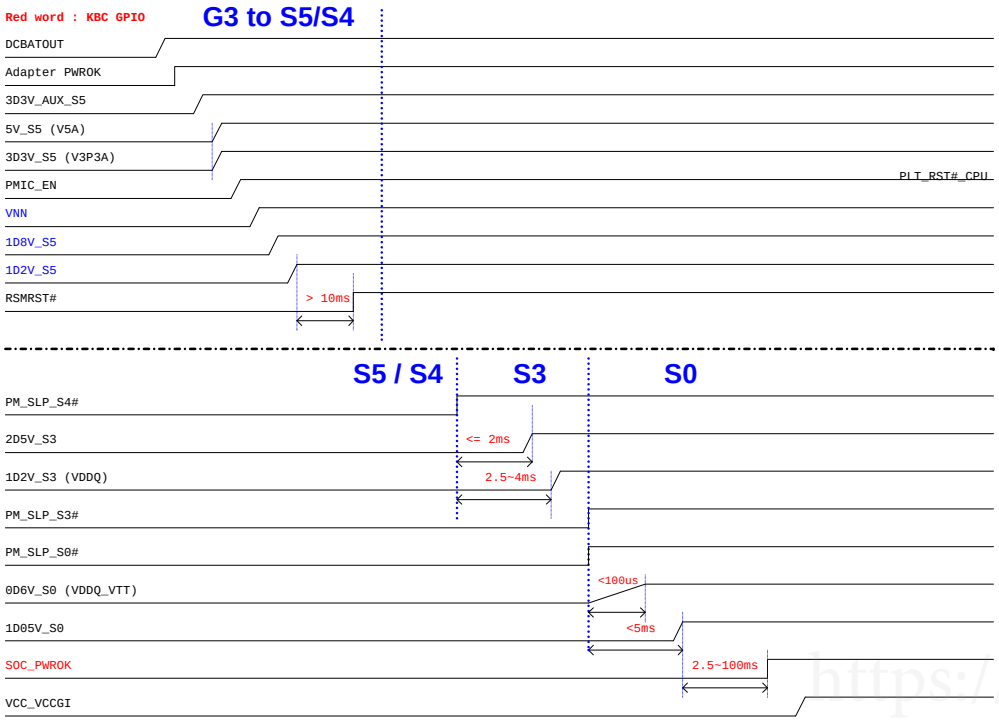
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

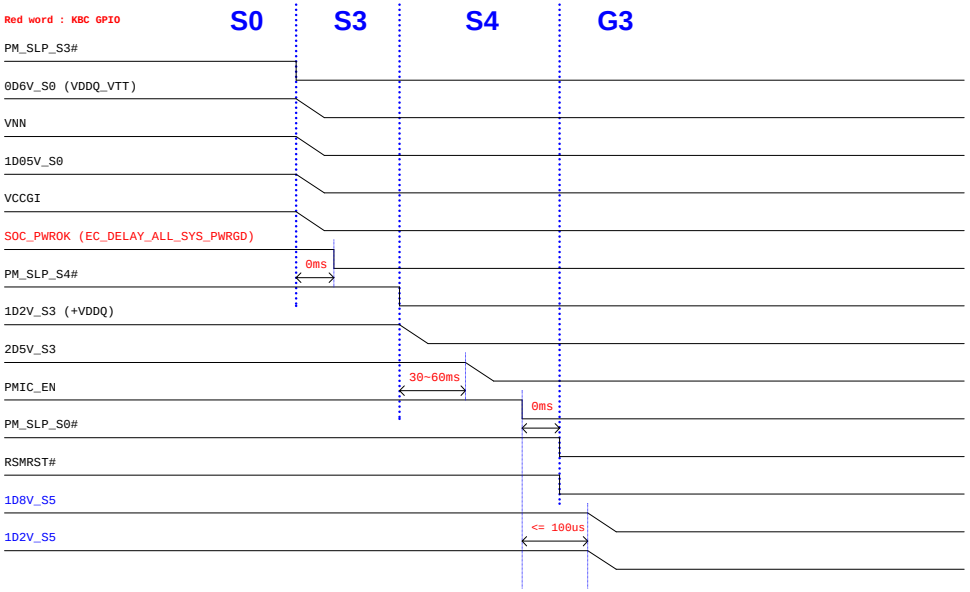
Size	Document Number	Rev
A4	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 101 of 104

Intel-Power Up Sequence



Intel-Power Down Sequence



<Variant Name>

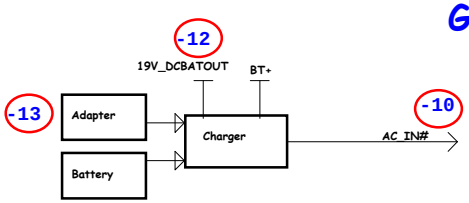
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

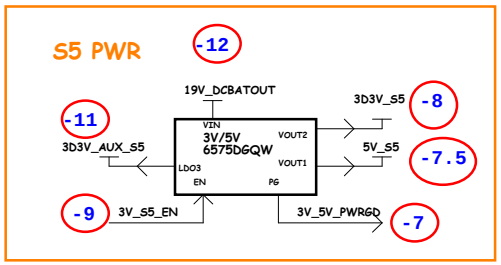
Title: Power Sequence

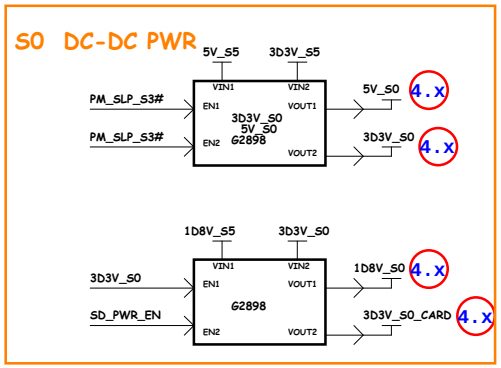
Size	Document Number	Rev
A2	Leia	-1M

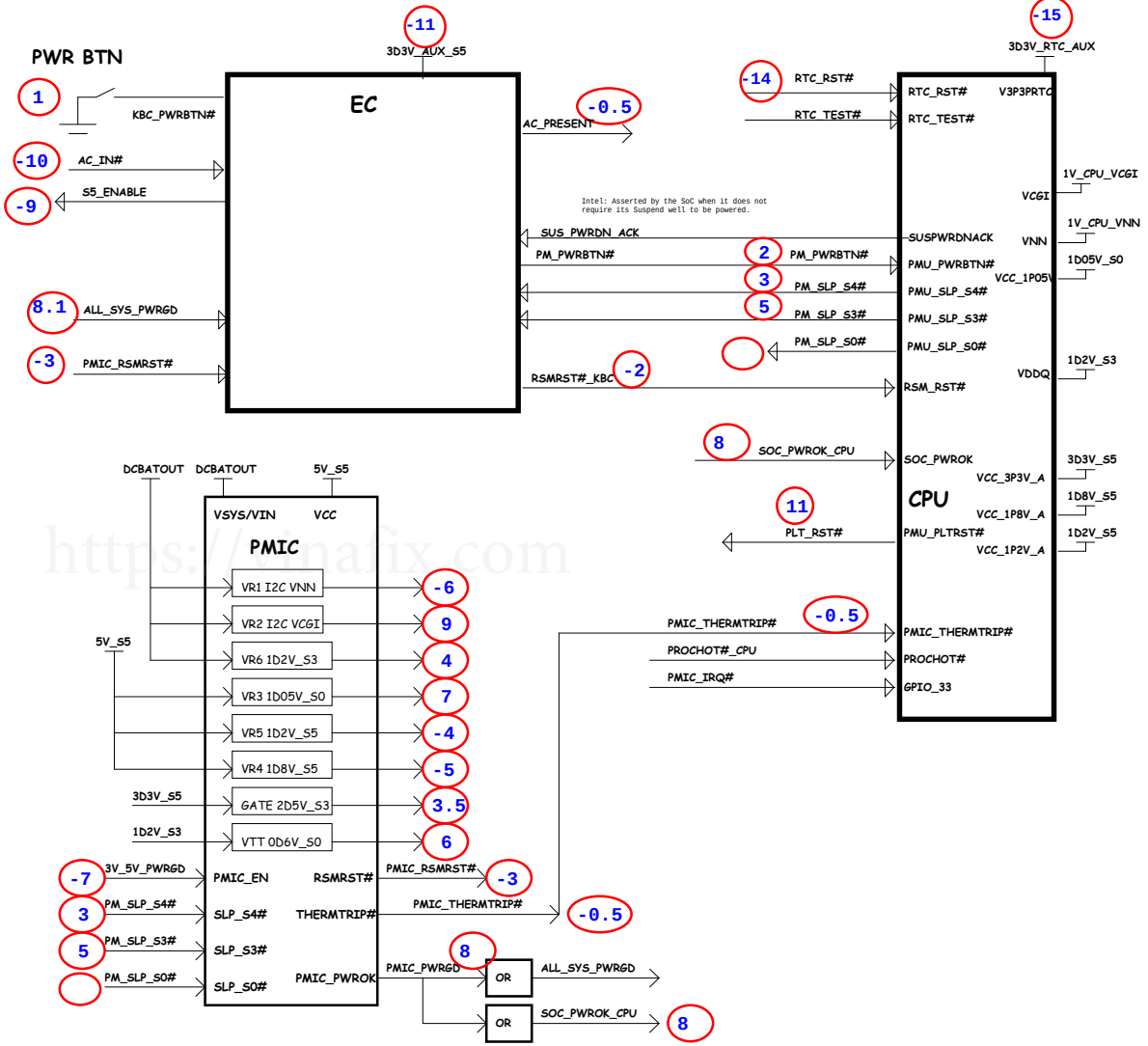
Date: Thursday, December 28, 2017 Sheet 102 of 104

Gemini LAKE SEQUENCE & BLOCK DIAGRAM









<Variant Name>

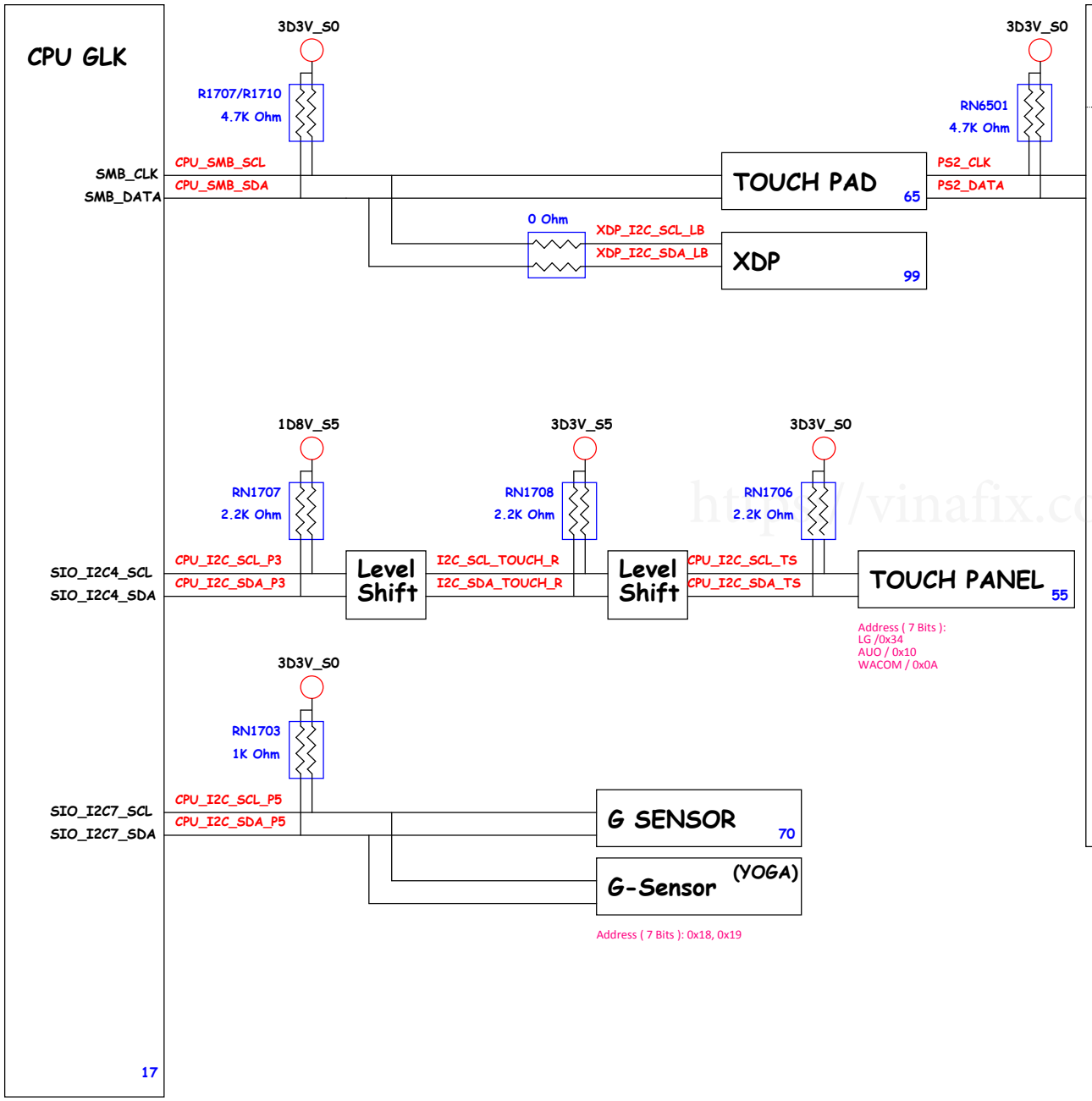
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

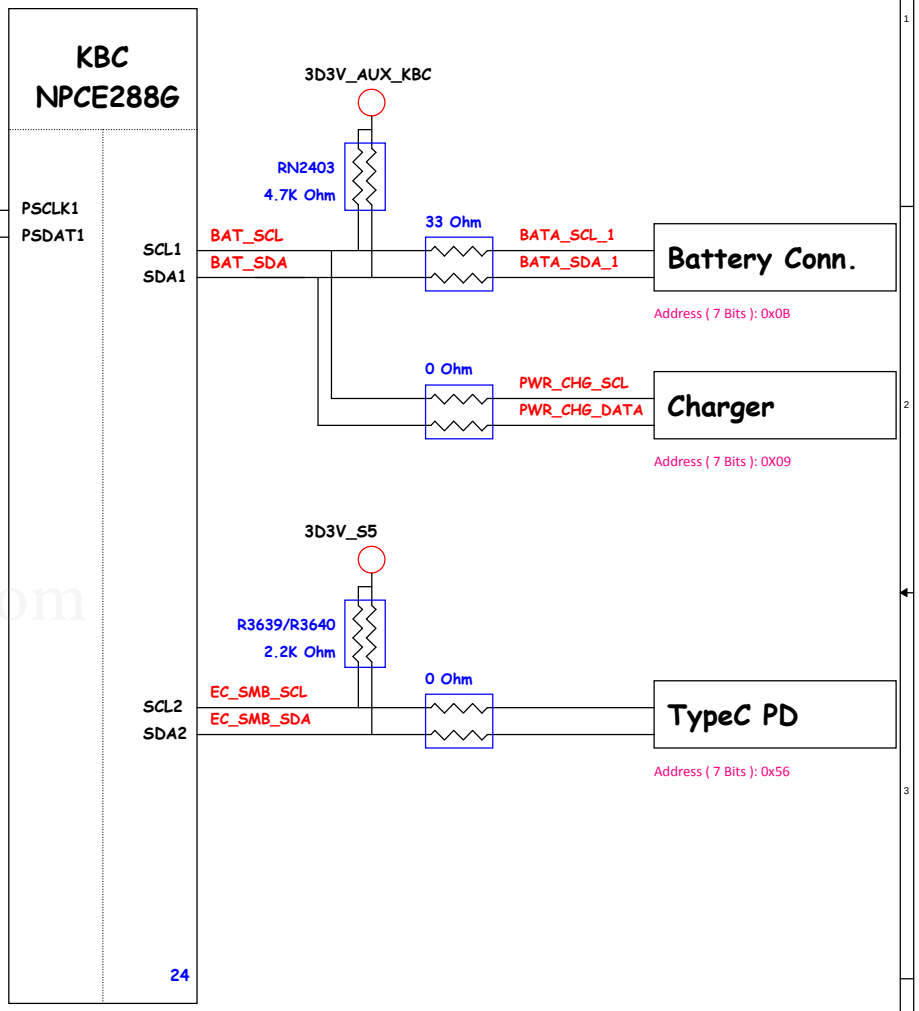
Size: A2 | Document Number: Leia | Rev: -1M

Date: Thursday, December 28, 2017 | Sheet 103 of 104

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

Size	Document Number	Rev
A3	Leia	-1M

Date: Thursday, December 28, 2017 Sheet 104 of 104