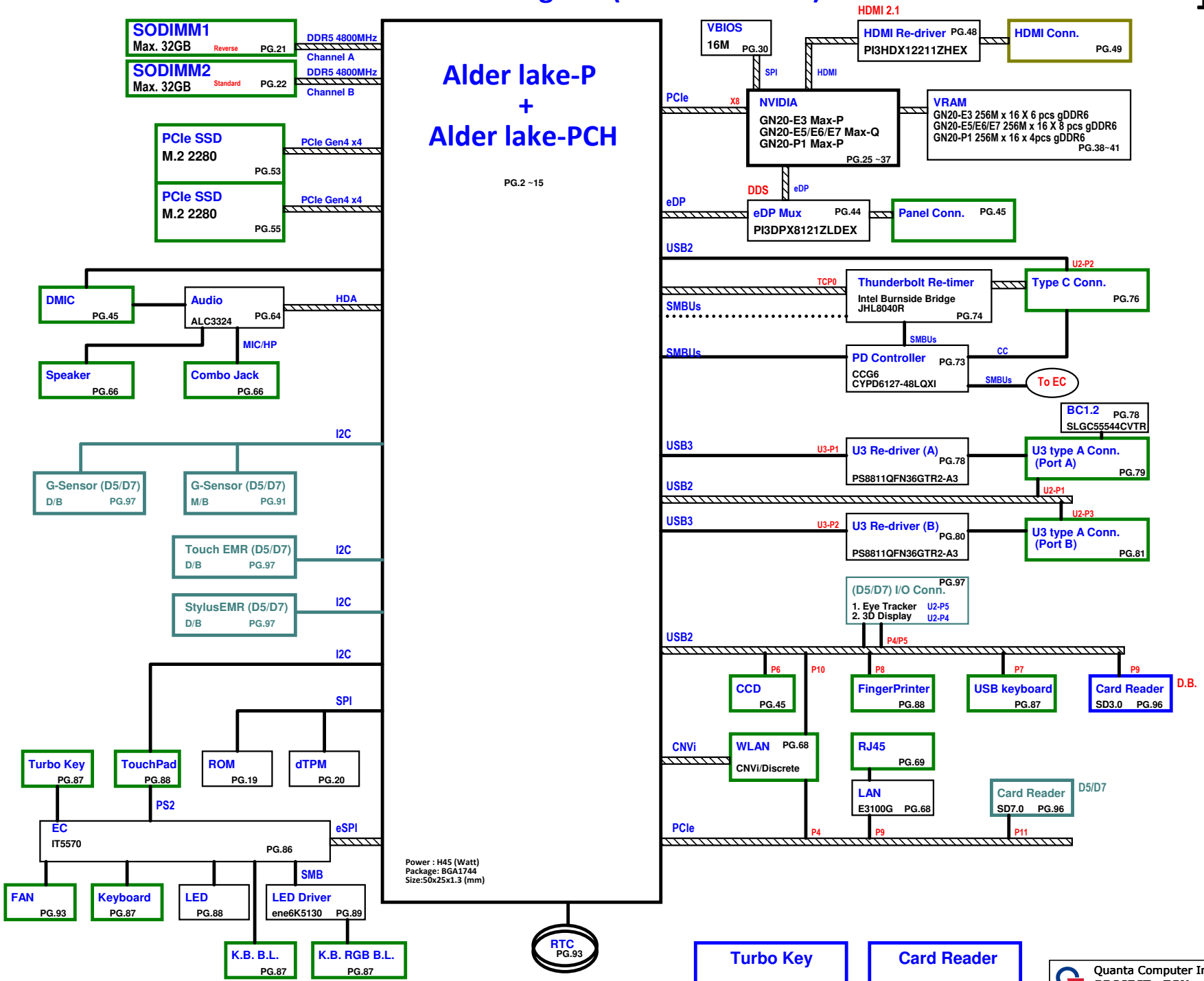
2022 ADL Block Diagram (Roadster - ZGN)



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	ZGN Block Diagram	A1A
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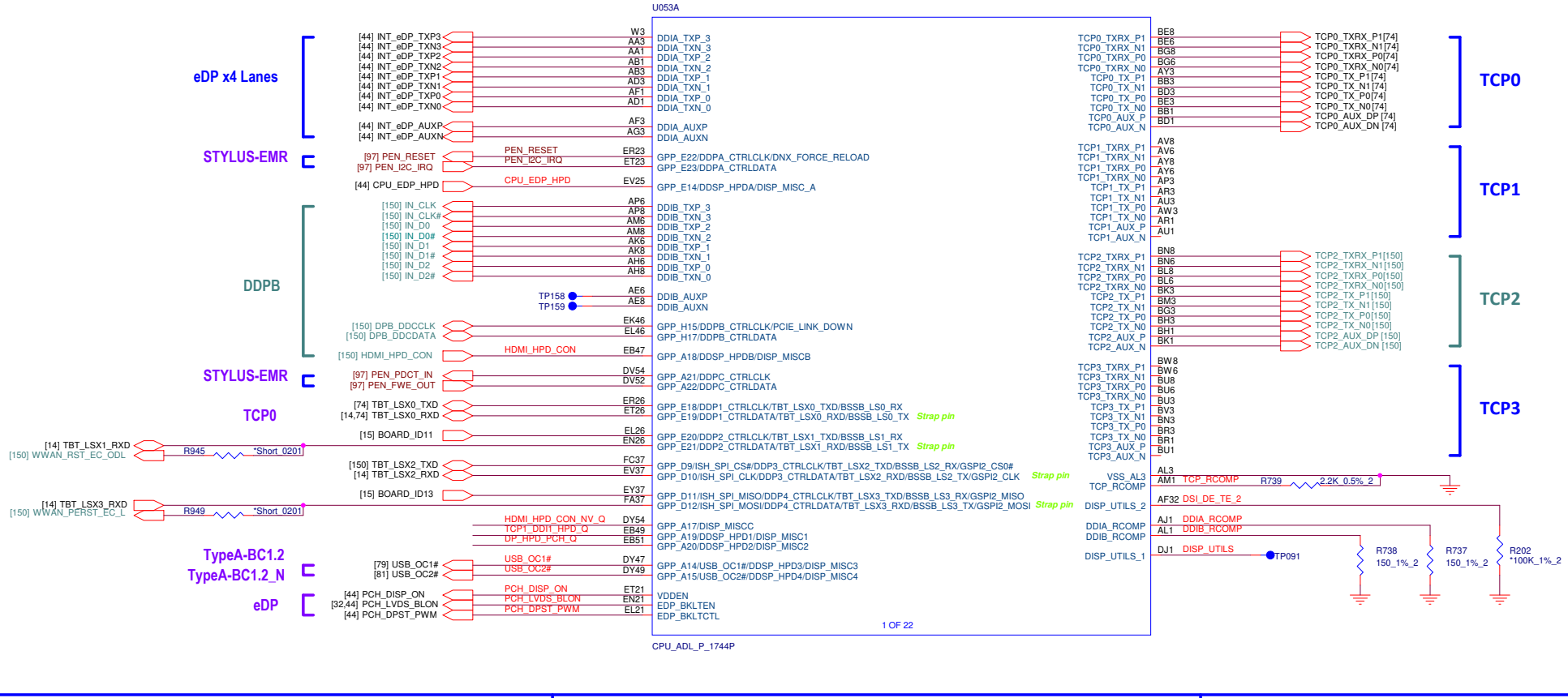
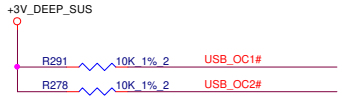
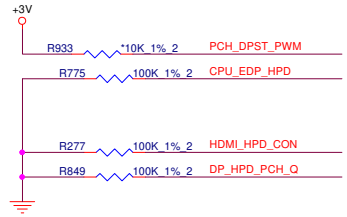


USB_OC

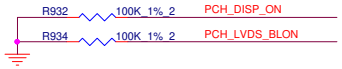


eDP

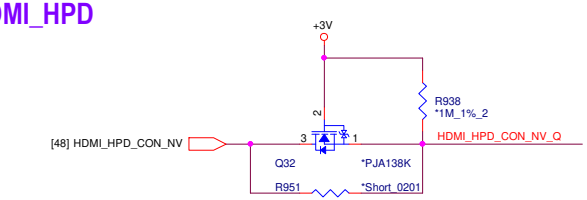


Disable Termination

Glitch Free

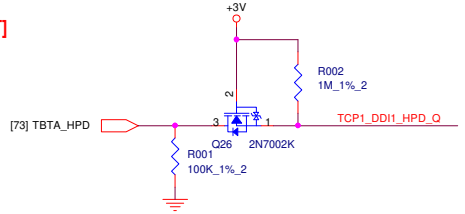


HDMI_HPD

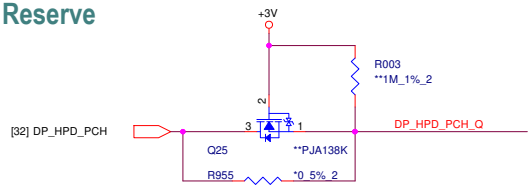


TBT_HPD

[No need for iTBT]



DP Reserve



Concept D Reserve

Quanta Computer Inc. PROJECT : ZGN		
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ALDER LAKE Processor DDR5 (NIL)

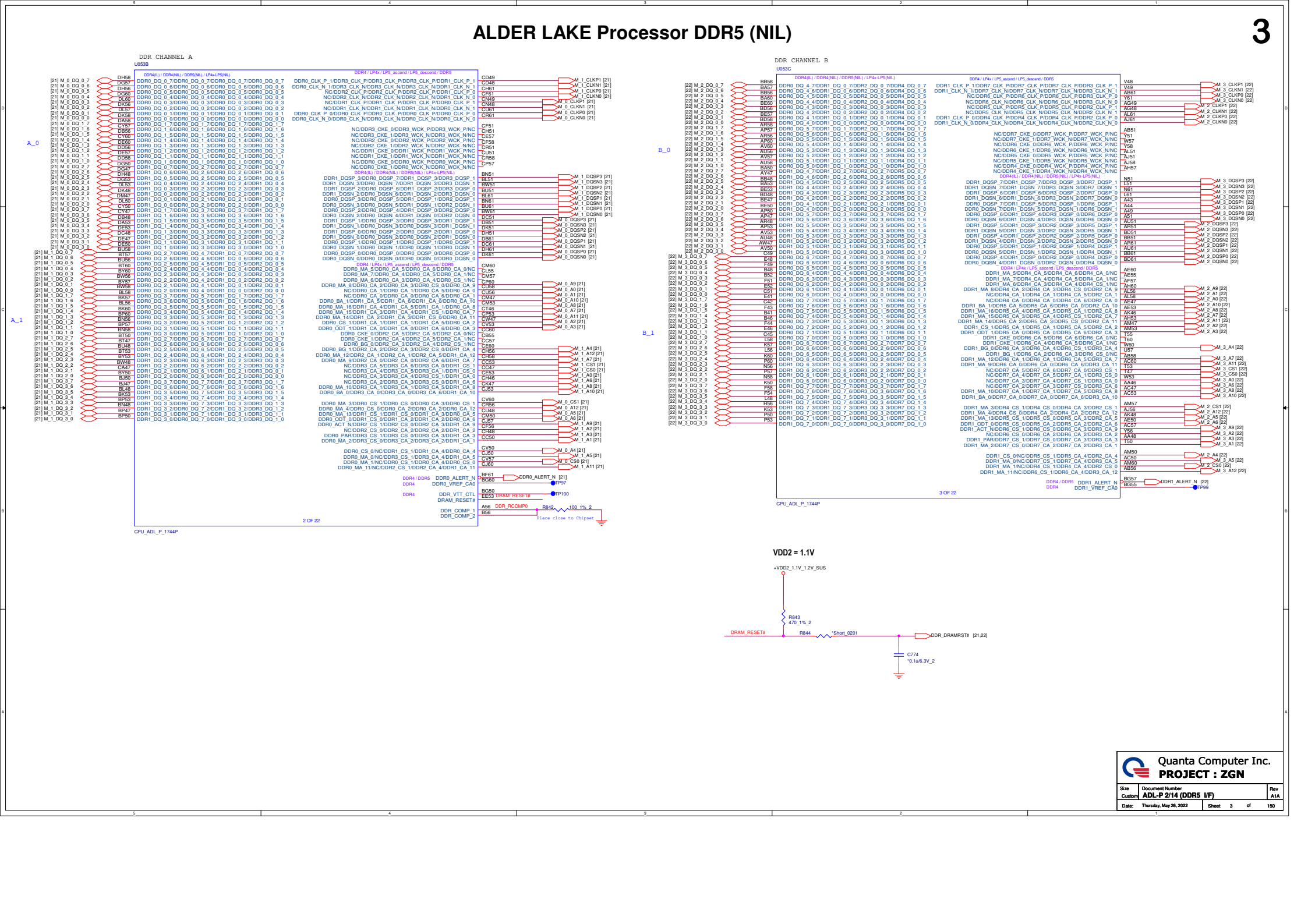
DDR CHANNEL A

U053B

DDR CHANNEL B

U053C

VDD2 = 1.1V



Quanta Computer Inc.	
PROJECT : ZGN	
Size: Custom	Document Number: ADL-P 2/14 (DDR5 I/F)
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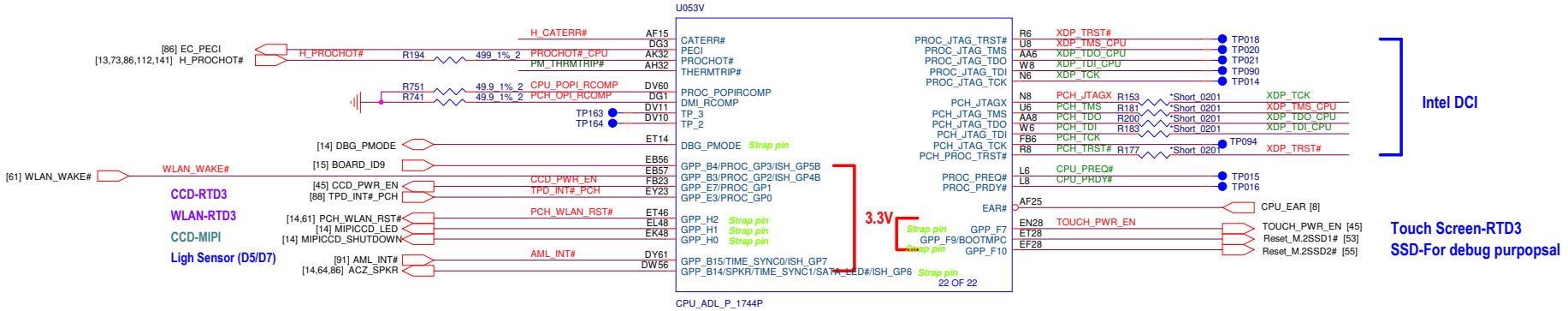
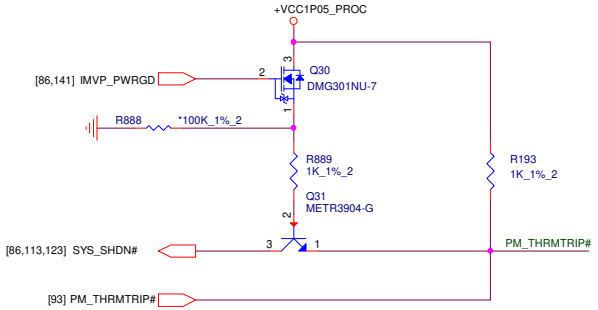
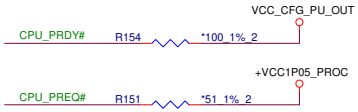


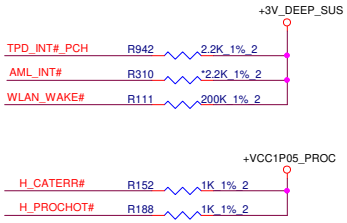
THERMAL TRIP



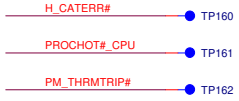
MIPI 60



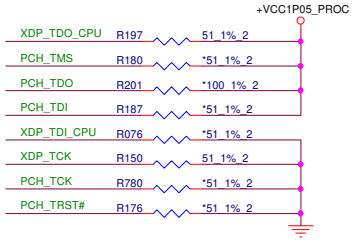
PU



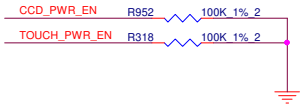
Debug Purposal



DCI



PD



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PROJECT : ZGN

Size	Document Number	Rev
Custom	ADL-P 3/14 (CPU MISC/JTA)	A1A
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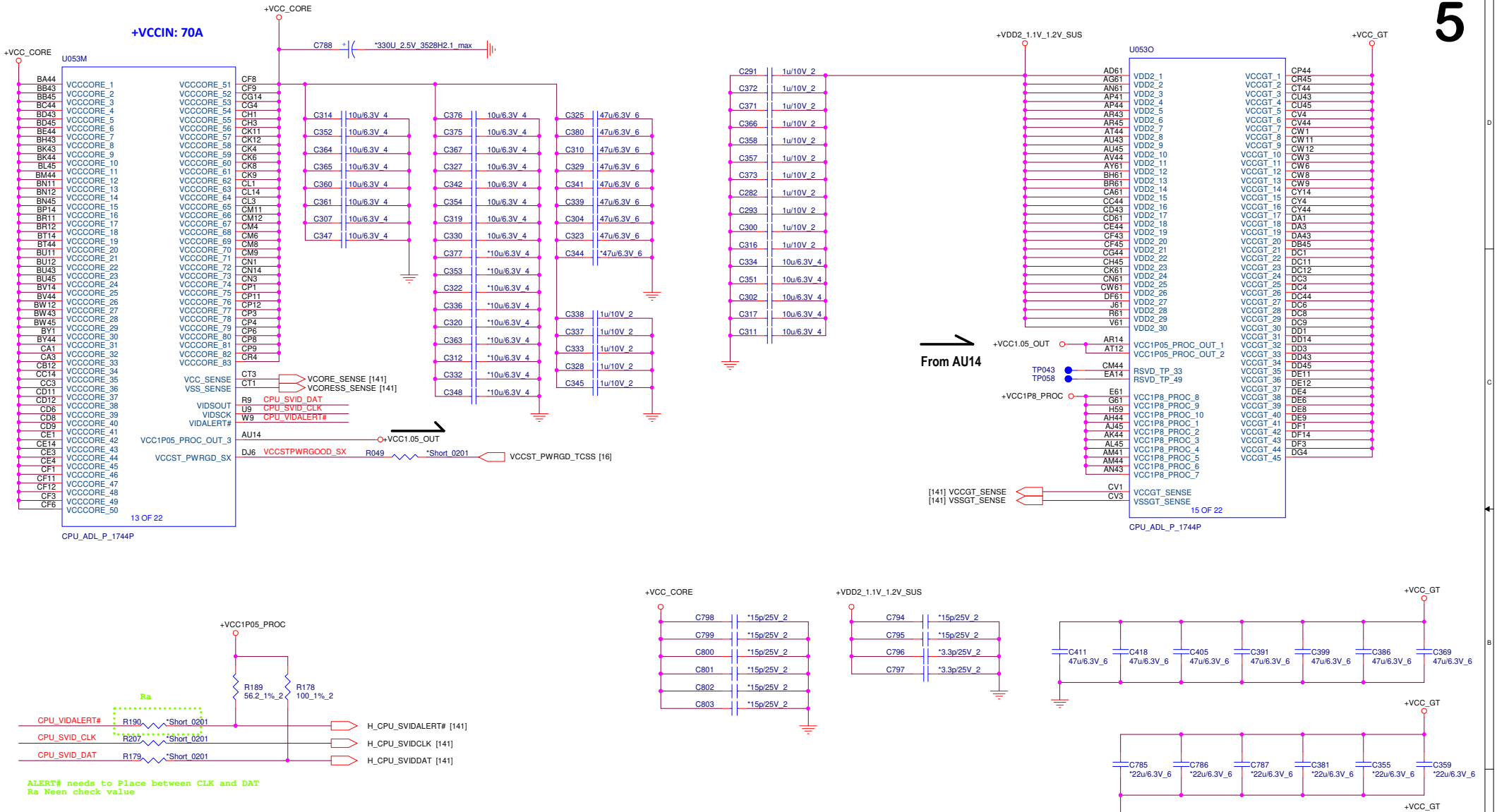

VCCCORE [PDG.0.81]	VCCGT [PDG.0.81]	VCC1P8_PROC [PDG.0.81]	VDD2 [PDG.0.81]
IA Core	Graphic	CPU PCIe	DDR PHY
Primary Side 330uF 7343 x 3 47uF 0603 x 8 22uF 0402 x 2 Secondary Side 22uF 0402 x 6	Primary Side 330uF 7343 x 2 47uF 0603 x 7 22uF 0402 x 2 Placeholder 0603 x 1 Secondary Side 22uF 0402 x 6 10uF 0402 x 2 Placeholder 0402 x1 Placeholder 0402/0603 x1	Primary or Secondary Side 1uF 0402 x1 10uF 0402 x 1 LDO side 10uF 0402 x 2 Placeholder 0603 x2	Primary Side 1uF 0402 x 2 Secondary Side Placeholder 0402 x2 10uF 0402 x 3 1uF 0402 x 4

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Custom	ADL-P 4/14 (VCCIN/VDDQ)	A1A
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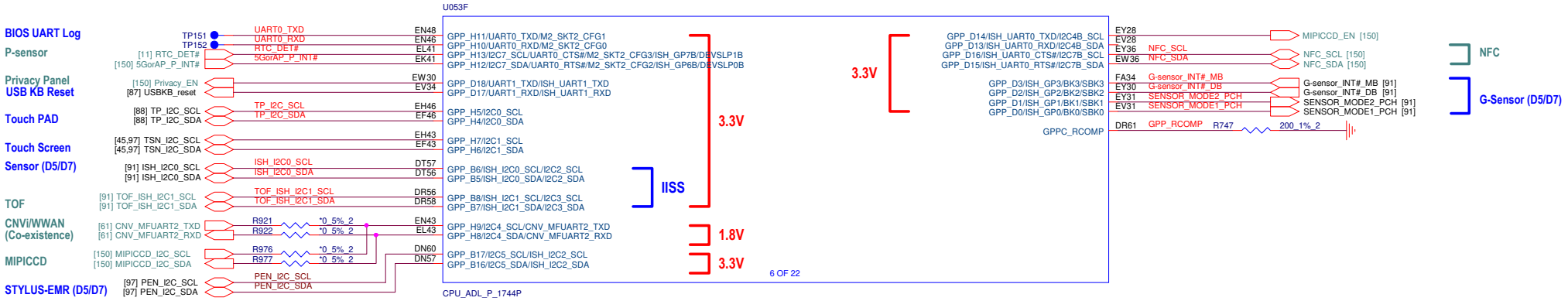

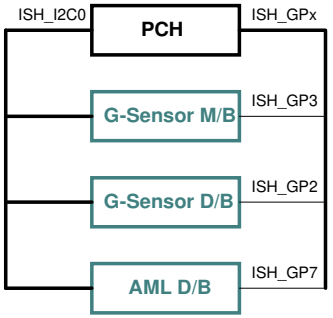

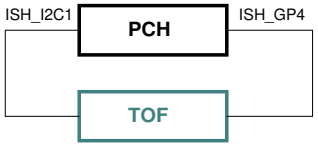

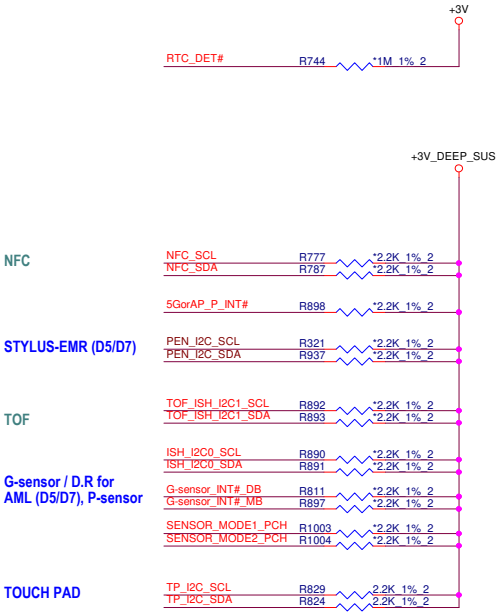

Quanta Computer Inc.
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Custom	ADL-P 5/14 (I2C/ISH)	A1A
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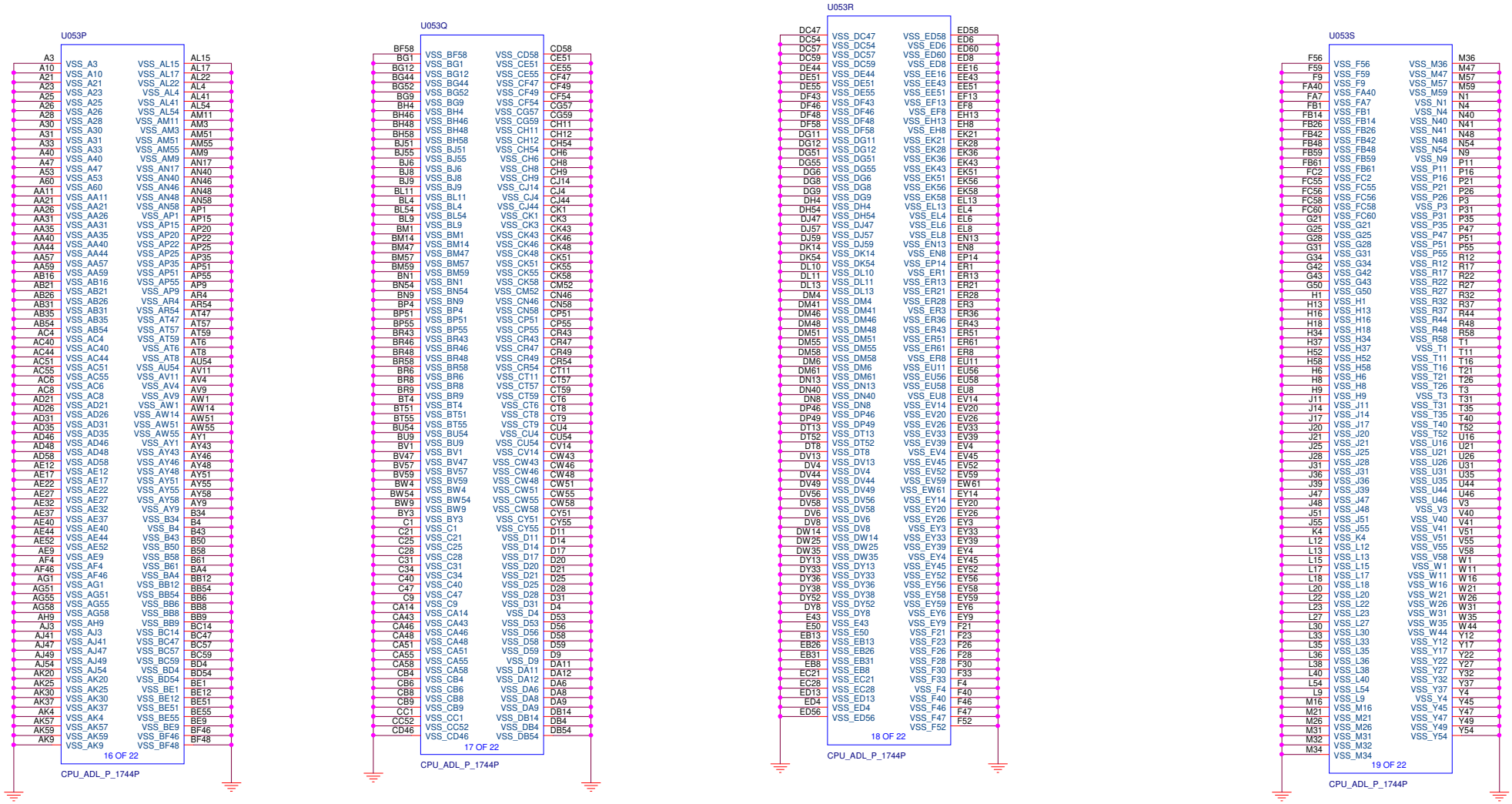

Quanta Computer Inc.
PROJECT : ZGN

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Custom	ADL_P 6/14 (GND)	A1A
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EAR

Stall CPU reset sequence until de-asserted:
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall

+VCC1P05_PROC, R182 1K_1%_2, [4] CPU_EAR, R184 *1K_1%_2

MoW-WW50

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

CFG0
1: (DEFAULT) NORMAL OPERATION; NO STALL

CFG0 R155 *0_5%_2 CFG0_R, R157 *1K_1%_2

RSVD

PCH/ PCH LESS MODE SELECTION

CFG1
1: (DEFAULT) NORMAL OPERATION
0: PCH-LESS MODE

CFG1, R169 *1K_1%_2

RSVD

LANE Reversal for PEG D1:F0

CFG2
1: (DEFAULT)NORMAL OPERATION
0: LANE REVERSAL

CFG2, R168 *1K_1%_2

PCIE Gen5 (x8)

PCIE PORT BIFURCATION STRAPS

CFG[6:5]
11: DEVICE1 FUNTION 0 ENBLED
10: DEVICE1 FUNCTION0, DEVICE1 FUNCTION 1 ENBLED

CFG5, R210 *1K_1%_2; CFG6, R206 *1K_1%_2

RSVD

NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9
1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT
0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

CFG9, R198 *1K_1%_2

MoW-WW50

PM SYNC LEGACY

CFG12
1: (DEFAULT) PMSYNC 2.0
0: LEGACY

CFG12, R212 *1K_1%_2

RSVD

PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG3
1: DISABLED
0: ENABLED

SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

CFG3, R195 *1K_1%_2

RSVD

PEG DEFER TRAINING

CFG7
1: (DEFAULT) PEG TRAIN IMMEEDIATELY FOLLOWING XXRESETB DEASSERTION
0: PEG WAIT FOR BIOS FOR TRAINING

CFG7, R216 *1K_1%_2

RSVD

SAFE MODE BOOT

CFG10
1: POWER FEATURES ACTIVATED DURING RESETT
0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

CFG10, R213 *1K_1%_2

MoW-WW50

PMSYNC AYNC MODE- PM SYNC

CFG13
1: (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)
0: ASYNC - 4-24MHZ CYCLES PER BIT

CFG13, R204 *1K_1%_2

RSVD

PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG4
1: DISABLED

0: ENABLED

CFG4, R185 *1K_1%_2

RSVD

ALLOW THE USE OF NOA ON LOCKED UNITS

CFG8
1: DISABLED(DEFAULT): IN THHIS CASE, NOA WILL BE DISABLE IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS

0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

CFG8, R214 *1K_1%_2

RSVD

DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR ULX-ULT

CFG11
1:(DEFAULT)DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED
0: DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

CFG11, R211 *1K_1%_2

RSVD

PEG60 Lane Reversal

CFG14
1: (Default) Normal
0: Reversed

CFG14, R205 *1K_1%_2

PCIE Gen4 (CHA)

PEG62 Lane Reversal

CFG15
1: (Default) Normal
0: Reversed

CFG15, R203 *1K_1%_2

PCIE Gen4 (CHB)

CFG[17:16]

RSVD

U053U

CPU_ADL_P_1744P

21 OF 22

3.3V Strap pin

GPP_B18/ADR_COMPLETE → PEN_GPIO0 [14,97] STYLUS-EMR (D5/D7)

3.3V GPP_T3 GPP_T2 → BOARD_ID16 [15] BOARD_ID15 [15]

U053T

CPU_ADL_P_1744P

20 OF 22

VCC_CFG_PU_OUT

SKTOCC_N -> H_PRESENT_N

+3VPCU, +3V_DEEP_SUS

SKTOCC# R192 *0_5%_2, R728 *10K_1%_2, R137 *10K_1%_2, R730 *10K_1%_2, Q012 *PJA138K → RSMRST# [16,86]

U053D

CPU_ADL_P_1744P

4 OF 22

VCC_CFG_PU_OUT

R156 *1K_1%_2 CFG0_R
R165 *1K_1%_2 CFG1
R162 1K_1%_2 CFG2
R160 *1K_1%_2 CFG3
R158 *1K_1%_2 CFG4
R159 *1K_1%_2 CFG5
R161 *1K_1%_2 CFG6
R170 *1K_1%_2 CFG7
R163 *1K_1%_2 CFG8
R171 1K_1%_2 CFG9
R166 1K_1%_2 CFG10
R174 *1K_1%_2 CFG11
R172 *1K_1%_2 CFG12
R164 *1K_1%_2 CFG13
R167 1K_1%_2 CFG14
R175 1K_1%_2 CFG15
R220 10K_1%_2 MIPI60_BPM0
R219 10K_1%_2 MIPI60_BPM1
R215 10K_1%_2 MBP2#
R209 10K_1%_2 MBP3#
R173 *51_1%_2 CFG16

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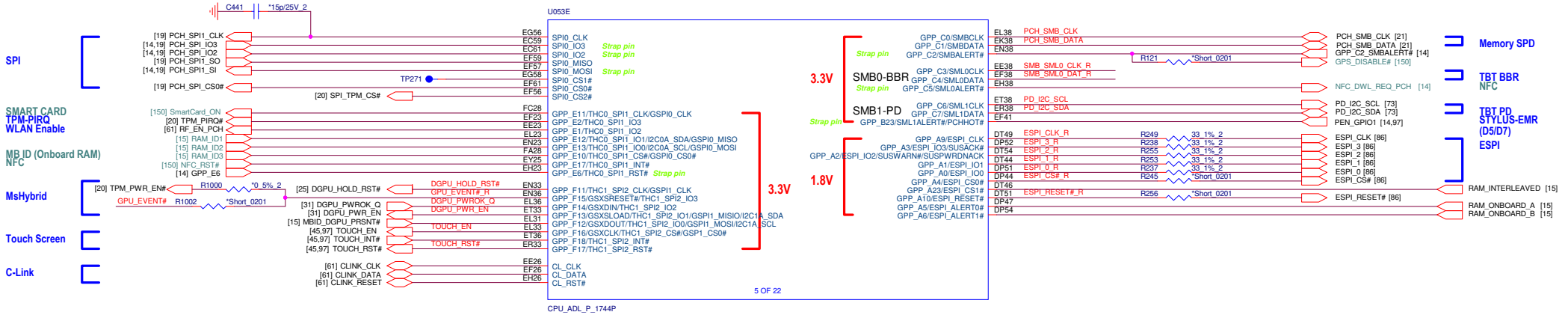

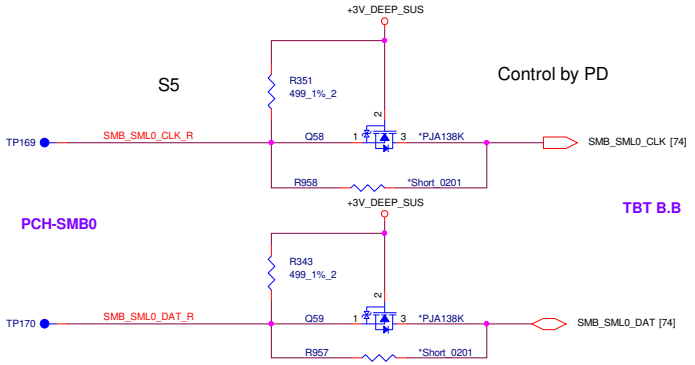

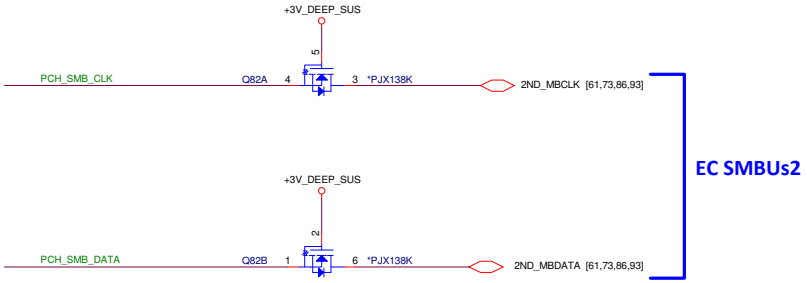

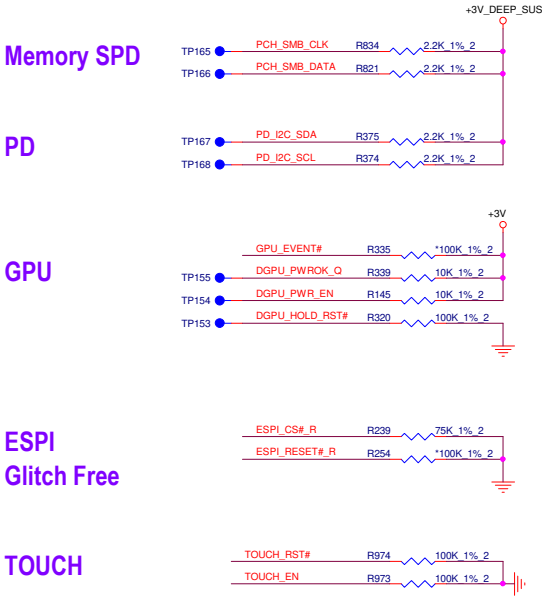

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Size	Document Number	Rev
Custom	ADL-P 8/14 (SMBus/SPI)	A1A
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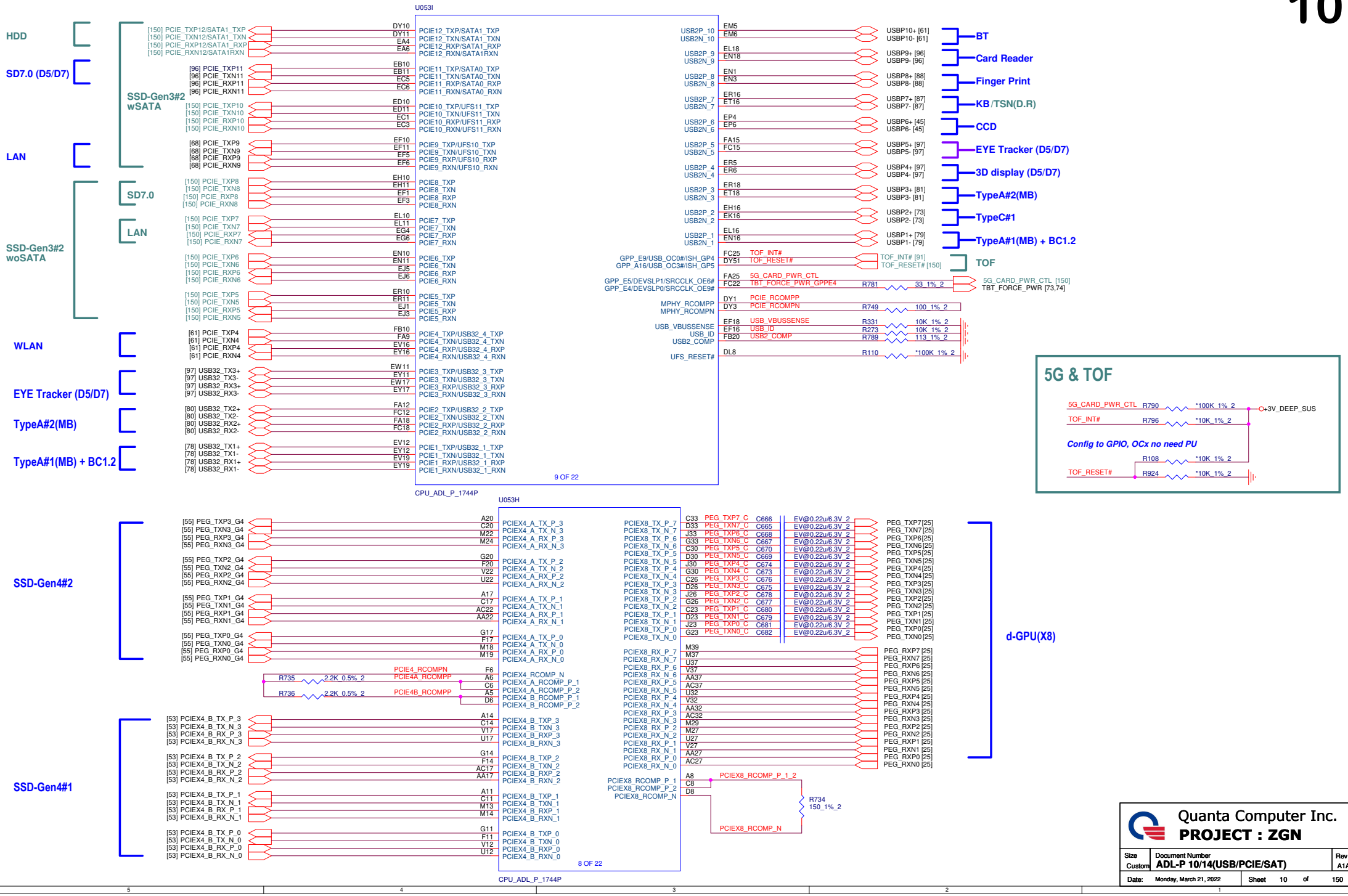

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U053J

CPU_ADL_P_1744P

CNVi

CSI x2

3.3V

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CNVi-Tx

CNVi-Tx Clock

CNVi-Rx

CNVi-Rx Clock

CNVi-BT

CNVi-RF

Strap pin

Strap pin

Glitch Free

For M.S BIOS must disable unuse port, so the ME/BIOS shoudl be different

U053K

CPU_ADL_P_1744P

(6) LAN

(5) SD7.0 (D5/D7)

(4) dGPUx8

(3) SSD-Gen4#2

(2) SSD2-Gen3#2

(1) WLAN

(0) SSD-Gen4#1

3.3V

1.8V

Gen4

Gen4

Gen4

1.8V

3.3V

11 OF 22

(6) LAN
(5) SD7.0
(2) dGPUx8
(3) SSD-Gen4#2
(2) SSD-Gen3#2
(1) WLAN
(0) SSD-Gen4#1

PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices

- CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support
- CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

Any unused CLKOUT_PCIE_P/N differential pair not being routed on a

RTC Clock 32.768KHz

Crystal Components with Surrounding 10 mil Wide GND Shield Trace

Break Out:4-10 mil Wide GND Shield Trace

Check Y1/Y4 all need pilot run A to C1

Check Y4 for C2/RAMP

Crystal 38.4MHz

RTC Circuitry(RTC)

RTC Power trace width 20mils.

Q019 *2N7002K

Q22 2N7002KTB

Q23 *2N7002KTB

Y3 38.4MHZ/20ppm

Y4 Y4@32.768KHZ/20ppm

Y1 Y1@32.768KHZ/20ppm

Quanta Computer Inc.

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VGA_DDS / DMIC

U053G

[44] LCDVCC_CTL_PCH — LCDVCC_CTL_PCH — EY34 — GPP_D19/I2S_MCLK1_OUT — 3.3V

[44] PWM_OUT_EN — EV53 — GPP_S0/SNDW0_CLK/I2S1_SCLK
[32] MUX_CTRL_PCH — EY53 — GPP_S1/SNDW0_DATA/I2S1_SFRM

[45] DMIC_CLK0_1V8 — FA50 — GPP_S2/SNDW1_CLK/DMIC_CKL_A0/I2S1_TXD
[45] DMIC_DATA0_1V8 — FC50 — GPP_S3/SNDW1_DATA/DMIC_DATA0/I2S1_RXD

[15] BOARD_ID1 — EV50 — GPP_S4/SNDW2_CLK/DMIC_CLK_B0
[15] BOARD_ID2 — EY50 — GPP_S5/SNDW2_DATA/DMIC_CLK_B1

[15] BOARD_ID3 — EW48 — GPP_S6/SNDW3_CLK/DMIC_CLK_A1
[15] BOARD_ID4 — EY48 — GPP_S7/SNDW3_DATA/DMIC_DATA1

1.8V

GPP_R0/HDA_BCLK/I2S0_SCLK/DMIC_CLK_B0/HDAPROC_BCLK — ER56 — BIT_CLK — R792 33_1%_2 — BIT_CLK_AUDIO [64]
GPP_R1/HDA_SYNC/I2S0_SFRM/DMIC_CLK_B1 — EP60 — ACZ_SYNC — R386 33_1%_2 — ACZ_SYNC_AUDIO [64]
Strap pin GPP_R2/HDA_SDO/I2S0_TXD/HDAPROC_SDO — ER57 — ACZ_SDOUT — R492 33_1%_2 — ACZ_SDOUT_AUDIO [64]
GPP_R3/HDA_SDI0/I2S0_RXD/HDAPROC_SDI — ER59 — ACZ_SDIN0_AUDIO [64]

GPP_R4/HDA_RST#/I2S2_SCLK/DMIC_CLK_A0 — ER53 — ACZ_RST# — R918 *0_5%_2 — R363 33_1%_2 — ACZ_RST#_AUDIO [64]
GPP_R5/HDA_SDI1/I2S2_SFRM/DMIC_DATA0 — ET53 — PCM_CLK [61]
GPP_R6/I2S2_TXD/DMIC_CLK_A1 — EB44 — Panel_OD_PCH [45]
GPP_R7/I2S2_RXD/DMIC_DATA1 — EB46 — GPP_R7 — R917 *0_5%_2 — R968 *0_5%_2 — BOARD_ID8 [15] — PCM_IN [61]

3.3V — GPP_A11/PMC_I2C_SDA — DV51 — PCH_TBT_PERST# — R923 *Short_0201 — BT_OFF_PCH# [61]
GPP_A13/PMC_I2C_SCL — DV47

SNDW_RCOMP_1 — FA53 — SNDW_RCOMP — R813 200_1%_2
SNDW_RCOMP_2 — FC53

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CPU_ADL_P_1744P

TouchPad

U053L

[16,21,22,86,123] SLP_SUS#_EC — SLP_SUS#_EC — EN53 — SLP_SUS#

[88] PTP_PWR_EN# — PTP_PWR_EN# — EG60 — GPD10/SLP_S5#
[16,21,22,86,114,146] SUSC# — SUSC# — EP56 — GPD5/SLP_S4#
[16,86,124] SUSB# — SUSB# — EM59 — GPD4/SLP_S3#
SLP_A# — EM57 — GPD6/SLP_A#
SLP_WLAN#_R — EJ57 — GPD9/SLP_WLAN#

[20,61,86] AP_SLP_S0_L — AP_SLP_S0_L — DW59 — GPP_B12/SLP_S0#
[150] SLP_LAN# — SLP_LAN# — EK53 — SLP_LAN#

[16] RSMRST#_PCH — R925 *Short_0201 — RSMRST#_R — EH53 — RSMRST#
SYS_RESET# — EK26 — SYS_RESET#
PLTRST#_PCH — DW57 — GPP_B13/PLTRST#

PCH_DSWROK — EE48 — DSW_PWROK
SYS_PWROK — EK23 — SYS_PWROK
[16] PCH_PWROK_R — PCH_PWROK_R — EH51 — PCH_PWROK

+3V_RTC — R926 1M_1%_2 — INTRUDER# — DY44 — INTRUDER#
[14] INPUT3VSEL — EL53 — SPIVCCIOSEL Strap pin

PROCPWRGD — BG11 — PROCPWRGD

12 OF 22

CPU_ADL_P_1744P

PD - ALERT — GPP_B11/PMCALERT# — EM61 — R959 *Short_0201 — DNBSWON# [86]
3.3V — GPP_H18/PROC_C10_GATE# — EM56 — BATLOW# — EJ59 — ADP_PRES_OUT — AC_PRESENT_EC [86]
GPP_H3/SX_EXIT_HOLDOFF# — EA56 — PD_I2C_INT# — EA46 — CPU_C10_GATE# — ET48 — SmartCard_PWRSV# — PD_I2C_INT# [73] / SmartCard_PWRSV# [150]

WAKE# — ET51 — PCIE_WAKE# — PCIE_WAKE# [96]

3.3V — GPD2/LAN_WAKE# — EP58 — LAN_WAKE#_GPD2
GPD11/LANPHYPC — EJ56 — LAN_DIS#

Strap pin GPD7 — EK60 — BOARD_ID14 [14,15]

GPP_E8/SLP_DRAM# — FA22 — GPP_E8 — R130 *0_5%_2 — R131 *Short_0201 — WWAN_RF_DISABLE_ODL [150] — SLP_DRAM# [114,146]

VCCST_PWRGD — DJ8 — H_VCCST_PWRGD — R236 60.4_1%_2 — H_VCCST_PWRGD_R
VCCST_OVERRIDE — DK4 — VCCST_OVERRIDE — VCCST_OVERRIDE [16]

3.3V — GPP_F20/EXT_PWR_GATE# — EH28 — MBID_VPRO_DET [15]
GPP_F21/EXT_PWR_GATE2# — EH31 — GC6FBEN_Q [32] — GC63.0 Don't Need
R966 *Short_0201 — MIPI_PWR_MS# [150]

R104 *100K_1%_2 — VCCDSW_3P3

PU/PD

+3V
VCCST_OVERRIDE — R743 *100K_1%_2
SmartCard_PWRSV# — R362 *10K_1%_2
SYS_RESET# — R342 *10K_1%_2

+3V_DEEP_SUS
R793 10K_1%_2
GPP_E8 — R807 *10K_1%_2
LAN_WAKE#_GPD2 — R382 10K_1%_2
PCIE_WAKE# — R368 8.2K_1%_2
BATLOW# — R785 10K_1%_2
ADP_PRES_OUT — R772 100K_1%_2
PD_I2C_INT# — R391 10K_1%_2
CPU_C10_GATE# — R350 *100K_1%_2
R344 100K_1%_2
RSMRST#_R — R931 100K_1%_2
SYS_PWROK — R103 100K_1%_2
PCH_PWROK_R — R393 100K_1%_2
PROCPWRGD — R225 *10K_1%_2
LCDVCC_CTL_PCH — R971 100K_1%_2
LAN_DIS# — R769 *30.1K_1%_4
GPP_E8 — R1019 100K_1%_2
PCH_TBT_PERST# — R954 100K_1%_2

+1.8V_DEEP_SUS
GPP_R7 — R467 *100K_1%_2

PLTRST# (Buffer)

+3V_DEEP_SUS
C462 0.1u/6.3V_2
PLTRST#_PCH — R956 *100K_1%_2 — U022 *MC74VHC1G08DFT2G — R839 100K_1%_2 — PLTRST# [20,25,53,55,61,68,96]
R338 *Short_0201

DSW_PWROK

[16] PCH_DSWROK — PCH_DSWROK — R930 *0_5%_2 — RSMRST#_R
R398 *0_5%_2 — DPWROK_EC [16,86]
R396 100K_1%_2
R399 *1M_1%_2 — C477 *0.01u/10V_2

BBR Reset

+3V_DEEP_SUS
C775 0.1u/6.3V_2
PCH_TBT_PERST# — U56 *MC74VHC1G08DFT2G — TCP_RETIMER_PERST# [74]
PLTRST#_PCH — R847 *100K_1%_2
R838 *0_5%_2

SYS_PWROK

SYS_PWROK — R927 *10K_1%_2 — EC_SYS_PWROK [86]
R929 *Short_0201

PCH_PWROK

PCH_PWROK_R — R392 *0_5%_2 — PCH_PWROK [16,86]

VCCST_PWRGD

VRON_IMVP9 — R100 *0_5%_2
[16,86] HWPG — R865 *0_5%_4
+3V_DEEP_SUS — C664 0.1u/6.3V_2
SUSB# — U41 MC74VHC1G08DFT2G — R394 100K_1%_2
+3V_DEEP_SUS — R866 47K_1%_2 — Q29A PJX138K
+VCC1P05_PROC — R762 1K_1%_2 — H_VCCST_PWRGD_R — Q29B PJX138K
R109 *100_1%_2 — D741 *RB500V-40

VRON_IMVP9

+3V_DEEP_SUS
C780 *0.1u/6.3V_2
HWPG_VDDR [86,114]
R999 *0_5%_2
DRAM_PWR_GOOD [21,22,86]
U61 *MC74VHC1G08DFT2G
+3V_DEEP_SUS
C779 0.1u/6.3V_2
[141] VRON_IMVP9 — VRON_IMVP9 — SUSB# — VRON [86]
R997 100K_1%_2 — U60 MC74VHC1G08DFT2G

Glitch Free

+3V_DEEP_SUS
AP_SLP_S0_L — R752 100K_1%_2
R753 *100K_1%_2
ACZ_RST# — R352 100K_1%_2
SLP_SUS#_EC — R369 100K_1%_2
PTP_PWR_EN# — R970 100K_1%_2
SUSC# — R015 100K_1%_2
SUSB# — R805 100K_1%_2
SLP_A# — R005 100K_1%_2
SLP_WLAN#_R — R975 100K_1%_2
SLP_LAN# — R031 100K_1%_2
BIT_CLK — R778 *100K_1%_2
C529 22p/25V_2

LAN WAKE

S3
PCIE_WAKE# — R1016 *Short_0201
S0ix-D3 Cold
LAN_WAKE#_GPD2 — R1015 *0_5%_2 — LAN_WAKE# [68]

WoWLAN

For Dis. module only

+3V_DEEP_SUS
R614 10K_1%_2
[61] SLP_WLAN_PWR# — Q55 2N7002KTB — SLP_WLAN#_R

TP177 SLP_SUS#_EC
TP179 SUSC#
TP180 SUSB#
TP181 AP_SLP_S0_L
TP184 PLTRST#_PCH
TP182 RSMRST#_R
TP183 SYS_RESET#
TP185 PCH_DSWROK
TP186 SYS_PWROK
TP187 PCH_PWROK_R
TP188 PROCPWRGD
TP189 H_VCCST_PWRGD
TP190 VCCST_OVERRIDE
TP247 CPU_C10_GATE#

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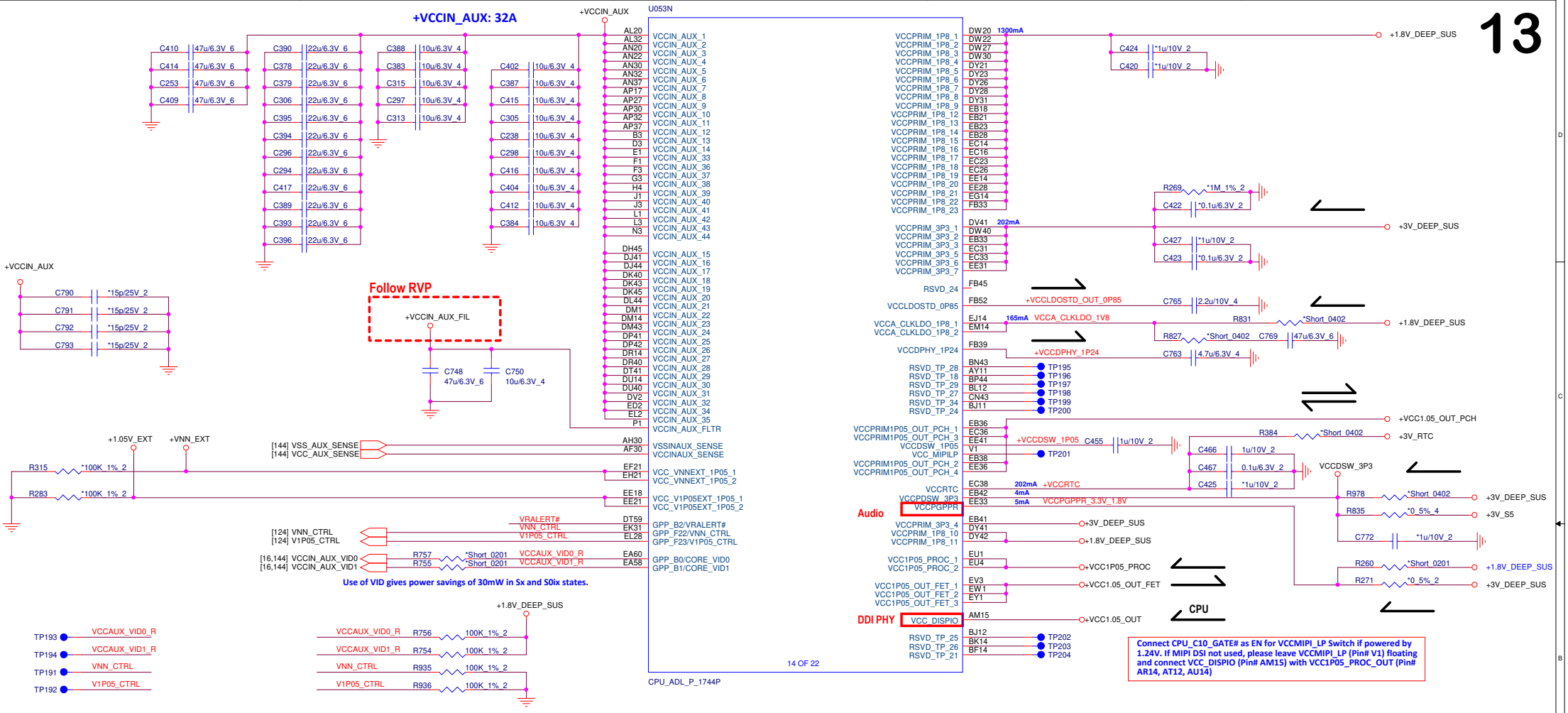
+VCCIN_AUX: 32A



Connect CPU_C10_GATE# as EN for VCCMIPI_LP Switch if powered by 1.24V. If MIPI DSI not used, please leave VCCMIPI_LP (Pin# V1) floating and connect VCC_DISPIO (Pin# AM15) with VCC1P05_PROC_OUT (Pin# AR14, AT12, AU14)

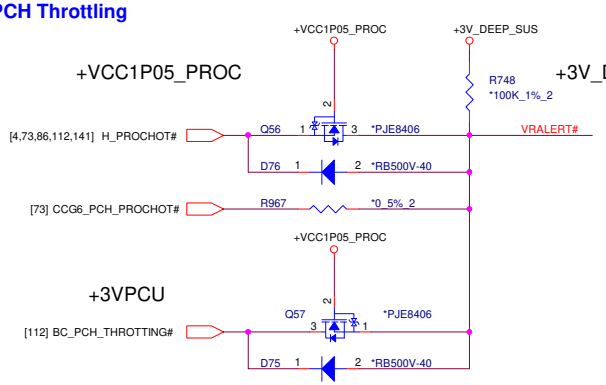
Platform state	VNN_CTRL	VNNEXT_1P05
S0	0	0.78
S0I2.X	0	0.78
SOi3.X	1	0.7
SX	0	1.05

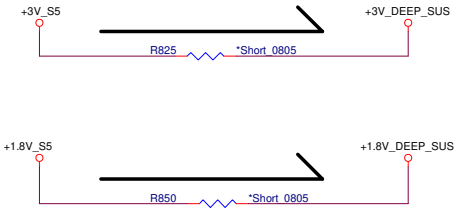
Platform state	VNN_CTRL	V1P05EXT_1P05
S0	0	1.05
S0I2.X,SOi3.0-1	0	1.05
SOi3.2-4	1	0.96
SX	0	1.05

SLP_SUS#	VID1	VID0	SLP_S0#	VCCIN_AUX	Comments
0	X	X	X	OFF	FIVR input is OFF
1	0	0	0	0	S0ix
1	0	1	1	1.1	Retention FIVR voltage, no VCCIN_AUX FIVRs active in CPU
1	1	0	1	1.65	Low current mode
1	1	1	1	1.8	High current mode

Leakage from VCCIN_AUX is expected behavior when CORE_VID[1:0]=00; this leakage voltage may be as high as 1.15 V during Sx and S0ix states.

PCH Throttling





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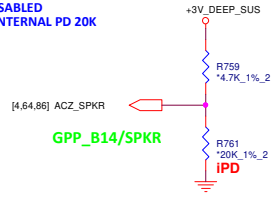
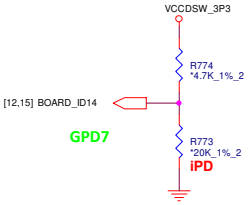
TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

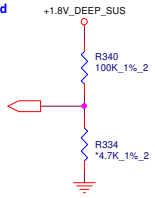


RSVD



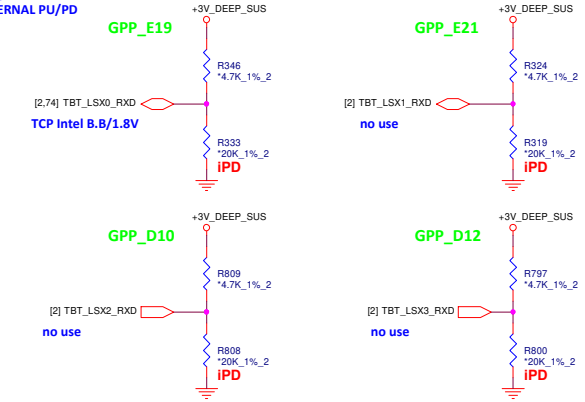
M.2 CNVi Mode Select

High: Integrated CNVi disabled
Low: Integrated CNVi enabled
An external pull-up or pull-down is required
Enable by device driven low



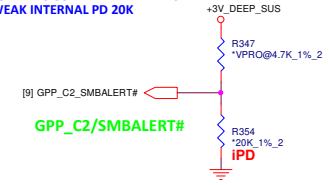
TBT LSX PINS VCCIO CONFIGURATION

High: 3.3V
Low: 1.8V
NO INTERNAL PU/PD



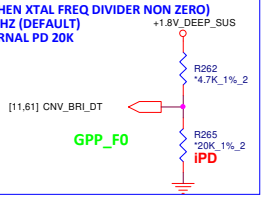
TLS CONFIDENTIALITY

HIGH - TLS CONFIDENTIALITY ENABLE
LOW - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K



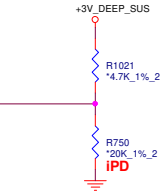
XTAL FREQUENCE SEL

High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K



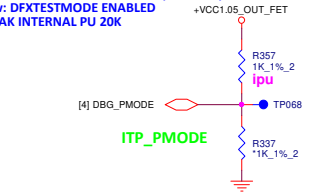
NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



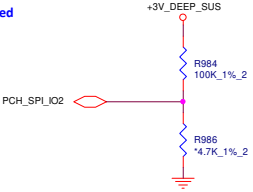
(RSVD) ITP PMODE

High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K



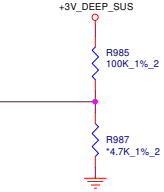
(RSVD) CONSENT STRAP

PU is required



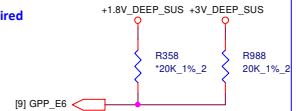
(RSVD) A0 PERSONALITY STRAP

PU is required



JTAG ODT Disable

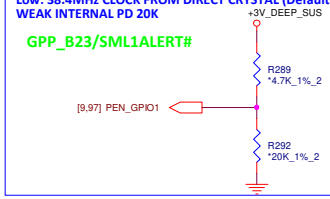
PU is required



CPUNSSC CLOCK FREQ

HVM ONLY

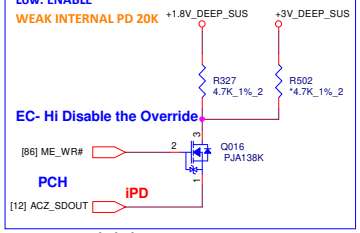
High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K



Flash Descriptor Security Override

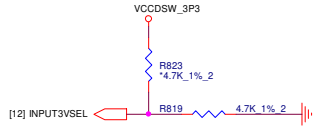
High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

GPP_R2



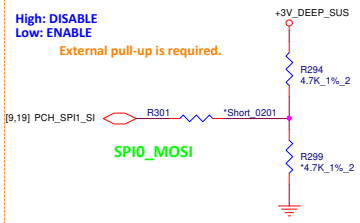
3V SELECT STRAP

0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K ohm pull-up to DSW_PWROK)



(RSVD) BOOT HALT

High: DISABLE
Low: ENABLE
External pull-up is required.



Reserve

GPP_F7

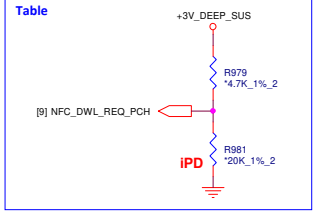
Reserve

GPP_F10

Boot Strap 0/1/2/3

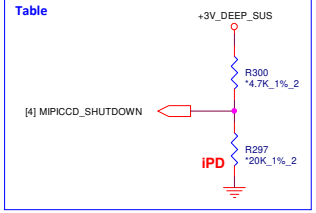
Boot Strap 0 GPP_C5

Table



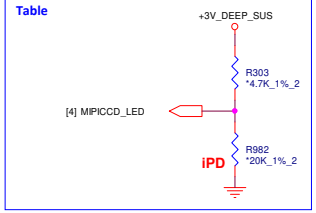
Boot Strap 1 GPP_H0

Table



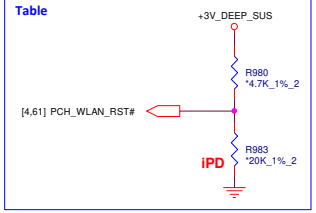
Boot Strap 2 GPP_H1

Table



Boot Strap 3 GPP_H2

Table



Boot Strap	4-bit boot strap configuration encodings
0000	BIOS/CSME on SPI , eSPI is enabled
0010	BIOS/CSME on SPI , eSPI is disabled
0100	BIOS on eSPI Peripheral Channel; CSME on master SPI
1000	BIOS/CSME on eSPI
1100	BIOS on eSPI peripheral Channel; CSME on slave SPI

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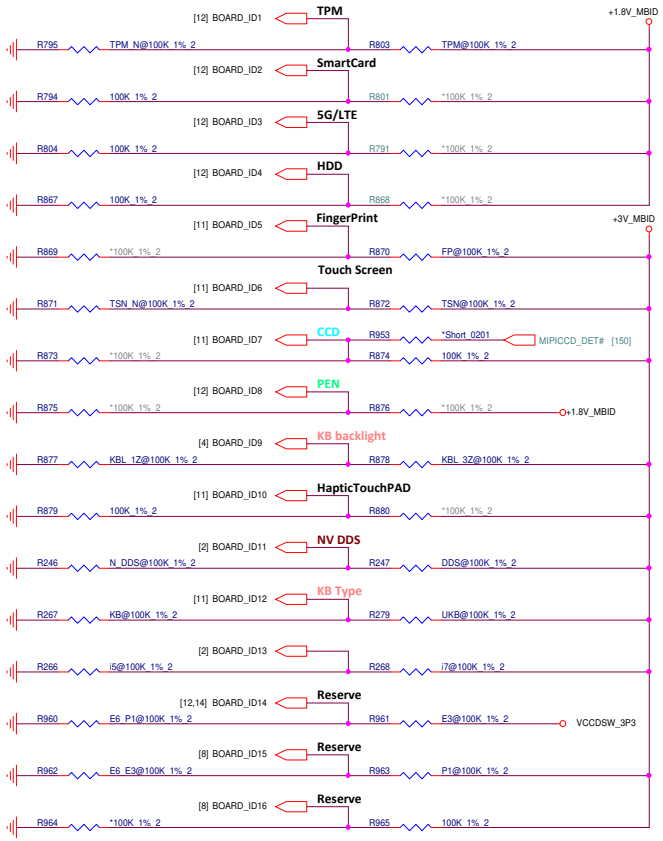
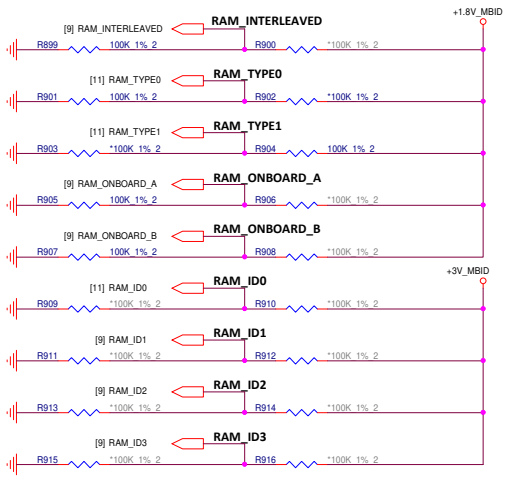
MBID

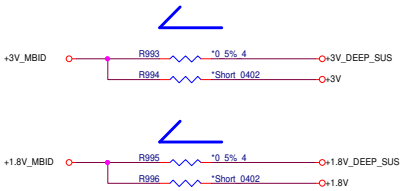
Option Value to meet project requirement

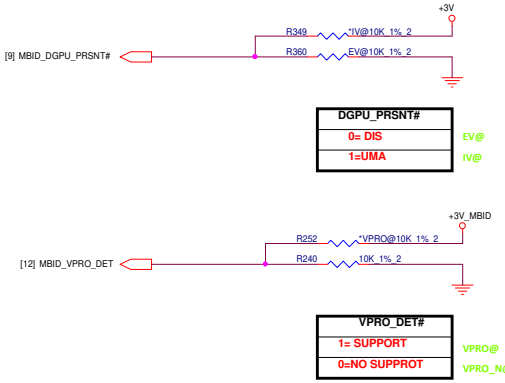
ID.NO	Function	Low	High
BOARD_ID1	TPM	0=No TPM_N@	1=Yes TPM@
BOARD_ID2	SmartCard	0=No SM_N@	1=Yes SM@
BOARD_ID3	5G/LTE	0=No 5G_LTE_N@	1=Yes 5G_LTE@
BOARD_ID4	HDD	0=No HDD_N@	1=Yes HDD@
BOARD_ID5	FingerPrint	0=No FP_N@	1=Yes FP@
BOARD_ID6	Touch Screen	0=No Cable/DB	1=Yes
BOARD_ID7	CCD	0=MIPI Cable/DB	1=USB
BOARD_ID8	PEN Type	0=AES AES@	1=EMR EMR@
BOARD_ID9	KB backlight	0=ON/OFF KBL_ONOFF_NUSB@	1=RGB KBL_RGB_NUSB@
BOARD_ID10	HapticTouchPAD	0=No Hap-TP_N@	1=Yes Hap-TP@
BOARD_ID11	NV DDS	0=No DDS_N@	1=Yes DDS@
BOARD_ID12	KB Type	0=Non-USB IF USBKB_N@	1=USB IF USBKB@
BOARD_ID13	CPU Type	0=No i5@	1=Yes i7@
BOARD_ID14	GPU_ID0	0=No (default) E6_P1@	1=Yes E3@
BOARD_ID15	GPU_ID1	0=No (default) E6_E3@	1=Yes P1@
BOARD_ID16	14"/16"	0=No 14"(ZGF)	1=Yes (default) 16"(ZGN)



	Function	Low	High
	RAM_INTERLEAVED	0=No	1=Yes
	RAM_TYPE0	RAM_TYPE1 / RAM_TYPE0 00 / 01 / 10 /11 00=DDR4, 01=LPDDR4 10=DDR5, 11=LPDDR5	
	RAM_TYPE1		
XX@ XX@	RAM_ONBOARD_A	0=No	1=Yes
XX@ XX@	RAM_ONBOARD_B	0=No	1=Yes
XX@ XX@	RAM_ID0	Project list Config	
XX@ XX@	RAM_ID1		
XX@ XX@	RAM_ID2	Socket define low for all pin	
XX@ XX@	RAM_ID3		







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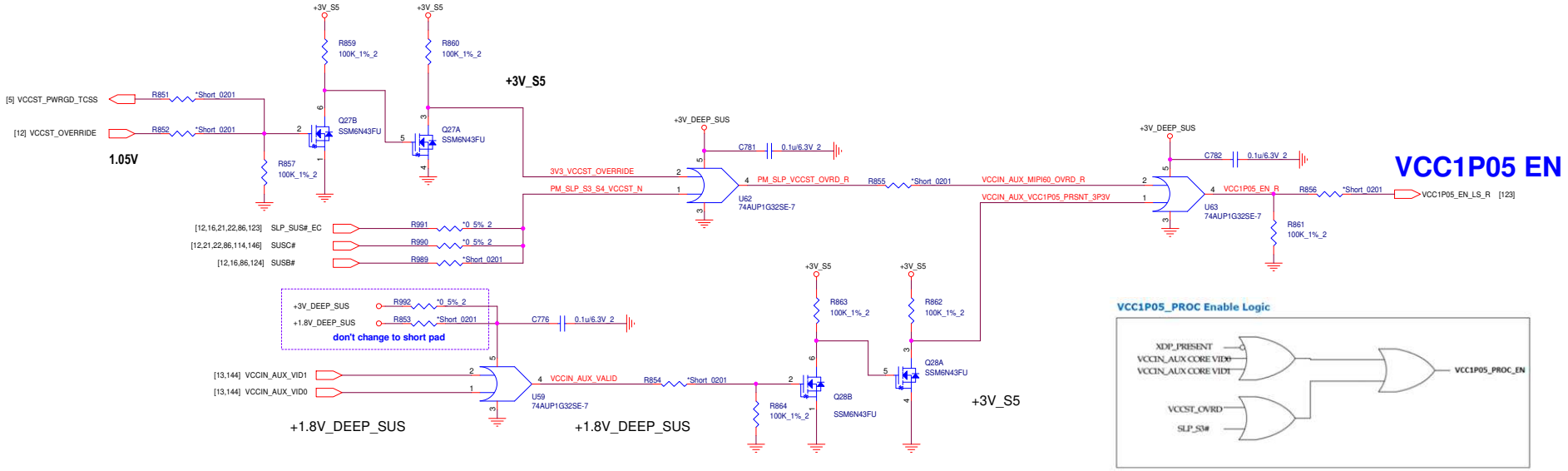
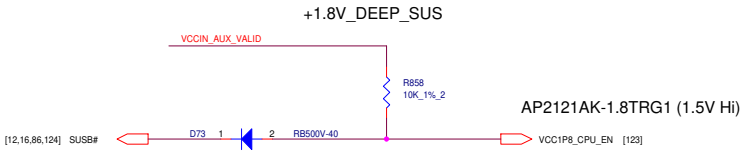
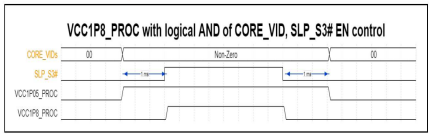
VCC1P05 EN



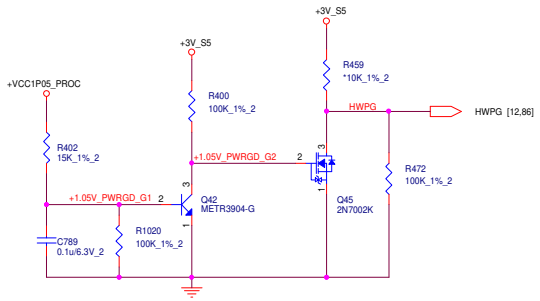
+VCC1P8_PROC EN



VCC1P8_PROC with logical AND of CORE_VIDs, SLP_S3# EN Control

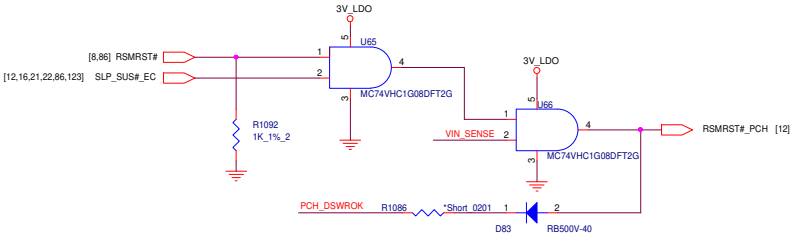


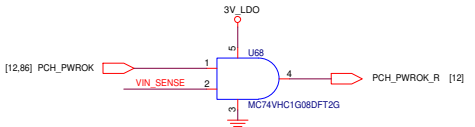
VCCST(+VCC1P05_PROC) - HWPG

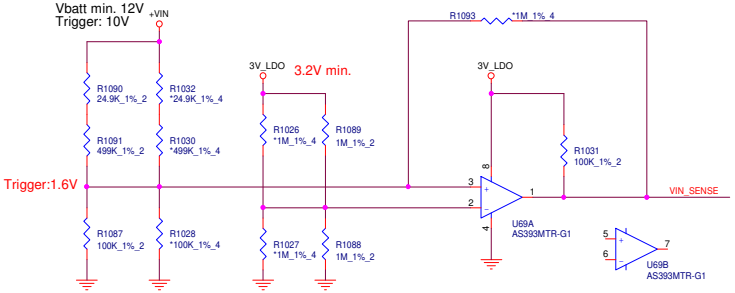


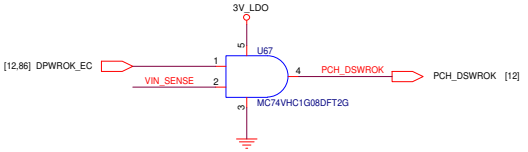
Surprise Power Down

(EC must take RSMRST# low with DPWROK_EC too)









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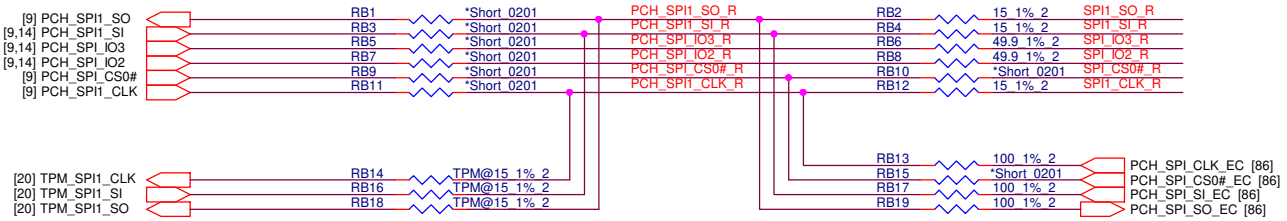
PCH

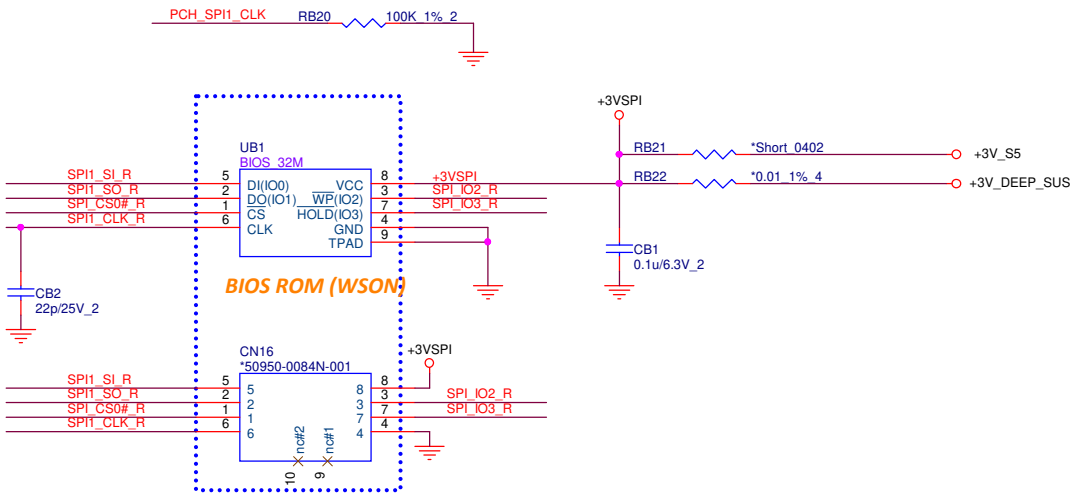
TPM

ROM

EC

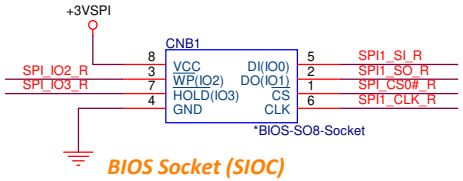


For Glitch Free



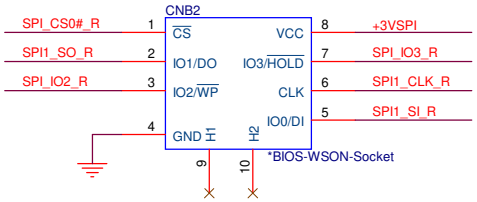
BIOS Socket (WSON)

DFHS08FS060 for WSON 8x6 (32M)



BIOS Socket (SIOC)

DG008000011 for SOIC8 (16M)



BIOS Socket (WSON)

DFHS08FS046 for WSON 6x5 (16M)

	Vender	Size	P/N	WSON8
	Winbond	32M	AKE3JF-KN01	W25Q256JVEIN
	MAX	32M	AKE3JZ-KZ01	MX25L25673GZ4I-08G
	Winbond	16M	AKE3DF-KN01	W25Q128JVSIQ(SOIC)

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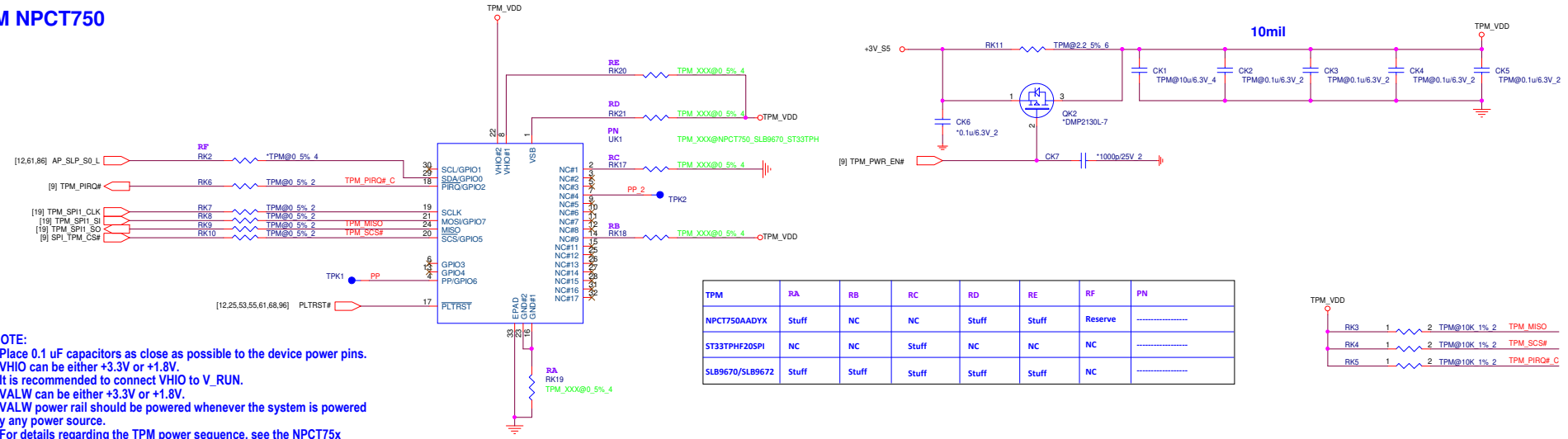
TPM NPCT750



TPM	RA	RB	RC	RD	RE	RF	PN
NPCT750AADYX	Stuff	NC	NC	Stuff	Stuff	Reserve	----------
ST33TPHF20SPI	NC	NC	Stuff	NC	NC	NC	----------
SLB9670/SLB9672	Stuff	Stuff	Stuff	Stuff	Stuff	NC	----------

NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- VHIO can be either +3.3V or +1.8V.
- It is recommended to connect VHIO to V_RUN.
- VALW can be either +3.3V or +1.8V.
- VALW power rail should be powered whenever the system is powered by any power source.
- For details regarding the TPM power sequence, see the NPCT75x Datasheet and Board Design Guidelines.

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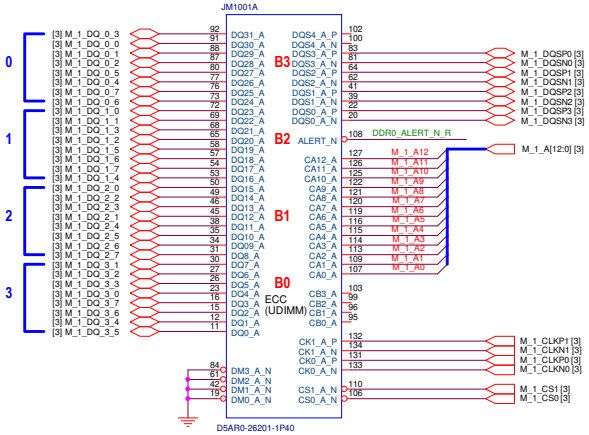
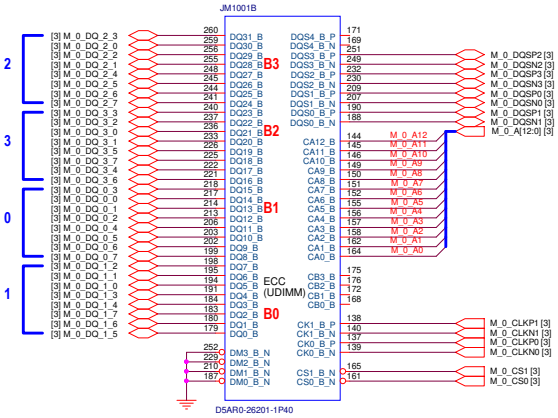
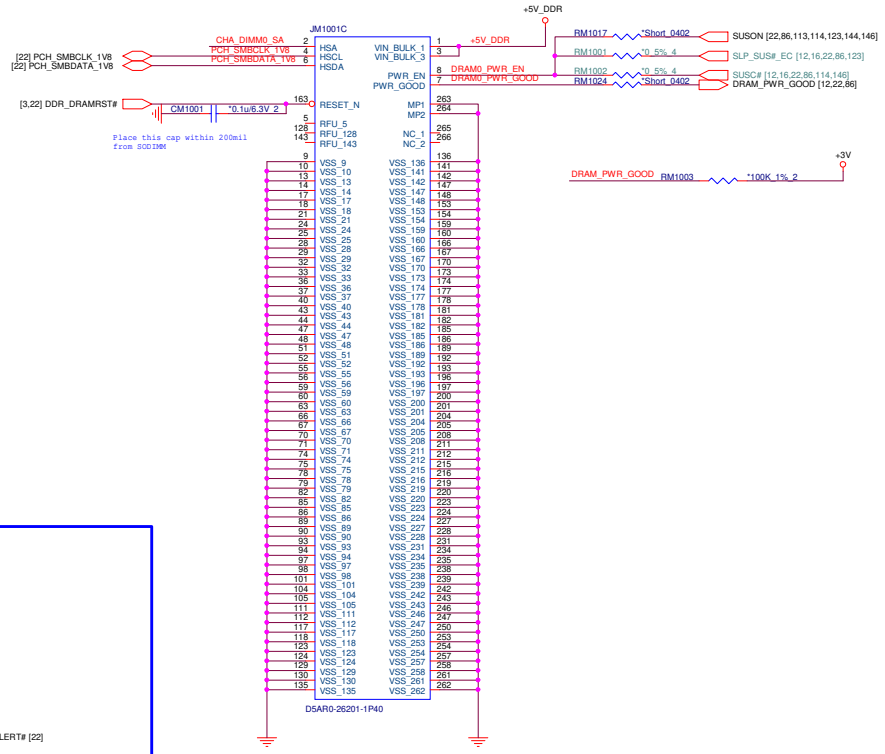
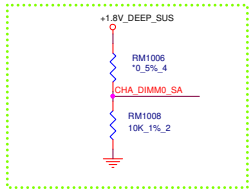
DDR5 SODIMM (Reverse)





To DDR5 PMIC

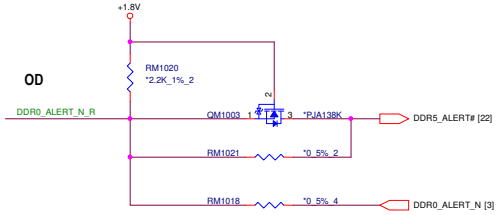




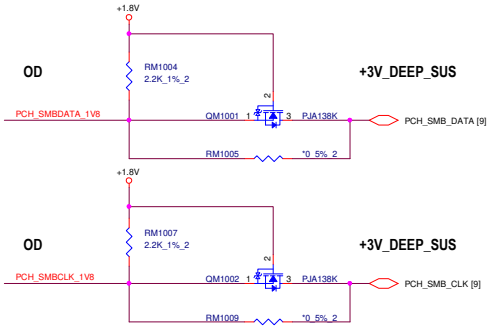
10K ,15.4K,23.2K,35.7K

CPU	CKE0/1 CH.A DIMM1 (JM1001)	CKE0/1 CH.B DIMM2 (JM1002)

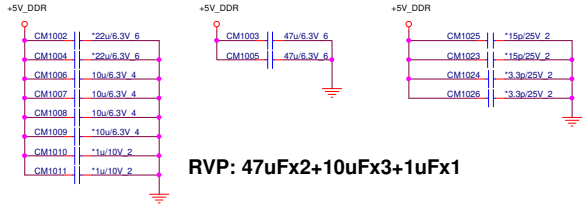
DDR5 CRC / Parity error indicator



Debug purposal



Place these Caps near So-Dimm



RVP: 47uFx2+10uFx3+1uFx1

Memeoy Size Note [619501 - P.112]
Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size should be greater or equal to channel B size.

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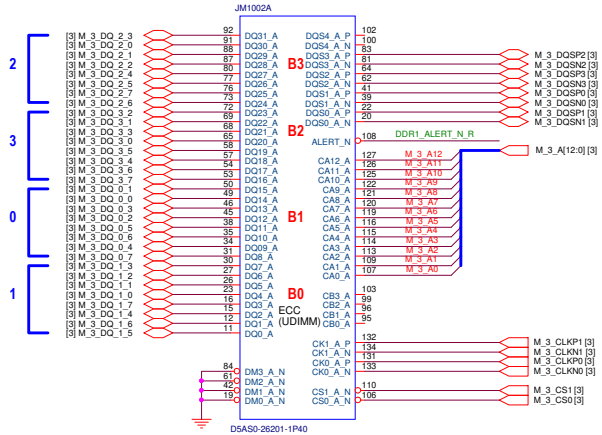
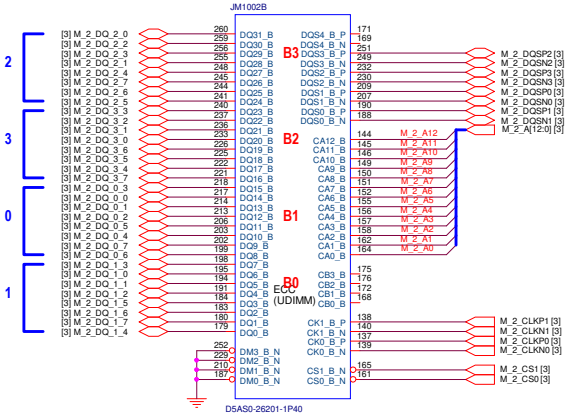
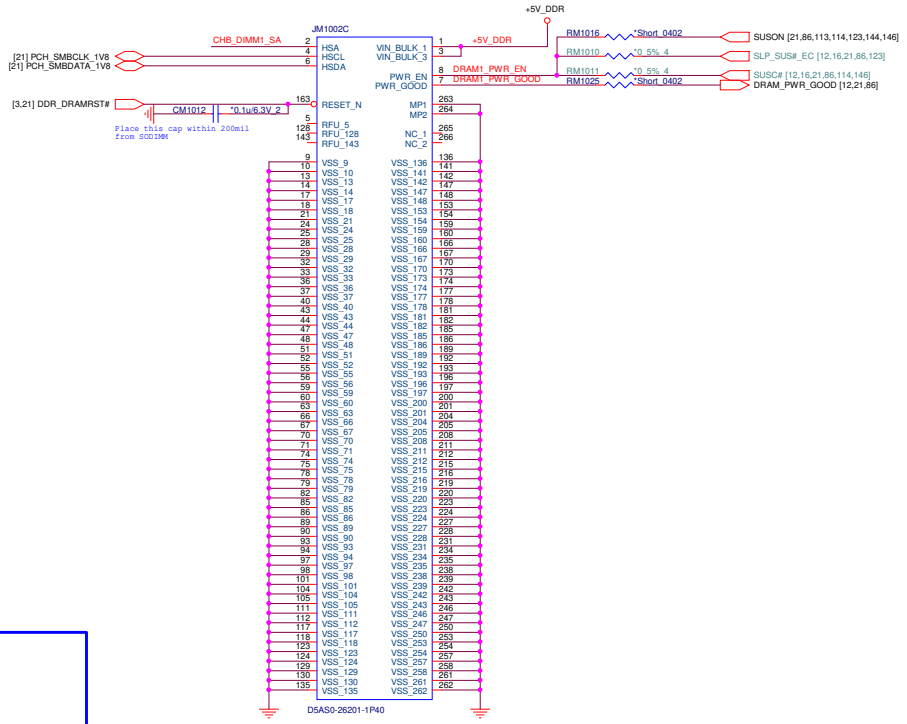
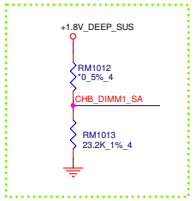
DDR5 SODIMM (Standard)





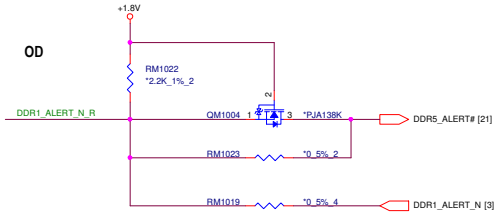
To DDR5 PMIC



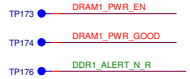


10K,15.4K 23.2K,35.7K

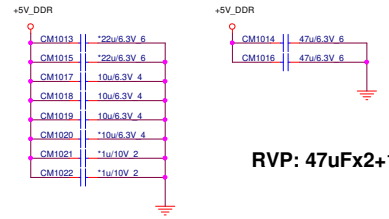
DDR5 CRC / Parity error indicator



Debug purposal



Place these Caps near So-Dimm



RVP: 47uFx2+10uFx3+1uFx1

CPU	CKE0/1 CH.A DIMM1 (JM1001)	CKE0/1 CH.B DIMM2 (JM1002)

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+1V_GFX [28,29,34,131]
+1.8V_AON [26,30,31,32,35,38,39,40,41,45,48,126,130,131]

DG:1.8V
+1.8V_AON
1.8V
3V
[31] DGPU_PWROK
[11] PCIE_CLKREQ_4#
QG9 EV@PJE8406
RG76 EV@10K_1%_2
PEGX_RST#
PEX_CLKREQ

UG6A
GN20-E7
BGA2714
COMMON
1/24 PCI_EXPRESS

		BR31	PEX_WAKE
		BT30	PEX_RST
		BP31	PEX_CLKREQ
[11] CLK_VGA_P		BJ30	PEX_REFCLK
[11] CLK_VGA_N		BK30	PEX_REFCLK
[10] PEG_RXP0	CG390 EV@0.22u/6.3V_2 PEG_RXP0_C	BL31	PEX_TX0
[10] PEG_RXN0	CG389 EV@0.22u/6.3V_2 PEG_RXN0_C	BM31	PEX_TX0
[10] PEG_TXP0		BR32	PEX_RX0
[10] PEG_TXN0		BT32	PEX_RX0
[10] PEG_RXP1	CG377 EV@0.22u/6.3V_2 PEG_RXP1_C	BJ32	PEX_TX1
[10] PEG_RXN1	CG376 EV@0.22u/6.3V_2 PEG_RXN1_C	BK32	PEX_TX1
[10] PEG_TXP1		BP33	PEX_RX1
[10] PEG_TXN1		BR33	PEX_RX1
[10] PEG_RXP2	CG388 EV@0.22u/6.3V_2 PEG_RXP2_C	BL33	PEX_TX2
[10] PEG_RXN2	CG387 EV@0.22u/6.3V_2 PEG_RXN2_C	BM33	PEX_TX2
[10] PEG_TXP2		BR34	PEX_RX2
[10] PEG_TXN2		BT34	PEX_RX2
[10] PEG_RXP3	CG375 EV@0.22u/6.3V_2 PEG_RXP3_C	BJ34	PEX_TX3
[10] PEG_RXN3	CG374 EV@0.22u/6.3V_2 PEG_RXN3_C	BK34	PEX_TX3
[10] PEG_TXP3		BP35	PEX_RX3
[10] PEG_TXN3		BR35	PEX_RX3
[10] PEG_RXP4	CG386 EV@0.22u/6.3V_2 PEG_RXP4_C	BL35	PEX_TX4
[10] PEG_RXN4	CG385 EV@0.22u/6.3V_2 PEG_RXN4_C	BM35	PEX_TX4
[10] PEG_TXP4		BR36	PEX_RX4
[10] PEG_TXN4		BT36	PEX_RX4
[10] PEG_RXP5	CG373 EV@0.22u/6.3V_2 PEG_RXP5_C	BJ36	PEX_TX5
[10] PEG_RXN5	CG372 EV@0.22u/6.3V_2 PEG_RXN5_C	BK36	PEX_TX5
[10] PEG_TXP5		BP37	PEX_RX5
[10] PEG_TXN5		BR37	PEX_RX5
[10] PEG_RXP6	CG384 EV@0.22u/6.3V_2 PEG_RXP6_C	BL37	PEX_TX6
[10] PEG_RXN6	CG383 EV@0.22u/6.3V_2 PEG_RXN6_C	BM37	PEX_TX6
[10] PEG_TXP6		BP38	PEX_RX6
[10] PEG_TXN6		BT38	PEX_RX6
[10] PEG_RXP7	CG371 EV@0.22u/6.3V_2 PEG_RXP7_C	BJ38	PEX_TX7
[10] PEG_RXN7	CG370 EV@0.22u/6.3V_2 PEG_RXN7_C	BK38	PEX_TX7
[10] PEG_TXP7		BP39	PEX_RX7
[10] PEG_TXN7		BR39	PEX_RX7
		BL39	PEX_TX8
		BM39	PEX_TX8
		BR40	PEX_RX8
		BT40	PEX_RX8
		BJ40	PEX_TX9
		BK40	PEX_TX9
		BP41	PEX_RX9
		BR41	PEX_RX9
		BL41	PEX_TX10
		BM41	PEX_TX10
		BR42	PEX_RX10
		BT42	PEX_RX10
		BJ42	PEX_TX11
		BK42	PEX_TX11
		BP43	PEX_RX11
		BR43	PEX_RX11
		BL43	PEX_TX12
		BM43	PEX_TX12
		BR44	PEX_RX12
		BT44	PEX_RX12
		BJ44	PEX_TX13
		BK44	PEX_TX13
		BP45	PEX_RX13
		BR45	PEX_RX13
		BL45	PEX_TX14
		BM45	PEX_TX14
		BR46	PEX_RX14
		BT46	PEX_RX14
		BL47	PEX_TX15
		BM47	PEX_TX15
		BP47	PEX_RX15
		BR47	PEX_RX15

1.0V
+1V_GFX

PEX_DVDD	BF32	CG334 EV@1u/10V_2	CG356 EV@22u/6.3V_6
PEX_DVDD	BF34	CG345 EV@1u/10V_2	CG526 EV@22u/6.3V_6
PEX_DVDD	BF35	CG352 EV@1u/10V_2	CG524 EV@10u/6.3V_4
PEX_DVDD	BF37	CG351 EV@1u/10V_2	CG527 EV@10u/6.3V_4
PEX_DVDD	BG32	CG350 EV@1u/10V_2	CG361 EV@10u/6.3V_4
PEX_DVDD	BG34	CG332 EV@1u/10V_2	
PEX_DVDD	BG35	CG523 EV@4.7u/6.3V_4	
PEX_DVDD	BG37	CG322 EV@4.7u/6.3V_4	
PEX_DVDD	BH32		
PEX_DVDD	BH34		
PEX_DVDD	BH35		
PEX_DVDD	BH37		
PEX_CVDD	BF31		
PEX_CVDD	BG31		
PEX_CVDD	BH31		

PEX_DVDD/PEX_CVDD
UNDER GPU: [6x1uF + 2x4.7uF]
NEAR GPU: [3x10uF + 2x22uF]

+1.8V_AON

PEX_HVDD	BF38	CG367 EV@1u/10V_2	CG397 EV@4.7u/6.3V_4	CG395 EV@22u/6.3V_6
PEX_HVDD	BF40	CG379 EV@1u/10V_2	CG399 EV@4.7u/6.3V_4	CG398 EV@22u/6.3V_6
PEX_HVDD	BF41	CG331 EV@1u/10V_2		CG394 EV@10u/6.3V_4
PEX_HVDD	BG38	CG391 EV@1u/10V_2		CG404 EV@10u/6.3V_4
PEX_HVDD	BG40	CG381 EV@1u/10V_2		CG402 EV@10u/6.3V_4
PEX_HVDD	BG41	CG315 EV@1u/10V_2		
PEX_HVDD	BG43	CG368 EV@1u/10V_2		
PEX_HVDD	BG44	CG378 EV@1u/10V_2		
PEX_HVDD	BH38	CG318 EV@1u/10V_2		
PEX_HVDD	BH40			
PEX_HVDD	BH41			
PEX_HVDD	BH43			
PEX_HVDD	BH44			

PEX_HVDD/PEX_PLL_HVDD
UNDER GPU: [9x1uF + 2x4.7uF]
NEAR GPU: [3x10uF + 2x22uF]

+1.8V_AON
PEX_PLL_HVDD BF43 +PEX_PLL_HVDD RG107 EV@0_5%_4
CG408 EV@1u/10V_2

PEX_CVDD_SENSE BK46

PEX_TERMP BT50 PEX_TERMP RG137 EV@2.49K_1%_2

GPU PEX RST#

+1.8V_AON
3V
1.8V
RG75 *EV@Short_0201
CG396 EV@0.1u/6.3V_2
[9] DGPU_HOLD_RST#
[12,20,53,55,61,68,96] PLTRST#
UG1 EV@NL17SZ08DFT2G
RG68 *EV@Short_0201 PEGX_RST#
PEGX_RST# [31,32]
RG69 EV@100K_1%_2

TP205 PEGX_RST#
TP206 DGPU_HOLD_RST#

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+FBVDDQ_MEM [27,35,38,39,40,41,130]
+FBA_PLL_AVDD [27]
+1.8V_AON [25,30,31,32,35,38,39,40,41,45,48,126,130,131]

UG6B
GN20-E7
BGA2714
COMMON
2/24 FBA

[38] VMA_DQ[63:0] → VMA_DQ[63:0]

FBA_D0 AC51 VMA_DQ0
FBA_D1 AB48 VMA_DQ1
FBA_D2 AC52 VMA_DQ2
FBA_D3 AC49 VMA_DQ3
FBA_D4 AF52 VMA_DQ4
FBA_D5 AC54 VMA_DQ5
FBA_D6 AE51 VMA_DQ6
FBA_D7 AF51 VMA_DQ7
FBA_D8 W51 VMA_DQ8
FBA_D9 W50 VMA_DQ9
FBA_D10 W53 VMA_DQ10
FBA_D11 Y54 VMA_DQ11
FBA_D12 Y52 VMA_DQ12
FBA_D13 Y51 VMA_DQ13
FBA_D14 Y49 VMA_DQ14
FBA_D15 AB51 VMA_DQ15
FBA_D16 AM54 VMA_DQ16
FBA_D17 AL51 VMA_DQ17
FBA_D18 AM52 VMA_DQ18
FBA_D19 AJ54 VMA_DQ19
FBA_D20 AM47 VMA_DQ20
FBA_D21 AM51 VMA_DQ21
FBA_D22 AP50 VMA_DQ22
FBA_D23 AM49 VMA_DQ23
FBA_D24 AF54 VMA_DQ24
FBA_D25 AF49 VMA_DQ25
FBA_D26 AH51 VMA_DQ26
FBA_D27 AF47 VMA_DQ27
FBA_D28 AJ52 VMA_DQ28
FBA_D29 AJ51 VMA_DQ29
FBA_D30 AH48 VMA_DQ30
FBA_D31 AJ49 VMA_DQ31
FBA_D32 BA49 VMA_DQ32
FBA_D33 BD47 VMA_DQ33
FBA_D34 BD54 VMA_DQ34
FBA_D35 BD52 VMA_DQ35
FBA_D36 BC51 VMA_DQ36
FBA_D37 BD51 VMA_DQ37
FBA_D38 BF51 VMA_DQ38
FBA_D39 BD49 VMA_DQ39
FBA_D40 BG52 VMA_DQ40
FBA_D41 BG51 VMA_DQ41
FBA_D42 BG54 VMA_DQ42
FBA_D43 BF49 VMA_DQ43
FBA_D44 BJ54 VMA_DQ44
FBA_D45 BG50 VMA_DQ45
FBA_D46 BJ52 VMA_DQ46
FBA_D47 BK53 VMA_DQ47
FBA_D48 AP51 VMA_DQ48
FBA_D49 AP53 VMA_DQ49
FBA_D50 AR52 VMA_DQ50
FBA_D51 AR54 VMA_DQ51
FBA_D52 AU51 VMA_DQ52
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FBA_D54 AV51 VMA_DQ54
FBA_D55 AR49 VMA_DQ55
FBA_D56 AV49 VMA_DQ56
FBA_D57 AV54 VMA_DQ57
FBA_D58 AY51 VMA_DQ58
FBA_D59 AV52 VMA_DQ59
FBA_D60 AY48 VMA_DQ60
FBA_D61 BA54 VMA_DQ61
FBA_D62 BA52 VMA_DQ62
FBA_D63 BA51 VMA_DQ63

FBA-CH0

FBA_CMD0 Y53 CA8_A
FBA_CMD1 AA56 CA0_A
FBA_CMD2 AB55 CA9_A
FBA_CMD3 AB56 RST*
FBA_CMD4 AC56 CA9_B
FBA_CMD5 AC53 CA0_B
FBA_CMD6 AD56 CA8_B
FBA_CMD7 AE55 CA2_B
FBA_CMD8 AE56 CA4_B
FBA_CMD9 AF56 CABI_B
FBA_CMD10 AF53 CABI_A
FBA_CMD11 AG56 CA4_A
FBA_CMD12 AH55 CA2_A
FBA_CMD13 AH56 CA1_A
FBA_CMD14 AJ56 CKE_A
FBA_CMD15 AJ53 CA3_A
FBA_CMD16 AK56 CA5_B
FBA_CMD17 AL55 CKE_B
FBA_CMD18 AL56 CA1_B
FBA_CMD19 AM56 CA7_B
FBA_CMD20 AM53 CA3_B
FBA_CMD21 AN56 CA6_B
FBA_CMD22 AP55 CA6_A
FBA_CMD23 AP56 CA7_A
FBA_CMD24 AR56 CA3_A
FBA_CMD25_NC AR53
FBA_CMD26_NC AT56
FBA_CMD27 AR55 DEBUG0

FBA_CMD[52:0] [38]

FBA-CH1

FBA_CMD28 BM56 CA8_B
FBA_CMD29 BM55 CA0_B
FBA_CMD30 BL56 CA9_B
FBA_CMD31 BK55 RST*
FBA_CMD32 BK56 CA9_A
FBA_CMD33 BJ56 CA0_A
FBA_CMD34 BJ55 CA8_A
FBA_CMD35 BH56 CA2_A
FBA_CMD36 BG53 CA4_A
FBA_CMD37 BG56 CABI_A
FBA_CMD38 BF56 CABI_B
FBA_CMD39 BF55 CA4_B
FBA_CMD40 BE56 CA2_B
FBA_CMD41 BD53 CKE_B
FBA_CMD42 BD56 CA5_B
FBA_CMD43 BC56 CA5_A
FBA_CMD44 BC55 CKE_A
FBA_CMD45 BB56 CA1_A
FBA_CMD46 BA55 CA3_A
FBA_CMD47 BA56 CA7_A
FBA_CMD48 AY56 CA6_A
FBA_CMD49 AY55 CA6_B
FBA_CMD50 AW56 CA3_B
FBA_CMD51 AV53 CA7_B
FBA_CMD52 AV56 CA1_B
FBA_CMD53_NC AU56
FBA_CMD54_NC AU55
FBA_CMD55 AV55 DEBUG1

[38] FBA_DBI[7:0]

FBA_DBI0 AE50 FBA_DQM0
FBA_DBI1 AB50 FBA_DQM1
FBA_DBI2 AL50 FBA_DQM2
FBA_DBI3 AH50 FBA_DQM3
FBA_DBI4 BC50 FBA_DQM4
FBA_DBI5 BF50 FBA_DQM5
FBA_DBI6 AU50 FBA_DQM6
FBA_DBI7 AY50 FBA_DQM7

[38] FBA_EDC[7:0]

FBA_EDC0 AE53 FBA_DQS_WP0
FBA_EDC1 AB53 FBA_DQS_WP1
FBA_EDC2 AL53 FBA_DQS_WP2
FBA_EDC3 AH53 FBA_DQS_WP3
FBA_EDC4 BC53 FBA_DQS_WP4
FBA_EDC5 BF53 FBA_DQS_WP5
FBA_EDC6 AU53 FBA_DQS_WP6
FBA_EDC7 AY53 FBA_DQS_WP7

BN37 BN38 BN39 BN4 BN40 BN41 BN42 BN43 GND

FBA_CLK0 AP48 VMA_CLK0 [38]
FBA_CLK0 AP47 VMA_CLK0# [38]
FBA_CLK1 AR48 VMA_CLK1 [38]
FBA_CLK1 AR47 VMA_CLK1# [38]

FBA_WCK01 AE48 VMA_WCK01 [38]
FBA_WCK01 AE47 VMA_WCK01# [38]
FBA_WCKB01 AC48 VMA_WCKB01 [38]
FBA_WCK23 AC47 VMA_WCKB01# [38]
FBA_WCK23 AL48 VMA_WCK23 [38]
FBA_WCKB23 AL47 VMA_WCK23# [38]
FBA_WCKB23 AJ48 VMA_WCKB23 [38]
FBA_WCK45 AJ47 VMA_WCKB23# [38]
FBA_WCK45 BA47 VMA_WCK45 [38]
FBA_WCKB45 BA48 VMA_WCK45# [38]
FBA_WCKB45 BC48 VMA_WCKB45 [38]
FBA_WCK67 BC47 VMA_WCKB45# [38]
FBA_WCK67 AU48 VMA_WCK67 [38]
FBA_WCKB67 AU47 VMA_WCK67# [38]
FBA_WCKB67 AV48 VMA_WCKB67 [38]
AV47 VMA_WCKB67# [38]

+FBA_PLL_AVDD
+1.8V_AON
FB_PLLVDD AC46 AE11 AP46
LG2 1 2 EV@HCB1005KF-330T30_3A

CG407 EV@22u/6.3V_6
CG406 EV@4.7u/6.3V_4
CG197 EV@1u/10V_2
CG198 EV@1u/10V_2
CG123 EV@1u/10V_2
CG184 EV@1u/10V_2
CG305 EV@1u/10V_2
CG245 EV@1u/10V_2

FB_PLLVDD
UNDER GPU: [6x1uF]
NEAR GPU: [1x22uF + 1x4.7uF]

UG6C
GN20-E7
BGA2714
COMMON
3/24 FBB

[39] VMB_DQ[63:0]

FBB_D0 D37 VMB_DQ0
FBB_D1 J37 VMB_DQ1
FBB_D2 G37 VMB_DQ2
FBB_D3 F37 VMB_DQ3
FBB_D4 H38 VMB_DQ4
FBB_D5 E38 VMB_DQ5
FBB_D6 F40 VMB_DQ6
FBB_D7 D40 VMB_DQ7
FBB_D8 F34 VMB_DQ8
FBB_D9 J34 VMB_DQ9
FBB_D10 D34 VMB_DQ10
FBB_D11 G34 VMB_DQ11
FBB_D12 E35 VMB_DQ12
FBB_D13 K34 VMB_DQ13
FBB_D14 H35 VMB_DQ14
FBB_D15 K35 VMB_DQ15
FBB_D16 G47 VMB_DQ16
FBB_D17 E44 VMB_DQ17
FBB_D18 F46 VMB_DQ18
FBB_D19 F44 VMB_DQ19
FBB_D20 E46 VMB_DQ20
FBB_D21 C47 VMB_DQ21
FBB_D22 E47 VMB_DQ22
FBB_D23 G49 VMB_DQ23
FBB_D24 G40 VMB_DQ24
FBB_D25 C41 VMB_DQ25
FBB_D26 E41 VMB_DQ26
FBB_D27 F41 VMB_DQ27
FBB_D28 F43 VMB_DQ28
FBB_D29 C44 VMB_DQ29
FBB_D30 H41 VMB_DQ30
FBB_D31 H44 VMB_DQ31
FBB_D32 L51 VMB_DQ32
FBB_D33 L52 VMB_DQ33
FBB_D34 N51 VMB_DQ34
FBB_D35 L49 VMB_DQ35
FBB_D36 L54 VMB_DQ36
FBB_D37 N47 VMB_DQ37
FBB_D38 P51 VMB_DQ38
FBB_D39 P49 VMB_DQ39
FBB_D40 T51 VMB_DQ40
FBB_D41 P52 VMB_DQ41
FBB_D42 P54 VMB_DQ42
FBB_D43 U47 VMB_DQ43
FBB_D44 U51 VMB_DQ44
FBB_D45 U52 VMB_DQ45
FBB_D46 U54 VMB_DQ46
FBB_D47 U49 VMB_DQ47
FBB_D48 D52 VMB_DQ48
FBB_D49 C53 VMB_DQ49
FBB_D50 C54 VMB_DQ50
FBB_D51 C55 VMB_DQ51
FBB_D52 D55 VMB_DQ52
FBB_D53 D54 VMB_DQ53
FBB_D54 F56 VMB_DQ54
FBB_D55 F49 VMB_DQ55
FBB_D56 G53 VMB_DQ56
FBB_D57 H49 VMB_DQ57
FBB_D58 H51 VMB_DQ58
FBB_D59 G51 VMB_DQ59
FBB_D60 H52 VMB_DQ60
FBB_D61 H54 VMB_DQ61
FBB_D62 K48 VMB_DQ62
FBB_D63 K51 VMB_DQ63

FBB-CH0

FBB_CMD0 B37 CA8_A
FBB_CMD1 A37 CA0_A
FBB_CMD2 A38 CA9_A
FBB_CMD3 D38 RST*
FBB_CMD4 A39 CA9_B
FBB_CMD5 B40 CA0_B
FBB_CMD6 A40 CA8_B
FBB_CMD7 A41 CA2_B
FBB_CMD8 D41 CA4_B
FBB_CMD9 A42 CABI_B
FBB_CMD10 B43 CABI_A
FBB_CMD11 A43 CA4_A
FBB_CMD12 A44 CA2_A
FBB_CMD13 D44 CA1_A
FBB_CMD14 A45 CKE_A
FBB_CMD15 B46 CA3_A
FBB_CMD16 A46 CA5_B
FBB_CMD17 A47 CKE_B
FBB_CMD18 D47 CA1_B
FBB_CMD19 A48 CA7_B
FBB_CMD20 B49 CA3_B
FBB_CMD21 A49 CA6_B
FBB_CMD22 B50 CA6_A
FBB_CMD23 A50 CA7_A
FBB_CMD24 C50 CA3_A
FBB_CMD25_NC A51
FBB_CMD26_NC B52
FBB_CMD27 C52 DEBUG0

FBB_CMD[52:0] [39]

FBB-CH1

FBB_CMD28 Y56 CA8_B
FBB_CMD29 W56 CA0_B
FBB_CMD30 W55 CA9_B
FBB_CMD31 V56 RST*
FBB_CMD32 U53 CA9_A
FBB_CMD33 U56 CA0_A
FBB_CMD34 T56 CA8_A
FBB_CMD35 T55 CA2_A
FBB_CMD36 R56 CA4_A
FBB_CMD37 P53 CABI_A
FBB_CMD38 P56 CABI_B
FBB_CMD39 N56 CA4_B
FBB_CMD40 N55 CA2_B
FBB_CMD41 M56 CKE_B
FBB_CMD42 L53 CA5_B
FBB_CMD43 L56 CA5_A
FBB_CMD44 K56 CKE_A
FBB_CMD45 K55 CA1_A
FBB_CMD46 J56 CA3_A
FBB_CMD47 H53 CA7_A
FBB_CMD48 H56 CA6_A
FBB_CMD49 G56 CA6_B
FBB_CMD50 G55 CA3_B
FBB_CMD51 E56 CA7_B
FBB_CMD52 B54 CA1_B
FBB_CMD53_NC B53
FBB_CMD54_NC A52
FBB_CMD55 E55 DEBUG1

[39] FBB_DBI[7:0]

FBB_DBI0 F38 FBB_DQM0
FBB_DBI1 F35 FBB_DQM1
FBB_DBI2 G46 FBB_DQM2
FBB_DBI3 G43 FBB_DQM3
FBB_DBI4 N50 FBB_DQM4
FBB_DBI5 T50 FBB_DQM5
FBB_DBI6 E49 FBB_DQM6
FBB_DBI7 K50 FBB_DQM7

[39] FBB_EDC[7:0]

FBB_EDC0 C38 FBB_DQS_WP0
FBB_EDC1 C35 FBB_DQS_WP1
FBB_EDC2 D46 FBB_DQS_WP2
FBB_EDC3 D43 FBB_DQS_WP3
FBB_EDC4 N53 FBB_DQS_WP4
FBB_EDC5 T53 FBB_DQS_WP5
FBB_EDC6 E53 FBB_DQS_WP6
FBB_EDC7 K53 FBB_DQS_WP7

BN44 BN45 BN46 BN47 BN48 BN6 BN9 BP1 GND

FBB_CLK0 K44 VMB_CLK0 [39]
FBB_CLK0 J44 VMB_CLK0# [39]
FBB_CLK1 J46 VMB_CLK1 [39]
FBB_CLK1 K46 VMB_CLK1# [39]

FBB_WCK01 J40 VMB_WCK01 [39]
FBB_WCK01 K40 VMB_WCK01# [39]
FBB_WCKB01 K38 VMB_WCKB01 [39]
FBB_WCKB01 J38 VMB_WCKB01# [39]
FBB_WCK23 J43 VMB_WCK23 [39]
FBB_WCK23 K43 VMB_WCK23# [39]
FBB_WCKB23 K41 VMB_WCKB23 [39]
FBB_WCKB23 J41 VMB_WCKB23# [39]
FBB_WCK45 P47 VMB_WCK45 [39]
FBB_WCK45 P48 VMB_WCK45# [39]
FBB_WCKB45 T48 VMB_WCKB45 [39]
FBB_WCKB45 T47 VMB_WCKB45# [39]
FBB_WCK67 K47 VMB_WCK67 [39]
FBB_WCK67 J47 VMB_WCK67# [39]
FBB_WCKB67 L47 VMB_WCKB67 [39]
FBB_WCKB67 L48 VMB_WCKB67# [39]

+FBA_PLL_AVDD
FB_PLLVDD L17 +FBA_PLL_AVDD
CG98 EV@1u/10V_2

CKE_A

+FBVDDQ_MEM → RG37 EV@10K_1%_2 → FBA_CMD14 FBA_CMD44
+FBVDDQ_MEM → RG50 EV@10K_1%_2

CKE_B

+FBVDDQ_MEM → RG39 EV@10K_1%_2 → FBA_CMD17 FBA_CMD41
+FBVDDQ_MEM → RG51 EV@10K_1%_2

RESET

FBA_CMD3 FBA_CMD31
RG132 EV@10K_1%_2
RG28 EV@10K_1%_2

CKE_A

+FBVDDQ_MEM → RG3 EV@10K_1%_2 → FBB_CMD14 FBB_CMD44
+FBVDDQ_MEM → RG21 EV@10K_1%_2

CKE_B

+FBVDDQ_MEM → RG17 EV@10K_1%_2 → FBB_CMD17 FBB_CMD41
+FBVDDQ_MEM → RG20 EV@10K_1%_2

RESET

FBB_CMD3 FBB_CMD31
RG25 EV@10K_1%_2
RG11 EV@10K_1%_2

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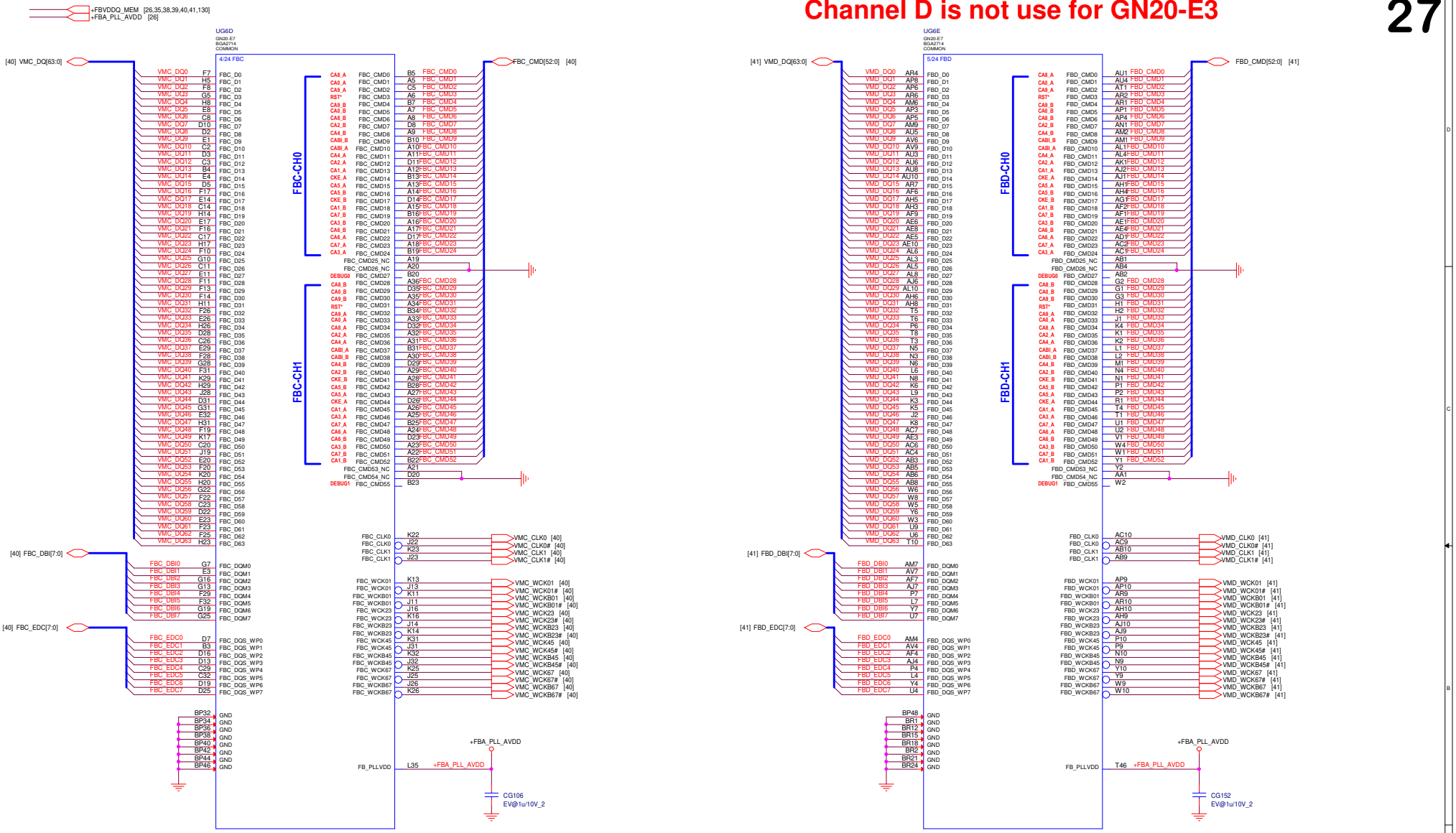
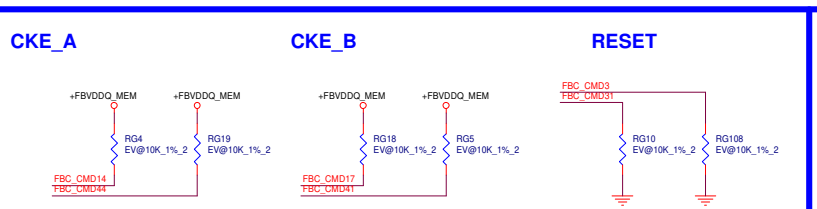
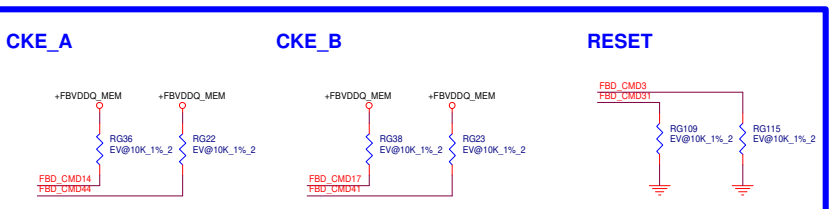
Channel D is not use for GN20-E3







Quanta Computer Inc.
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Size	Document Number	Rev
C	Memory-FB/CD	A1A
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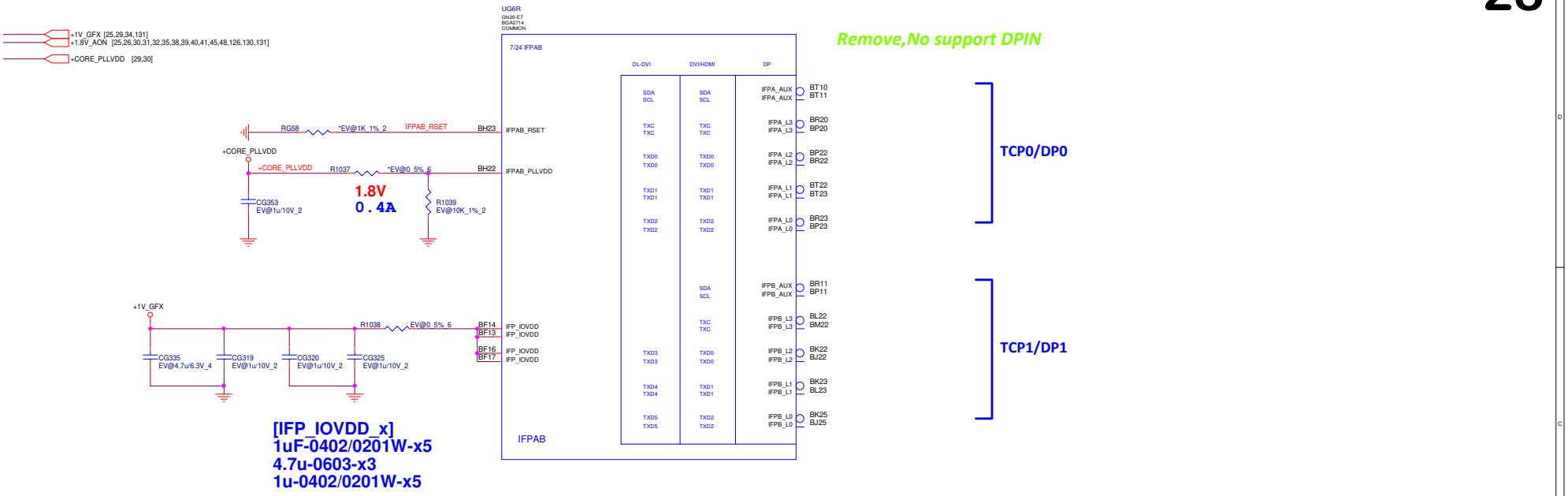

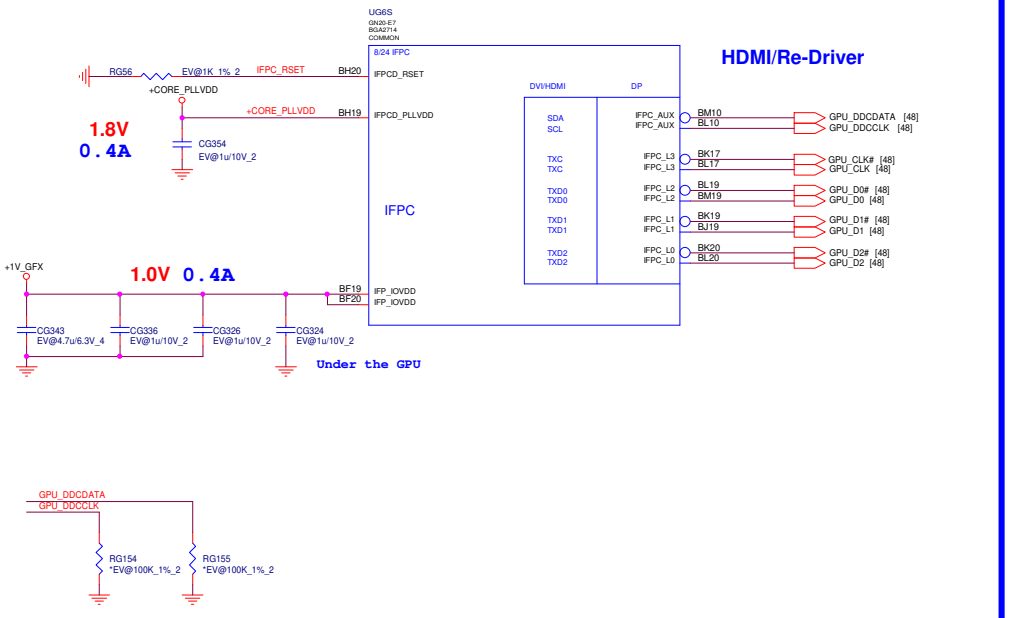

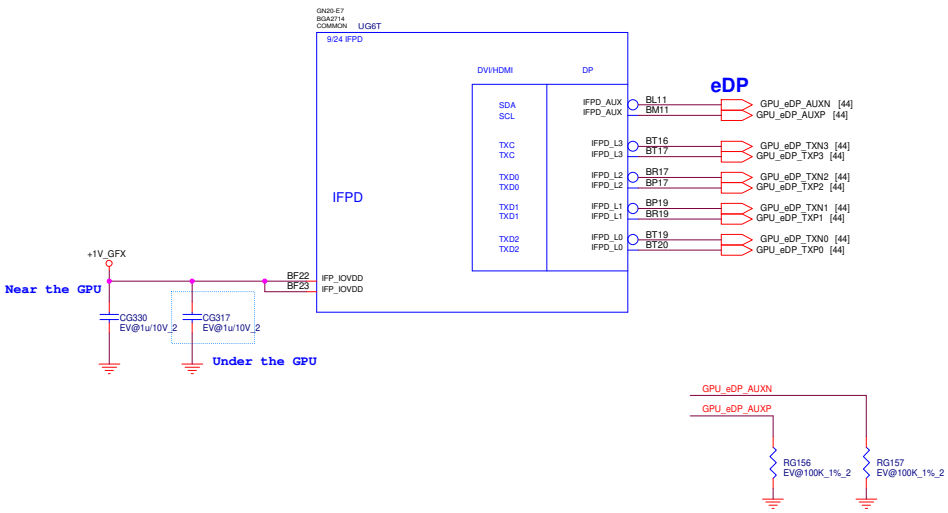

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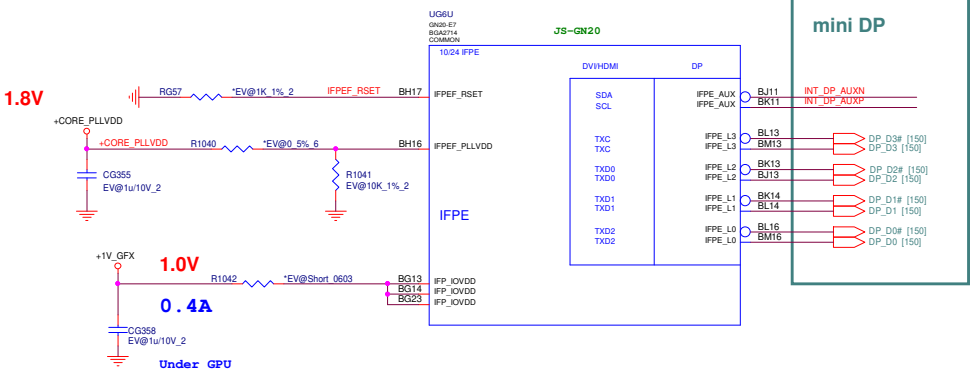
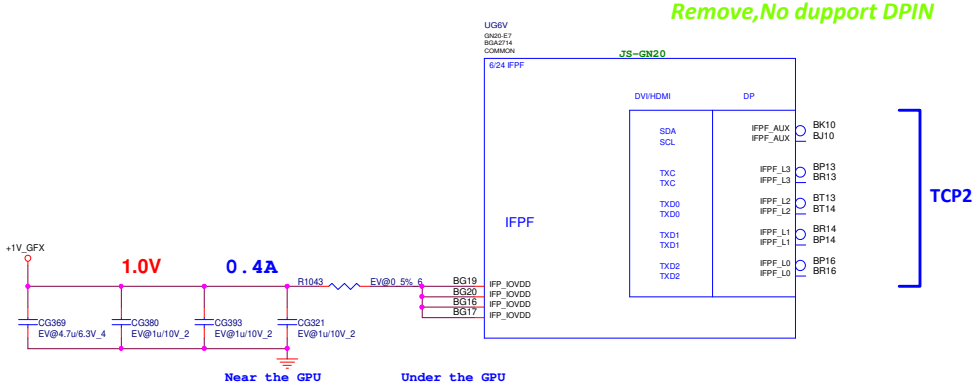
Option No support DP,remove

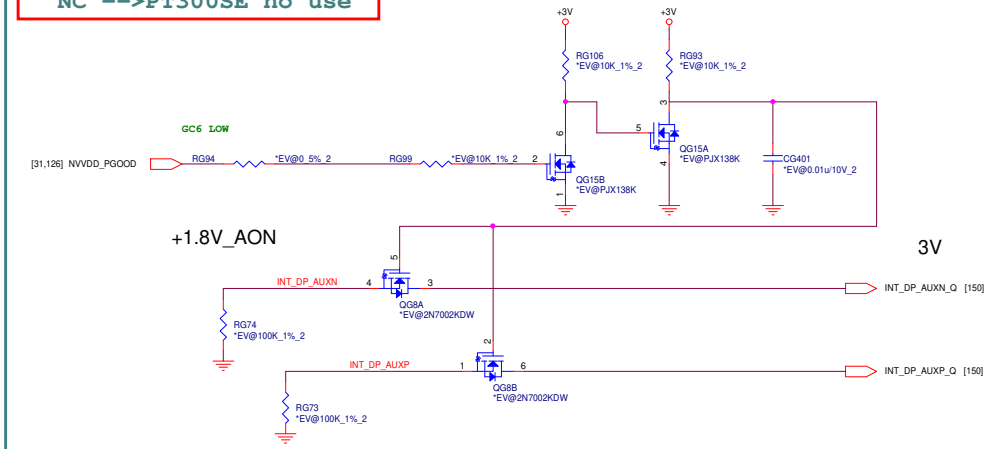


Remove,No dupport DPIN



Option No support DP,remove

NC -->PT300SE no use



For DP port , prevent backdrive leakage current into GPU while HDMI mode

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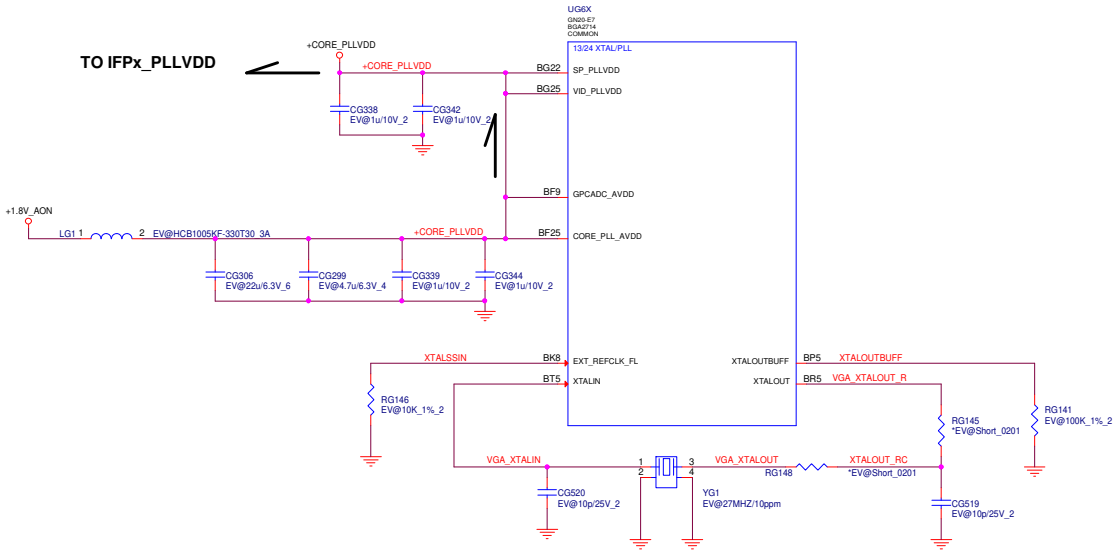
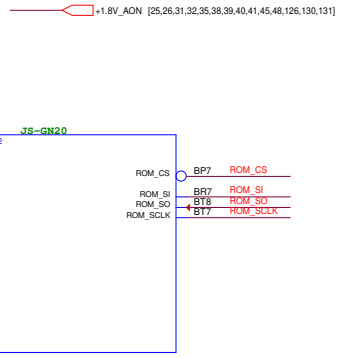
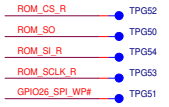
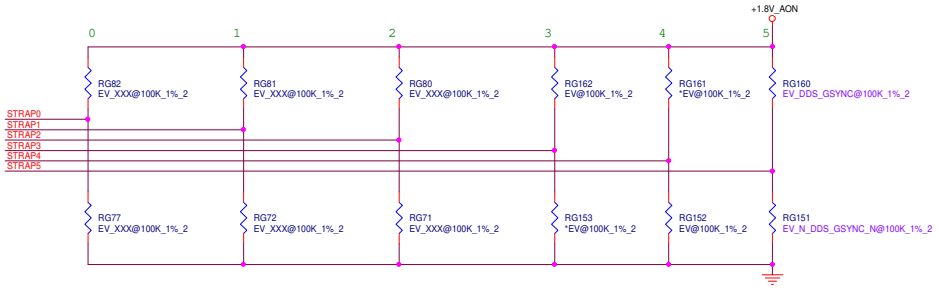
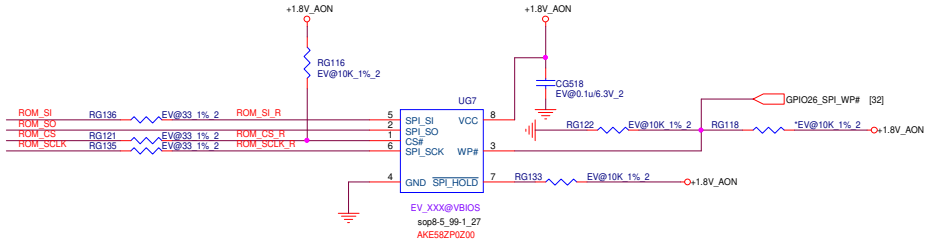




Vendor	Description	Size	P/N	GPU
WND	W25Q16JWSNIQ	16Mb	AKE58ZN0N03	
MAX	MX25U1633FM1I	16Mb	AKE58ZP0Z00	



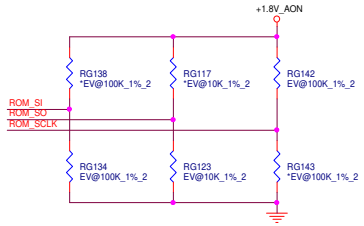




	STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
	L	L	L	0	0	0	0
Non-GSYNC	L	L	H	0	0	0	1
	L	H	L	0	0	1	0
	L	H	H	0	0	1	1
	H	L	L	0	1	0	0
GSYNC	H	L	H	0	1	0	1

STRAP2	STRAP1	STRAP0
L	H	L
L	L	H
L	L	L
L	M	L
H	L	H

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT Strap
L	L	L	FS_OVERT# function DISABLED
L	L	H	FS_OVERT# function ENABLED(Default)



VRAM Table for GN20-E GDDR6

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
2 (0x2)	IC SGRAM(180P)H56C8H24AIR-S2C STNBS	Hynix	H56C8H24AIR-S2C		AKG5QGUTW43
1 (0x1)	IC SGRAM(180P)MT61K256M32JE(DC1940)STNBS	Micron	MT61K256M32JE		AKG5QGDTL08
0 (0x0)	IC SGRAM(180P)K4Z80325BC-HC(DC2001)STNBS	Samsung	K4Z80325BC-HC		AKG58G0T519
9 (0x9)		Samsung			
5 (0x5)	IC SGRAM(180P) H56G32CS4DX005(BGA)STNBS	Hynix C-die	H56G32CS4DX005		AKG5QGUTW50

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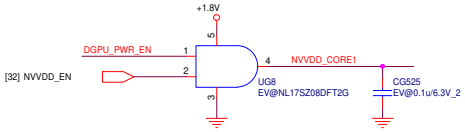
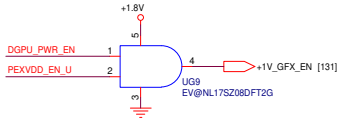
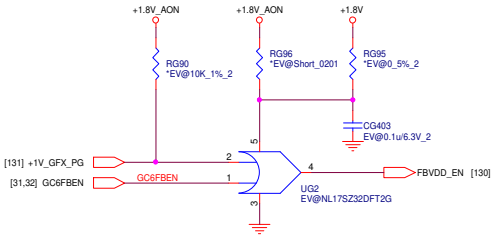
(2) NVVDD ENABLE



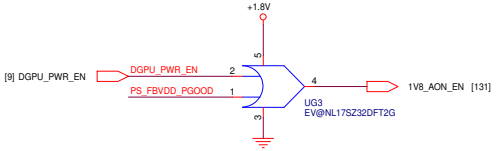
(3) PEX_VDD_ENABLE



(4) FBVDDQ ENABLE

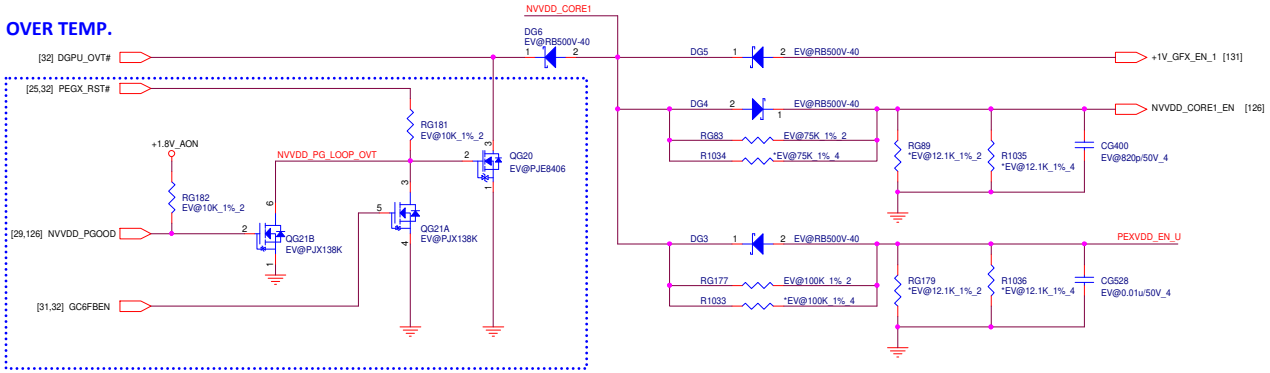


(1) 1V8_AON ENABLE



(DGPU_PWR_EN) --> 1V8_AON(VPP) -->(NVVDD_EN) --> NVVDD --> (NVVDD_PG) --> PEXVDD (1V_GFX) --> FBVDD --> (FBVDD_PG) --> (DGPU_PWROK_Q) --> (PEX_RST#)

OVER TEMP.



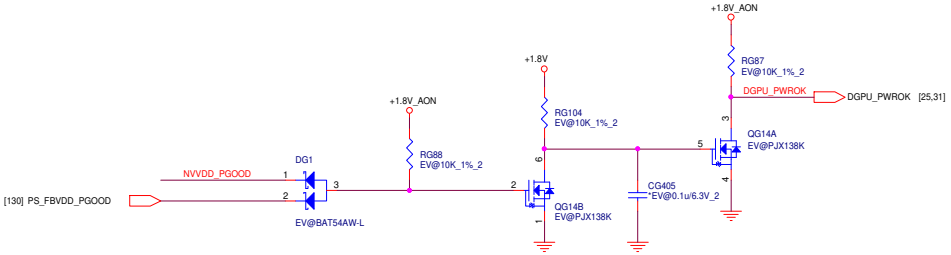
NVVDD POWER GOOD LOOPBACK
![!(NVVDD_PGOOD || GC6FBEN) && (PEGX_RST#)]

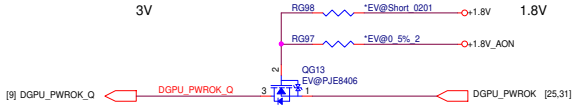
PEX_VDD_ENABLE

Table 4.6 Low Power State Summary

Low Power Features	1V8	NV3V3	MSVDD	NVVDD	PEXVDD	VPP	FBVDD	3V3	PWR_SRC
Normal Operation	ON	ON	ON	ON	ON	ON	ON	ON	ON
P-State 4.0 Rail Gating (NVVDD & MSVDD split)	ON	ON	ON	OFF	ON	ON	ON	ON	ON
P-State 4.0 Rail Gating (NVVDD & MSVDD merged)	ON	ON	ON	ON	ON	ON	ON	ON	ON
GC6 3.0	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON
GC-OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

POWER GOOD





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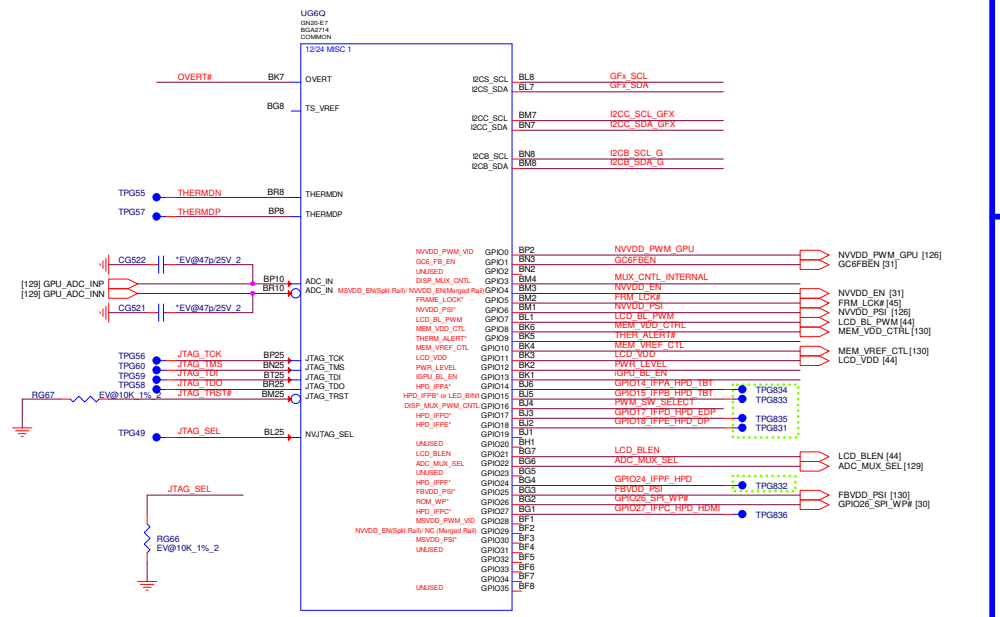
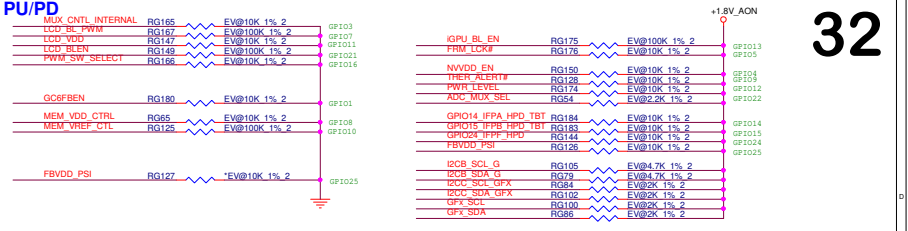
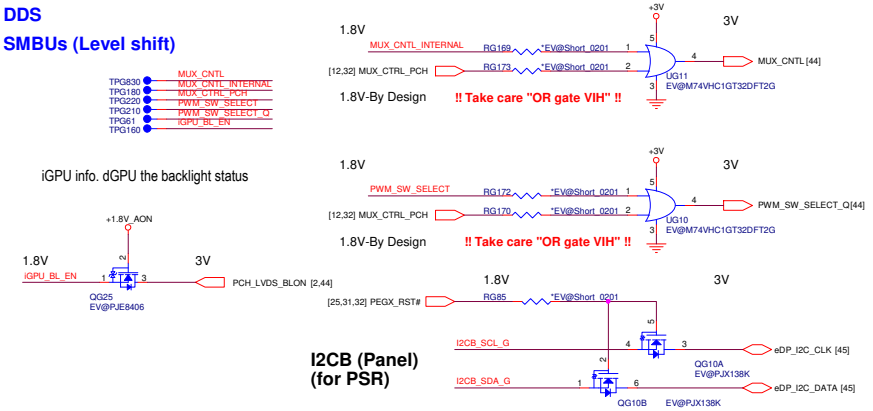


PU/PD

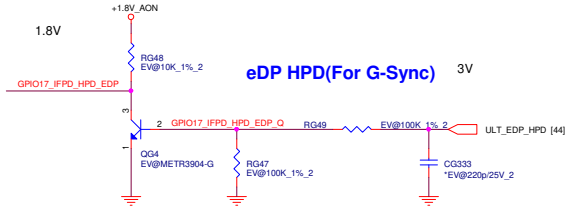


DDS

SMBUs (Level shift)



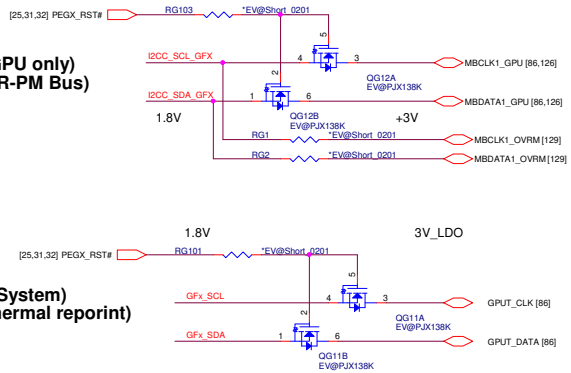
eDP HPD(For G-Sync)



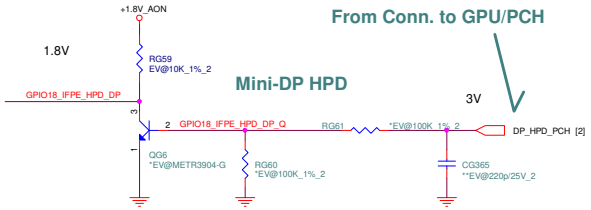
Remove,No dupport DPIN

TBT DPI0 HPD

SMBUs (Level shift)



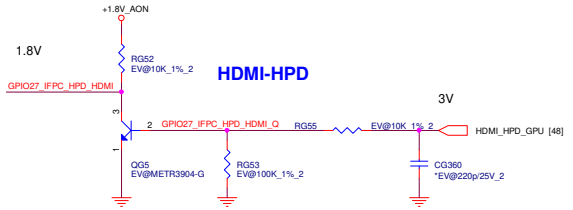
Mini-DP HPD



Remove,No dupport DPIN

TBT DPI1 HPD

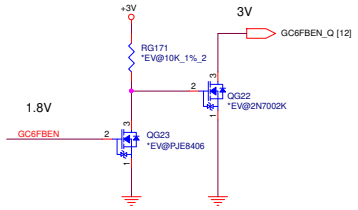
HDMI-HPD



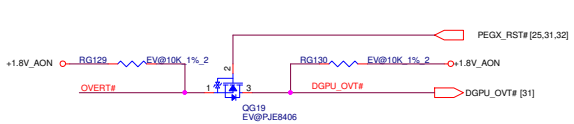
Remove,No dupport DPIN

TBT DPI2 HPD

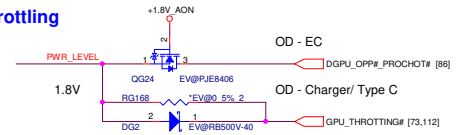
GC6 2.1 FB enable (Level shift)-PCH



DGPU THERMAL ALERT



GPU Throttling



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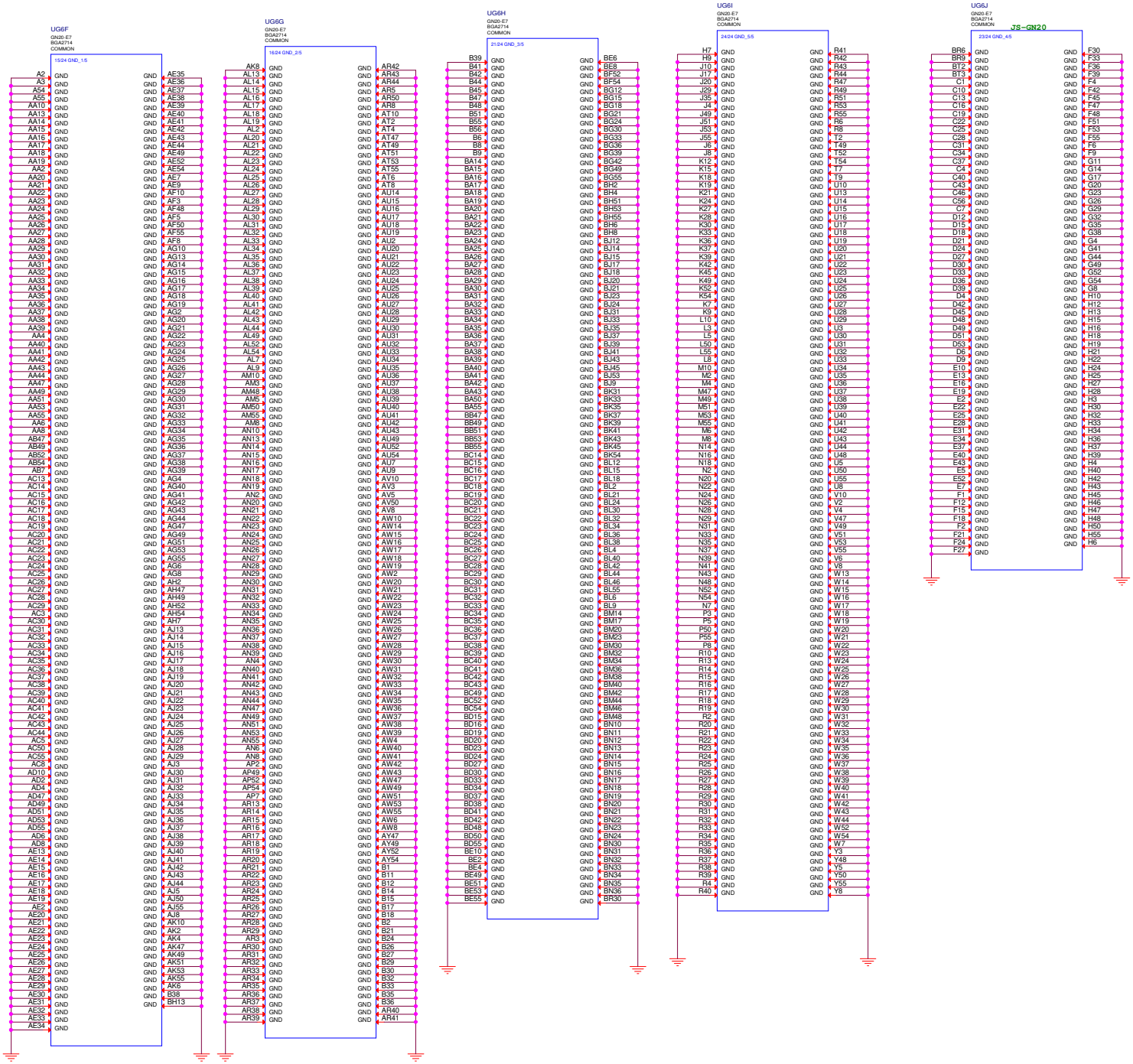
UG6F
GND20-E7
BGA2714
COMMON
15/24 GND_1,5
UG6G
GND20-E7
BGA2714
COMMON
16/24 GND_2,5
UG6H
GND20-E7
BGA2714
COMMON
21/24 GND_3,5
UG6I
GND20-E7
BGA2714
COMMON
24/24 GND_5,5
UG6J
GND20-E7
BGA2714
COMMON
JS-GN20
23/24 GND_4,5

NVVDD [126,127]
+1V_GFX [25,28,29,131]

UG6M
GN20-E7
BGA2714
COMMON
17/24 VDD_1/2

UG6N
GN20-E7
BGA2714
COMMON
18/24 VDD_2/2

UG6K
GN20-E7
BGA2714
COMMON
11/24 XVDD
CONFIGURABLE
POWER CHANNELS
(NC on substrate)

UG6L
GN20-E7
BGA2714
COMMON
22/24 VDDMS

VDD_SENSE BT48
GND_SENSE BR48
VGPU_CORE_SENSE [34,126]
VSS_GPU_SENSE [34,126]

VDDMS_SENSE BP49
GNDMS_SENSE BR49
VDDMS_SENSE RG140 *EV@0_5%_2
GNDMS_SENSE RG139 *EV@0_5%_2
VGPU_CORE_SENSE [34,126]
VSS_GPU_SENSE [34,126]

Near GPU

NVVDD
3+1=4 X 330u
CG171 EV@330U 2.5V 3528H2.1 max
CG202 EV@560u/2V 7343H1.9
CG201 EV@330u/2V 7343H1.9
CG170 EV@330U 2.5V 3528H2.1 max

NVVDD
4+3=7 X 47u
CG180 EV@47u/6.3V 8
CG211 EV@47u/6.3V 8
CG166 EV@47u/6.3V 8
CG181 EV@47u/6.3V 8
CG193 EV@47u/6.3V 8
CG168 EV@47u/6.3V 8
CG195 EV@47u/6.3V 8
12+11=23 X 10u
CG241 EV@10u/6.3V 4
CG227 EV@10u/6.3V 4
CG258 EV@10u/6.3V 4
CG225 EV@10u/6.3V 4
CG238 EV@10u/6.3V 4
CG239 EV@10u/6.3V 4
CG229 EV@10u/6.3V 4
CG252 EV@10u/6.3V 4
CG274 EV@10u/6.3V 4
CG210 EV@10u/6.3V 4
CG273 EV@10u/6.3V 4
CG257 EV@10u/6.3V 4
CG259 EV@10u/6.3V 4
CG272 EV@10u/6.3V 4
CG269 EV@10u/6.3V 4
CG256 EV@10u/6.3V 4
CG242 EV@10u/6.3V 4
CG255 EV@10u/6.3V 4
CG228 EV@10u/6.3V 4
CG243 EV@10u/6.3V 4
CG270 EV@10u/6.3V 4
CG223 EV@10u/6.3V 4
CG226 EV@10u/6.3V 4
2 X 4.7u
CG271 EV@4.7u/6.3V 4
CG240 EV@4.7u/6.3V 4

NVVDD
37+29=66 X 1u
CG289 EV@1u/10V 2
CG222 EV@1u/10V 2
CG283 EV@1u/10V 2
CG258 EV@1u/10V 2
CG300 EV@1u/10V 2
CG304 EV@1u/10V 2
CG113 EV@1u/10V 2
CG150 EV@1u/10V 2
CG151 EV@1u/10V 2
CG147 EV@1u/10V 2
CG149 EV@1u/10V 2
CG140 EV@1u/10V 2
CG117 EV@1u/10V 2
CG103 EV@1u/10V 2
CG115 EV@1u/10V 2
CG205 EV@1u/10V 2
CG217 EV@1u/10V 2
CG183 EV@1u/10V 2
CG176 EV@1u/10V 2
CG284 EV@1u/10V 2
CG188 EV@1u/10V 2
CG301 EV@1u/10V 2
CG316 EV@1u/10V 2
CG311 EV@1u/10V 2
CG298 EV@1u/10V 2
CG310 EV@1u/10V 2
CG313 EV@1u/10V 2
CG287 EV@1u/10V 2
CG294 EV@1u/10V 2
CG309 EV@1u/10V 2
CG295 EV@1u/10V 2
CG267 EV@1u/10V 2
CG231 EV@1u/10V 2
CG145 EV@1u/10V 2
CG288 EV@1u/10V 2
CG312 EV@1u/10V 2
CG340 EV@1u/10V 2
CG341 EV@1u/10V 2
CG260 EV@1u/10V 2
CG186 EV@1u/10V 2
CG138 EV@1u/10V 2
CG282 EV@1u/10V 2
CG254 EV@1u/10V 2
CG218 EV@1u/10V 2
CG237 EV@1u/10V 2
CG285 EV@1u/10V 2
CG302 EV@1u/10V 2
CG126 EV@1u/10V 2
CG114 EV@1u/10V 2
CG142 EV@1u/10V 2
CG122 EV@1u/10V 2
CG133 EV@1u/10V 2
CG135 EV@1u/10V 2
CG132 EV@1u/10V 2
CG125 EV@1u/10V 2
CG134 EV@1u/10V 2
CG148 EV@1u/10V 2
CG246 EV@1u/10V 2
CG200 EV@1u/10V 2
CG160 EV@1u/10V 2
CG111 EV@1u/10V 2
CG297 EV@1u/10V 2
CG286 EV@1u/10V 2
CG307 EV@1u/10V 2
CG296 EV@1u/10V 2
CG314 EV@1u/10V 2

Under GPU

NVVDD
CG548 15p/25V_2
CG549 15p/25V_2
CG550 15p/25V_2

+1V_GFX
CG551 *15p/25V_2
CG554 *3.3p/25V_2

NVVDD
UNDER GPU
[37x1uF + 2x4.7uF + 12x10uF + 4x47uF]
Col-ayout
[3x330uF]
or
[12x1uF + 3x4.7uF + 3x10uF + 16x47uF]

MSVDD
UNDER GPU
[29x1uF + 11x10uF + 3x47uF]
Col-ayout
[1x330uF]
or
[4x10uF + 4x47uF]

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C	POWER	A1A
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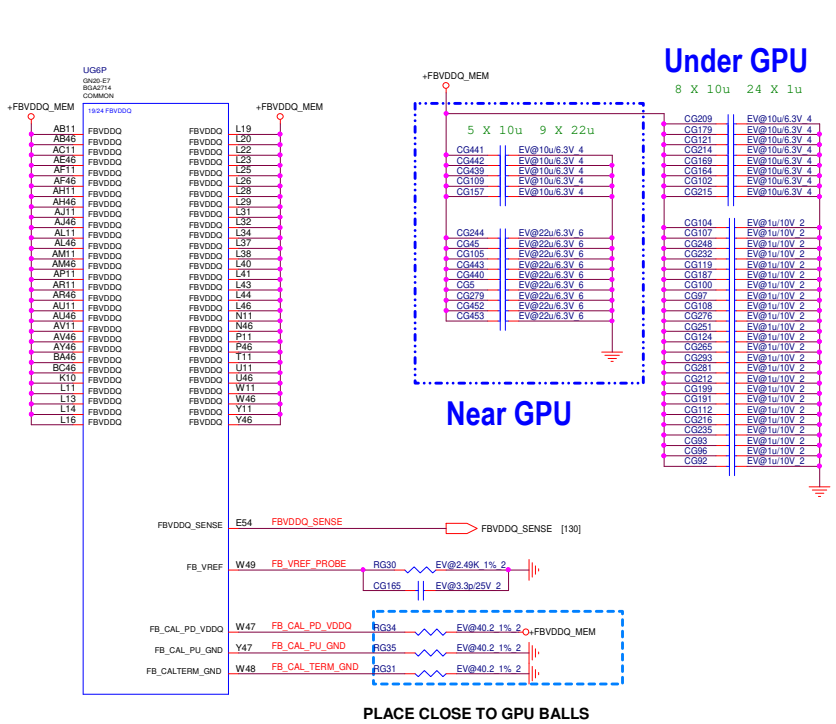
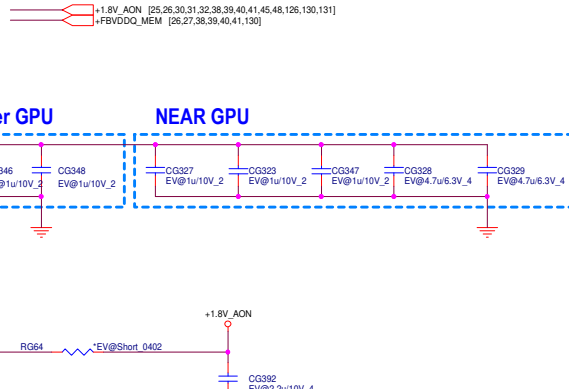


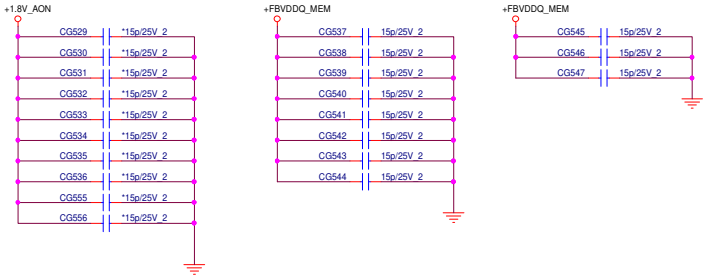
FBVDDQ-GPU side

UNDER GPU
[24x1uF + 8x10uF]
NEAR GPU
[5x10uF + 9x22uF]



1V8

UNDER GPU
[2x1uF]
NEAR GPU
[3x1uF + 2x4.7uF]



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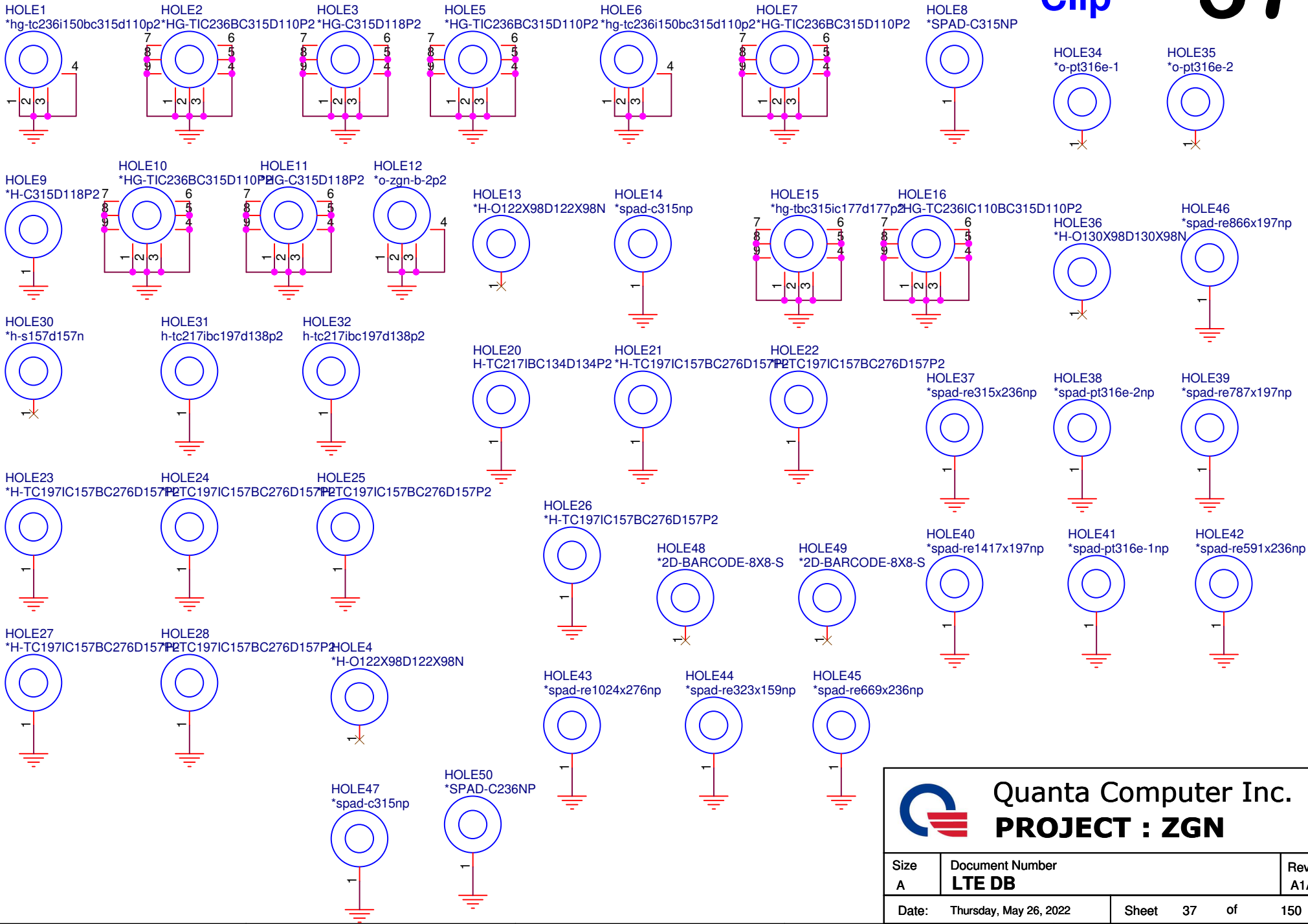
Hole

Clip

37



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A	**LTE DB**	A1A
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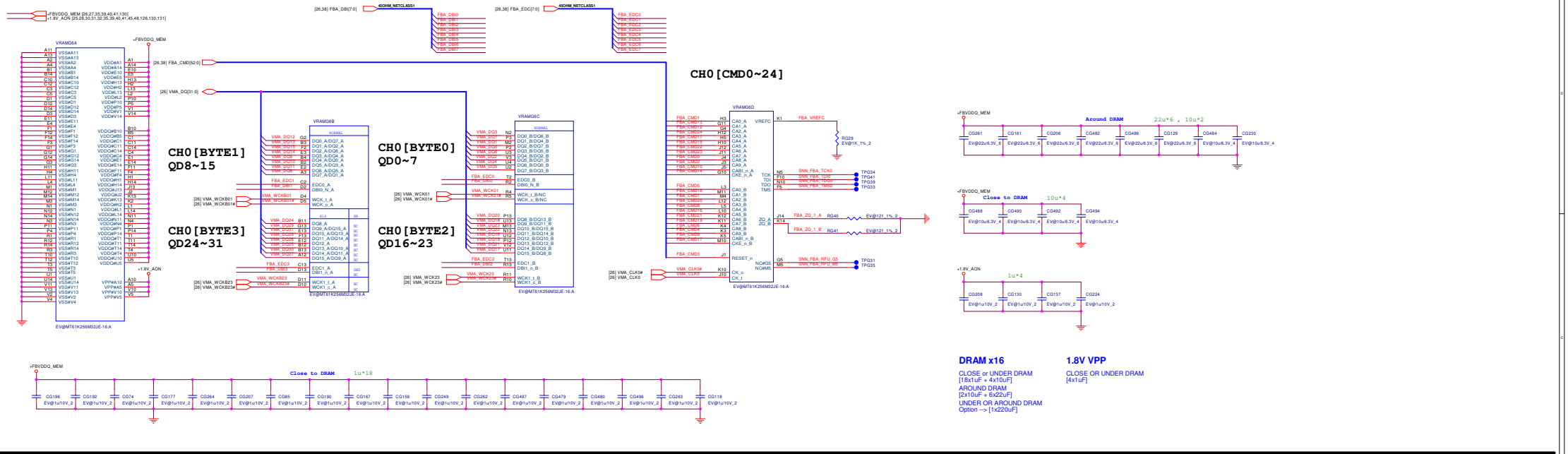
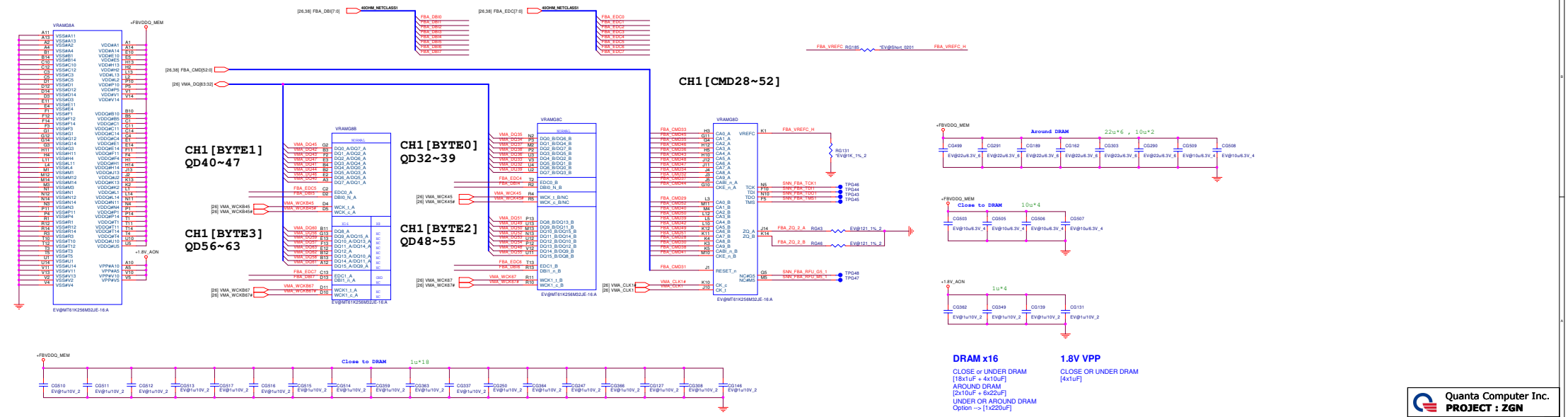
MEMORY: FBA Partition 31..0 x16 Dual Channel DRAM



MEMORY: FBA Partition 63..32 x16 Dual Channel DRAM



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Size	Document Number	Rev
D	GDDR6	A1A
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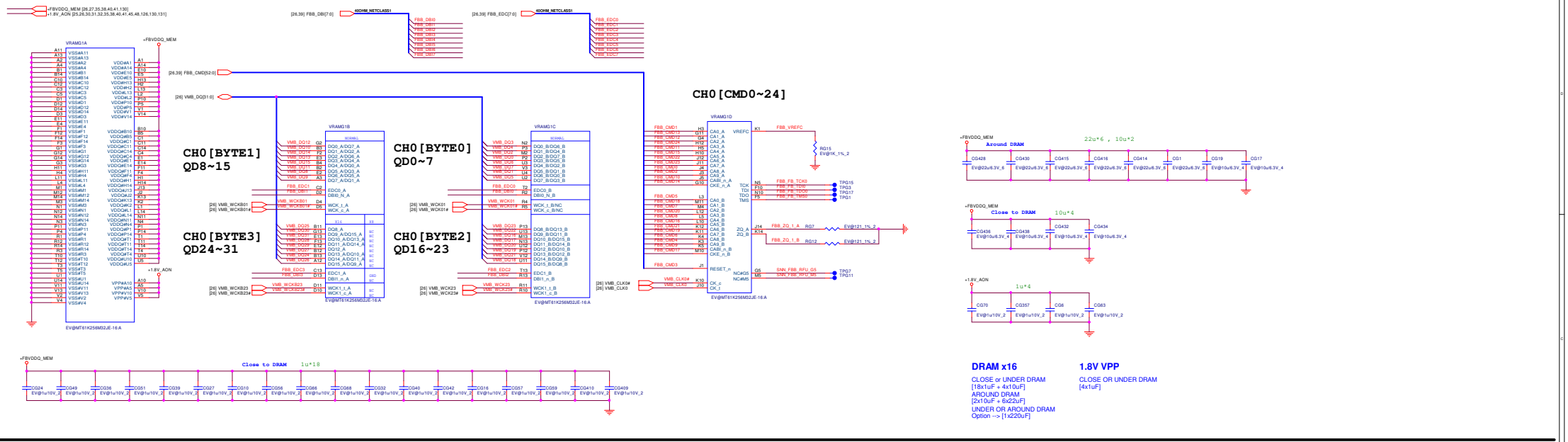
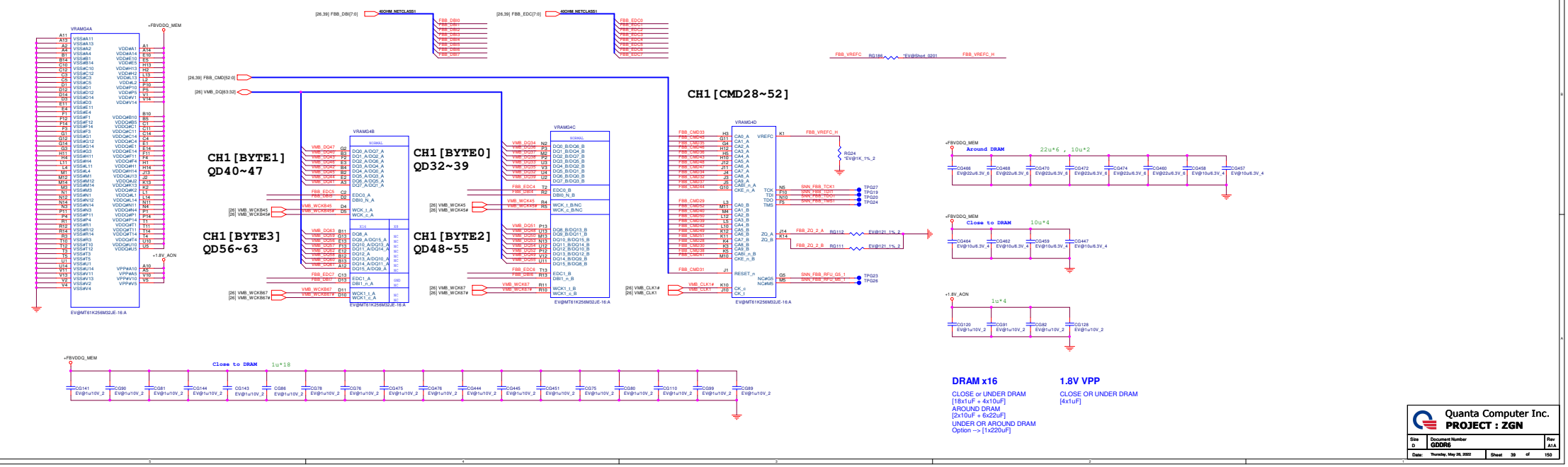
MEMORY: FBB Partition 31..0 x16 Dual Channel DRAM



MEMORY: FBB Partition 63..32 x16 Dual Channel DRAM



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D	GDDR6	A1A
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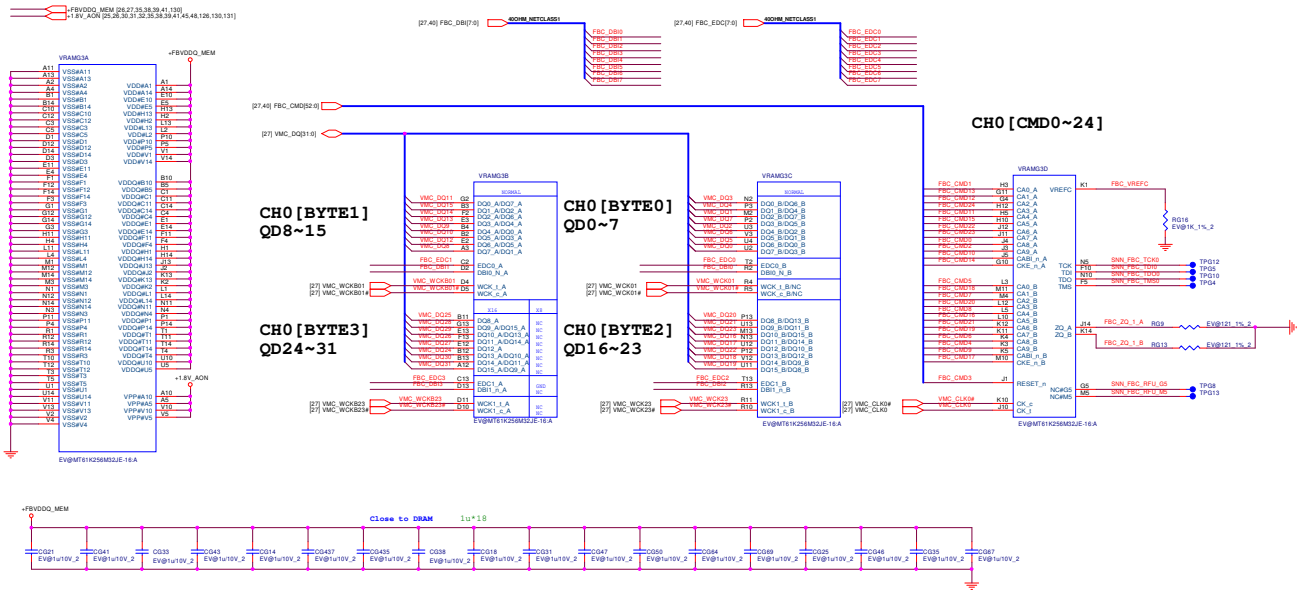
MEMORY: FBC Partition 31..0 x16 Dual Channel DRAM



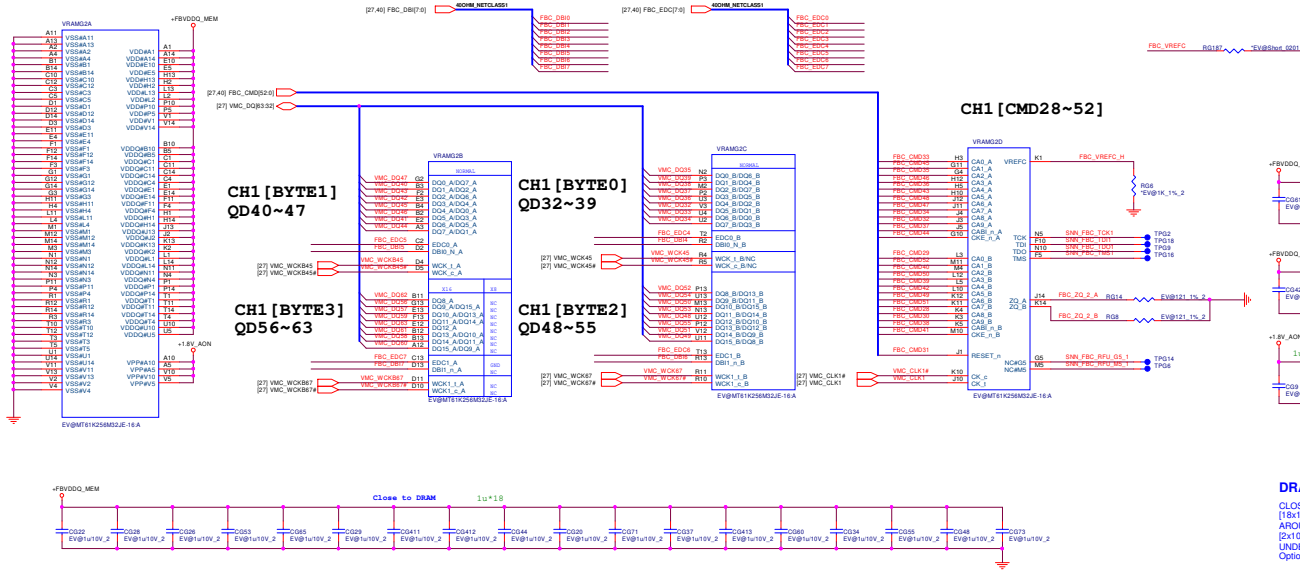
DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

MEMORY: FBC Partition 63..32 x16 Dual Channel DRAM



DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

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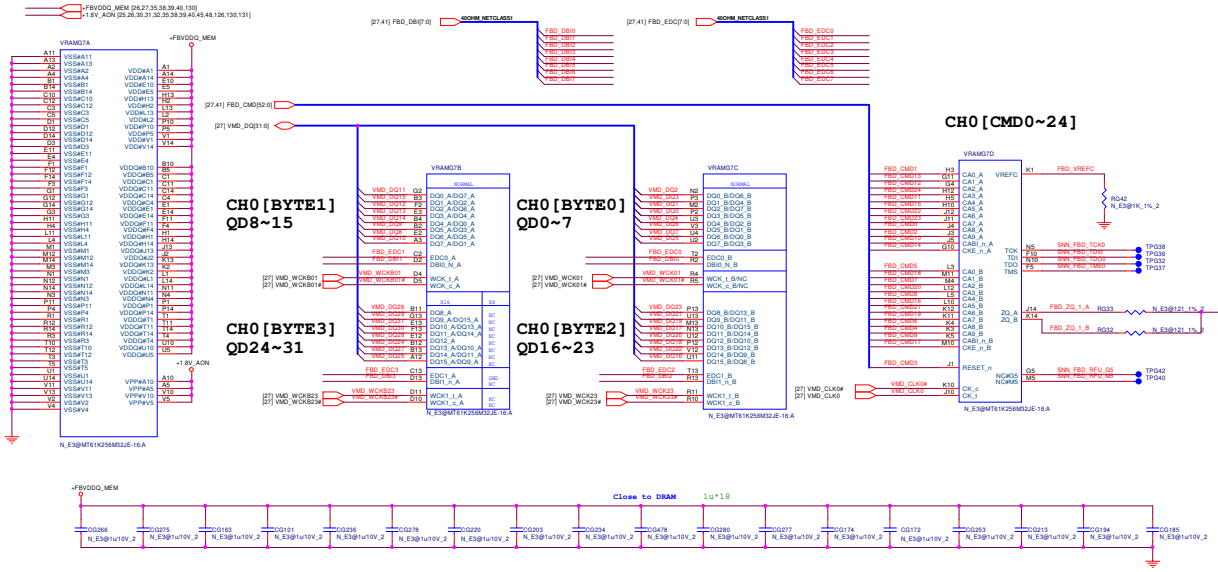
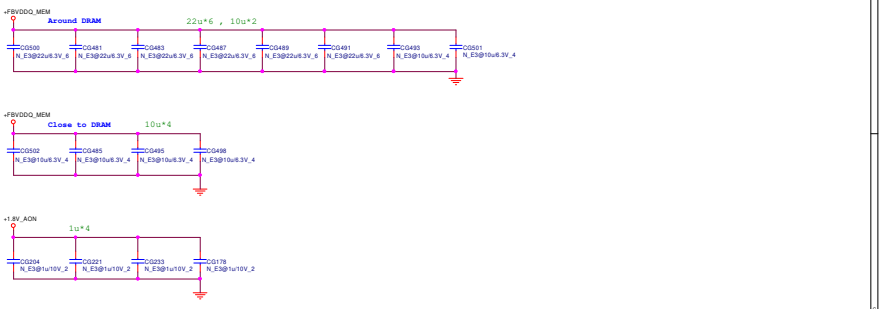
MEMORY: FBD Partition 31..0 x16 Dual Channel DRAM

Channel D is not use for GN20-E3





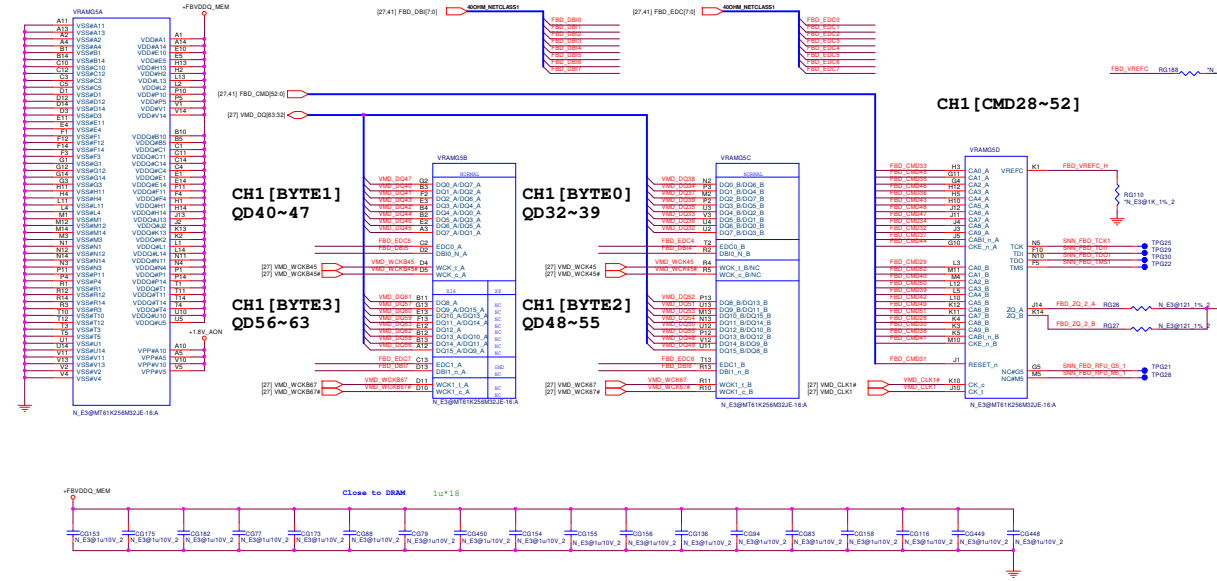
DRAM x16

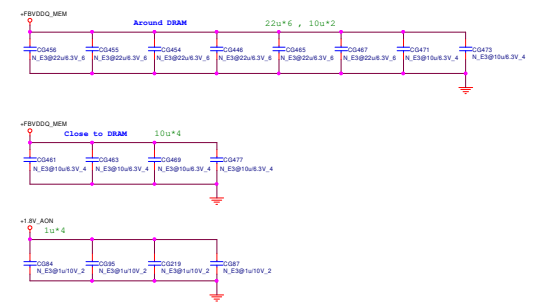
CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

MEMORY: FBD Partition 63..32 x16 Dual Channel DRAM





DRAM x16

CLOSE or UNDER DRAM
[18x1uF + 4x10uF]
AROUND DRAM
[2x10uF + 6x22uF]
UNDER OR AROUND DRAM
Option --> [1x220uF]

1.8V VPP

CLOSE OR UNDER DRAM
[4x1uF]

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MUX Control

SEL	Selected Port
1	Port A
0	Port B

0: CPU
1: GPU

Input EQ

Port A		
Value	EQ0	EQ1
3.2 dB	0	0/R
3.8 dB	0	F/1
4.7 dB	R	0/R
5.9 dB	R	F/1
7.0 dB	F	0/R
7.8 dB	F	F/1
9.0 dB	1	0/R
10.3 dB	1	F/1

Port B		
Value	EQ2	EQ1
3.2 dB	0	0/F
3.8 dB	0	R/1
4.7 dB	R	0/F
5.9 dB	R	R/1
7.0 dB	F	0/F
7.8 dB	F	R/1
9.0 dB	1	0/F
10.3 dB	1	R/1

Path Control

BSS138:BAM01380009 vendor spec

Gain and Output Swing

Gain	Swing	AFS or BFS
-3.5 dB	4.7K	0
-0.5 dB	4.7K	R
-3.5 dB	NC	F
-0.5 dB	NC	1

State	Pull-up	Pull-down
0	NC	0
R	NC	68K
F	NC	NC
1	0	NC

CPU HPD
GPU HPD

GPU PWM Level shift

1.8V

3V

PWM OUT Enable Level shift

1.8V - GPP_Sx

3V

Backlight On

!! Take care "OR gate VIH" !!

Power

PWM (Backlight)

A	INH	Out
L	L	COM=Y1
H	L	COM=Y2
x	H	None

LCDVCC

!! Take care "OR gate VIH" !!

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eDP

NV DDS support G-SYNC-DD only but NVSR

MAX 1.2A

G-SYNC NVSR

DDS/G-SYNC DD

DMIC

CCD

Take Card mini LED panel (36W/12V=3A (120mis)

Touch Screen Conn.

Touch Screen Power on eDP conn.

OLED - Power Conn.

VO1: 1.3A(52mils) / VO2: 3.6A (145mils)

OLED Panel remind
- VO1=ELVDD, VO2=ELVSS, Swire=EL_ON2 用AWG34
- 所有Power, "GND" 感受有實體cable 接出, 否則會有Abnormal display風險
- PMIC GND 用AWG34
- EL_ON3 Connect system GPIO(1.8V), like BL_EN and detail timing will release after kick off .
- 需用Coaxial線

AES Stylus

20 mils

Panel OD control

1.8V

LCDVCC

2.5A / 100mils

Touch Screen Power

Backlight

CCD PWR

MIC PWR

DMIC Level Shift (PCH)

DMIC Voltage must be 1.8V

HALL Sensor

DB GMR/HALL Sensor

Remove 1pcs before measure

045

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Size	Document Number	Rev
A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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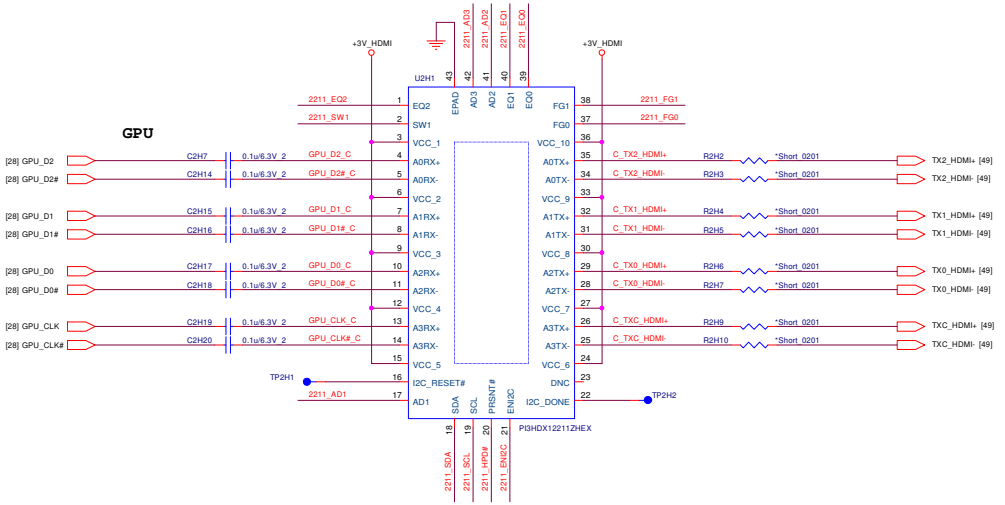
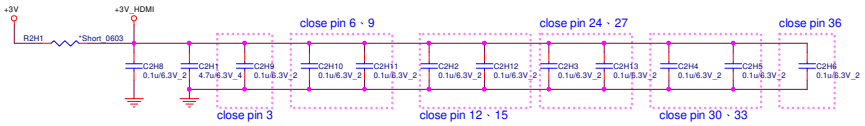
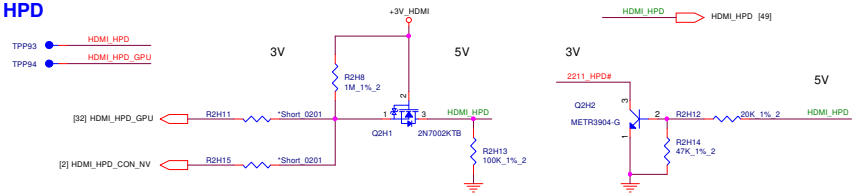
HDMI 2.1 ReDriver(HDM)



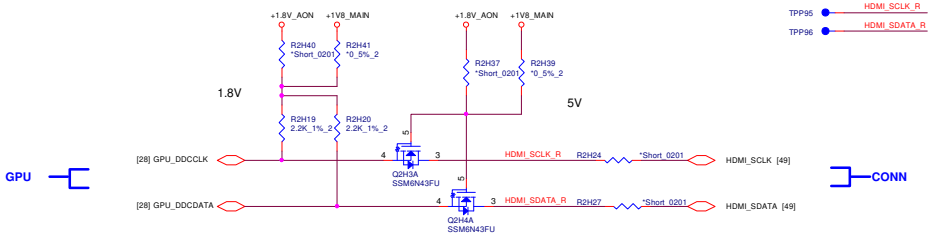
POWER



HPD



DDC

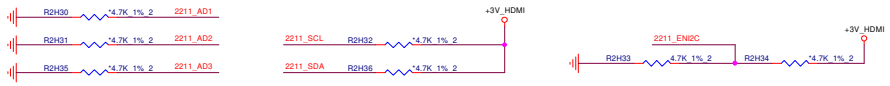


EQ2	EQ1	EQ0	Input EQ at 12Gbps
0	0	0	6.8dB
0	0	1	7.8dB
0	1	0	9.2dB
0	1	1	10.7dB
1	0	0	12.2dB
1	0	1	13.4dB
1	1	0	14.8dB
1	1	1	16.4dB

FG1	FG0	Output Pre-emphassis
0	0	-3.5dB
0	1	-2dB
1	0	-0.5dB
1	1	1.5dB

SW1	Output Pre-emphassis Swing
0	1000mV
1	1200mV

Reserve for I2C mode



0: GPIO Mode <--- Default
1: I2C Mode
NC: EEPROM

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Custom	HDMI Re-Driver(PI3HDX12211ZHEX)	A1A
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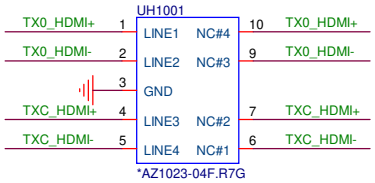
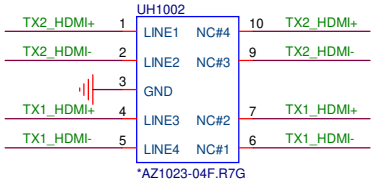
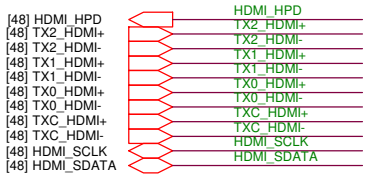
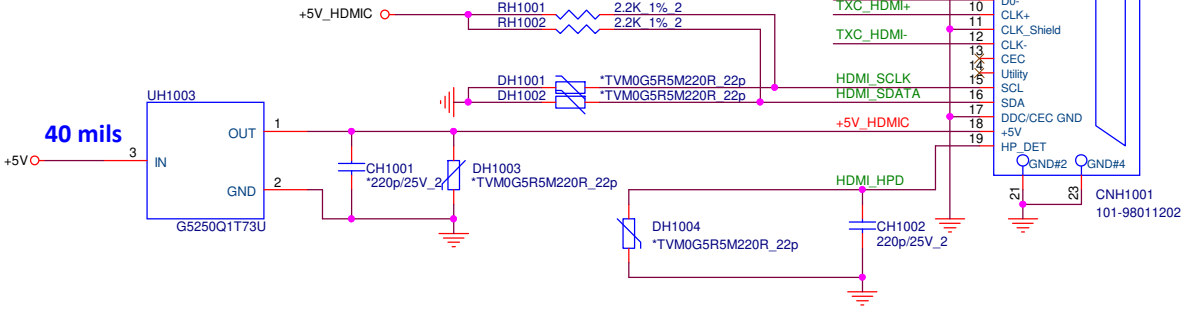
For ESD

Layout note:Place close to HDMI Conn









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Custom	**HDMI CONN**	A1A
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A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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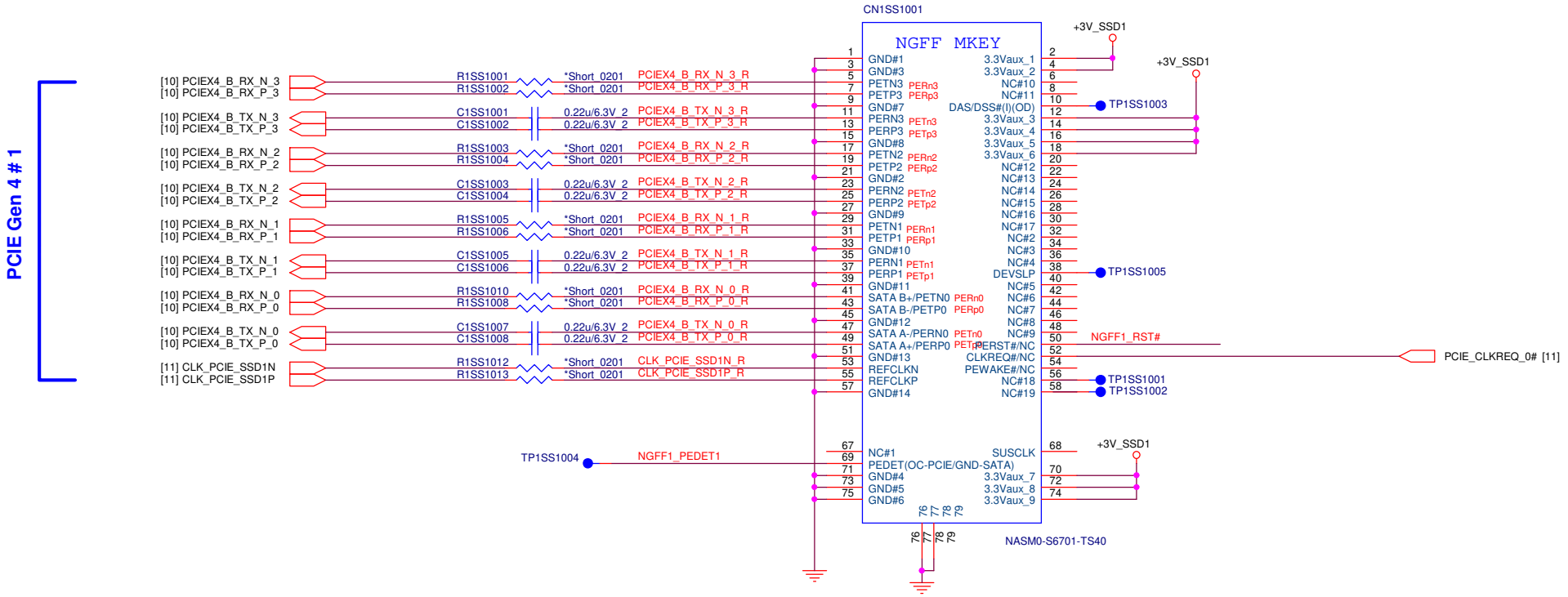
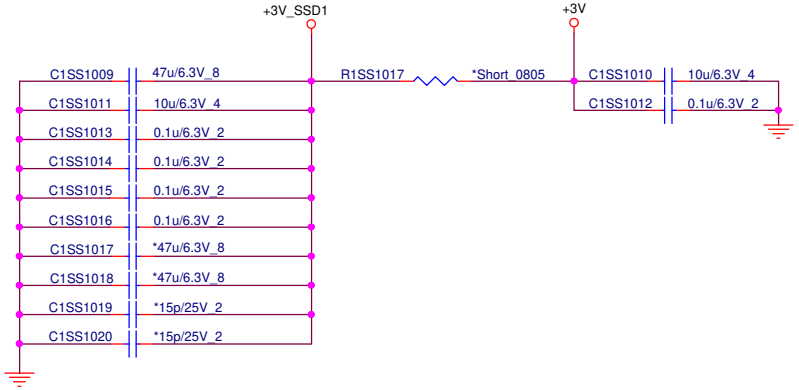
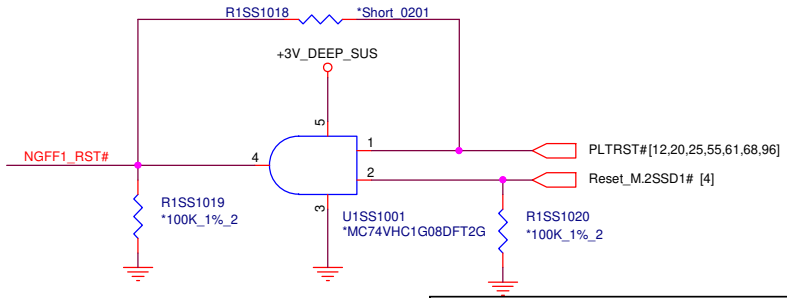
NGFF_M.2 SSD #1 (NGF)

PCIE 1X4 LR /SATA



DECOUPLING





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B	NGFF SSD #1 / PCIE/STAT	A1A
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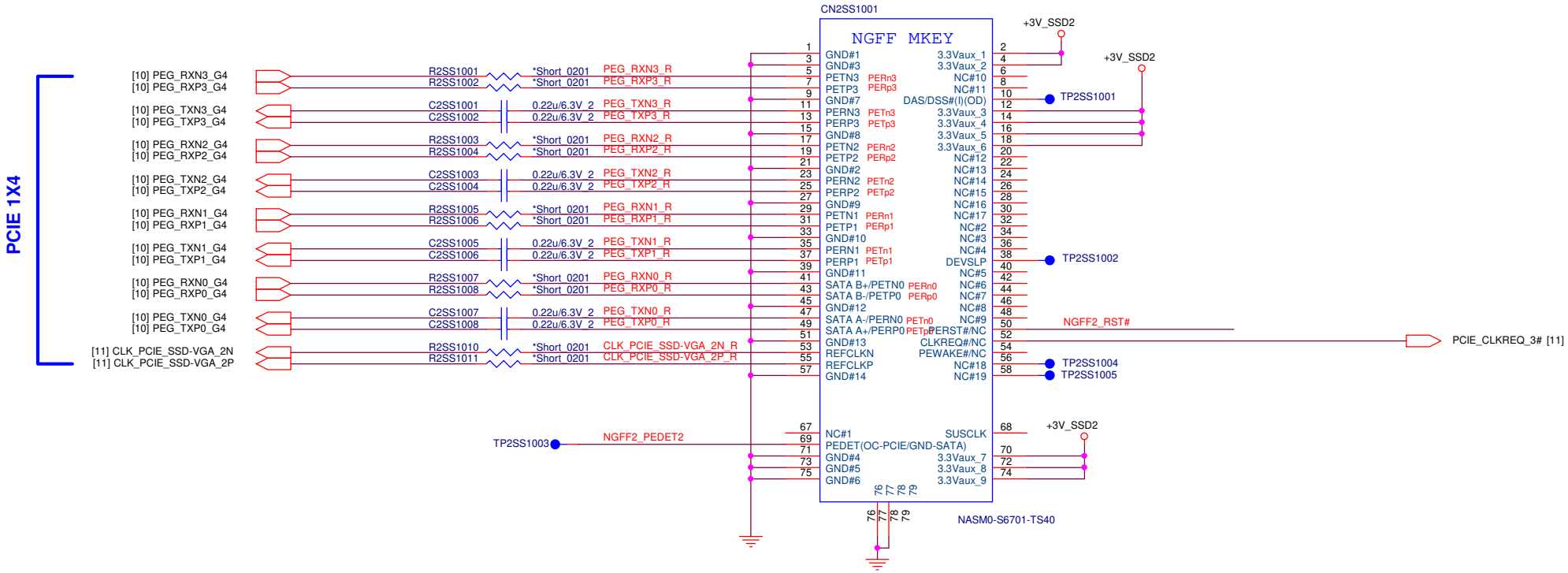
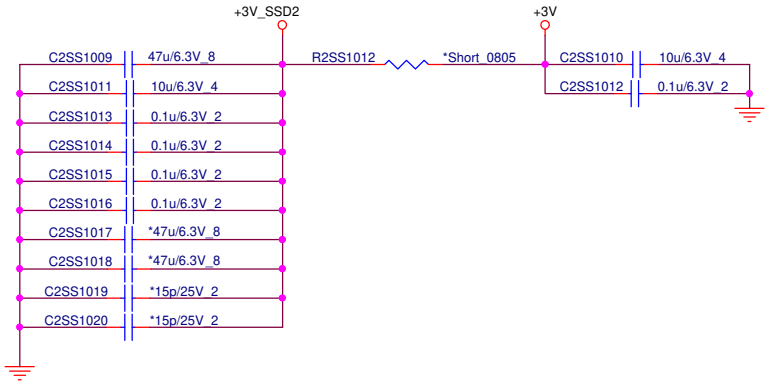
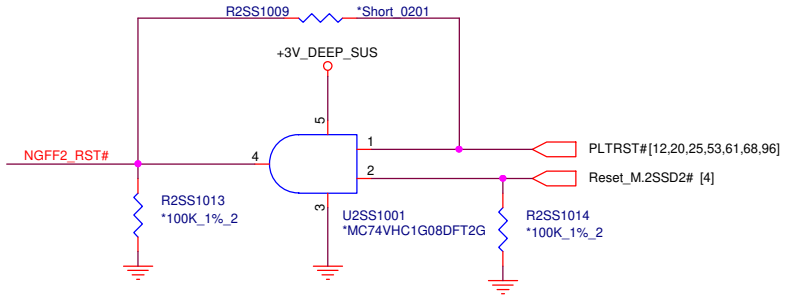
NGFF_M.2 SSD #2 (NGF)



DECOUPLING





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B	NGFF SSD #2 /PCIE	A1A
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NGFF_M.2 WiFi & BT (NGF)

E-Key

CN1FW1001
NASE0-S6701-TSH4

NGFF EKEY

BT
CNVi RX
DISCRETE WIFI
CNVi TX

PU/PD

LEVEL SHIFT

POWER SWITCH

Wake

By Control

S0

S5

WLANPWR# --> RSMRST#

M.S. for Dis. module only

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A	**LTE DB**	A1A

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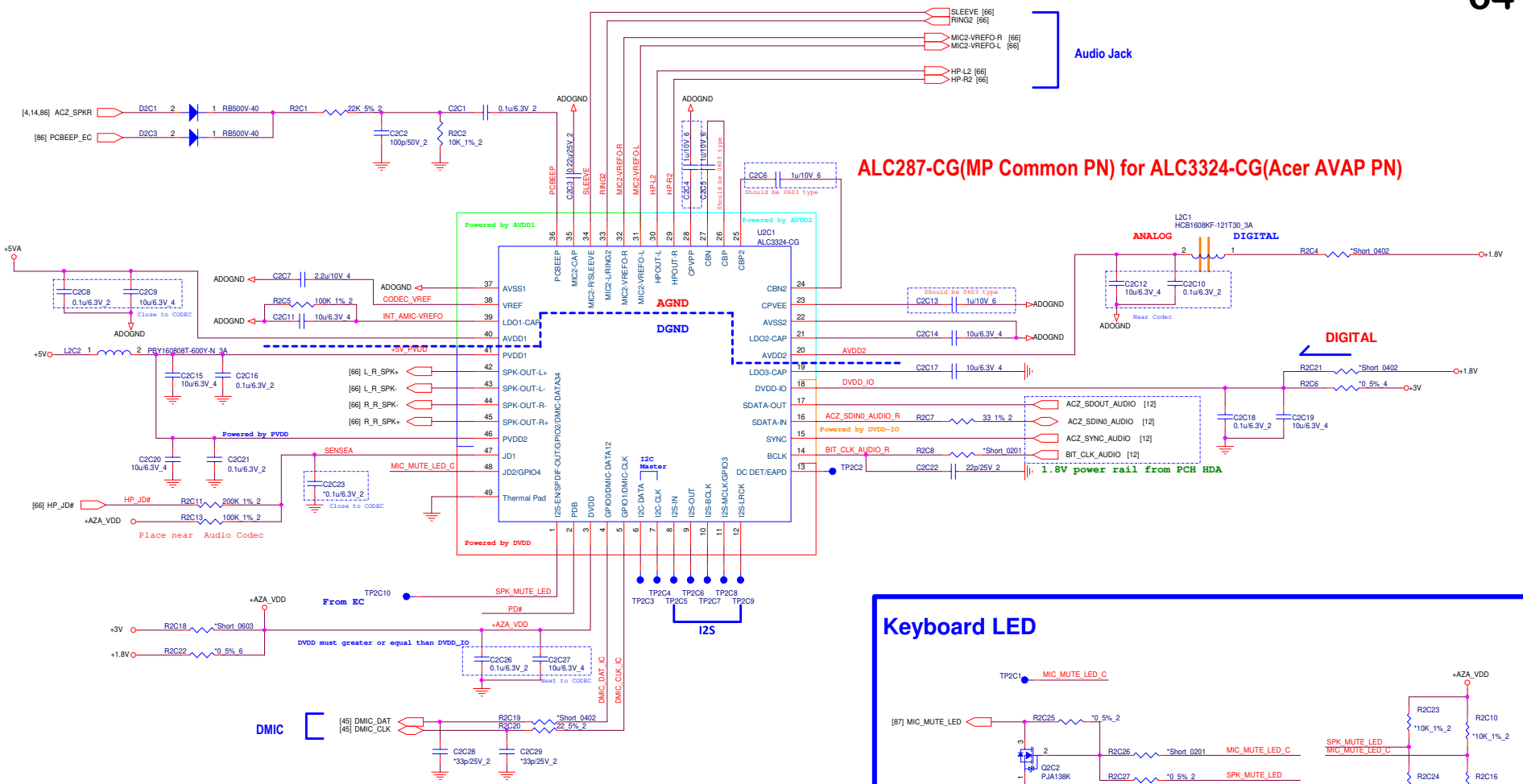
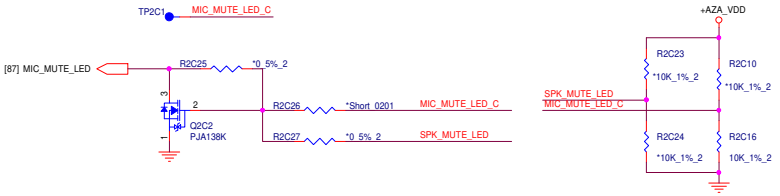
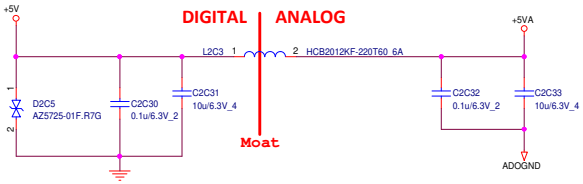
Codec ALC3324 (ADO)



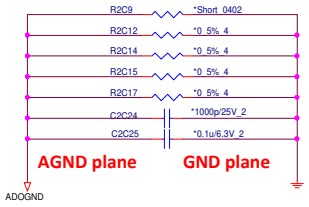
Keyboard LED



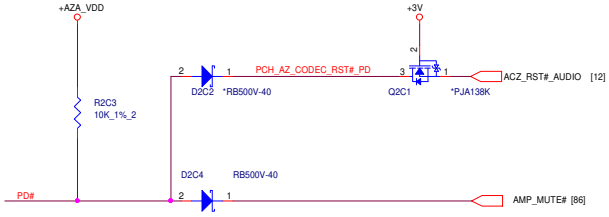
Codec PWR 5V(ADO)



GROUND MOAT



Mute(ADO)



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C	Azalia ALC295M	A1A
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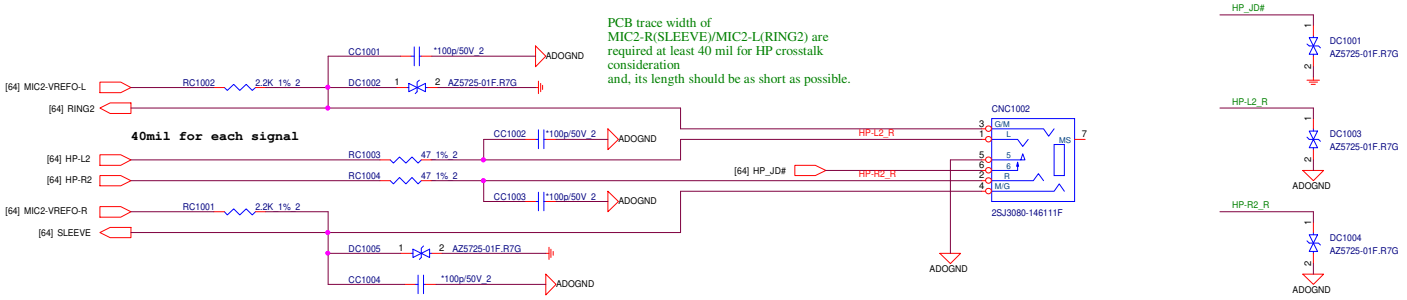
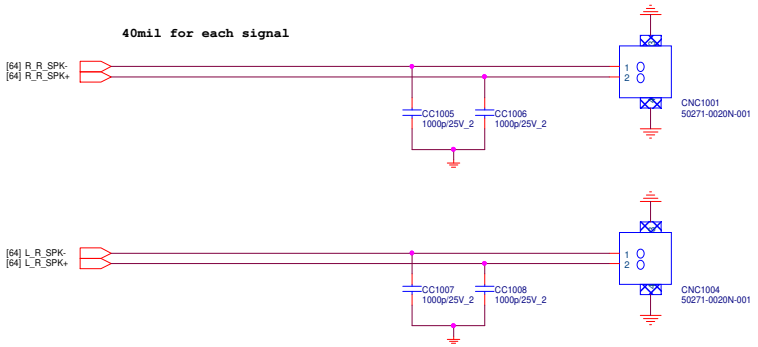
Universal Audio Jack (ADO)





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Size	Document Number	Rev
C	Audio Codec/HP/SPK	A1A
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A	**LTE DB**	A1A

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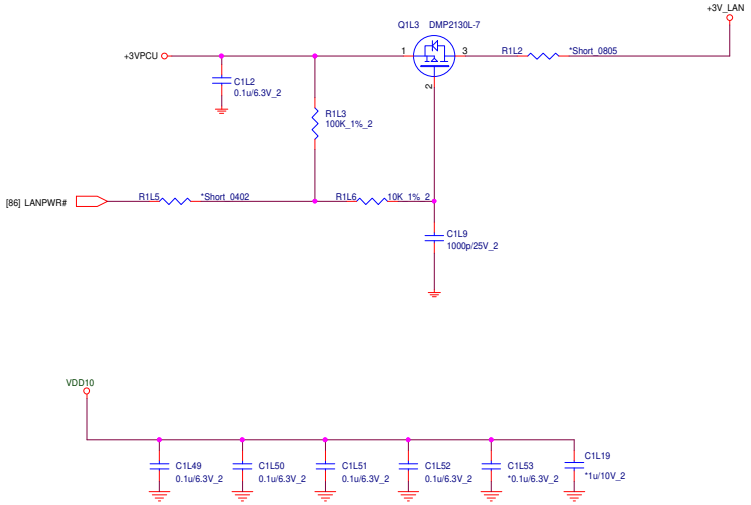
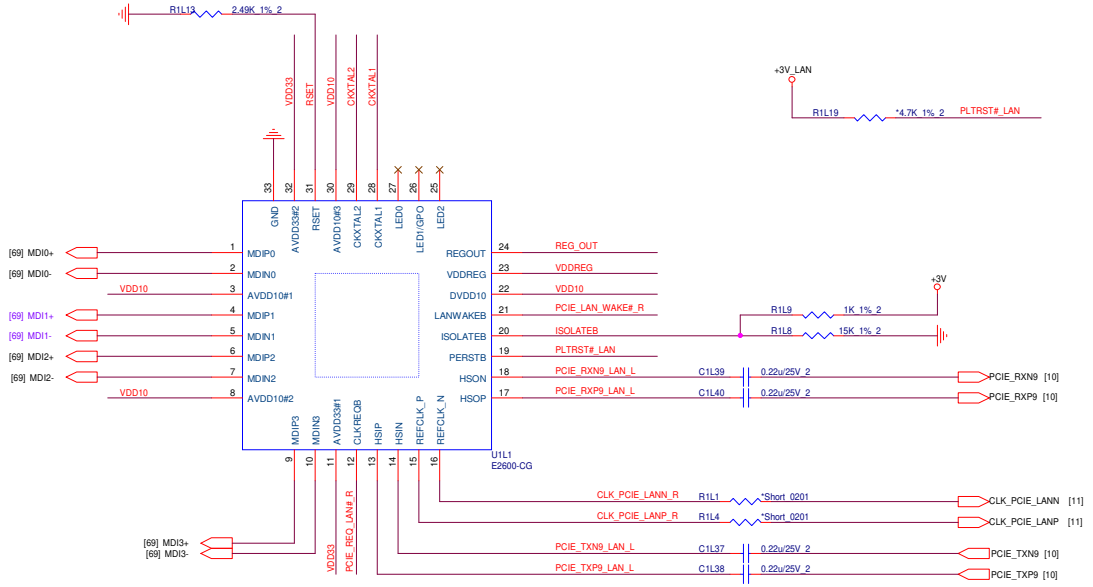
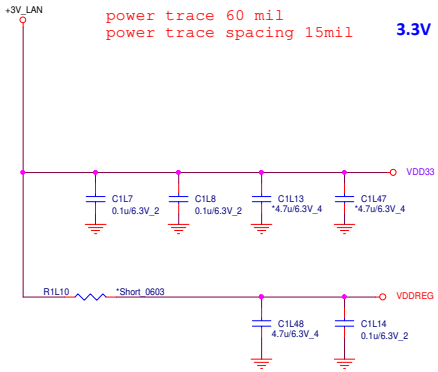
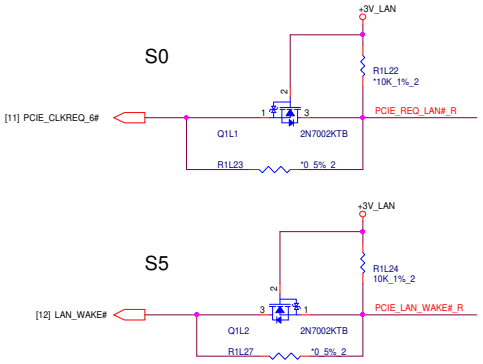
E2600-CG (LAN)

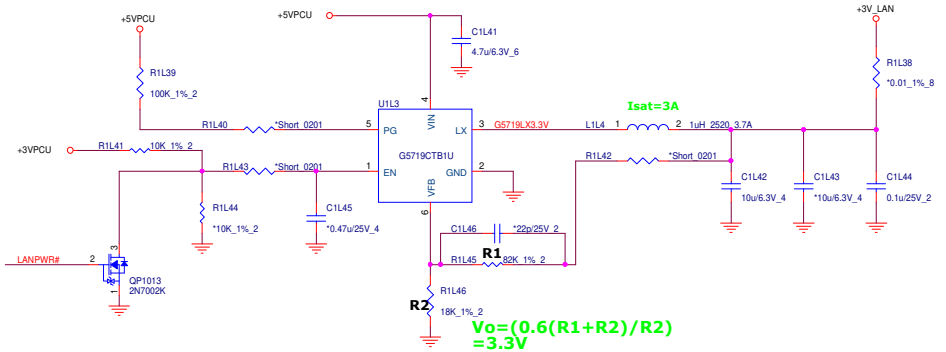


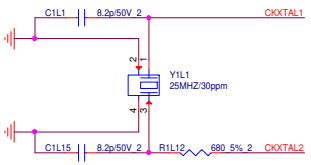




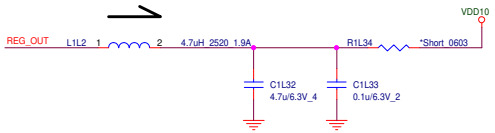
Backdrive protection (PMC)







SWR (E2600-CG SWR mode)



PLTRST#

D3 Hot - ALDPS only

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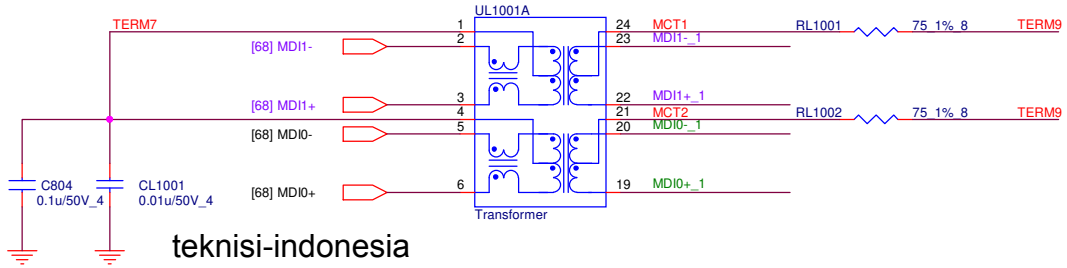
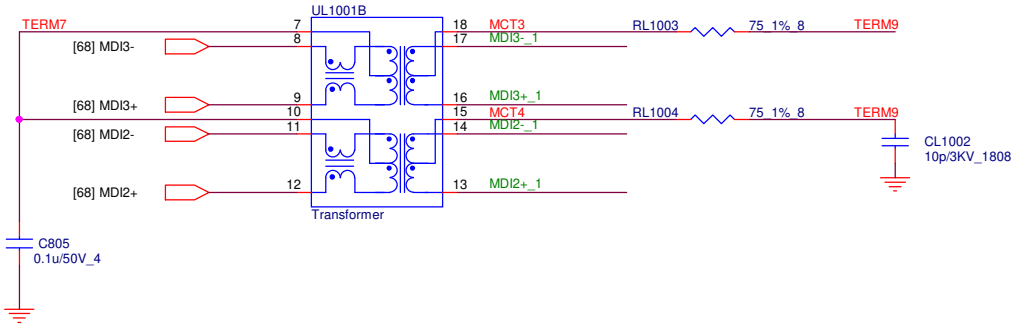
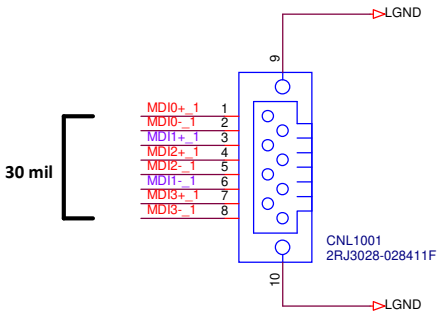
Tramsformer

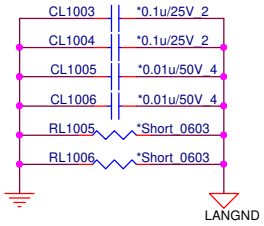


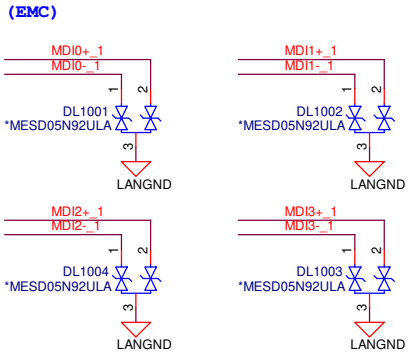
teknisi-indonesia



RJ45 Connector







Distance between DGND & LGND should have at least 60 mils

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B	**LAN Power**	A1A
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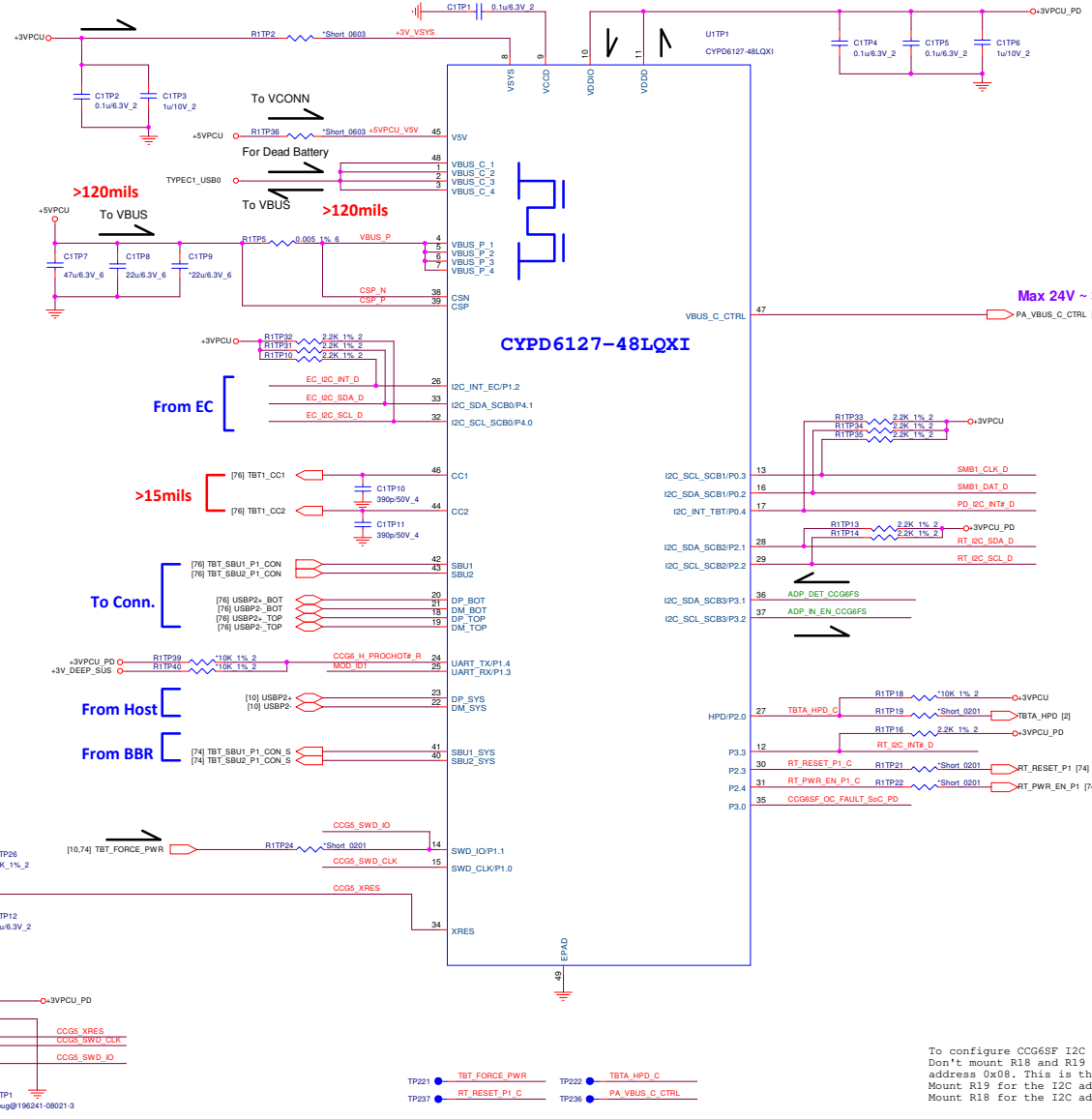
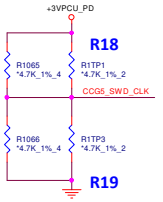
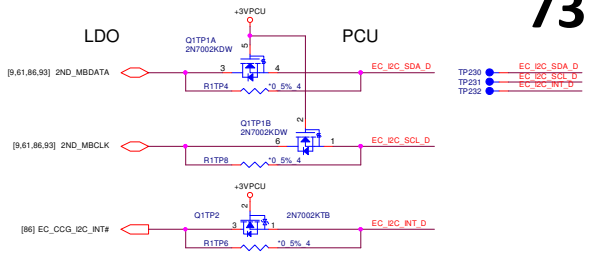
CYPD6127-48LQXI (CCG6SF)



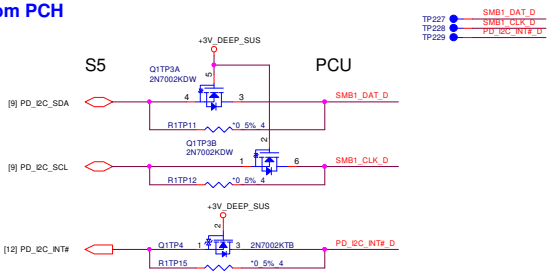
To configure CCG6SF I2C address
Don't mount R18 and R19 for the I2C address 0x08. This is the default one.
Mount R19 for the I2C address 0x40.
Mount R18 for the I2C address 0x42.



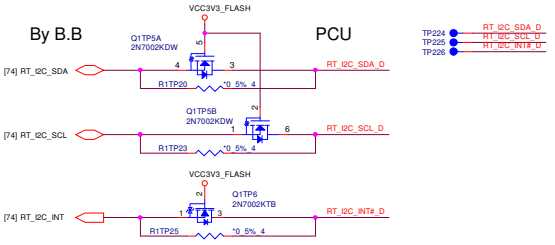
TO EC



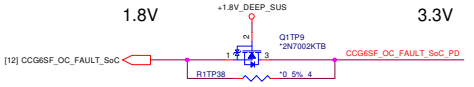
From PCH



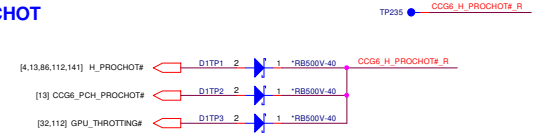
TO BBR

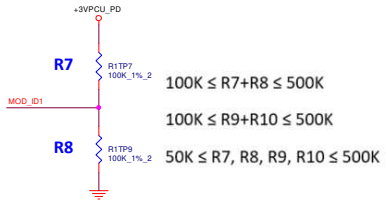


OCP



PROCHOT





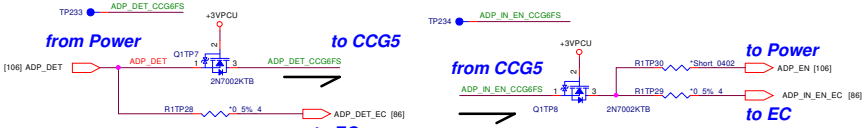
Please make sure to choose these resistors (R7, R8, R9 and R10) based on the above guidelines

	Platform ID		CCG6SF Single Port			
	MOD_ID1	MOD_ID2	Description (Dual port)		R7	R8
Notebooks	L8	NA	Reserved	L8 = VDDD	0	100K
	L7	NA	Reserved	L7 = 7* VDDD/8	56K	392K
	L6	NA	Reserved	L6 = 6* VDDD/8	110K	330K
	L5	NA	Reserved	L5 = 5* VDDD/8	76.8K	127K
	L4	NA	TBT4 with B.B*1	L4 = 4* VDDD/8	100K(CS41001FE08)	100K(CS41001FE08)
	L3	NA	Reserved	L3 = 3* VDDD/8	127K	76.8K
	L2	NA	Reserved	L2 = 2* VDDD/8	330K	110K
	L1	NA	Reserved	L1 = VDDD/8	392K	56K
	L0	NA	Reserved	L0 = 0V	100K	0

Adapter

ADP Insert	ADP_DET
Y	Low
N	Hi

ADP_EN	ADP Switch
Hi	ON
Low	OFF



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Custom	073 -- Cypress CCG6SF	A1A
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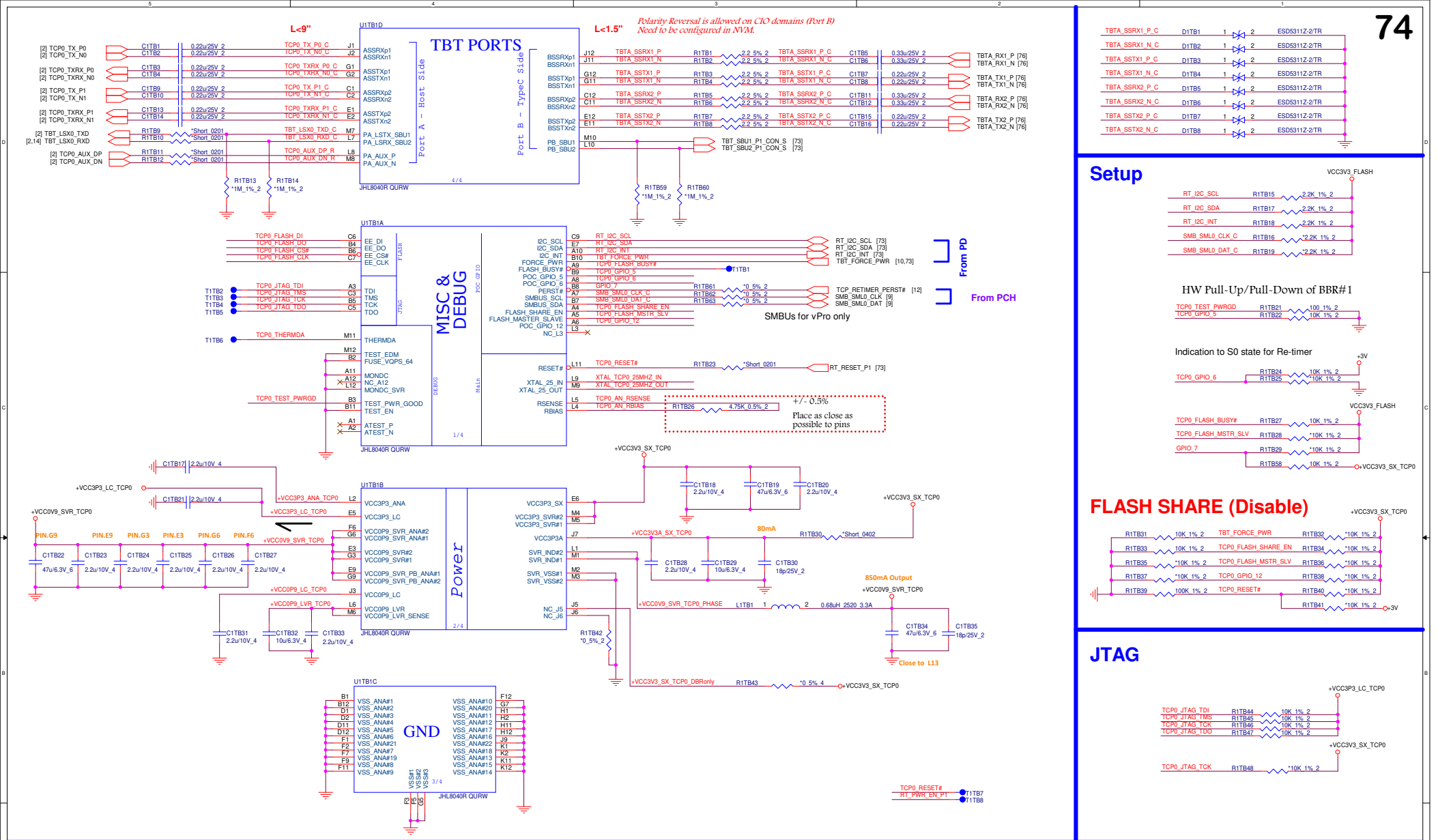
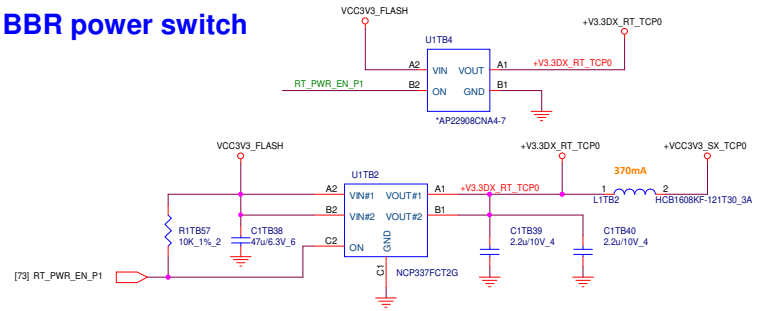


Setup

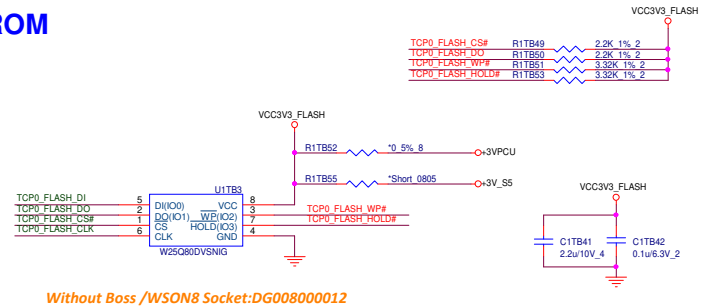
FLASH SHARE (Disable)

JTAG

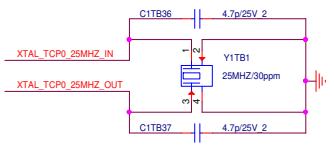
BBR power switch



ROM



Crystal



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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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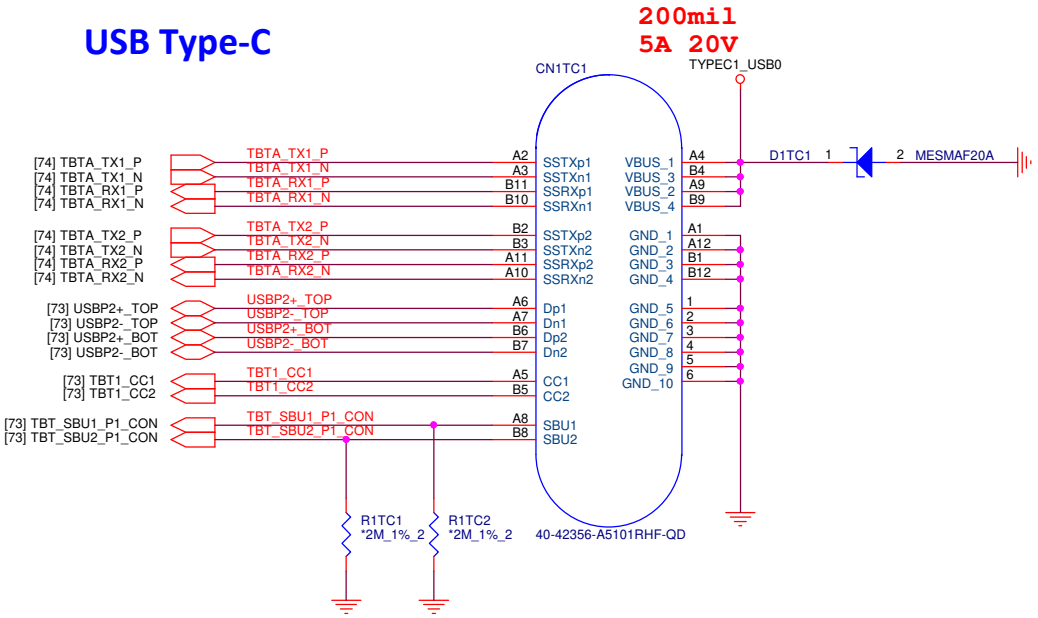
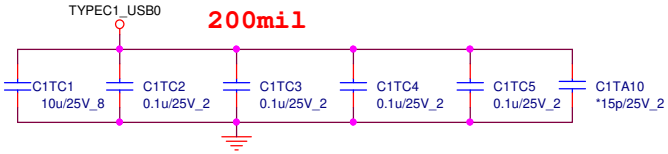
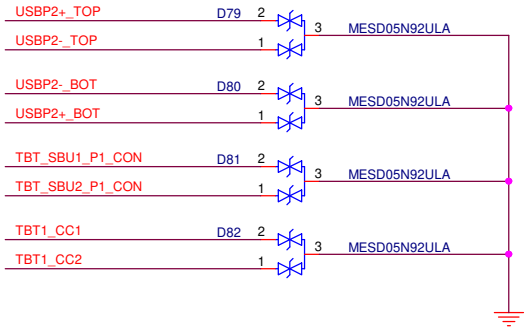
USB Type-C

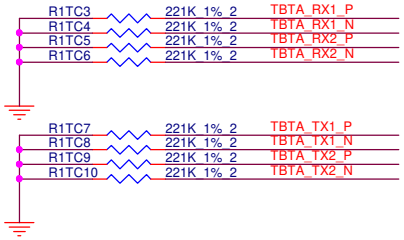


Power Capacitance



ESD





Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	**USB Type C #1**	A1A
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Quanta Computer Inc.

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Size	Document Number	Rev
A	**LTE DB**	A1A

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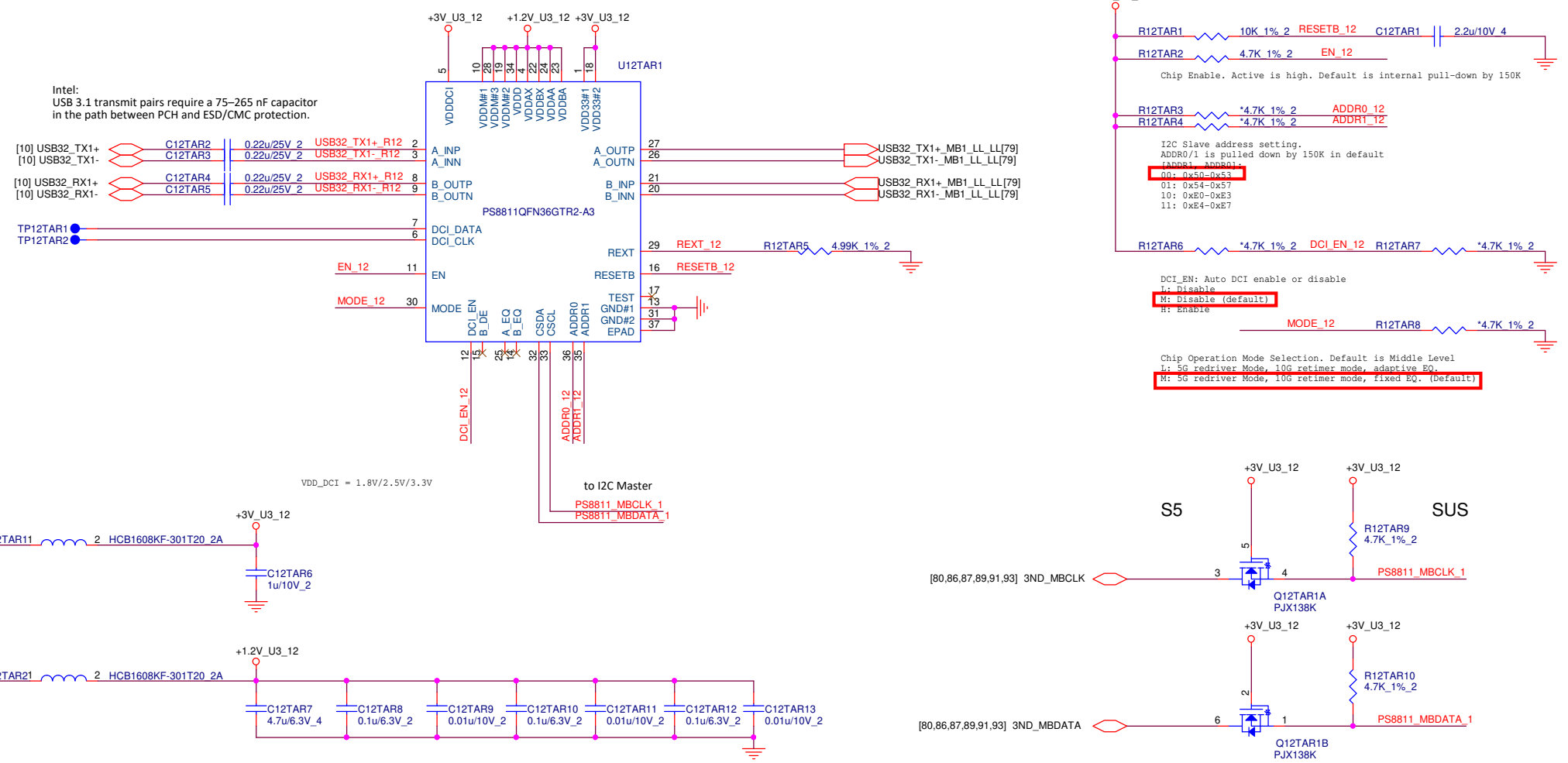
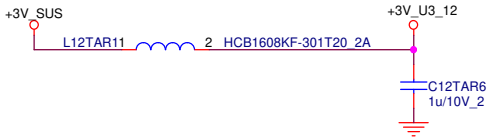
USB Type A #1 - Re-driver





Decoupling caps need be placed as close to power pins as possible.
1.2 V power ripple requirement: < 30 mV

Quanta Computer Inc.
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Size	Document Number	Rev
B	TypeA1-PS8811QFN36GTR2	A1A
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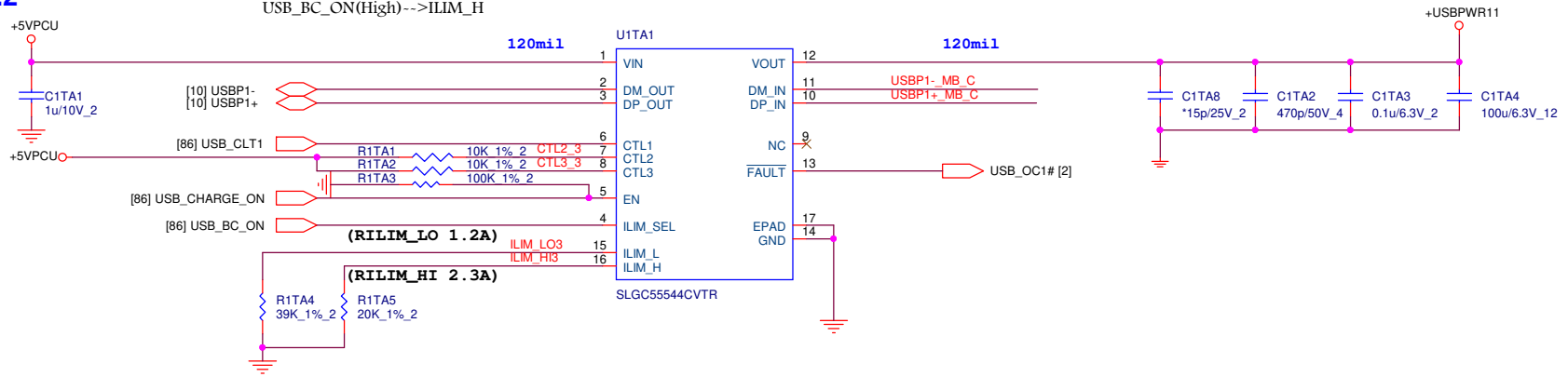
USB Charger (UBC)_BC 1.2

Part Number	Description
AL002544001	TPS2544RTER
AL055544001	SLGC55544CVTR

USB_BC_ON(Low)-->ILIM_L
USB_BC_ON(High)-->ILIM_H

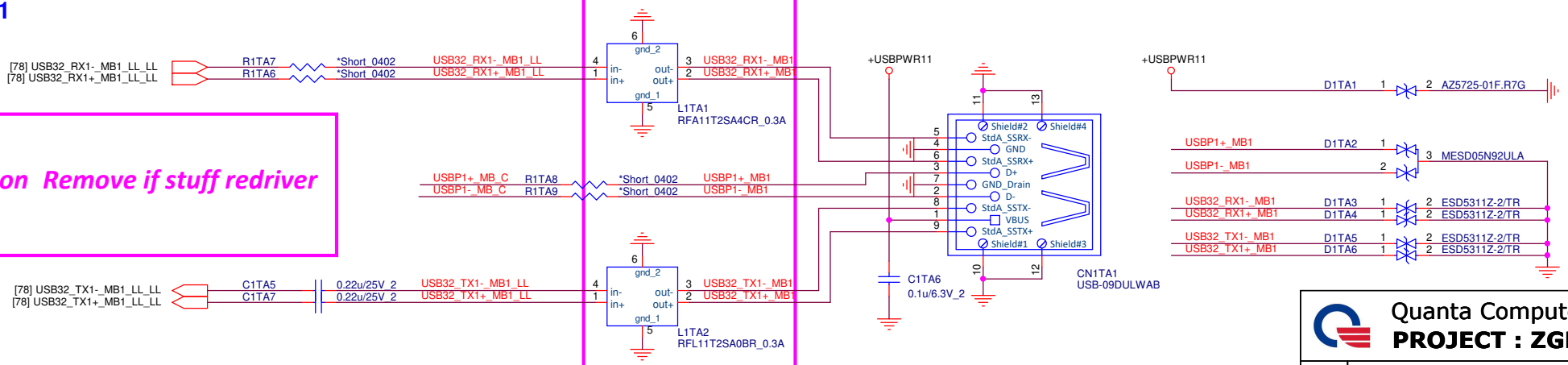


USB Power

TypeA#1

Option
Check RF Level2 SPEC and remove, short directly

Option Remove if stuff redriver



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
B	TypeA1-CONN/BC1.2	A1A
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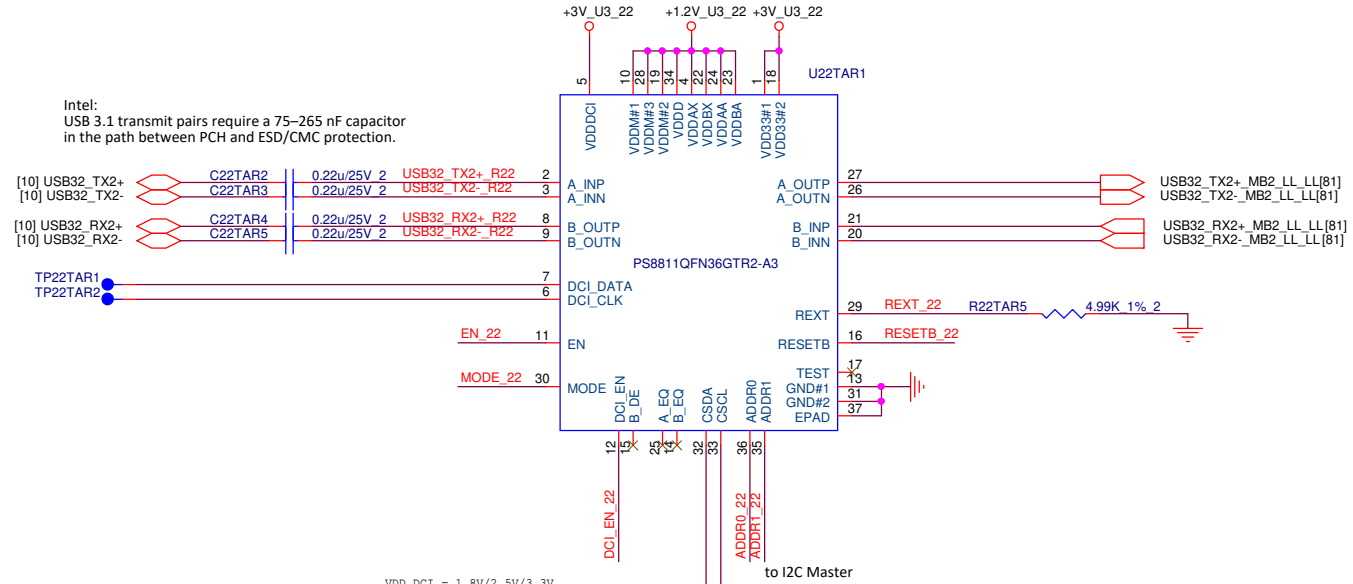
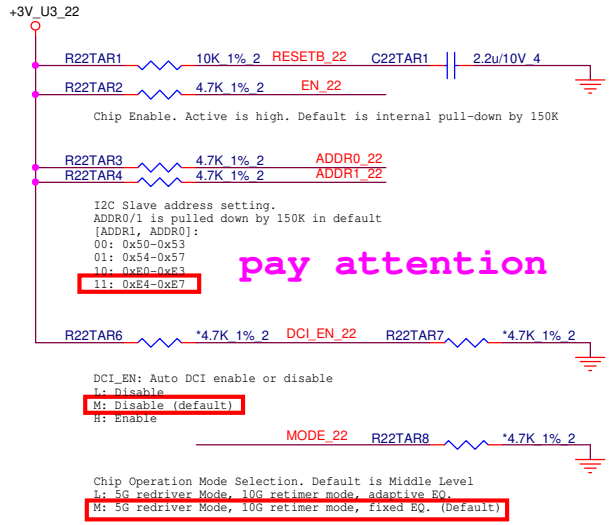
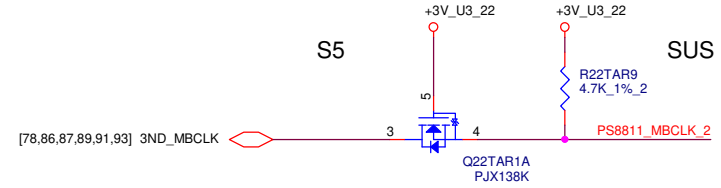
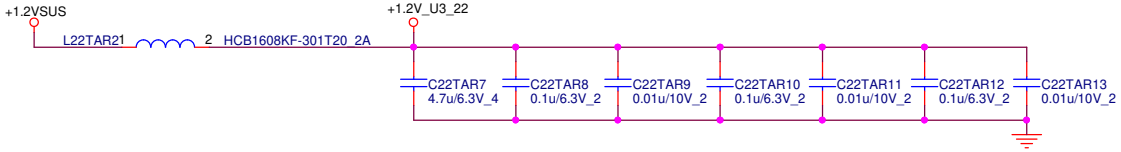
USB Type A #2 - Re-driver









Decoupling caps need be placed as close to power pins as possible.
1.2 V power ripple requirement: < 30 mV

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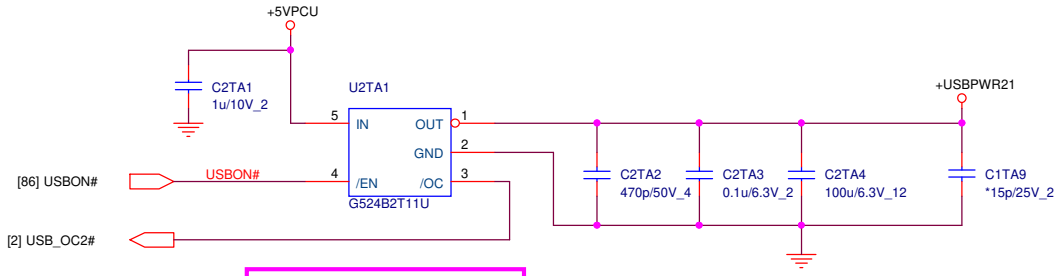
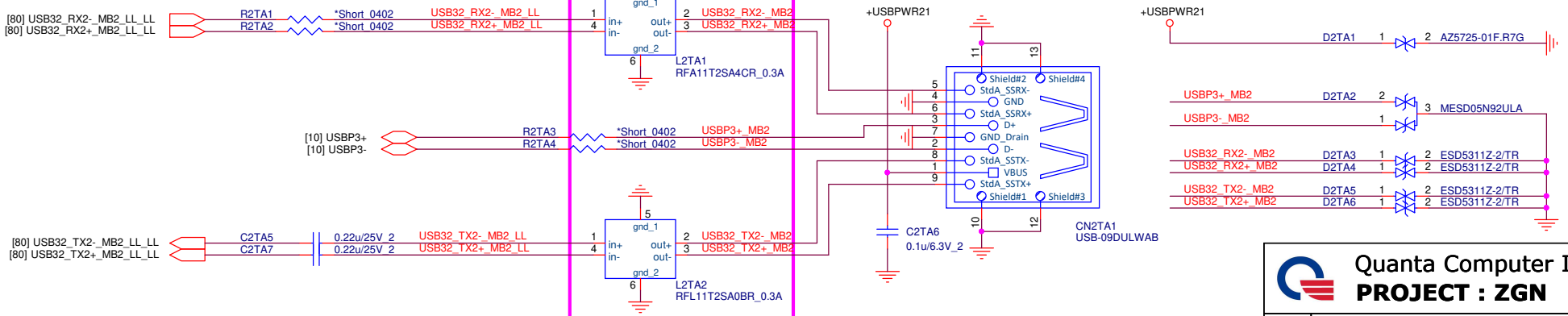
USB Charger (UBC)_BC 1.2

USB Power



TypeA#2

Option
Check RF Level2 SPEC and remove, short directly



Quanta Computer Inc.
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B	TypeA2-CONN	A1A
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Quanta Computer Inc.

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Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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Quanta Computer Inc.

PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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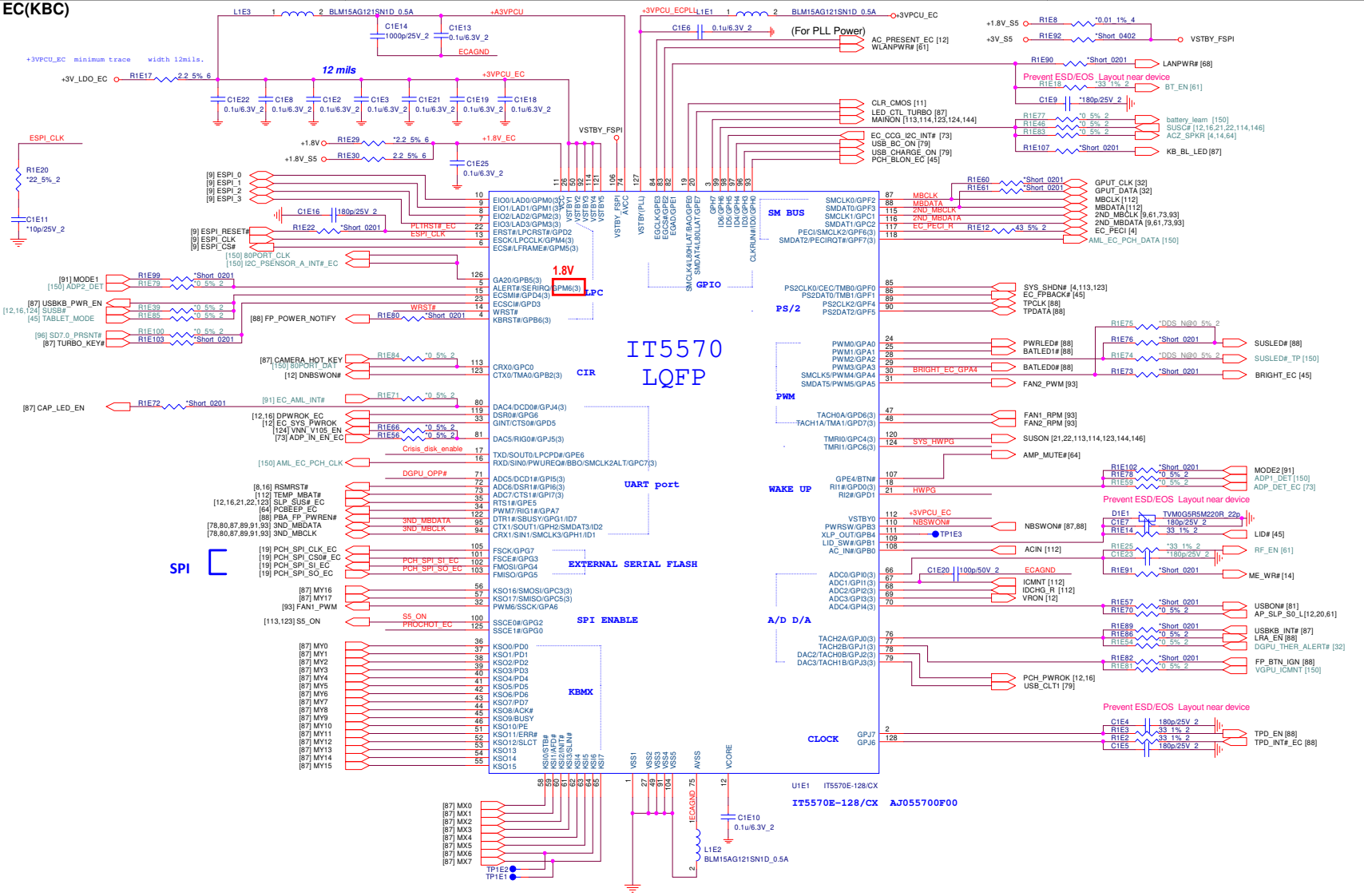
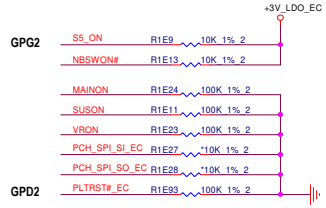
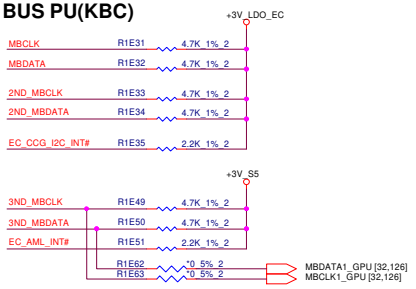
EC(KBC)



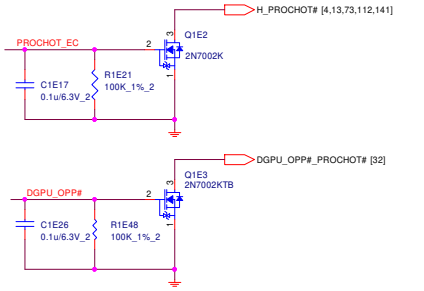
GPG2 / GPD2



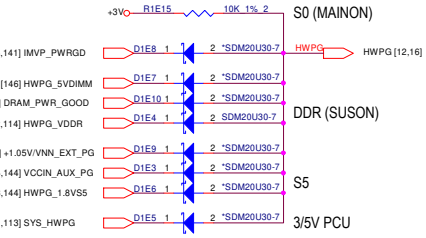
SM BUS PU(KBC)



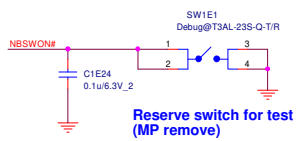
PROHOT#



HWPG(KBC)



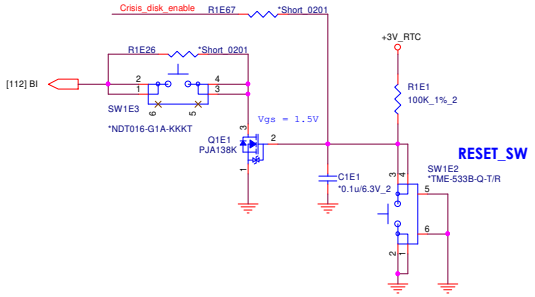
Reserve switch for test (MP remove)



Reserve switch for test (MP remove)

recommad use same as SW2 shortage problem

Reset SW (FSW)



SMBUS	
SM Bus 0	Battery/GPU
SM Bus 1	Debug Card/ PD/ Thermal Sensor (Local:CPU;Remote Panel)
SM Bus 2	N/A
SM Bus 3	U3 Re-driver1/ U3 Re-drivr2/ LED Driver/ Ambient Light Sensor/ Thermal Sensor (Local:GPU;Remote DDR5)

Quanta Computer Inc.
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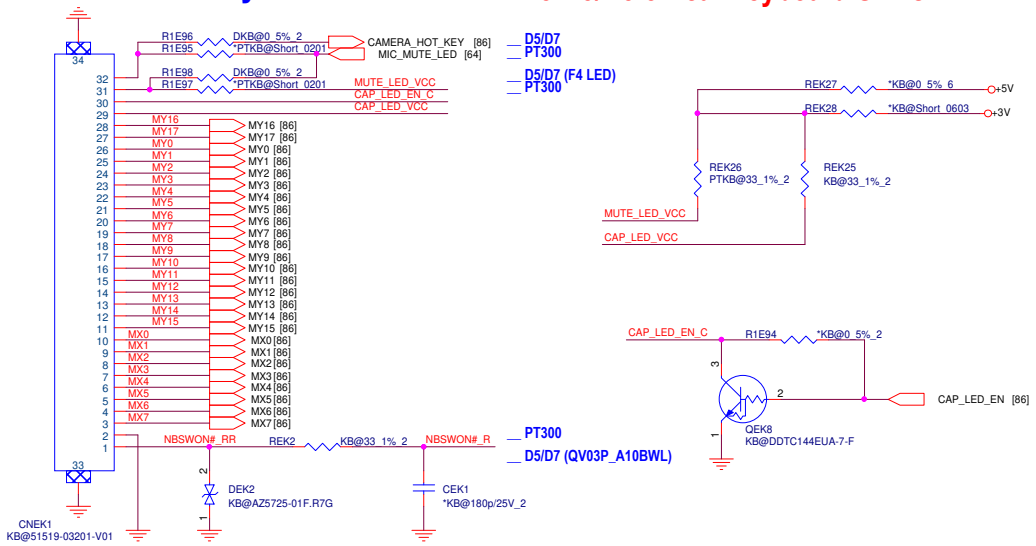
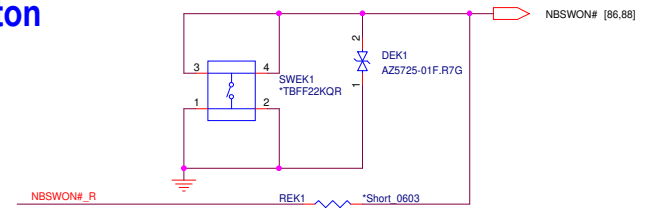
Tranditional keybord

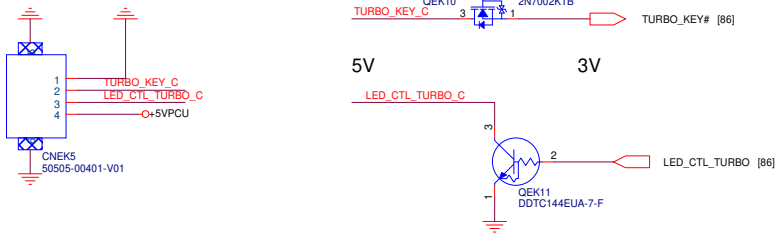
No D5/D5 offical Keyboard SPEC



Power Button

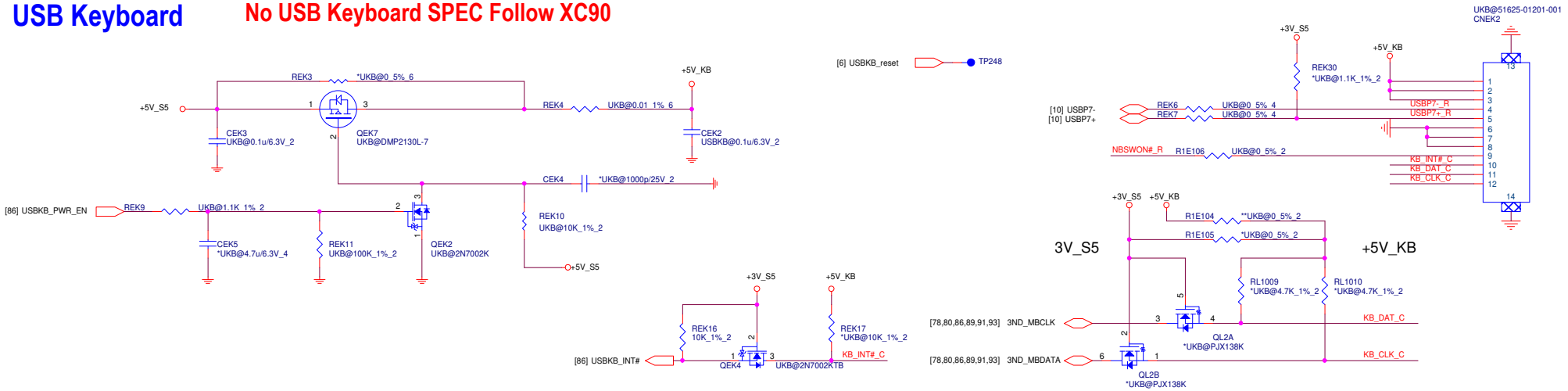


Turbo Button

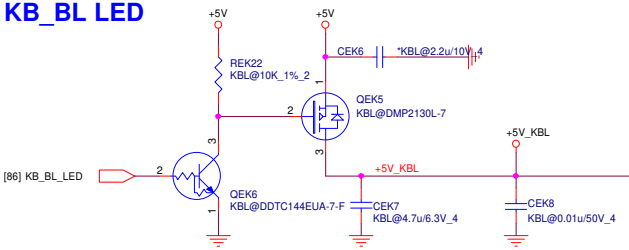


USB Keyboard

No USB Keyboard SPEC Follow XC90

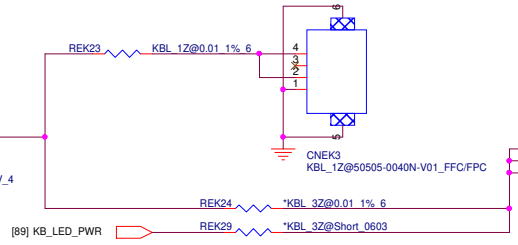


KB_BL LED

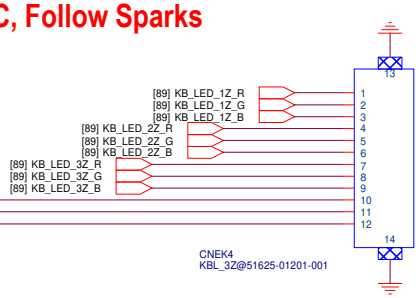


Single Color (D5/D7)

No Backlight SPEC, Follow Sparks



3-Zone RGB (PT300)



1.5A (60mils)

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Custom	TP/KB/Light Bar	A1A
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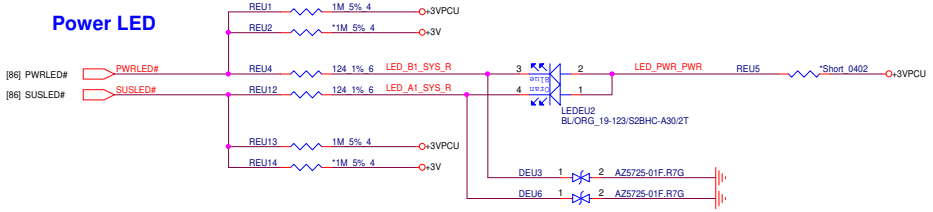
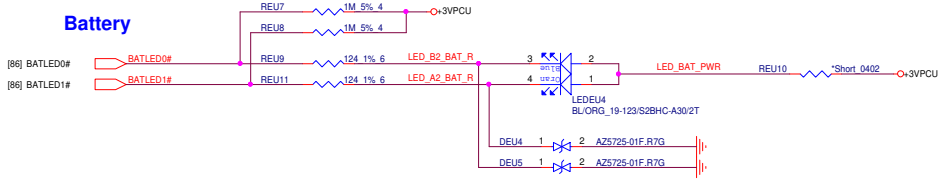
UIF

Power LED

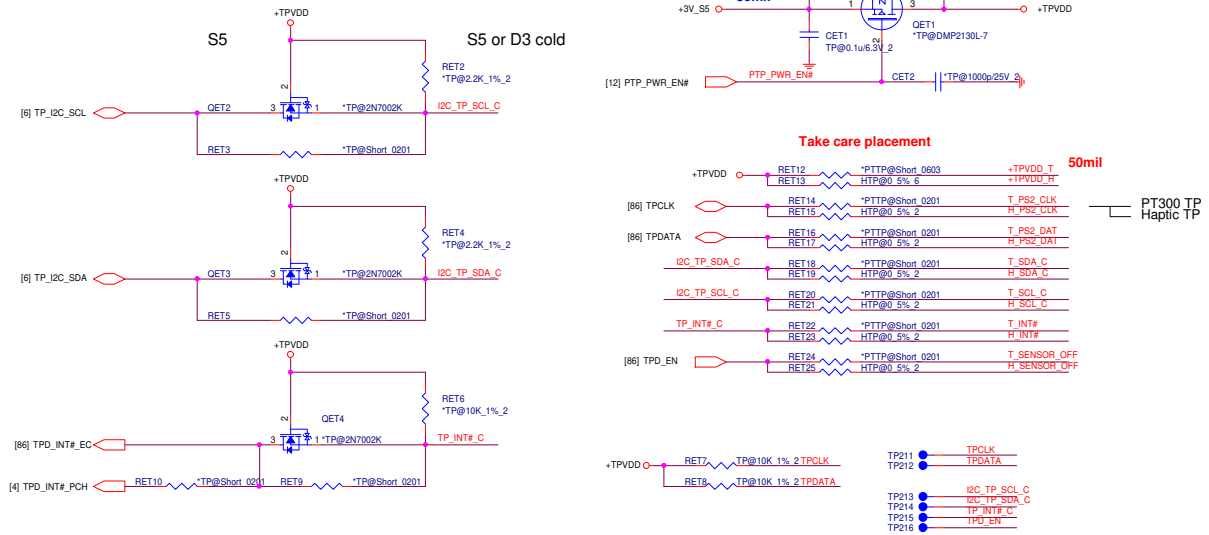


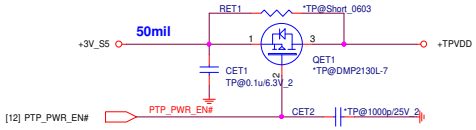
Battery



Touch Pad

Cannot wake once D3 Cold implement

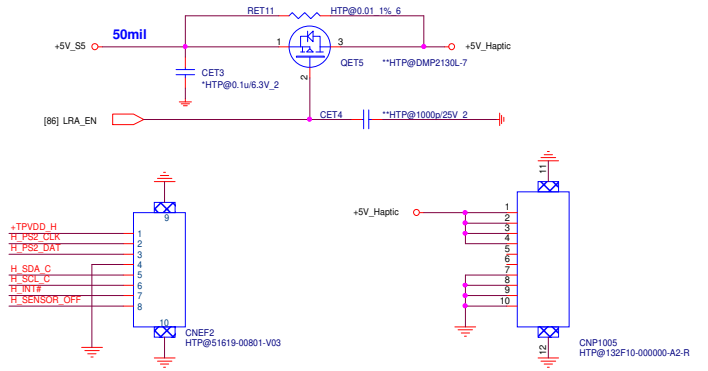




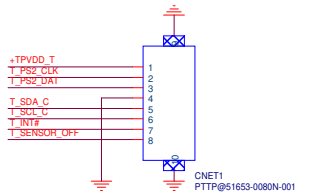
Take care placement

Haptic TouchPAD (D5/D7)

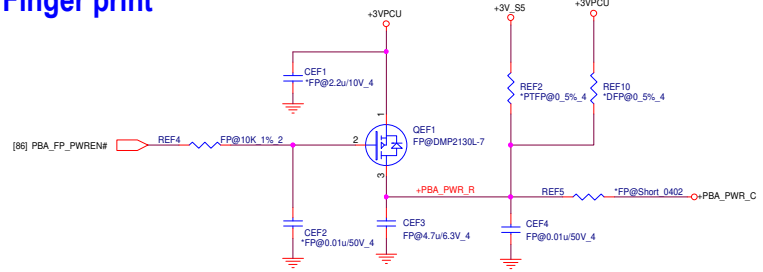
No Haptic Touch SPEC, Follow Beatles



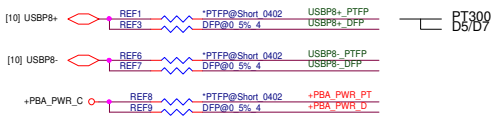
TouchPAD (PT300)



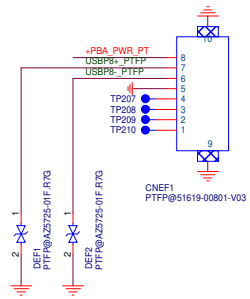
Finger print



Take care placement



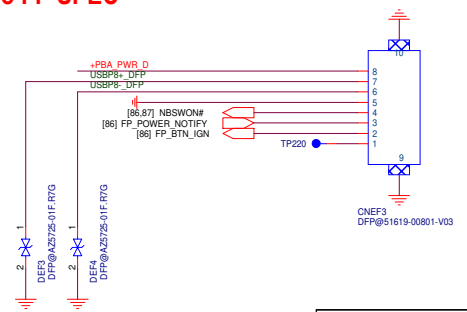
FP (PT300) - Secure ID PAD



FP (D5/D7) - POA Like (FP on keyboard)

Should be (QF03P_A11BWL) + (FP)

No FP SPEC



FP_PWR_NTFY:System power status notify, to info FP keep data or not (Hi-power on; low-power off)

FP_BTN_IGN:Notify system to ignore PWR_BTN signal while Enroll/Verify Process
(While Hi notify EC to keep power while FP is working)

Quanta Computer Inc.
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C	UIF LED	A1A
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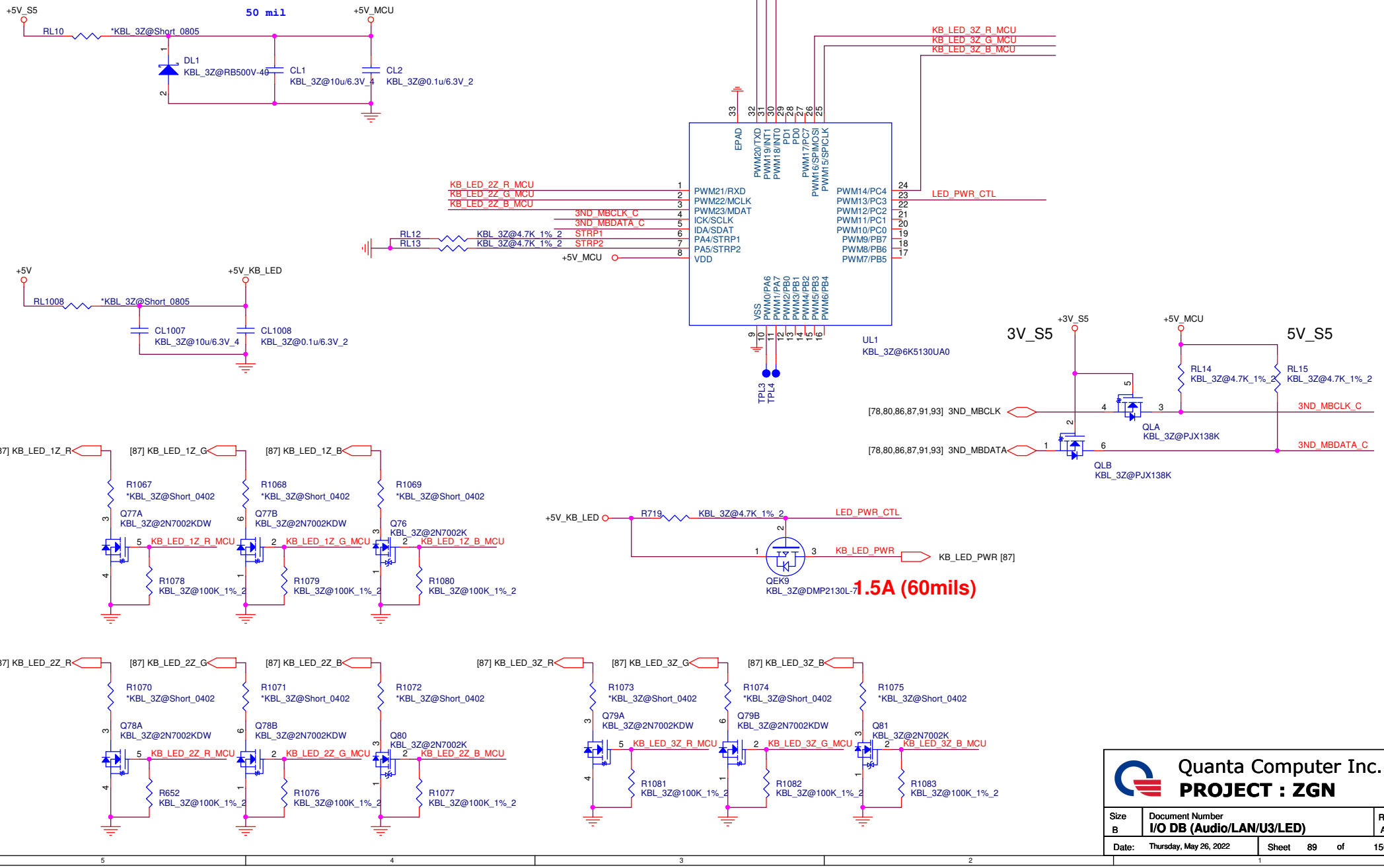
LED Driver [ene6K5130]



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PROJECT : ZGN

Size	Document Number	Rev
B	I/O DB (Audio/LAN/U3/LED)	A1A
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Custom	I/O DB (Audio/LAN/U3/LED)	A1A
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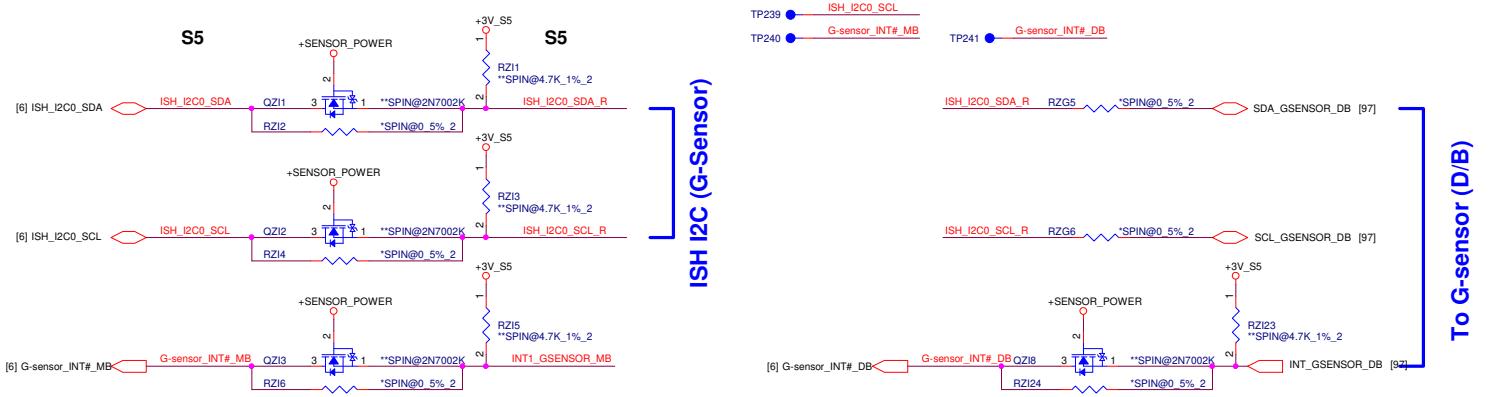
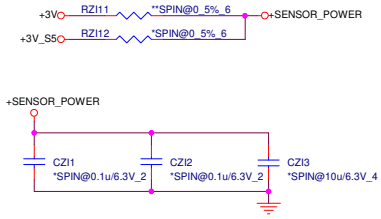
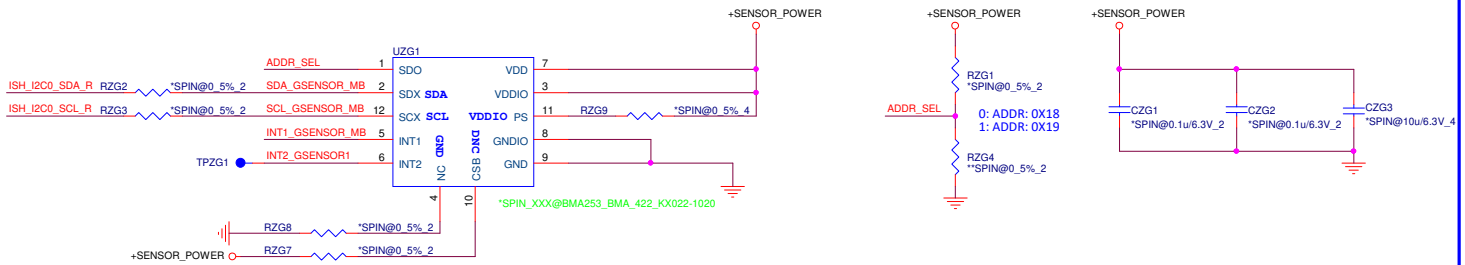
Sensor (D5/D7)



Power



G-sensor (M/B) E-Zel SKU remove on board G-sensor (Need change to BMI260 14 pin)

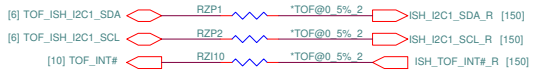


BMA253 AL000253A00
SDO I2C Address:
PU:0X19 (M/B)
PD:0X18 (D/B)

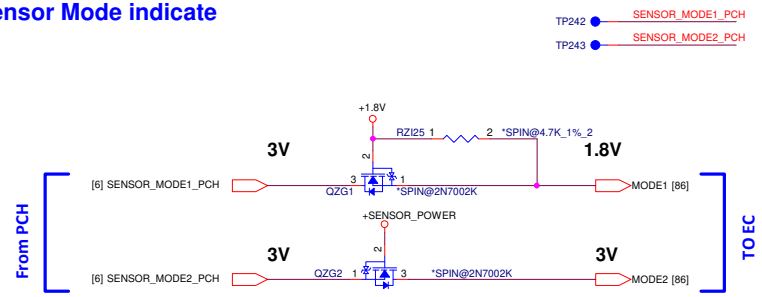
KX022-1020 AL001020A00
SDO I2C Address:
PU:0x1F (M/B)
PD:0x1E (D/B)

BMA422 ----------

TOF Sensor (For P6 only)

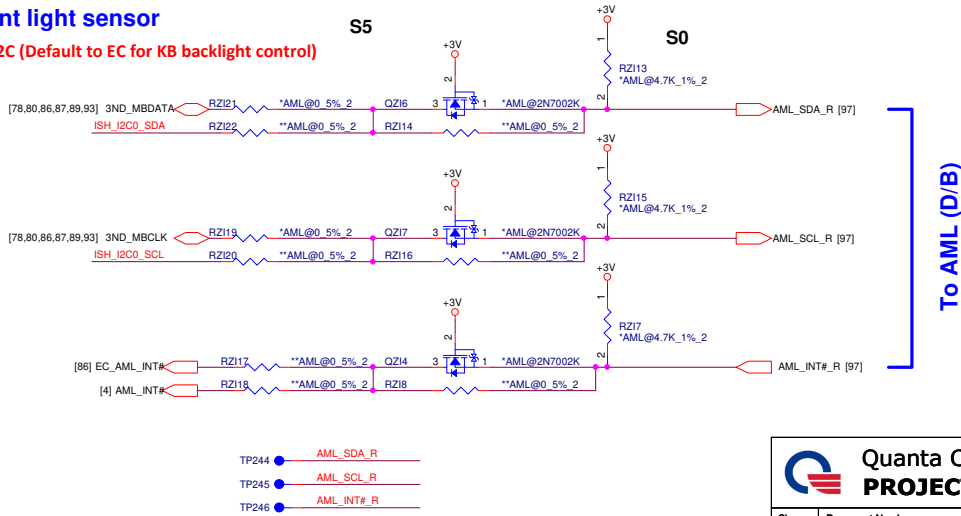


G-sensor Mode indicate



Ambient light sensor

AML I2C (Default to EC for KB backlight control)



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
Custom	Touch / POA	A1A
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PROJECT : ZGN

Size	Document Number	Rev
A	**LTE DB**	A1A

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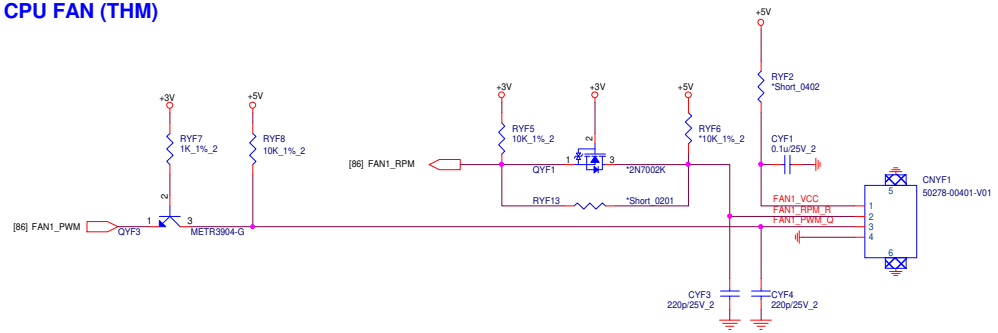
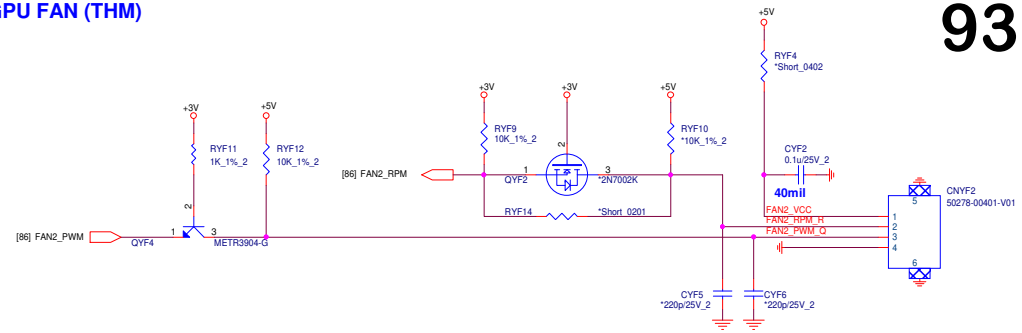
CPU FAN (THM)

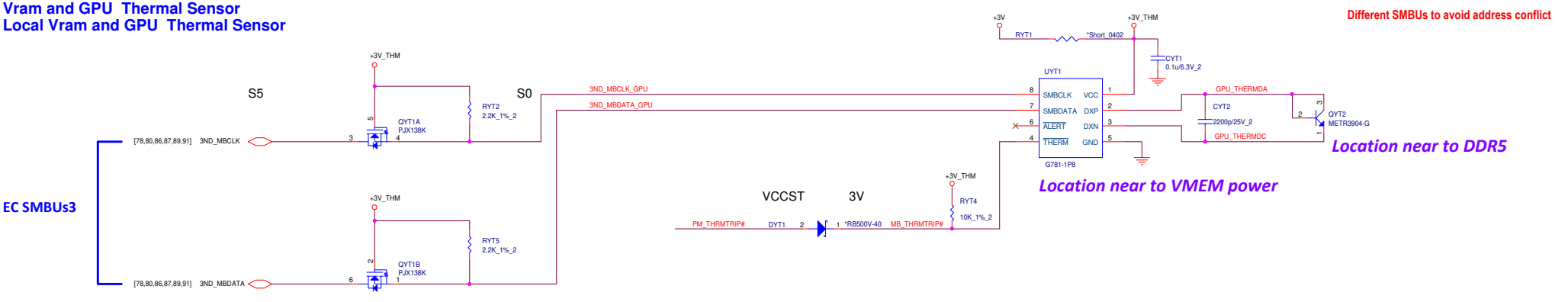


GPU FAN (THM)



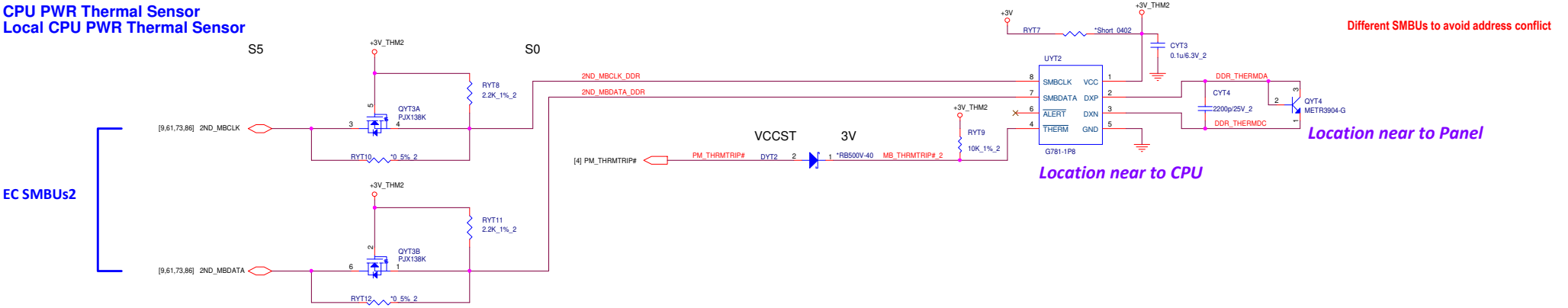
Vram and GPU Thermal Sensor
Local Vram and GPU Thermal Sensor

Different SMBUs to avoid address conflict



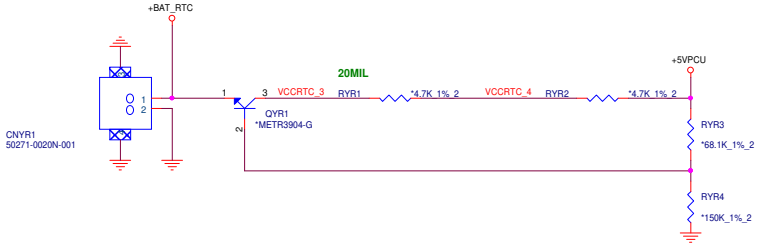
CPU PWR Thermal Sensor
Local CPU PWR Thermal Sensor

Different SMBUs to avoid address conflict



Coin Battery Charging

PT300 non chargeable type



Quanta Computer Inc.
PROJECT : ZGN

Size	Document Number	Rev
C	FAN/Thermal Sensor	A1A
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A	**LTE DB**	A1A

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Size	Document Number	Rev
A	**LTE DB**	A1A

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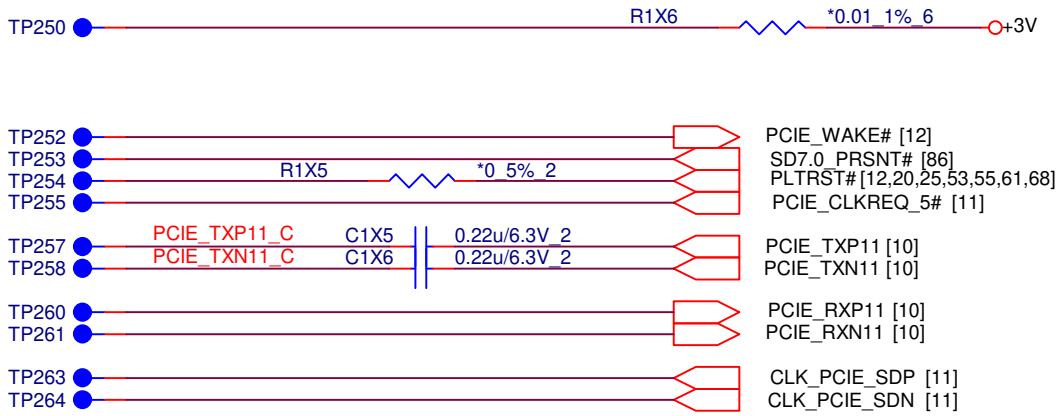
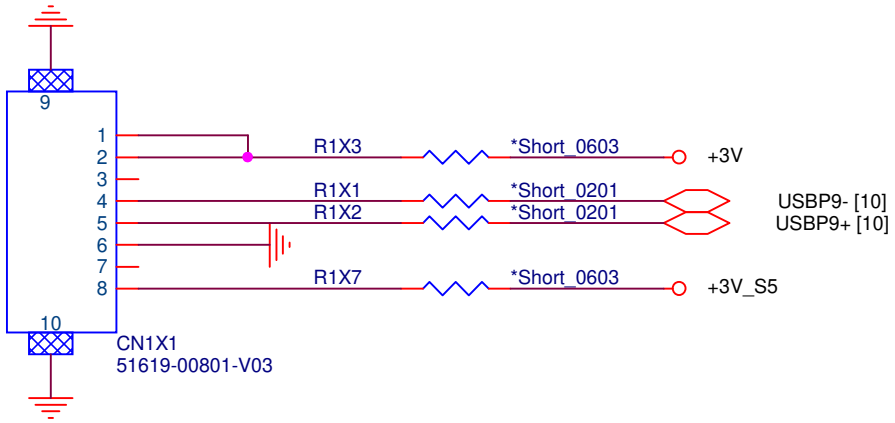
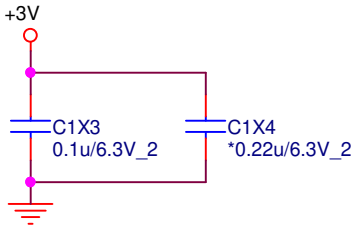
(Concept D) Card reader (SD7.0)



(PT300) Card reader (SD3.0)





Quanta Computer Inc.

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A	**DB1 :SD Card+UIF**	A1A
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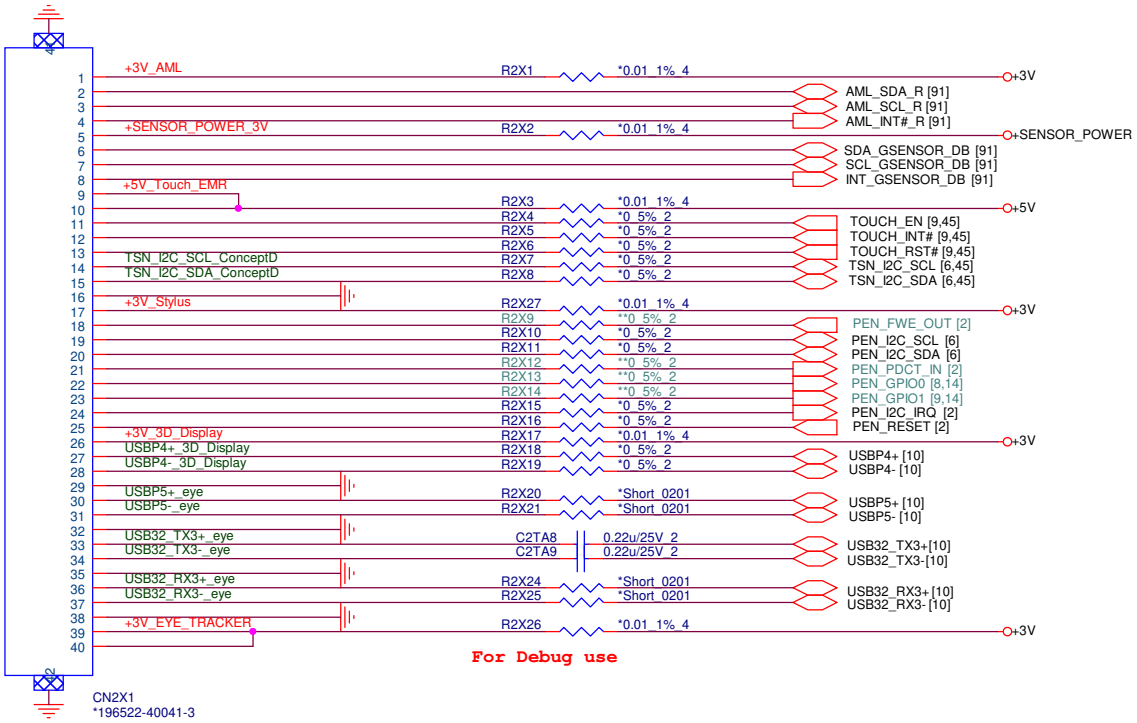
Concept D only (AML+G-sensor+EMR Touch+3D display+EYE Tracker)



Ambient light sensor

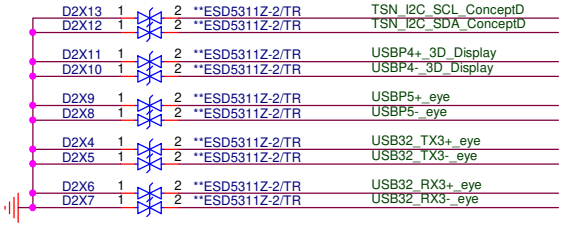
GSENSOR

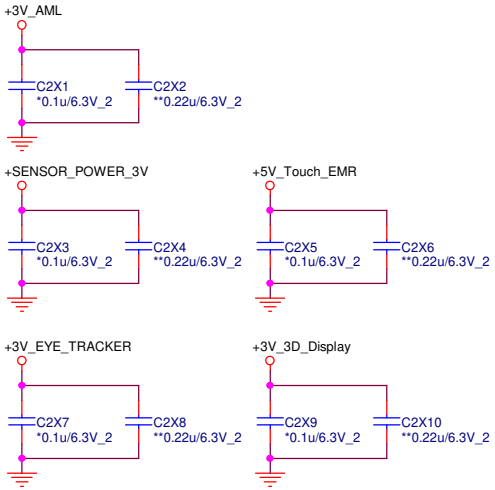
Touch-EMR (I2C)

STYLUS-EMR

3D display

EYE tracker





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Size	Document Number	Rev
B	LTE DB	A1A
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A	**LTE DB**	A1A

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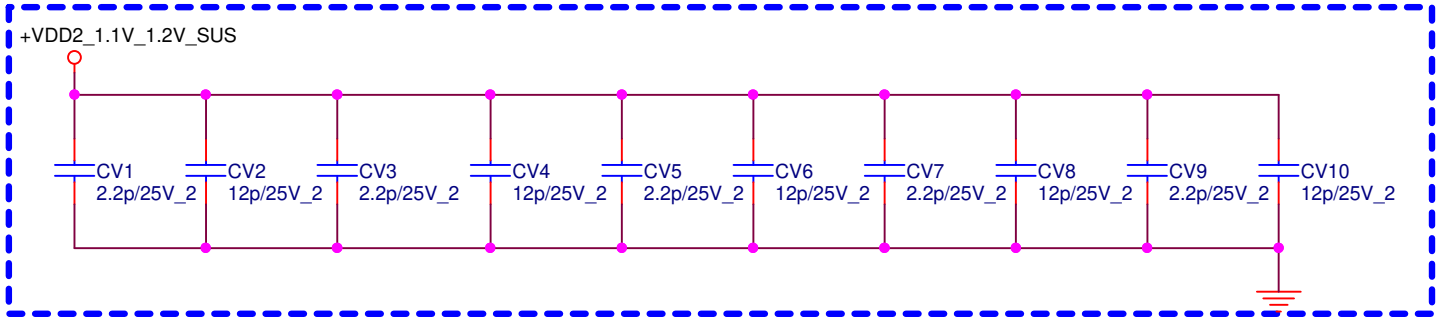
EMC CAPS

PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



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A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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A	**LTE DB**	A1A

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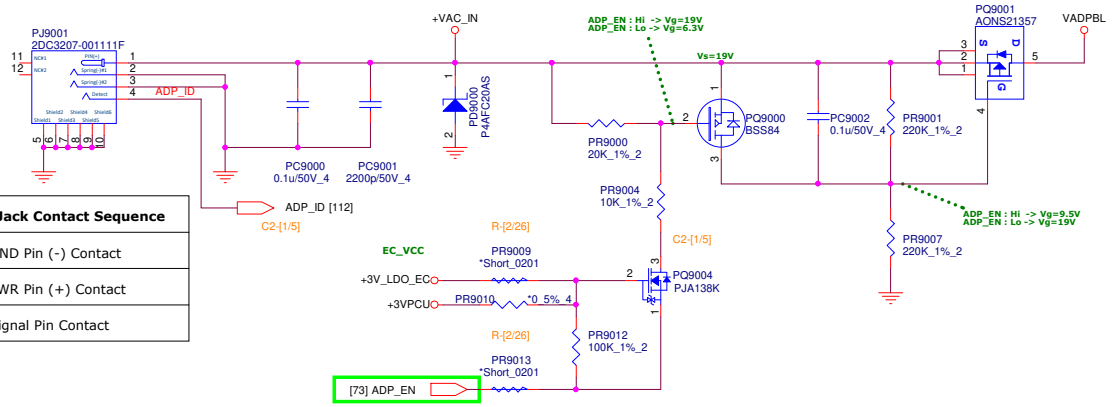
Option for serch.
Project need to check PM support ADP & show into circuit.
Value use SP@ for BOM build notice.

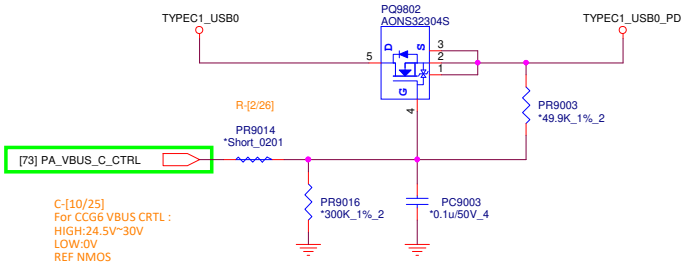
ADP=19V



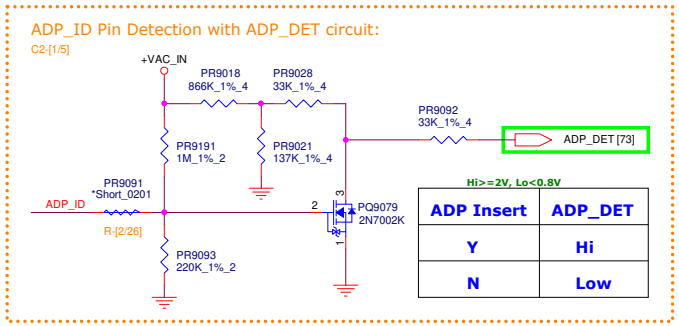
DC Jack Contact Sequence
1. GND Pin (-) Contact
2. PWR Pin (+) Contact
3. Signal Pin Contact

ADP_EN	ADP Switch (PQ9001)
Hi	ON
Low	OFF

Type C PD=20V



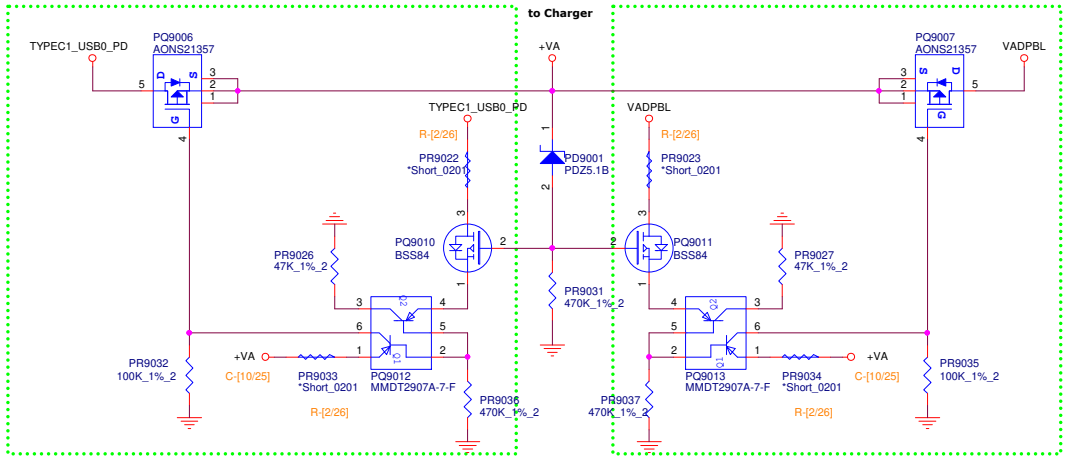
CCG6: PA_VBUS_C_CTRL	Type C Switch (PQ9802)
High	ON
Low	OFF



ADP Insert	ADP_DET
Y	Hi
N	Low

Ideal Diode for Type-C Port

Ideal Diode for Adapter



Vi compare	Vo (=PVADPTR)
TYPEC1_USB0 > VADPBL	TYPEC1_USB0
TYPEC1_USB0 < VADPBL	VADPBL

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Custom	ADP-IN & TYPE-C	A1A
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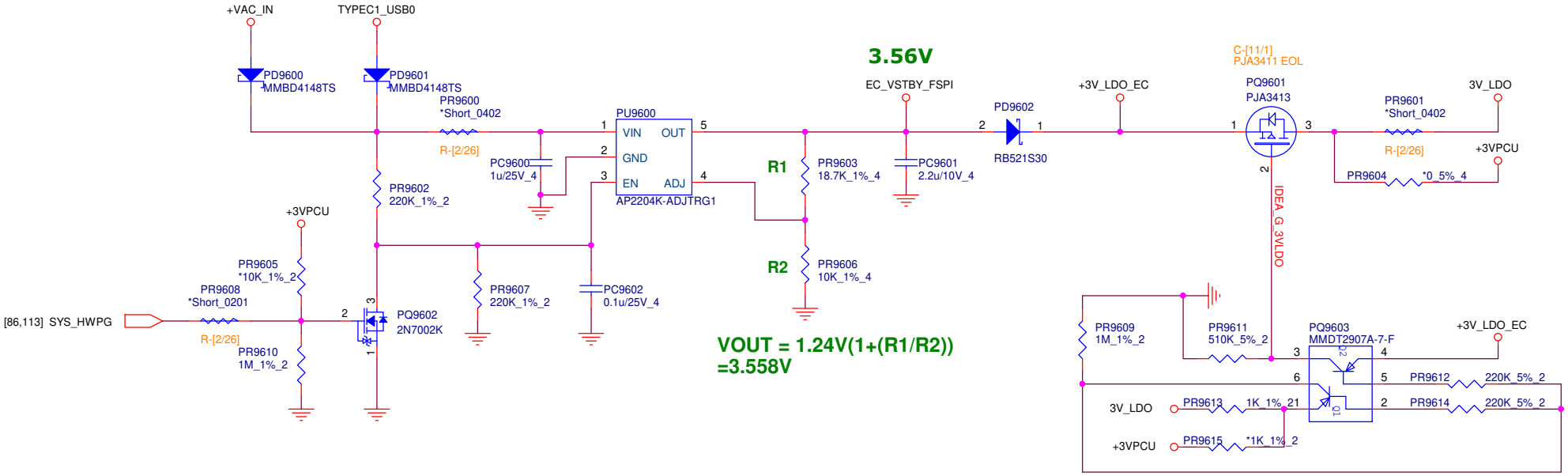
Dead Battery

+VAC_IN [106,112]
TYPEC1_USB0 [73,76,106]

3V_LDO [16,113]
+3V_LDO_EC [86,106,113]
+3VPCU [8,11,45,68,73,74,88,106,112,113,123]

For EC



PU9601 remove.
EE PD IC CYPD6127-48LQXIT(ARXW5FSB000) CYPRESS Integrated high-voltage LDO operational up to 21.5 V for dead battery mode operation.

Quanta Computer Inc. PROJECT : ZGN		
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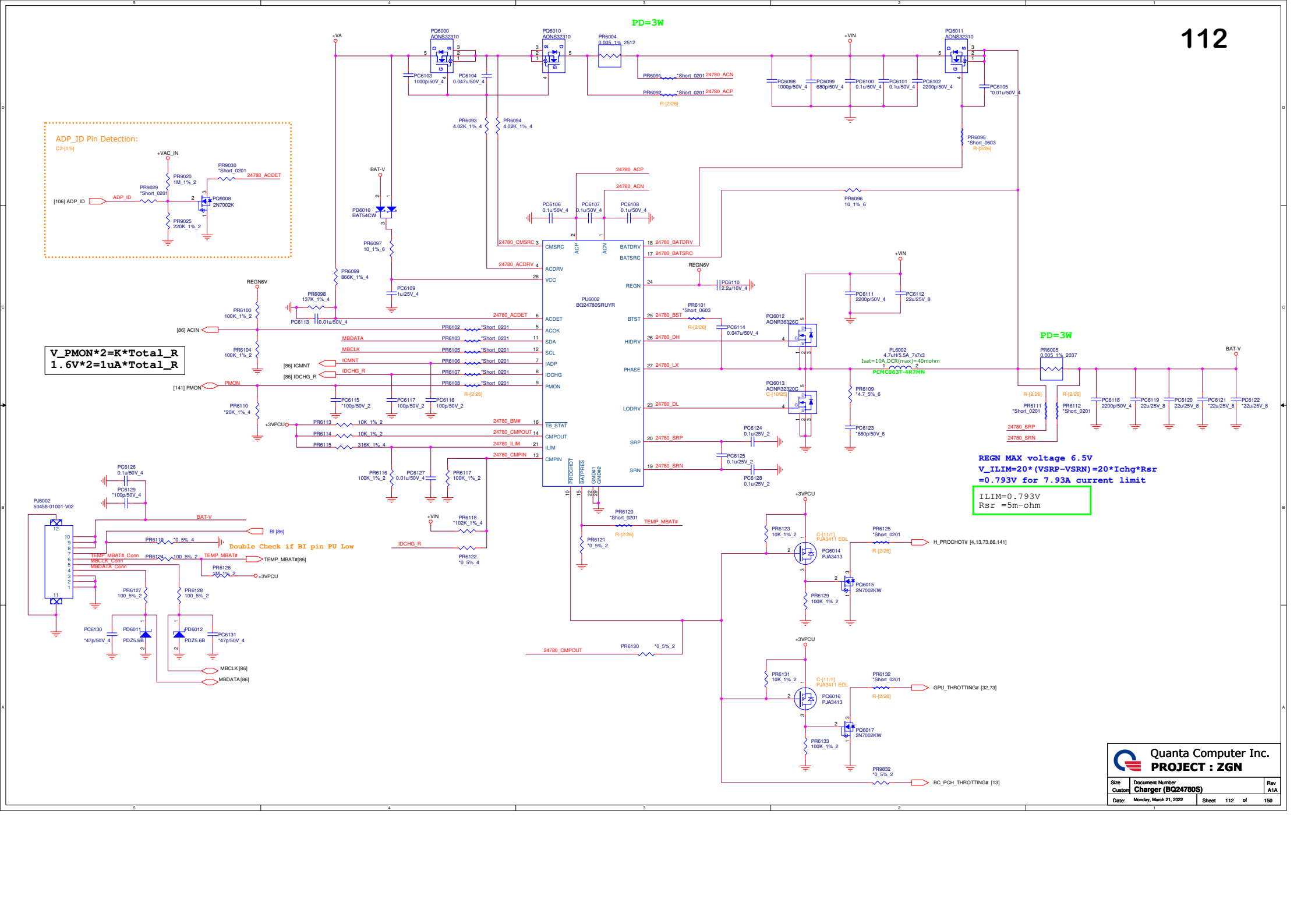
PD=3W
ADP_ID Pin Detection:
C2-[1/5]
+VAC_IN
PR9020 1M_1%_2
PR9030 *Short_0201
24780_ACDET
PR9029 *Short_0201
[106] ADP_ID
ADP_ID
PQ9008 2N7002K
PR9025 220K_1%_2
+VA
PQ6000 AONS32310
PQ6010 AONS32310
PR6004 0.005_1%_2512
PR6091 *Short_0201 24780_ACN
PR6092 *Short_0201 24780_ACP
R-[2/26]
+VIN
PQ6011 AONS32310
PC6098 1000p/50V_4
PC6099 680p/50V_4
PC6100 0.1u/50V_4
PC6101 0.1u/50V_4
PC6102 2200p/50V_4
PC6105 *0.01u/50V_4
PC6103 1000p/50V_4
PC6104 0.047u/50V_4
PR6093 4.02K_1%_4
PR6094 4.02K_1%_4
PR6095 *Short_0603
R-[2/26]
BAT-V
PD6010 BAT54CW
PR6097 10_1%_6
PR6096 10_1%_6
24780_ACP
24780_ACN
PC6106 0.1u/50V_4
PC6107 0.1u/50V_4
PC6108 0.1u/50V_4
24780_CMSRC
24780_ACDRV
PR6099 866K_1%_4
PC6109 1u/25V_4
REGN6V
PR6098 137K_1%_4
PC6113 0.01u/50V_4
PR6100 100K_1%_2
PR6104 100K_1%_2
[86] ACIN
PU6002 BQ24780SRUYR
CMSRC
ACP
ACN
ACDRV
VCC
ACDET
ACOK
SDA
SCL
IADP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
PROCHOT
BATPRES
GND#1
GND#2
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LODRV
SRP
SRN
24780_ACDRV
24780_ACDET
24780_BATDRV
24780_BATSRC
24780_BST
24780_DH
24780_LX
24780_DL
24780_SRP
24780_SRN
24780_BM#
24780_CMPOUT
24780_ILIM
24780_CMPIN
PC6110 2.2u/10V_4
PR6101 *Short_0603
R-[2/26]
PC6114 0.047u/50V_4
PQ6012 AONR36326C
PC6111 2200p/50V_4
PC6112 22u/25V_8
PL6002 4.7uH/5.5A_7x7x3 Isat=10A,DCR(max)=40mohm PCMC063T-4R7MN
PR6109 *4.7_5%_6
PC6123 *680p/50V_6
PQ6013 AONR32320C
C-[10/25]
PC6124 0.1u/25V_2
PC6125 0.1u/25V_2
PC6128 0.1u/25V_2
PD=3W
PR6005 0.005_1%_2037
PR6111 *Short_0201
PR6112 *Short_0201
PC6118 2200p/50V_4
PC6119 22u/25V_8
PC6120 22u/25V_8
PC6121 *22u/25V_8
PC6122 *22u/25V_8
BAT-V
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 7.93A current limit
ILIM=0.793V
Rsr =5m-ohm
V_PMON*2=K*Total_R
1.6V*2=1uA*Total_R
[86] ICMNT
[86] IDCHG_R
[141] PMON
PMON
MBDATA
MBCLK
ICMNT
IDCHG_R
PR6102 *Short_0201
PR6103 *Short_0201
PR6105 *Short_0201
PR6106 *Short_0201
PR6107 *Short_0201
PR6108 *Short_0201
R-[2/26]
PC6115 *100p/50V_2
PC6117 100p/50V_2
PC6116 100p/50V_2
PR6110 *20K_1%_4
+3VPCU
PR6113 10K_1%_2
PR6114 10K_1%_2
PR6115 316K_1%_4
PR6116 100K_1%_2
PC6127 0.01u/50V_4
PR6117 100K_1%_2
+VIN
PR6118 *102K_1%_4
IDCHG_R
PR6122 *0_5%_4
PR6120 *Short_0201
TEMP_MBAT#
R-[2/26]
PR6121 *0_5%_2
PJ6002 50458-01001-V02
PC6126 0.1u/50V_4
PC6129 *100p/50V_4
BAT-V
BI [86]
PR6119 *0_5%_4
Double Check if BI pin PU Low
TEMP_MBAT#_Conn
MBCLK_Conn
MBDATA_Conn
PR6124 100_5%_2
TEMP_MBAT#
TEMP_MBAT#[86]
PR6126 1M_1%_2
+3VPCU
PR6127 100_5%_2
PR6128 100_5%_2
PC6130 *47p/50V_4
PD6011 PDZ5.6B
PD6012 PDZ5.6B
PC6131 *47p/50V_4
MBCLK [86]
MBDATA [86]
+3VPCU
PR6123 10K_1%_2
C-[11/1] PJA3411 EOL
PQ6014 PJA3413
PR6125 *Short_0201
R-[2/26]
H_PROCHOT# [4,13,73,86,141]
PQ6015 2N7002KW
PR6129 100K_1%_2
24780_CMPOUT
PR6130 *0_5%_2
+3VPCU
PR6131 10K_1%_2
C-[11/1] PJA3411 EOL
PQ6016 PJA3413
PR6132 *Short_0201
R-[2/26]
GPU_THROTTING# [32,73]
PQ6017 2N7002KW
PR6133 100K_1%_2
PR9832 *0_5%_2
BC_PCH_THROTTING# [13]
Quanta Computer Inc.
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Size Custom
Document Number Charger (BQ24780S)
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+VIN [16,45,112,114,123,127,131,141,142,143,144,145,146]
+5VPCU [68,73,79,81,87,93,123]
+3VPCU [8,11,45,68,73,74,88,106,111,112,123]
SYS_SHDN# [4,86,123]
3V_LDO [16,111]

[86,111] SYS_HWPG

+5VPCU
5 Volt +/- 5%
TDC : 11.8A
PEAK : 15.74A
OCP : 18.5A
Width : 480mil

+3VPCU
3.3 Volt +/- 5%
TDC : 9A
PEAK : 12A
OCP : 17.4A
Width : 360mil

PU3005
RT6575AGQW

Rds(on)=4.7m ohm

Rds(on)=4.7m ohm

OCP:18.5A (For BAT 4S1P)
L(ripple current)
=(12-5)*5/(2.2u*0.3M*12)
=4.419A
Iocp=18.5-(4.419/2)=16.29A
Vth=(16.29A*4.7mOhm)+1mV=76.56mV
R(Ilim)=(76.56mV*8)/10uA
~60.45K

OCP:17.4A (For BAT 4S1P)
L(ripple current)
=(12-3.3)*3.3/(1.5u*0.355M*12)
~4.493A
Iocp=17.4-(4.493/2)=15.15352A
Vth=(15.15352A*4.7mOhm)+1mV=71.222mV
R(Ilim)=(71.222mV*8)/10uA
=56.177K

Power Auto Recovery
(Stuff on Dead Battery page)

+5V_S5 [87,88,89,114,126,127,130,131,141,142,143,144]
+5V [49,64,87,89,93,97,123]
+3V_S5 [13,16,19,20,45,61,74,86,87,88,89,91,96,123,124,126,129,131,144,146]
+3V [2,6,9,11,12,15,21,29,32,44,45,48,53,55,61,64,68,74,86,87,88,91,93,96,97,114,123,126,130,131,141,144]

TDC : 5.63A
PEAK : 7.5A
Width : 100mil

TDC : 1.68A
PEAK : 2.24A
Width : 220mil

TDC : 4.68A
PEAK : 6.24A
Width : 140mil

TDC : 4.5A
PEAK : 6A
Width : 240mil

JW7110DFNC_TRPBF

TDC : 0.05A
PEAK : 0.1A
Width : 20mil

[21,22,86,114,123,144,146] SUSON

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+VIN [16,45,112,113,123,127,131,141,142,143,144,145,146]
+VDD2_1.1V_1.2V_SUS [3,5,101,131]
+3V [2,6,9,11,12,15,21,29,32,44,45,48,53,55,61,64,68,74,86,87,88,91,93,96,97,113,123,126,130,131,141,144]
+5V_S5 [87,88,89,113,126,127,130,131,141,142,143,144]

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Option
+VDDQ / +VDDQ_VTT no use on DDR5

+VDD2_1.1V_1.2V
1.116 Volt +/- 5%
TDC : 5.35A
PEAK : 7.13A
OCP : 14.285A
Width : 220mil

OCP=13.86A
Fsw=500KHz
Rds(on)=15.9m ohm
Vo=0.75*(1+R1/R2)

OCP_RTK=14.4A [RTK]
L ripple current
=(12-1.116364)*1.116364/(1u*499k*12) =2.029A
Vtrip=14.285-(2.029/2)*15.9mohm=211.0mV
Rlimit=211.0mV/5uA*10=422Kohm

GMT_current limit=200mV
OCP_GMT=(200mV/15.9mohm)+(2.029/2)=13.59A [GMT]

VID	Ref. Voltage
High	0.675V
Low	0.75V

VID	R1	R2	Vout
High	8.2K_1%_2 CS28201FE00	10K_1%_2 CS31001FE14	1.2285V
Low	8.06K_1%_2 CS28061FE00	15.8K_1%_2 CS31581FE00	1.116V Default

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Size	Document Number	Rev
Custom	DDR4_+VDD2_1.1V_1.2V (G5619RZ1U)	A1A
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Custom	GPIO	A1A
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+1.8V_S5
1.8Volt +/- 5%
TDC : 1.83A
PEAK : 2.44A
Width : 80mil

PU4005 JW5213DFND#TRPBF
PL4005 1uH/3.7A_2.5x2.0x1.2 Isat=3.8A,DCR=43mohm
R1 PR4062 20K_1%_4
R2 PR4064 10K_1%_2
Vo=0.6*(R1+R2)/R2
=1.8V

TDC : 0.08A
PEAK : 0.1A
Width : 5mil

PU4010 AP2121AK-1.8TRG1

TDC : 0.08A
PEAK : 0.1A
Width : 5mil

TDC : 0.63A
PEAK : 0.84A
Width : 30mil

PU4011 JW7110DFNC_TRPBF

For USB3.0 retimer:

+1.2VSUS
1.2Volt +/- 5%
TDC : 0.6A
PEAK : 0.8A
Width : 20mil

PU4006 JW5222RSOTB_TRPBF
PL4006 2.2uH/1.85A_2.5x2.0x1.2 Isat=2.15A,DCR=80mohm
R1 PR4073 15K_1%_4
R2 PR4074 15K_1%_4
Vo=(0.6(R1+R2)/R2)
=1.2V

Thermal protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=95.5'C

PU4007 TMP708AIDBVR
Rset(Kohm)=0.0012T*T-0.9308T+96.147
=29.4K ohm
C2-[12/3] Follow ZGF

HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

PQ4004 DDTC144EUA-7-F
PQ4005 2N7002K
PQ4006 2N7002K
PQ4007 2N7002K
PQ4009 2N7002K

Quanta Computer Inc.
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C	+1.8V_S5/1.2V /Thermal	A1A
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+3V_S5 [13,16,19,20,45,61,74,86,87,88,89,91,96,113,123,126,129,131,144,146]
+VNN_EXT [13]
+1.05V_EXT [13]

+VNN_EXT
1.05 / 0.76 Volt +/- 5%
PEAK : 0.5A
Width : 40mil

PJ1005 *Short_0603
+3V_S5 — R-[2/26] — 659SVIN_VNN
PC1465 VNN@0.01u/50V_4
PC1466 VNN@10u/6.3V_4

PU1023 VNN@SYV659LQWC
+3V_S5 — PR1439 VNN@10K_1%_2
+VNN_EXT_PWRGD — PR1440 *Short_0201
[86] VNN_V105_EN — PR1441 *0_5%_2 — 659EN_VNN
[86,124,144] VCCIN_AUX_PG — PR1483 VNN@0_5%_2
R-[2/26]
PC1468 VNN@0.1u/6.3V_2
659PG_VNN
659MODE_VNN
659FB_VNN
659LX_VNN
PG, EN, MODE, IN, LX, FB, GND

PR1438 VNN@2.2_5%_6 — SN_VNN — PC1467 VNN@2200p/25V_2
PL1020 VNN@1uH/3.7A_2.5x2.0x1.2
Isat=3.8A,DCR=43mohm
+VNN_EXT_SRC
PJ1006 VNN@0_5%_8
PC1469 VNN@0.1u/6.3V_2
PC1470 VNN@22u/6.3V_6
PC1471 VNN@10u/6.3V_4

PC1472 VNN@470p/25V_2
PR1442 *Short_0201 — R-[2/26]
PR1443 VNN@3K_1%_2 — R1
R2
PR1445 VNN@6.49K_1%_2
PR1446 VNN@10K_1%_2

VNN=0.6*(R1+R2)/R2

MAINON=H	0.78V
MAINON=L	1.05V

PR1444 VNN@1K_1%_4 — 659MODE_VNN_1
PR1447 *0_5%_2 — VNN_CTRL_R
MAINON [86,113,114,123,124,144]
PC1473 VNN@100p/50V_2
PR1449 *Short_0201 — R-[2/26]
659MODE_VNN_3
PR1450 VNN@1K_1%_4
PC1474 VNN@1000p/50V_2
PR1451 VNN@1M_1%_2 — C-[10/25]
PR1452 VNN@1M_1%_2 — C-[10/25]
PR1448 VNN@10K_1%_2
PQ1003A VNN@2N7002KDW
PQ1003B VNN@2N7002KDW

+3V_DEEP_SUS
PC1490 *0.1u/6.3V_2
VNN_CTRL_R
VNN_CTRL [13]
SUSB# [12,16,86]
PU1025 *NL17SZ08DFT2G

+1.05V_EXT
1.05Volt +/- 5%
PEAK : 0.5A
Width : 40mil

PJ1007 *Short_0603
+3V_S5 — R-[2/26] — 659SVIN_105
PC1475 VNN@0.01u/50V_4
PC1476 VNN@10u/6.3V_4

PU1024 VNN@SYV659LQWC
+3V_S5 — PR1454 VNN@10K_1%_2
[86] +1.05V/VNN_EXT_PG — PR1455 *Short_0201
+VNN_EXT_PWRGD — PR1456 *0_5%_2 — 659EN_105
[86,124,144] VCCIN_AUX_PG — PR1484 VNN@10K_1%_2
R-[2/26]
PC1478 VNN@0.1u/6.3V_2
659PG_105
659MODE_105
659FB_105
659LX_105
PG, EN, MODE, IN, LX, FB, GND

PR1453 VNN@2.2_5%_6 — SN_105 — PC1477 VNN@2200p/25V_2
PL1021 VNN@1uH/3.7A_2.5x2.0x1.2
Isat=3.8A,DCR=43mohm
+1.05V_EXT_SRC
PJ1008 VNN@0_5%_8
PC1479 VNN@0.1u/6.3V_2
PC1480 VNN@22u/6.3V_6
PC1481 VNN@10u/6.3V_4

PC1482 VNN@22p/50V_2
PR1457 *Short_0201 — R-[2/26]
PR1458 VNN@6.04K_1%_2 — R1
R2
PR1459 VNN@40.2K_1%_2
PR1460 VNN@10K_1%_2

+1.05V_EXT=0.6*(R1+R2)/R2

MAINON=H	0.96V
MAINON=L	1.05V

PR1461 VNN@1K_1%_4 — 659MODE_105_1
PR1462 VNN@0_5%_2
V1P05_CTRL [13]
MAINON [86,113,114,123,124,144]
PC1483 VNN@100p/50V_2
PR1464 *0_5%_2
659MODE_105_3
PR1465 VNN@1K_1%_4
PC1484 VNN@1000p/50V_2
PR1466 VNN@1M_1%_2 — C-[10/25]
PR1467 VNN@1M_1%_2 — C-[10/25]
PR1463 VNN@10K_1%_2
PQ1004A VNN@2N7002KDW
PQ1004B VNN@2N7002KDW

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Custom	+VNN_EXT & +1.05V_EXT (SYV659LQWC)	A1A
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Custom	GPIO	A1A
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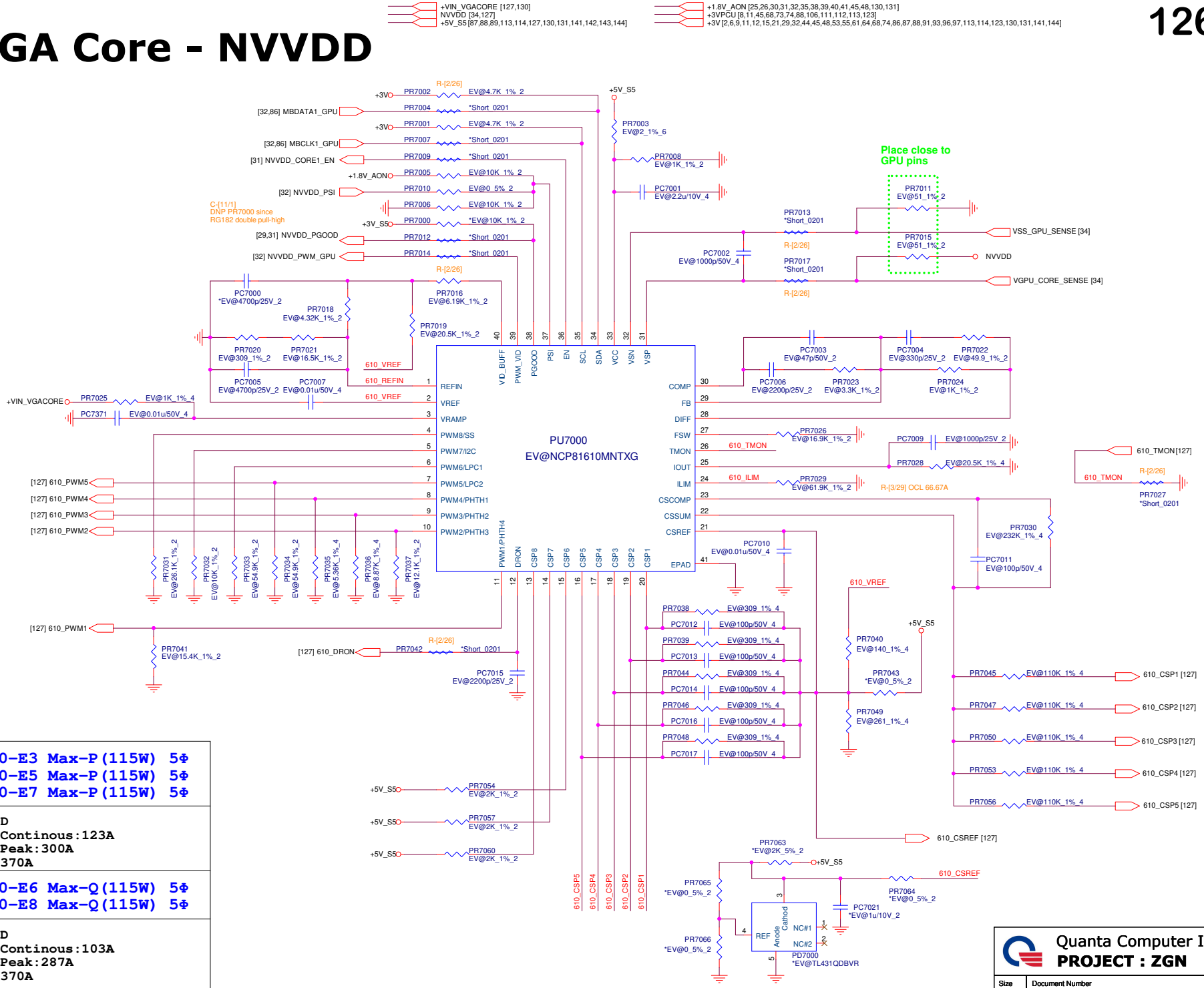
VGA Core - NVVDD



GN20-E3 Max-P (115W) 5Φ **GN20-E5 Max-P (115W) 5Φ** **GN20-E7 Max-P (115W) 5Φ**
NVVDD **EDP-Continous:123A** **EDP-Peak:300A** **OCP:370A**
GN20-E6 Max-Q (115W) 5Φ **GN20-E8 Max-Q (115W) 5Φ**
NVVDD **EDP-Continous:103A** **EDP-Peak:287A** **OCP:370A**

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Custom	+VGPU (NCP81610)	A1A
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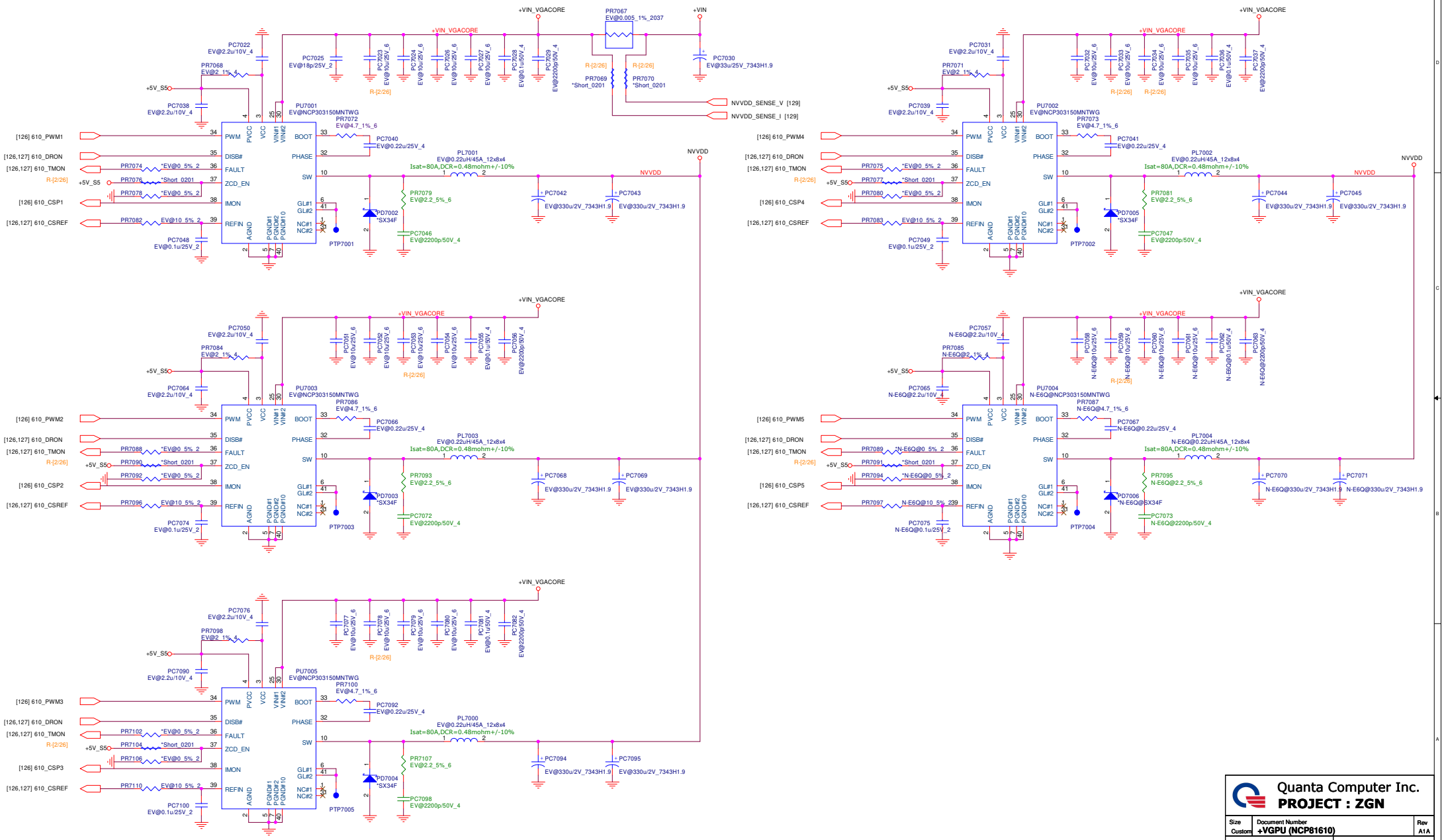
+VIN_VGACORE [126,130]
NVVDD [34,126]
+5V_S5 [87,88,89,113,114,126,130,131,141,142,143,144]



Quanta Computer Inc.
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Size	Document Number	Rev
Custom	+VGPU (NCP81610)	A1A
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Custom	GPIO	A1A
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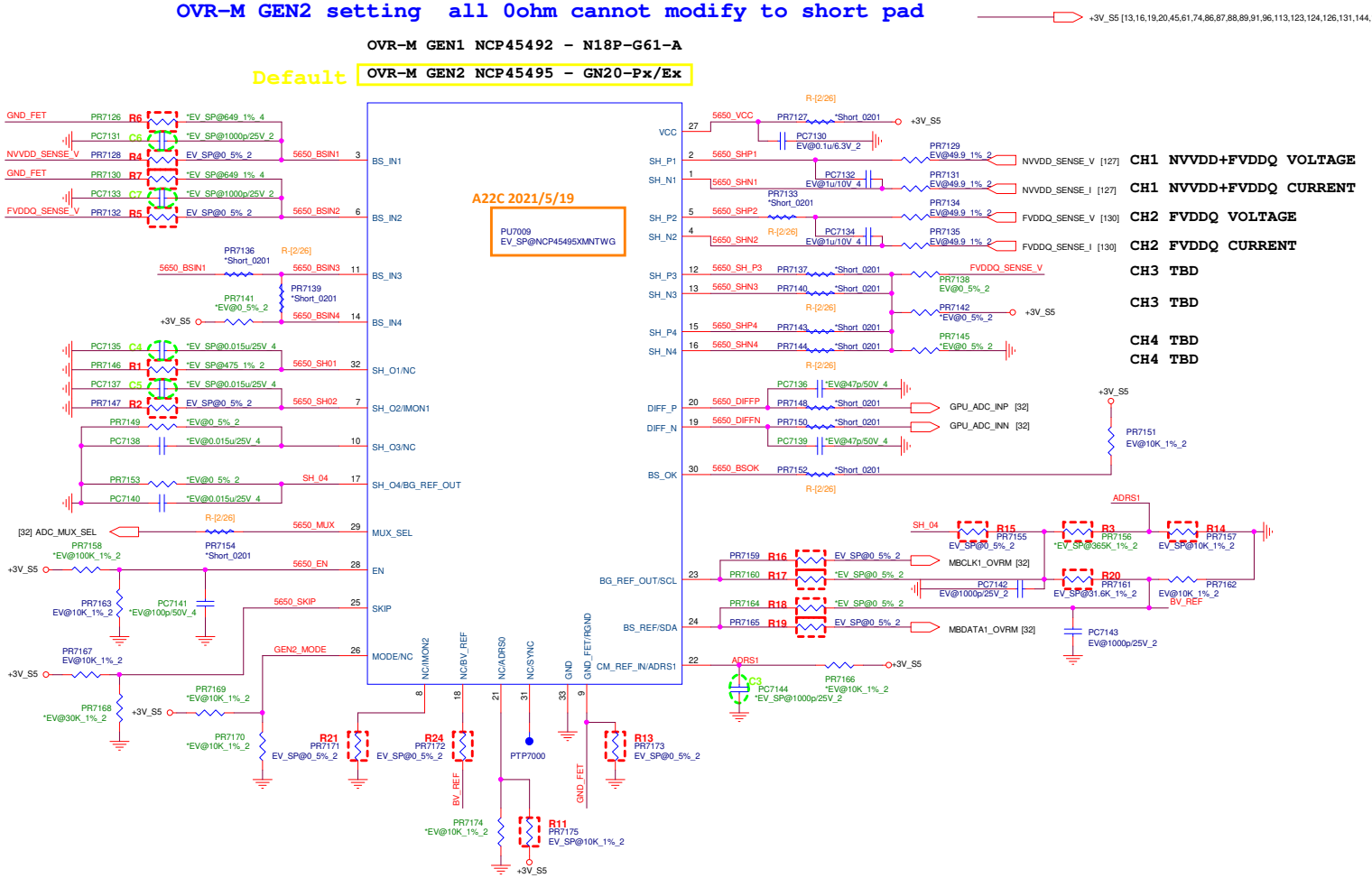
OVR-M GEN2 setting all 0ohm cannot modify to short pad

OVR-M GEN1 NCP45492 - N18P-G61-A

Default OVR-M GEN2 NCP45495 - GN20-Px/Ex



		Default			
		Gen2 - GN20-P1-A1/QN20-P1-A1 NCP45495 / AL045495000		Gen1 - N18P-G61-A NCP45492 / AL045492000	
	Location	Value	PN	Value	PN
Pin3	R4 -PR7128	0 ohm_2	CS00001JE18	75K ohm_2	CS37501FE00
	R6 -PR7126	NC		649 ohm_4	CS16492FB13
	C6 -PC7131	NC		1nF_2	CH2104K1E00
Pin6	R5 -PR7132	0 ohm_2	CS00001JE18	75K ohm_2	CS37501FE00
	R7 -PR7130	NC		649 ohm_4	CS16492FB13
	C7 -PC7133	NC		1nF_2	CH2104K1E00
Pin7	R2 -PR7147	0 ohm_2	CS00001JE18	475 ohm_2	CS14751FE00
	C5 -PC7137	NC		15nF_4	CH3154K1B00
Pin8	R21-PR7171	0 ohm_2	CS00001JE18	NC	
Pin9	R13-PR7173	0 ohm_2	CS00001JE18	NC	
Pin18	R24-PR7172	0 ohm_2	CS00001JE18	NC	
Pin21	R11-PR7175	10K ohm_2	CS31001FE14	NC	
Pin22	C3 -PC7144	NC		1nF_2	CH2104K1E00
Pin23	R3 -PR7156	NC		365K ohm_2	CS43651FE01
	R14-PR7157	10K ohm_2	CS31001FE14	681K ohm_2	CS46811FE01
	R15-PR7155	0 ohm_2	CS00001JE18	NC	
	R16-PR7159	0 ohm_2	CS00001JE18	NC	
	R17-PR7160	NC		0 ohm_2	CS00001JE18
	R20-PR7161	31.6K ohm_2	CS33161FE00	243K ohm_2	CS42431FE00
Pin24	R18-PR7164	NC		0 ohm_2	CS00001JE18
	R19-PR7165	0 ohm_2	CS00001JE18	NC	
Pin32	R1-PR7146	NC		475 ohm_2	CS14751FE00
	C4-PC7135	NC		15nF_4	CH3154K1B00

Quanta Computer Inc.

PROJECT : ZGF

Size	Document Number	Rev
	OVR-M GEN2	1A

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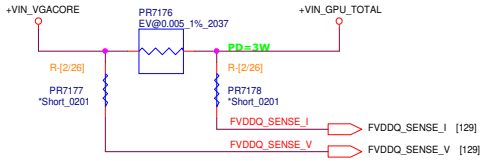
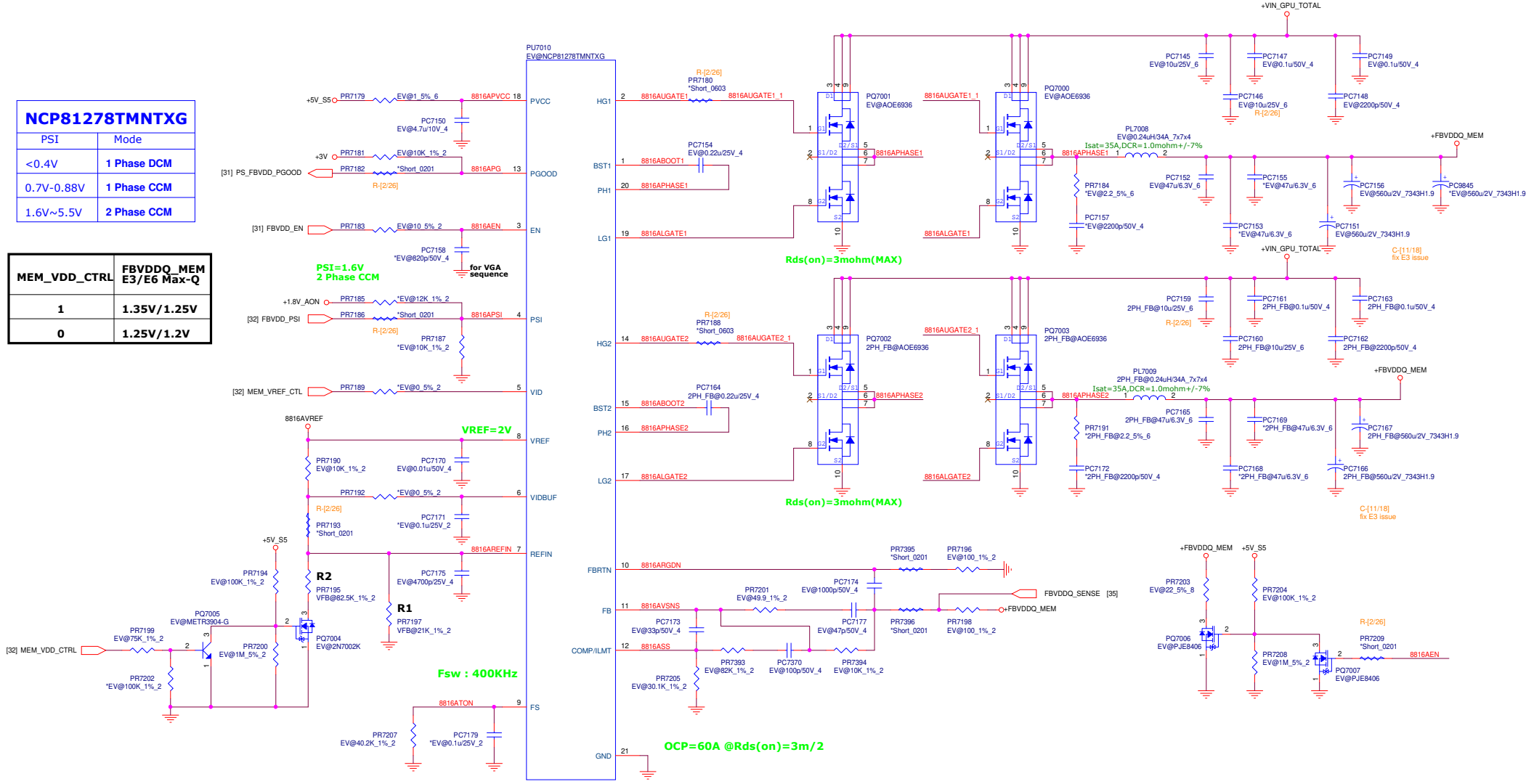
VGA Core - FBVDDQ_MEM



NCP81278TMNTXG	
PSI	Mode
<0.4V	1 Phase DCM
0.7V-0.88V	1 Phase CCM
1.6V~5.5V	2 Phase CCM

MEM_VDD_CTRL	FBVDDQ_MEM E3/E6 Max-Q
1	1.35V/1.25V
0	1.25V/1.2V



VFB@ FBVDDQ_MEM	R1 (PR7197)	R2 (PR7195)
GN20-E3 1.35V/1.25V	21K_1%_2 CS32101FE00	82.5K_1%_2 CS38251FE01
GN20-E6 Max-Q 1.25V/1.2V	16.9K_1%_2 CS31691FE00	150K_1%_2 CS41501FE06

GN20-E3 (115W) 2Φ GN20-E5 (125W) 2Φ GN20-E7 (150W) 2Φ	GN20-E6 Max-Q (90W) 2Φ GN20-E8 Max-Q (90W) 2Φ
FBVDDQ_MEM EDP-Continous:45A EDP-Peak:59A OCP:70A	NVVDD EDP-Continous:34A EDP-Peak:45A OCP:70A

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Custom	+FBVDDQ_MEM (NCP81278T)	A1A
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+3VPCU [8,11,45,68,73,74,88,106,111,112,113,123]
+1.8V_AON [25,26,30,31,32,35,38,39,40,41,45,48,126,130]
+5VPCU [68,73,79,81,87,93,113,123]
+VIN [16,45,112,113,114,123,127,141,142,143,144,145,146]
+VDD2_1.1V_1.2V_SUS [3,5,101,114]
+5V_S5 [87,88,89,113,114,126,127,130,141,142,143,144]
+3V [2,6,9,11,12,15,21,29,32,44,45,48,53,55,61,64,68,74,86,87,88,91,93,96,97,113,114,123,126,130,141,144]

+1.8V_AON
1.8Volt +/- 5%
TDC : 5.18A
PEAK : 6.91A
Width : 210mil
FSW : 600KHZ

PU7027 EV@SY8386RHC
PL7021 EV@1.5uH/9A_7x7x3 Isat=18A,DCR=14mohm
R1
R2 Vo=0.6/R2 *(R1+R2)

+1V_GFX(1.0V)
TDC : 3.15A
PEAK : 4.2A
Width : 130mil

PQ7012 EV@AONR32320C
PU7013 EV@G9336ADJTP1U
PQ7013 EV@2N7002K
PQ7014 EV@DMG1012T-7
PQ7015 EV@2N7002K
PD7001 EV@1SS355
R1
R2
Vout1=(1+R1/R2)*0.5 =0.95V

PQ7008 EV@DDTC144EUA-7-F
PQ7009 EV@2N7002KW

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Size: Custom	Document Number: +1.8V_AON & +1.8V_MAIN & +1V_GFX	Rev: A1A
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Custom	GPIO	A1A
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Custom	GPIO	A1A
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Custom	GPIO	A1A
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Size	Document Number	Rev
Custom	GPIO	A1A
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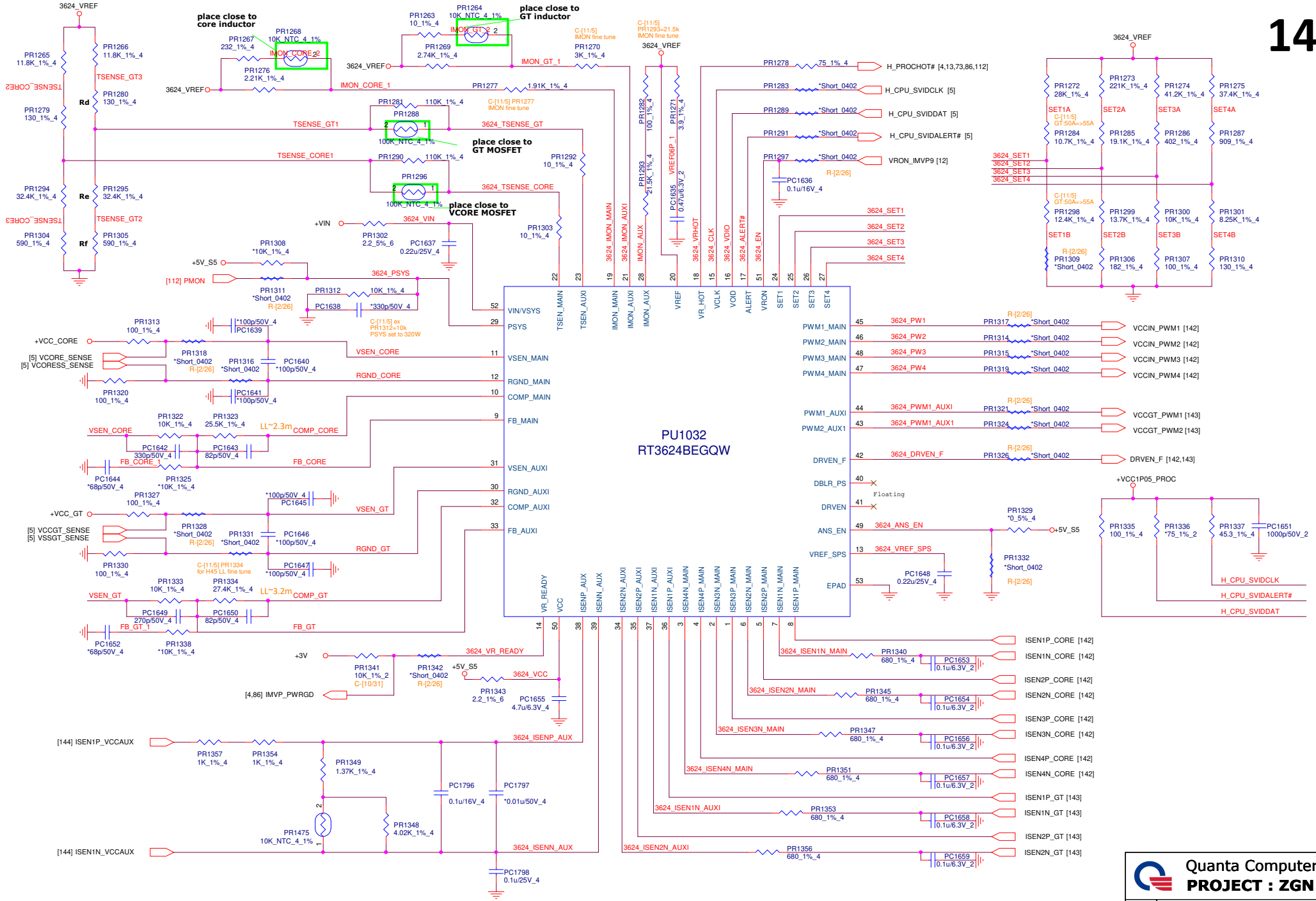

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Size: Custom	Document Number: CPU VR (RT3624BE)	Rev: A1A
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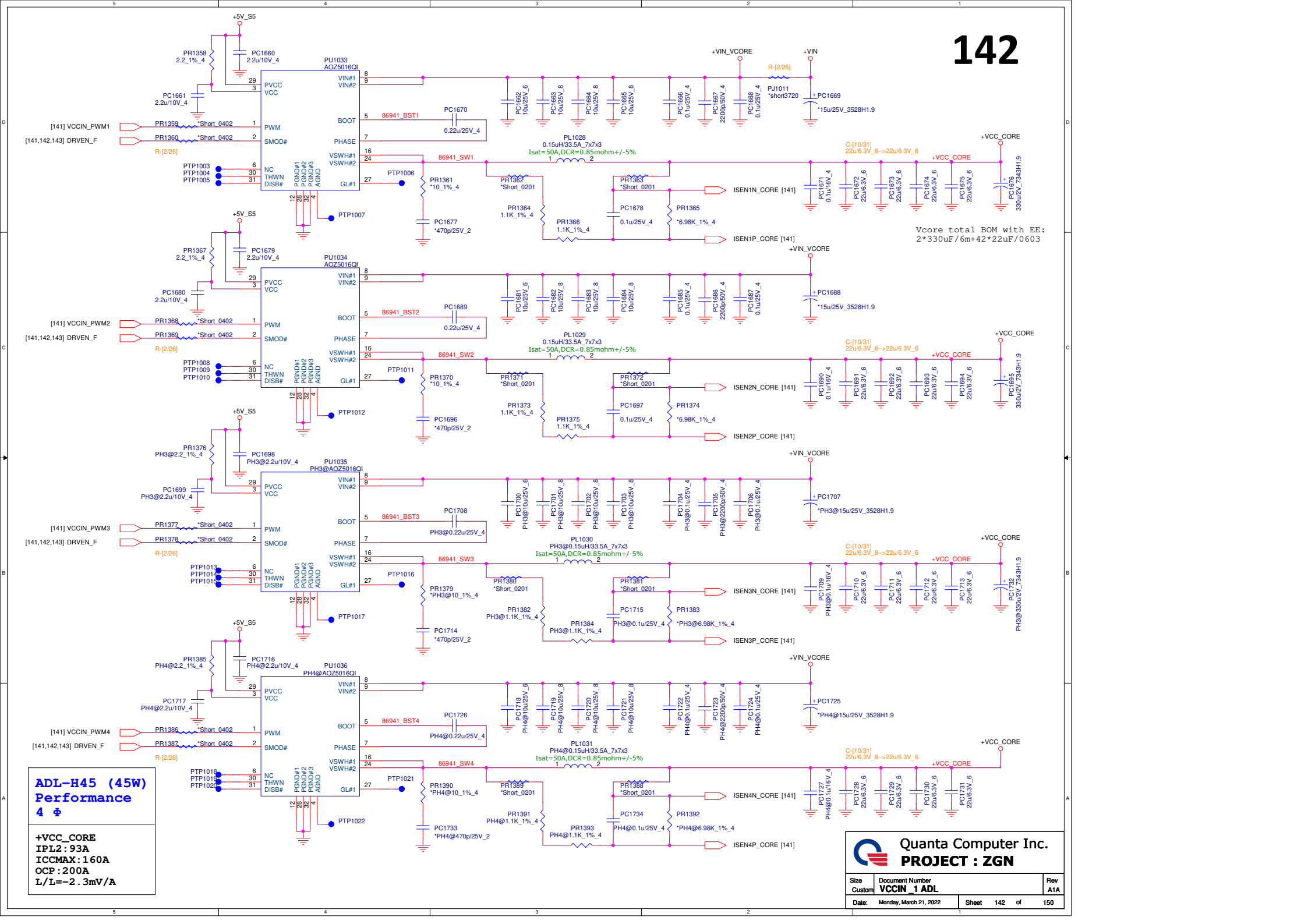
142
+5V_S5
PU1033
AOZ5016QI
PU1034
AOZ5016QI
PU1035
PH3@AOZ5016QI
PU1036
PH4@AOZ5016QI
+VIN_VCORE
+VIN
+VCC_CORE
PJ1011
*short3720
PL1028
0.15uH/33.5A_7x7x3
Isat=50A,DCR=0.85mohm+/-5%
PL1029
0.15uH/33.5A_7x7x3
Isat=50A,DCR=0.85mohm+/-5%
PL1030
PH3@0.15uH/33.5A_7x7x3
Isat=50A,DCR=0.85mohm+/-5%
PL1031
PH4@0.15uH/33.5A_7x7x3
Isat=50A,DCR=0.85mohm+/-5%
[141] VCCIN_PWM1
[141] VCCIN_PWM2
[141] VCCIN_PWM3
[141] VCCIN_PWM4
[141,142,143] DRVEN_F
86941_BST1
86941_BST2
86941_BST3
86941_BST4
86941_SW1
86941_SW2
86941_SW3
86941_SW4
ISEN1N_CORE [141]
ISEN1P_CORE [141]
ISEN2N_CORE [141]
ISEN2P_CORE [141]
ISEN3N_CORE [141]
ISEN3P_CORE [141]
ISEN4N_CORE [141]
ISEN4P_CORE [141]
Vcore total BOM with EE:
2*330uF/6m+42*22uF/0603
ADL-H45 (45W)
Performance
4 Φ
+VCC_CORE
IPL2:93A
ICCMAX:160A
OCP:200A
L/L=-2.3mV/A
Quanta Computer Inc.
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Size
Custom
Document Number
VCCIN_1 ADL
Rev
A1A
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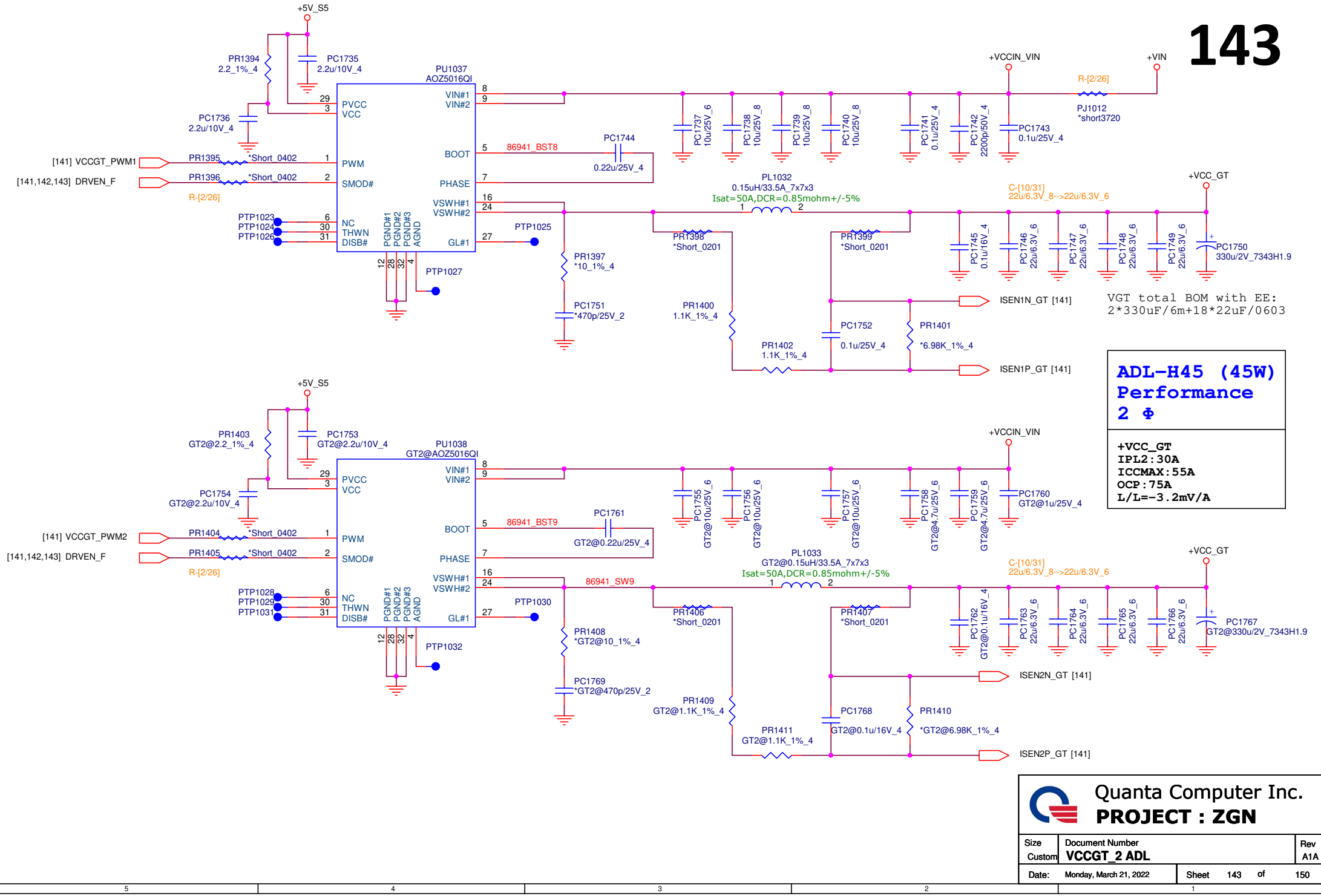

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Size	Document Number	Rev
Custom	VCCGT_2 ADL	A1A
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VID1	VID0	O/P
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

Default

+VIN [16,45,112,113,114,123,127,131,141,142,143,145,146]
+VCCIN_AUX [13]

+5V_S5 [87,88,89,113,114,126,127,130,131,141,142,143]
+3V_S5 [13,16,19,20,45,61,74,86,87,88,89,91,96,113,123,124,126,129,131,146]
+3V [2,6,9,11,12,15,21,29,32,44,45,48,53,55,61,64,68,74,86,87,88,91,93,96,97,113,114,123,126,130,131,141]

PR1412 *0_5%_4 +3V_S5
PR1413 *100K_1%_2 VCCIN_AUX_VID0
PR1414 *100K_1%_2 VCCIN_AUX_VID1
PR1416 *100K_1%_2
PR1417 *100K_1%_2

DNS siince P/H on EE side

C-[10/25]
OCP~45A@LMOS=3.5m

PR1418 274K_1%_2

PU1039 RT6543BGQW

1	CS_DIS	RT6543_CS_DSI	PR1418 274K_1%_2
4	PGOOD	RT6543_PG	PR1423 *Short_0201
15	PVCC	RT6543_VCC	PR1421 5.1_1%_6
16	VCC		PC1773 1u/6.3V_4
17	VID1	RT6543_VID1	PR1424 *Short_0201
18	VID0	RT6543_VID0	PR1425 *Short_0201
19	EN	RT6543_EN	PR1426 *10K_1%_4
9	FSWSEL	RT6543_FSWSEL	PR1434 *100K_1%_4
20	VSYS	RT6543_VSYS	PC1774 0.1u/25V_4
11	UGATE	RT6543_UG	PR1419 1_5%_6
10	BOOT	RT6543_BOOT	PC1779 0.1u/25V_4
12	PH	RT6543_PH	
13	LGATE	RT6543_LG	
14	PGND		
2	ISENSEP	RT6543_ISP	PR1427 *0_5%_4
3	ISENSEN	RT6543_ISN	
8	VOUT	RT6543_VOUT	
5	COMP	RT6543_COMP	PC1792 2200p/50V_4 + PR1431 10K_1%_4 + PC1793 *470p/50V_4 + PR1432 *1.4K_1%_4 + PC1794 27p/50V_4
6	FB	RT6543_FB	PR1436 6.34K_1%_4
7	RGND	RT6543_RGND	PC1795 *0.1u/25V_4
21	AGND		

+5V_S5 PR1421 5.1_1%_6
+3V_S5 PR1481 10K_1%_2
+3V PR1420 *10K_1%_2
[86,124] VCCIN_AUX_PG
R-[2/26]
[13,16] VCCIN_AUX_VID1
[13,16] VCCIN_AUX_VID0
[21,22,86,113,114,123,146] SUSON
R-[2/26]
[86,123] HWPG_1.8VS5
[86,113,114,123,124] MAINON
PC1791 *0.1u/16V_4
PR1435 *100K_1%_4

PR1415 2.2_5%_6

PC1775 10u/25V_6
PC1770 10u/25V_6
PC1771 10u/25V_6
PC1776 10u/25V_6
PC1777 0.1u/25V_4
PC1772 2200p/50V_4
PC1778 0.1u/25V_4

+VIN_VCCIN_AUX
R-[2/26]
+VIN
PJ1009 *short3720

VAUX total BOM with EE:
a. 1pcs 330uF/6m
b. 18pcs 22uF/0603 MLCC includ EE side
c. Reserve 4pcs 22uF/6.3V MLCC

C-[10/25]
Modification of AOS supply requirements

Isat=41A
DCR=2.1m-ohm+/-7%

PQ1005 AONY36354
PR1422 *2.2_5%_6
PC1786 *2200p/25V_2
PR1429 *Short_0402
LMOS(max)=3.5m

PL1034 0.22uH/23A_7x7x3
PR1479 *Short_0201
PR1478 *Short_0201
ISEN1N_VCCAUX
ISEN1P_VCCAUX

PC1780 0.1u/16V_4
PC1783 22u/6.3V_6
PC1781 22u/6.3V_6
PC1787 22u/6.3V_6
PC1789 22u/6.3V_6
PC1784 *22u/6.3V_6
PC1788 *22u/6.3V_6
PC1785 *22u/6.3V_6
PC1790 *22u/6.3V_6
PC1782 330u/2.5V_7343H1.9

+VCCIN_AUX
PR1433 100_1%_2
PR1437 *Short_0201 VCC_AUX_SENSE [13]
PR1472 *Short_0201 VSS_AUX_SENSE [13]
R-[2/26]
PR1473 100_1%_2

PR1476 9.09K_1%_4
ISEN1P_VCCAUX
ISEN1P_VCCAUX [141]
PR1470 *Short_0201
PC1800 *0.01u/50V_4
PC1799 0.22u/10V_4
PR1480 357_1%_4
PR1477 909_1%_4
PR1471 10K_NTC_4_1%
PR1469 *Short_0201
ISEN1N_VCCAUX
ISEN1N_VCCAUX [141]

ADL-H45 (45W) Performance 1 Φ

+VCCIN_AUX
IPL2:18A
ICCMAX:34A
OCP:45A
L/L=-2.0mV/A

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VO1 (4.6 Volt)
TDC : 0.98A
PEAK : 1.3A
Width : 40mil
FSW : 1.432MHZ

OLED ELVDD

VO2 (-4 Volt) (-8~-1)
TDC : 2.7A
PEAK : 3.6A
Width : 144mil
FSW : 1.145MHZ

OLED ELVSS

3201_LDO
+VIN
VO1
VO2

PC9825 OLE@1u/25V_4
PC9826 OLE@4.7u/25V_6
PC9827 OLE@22u/25V_8 cloase to Pin27/28/29 (VO2_S/3)

BC207M1QZ00
DIODE TVS
PE4207M1Q
(7.8V,21A,30KV)
SAM request: 6VClamp TVS Diode
PD9801 OLE@PE4207M1Q

PC9828 OLE@22u/25V_8
PC9829 OLE@22u/25V_8
PC9830 OLE@22u/25V_8

PL9802 OLE@2.2uH/3.2A_3.2x2.5x1.2
Isat=4A,DCR=70mohm
HMMQ32251B-2R2MS

PU9802
OLE@SM3201C

E-PAD PGND1#2 PGND1#1 VO1_FBS NC2 VLDO AVIN PGND2 VO2_S VO2_3#2 VO2_3#1
LX1#1 LX1#2 BST1 PVIN1#1 PVIN1#2 PVIN2 LX2_1 BST2_1
LX2_3#2 LX2_3#1 BST2_3 DRV3 DRV2 BST2_2 LX2_2#2 LX2_2#1
VO2_1 nEN2PH NC3 NC4 AGND SWIRE nFD NC1 VO2_2#1 VO2_2#2

PC9832 OLE@0.22u/25V_4
PC9838 OLE@0.22u/25V_4

PL9804 OLE@4.7uH/1.5A_2.0x1.6x1.0
Isat=1.9A,DCR=210mohm
HTTX20161T-4R7MDR
SAM request: ISAT 1.6A

PC9833 OLE@10u/25V_8
PC9834 OLE@10u/25V_8
PC9835 OLE@10u/25V_8
PC9836 OLE@10u/25V_8

floating
PR9829 OLE@0_5%_2
PR9830 OLE@0_5%_2
SWIRE_C

PC9843 OLE@22u/25V_8 cloase to Pin17/18 (VO2_2#1/#2)
PC9844 OLE@22u/25V_8 cloase to Pin9

SAM request: VR:30V, IF(ON):2.0A
PD9800 OLE@SDM2U30CSP-7
2nd source: NSR20F30NXT5G

PL9803 OLE@2.2uH/3.2A_3.2x2.5x1.2
Isat=4A,DCR=70mohm
HMMQ32251B-2R2MS
SAM request: IDC 4.3A

PC9831 OLE@0.22u/25V_4
PC9837 OLE@0.22u/25V_4

PQ9804
OLE@QH8K22TCR

PL9805 OLE@2.2uH/3.2A_3.2x2.5x1.2
Isat=4A,DCR=70mohm
HMMQ32251B-2R2MS

PC9839 OLE@10u/25V_8
PC9840 OLE@10u/25V_8
PC9841 OLE@10u/25V_8
PC9842 OLE@10u/25V_8

SAM request: VR:30V, IF(ON):2.0A
PD9802 OLE@SDM2U30CSP-7
2nd source: NSR20F30NXT5G

VO2
-4 Volt (-8~-1)
TDC : 3.6A
Width : 144mil
FSW : 1.145MHZ

OLED ELVSS

SWIRE_C PR9833 OLE@0_5%_2 SWIRE [45]

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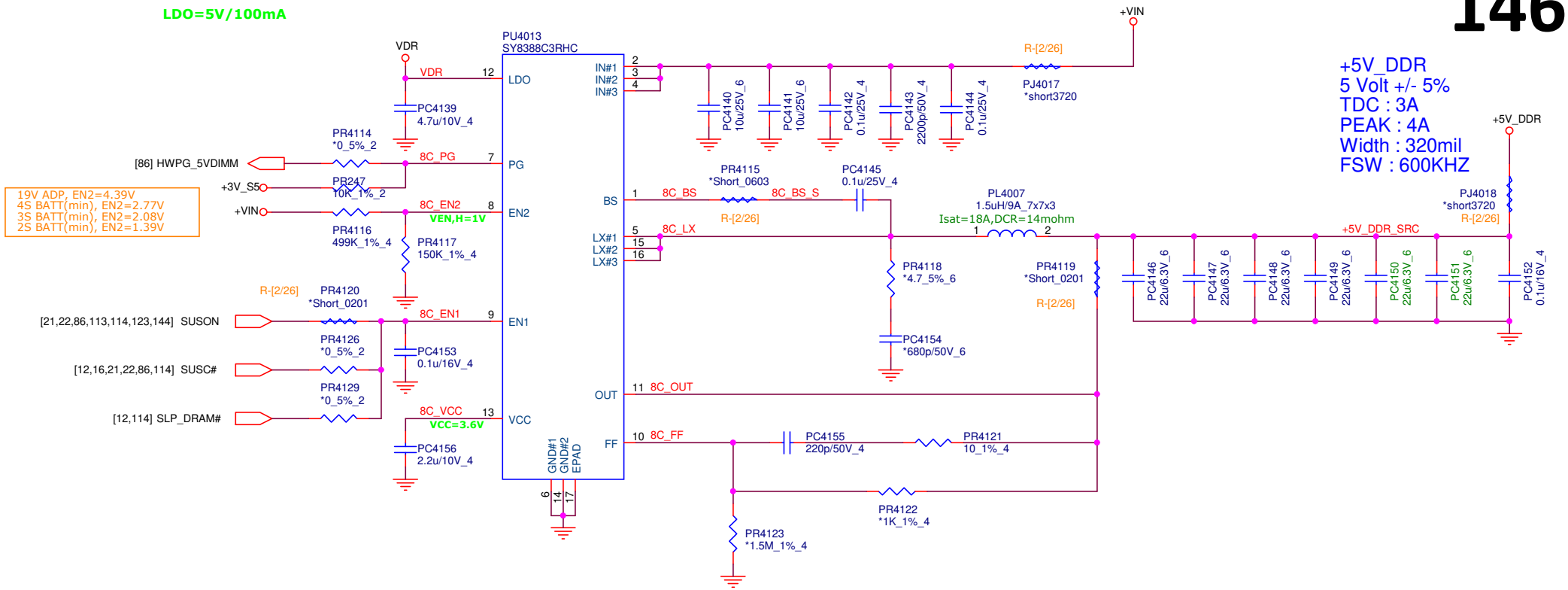
LDO=5V/100mA



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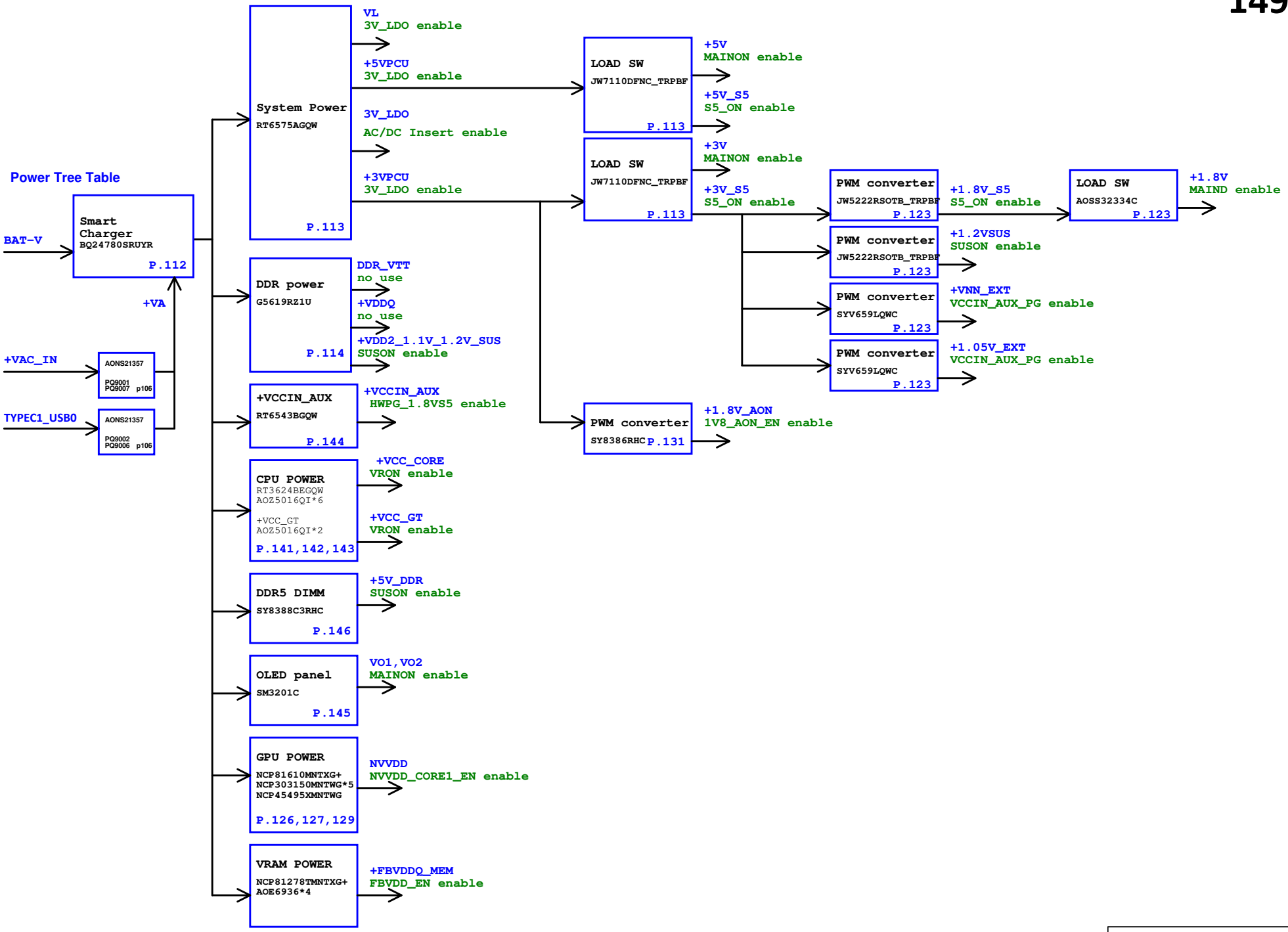
Power Tree Table



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HDMI-ADL

[2] IN_CLK — TTPP1
[2] IN_CLK# — TTPP4
[2] IN_D0 — TTPP7
[2] IN_D0# — TTPP10
[2] IN_D1 — TTPP13
[2] IN_D1# — TTPP15
[2] IN_D2 — TTPP18
[2] IN_D2# — TTPP20
[2] DPB_DDCCLK — TTPP21
[2] DPB_DDCDATA — TTPP23
[2] HDMI_HPD_CON — TTPP125

DP-NV

[29] DP_D3# — TTPP27
[29] DP_D3 — TTPP30
[29] DP_D2# — TTPP33
[29] DP_D2 — TTPP36
[29] DP_D1# — TTPP39
[29] DP_D1 — TTPP42
[29] DP_D0# — TTPP45
[29] DP_D0 — TTPP48
[29] INT_DP_AUXN_Q — TTPP50
[29] INT_DP_AUXP_Q — TTPP53

Sensor

[10] TOF_RESET# — TTPP22
[6] 5GorAP_P_INT# — TTPP25
[45] LID#_DB — TTPP51
[45] LID#_GMR_DB — TTPP54
[91] ISH_TOF_INT#_R — TTPP106
[91] ISH_I2C1_SDA_R — TTPP107
[91] ISH_I2C1_SCL_R — TTPP108

TCP

[2] TCP2_TXRX_P1 — TTPP26
[2] TCP2_TXRX_N1 — TTPP29
[2] TCP2_TXRX_P0 — TTPP32
[2] TCP2_TXRX_N0 — TTPP35
[2] TCP2_TX_P1 — TTPP38
[2] TCP2_TX_N1 — TTPP41
[2] TCP2_TX_P0 — TTPP44
[2] TCP2_TX_N0 — TTPP47
[2] TCP2_AUX_DP — TTPP49
[2] TCP2_AUX_DN — TTPP52
[2] TBT_LSX2_TXD — TTPP112

EC

[86] ADP1_DET — TTPP115
[86] ADP2_DET — TTPP116
[86] VGPU_ICMNT — TTPP117
[86] battery_learn — TTPP118
[86] SUSLED#_TP — TTPP119
[86] 80PORT_DAT — TTPP135

NFC

[6] NFC_SCL — TTPP56
[6] NFC_SDA — TTPP58
[11] NFC_IRQ — TTPP60
[9] NFC_RST# — TTPP63

PCIE

[10] PCIE_TXP12/SATA1_TXP — TTPP64
[10] PCIE_TXN12/SATA1_TXN — TTPP65
[10] PCIE_RXP12/SATA1_RXP — TTPP67
[10] PCIE_RXN12/SATA1RXN — TTPP69
[10] PCIE_TXP10 — TTPP76
[10] PCIE_TXN10 — TTPP78
[10] PCIE_RXP10 — TTPP79
[10] PCIE_RXN10 — TTPP80
[10] PCIE_TXP8 — TTPP82
[10] PCIE_TXN8 — TTPP84
[10] PCIE_RXP8 — TTPP86
[10] PCIE_RXN8 — TTPP88
[10] PCIE_TXP7 — TTPP90
[10] PCIE_TXN7 — TTPP92
[10] PCIE_RXP7 — TTPP93
[10] PCIE_RXN7 — TTPP94
[10] PCIE_TXP6 — TTPP96
[10] PCIE_TXN6 — TTPP98
[10] PCIE_RXP6 — TTPP99
[10] PCIE_RXN6 — TTPP100
[10] PCIE_TXP5 — TTPP102
[10] PCIE_TXN5 — TTPP103
[10] PCIE_RXP5 — TTPP104
[10] PCIE_RXN5 — TTPP105

MIPICCD

[15] MIPICCD_DET# — TTPP121
[6] MIPICCD_EN — TTPP122
[11] MIPI_CSI_DP1 — TTPP126
[11] MIPI_CSI_DN1 — TTPP127
[11] MIPI_CSI_DP0 — TTPP128
[11] MIPI_CSI_DN0 — TTPP129
[11] MIPI_CSI_CLKP — TTPP130
[11] MIPI_CSI_CLKN — TTPP131
[12] MIPI_PWR_MS# — TTPP132
[6] MIPICCD_I2C_SCL — TTPP133
[6] MIPICCD_I2C_SDA — TTPP134

5G

[9] GPS_DISABLE# — TTPP81
[2] WWAN_RST_EC_ODL — TTPP83
[11] 5G_CARD_PWR_EC — TTPP85
[2] WWAN_PERST_EC_L — TTPP87
[86] I2C_PSENSOR_A_INT#_EC — TTPP91
[10] 5G_CARD_PWR_CTL — TTPP113
[11] WWAN_WAKE_ODL — TTPP114
[12] WWAN_RF_DISABLE_ODL — TTPP136

Intel LAN

[12] SLP_LAN# — TTPP137

Smart Card

[12] SmartCard_PWRSV# — TTPP75
[9] SmartCard_ON — TTPP77

CLK

[11] CLK_PCIE_SSD2P — TTPP8
[11] CLK_PCIE_SSD2N — TTPP11
[11] PCIE_CLKREQ_2# — TTPP16

AML

[86] AML_EC_PCH_CLK — TTPP139
[86] AML_EC_PCH_DATA — TTPP141

Debug Card

[86] 80PORT_CLK — TTPP97

Panel

[6] Privacy_EN — TTPP101

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