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IH11K-MHS VER 6.0

CPU:

Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:

SPT-H PCH

Main Memory:

Dual Channel/DDR-III*2(Max 16GB) 1066/1333/1600

Onboard Device:

Super I/O:IT8613E
LAN:Realtek 8111H
HD Codec:ALC887

Power solution:

CPU Voltage Regulators:3phase by RT3606 high 1 Low 1 OV by RT3606
DDR Voltage Regulators:1Phase by UP1514 high 1 Low 1 OV by IT8613E

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT *2

REAR IO:

PS/2 PORT
DVI Port
VGA Port
USB3.0 PORT *2
Gb RJ-45 +2 layer USB3.0 Ports
Audio Jackets (3 PORT)

Front I/O:

SATA3 *6
USB 2.0 Header * 2 Serial header
USB 3.0 Header * 1 Front Audio Header
CPU FAN *1
System FAN *1

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Title: INDEX
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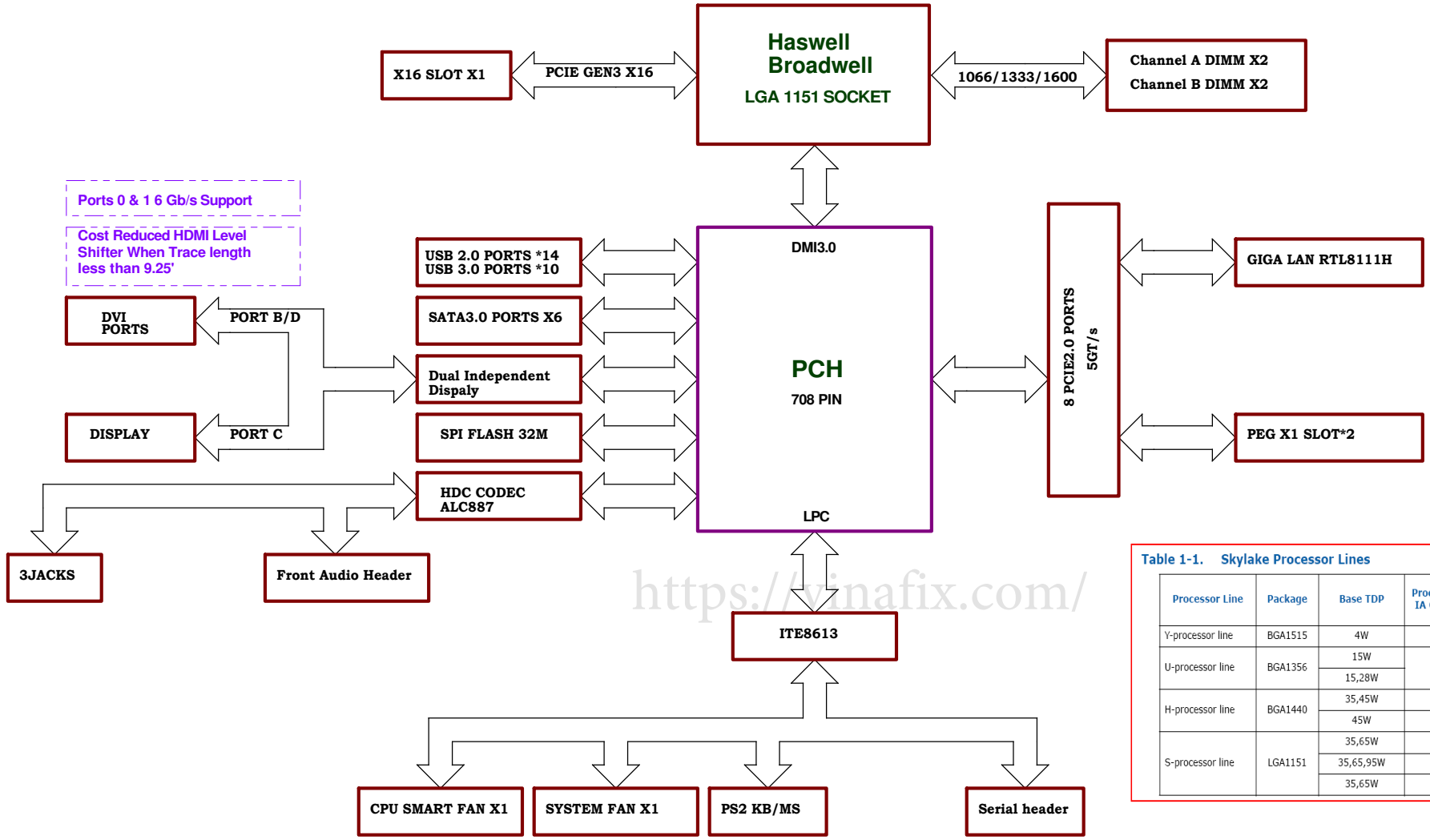

Table 1-1. Skylake Processor Lines

Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2		1-Chip
		15,28W		GT3	64 MB	
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	

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Title: BLOCK DIAGRAM

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Title: POWER DELIVERY

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1.VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)

2.VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)

3.VER0.60:CHANGE CPU POWER CONN TO 2*2(PAGE39)

4.VER0.60:NEW ADD COLAY FOR V_SA_IO(PAGE38)

5.VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)

6.VER0.6:COST DOWN(REMOVE CT6)(PAGE26)

7.VER0.6:COST DOWN(MODIFY F6/GF3 SIZE)(PAGE21/34)

8.VER0.6:COST DOWN(MODIFY MC36 SIZE)(PAGE11)

9.VER0.6:COST DOWN(MCT2/3/CT11 CHANGE TO 560UF)(PAGE31/32)

10.VER0.6:COST DOWN(MC38 /NI)(PAGE11)

11.VER0.6:COST DOWN(YC23 /NI)(PAGE18)

12.VER0.6:COST DOWN(YC16/17/21 /NI)(PAGE18)

13.VER0.6:COST DOWN(LC18/MC5/6 CHANGE TO 10UF 0603 SIZE)(PAGE11/27)

14.VER0.6:COST DOWN(PC155 CHANGE TO 10UF 0603 SIZE)(PAGE39)

15.VER0.6:COST DOWN(C165/MC9 CHANGE TO 1UF 0805 SIZE)(PAGE31/38)

16.VER0.6:COST DOWN(YC11/26 /NI)(PAGE18)

17.VER0.6:COST DOWN(CHANGE TO RN 8P4R)(PAGE17)

18.VER0.6:ATXPG MODIFY(PAGE23/36)

19.VER0.6:COST DOWN(PAGE33)

20.VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904)(PAGE30/33/39)

21.VER0.6:COST DOWN(SHORT 0402)(PAGE8/11/12/16/19/23/33/39)

22.VER0.6:COST DOWN(SHORT 0805)(PAGE18/37/39/40)

23.VER0.6:COST DOWN(BEAD COLAY)(PAGE29)

24.VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606)(PAGE39/40/41)

25.VER0.6:COST DOWN(POWER_JUSB4/POWER_JUSB5 COLAY)(PAGE25/34)

26.VER0.6:MIC MODIFY BY KEVIN(PAGE28)

27.VER0.6:ACPI MODIFY BY KEVIN(PAGE30)

28.VER0.6:IO MODIFY BY KEVIN(PAGE23/27)

29.VER0.6:V_SA_IO MODIFY BY KEVIN(PAGE38)

30.VER0.65:PCIECLKRQ2# MODIFY(PAGE17)

31.VER0.65:PU1 core power change to +12V(PAGE39)

32.VER0.65:SET2_3606 MODIFY(PAGE39)

33.VER0.65:PWM FAE MODIFY(PAGE40/41)

34.VER0.65:IO MODIFY BY PETER(PAGE23)

35.VER0.65:DDR4_DRAMRST_N MODIFY BY PETER(PAGE11)

36.VER0.65:NEW ADD SATA CONN(PAGE14/24)

37.VER0.65:NEW ADD 100UF COLAY CAP(PAGE30/31/32)

38.VER6.0:NEW ADD 100UF AUDIO CAP(PAGE28)

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Title: CHANGELIST

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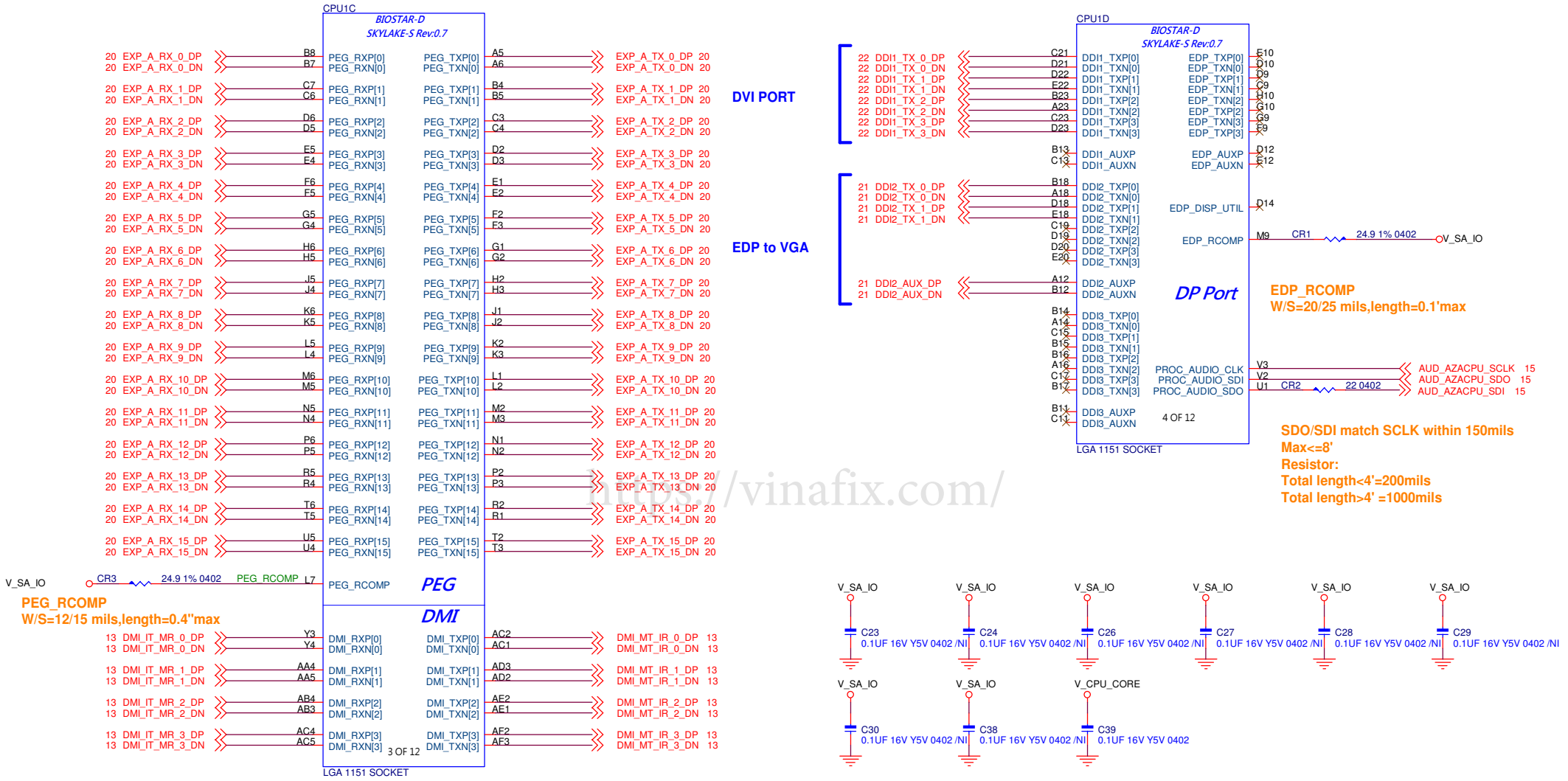

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Title	CPU PCIEX16/DMI/FDI	
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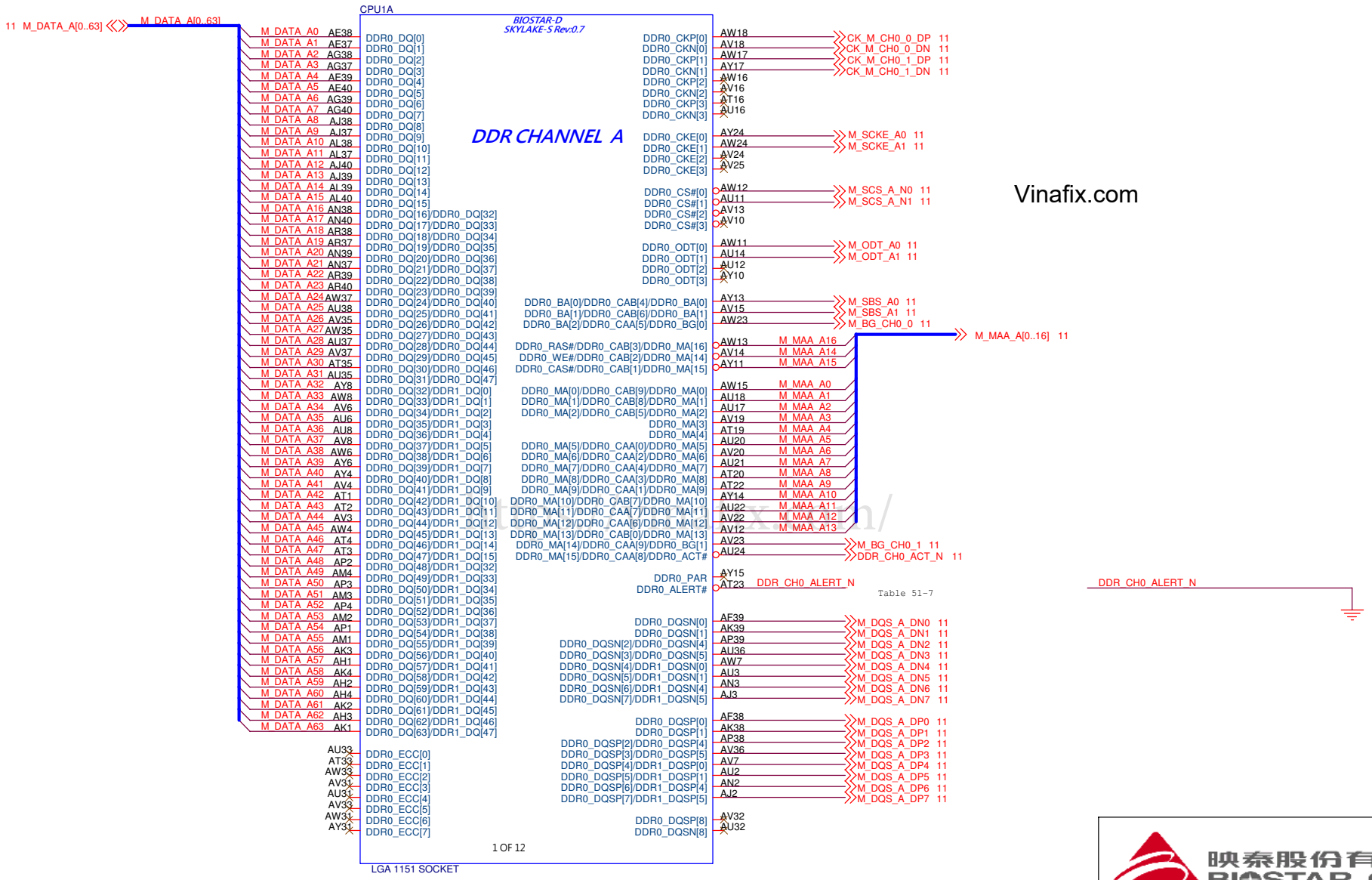
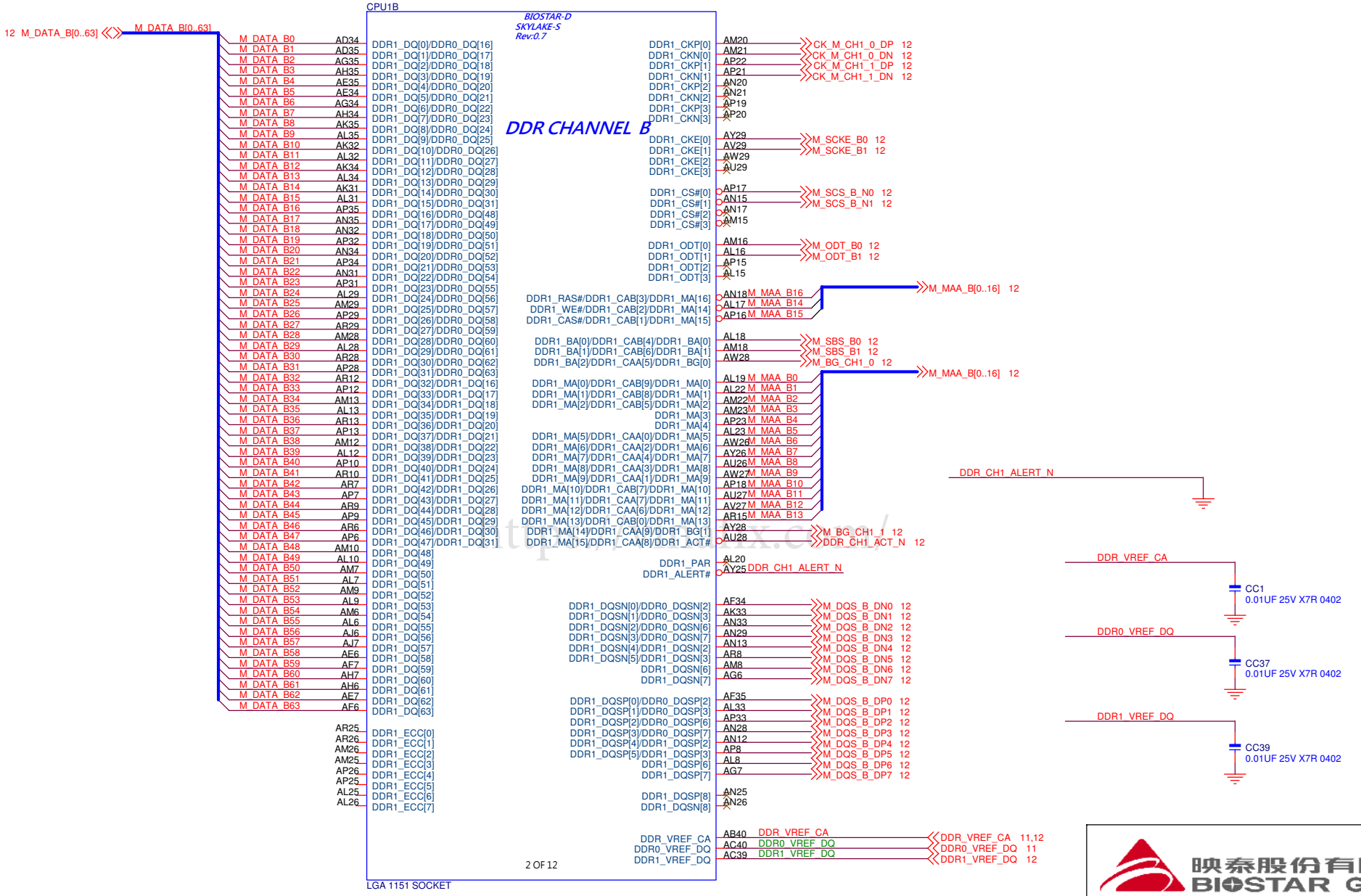


Title	CPU DDR3 CHANNEL A		
Size B	Document Number	IH11K-MHS	Rev 6.0
Date: Thursday, November 26, 2015	Sheet 6 of 42		



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Title	CPU DDR3 CHANNEL B	
Size B	Document Number IH11K-MHS	Rev 6.0
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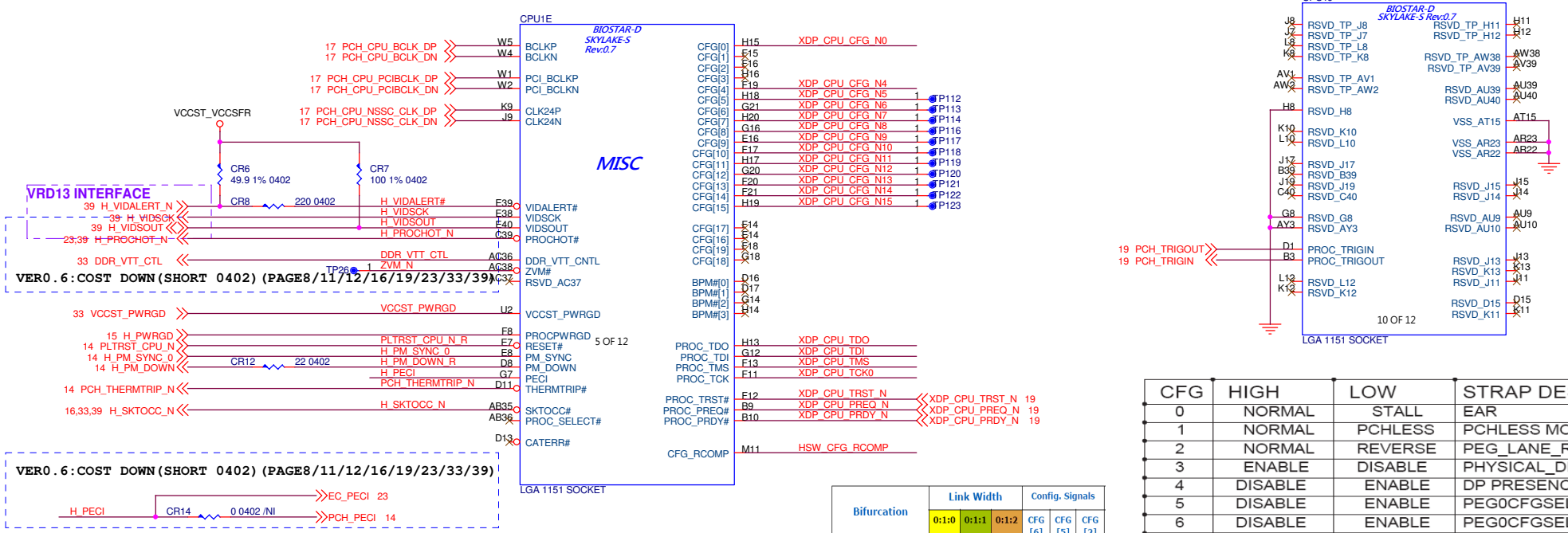
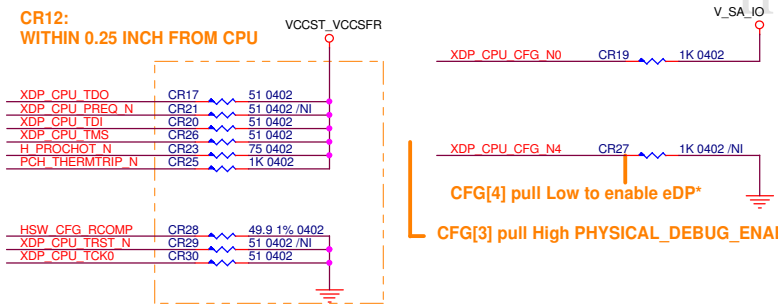
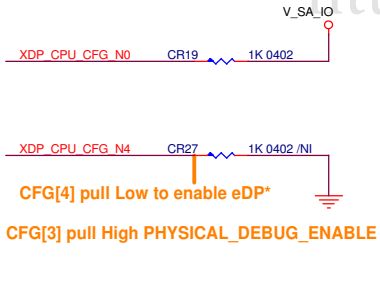
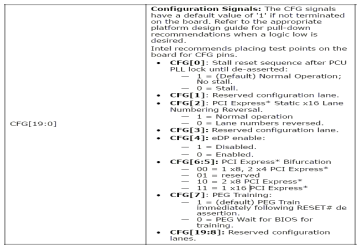






Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 **Reversed**	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 **Reversed**	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0



CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		
ALL PINS HAVE INTERNAL PULL-UPS			

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Title	CPU MISC	
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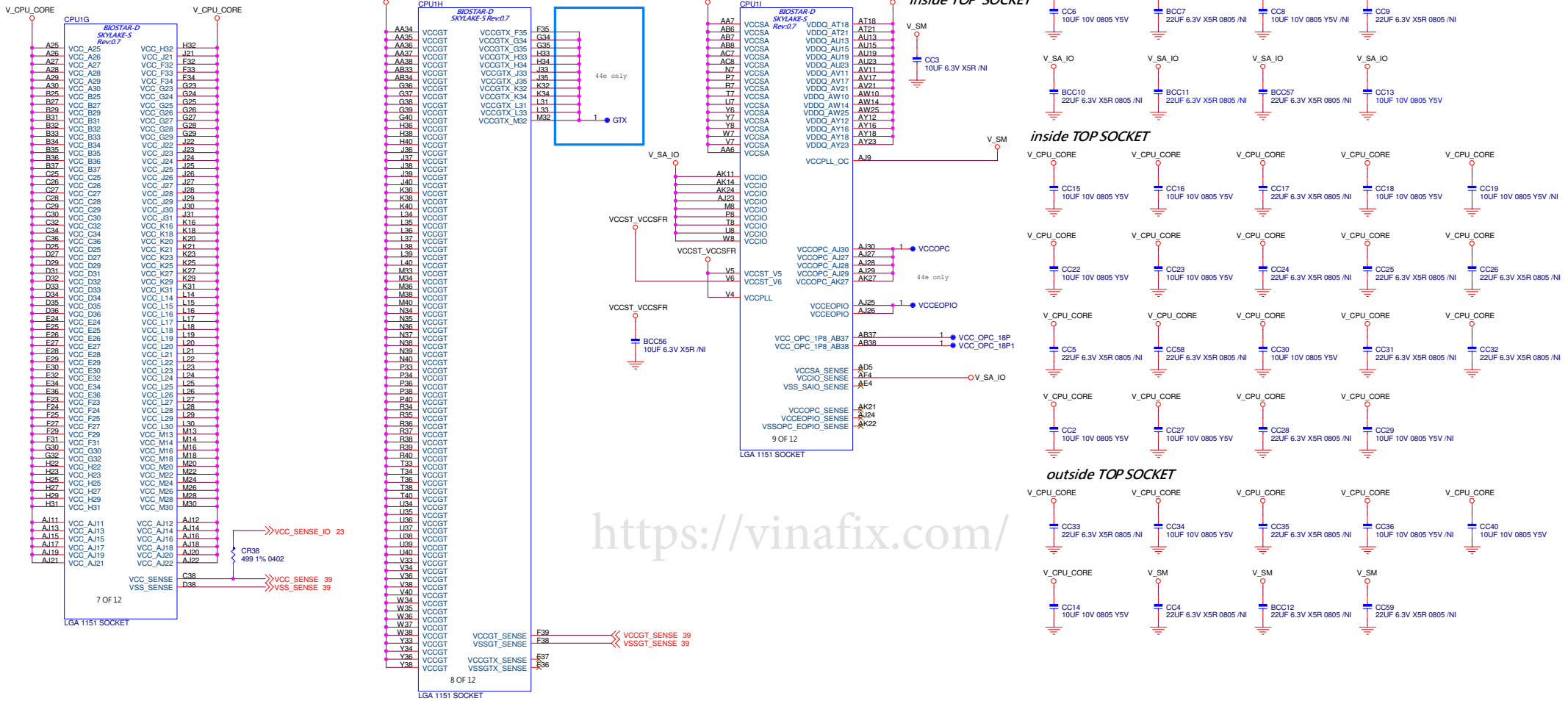

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Title: CPU POWER

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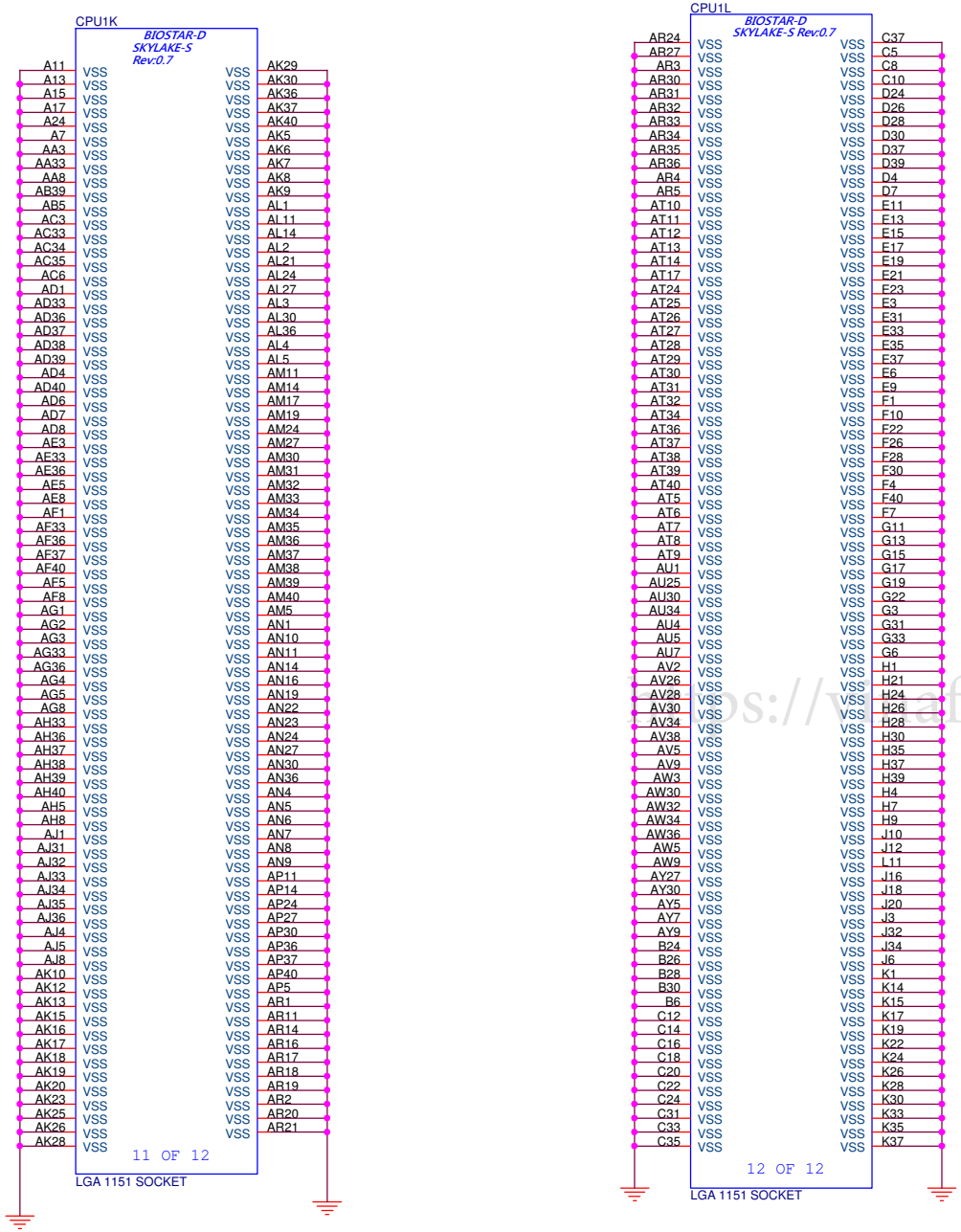

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Title: CPU GND

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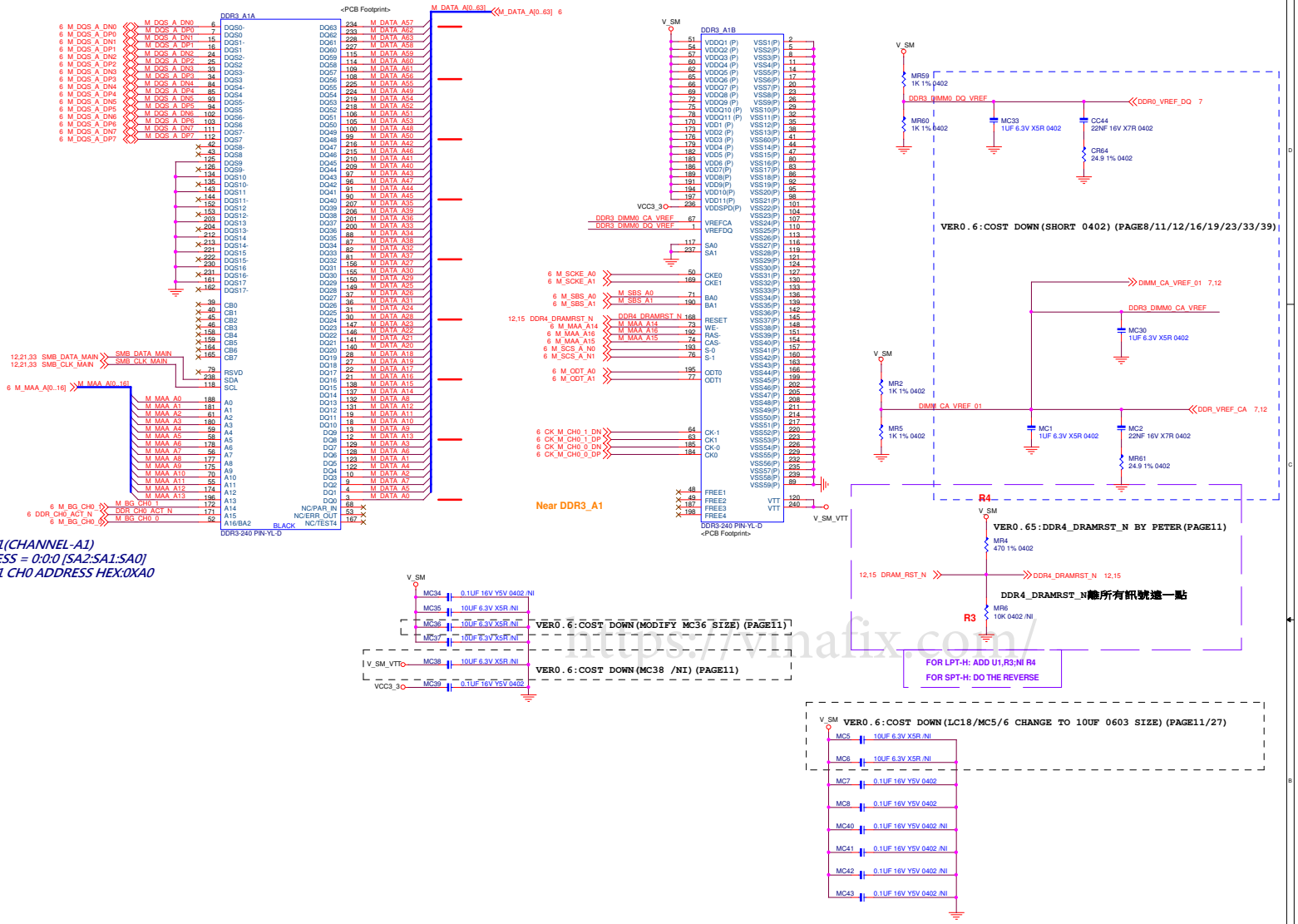

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Title	DDR3L DIMMA1		
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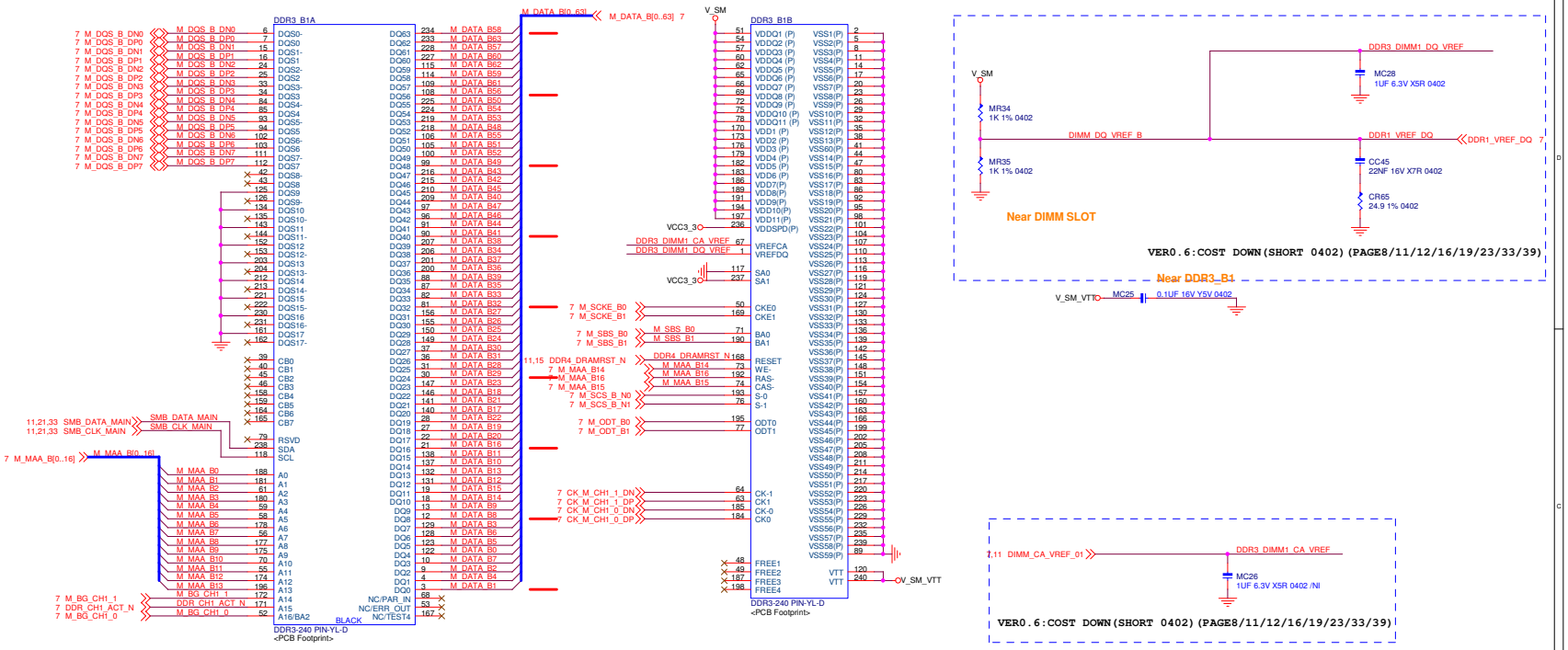

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Title: DDR3L DIMMB1

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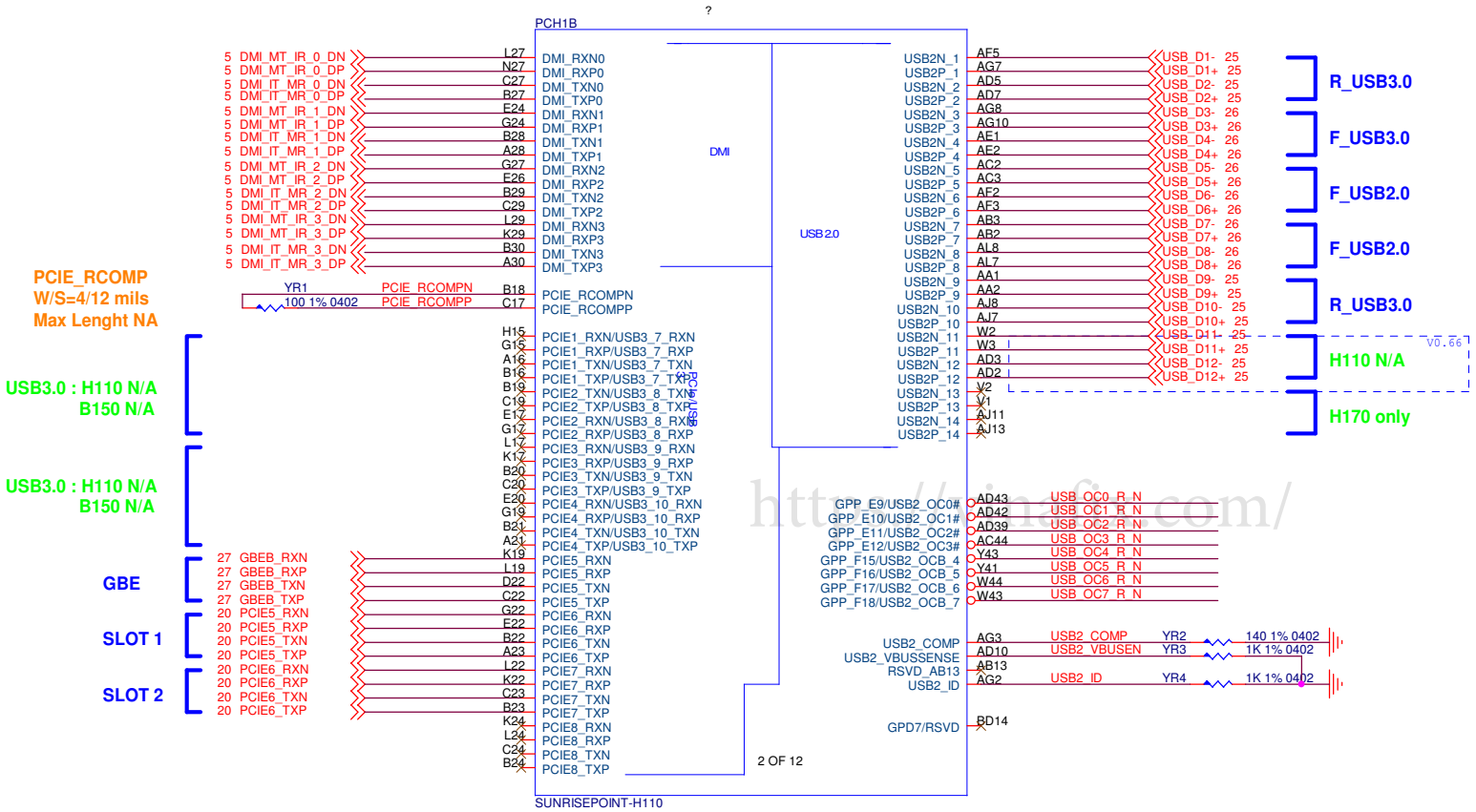
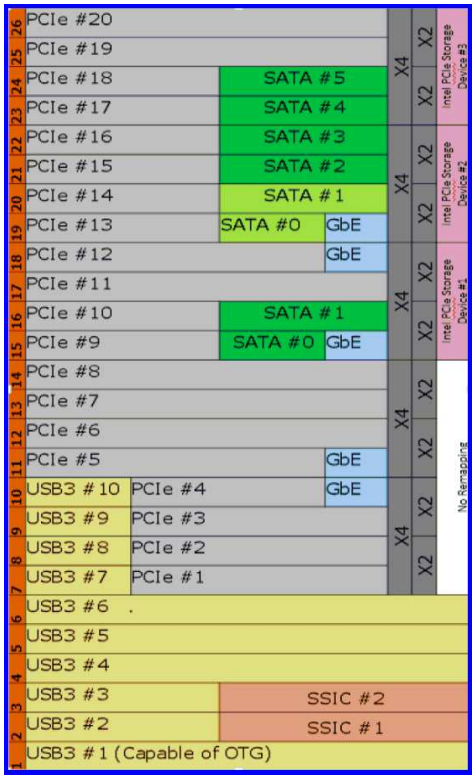
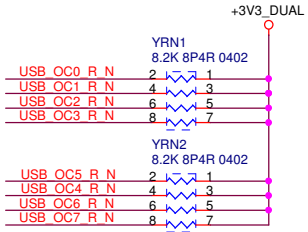
PCH PART: Y+Reference







Title	PCH DMI/PCIE/USB	
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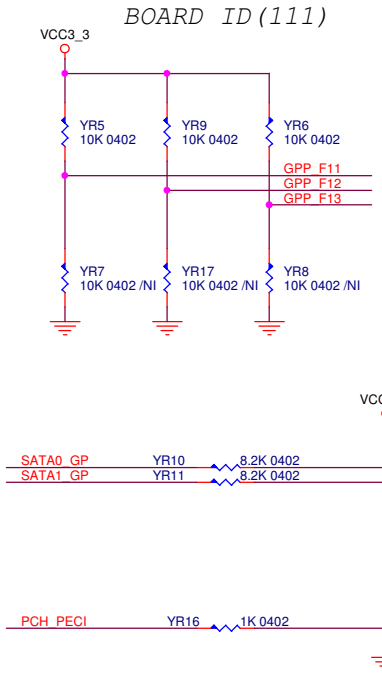
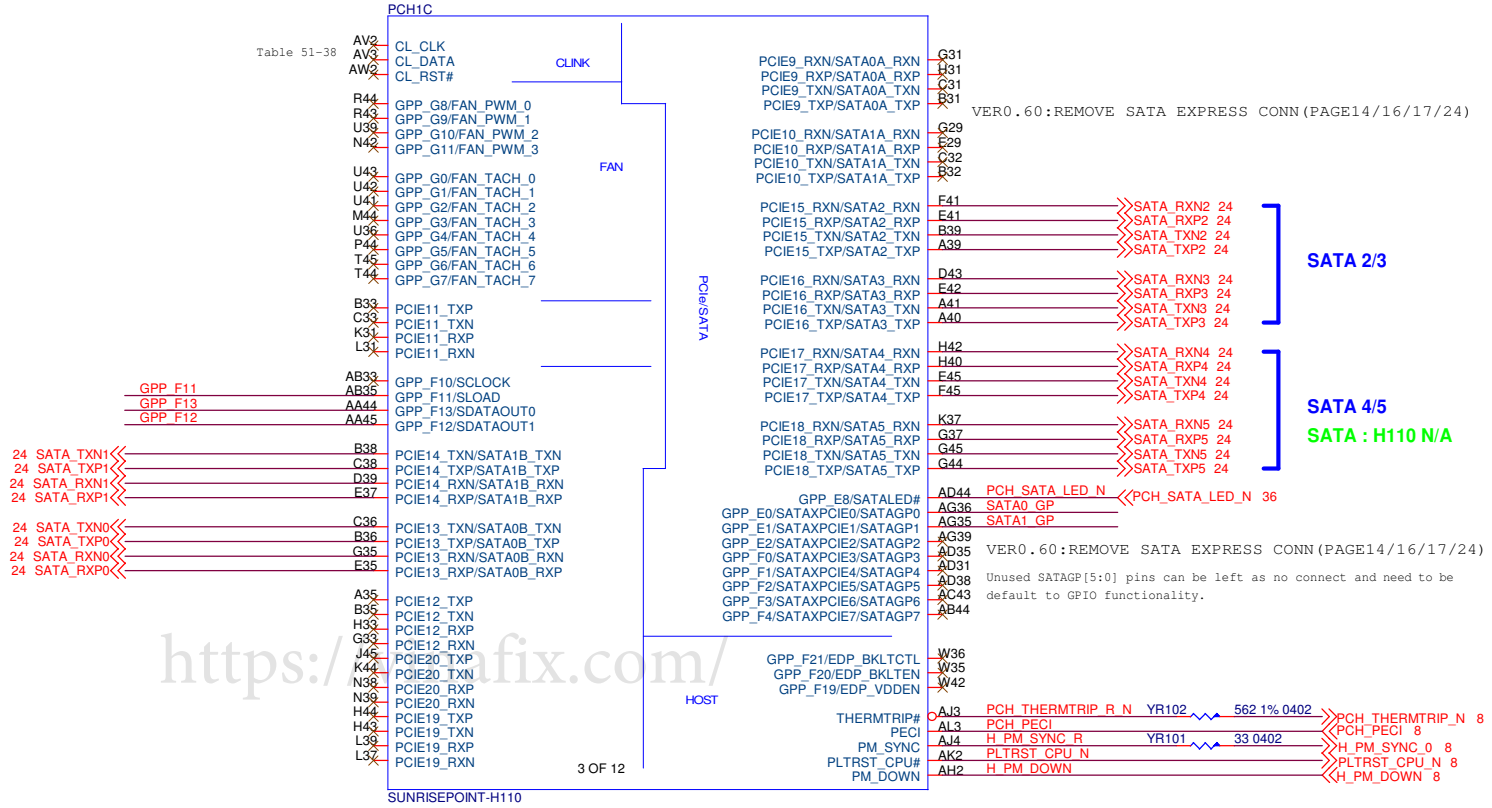
PCH PART: Y+Reference





GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

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Title	PCH CLINK/SATA/CPU HOST	
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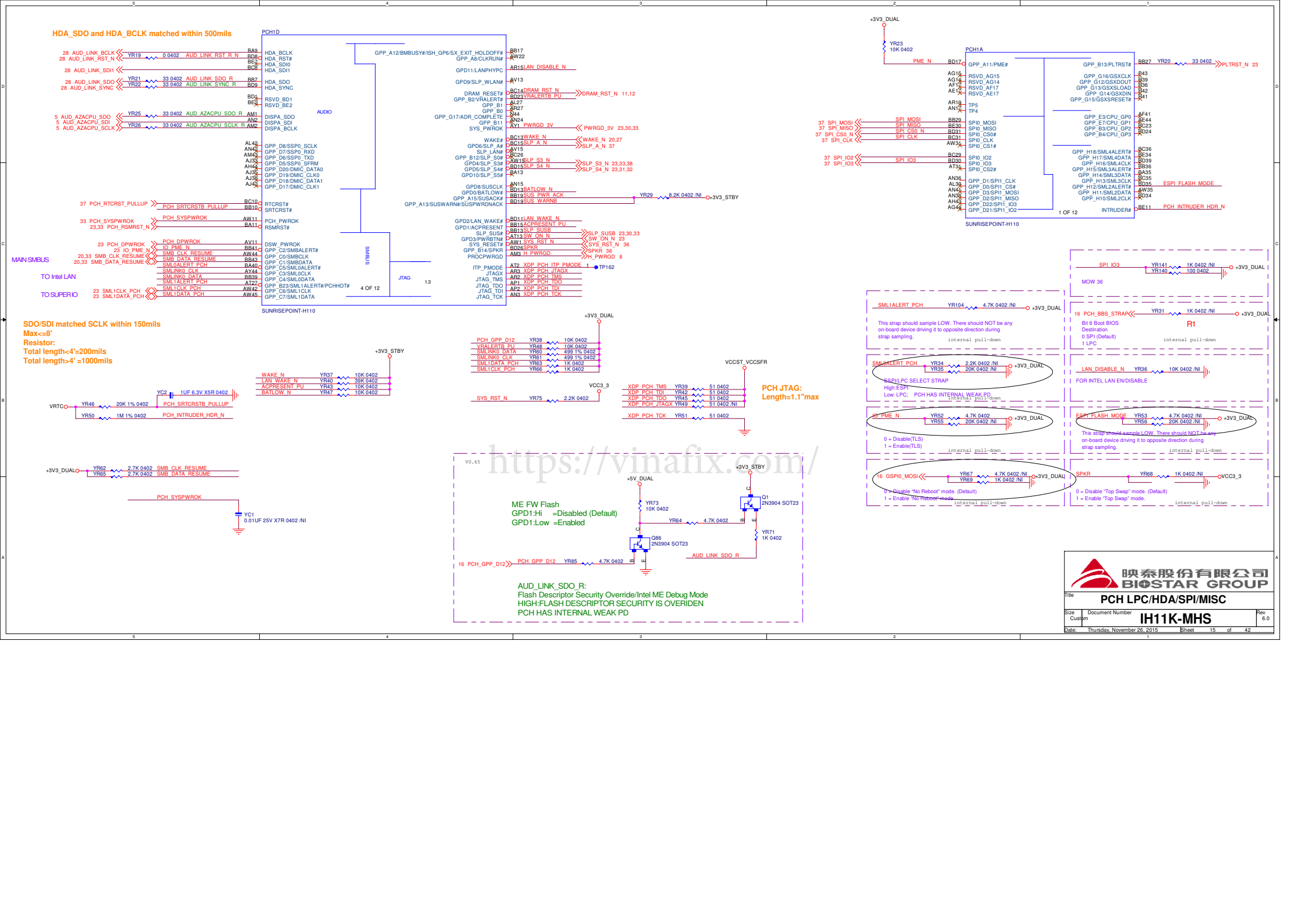
HDA_SDO and HDA_BCLK matched within 500mils
PCH1D
HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
RSVD_BD1
RSVD_BE2
AUDIO
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/SSP0_SCLK
GPP_D7/SSP0_RXD
GPP_D6/SSP0_TXD
GPP_D5/SSP0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
SMBUS
JTAG
4 OF 12
SUNRISEPOINT-H110
GPP_A12/BMBUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD8/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
PCH1A
GPP_A11/PME#
RSVD_AG15
RSVD_AG14
RSVD_AF17
RSVD_AE17
TP5
TP4
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
GPP_B13/PLTRST#
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
1 OF 12
SUNRISEPOINT-H110
MAIN SMBUS
TO Intel LAN
TO SUPERIO
SDO/SDI matched SCLK within 150mils
Max<=8'
Resistor:
Total length<4'=200mils
Total length>4' =1000mils
PCH JTAG:
Length=1.1"max
ME FW Flash
GPD1:Hi =Disabled (Default)
GPD1:Low =Enabled
AUD_LINK_SDO_R:
Flash Descriptor Security Override/Intel ME Debug Mode
HIGH:FLASH DESCRIPTOR SECURITY IS OVERIDEN
PCH HAS INTERNAL WEAK PD
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
ESPI/LPC SELECT STRAP
High:ESPI
Low: LPC; PCH HAS INTERNAL WEAK PD
0 = Disable(TLS)
1 = Enable(TLS)
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC
FOR INTEL LAN EN/DISABLE
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.
MOW 36
R1
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BIOSTAR GROUP
PCH LPC/HDA/SPI/MISC
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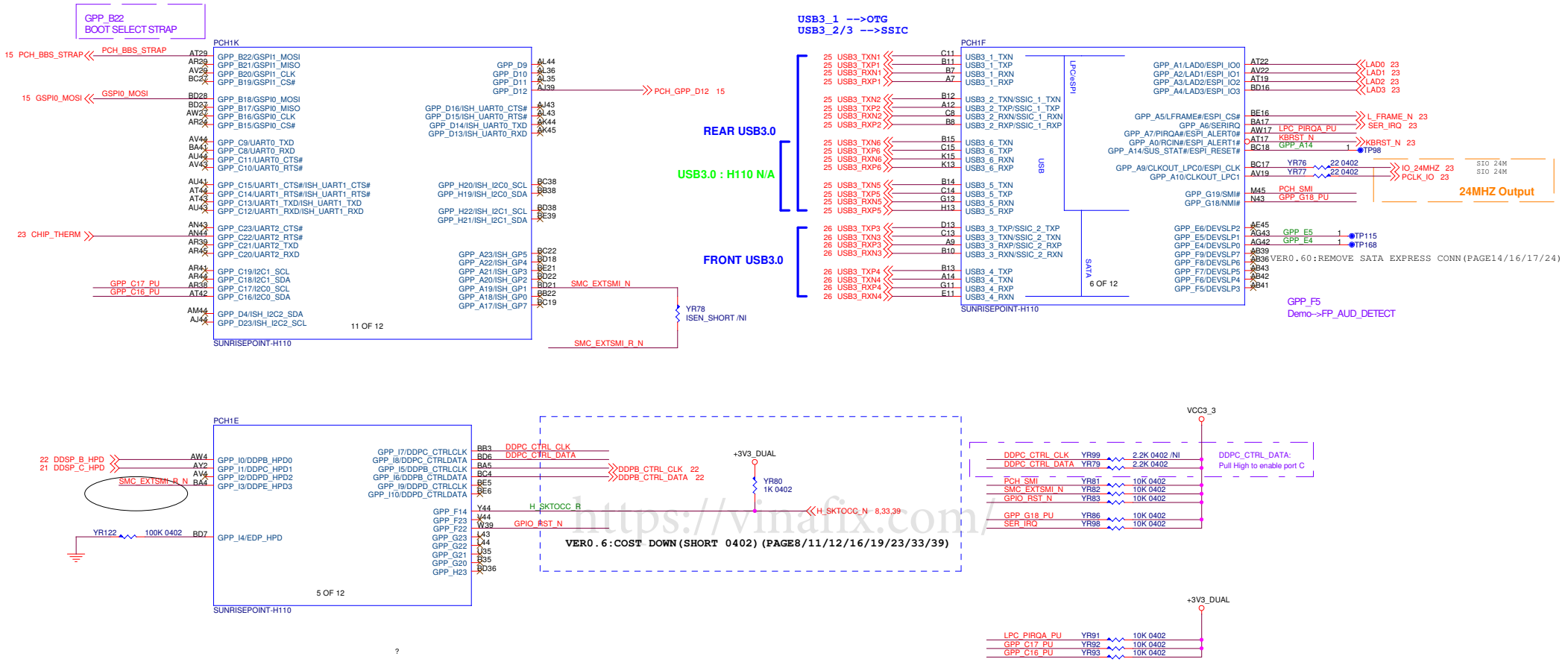
PCH PART: Y+Reference



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Title	PCH LPC/DP/USB3/UART
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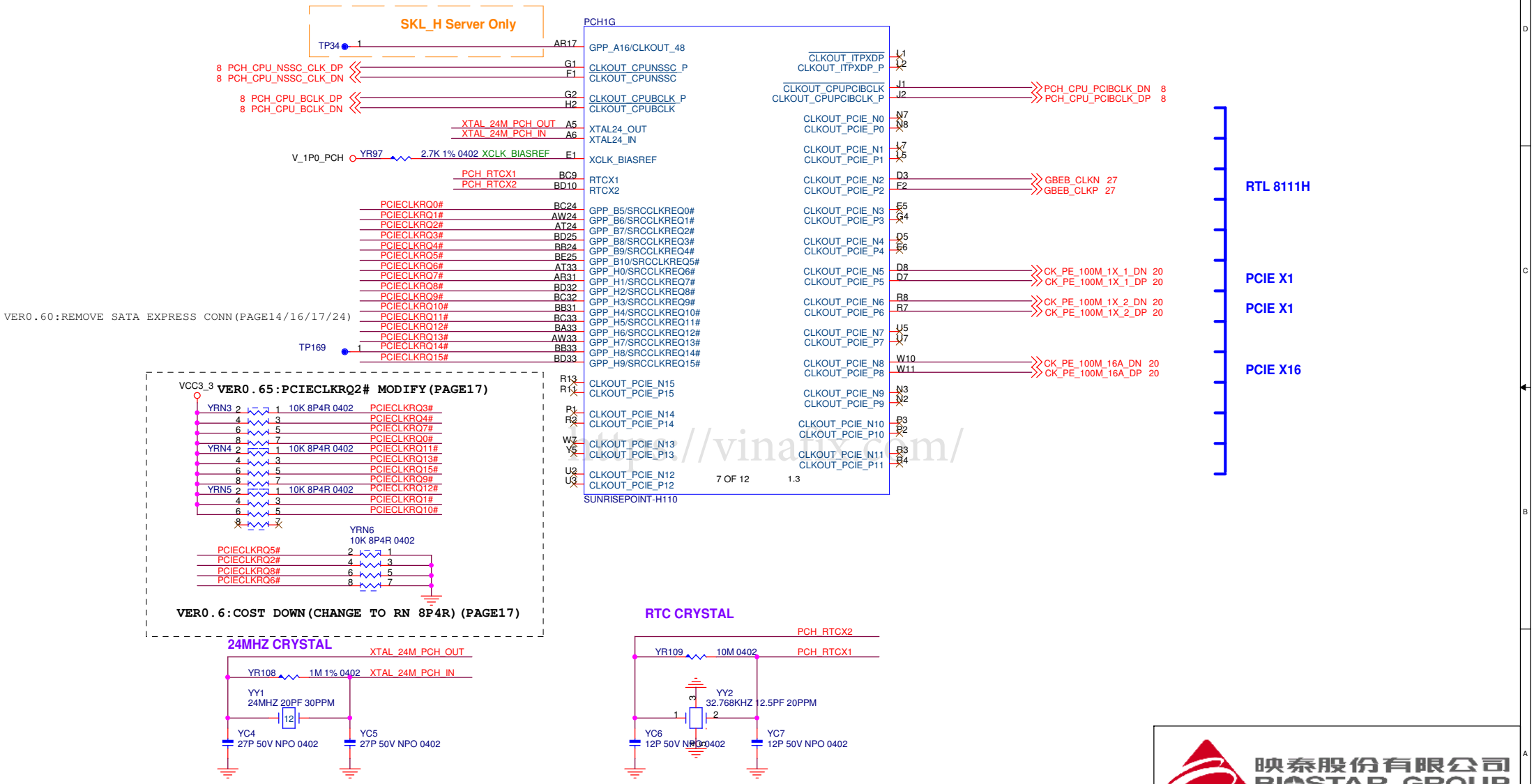

Title	PCH CLOCK BUFFER	
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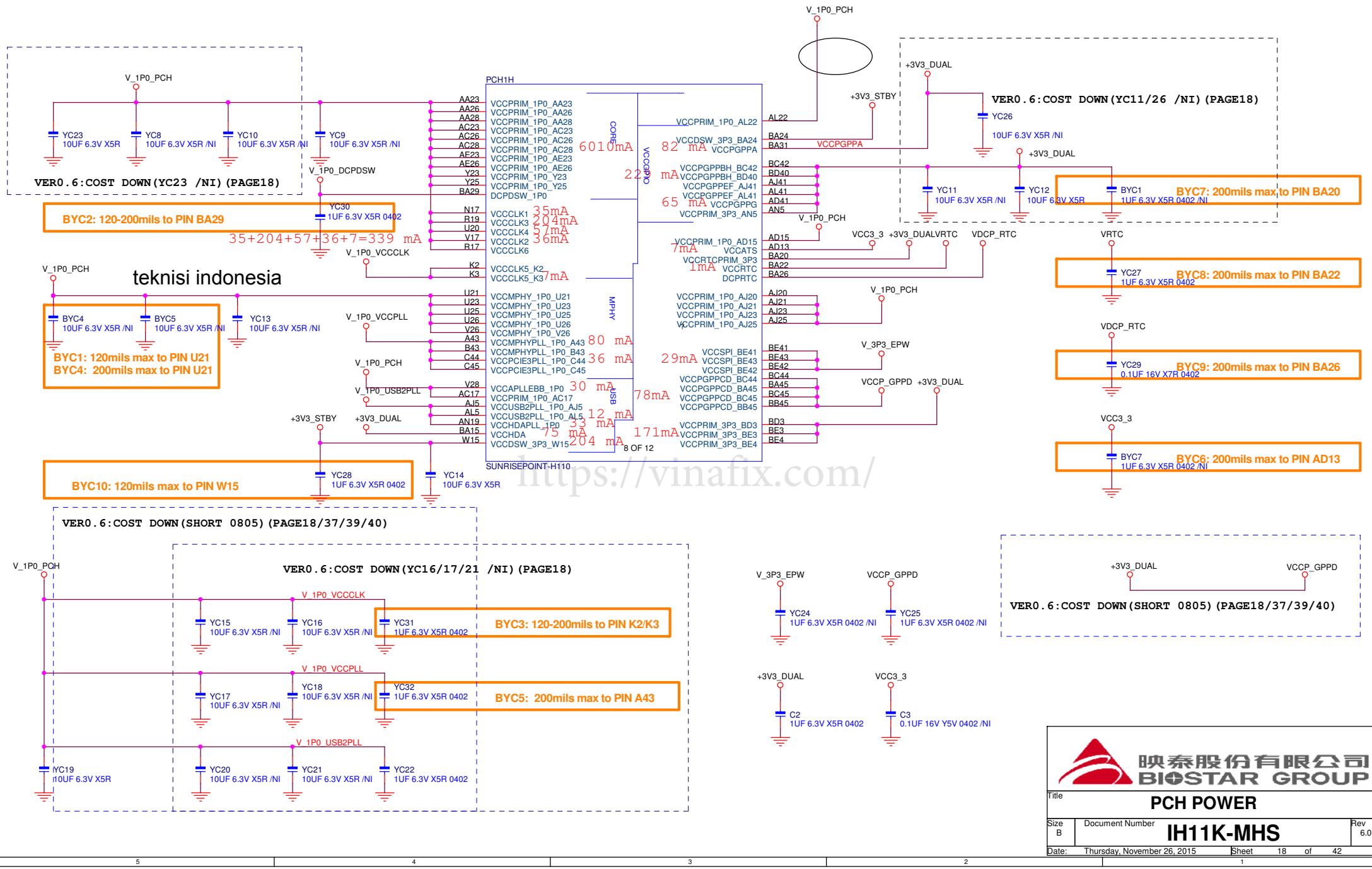

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Title	PCH POWER	
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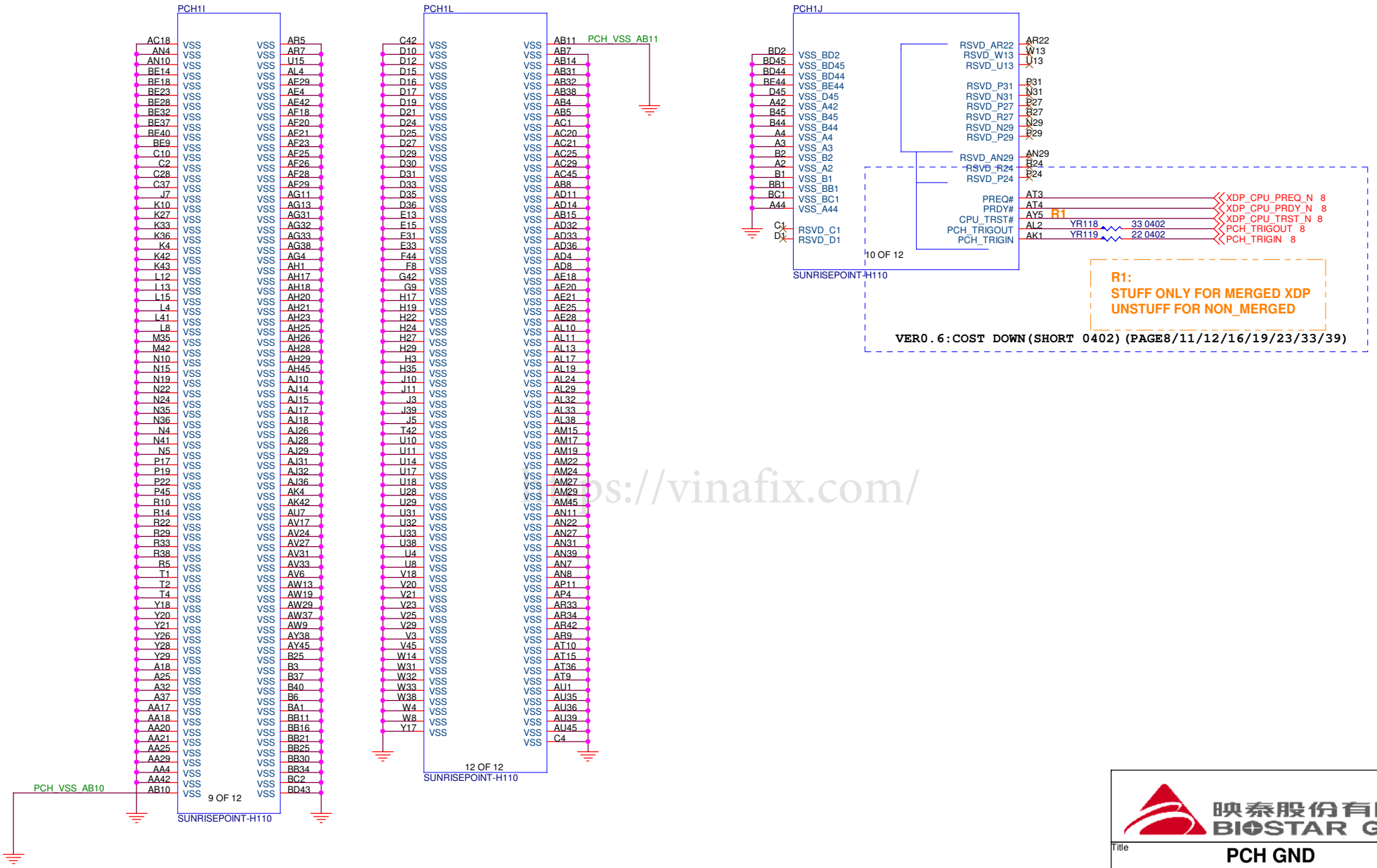

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BIOSTAR GROUP

Title	PCH GND	
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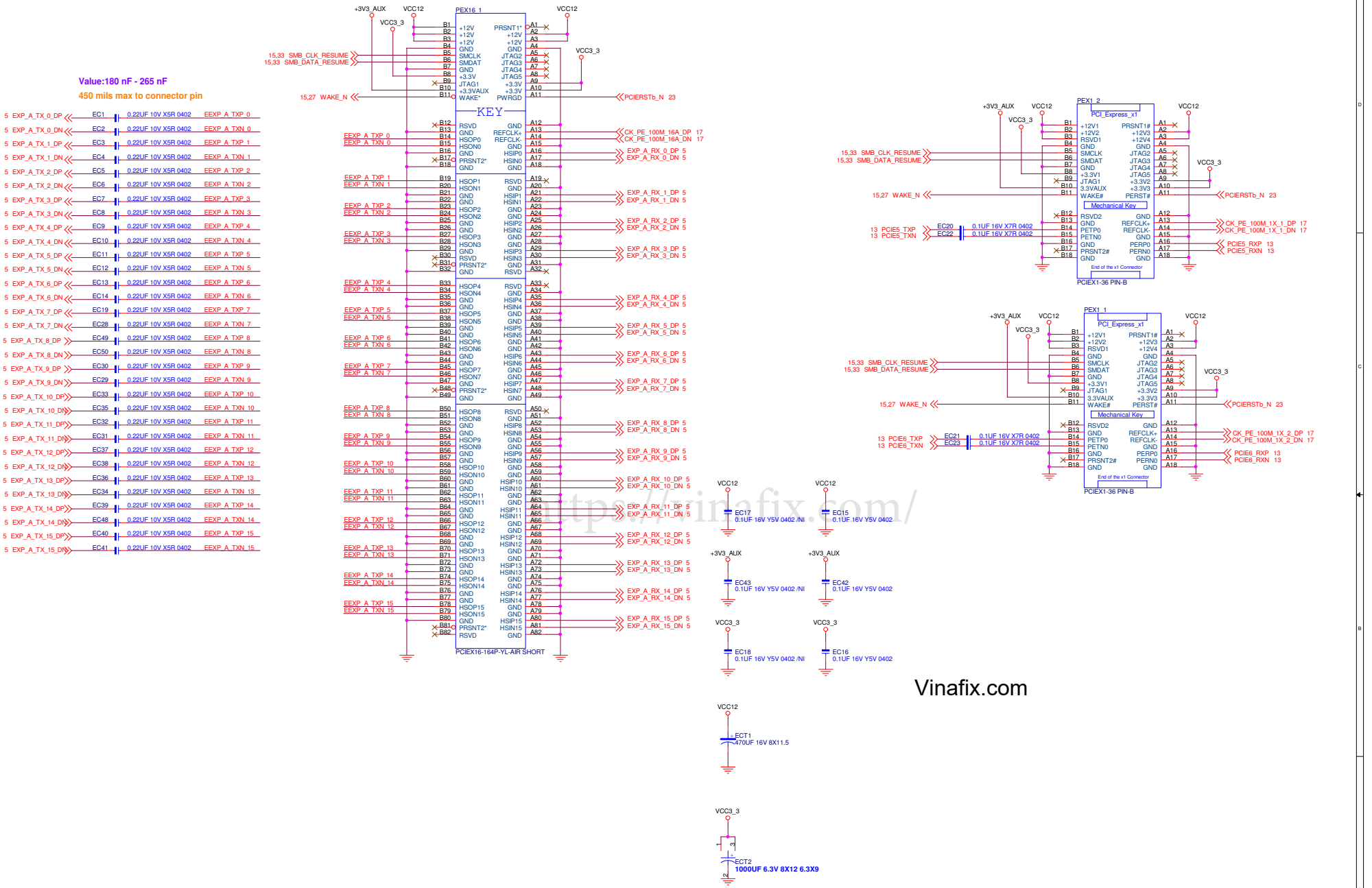
SLOT PART: E+Reference



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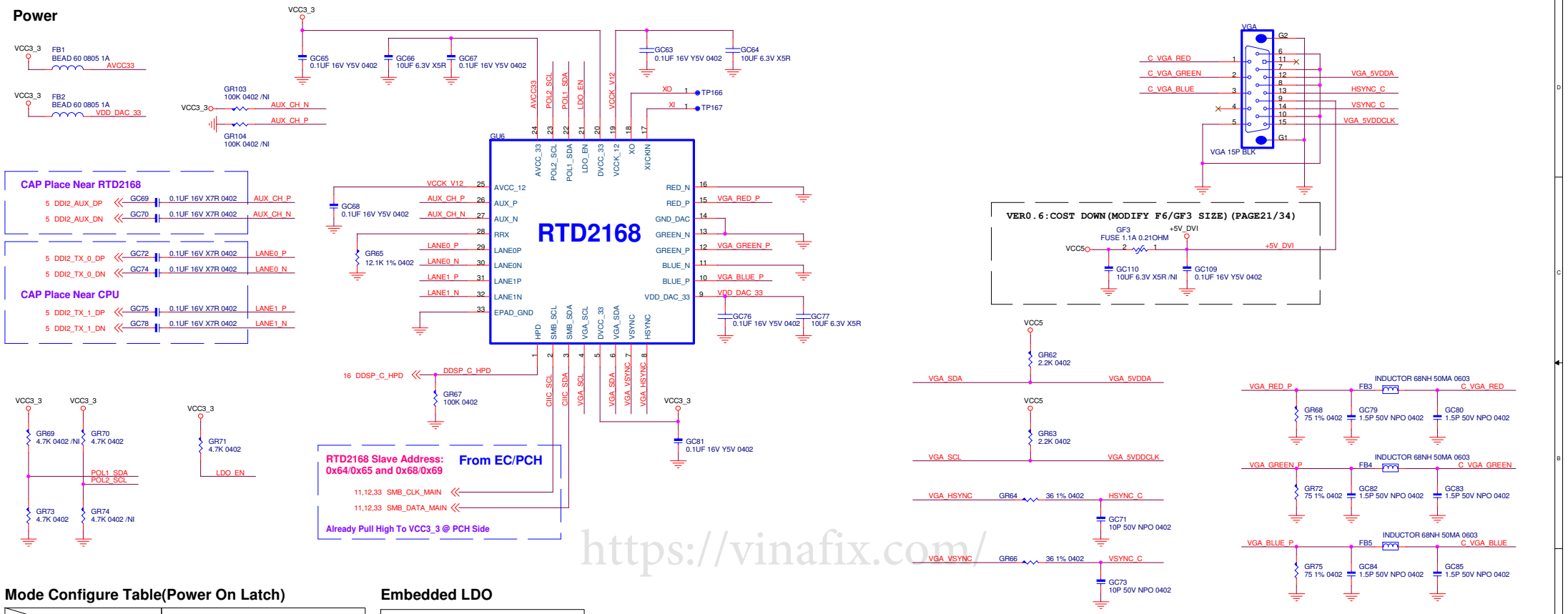
Title: PCIEX16 SLOT 1 & 2

Size: C | Document Number: IH11K-MHS | Rev: 6.0

Date: Thursday, November 26, 2015 | Sheet 20 of 42



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	**EEPROM MODE**

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	**VCCK_V12 from Embedded LDO**

Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW

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Title: **RTD2168 EDP to VGA**

Size: Custom | Document Number: **IH11K-MHS** | Rev: 6.0

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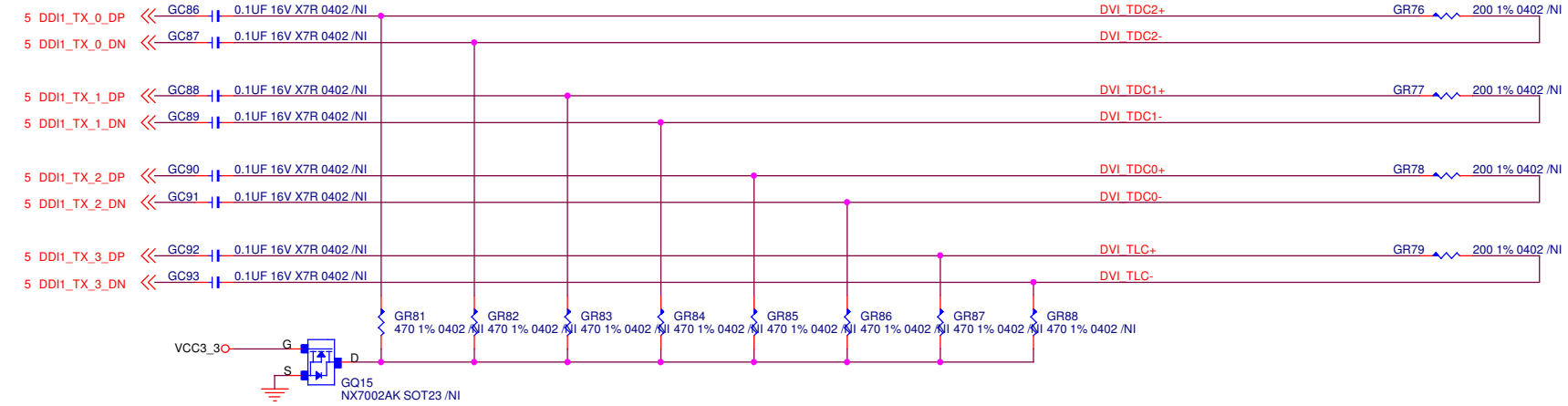

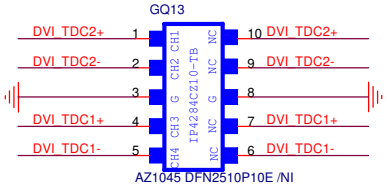

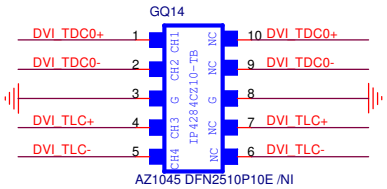

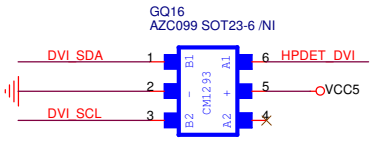

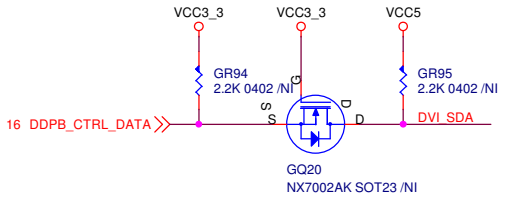

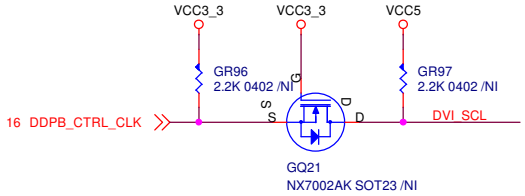

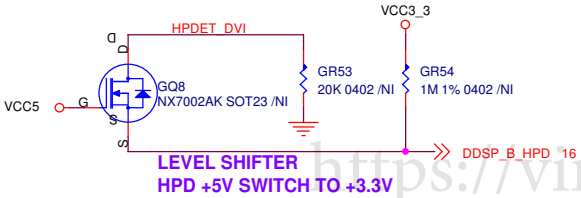

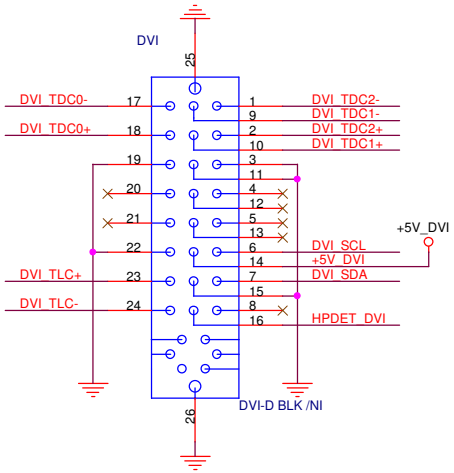

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BIOSTAR GROUP

Title: DVI-I CONNECTOR

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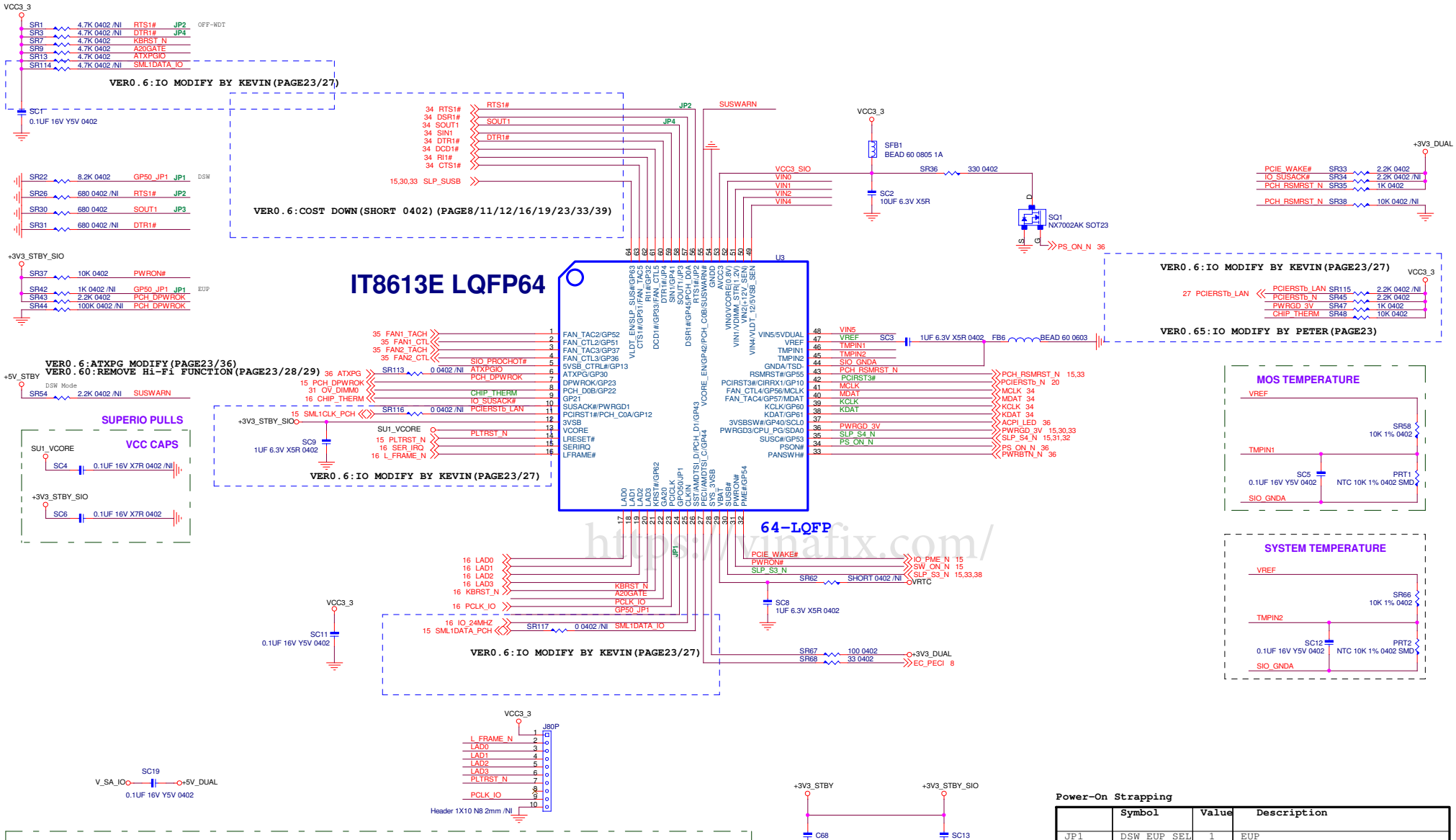

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-24		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-56		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin-58		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-60		0	Enable K8 Power Sequence

Title	SIO IT8613E		
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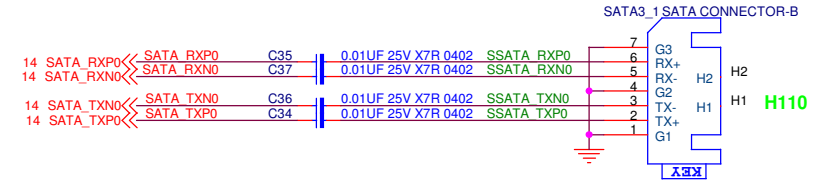

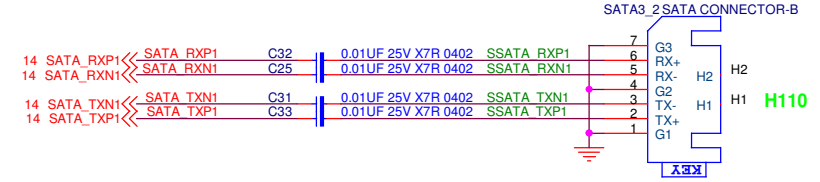

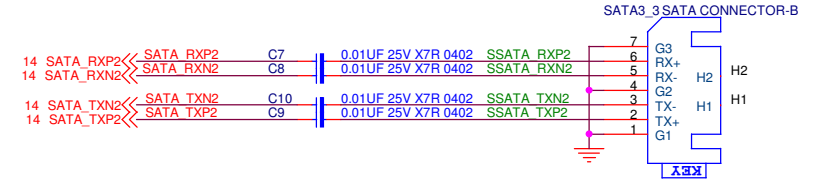

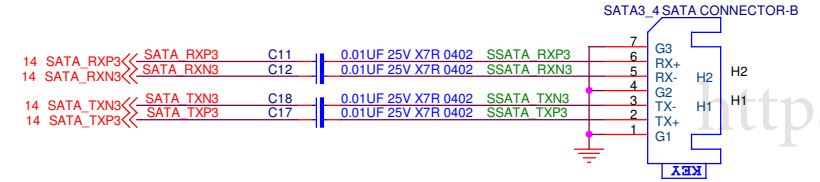

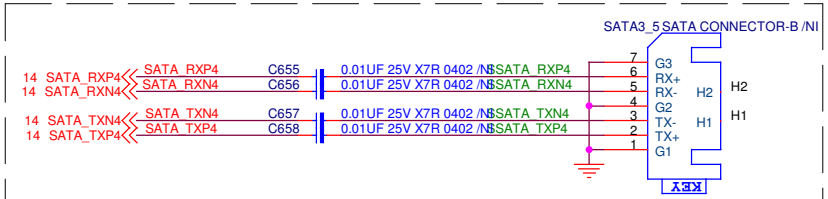

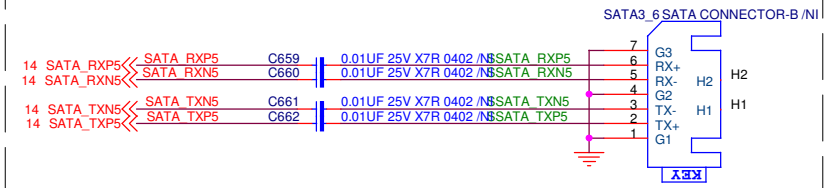

VER0.65:NEW ADD SATA CONN(PAGE14/24)

VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)

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Title: SATA EXPRESS

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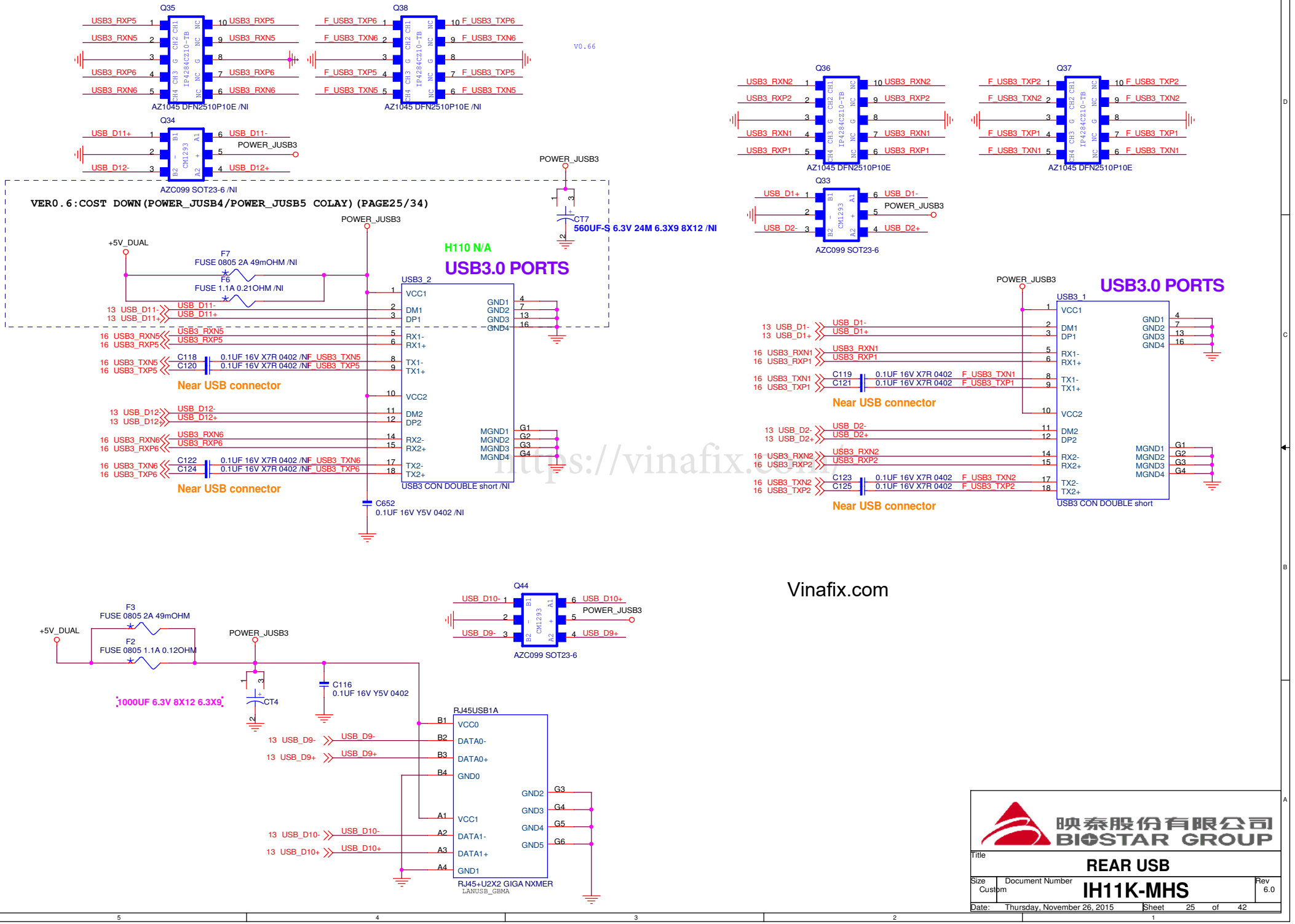
Q35
USB3_RXP5
USB3_RXN5
USB3_RXP6
USB3_RXN6
AZ1045 DFN2510P10E /NI
Q38
F_USB3_TXP6
F_USB3_TXN6
F_USB3_TXP5
F_USB3_TXN5
AZ1045 DFN2510P10E /NI
V0.66
Q34
USB_D11+
USB_D11-
POWER_JUSB3
USB_D12-
USB_D12+
AZC099 SOT23-6 /NI
Q36
USB3_RXN2
USB3_RXP2
USB3_RXN1
USB3_RXP1
AZ1045 DFN2510P10E
Q37
F_USB3_TXP2
F_USB3_TXN2
F_USB3_TXP1
F_USB3_TXN1
AZ1045 DFN2510P10E
Q33
USB_D1+
USB_D1-
POWER_JUSB3
USB_D2-
USB_D2+
AZC099 SOT23-6
VER0.6:COST DOWN(POWER_JUSB4/POWER_JUSB5 COLAY) (PAGE25/34)
POWER_JUSB3
CT7
560UF-S 6.3V 24M 6.3X9 8X12 /NI
H110 N/A
USB3.0 PORTS
+5V_DUAL
F7
FUSE 0805 2A 49mOHM /NI
F6
FUSE 1.1A 0.21OHM /NI
USB3_2
VCC1
DM1
DP1
RX1-
RX1+
VCC2
DM2
DP2
RX2-
RX2+
TX1-
TX1+
TX2-
TX2+
GND1
GND2
GND3
GND4
MGND1
MGND2
MGND3
MGND4
C118
C120
0.1UF 16V X7R 0402 /NF_USB3_TXN5
0.1UF 16V X7R 0402 /NF_USB3_TXP5
C122
C124
0.1UF 16V X7R 0402 /NF_USB3_TXN6
0.1UF 16V X7R 0402 /NF_USB3_TXP6
Near USB connector
Near USB connector
USB3 CON DOUBLE short /NI
C652
0.1UF 16V Y5V 0402 /NI
POWER_JUSB3
USB3.0 PORTS
USB3_1
C119
C121
0.1UF 16V X7R 0402
F_USB3_TXN1
F_USB3_TXP1
C123
C125
0.1UF 16V X7R 0402
F_USB3_TXN2
F_USB3_TXP2
Near USB connector
Near USB connector
USB3 CON DOUBLE short
Q44
USB_D10-
USB_D10+
POWER_JUSB3
USB_D9-
USB_D9+
AZC099 SOT23-6
F3
FUSE 0805 2A 49mOHM
+5V_DUAL
F2
FUSE 0805 1.1A 0.12OHM
POWER_JUSB3
1000UF 6.3V 8X12 6.3X9
CT4
C116
0.1UF 16V Y5V 0402
RJ45USB1A
VCC0
DATA0-
DATA0+
GND0
VCC1
DATA1-
DATA1+
GND1
GND2
GND3
GND4
GND5
RJ45+U2X2 GIGA NXMER
LANUSB_GBMA
Vinafix.com
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Title
REAR USB
Size
Custom
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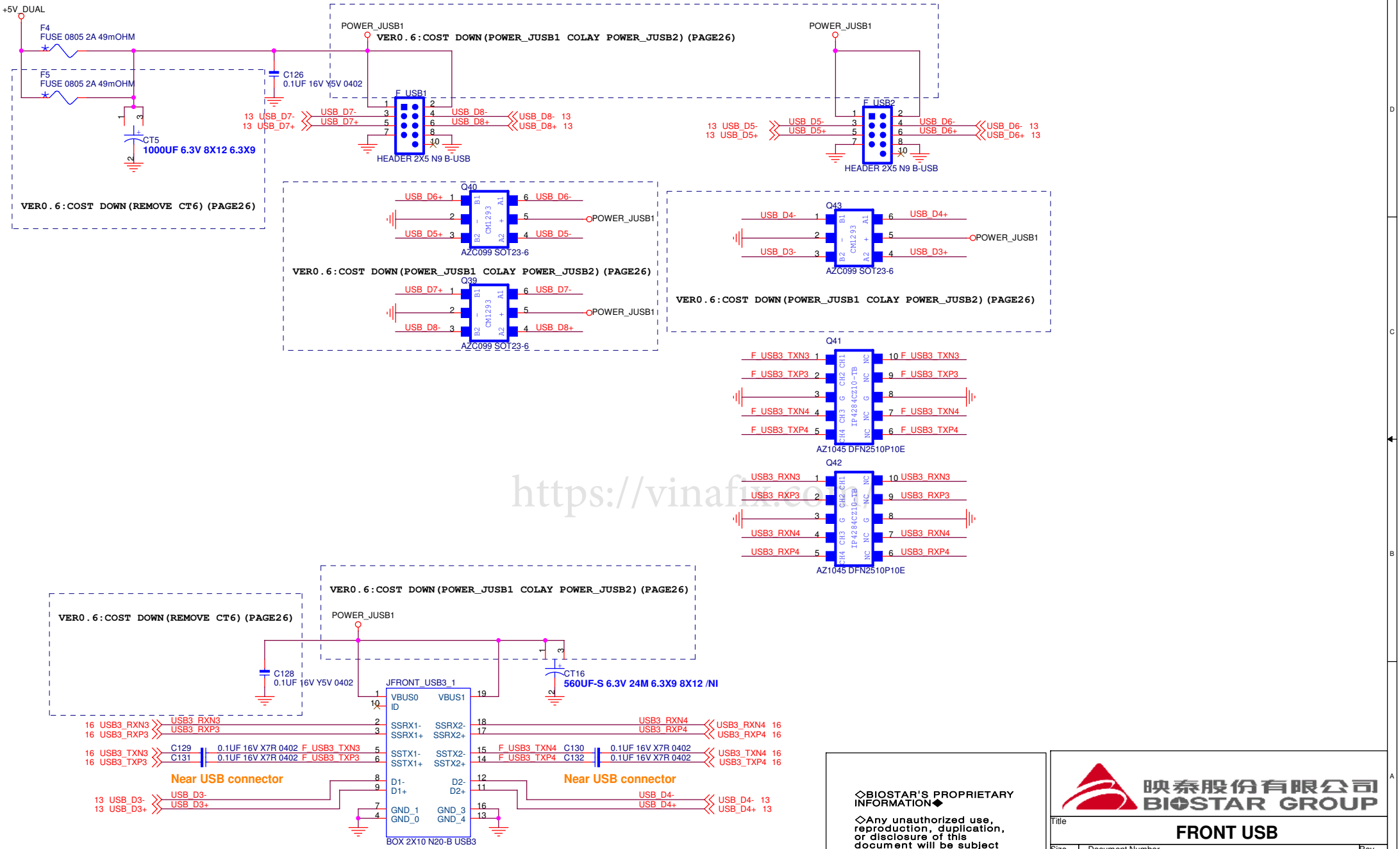
+5V_DUAL
F4
FUSE 0805 2A 49mOHM
F5
FUSE 0805 2A 49mOHM
CT5
1000UF 6.3V 8X12 6.3X9
VER0.6:COST DOWN(REMOVE CT6)(PAGE26)
C126
0.1UF 16V Y5V 0402
POWER_JUSB1
VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)
F_USB1
HEADER 2X5 N9 B-USB
F_USB2
HEADER 2X5 N9 B-USB
Q40
Q39
Q43
AZC099 SOT23-6
Q41
Q42
AZ1045 DFN2510P10E
C128
0.1UF 16V Y5V 0402
CT16
560UF-S 6.3V 24M 6.3X9 8X12 /NI
JFRONT_USB3_1
BOX 2X10 N20-B USB3
Near USB connector
Near USB connector
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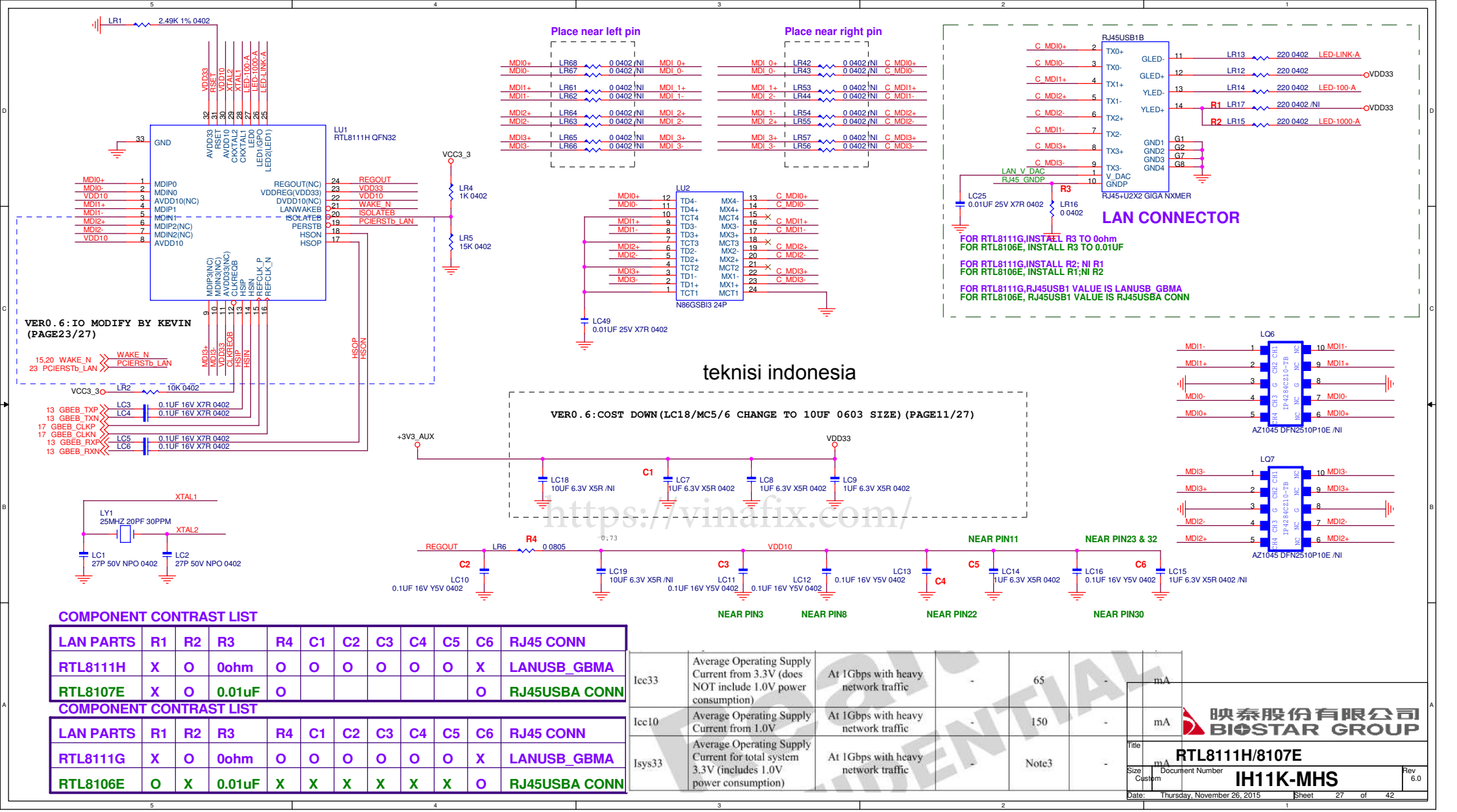

COMPONENT CONTRAST LIST

LAN PARTS	R1	R2	R3	R4	C1	C2	C3	C4	C5	C6	RJ45 CONN
RTL8111H	X	O	0ohm	O	O	O	O	O	O	X	LANUSB_GBMA
RTL8107E	X	O	0.01uF	O						O	RJ45USBA CONN

COMPONENT CONTRAST LIST

LAN PARTS	R1	R2	R3	R4	C1	C2	C3	C4	C5	C6	RJ45 CONN
RTL8111G	X	O	0ohm	O	O	O	O	O	O	X	LANUSB_GBMA
RTL8106E	O	X	0.01uF	X	X	X	X	X	X	O	RJ45USBA CONN

Icc33	Average Operating Supply Current from 3.3V (does NOT include 1.0V power consumption)	At 1Gbps with heavy network traffic	-	65	-	mA
Icc10	Average Operating Supply Current from 1.0V	At 1Gbps with heavy network traffic	-	150	-	mA
Isys33	Average Operating Supply Current for total system 3.3V (includes 1.0V power consumption)	At 1Gbps with heavy network traffic	-	Note3	-	mA

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Title	RTL8111H/8107E	
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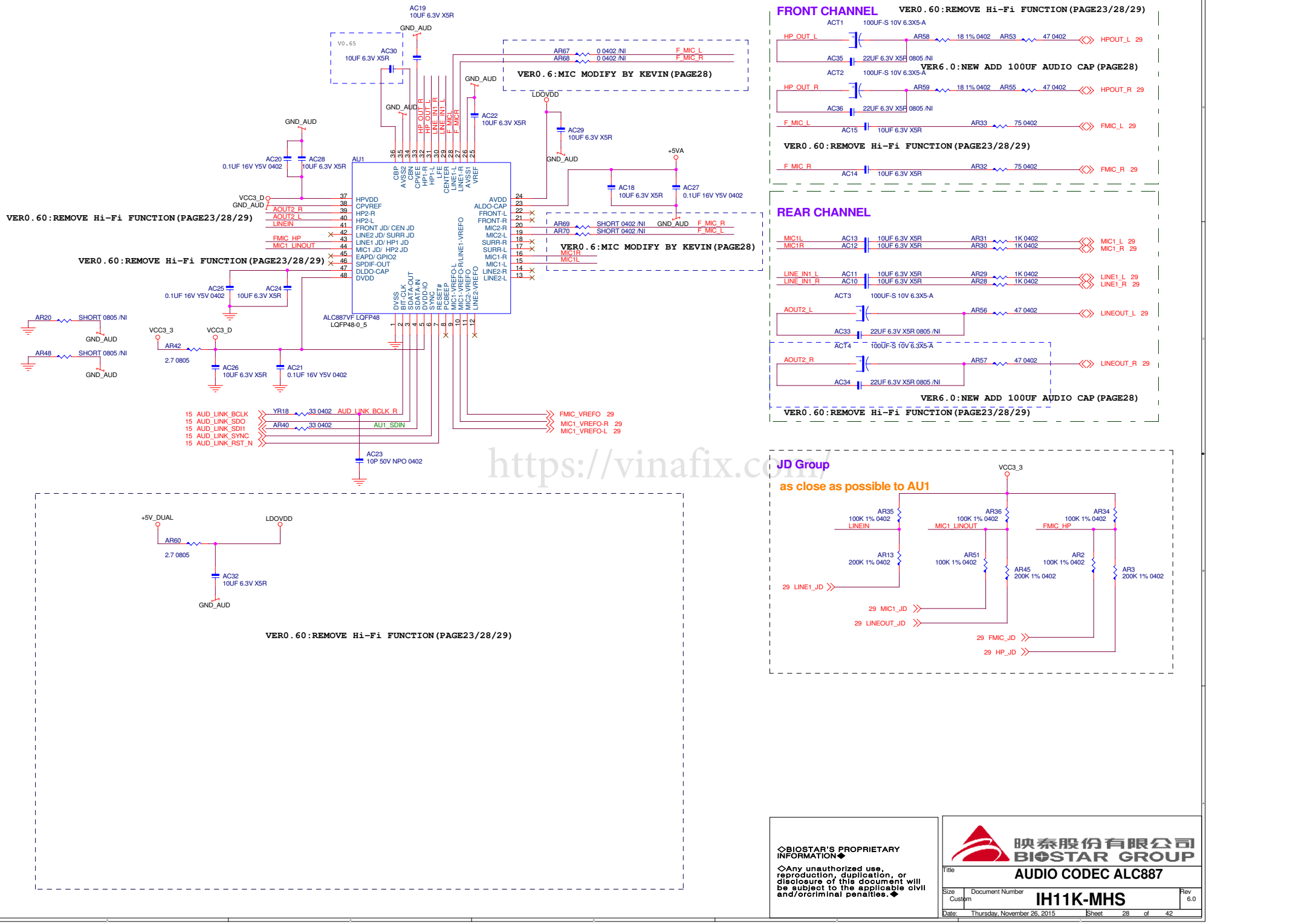

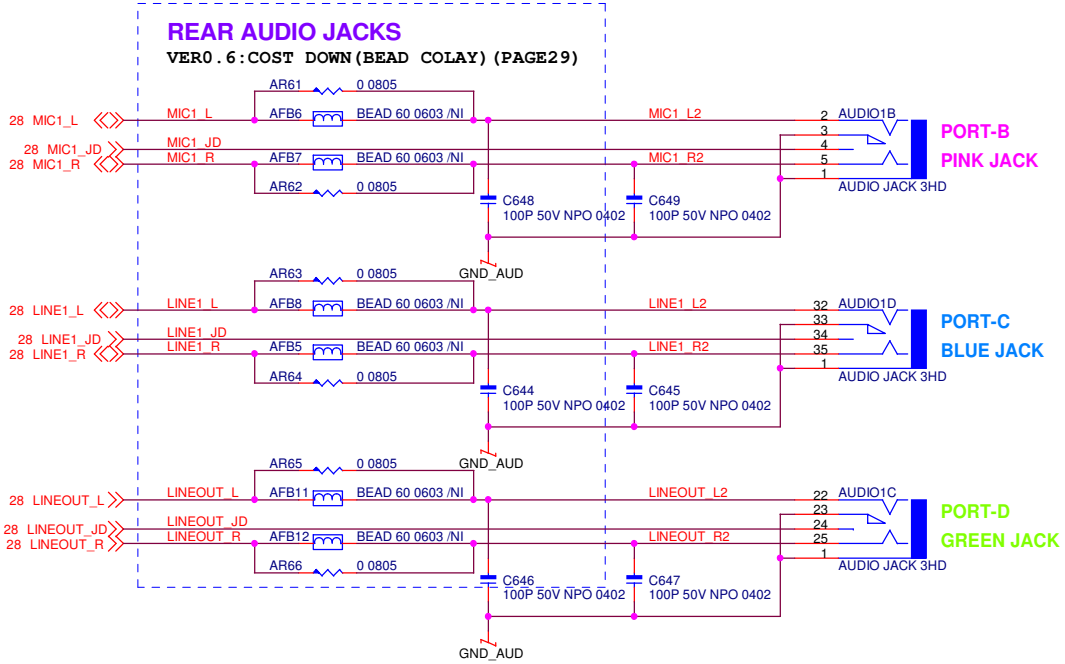

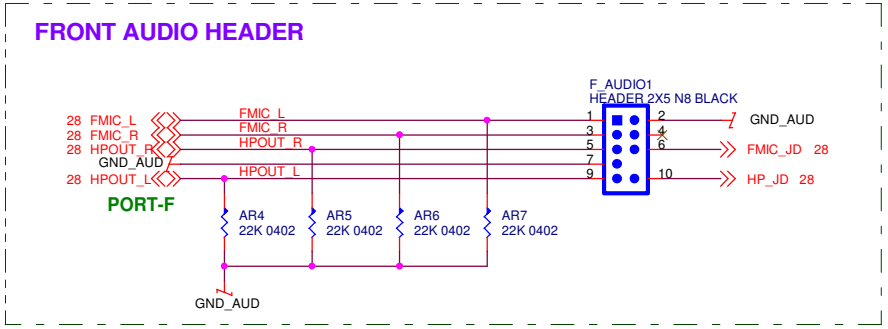

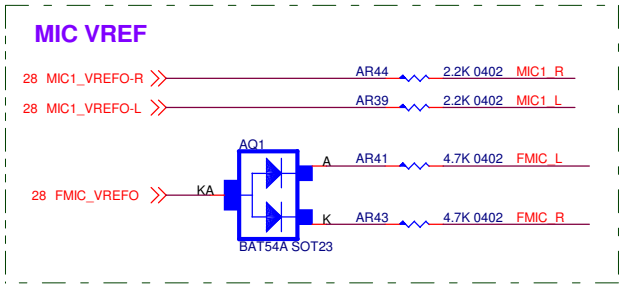

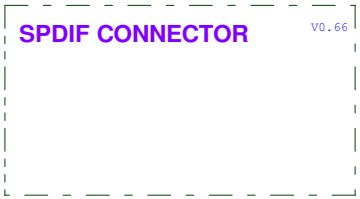

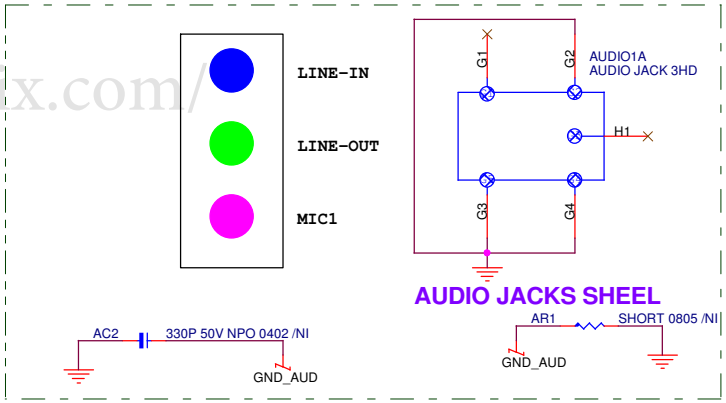

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Title: AUDIO CONNECTOR

Size	Document Number	Rev
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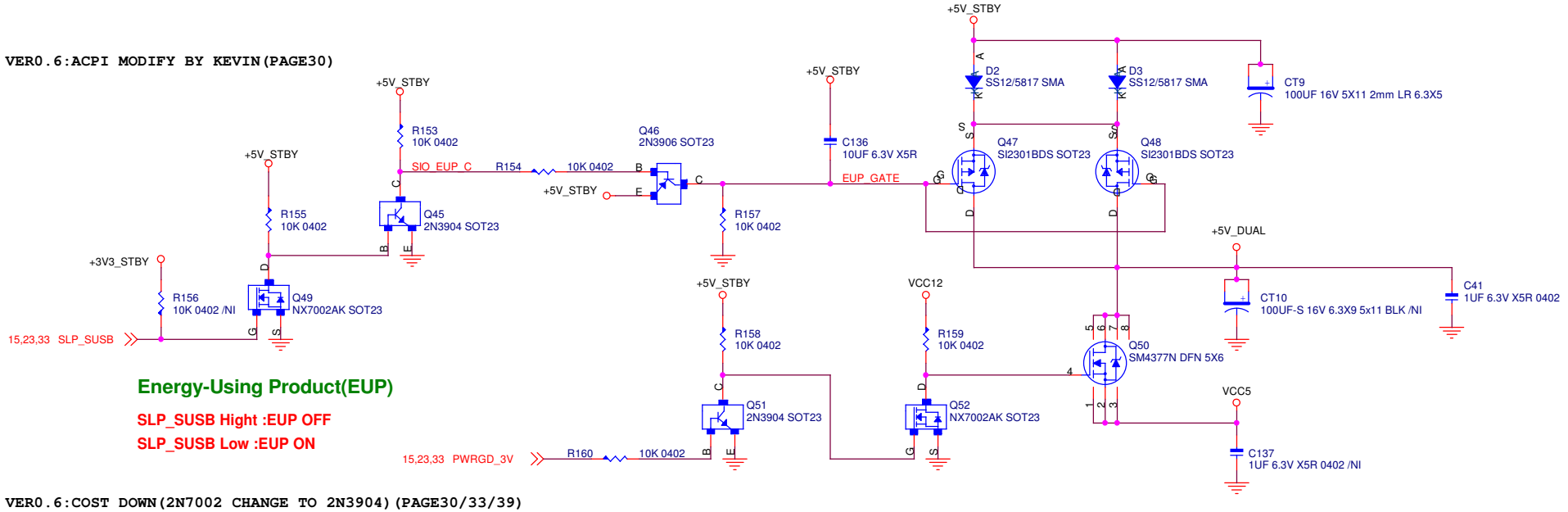
VER0.6:ACPI MODIFY BY KEVIN(PAGE30)



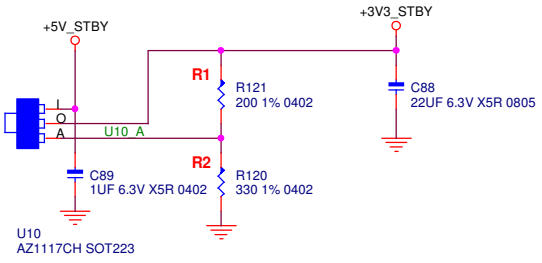
Energy-Using Product(EUP)

SLP_SUSB Hight :EUP OFF

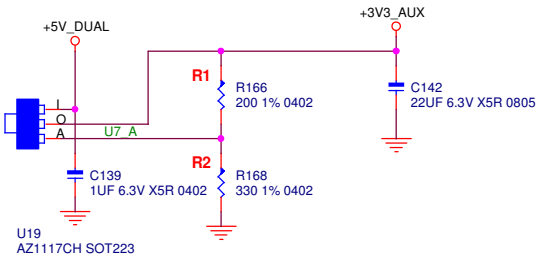
SLP_SUSB Low :EUP ON

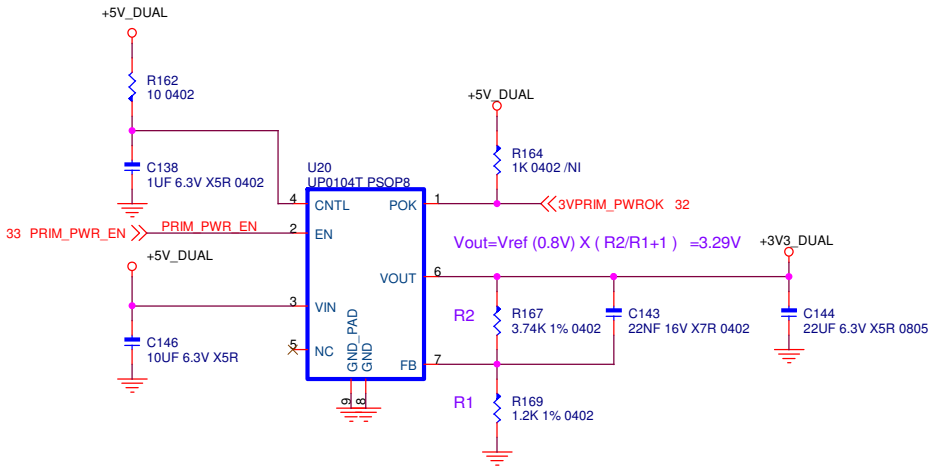
VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904)(PAGE30/33/39)

Vout=Vref (1.25V) X (1+R2/R1)=3.3125V



Vout=Vref (1.25V) X (1+R2/R1)=3.3125V





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Title	ACPI POWER	
Size B	Document Number IH11K-MHS	Rev 6.0
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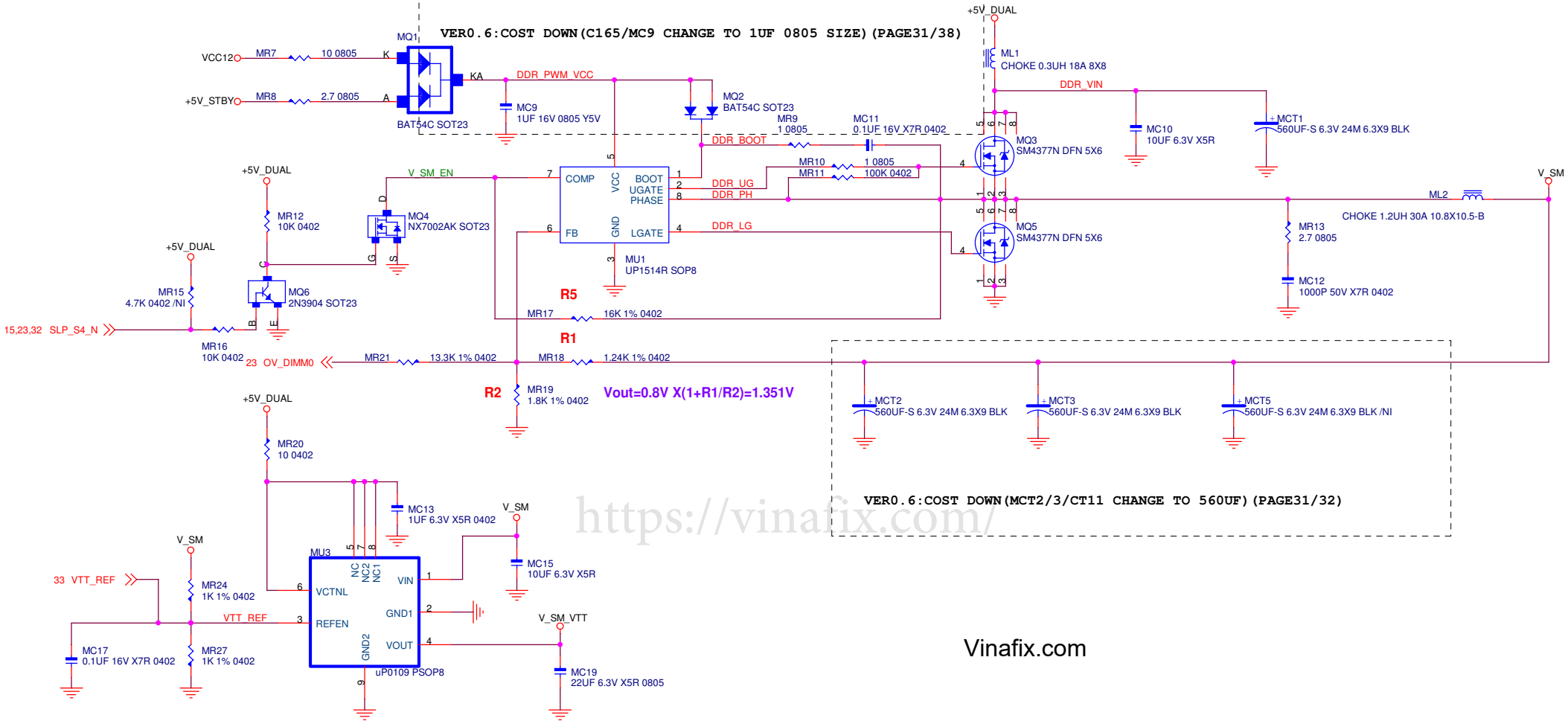
MEMORY PART:M+Reference



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Title	MEMORY DC-DC	
Size B	Document Number IH11K-MHS	Rev 6.0
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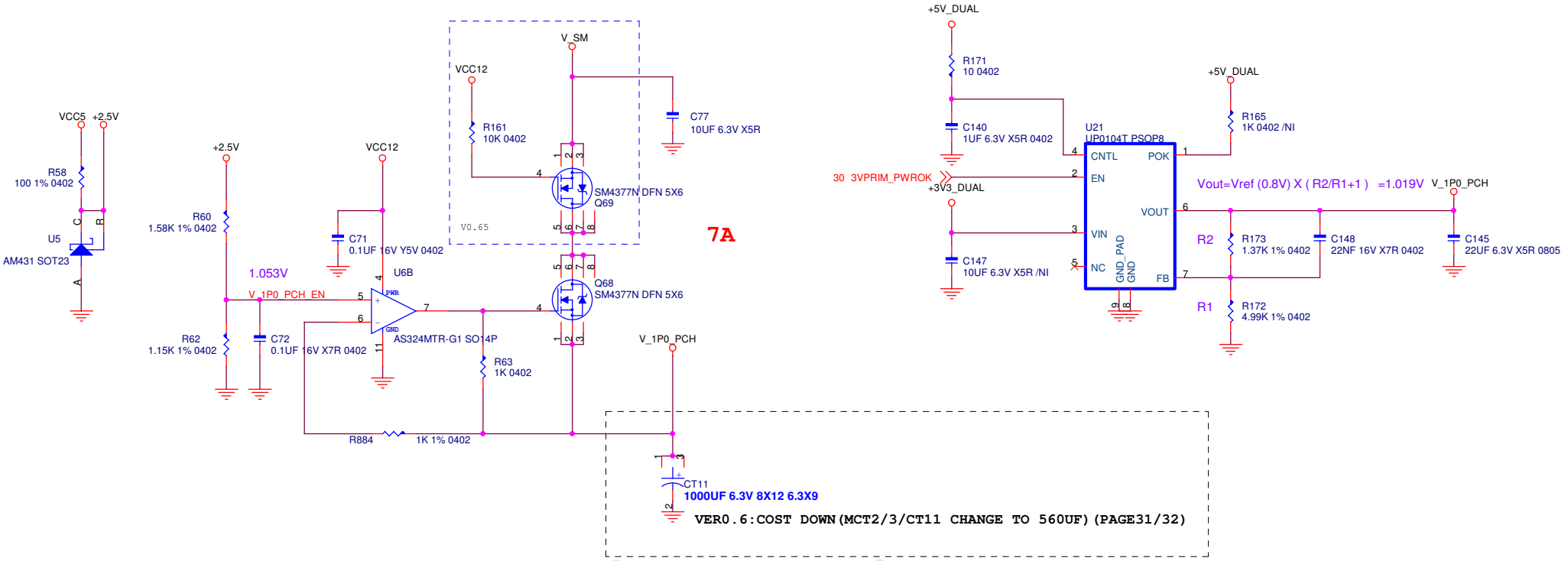

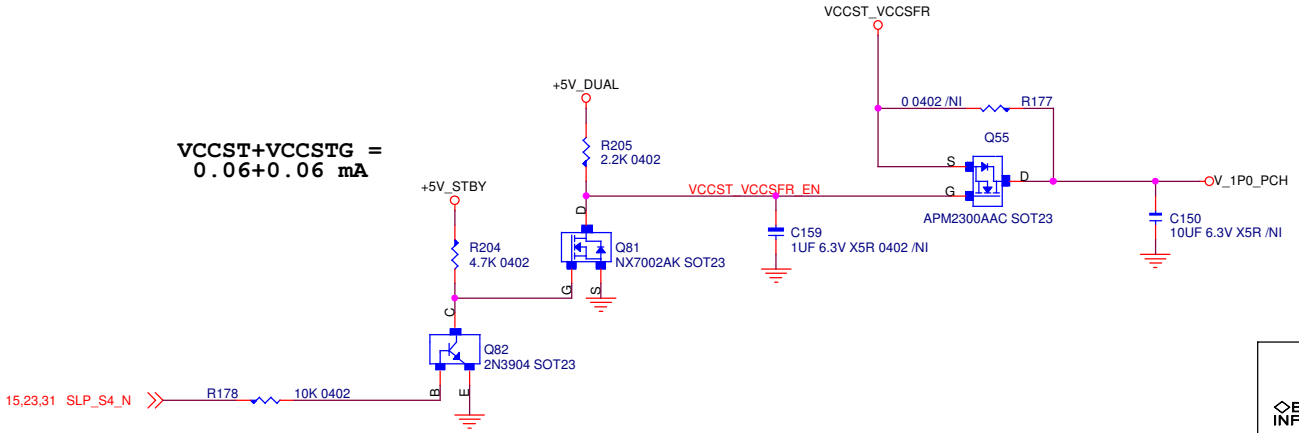

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Title	V_1P0_PCH	
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39 VR_RDY >> VR_RDY — R210 — PCH_SYSPWROK >> PCH_SYSPWROK 15

ISEN_SHORT /NI

1.045V

VER0.6:COST DOWN(SHORT 0402)(PAGE8/11/12/16/19/23/33/39)

VCCST_VCCSFR

R211 10K 0402

VCCST_PWRGD 8

Q56 NX7002AK SOT23

CC38 0.01UF 25V X7R 0402 /NI

+5V_DUAL

R184 4.7K 0402

VCC3_3

VCCSTPWRGDG

R185 1K 0402

Q57 2N3904 SOT23

39 VR_RDY >> R187 10K 0402

+5V_STBY

PCH_RSMRST_N 15,23

R188 10K 0402

Q58 NX7002AK SOT23

Q59 2N3904 SOT23

VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904)(PAGE30/33/39)

15,23,30 SLP_SUSB >> R189 10K 0402

+5V_DUAL

VCORE_EN >> VCORE_EN 39

Q60 NX7002AK SOT23

TR1 4.7K 0402

PWR_EN

V_SA_IO

TQ1 2N3904 SOT23

+5V_DUAL

TR3 8.2K 0402

R75 10K 0402

TC1 1UF 6.3V X5R 0402

VR_RDY >> VR_RDY 39

Q64 NX7002AK SOT23

TQ2 2N3904 SOT23

15,23,38 SLP_S3_N >> TR5 10K 0402

+5V_DUAL

R170 2.2K 0402 /NI

PRIM_PWR_EN 30

+5V_DUAL

R174 4.7K 0402 /NI

Q53 NX7002AK SOT23 /NI

Q54 2N3904 SOT23 /NI

15,23,30 SLP_SUSB >> R176 10K 0402 /NI

Use of DDR_VTT_CNTL to control VTT power gate is optional
for additional power savings in Idle power states.
If not used,
VTT should be controlled by SLP_S3#

+5V_DUAL

MR33 10K 0402

VTT_REF >> VTT_REF 31

MQ10 NX7002AK SOT23

VTTREFG

MQ9 2N3904 SOT23

15,23,38 SLP_S3_N >> MR58 10K 0402

8 DDR_VTT_CTL >> MR30 10K 0402 /NI

VCC3_3

R192 2.7K 0402

Q65 NX7002AK SOT23

15,20 SMB_CLK_RESUME >> SMB_CLK_MAIN 11,12,21

VCC12

VCC3_3

R193 1K 0402

R194 2.7K 0402

15,20 SMB_DATA_RESUME >> SMB_DATA_MAIN 11,12,21

Q67 NX7002AK SOT23

FOR POWER TEST

PWRGD_3V 15,23,30

Q66 2N3904 SOT23

8,16,39 H_SKTOCC_N >> R195 10K 0402

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Title: RESUME RESET LOGIC

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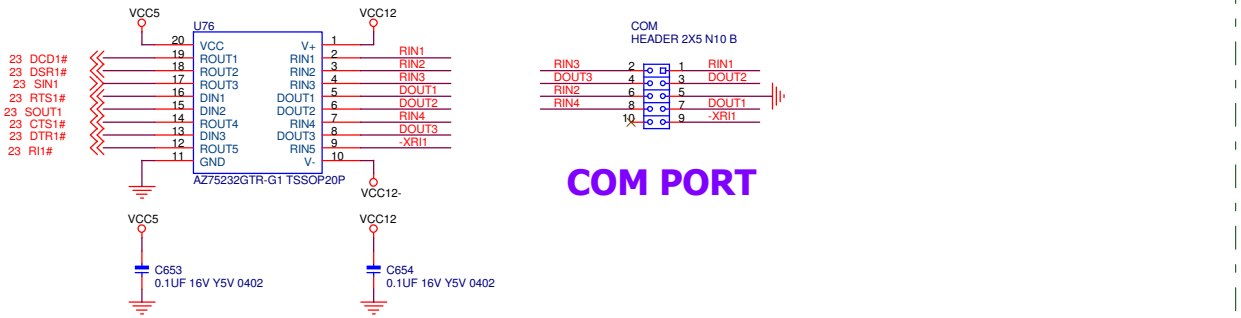

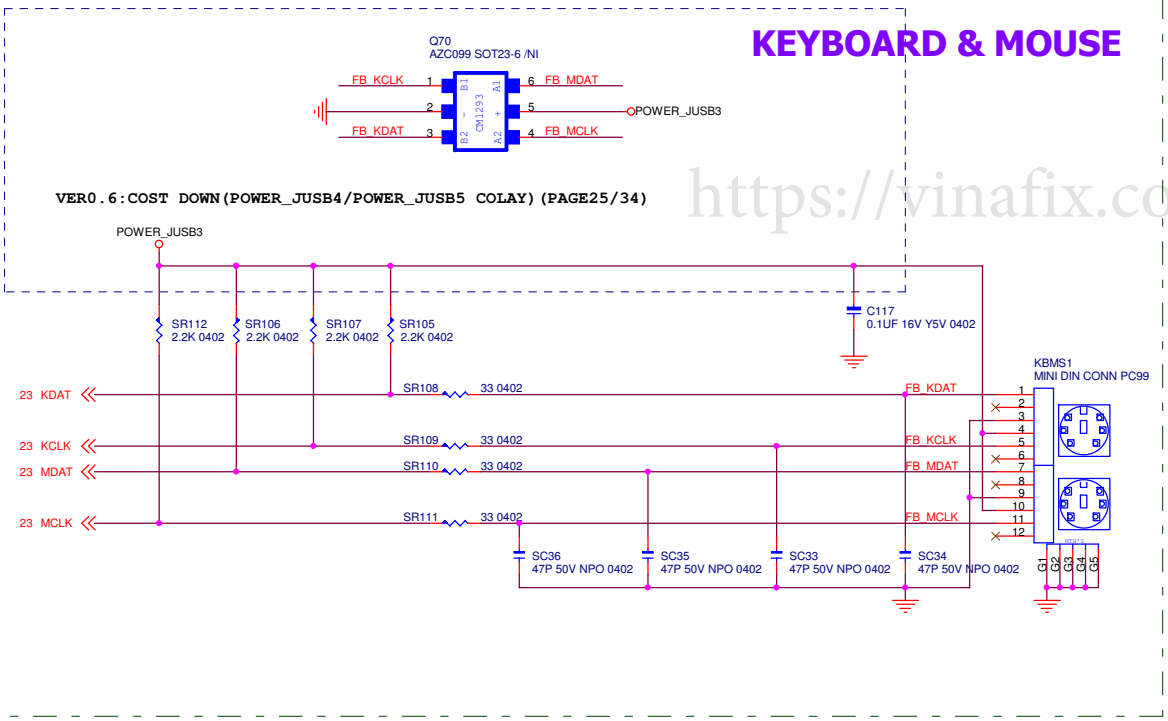

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Title: COM1 / PS2 CONN

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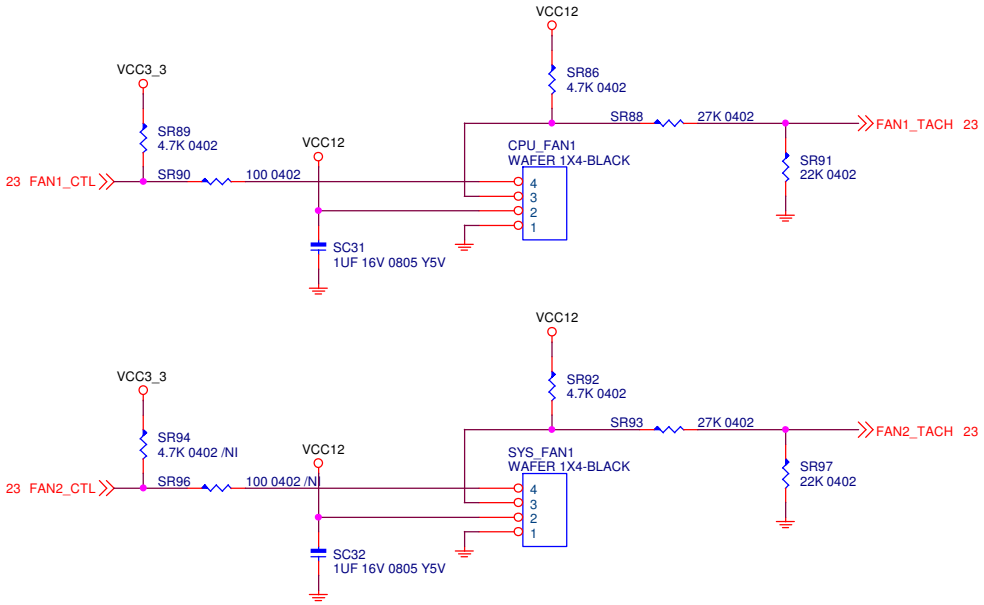

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Title: FAN & PS2

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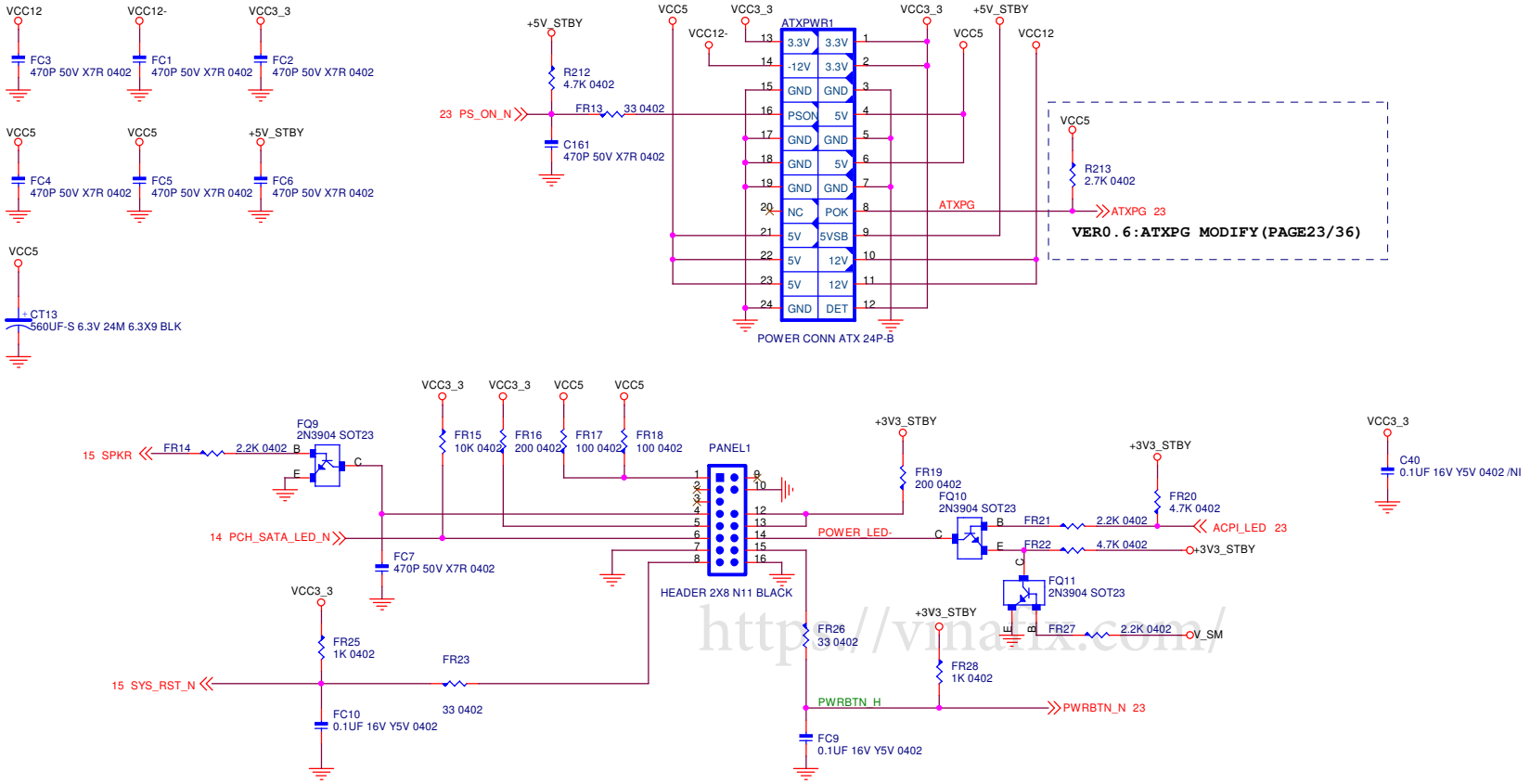
FP PART: F+Reference



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Title	24PIN CONN & FP	
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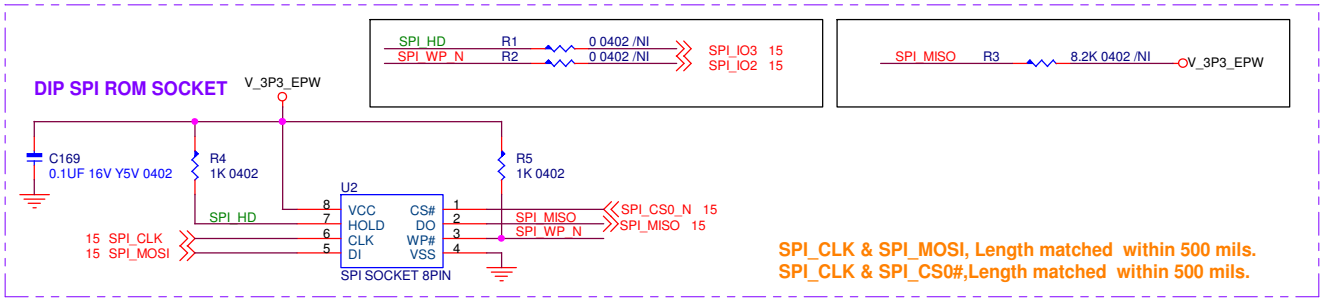

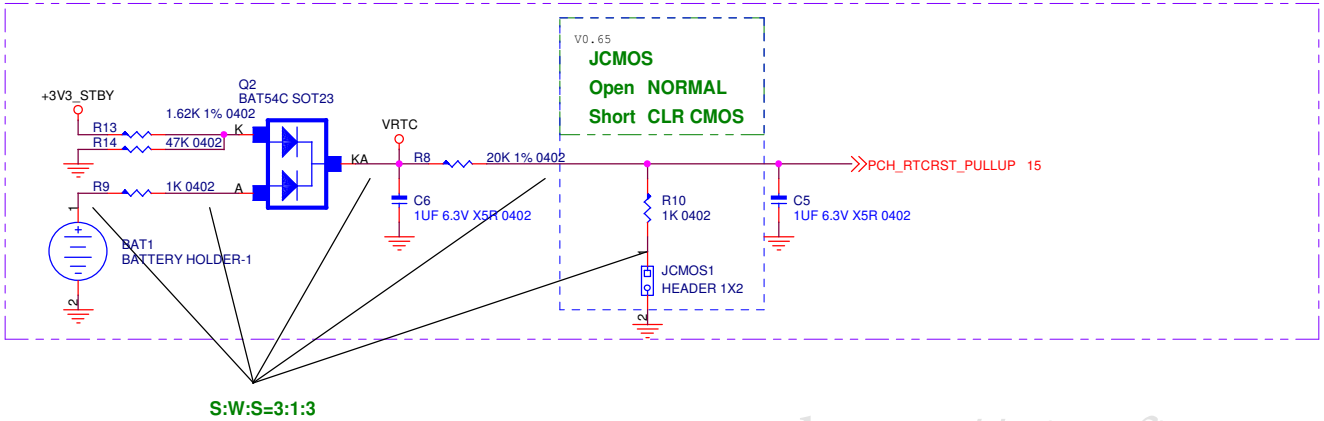

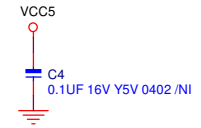

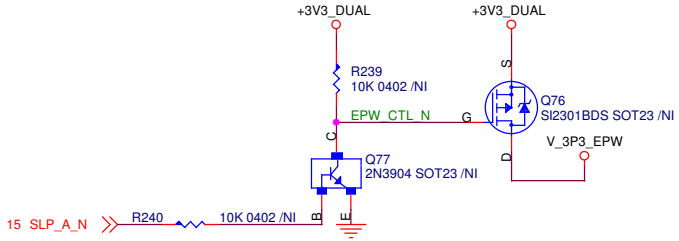

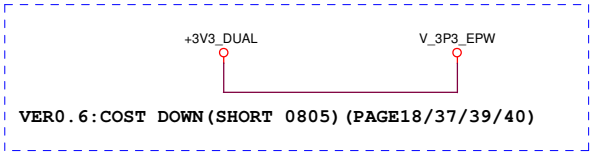

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Title	SPI ROM/RTC CRYSTAL/BAT	
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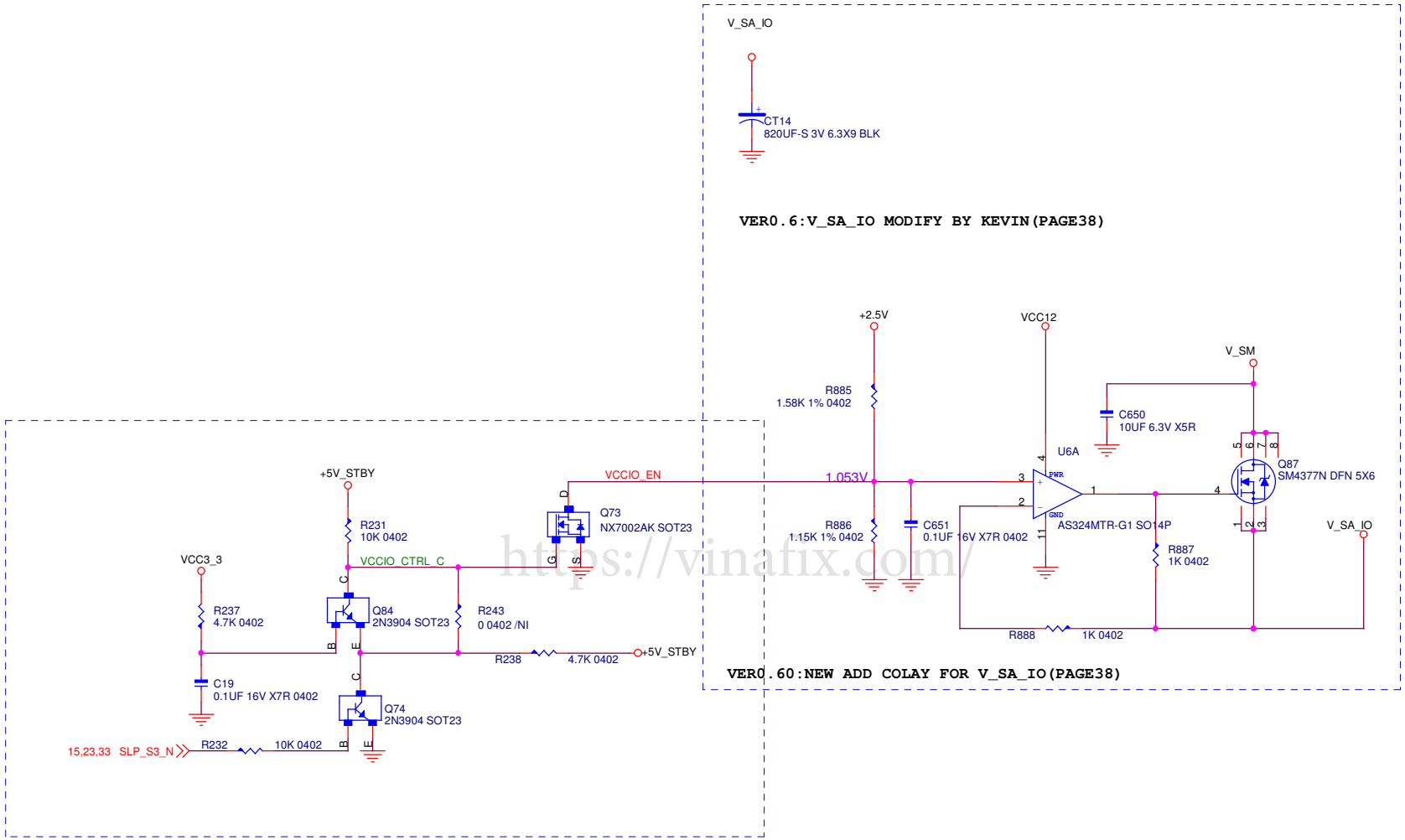

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Title	VCCIO/VCCSA DC-DC	
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VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606)(PAGE39/40/41)

VER0.65:PU1 core power change to +12V(PAGE39)

VER0.65:PU1 core power change to +12V(PAGE39)

VER0.60:CHANGE CPU POWER CONN TO 2*2(PAGE39)

VER0.65:PU1 core power change to +12V(PAGE39)

PWM Fequency= 400KHz

close to VCORE phase1 choke

close to VCCGT phase1 choke

VER0.65:SET2_3606 MODIFY(PAGE39)

DEFAULT : H --> BOOT 0.8V

ADD CPU : L --> BOOT FROM CPU

DEFAULT : 5V--> OUTOUT 0.8V

ADD CPU : FLOAT --> OUTOUT FROM CPU

Sensor POR Min 2V

Close to PIN14

Close to PIN33

Close to PIN28,PIN29

RT3606BC WQFN60

Title	RT3606 DC-DC CONVERTE
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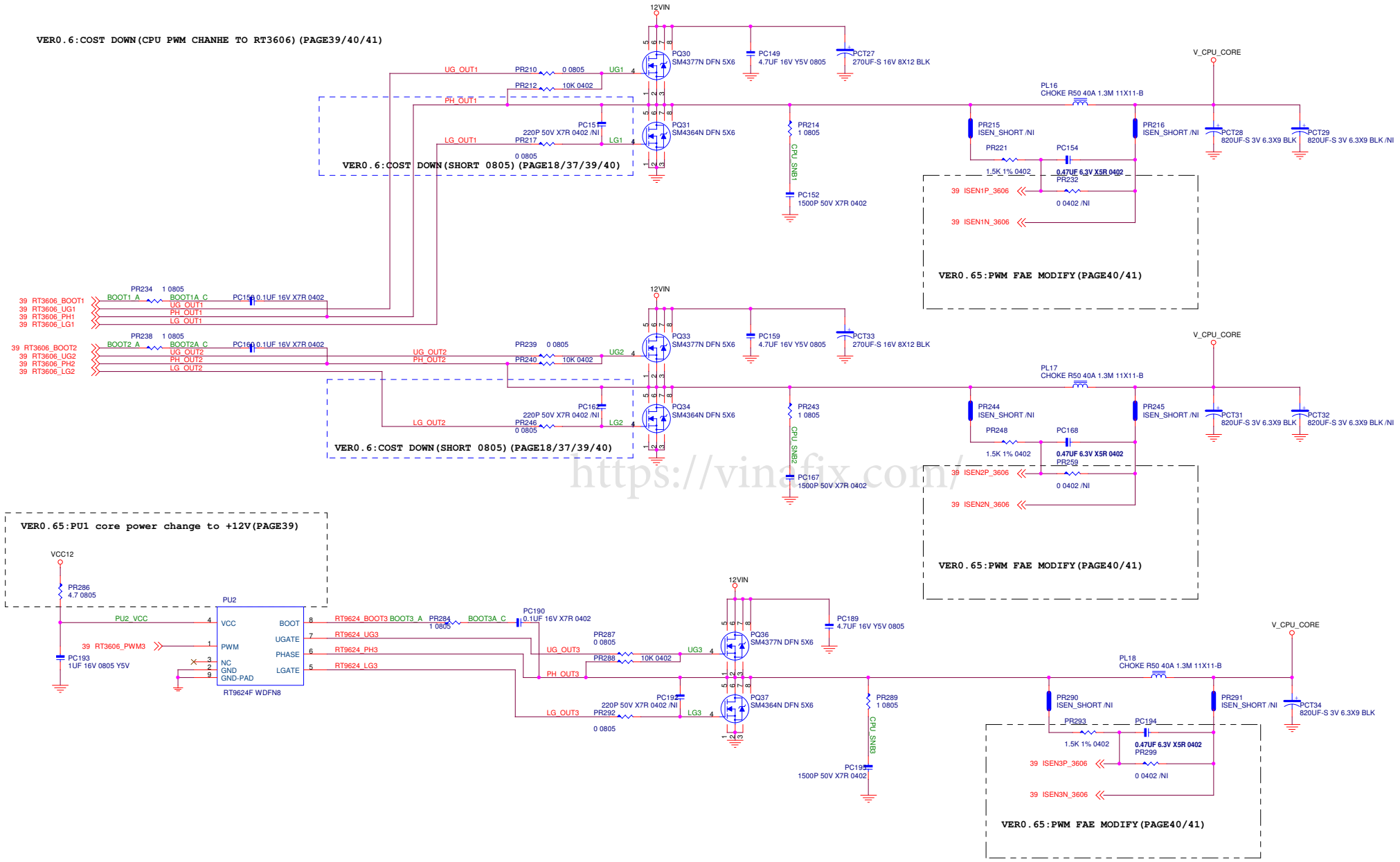

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Title	RT3606_VCORE_PHASE		
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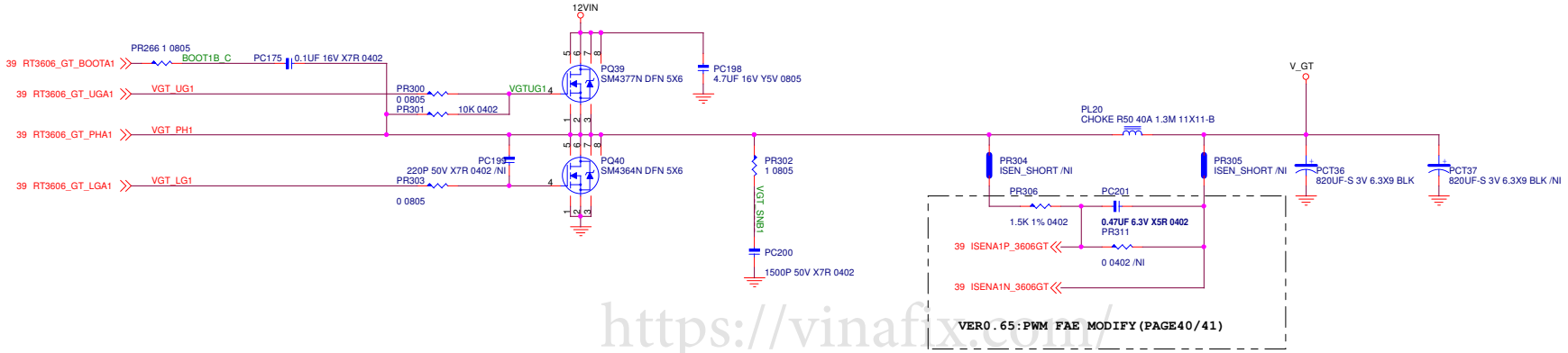
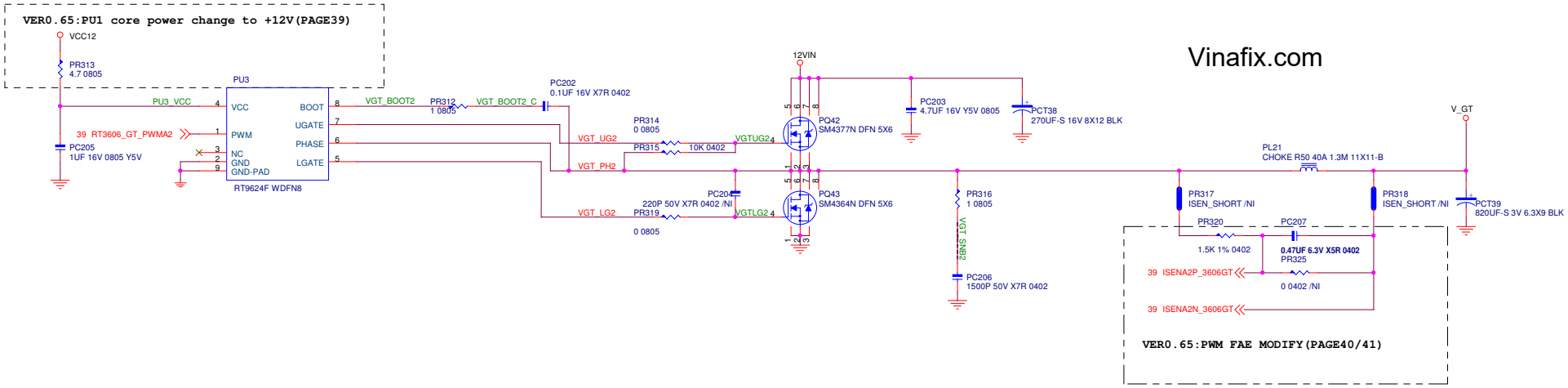
VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606)(PAGE39/40/41)

Skylake S-line 42 95W RT3606_VGT





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Title	RT3606_VGT_PHASE	
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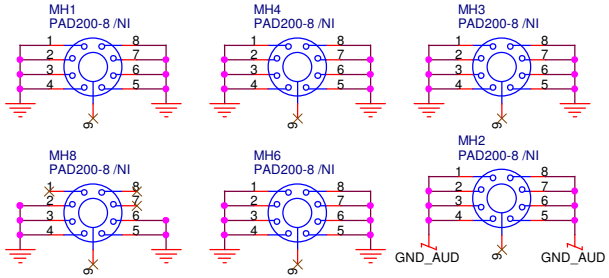

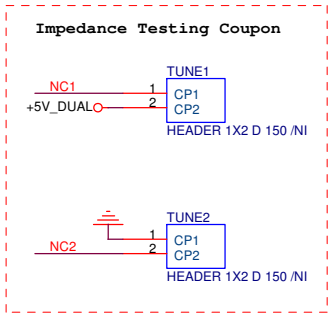

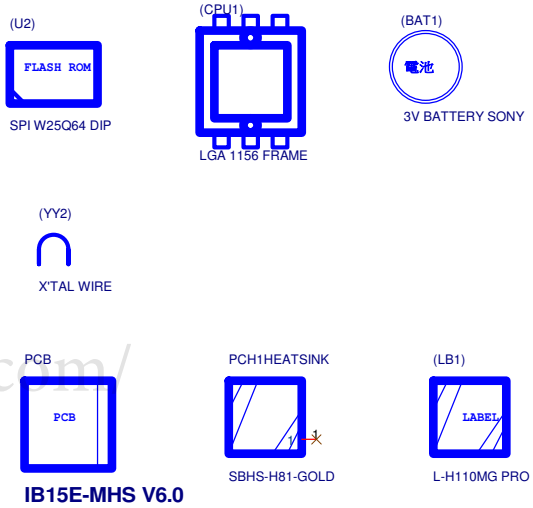

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Title	BOM	
Size B	Document Number IH11K-MHS	Rev 6.0
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