Gold Coast- MT / DT

Intel PROCESSOR SANDY BRIDGE LGA1155

Intel Cougar Point

REV A00

DELL INC.

Title: TBD

DWG NO: Gold Coast_MT/DT

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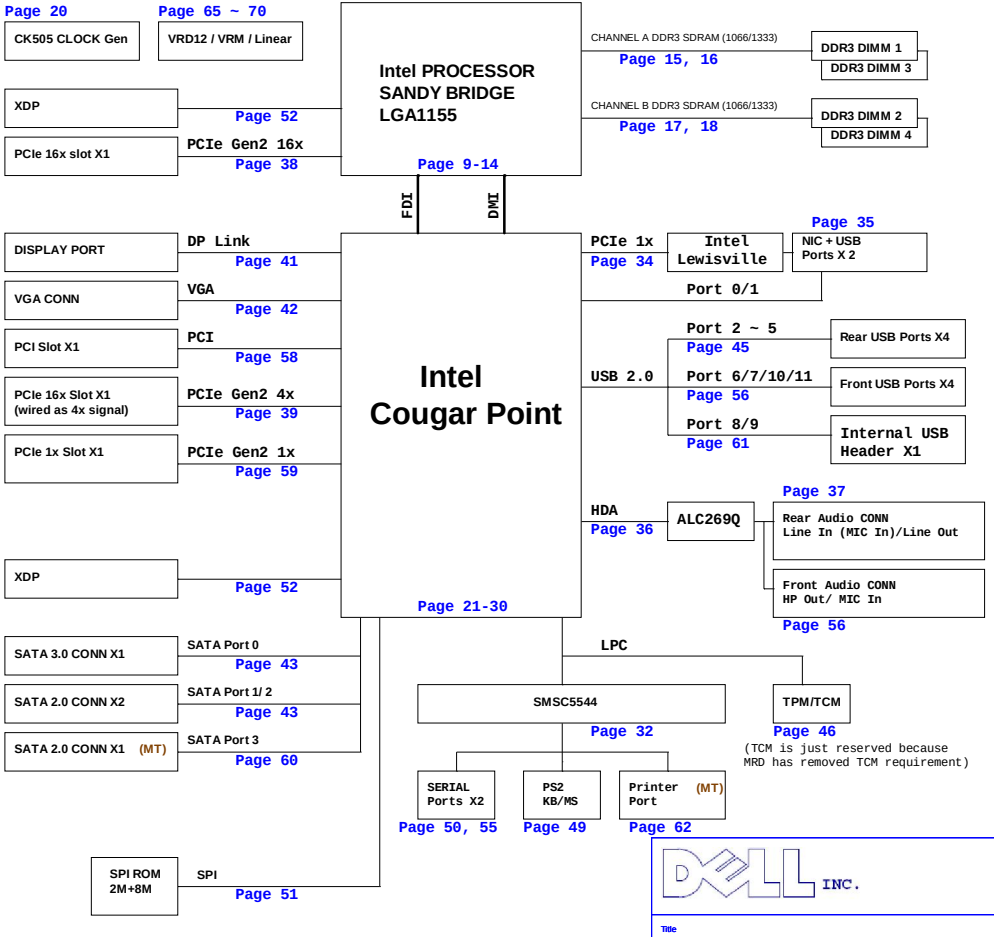

DELL INC.

Title: Index / Block diagram

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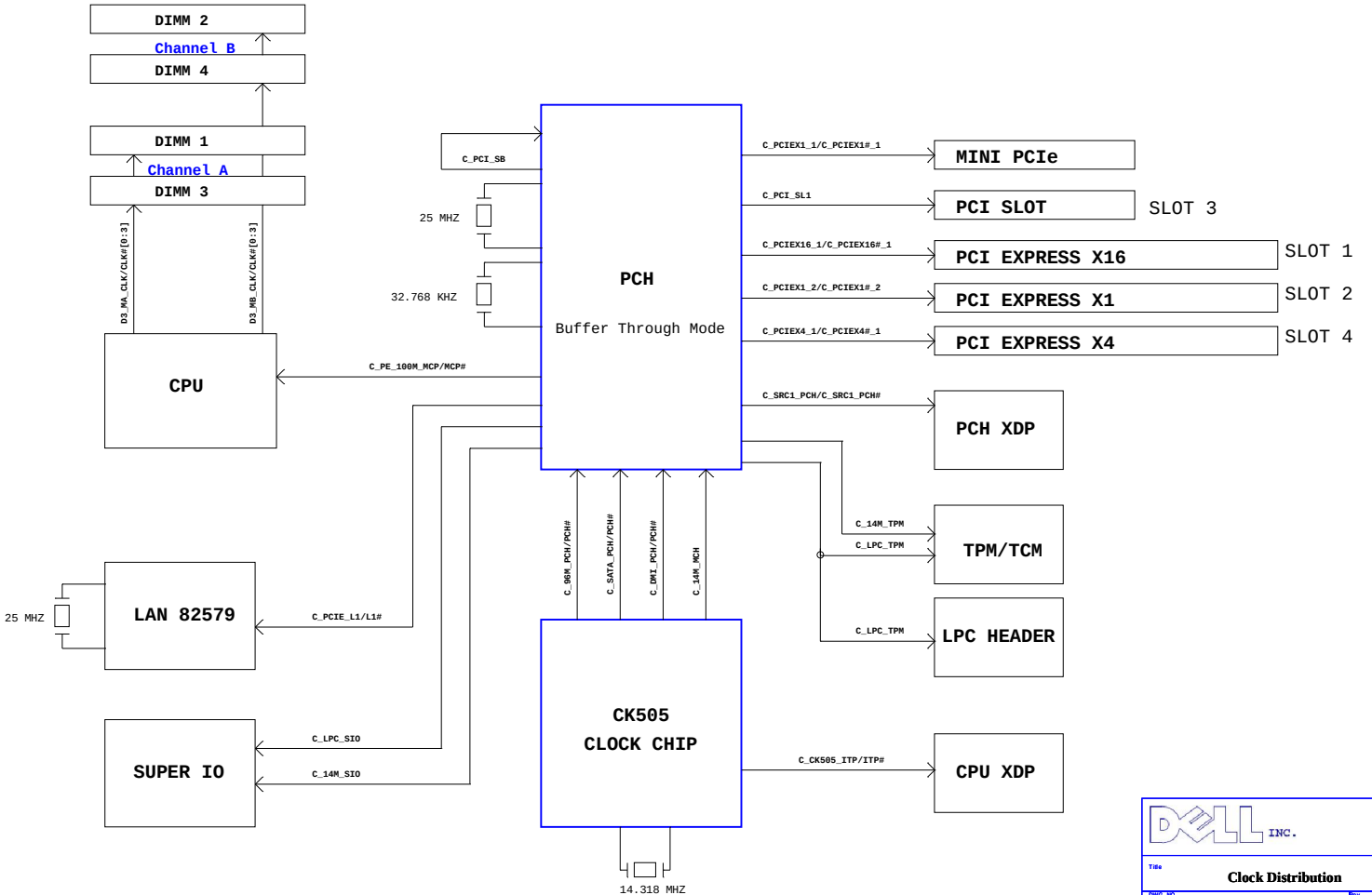
DIMM 2
Channel B
DIMM 4
DIMM 1
Channel A
DIMM 3
D3_MA_CLK/CLK#[0:3]
D3_MB_CLK/CLK#[0:3]
CPU
C_PE_100M_MCP/MCP#
C_PCI_SB
25 MHZ
32.768 KHZ
PCH
Buffer Through Mode
C_PCIEX1_1/C_PCIEX1#_1
MINI PCIe
C_PCI_SL1
PCI SLOT
SLOT 3
C_PCIEX16_1/C_PCIEX16#_1
PCI EXPRESS X16
SLOT 1
C_PCIEX1_2/C_PCIEX1#_2
PCI EXPRESS X1
SLOT 2
C_PCIEX4_1/C_PCIEX4#_1
PCI EXPRESS X4
SLOT 4
C_SRC1_PCH/C_SRC1_PCH#
PCH XDP
C_14M_TPM
C_LPC_TPM
TPM/TCM
C_LPC_TPM
LPC HEADER
C_96M_PCH/PCH#
C_SATA_PCH/PCH#
C_DMI_PCH/PCH#
C_14M_MCH
25 MHZ
LAN 82579
C_PCIE_L1/L1#
CK505
CLOCK CHIP
C_LPC_SIO
C_14M_SIO
SUPER IO
C_CK505_ITP/ITP#
CPU XDP
14.318 MHZ
DELL INC.
Title
Clock Distribution
DWG NO
Gold Coast_MT/DT
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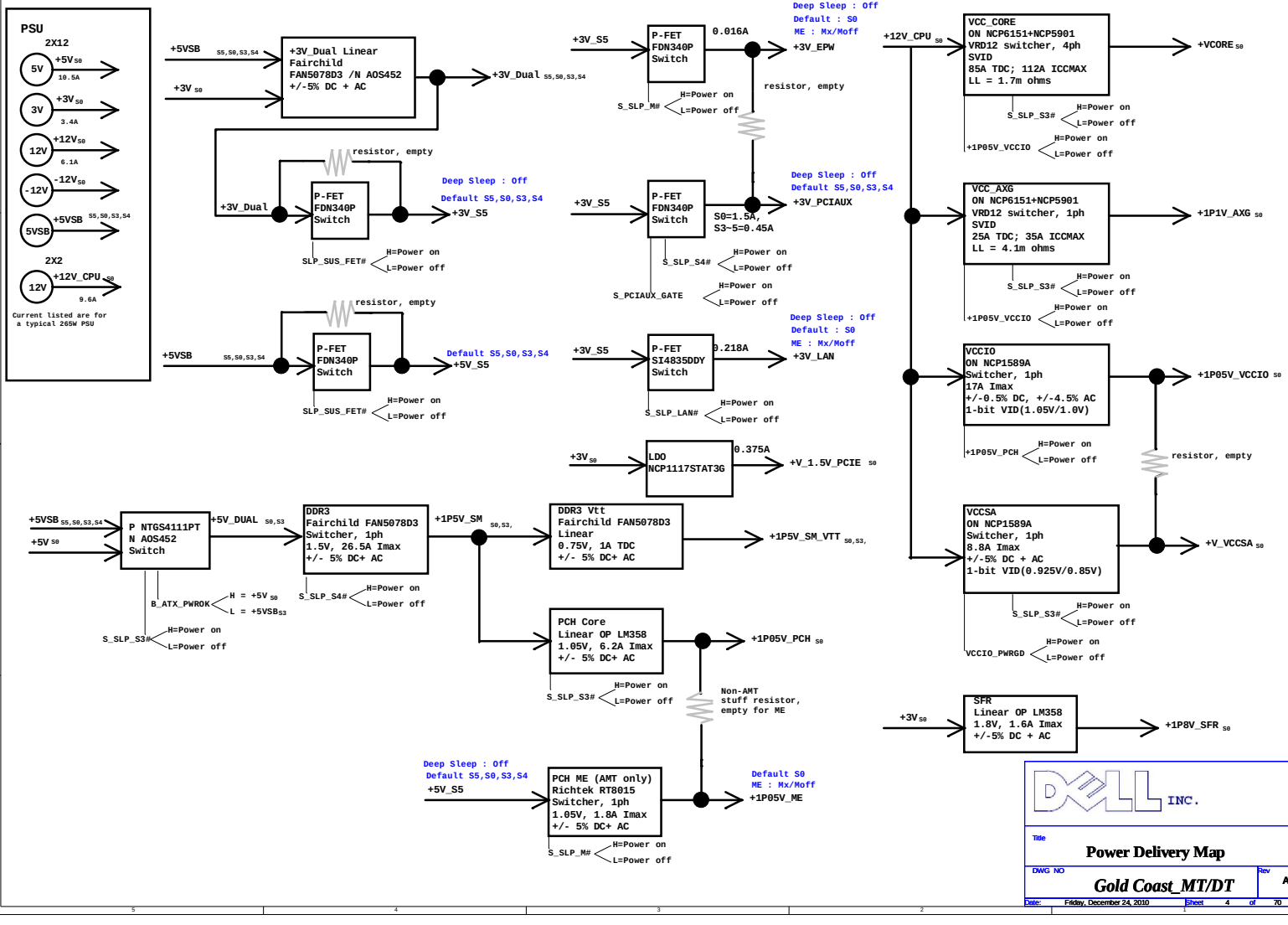
POWER DELIVERY MAP



DELL INC.

Title: **Power Delivery Map**

DWG NO: *Gold Coast_MT/DT*

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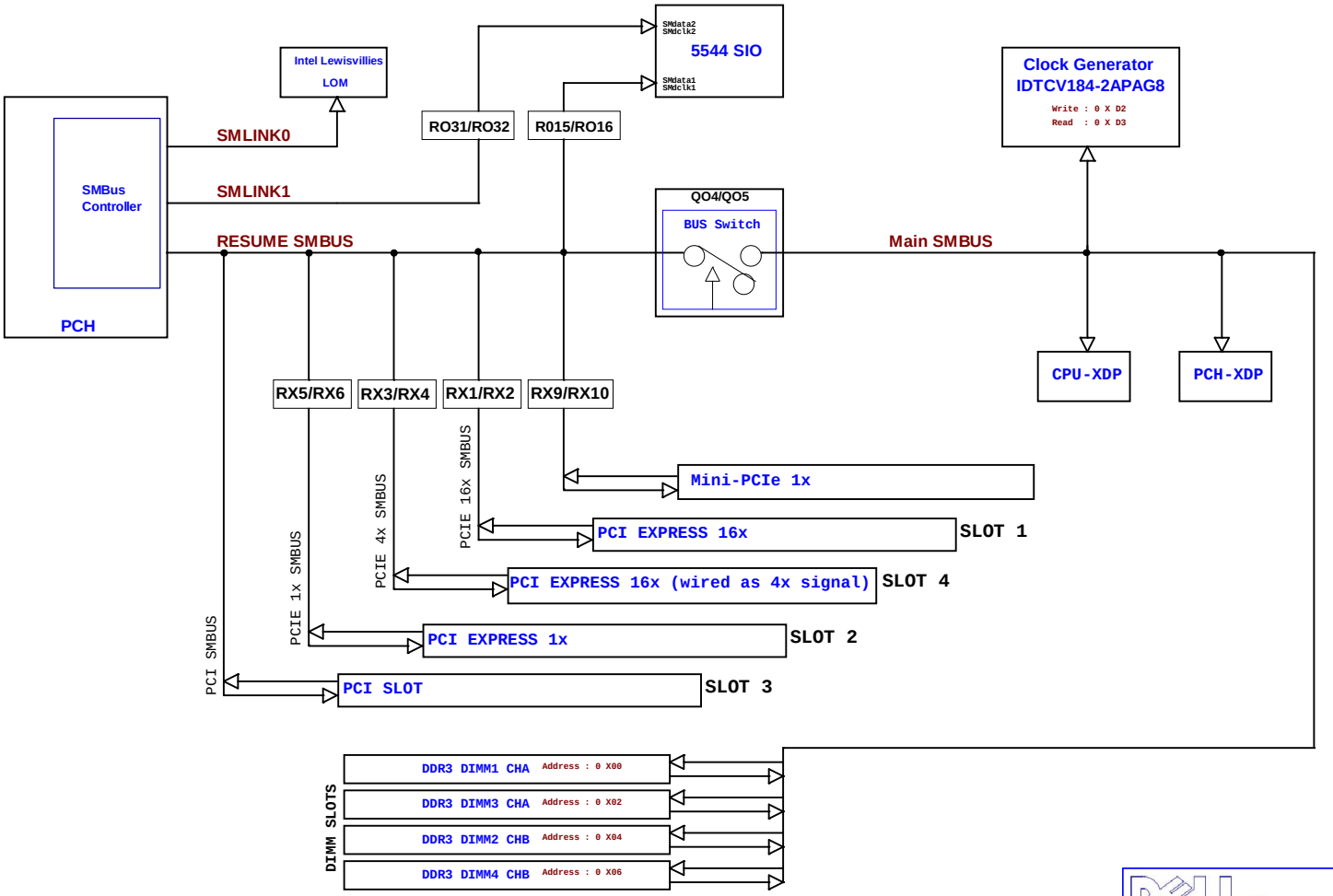
SMBUS DIAGRAM



DELL INC.

Title: BLOCK DIAGRAM

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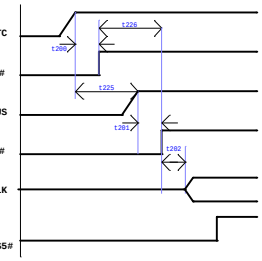
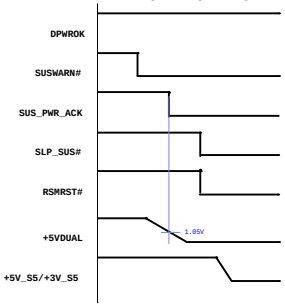
POWER ON Timing Diagram

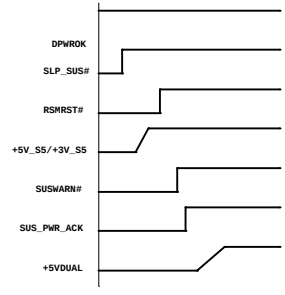
G3 to S4/S5 Timing Diagram

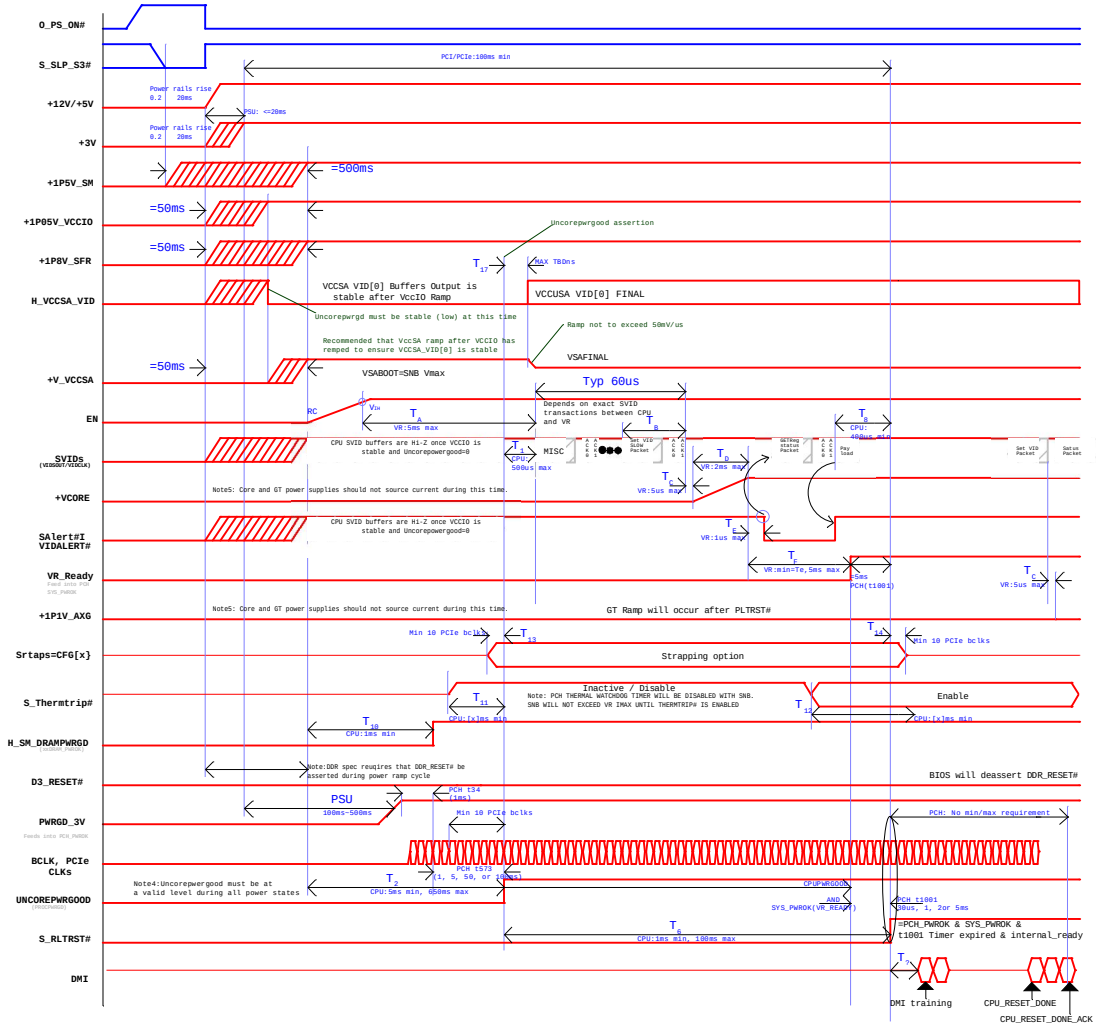


Deep Sleep Entry



Deep Sleep Exit





DELL INC.

Title: **Power On Sequence**

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RESET / Power Good MAP

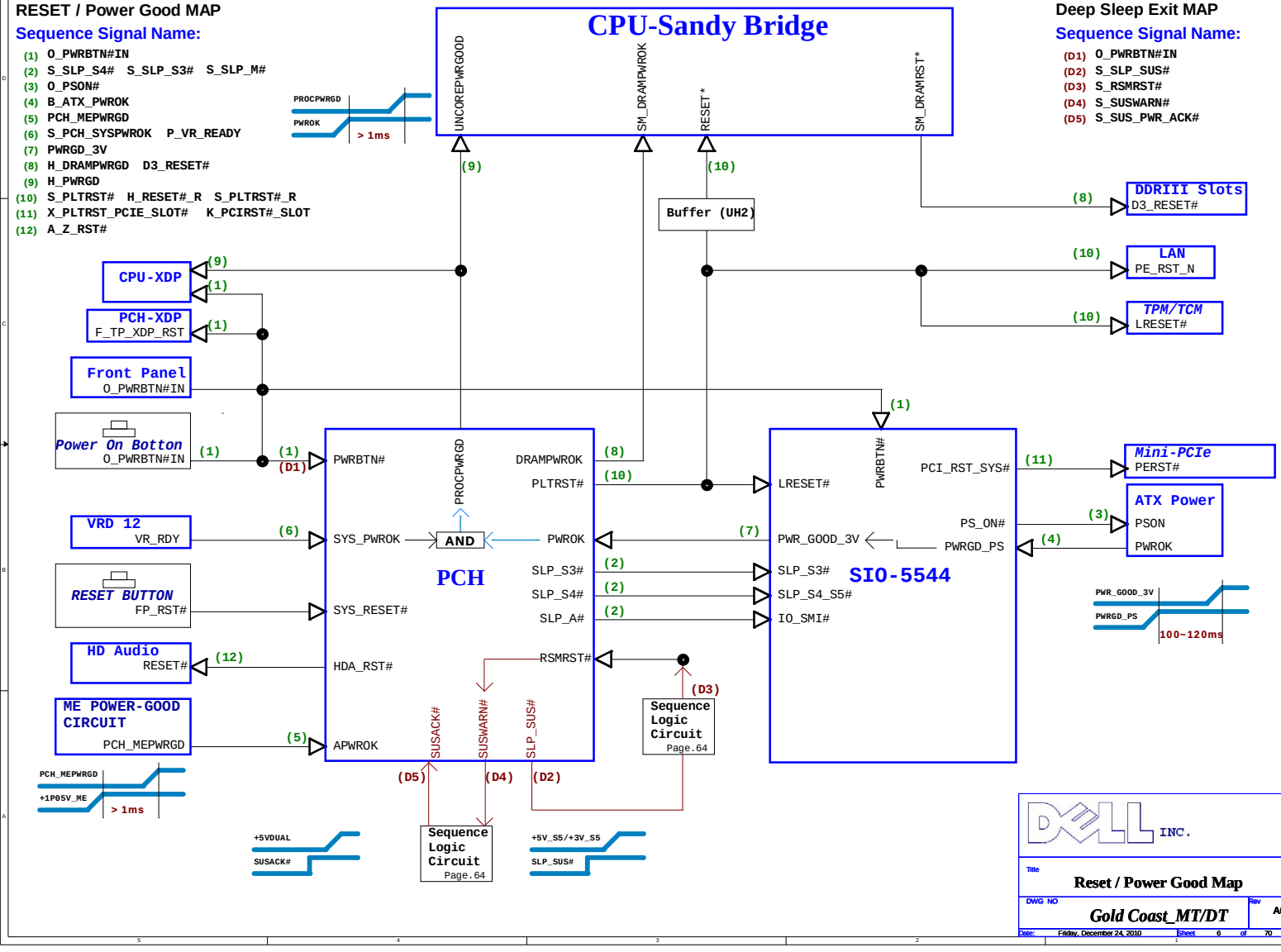
Sequence Signal Name:

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) S_PLTRST# H_RESET#_R S_PLTRST#_R
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#

Deep Sleep Exit MAP

Sequence Signal Name:

(D1) O_PWRBTN#IN
(D2) S_SLP_SUS#
(D3) S_RSMRST#
(D4) S_SUSWARN#
(D5) S_SUS_PWR_ACK#



DELL INC.

Title: Reset / Power Good Map

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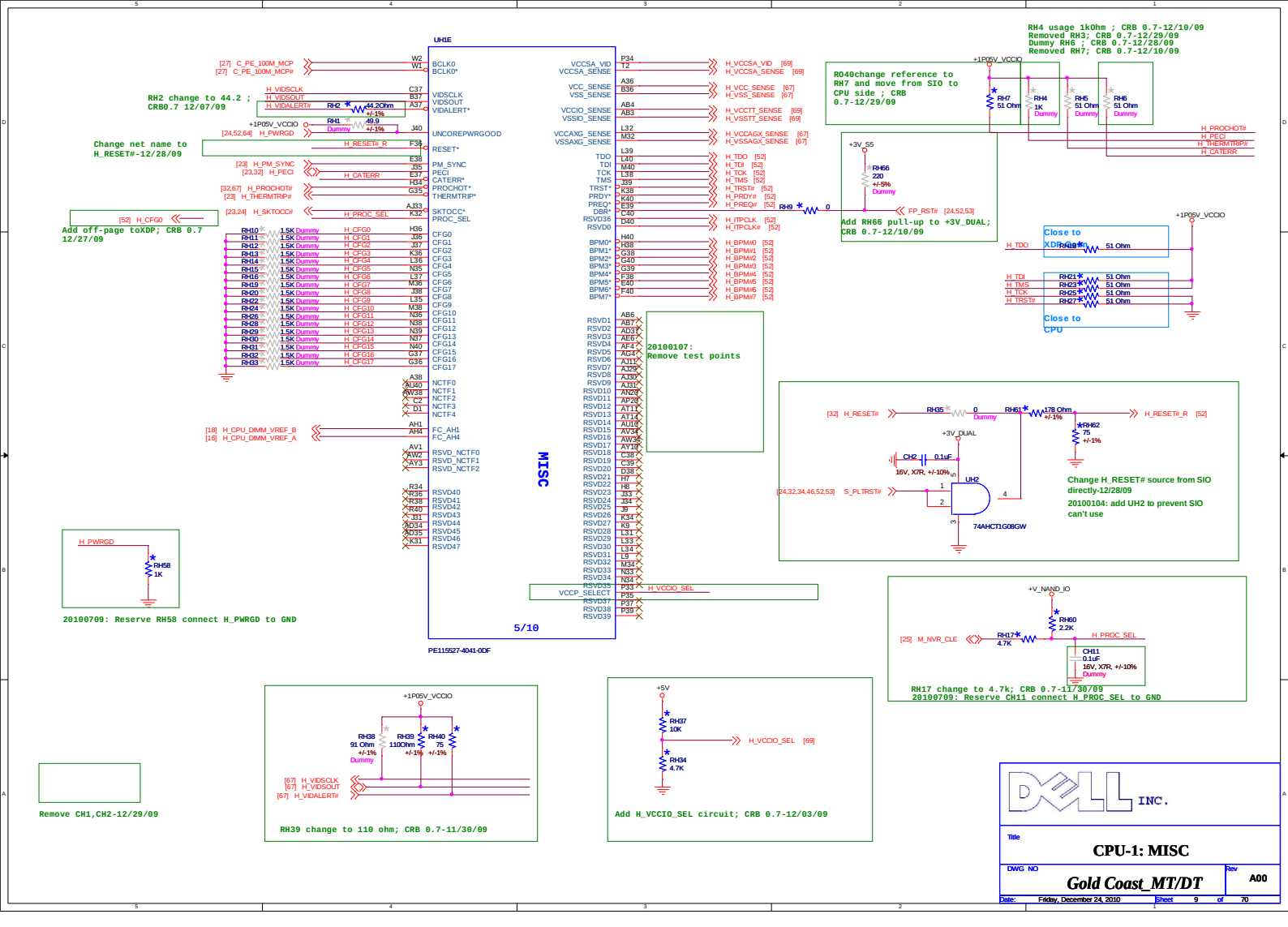
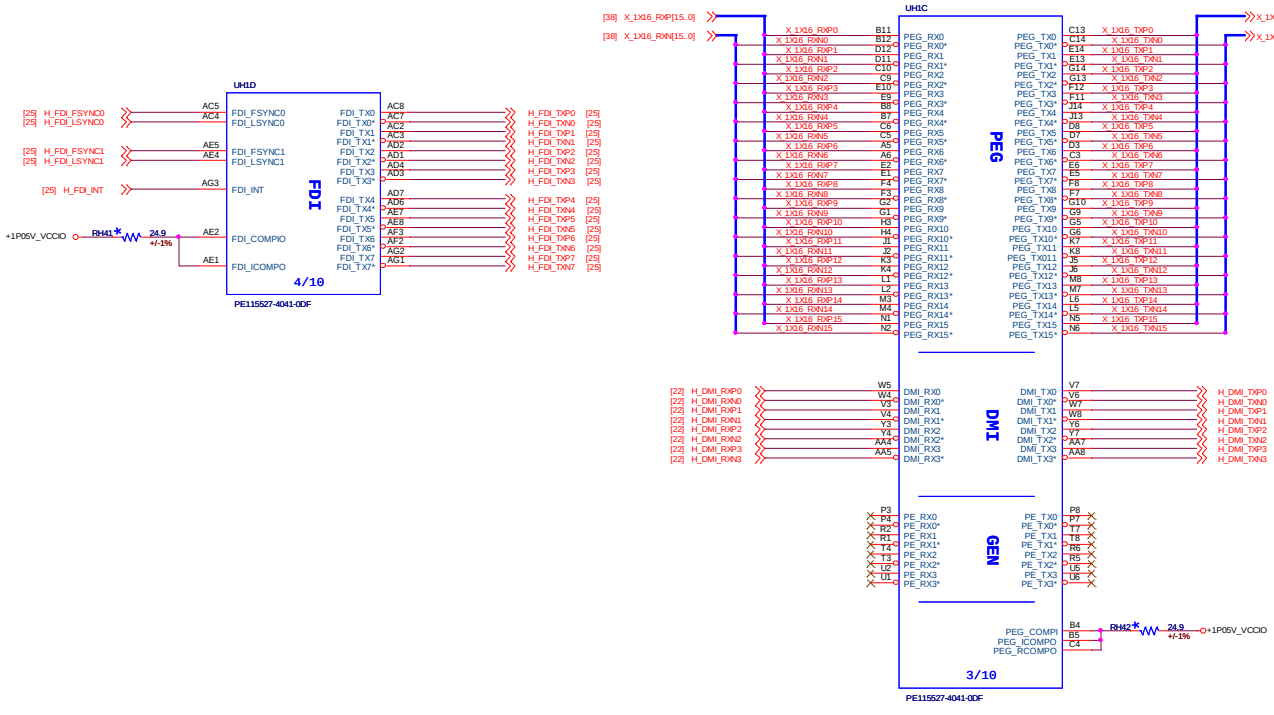

RH4 usage 1kOhm ; CRB 0.7-12/10/09
Removed RH3; CRB 0.7-12/29/09
Dummy RH6 ; CRB 0.7-12/28/09
Removed RH7; CRB 0.7-12/10/09
RO40change reference to RH7 and move from SIO to CPU side ; CRB 0.7-12/29/09
RH2 change to 44.2 ; CRB0.7 12/07/09
Change net name to H_RESET#-12/28/09
Add off-page toXDP; CRB 0.7 12/27/09
Add RH66 pull-up to +3V_DUAL; CRB 0.7-12/10/09
Close to XDP
Close to CPU
20100107: Remove test points
Change H_RESET# source from SIO directly-12/28/09
20100104: add UH2 to prevent SIO can't use
20100709: Reserve RH58 connect H_PWRGD to GND
RH17 change to 4.7k; CRB 0.7-11/30/09
20100709: Reserve CH11 connect H_PROC_SEL to GND
RH39 change to 110 ohm; CRB 0.7-11/30/09
Add H_VCCIO_SEL circuit; CRB 0.7-12/03/09
Remove CH1,CH2-12/29/09
MISC
5/10
PE115527-4041-0DF
74AHCT1G08GW
DELL INC.
CPU-1: MISC
Gold Coast_MT/DT
A00
Friday, December 24, 2010



Title	CPU-2: FDI/PCIe/DMI
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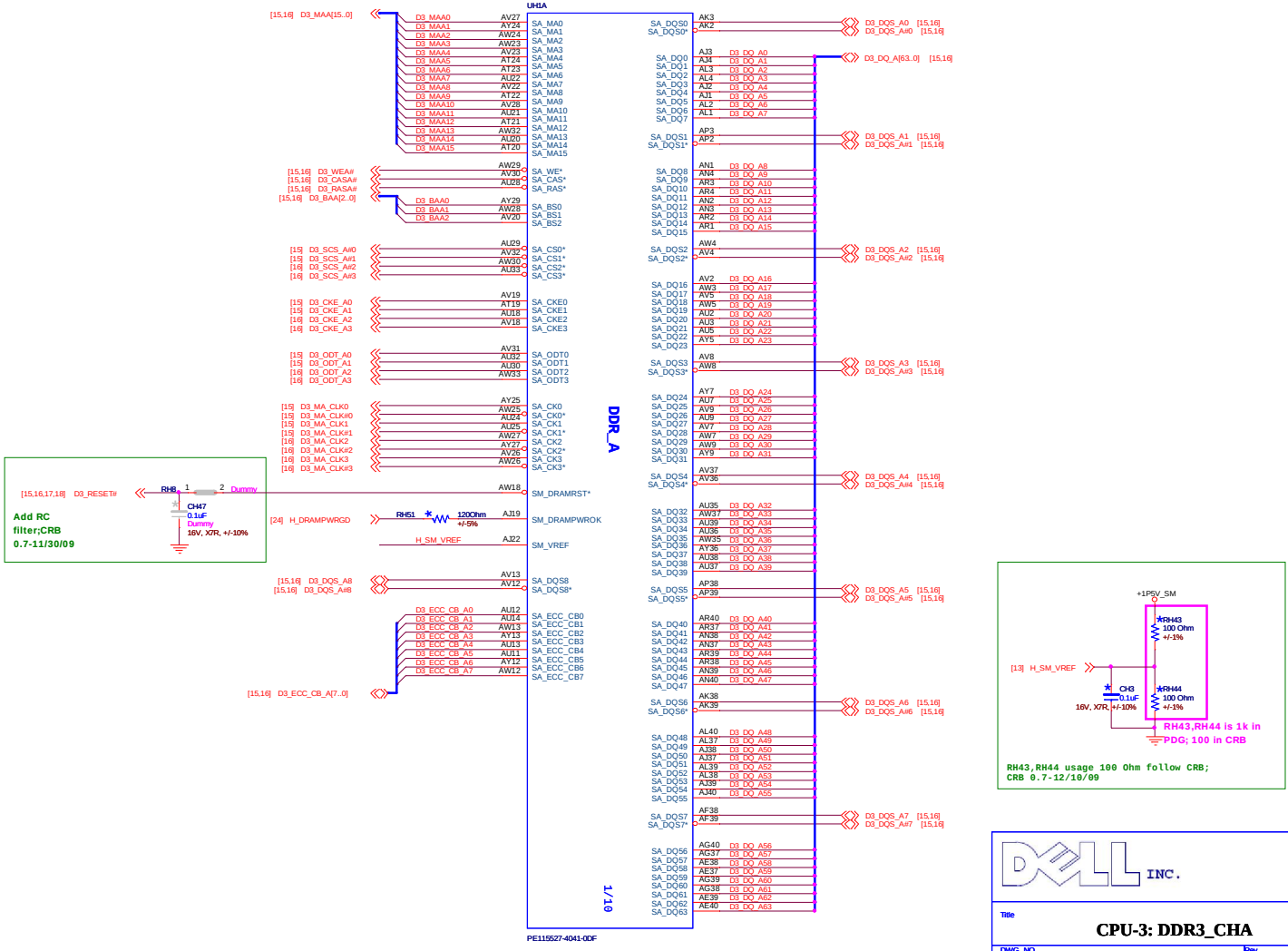

DELL INC.

Title

CPU-3: DDR3_CHA

DWG NO

Gold Coast_MT/DT

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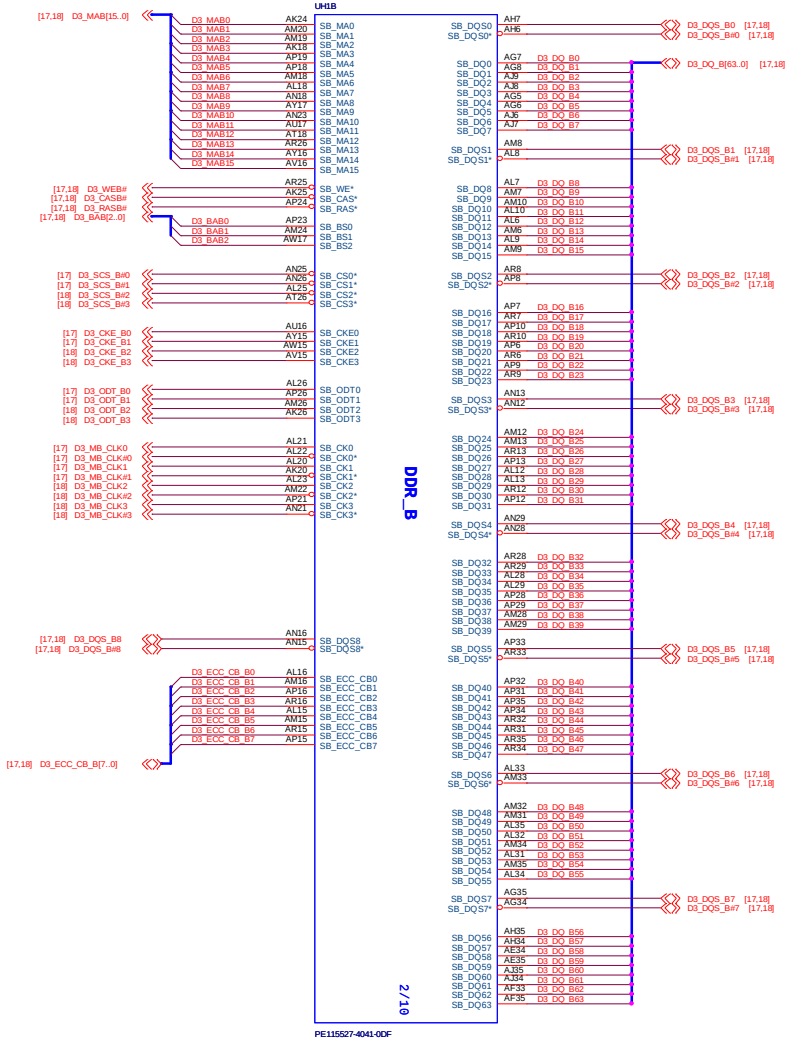

DELL INC.

Title: CPU-4: DDR3_CHB

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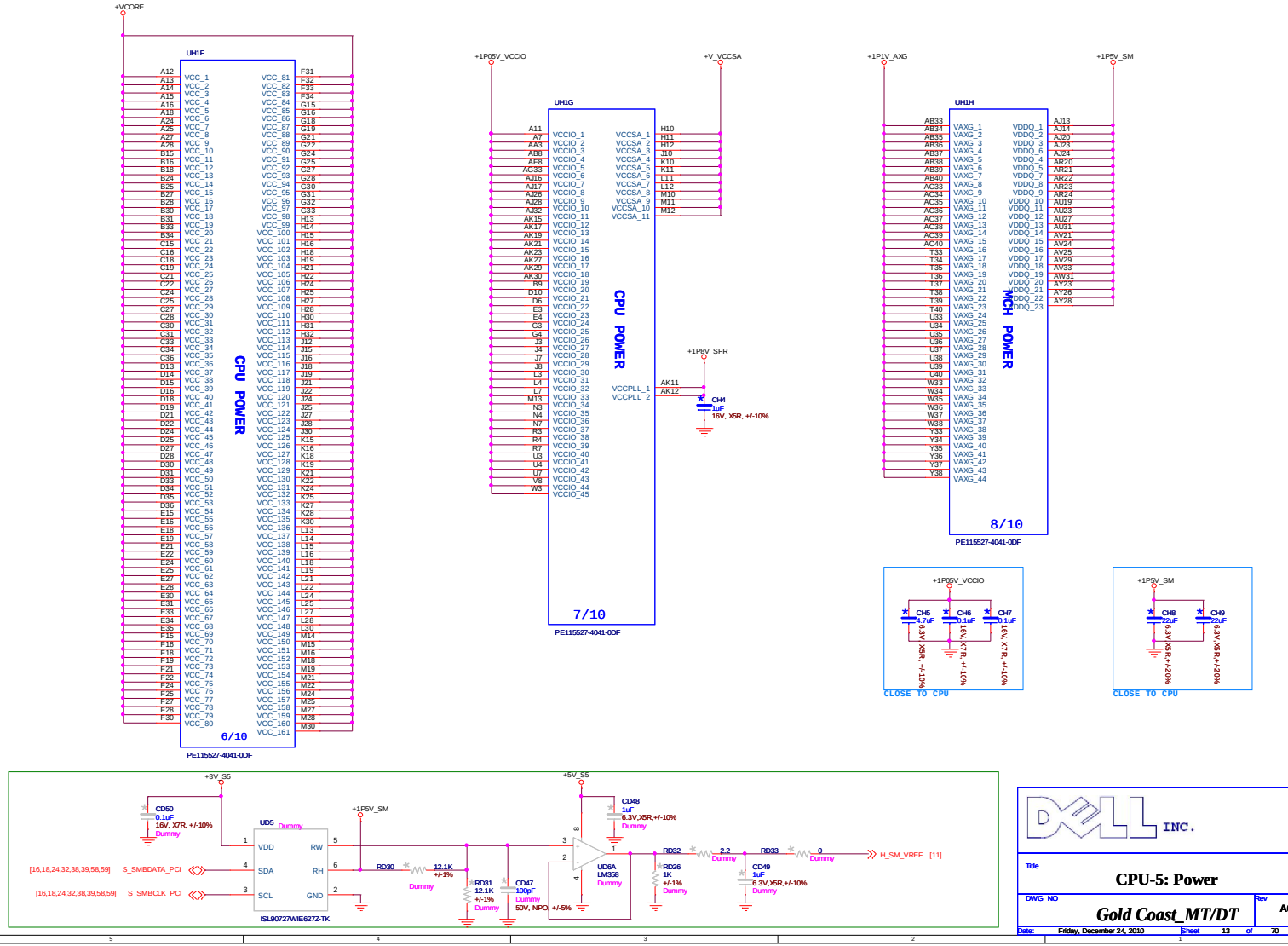
+VCORE
UH1F
CPU POWER
6/10
PE115527-4041-0DF
+1P05V_VCCIO
+V_VCCSA
UH1G
CPU POWER
7/10
PE115527-4041-0DF
+1P8V_SFR
CH4
1uF
16V, X5R, +/-10%
+1P1V_AXG
+1P5V_SM
UH1H
MCH POWER
8/10
PE115527-4041-0DF
+1P05V_VCCIO
CH5
4.7uF
6.3V, X5R, +/-10%
CH6
0.1uF
16V, X7R, +/-10%
CH7
0.1uF
16V, X7R, +/-10%
CLOSE TO CPU
+1P5V_SM
CH8
22uF
6.3V, X5R, +/-20%
CH9
22uF
6.3V, X5R, +/-20%
CLOSE TO CPU
+3V_S5
CD50
0.1uF
16V, X7R, +/-10%
Dummy
UD5
Dummy
VDD
SDA
SCL
RW
RH
GND
ISL9027WIE627Z-TK
[16,18,24,32,38,39,58,59]
S_SMBDATA_PCI
[16,18,24,32,38,39,58,59]
S_SMBCLK_PCI
+1P5V_SM
RD30
12.1K
+/-1%
Dummy
RD31
12.1K
+/-1%
Dummy
CD47
100pF
Dummy
50V, NPO
+/-5%
+5V_S5
CD48
1uF
6.3V, X5R, +/-10%
Dummy
UD6A
LM358
Dummy
RD32
1K
+/-1%
Dummy
RD33
2.2
Dummy
CD49
1uF
6.3V, X5R, +/-10%
Dummy
0
Dummy
H_SM_VREF [11]
DELL INC.
Title
CPU-5: Power
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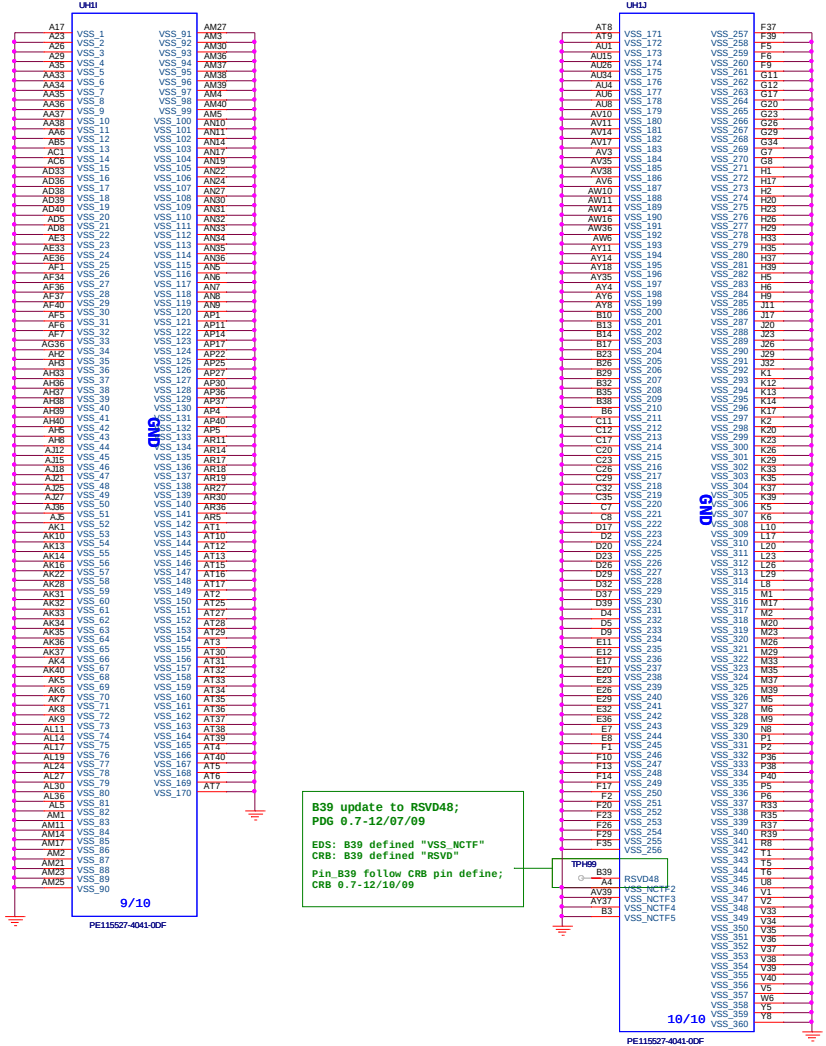
UH1I
A17 A23 A26 A29 A35 AA33 AA34 AA35 AA36 AA37 AA38 AA6 AB5 AC1 AC6 AD33 AD36 AD38 AD39 AD40 AD5 AD8 AE3 AE33 AE36 AF1 AF34 AF36 AF37 AF40 AF5 AF6 AF7 AG36 AH2 AH3 AH33 AH36 AH37 AH38 AH39 AH40 AH5 AH8 AJ12 AJ15 AJ18 AJ21 AJ25 AJ27 AJ36 AK1 AK10 AK13 AK14 AK16 AK22 AK28 AK31 AK32 AK33 AK34 AK35 AK36 AK37 AK4 AK40 AK5 AK6 AK7 AK8 AK9 AL11 AL14 AL17 AL19 AL24 AL27 AL30 AL36 AL5 AM1 AM11 AM14 AM17 AM2 AM21 AM23 AM25
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90
VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138 VSS_139 VSS_140 VSS_141 VSS_142 VSS_143 VSS_144 VSS_145 VSS_146 VSS_147 VSS_148 VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170
AM27 AM3 AM30 AM36 AM37 AM38 AM39 AM4 AM40 AM5 AM10 AN11 AN14 AN17 AN19 AN22 AN24 AN27 AN30 AN31 AN32 AN33 AN34 AN35 AN36 AN5 AN6 AN7 AN8 AN9 AP1 AP11 AP14 AP17 AP22 AP25 AP27 AP30 AP36 AP37 AP4 AP40 AP5 AR11 AR14 AR17 AR18 AR19 AR27 AR30 AR36 AR5 AT1 AT10 AT12 AT13 AT15 AT16 AT17 AT2 AT25 AT27 AT28 AT29 AT3 AT30 AT31 AT32 AT33 AT34 AT35 AT36 AT37 AT38 AT39 AT4 AT40 AT5 AT6 AT7
GND
9/10
PE115527-4041-0DF
B39 update to RSVD48;
PDG 0.7-12/07/09
EDS: B39 defined "VSS_NCTF"
CRB: B39 defined "RSVD"
Pin_B39 follow CRB pin define;
CRB 0.7-12/10/09
UH1J
AT8 AT9 AU1 AU15 AU26 AU34 AU4 AU6 AU8 AV10 AV11 AV14 AV17 AV3 AV35 AV38 AV6 AW10 AW11 AW14 AW16 AW36 AW6 AY11 AY14 AY18 AY35 AY4 AY6 AY8 B10 B13 B14 B17 B23 B26 B29 B32 B35 B38 B6 C11 C12 C17 C20 C23 C26 C29 C32 C35 C7 C8 D17 D2 D20 D23 D26 D29 D32 D37 D39 D4 D5 D9 E11 E12 E17 E20 E23 E26 E29 E32 E36 E7 E8 F1 F10 F13 F14 F17 F2 F20 F23 F26 F29 F35
VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179 VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198 VSS_199 VSS_200 VSS_201 VSS_202 VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220 VSS_221 VSS_222 VSS_223 VSS_224 VSS_225 VSS_226 VSS_227 VSS_228 VSS_229 VSS_230 VSS_231 VSS_232 VSS_233 VSS_234 VSS_235 VSS_236 VSS_237 VSS_238 VSS_239 VSS_240 VSS_241 VSS_242 VSS_243 VSS_244 VSS_245 VSS_246 VSS_247 VSS_248 VSS_249 VSS_250 VSS_251 VSS_252 VSS_253 VSS_254 VSS_255 VSS_256
VSS_257 VSS_258 VSS_259 VSS_260 VSS_261 VSS_262 VSS_263 VSS_264 VSS_265 VSS_266 VSS_267 VSS_268 VSS_269 VSS_270 VSS_271 VSS_272 VSS_273 VSS_274 VSS_275 VSS_276 VSS_277 VSS_278 VSS_279 VSS_280 VSS_281 VSS_282 VSS_283 VSS_284 VSS_285 VSS_286 VSS_287 VSS_288 VSS_289 VSS_290 VSS_291 VSS_292 VSS_293 VSS_294 VSS_295 VSS_296 VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305 VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313 VSS_314 VSS_315 VSS_316 VSS_317 VSS_318 VSS_319 VSS_320 VSS_321 VSS_322 VSS_323 VSS_324 VSS_325 VSS_326 VSS_327 VSS_328 VSS_329 VSS_330 VSS_331 VSS_332 VSS_333 VSS_334 VSS_335 VSS_336 VSS_337 VSS_338 VSS_339 VSS_340 VSS_341 VSS_342 VSS_343 VSS_344 VSS_345 VSS_346 VSS_347 VSS_348 VSS_349 VSS_350 VSS_351 VSS_352 VSS_353 VSS_354 VSS_355 VSS_356 VSS_357 VSS_358 VSS_359 VSS_360
F37 F39 F5 F6 F9 G11 G12 G17 G20 G23 G26 G29 G34 G7 G8 H1 H17 H2 H20 H23 H26 H29 H33 H35 H37 H39 H5 H6 H9 J11 J17 J20 J23 J26 J29 J32 K1 K12 K13 K14 K17 K2 K20 K23 K26 K29 K33 K35 K37 K39 K5 K6 L10 L17 L20 L23 L26 L29 L8 M1 M17 M2 M20 M23 M26 M29 M33 M35 M37 M39 M5 M6 M9 N8 P1 P2 P36 P38 P40 P5 P6 R33 R35 R37 R39 R8 T1 T5 T6 T8 V1 V2 V33 V34 V35 V36 V37 V38 V39 V40 V5 W6 Y5 Y8
GND
TPH99
B39
A1 RSVD48
AV39 VSS_NCTF2
AY37 VSS_NCTF3
B3 VSS_NCTF4
VSS_NCTF5
10/10
PE115527-4041-0DF
MLH1 MLH
MLH2 MLH
MLH3 MLH
MLH4 MLH
2D lable
UH1_1
Backplate
UH1_B
Backplate
DELL INC.
Title
CPU-6: GND
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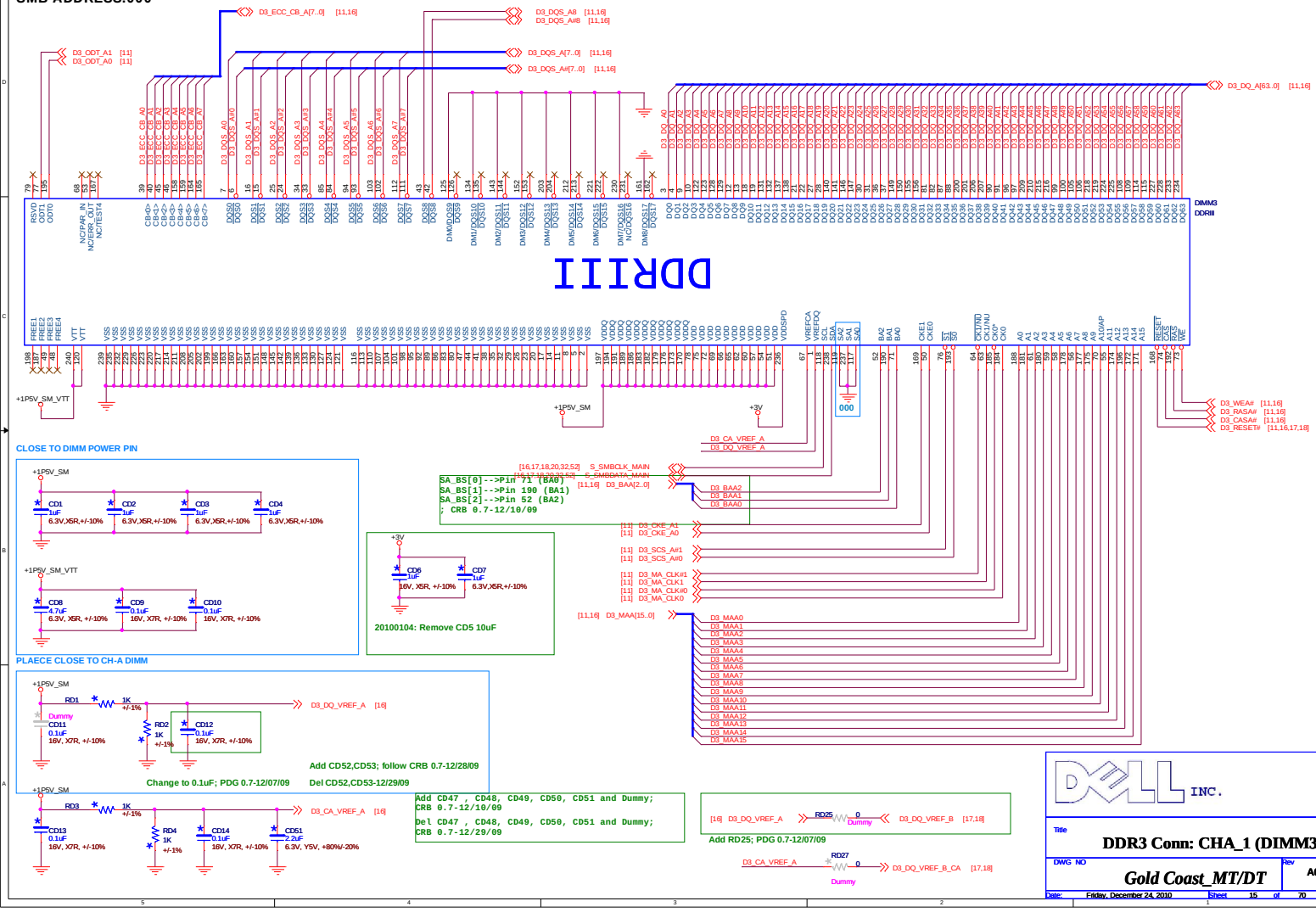
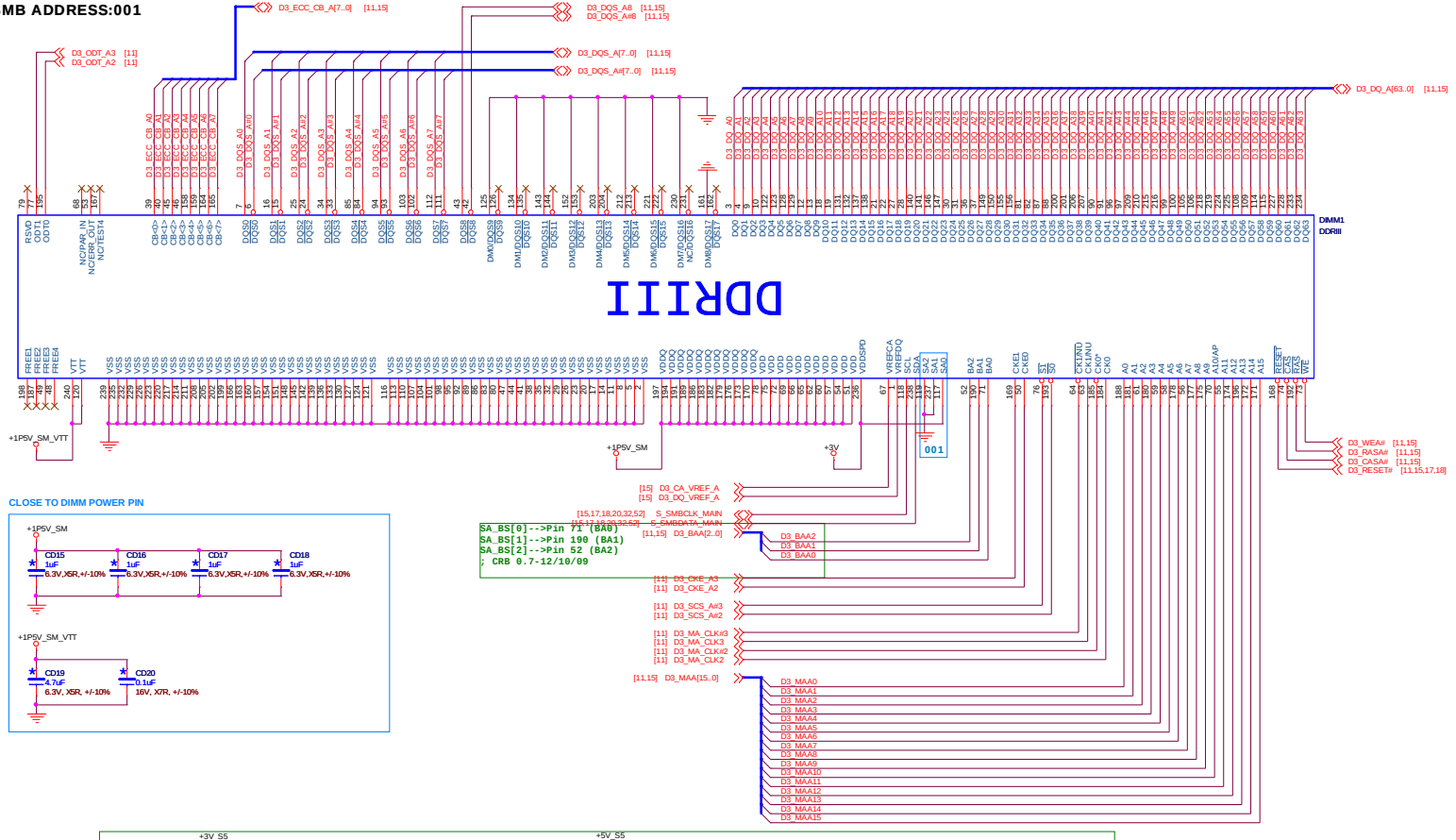
CHANNEL A BANK 1
SMB ADDRESS:000



CHANNEL A BANK 2
SMB ADDRESS:001



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Title	DDR3 Conn: CHA_2 (DIMM1)
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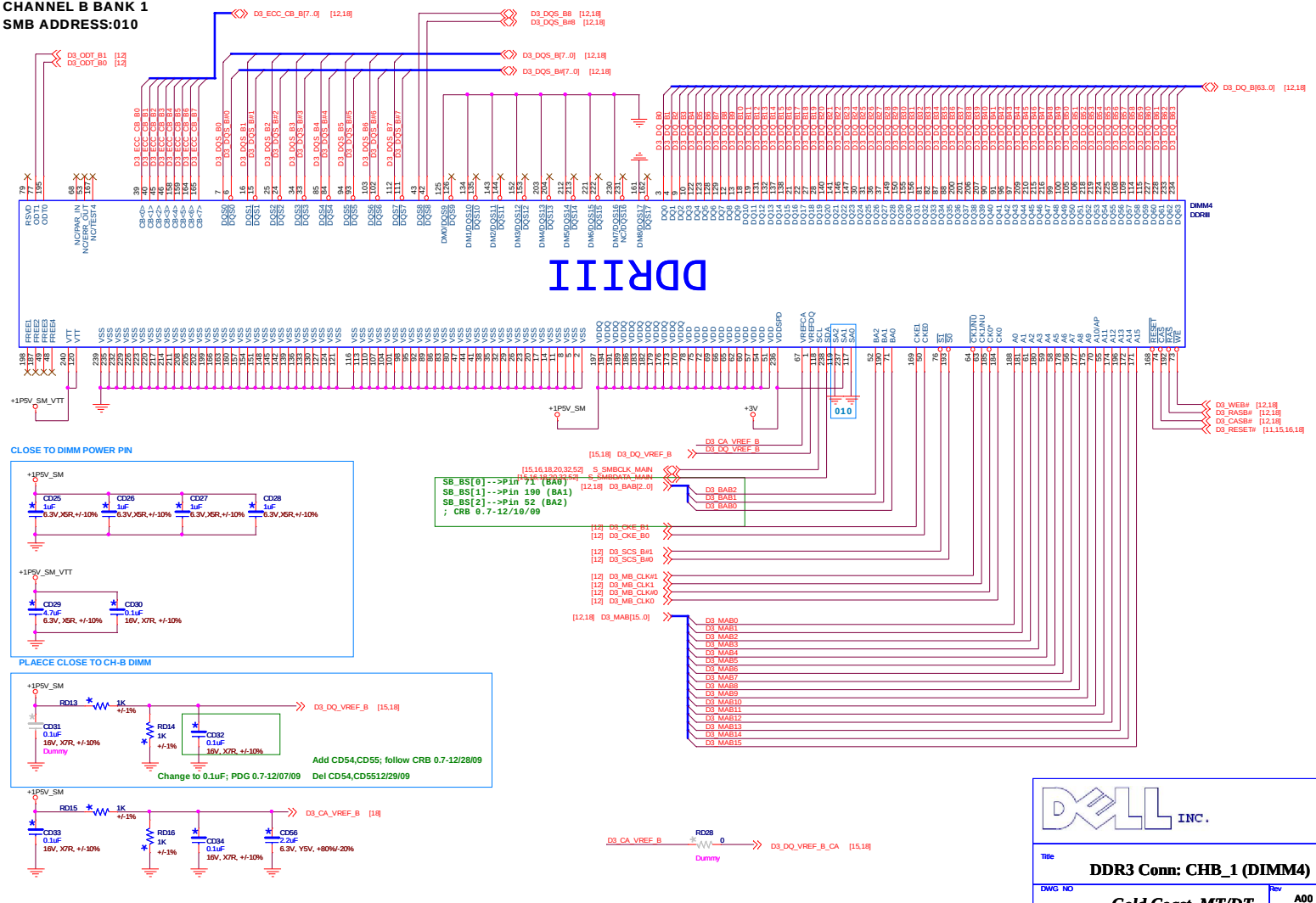
CHANNEL B BANK 1
SMB ADDRESS:010



Title	DDR3 Conn: CHB_1 (DIMM4)
DWG NO	Gold Coast_MT/DT
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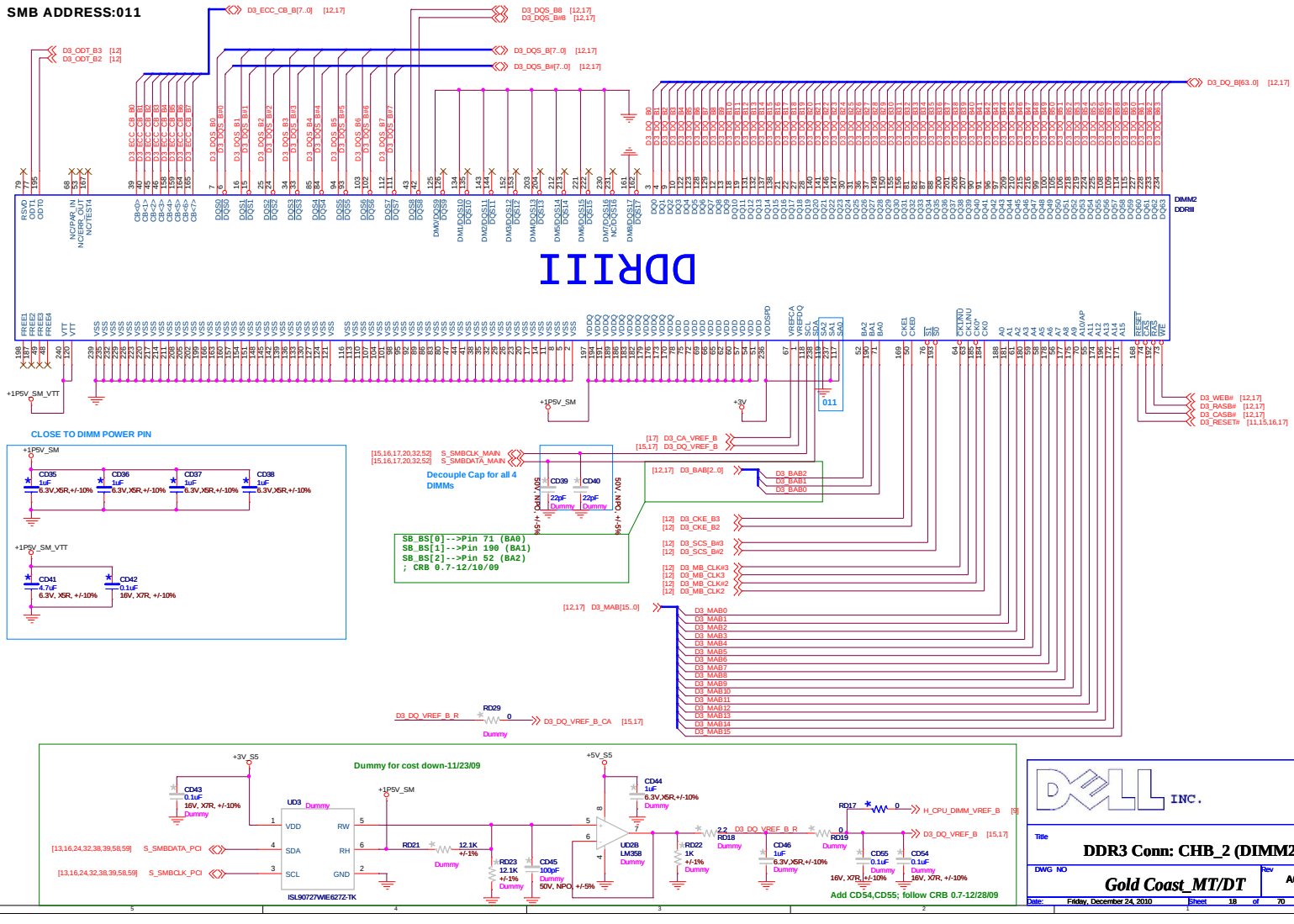
CHANNEL B BANK 2
SMB ADDRESS:011
DDRIII
DIMM2
DDRIII
CLOSE TO DIMM POWER PIN
Decouple Cap for all 4 DIMMs
SB_BS[0]-->Pin 71 (BA0)
SB_BS[1]-->Pin 190 (BA1)
SB_BS[2]-->Pin 52 (BA2)
; CRB 0.7-12/10/09
Dummy for cost down-11/23/09
Add CD54,CD55; follow CRB 0.7-12/28/09
ISL90727WIE627Z-TK
DELL INC.
DDR3 Conn: CHB_2 (DIMM2)
Gold Coast_MT/DT
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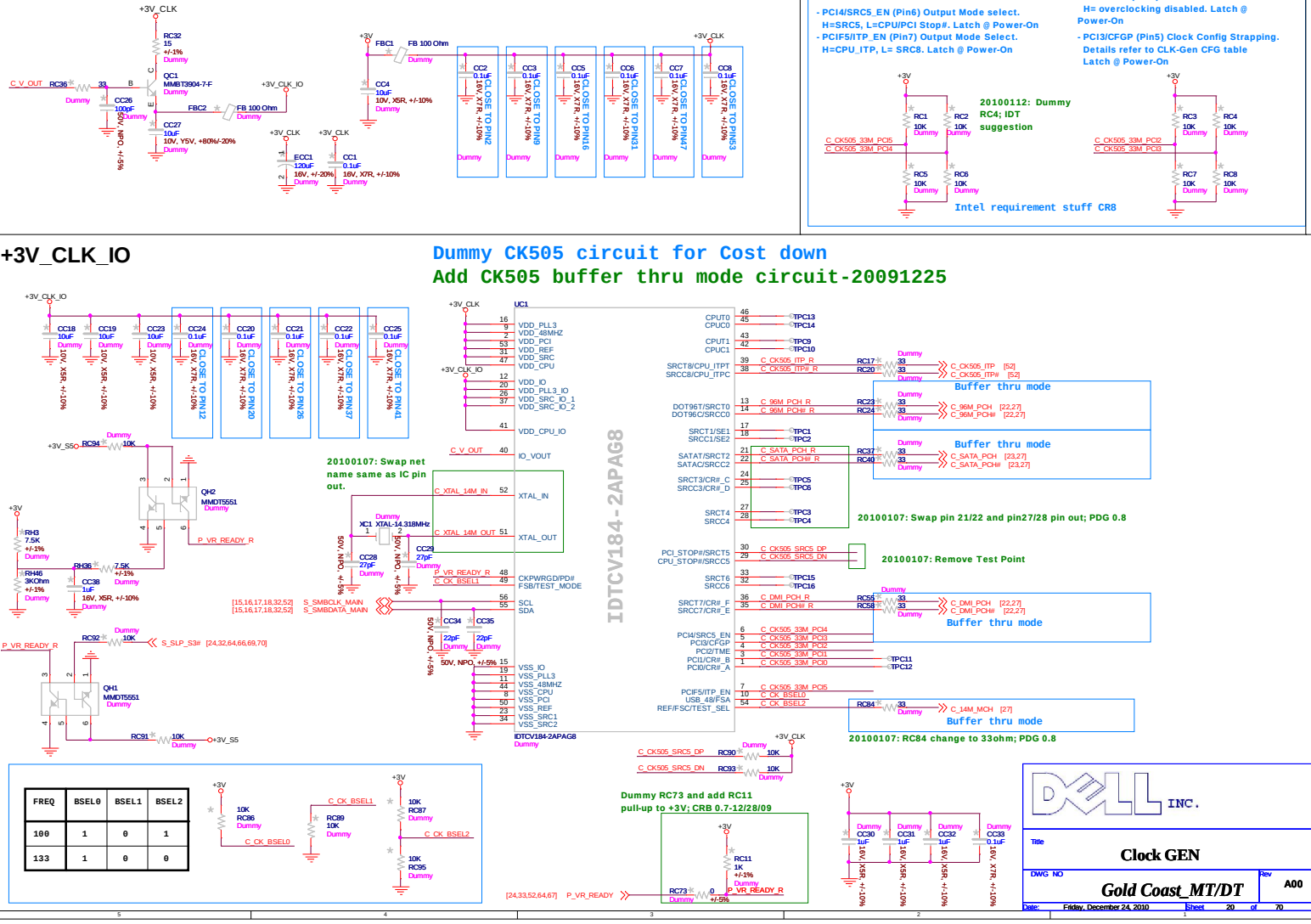
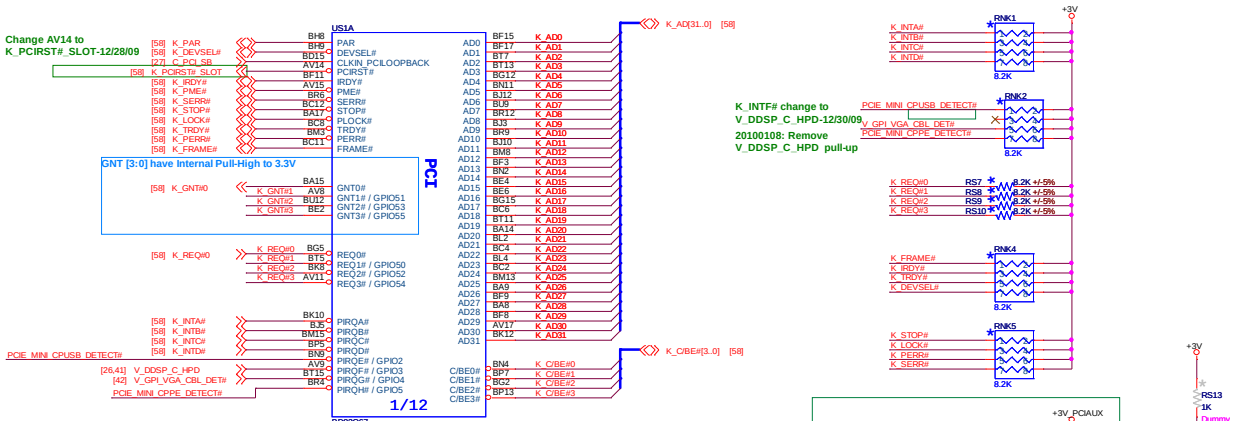
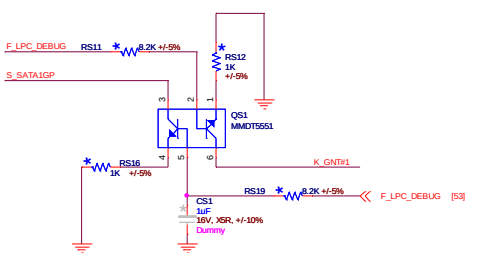
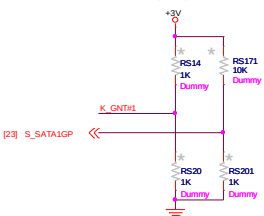

+3V_CLK_IO
Dummy CK505 circuit for Cost down
Add CK505 buffer thru mode circuit-20091225
- PCI4/SRC5_EN (Pin6) Output Mode select.
H=SRC5, L=CPU/PCI Stop#. Latch @ Power-On
- PCIF5/ITP_EN (Pin7) Output Mode Select.
H=CPU_ITP, L= SRC8. Latch @ Power-On
- PCI2/TME (Pin4) Trust Mode Enable.
H= overclocking disabled. Latch @ Power-On
- PCI3/CFGP (Pin5) Clock Config Strapping.
Details refer to CLK-Gen CFG table
Latch @ Power-On
20100112: Dummy RC4; IDT suggestion
Intel requirement stuff CR8
IDTCV184-2APAG8
20100107: Swap net name same as IC pin out.
20100107: Swap pin 21/22 and pin27/28 pin out; PDG 0.8
20100107: Remove Test Point
20100107: RC84 change to 33ohm; PDG 0.8
Buffer thru mode
Dummy RC73 and add RC11 pull-up to +3V; CRB 0.7-12/28/09
FREQ BSEL0 BSEL1 BSEL2
100 1 0 1
133 1 0 0
DELL INC.
Title
Clock GEN
DWG NO
Gold Coast_MT/DT
Rev
A00
Date: Friday, December 24, 2010
Sheet 20 of 70





S_SATA1GP has external 10k pull-up; CRB 0.7



20091209: Have to check with Intel

20091230: Reserved RS171 and RS201 for Boot select

Boot BIOS Select

Boot Device	GNT1	SATA1GP
LPC	0	0
PCI	1	0
NAND	0	1
SPI	1	1

GNT3# Internal pull-up.

DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode

GNT2#/GPIO53:ESI strap for server platform
ONLY,Do not pull low.

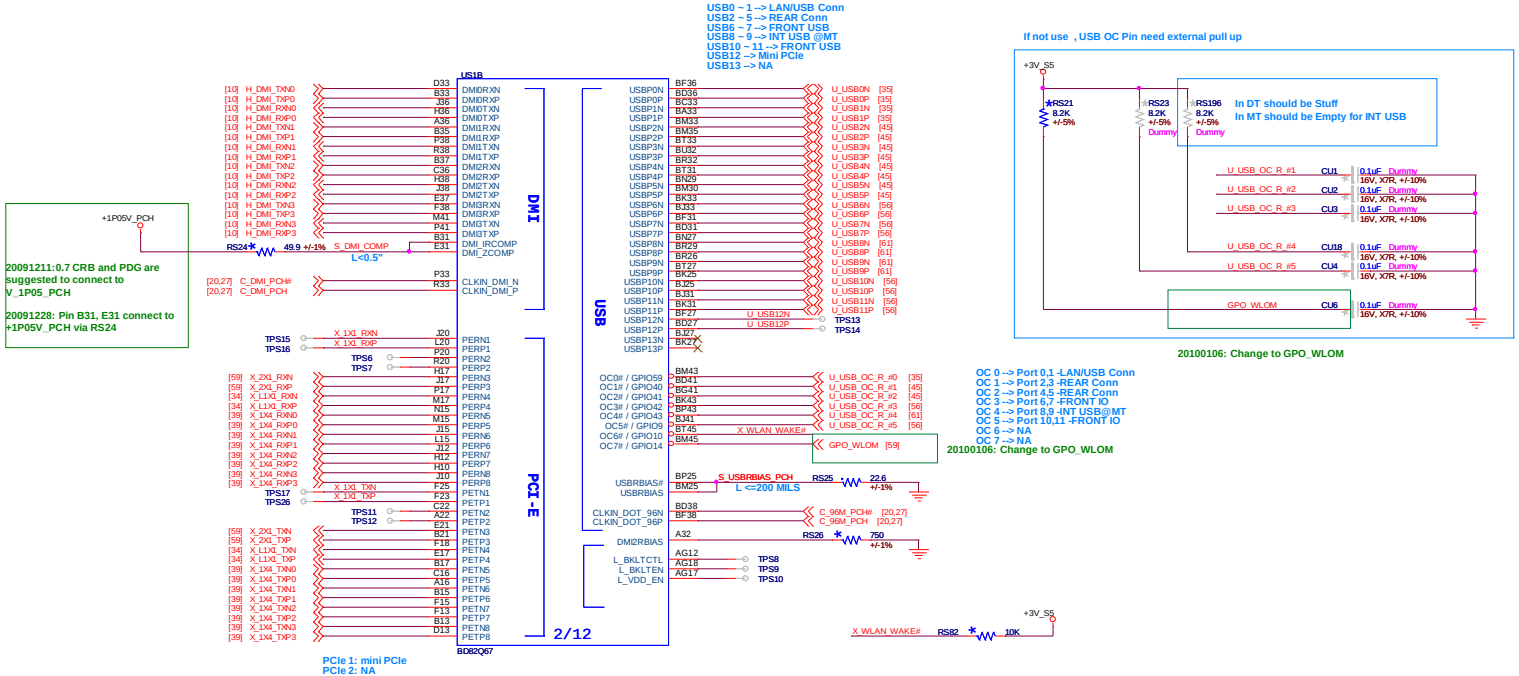
DELL INC.

Title: **PCH-1: PCI**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

Date: Friday, December 24, 2010 Sheet 21 of 70



Title	PCH-2: DMI/PCIe/USB
DWG NO	Gold Coast_MT/DT
Rev	A00
Date:	Friday, December 24, 2010
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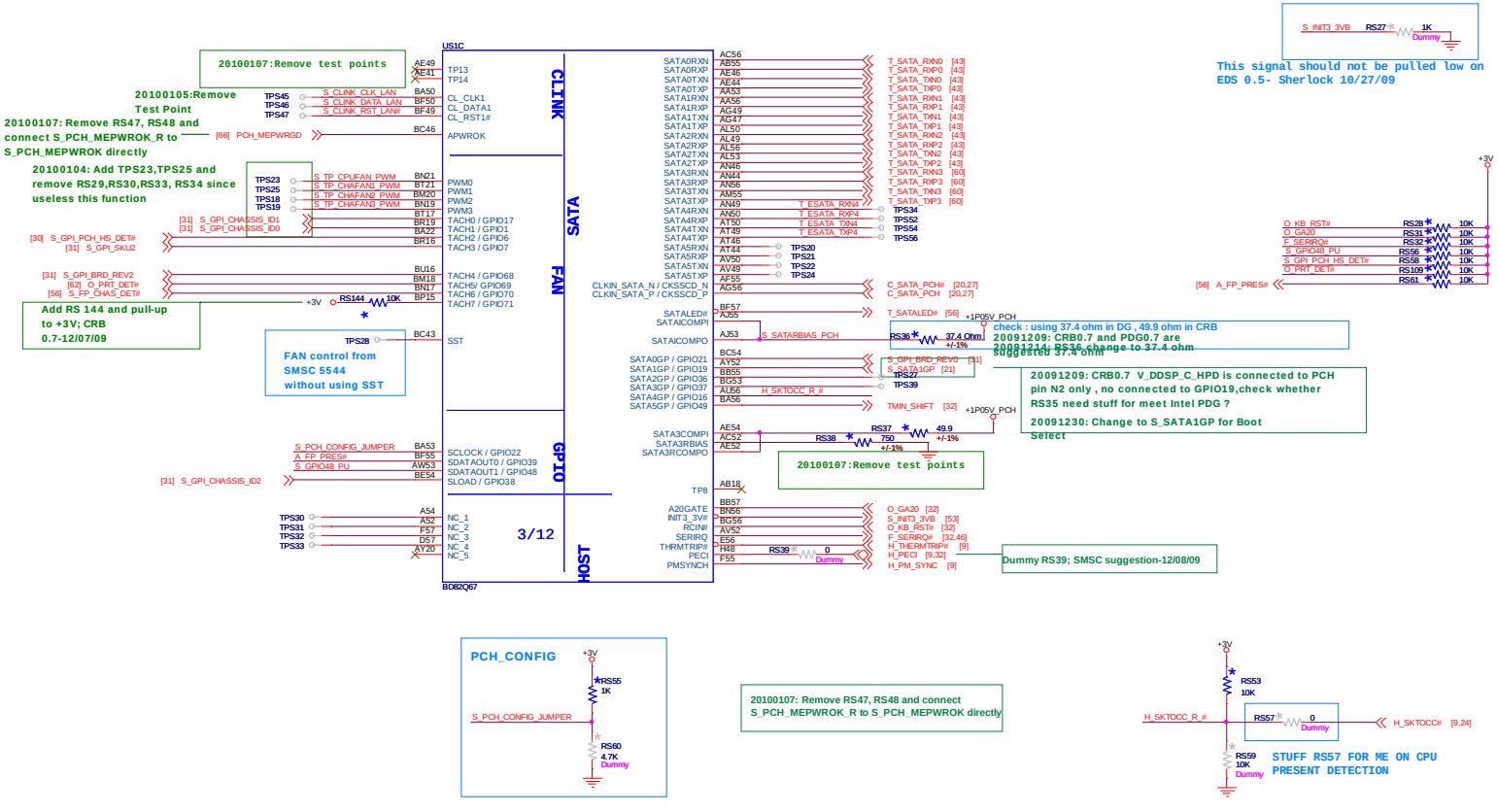

Title	PCH-3: SATA/HOST/FAN
DWG NO	Gold Coast_MT/DT
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Date:	Friday, December 24, 2010
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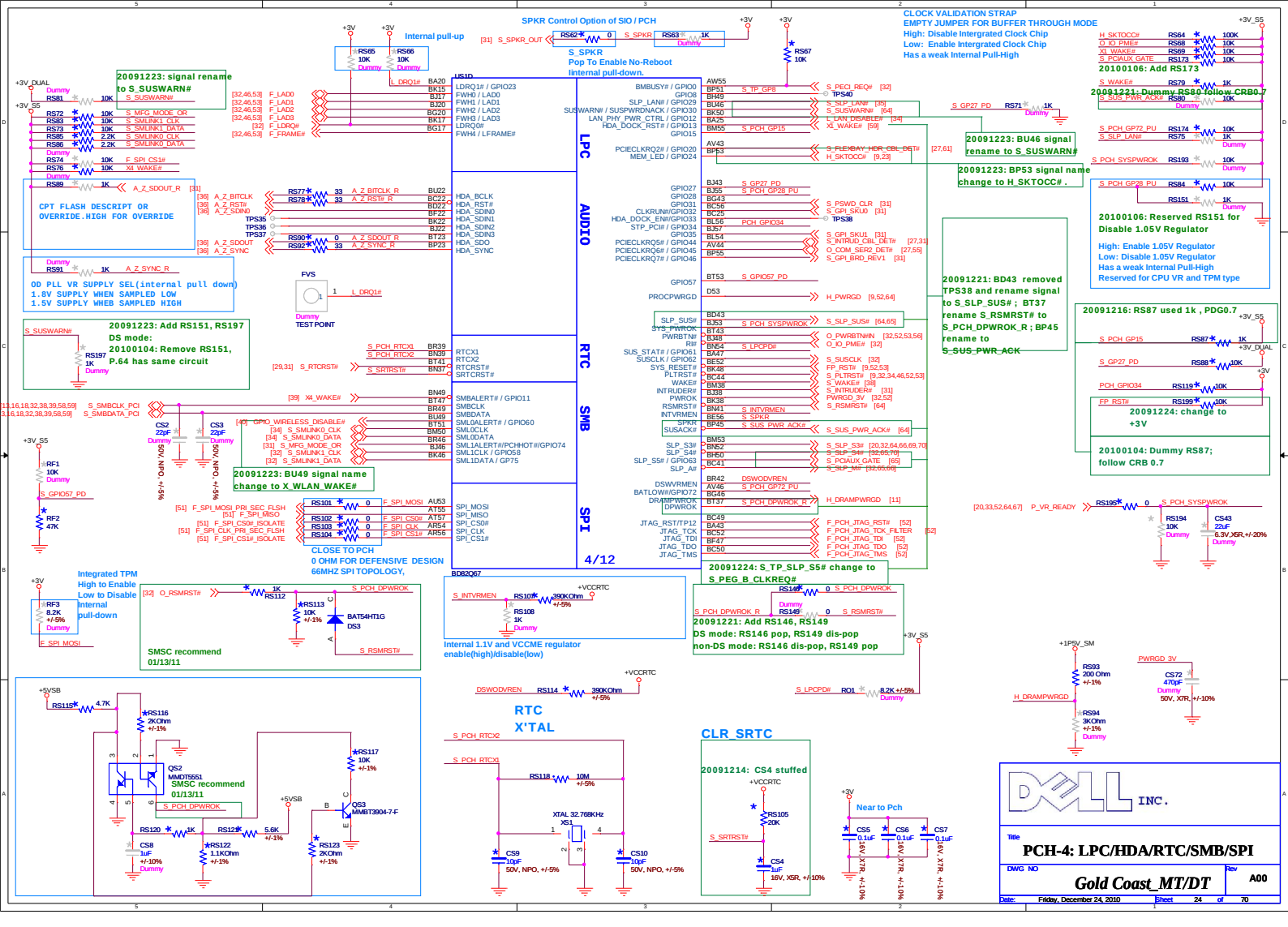
SPKR Control Option of SIO / PCH
Internal pull-up
S_SPKR
Pop To Enable No-Reboot
Internal pull-down.
CLOCK VALIDATION STRAP
EMPTY JUMPER FOR BUFFER THROUGH MODE
High: Disable Intergrated Clock Chip
Low: Enable Intergrated Clock Chip
Has a weak Internal Pull-High
20091223: signal rename to S_SUSWARN#
CPT FLASH DESCRIPT OR OVERRIDE.HIGH FOR OVERRIDE
OD PLL VR SUPPLY SEL(internal pull down)
1.8V SUPPLY WHEN SAMPLED LOW
1.5V SUPPLY WHEB SAMPLED HIGH
20091223: Add RS151, RS197
DS mode:
20100104: Remove RS151,
P.64 has same circuit
20091223: BU49 signal name change to X_WLAN_WAKE#
CLOSE TO PCH
0 OHM FOR DEFENSIVE DESIGN
66MHZ SPI TOPOLOGY,
Integrated TPM
High to Enable
Low to Disable
Internal pull-down
SMSC recommend 01/13/11
Internal 1.1V and VCCME regulator enable(high)/disable(low)
20091221: Add RS146, RS149
DS mode: RS146 pop, RS149 dis-pop
non-DS mode: RS146 dis-pop, RS149 pop
20091224: S_TP_SLP_S5# change to S_PEG_B_CLKREQ#
20091223: BU46 signal rename to S_SUSWARN#
20091223: BP53 signal name change to H_SKTOCC# .
20091221: BD43 removed TPS38 and rename signal to S_SLP_SUS# ; BT37 rename S_RSMRST# to S_PCH_DPWROK_R ; BP45 rename to S_SUS_PWR_ACK
20100106: Add RS173
20091221: Dummy RS80 follow CRB0.7
20100106: Reserved RS151 for Disable 1.05V Regulator
High: Enable 1.05V Regulator
Low: Disable 1.05V Regulator
Has a weak Internal Pull-High
Reserved for CPU VR and TPM type
20091216: RS87 used 1k , PDG0.7
20091224: change to +3V
20100104: Dummy RS87; follow CRB 0.7
RTC X'TAL
CLR_SRTC
20091214: CS4 stuffed
Near to Pch
LPC
AUDIO
RTC
SMB
SPI
4/12
PCH-4: LPC/HDA/RTC/SMB/SPI
Gold Coast_MT/DT
DELL INC.
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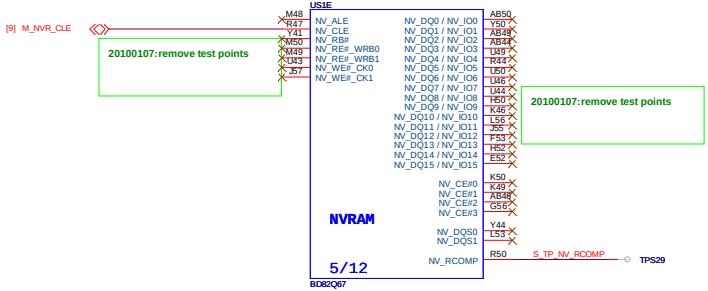
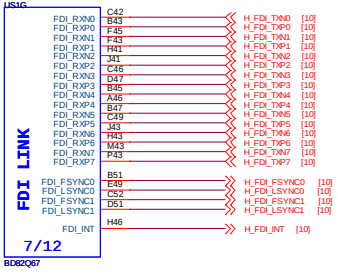
20100106: Remove ONFI function since not support

S_NVR_CLE internal pull-down.





DELL INC.

Title: PCH-5/7: NVRAM/FDI

DWG NO: Gold Coast_MT/DT

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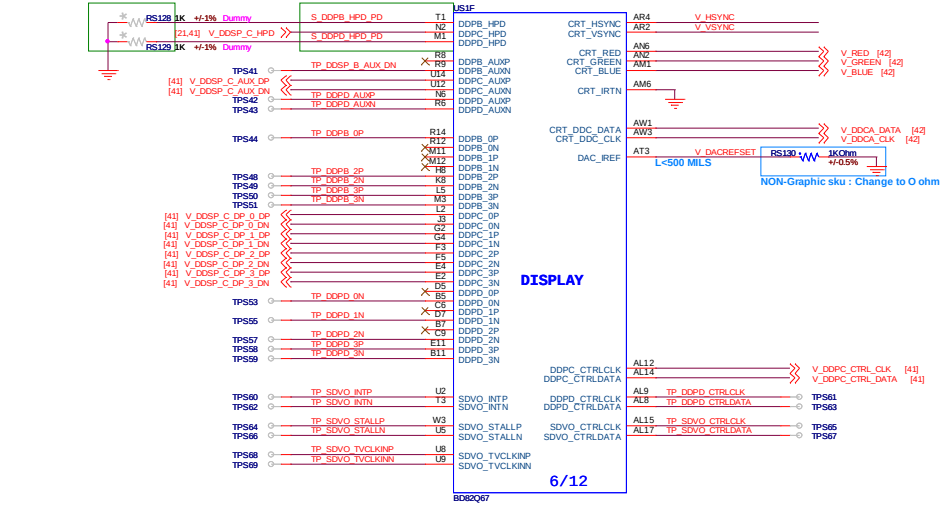
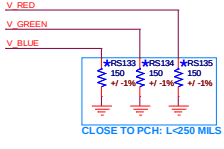
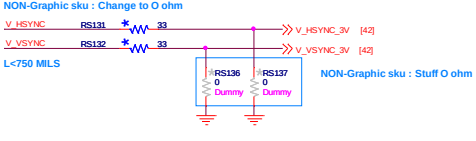
20100108: Dummy RS128,RS129: CRB 0.7

20100107: Correct pin T1 and M1 net name to S_DDPB_HPD_PD and S_DDPD_HPD_PD







DELL INC.

Title

PCH-6: Display

DWG NO

Gold Coast_MT/DT

Rev

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20100106: Remove RS96; CRB 0.7
20100106: Swap C_PCH_PCI0_R and C_PCI_SL1_R; CRB 0.7
20100106: Disconnect AT11 and left Test point; CRB 0.7

20100106: Change to 22ohm; PDG 0.8

20100107: Swap CLKOUTFLEX CLK out; PDG 0.8

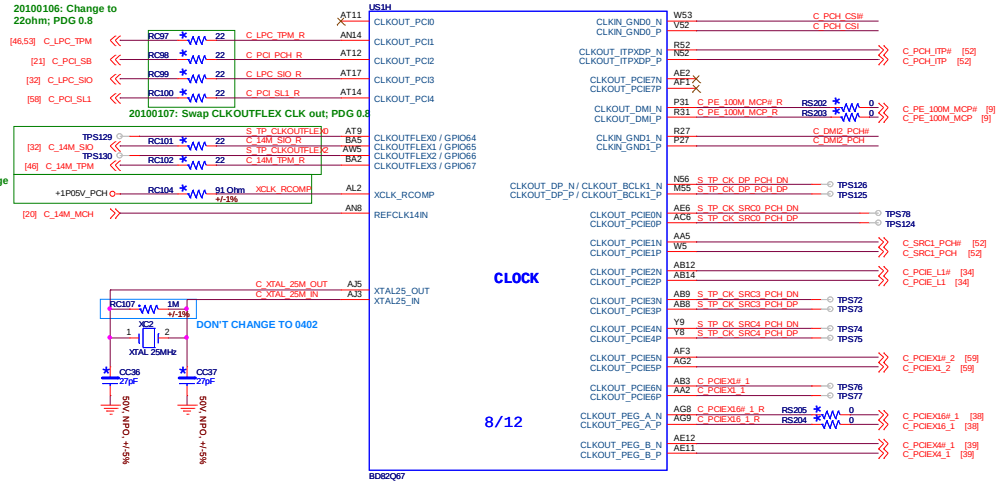
20100108: Change Power Source

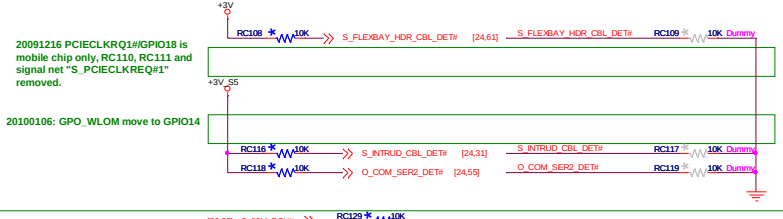
20091216 PCIECLKRQ1#/GPIO18 is mobile chip only, RC110, RC111 and signal net "S_PCIECLKREQ#1" removed.

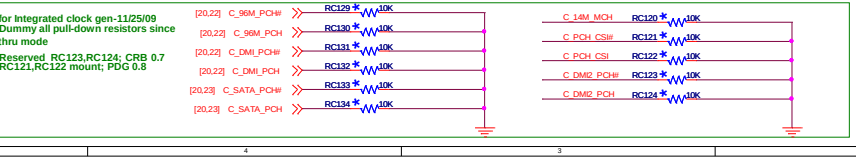
20100106: GPO_WLOM move to GPIO14

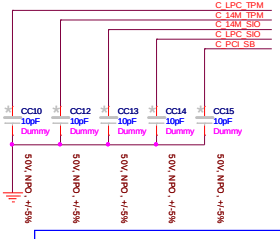
Pull-down for Integrated clock gen-11/25/09
20100105: Dummy all pull-down resistors since use buffer thru mode

20100106: Reserved_RC123,RC124; CRB 0.7
20100107: RC121,RC122 mount; PDG 0.8









DELL INC.

Title: **PCH-8: Clock**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

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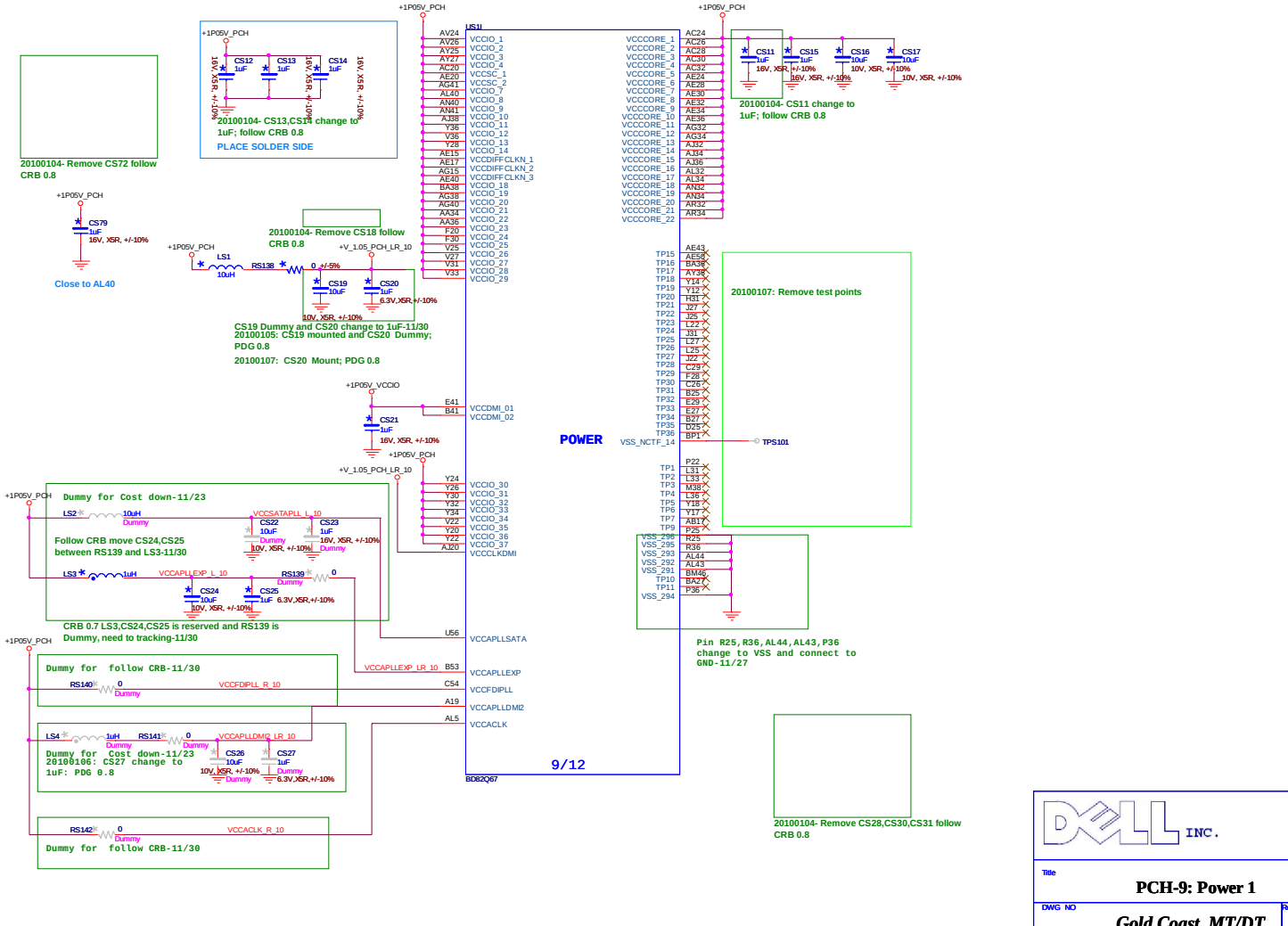

DELL INC.

Title: PCH-9: Power 1

DWG NO: Gold Coast_MT/DT

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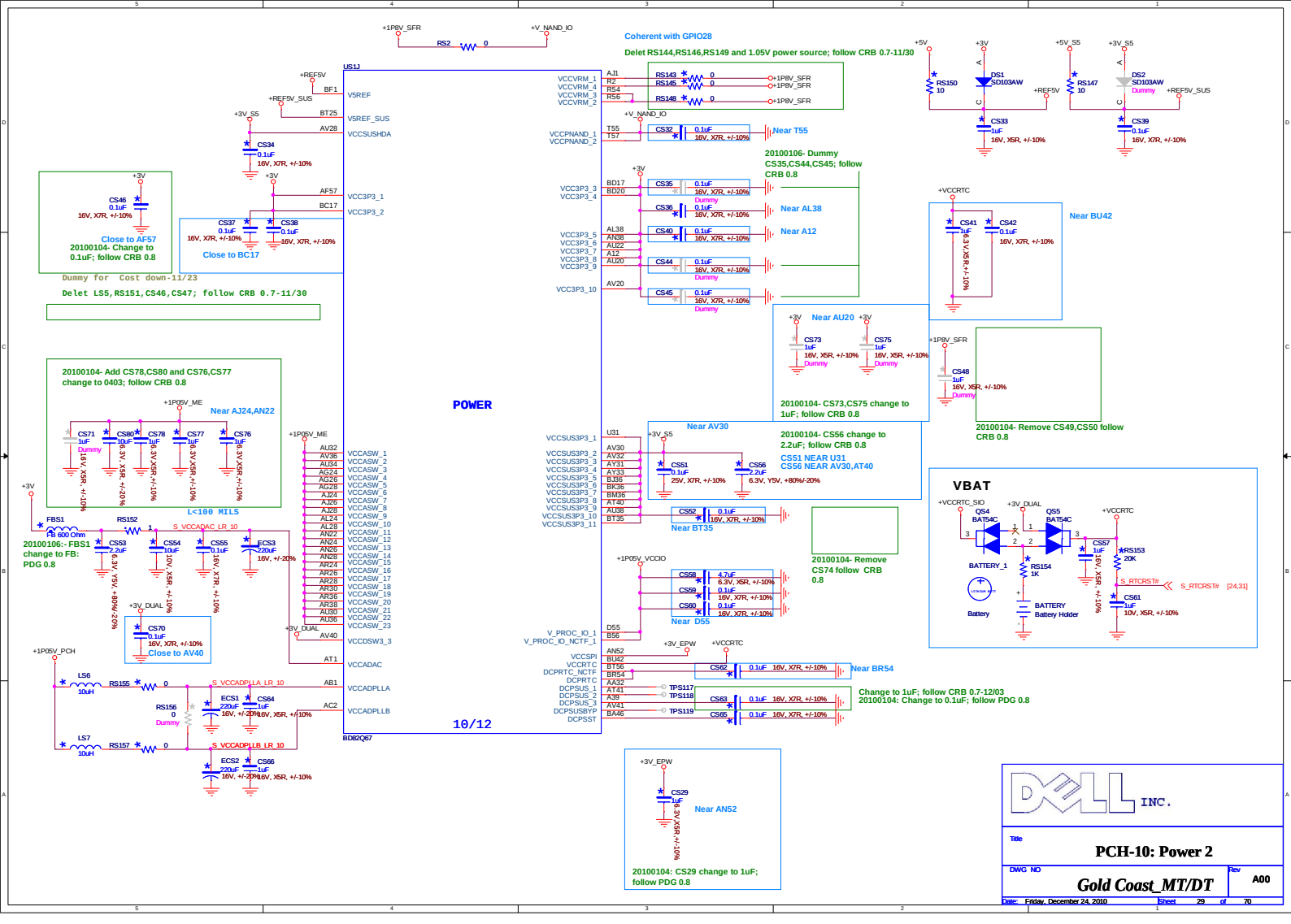
POWER
US1J
BD82Q67
10/12
Coherent with GPIO28
Delet RS144,RS146,RS149 and 1.05V power source; follow CRB 0.7-11/30
Dummy for Cost down-11/23
Delet LS5,RS151,CS46,CS47; follow CRB 0.7-11/30
20100104- Add CS78,CS80 and CS76,CS77 change to 0403; follow CRB 0.8
Near AJ24,AN22
L<100 MILS
20100106:- FBS1 change to FB: PDG 0.8
Close to AF57
20100104- Change to 0.1uF; follow CRB 0.8
Close to BC17
Near AV30
20100104- CS56 change to 2.2uF; follow CRB 0.8
CS51 NEAR U31
CS56 NEAR AV30,AT40
Near BT35
20100104- Remove CS74 follow CRB 0.8
Near D55
Near BR54
Change to 1uF; follow CRB 0.7-12/03
20100104: Change to 0.1uF; follow PDG 0.8
Near AN52
20100104: CS29 change to 1uF; follow PDG 0.8
Near AL38
Near A12
Near AU20
20100104- CS73,CS75 change to 1uF; follow CRB 0.8
Near BU42
20100104- Remove CS49,CS50 follow CRB 0.8
20100106- Dummy CS35,CS44,CS45; follow CRB 0.8
Near T55
Close to AV40
VBAT
BATTERY_1
Battery
BATTERY
Battery Holder
DELL INC.
Title
PCH-10: Power 2
DWG NO
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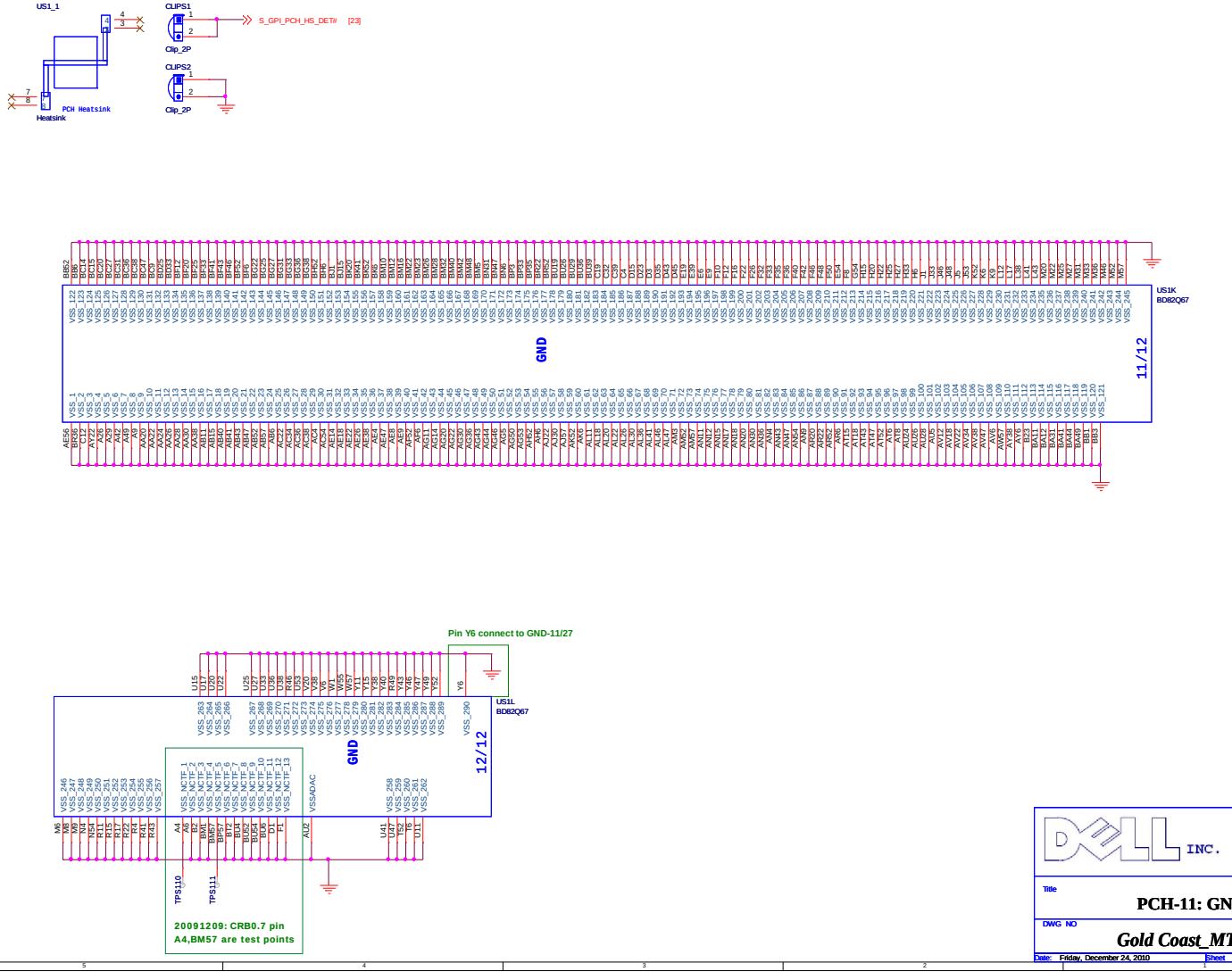

DELL INC.

Title

PCH-11: GND

DWG NO

Gold Coast_MT/DT

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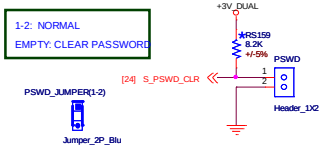
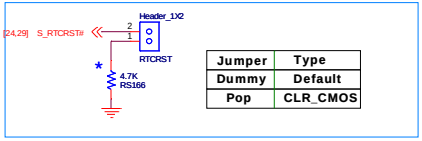
Clear Password

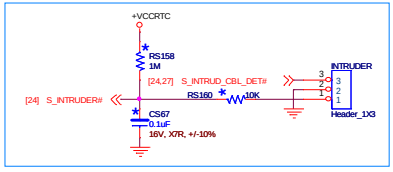


CLR_CMOS

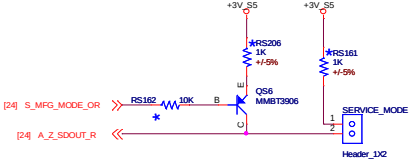


Jumper	Type
Dummy	Default
Pop	CLR_CMOS

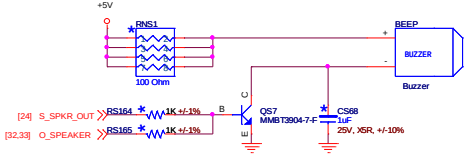
Chassis Intruder



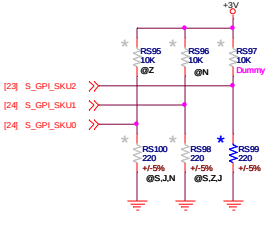
SERVICE_MODE



BEEP



SKU ID



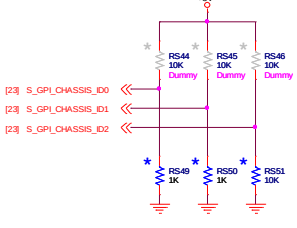
SKU ID

SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	non TPM/TCM
1	1	Reserved

Chassis ID

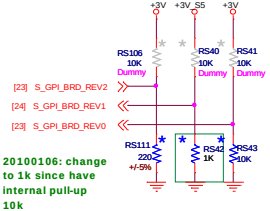
check : need to update table

ID2	ID1	ID0	Type
1	0	1	SFF
1	0	0	Tambor
0	0	0	MT/DT
0	1	1	USFF



BOARD ID

Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



20100106: change to 1k since have internal pull-up 10k

DELL INC.

Title: PCH MISC Conn/BUZ/ID

DWG NO: Gold Coast_MT/DT

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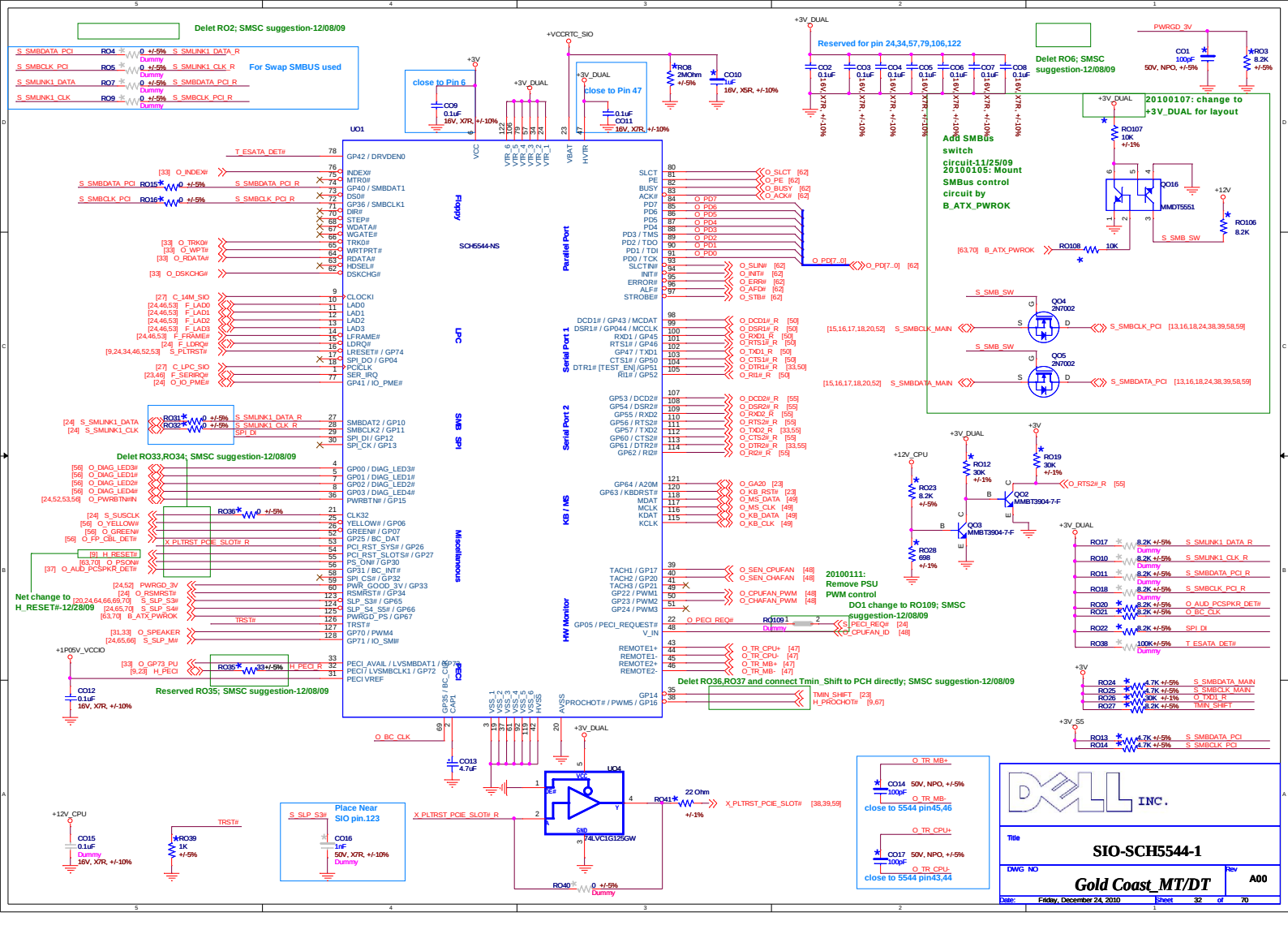
Delet RO2; SMSC suggestion-12/08/09
S_SMBDATA_PCI RO4 0 +/-5% S_SMLINK1_DATA_R
S_SMBCLK_PCI RO5 0 +/-5% S_SMLINK1_CLK_R
S_SMLINK1_DATA RO7 0 +/-5% S_SMBDATA_PCI_R
S_SMLINK1_CLK RO9 0 +/-5% S_SMBCLK_PCI_R
Dummy
For Swap SMBUS used
close to Pin 6
close to Pin 47
+3V_DUAL
+VCCRTC_SIO
Reserved for pin 24,34,57,79,106,122
Delet RO6; SMSC suggestion-12/08/09
PWRGD_3V
20100107: change to +3V_DUAL for layout
Add SMBus switch circuit-11/25/09
20100105: Mount SMBus control circuit by B_ATX_PWROK
UO1
SCH5544-NS
Floppy
Parallel Port
Serial Port 1
Serial Port 2
LPC
SMB SPI
KB / MS
Miscellaneous
HW Monitor
PCI
T_ESATA_DET#
S_SMBDATA_PCI
S_SMBCLK_PCI
RO15
RO16
O_PD[7..0]
S_SMBCLK_MAIN
S_SMBDATA_MAIN
Delet RO33,RO34; SMSC suggestion-12/08/09
Net change to H_RESET#-12/28/09
Reserved RO35; SMSC suggestion-12/08/09
Delet RO36,RO37 and connect Tmin_Shift to PCH directly; SMSC suggestion-12/08/09
20100111: Remove PSU PWM control
DO1 change to RO109; SMSC suggestion-12/08/09
Place Near SIO pin.123
DELL INC.
Title
SIO-SCH5544-1
DWG NO
Gold Coast_MT/DT
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A00
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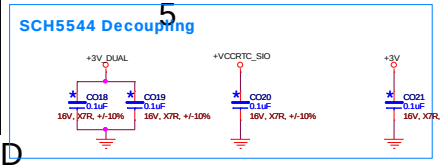
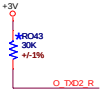
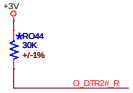
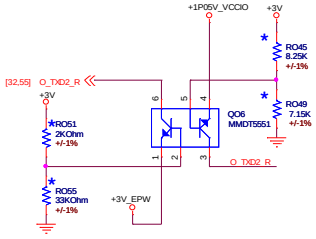
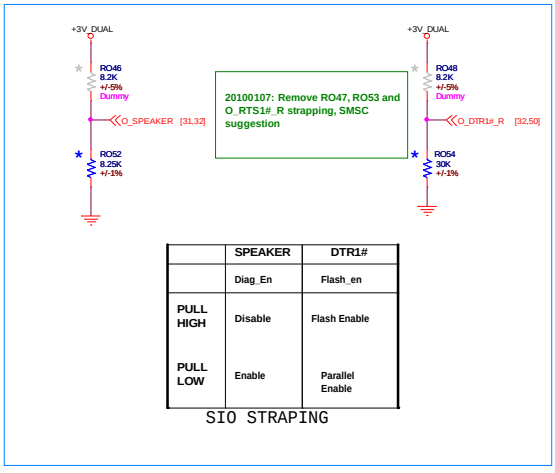




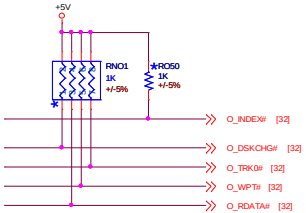


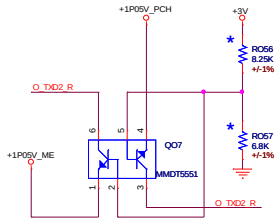


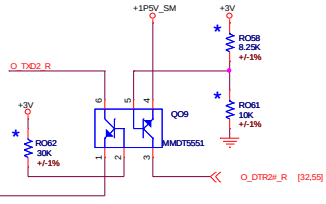


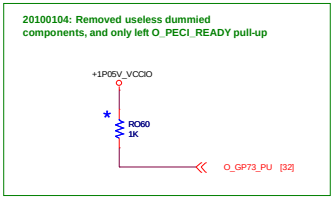
	SPEAKER	DTR1#
	Diag_En	Flash_en
PULL HIGH	Disable	Flash Enable
PULL LOW	Enable	Parallel Enable

SIO STRAPING









5544 PRE-POST DIAG PG GENERATION

DELL INC.

Title: SIO-SCH5544-2 (MISC)

DWG NO: Gold Coast_MT/DT

Rev: A00

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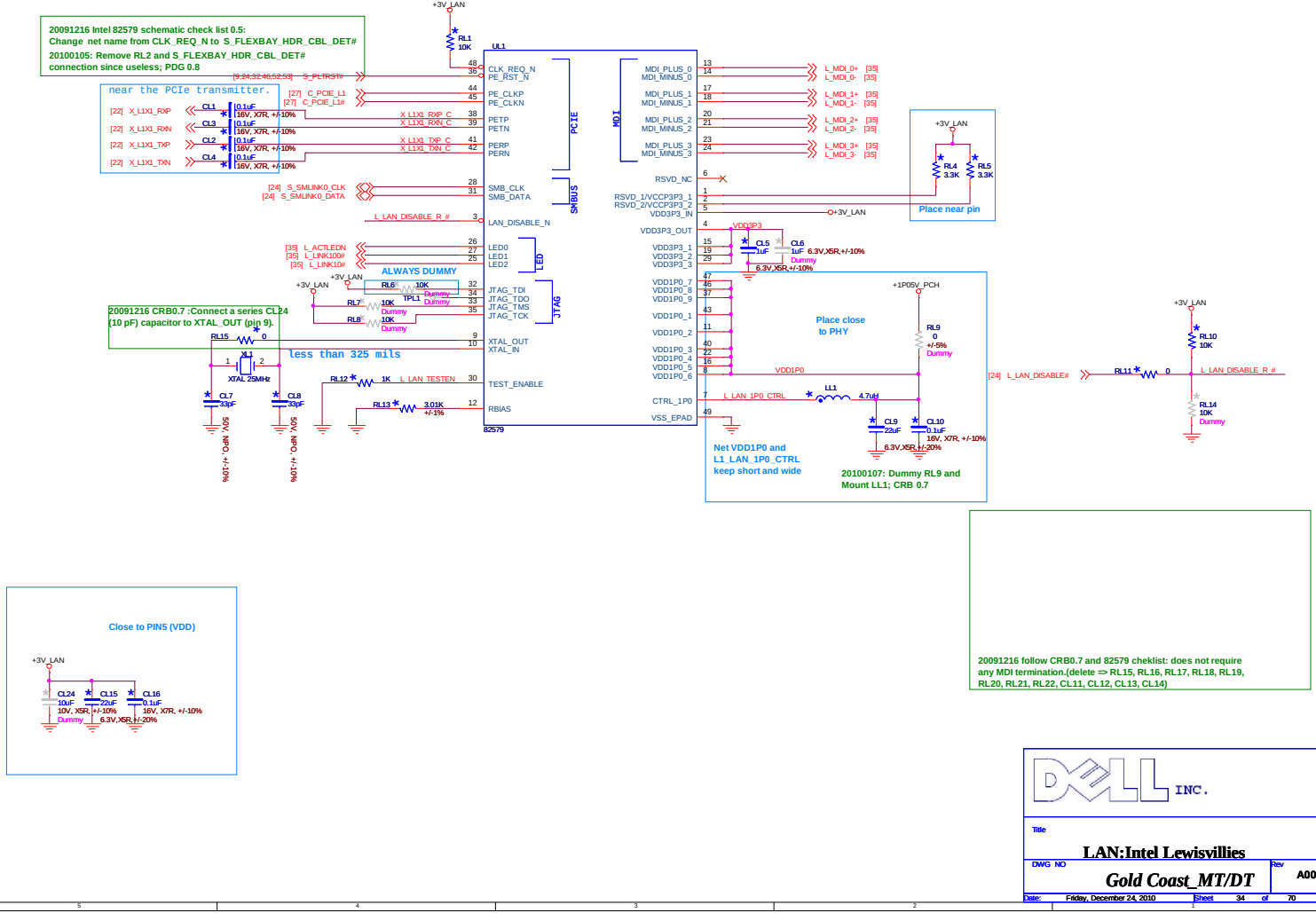
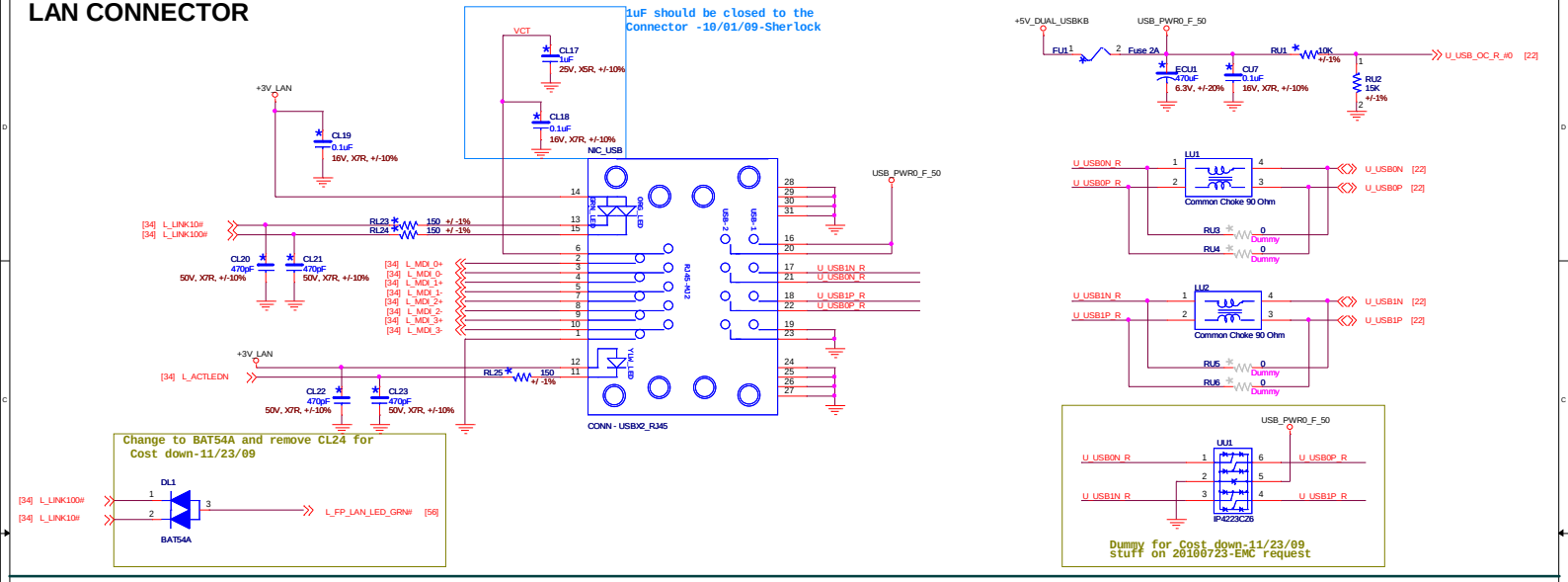
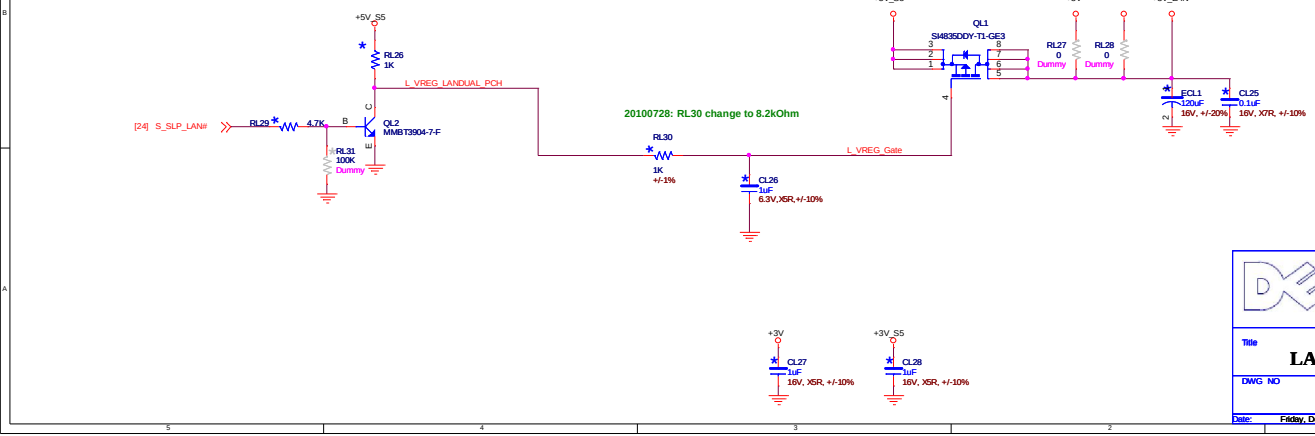

20091216 Intel 82579 schematic check list 0.5:
Change net name from CLK_REQ_N to S_FLEXBAY_HDR_CBL_DET#
20100105: Remove RL2 and S_FLEXBAY_HDR_CBL_DET# connection since useless; PDG 0.8
near the PCIe transmitter.
20091216 CRB0.7 :Connect a series CL24 (10 pF) capacitor to XTAL_OUT (pin 9).
less than 325 mils
ALWAYS DUMMY
Close to PIN5 (VDD)
Place near pin
Place close to PHY
Net VDD1P0 and L1_LAN_1P0_CTRL keep short and wide
20100107: Dummy RL9 and Mount LL1; CRB 0.7
20091216 follow CRB0.7 and 82579 cheklist: does not require any MDI termination.(delete => RL15, RL16, RL17, RL18, RL19, RL20, RL21, RL22, CL11, CL12, CL13, CL14)
U1
82579
+3V_LAN
+1P05V_PCH
VDD1P0
L_LAN_1P0_CTRL
L_LAN_DISABLE#
L_LAN_DISABLE_R_#
S_PLTRST#
C_PCIE_L1
C_PCIE_L1#
S_SMLINK0_CLK
S_SMLINK0_DATA
L_LAN_TESTEN
L_ACTLEDN
L_LINK100#
L_LINK10#
X_L1X1_RXP_C
X_L1X1_RXN_C
X_L1X1_TXP_C
X_L1X1_TXN_C
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETP
PETN
PERP
PERN
SMB_CLK
SMB_DATA
LAN_DISABLE_N
LED0
LED1
LED2
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
XTAL_OUT
XTAL_IN
TEST_ENABLE
RBIAS
MDI_PLUS_0
MDI_MINUS_0
MDI_PLUS_1
MDI_MINUS_1
MDI_PLUS_2
MDI_MINUS_2
MDI_PLUS_3
MDI_MINUS_3
L_MDI_0+
L_MDI_0-
L_MDI_1+
L_MDI_1-
L_MDI_2+
L_MDI_2-
L_MDI_3+
L_MDI_3-
RSVD_NC
RSVD_1/VCCP3P3_1
RSVD_2/VCCP3P3_2
VDD3P3_IN
VDD3P3_OUT
VDD3P3_1
VDD3P3_2
VDD3P3_3
VDD1P0_7
VDD1P0_8
VDD1P0_9
VDD1P0_1
VDD1P0_2
VDD1P0_3
VDD1P0_4
VDD1P0_5
VDD1P0_6
CTRL_1P0
VSS_EPAD
PCI-E
MDI
SMBUS
LED
JTAG
XTAL 25MHz
RL1 10K
RL2 10K
RL4 3.3K
RL5 3.3K
RL6 10K
RL7 10K
RL8 10K
RL9 0 +/-5% Dummy
RL10 10K
RL11 0
RL12 1K
RL13 3.01K +/-1%
RL14 10K Dummy
RL15 0
RL16 0
RL17 0
RL18 0
RL19 0
RL20 0
RL21 0
RL22 0
CL1 0.1uF 16V, X7R, +/-10%
CL2 0.1uF 16V, X7R, +/-10%
CL3 0.1uF 16V, X7R, +/-10%
CL4 0.1uF 16V, X7R, +/-10%
CL5 1uF
CL6 1uF 6.3V,X5R,+/-10%
CL7 33pF 50V, NPO, +/-10%
CL8 33pF 50V, NPO, +/-10%
CL9 22uF 6.3V,X5R,+/-20%
CL10 0.1uF 16V, X7R, +/-10%
CL24 10uF 10V, X5R, +/-10% Dummy
CL15 22uF 6.3V,X5R,+/-20%
CL16 0.1uF 16V, X7R, +/-10%
LL1 4.7uH
TPL1 Dummy
Dummy
DELL INC.
Title
LAN:Intel Lewisvillies
DWG NO
Gold Coast_MT/DT
Rev
A00
Date: Friday, December 24, 2010
Sheet 34 of 70

LAN CONNECTOR

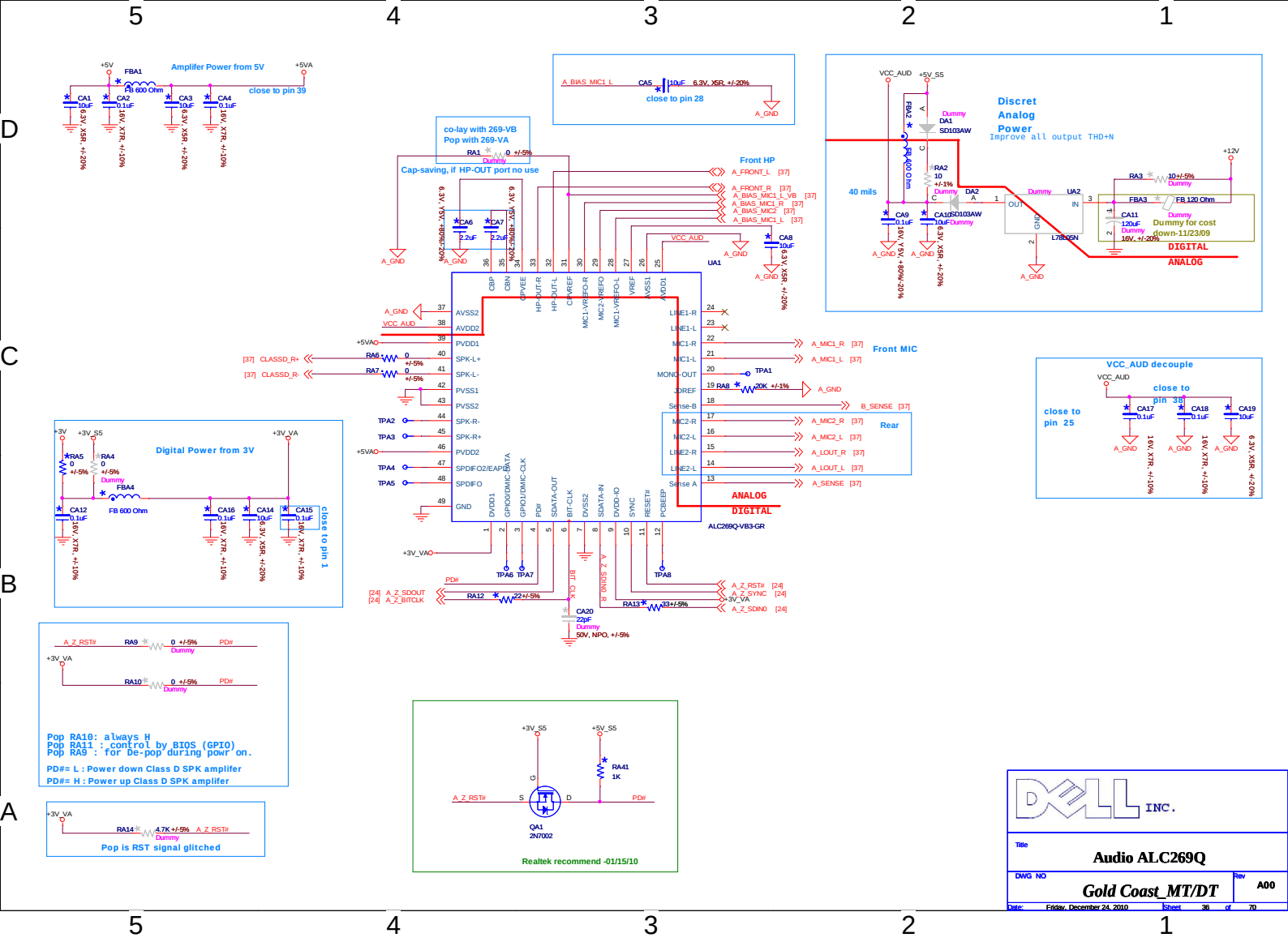


LAN POWER



DELL INC.

Title	LAN Power & LAN/USB Conn
DWG NO	Gold Coast_MT/DT
Rev	A00
Date: Friday, December 24, 2010	Sheet 35 of 70


5
4
3
2
1
D
C
B
A
Amplifer Power from 5V
close to pin 39
FB 600 Ohm
co-lay with 269-VB
Pop with 269-VA
Cap-saving, if HP-OUT port no use
close to pin 28
Front HP
Discret Analog Power
Improve all output THD+N
40 mils
DIGITAL
ANALOG
Front MIC
Rear
ANALOG
DIGITAL
ALC269Q-VB3-GR
VCC_AUD decouple
close to pin 25
close to pin 38
Digital Power from 3V
close to pin 1
Pop RA10: always H
Pop RA11 : control by BIOS (GPIO)
Pop RA9 : for De-pop during powr on.
PD#= L : Power down Class D SPK amplifer
PD#= H : Power up Class D SPK amplifer
Pop is RST signal glitched
Realtek recommend -01/15/10
DELL INC.
Title
Audio ALC269Q
DWG NO
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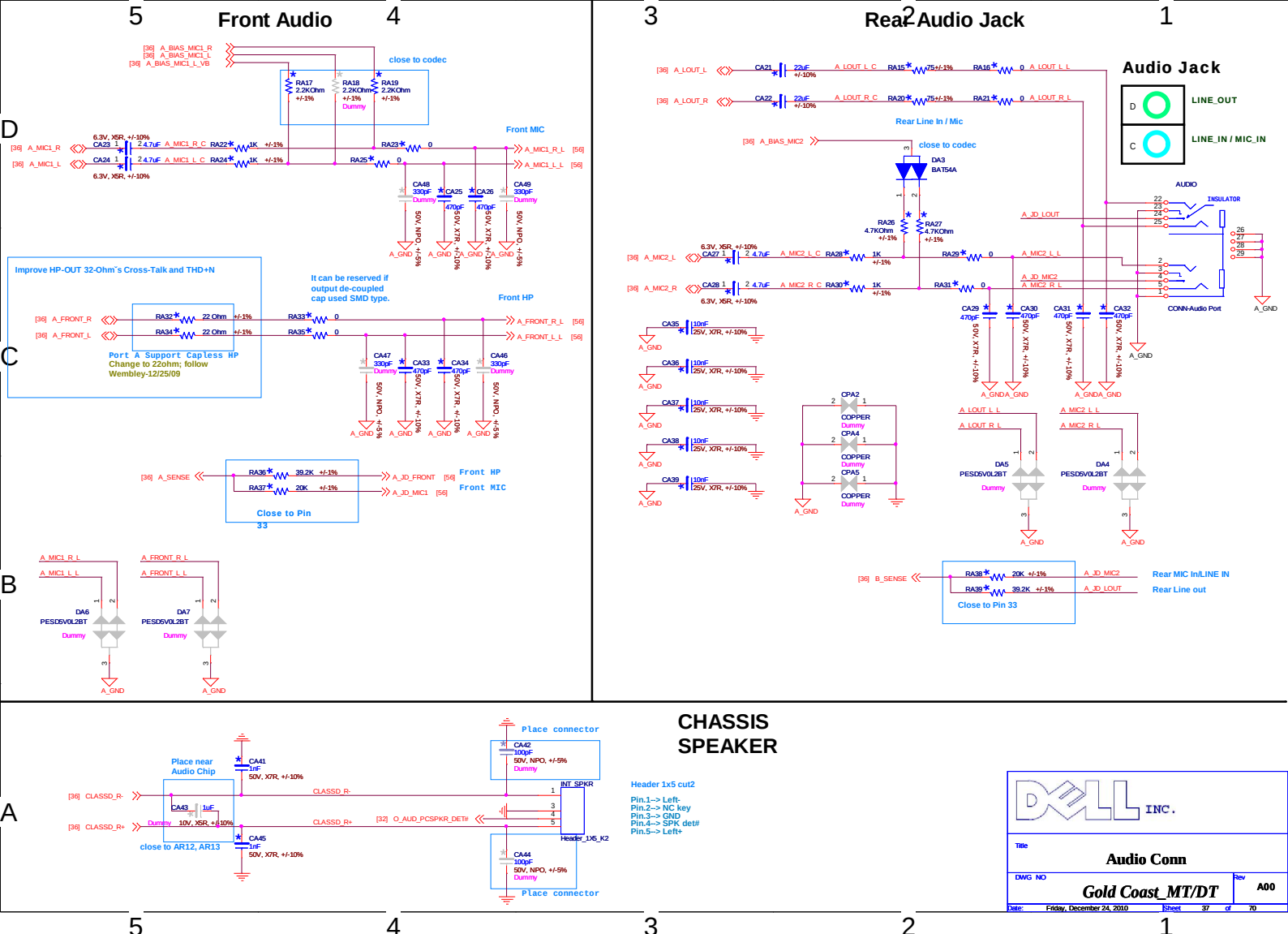
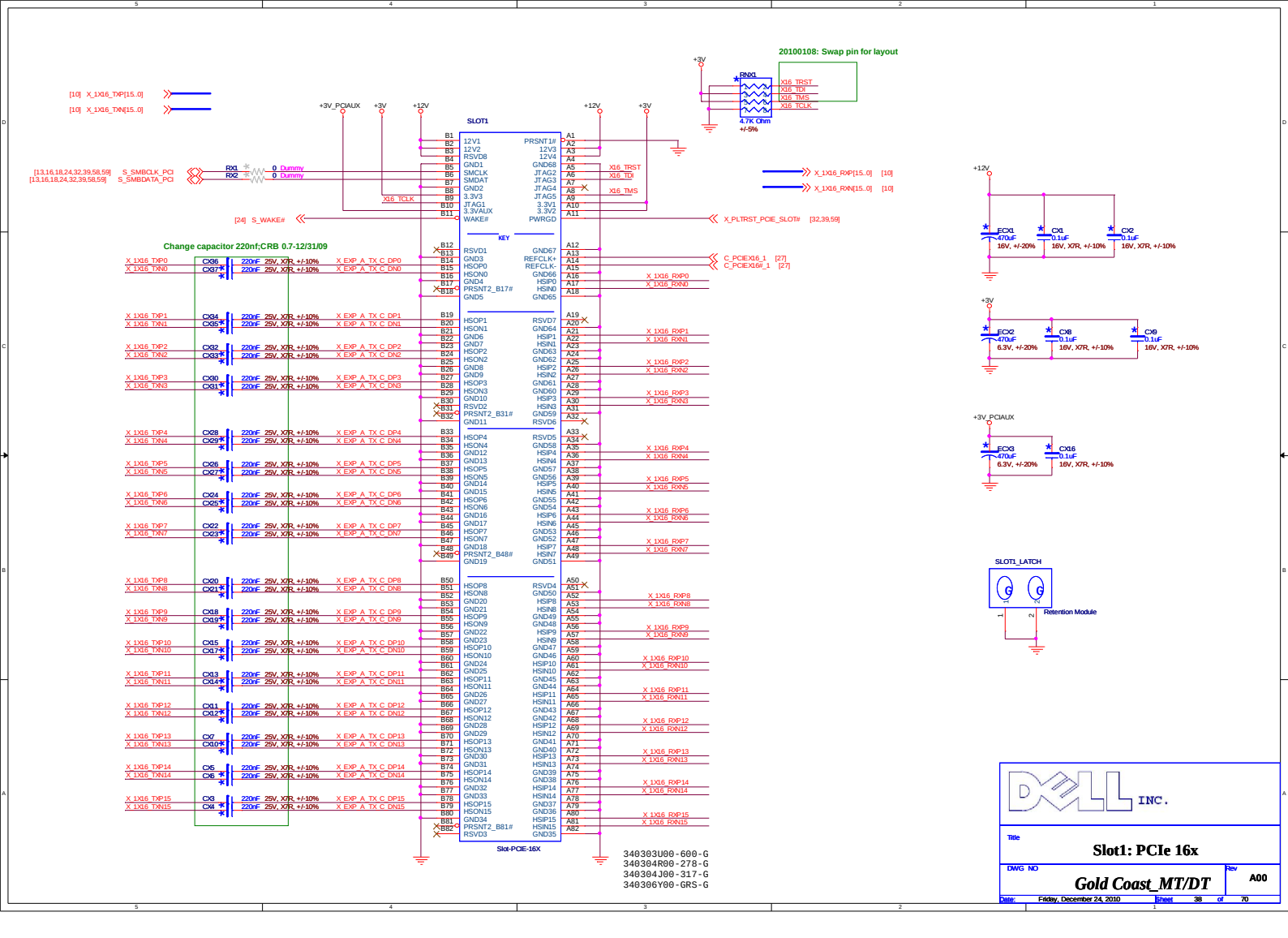
Sheet 36 of 70


Front Audio
Rear Audio Jack
CHASSIS SPEAKER
close to codec
Front MIC
Improve HP-OUT 32-Ohm~s Cross-Talk and THD+N
It can be reserved if output de-coupled cap used SMD type.
Front HP
Port A Support Capless HP
Change to 22ohm; follow Wembley-12/25/09
Close to Pin 33
Front HP
Front MIC
Audio Jack
LINE_OUT
LINE_IN / MIC_IN
Rear Line In / Mic
close to codec
AUDIO
INSULATOR
CONN-Audio Port
Rear MIC In/LINE IN
Rear Line out
Close to Pin 33
Place near Audio Chip
close to AR12, AR13
Place connector
INT_SPKR
Header_1X5_K2
Header 1x5 cut2
Pin.1--> Left-
Pin.2--> NC key
Pin.3--> GND
Pin.4--> SPK det#
Pin.5--> Left+
DELL INC.
Title
Audio Conn
DWG NO
Gold Coast_MT/DT
Rev
A00
Date: Friday, December 24, 2010
Sheet 37 of 70


20100108: Swap pin for layout
SLOT1
Change capacitor 220nf;CRB 0.7-12/31/09
Slot-PCIE-16X
KEY
RNX1
4.7K Ohm
+/-5%
X16_TRST
X16_TDI
X16_TMS
X16_TCLK
[10] X_1X16_TXP[15..0]
[10] X_1X16_TXN[15..0]
[13,16,18,24,32,39,58,59] S_SMBCLK_PCI
[13,16,18,24,32,39,58,59] S_SMBDATA_PCI
[24] S_WAKE#
[32,39,59] X_PLTRST_PCIE_SLOT#
[10] X_1X16_RXP[15..0]
[10] X_1X16_RXN[15..0]
C_PCIEX16_1 [27]
C_PCIEX16#_1 [27]
+3V_PCIAUX
+3V
+12V
FCX1 470uF 16V, +/-20%
CX1 0.1uF 16V, X7R, +/-10%
CX2 0.1uF 16V, X7R, +/-10%
FCX2 470uF 6.3V, +/-20%
CX8 0.1uF 16V, X7R, +/-10%
CX9 0.1uF 16V, X7R, +/-10%
FCX3 470uF 6.3V, +/-20%
CX16 0.1uF 16V, X7R, +/-10%
SLOT1_LATCH
Retention Module
340303U00-600-G
340304R00-278-G
340304J00-317-G
340306Y00-GRS-G
DELL INC.
Title
Slot1: PCIe 16x
DWG NO
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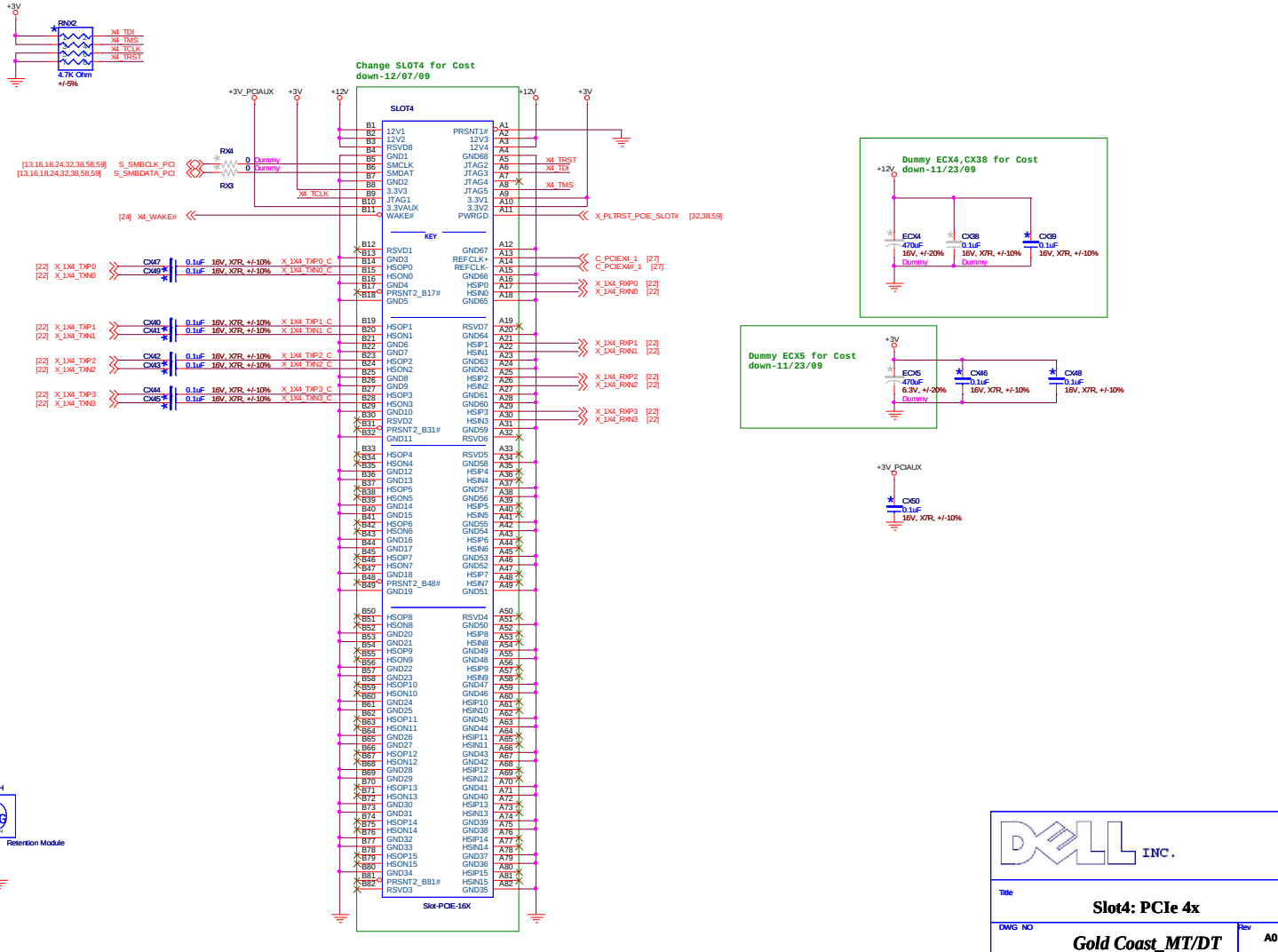

Title	Slot4: PCIe 4x
DWG NO	Gold Coast_MT/DT
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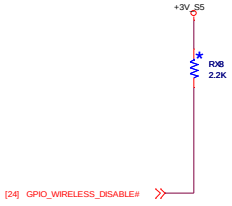
Sheet	39 of 70



DELL INC.

Title

TBD

DWG NO

Gold Coast_MT/DT

Rev

A00

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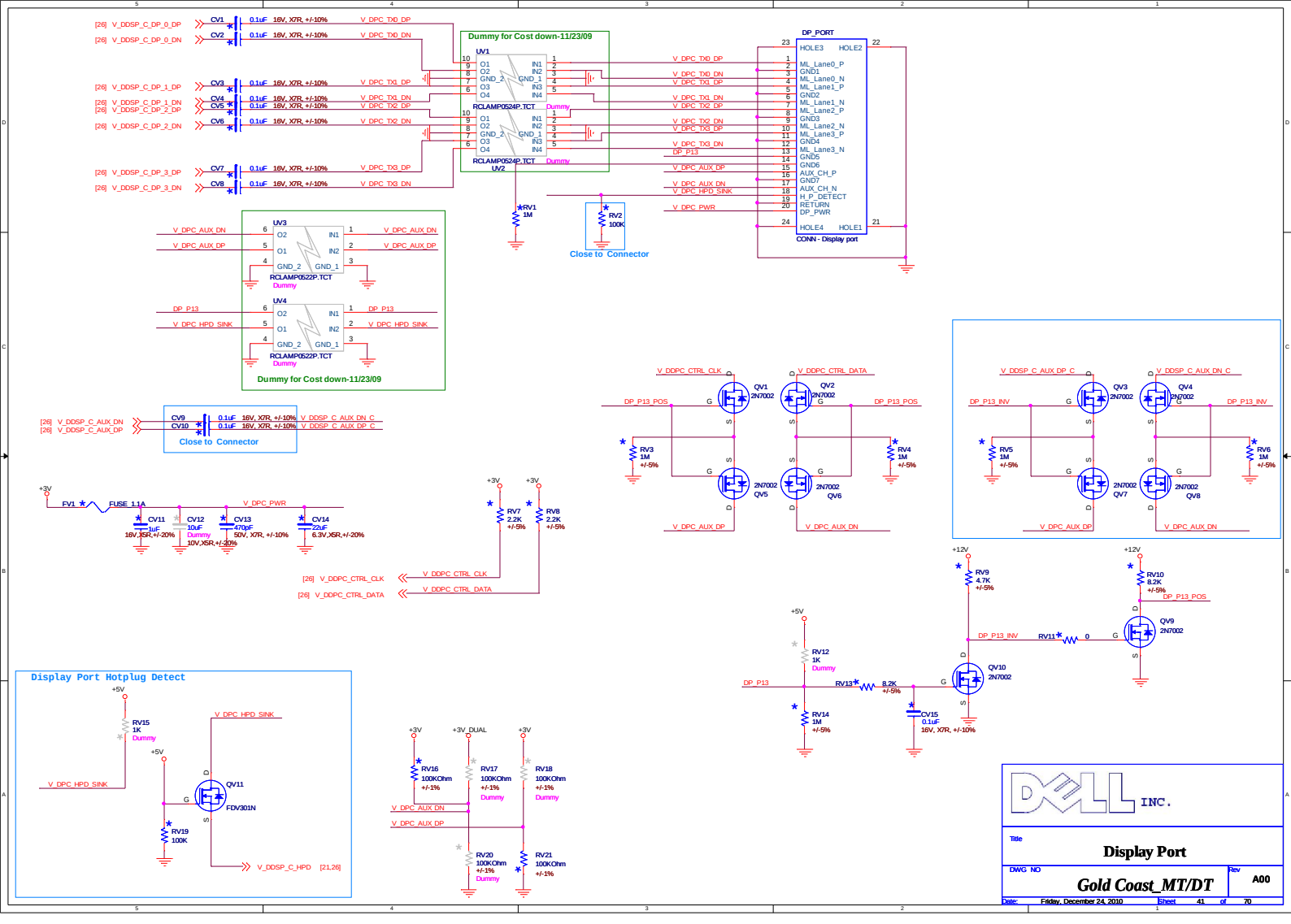
Dummy for Cost down-11/23/09
Close to Connector
DP_PORT
CONN - Display port
Dummy for Cost down-11/23/09
Close to Connector
Display Port Hotplug Detect
DELL INC.
Title
Display Port
DWG NO
Gold Coast_MT/DT
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A00
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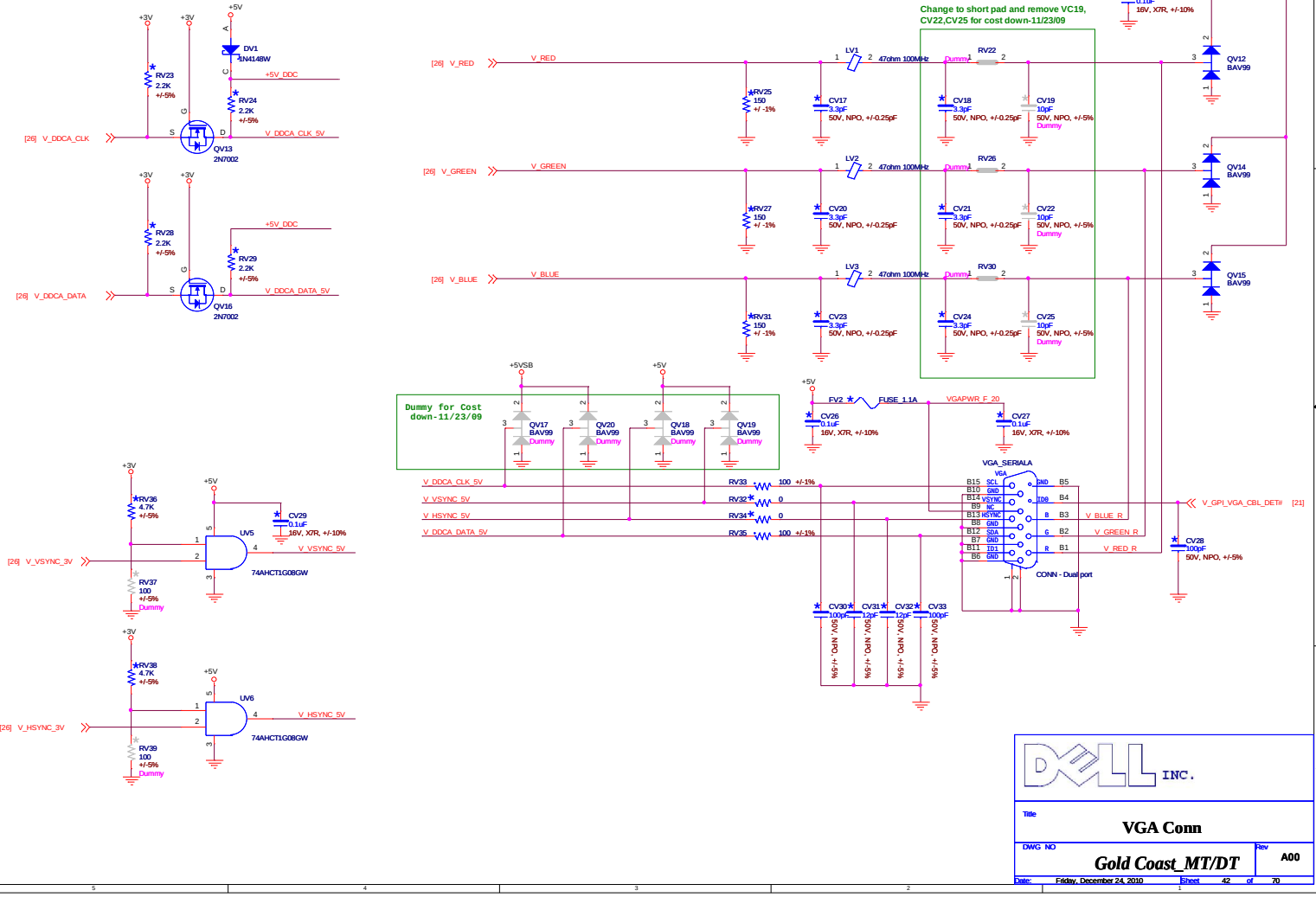
VGA Connector



DELL INC.

Title: **VGA Conn**

DWG NO: ***Gold Coast_MT/DT***

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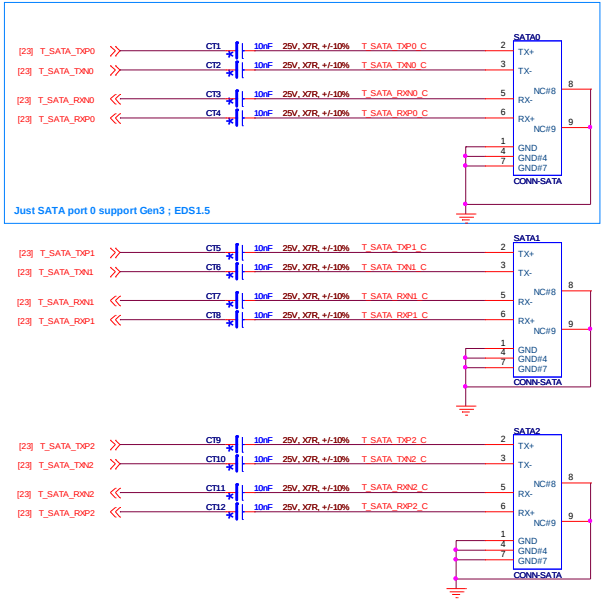
SATA x 3



DELL INC.

Title: **SATA Conn**

DWG NO: ***Gold Coast_MT/DT***

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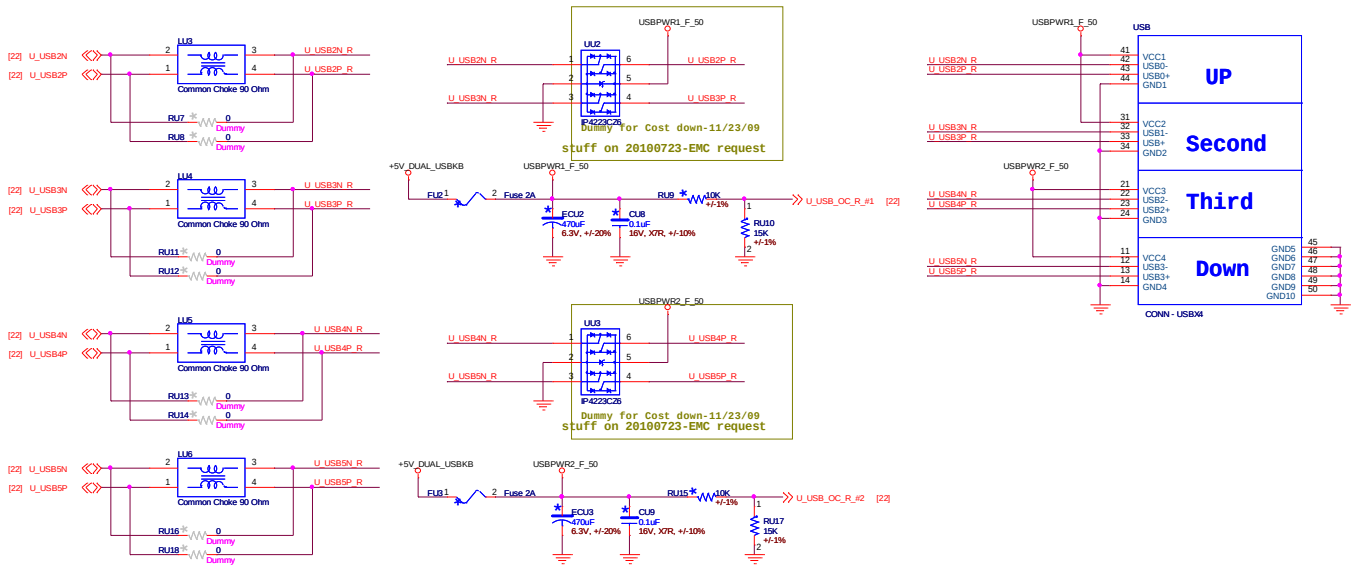
Rear USB CONNECTOR



DELL INC.

Title: Rear USB

DWG NO: Gold Coast_MT/DT

Rev: A00

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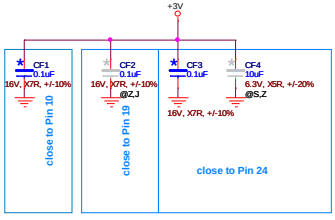
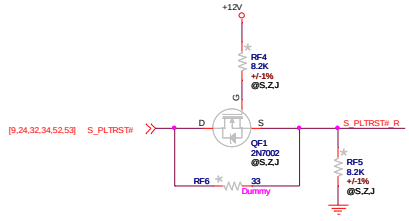
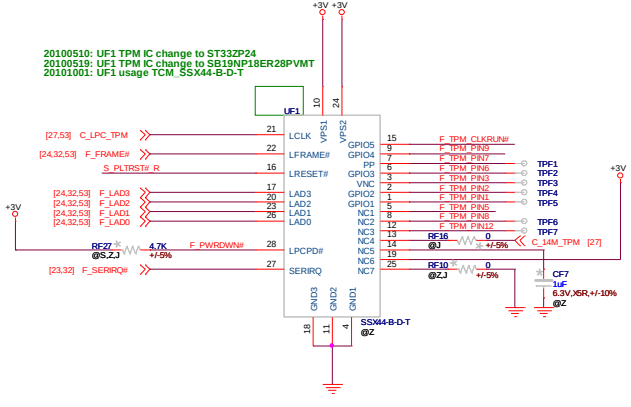
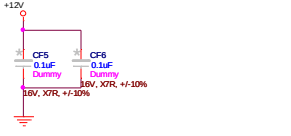
TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

(Default) ST Micro	POP S	CF4
ZTE	POP Z	CF2,CF4,CF7,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21









20101001: add UF2 usage TPM_SB19NP18ER28PVMK

DELL INC.

Title: **TPM & TCM**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

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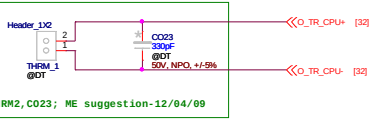
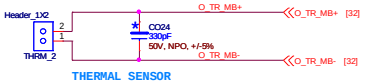
Change net to O_TR_MB+/-; SMSC suggestion-12/08/09
Removed THRM1 since useless-01/01/10



Dummy THRM2,CO23; ME suggestion-12/04/09



THERMAL SENSOR

DELL INC.

Title: Thermal Sensor Conn

DWG NO: Gold Coast_MT/DT

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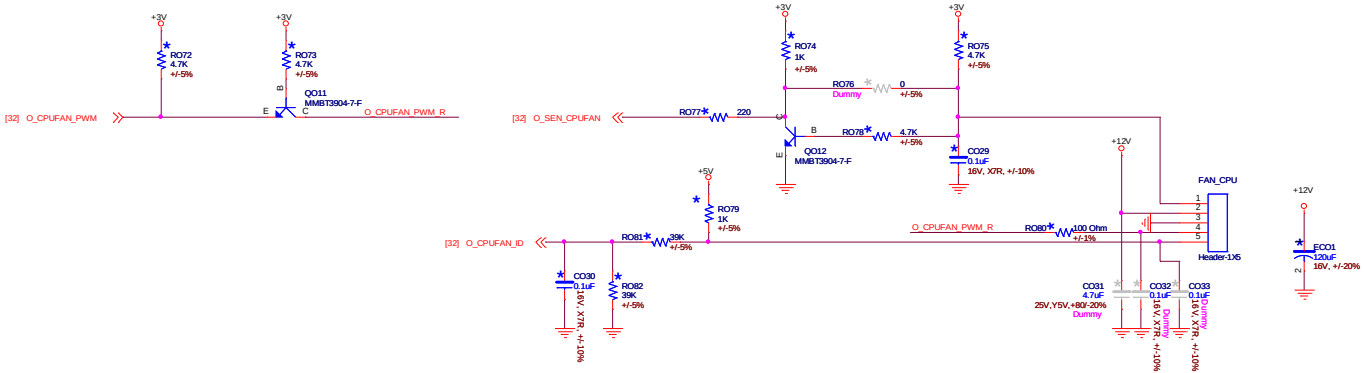
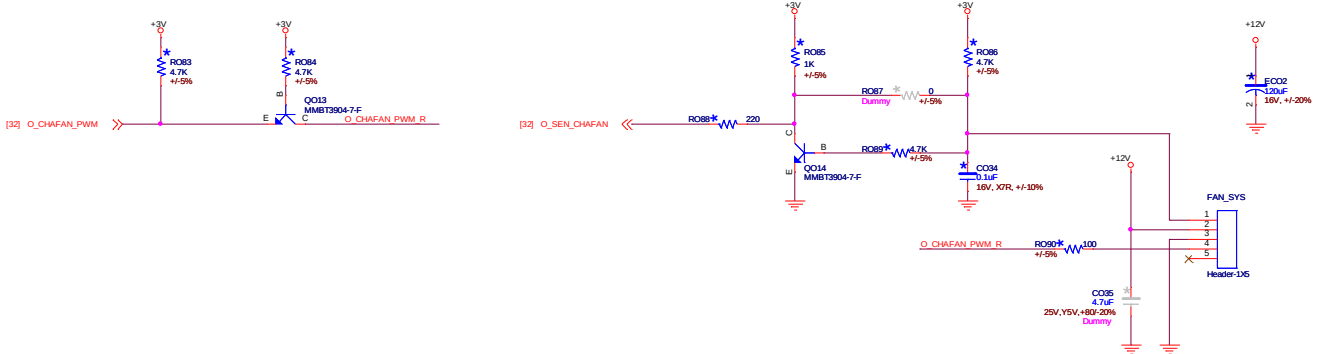
CPU Fan



SYS Fan



PSU Fan

20100111: Remove PSU PWM control

DELL INC.	
Title	FAN
DWG NO	Gold Coast_MT/DT
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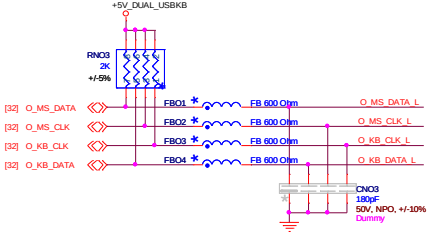
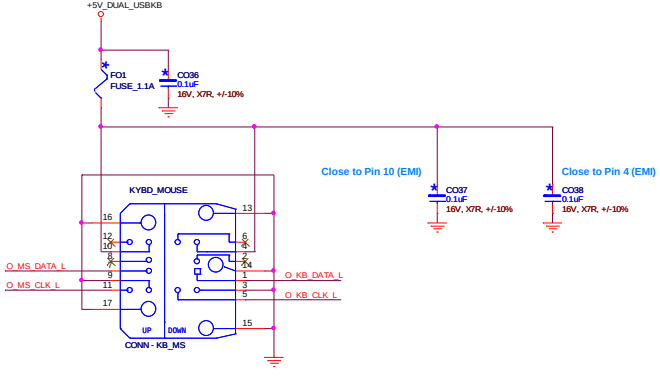
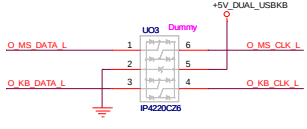
KB/MS







Title	PS2 Conn
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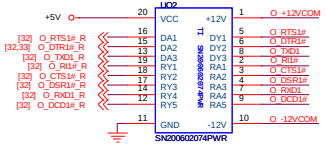
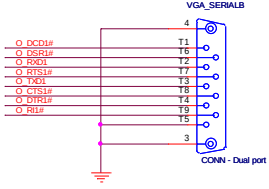
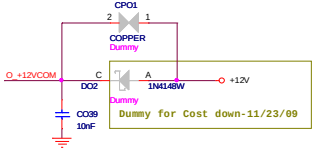
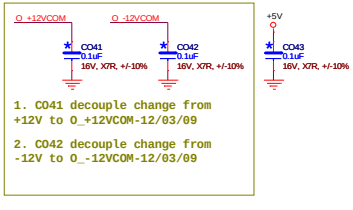
Serial Port 1

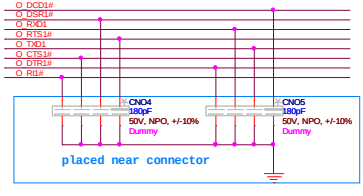


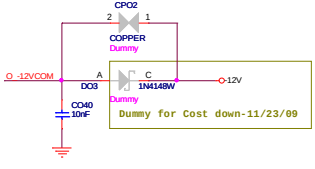




placed near GD75232







DELL INC.

Title: COM1

DWG NO: Gold Coast_MT/DT

Rev: A00

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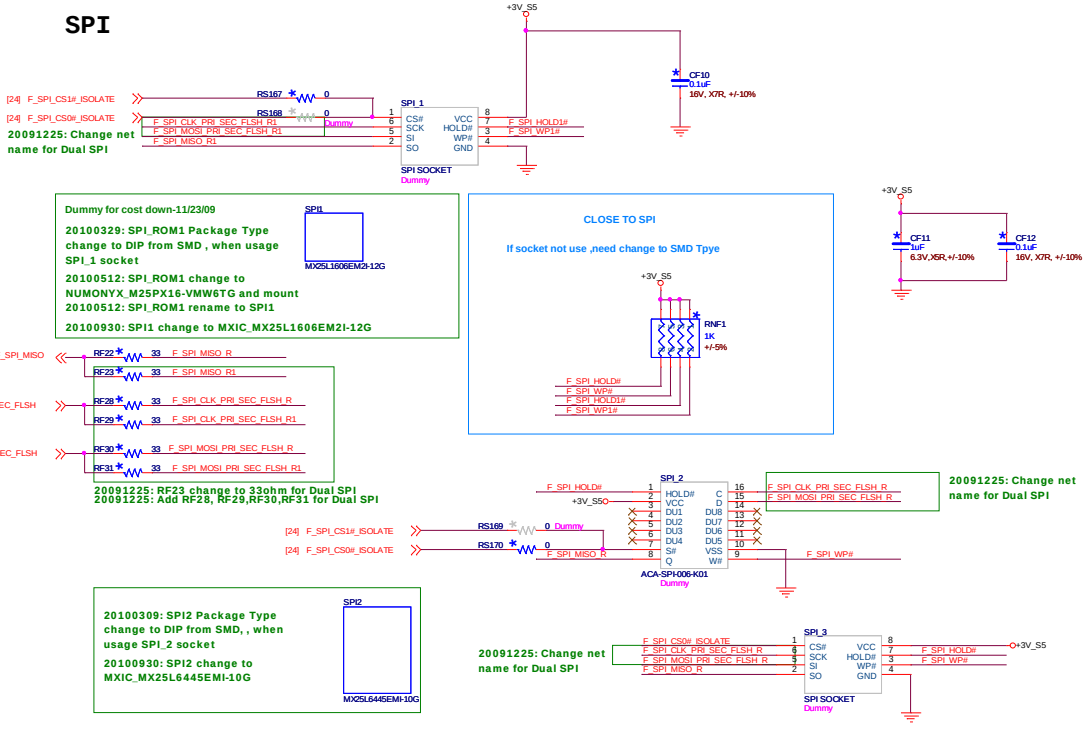
SPI



DELL INC.

Title: SPI

DWG NO: Gold Coast_MT/DT

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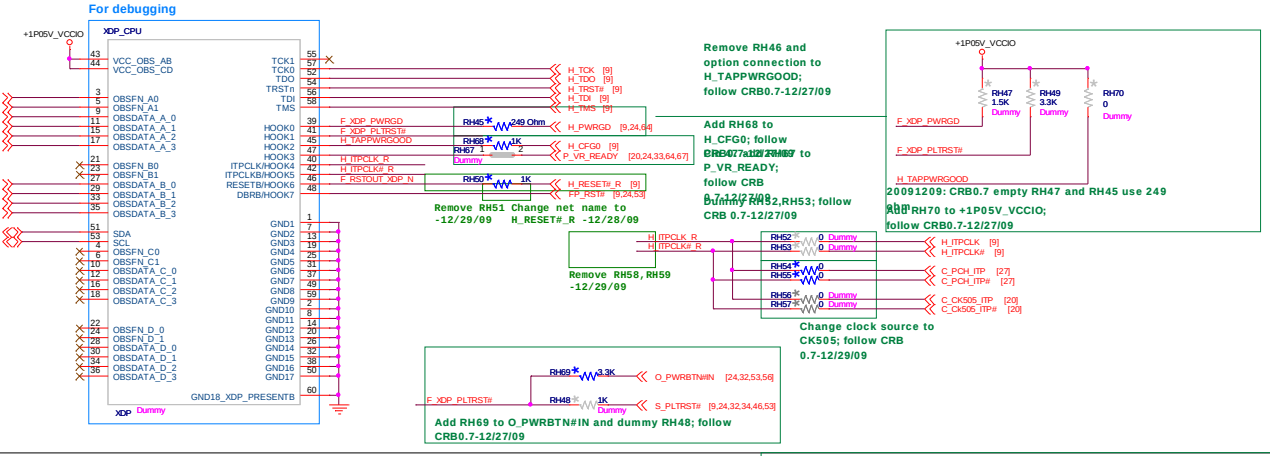
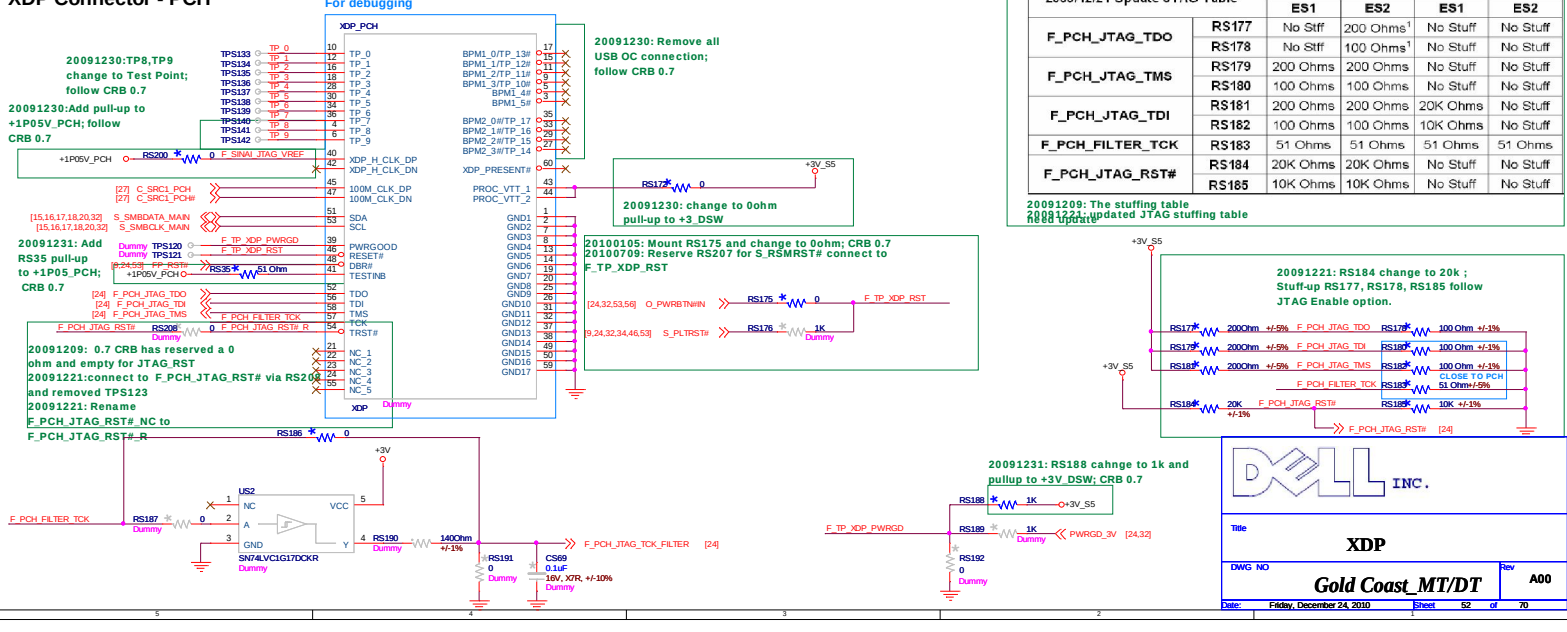
XDP Connector - CPU



XDP Connector - PCH



2009/12/21 Update JTAG Table		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms[1]	No Stuff	No Stuff
	RS178	No Stff	100 Ohms[1]	No Stuff	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms	No Stuff
	RS182	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff	No Stuff

20091209: The stuffing table
20091221: updated JTAG stuffing table need update

Title	XDP
DWG NO	Gold Coast_MT/DT
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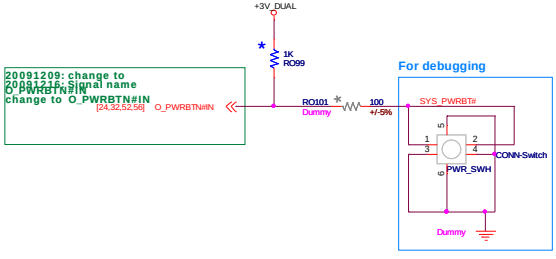
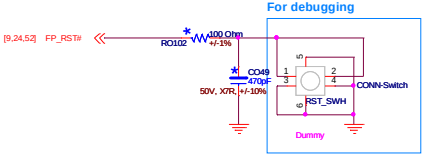
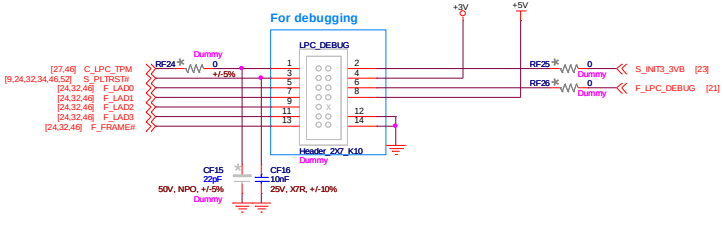
Power Bottom

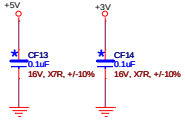


Reset Bottom



LPC DEBUG





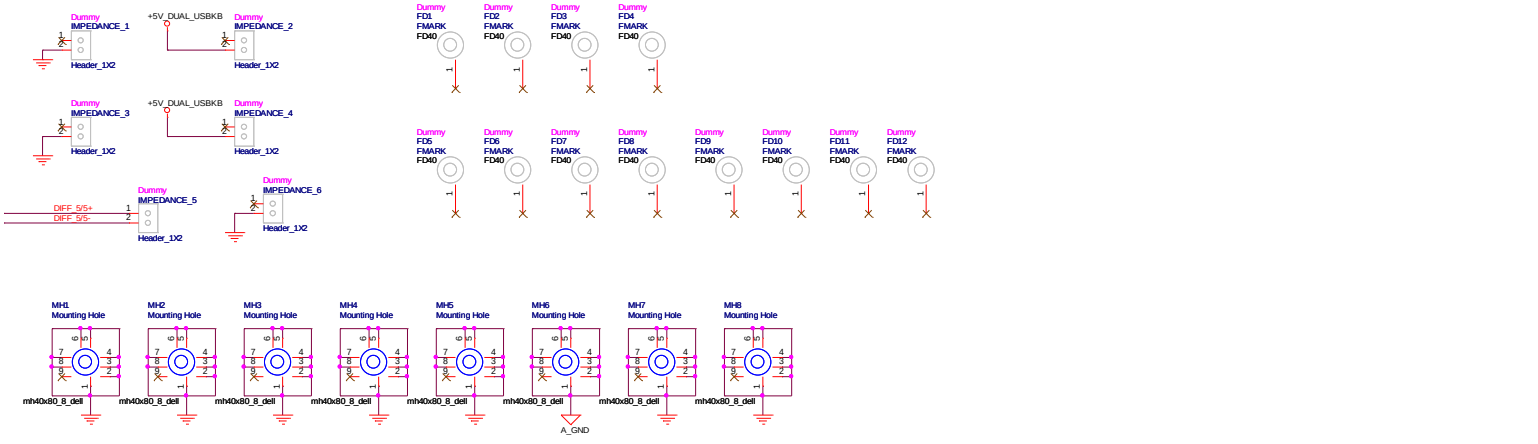
DELL INC.

Title: **Pilot Run Conn**

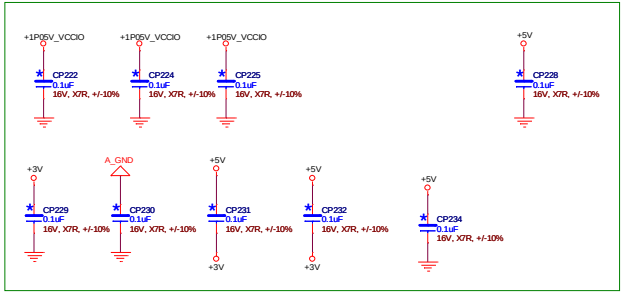
DWG NO: ***Gold Coast_MT/DT***

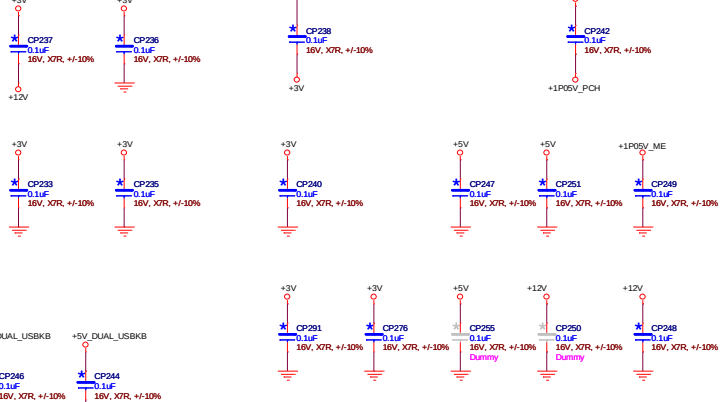
Rev: A00

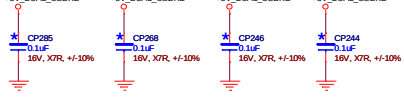
Date: Friday, December 24, 2010 Sheet 53 of 70



20100108: Add for EMI







DELL INC.

Title: **EMI**

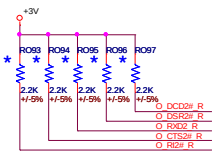
DWG NO: ***Gold Coast_MT/DT***

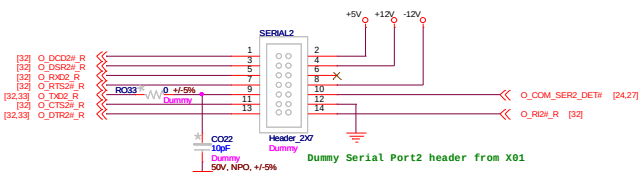
Rev: A00

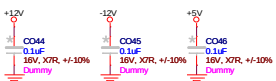
Date: Friday, December 24, 2010 Sheet 54 of 70

Move PWR_SW conn to
page56 20091126

Serial Port 2 Header







DELL INC.

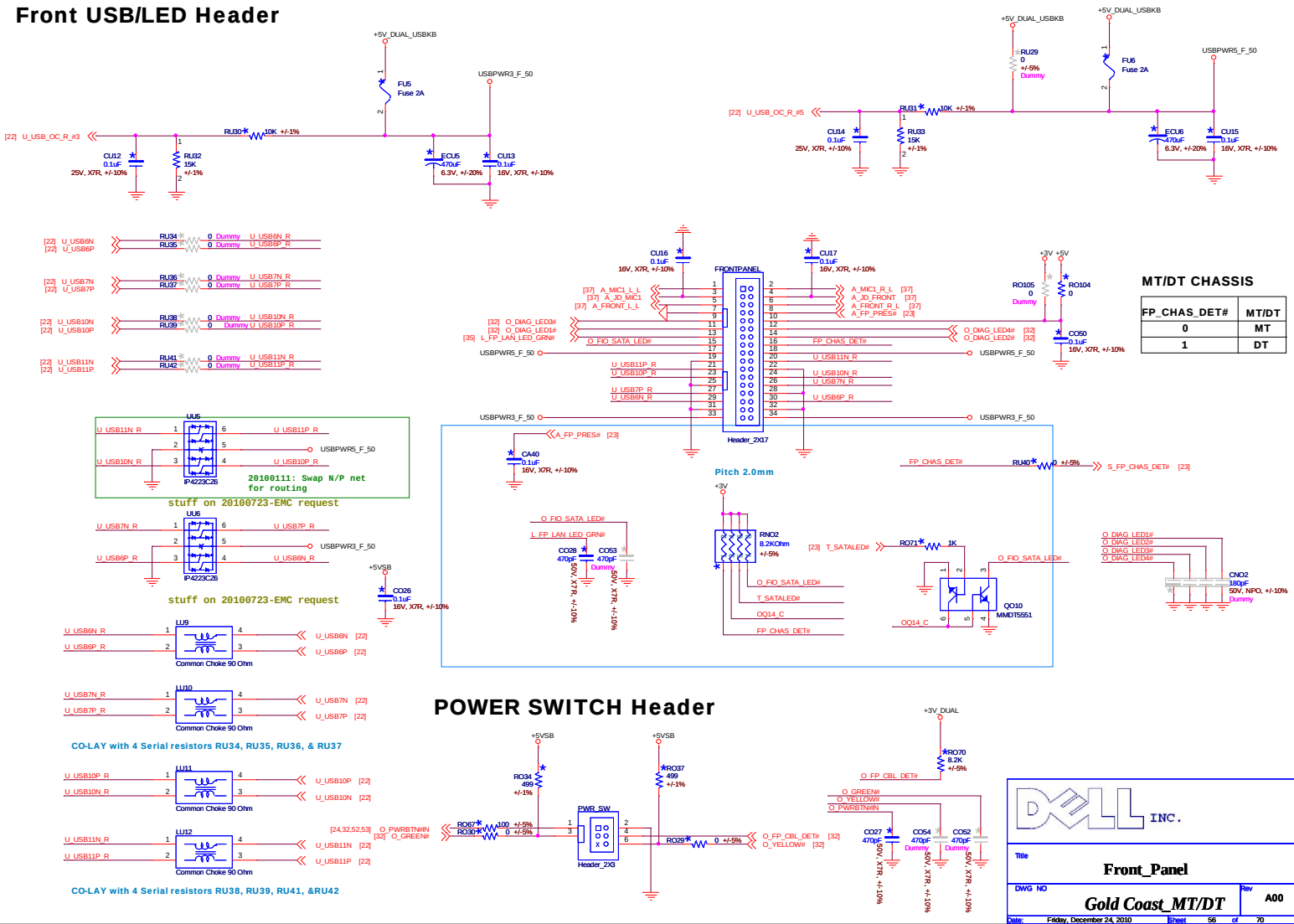
Title
COM2 HDR

DWG NO
Gold Coast_MT/DT

Rev
A00

Date: Friday, December 24, 2010 Sheet 55 of 70

Front USB/LED Header



POWER SWITCH Header

DELL INC.

Title: Front_Panel

DWG NO: Gold Coast_MT/DT

Rev: A00

Date: Friday, December 24, 2010 Sheet 56 of 70

IRQ: CDAB
IDSEL: AD18
REQ/GNT: 0

For pci slot used
Moved from PCH section-12/30/09

SLOT3
Slot-PCI

Dummy for Cost down-11/23/09

DELL INC.

Title: Slot3: PCI

DWG NO: Gold Coast_MT/DT

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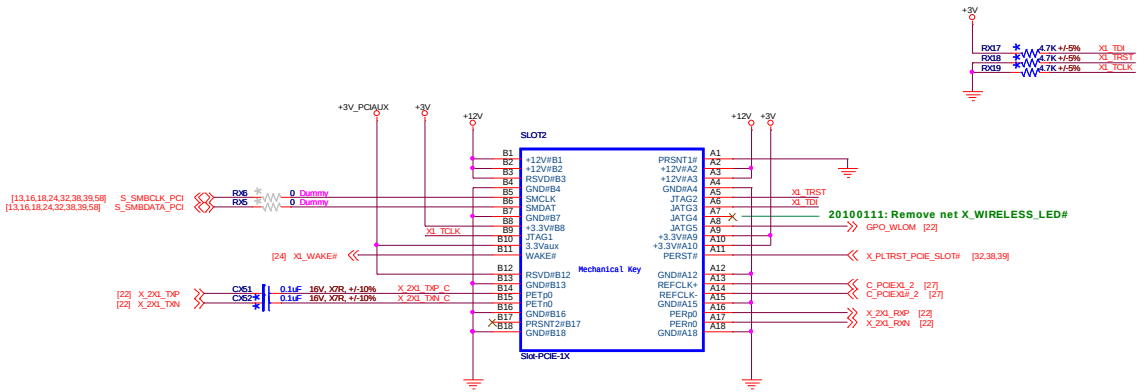
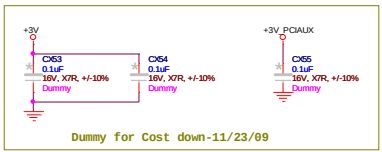




DELL INC.

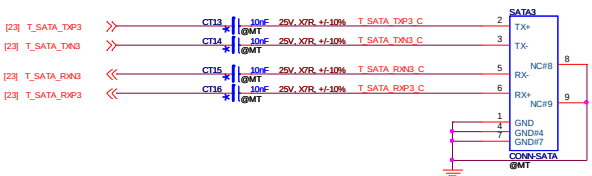
Title: **Slot2: PCIe 1x**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

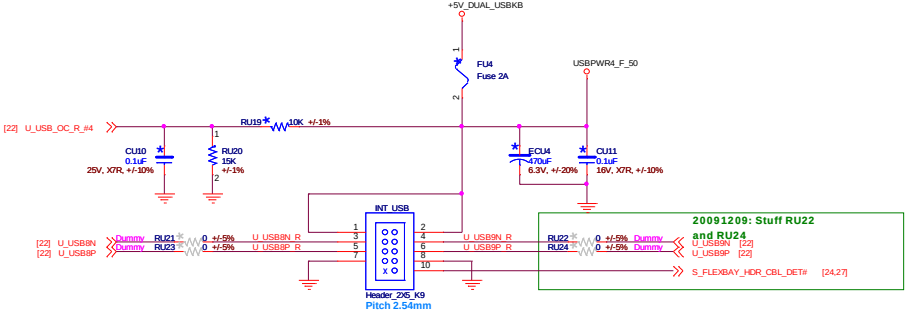
Date: Friday, December 24, 2010 Sheet 59 of 70

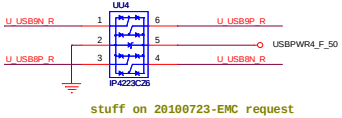
SATA port 3 only for MT



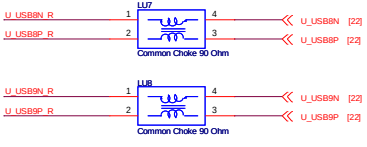
DELL INC.		
Title	SATA_MT	
DWG NO	Gold Coast_MT/DT	Rev A00
Date: Friday, December 24, 2010	Sheet 60 of 70	

FLEXBAY





stuff on 20100723-EMC request



CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24

DELL INC.

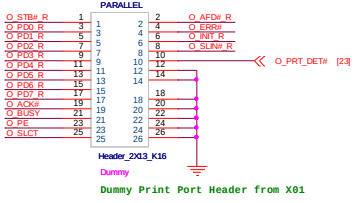
Title: **Flexbay USB**

DWG NO: *Gold Coast_MT/DT*

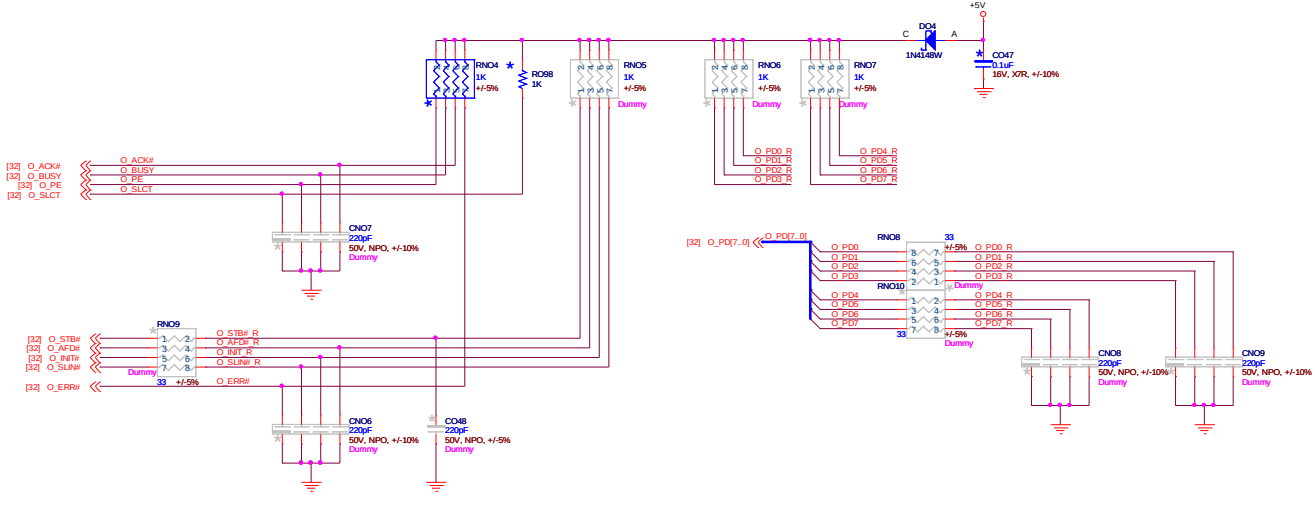
Rev: A00

Date: Friday, December 24, 2010 Sheet 61 of 70

Print Port



Dummy Print Port Header from X01



DELL INC.		
Title	PRT Port	
DWG NO	Gold Coast_MT/DT	Rev A00
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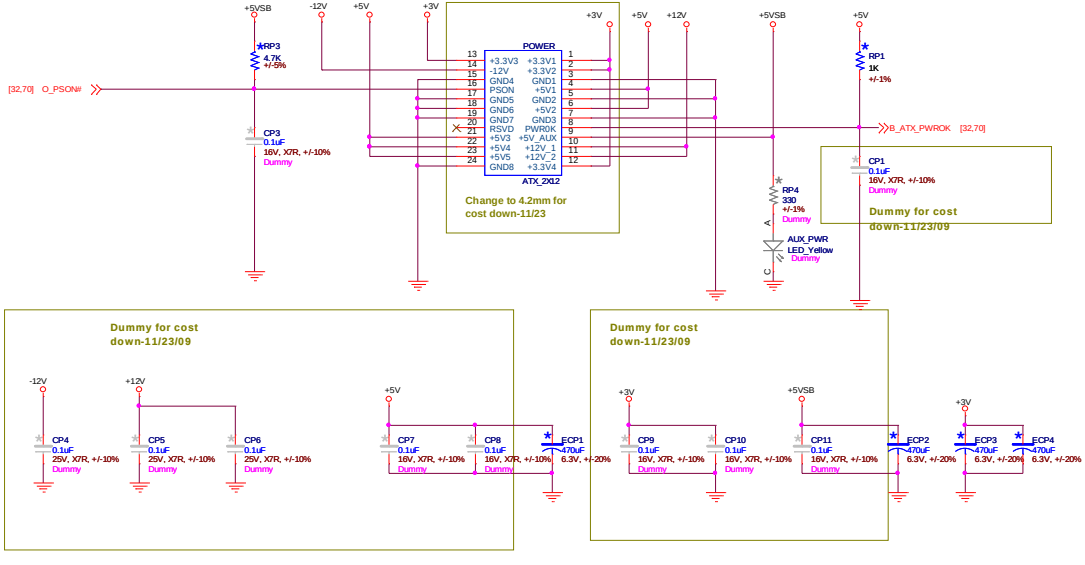
ATX POWER CONNECTOR



DELL INC.

Title: **Power Conn**

DWG NO: ***Gold Coast_MT/DT***

Rev: A00

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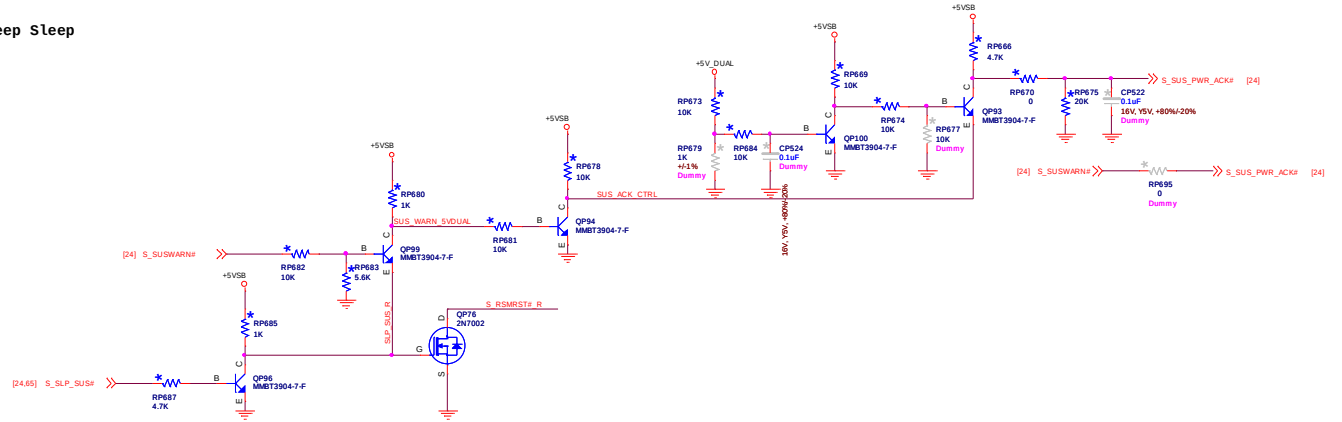
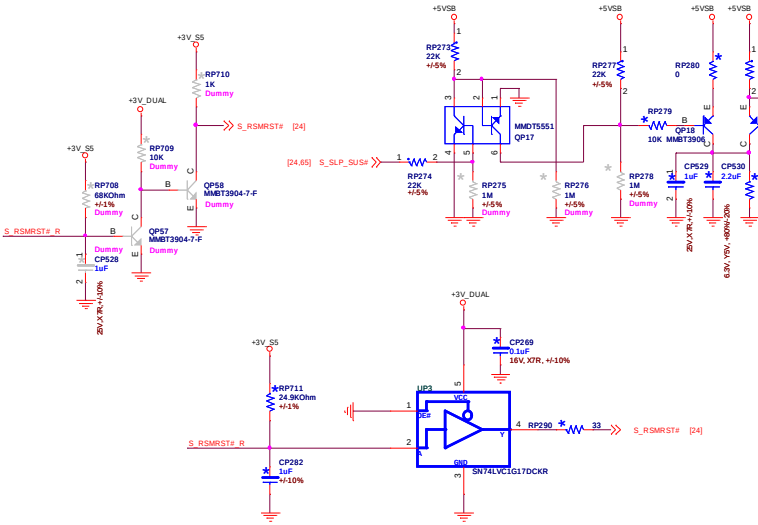
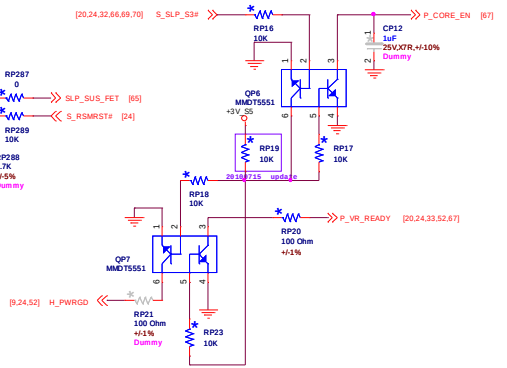
For Deep Sleep



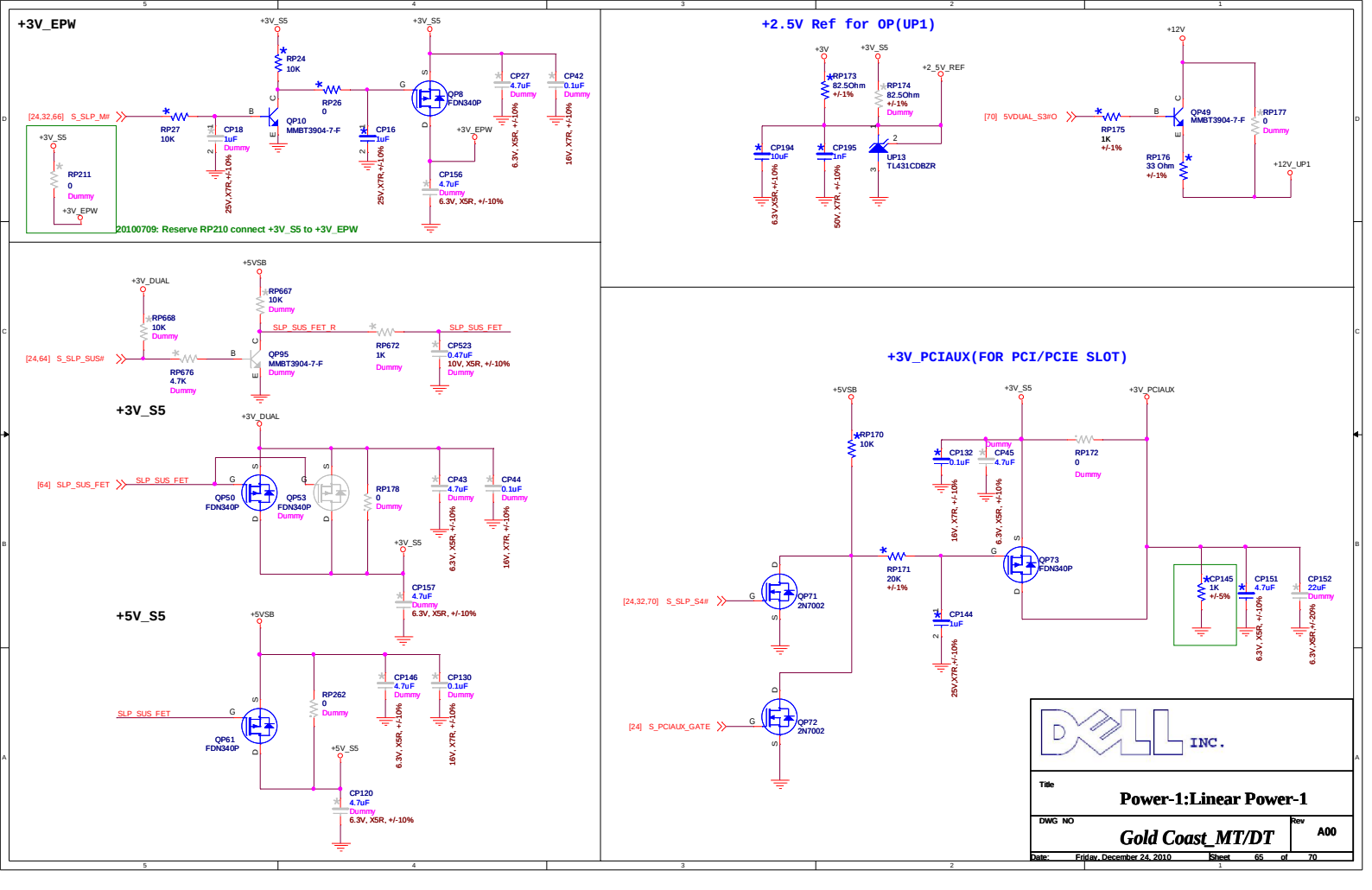
RESUME RESET Logic



VR_READY DEFENSIVE



DELL INC.		
Title	Power Sequence	
DWG NO	Gold Coast_MT/DT	Rev A00
Date: Friday, December 24, 2010	Sheet 64 of 70	


+3V_EPW
+3V_S5
RP24
10K
RP26
0
QP10
MMBT3904-7-F
QP8
FDN340P
CP27
4.7uF
Dummy
CP42
0.1uF
Dummy
[24,32,66] S_SLP_M#
RP27
10K
CP18
1uF
Dummy
CP16
1uF
RP211
0
Dummy
+3V_EPW
CP156
4.7uF
Dummy
6.3V, XSR, +/-10%
25V,X7R,+/-10%
6.3V, XSR, +/-10%
16V, X7R, +/-10%
20100709: Reserve RP210 connect +3V_S5 to +3V_EPW
+2.5V Ref for OP(UP1)
+3V
RP173
82.5Ohm
+/-1%
RP174
82.5Ohm
+/-1%
Dummy
+2_5V_REF
CP194
10uF
CP195
1nF
UP13
TL431CDBZR
6.3V,X5R,+/-10%
50V, X7R, +/-10%
+12V
[70] 5VDUAL_S3#O
QP49
MMBT3904-7-F
RP175
1K
+/-1%
RP177
0
Dummy
RP176
33 Ohm
+/-1%
+12V_UP1
+5VSB
+3V_DUAL
RP667
10K
Dummy
RP668
10K
Dummy
SLP_SUS_FET_R
SLP_SUS_FET
[24,64] S_SLP_SUS#
QP95
MMBT3904-7-F
Dummy
RP672
1K
Dummy
CP523
0.47uF
10V, XSR, +/-10%
Dummy
RP676
4.7K
Dummy
+3V_S5
[64] SLP_SUS_FET
QP50
FDN340P
QP53
FDN340P
Dummy
RP178
0
Dummy
CP43
4.7uF
Dummy
CP44
0.1uF
Dummy
CP157
4.7uF
Dummy
6.3V, XSR, +/-10%
+5V_S5
QP61
FDN340P
RP262
0
Dummy
CP146
4.7uF
Dummy
CP130
0.1uF
Dummy
CP120
4.7uF
Dummy
6.3V, XSR, +/-10%
+3V_PCIAUX(FOR PCI/PCIE SLOT)
+3V_PCIAUX
RP170
10K
CP132
0.1uF
CP45
4.7uF
RP172
0
Dummy
RP171
20K
+/-1%
QP73
FDN340P
[24,32,70] S_SLP_S4#
QP71
2N7002
CP144
1uF
[24] S_PCIAUX_GATE
QP72
2N7002
CP145
1K
+/-5%
CP151
4.7uF
CP152
22uF
Dummy
16V, X7R, +/-10%
6.3V, XSR, +/-10%
25V,X7R,+/-10%
6.3V,X5R,+/-20%
DELL INC.
Title
Power-1:Linear Power-1
DWG NO
Gold Coast_MT/DT
Rev
A00
Date: Friday, December 24, 2010
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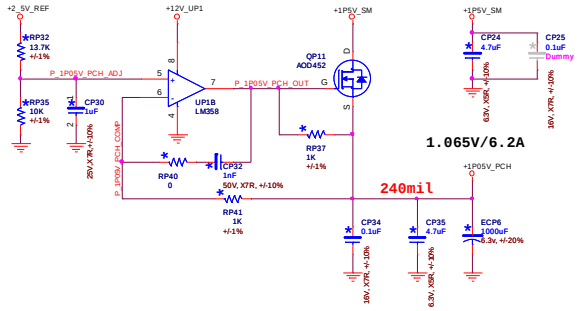
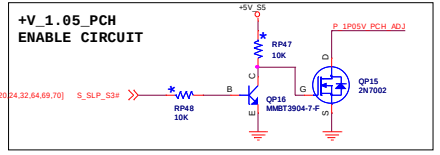
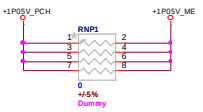
+V_1.05_PCH

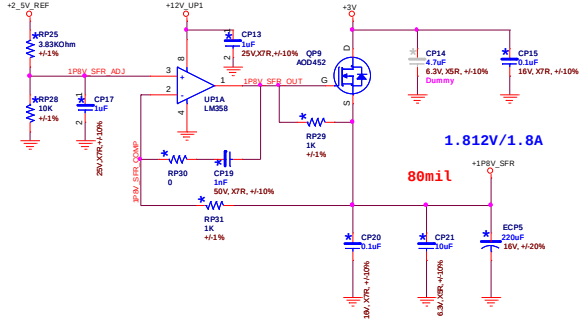


+V_1.05_PCH ENABLE CIRCUIT

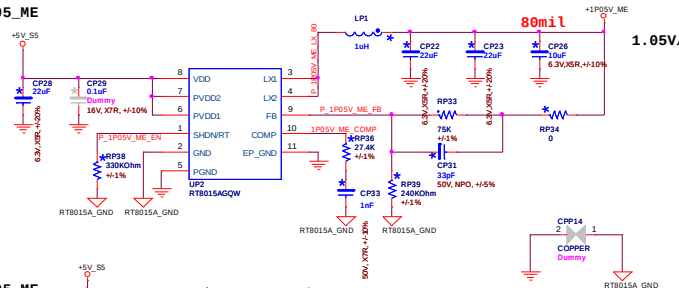




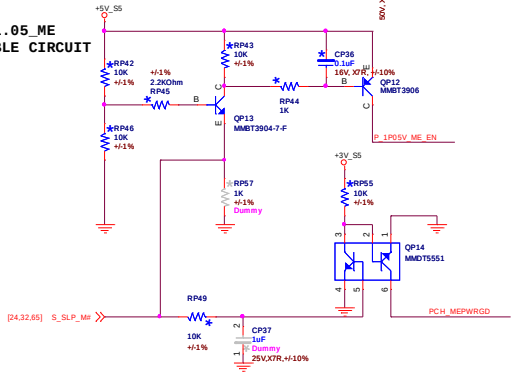
+V_1P8_SFR

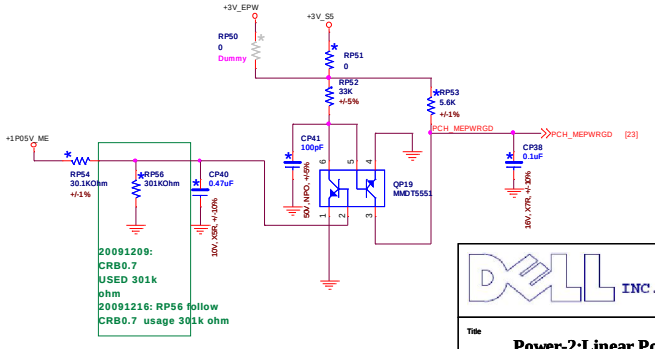


+V_1.05_ME



+V_1.05_ME ENABLE CIRCUIT





DELL INC.

Title	Power-2:Linear Power-2
DWG NO	Gold Coast_MT/DT
Rev	A00
Date:	Friday, December 24, 2010
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Sugar Bay VR12 POWER - 4+1 PHASE

VCC_CORE

VCC_AXG

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

3PHASE OPTION

VCORE VBOOT SET AT 0V

V_GT IMAX SET AT 35A

PWM ADDRESS

VCORE IMAX SET AT 120A

OPTION: DISALBE V_GT

PUT COLSE TO V_GT HOT SPOT

work F= 300khz

BOTTOM PAD CONNECT TO GND Through 4 VIAs

PUT COLSE TO VCORE HOT SPOT

Set 110deg OTP

Green mark is update from 20100720

Green mark is update from 20100726

Green mark is update from 20100830

Green mark is update from 20101012

DELL INC.

Title: Power-3: Vcore PWM

DWG NO: Gold Coast_MT/DT

Rev: A00

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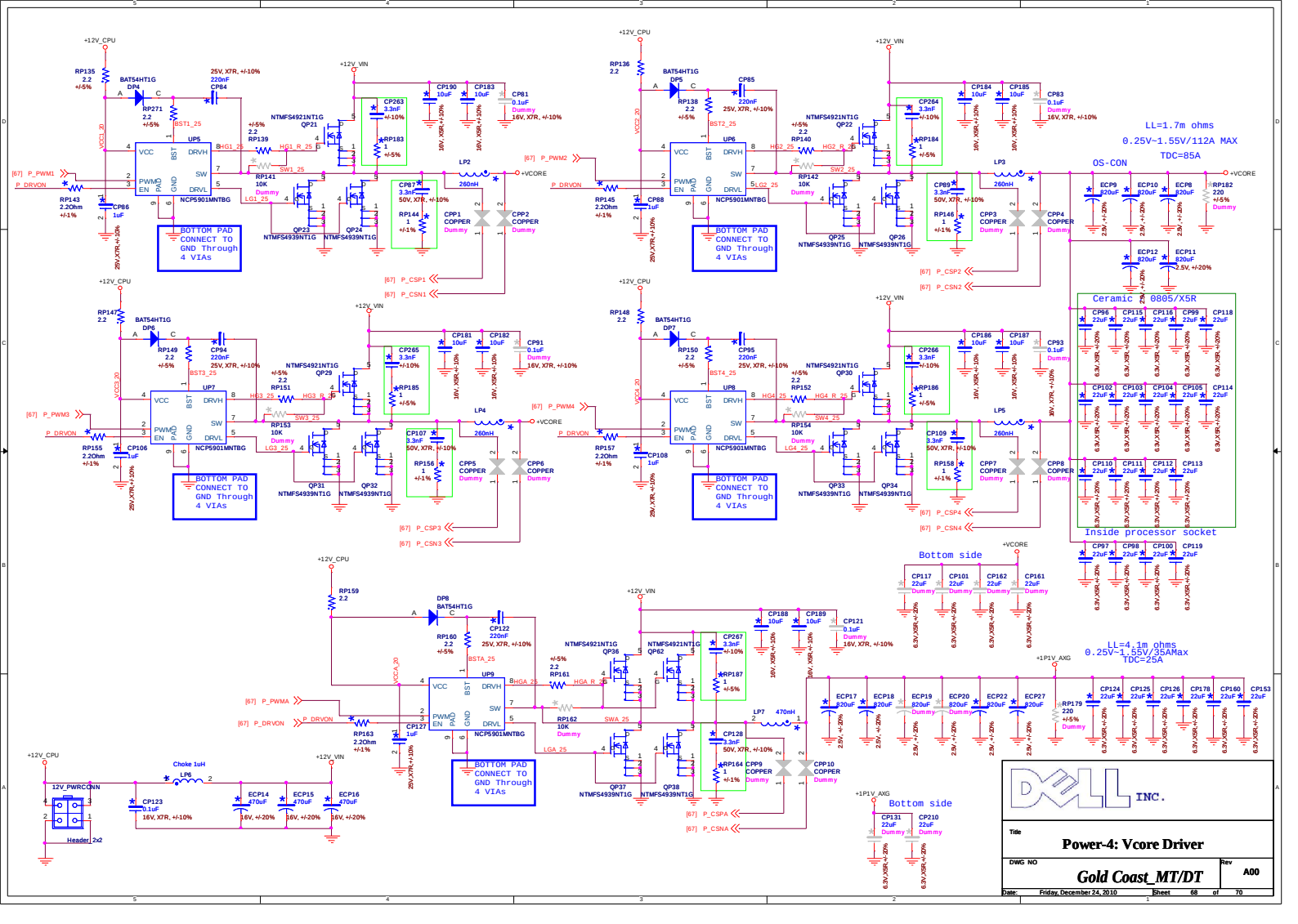
LL=1.7m ohms
0.25V~1.55V/112A MAX
TDC=85A
OS-CON
Ceramic 0805/X5R
Inside processor socket
Bottom side
LL=4.1m ohms
0.25V~1.55V/35AMax
TDC=25A
Bottom side
DELL INC.
Title
Power-4: Vcore Driver
DWG NO
Gold Coast_MT/DT
Rev
A00
Date: Friday, December 24, 2010
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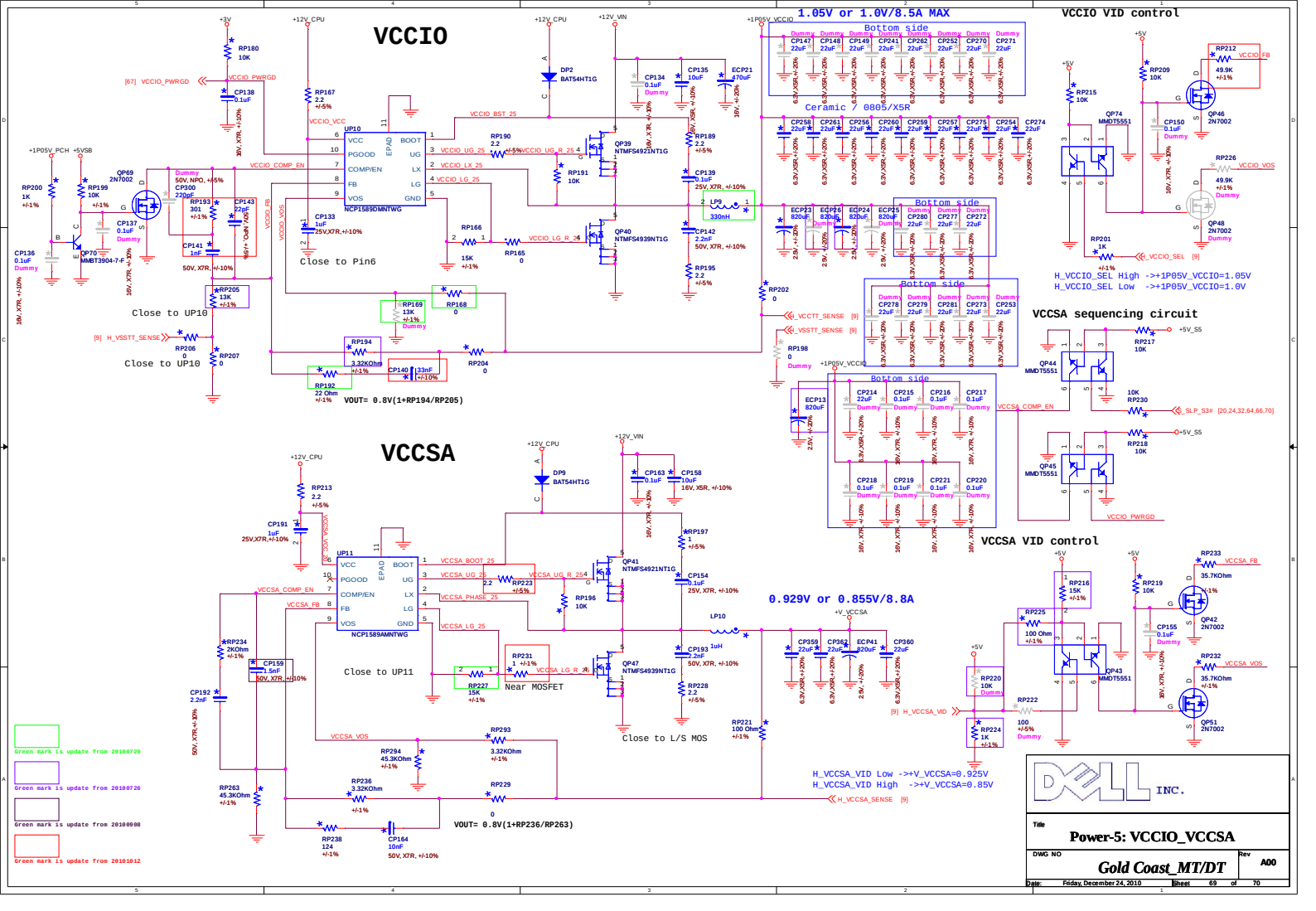
VCCIO
1.05V or 1.0V/8.5A MAX
VCCIO VID control
Ceramic 7 0805/X5R
Bottom side
Close to Pin6
Close to UP10
Close to UP10
VOUT= 0.8V(1+RP194/RP205)
H_VCCIO_SEL High ->+1P05V_VCCIO=1.05V
H_VCCIO_SEL Low ->+1P05V_VCCIO=1.0V
VCCSA sequencing circuit
VCCSA
0.929V or 0.855V/8.8A
VCCSA VID control
Close to UP11
Near MOSFET
Close to L/S MOS
VOUT= 0.8V(1+RP236/RP263)
H_VCCSA_VID Low ->+V_VCCSA=0.925V
H_VCCSA_VID High ->+V_VCCSA=0.85V
Green mark is update from 20100720
Green mark is update from 20100726
Green mark is update from 20100908
Green mark is update from 20101012
DELL INC.
Title
Power-5: VCCIO_VCCSA
DWG NO
Gold Coast_MT/DT
Rev
A00
Date: Friday, December 24, 2010
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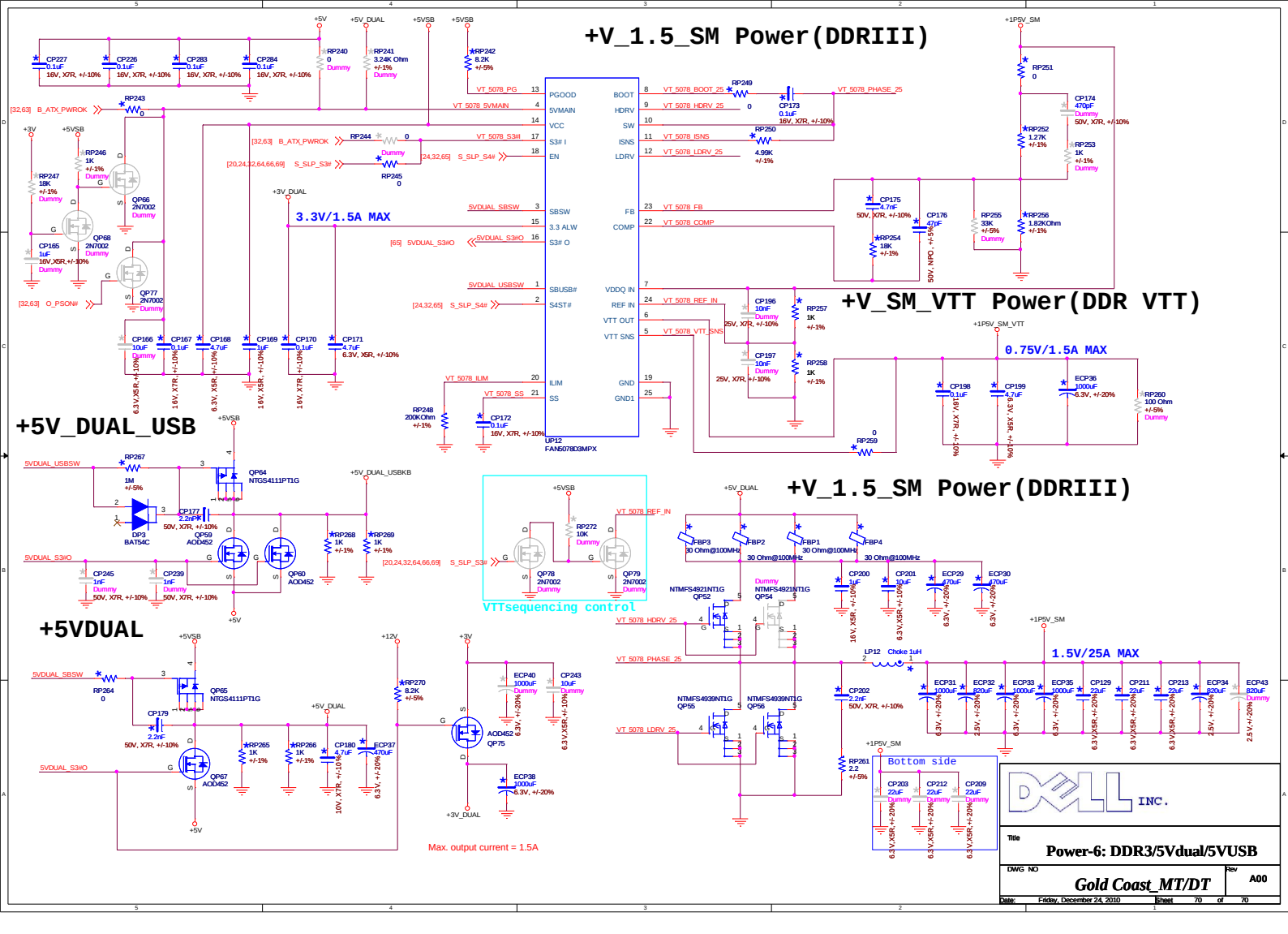
+V_1.5_SM Power(DDRIII)
+V_SM_VTT Power(DDR VTT)
+5V_DUAL_USB
+V_1.5_SM Power(DDRIII)
+5VDUAL
3.3V/1.5A MAX
0.75V/1.5A MAX
1.5V/25A MAX
VTTsequencing control
Bottom side
Max. output current = 1.5A
UP12
FAN5078D3MPX
PGOOD
5VMAIN
VCC
S3# I
EN
BOOT
HDRV
SW
ISNS
LDRV
SBSW
3.3 ALW
S3# O
SBUSB#
S4ST#
FB
COMP
VDDQ IN
REF IN
VTT OUT
VTT SNS
ILIM
SS
GND
GND1
DELL INC.
Power-6: DDR3/5Vdual/5VUSB
Gold Coast_MT/DT
A00
Friday, December 24, 2010
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IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot3	C	D	A	B	18	0	0

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Clock Gen.

FREQ	C_CK_BSEL0	C_CK_BSEL1	C_CK_BSEL2
100	1	0	1
133	1	0	0

Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	C_CK505_33M_PCI2	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI4/SRC5_EN (PIN6)	C_CK505_33M_PCI4	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCIF5/ITP_EN (PIN7)	C_CK505_33M_PCI5	1	CPU_ITP
		0	SRC8 DEFAULT
PCI3/CFGP (PIN5)	C_CK505_33M_PCI3	Low	See CFG Table DEFAULT (Set SATA and SRC come from PLL4)
		Mid	See CFG Table
		High	See CFG Table

SIO SMSC5544

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#_R	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description
High	1.5V
Low	1.8V DEFAULT

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled. DEFAULT

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable DEFAULT
Low	Topblock swap mode: Enable

No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable DEFAULT

Integrated 1.05V VRM

INTVRMEN	Description
High	Integrated 1.05V VRM: Enable DEFAULT
Low	Integrated 1.05V VRM: Disable

TLS Confidentiality

GPIO15 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality DEFAULT

Flash Descriptor Override Strap

HDA_SDO	Description
High	Flash descriptor security will be override
Low	Disable ME in Manufacturing Mode DEFAULT

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description
Low	DMI Rx Termination Voltage DEFAULT

DMI Termination Voltage

NV_CLE (IN-PU)	Description
High	DMI and FDI Tx/Rx Termination Voltage DEFAULT

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
Low	High	Flash cycle routed to NAND
High	High	Flash cycle routed to SPI DEFAULT

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description
High	Enable DEFAULT
Low	Disable

Digital Port C Strap

DDPC_CTRLDATA	Description
High	Configure Port C DEFAULT
Low	Disable

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Title: GPIO/IRQ/IDSEL Table

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PCH GPIO Summary

GPIO	Type	Power Well	Default	IN-PU/PD	EX-PU/PD	Schematic Usage
GPIO[0]	I/O	Core	GPI	--	10k pull-up to +3V	S_PECI_REQ#
GPIO[1]	I/O	Core	GPI	20K IN-PU (only on TACH1)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_GPI_CHASSIS_ID0
GPIO[2]	IIOD	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPUSB_DETECT#
GPIO[3]	IIOD	Core	GPI	--	--	V_DDSP_C_HPD
GPIO[4]	IIOD	Core	GPI	--	8.2k pull-up to +3V	V_GPI_VGA_CBL_DET#
GPIO[5]	IIOD	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPPE_DETECT#
GPIO[6]	I/O	Core	GPI	20K IN-PU (only on TACH2)	10k pull-up to +3V	S_GPI_PCH_HS_DET#
GPIO[7]	I/O	Core	GPI	20K IN-PU (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_SHU2
GPIO[8]	I/O	Suspend	GPO	20K IN-PU	--	S_TP_OP#
GPIO[9]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	U_USB_OC_R_#5
GPIO[10]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	X_WLAN_WAKE#
GPIO[11]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	X4_WAKE#
GPIO[12]	I/O	Suspend	Native	--	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	L_LAN_DISABLE#
GPIO[13]	I/O	Suspend	GPI	--	10k pull-up to +2V_S5	X1_WAKE#
GPIO[14]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5	GPO_WL0M
GPIO[15]	I/O	Suspend	GPO	20K IN-PD	1k pull-up to +3V_S5 (dummy)	S_PCH_GP15
GPIO[16]	I/O	Core	GPI	--	10k pull-up to +3V 10k pull-down to GND (dummy)	H_SKTOCC_R_#
GPIO[17]	I/O	Core	GPI	20K IN-PU (only on TACH0)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_GPI_CHASSIS_ID1
GPIO[18]	I/O	Core	GPI	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	S_SATA1GP
GPIO[20]	I/O	Core	Native	--	10k pull-up to +3V 10k pull-down to GND (dummy)	S_FLEXBAY_HDR_CBL_DET#
GPIO[21]	I/O	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_GPI_BRD_REV0
GPIO[22]	I/O	Core	GPI	--	1k pull-up to +3V 4.7k pull-down to GND (dummy)	S_PCH_CONFIG_JUMPER
GPIO[23]	I/O	Core	Native	20K IN-PU	10k pull-up to +3V (dummy)	L_DRQ1#
GPIO[24]	I/O	Suspend	GPO	--	100k pull-up to +3V_S5	H_SKTOCC#
GPIO[27]	I/O	Deep Sleep	GPI	20K IN-PU	10k pull-up to +3V_DUAL 1k pull-down to GND (dummy)	S_GP27_PD
GPIO[28]	I/O	Suspend	GPO	20K IN-PU	10k pull-up to +3V_S5 1k pull-down to GND (dummy)	S_PCH_OP28_PU
GPIO[29]	I/O	Suspend	Native	--	1k pull-up to +3V_S5 (dummy)	S_SLP_LAN#
GPIO[30]	I/O	Deep Sleep	Native	--	10k pull-up to +3V_DUAL (dummy) 1k pull-down to GND (dummy)	S_SUSWARN#
GPIO[31]	I/O	Deep Sleep	GPI	TBD IN-PD	8.2k pull-up to +3V_DUAL	S_PSWD_CLR
GPIO[32]	I/O	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_SHU0
GPIO[33]	I/O	Core	GPO	--	---	--
GPIO[34]	I/O	Core	GPI	--	10k pull-up to +3V	PCH_GPIO34
GPIO[35]	I/O	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_SHU1
GPIO[36]	I/O	Core	GPI	20K IN-PD	---	S_PCH_GP36
GPIO[37]	I/O	Core	GPI	20K IN-PD	---	S_PCH_GP37
GPIO[38]	I/O	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_GPI_CHASSIS_ID2
GPIO[39]	I/O	Core	GPI	--	10k pull-up to +3V	A_FP_PRES#
GPIO[40]	I/O	Suspend	Native	--	---	U_USB_OC_R_#1
GPIO[41]	I/O	Suspend	Native	--	---	U_USB_OC_R_#2
GPIO[42]	I/O	Suspend	Native	--	---	U_USB_OC_R_#3
GPIO[43]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	U_USB_OC_R_#4
GPIO[44]	I/O	Suspend	Native	20K IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	S_INTRUD_CBL_DET#
GPIO[45]	I/O	Suspend	Native	--	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	O_COM_SER2_DET#
GPIO[46]	I/O	Suspend	Native	20K IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	S_GPI_BRD_REV1
GPIO[48]	I/O	Core	GPI	--	10k pull-up to +3V	S_GPIO48_PU
GPIO[49]	I/O	Core	GPI	--	8.2k pull-up to +3V	TMIN_SHIFT
GPIO[50]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#1
GPIO[51]	I/O	Core	Native	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	K_GNT#1
GPIO[52]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#2
GPIO[53]	I/O	Core	Native	20K IN-PU	1k pull-down to GND (dummy)	K_GNT#2
GPIO[54]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#3
GPIO[55]	I/O	Core	Native	20K IN-PU	1k pull-down to GND (dummy)	K_GNT#3
GPIO[57]	I/O	Suspend	GPI	--	10k pull-up to +3V_S5 (dummy) 47k pull-down to GND	S_GPI057_PD
GPIO[58]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_CLK
GPIO[59]	I/O	Suspend	Native	--	---	U_USB_OC_R_#0
GPIO[60]	I/O	Suspend	Native	--	2.2k pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#
GPIO[61]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	S_LPCPD#
GPIO[62]	I/O	Suspend	Native	--	--	S_SUSCLK
GPIO[63]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_PCIAUX_GATE
GPIO[64]	I/O	Core	Native	20K IN-PD	---	S_TP_CLKOUTFLEX0
GPIO[65]	I/O	Core	Native	20K IN-PD	---	C_14M_SIO_R
GPIO[66]	I/O	Core	Native	20K IN-PD	---	S_TP_CLKOUTFLEX2
GPIO[67]	I/O	Core	Native	20K IN-PD	---	C_14M_TPM_R
GPIO[68]	I/O	Core	GPI	20K IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_BRD_REV2
GPIO[69]	I/O	Core	GPI	20K IN-PU (only on TACH5)	10k pull-up to +3V	O_FRT_DET#
GPIO[70]	I/O	Core	Native	20K IN-PU (only on TACH6)	8.2k pull-up to +3V	S_FP_CHAS_DET#
GPIO[71]	I/O	Core	Native	20K IN-PU (only on TACH7)	10k pull-up to +3V	--
GPIO[72]	I/O	Suspend	Native (Mobile Only)	20K IN-PU	10k pull-up to +3V_S5	S_PCH_GP72_PU
GPIO[74]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_MFG_MODE_OR
GPIO[75]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_DATA

GPIO	PIN NAME	Power well	Buffer Type	EX-PU/PD	Signal Name
GP000	(DAQ_LED3#) GP000	VTR	IO	NA	O_DAQ_LED3#
GP001	(DAQ_LED1#) GP001	VTR	IO	NA	O_DAQ_LED1#
GP002	(DAQ_LED2#) GP002	VTR	IO	NA	O_DAQ_LED2#
GP003	(DAQ_LED4#) GP003	VTR	IO	NA	O_DAQ_LED4#
GP004	GP004	VTR	IO	NA	NC
GP005	(H_CPURST#) GP005 / PECI_REQUEST#	VTR	IO/OD	1.5k pull-up to +3V	O_PECI_REQ#
GP006	YELLOW## / GP006	VTR	OA0	NA	O_YELLOW#
GP007	GREEN## / GP007	VTR	OA0	NA	O_GREEN#
GP010	SMBDAT2 / GP010	VTR	IOD/A0	8.2k pull-up to +2V_DUAL(dummy)	S_SMLINK1_DATA_R
GP011	SMBCLK2 / GP011	VTR	IOD/A0	8.2k pull-up to +2V_DUAL (dummy)	S_SMLINK1_CLK_R
GP012	GP012	VTR	IO	8.2k pull-up to +3V_DUAL	SPI_DI
GP013	GP013	VTR	IO	NA	NC
GP014	(TMIN_SHIFT) GP014	VTR	IO	8.2k pull-up to +3V	TMIN_SHIFT
GP015	PWRBTN## / GP015	VTR	I/O	1k pull-up to +3V_DUAL	O_PWRBTN#IN
GP016	PROCHOT_IN##/PROCHOT_OUT#/GP016	VTR	I/OD/IOD	51ohm pull-up to +1P05V_VCCIO	H_PROCHOT#
GP017	TACH1 / GP017	VTR	I/O	1k pull-up to +3V	O_SEN_CPUFAN
GP020	TACH2 / GP020	VTR	I/O	1k pull-up to +3V	O_SEN_CHAFAN
GP021	TACH3 / GP021	VTR	I/O	NA	NC
GP022	PWM1 / GP022	VTR	OD/A0	4.7k pull-up to +2V	O_CPUFAN_PWM
GP023	PWM2 / GP023	VTR	OD/A0	4.7k pull-up to +2V	O_CHAFAN_PWM
GP024	PWM3 / GP024	VTR	OD/A0	NA	NC
GP026	(FP_CBL_DET#) GP026	VTR	IO	8.2k pull-up to +3V_S5	O_FP_CBL_DET#
GP026	PCI_RST_SYS## / GP026	VTR	OA0	NA	X_PLTRST_PCIE_SLOT#
GP027	PCI_RST_SLOT5## / GP027	VTR	OA0	NA	H_RESET#
GP030	PS_ON## / GP030	VTR	OD/A0	4.7k pull-up to +5VSB	O_PSON#
GP031	(PC_SPKR_DET) GP031	VTR	IO	8.2k pull-up to +2V_DUAL	O_AUD_PCSPKR_DET#
GP032	GP032	VTR	IO	NA	NC
GP033	PWR_GOOD_3V / GP033	VTR	OA0	NA	PWRGD_3V
GP034	RSMRST## / GP034	VTR	OA0	0.1uF pull-down to GND	O_RSMRST#
GP035	GP035	VTR	IO	8.2k pull-up to +3V_DUAL	O_BC_CLK
GP036	GP036 / SMB_CLK1	VTR	IO/OD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBCLK_PCI_R
GP040	GP040 / SMB_DAT1	VTR	IO/OD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBDATA_PCI_R
GP041	GP041 / IO_PME#	VTR	IO/OD	1.5k pull-up to +3V_S5	O_IO_PME#
GP042	GP042 / DRVDEN0	VTR	IO/O	100k pull-up to +3V_DUAL(dummy)	T_ESKTA_DET#
GP043	DCD1#/ GP043 / MCDAT	VTR	I/IO/O	NA	O_DCD1#_R
GP044	DSR1#/ GP044 / MCCLK	VTR	I/IO/O	NA	O_DSR1#_R
GP045	RXD1 / GP045	VTR	I/O	NA	O_RXD1_R
GP046	RTS1# / GP046	VTR	OA0	NA	O_RTS1#_R
GP047	(5V_PRSNT) GP047 / TXD1	VTR	IO/O	NA	O_TXD1_R
GP050	CTS1#/ GP050	VTR	I/IO	NA	O_CTS1#_R
GP051	DTR1#(TEST_EN)/ GP051	VTR	OA0	8.2k pull-up to +2V_DUAL(dummy) 30k pull-down to GND	O_DTR1#_R
GP052	RI1#/ GP052	VTR	I/O	NA	O_RI1#_R
GP053	GP053 / DCD2#	VTR	IOI	2.2k pull-up to +3V	O_DCD2#_R
GP054	GP054 / DSR2#	VTR	IOI	2.2k pull-up to +3V	O_DSR2#_R
GP055	GP055 / RXD2	VTR	IOI	2.2k pull-up to +3V	O_RXD2_R
GP056	(PWR2_PRSNT) GP056 / RTS2#	VTR	IO/O	30k pull-up to +3V	O_RTS2#_R
GP057	(MB_REV_P3) GP057 / TXD2	VTR	IO/O	30k pull-up to +3V	O_TXD2_R
GP060	GP060 / CTS2#	VTR	IOI	2.2k pull-up to +3V	O_CTS2#_R
GP061	(MEM_REV_P0) GP061 / DTR2#	VTR	IO/O	30k pull-up to +3V	O_DTR2#_R
GP062	GP062 / RI2#	VTR	IOI	2.2k pull-up to +3V	O_RI2#_R
GP063	GP063 / KBDRST#	VTR	IO/OD	1.5k pull-up to +3V	O_KB_RST#
GP064	GP064 / A20M	VTR	IO/OD	1.5k pull-up to +3V	O_GA20
GP065	SLP_S3# / GP065	VTR	I/O	NA	S_SLP_S3#
GP066	SLP_S4_S5# / GP066	VTR	I/O	NA	S_SLP_S4#
GP067	PWRGD_PS / GP067	VTR	I/O	1k pull-up to +5V	B_ATX_PWROK
GP070	SPEAKER (DAQ_EN#) / GP070	VTR	OA0	8.2k pull-up to +2V_DUAL(dummy) 8.25k pull-down to GND	O_SPEAKER
GP071	(SLP_M#) GP071 / IO_SMI#	VTR	IO/OD	NA	S_SLP_M#
GP072	PECI / LVSNB_CLK1 / GP072	VTR	PECI_IO/IOD/IO	1k pull-up to +1P05V_VCCIO (dummy)	H_PECI_R
GP073	PECI_READY / LVSNB_DAT1 / GP073	VTR	PECI_I/OD/A0	1k pull-up to +1P05V_VCCIO	O_GP73_PU

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Title: **GPIO Table**

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