MS-7379 uATX

PCB Size 244*215mm(OSP)

Version :2.0

Cover Sheet	1
Block Diagram/Clock Map/Power Map	2-4
Intel LGA775 CPU	5-7
Intel Bearlake G31 - MCH	8-11
Intel ICH7 - PCI & DMI & CPU & IRQ	12
Intel ICH7 - LPC & ATA & USB & GPIO	13
Intel ICH7 - POWER	14
Clock Gen- RTM876-660	15
LPC I/O - W83627DHG	16
Azalia - ALC883/888/861D/660	17
LAN REALTEK RTL8101E/8111B	18
DDR II System Memory 1 & 2	19-20
DDR II VTT Decoupling	21
PCI EXPRESS X16 &X1 Slot	22
PCI Slot 1 & 2	23
ATA33/66/100 IDE & SATA Connectors	24
VGA connector	25
USB Connectors	26
ATX Connetcor & Front Panel & Fan	27
ACPI MS7 & SYSTEM POWER	28
VRM 11 -ST L6703	29
HISTORY	30
AutoBOM parts	31-34

CPU:

Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield processors in LGA775 Package.

System Chipset:

Intel Bearlake G31 - MCH (North Bridge)
Intel ICH7/ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI 4M EEPROM
Aliza Codec -- ALC883/888/861D/660
LPC Super I/O -- W83627DHG
LAN-- REALTEK RTL8101E/8111B
Clock Gen- RTM876-660

Main Memory:

Dual Channel DDR II * 2 (Max 2GB)

Expansion Slots:

PCI2.2 SLOT * 2
PCI EXPRESS X16 SLOT
PCI EXPRESS X1 SLOT

RICH PWM:

Controller: ST L6703

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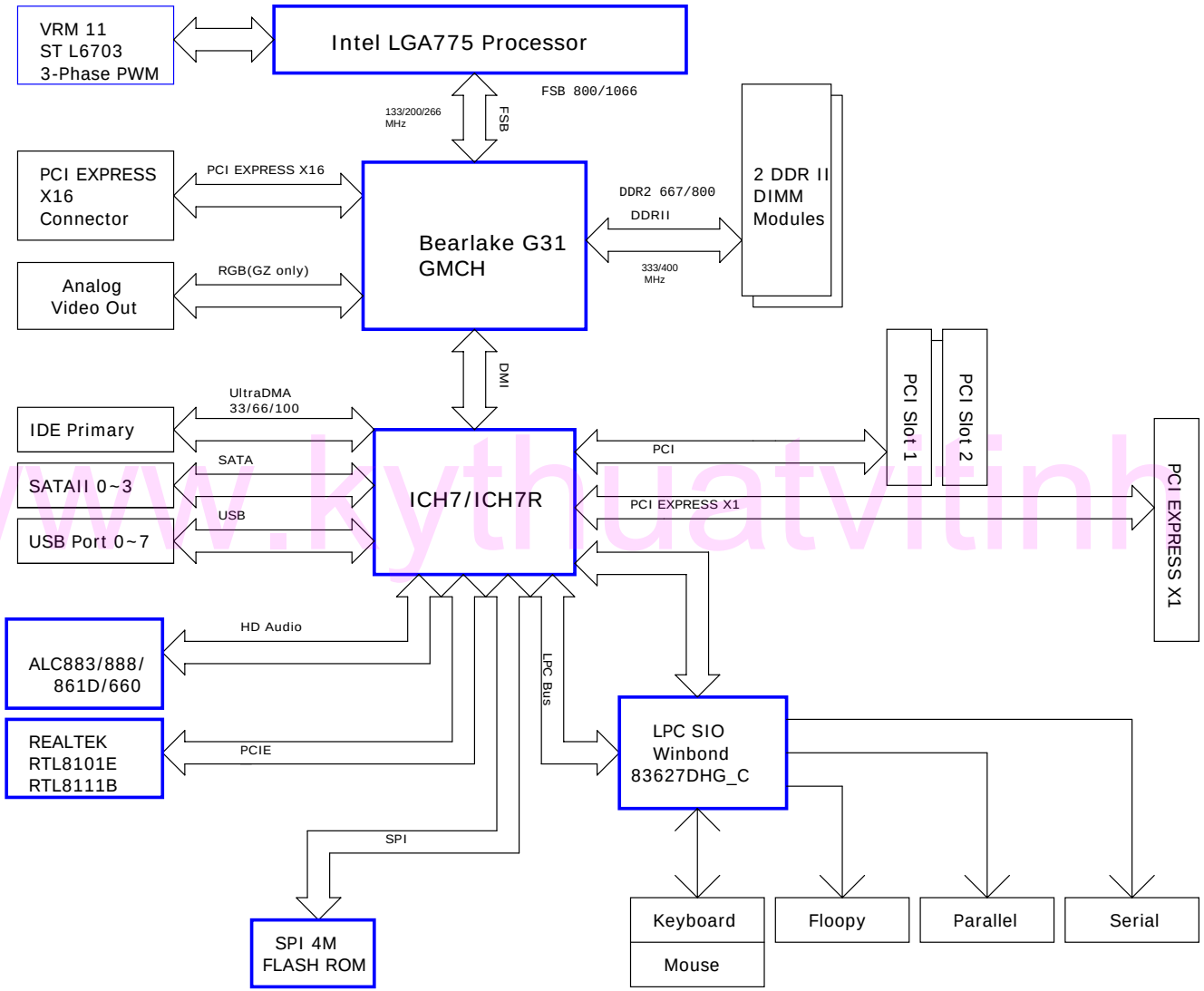
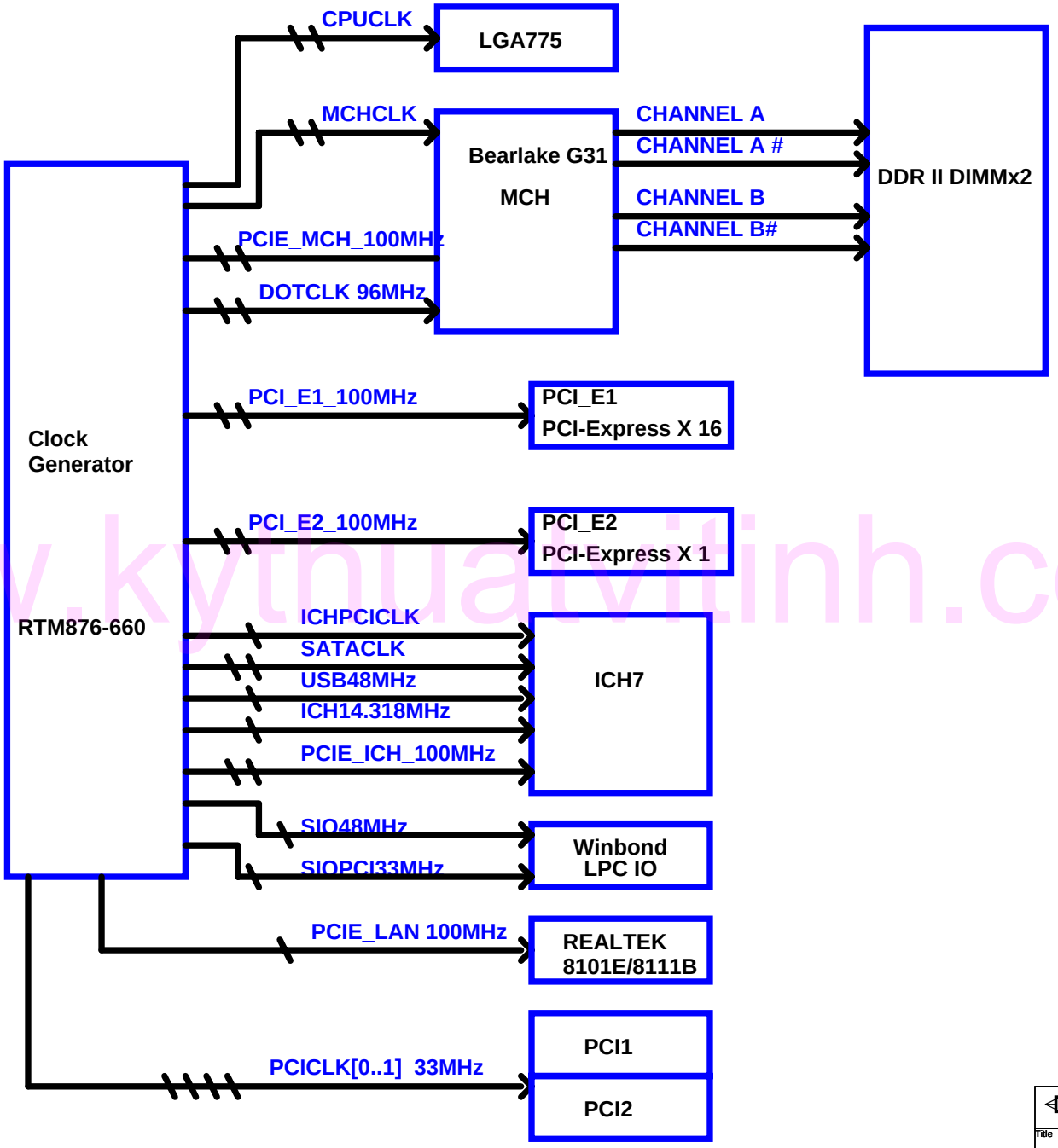
Title	COVER SHEET	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 1 of 34	

Block Diagram



MSI	MICRO-STAR INt'L CO., LTD.	
Title	BLOCK DIAGRAM	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 2 of 34	

CLOCK MAP



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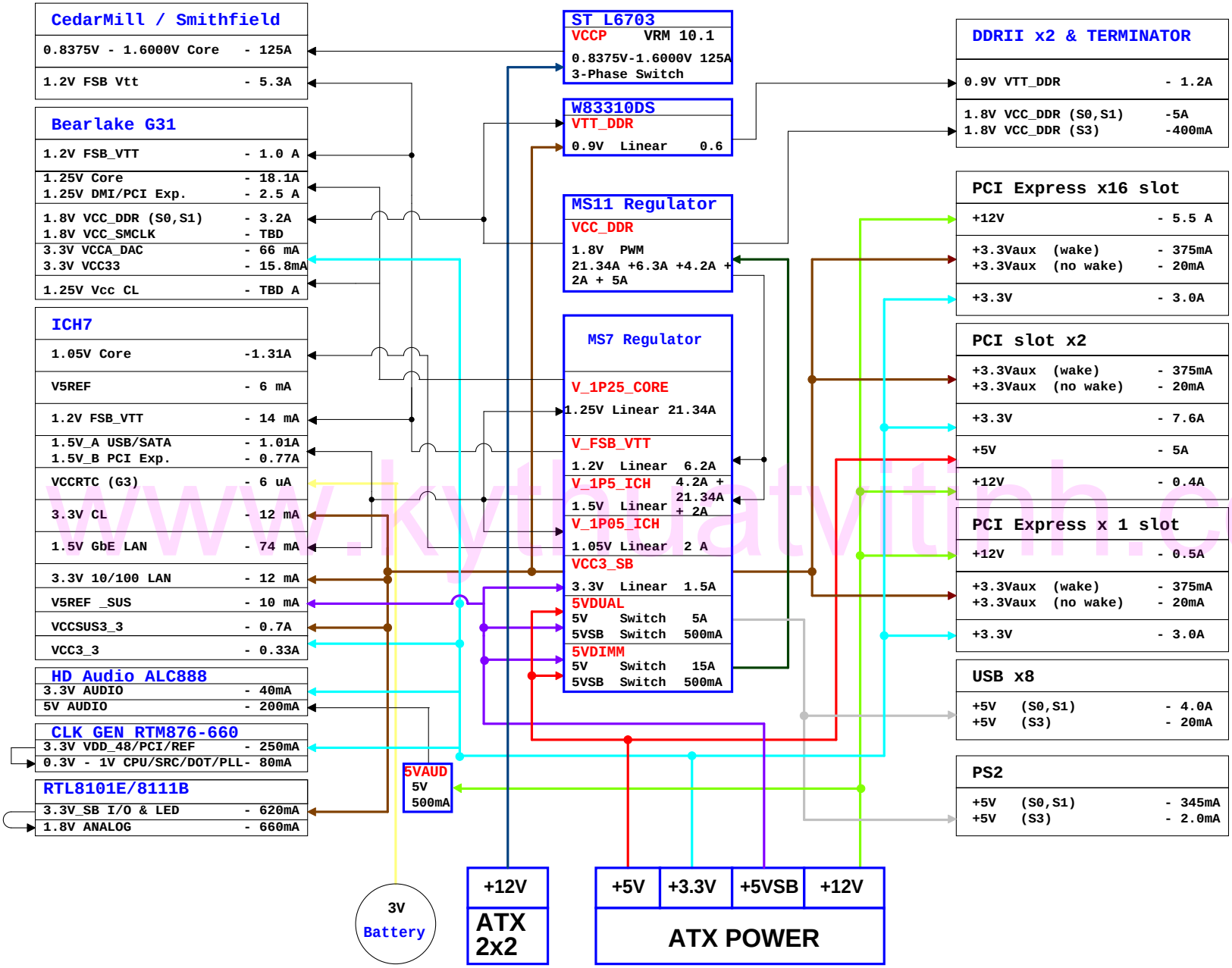
Title	CLOCK MAP	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 3 of 34	



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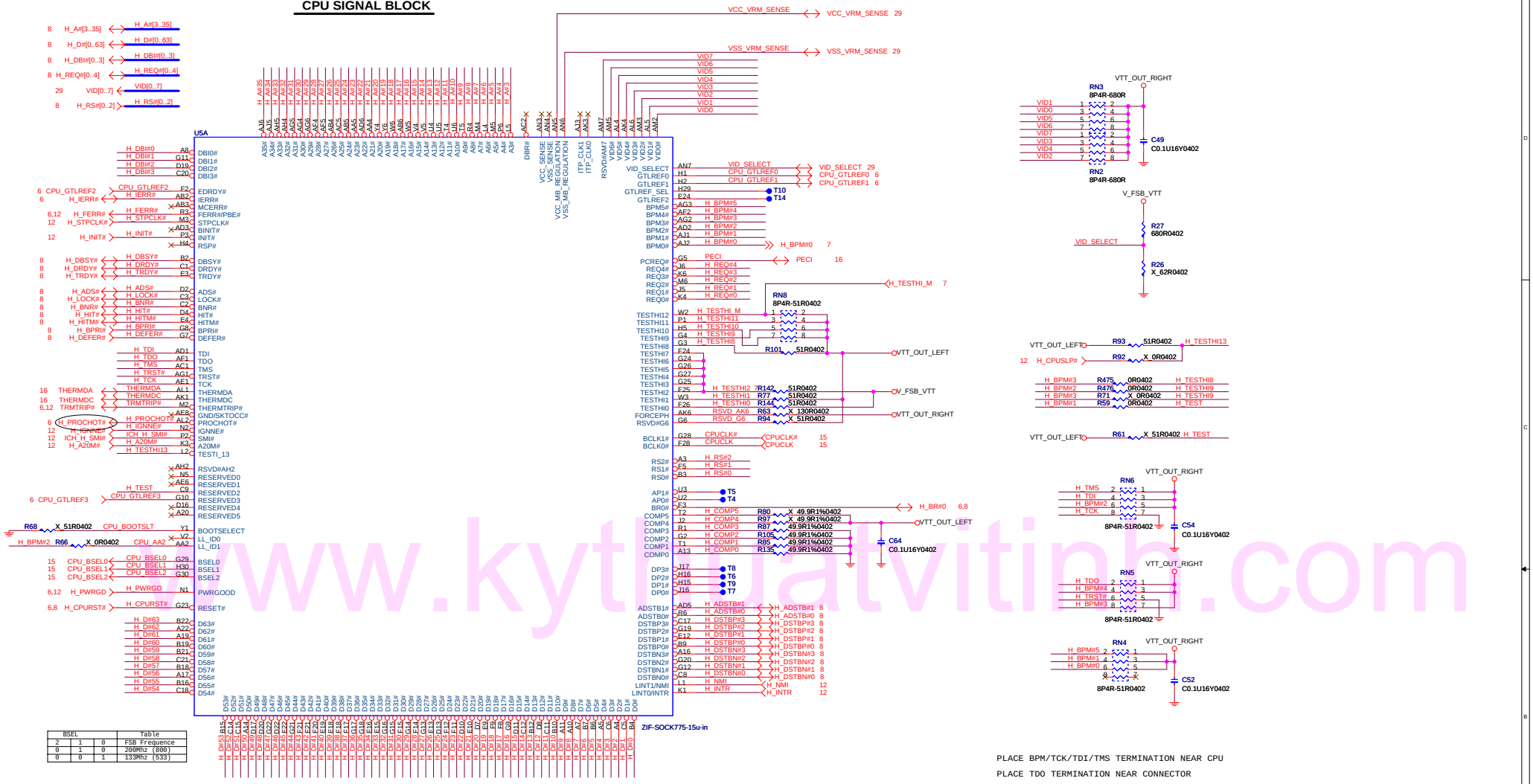
Title: POWER MAP

Size | Document Number: MS-7379 | Rev: 2.0

Date: Thursday, July 12, 2007 | Sheet 4 of 34

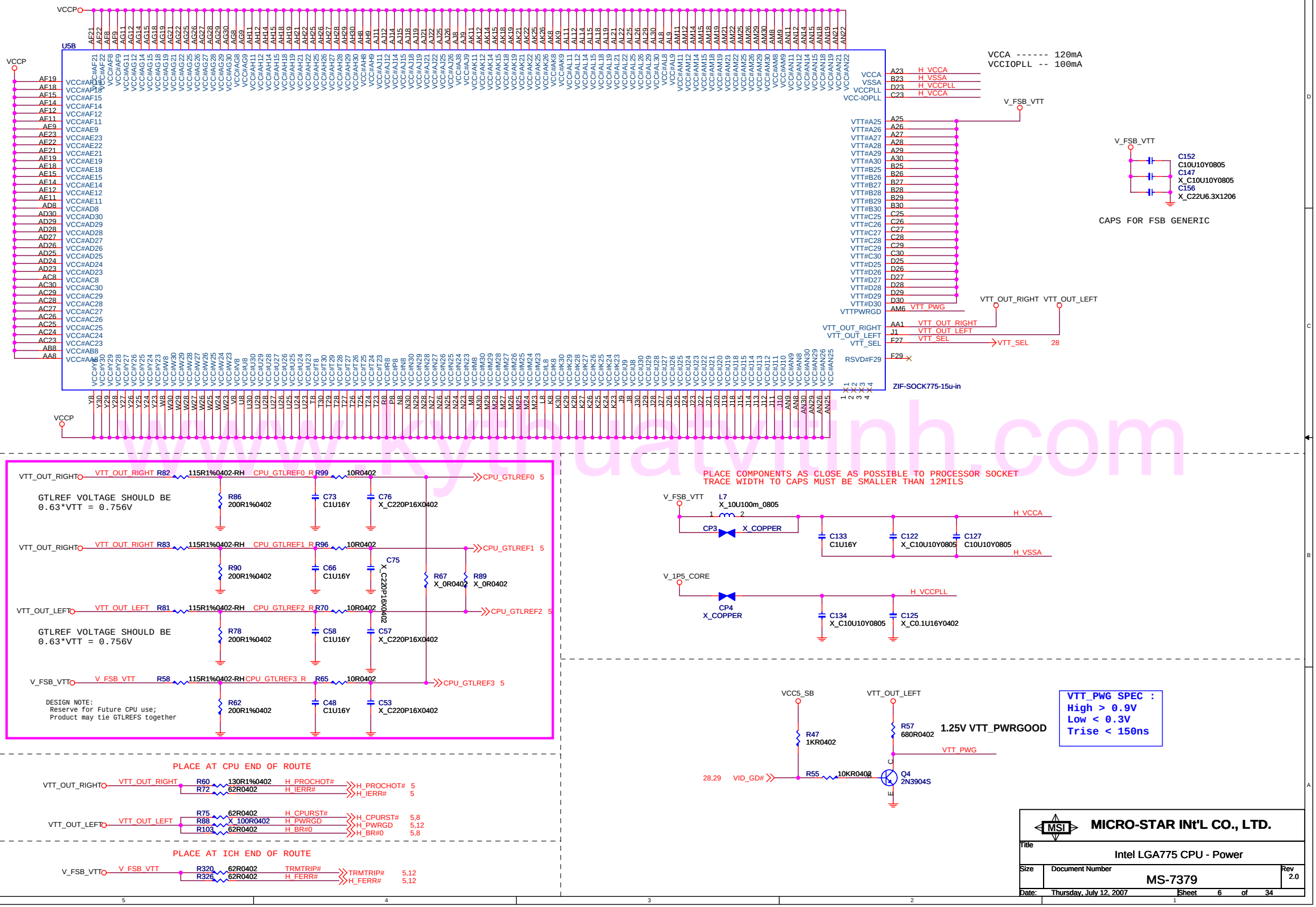
CPU SIGNAL BLOCK



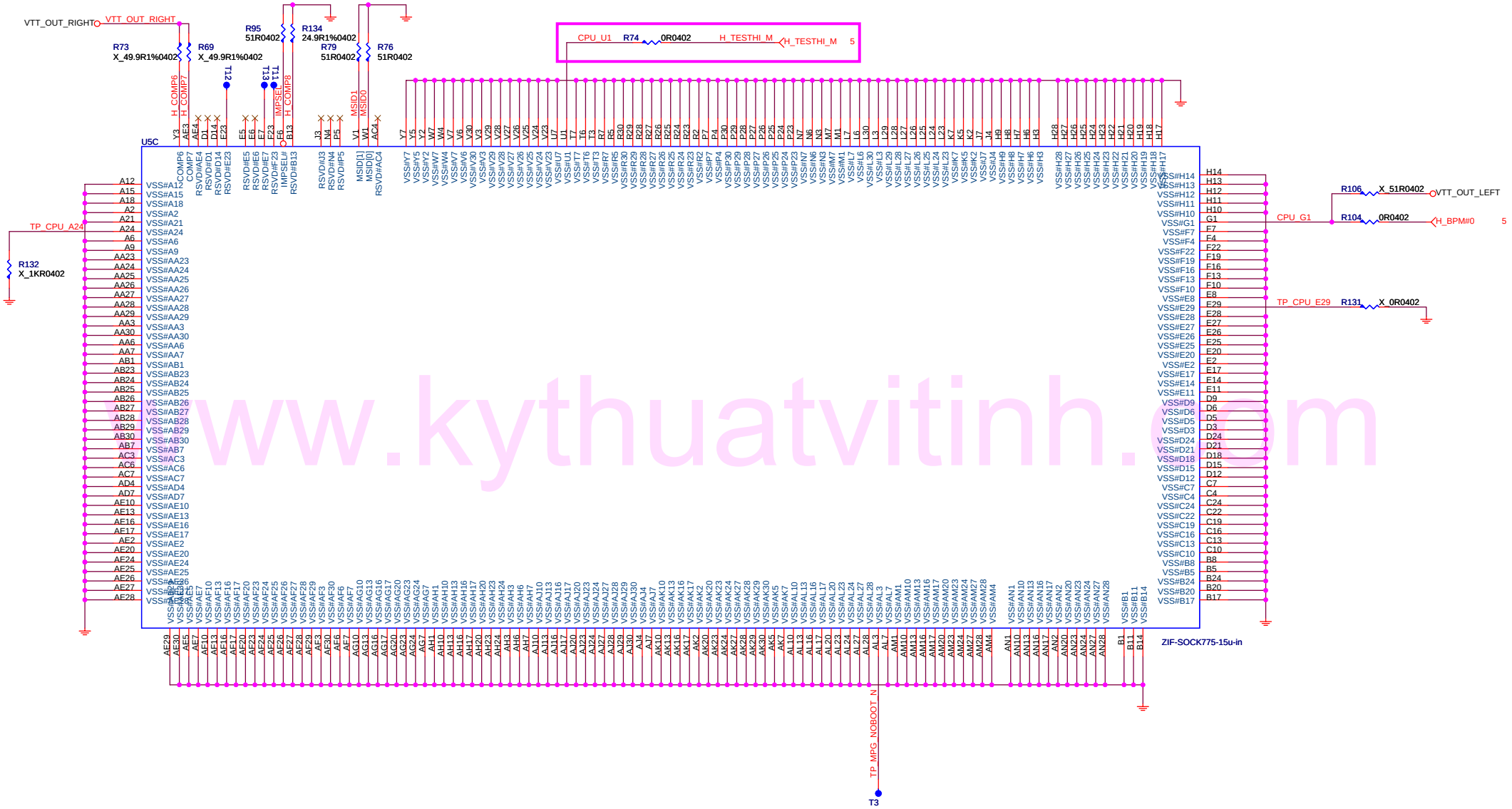
PLACE BPM/TCK/TDI/TMS TERMINATION NEAR CPU

PLACE TDO TERMINATION NEAR CONNECTOR

MSI	MICRO-STAR INt'L CO., LTD.	
Title	Intel LGA775 CPU - Signals	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 5 of 34	


VCCP
U5B
VCCA ----- 120mA
VCCIOPLL -- 100mA
VCCA
VSSA
VCCPLL
VCC-IOPLL
H_VCCA
H_VSSA
H_VCCPLL
H_VCCA
V_FSB_VTT
VTT_PWG
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
RSVD#F29
ZIF-SOCK775-15u-in
C152
C10U10Y0805
C147
X_C10U10Y0805
C156
X_C22U6.3X1206
CAPS FOR FSB GENERIC
VTT_OUT_RIGHT R82 115R1%0402-RH CPU_GTLREF0_R R99 10R0402
CPU_GTLREF0
GTLREF VOLTAGE SHOULD BE
0.63*VTT = 0.756V
R86 200R1%0402
C73 C1U16Y
C76 X_C220P16X0402
VTT_OUT_RIGHT R83 115R1%0402-RH CPU_GTLREF1_R R96 10R0402
CPU_GTLREF1
R90 200R1%0402
C66 C1U16Y
C75 X_C220P16X0402
R67 X_0R0402
R89 X_0R0402
VTT_OUT_LEFT R81 115R1%0402-RH CPU_GTLREF2_R R70 10R0402
CPU_GTLREF2
GTLREF VOLTAGE SHOULD BE
0.63*VTT = 0.756V
R78 200R1%0402
C58 C1U16Y
C57 X_C220P16X0402
V_FSB_VTT R58 115R1%0402-RH CPU_GTLREF3_R R65 10R0402
CPU_GTLREF3
DESIGN NOTE:
Reserve for Future CPU use;
Product may tie GTLREFS together
R62 200R1%0402
C48 C1U16Y
C53 X_C220P16X0402
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS
V_FSB_VTT
L7
X_10U100m_0805
CP3
X_COPPER
C133 C1U16Y
C122 X_C10U10Y0805
C127 C10U10Y0805
H_VCCA
H_VSSA
V_1P5_CORE
CP4
X_COPPER
H_VCCPLL
C134 X_C10U10Y0805
C125 X_C0.1U16Y0402
PLACE AT CPU END OF ROUTE
VTT_OUT_RIGHT R60 130R1%0402 H_PROCHOT#
R72 62R0402 H_IERR#
H_PROCHOT# 5
H_IERR# 5
VTT_OUT_LEFT R75 62R0402 H_CPURST#
R88 X_100R0402 H_PWRGD
R103 62R0402 H_BR#0
H_CPURST# 5,8
H_PWRGD 5,12
H_BR#0 5,8
PLACE AT ICH END OF ROUTE
V_FSB_VTT R320 62R0402 TRMTRIP#
R326 62R0402 H_FERR#
TRMTRIP# 5,12
H_FERR# 5,12
VCC5_SB
VTT_OUT_LEFT
R47 1KR0402
R57 680R0402
1.25V VTT_PWRGOOD
VTT_PWG
28,29 VID_GD#
R55 10KR0402
Q4 2N3904S
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
MSI
MICRO-STAR INt'L CO., LTD.
Title
Intel LGA775 CPU - Power
Size
Document Number
MS-7379
Rev
2.0
Date: Thursday, July 12, 2007
Sheet 6 of 34

	2005 Performance FMB platform 1	2005 Mainstream/Value FMB platform 2	2006 65W FMB platform 3
MSID1	0	0	0
MSID0	0	NC	NC



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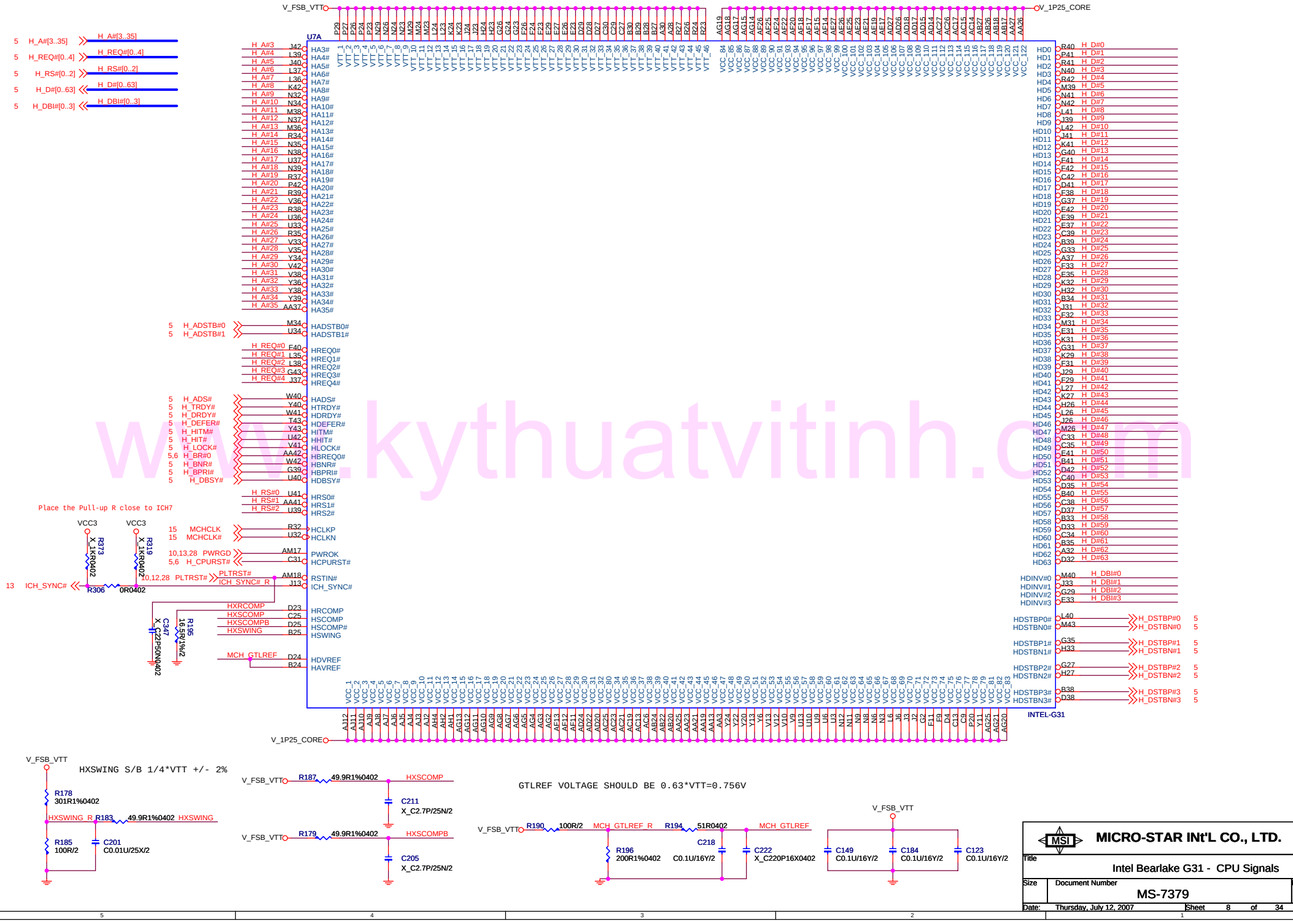
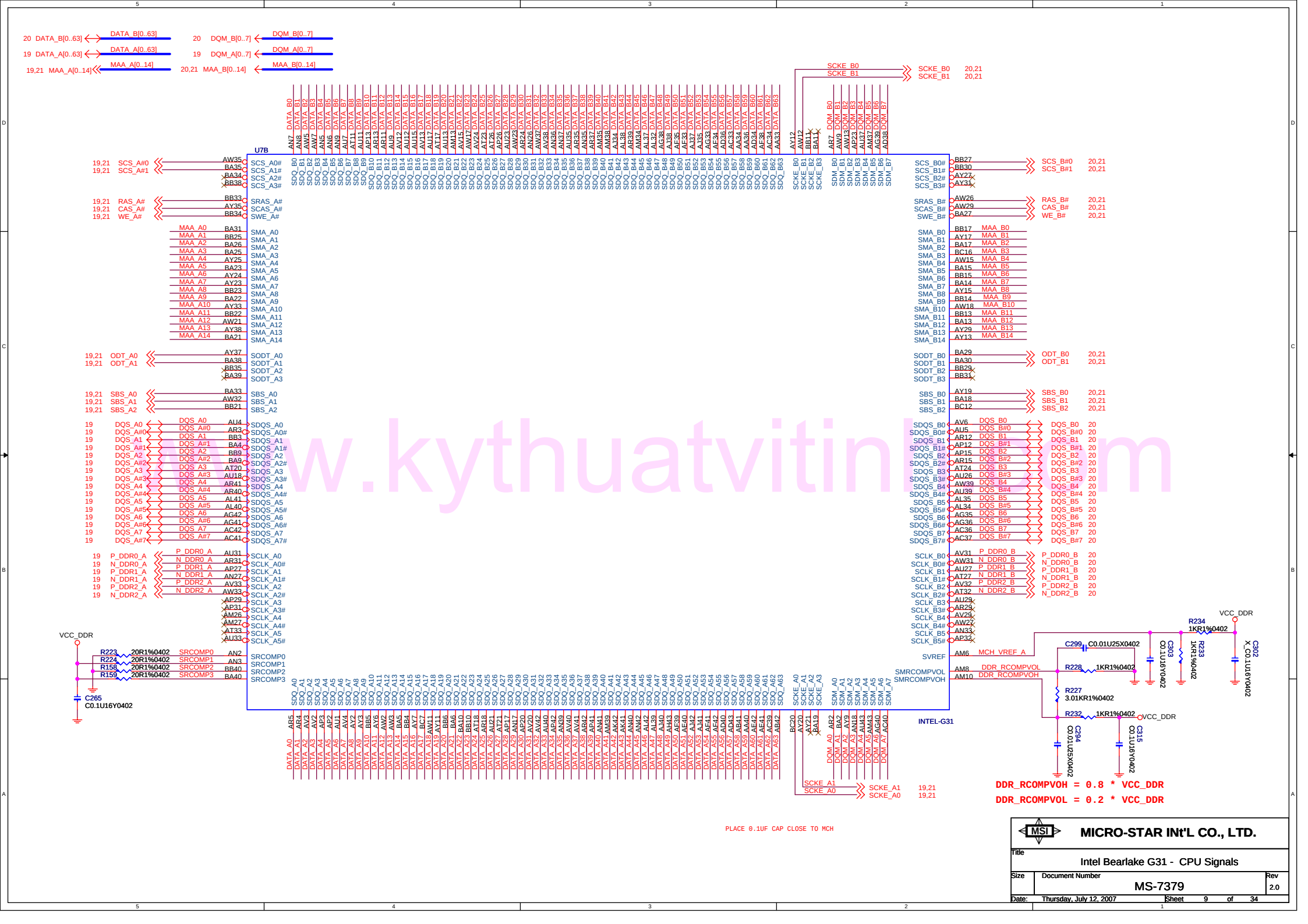
Title	Intel LGA775 CPU - GND	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 7 of 34	





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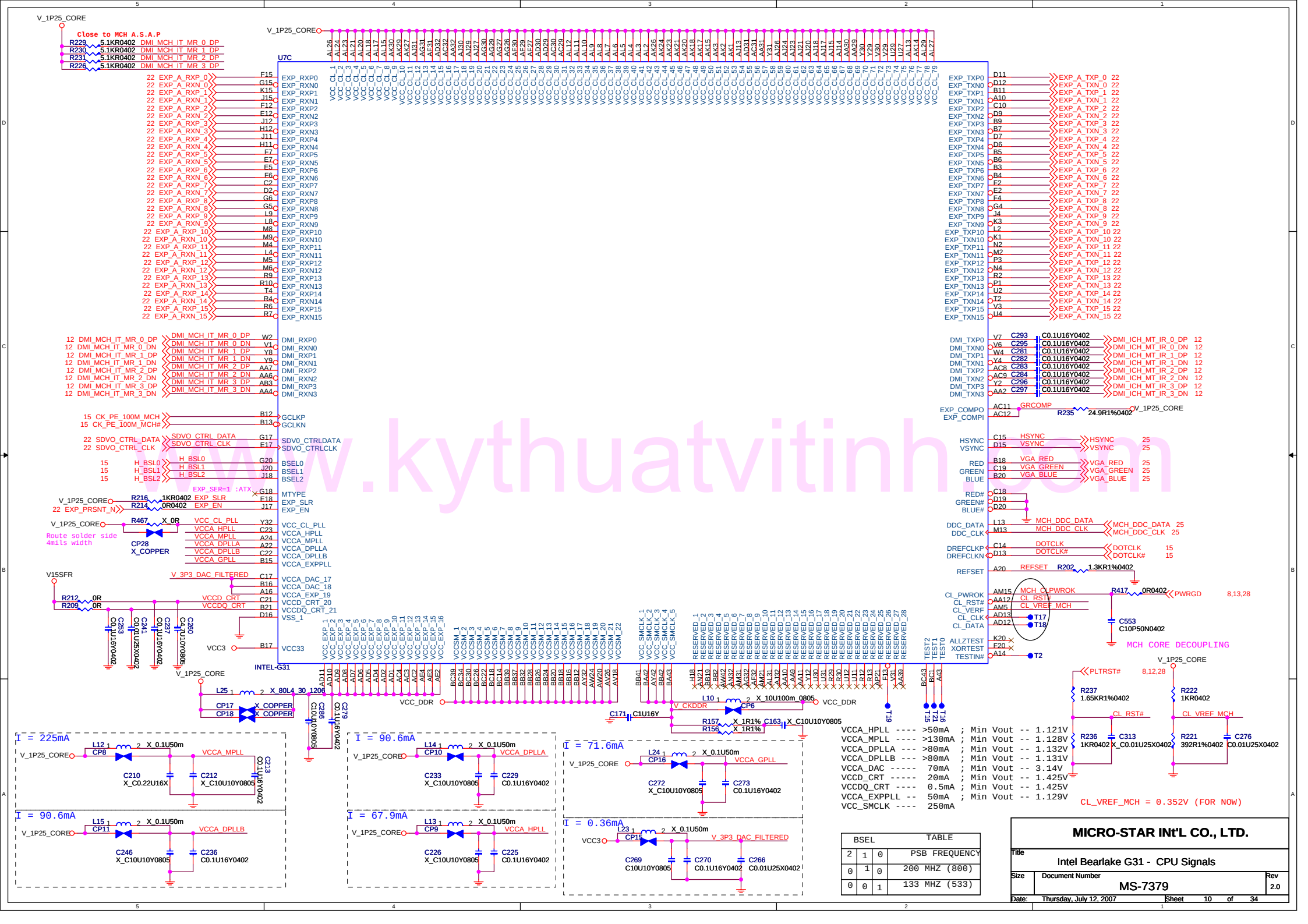
Title	Intel Bearlake G31 - CPU Signals	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 9 of 34	



Place close to GMCH

VCC_DDR

C227 X_C2.2U6.3Y
C198 C2.2U6.3Y
C202 X_C2.2U6.3Y
C261 X_C2.2U6.3Y
C217 C2.2U6.3Y
C242 C2.2U6.3Y

MCH MEMORY DECOUPLING

VCC_DDR

EC26 X_.CD1000U6.3EL11.5-

MCH CORE DECOUPLING

V_1P25_CORE

C285 C10U10Y0805
C298 X_C10U10Y0805
C300 C0.1U16Y0402
C301 X_C10U10Y0805
C318 C0.1U16Y0402
C332 C0.1U16Y0402
C342 X_C10U10Y0805
C312 X_C10U10Y0805
C366 C0.1U16Y0402

5020 Parts

V_1P25_CORE

C586 X_C10U10Y0805
C587 X_C10U10Y0805
C590 X_C10U10Y0805
C591 X_C10U10Y0805
C592 X_C10U10Y0805

V_FSB_VTT

C588 X_C0.1U16X-1
C589 X_C0.1U16X-1

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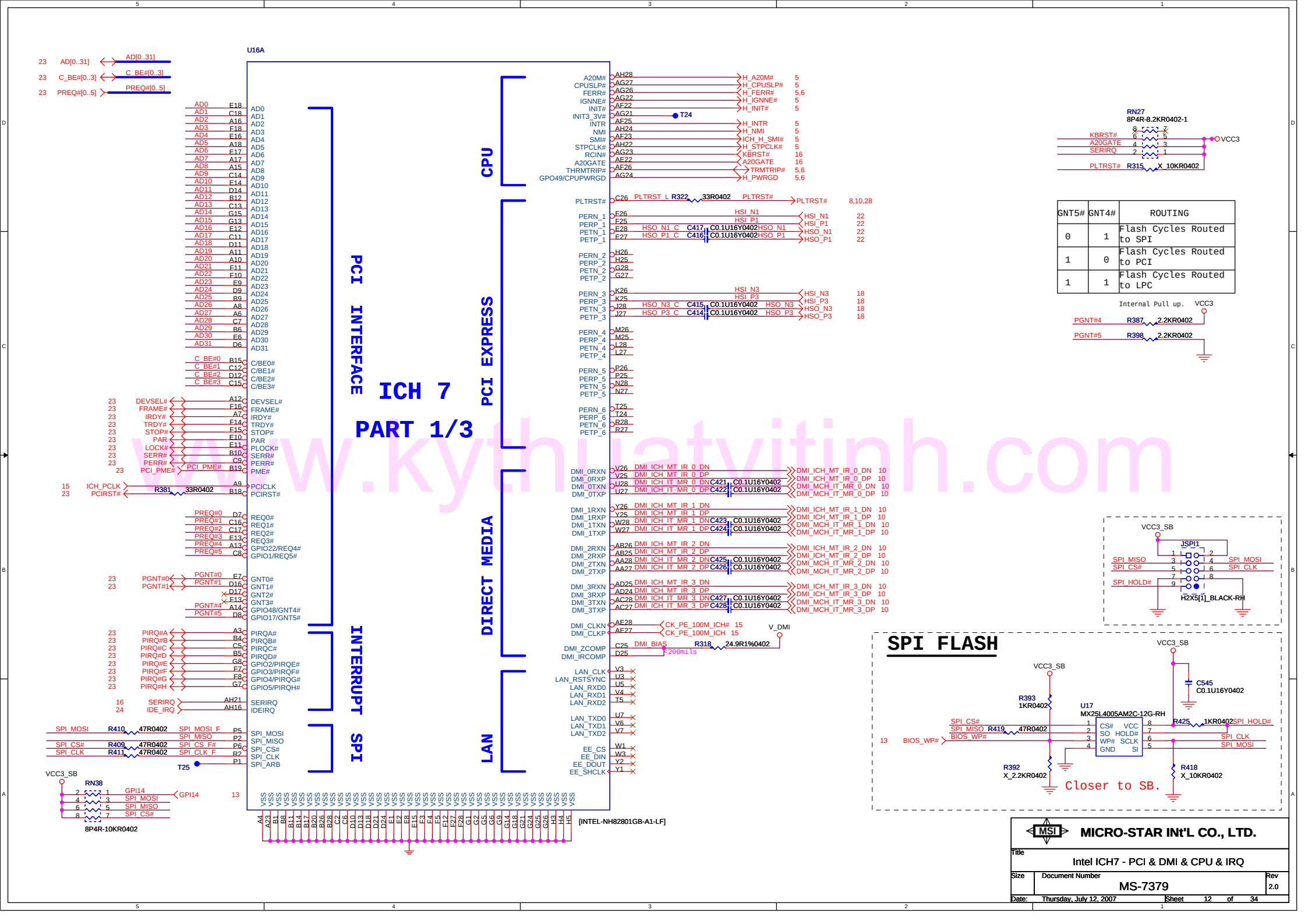
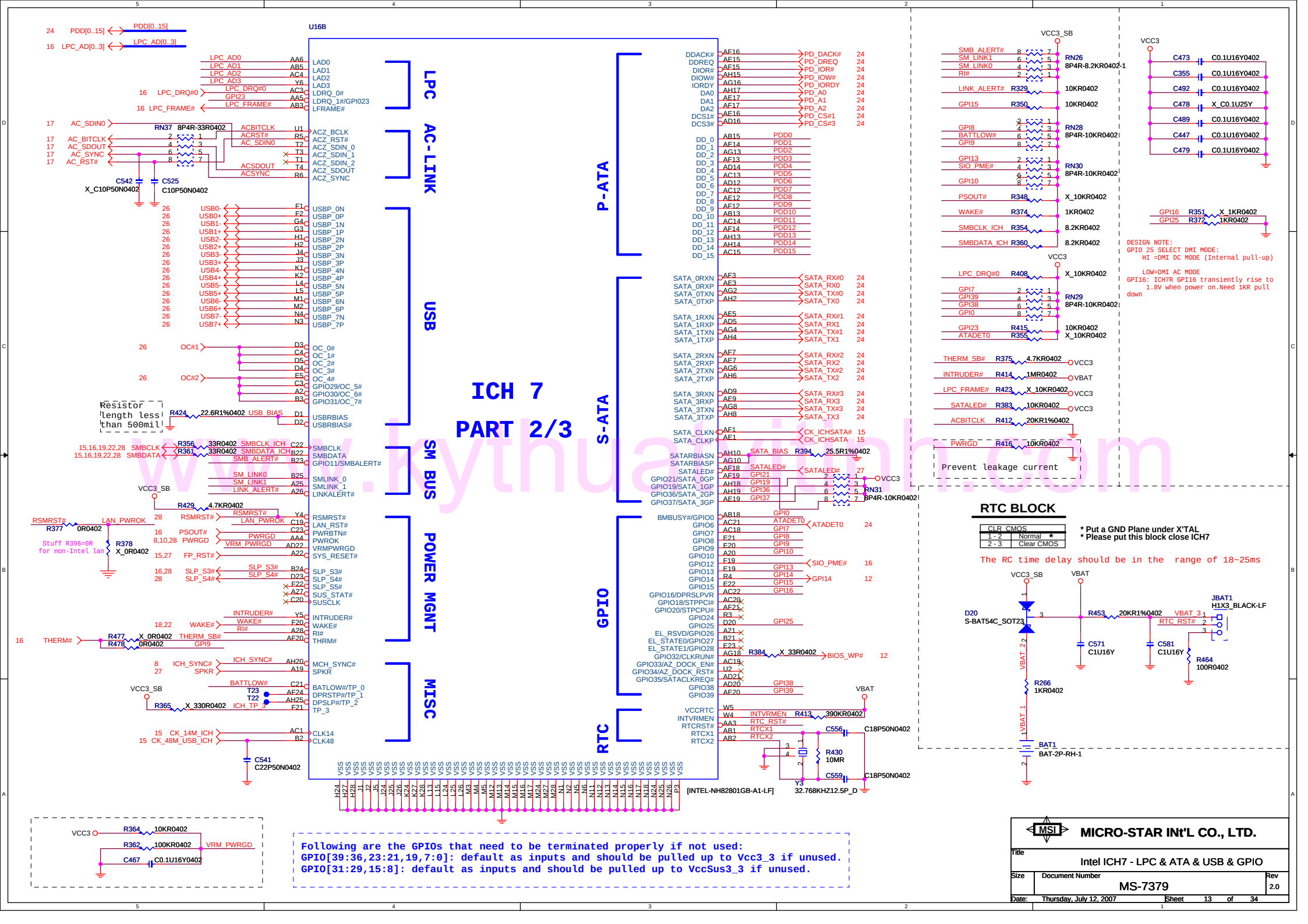
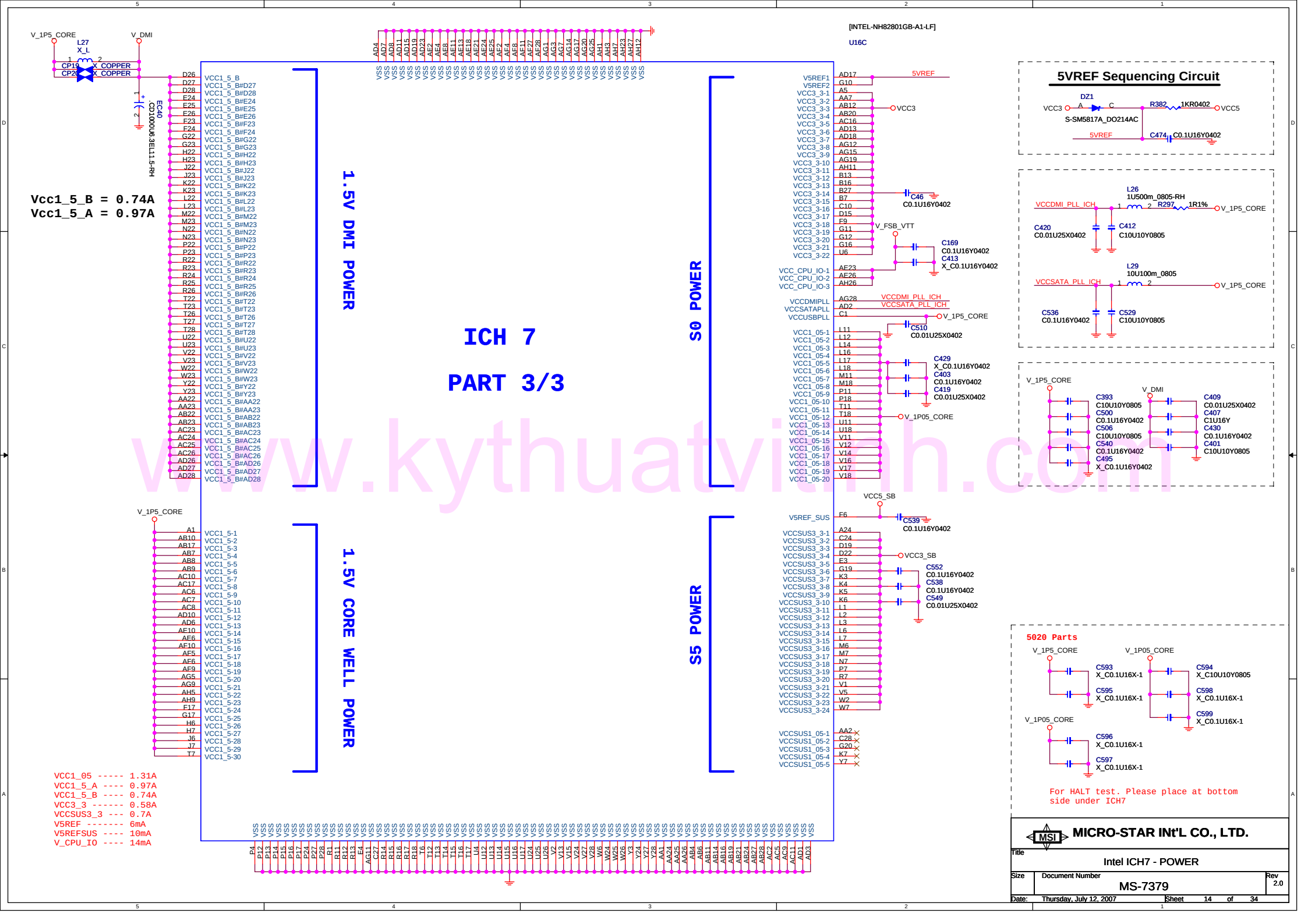
Title	Intel Bearlake G31 - CPU Signals	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 11 of 34	

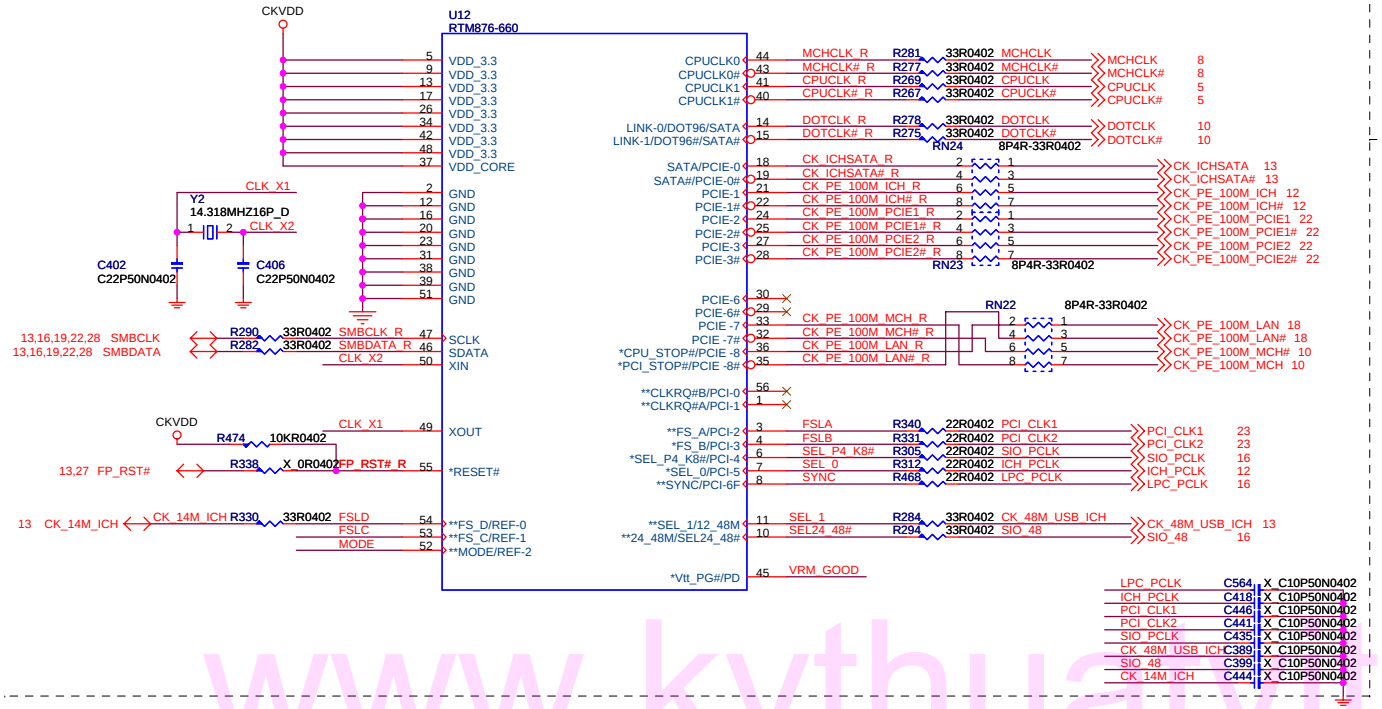


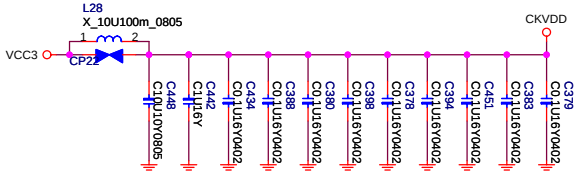
GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC


ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
U16B
RTC BLOCK
CLR_CMOS
1 - 2 Normal *
2 - 3 Clear CMOS
* Put a GND Plane under X'TAL
* Please put this block close ICH7
The RC time delay should be in the range of 18~25ms
Prevent leakage current
Resistor length less than 500mil
Stuff R396=0R for non-Intel lan
DESIGN NOTE:
GPIO 25 SELECT DMI MODE:
HI =DMI DC MODE (Internal pull-up)
LOW=DMI AC MODE
GPI16: ICH7R GPI16 transiently rise to 1.8V when power on.Need 1KR pull down
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
[INTEL-NH82801GB-A1-LF]
MICRO-STAR INt'L CO., LTD.
Intel ICH7 - LPC & ATA & USB & GPIO
MS-7379
2.0
Thursday, July 12, 2007
Sheet 13 of 34

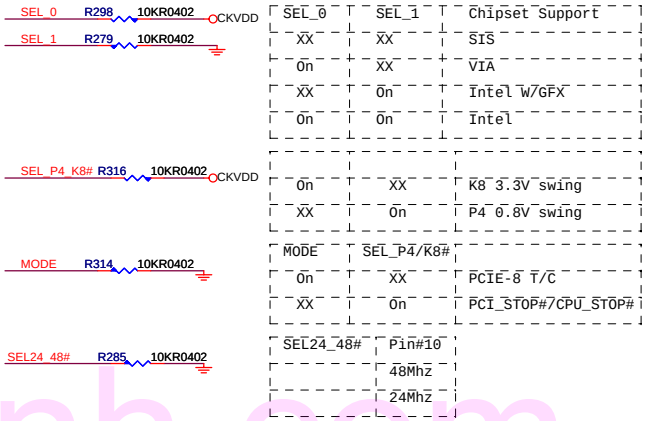


Clock Generator - RTM876-660





STRAPPING RESISTOR



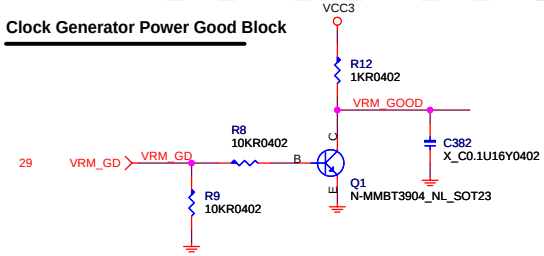
SEL_0	SEL_1	Chipset Support
XX	XX	SIS
On	XX	VIA
XX	On	Intel W/GFX
On	On	Intel

SEL_P4_K8#	MODE	
On	XX	K8 3.3V swing
XX	On	P4 0.8V swing

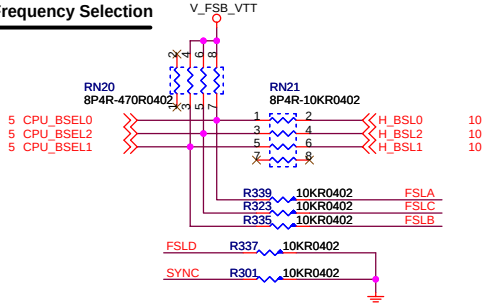
MODE	SEL_P4/K8#	
On	XX	PCIE-8 T/C
XX	On	PCI_STOP#/CPU_STOP#

SEL24_48#	Pin#10
	48Mhz
	24Mhz

Clock Generator Power Good Block



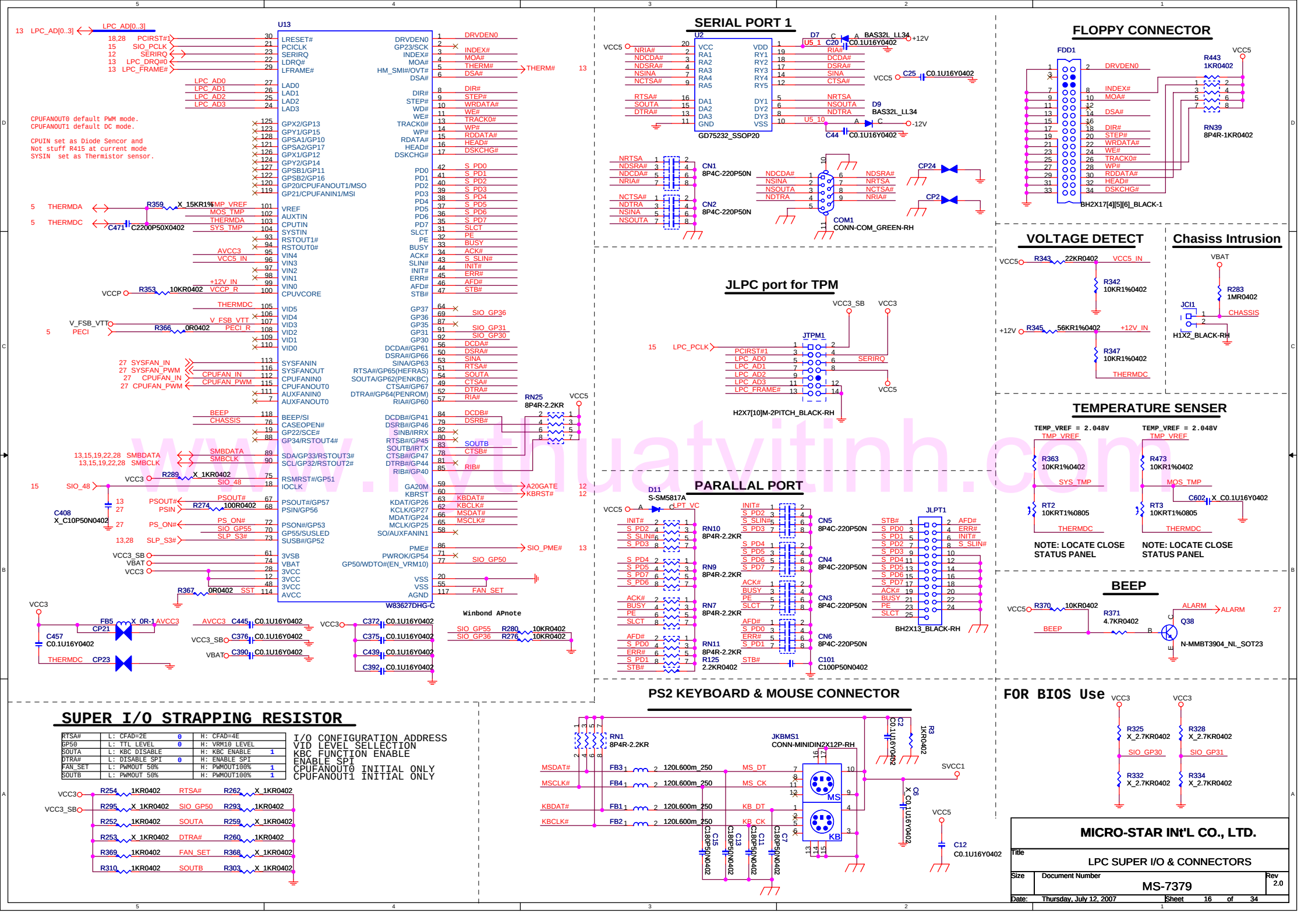
CPU Frequency Selection



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	200M

MICRO-STAR INt'L CO., LTD.

Title	Clock Generator -RTM876-660	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 15 of 34	



ALC888 CODEC

883 :B09-LC88304-R09
888: B09-LC88804-R09
861D:B09-LC86124-R09

Trace Width 20mils.

U18 ALC888/LQFP48

CD/IN HEADERS

CD_IN1 — AUDIO-CDIN1X4

ALC888 JACK

AUDIO1A (Upper) — AUDIO1B (Middle) — AUDIO1C (Down)
AUDIO2A (Upper) — AUDIO2B (Middle) — AUDIO2C (Down)

LINE_IN
SURR
LINE_OUT
CEN/BAS
MIC1
SIDESURR

PN:N54-26F0151-S42

ALC883 JACK DETECT

SPDIF_OUT

JSP1 BH1X3_BLACK-RH

Azalia Front Audio Connector

Place those component close to audio connector.

JAUD1 YJ205-IA

CN7 8P4C-470P50N

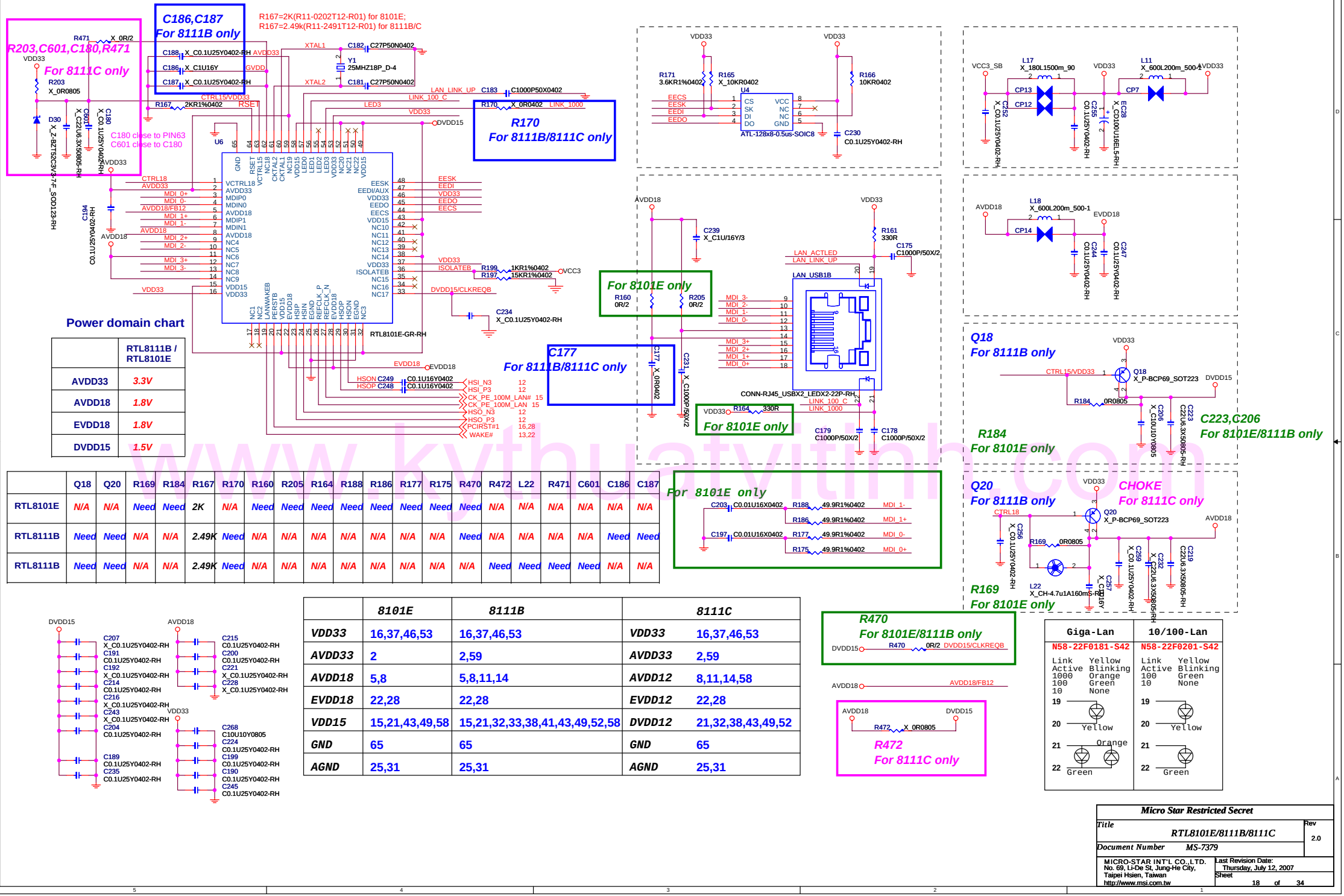
AUDIO CODE REGULATORS

U19 LT1087S_SOT89

Trace Width 30mils.

For EMI

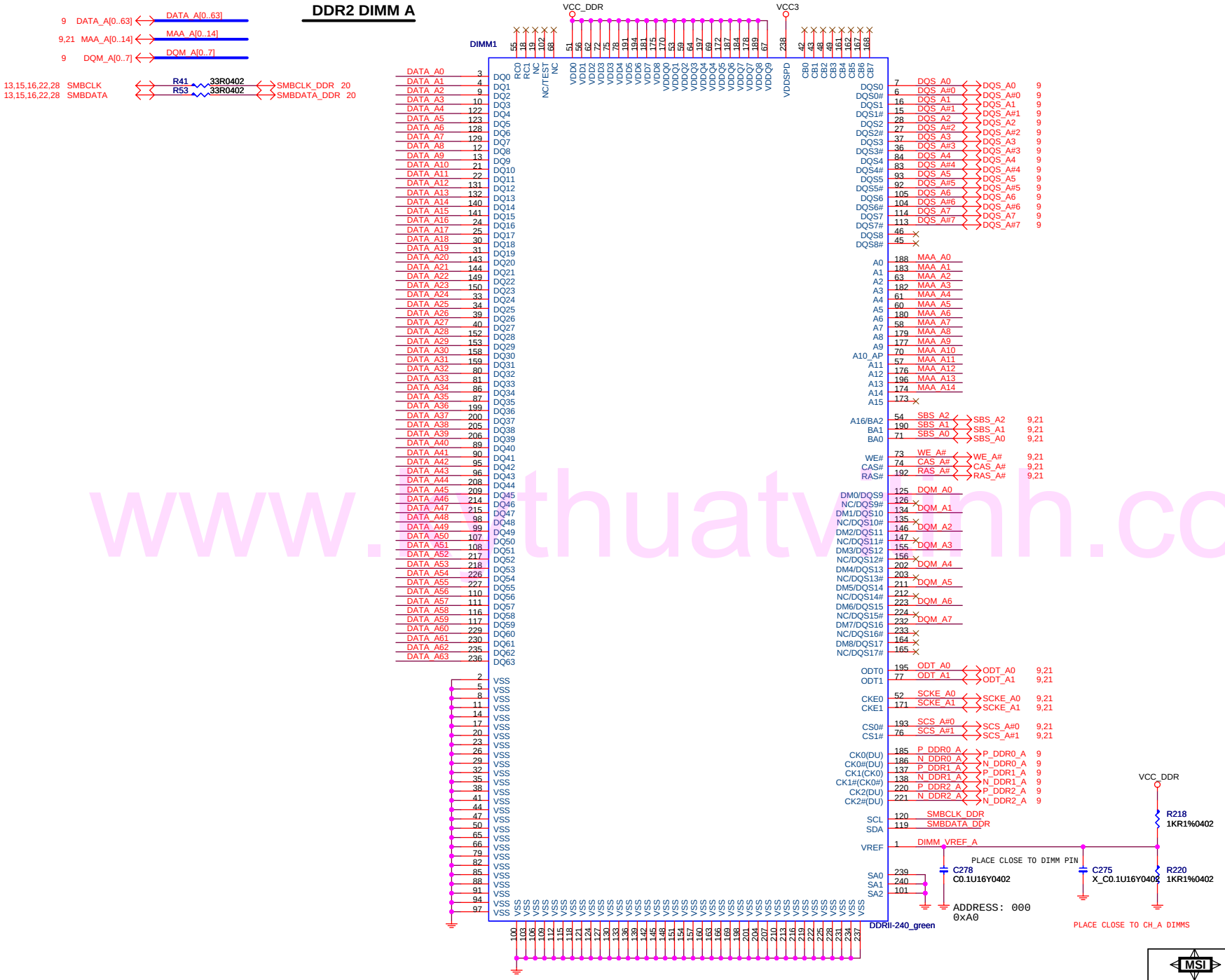
<OrgAddr1>	MICRO-STAR INt'L CO., LTD.
Title	ALC888 CO-LAY ALC883 CODEC
Size	Document Number: MS-7379
Rev	2.0
Date:	Thursday, July 12, 2007
Sheet	17 of 34



	Q18	Q20	R169	R184	R167	R170	R160	R205	R164	R188	R186	R177	R175	R470	R472	L22	R471	C601	C186	C187
RTL8101E	N/A	N/A	Need	Need	2K	N/A	Need	Need	Need	Need	Need	Need	Need	Need	N/A	N/A	N/A	N/A	N/A	N/A
RTL8111B	Need	Need	N/A	N/A	2.49K	Need	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Need	N/A	N/A	N/A	Need	Need	
RTL8111B	Need	Need	N/A	N/A	2.49K	Need	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Need	Need	Need	Need	N/A	N/A

	8101E	8111B	8111C	
VDD33	16,37,46,53	16,37,46,53	VDD33	16,37,46,53
AVDD33	2	2,59	AVDD33	2,59
AVDD18	5,8	5,8,11,14	AVDD12	8,11,14,58
EVDD18	22,28	22,28	EVDD12	22,28
VDD15	15,21,43,49,58	15,21,32,33,38,41,43,49,52,58	DVDD12	21,32,38,43,49,52
GND	65	65	GND	65
AGND	25,31	25,31	AGND	25,31

DDR2 DIMM A



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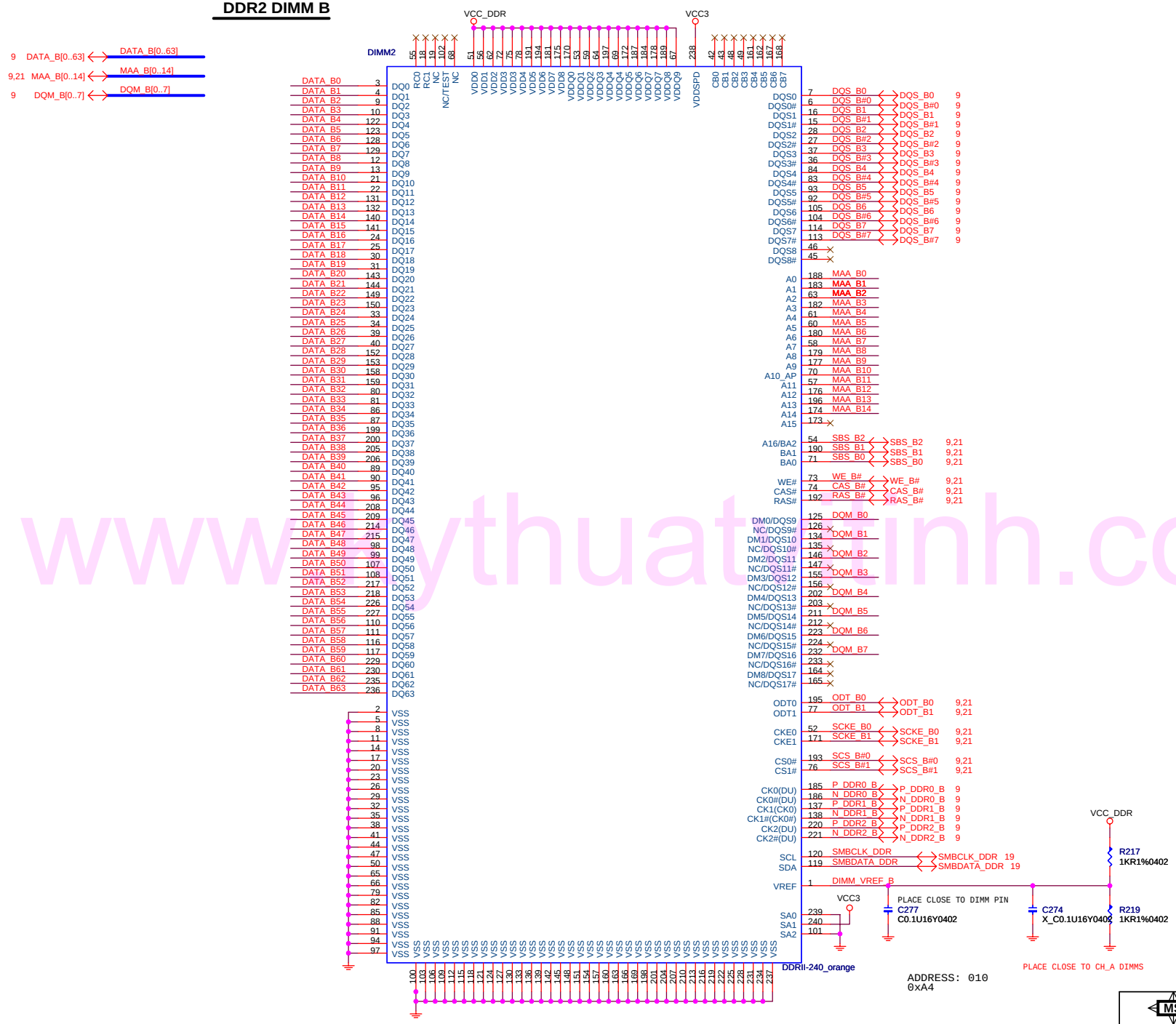
Title	DDR II DIMM A	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 19 of 34	

DDR2 DIMM B



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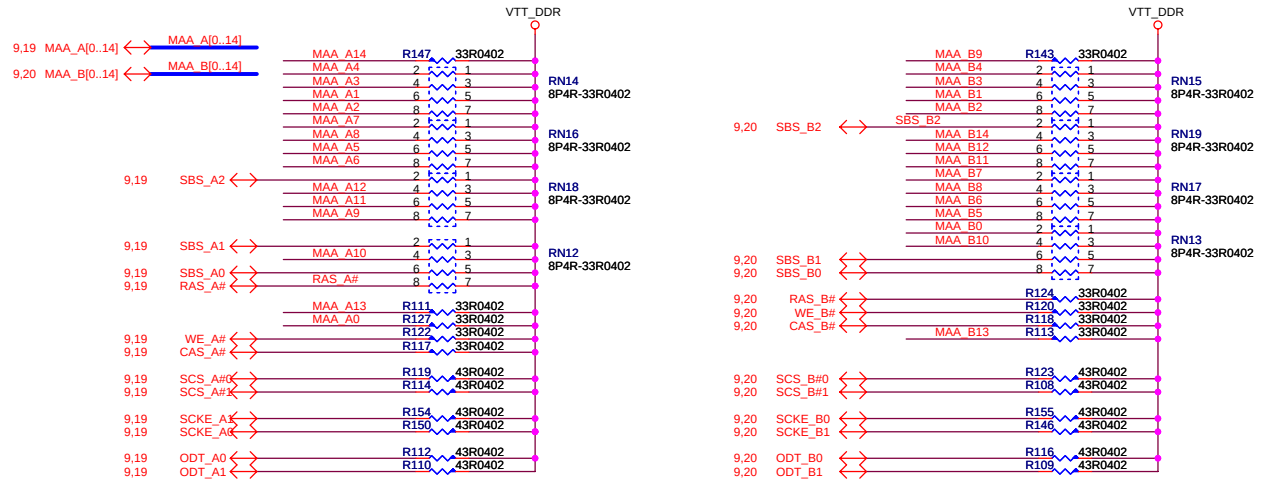
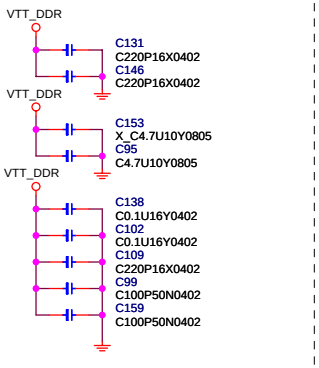
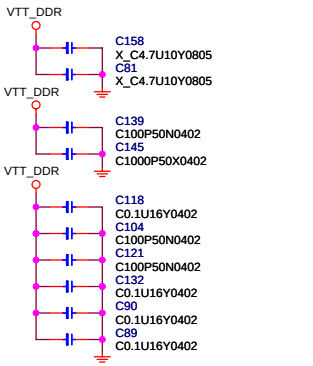
Title	DDR II DIMM A & B	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 20 of 34	

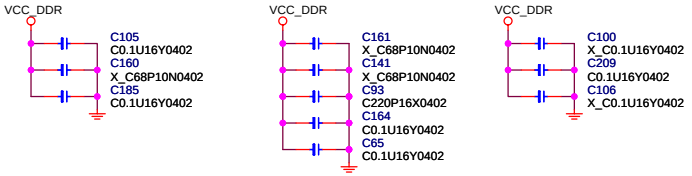


CHANNEL A V_SM_VTT DECOUPLING CAPS

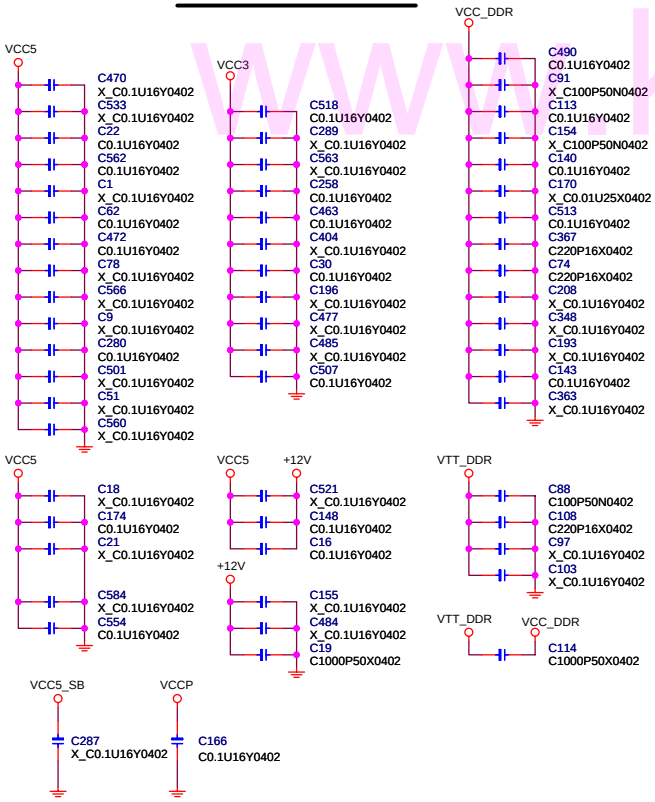


CHANNEL B V_SM_VTT DECOUPLING CAPS

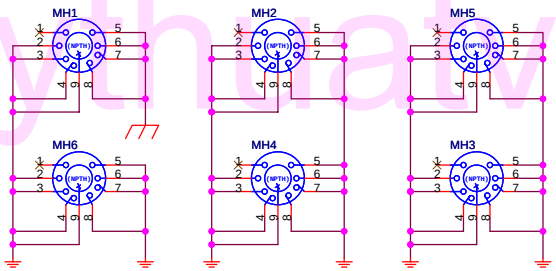




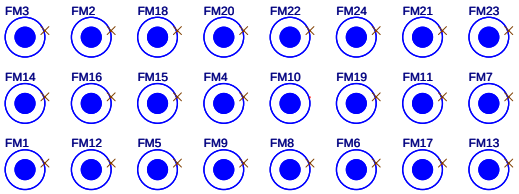
FOR EMI RESERVED



Mounting Holes

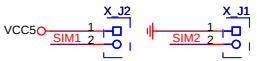


Optics Orientation Holes



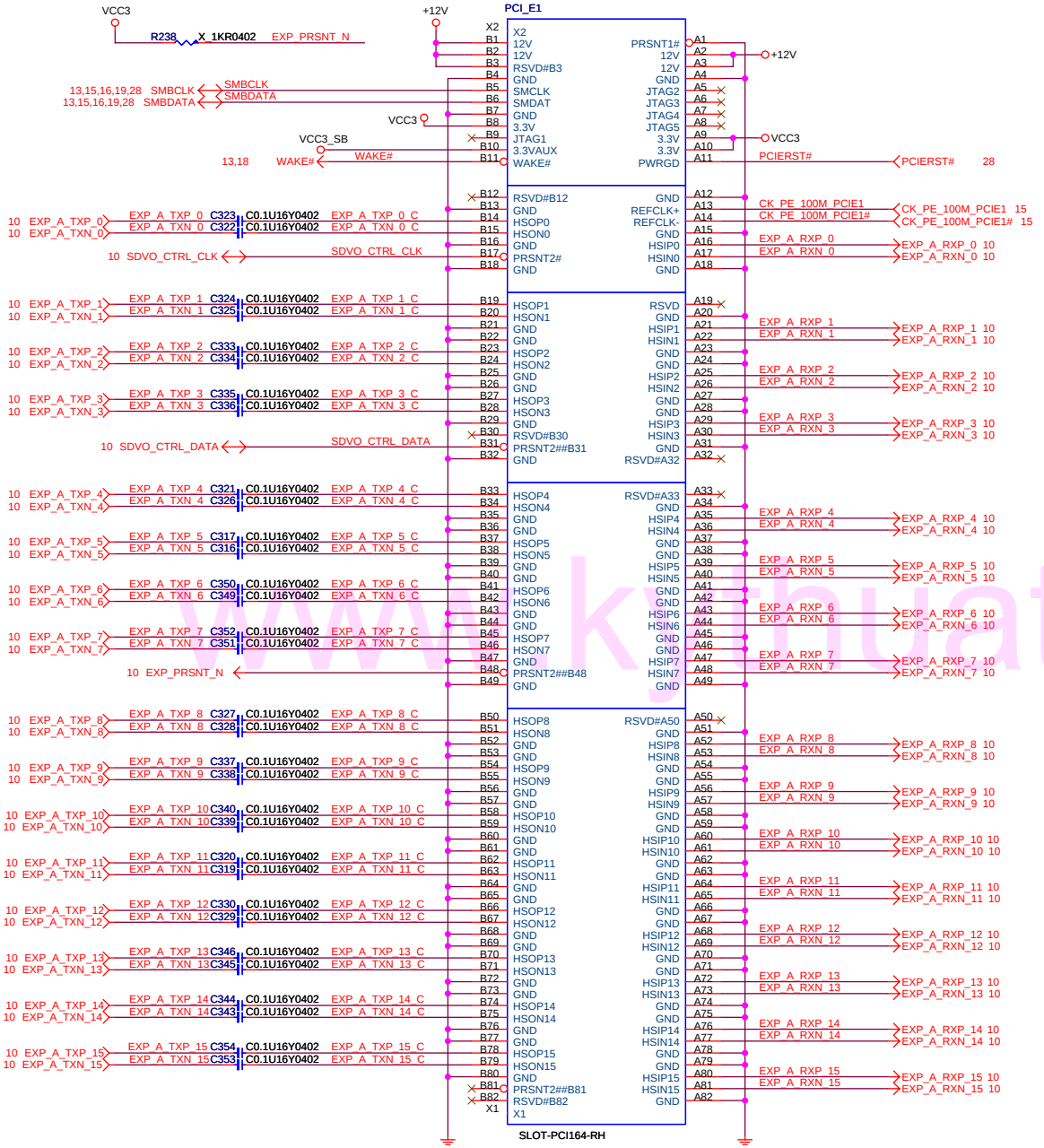
Impedence Calculator

Routing 4:4 for 50ohm +-15% impedence on 1080 stack-up

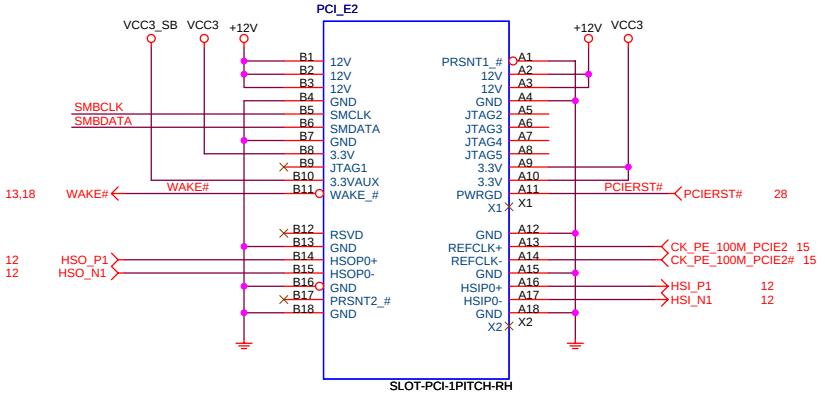


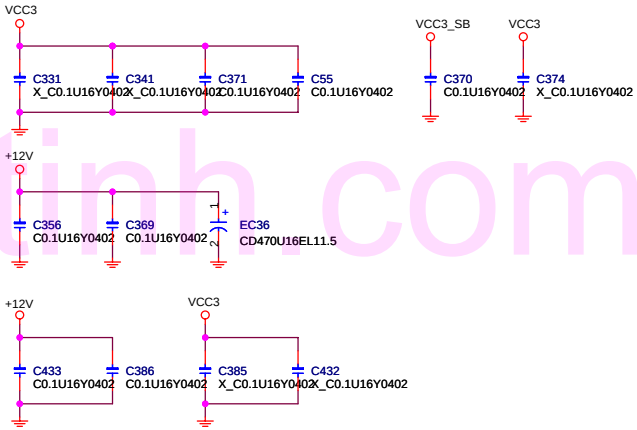
<OrgAddr1>	MSI MICRO-STAR INt'L CO., LTD.	
Title	DDR II VTT DECOUPLING	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 21 of 34	

PCI EXPRESSX16 PORT



PCI EXPRESSX1 PORT

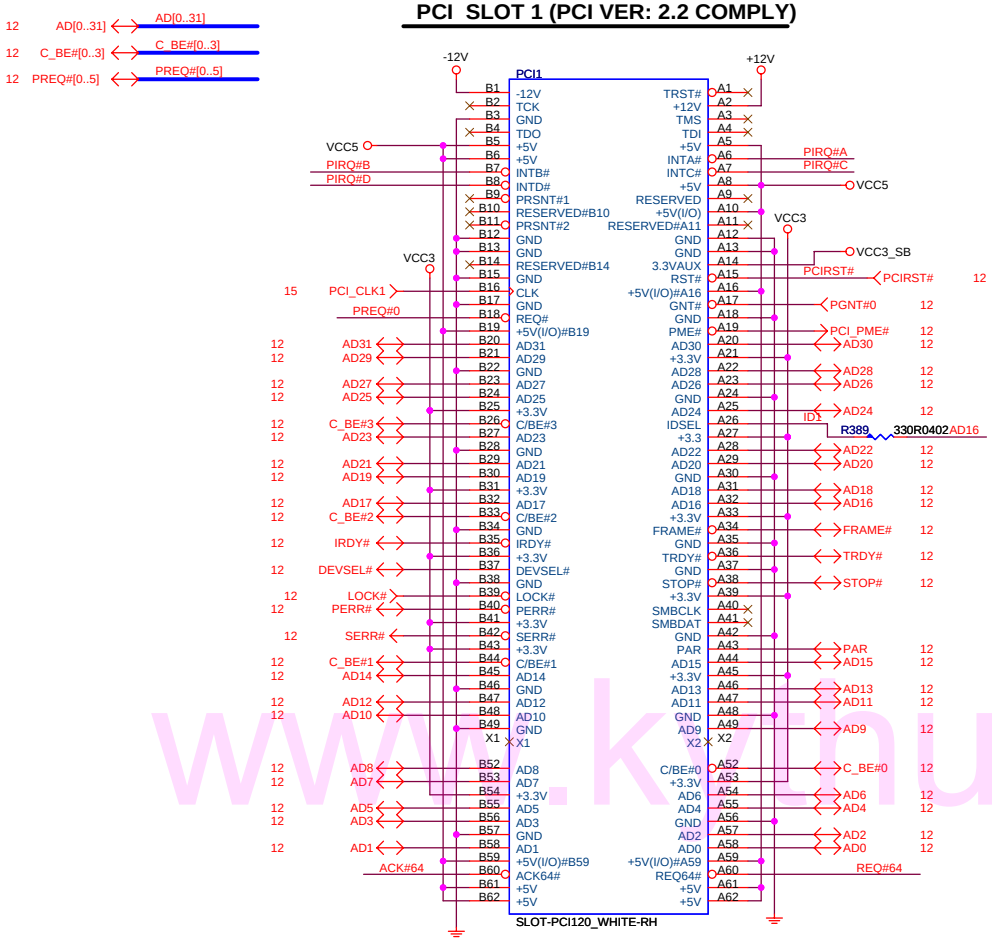




MSI MICRO-STAR INt'L CO., LTD.

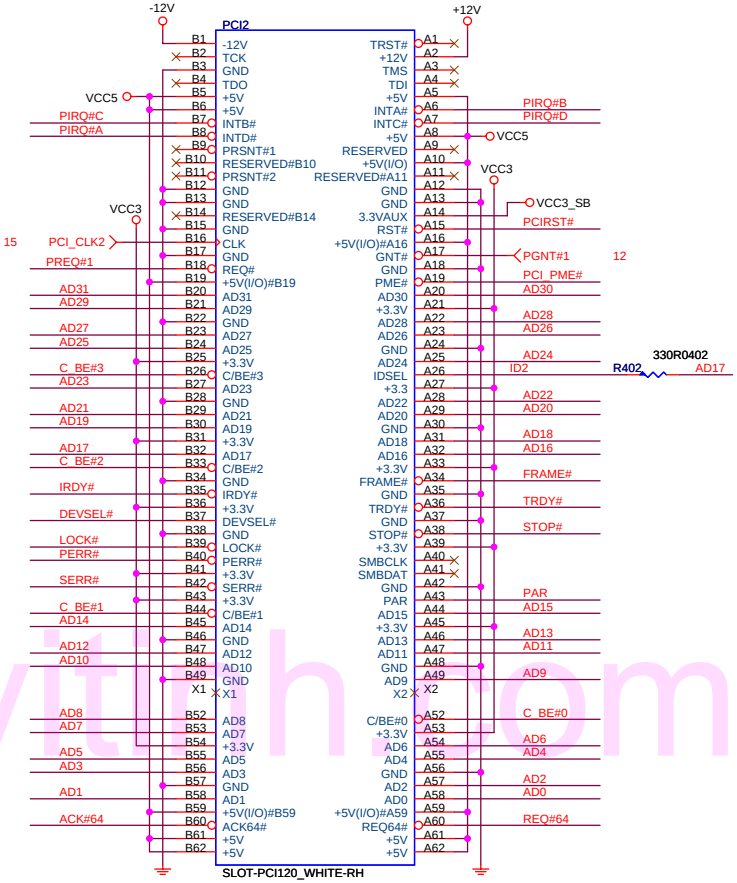
Title	PCI EXPRESS X16 & X1 PORT	
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 22 of 34	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



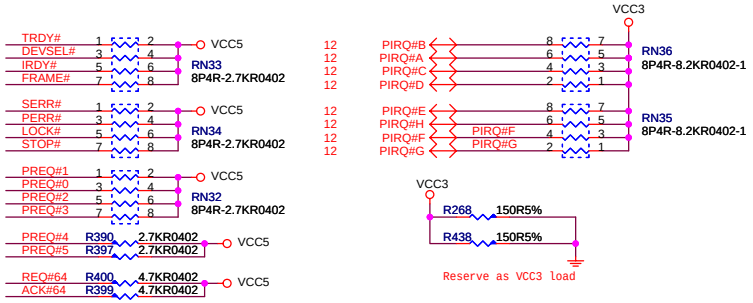
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

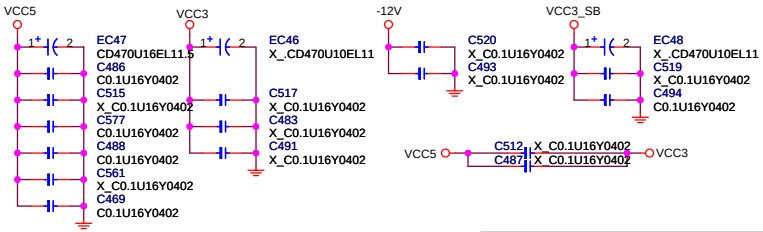


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



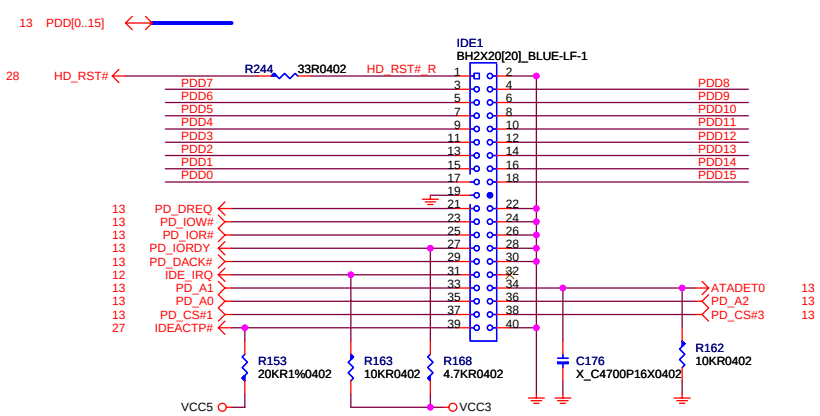
PCI SLOT DECOUPLING CAPACITORS



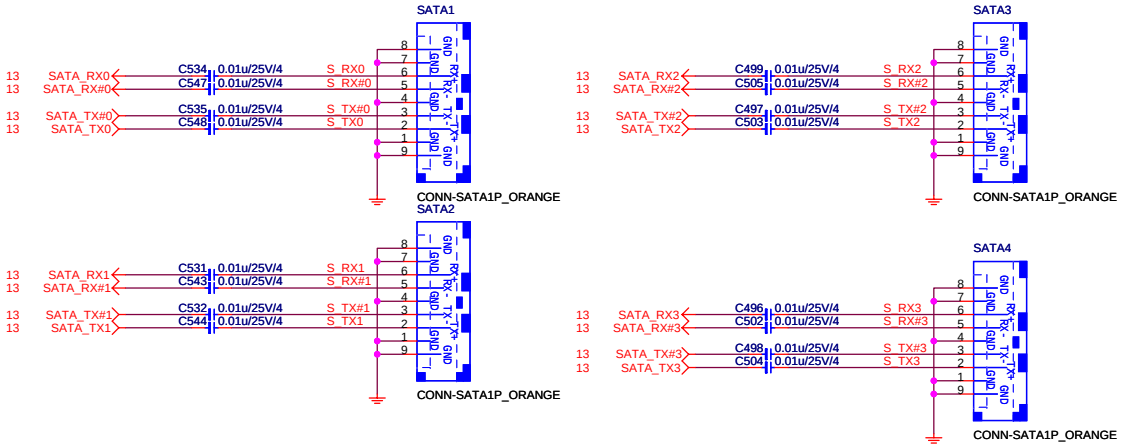
MSI **MICRO-STAR INt'L CO., LTD.**

Title	PCI 1~ 2 Slots	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 23 of 34	

ATA 33/66/100 IDE Connectors



SERIAL ATA CONNECTOR BLOCK



MICRO-STAR INt'L CO., LTD.

Title: ATA33/66/100 IDE & SATA Connectors

Size | Document Number: MS-7379 | Rev: 2.0

Date: Thursday, July 12, 2007 | Sheet 24 of 34

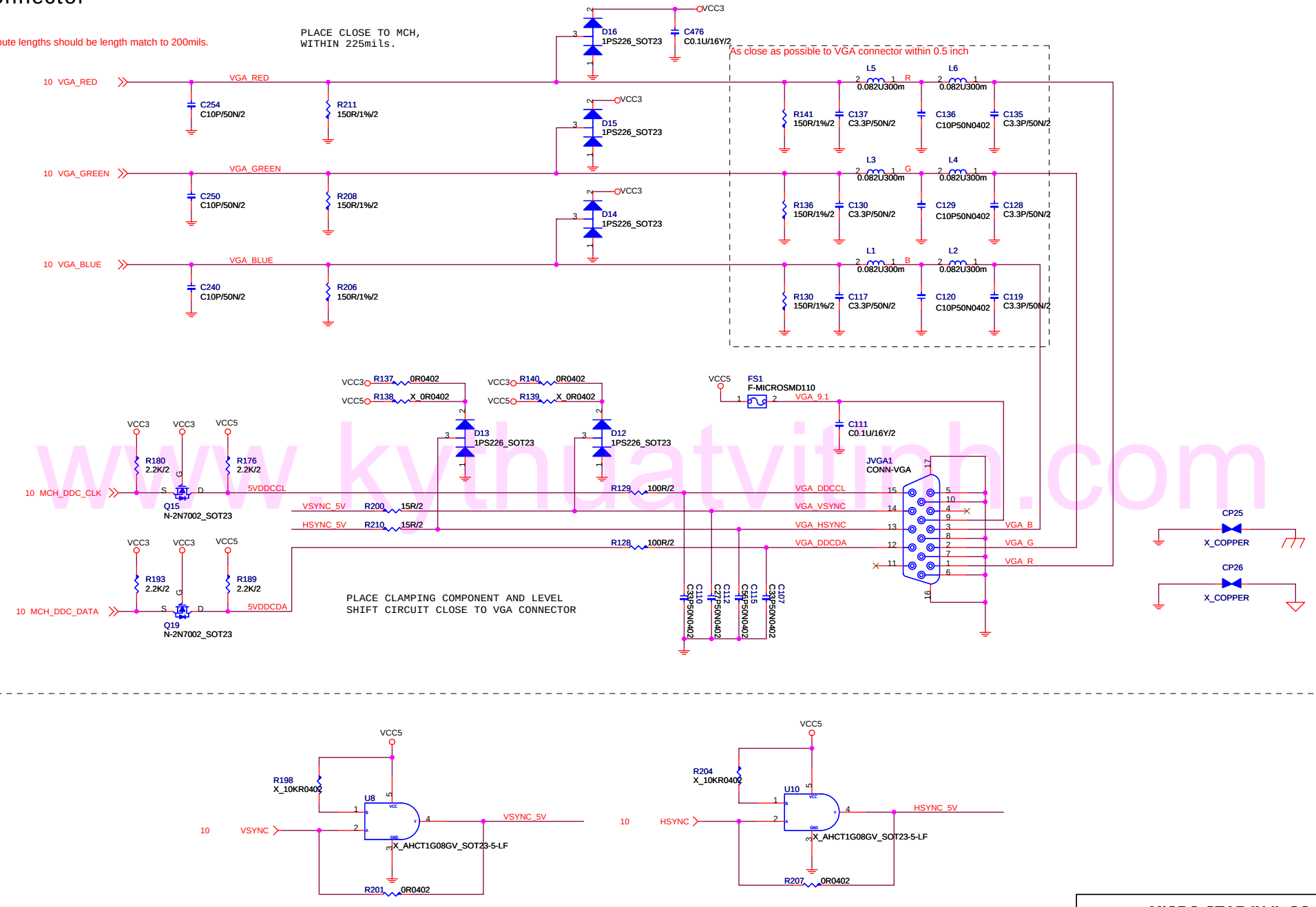
Video Connector

PLACE CLOSE TO VGA CONNECTOR

Thw R ,G ,B route lengths should be length match to 200mils.

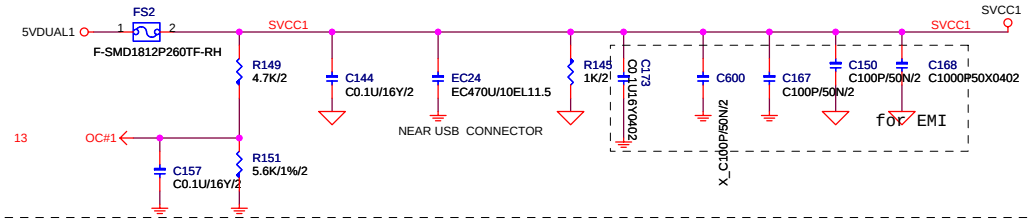
PLACE CLOSE TO MCH, WITHIN 225mils.

As close as possible to VGA connector within 0.5 inch

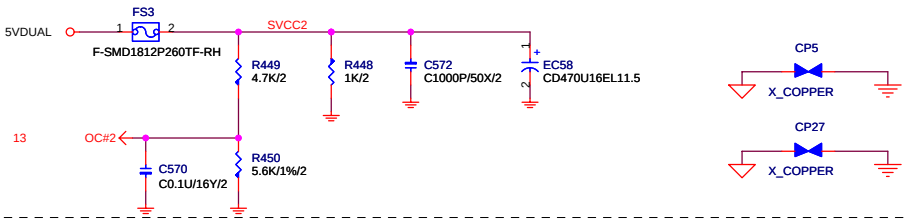


<OrgAddr1>	MICRO-STAR INt'L CO., LTD.
Title	VGA connector
Size	Document Number: MS-7379
Rev	2.0
Date:	Thursday, July 12, 2007
Sheet	25 of 34

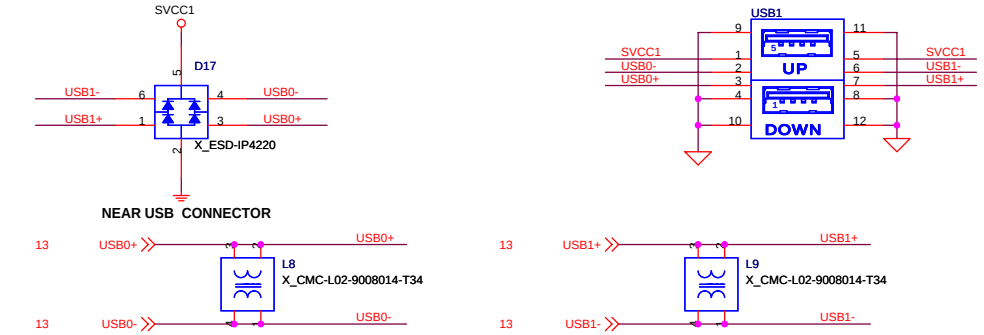
POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



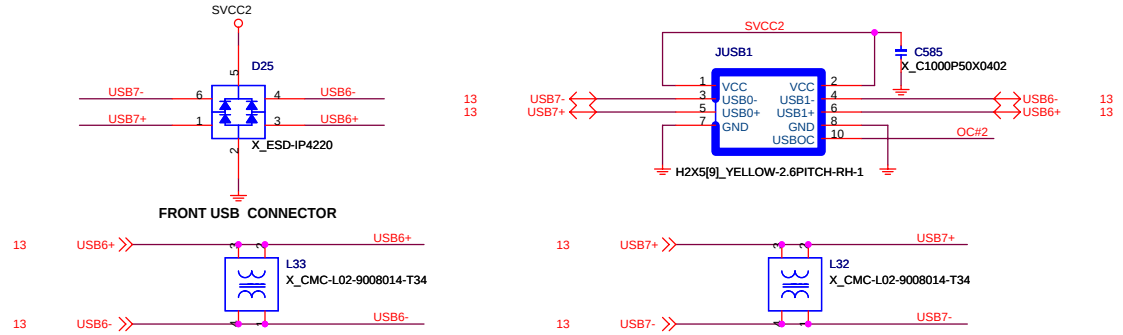
POWER CIRCUIT FOR USB PORT (FRONT)



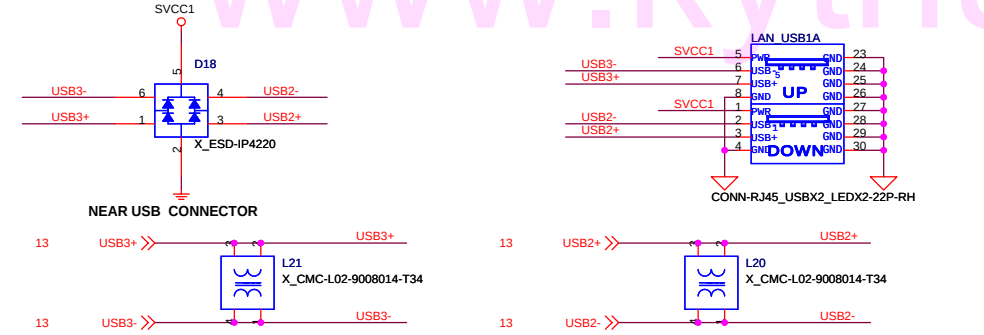
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



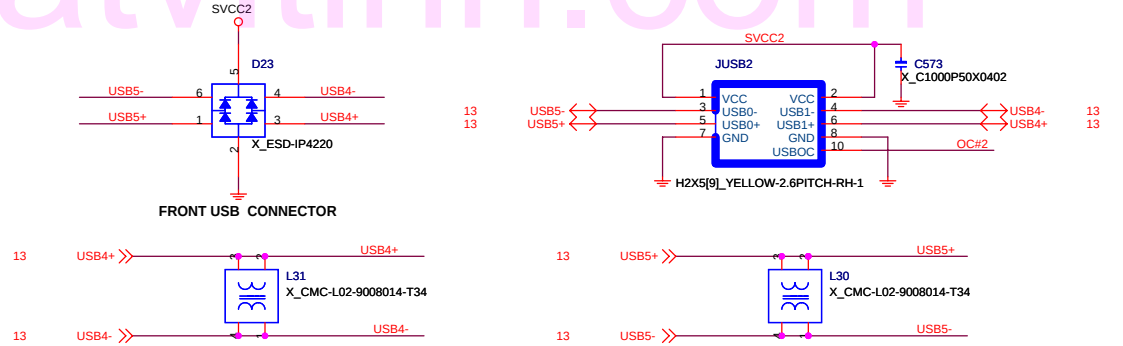
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



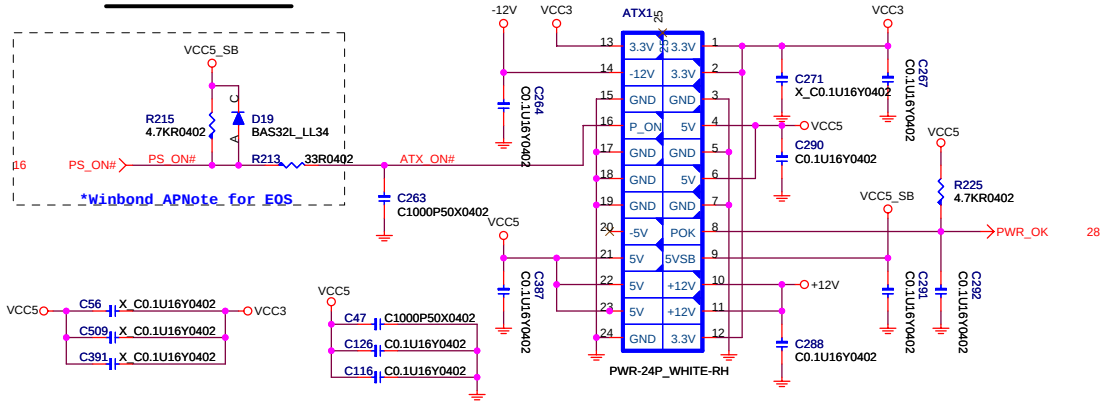
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



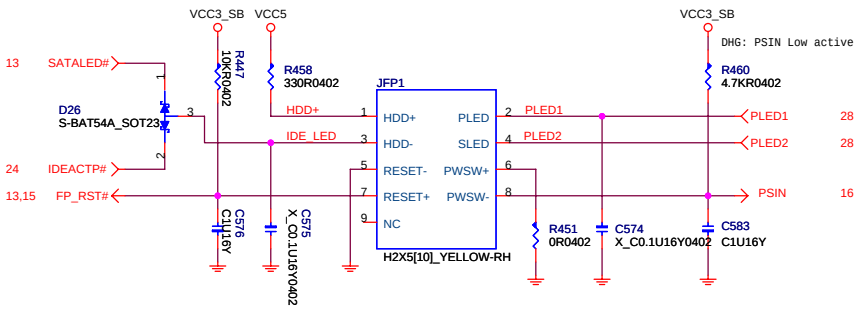
MSI MICRO-STAR INt'L CO., LTD.

Title	USB Connectors	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 26 of 34	

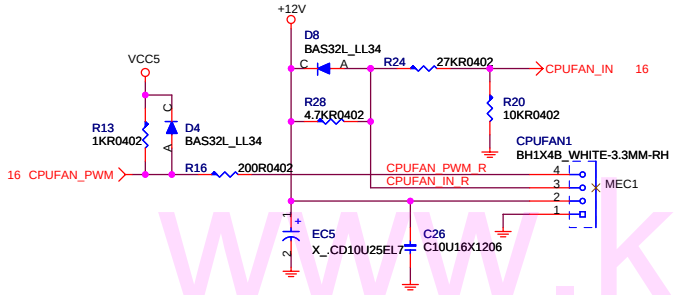
ATX Connector



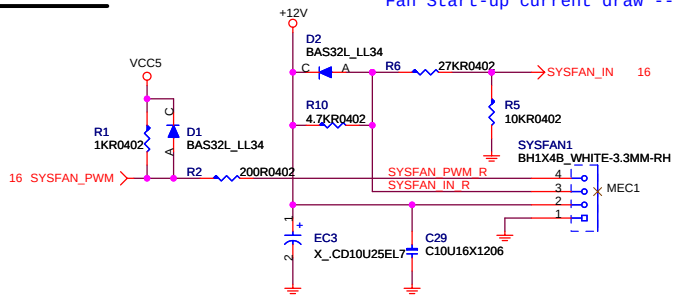
INTEL/PB Front Panel Connector



CPU FAN

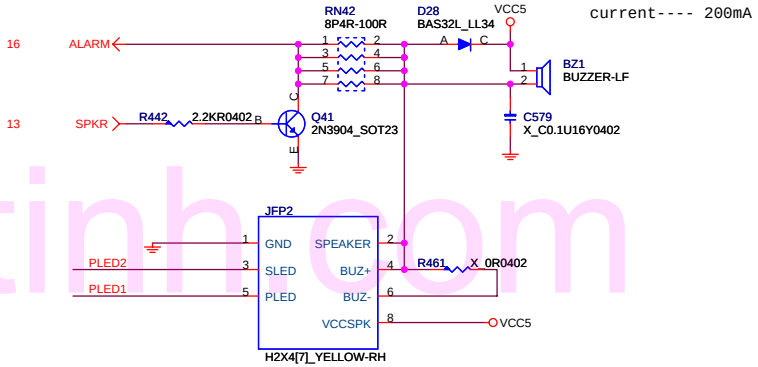


SYSTEM FAN



Peak FAN current draw ------ 1.5A
Average FAN current draw --- 1.1A
Fan Start-up current draw -- 2.2A

MSI Front Panel Connector



MICRO-STAR INt'L CO., LTD.

Title	ATX Connector & Front Panel	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 27 of 34	

ACPI Controller

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

DDR AND DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

5V DUAL Power

V_1P25_CORE 18.1A+2.47A+2.94A

V_1P5_CORE 4.2A + 23.5A +2A

V_1P05_CORE 2A

V_FSB_VTT 6.2A

VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

5VDIMM 12A

VCC_DDR 1.8V 29.7A + 3.2A+5A

DDR VTT Power 1.2A

CHARGE PUMP VOLTAGE OUTPUT

if use Q44, R243=300R, R253=2.1KR

Close to MS11

CLOSE TO DEVICE FB

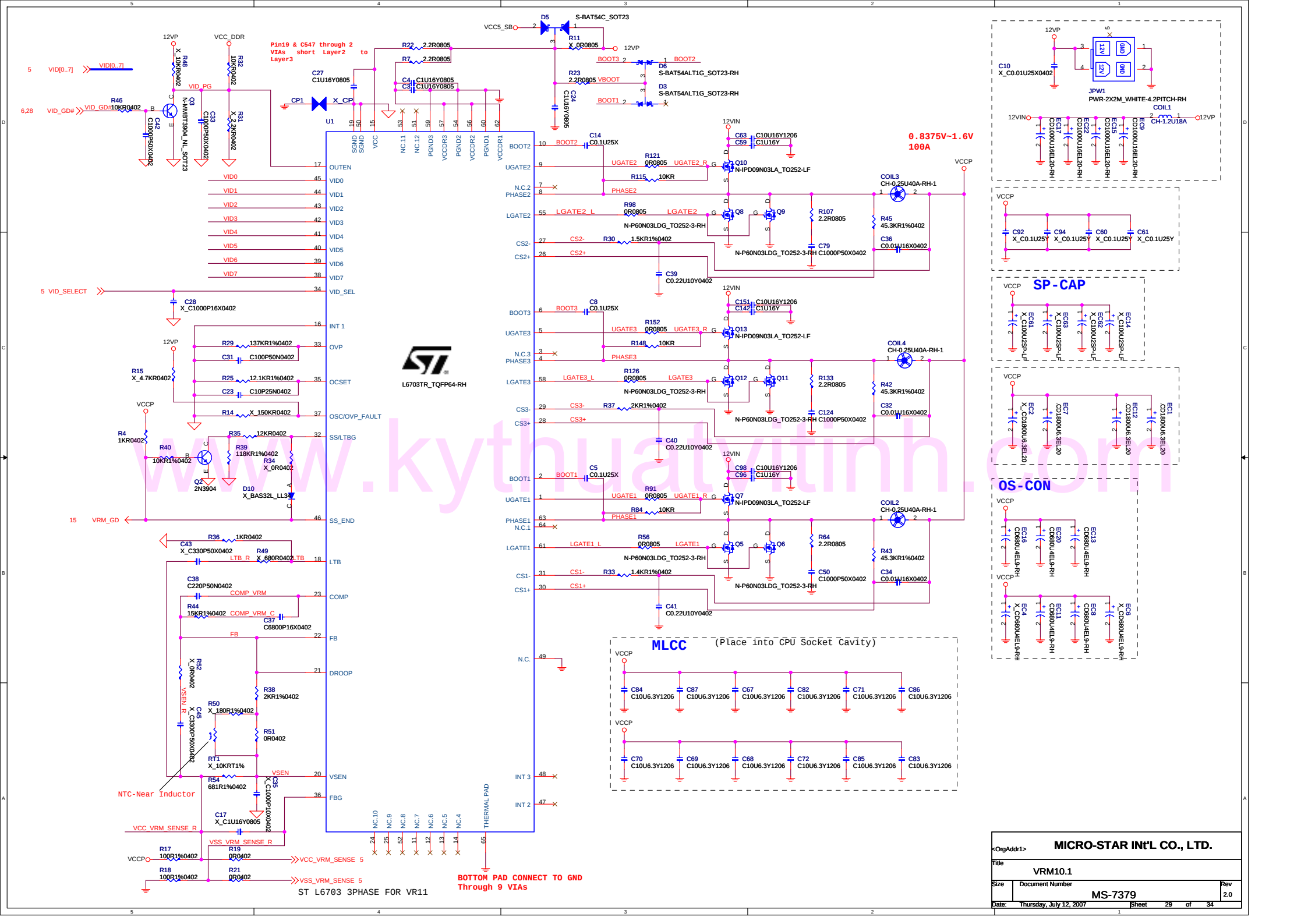
CLOSE TO CHOKE OUTPUT

Place snubber R304,C331 near Drain&Source of FET

Vo = Vref (1+R2/R1) + IadjxR2
where Vref=1.25V, Iadj=55uA

Q16 USE LOW-Rds(on) MOSFET
AVL: D03-0903BDB-N03
D03-09N030B-I14
D03-78N030B-P03

MICRO-STAR INt'L CO., LTD.	
Title	ACPI CONTROLLER MS7 & MS11
Size	Document Number: MS-7379
Rev	2.0
Date:	Thursday, July 12, 2007
Sheet	28 of 34



1.P18- C186 change to C0603
2.P23- ADD R438 R268 200Ohm
3.P26-change OC# circuits
4.P18-add 8111C circuits
5.P16-add MOS TEMPERATURE SENSER circuits
6.P28-add c603
7.P16-add c602
8.P15-add R474
9.P25-change C136,C129,C120=10PF,R200,R210=15Ohm.
  C115=56P,C112=27P
10.P13-change R424=18Ohm
11.P13-change R394=25.5Ohm
12.P16-change VCC_KM to VCC5_SB

MICRO-STAR INt'L CO., LTD.		
Title: History		
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 30 of 34	

Auto-BOM Manual Parts

PCB1

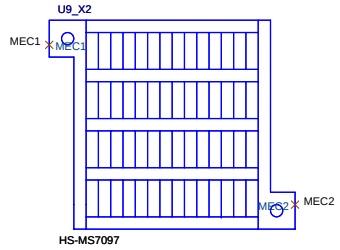
PCB

CON2_1

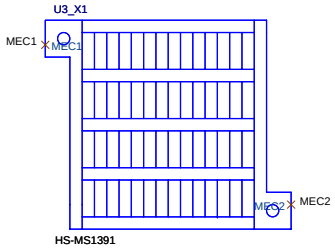
B_BAT1

BAT-BCR2032P-RH

G31 HEATSINK



ICH7 HEATSINK



@MaCH 060113

A10: 946GZ+RTL8110SC/8100C+VGA+ALC883
A20: 946PL+INTEL 82562V+PCI_EX16+ALC883

MSI <Organization>

MICRO-STAR INt'L CO., LTD.

Title: AutoBOM		
Size	Document Number: MS-7379	Rev: 2.0
Date: Thursday, July 12, 2007	Sheet 31 of 34	

ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	PIRQ#E
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	PIRQ#F
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	PIRQ#G
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	PIRQ#H
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	SMB_ALERT#
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	0	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	N/A	PGNT#5
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	1	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	1	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	PREQ#4
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC (NO CHANGE)
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	1	HW PULL LOW
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	0	NC
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	0	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	0	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	OC#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	1	BIOS_WP#
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	1	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	0	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	1	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	PGNT#4
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO W83627EHF

GPIO	Alt Func	PIN	USAGE	Input/Output	NOTES
GP24	MDAT	66	MSDAT#	I/OD16ts	PS2 Mouse Data.
GP25	MCLK	65	MSCLK#	I/OD16ts	PS2 Mouse Clock.
GP26	KDAT	63	KBDAT#	I/OD16ts	Keyboard Data.
GP27	KCLK	62	KBCLK#	I/OD16ts	Keyboard Clock.
GP32	SCL/RSTOUT2#	90	SMBCLK_ISO	INts	Serial Bus clock.
GP33	SDA/RSTOUT3#	89	SMBDATA_ISO	I/OD12ts	Serial bus bi-directional Data.
GP35	Unmultiplexed	87	UNUSED		
GP36	Unmultiplexed	69	UNUSED		
GP37	Unmultiplexed	64	UNUSED		
GP54	PWROK	71	UNUSED		
GP40	RIB#	85	RIB#	INt	Ring Indicator.
GP41	DCDB#	84	DCDB#	INt	Data Carrier Detect.
GP42	IRTX/SOUTB	83	IRTX(SOUTB)	OUT8	IR Transmitter output./UART B Serial Output.
GP43	IRRX/SINB	82	IRRX(SINB)	INt	Serial Input./IR Receiver input.

SIO W83627EHF(CONTINUE)

GPIO	Alt Func	PIN	USAGE	Input/Output	NOTES
GP44	DTRB#	81	DTRB#	OUT8	UART B Data Terminal Ready.
GP45	RTSB#	80	RTSB#	OUT8	UART B Request To Send.
GP46	DSRB#	79	DSRB#	INt	Data Set Ready.
GP47	CTSB#	78	CTSB#	INt	Clear To Send.
GP50	EN_VRM10/WDTO#	77	STRAPPED DOWN	INcd	defined as VID transition voltage level
GP51	RSMRST#	75	RSMRST#	OD12	Resume reset signal output.
GP52	SUSB#	73	SLP_S3#	INt	System S3 states input.
GP53	PSON#	72	PSON#	OD12	This pin generates the PWRCTL# signal while the power failure.
GP56	PSIN	68	PSIN	INtd	Panel Switch Input.
GP57	PSOUT#	67	PSOUT#	OD12	Panel Switch Output.
GP60	RIA#	57	RIA#	INt	Ring Indicator.
GP61	DCDA#	56	DCDA#	INt	Data Carrier Detect.
GP62	SOUTA/PENKBC	54	SOUTA	OUT8	UART A Serial Output.
GP63	SINA	53	SINA	INt	Serial Input.
GP64	DTRA#/PENROM	52	DTRA#	OUT8	UART A Data Terminal Ready.
GP65	RTSA#/HEFRAS	51	RTSA#	OUT8	UART A Request To Send.
GP66	DSRA#	50	DSRA#	INt	Data Set Ready.
GP67	CTSA#	49	CTSA#	INt	Clear To Send.

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
LAN	PIRQ#E	PREQ#4 PGNT#4	AD20	PCI_LAN
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM 1	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM 2	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

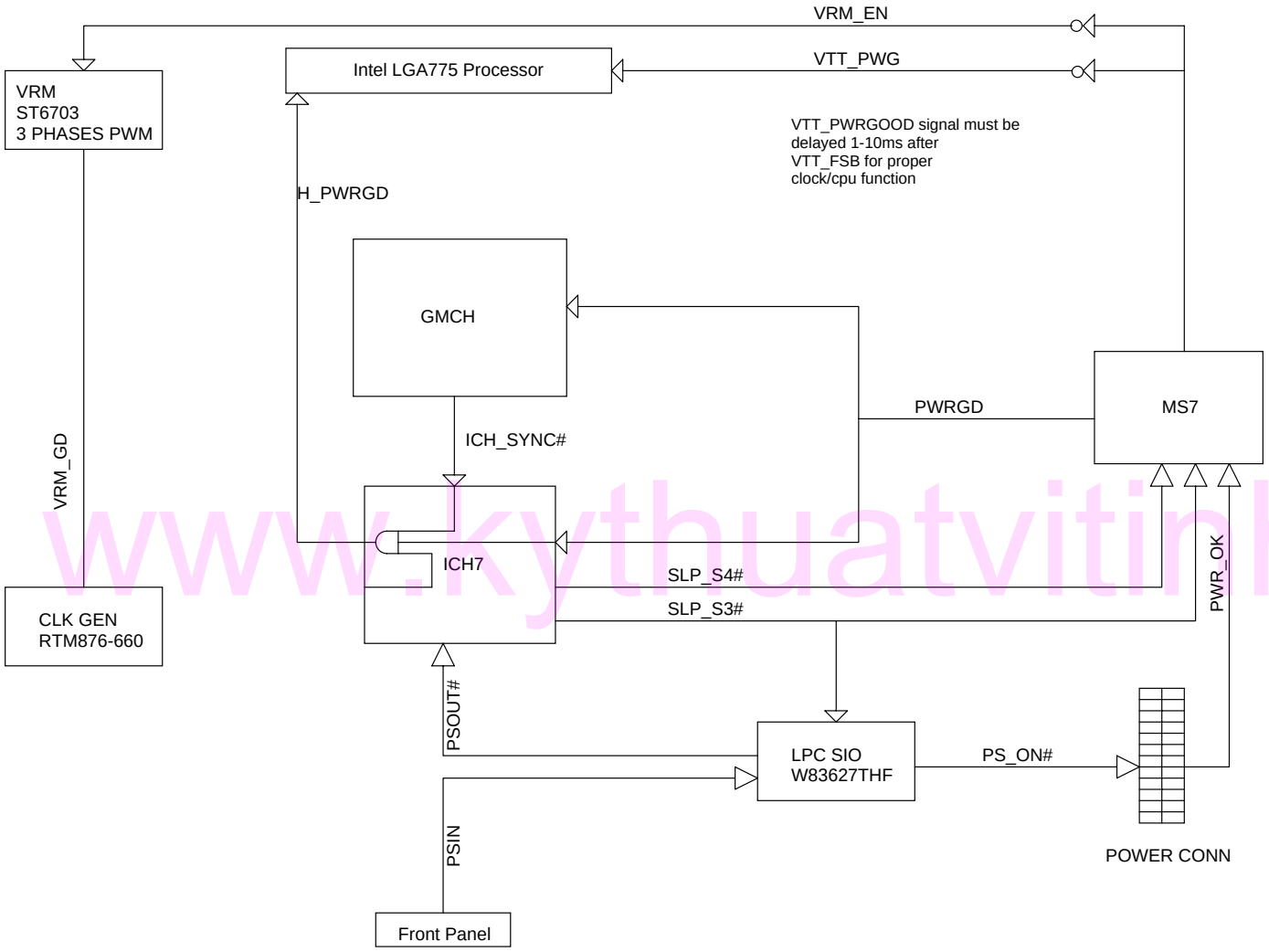
JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

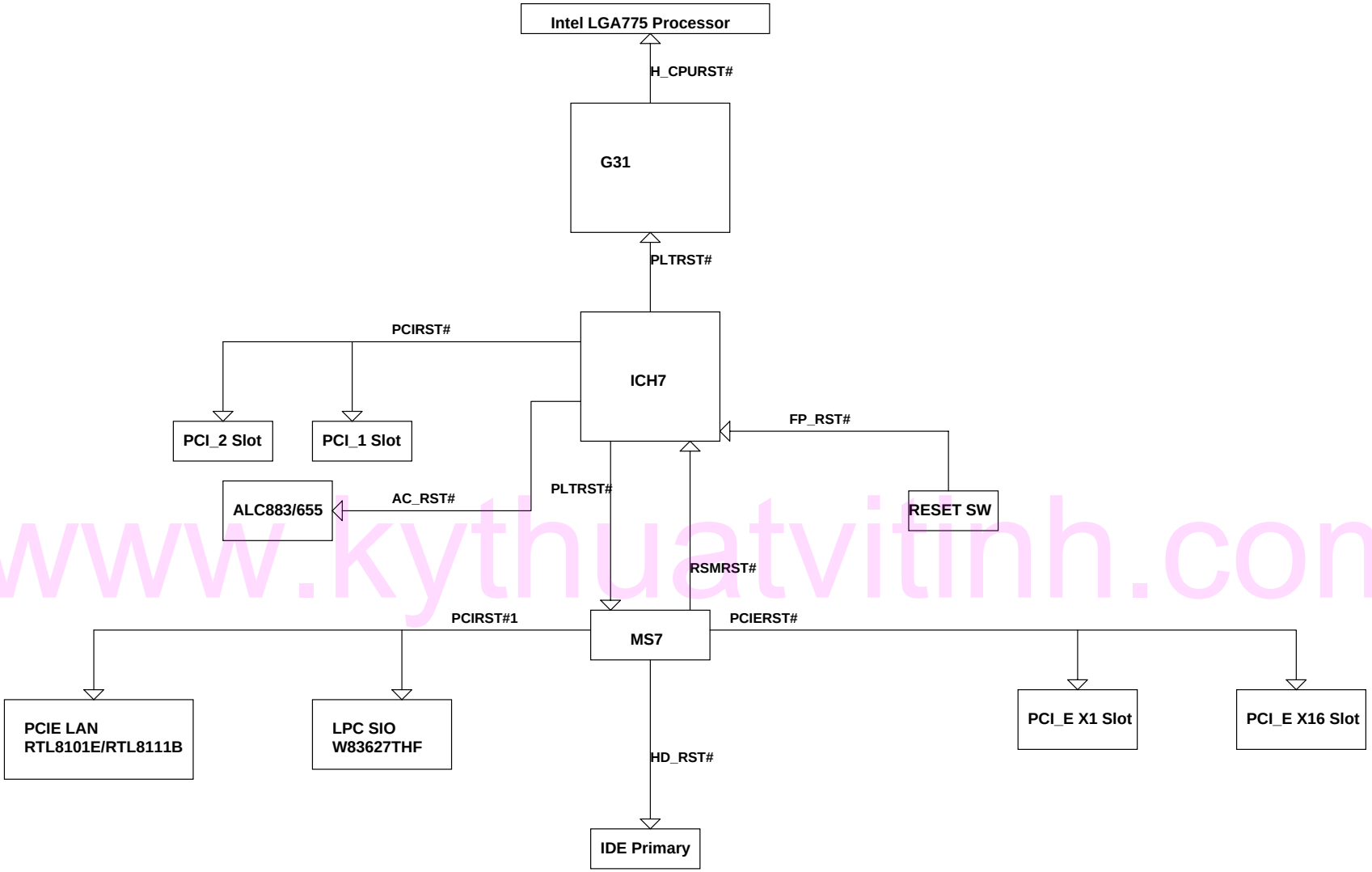
JCI1	***Chassis Intrusion***
Open	Normal
(1-2)	Chassis Open

Title	GPIO MAP & JUMPER SETTING		
Size	Document Number	MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 32 of 34		

PWROK MAP



Title	POWEROK MAP	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 33 of 34	



Title	RESET MAP	
Size	Document Number MS-7379	Rev 2.0
Date: Thursday, July 12, 2007	Sheet 34 of 34	