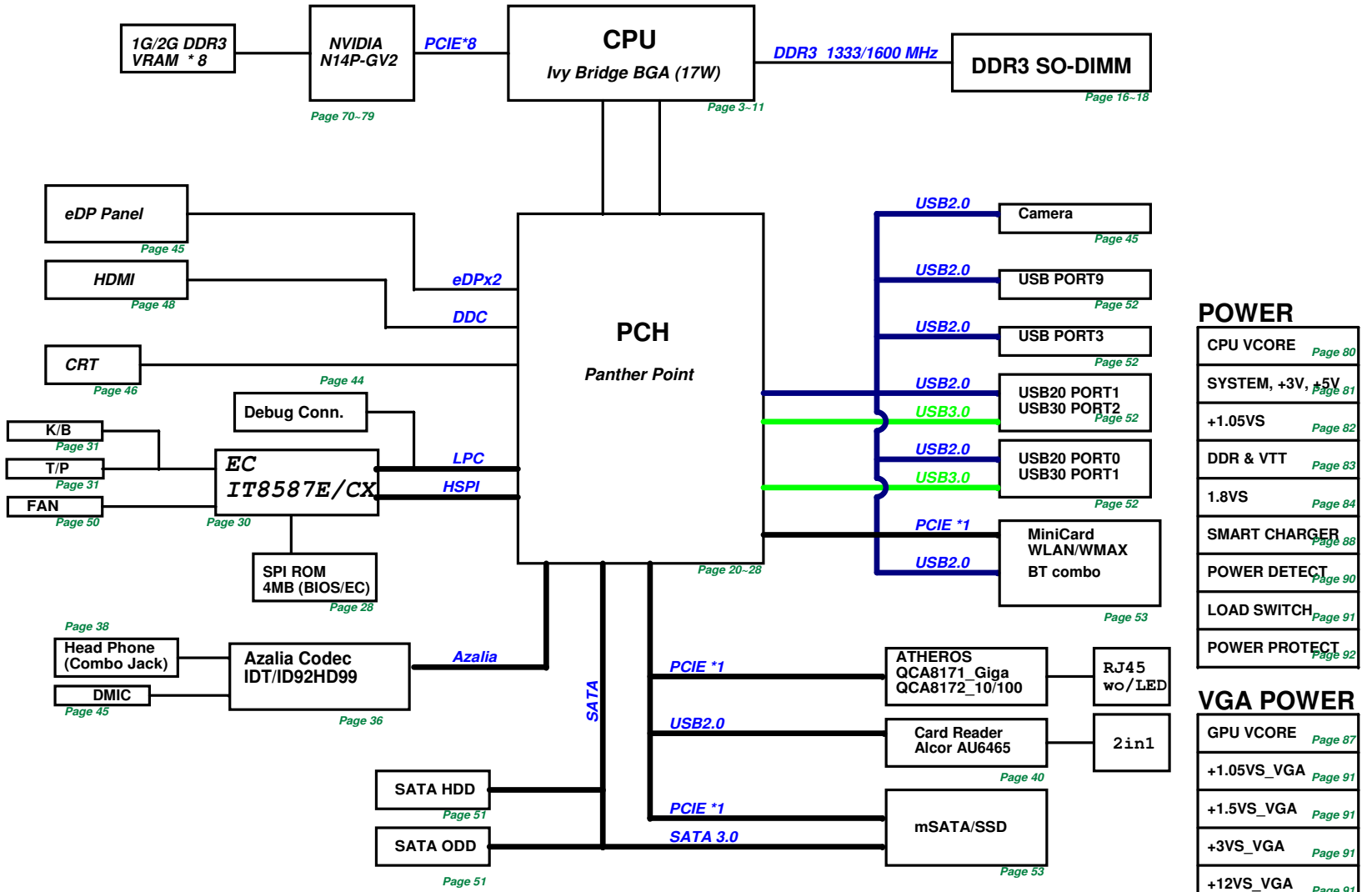
10FTG 15" CHIEF RIVER Schematics Rev 1.1

BLOCK DIAGRAM

SYSTEM PAGE REF.



POWER

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VGA POWER

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+1.5VS_VGA	Page 91
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Reset Circuit Page 32	Skew Holes Page 65

PEGATRON Title : Block Diagram
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size: Custom | Project Name: VGFTG | Rev: 1.1
Date: Tuesday, December 11, 2012 | Sheet 1 of 104

PCH_CPT GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	ID PX/UMA,DSC	PCB_ID4	EXT PU REV PD	+3VS
GPIO 01	ID STD/EN	PCB_ID6	EXT PU REV PD	+3VS
GPIO 02		MPC_PWR_CTRL#	EXT PU REV PD	+3VS
GPIO 03		SATA_ODD_DA#	EXT PU	+3VS
GPIO[4:5]		EXTTS_SNI_DRV[0:1]_PCH	EXT PU	+3VS
GPIO 06	ID Pre/Main	PCB_ID7	EXT PU REV PD	+3VS
GPIO 07	ID USB3.0	PCB_ID3	EXT PU REV PD	+3VS
GPIO 08		BT_ON/OFF#	EXT PU	+3VSUS_ORG
GPIO 09	ID Speaker	ONKYO_DET1	EXT PU	+3VSUS_ORG
GPIO 10	ID Sleep & Music	PCB_ID11	EXT PU REV PD	+3VSUS_ORG
GPIO 11		EXT_SCI#	EXT PU	+3VSUS_ORG
GPIO 12		GPIO12	EXT PU	+3VSUS_ORG
GPIO 13		GPIO13	EXT PU	+3VSUS_ORG
GPIO 14		PCB_ID10	EXT PU REV PD	+3VSUS_ORG
GPIO 15		EXT_SMI#	EXT PU	+3VSUS_ORG
GPIO 16	Clear PWD	GPIO16		+3VS
GPIO 17		DGPU_PWROK	EXT PU REV PD	+3VS
GPIO 18		CLK_REQ1#	EXT PU	+3VS
GPIO 19		BBS_BIT0	REV PD	+3VS
GPIO 20	WLAN	CLK_REQ_WLAN#	EXT PU REV PD	+3VS
GPIO 21	ID 17W/35W/45W	PCB_ID8	EXT PD REV PU	+3VS
GPIO 22		WLAN_LED	EXT PD	+3VS
GPIO 23		GPIO23	TEST POINT	+3VS
GPIO 24		GPIO24	EXT PU	+3VSUS_ORG
GPIO 25	LAN	CLK_REQ_LAN#	EXT PU REV PD	+3VSUS_ORG
GPIO 26		CLK_REQ4#	EXT PU	+3VSUS_ORG
GPIO 27		GPIO27	PD	+3VSUS_ORG
GPIO 28		PLL_ODVR_EN	REV PD	+3VSUS_ORG
GPIO 29		GPIO29	REV PU	+3VSUS_ORG
GPIO 30		ME_SUSPWRDNACK	EXT PU	+3VSUS_ORG
GPIO 31		ME_AC_PRESENT	EXT PU	+3VSUS_ORG
GPIO 32		PM_CLKRUN#	EXT PU	+3VS
GPIO 33		HDA_DOCK_EN#	TEST POINT	+3VS
GPIO 34	ID HDMI SKU	PCB_ID2	EXT PU REV PD	+3VS
GPIO 35		CRT_IN#	EXT PU	+3VS
GPIO 36		SATA_ODD_PRSNT#_R	EXT PU	+3VS
GPIO 37		FDI_OVRVLTG	EXT PD REV PU	+3VS
GPIO 38		PCB_ID0	EXT PD REV PU	+3VS
GPIO 39		PCB_ID1	EXT PD REV PU	+3VS
GPIO 40		GPIO40	EXT PU	+3VSUS_ORG
GPIO 41		GPIO41	EXT PU	+3VSUS_ORG
GPIO 42		GPIO42	EXT PU	+3VSUS_ORG
GPIO 43	ID Speaker	HARMAN_DET2	EXT PU	+3VSUS_ORG
GPIO 44		CLK_REQ5#	EXT PU	+3VSUS_ORG
GPIO 45		CLK_REQ6#	EXT PU	+3VSUS_ORG
GPIO 46		CLK_REQ7#	EXT PU	+3VSUS_ORG
GPIO 47		CLKREQ_PEG#	EXT PU REV PD	+3VSUS_ORG
GPIO 48	ID 17W/35W/45W	PCB_ID9	EXT PU REV PD	+3VS
GPIO 49	ID zero Power ODD	PCB_ID5	EXT PU REV PD	+3VS
GPIO 50		DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 51		BBS_BIT1	REV PD	+3VS
GPIO 52	ID eDP/LVDS	PCB_ID12	EXT PD REV PU	+3VS
GPIO 53		KB_LED_ID	REV PU	+3VS
GPIO 54		DGPU_PWR_EN	EXT PU	+3VS
GPIO 55		STP_A16OVR	REV PD	+3VS
GPIO 56		CLK_REQ_PEG_B#	EXT PU	+3VSUS_ORG
GPIO 57		WLAN_ON		+3VSUS_ORG
GPIO 58		SML1_CLK	EXT PU	+3VSUS_ORG
GPIO 59		GPIO59	EXT PU	+3VSUS_ORG
GPIO 60		DRAMRST_CNTRL_PCH	EXT PU	+3VSUS_ORG
GPIO 61		PM_SUS_STAT#	TEST POINT	+3VSUS_ORG
GPIO 62		SUSCLK	TEST POINT	+3VSUS_ORG
GPIO 63		SLP_S5#	TEST POINT	+3VSUS_ORG
GPIO 64		DGPU_EDID_SELECT#	REV PU	+3VS
GPIO 65		CLK_USB48_CR		+3VS
GPIO 66		GPIO66	TEST POINT	+3VS
GPIO 67		DGPU_PRSNT#	EXT PD REV PU	+3VS
GPIO 68		SATA_ODD_PWRGT	EXT PU	+3VS
GPIO 69		TV_DET	EXT PD	+3VS
GPIO[70:71]		GPIO[70:71]	EXT PU	+3VS
GPIO 72		BATLOW#	EXT PU& TP	+3VSUS_ORG
GPIO 73		CLK_REQ0#	EXT PU	+3VSUS_ORG
GPIO 74		SML1_ALERT#	EXT PU	+3VSUS_ORG
GPIO 75		SML1_DAT	EXT PU	+3VSUS_ORG

EC IT8587

EC GPIO	Use As	Signal Name
GPA0		PWR_WHITE_LED#
GPA1		BAT_ORG_LED#
GPA2		KEYBOARD_LED#
GPA3		DC_IN_LED#
GPA4		WLAN_RST#
GPA5		CHGCB2#
GPA6		THERM_ALERT#_EC
GPA7		PCH_FLASH_DESCRIPTOR
GPB0		NUM_LED#
GPB1		CAP_LED#
GPB2		THRO_CPU
GPB3		SMB0_CLK
GPB4		SMB0_DAT
GPB5		A20GATE
GPB6		RCIN#
GPB7		PM_RSMRST#
GPC0		CRX0
GPC1		SMB1_CLK
GPC2		SMB1_DAT
GPC3		KSO16
GPC4		AC_IN_OC
GPC5		KSO17
GPC6		BAT1_IN_OC#
GPC7		ME_AC_PRESENT
GPD0		PM_SUSB#
GPD1		PM_SUSC#
GPD2		BUF_PLT_RST#
GPD3		EXT_SCI#
GPD4		EXT_SMI#
GPD5		PM_PWROK
GPD6		FAN0_TACH
GPD7		USBP01_EN
GPE0		VSUS_ON
GPE1		SUSC_EC#
GPE2		SUSB_EC#
GPE3		CPU_VRON
GPE4		PWR_SW#_M
GPE5		USB_OC01#_EC
GPE6		LID_SW#
GPE7		USB_OC2#_EC
GPF0		BAT_LEARN
GPF1		ME_SUSPWRDNACK
GPF2		PM_PWRBTN#
GPF3		TEST pin
GPF4		TP_CLK
GPF5		TP_DAT
GPF6		H_PECI_EC
GPF7		LCD_BACKOFF#
GPG0		HDMI_HPD_M
GPG1		NC
GPG2		FB_CLAMP_TGL_REQ#
GPG6		HDPINT#
GPH0		PM_CLKRUN#
GPH1		CHGCB0#
GPH2		CHGCB1#
GPH3		KB_ID
GPH4		JACK_IN#
GPH5		HDPLOC
GPH6		HDPACT
GPI0		AD_IINP
GPI1		SUS_PWRGD
GPI2		ALL_SYSTEM_PWRGD
GPI3		VRM_PWRGD
GPI4		ADAPT_AD
GPI5		BACK_EN_C
GPI6		WLAN_ON_EC
GPI7		IMON
GPJ0		SLP_MUSIC_EN
GPJ1		BAT_OFF#
GPJ2		OP_SD#
GPJ3		USBSLP_EN
GPJ4		GPU_FB_CLAMP
GPJ5		CTL_FAN
GPJ6		SW_RTCRST
GPJ7		LAN_PWR_EN#
GPM0		LPC_AD0
GPM1		LPC_AD1
GPM2		LPC_AD2
GPM3		LPC_AD3
GPM4		CLK_KBCPCI_PCH
GPM5		LPC_FRAME#
GPM6		INT_SERIRQ

EC Name	Use As	Signal Name
WRST#		EC_RST#
FSCE#		SCE#
FSCK		SCK
FMOSI		SI
FMISO		SO
KSI0		KSI0
KSI1		KSI1
KSI2		KSI2
KSI3		KSI3
KSI4		KSI4
KSI5		KSI5
KSI6		KSI6
KSI7		KSI7
KSO0		KSO0
KSO1		KSO1
KSO2		KSO2
KSO3		KSO3
KSO4		KSO4
KSO5		KSO5
KSO6		KSO6
KSO7		KSO7
KSO8		KSO8
KSO9		KSO9
KSO10		KSO10
KSO11		KSO11
KSO12		KSO12
KSO13		KSO13
KSO14		KSO14
KSO15		KSO15

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	WLAN
PCIE 3	LAN
PCIE 4	N/A
PCIE 5	N/A
PCIE 6	N/A
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	mSATA
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

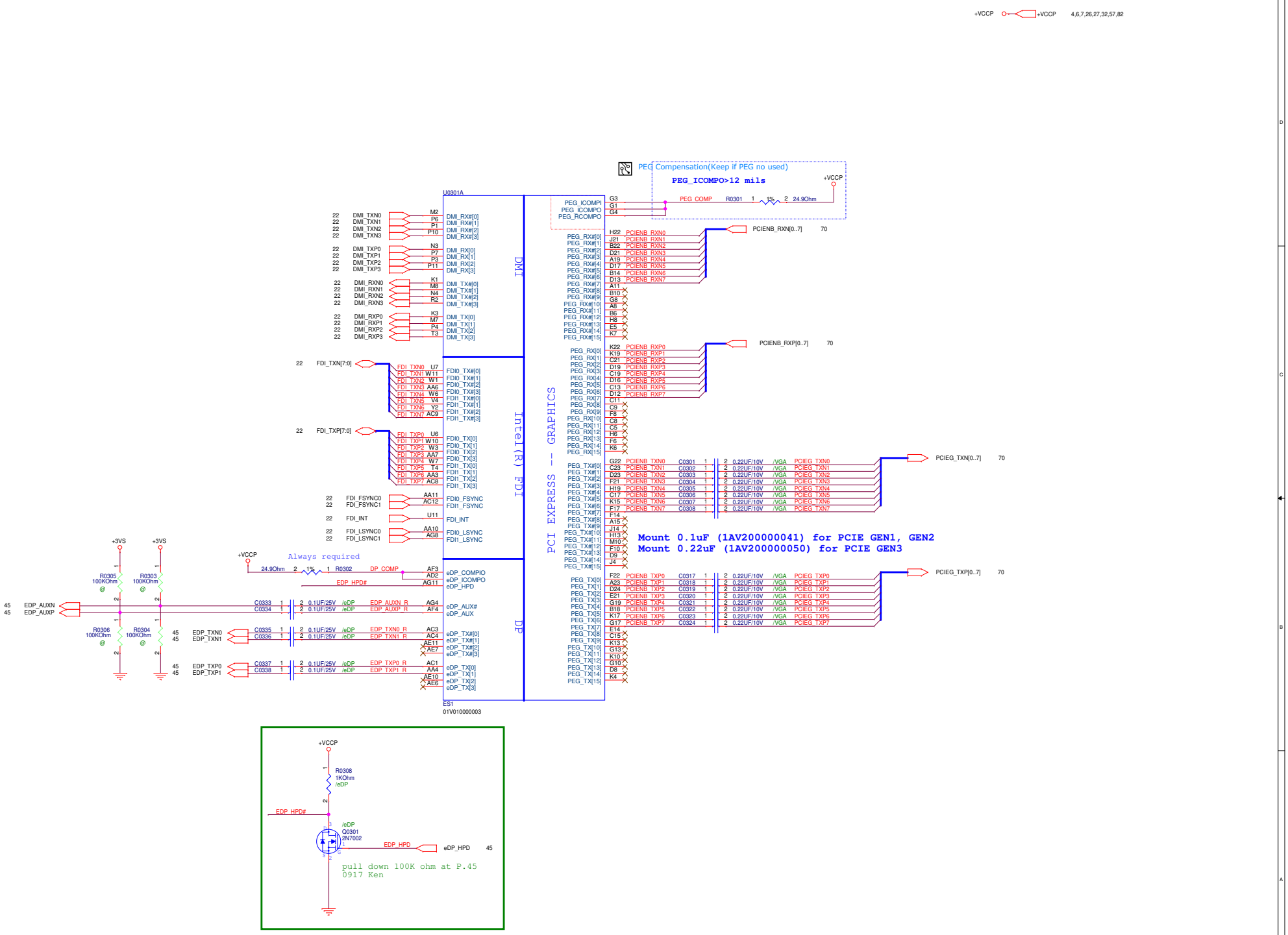
USB 0	USB 3.0 Port(Right Front)
USB 1	USB 3.0 Port (Right Back)
USB 2	WIFI/BT
USB 3	USB-Reserve
USB 4	TV Tuner Card1
USB 5	TV Tuner Card2
USB 6	N/A
USB 7	N/A
USB 8	Card reader
USB 9	USB(Left Front)
USB 10	Camera
USB 11	Touch Panel
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

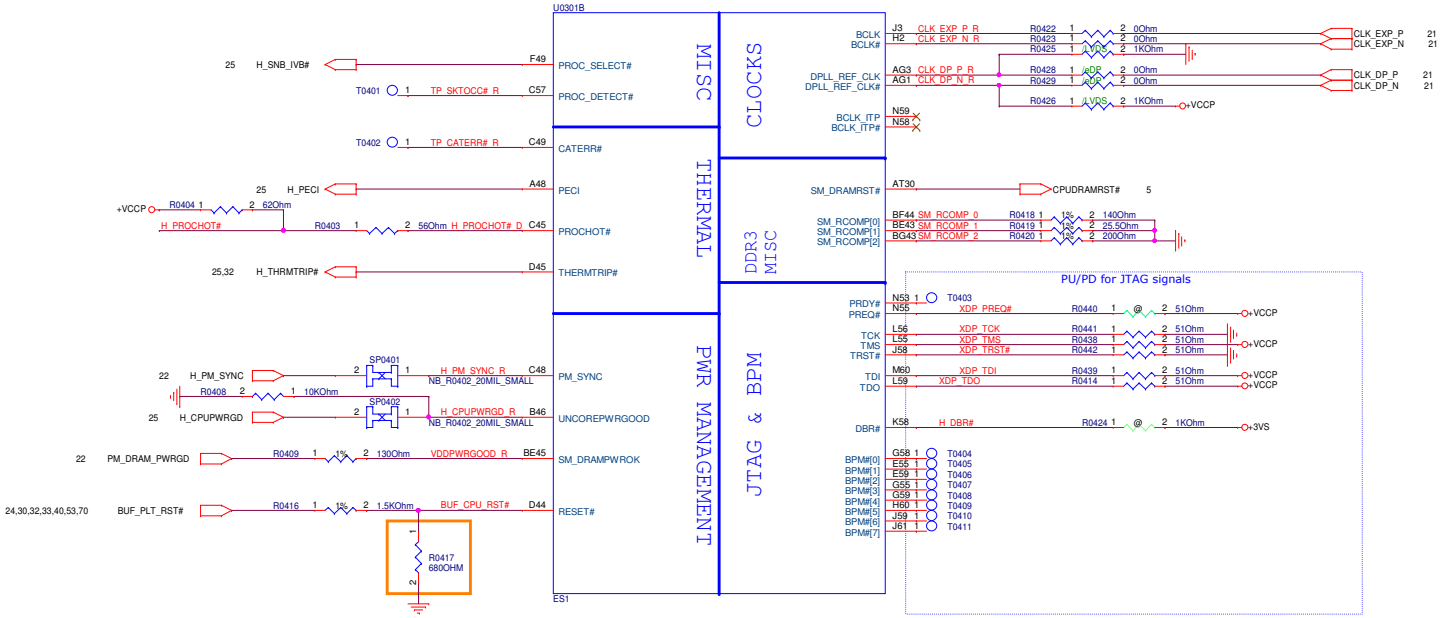
Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 2 of 104



PEGATRON	Title: CRU(1)_DMI,DP,PEG,FDI		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 3 of 104		

+1.5V → +1.5V 5,7,16,17,18,57,83
+3VS → +3VS 3,16,17,20,21,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+3VSUS → +3VSUS 22,24,27,28,30,33,34,37,53,62,81,92
+VCCP → +VCCP 3,6,7,26,27,32,57,82
+3V → +3V 24,44,45,57,91

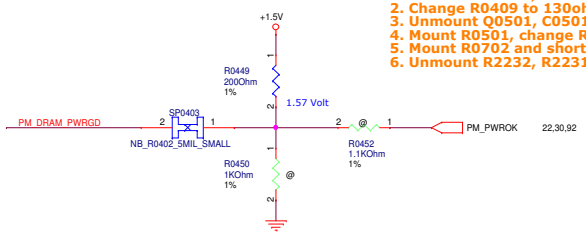


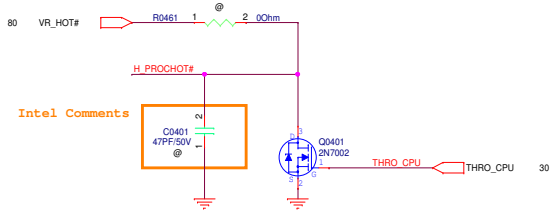
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

Different from EVEREST

If don't support S3 power reduction
1. Unmount R0450, R0452
2. Change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106
3. Unmount Q0501, C0501, R0506, R0507
4. Mount R0501, change R0508 to 0ohm from 1kohm
5. Mount R0702 and short JP0701
6. Unmount R2232, R2231, Q2203





PEGATRON
Title : CPU(1)_CLK,MISC,JTAG
Engineer: Jim3_Liu
BG1-CSC-HW R&D Dept.5
Size C | Project Name VGFTG | Rev 1.1
Date: Tuesday, December 11, 2012 | Sheet 4 of 104

+1.5V +1.5V 4,7,16,17,18,57,83

U0301C

DDR SYSTEM MEMORY A

16 M_A_DQ[63:0]

M_A_DQ0	AG6	SA_DQ[0]
M_A_DQ1	AJ6	SA_DQ[1]
M_A_DQ2	AP11	SA_DQ[2]
M_A_DQ3	AL6	SA_DQ[3]
M_A_DQ4	AJ10	SA_DQ[4]
M_A_DQ5	AJ8	SA_DQ[5]
M_A_DQ6	AL8	SA_DQ[6]
M_A_DQ7	AL7	SA_DQ[7]
M_A_DQ8	AR11	SA_DQ[8]
M_A_DQ9	AP6	SA_DQ[9]
M_A_DQ10	AU6	SA_DQ[10]
M_A_DQ11	AV9	SA_DQ[11]
M_A_DQ12	AR6	SA_DQ[12]
M_A_DQ13	AP8	SA_DQ[13]
M_A_DQ14	AT13	SA_DQ[14]
M_A_DQ15	AU13	SA_DQ[15]
M_A_DQ16	BC7	SA_DQ[16]
M_A_DQ17	BB7	SA_DQ[17]
M_A_DQ18	BA13	SA_DQ[18]
M_A_DQ19	BB11	SA_DQ[19]
M_A_DQ20	BA7	SA_DQ[20]
M_A_DQ21	BA9	SA_DQ[21]
M_A_DQ22	BB9	SA_DQ[22]
M_A_DQ23	AY13	SA_DQ[23]
M_A_DQ24	AV14	SA_DQ[24]
M_A_DQ25	AR14	SA_DQ[25]
M_A_DQ26	AY17	SA_DQ[26]
M_A_DQ27	AR19	SA_DQ[27]
M_A_DQ28	BA14	SA_DQ[28]
M_A_DQ29	AU14	SA_DQ[29]
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M_A_DQ35	BC48	SA_DQ[35]
M_A_DQ36	BC45	SA_DQ[36]
M_A_DQ37	AR45	SA_DQ[37]
M_A_DQ38	AT48	SA_DQ[38]
M_A_DQ39	AY48	SA_DQ[39]
M_A_DQ40	BA49	SA_DQ[40]
M_A_DQ41	AV49	SA_DQ[41]
M_A_DQ42	BB51	SA_DQ[42]
M_A_DQ43	AY53	SA_DQ[43]
M_A_DQ44	BB49	SA_DQ[44]
M_A_DQ45	AU49	SA_DQ[45]
M_A_DQ46	BA53	SA_DQ[46]
M_A_DQ47	BB55	SA_DQ[47]
M_A_DQ48	BA55	SA_DQ[48]
M_A_DQ49	AV56	SA_DQ[49]
M_A_DQ50	AP50	SA_DQ[50]
M_A_DQ51	AP53	SA_DQ[51]
M_A_DQ52	AV54	SA_DQ[52]
M_A_DQ53	AT54	SA_DQ[53]
M_A_DQ54	AP56	SA_DQ[54]
M_A_DQ55	AP52	SA_DQ[55]
M_A_DQ56	AN57	SA_DQ[56]
M_A_DQ57	AN53	SA_DQ[57]
M_A_DQ58	AG56	SA_DQ[58]
M_A_DQ59	AG53	SA_DQ[59]
M_A_DQ60	AN55	SA_DQ[60]
M_A_DQ61	AN52	SA_DQ[61]
M_A_DQ62	AG55	SA_DQ[62]
M_A_DQ63	AK56	SA_DQ[63]

SA_CK[0]	AU36	M_A_DIM0_CLK_DDR0 16
SA_CK#[0]	AV36	M_A_DIM0_CLK_DDR#0 16
SA_CKE[0]	AY26	M_A_DIM0_CKE0 16
SA_CK[1]	AT40	M_A_DIM0_CLK_DDR1 16
SA_CK#[1]	AU40	M_A_DIM0_CLK_DDR#1 16
SA_CKE[1]	BB26	M_A_DIM0_CKE1 16
SA_CS#[0]	BB40	M_A_DIM0_CS#0 16
SA_CS#[1]	BC41	M_A_DIM0_CS#1 16
SA_ODT[0]	AY40	M_A_DIM0_ODT0 16
SA_ODT[1]	BA41	M_A_DIM0_ODT1 16

SA_DQS#[0]	AL11	M_A_DQS#0	M_A_DQS#[7:0] 16
SA_DQS#[1]	AR8	M_A_DQS#1	
SA_DQS#[2]	AV11	M_A_DQS#2	
SA_DQS#[3]	AT17	M_A_DQS#3	
SA_DQS#[4]	AV45	M_A_DQS#4	
SA_DQS#[5]	AY51	M_A_DQS#5	
SA_DQS#[6]	AT55	M_A_DQS#6	
SA_DQS#[7]	AK55	M_A_DQS#7	

SA_DQS[0]	AJ11	M_A_DQS0	M_A_DQS[7:0] 16
SA_DQS[1]	AR10	M_A_DQS1	
SA_DQS[2]	AY11	M_A_DQS2	
SA_DQS[3]	AU17	M_A_DQS3	
SA_DQS[4]	AW45	M_A_DQS4	
SA_DQS[5]	AV51	M_A_DQS5	
SA_DQS[6]	AT56	M_A_DQS6	
SA_DQS[7]	AK54	M_A_DQS7	

SA_MA[0]	BG35	M_A_A0	M_A_A[15:0] 16
SA_MA[1]	BB34	M_A_A1	
SA_MA[2]	BE35	M_A_A2	
SA_MA[3]	BD35	M_A_A3	
SA_MA[4]	AT34	M_A_A4	
SA_MA[5]	AU34	M_A_A5	
SA_MA[6]	BB32	M_A_A6	
SA_MA[7]	AT32	M_A_A7	
SA_MA[8]	AY32	M_A_A8	
SA_MA[9]	AV32	M_A_A9	
SA_MA[10]	BE37	M_A_A10	
SA_MA[11]	BA30	M_A_A11	
SA_MA[12]	BC30	M_A_A12	
SA_MA[13]	AW41	M_A_A13	
SA_MA[14]	AY28	M_A_A14	
SA_MA[15]	AU26	M_A_A15	

16 M_A_BS0	BD37	SA_BS[0]
16 M_A_BS1	BF36	SA_BS[1]
16 M_A_BS2	BA28	SA_BS[2]
16 M_A_CAS#	BE39	SA_CAS#
16 M_A_RAS#	BD39	SA_RAS#
16 M_A_WE#	AT41	SA_WE#

ES1
01V010000003

U0301D

DDR SYSTEM MEMORY B

17 M_B_DQ[63:0]

M_B_DQ0	AL4	SB_DQ[0]
M_B_DQ1	AL1	SB_DQ[1]
M_B_DQ2	AN3	SB_DQ[2]
M_B_DQ3	AR4	SB_DQ[3]
M_B_DQ4	AK4	SB_DQ[4]
M_B_DQ5	AK3	SB_DQ[5]
M_B_DQ6	AN4	SB_DQ[6]
M_B_DQ7	AR1	SB_DQ[7]
M_B_DQ8	AU4	SB_DQ[8]
M_B_DQ9	AT2	SB_DQ[9]
M_B_DQ10	AV4	SB_DQ[10]
M_B_DQ11	BA4	SB_DQ[11]
M_B_DQ12	AU3	SB_DQ[12]
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M_B_DQ19	BF12	SB_DQ[19]
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M_B_DQ21	BD10	SB_DQ[21]
M_B_DQ22	BD14	SB_DQ[22]
M_B_DQ23	BE13	SB_DQ[23]
M_B_DQ24	BF16	SB_DQ[24]
M_B_DQ25	BE17	SB_DQ[25]
M_B_DQ26	BE18	SB_DQ[26]
M_B_DQ27	BE21	SB_DQ[27]
M_B_DQ28	BE14	SB_DQ[28]
M_B_DQ29	BG14	SB_DQ[29]
M_B_DQ30	BG18	SB_DQ[30]
M_B_DQ31	BF19	SB_DQ[31]
M_B_DQ32	BD50	SB_DQ[32]
M_B_DQ33	BF48	SB_DQ[33]
M_B_DQ34	BD53	SB_DQ[34]
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M_B_DQ37	BE49	SB_DQ[37]
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M_B_DQ53	AU61	SB_DQ[53]
M_B_DQ54	AN58	SB_DQ[54]
M_B_DQ55	AR58	SB_DQ[55]
M_B_DQ56	AK58	SB_DQ[56]
M_B_DQ57	AL58	SB_DQ[57]
M_B_DQ58	AG58	SB_DQ[58]
M_B_DQ59	AG59	SB_DQ[59]
M_B_DQ60	AM60	SB_DQ[60]
M_B_DQ61	AL59	SB_DQ[61]
M_B_DQ62	AF61	SB_DQ[62]
M_B_DQ63	AH60	SB_DQ[63]

SB_CK[0]	BA34	M_B_DIM0_CLK_DDR0 17
SB_CK#[0]	AY34	M_B_DIM0_CLK_DDR#0 17
SB_CKE[0]	AR22	M_B_DIM0_CKE0 17
SB_CK[1]	BA36	M_B_DIM0_CLK_DDR1 17
SB_CK#[1]	BB36	M_B_DIM0_CLK_DDR#1 17
SB_CKE[1]	BF27	M_B_DIM0_CKE1 17
SB_CS#[0]	BE41	M_B_DIM0_CS#0 17
SB_CS#[1]	BE47	M_B_DIM0_CS#1 17
SB_ODT[0]	AT43	M_B_DIM0_ODT0 17
SB_ODT[1]	BG47	M_B_DIM0_ODT1 17

SB_DQS#[0]	AL3	M_B_DQS#0	M_B_DQS#[7:0] 17
SB_DQS#[1]	AV3	M_B_DQS#1	
SB_DQS#[2]	BG11	M_B_DQS#2	
SB_DQS#[3]	BD17	M_B_DQS#3	
SB_DQS#[4]	BG51	M_B_DQS#4	
SB_DQS#[5]	BA59	M_B_DQS#5	
SB_DQS#[6]	AT60	M_B_DQS#6	
SB_DQS#[7]	AK59	M_B_DQS#7	

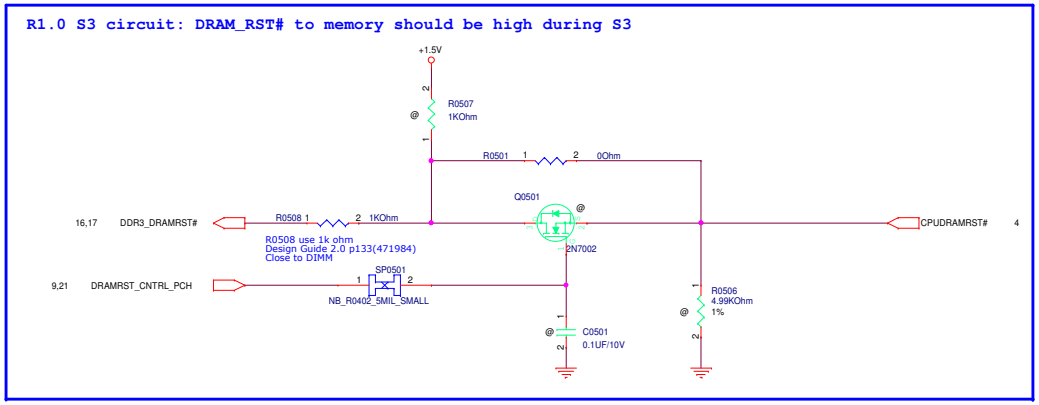
SB_DQS[0]	AM2	M_B_DQS0	M_B_DQS[7:0] 17
SB_DQS[1]	AV1	M_B_DQS1	
SB_DQS[2]	BE11	M_B_DQS2	
SB_DQS[3]	BD18	M_B_DQS3	
SB_DQS[4]	BE51	M_B_DQS4	
SB_DQS[5]	BA61	M_B_DQS5	
SB_DQS[6]	AR59	M_B_DQS6	
SB_DQS[7]	AK61	M_B_DQS7	

SB_MA[0]	BF32	M_B_A0	M_B_A[15:0] 17
SB_MA[1]	BE33	M_B_A1	
SB_MA[2]	BD33	M_B_A2	
SB_MA[3]	AU30	M_B_A3	
SB_MA[4]	BD30	M_B_A4	
SB_MA[5]	AV30	M_B_A5	
SB_MA[6]	BG30	M_B_A6	
SB_MA[7]	BD29	M_B_A7	
SB_MA[8]	BE30	M_B_A8	
SB_MA[9]	BE28	M_B_A9	
SB_MA[10]	BD43	M_B_A10	
SB_MA[11]	AT28	M_B_A11	
SB_MA[12]	AV28	M_B_A12	
SB_MA[13]	BD46	M_B_A13	
SB_MA[14]	AT26	M_B_A14	
SB_MA[15]	AU22	M_B_A15	

17 M_B_BS0	BG39	SB_BS[0]
17 M_B_BS1	BD42	SB_BS[1]
17 M_B_BS2	AT22	SB_BS[2]
17 M_B_CAS#	AV43	SB_CAS#
17 M_B_RAS#	BF40	SB_RAS#
17 M_B_WE#	BD45	SB_WE#

ES1
01V010000003

R1.0 S3 circuit: DRAM_RST# to memory should be high during S3

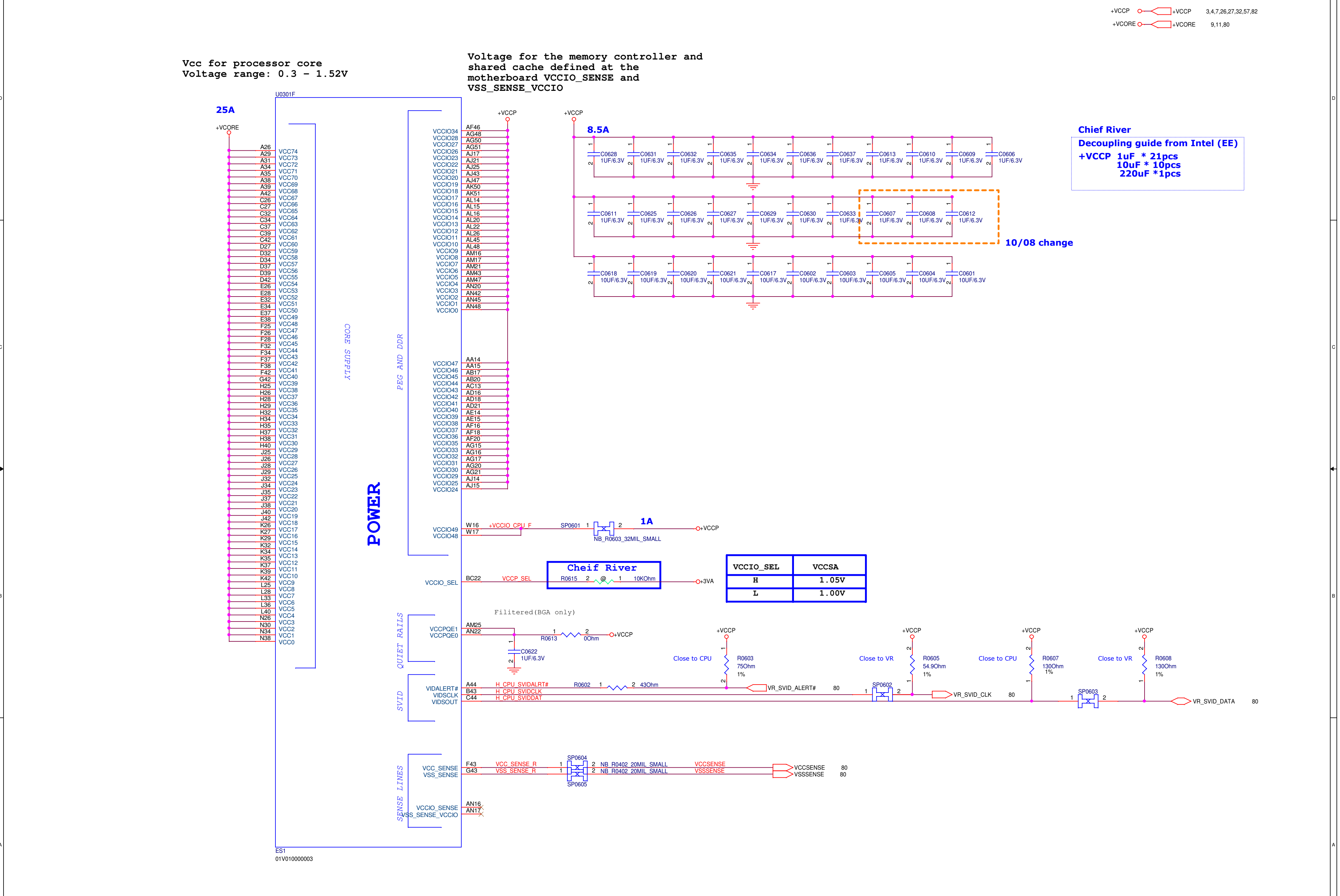


PEGATRON Title : CPU(3)_DDR3

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 5 of 104



VCCIO_SEL	VCCSA
H	1.05V
L	1.00V

PEGATRON Title : CPU(4)_Processor Power

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 6 of 104

+VCCP +VCCP 3,4,6,26,27,32,57,82
+1.5V +1.5V 4,5,16,17,18,57,83
+VCCSA +VCCSA 57,82
+1.8VS +1.8VS 25,26,84
+VGFX_CORE +VGFX_CORE 9,80
+V_SM_VREF +V_SM_VREF 18

Decoupling guide from Intel PDDG R0.8
+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

Graphics core voltage Voltage range: 0 - 1.52V

+VGFX_CORE

C0725 1UF/6.3V, C0727 1UF/6.3V, C0731 1UF/6.3V, C0726 1UF/6.3V, C0732 1UF/6.3V, C0729 1UF/6.3V, C0730 1UF/6.3V, C0728 1UF/6.3V
C0717 1UF/6.3V, C0719 1UF/6.3V, C0722 1UF/6.3V, C0790 10UF/6.3V, C0791 10UF/6.3V, C0788 10UF/6.3V, C0789 10UF/6.3V, C0787 10UF/6.3V
C0786 10UF/6.3V, C0738 22UF/6.3V, C0739 22UF/6.3V, C0740 22UF/6.3V, C0741 22UF/6.3V, C0742 22UF/6.3V, C0743 22UF/6.3V
@ CE0703 330UF/2.5V vx_c3528_h79

U0301G

AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 V47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y51
VAXG21 VAXG20 VAXG19 VAXG18 VAXG17 VAXG16 VAXG15 VAXG14 VAXG13 VAXG12 VAXG11 VAXG10 VAXG9 VAXG8 VAXG7 VAXG6 VAXG5 VAXG4 VAXG3 VAXG2 VAXG1 VAXG0 VAXG55 VAXG54 VAXG53 VAXG52 VAXG51 VAXG50 VAXG49 VAXG48 VAXG47 VAXG46 VAXG45 VAXG44 VAXG43 VAXG42 VAXG41 VAXG40 VAXG39 VAXG38 VAXG37 VAXG36 VAXG35 VAXG34 VAXG33 VAXG32 VAXG31 VAXG30 VAXG29 VAXG28 VAXG27 VAXG26 VAXG25 VAXG24 VAXG23 VAXG22

GRAPHICS

POWER

DDR3 - 1.5V RAILS

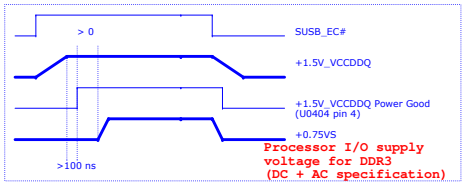
(Without Implement S3 circuit)

SM_VREF AY43 +V_SM_VREF +V_SM_VREF
+V_SM_REF 10mil

VDDQ25 VDDQ24 VDDQ23 VDDQ22 VDDQ21 VDDQ20 VDDQ19 VDDQ18 VDDQ17 VDDQ16 VDDQ15 VDDQ14 VDDQ13 VDDQ12 VDDQ11 VDDQ10 VDDQ9 VDDQ8 VDDQ7 VDDQ6 VDDQ5 VDDQ4 VDDQ3 VDDQ2 VDDQ1 VDDQ0
AJ28 AJ33 AJ36 AJ40 AL30 AL34 AL38 AL42 AM33 AM36 AM40 AN30 AN34 AN38 AR26 AR28 AR30 AR32 AR34 AR36 AR40 AV41 AW26 BA40 BB28 BG33

+1.5V
5A
C0704 1UF/6.3V, C0709 1UF/6.3V, C0705 1UF/6.3V, C0706 1UF/6.3V, C0707 1UF/6.3V, C0708 1UF/6.3V, C0713 1UF/6.3V, C0710 1UF/6.3V, C0712 1UF/6.3V, C0711 1UF/6.3V
C0775 10UF/6.3V, C0774 10UF/6.3V, C0772 10UF/6.3V, C0769 10UF/6.3V, C0767 10UF/6.3V, C0765 10UF/6.3V, C0770 10UF/6.3V, C0768 10UF/6.3V

Chief River
Decoupling guide from Intel (EE)
+1.5VS_VCCDDQ
1uF * 10pcs
10uF * 8pcs



80 VCCGT_SENSE
80 VSSGT_SENSE
SP0701 SP0702
VCCGT_SENSE 2 1 NB_R0402_20MIL_SMALL VCCGT_SENSE_R F45
VSSGT_SENSE 2 1 NB_R0402_20MIL_SMALL VSSGT_SENSE_R G45
VAXG_SENSE
VSSAXG_SENSE

SENSE LINES

QUIET RAILS

Filtered(BGA Only)
+1.5V
+1.5VS_VCCDDQ_R
AM28 AN26 VCCDQ1 VCCDQ0
1A
R0707 1 2 0Ohm
C0714 1UF/6.3V

PLL supply voltage
(DC + AC specification)

+1.8VS
10/08 change
C0780 22UF/6.3V
1.2A
C0761 1UF/6.3V, C0764 1UF/6.3V
BB3 BC1 BC4 VCCPLL2 VCCPLL1 VCCPLL0

1.8V RAIL

VDDQ_SENSE
VSS_SENSE_VDDQ
BC43 BA43 T0701 T0702

SENSE LINES

+VCCSA
2.4A
C0735 1UF/6.3V, C0736 1UF/6.3V, C0733 1UF/6.3V, C0734 1UF/6.3V, C0737 1UF/6.3V
C0783 10UF/6.3V, C0781 10UF/6.3V, C0792 10UF/6.3V, C0777 10UF/6.3V, C0793 10UF/6.3V
L17 L21 N16 N20 N22 P17 P20 R16 R18 R21 U15 V16 V17 V18 V21 W20
VCCSA15 VCCSA14 VCCSA13 VCCSA12 VCCSA11 VCCSA10 VCCSA9 VCCSA8 VCCSA7 VCCSA6 VCCSA5 VCCSA4 VCCSA3 VCCSA2 VCCSA1 VCCSA0

SA RAIL

U10 VCCSA_SENSE VCCSA_SENSE
R0704 1 @ 2 0Ohm Close to CPU

VCCSA_VID[0] D48 VCCSA_SEL0 VCCSA_SEL0 82
VCCSA_VID[1] D49 VCCSA_SEL1 VCCSA_SEL1 82

Chief River

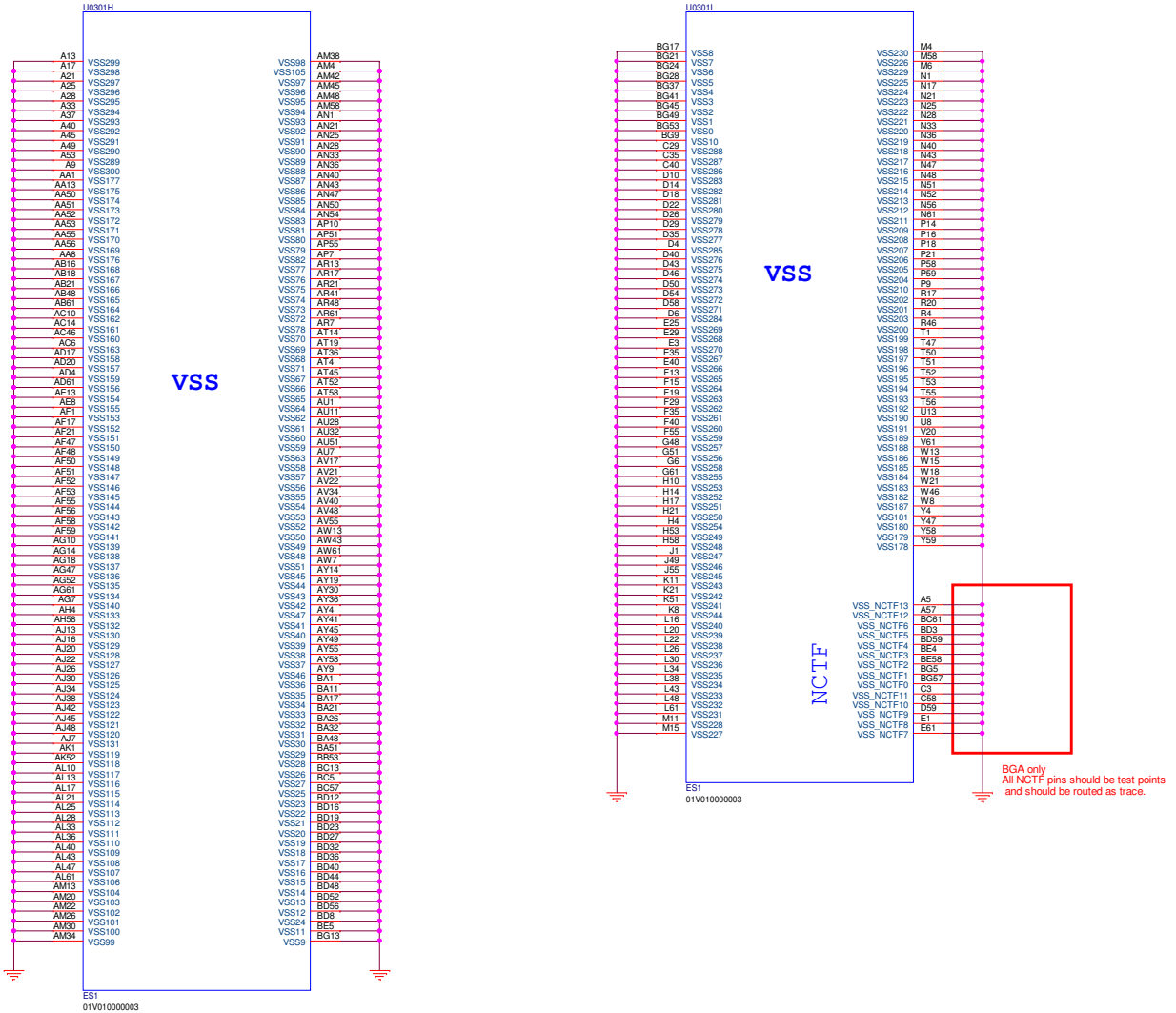
Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

ES1
01V010000003

+VCCP
R0708 1KOhm @
R0709 1KOhm @
VCCSA_SEL0
VCCSA_SEL1
R0701 1KOhm
R0702 1KOhm

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V

PEGATRON Title : CPU(5)_Graphics Power
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size C | Project Name VGFTG | Rev 1.1
Date: Tuesday, December 11, 2012 | Sheet 7 of 104



PEGATRON Title : CPU(6)_GND

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 8 of 104

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

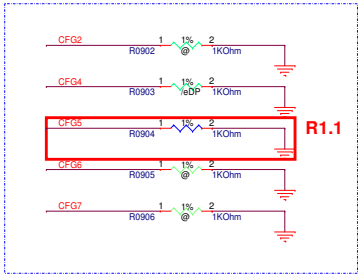
- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed

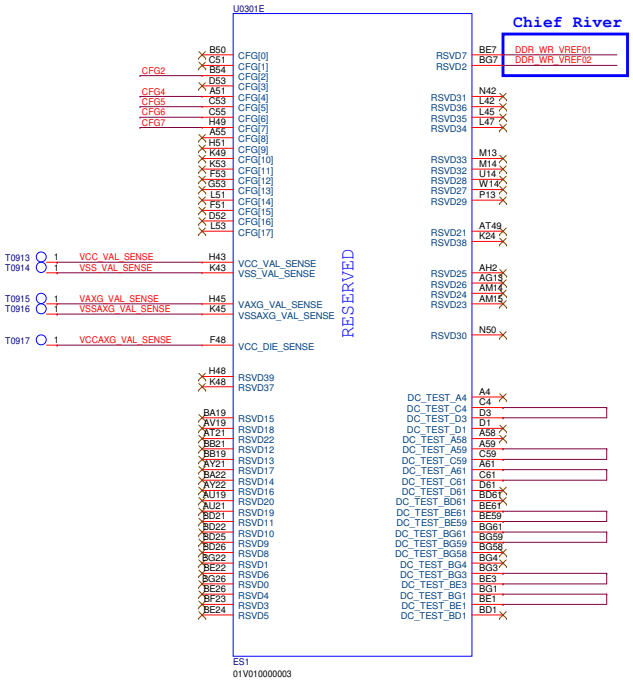
CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

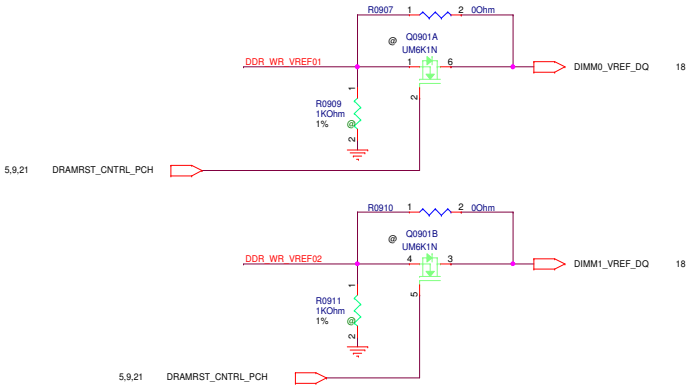
CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

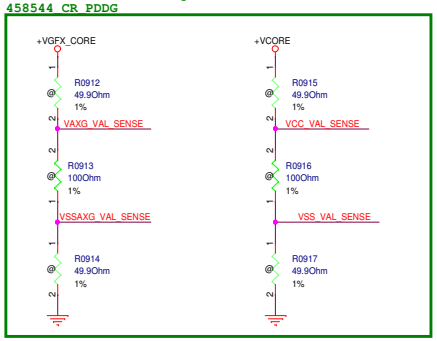




PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



For iFDIM testing
R0912~ R0917 close to pin < 1 inch
458544 CR PDDG



PEGATRON Title : CPU(7)_RESERVED

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 9 of 104

PEGATRON

Title : CPU_PCH_XDP*****

BG1-CSC-HW R&D Dept.5

Engineer: Jim3_Liu

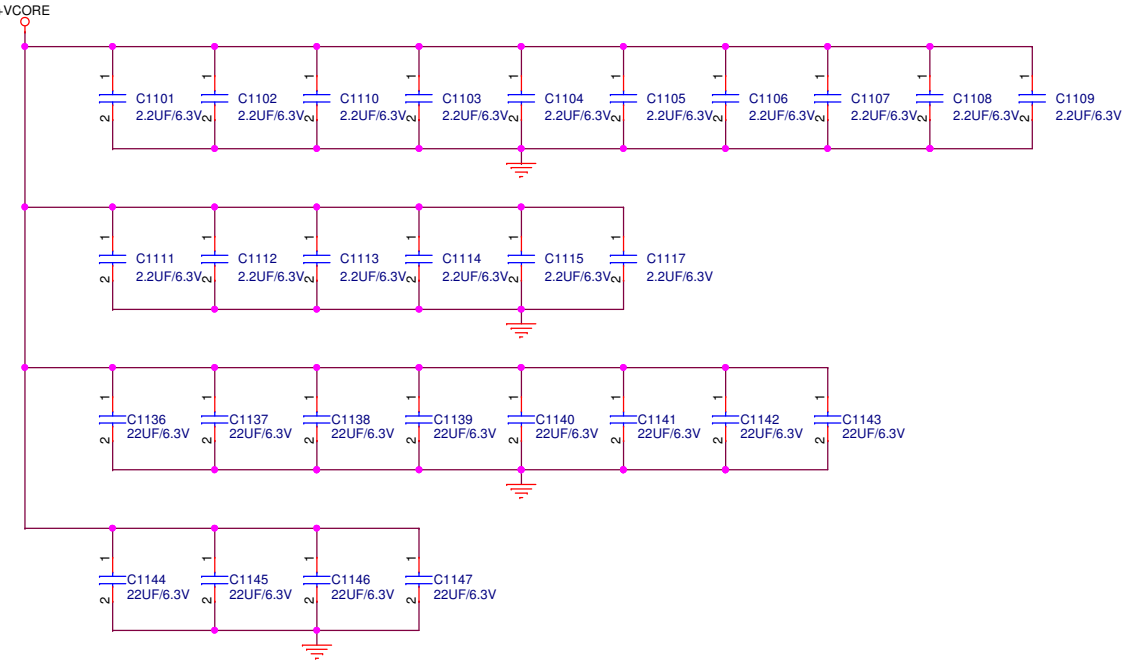
Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 10 of 104

Chief River

Decoupling guide from Intel PDDG R0.8

+VCORE 2.2uF * 16 pcs
22uF * 12 pcs



PEGATRON Title : CPU DECOUPLING

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
B	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 11 of 104

+1.5V +1.5V 4,5,7,17,18,57,83

+0.75VS +0.75VS 17,57,83

+3VS +3VS 3,4,17,20,21,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92

+V_VREF_CA_DIMM0 +V_VREF_CA_DIMM0 18

+V_VREF_DQ_DIMM0 +V_VREF_DQ_DIMM0 18

+1.5V

Layout Note: Place these caps near SO DIMM 0

@ CE1601 330UF/2.5V 1BV080000031

vx_c0603_small

C1609 10UF/6.3V

C1610 10UF/6.3V

C1611 10UF/6.3V

C1612 10UF/6.3V @

C1613 10UF/6.3V @

C1620 10UF/6.3V @

+0.75VS

C1616 1UF/6.3V

C1617 1UF/6.3V

C1618 1UF/6.3V @

C1619 1UF/6.3V @

H4.0mm,REV

5 M_A_A[15:0]

M_A_A0 98 M_A_A1 97 M_A_A2 96 M_A_A3 95 M_A_A4 92 M_A_A5 91 M_A_A6 90 M_A_A7 86 M_A_A8 89 M_A_A9 85 M_A_A10 107 M_A_A11 84 M_A_A12 83 M_A_A13 119 M_A_A14 80 M_A_A15 78

M_A_DIM0_CLK_DDR0 C1602 10PF/50V @ 1% 150Ohm R1603 @

M_A_DIM0_CLK_DDR#0

M_A_DIM0_CLK_DDR1 C1601 10PF/50V @ 1% 150Ohm R1604 @

M_A_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

5 M_A_DIM0_CLK_DDR1 102 CK1

5 M_A_DIM0_CLK_DDR#1 104 CK1#

5 M_A_DIM0_CLK_DDR0 101 CK0

5 M_A_DIM0_CLK_DDR#0 103 CK0#

5 M_A_DIM0_CS#1 121 S1#

5 M_A_DIM0_CS#0 114 S0#

5 M_A_DIM0_ODT1 120 ODT1

5 M_A_DIM0_ODT0 116 ODT0

5 M_A_WE# 113 WE#

5 M_A_RAS# 110 RAS#

5 M_A_CAS# 115 CAS#

5 M_A_BS2 79 BA2

5 M_A_BS1 108 BA1

5 M_A_BS0 109 BA0

5 M_A_DIM0_CKE1 74 CKE1

5 M_A_DIM0_CKE0 73 CKE0

SMBus Slave Address: A0H

1 3 RN1601A 10KOhm 2 4 RN1601B 10KOhm 201 SA1 197 SA0

5 M_A_DQS[7:0]

M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7

5 M_A_DQS#[7:0]

M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7

M_A_DQS7 188 M_A_DQS#7 186 M_A_DQS6 171 M_A_DQS#6 169 M_A_DQS5 154 M_A_DQS#5 152 M_A_DQS4 137 M_A_DQS#4 135 M_A_DQS3 64 M_A_DQS#3 62 M_A_DQS2 47 M_A_DQS#2 45 M_A_DQS1 29 M_A_DQS#1 27 M_A_DQS0 12 M_A_DQS#0 10

DM should connect to GND directly
Design Guide 0.9 p86 (436735)

187 DM7 170 DM6 153 DM5 136 DM4 63 DM3 46 DM2 28 DM1 11 DM0

17,28,31 SMB_CLK_S 202 SCL

17,28,31 SMB_DAT_S 200 SDA

RESET# 30 DDR3_DRAMRST# 5,17

J1601A

DQ0 5 M_A_DQ0 DQ1 7 M_A_DQ1 DQ2 15 M_A_DQ6 DQ3 17 M_A_DQ5 DQ4 4 M_A_DQ4 DQ5 6 M_A_DQ2 DQ6 16 M_A_DQ3 DQ7 18 M_A_DQ7 DQ8 21 M_A_DQ13 DQ9 23 M_A_DQ8 DQ10 33 M_A_DQ10 DQ11 35 M_A_DQ14 DQ12 22 M_A_DQ9 DQ13 24 M_A_DQ12 DQ14 34 M_A_DQ15 DQ15 36 M_A_DQ11 DQ16 39 M_A_DQ16 DQ17 41 M_A_DQ21 DQ18 51 M_A_DQ23 DQ19 53 M_A_DQ18 DQ20 40 M_A_DQ20 DQ21 42 M_A_DQ17 DQ22 50 M_A_DQ22 DQ23 52 M_A_DQ19 DQ24 57 M_A_DQ29 DQ25 59 M_A_DQ24 DQ26 67 M_A_DQ26 DQ27 69 M_A_DQ31 DQ28 56 M_A_DQ30 DQ29 58 M_A_DQ28 DQ30 68 M_A_DQ25 DQ31 70 M_A_DQ27 DQ32 129 M_A_DQ39 DQ33 131 M_A_DQ37 DQ34 141 M_A_DQ33 DQ35 143 M_A_DQ38 DQ36 130 M_A_DQ32 DQ37 132 M_A_DQ36 DQ38 140 M_A_DQ35 DQ39 142 M_A_DQ34 DQ40 147 M_A_DQ40 DQ41 149 M_A_DQ44 DQ42 157 M_A_DQ46 DQ43 159 M_A_DQ47 DQ44 146 M_A_DQ45 DQ45 148 M_A_DQ41 DQ46 158 M_A_DQ43 DQ47 160 M_A_DQ42 DQ48 163 M_A_DQ53 DQ49 165 M_A_DQ52 DQ50 175 M_A_DQ55 DQ51 177 M_A_DQ50 DQ52 164 M_A_DQ49 DQ53 166 M_A_DQ48 DQ54 174 M_A_DQ54 DQ55 176 M_A_DQ51 DQ56 181 M_A_DQ58 DQ57 183 M_A_DQ62 DQ58 191 M_A_DQ57 DQ59 193 M_A_DQ61 DQ60 180 M_A_DQ63 DQ61 182 M_A_DQ56 DQ62 192 M_A_DQ60 DQ63 194 M_A_DQ59

0 1 2 3 4 5 6 7

M_A_DQ[63:0] 5

DDR3_DIMM_204P

12V02GIRM001

M: 1202-000R000

S: 1202-00K7000

S: 1202-00LP000

+1.5V

C1605 0.1UF/16V

C1606 0.1UF/16V

C1607 0.1UF/16V

C1608 0.1UF/16V

Layout Note: Place these caps near SO DIMM 0

J1601B

VDD1 75 VDD2 76 VDD3 81 VDD4 82 VDD5 87 VDD6 88 VDD7 93 VDD8 94 VDD9 99 VDD10 100 VDD11 105 VDD12 106 VDD13 111 VDD14 112 VDD15 117 VDD16 118 VDD17 123 VDD18 124

VSS1 2 VSS2 3 VSS3 8 VSS4 9 VSS5 13 VSS6 14 VSS7 19 VSS8 20 VSS9 25 VSS10 26 VSS11 31 VSS12 32 VSS13 37 VSS14 38 VSS15 43 VSS16 44 VSS17 48 VSS18 49 VSS19 54 VSS20 55 VSS21 60 VSS22 61 VSS23 65 VSS24 66 VSS25 71 VSS26 72 VSS27 127 VSS28 128 VSS29 133 VSS30 134 VSS31 138 VSS32 139 VSS33 144 VSS34 145 VSS35 150 VSS36 151 VSS37 155 VSS38 156 VSS39 161 VSS40 162 VSS41 167 VSS42 168 VSS43 172 VSS44 173 VSS45 178 VSS46 179 VSS47 184 VSS48 185 VSS49 189 VSS50 190 VSS51 195 VSS52 196

GND1 207 GND2 208

T1601 1 PM_EXTTS#0_DIM_A

Reserve

EVENT# 198 TEST 125

NC1 77 NC2 122

NP_NC1 205 NP_NC2 206

VTT1 203 VTT2 204

VREFCA 126 VREFDQ 1

VDDSPD 199

DDR3_DIMM_204P

12V02GIRM001

MAX: 0.75A

TDC: 0.75A

+0.75VS

+3VS

+V_VREF_CA_DIMM0

W/S=20/20

C1624 2.2UF/6.3V @

C1623 0.1UF/16V

+V_VREF_DQ_DIMM0

W/S=20/20

C1622 2.2UF/6.3V @

C1625 0.1UF/16V

C1615 0.1UF/16V

C1614 2.2UF/6.3V @

PEGATRON	Title : DDR3(1)_SO-DIMM0		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 16 of 104		

+1.5V → +1.5V 4,5,7,16,18,57,83

+0.75VS → +0.75VS 16,57,83

+3VS → +3VS 3,4,16,20,21,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92

+V_VREF_CA_DIMM0 → +V_VREF_CA_DIMM0 16,18

+V_VREF_DQ_DIMM0 → +V_VREF_DQ_DIMM0 16,18

Layout Note: Place these caps near SO DIMM 1

+1.5V

@ CE1701 330UF/2.5V

1BV080000031

C1709 22UF/6.3V, C1710 22UF/6.3V, C1711 22UF/6.3V, C1712 22UF/6.3V @, C1713 22UF/6.3V @, C1726 22UF/6.3V @

+0.75VS

C1716 1UF/6.3V, C1717 1UF/6.3V, C1718 1UF/6.3V @, C1719 1UF/6.3V @

M_B_DIM0_CLK_DDR0 → C1720 10PF/50V @ → 1% 150Ohm R1707 @ → M_B_DIM0_CLK_DDR#0

M_B_DIM0_CLK_DDR1 → C1721 10PF/50V @ → 1% 150Ohm R1708 @ → M_B_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

H4.0mm,STD

5 M_B_A[15:0]

J1701A

M_B_A0 98 A0, M_B_A1 97 A1, M_B_A2 96 A2, M_B_A3 95 A3, M_B_A4 92 A4, M_B_A5 91 A5, M_B_A6 90 A6, M_B_A7 86 A7, M_B_A8 89 A8, M_B_A9 85 A9, M_B_A10 107 A10/AP, M_B_A11 84 A11, M_B_A12 83 A12/BC#, M_B_A13 119 A13, M_B_A14 80 A14, M_B_A15 78 A15

5 M_B_DIM0_CLK_DDR1 → 102 CK1, 104 CK1#

5 M_B_DIM0_CLK_DDR#1 → 101 CK0, 103 CK0#

5 M_B_DIM0_CLK_DDR#0

5 M_B_DIM0_CS#1 → 121 S1#

5 M_B_DIM0_CS#0 → 114 S0#

5 M_B_DIM0_ODT1 → 120 ODT1

5 M_B_DIM0_ODT0 → 116 ODT0

5 M_B_WE# → 113 WE#

5 M_B_RAS# → 110 RAS#

5 M_B_CAS# → 115 CAS#

5 M_B_BS2 → 79 BA2

5 M_B_BS1 → 108 BA1

5 M_B_BS0 → 109 BA0

5 M_B_DIM0_CKE1 → 74 CKE1

5 M_B_DIM0_CKE0 → 73 CKE0

SMBus Slave Address: A4H

+3VS → RN1701A 1 2 10KOhm 201 SA1; RN1701B 3 4 10KOhm 197 SA0

5 M_B_DQS[7:0]

M_B_DQS0, M_B_DQS1, M_B_DQS2, M_B_DQS3, M_B_DQS4, M_B_DQS5, M_B_DQS6, M_B_DQS7

5 M_B_DQS#[7:0]

M_B_DQS#0, M_B_DQS#1, M_B_DQS#2, M_B_DQS#3, M_B_DQS#4, M_B_DQS#5, M_B_DQS#6, M_B_DQS#7

M_B_DQS7 188 DQS7, M_B_DQS#7 186 DQS#7, M_B_DQS6 171 DQS6, M_B_DQS#6 169 DQS#6, M_B_DQS5 154 DQS5, M_B_DQS#5 152 DQS#5, M_B_DQS4 137 DQS4, M_B_DQS#4 135 DQS#4, M_B_DQS3 64 DQS3, M_B_DQS#3 62 DQS#3, M_B_DQS2 47 DQS2, M_B_DQS#2 45 DQS#2, M_B_DQS1 29 DQS1, M_B_DQS#1 27 DQS#1, M_B_DQS0 12 DQS0, M_B_DQS#0 10 DQS#0

DM should connect to GND directly
Design Guide 0.9 p86 (436735)

M_B_DM7 187 DM7, M_B_DM6 153 DM6, M_B_DM5 136 DM5, M_B_DM4 63 DM4, M_B_DM3 46 DM3, M_B_DM2 28 DM2, M_B_DM1 11 DM1, M_B_DM0 DM0

16,28,31 SMB_CLK_S → 202 SCL

16,28,31 SMB_DAT_S → 200 SDA

RESET# 30 → DDR3_DRAMRST# 5,16

DDR3_DIMM_204P

12V02GISM001

M: 1202-00HK000

S: 1202-00K4000

S: 1202-00LU000

5 M_B_DQ[63:0]

DQ0 7 M_B_DQ0, DQ1 15 M_B_DQ4, DQ2 17 M_B_DQ2, DQ3 4 M_B_DQ6, DQ4 6 M_B_DQ5, DQ5 16 M_B_DQ1, DQ6 18 M_B_DQ3, DQ7 21 M_B_DQ7, DQ8 23 M_B_DQ12, DQ9 33 M_B_DQ8, DQ10 35 M_B_DQ10, DQ11 22 M_B_DQ14, DQ12 24 M_B_DQ13, DQ13 34 M_B_DQ9, DQ14 36 M_B_DQ11, DQ15 39 M_B_DQ15, DQ16 41 M_B_DQ20, DQ17 51 M_B_DQ16, DQ18 53 M_B_DQ18, DQ19 40 M_B_DQ19, DQ20 42 M_B_DQ22, DQ21 50 M_B_DQ23, DQ22 52 M_B_DQ17, DQ23 57 M_B_DQ21, DQ24 59 M_B_DQ28, DQ25 67 M_B_DQ29, DQ26 69 M_B_DQ26, DQ27 56 M_B_DQ30, DQ28 58 M_B_DQ24, DQ29 68 M_B_DQ25, DQ30 70 M_B_DQ27, DQ31 129 M_B_DQ31, DQ32 131 M_B_DQ37, DQ33 141 M_B_DQ33, DQ34 143 M_B_DQ39, DQ35 130 M_B_DQ35, DQ36 132 M_B_DQ32, DQ37 140 M_B_DQ36, DQ38 142 M_B_DQ34, DQ39 147 M_B_DQ38, DQ40 149 M_B_DQ41, DQ41 157 M_B_DQ42, DQ42 159 M_B_DQ46, DQ43 146 M_B_DQ45, DQ44 148 M_B_DQ44, DQ45 158 M_B_DQ40, DQ46 160 M_B_DQ47, DQ47 163 M_B_DQ43, DQ48 165 M_B_DQ51, DQ49 175 M_B_DQ50, DQ50 177 M_B_DQ53, DQ51 164 M_B_DQ52, DQ52 166 M_B_DQ54, DQ53 174 M_B_DQ55, DQ54 176 M_B_DQ48, DQ55 181 M_B_DQ49, DQ56 183 M_B_DQ60, DQ57 191 M_B_DQ63, DQ58 193 M_B_DQ58, DQ59 180 M_B_DQ62, DQ60 182 M_B_DQ57, DQ61 192 M_B_DQ61, DQ62 194 M_B_DQ59, DQ63 M_B_DQ56

Layout Note: Place these caps near SO DIMM 1

+1.5V

C1705 0.1UF/16V, C1706 0.1UF/16V

+1.5V

C1707 0.1UF/16V, C1708 0.1UF/16V

J1701B

VDD1 75, VDD3 81, VDD5 87, VDD7 93, VDD9 99, VDD11 105, VDD13 111, VDD15 117, VDD17 123

VDD2 76, VDD4 82, VDD6 88, VDD8 94, VDD10 100, VDD12 106, VDD14 112, VDD16 118, VDD18 124

VSS1 2, VSS3 8, VSS5 13, VSS7 19, VSS9 25, VSS11 31, VSS13 37, VSS15 43, VSS17 48, VSS19 54, VSS21 60, VSS23 65, VSS25 71, VSS27 127, VSS29 133, VSS31 138, VSS33 144, VSS35 150, VSS37 155, VSS39 161, VSS41 167, VSS43 172, VSS45 178, VSS47 184, VSS49 189, VSS51 195

VSS2 3, VSS4 9, VSS6 14, VSS8 20, VSS10 26, VSS12 32, VSS14 38, VSS16 44, VSS18 49, VSS20 55, VSS22 61, VSS24 66, VSS26 72, VSS28 128, VSS30 134, VSS32 139, VSS34 145, VSS36 151, VSS38 156, VSS40 162, VSS42 168, VSS44 173, VSS46 179, VSS48 185, VSS50 190, VSS52 196

GND1 207, GND2 208

T1701 1 PM_EXTTS#0_DIM_B

Reserve

EVENT# 198, TEST 125

NC1 77, NC2 122

NP_NC1 205, NP_NC2 206

VTT1 203, VTT2 204 → +0.75VS

VREFCA 126, VREFDQ 1

VDDSPD 199

+3VS

C1715 0.1UF/16V, C1714 2.2UF/6.3V @

+V_VREF_CA_DIMM1

W/S=20/20

C1724 2.2UF/6.3V @, C1723 0.1UF/16V

+V_VREF_DQ_DIMM1

W/S=20/20

C1722 2.2UF/6.3V @, C1725 0.1UF/16V

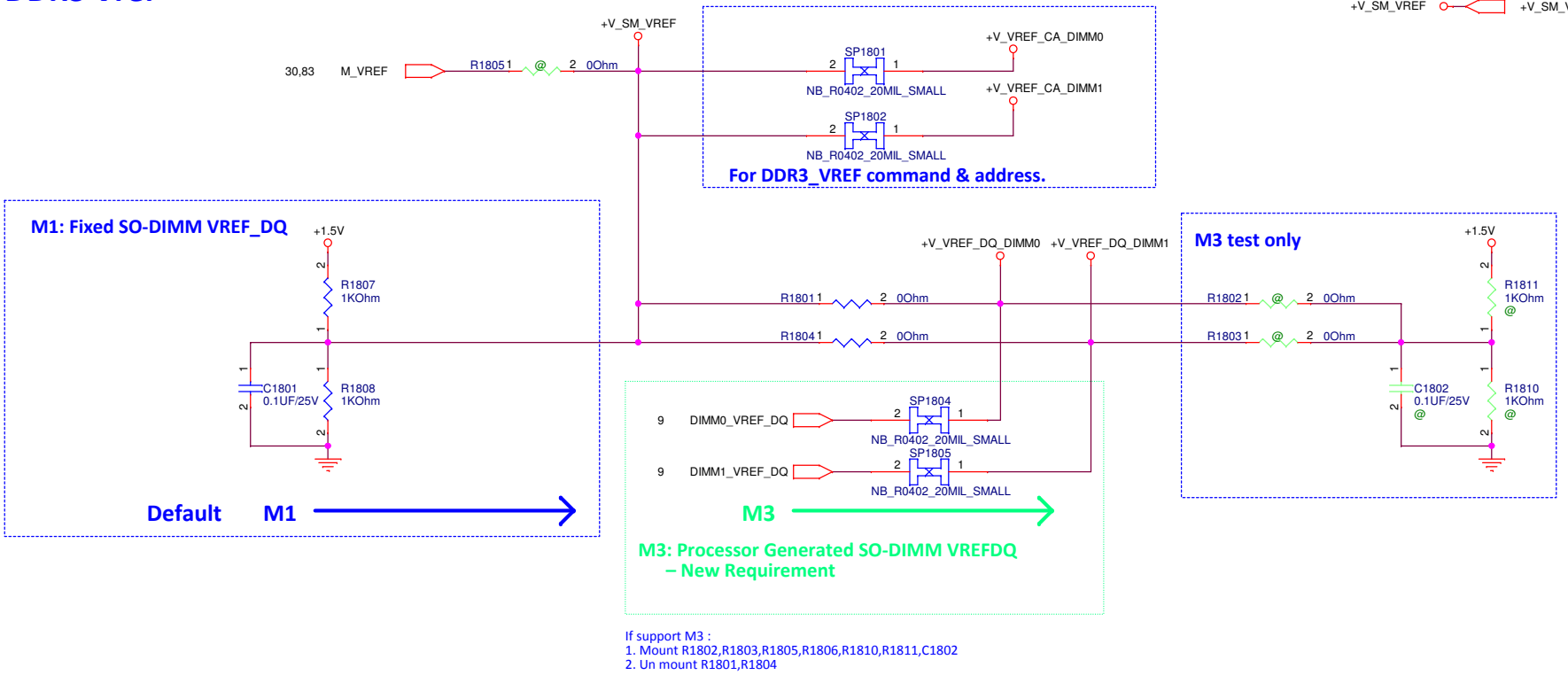
DDR3_DIMM_204P

12V02GISM001

PEGATRON	Title : DDR3(2)_SO-DIMM1		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 17 of 104		

DDR3 Vref

+V_VREF_CA_DIMM0 → +V_VREF_CA_DIMM0 16
+V_VREF_DQ_DIMM0 → +V_VREF_DQ_DIMM0 16
+V_VREF_CA_DIMM1 → +V_VREF_CA_DIMM1 17
+V_VREF_DQ_DIMM1 → +V_VREF_DQ_DIMM1 17
+V_SM_VREF → +V_SM_VREF 7



If support M3 :
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

PEGATRON	Title : DDR3(3)_CA/DQ Voltage	
BG1-CSC-HW R&D Dept.5	Engineer:	
Size: B	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 18 of 104	

RTC battery

+RTCBAT — R2001 2 — 1 1KOhm +RTC_BAT — 2 — D2001 (+3VA / +VCC_RTC, 0.8V/0.2mA, 07V030000001) — C2003 1UF/6.3V — GND

J2001 BATT_HOLDER_2P 12V20GBSM000

M: 1220-001O000
S: 1220-00F2000
S :1220-00HD000

Request by CSC for CMOS clear function

CMOS Settings	JRST2001	TPM Settings	JRST2002
Clear CMOS	Shunt	Clear ME RTC Registers	Shunt
Keep CMOS	Open	Keep ME RTC Registers	Open

+VCC_RTC — +VCC_RTC 22,27
+3VA — +3VA 6,30,33,37,57,60,65,81,88,93
+3VS — +3VS 3,4,16,17,21,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+3VSUS_ORG — +3VSUS_ORG 21,22,24,25,27
+VTT_PCH_VCCIO — +VTT_PCH_VCCIO 26,27
+5VS — +5VS 27,30,31,36,37,46,48,50,51,56,57,58,62,66,80,87,91

+VCC_RTC — RTCRST# RC delay should be 18ms~25ms — R2003 20KOhm — C2004 1UF/6.3V — JRST2001 SGL_JUMP — GND

R1.1 2012/11/30 delete

EC reset CMOS feature

+VCC_RTC — R2004 20KOhm — R2005 1MOhm — C2005 1UF/6.3V — JRST2002 SGL_JUMP — GND

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN — R2030 1% 330KOhm — GND

+5VS — reserved for leakage — Q2010 2N7002 — R2012 0Ohm — R2011 1MOhm 0V240000006 — GND

36 ACZ_SYNC_AUD — R2009 33Ohm — ACZ_SYNC_C — ACZ_SYNC

GPIO13 — R2028 10KOhm — +3VSUS_ORG

XDP reserved

PCH_JTAG_TMS — R2040 220Ohm
PCH_JTAG_TDO — R2038 220Ohm
PCH_JTAG_TDI — R2039 220Ohm
R2041 100Ohm
R2042 100Ohm
R2043 100Ohm
PCH_JTAG_TCK_BUF — R2044 51Ohm
+3VSUS_ORG — GND

Strap information:

SB_SPKR: No reboot strap
Low: Disable
High:Enable
SB_SPKR — R2020 1KOhm — +3VS

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUT which sample high on the rising edge of PWROK will also disable Intel ME.
ACZ_SDOUT — R2034 1KOhm — +3VSUS_ORG

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V
High: 1.5V
note :
CRB has no strap
Hrron River Platform Schematic Design Checklist(438390 page 48)
ACZ_SYNC — R2036 1KOhm — +3VSUS_ORG

VCCVRAM use +1.5VS in mobile

C2001 18PF/50V — RTC_X1 — Xtal Spec:NC — X2001 32.768KHZ — R2002 10MOhm — C2002 18PF/50V — RTC_X2_C — SP2005 NB_R0402_20MIL_SMALL — RTC_X2 — GND

U2001A — COUGAR_POINT_ES1

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
SRTC_RST# — R2035 33Ohm ACZ_BCLK — ACZ_SYNC — R2052 33Ohm ACZ_RST# — R2055 33Ohm ACZ_SDOUT
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5
SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5; SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10; SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4; SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1; SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1
SATAICOMPO Y11, SATAICOMPI Y10 — SATA_COMP — R2007 1% 35.7OHM — +VTT_PCH_VCCIO
SATA3RCOMPO AB12, SATA3COMPI AB13 — SATA3_COMP — R2047 1% 42.2Ohm — +VTT_PCH_VCCIO
SATA3RBIAS AH1 — RBIAS_SATA3 — R2048 1% 750Ohm — GND
SATALED# P3 — SATALED# — R2025 10KOhm — +3VS
SATA0GP/GPIO21 V14 — PCB_ID8 — PCB_ID8 25
SATA1GP/GPIO19 P1 — BBS_BIT0_R — SP2003 NB_R0402_20MIL_SMALL — BBS_BIT0 24

LPC_AD0 30,44
LPC_AD1 30,44
LPC_AD2 30,44
LPC_AD3 30,44
LPC_FRAME# 30,44
SNN_PCH_DRQ#0 — T2024
GPIO23 — T2023
INT_SERIRQ 30,44

SATA_RXN0 51 — SATA_RXP0 51 — SATA_TXN0 51 — SATA_TXP0 51 — **0.HDD**
SATA_RXN2 51 — SATA_RXP2 51 — SATA_TXN2 51 — SATA_TXP2 51 — **2.ODD**

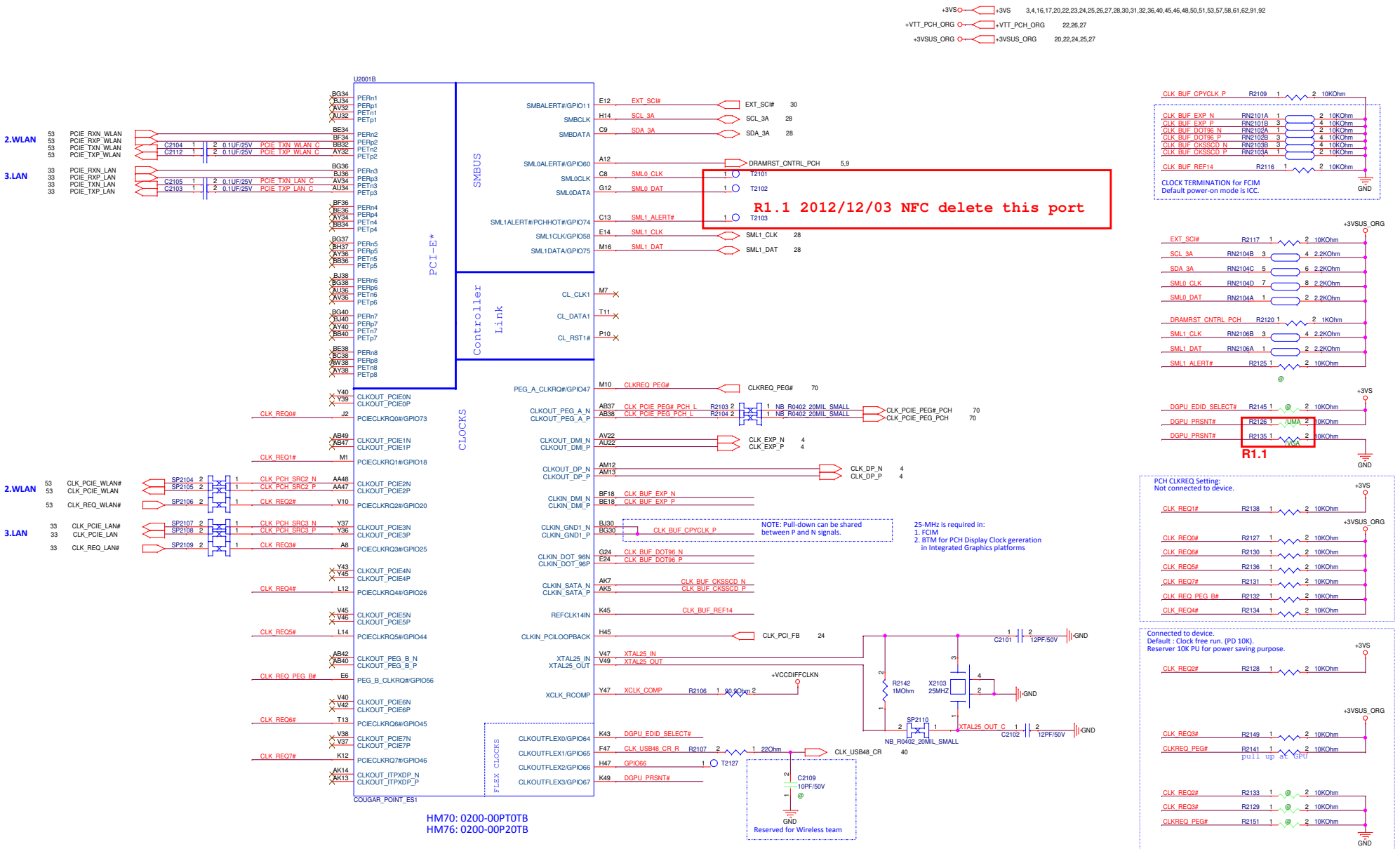
R1.1

Pull High — +3VS — INT_SERIRQ — R2026 10KOhm

PCH_FLASH_DESCRIPTOR — SP2006 NB_R0402_20MIL_SMALL
ACZ_SDOUT_AUD — R2055 33Ohm — ACZ_SDOUT
T2003 — HDA_DOCK_EN# — GPIO13
PCH_JTAG_TCK_BUF — PCH_JTAG_TMS — PCH_JTAG_TDI — PCH_JTAG_TDO
SPI_CLK 28,30 — SPI_CS0# 28 — SPI_CS1# 28,30 — SPI_SI 28,30 — SPI_SO 28,30

HM70: 0200-00PT0TB
HM76: 0200-00P20TB

PEGATRON	Title : PCH(1)_SATA,HDA,RTC,LPC		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 20 of 104		


+3VS +3VS 3,4,16,17,20,22,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS_ORG +3VSUS_ORG 20,22,24,25,27
U2001B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR_POINT_ES1
2.WLAN
3.LAN
PCIE_RXN_WLAN
PCIE_RXP_WLAN
PCIE_TXN_WLAN
PCIE_TXP_WLAN
PCIE_RXN_LAN
PCIE_RXP_LAN
PCIE_TXN_LAN
PCIE_TXP_LAN
0.1UF/25V
PCIE_TXN_WLAN_C
PCIE_TXP_WLAN_C
PCIE_TXN_LAN_C
PCIE_TXP_LAN_C
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
EXT_SCI#
SCL_3A
SDA_3A
DRAMRST_CNTRL_PCH
SML0_CLK
SML0_DAT
SML1_ALERT#
SML1_CLK
SML1_DAT
T2101
T2102
T2103
R1.1 2012/12/03 NFC delete this port
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
CLKREQ_PEG#
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLK_PCIE_PEG# PCH_L
CLK_PCIE_PEG_PCH_L
NB_R0402_20MIL_SMALL
CLK_PCIE_PEG# PCH
CLK_PCIE_PEG_PCH
CLKOUT_DMI_N
CLKOUT_DMI_P
CLK_EXP_N
CLK_EXP_P
CLKOUT_DP_N
CLKOUT_DP_P
CLK_DP_N
CLK_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLK_BUF_EXP_N
CLK_BUF_EXP_P
CLKIN_GND1_N
CLKIN_GND1_P
CLK_BUF_CPYCLK_P
NOTE: Pull-down can be shared between P and N signals.
25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration in Integrated Graphics platforms
CLKIN_DOT_96N
CLKIN_DOT_96P
CLK_BUF_DOT96_N
CLK_BUF_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
CLK_BUF_CKSSCD_N
CLK_BUF_CKSSCD_P
REFCLK14IN
CLK_BUF_REF14
CLKIN_PCILOOPBACK
CLK_PCI_FB
XTAL25_IN
XTAL25_OUT
+VCCDIFFCLKN
XCLK_RCOMP
XCLK_COMP
R2106 90.9Ohm
R2142 1MOhm
X2103 25MHZ
SP2110
C2101 12PF/50V
C2102 12PF/50V
XTAL25_OUT_C
NB_R0402_20MIL_SMALL
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
DGPU_EDID_SELECT#
CLK_USB48_CR_R
R2107 22Ohm
CLK_USB48_CR
DGPU_PRSNT#
T2127
C2109 10PF/50V
Reserved for Wireless team
CLK_REQ0#
CLK_REQ1#
CLK_REQ2#
CLK_REQ3#
CLK_REQ4#
CLK_REQ5#
CLK_REQ_PEG_B#
CLK_REQ6#
CLK_REQ7#
PCIECLKRQ0#/GPIO73
PCIECLKRQ1#/GPIO18
PCIECLKRQ2#/GPIO20
PCIECLKRQ3#/GPIO25
PCIECLKRQ4#/GPIO26
PCIECLKRQ5#/GPIO44
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
CLK_PCIE_WLAN#
CLK_PCIE_WLAN
CLK_REQ_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_LAN
CLK_REQ_LAN#
CLK_PCH_SRC2_N
CLK_PCH_SRC2_P
CLK_PCH_SRC3_N
CLK_PCH_SRC3_P
SP2104
SP2105
SP2106
SP2107
SP2108
SP2109
HM70: 0200-00PT0TB
HM76: 0200-00P20TB
CLK_BUF_CPYCLK_P R2109 10KOhm
CLK_BUF_EXP_N RN2101A
CLK_BUF_EXP_P RN2101B
CLK_BUF_DOT96_N RN2102A
CLK_BUF_DOT96_P RN2102B
CLK_BUF_CKSSCD_N RN2103B
CLK_BUF_CKSSCD_P RN2103A
CLK_BUF_REF14 R2116 10KOhm
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.
GND
+3VSUS_ORG
EXT_SCI# R2117 10KOhm
SCL_3A RN2104B 2.2KOhm
SDA_3A RN2104C 2.2KOhm
SML0_CLK RN2104D 2.2KOhm
SML0_DAT RN2104A 2.2KOhm
DRAMRST_CNTRL_PCH R2120 1KOhm
SML1_CLK RN2106B 2.2KOhm
SML1_DAT RN2106A 2.2KOhm
SML1_ALERT# R2125 10KOhm
+3VS
DGPU_EDID_SELECT# R2145 10KOhm
DGPU_PRSNT# R2126 10KOhm UMA
DGPU_PRSNT# R2135 10KOhm VGA
R1.1
PCH CLKREQ Setting:
Not connected to device.
CLK_REQ1# R2138 10KOhm
CLK_REQ0# R2127 10KOhm
CLK_REQ6# R2130 10KOhm
CLK_REQ5# R2136 10KOhm
CLK_REQ7# R2131 10KOhm
CLK_REQ_PEG_B# R2132 10KOhm
CLK_REQ4# R2134 10KOhm
Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
CLK_REQ2# R2128 10KOhm
CLK_REQ3# R2149 10KOhm
CLKREQ_PEG# R2141 10KOhm
pull up at GPU
CLK_REQ2# R2133 10KOhm
CLK_REQ3# R2129 10KOhm
CLKREQ_PEG# R2151 10KOhm
PEGATRON
Title : PCH(2)_PCIE,CLK,SMB,PEG
BG1-CSC-HW R&D Dept.5
Engineer: Jim3_Liu
Size C
Project Name VGFTG
Rev 1.1
Date: Tuesday, December 11, 2012
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+3VSUS_ORG — +3VSUS_ORG 20,21,24,25,27
+3VS — +3VS 3,4,16,17,20,21,23,24,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+VTT_PCH_ORG — +VTT_PCH_ORG 26,27
+3VA — +3VA 6,20,30,33,37,57,60,65,81,88,93
+VCC_RTC — +VCC_RTC 20,27
+3VSUS — +3VSUS 24,27,28,30,33,34,37,53,62,81,92
+5VSUS — +5VSUS 27,51,52,62,81,82
+12VSUS — +12VSUS 33,36,51,81,91

U2001C

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 — BC24 BE20 BG18 BG20 — DMI0RXN DMI1RXN DMI2RXN DMI3RXN
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 — BE24 BC20 BJ18 BJ20 — DMI0RXP DMI1RXP DMI2RXP DMI3RXP
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 — AW24 AW20 BB18 AV18 — DMI0TXN DMI1TXN DMI2TXN DMI3TXN
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 — AY24 AY20 AY18 AU18 — DMI0TXP DMI1TXP DMI2TXP DMI3TXP

+VTT_PCH_ORG — R2201 2 1% 1 49.9Ohm — DMI_COMP_R — BJ24 DMI_ZCOMP
GND — R2202 2 1% 1 750Ohm — RBIAS_CPY — BG25 DMI_IRCOMP — BH21 DMI2RBIAS

DMI

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7 — BJ14 AY14 BE14 BH13 BC12 BJ12 BG10 BG9 — FDI_TXN0 FDI_TXN1 FDI_TXN2 FDI_TXN3 FDI_TXN4 FDI_TXN5 FDI_TXN6 FDI_TXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7 — BG14 BB14 BF14 BG13 BE12 BG12 BJ10 BH9 — FDI_TXP0 FDI_TXP1 FDI_TXP2 FDI_TXP3 FDI_TXP4 FDI_TXP5 FDI_TXP6 FDI_TXP7
FDI_INT — AW16 — FDI_INT
FDI_FSYNC0 — AV12 — FDI_FSYNC0
FDI_FSYNC1 — BC10 — FDI_FSYNC1
FDI_LSYNC0 — AV14 — FDI_LSYNC0
FDI_LSYNC1 — BB10 — FDI_LSYNC1

FDI

DSWVRMEN — A18 — DSWODVREN — R2215 1 @ 2 330KOhm, R2214 1 2 330KOhm — GND, VCC_RTC

DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled

ME_SUSPWRDNACK — SP2203 2 1 NB_R0402_20MIL_SMALL — T2206 1 — SUSACK# — C12 SUSACK#
+3VS — R2205 2 10KOhm 1 — PM_SYSRST# — K3 SYS_RESET#
D2201 1 @ 2 1.2V/0.1A
SYS_PWROK — P12 SYS_PWROK
4,30,92 PM_PWROK — SP2212 2 1 NB_R0402_20MIL_SMALL — PM_PCH_PWROK_R — L22 PWROK
SP2201 2 1 NB_R0402_20MIL_SMALL
non-iAMT:connected to PWROK. — PM_APWROK_R — L10 APWROK
4 PM_DRAM_PWRGD — B13 DRAMPWROK
PM_RSMRST# has PD 10k ohm in EC — 30 PM_RSMRST# — SP2213 2 1 NB_R0402_20MIL_SMALL — PM_RSMRST_R — C21 RSMRST#
30 ME_SUSPWRDNACK — K16 SUSWARN#/SUSPWRDNACK/GPIO30
30 PM_PWRBTN# — SP2214 2 1 NB_R0402_20MIL_SMALL — E20 PWRBTN#
30 ME_AC_PRESENT — H20 ACPRESENT/GPIO31
T2201 1 — BATLOW# — E10 BATLOW#/GPIO72
T2202 1 — RI# — A10 RI#

System Power Management

CLKRUN#/GPIO32 — N3 — PM_CLKRUN# — 30
SUS_STAT#/GPIO61 — G8 — PM_SUS_STAT# — T2203 1
SUSCLK/GPIO62 — N14 — SUSCLK_C — T2207 1
SLP_S5#/GPIO63 — D10 — SLP_S5# — T2204 1
SLP_S4# — H4 — PM_SUSC# — 30
SLP_S3# — F4 — PM_SUSB# — 30
SLP_A# — G10 — ME_PM_SLP_M# — NC when non-iAMT
SLP_SUS# — G16 — SLP_SUS# — T2205 1
PMSYNCH — AP14 — H_PM_SYNC — 4
SLP_LAN#/GPIO29 — K14 — GPIO29 — NC when non-intel LAN

DPWROK — E22 — SP2202 2 1 — PM_RSMRST_R
NB_R0402_20MIL_SMALL
WAKE# — B9 — PCIE_WAKE# — 33,53

COUGAR_POINT_ES1

PANTHERPOINT
HM70: 0200-00PT0TB
HM76: 0200-00P20TB

+3VSUS_ORG
RI# — R2223 1 2 10KOhm
BATLOW# — R2224 1 2 10KOhm
PCIE_WAKE# — R2225 1 2 1KOhm
ME_PM_SLP_M# — R2226 1 @ 2 10KOhm
ME_SUSPWRDNACK — R2227 1 2 10KOhm
ME_AC_PRESENT — R2228 1 2 10KOhm
GPIO29 — R2229 1 @ 2 10KOhm

+3VS
PM_CLKRUN# — R2220 1 2 10KOhm
PM_PWROK — R2221 1 2 10KOhm
GND

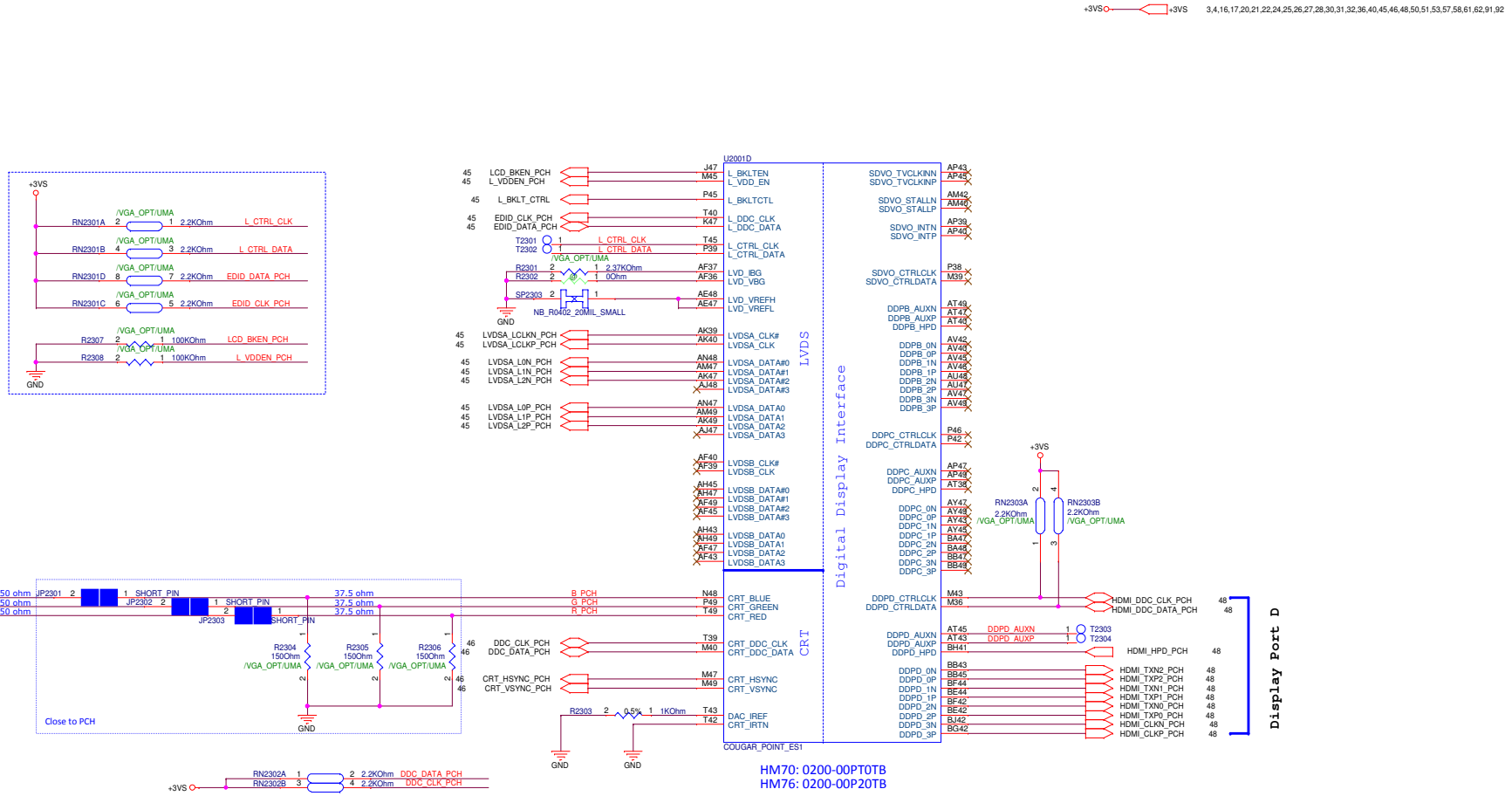
SYS_PWROK for PCH

92 DELAY_VR_AND_ALL_SYS — U2201 A 1, B 2, GND 3, VCC 5, Y 4 — SYS_PWROK
PM_PWROK — 1
+3VSUS
Vcc=2~5.5

Add for S3 power reduce

+3VSUS — R2230 10KOhm @
+5VSUS — R2232 10KOhm @
+12VSUS — R2231 100KOhm 1% @ — PS_S3CNTRL_1.5V
Q2203B UM6K1N @
GND
24,30,36,57,91,92 SUSB_EC# — SP2211 2 1 NB_R0402_20MIL_SMALL — Q2203A UM6K1N @
PM_SUSB# R2241 2 @ 1 0Ohm
GND

PEGATRON Title : PCH(3)_FDI,DMI,SYS PWR
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size C | Project Name VGFTG | Rev 1.1
Date: Tuesday, December 11, 2012 | Sheet 22 of 104



CRT Disable: (For discrete graphic)

1. NC:

CRT_RED,CRT_GREEN,CRT_BLUE

CRT_HSYCN,CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:

ALL

LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],

LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],

LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#

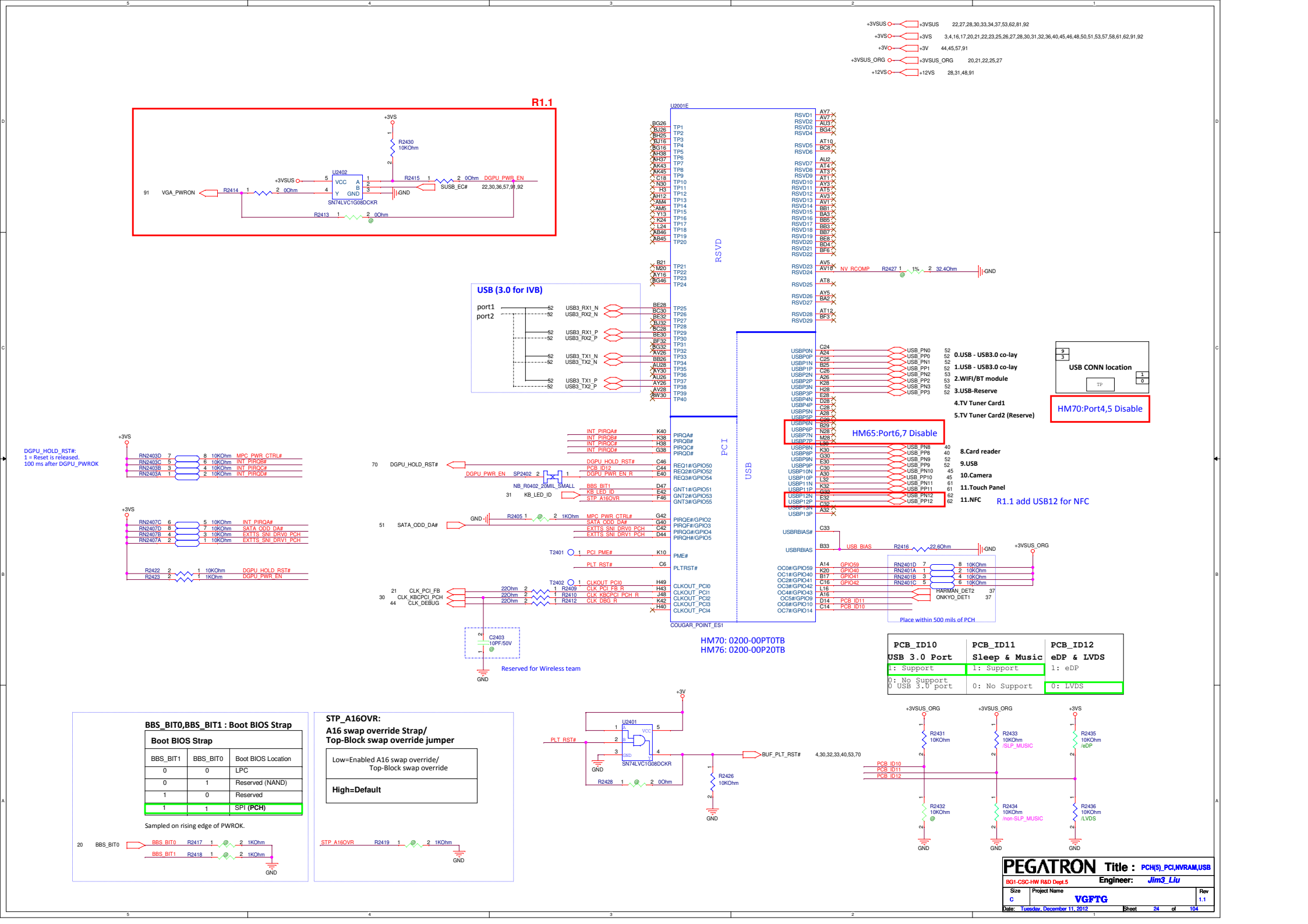
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH

LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

VccALVDS,VccTX_LVDS

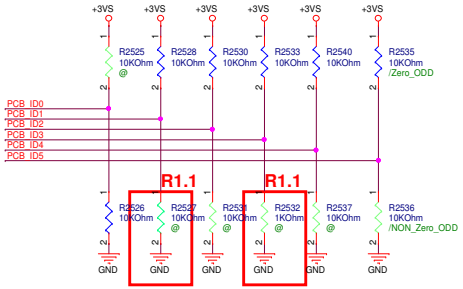
PEGATRON	Title : PCH(4)_DP,LVDS,CRT		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 23 of 104		


R1.1
U2001E
RSVD
USB (3.0 for IVB)
port1
port2
USB
PCI
COUGAR_POINT_ES1
USB CONN location
HM70:Port4,5 Disable
HM65:Port6,7 Disable
0.USB - USB3.0 co-lay
1.USB - USB3.0 co-lay
2.WIFI/BT module
3.USB-Reserve
4.TV Tuner Card1
5.TV Tuner Card2 (Reserve)
8.Card reader
9.USB
10.Camera
11.Touch Panel
11.NFC
R1.1 add USB12 for NFC
DGPU_HOLD_RST#:
1 = Reset is released.
100 ms after DGPU_PWROK
HM70: 0200-00PT0TB
HM76: 0200-00P20TB
Reserved for Wireless team
Place within 500 mils of PCH
PCB_ID10 USB 3.0 Port
PCB_ID11 Sleep & Music
PCB_ID12 eDP & LVDS
1: Support
0: No Support
0 USB 3.0 port
1: eDP
0: LVDS
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT1 BBS_BIT0 Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 Reserved
1 1 SPI (PCH)
Sampled on rising edge of PWROK.
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
Low=Enabled A16 swap override/
Top-Block swap override
High=Default
PEGATRON
Title : PCH(5)_PCI,NVRAM,USB
BG1-CSC-HW R&D Dept.5
Engineer: Jim3_Liu
Size C
Project Name VGFTG
Rev 1.1
Date: Tuesday, December 11, 2012
Sheet 24 of 104

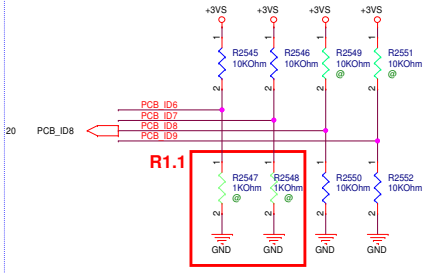
BIOS Rev. SKU

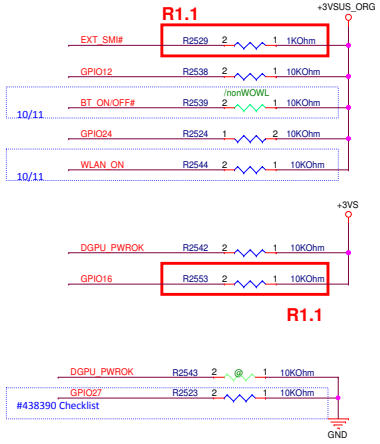
ID0	ID1	PCB Rev.
0	0	R1.0
0	1	R1.1
1	0	R2.0
1	1	R2.1

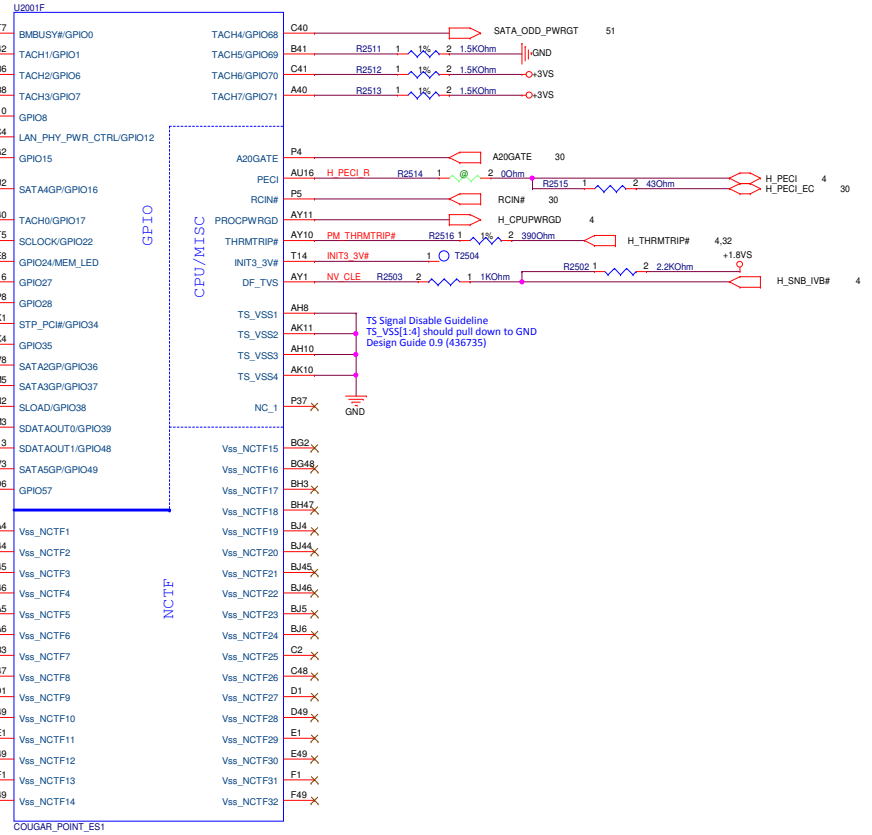
PCB_ID2	PCB_ID3 USB 3.0	PCB_ID4	PCB_ID5
1: HDMI	1: 2 port 1 port support Sleep & Charge	1:OPT/UMA	1:Zero_ODD
0:non-HDMI	0: 1 port	0:DSC	0:NON_Zero_ODD



PCB_ID6	PCB_ID7	PCB_ID8 PCB_ID9
1: Standard	1: Premium	0 0: 17W
		0 1: 35W
0: Entry	0: Mainstream	1 0: 45W
		1 1: Reserve

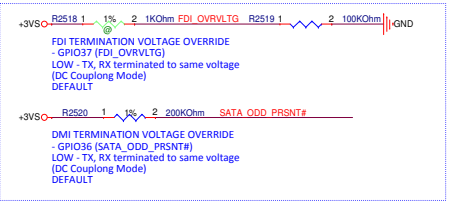


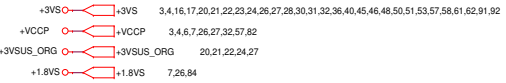




HM70: 0200-00PT0TB
HM76: 0200-00P20TB

Clear password for TODs required
Place ONTO D-part

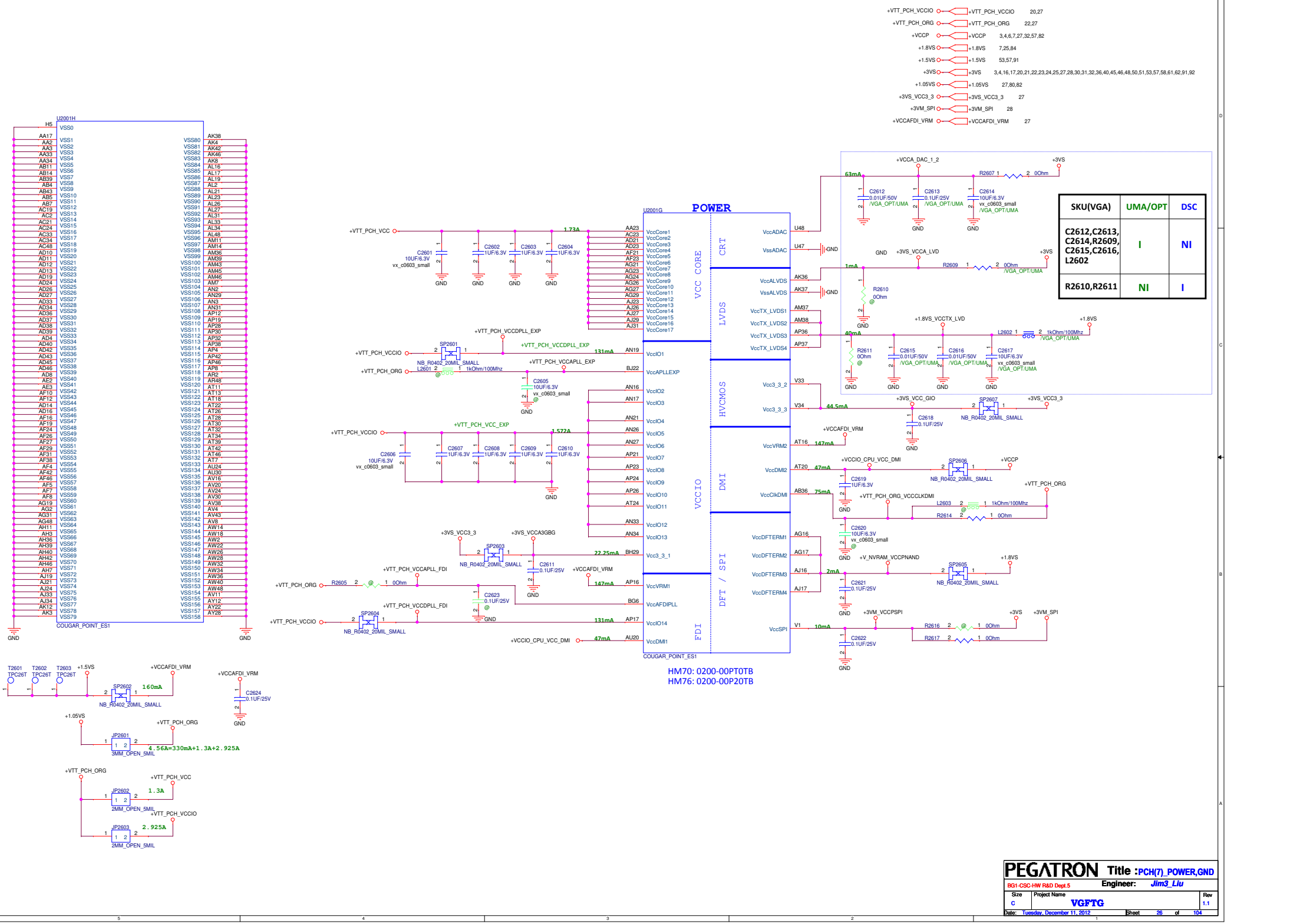


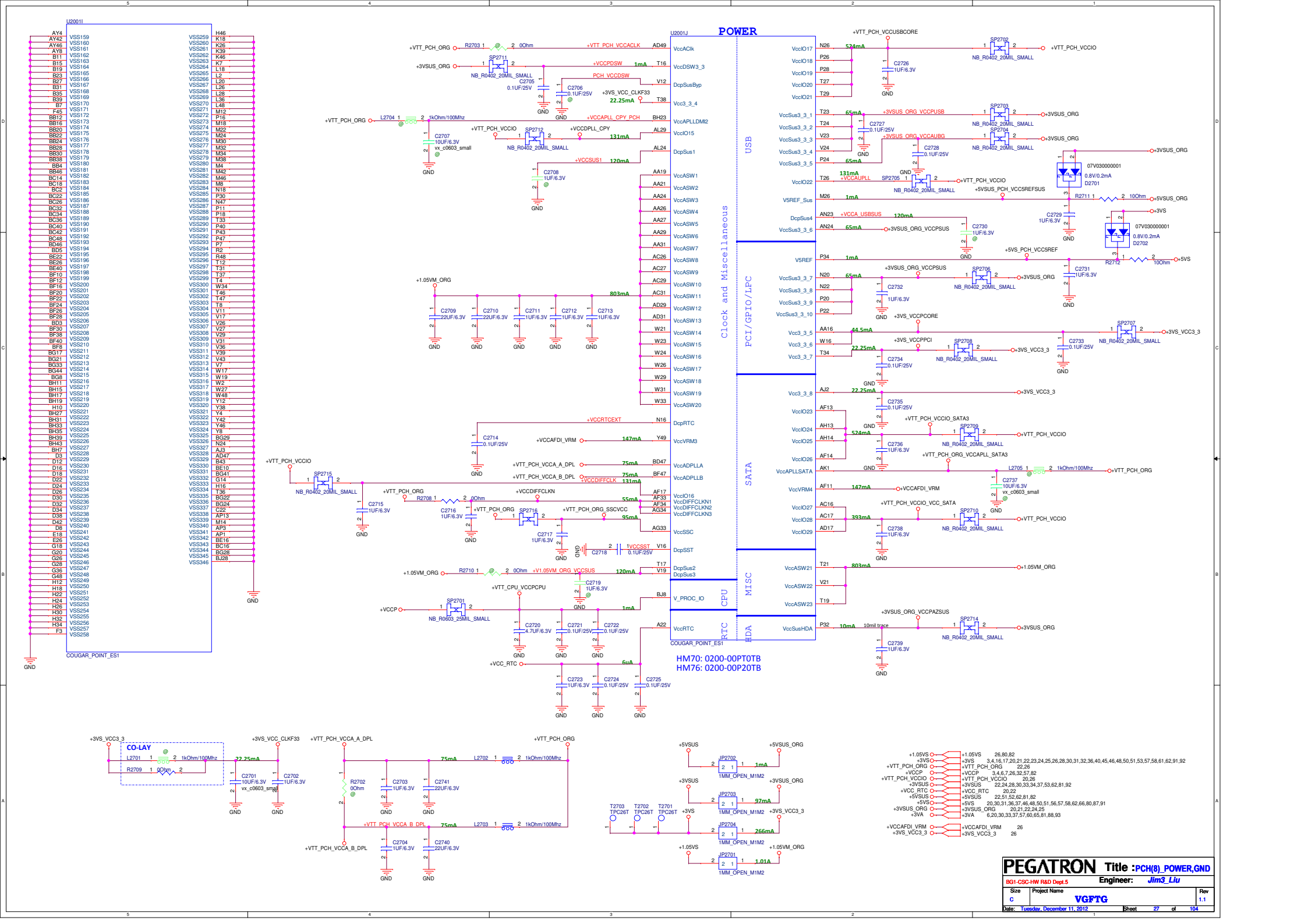


PEGATRON Title : PCH(6)_CPU,GPIO,MISC
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

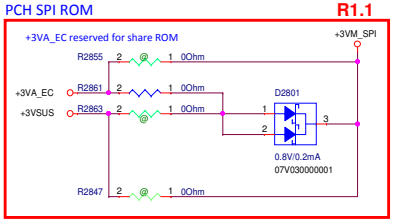
Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 25 of 104


+VTT_PCH_VCCIO +VTT_PCH_VCCIO 20,27
+VTT_PCH_ORG +VTT_PCH_ORG 22,27
+VCCP +VCCP 3,4,6,7,27,32,57,82
+1.8VS +1.8VS 7,25,84
+1.5VS +1.5VS 53,57,91
+3VS +3VS 3,4,16,17,20,21,22,23,24,25,27,28,30,31,32,36,40,45,46,48,50,51,53,57,58,61,62,91,92
+1.05VS +1.05VS 27,80,82
+3VS_VCC3_3 +3VS_VCC3_3 27
+3VM_SPI +3VM_SPI 28
+VCCAFDI_VRM +VCCAFDI_VRM 27
U2001H
COUGAR_POINT_ES1
U2001G
COUGAR_POINT_ES1
POWER
VCC CORE
LVDS
HVCMOS
DMI
VCCIO
DFT / SPI
FDI
SKU(VGA) UMA/OPT DSC
C2612,C2613, C2614,R2609, C2615,C2616, L2602 I NI
R2610,R2611 NI I
HM70: 0200-00PT0TB
HM76: 0200-00P20TB
PEGATRON Title :PCH(7)_POWER,GND
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size C Project Name VGFTG Rev 1.1
Date: Tuesday, December 11, 2012 Sheet 26 of 104


POWER
U2001I
COUGAR_POINT_ES1
U2001J
COUGAR_POINT_ES1
USB
PCI/GPIO/LPC
Clock and Miscellaneous
SATA
MISC
CPU
RTC
HDA
HM70: 0200-00PT0TB
HM76: 0200-00P20TB
CO-LAY
PEGATRON
Title :PCH(8)_POWER,GND
BG1-CSC-HW R&D Dept.5
Engineer: Jim3_Liu
Size C
Project Name VGFTG
Rev 1.1
Date: Tuesday, December 11, 2012
Sheet 27 of 104

PCH SPI ROM **R1.1**



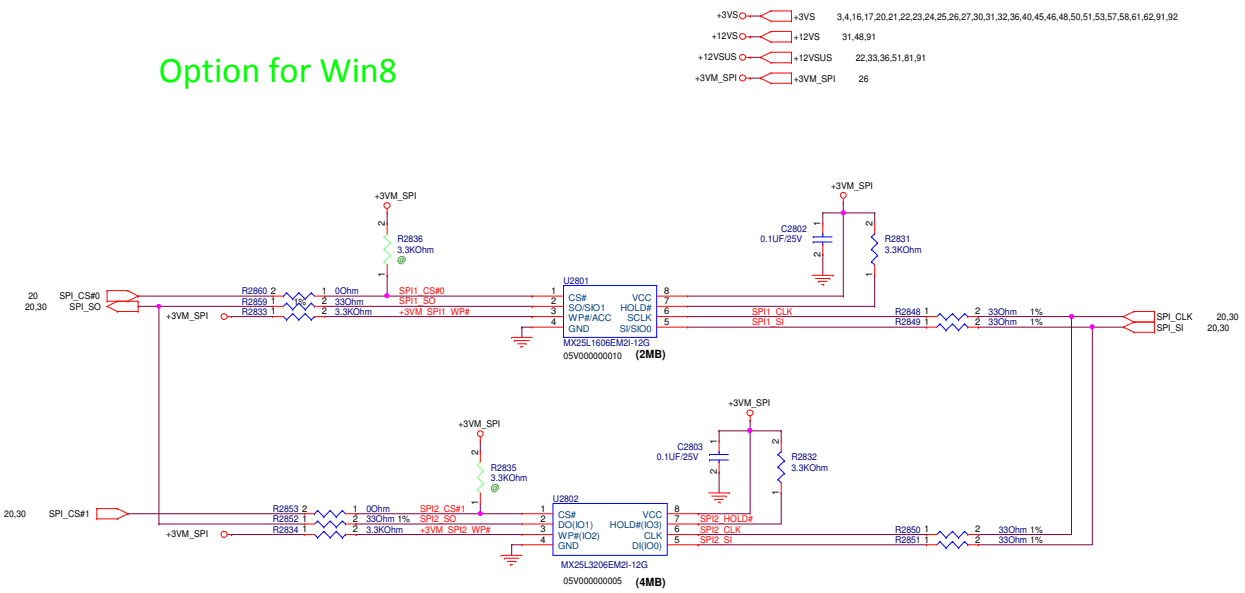
Configuration1(Win 7)

U2801	@	
U2802	@	
U2803	ME+BIOS+EC	4MB
ummount: R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802, R2869, R2870, R2868, D2802, U2801, R2835, R2836		

Configuration2(Win 8)

U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB
ummount: R2858, R2862, R2866, R2867, U2803		

Option for Win8



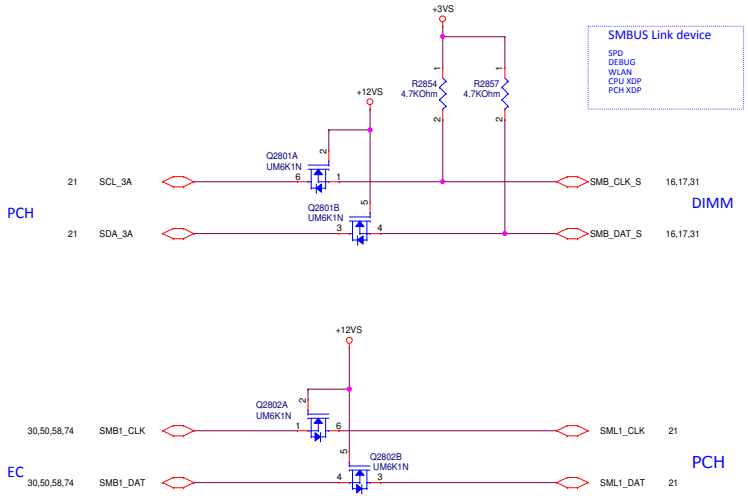
R1.1

Quad I/O Flash ROM part number.

U2801	ME Firmware	2MB	Pegatron P/N	Pegatron VX
	Winbond	2MB	0500-01H3000	05V000000023
	MXIC	2MB	0500-01HU000	

U2802	EC+BIOS	4MB	Pegatron P/N	Pegatron VX
	Winbond	4MB	0500-01FA000	05V000000022
	MXIC	4MB	0500-01HW000	

PCH SMBus

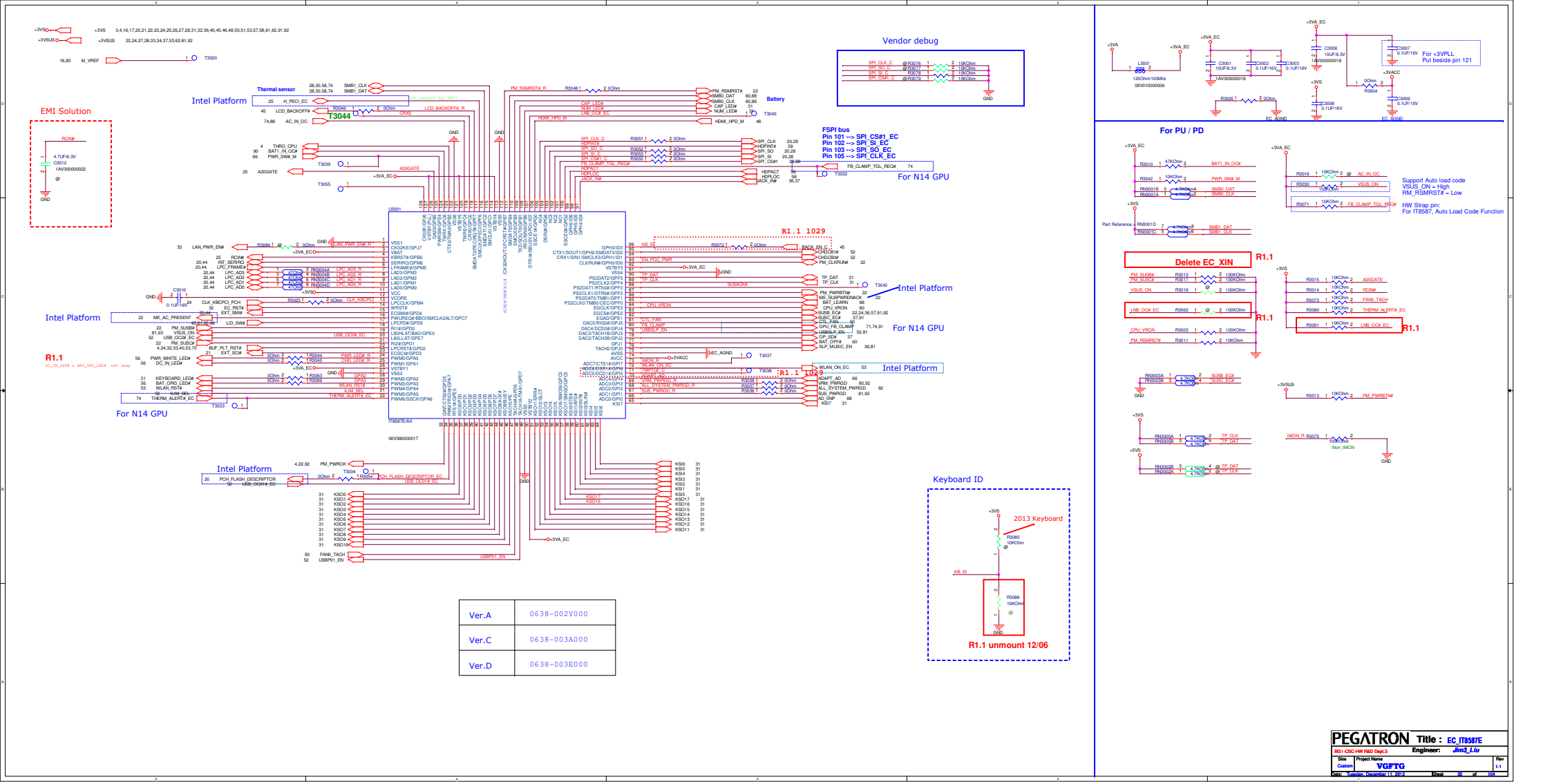


PEGATRON Title : PCH(9)_SPI,SMB

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 28 of 104



Ver.A	0638-002Y000
Ver.C	0638-003A000
Ver.D	0638-003E000

PEGATRON

Title : EC IT8587E

BG1-CSC-HW R&D Dept.5

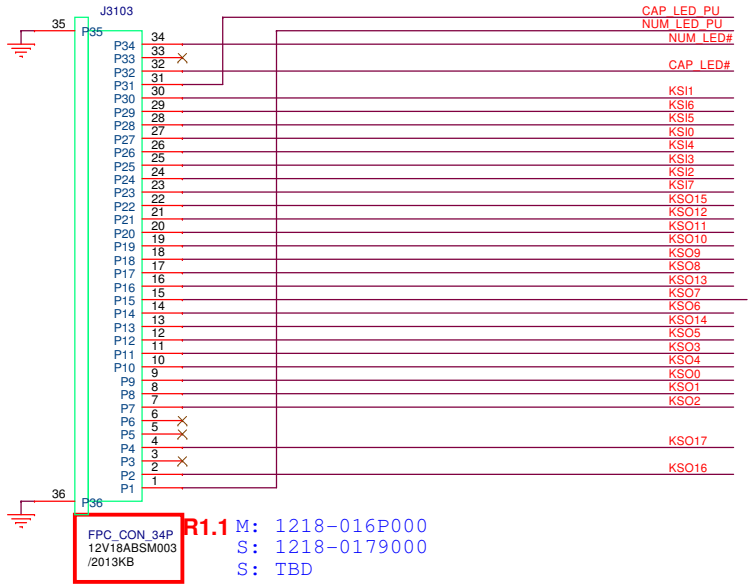
Engineer: Jim3_Liu

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 50 of 104

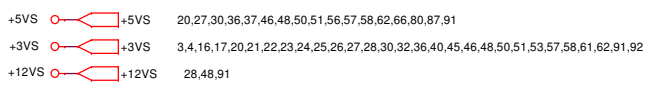
KB CONNECTER

BOTTOM SIDE for 2013 KB

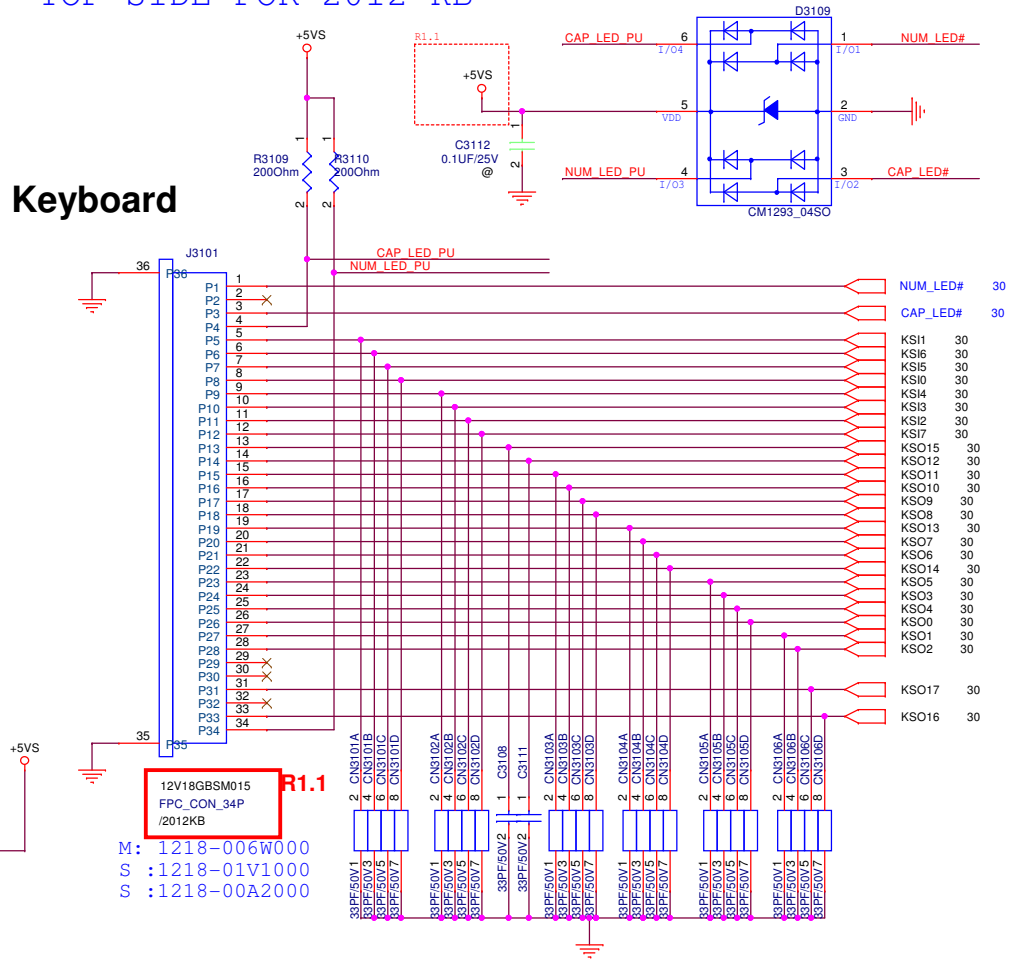


R1.1 M: 1218-016P000
S: 1218-0179000
S: TBD

TOP SIDE FOR 2012 KB

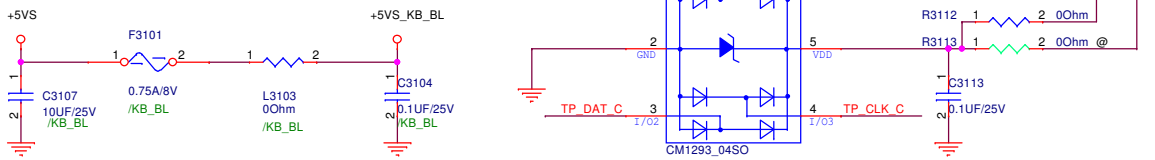


Keyboard



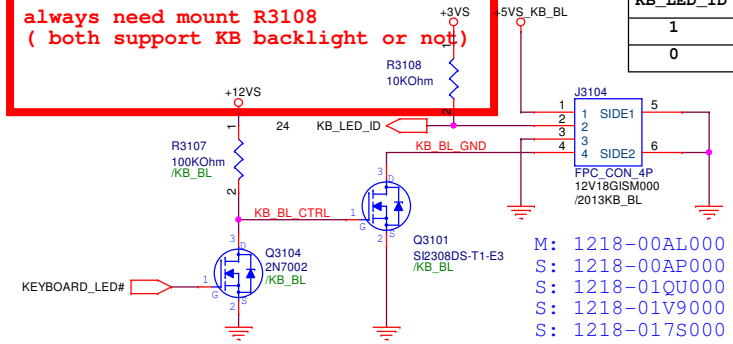
R1.1
M: 1218-006W000
S :1218-01V1000
S :1218-00A2000

Keyboard LED (暫定)

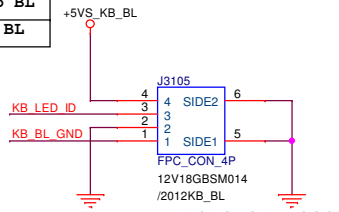


always need mount R3108
(both support KB backlight or not)

KB_LED_ID	
1	KB w/o BL
0	KB w/ BL

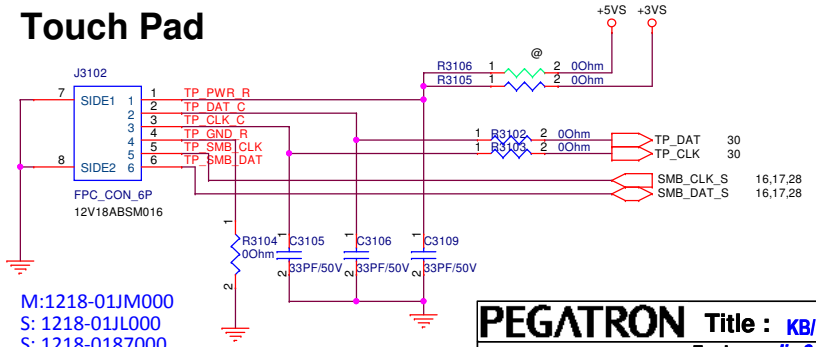


M: 1218-00AL000
S: 1218-00AP000
S: 1218-01QU000
S: 1218-01V9000
S: 1218-017S000



M: 1218-01S7000
S: TBD

Touch Pad



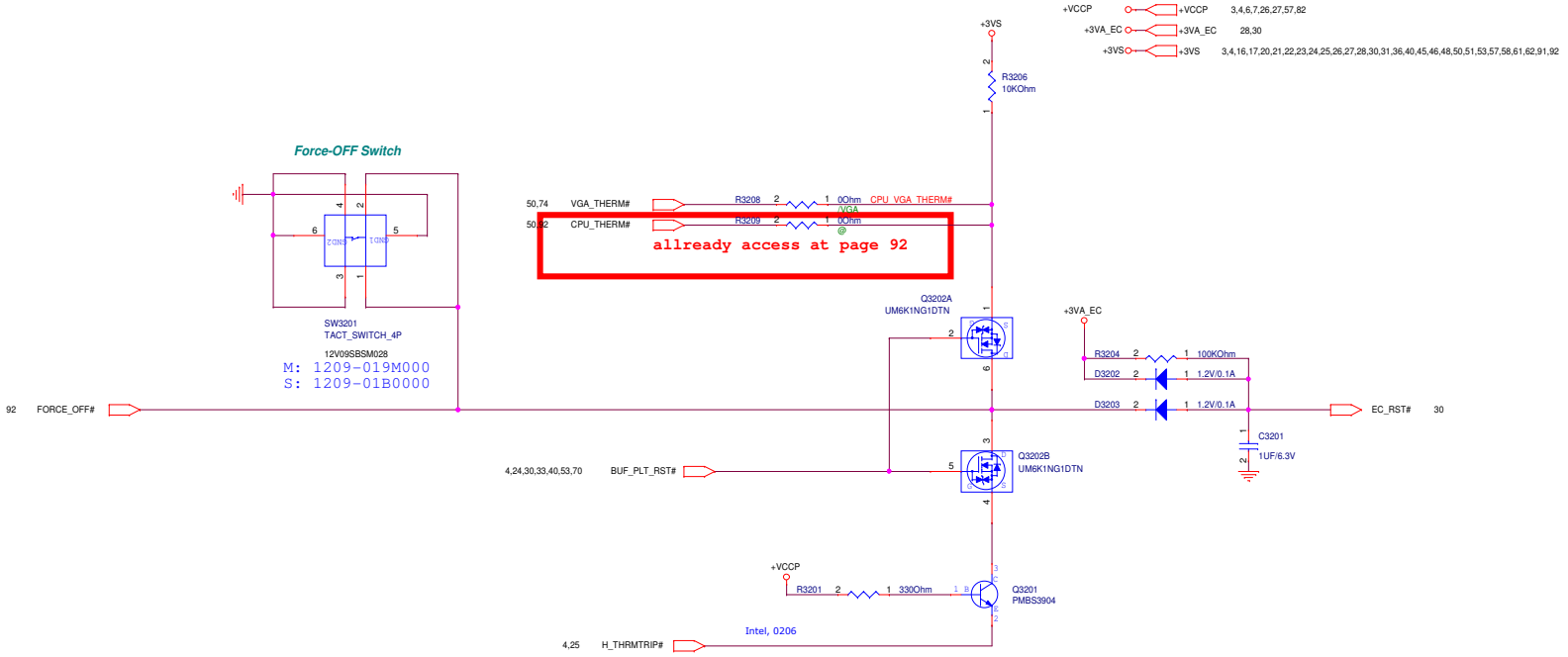
M:1218-01JM000
S: 1218-01JL000
S: 1218-0187000
S: CVILUX(TBD)

BOTTOM SIDE for 2013 KB

TOP SIDE FOR 2012 KB

PEGATRON Title : KB/ TP
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size: Custom | Project Name: VGFTG | Rev: 1.1
Date: Tuesday, December 11, 2012 | Sheet 31 of 104

Thermal Policy



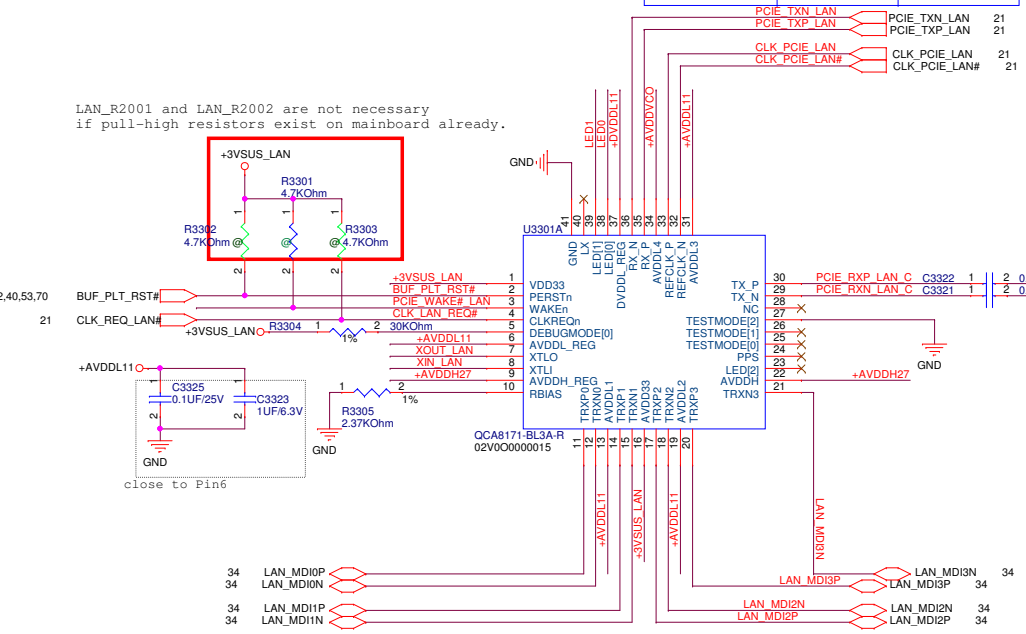
PEGATRON	Title : RST_Reset Circuit		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 32 of 104		

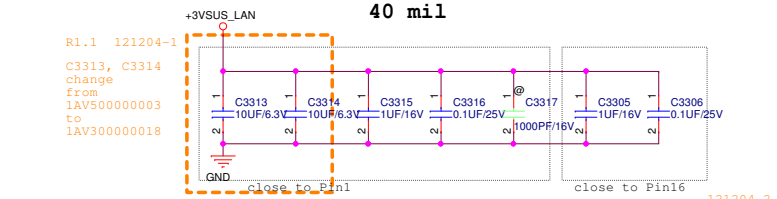
ATHEROS/QCA8171(gigaLAN)	02V0O0000015
ATHEROS/QCA8172(100LAN)	02V0O0000016

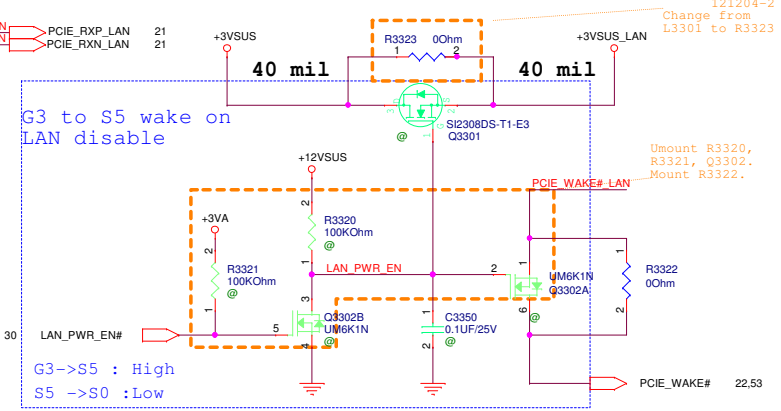
ATHEROS/QCA8171(gigaLAN) 020O-0040000
ATHEROS/QCA8172(100LAN) 020O-0041000

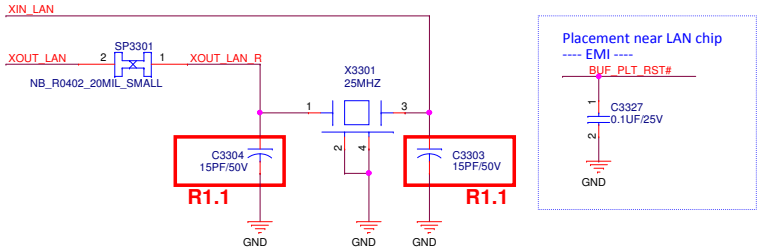
3.3V Current/Power	QCA8171	QCA8172
LDO mode	277 mA / 915 mW	111 mA / 366 mW
SWR mode	136 mA / 448 mW	56 mA / 183 mW

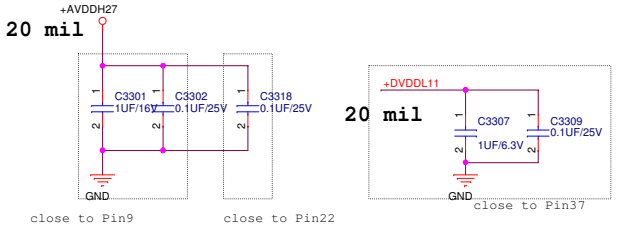
LAN_R2001 and LAN_R2002 are not necessary
if pull-high resistors exist on mainboard already.







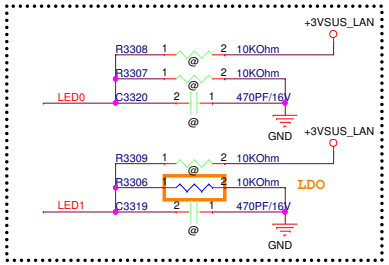




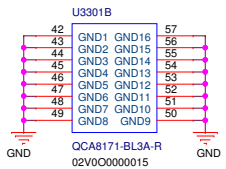
LED[0] -> 1:High core voltage ; 0:Low core voltage
(AVDDL/DVDDL 1.15-1.25V) (AVDDL/DVDDL 1.1V)

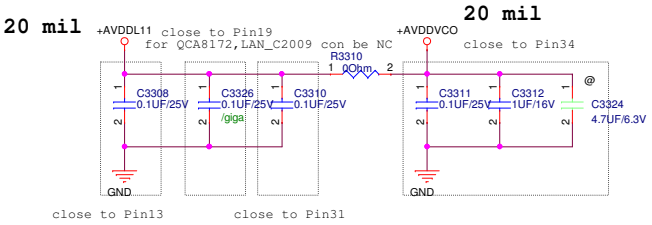
LED[1] -> 1:SWR ; 0:LDO

Both LEDO and LED1 with internal pull-high resistors in the chip,
LAN_R2006, vR2007, LAN_R2008 and LAN_R2009 must be removed.

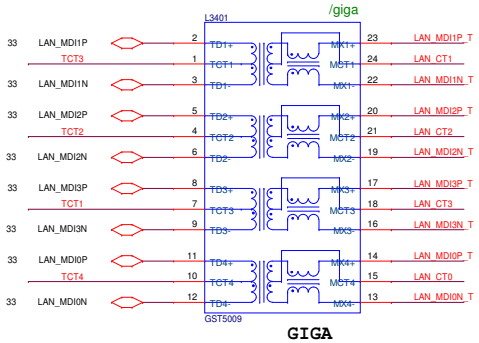


For QCA8171-C, it can only work at high core voltage mode

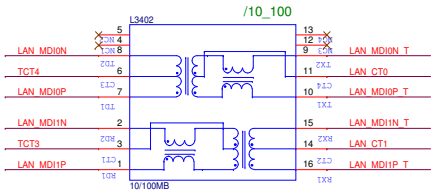




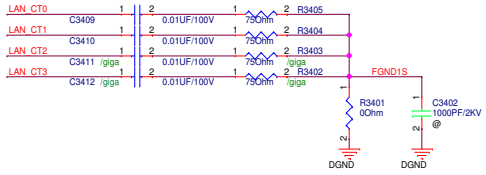
PEGATRON
Title : LAN-QCA8171/72
BG1-CSC-HW R&D Dept.5
Engineer: Jim3_Liu
Size: Custom | Project Name: VGFTG | Rev: 1.1
P/N:
Date: Tuesday, December 11, 2012 Sheet 33 of 104

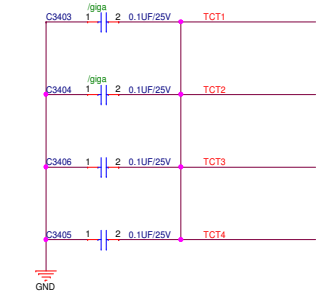


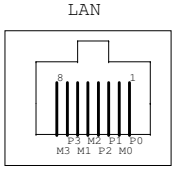
GIGA

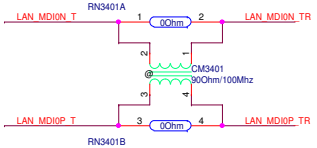


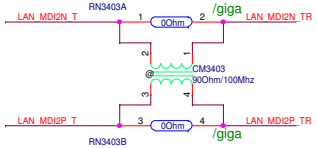
10M/100M

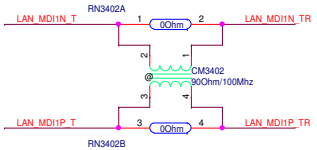


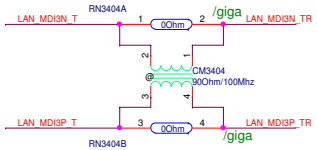


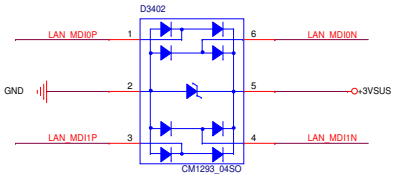


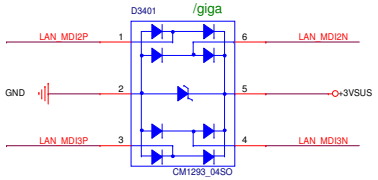


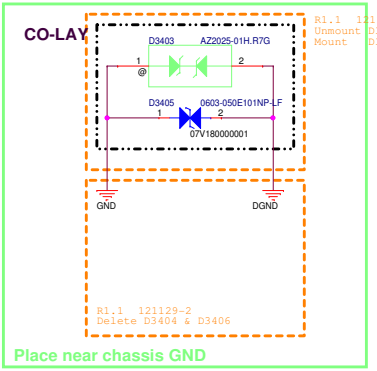






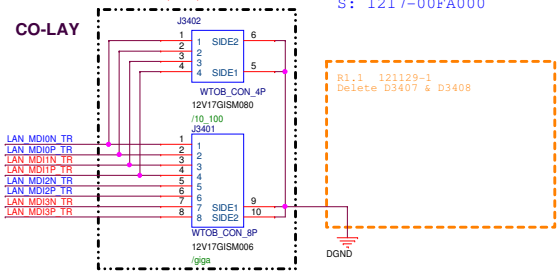






1217-002E000(BGA) 12V17GISM080

M: 1217-002E000
S: 1217-00FA000



1217-000K000(BGA) 12V17GISM006

M: 1217-000K000
S: 1217-007G000

PEGATRON	Title : RJ45	
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu	
Size: Custom	Project Name: VGFTG	Rev: 1.1
	P/N:	
Date: Tuesday, December 11, 2012	Sheet 34 of 104	

Place close to U3601 PIN 11

+5VSUS_AVDD

R3601 2.49KOhm 1%

SENSE_A

C3612 1000PF/16V

A_GND

If SENSE_A total length is greater than 6 inches, change C3631 to 0.1uF

Place close to U3601 PIN 12

+5VSUS_AVDD

R3603 10KOhm

SENSE_B

If SENSE_B is un-used, then pull high SENSE_B to +5VSUS_AVDD by 10Kohm resistor.

Placement near audio codec
---- EMI ----

DMIC_CLK — R3616 (220Ohm/100Mhz 09V010000025) — DMIC_CLK_R

C3626 12PF/50V

Note:
Kepp PVDD supply and speaker traces routed on DGND plane.
Keep away from AGND and other analog signals.

+12VSUS +12VSUS 22,33,51,81,91

+3VO +3VO 70,81,84,91

+5VO +5VO 81,82,83,84,91

+3VS +3VS 3,4,16,17,20,21,22,23,24,25,26,27,28,30,31,32,40,45,46,48,50,51,53,57,58,61,62,91,9

+5VS +5VS 20,27,30,31,37,46,48,50,51,56,57,58,62,66,80,87,91

+3VSUS_DVDD

C3602 1UF/6.3V

C3603 0.1UF/25V

C3604 4.7UF/6.3V

Place C3602~C3610 close to U3601

+5VSUS_AVDD

C3605 1UF/6.3V

C3606 0.1UF/25V

A_GND

+5VSUS_PVDD

C3607 4.7UF/6.3V

C3608 1UF/6.3V

C3609 0.1UF/25V

U3601A

DVDD_CORE 1
DVDD 7
AVDD1 21
AVDD2 32
PVDD1 33
PVDD2 39
PVSS 36

EMI reserved 20120924

C3623 10PF/50V @ 1AV200000001

20 ACZ_BCLK_AUD — BITCLK 5
20 ACZ_SDOUT_AUD — SDATA_OUT 4
20 ACZ_SDIN0 — SDATA_IN 6
20 ACZ_SYNC_AUD — SYNC 8
20,37 ACZ_RST#_AUD — RESET# 9

R3602 33Ohm Place R3602 close to U3601

C3624 1UF/6.3V 1AV200000038

EMI request 20120924

37 HP_JD# — R3605 20KOhm 1%

37 MIC_EXT_JD# — R3604 39.2KOhm 1%

Place R3604 & R3605 close to U3601

SENSE_A 11
SENSE_B 12

DMIC_CLK_R — DMIC_CLK/GPIO1 2
45 DMIC_DAT — DMIC_0/GPIO2 3
EAPD 40
Cap+ 30
Cap- 29
DVSS 41

C3613 Close to Codec

C3613 4.7UF/6.3V

+3VSUS_DVDD

R3619 10KOhm

37 MUTE_AMP#

92HD99B1X5NDGXWCX8
02V0P0000005

PORTD_+L 34 — H_SPKL+ 37
PORTD_-L 35 — H_SPKL- 37

Speaker

PORTD_+R 38 — H_SPKR+ 37
PORTD_-R 37 — H_SPKR- 37

PORTA_L 22 — MIC_IN_AC_E_L — MIC_IN_AC_E_L 37
PORTA_R 23 — MIC_IN_AC_E_R — MIC_IN_AC_E_R 37
VrefOut_A 19 — VREFOUT_A_E 37

Mic

1UF/6.3V C3619 A_GND

PORTB_L 25 — AC_HP_L 37
PORTB_R 26 — AC_HP_R 37

Headphone

PORTC_L 15
PORTC_R 16
VrefOut_C/GPIO4 20 — AUD_GPIO4# 37

R1.1

PORTF_L 13 — R3620 10KOhm MIC_IN_AC_E_L
PORTF_R 14 — R3621 10KOhm MIC_IN_AC_E_R

PCBeep 10 — PC_BEEP — C3618 0.1UF/25V — PC_BEEP_C — R3609 100KOhm — SB_SPKR 20

CAP2 18
VrefFilt 17
V- 28
Vreg(+2.5V) 31

C3614 4.7UF/6.3V
C3615 4.7UF/6.3V
C3616 4.7UF/6.3V
C3617 1UF/6.3V

AVSS2_1 24
AVSS2_2 27

R3610 10KOhm

A_GND

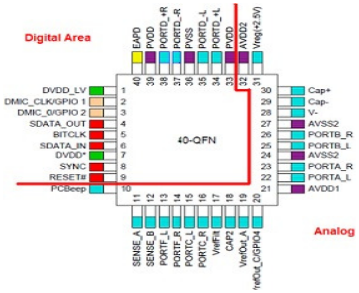
U3601B

42 DVSS1 — DVSS8 49
43 DVSS2 — DVSS7 48
44 DVSS3 — DVSS6 47
45 DVSS4 — DVSS5 46

92HD99B1X5NDGXWCX8
02V0P0000005

Audio Codec Power Rail

Digital Area



Analog

non-Sleep & Music --> +5VS & +3VS

Sleep & Music --> +5VO & +3VO

JP3602 R0603 — +5VSUS_AVDD (0.5A)

Moat

+5VS — /non-SLP_MUSIC R3611 0Ohm

+5VO — Q3601 IRFML8244TRPBF /SLP_MUSIC

VGS= 4.5V , Rdson = 41mOhm
VGS= 10V , Rdson = 24mOhm

1.5A

+5VSUS_PVDD (1A)

+3VS — /non-SLP_MUSIC R3612 0Ohm

+3VO — Q3602 IRFML8244TRPBF /SLP_MUSIC

VGS= 4.5V , Rdson = 41mOhm
VGS= 10V , Rdson = 24mOhm

+3VSUS_DVDD (0.1A)

/SLP_MUSIC C3622 0.22UF/16V MLCC +/-10% vx_c0402_small %

/SLP_MUSIC R3614 22KOhm vx_r0402_small 1%

R1.1

Sleep & Music without H/W EQ reserved

/SLP_MUSIC R3640 0Ohm /SLP_MUSIC

/SLP_MUSIC C3621 0.033UF/16V vx_c0402_small 10%

/SLP_MUSIC R3613 22KOhm vx_r0402_small 1%

+3VSUS_DVDD

R1.1

R3618 @ 10KOhm

JACK_IN

30,37 JACK_IN#

Q3605 2N7002 @

22,24,30,57,91,92

SUSB_EC#

D3601 0.8V/0.2mA @

+12VSUS

AMP_PWR_EN

Q3604 68@-5mA/Vceo=+/-50V

R3617 @ 100KOhm vx_r0402_small 1%

+12V_AUDIO_AMP (0.01A)

+12VSUS

/SLP_MUSIC

30,81 SLP_MUSIC_EN

Q3603 68@-5mA/Vceo=+/-50V

R3615 100KOhm vx_r0402_small 1%

+12V_AUDIO (0.01A)

Audio Codec Power Rail +5VSUS_PVDD/AVDD
Turn ON by MIC JACK_IN#
SUSB_EC# keeps +5VSUS_PVDD/AVDD for S0

Audio Codec Power Rail +3VSUS_DVDD
Turn ON by SLP_MUSIC_EN(keep H/W EQ.(present)

Place JP3604~JP3607 together and close to U3601.

JP3605 NB_R0603_32MIL_SMALL

JP3604 NB_R0603_32MIL_SMALL

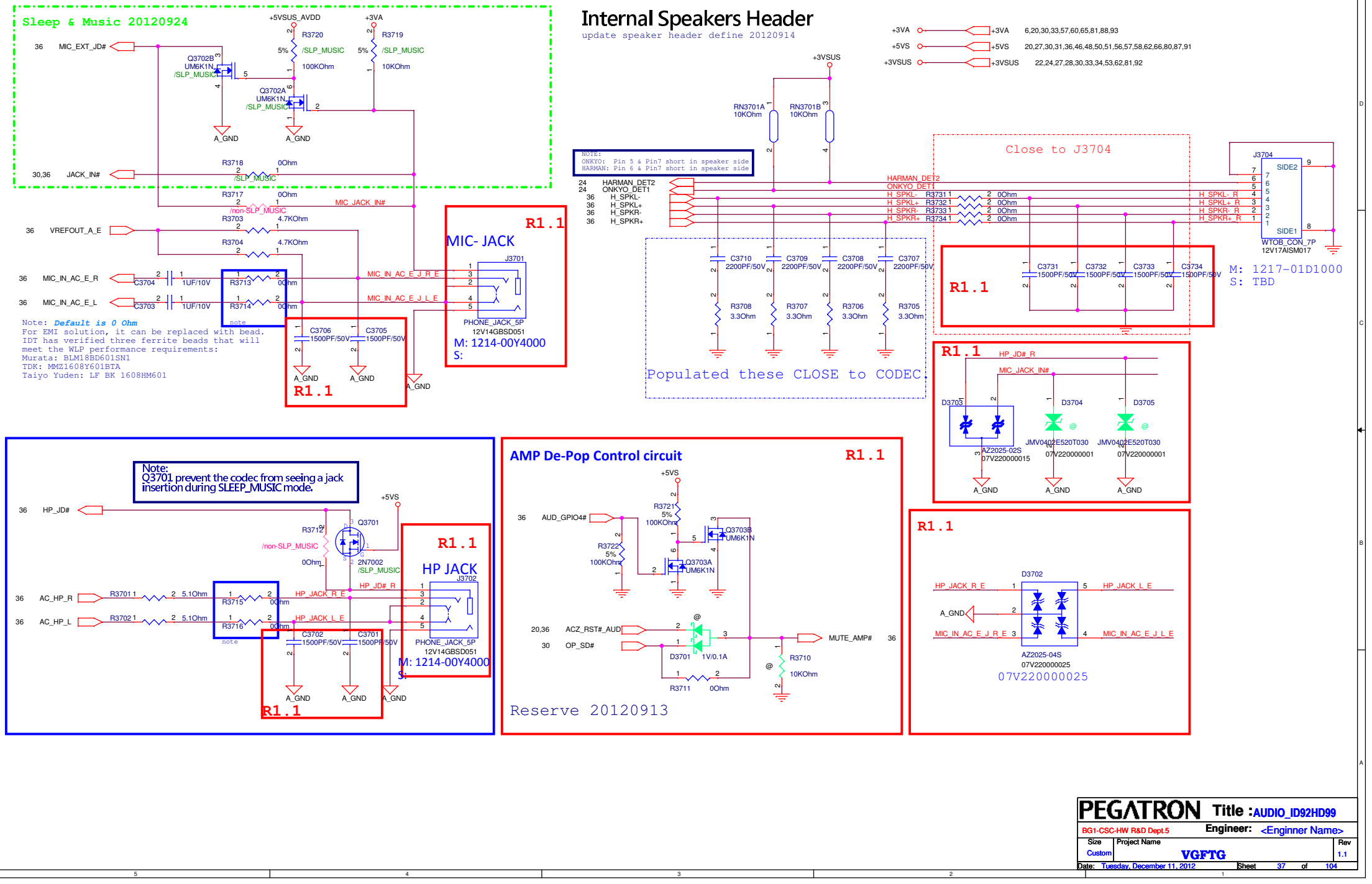
JP3606 NB_R0603_32MIL_SMALL

JP3607 NB_R0603_32MIL_SMALL

R1.1

A_GND

PEGATRON	Title : AUDIO_ID92HD99		
BG1-CSC-HW R&D Dept.5	Engineer: <Enginner Name>		
Size: Custom	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 36 of 104		

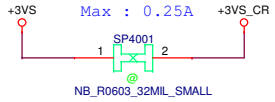


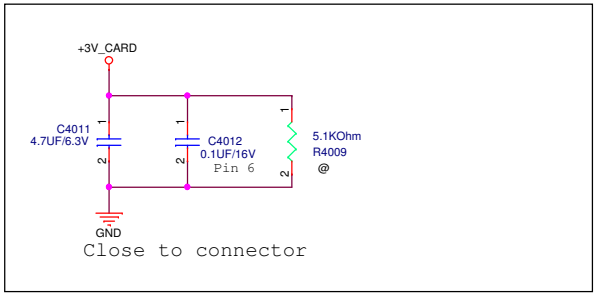
PEGATRON Title : AUDIO_ID92HD99

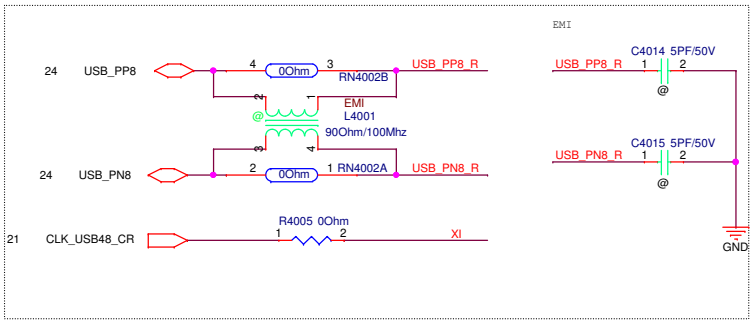
BG1-CSC-HW R&D Dept.5 Engineer: <Enginner Name>

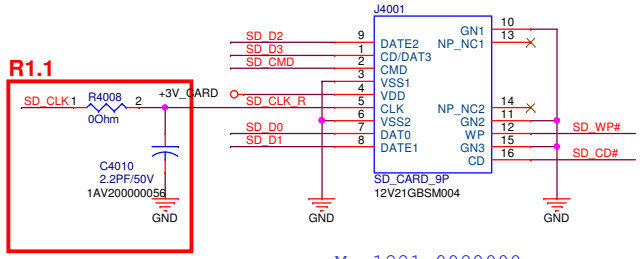
Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 37 of 104







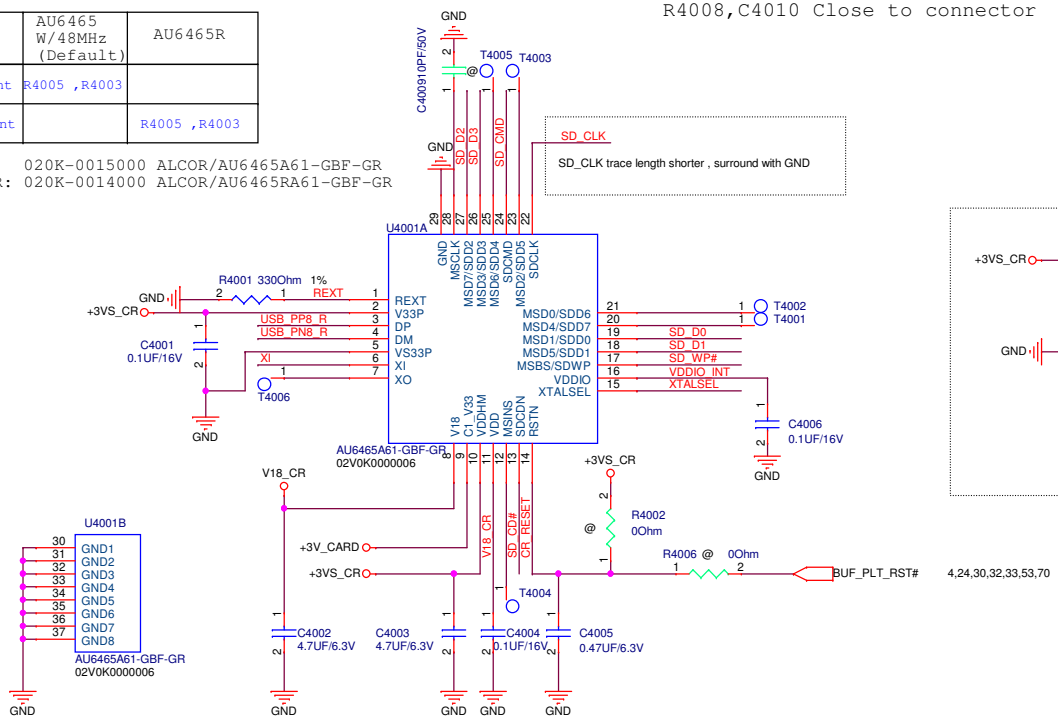


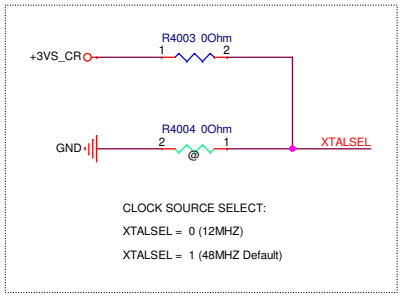
R4008,C4010 Close to connector

M: 1221-0089000
S :TBD

	AU6465 W/48MHz (Default)	AU6465R
Mount	R4005 ,R4003	
Unmount		R4005 ,R4003

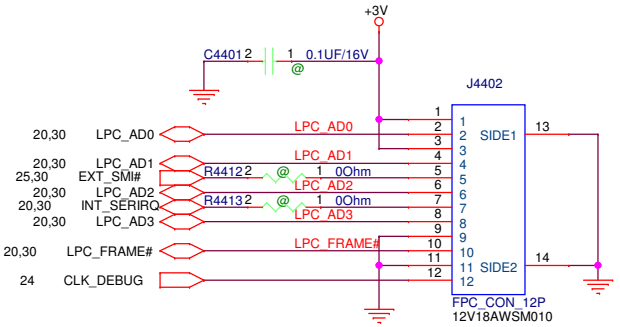
AU6465: 020K-0015000 ALCOR/AU6465A61-GBF-GR
AU6465R: 020K-0014000 ALCOR/AU6465RA61-GBF-GR





PEGATRON	Title : AU6465		
PEGATRON CORPORATION	Engineer: VGFTG		
Size: Custom	Project Name		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 40 of 104		

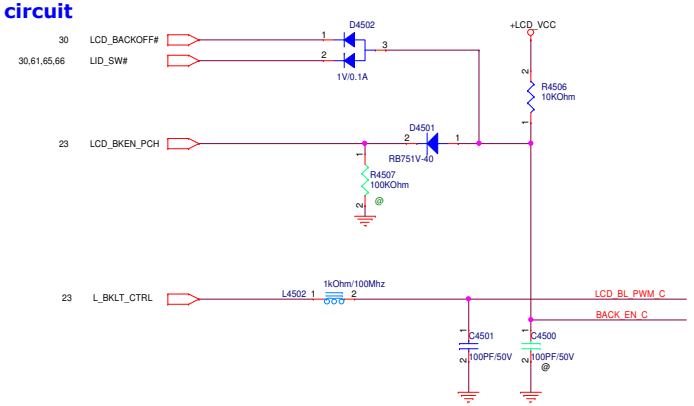
DEBUG CARD CONN.



M :1218-00I1000
S : 1218-01GU000
S : 1218-01BR000

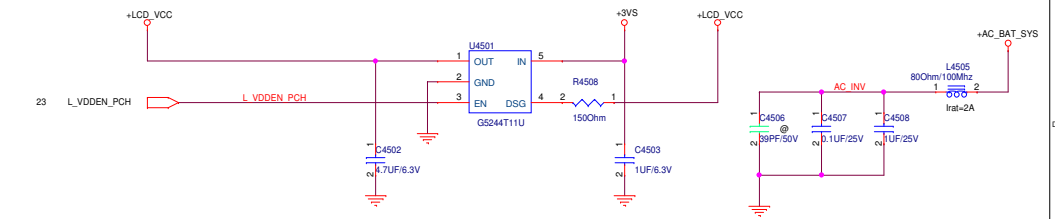
PEGATRON	Title : BUG_Debug	
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu	
Size: B	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 44 of 104	

Controller circuit

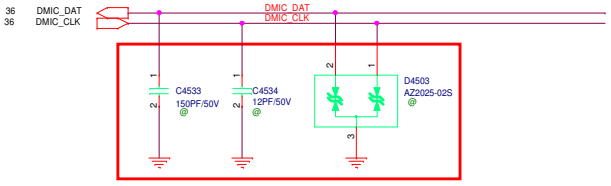


LCD_VCC for eDP

PCH

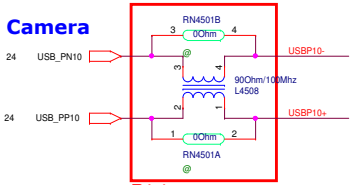


DMIC

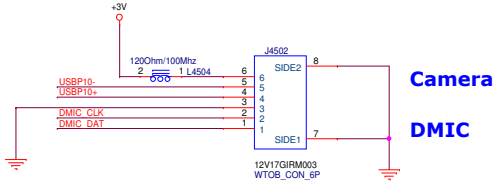


R1.1

Camera



R1.1

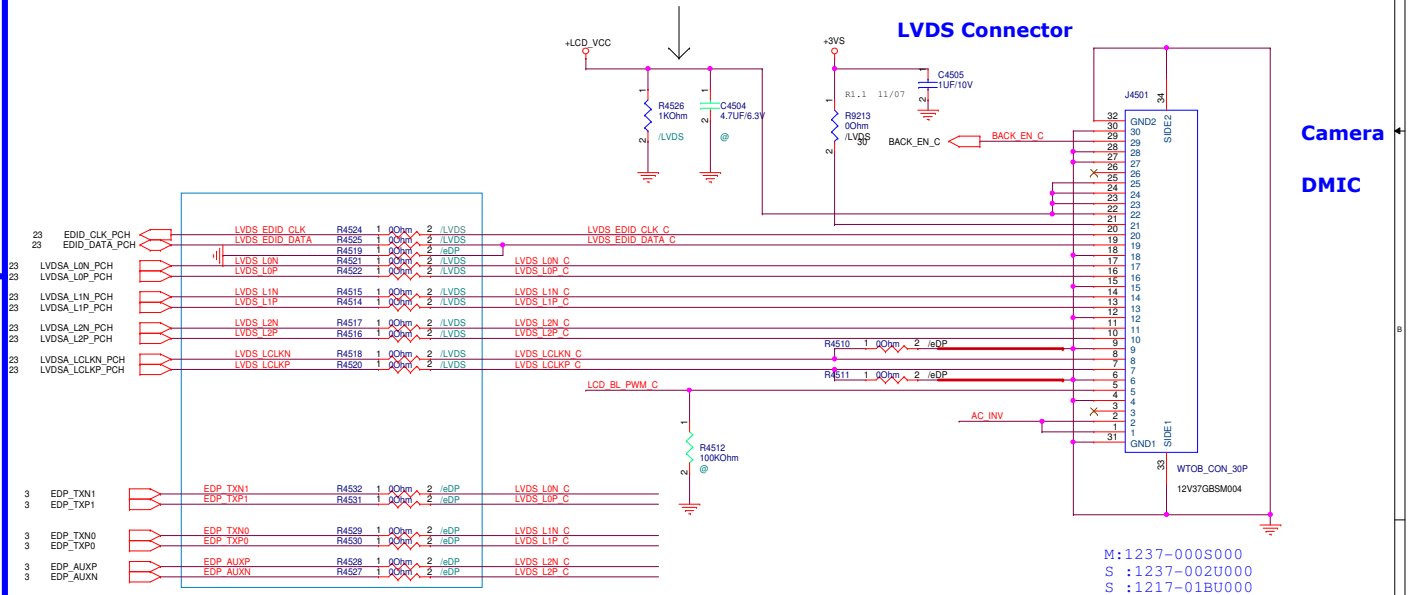


Camera

DMIC

NOTE:
1. Entire trace of Panel VCC should be wider than 80-mil

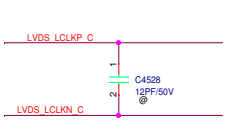
LVDS Connector

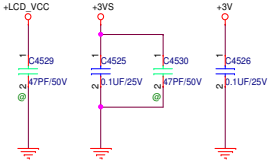


Camera

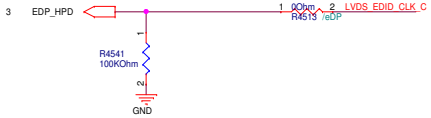
DMIC

M:1237-000S000
S :1237-002U000
S :1217-01BU000





eDP HPD

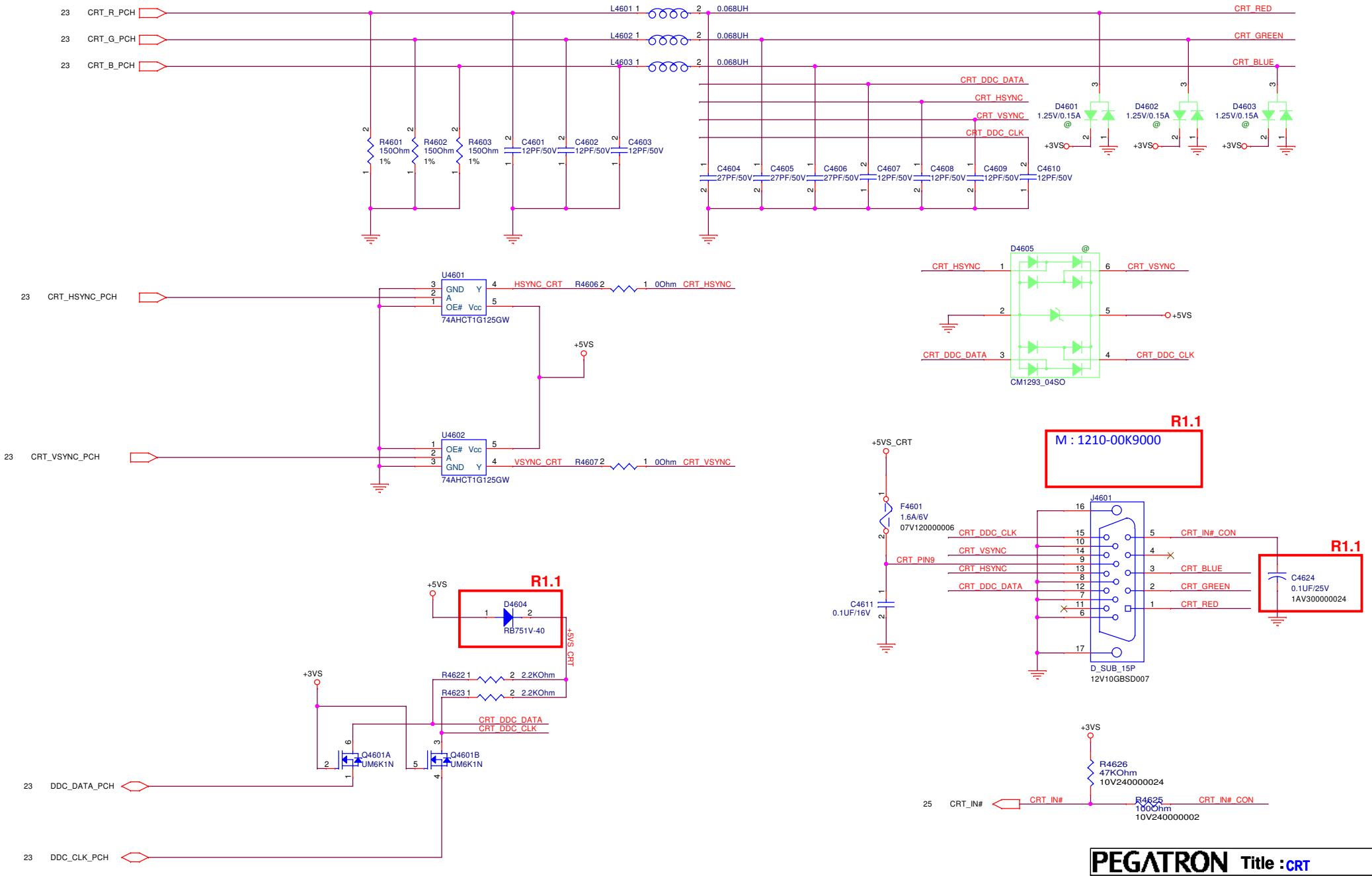


PEGATRON Title : LVDS OUT

Engineer:

Size	Project Name	Rev

Date: Tuesday, December 11, 2012 Sheet 45 of 104

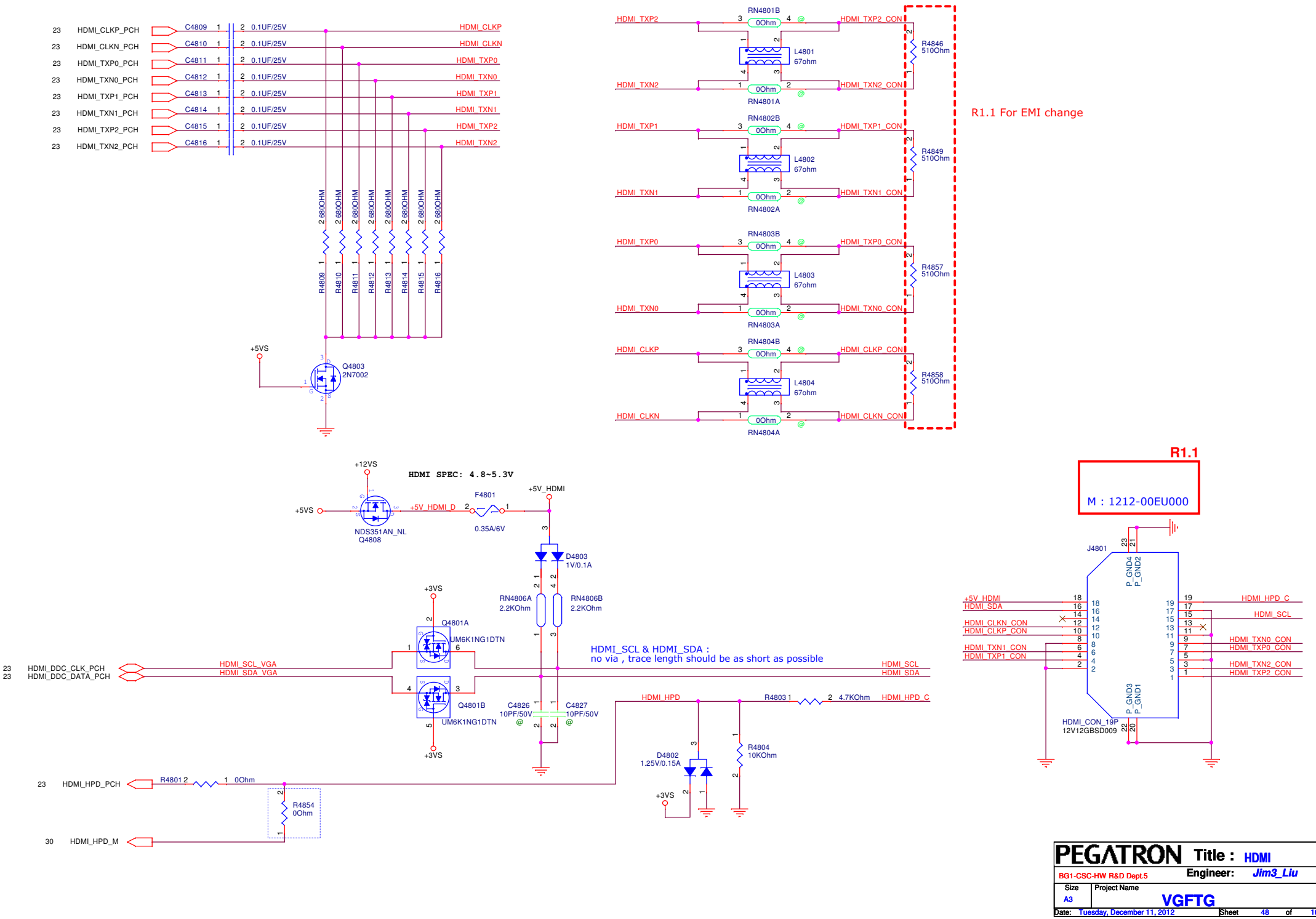


PEGATRON Title : CRT

BG1-CSC-HW R&D Dept.5 Engineer: Peter5 Huang

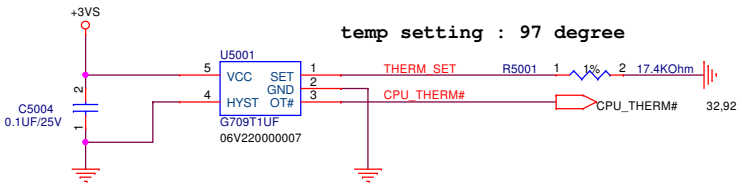
Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 46 of 104

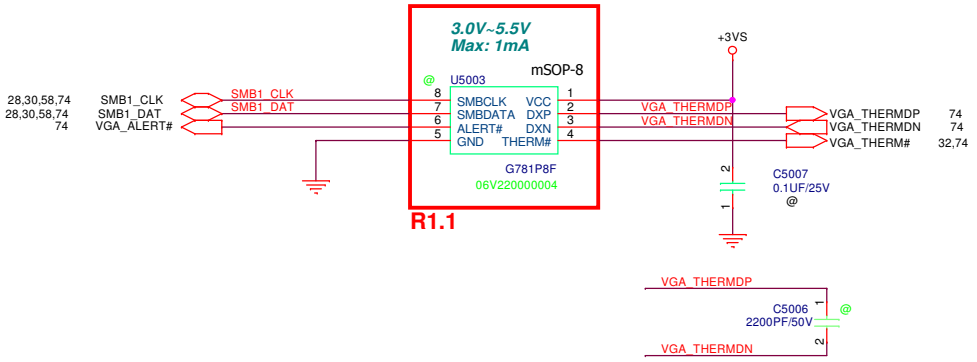


PEGATRON	Title : HDMI		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: A3	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 48 of 104		

U5001 Close to CPU

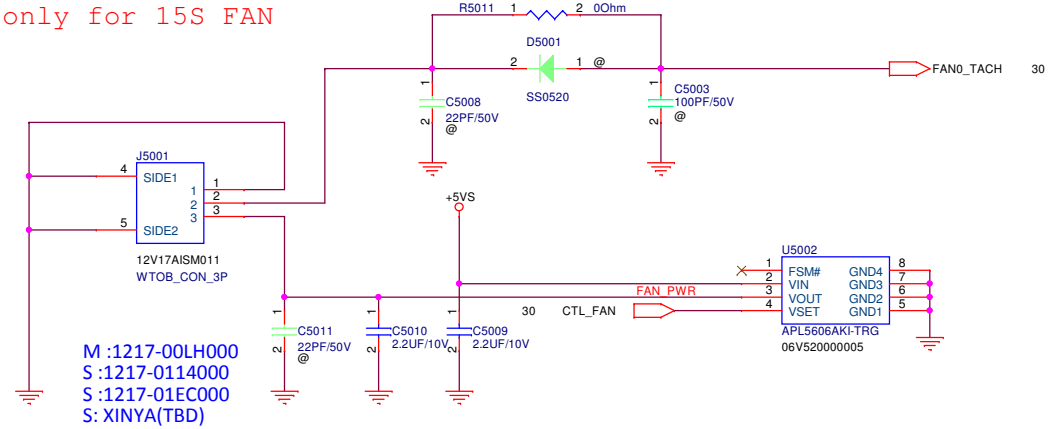


U5003 Close to GPU



FAN

only for 15S FAN

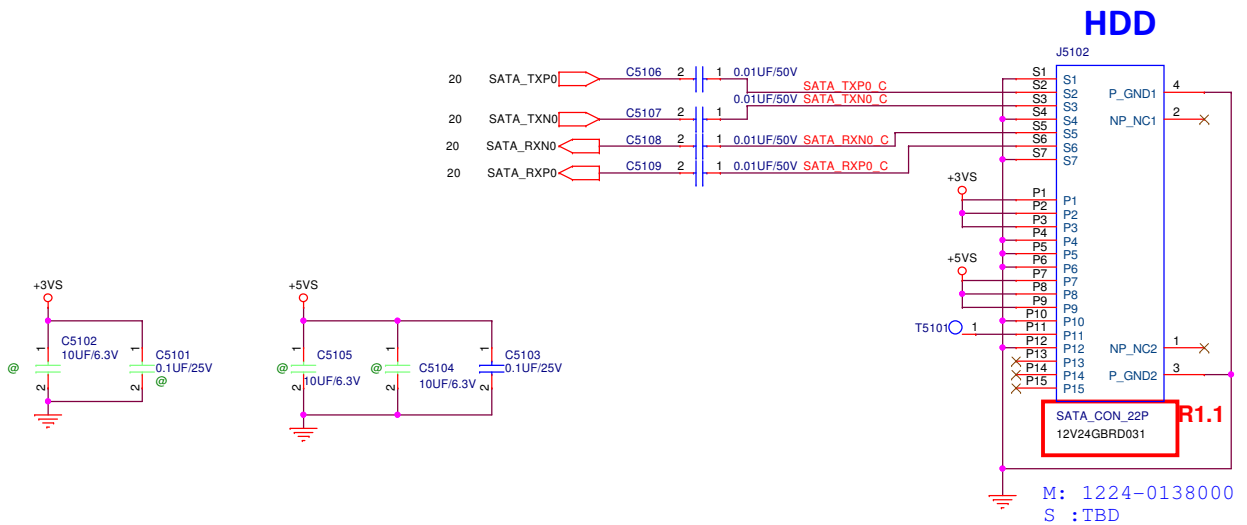


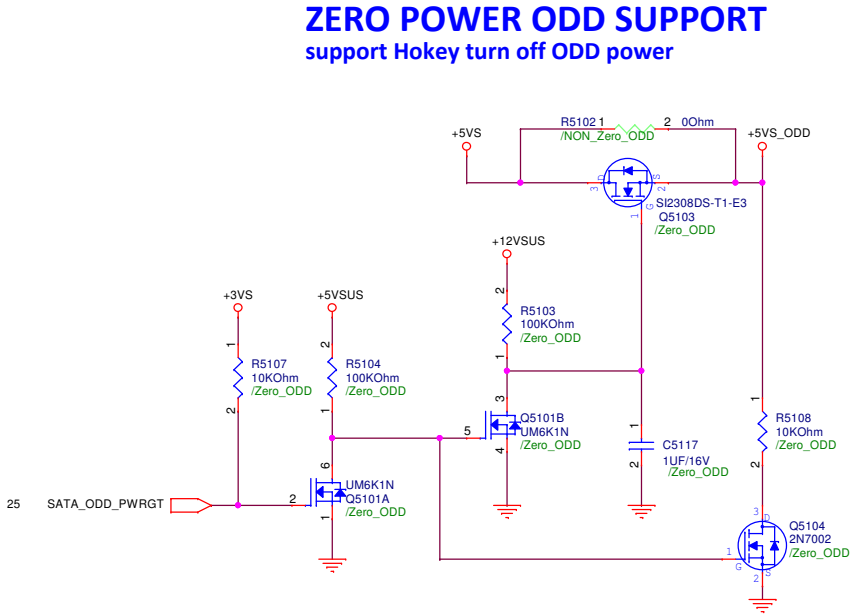
PEGATRON Title : THERMAL/ FAN

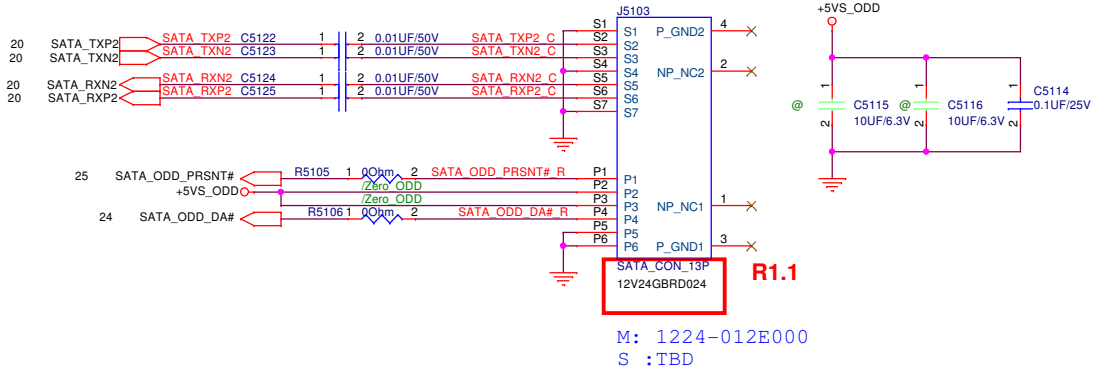
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 50 of 104

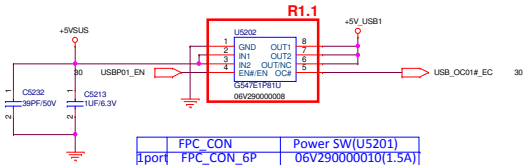




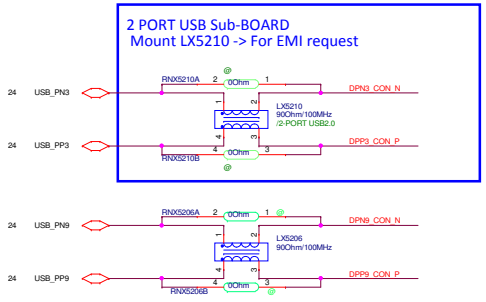


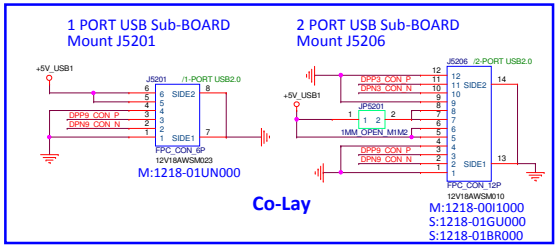
PEGATRON	Title : SATA HDD/ ODD		
BG1-CSC-HW R&D Dept.5	Engineer:		
Size: Custom	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 51 of 104		

USB 2.0 port x2 (Left Up)

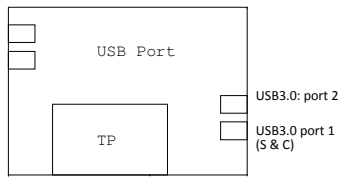


	FPC_CON	Power SW(U5201)
1port	FPC_CON_6P	06V290000010(1.5A)
2port	FPC_CON_12P	06V290000008(2.5A)

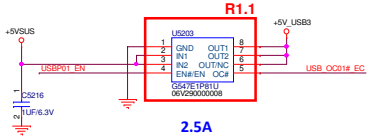


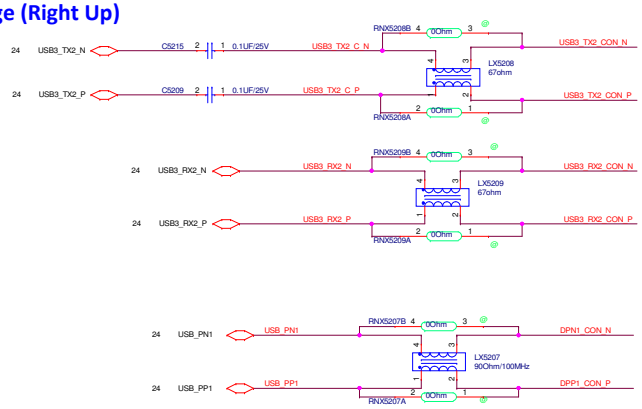


USB Sub-Board	Mount	Unmount
1port	J5201	J5206
2port	J5206	J5201

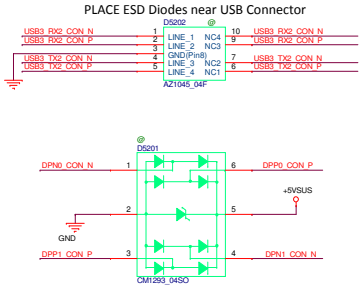


USB 3.0 ports x 1 without Sleep & Charge (Right Up)

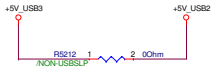


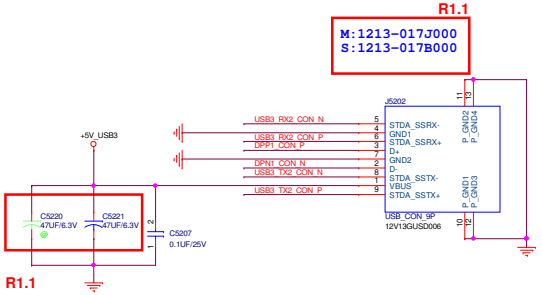


PLACE ESD Diodes near USB Connector



USBSLP / NON_USBSLP

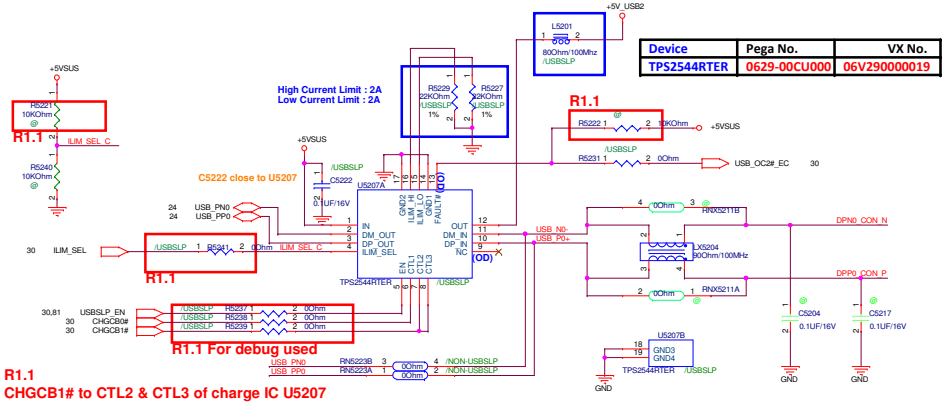




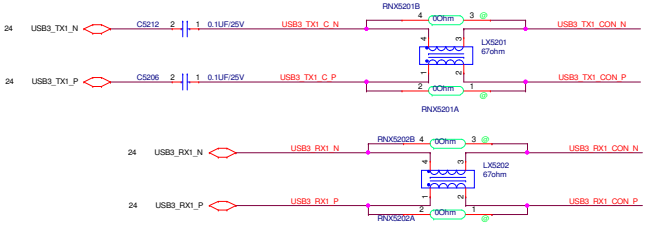
USB 3.0 ports x 1 with Sleep & Charge (Right Down)

TPS2544 Device True Table

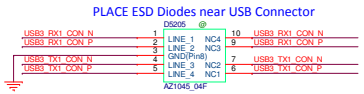
Sleep & Charge function Setting	State	Charging Mode	Wake up	CHGCB0#	CHGCB1#	ILIM_SEL	USBSLP_EN	Backup
Auto Mode	S0	CDP	NA	1	1	1	1	
	S3~S5	DCP Auto	NA	0	1	1	1	Wake up by KB/MS at S3 state
Alternative Mode	S0	CDP	NA	1	1	1	1	
	S3~S5	DCP Auto	NA	0	1	1	1	Wake up by KB/MS at S3 state
Disable	S0	CDP	NA	1	1	1	1	
	S3	SDP	Enable wake up	1	1	0	1	Wake up by KB/MS at S3 state
			Disable wake up	1	1	0	0	
	S4/S5	Discharge	NA	0	0	1	0	

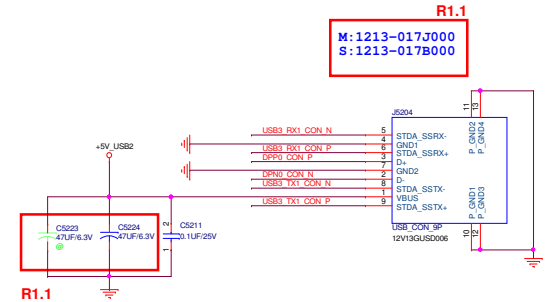


Device	Pega No.	VX No.
TPS2544RTER	0629-00CU000	06V290000019

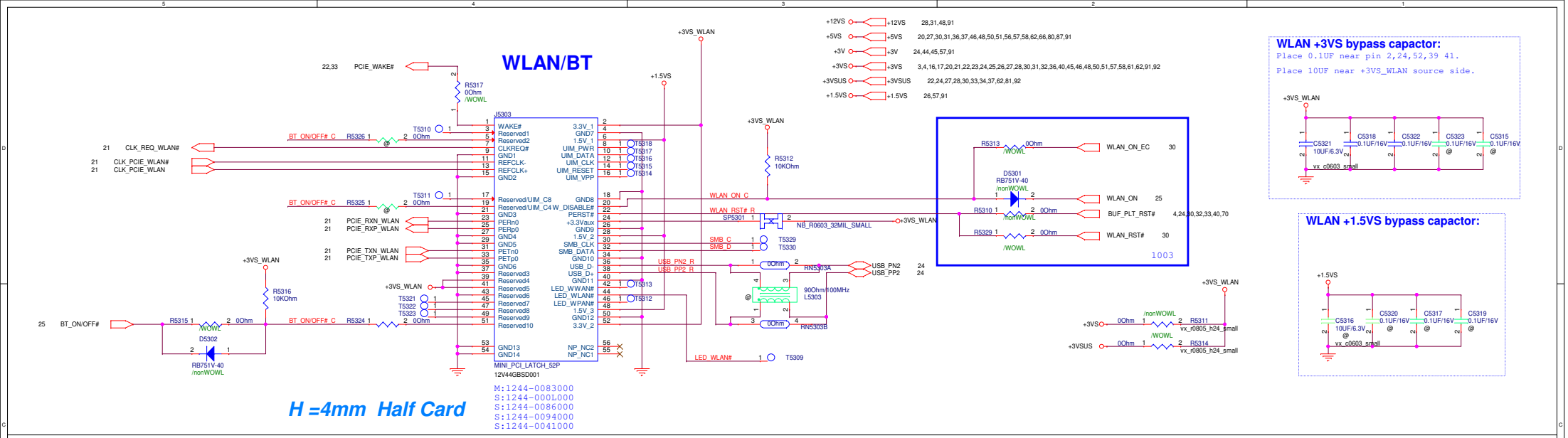


PLACE ESD Diodes near USB Connector



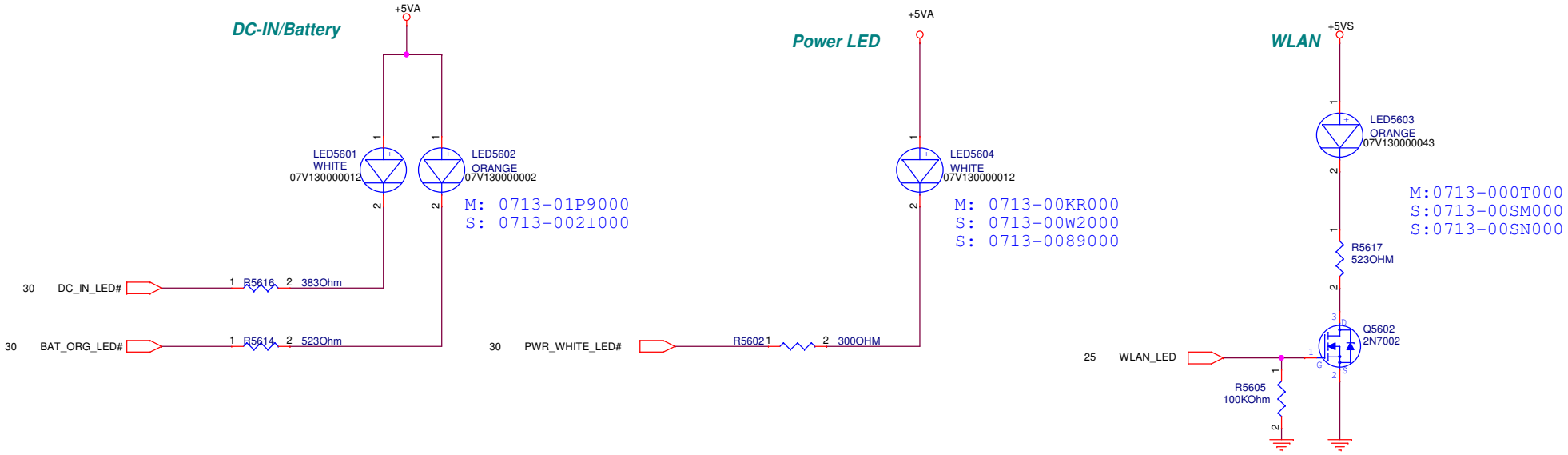


PEGATRON Title : USB JACK
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size: Custom | Project Name: VGFTG | Rev: 1.1
Date: Tuesday, December 11, 2012 | Sheet 52 of 104



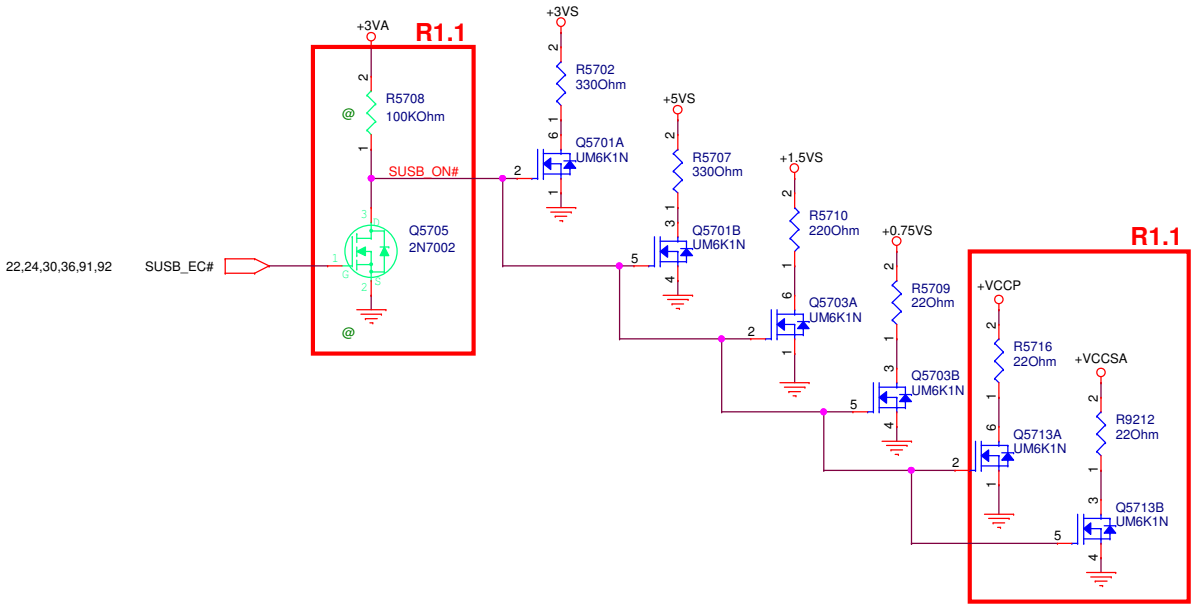
PEGATRON	Title : 53.TV_tuner		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: Custom	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 53 of 104		

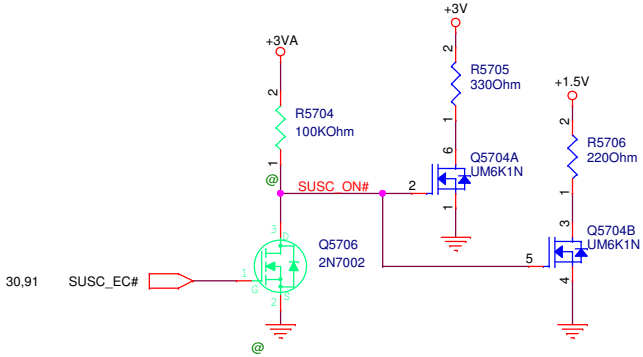
Order of Indicator LEDs

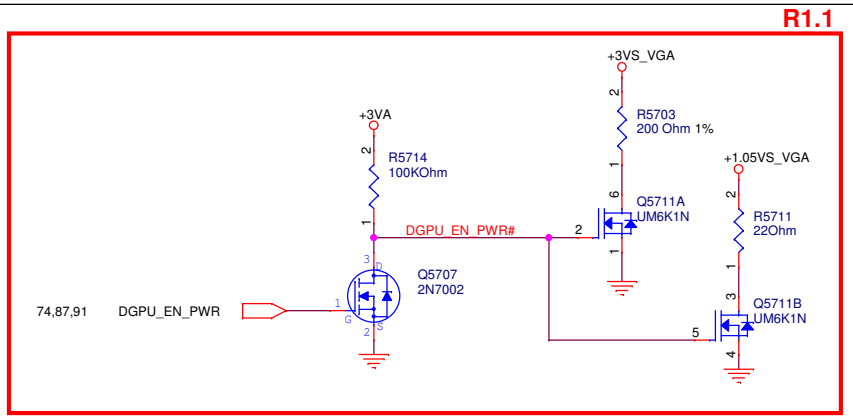


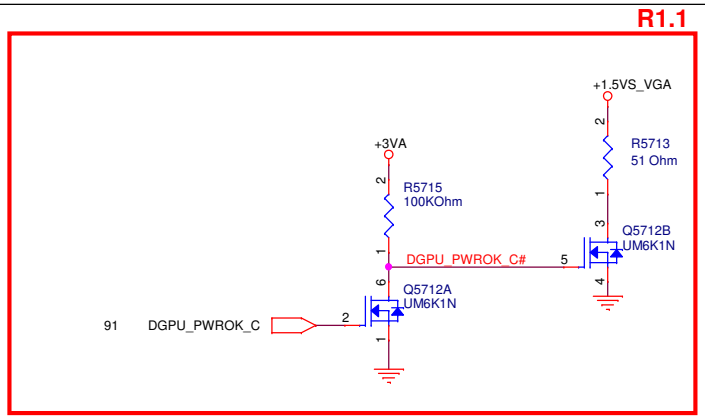
PEGATRON	Title : LED	
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu	
Size: B	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 56 of 104	

Discharge Circuit



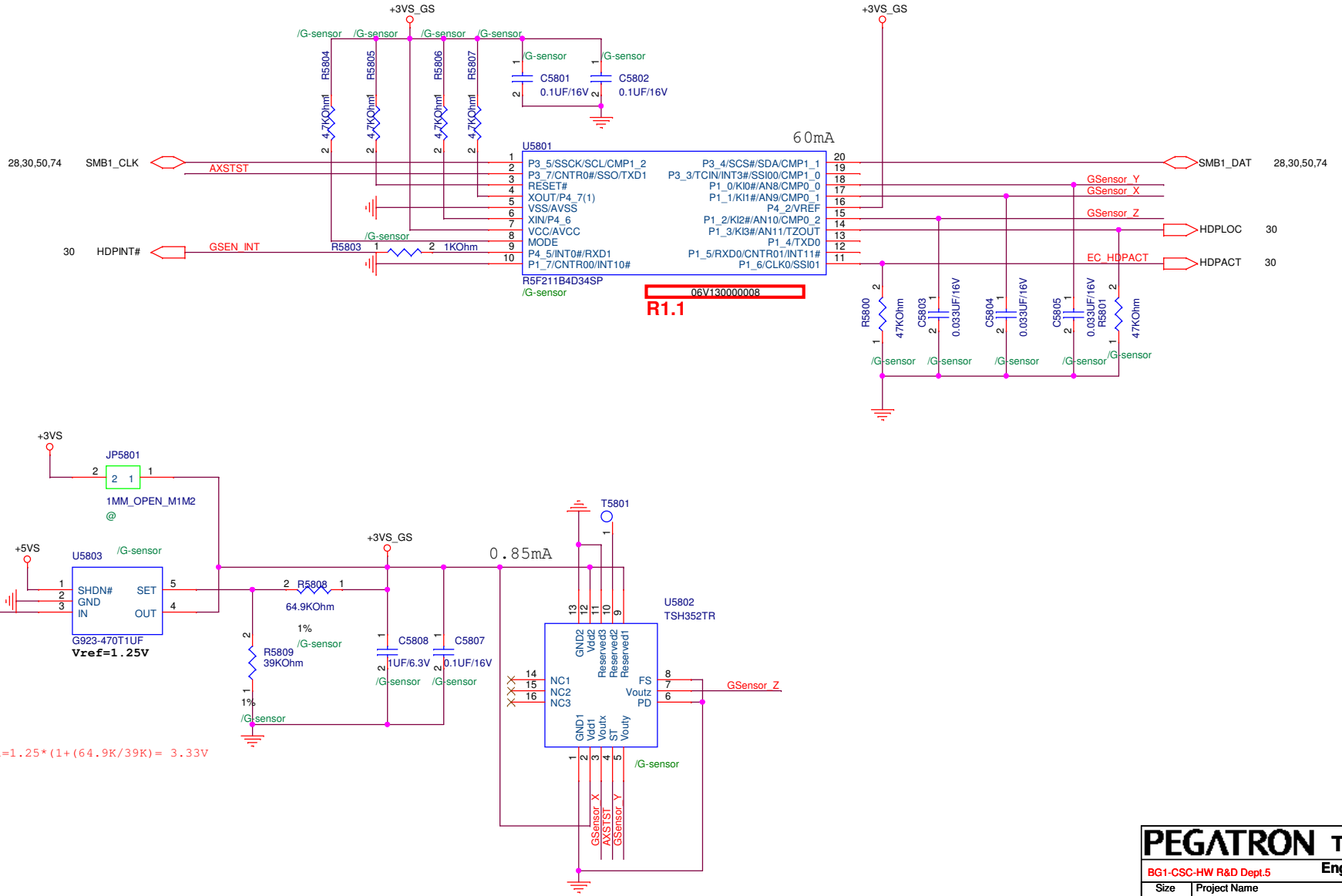






PEGATRON	Title : DC-IN/ DISCHARGE	
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu	
Size: B	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 57 of 104	

G-sensor



PEGATRON	Title : G-Sensor TSH35TR	
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu	
Size: B	Project Name	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 58 of 104	

CIR

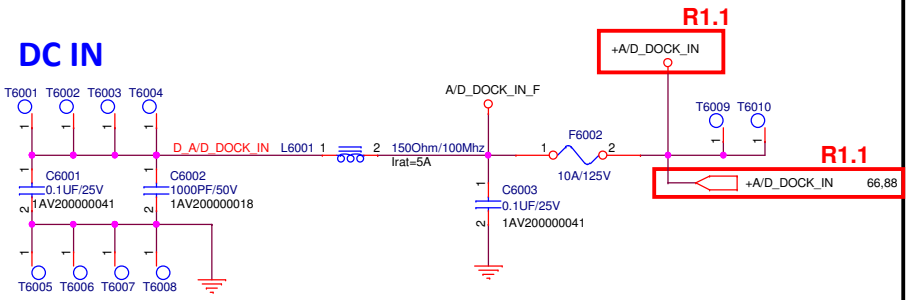
PEGATRON Title : CIR

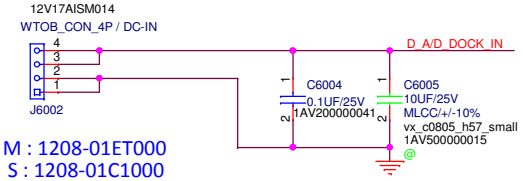
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
B		1.1

Date: Tuesday, December 11, 2012 Sheet 59 of 104

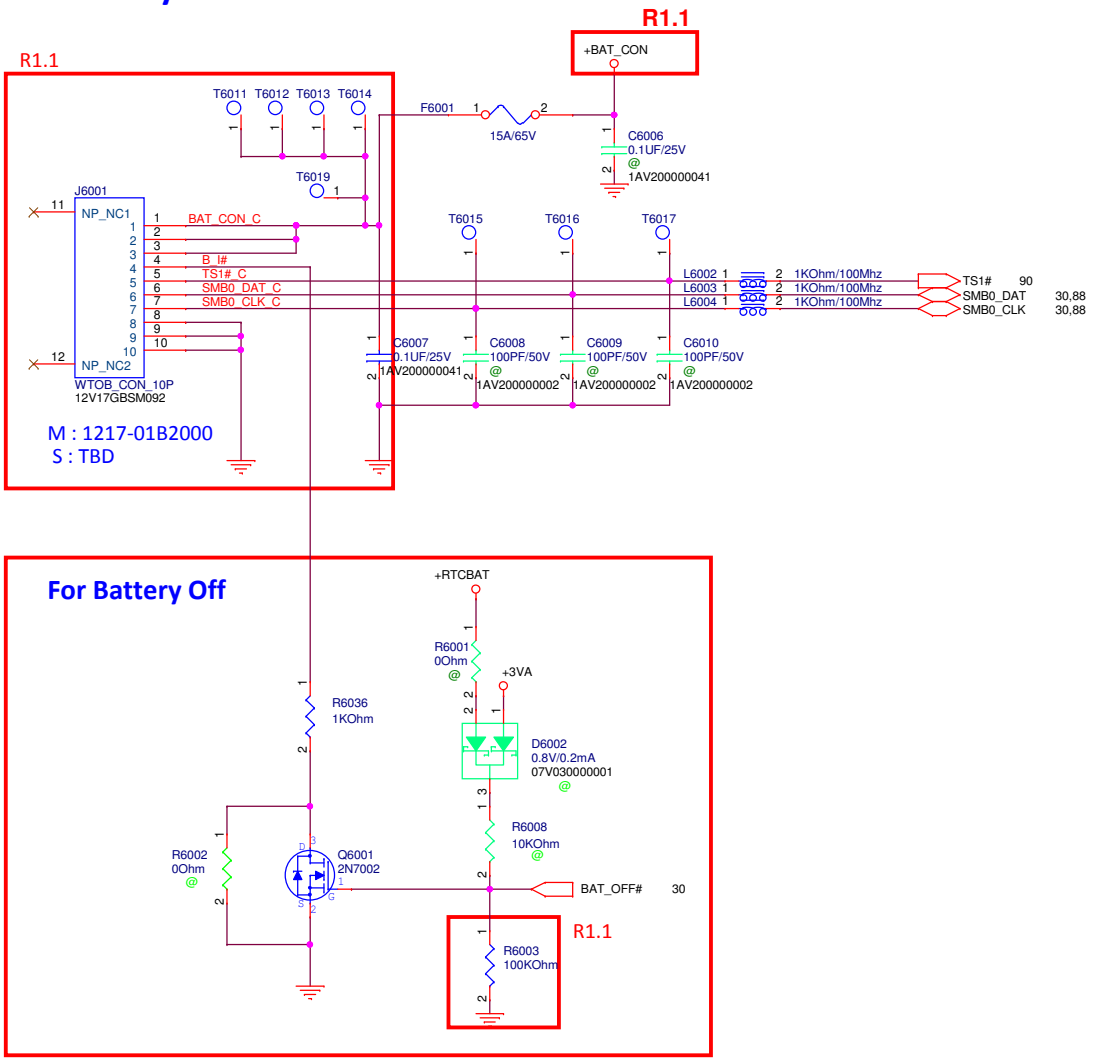
DC IN





M : 1208-01ET000
S : 1208-01C1000

Battery Connector

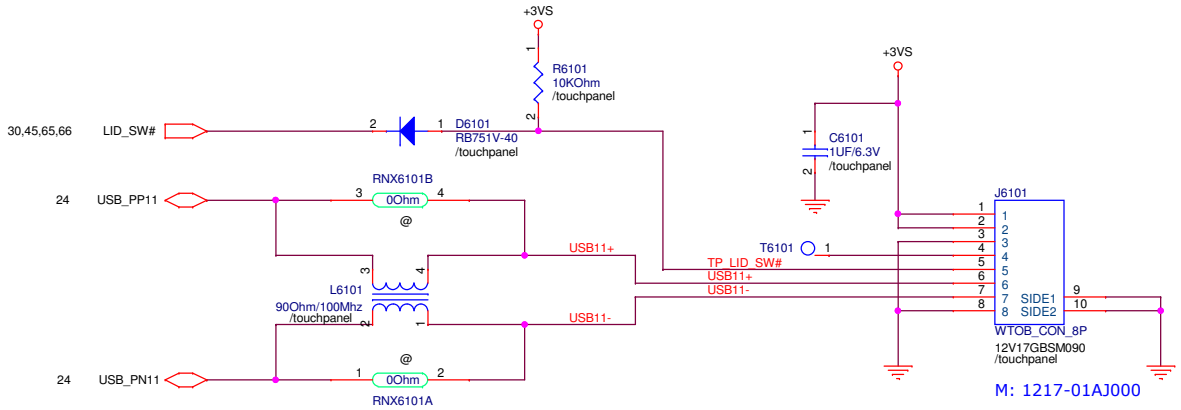


For Battery Off

PEGATRON	Title : DC-IN/ Battery	
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu	
Size: Custom	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 60 of 104	

Touch Pad Module

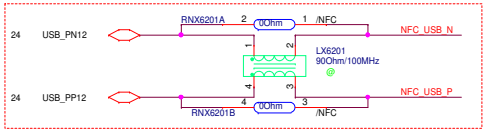
R1.1 add LID_SW# at pin5

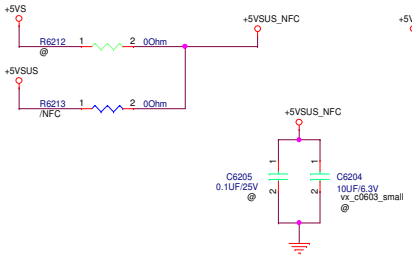


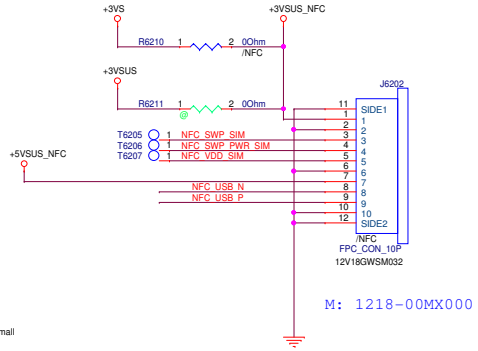
PEGATRON	Title : Touch Panel		
BG1-CSC-HW R&D Dept.5	Engineer:		
Size: Custom	Project Name		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 61 of 104		

R1.1

NFC USB only for non Shark Bay platform







M: 1218-00MX000

PEGATRON	Title : NFC CONN		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 62 of 104		

R1.1

BGA

CPU NUTx4

H6507 CT260B176D146 1308-00BQ000
H6508 CT260B176D146 1308-00BQ000
H6509 CT260B176D146 1308-00BQ000
H6510 CT260B176D146 1308-00BQ000

VGA NUTx2

H6511 CT260B176D146 1308-00BQ000
H6512 CT260B176D146 1308-00BQ000

R1.1

PCB : Screw A

H6529
NP NC GND1 GND2 GND4 GND3
ST335BD118N

PCB : Screw F

H6533
NP NC GND1 GND2 GND4 GND3
RT531X335SBD118N

PCB : Screw B

H6534
CT335B315D217

PCB : Screw G

H6537
D98_D118

PCB : Screw Cx3

H6530 CT276B315D118 S1V2YHCCMZ00
H6532 CT276B315D118 S1V2YHCCMZ00
H6536 CT276B315D118 S1V2YHCCMZ00
H6538 CT276B315D118 S1V2YHCCMZ00

GND PAD H*2

H6502 C236_NP
H6503 C236_NP

PCB : Screw D

H6535
CT276OBDO118X98

PCB : Screw E

H6531
A_GND
NP NC GND1 GND2 GND4 GND3
RT531X335CB335D118N

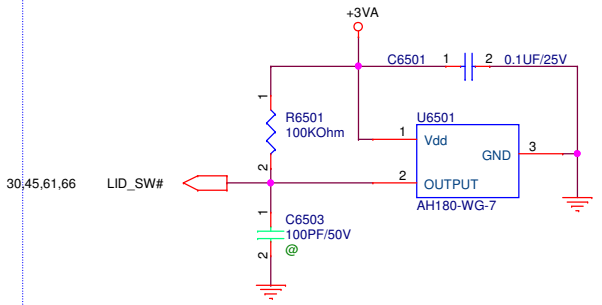
R1.1

FTG STG

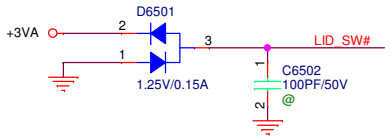
CPU PAD SCREWx4

H6539 CRT331X343B166D146
H6540 CRT331X343B166D146
H6542 CRT331X343B166D146
H6541 CRT331X343B166D146

LID Switch(Hall sensor)



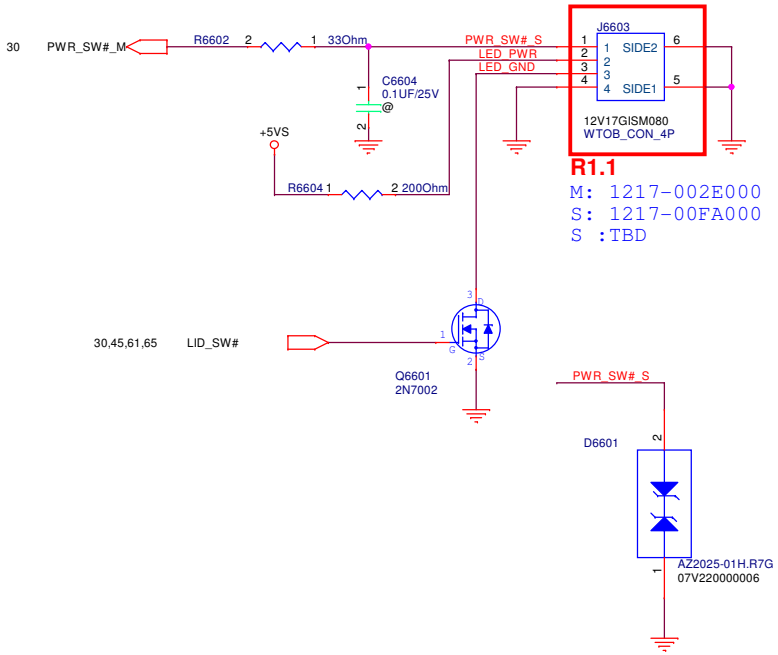
close toU3001



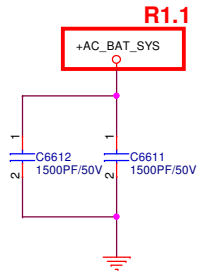
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

PEGATRON	Title: ME_CONN,Skew Hole	
	Engineer: Jim3_Liu	
Size: B	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 65 of 104	

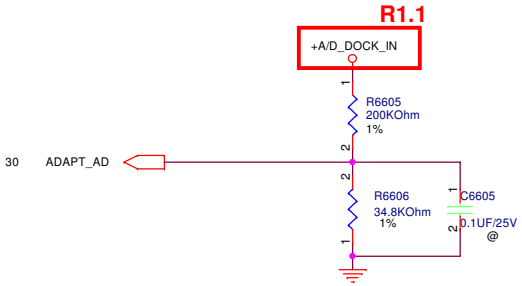
PWR BRD



EMI



ADAPTOR VOLTAGE DETECTOR.



PEGATRON Title : PWR BRD/ IO BRD

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
Custom	VGFTG	1.1

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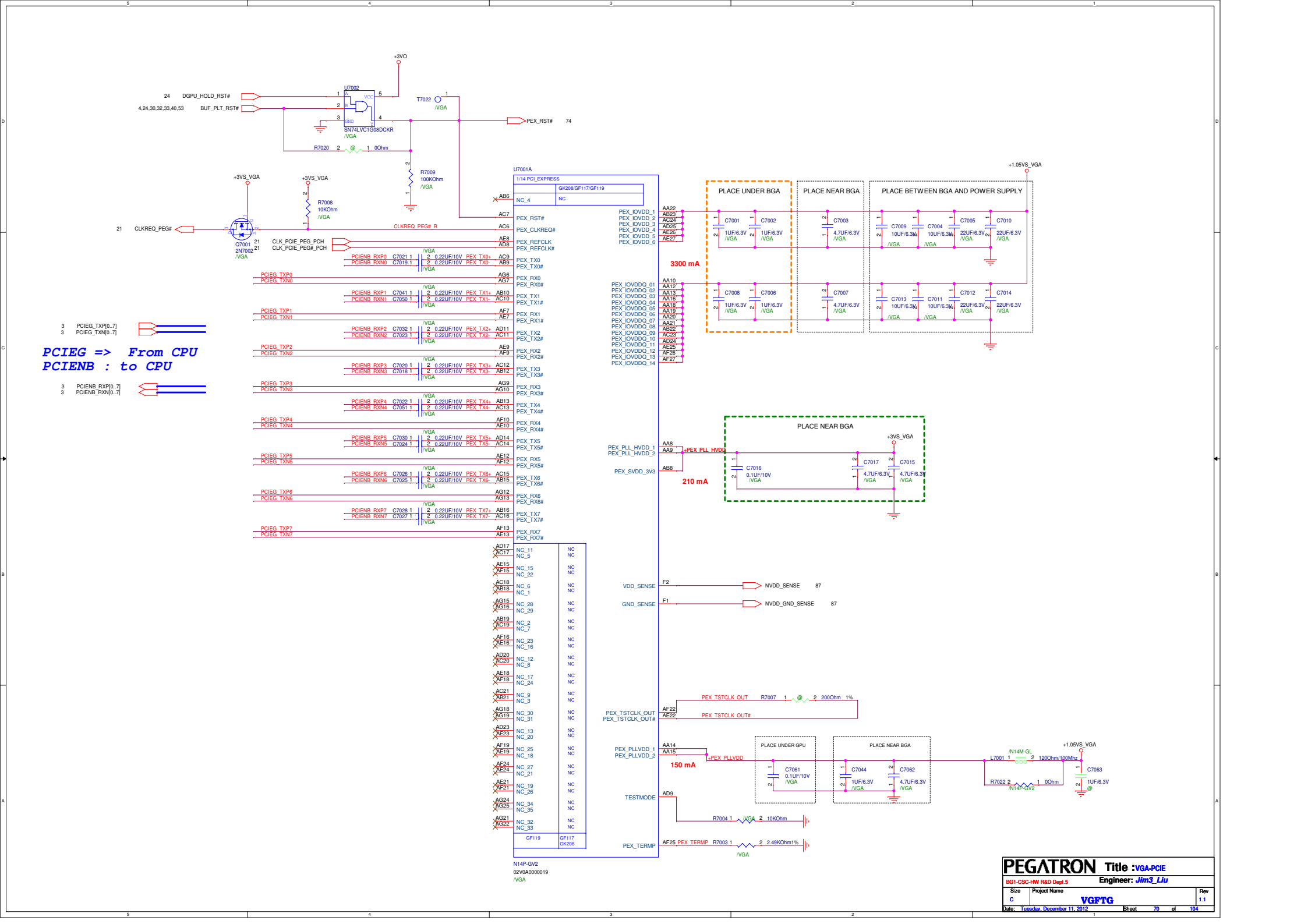
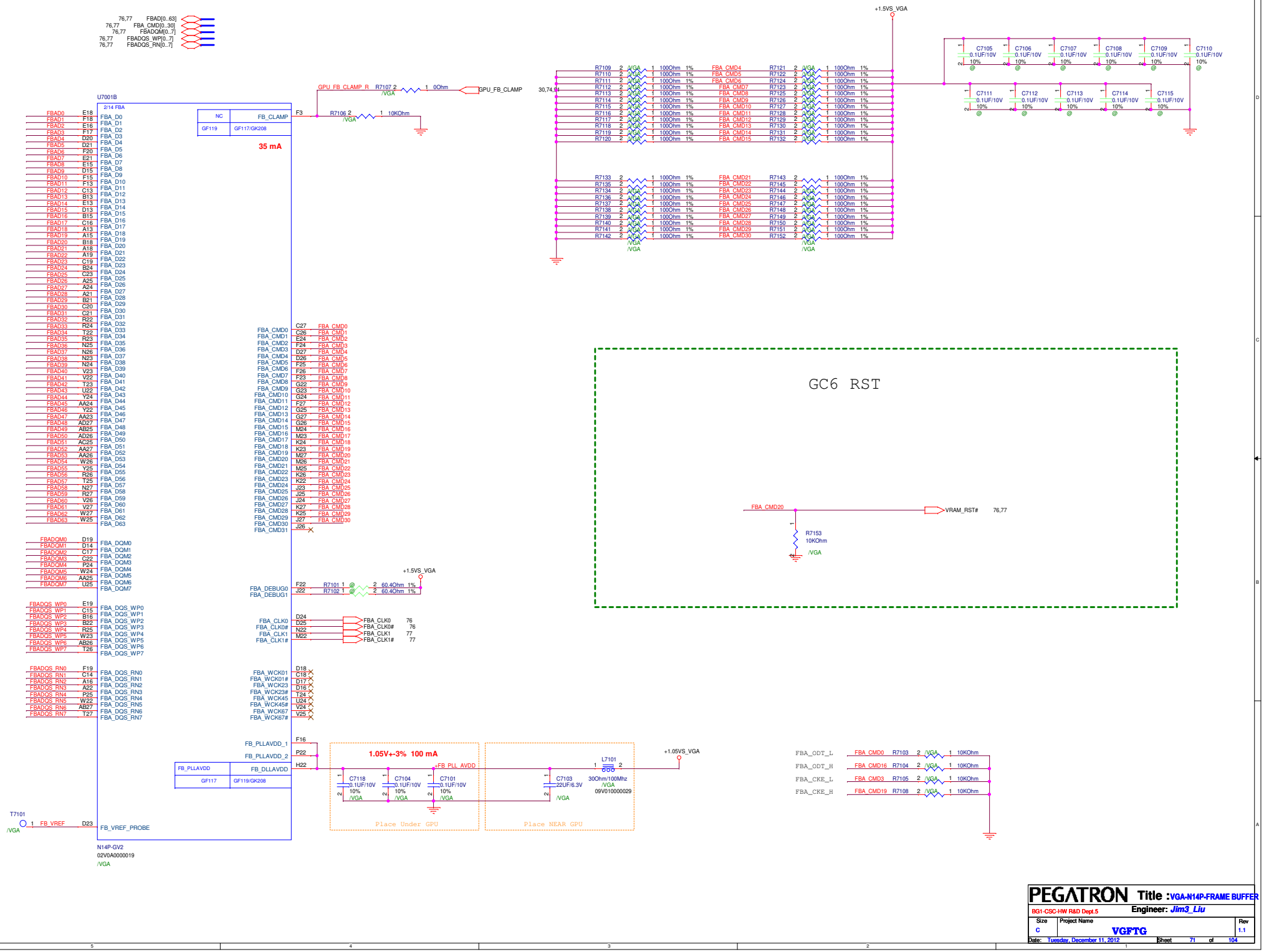


PEGATRON Title : VGA-PCIE

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 70 of 104



PEGATRON Title : VGA-N14P-FRAME BUFFER

BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

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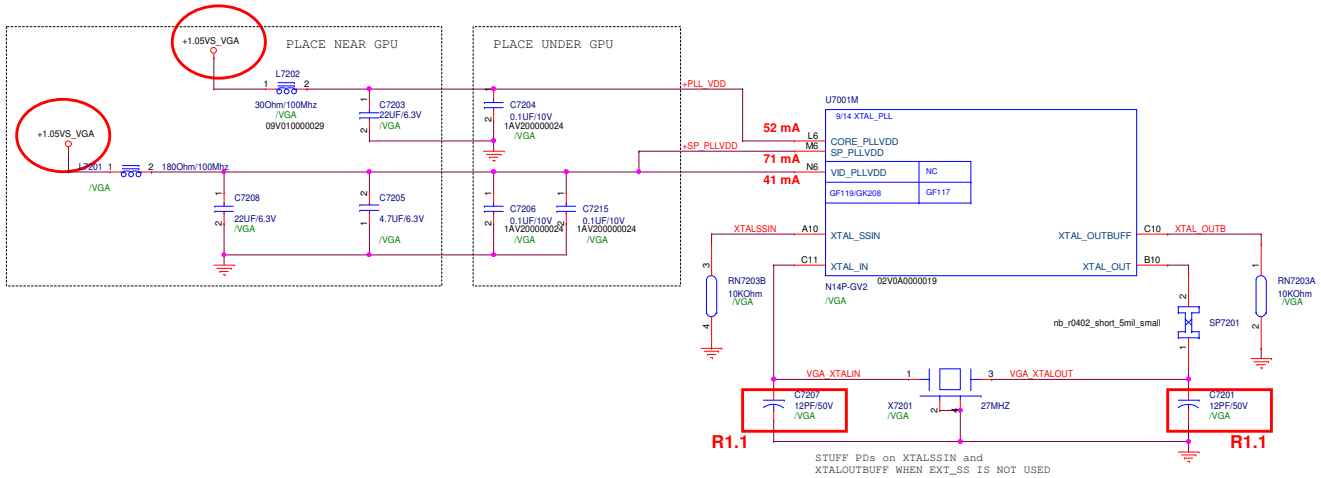
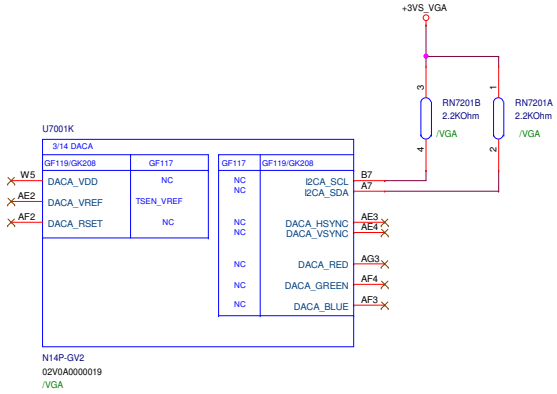




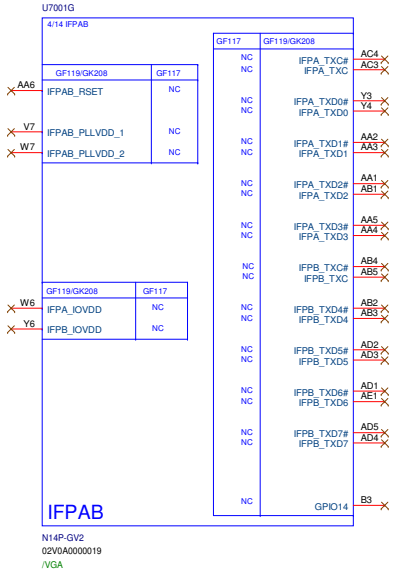
PEGATRON Title : VGA_RGB,XTAL

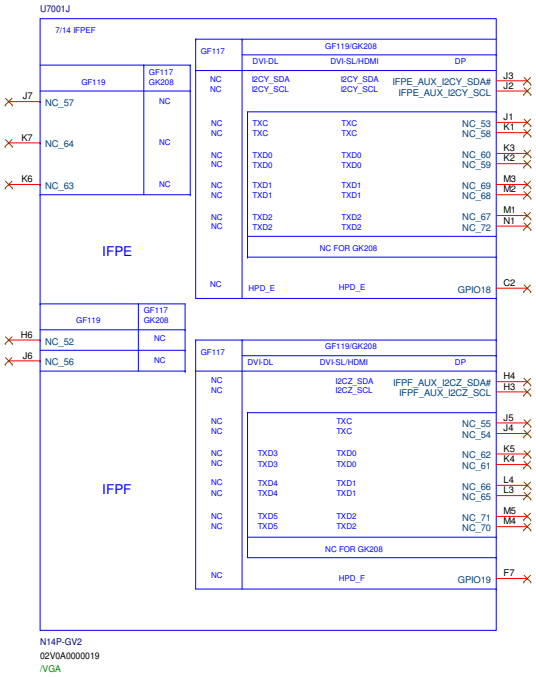
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

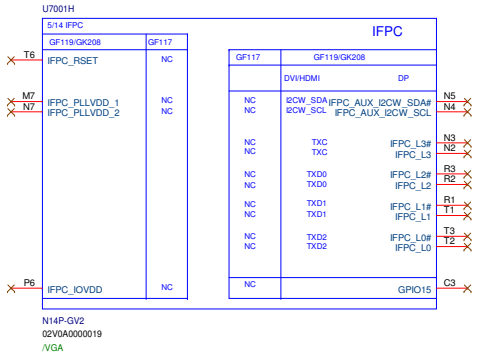
Size	Project Name	Rev
C	VGFTG	1.1

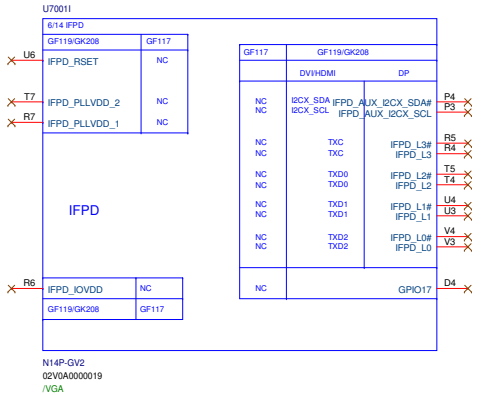
Date: Tuesday, December 11, 2012 Sheet 72 of 104

LVDS

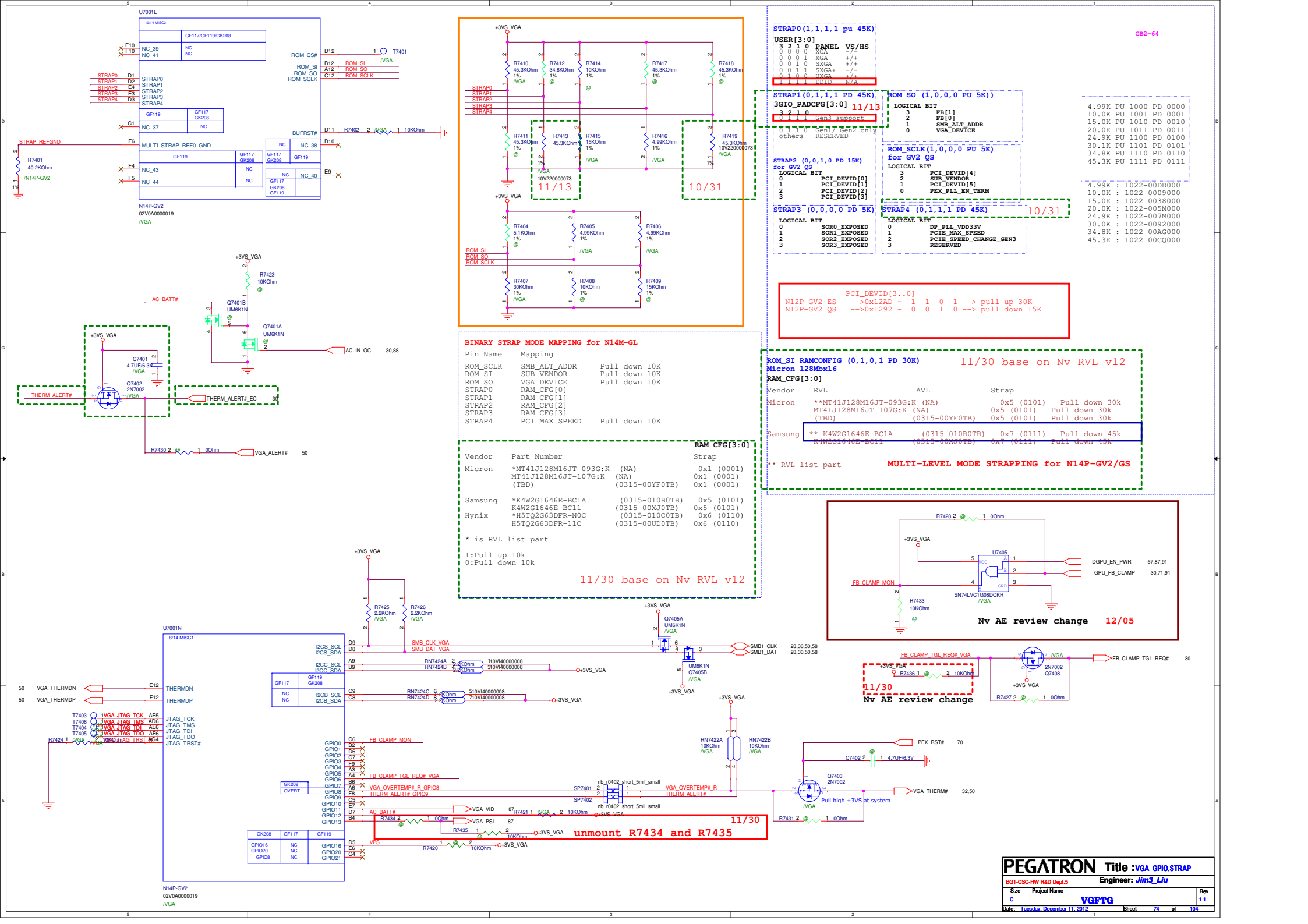


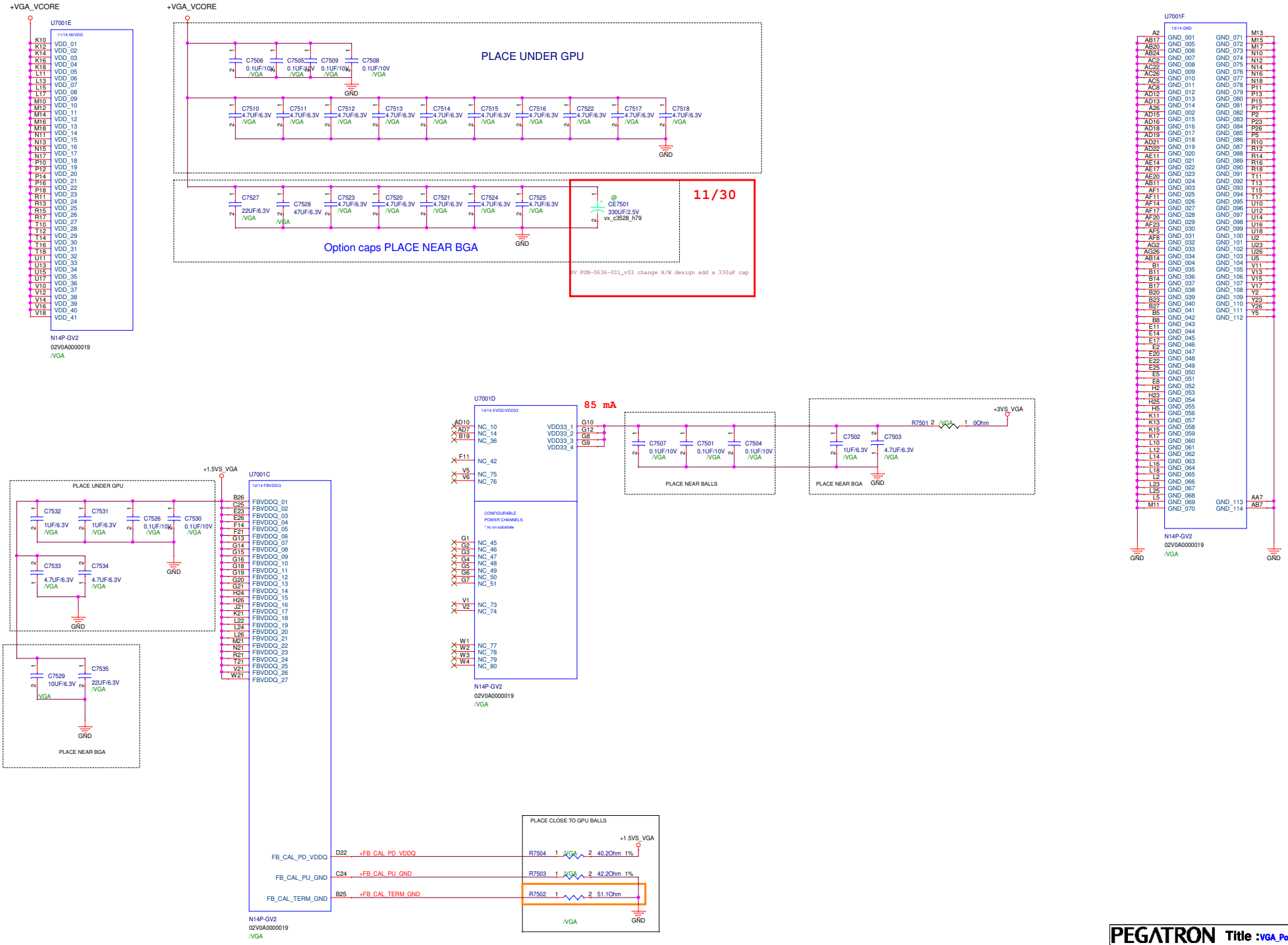






PEGATRON	Title : VGA_LVDS_HDMI		
BG1-CSC-HW R&D Dept.5	Engineer: Jim3_Liu		
Size: C	Project Name: VGFTG		Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 73 of 104		


U7001L
N14P-GV2
02V0A0000019
/VGA
STRAP0(1,1,1,1 pu 45K)
USER[3:0]
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA -/-
0 0 0 1 XGA +/+
0 0 1 0 SXGA +/+
0 0 1 1 SXGA+ -/-
0 1 0 0 UXGA +/+
1 1 1 1 EDID N/A
STRAP1(0,1,1,1 PD 45K)
3GIO_PADCFG[3:0] 11/13
3 2 1 0
0 1 1 1 Gen3 support
others RESERVED
STRAP2 (0,0,1,0 PD 15K)
for GV2 QS
LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
STRAP3 (0,0,0,0 PD 5K)
LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
ROM_SO (1,0,0,0 PU 5K))
LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE
ROM_SCLK(1,0,0,0 PU 5K)
for GV2 QS
LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEX_PLL_EN_TERM
STRAP4 (0,1,1,1 PD 45K) 10/31
LOGICAL BIT
0 DP_PLL_VDD33V
1 PCIE_MAX_SPEED
2 PCIE_SPEED_CHANGE_GEN3
3 RESERVED
GB2-64
4.99K PU 1000 PD 0000
10.0K PU 1001 PD 0001
15.0K PU 1010 PD 0010
20.0K PU 1011 PD 0011
24.9K PU 1100 PD 0100
30.1K PU 1101 PD 0101
34.8K PU 1110 PD 0110
45.3K PU 1111 PD 0111
4.99K : 1022-00DD000
10.0K : 1022-0009000
15.0K : 1022-0038000
20.0K : 1022-005M000
24.9K : 1022-007M000
30.0K : 1022-0092000
34.8K : 1022-00AG000
45.3K : 1022-00CQ000
PCI_DEVID[3..0]
N12P-GV2 ES -->0x12AD ~ 1 1 0 1 --> pull up 30K
N12P-GV2 QS -->0x1292 ~ 0 0 1 0 --> pull down 15K
BINARY STRAP MODE MAPPING for N14M-GL
Pin Name Mapping
ROM_SCLK SMB_ALT_ADDR Pull down 10K
ROM_SI SUB_VENDOR Pull down 10K
ROM_SO VGA_DEVICE Pull down 10K
STRAP0 RAM_CFG[0]
STRAP1 RAM_CFG[1]
STRAP2 RAM_CFG[2]
STRAP3 RAM_CFG[3]
STRAP4 PCI_MAX_SPEED Pull down 10K
RAM_CFG[3:0]
Vendor Part Number Strap
Micron *MT41J128M16JT-093G:K (NA) 0x1 (0001)
MT41J128M16JT-107G:K (NA) 0x1 (0001)
(TBD) (0315-00YF0TB) 0x1 (0001)
Samsung *K4W2G1646E-BC1A (0315-010B0TB) 0x5 (0101)
K4W2G1646E-BC11 (0315-00XJ0TB) 0x5 (0101)
Hynix *H5TQ2G63DFR-N0C (0315-010C0TB) 0x6 (0110)
H5TQ2G63DFR-11C (0315-00UD0TB) 0x6 (0110)
* is RVL list part
1:Pull up 10k
0:Pull down 10k
11/30 base on Nv RVL v12
ROM_SI RAMCONFIG (0,1,0,1 PD 30K)
Micron 128Mbx16
RAM_CFG[3:0]
11/30 base on Nv RVL v12
Vendor RVL AVL Strap
Micron **MT41J128M16JT-093G:K (NA) 0x5 (0101) Pull down 30k
MT41J128M16JT-107G:K (NA) 0x5 (0101) Pull down 30k
(TBD) (0315-00YF0TB) 0x5 (0101) Pull down 30k
Samsung ** K4W2G1646E-BC1A (0315-010B0TB) 0x7 (0111) Pull down 45k
K4W2G1646E-BC11 (0315-00XJ0TB) 0x7 (0111) Pull down 45k
** RVL list part
MULTI-LEVEL MODE STRAPPING for N14P-GV2/GS
Nv AE review change 12/05
11/30
Nv AE review change
unmount R7434 and R7435
11/30
Pull high +3VS at system
PEGATRON Title :VGA_GPIO,STRAP
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size C Project Name VGFTG Rev 1.1
Date: Tuesday, December 11, 2012 Sheet 74 of 104



PEGATRON Title : VGA_Power,GND

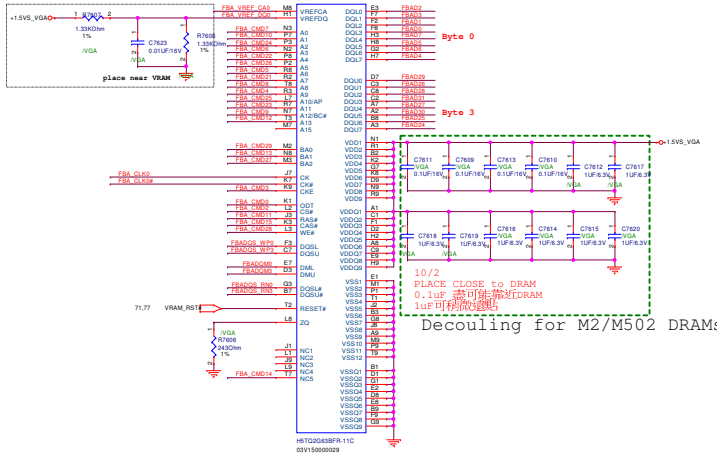
BG1-CSC-HW R&D Dept.5 Engineer: Jim3_Liu

Size	Project Name	Rev
C	VGFTG	1.1

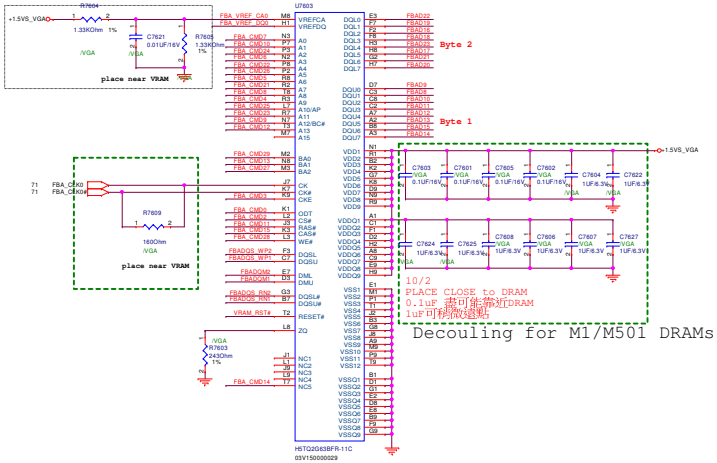
Date: Tuesday, December 11, 2012 Sheet 75 of 104

FBA Partition 31..0 RANK 0

TOP SIDE --- M2



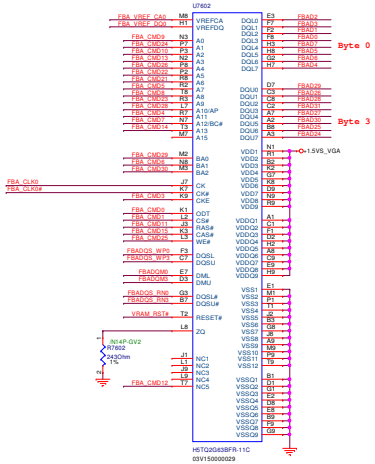
TOP SIDE --- M1



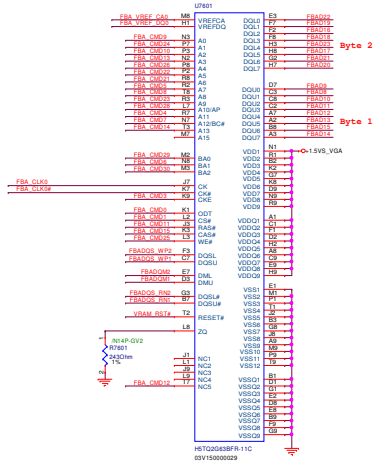
FBA Partition 31..0 RANK 1

BOT SIDE --- M502

10/3
For N14P-GV2



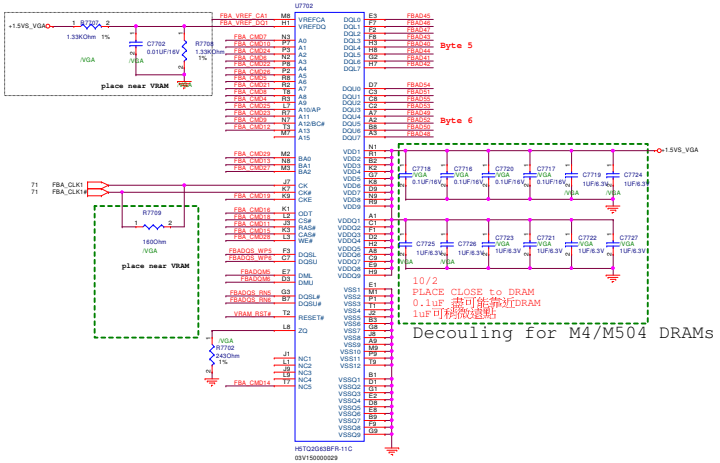
BOT SIDE --- M501



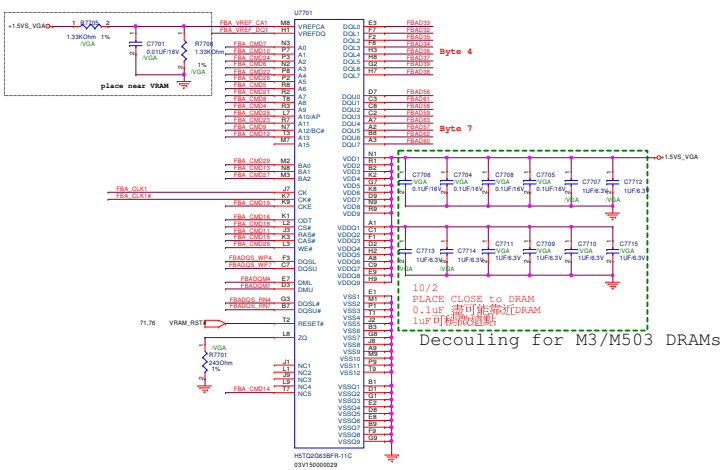
PEGATRON Title : VGA_FBA_HYNIX DDR3 [31:0]
SGI -CSC-HW R&D Dept.5 Engineer: Jim3_Liu
Size: D | Project Name: VGFTG | Rev: 1.1
Date: Tuesday, December 11, 2012 | Sheet 76 of 104

FBA Partition 63..32 RANK 0

TOP SIDE --- M4



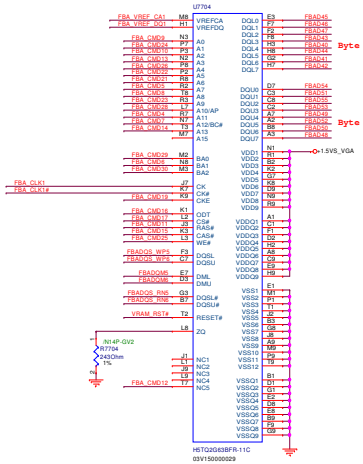
TOP SIDE --- M3



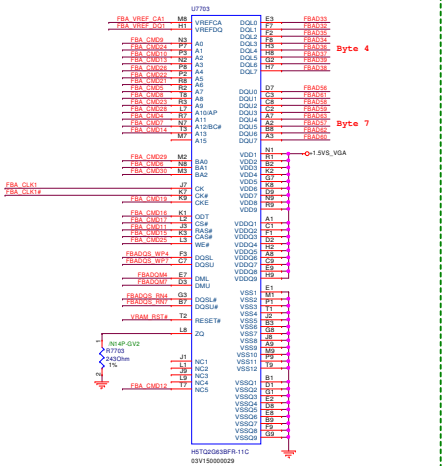
FBA Partition 63..32 RANK 1

BOT SIDE --- M504

10/3
For N14P-GV2

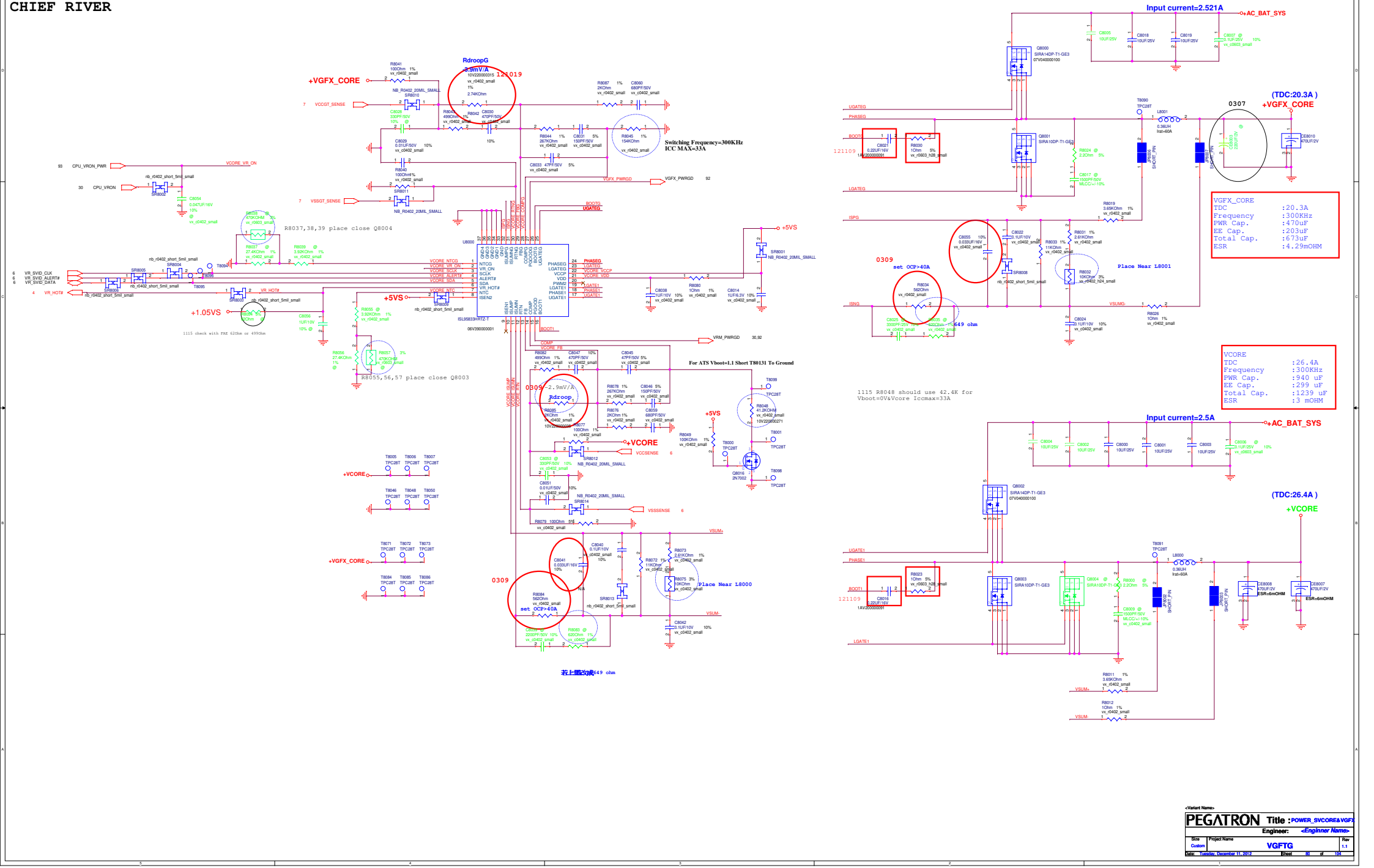


BOT SIDE --- M503

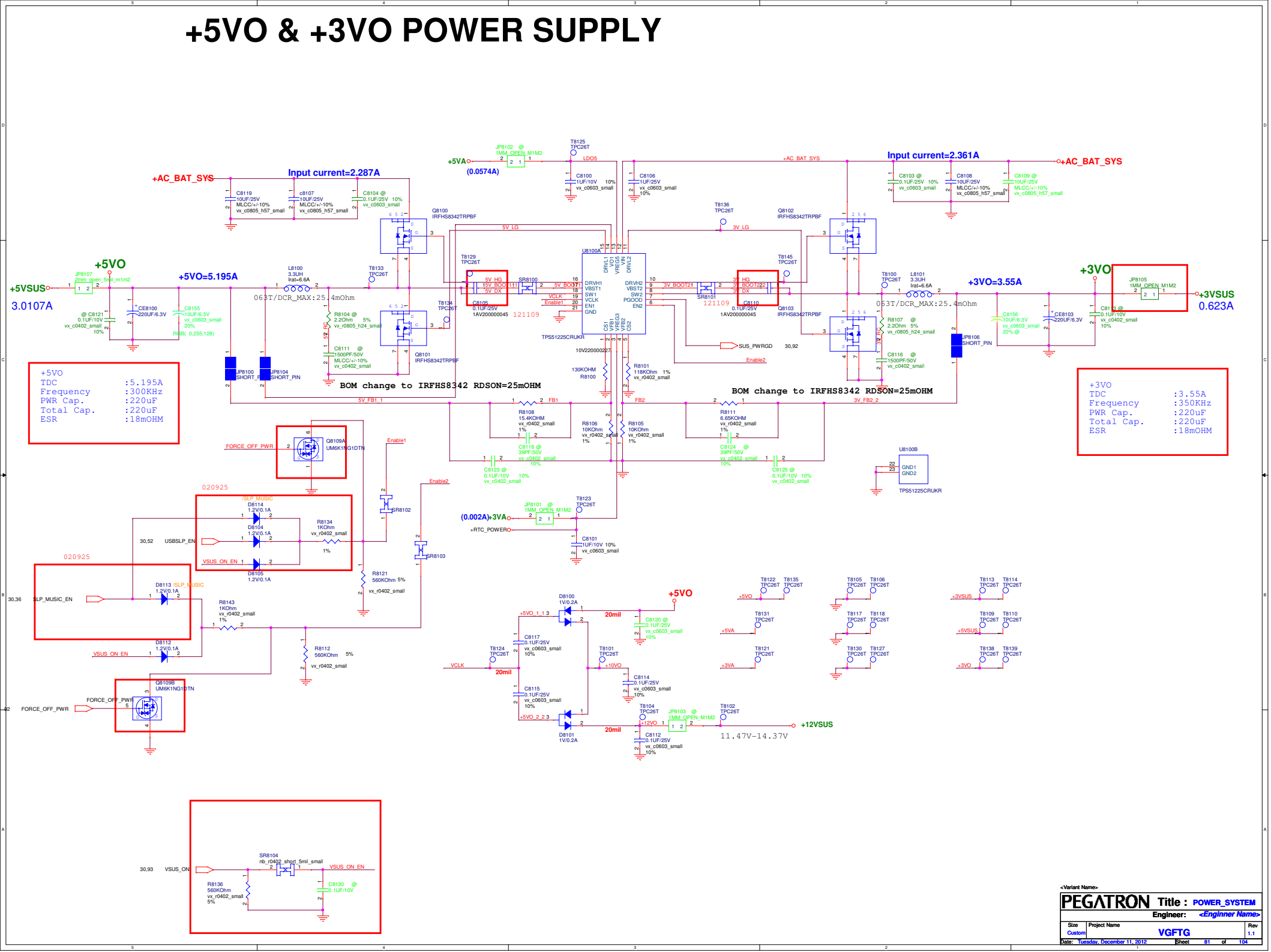


PEGATRON Title : VGA_FBA_HYNIX DDR3 [63:32]
SG1.ICSCHWS Engineer: Jim3_Liu
Size: D | Project Name: VGFTG | Rev: 1.1
Date: Tuesday, December 11, 2012 | Sheet 77 of 164

CHIEF RIVER


+VGFX_CORE
RdroopG
3.9mV/A
121019
Switching Frequency=300KHz
ICC MAX=33A
R8037,38,39 place close Q8004
R8055,56,57 place close Q8003
ISL95839HRTZ-T
06V390000001
+5VS
+1.05VS
+VCORE
+VGFX_CORE
For ATS Vboot=1.1 Short T80131 To Ground
0309
Place Near L8000
set OCP>40A
649 ohm
Input current=2.521A
+AC_BAT_SYS
(TDC:20.3A)
0307
VGFX_CORE
TDC :20.3A
Frequency :300KHz
PWR Cap. :470uF
EE Cap. :203uF
Total Cap. :673uF
ESR :4.29mOHM
Place Near L8001
VCORE
TDC :26.4A
Frequency :300KHz
PWR Cap. :940 uF
EE Cap. :299 uF
Total Cap. :1239 uF
ESR :3 mOHM
1115 R8048 should use 42.4K for
Vboot=0V&Vcore Iccmax=33A
Input current=2.5A
(TDC:26.4A)
+VCORE
ESR=6mOHM
PEGATRON
Title : POWER_SVCORE&VGFX
Engineer: <Engineer Name>
Project Name
VGFTG
Rev 1.1
Date: Tuesday, December 11, 2012
Sheet 80 of 104

+5VO & +3VO POWER SUPPLY



<Variant Name>

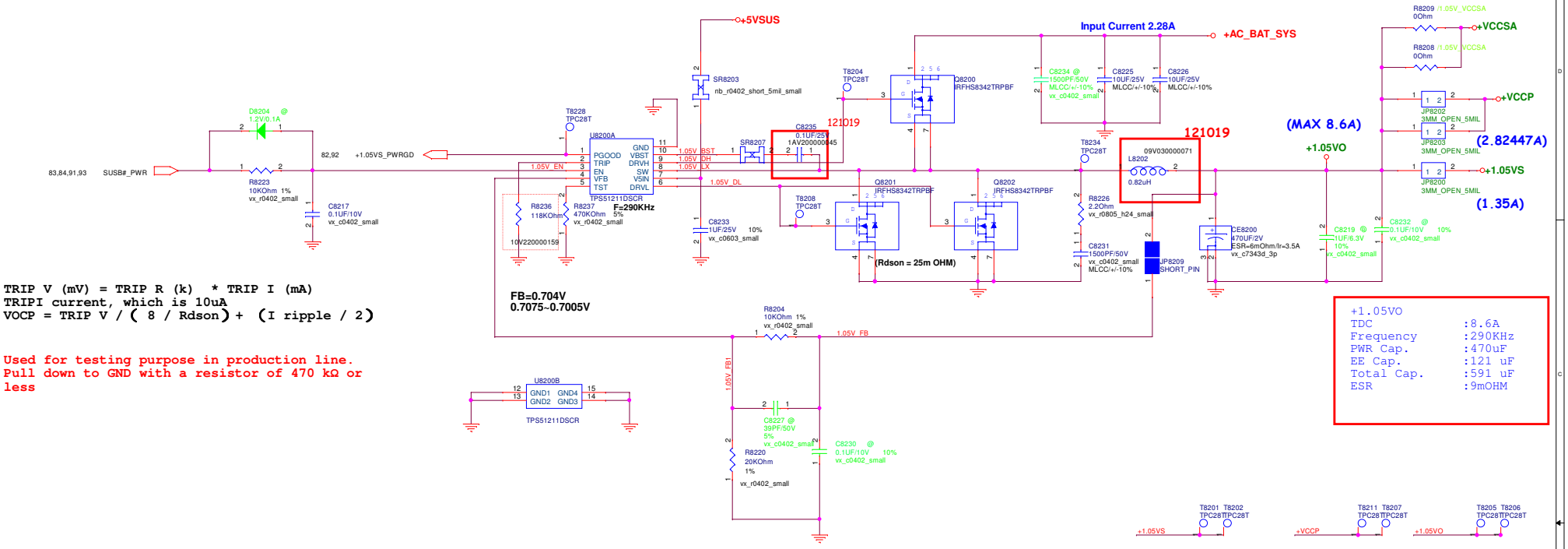
PEGATRON Title : POWER_SYSTEM

Engineer: <Engineer Name>

Size: Custom | Project Name: VGFTG | Rev: 1.1

Date: Tuesday, December 11, 2012 | Sheet 81 of 104

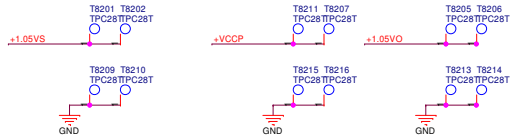
+1.05VO POWER SUPPLY



TRIP V (mV) = TRIP R (k) * TRIP I (mA)
TRIPI current, which is 10uA
VOCP = TRIP V / (8 / Rdson) + (I ripple / 2)

Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less

+1.05VO	
TDC	:8.6A
Frequency	:290KHz
PWR Cap.	:470uF
EE Cap.	:121 uF
Total Cap.	:591 uF
ESR	:9mOHM

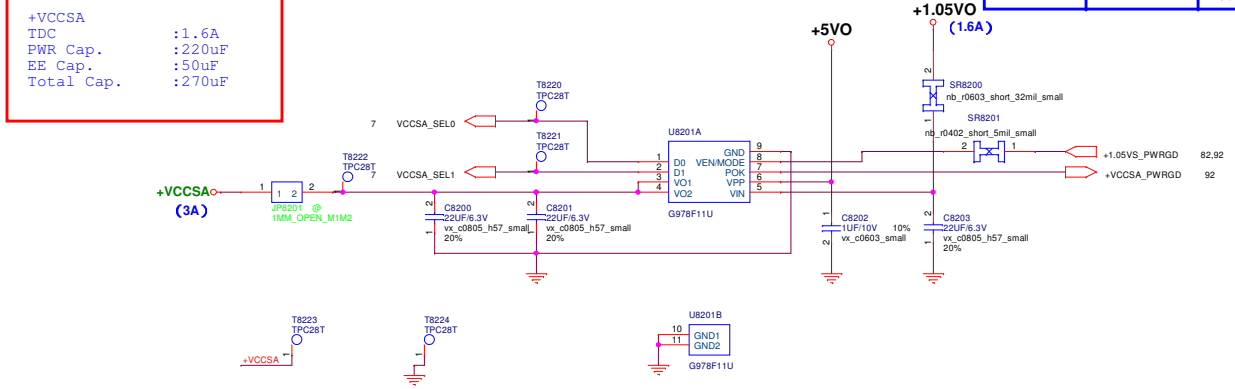


IVB VCCSA POWER SUPPLY

For Chief River (Vout = +-1.5%)

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

+VCCSA	
TDC	:1.6A
PWR Cap.	:220uF
EE Cap.	:50uF
Total Cap.	:270uF



<Variant Name>

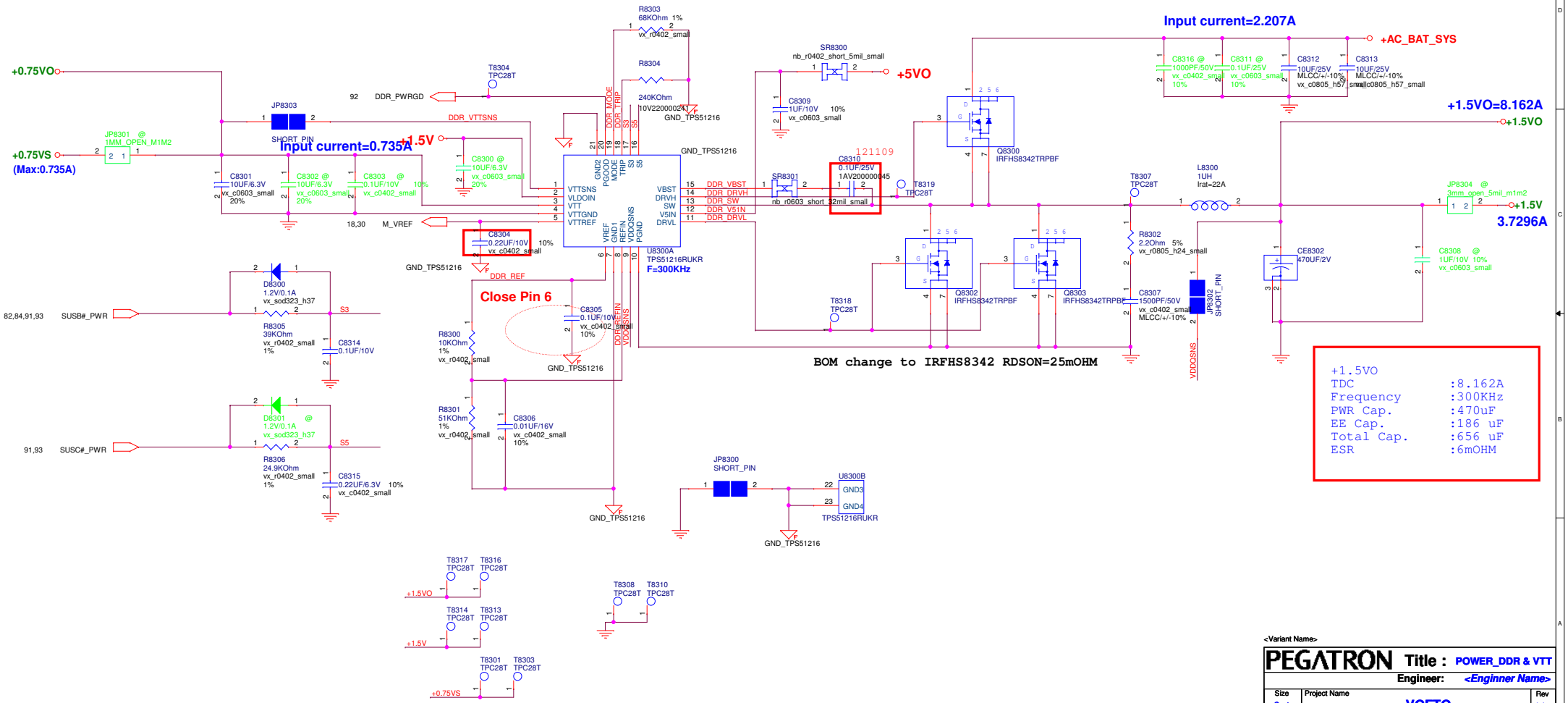
PEGATRON Title : POWER_+1.05VS

Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 82 of 104

DDR & VTT POWER SUPPLY



<Variant Name>

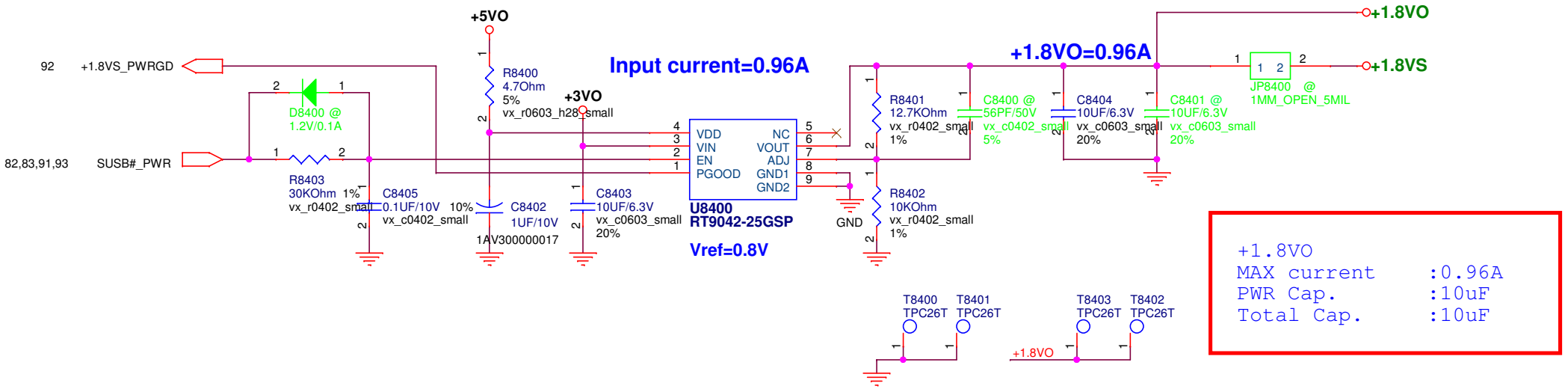
PEGATRON Title : POWER_DDR & VTT

Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 83 of 104

+1.8VS POWER SUPPLY



+1.8VO
MAX current :0.96A
PWR Cap. :10uF
Total Cap. :10uF

<Variant Name>

PEGATRON Title : POWER_+1.8VS

Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 84 of 104

<Variant Name>
<Engineer Name>

PEGATRON Title : N/A

Engineer:

Size	Project Name	Rev
A4		1.1

Date: Tuesday, December 11, 2012 Sheet 85 of 104

<Variant Name>

PEGATRON

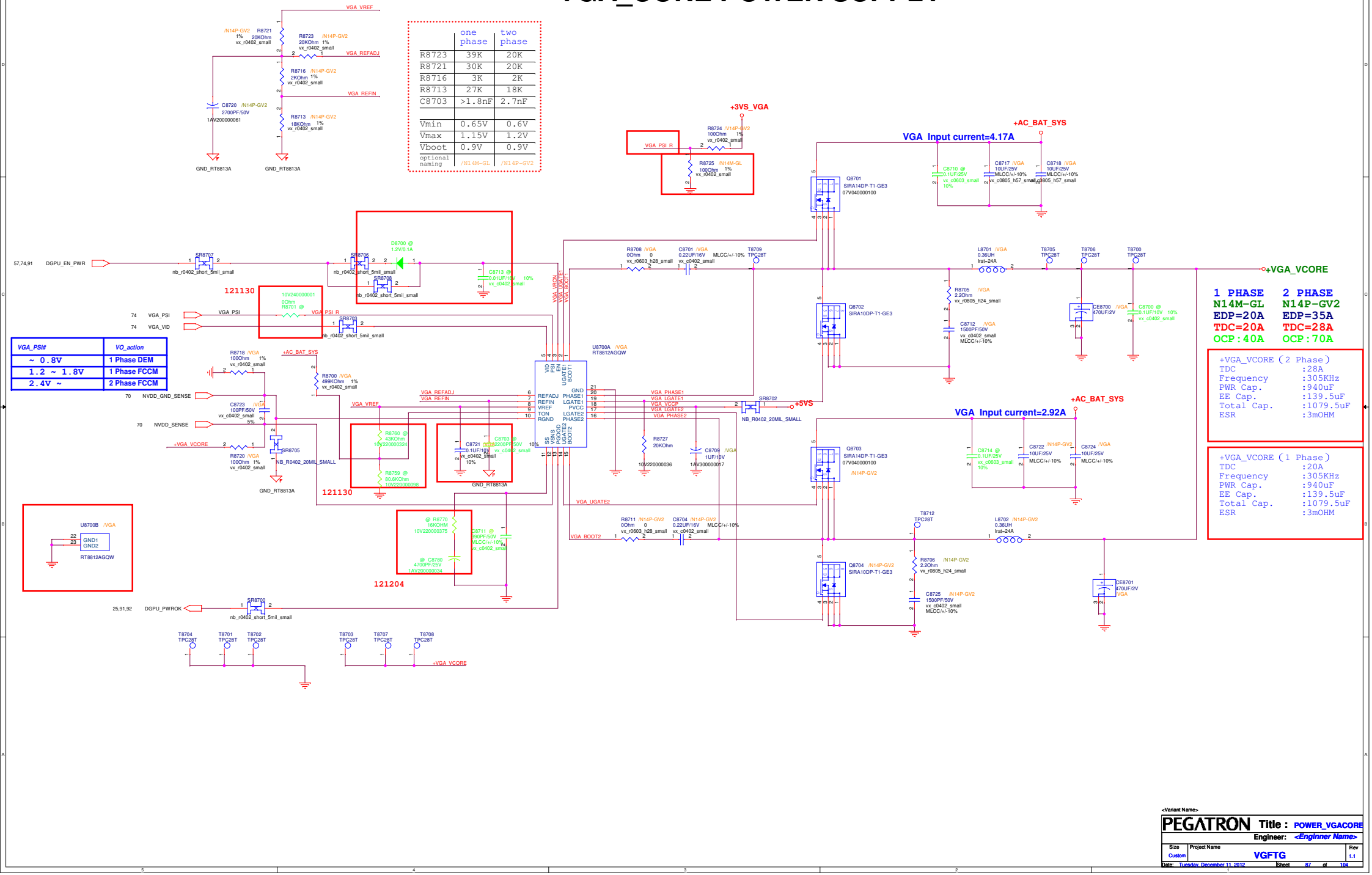
Title : POWER_1.5VS

Engineer: *<Enginner Name>*

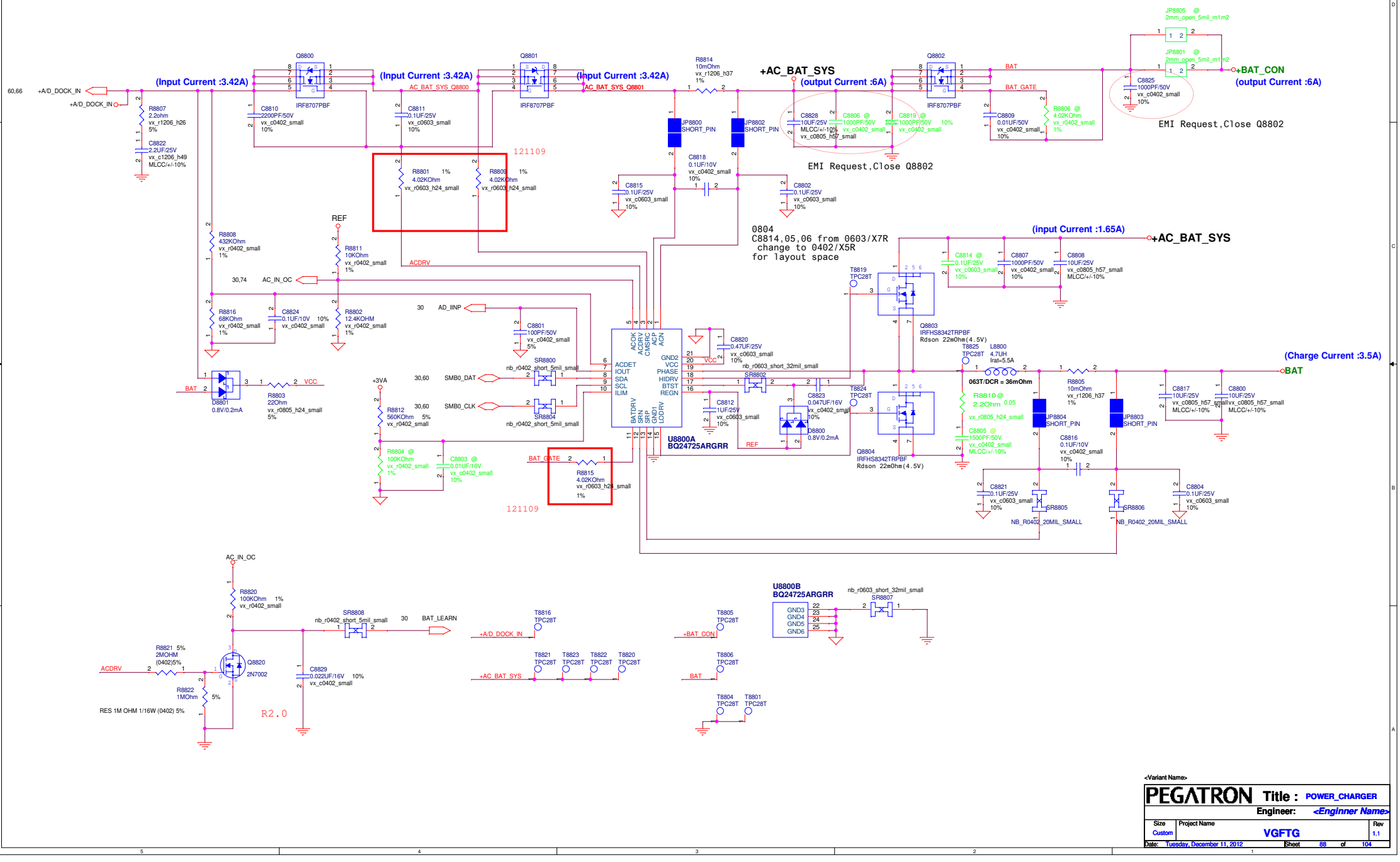
Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 86 of 104

VGA_CORE POWER SUPPLY



BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: <Enginner Name>

Size: Custom | Project Name: VGFTG | Rev: 1.1

Date: Tuesday, December 11, 2012 | Sheet 88 of 104

<Variant Name>

PEGATRON

Title : POWER_N/A

Engineer: *<Enginner Name>*

Size	Project Name	Rev
Custom	VGFTG	1.1

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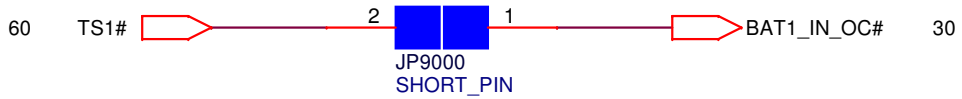
BATTERY IN DETECT



<Variant Name>

PEGATRON

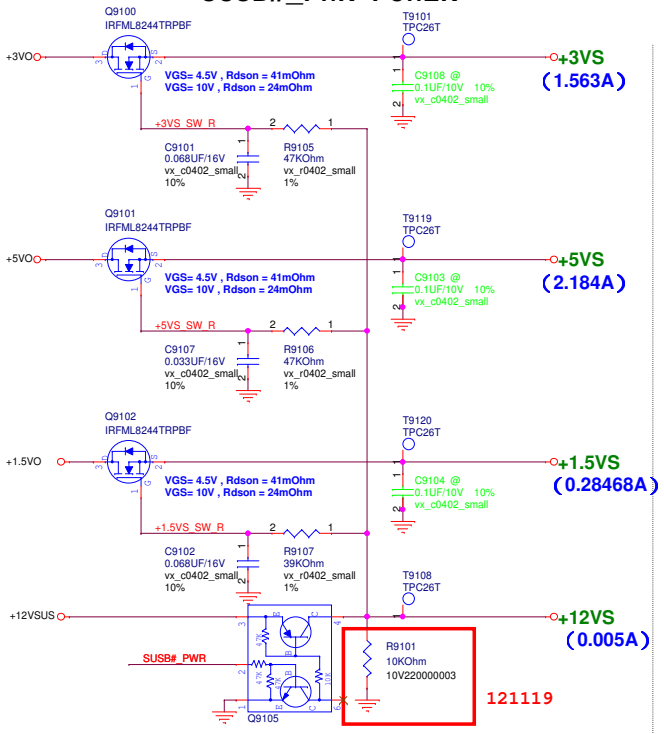
Title : POWER_DETECT

Engineer: *<Enginner Name>*

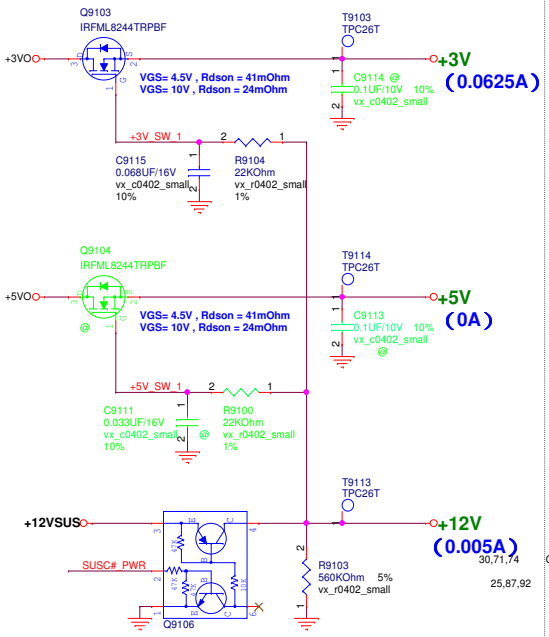
Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 90 of 104

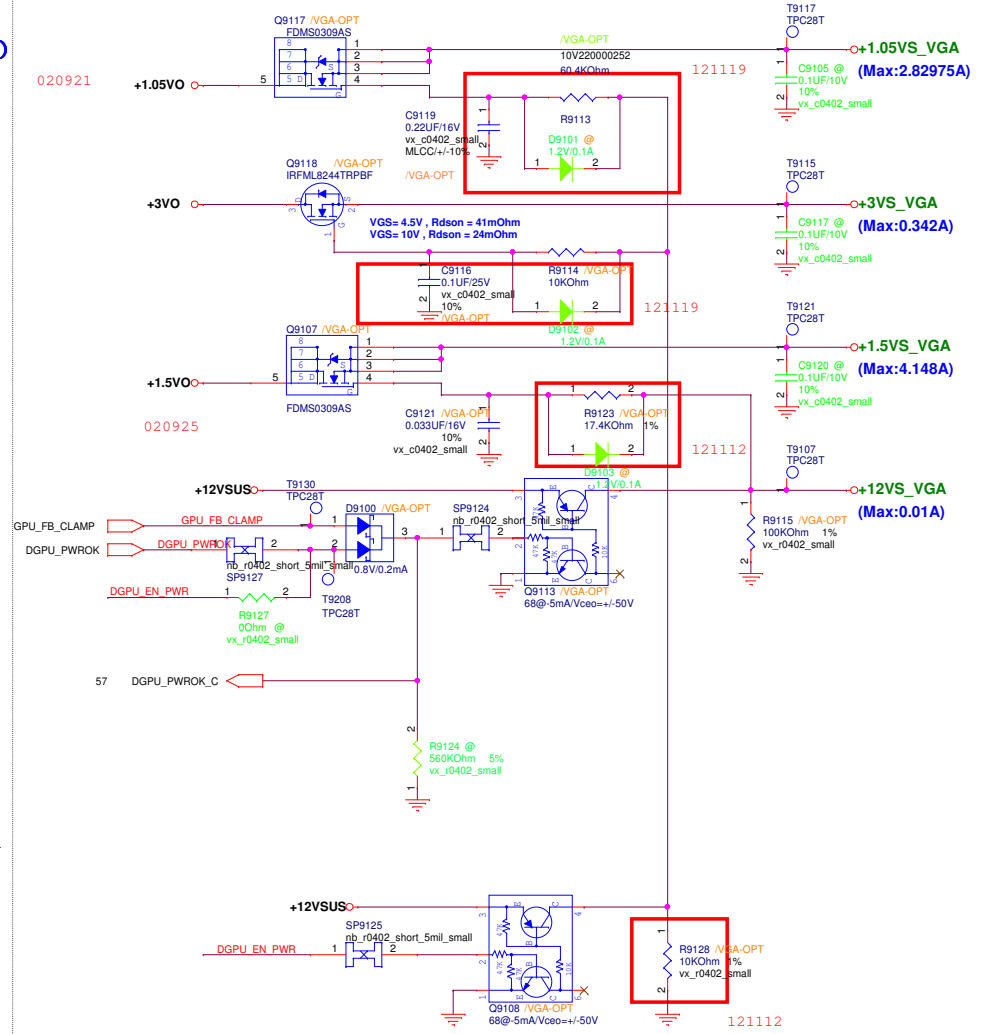
SUSB#_PWR POWER



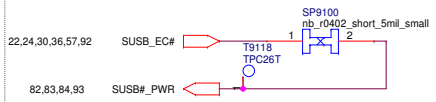
SUSC#_PWR POWER



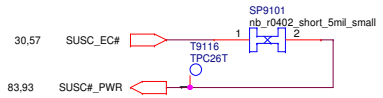
DSC#_PWR POWER(DGPU)



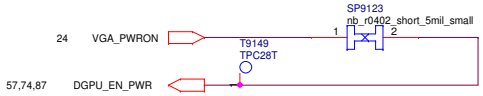
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



<Variant Name>

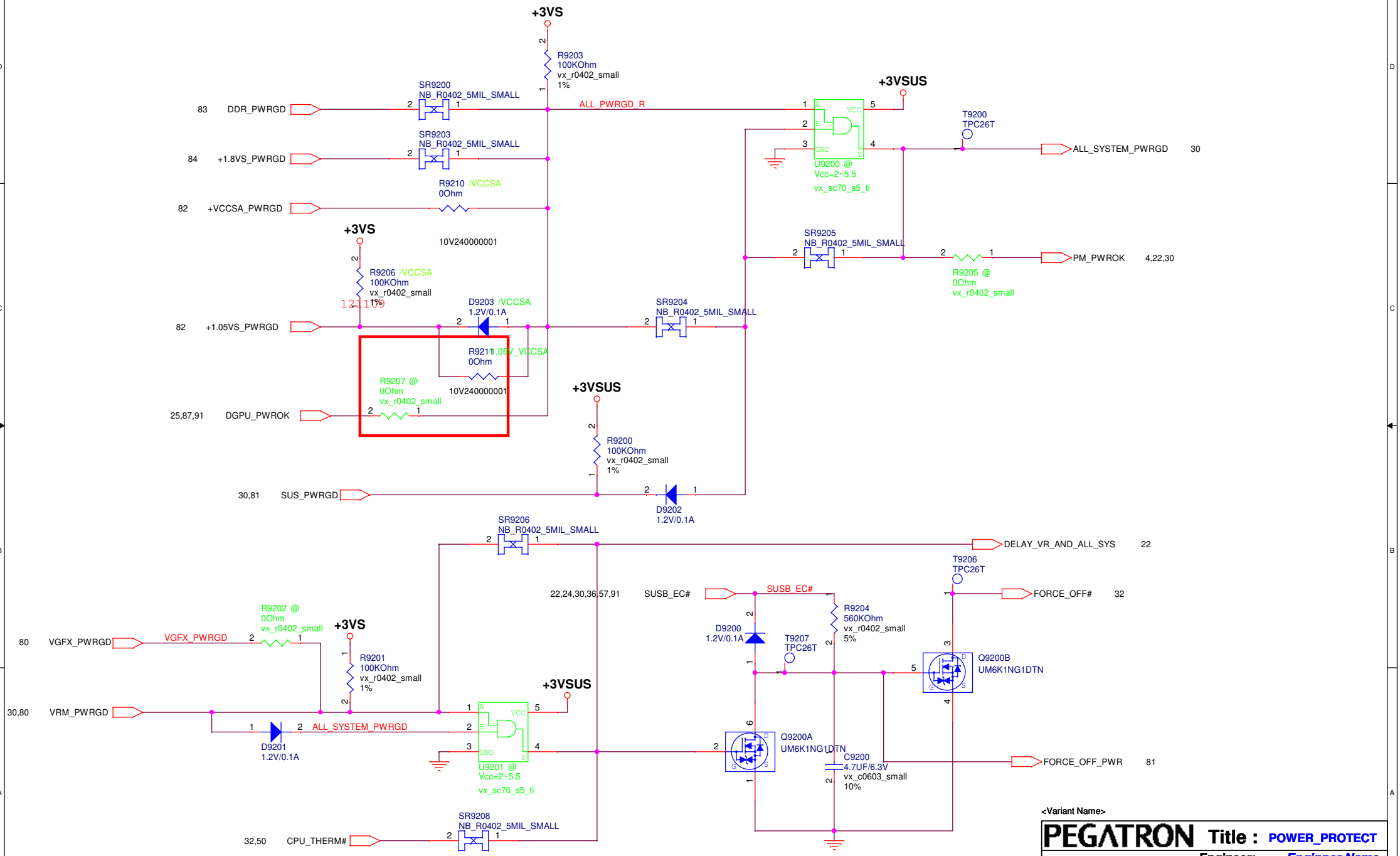
PEGATRON Title : POWER_LOAD SWITCH

Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 91 of 104

POWER GOOD DETECTER



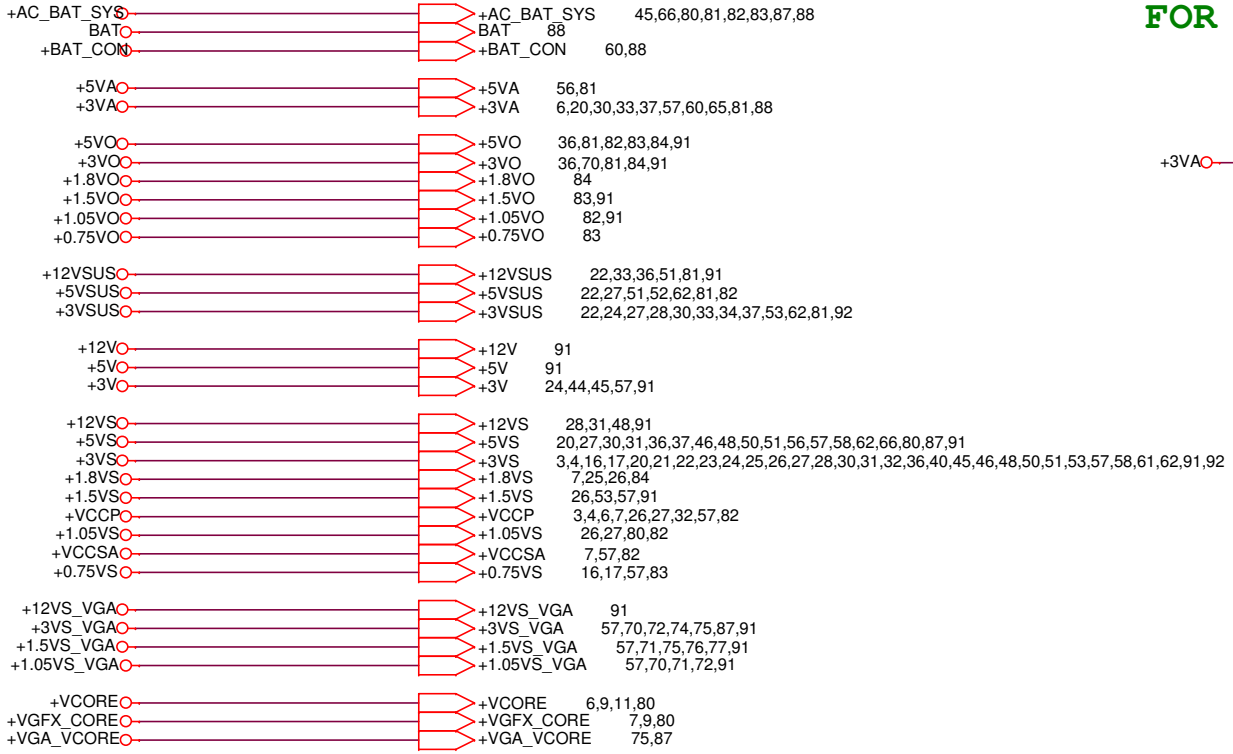
<Variant Name>

PEGATRON Title : POWER_PROTECT

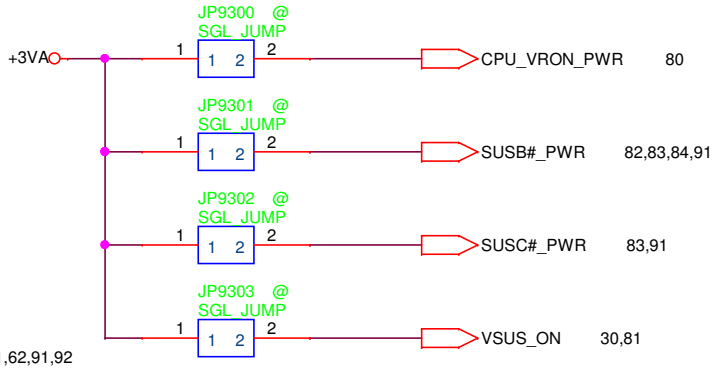
Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 92 of 104



FOR POWER TEST



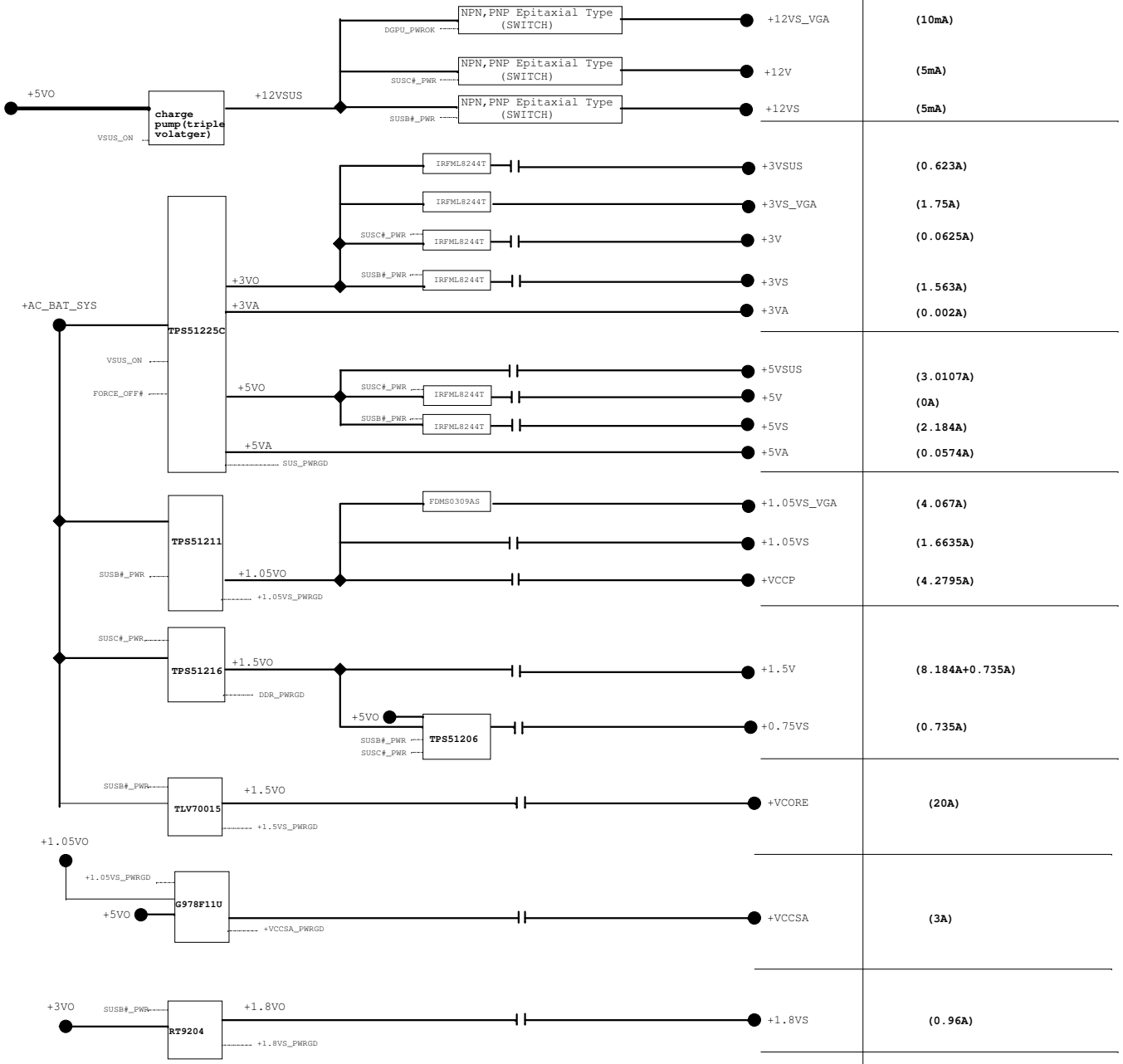
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: <Enginner Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 93 of 104



<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: <Engineer Name>

Size	Project Name	Rev
Custom	VGFTG	1.1

Date: Tuesday, December 11, 2012 Sheet 84 of 104

modify notice

Version	Date	Description

PEGATRON Title : Power History

Engineer: Kelly Liu

Size: Project Name: VGFTG Rev: 1.0

Date: Tuesday, December 11, 2012 Sheet 36 of 36

PEGATRON Title : FRAME BUFFER C

BG1-CSC-HW R&D Dept.5 Engineer: *Keby Liu*

Size	Project Name	Rev
C	VGFTG	1.1

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PEGATRON Title : ****

BG1-CSC-HW R&D Dept.5 Engineer: Keby Liu

Size	Project Name	Rev
Custom	VGFTG	1.1

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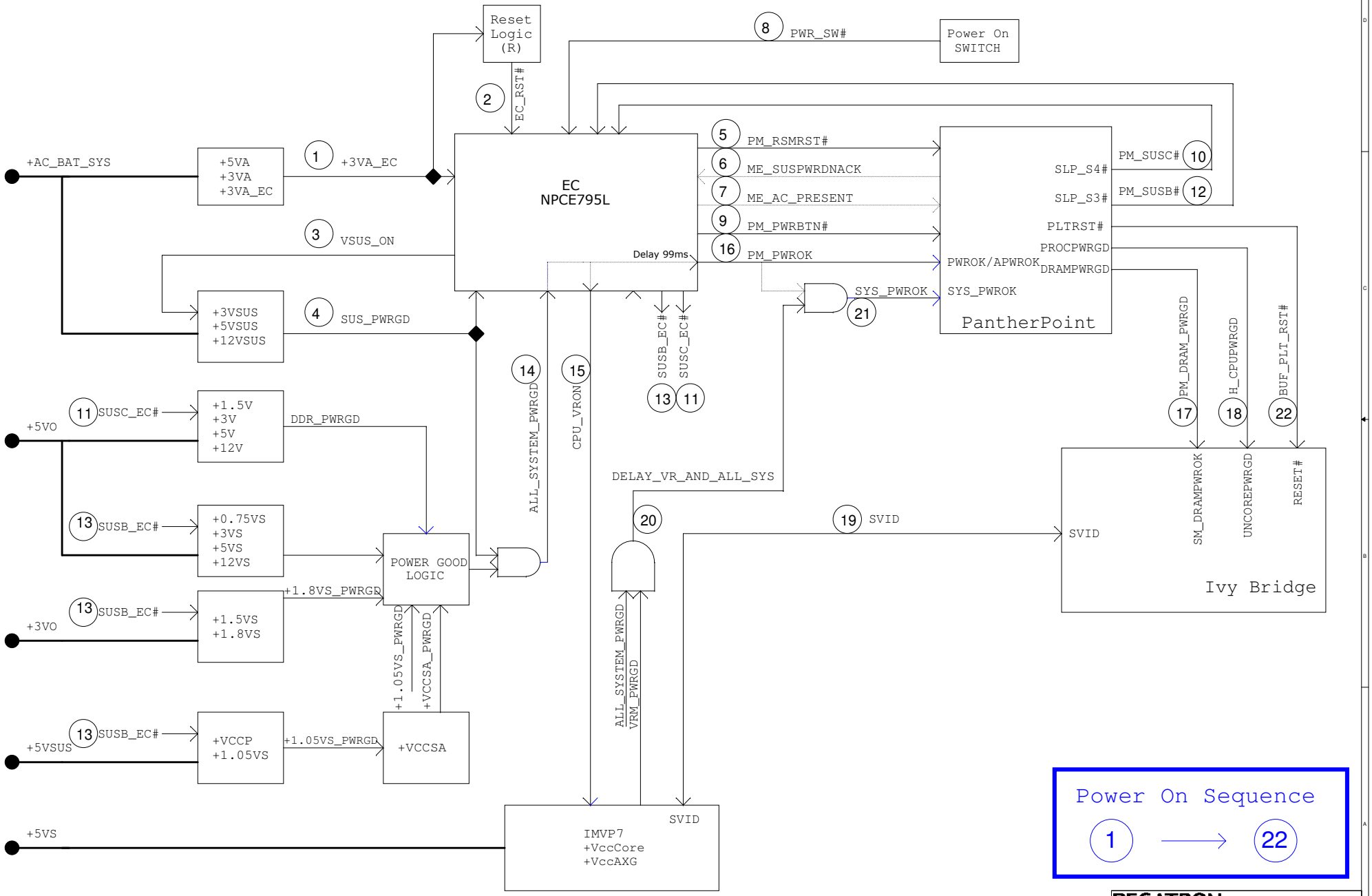
Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]



Power On Sequence

1 → 22

PEGATRON Title : Power On Sequence

BG1-CSC-HW R&D Dept.5 Engineer: Keby Liu

Size	Project Name	Rev
C	VGFTG	1.1

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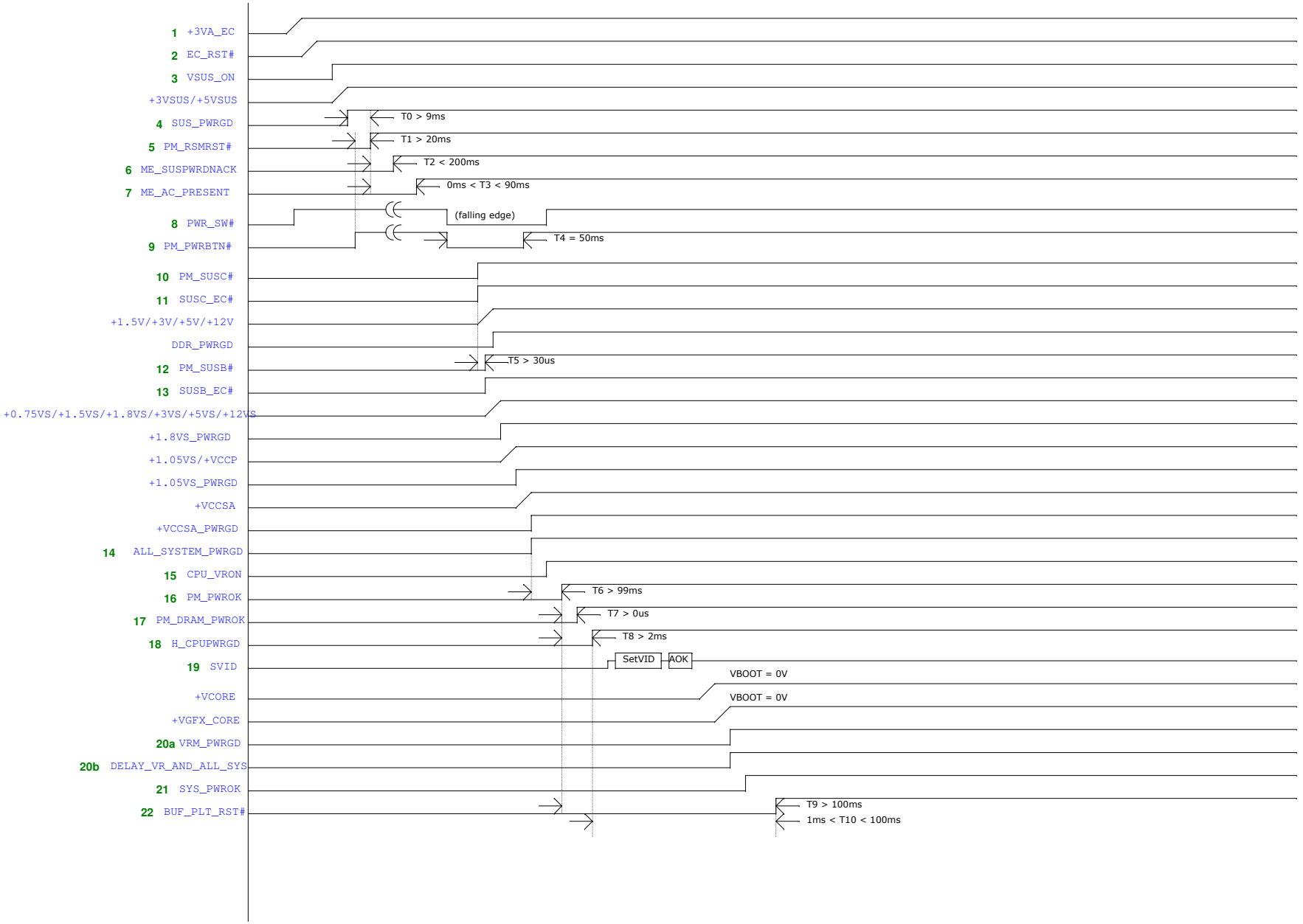
Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]



PEGATRON	Title : Power On Timing	
BG1-CSC-HW R&D Dept.5	Engineer: Keby Liu	
Size: C	Project Name: VGFTG	Rev: 1.1
Date: Tuesday, December 11, 2012	Sheet 99 of 104	