Compal Confidential

2014 S-series(400series) Rolo/Reeses/Raisinet

INTEL Sharkbay & Crescent bay ULT –U processor with DDR3L

Date : 2014/02/18

Version 0.5

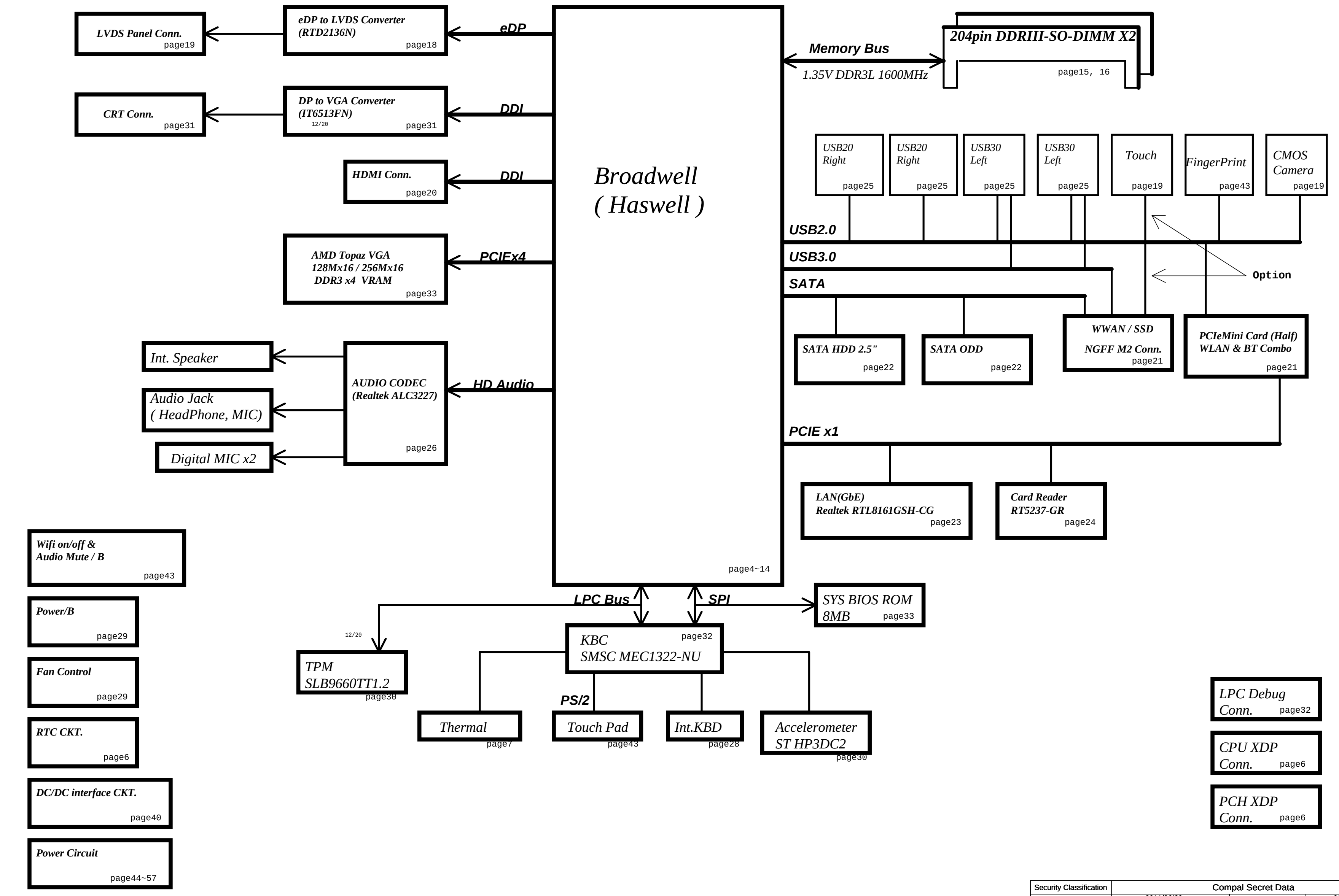
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: Cover Page		
				Size: B	Document Number: LA-B181P	Rev: 0.5
				Date: Tuesday, March 25, 2014	Sheet 1 of 62	

Compal Confidential

Model Name :

Intel Broadwell U / Haswell Block Diagram

Project Name :



CPU DC/DC TPS51622ARSMR	50~51
INPUTS	OUTPUTS
B+	VCC_VORE

SYSTEM DC/DC RT8243AZQW	47
INPUTS	OUTPUTS
B+	3VDS/5VDS

SYSTEM DC/DC RT8207MZQW	48
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS

SYSTEM DC/DC SY8206DQNC	49
INPUTS	OUTPUTS
B+	1.05VS

SYSTEM DC/DC SY8003DFC	52
INPUTS	OUTPUTS
B+	1.5VS

SYSTEM DC/DC RT8880BGQW	54~55
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8003DFC	56
INPUTS	OUTPUTS
B+	+1.8VS_VGA

SYSTEM DC/DC SY8003DFC	57
INPUTS	OUTPUTS
B+	+0.95VS_VGA

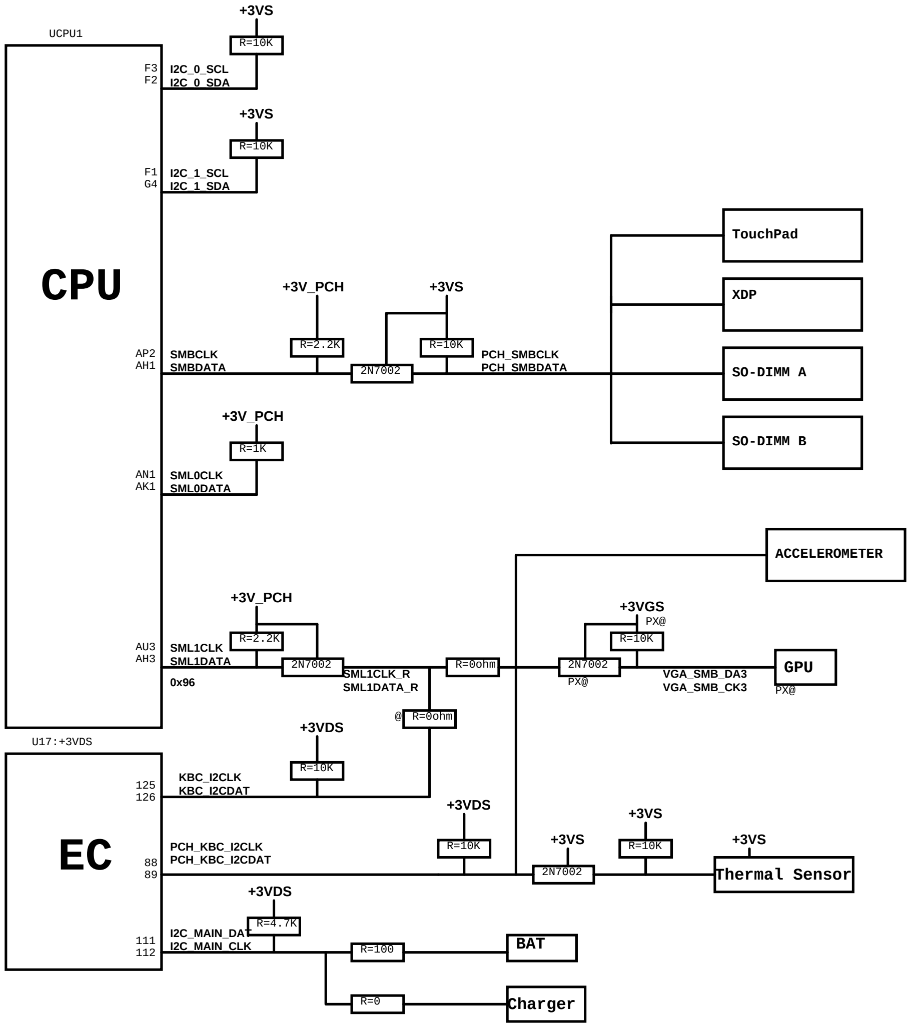
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: Block Diagrams
				Size: Custom; Document Number: LA-B181P; Rev: 0.5
				Date: Tuesday, March 25, 2014; Sheet 2 of 62

@ is NO SMT part (empty)
short@ : short pad , don't pop.
@EMI@,@ESD@,@RF@ : Reserve , don't pop.
RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel.
eDP@ : Support eDP panel.

WWAN@ : For WWAN function.

PX@ : GPU BOM config.

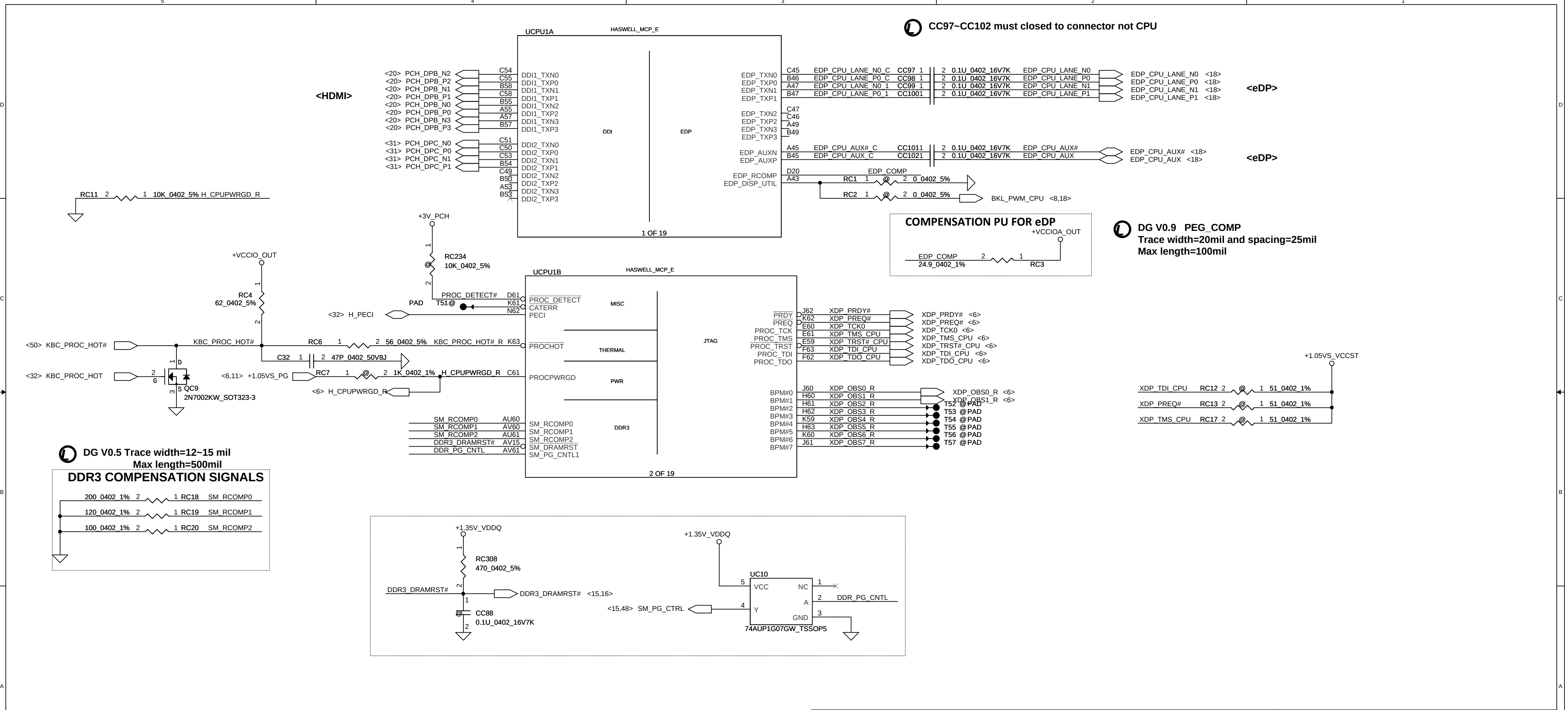


<USB2.0 port>

USB2.0 port	DESTINATION CS
0	USB 2.0(Right side)
1	USB 2.0(Right side)
2	USB 2.0(Left side)
3	WLAN/BT
4	Finger Print
5	WWAN Touch (Option)
6	Camera
7	USB 2.0(Left side)

<PCI-E,SATA,USB3.0>

Lane#	PCI-E		SATA	USB3.0	DESTINATION CS
1				0	USB3.0
2				1	USB3.0
3	1			2	WWAN (M.2)
4	2			3	Card reader(PCI-E)
5	3				10/100/1000 LAN
6	4				WLAN (M.2)
7	5				GPU(DIS only)
8					GPU(DIS only)
9					GPU(DIS only)
10					GPU(DIS only)
11	6	L3	3		2.5"HDD
12		L2	2		ODD
13		L1	1		
14		L0	0		SSD(NGFF)



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

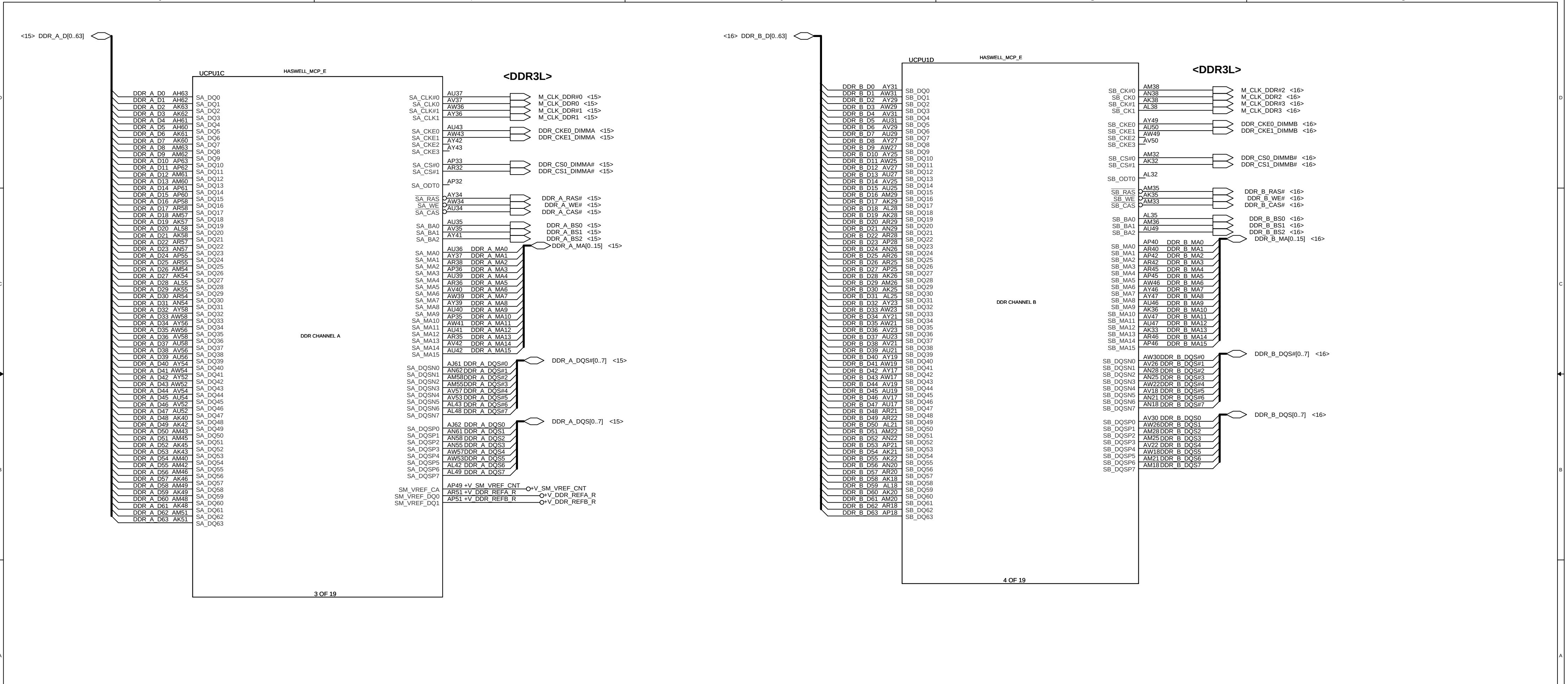
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title: ***DDI,MSIC,XDP***

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 4 of 62

Compal Electronics, Inc.



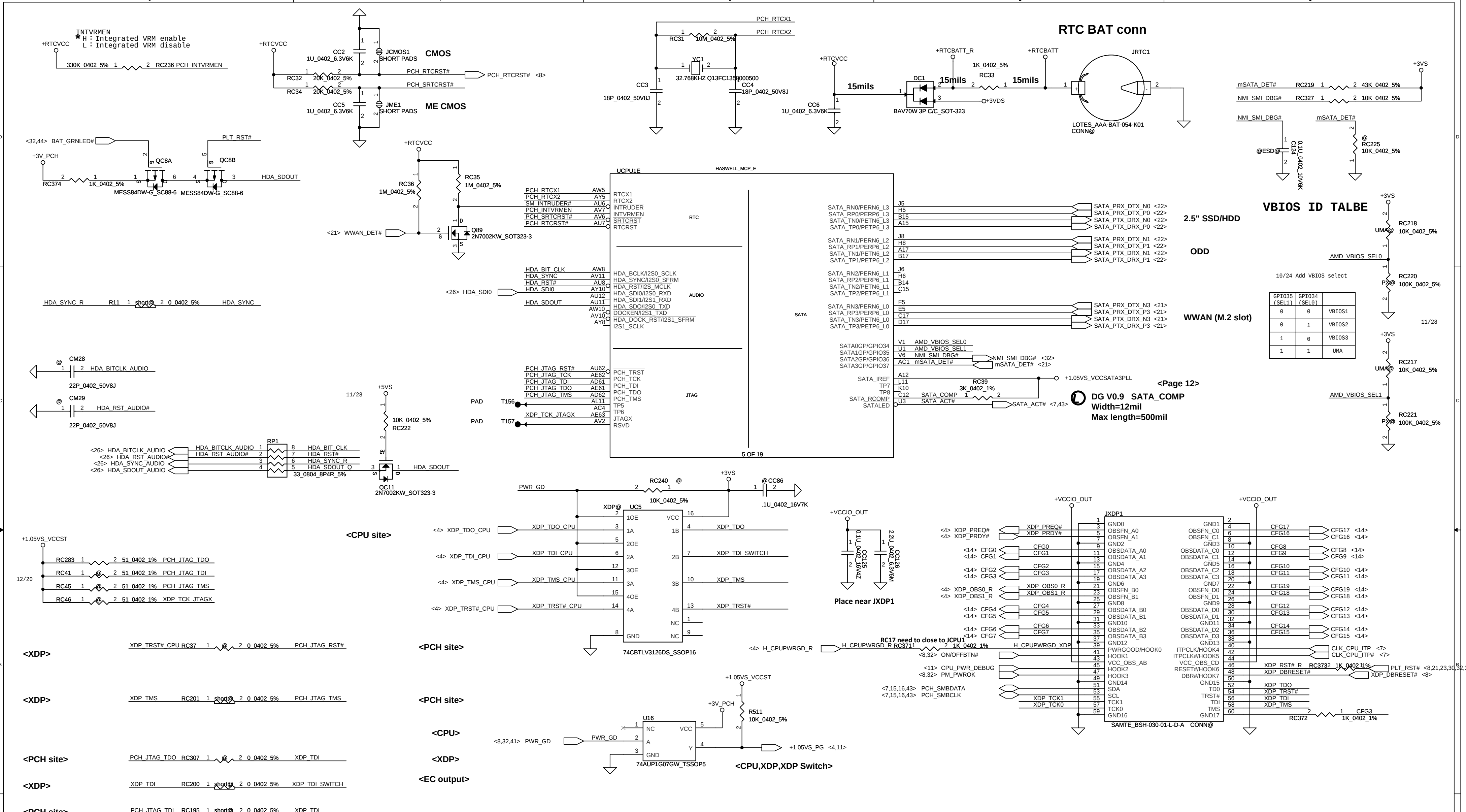
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title **DDRIII**

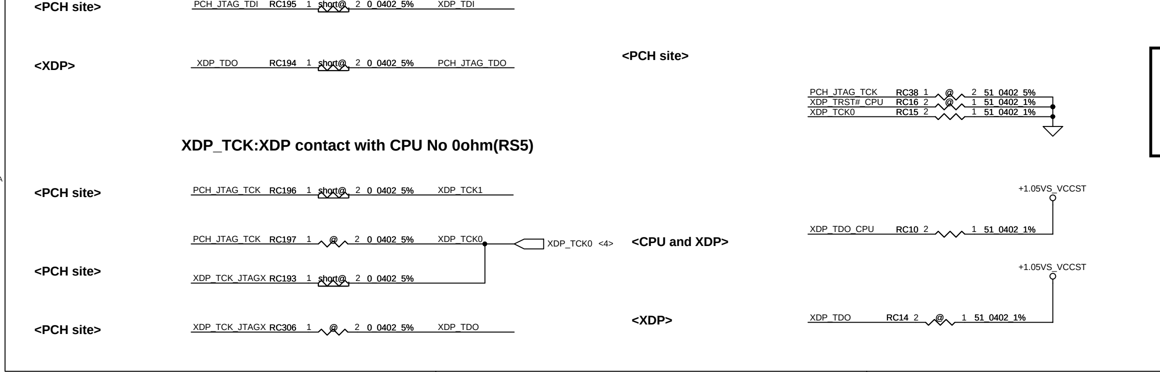
Size Custom | Document Number LA-B181P | Rev 0.5

Date: Tuesday, March 25, 2014 |

Compal Electronics, Inc.



GPIO35 (SEL1)	GPIO34 (SEL0)	
0	0	VBIOS1
0	1	VBIOS2
1	0	VBIOS3
1	1	UMA



Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

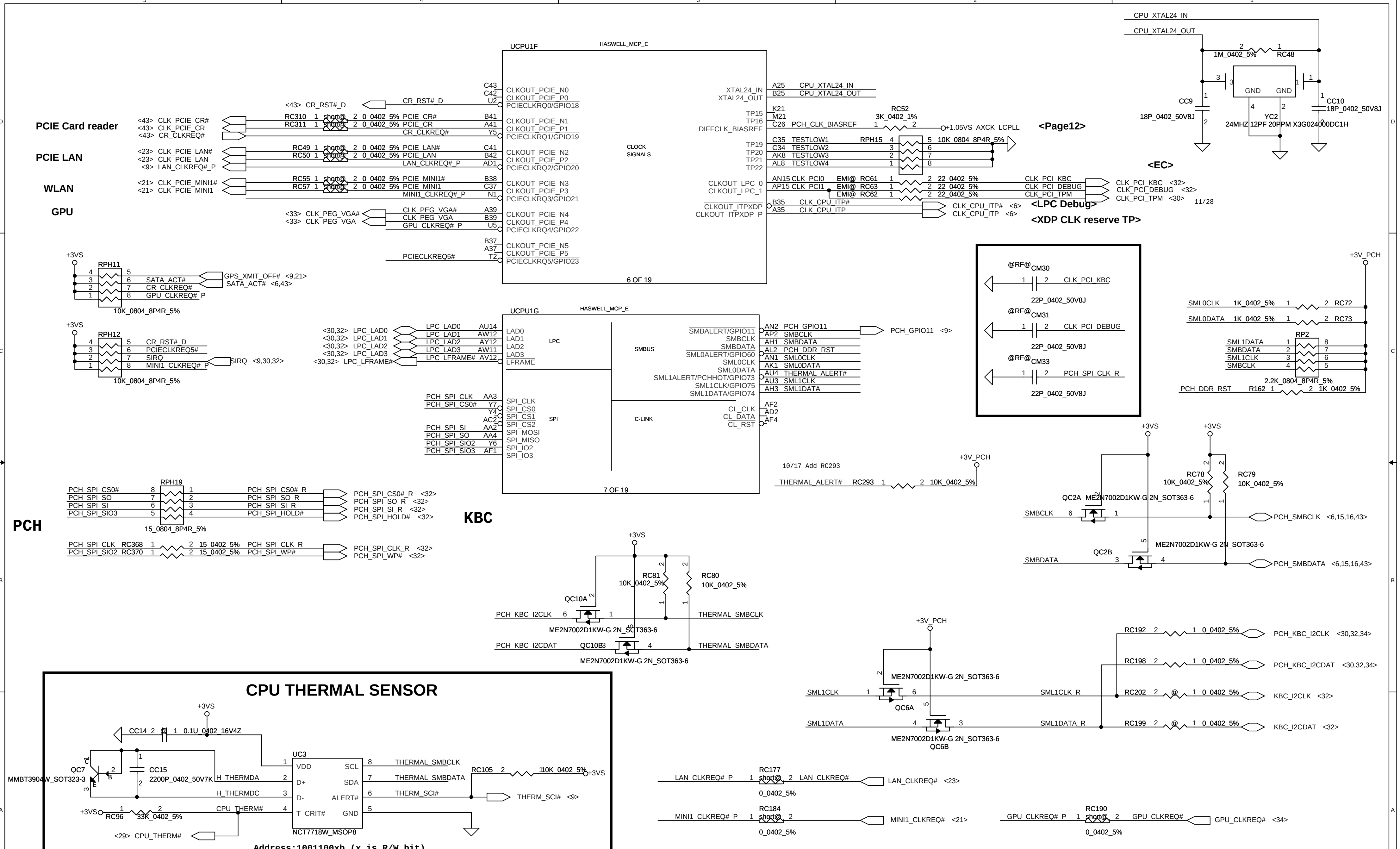
Security Classification: Compal Secret Data
Issued Date: 2011/06/29 — Deciphered Date: 2011/06/29

Compal Electronics, Inc.

Title: **RTC,SATA,HDA,JTAG**

Size: Custom — Document Number: LA-B181P — Rev: 0.5

Date: Tuesday, March 25, 2014 — Sheet 6 of 62



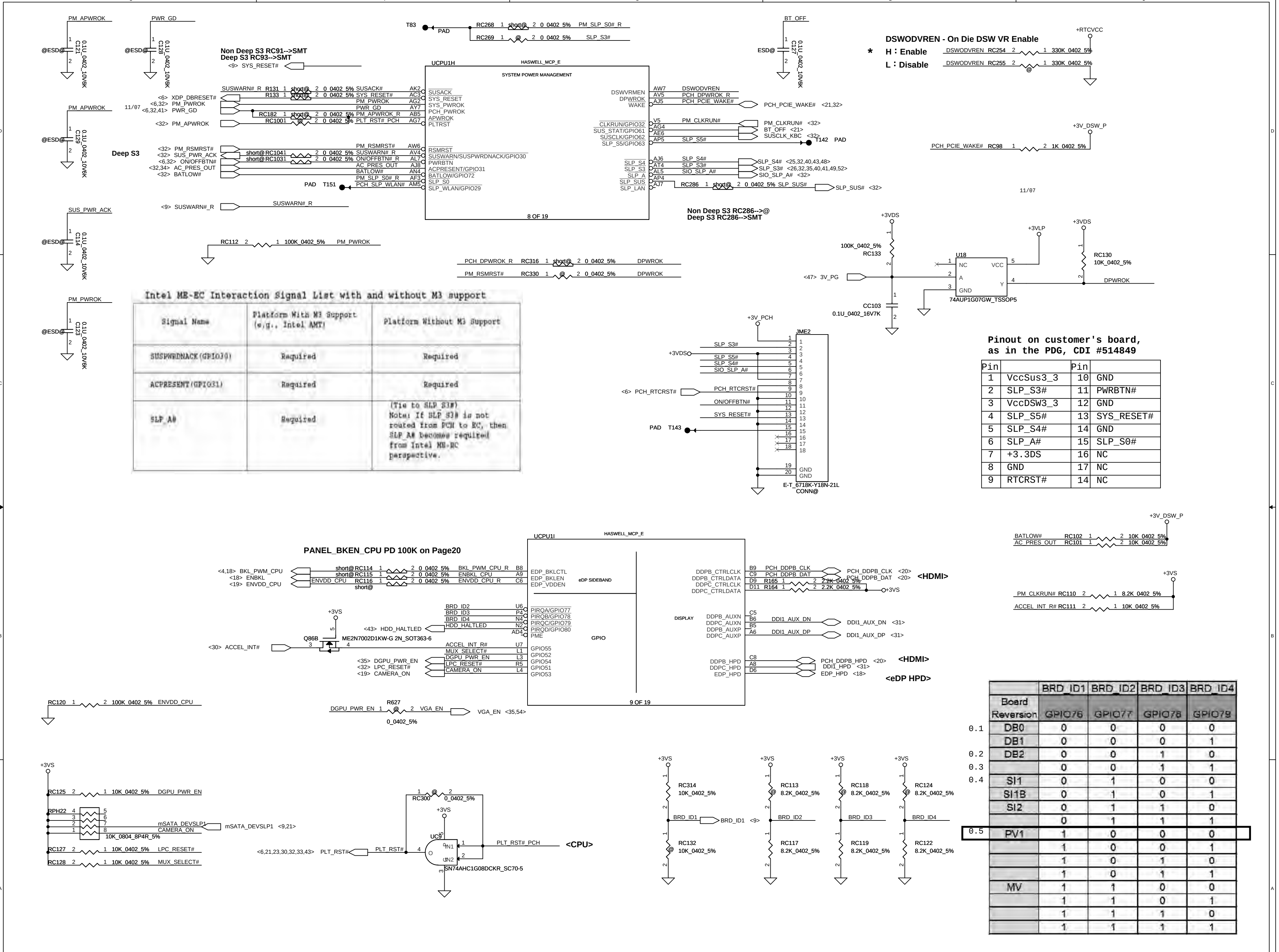
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **CLK,SPI,SMB,LPC**

Size: Custom — Document Number: LA-B181P — Rev: 0.5

Date: Tuesday, March 25, 2014 — Sheet 7 of 62



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC perspective.

Pinout on customer's board, as in the PDG, CDI #514849

Pin		Pin	
1	VccSus3_3	10	GND
2	SLP_S3#	11	PWRBTN#
3	VccDSW3_3	12	GND
4	SLP_S5#	13	SYS_RESET#
5	SLP_S4#	14	GND
6	SLP_A#	15	SLP_S0#
7	+3.3DS	16	NC
8	GND	17	NC
9	RTCRST#	14	NC

		BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4
	Board Reversion	GPIO76	GPIO77	GPIO78	GPIO79
0.1	DB0	0	0	0	0
	DB1	0	0	0	1
0.2	DB2	0	0	1	0
0.3		0	0	1	1
0.4	SI1	0	1	0	0
	SI1B	0	1	0	1
	SI2	0	1	1	0
		0	1	1	1
0.5	PV1	1	0	0	0
		1	0	0	1
		1	0	1	0
		1	0	1	1
	MV	1	1	0	0
		1	1	0	1
		1	1	1	0
		1	1	1	1

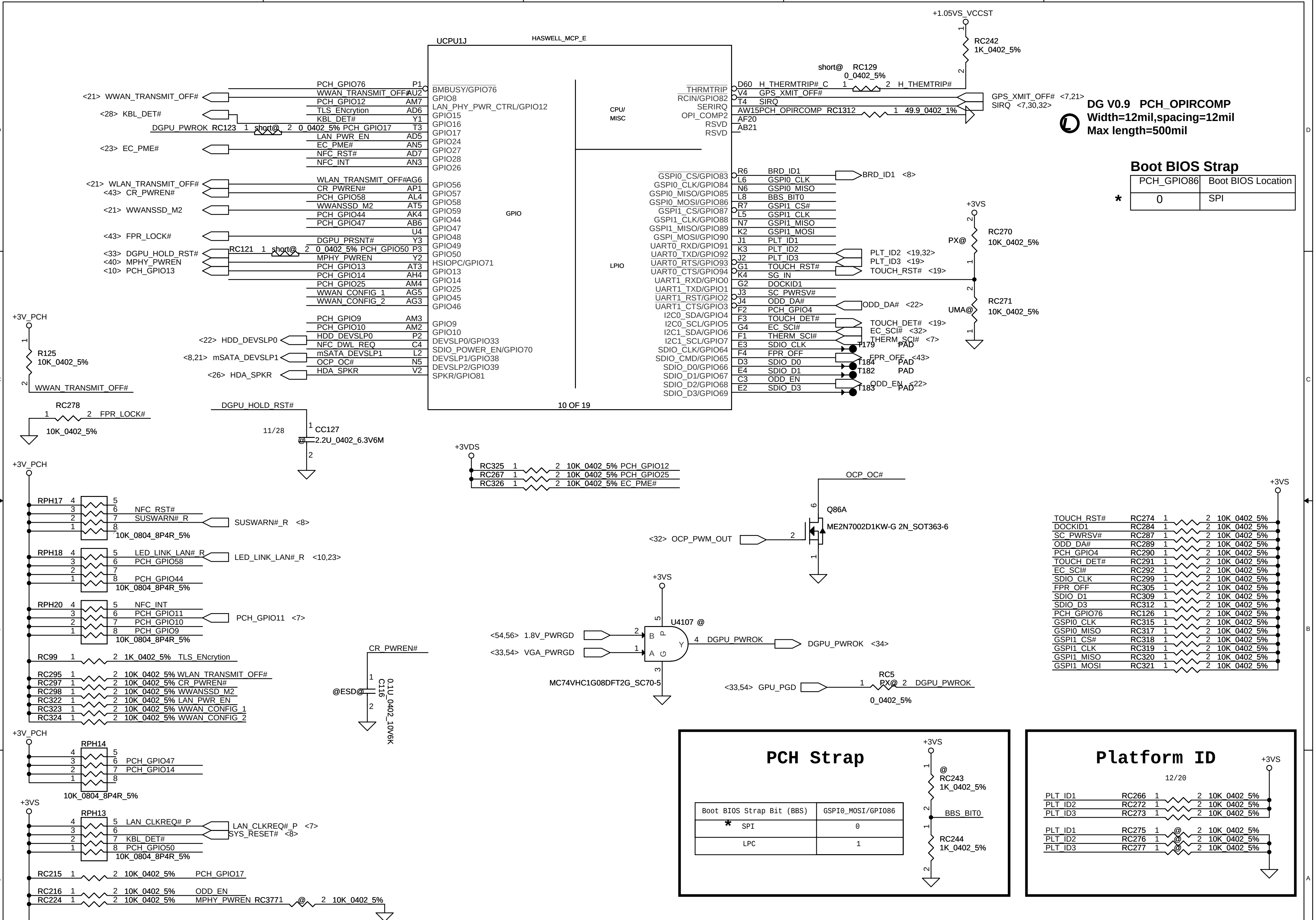
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PM,GPIO,DDI**

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



Boot BIOS Strap

	PCH_GPIO86	Boot BIOS Location
*	0	SPI

PCH Strap

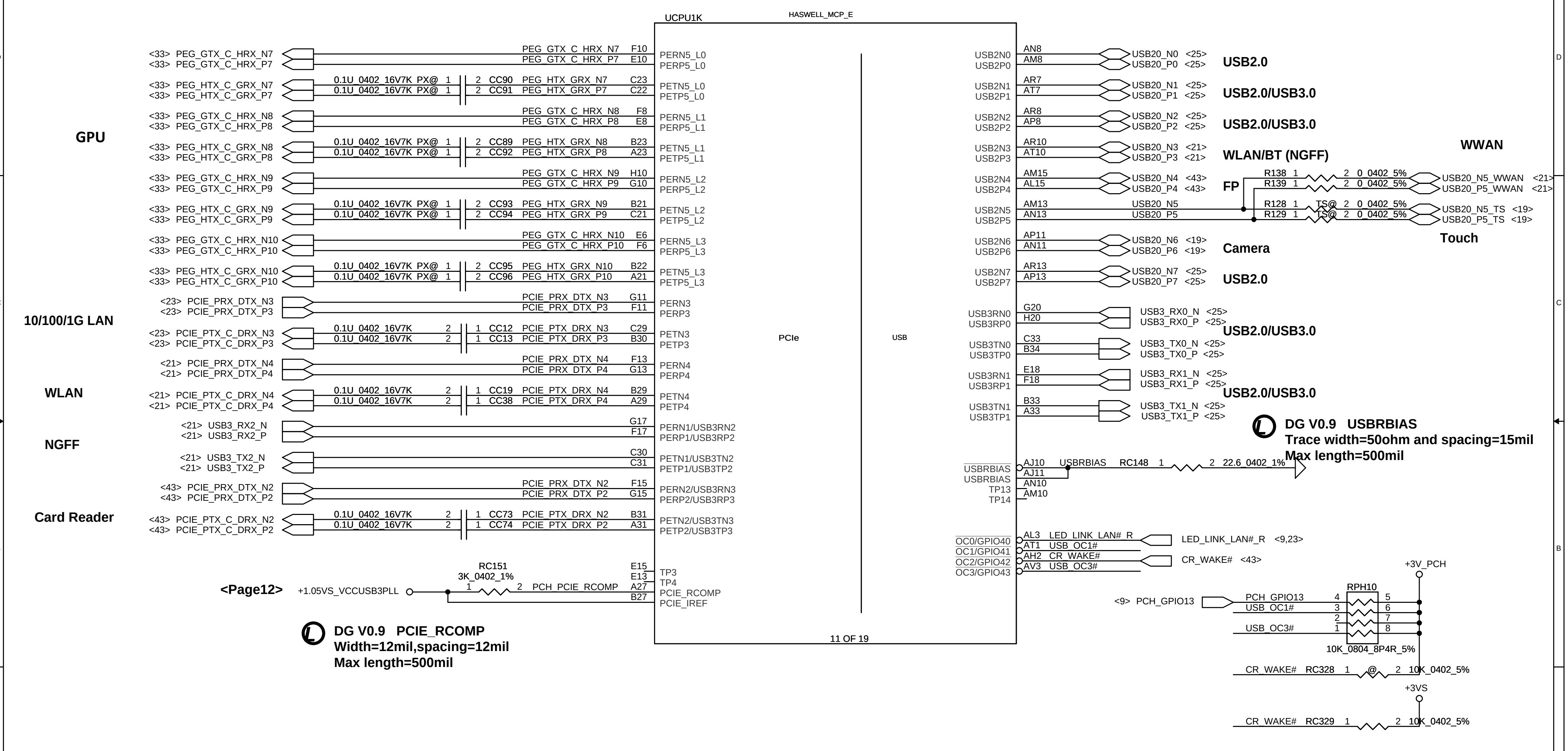
Boot BIOS Strap Bit (BBS)	GSPI0_MOSI/GPIO86
* SPI	0
LPC	1

Platform ID

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title: *GPIO,UART,I2C*

Size	Document Number	Rev
Custom	LA-B181P	0.5

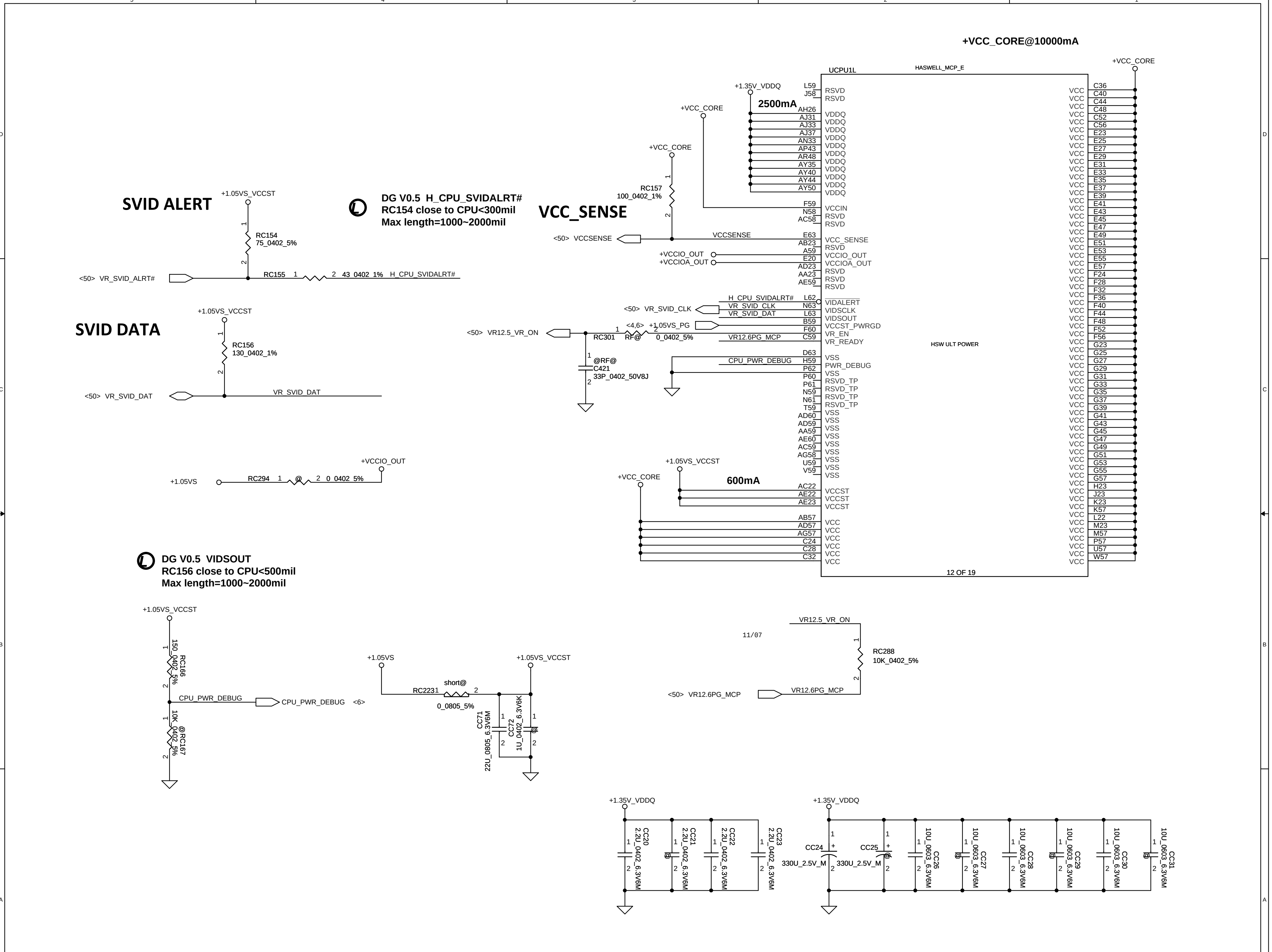


Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

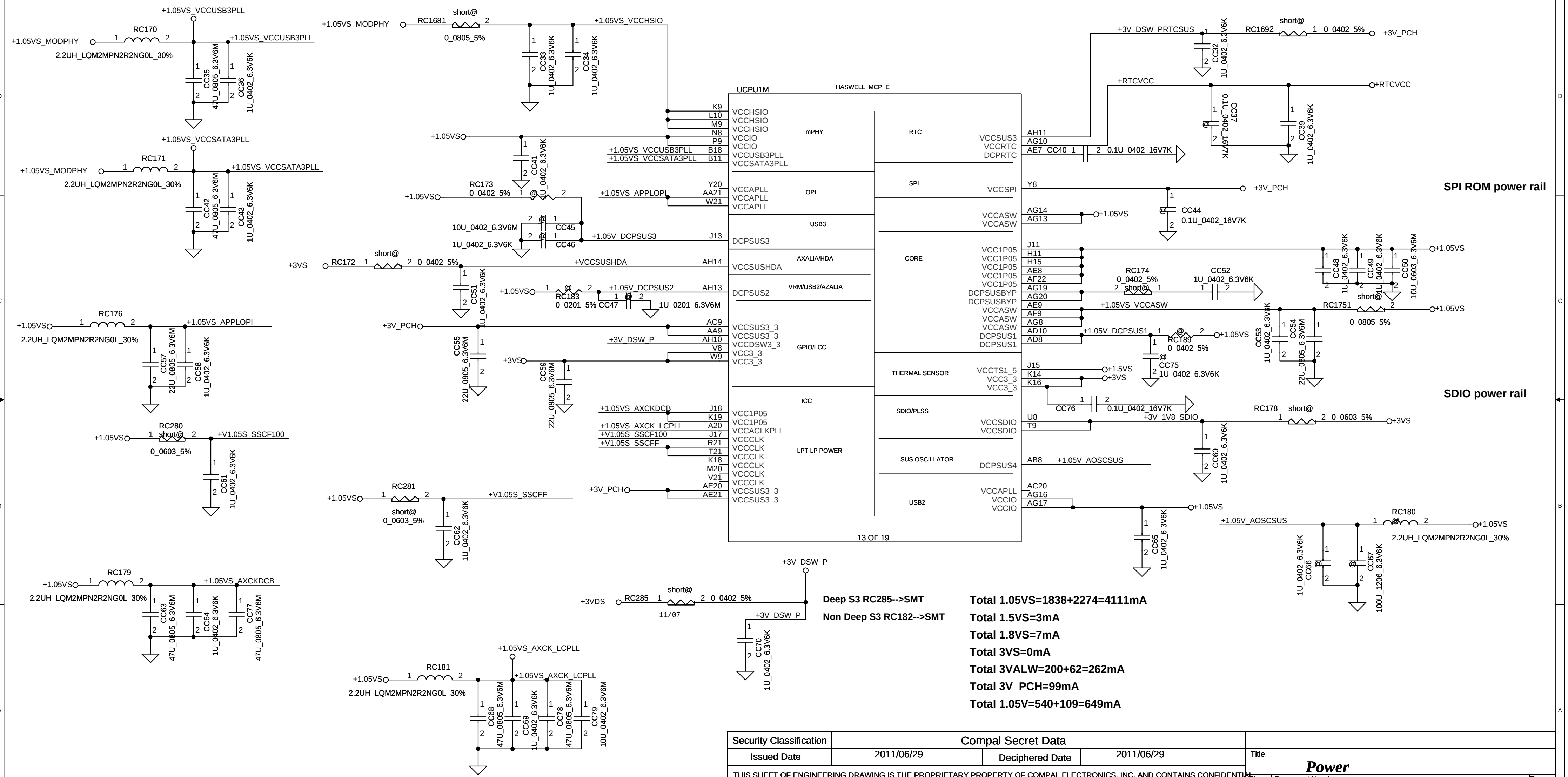
Title
PCIE,USB

Size: B | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date 2011/06/29	Title: Power
			Size: Custom — Document Number: LA-B181P — Rev 0.5
			Date: Tuesday, March 25, 2014 — Sheet 11 of 62



Deep S3 RC285-->SMT

Non Deep S3 RC182-->SMT

Total 1.05VS=1838+2274=4111mA

Total 1.5VS=3mA

Total 1.8VS=7mA

Total 3VS=0mA

Total 3VALW=200+62=262mA

Total 3V_PCH=99mA

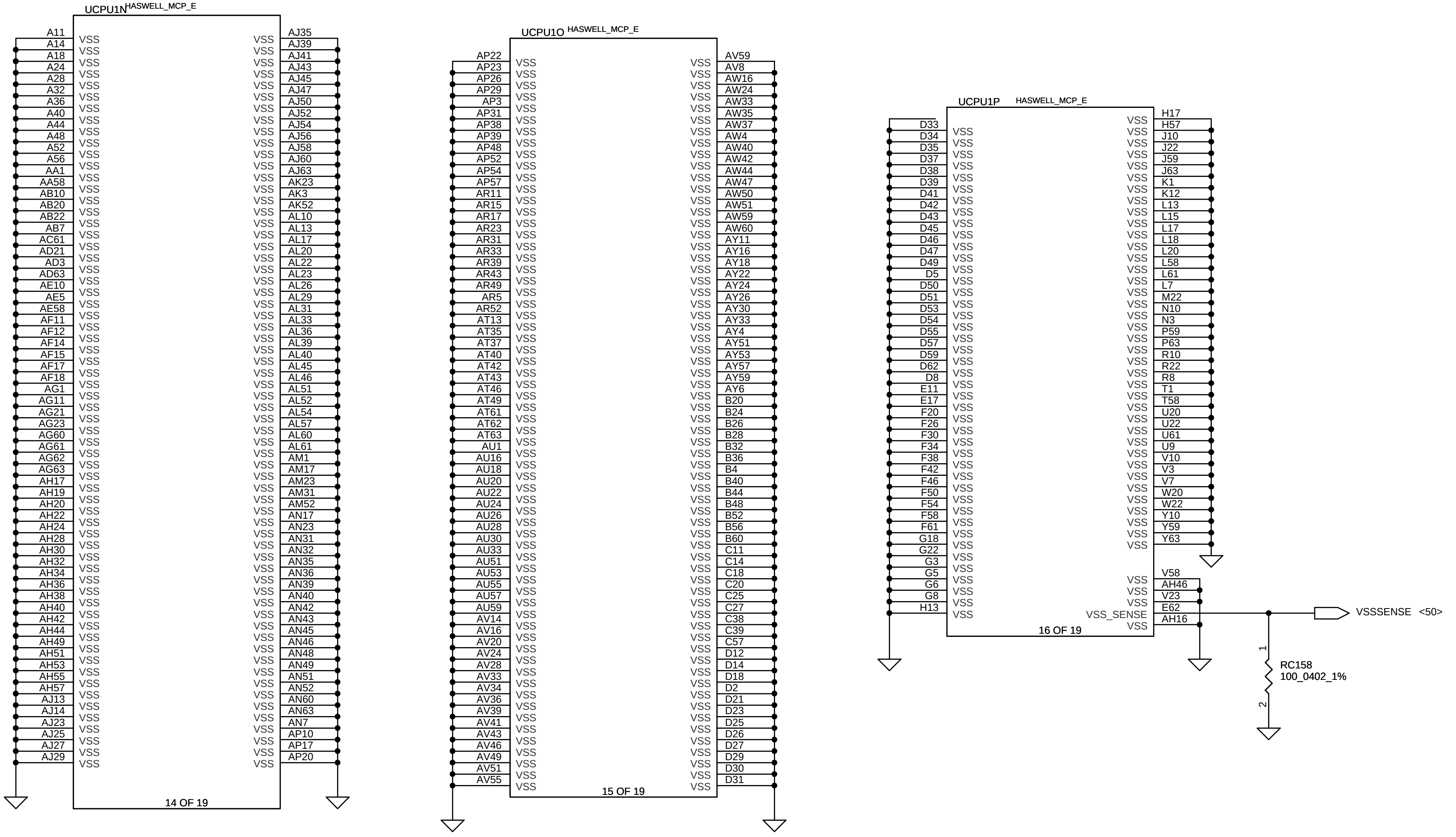
Total 1.05V=540+109=649mA

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title: **Power**

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014



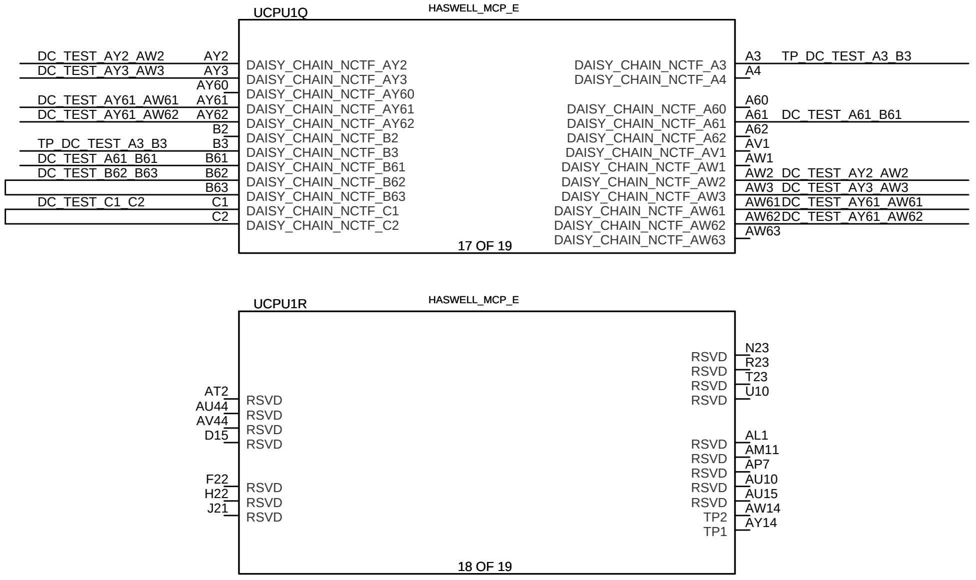
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

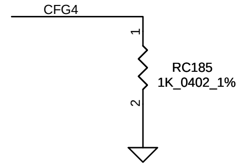
Compal Electronics, Inc.

Title: GND/VSSSEN

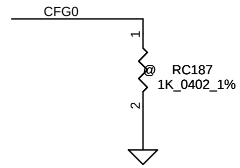
Size	Document Number	Rev
	LA-B181P	0.5

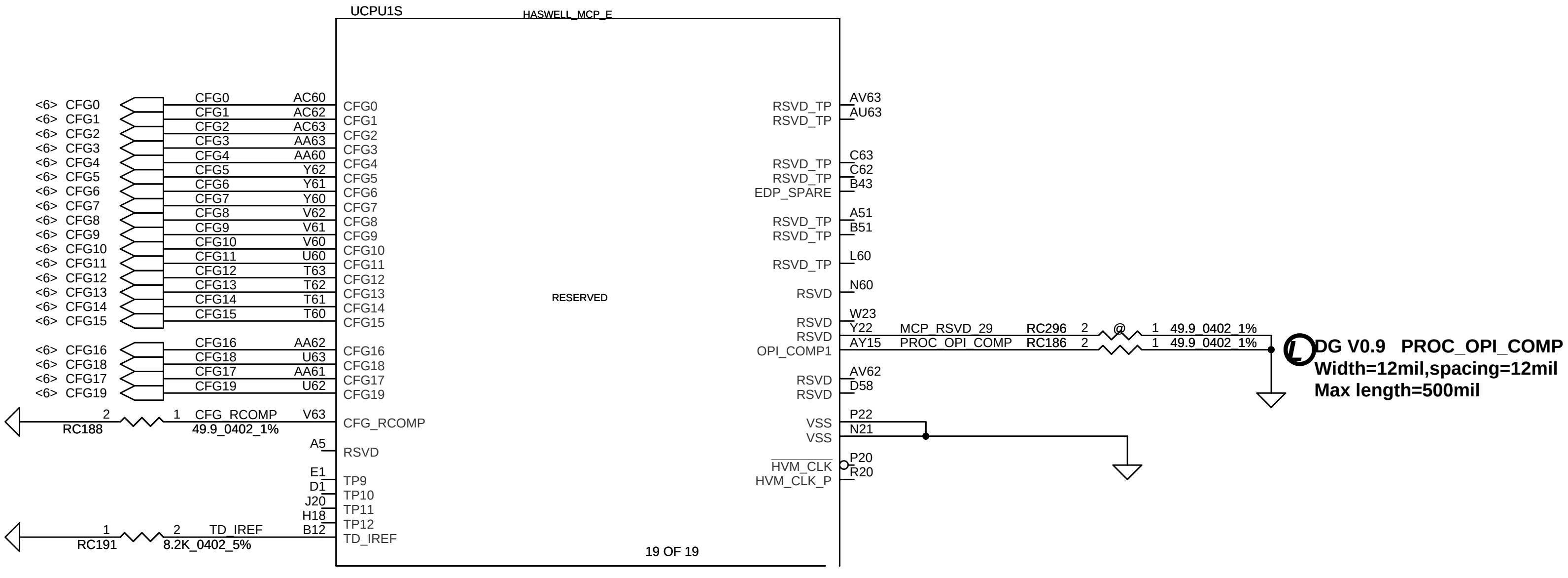
Date: Tuesday, March 25, 2014 | Sheet 13 of 62





Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



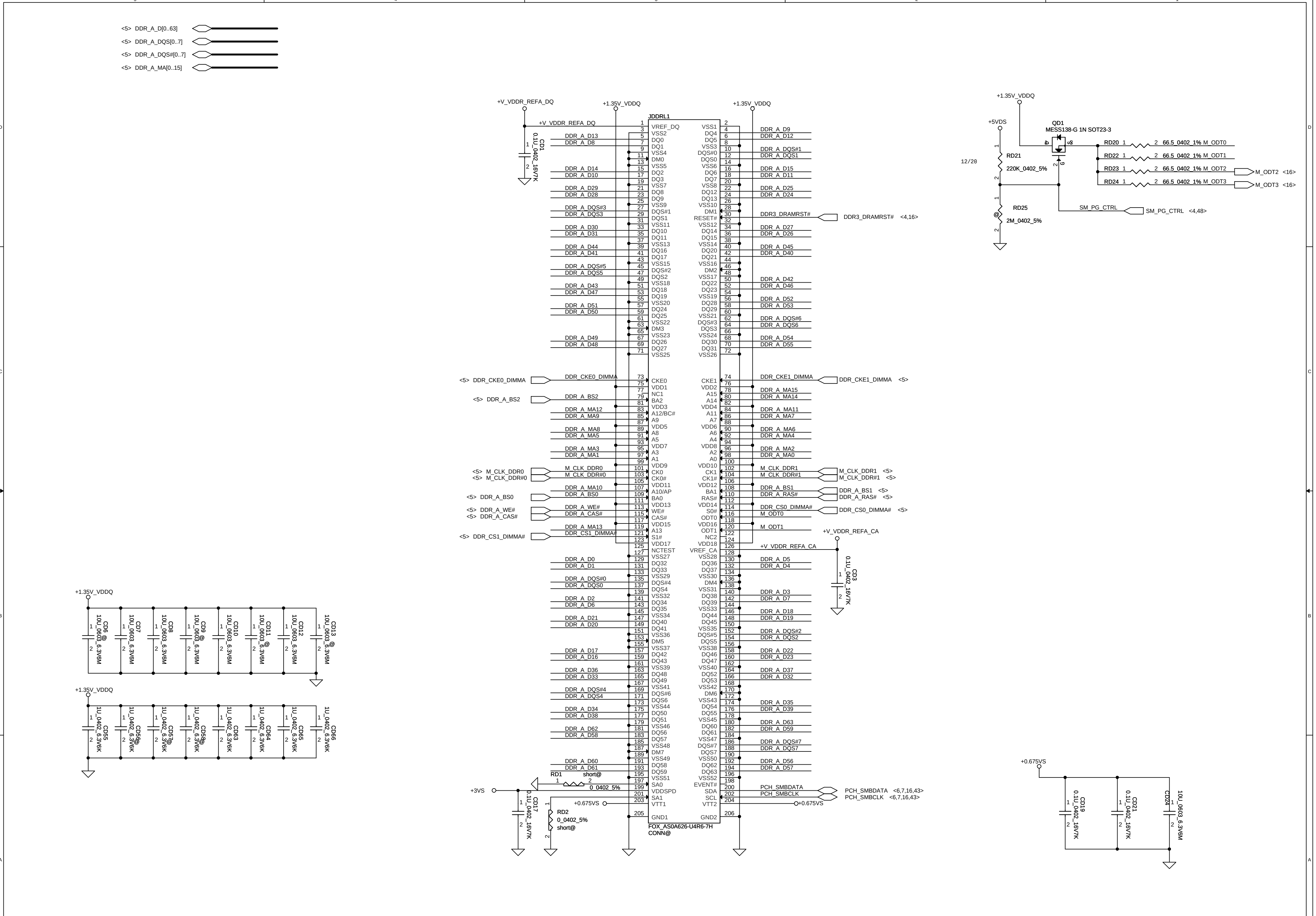


Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **RSVD/CFG**

Size | Document Number: LA-B181P | Rev: 0.5

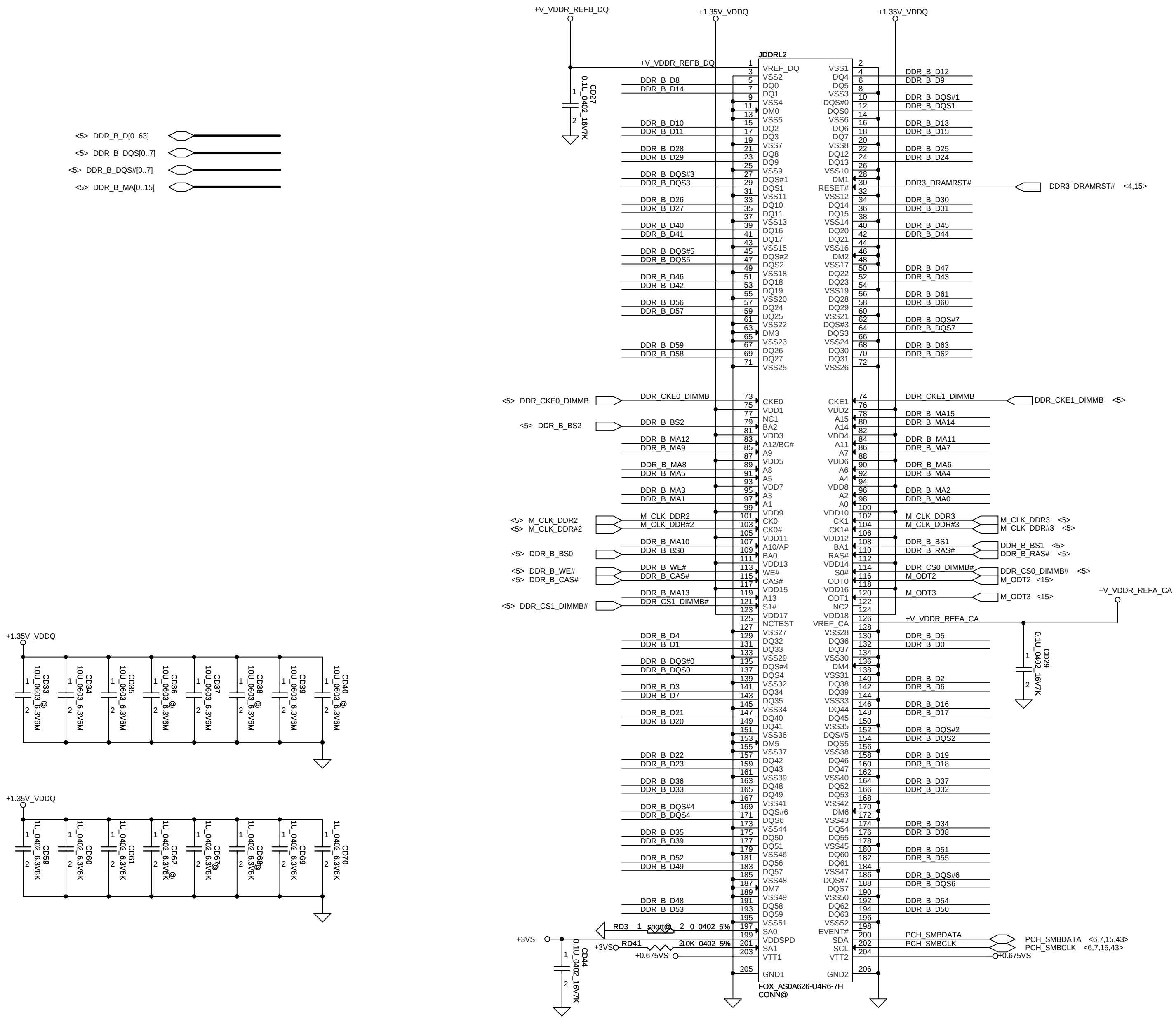


Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title: **DDR3L DIMM0**

Size: C | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

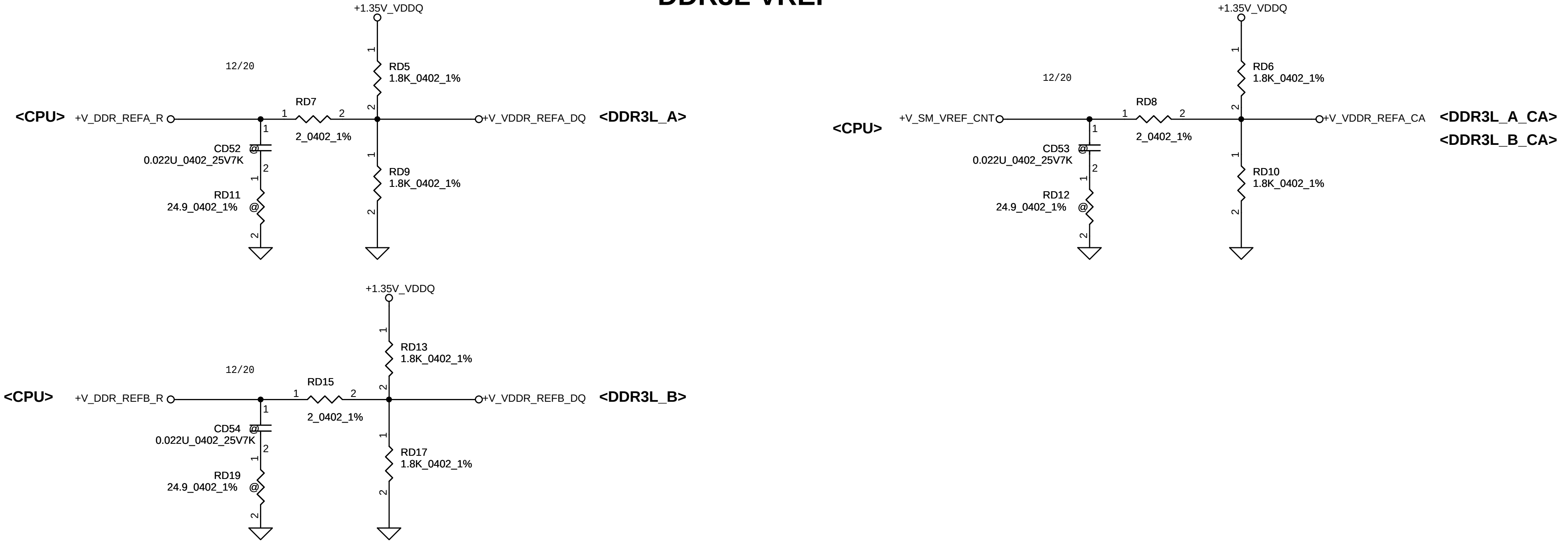
Compal Electronics, Inc.

Title: DDR3L DIMM1

Size | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 16 of 62

DDR3L VREF



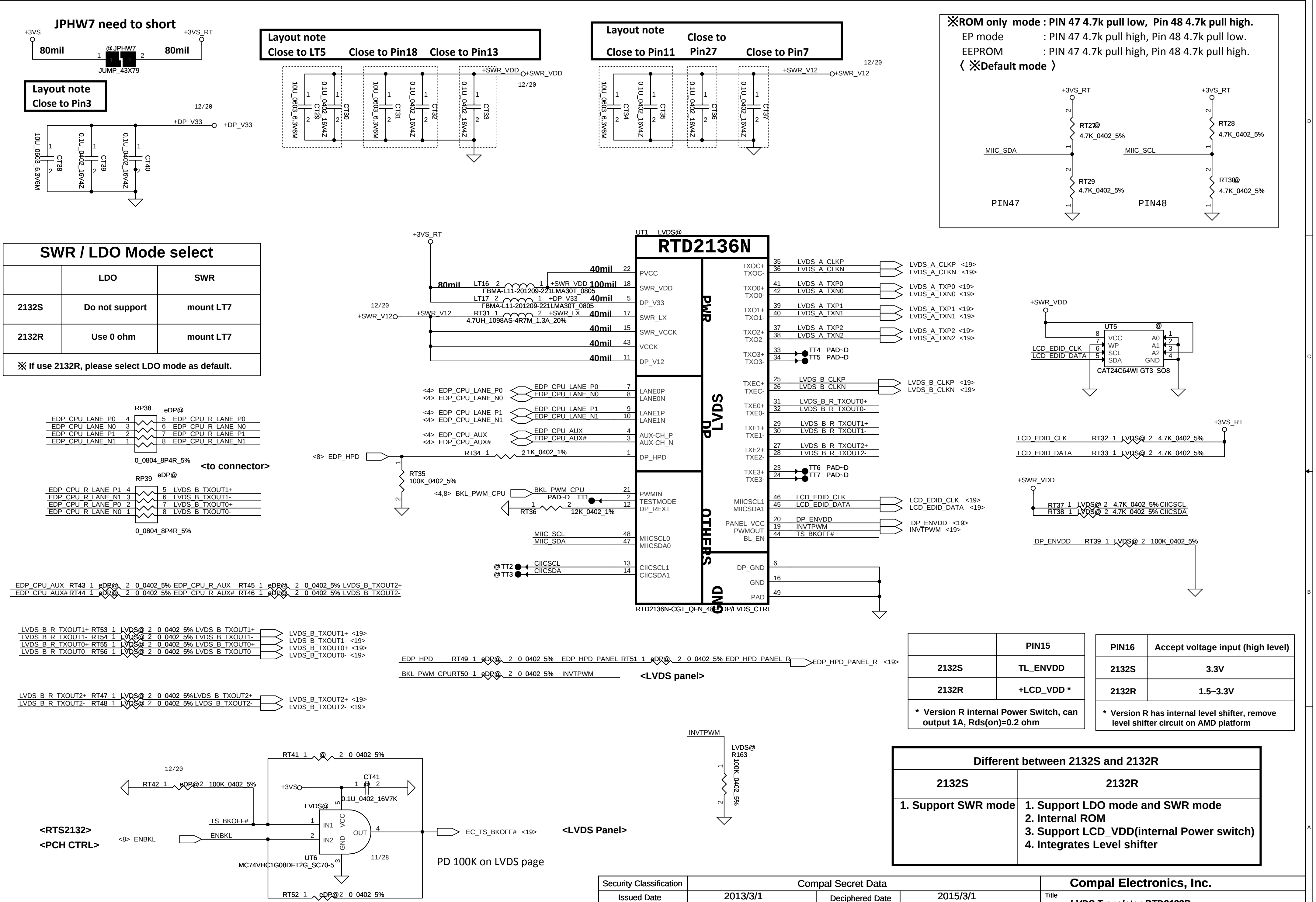
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: *DDR3L VREF*

Size | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

※ If use 2132R, please select LDO mode as default.

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R

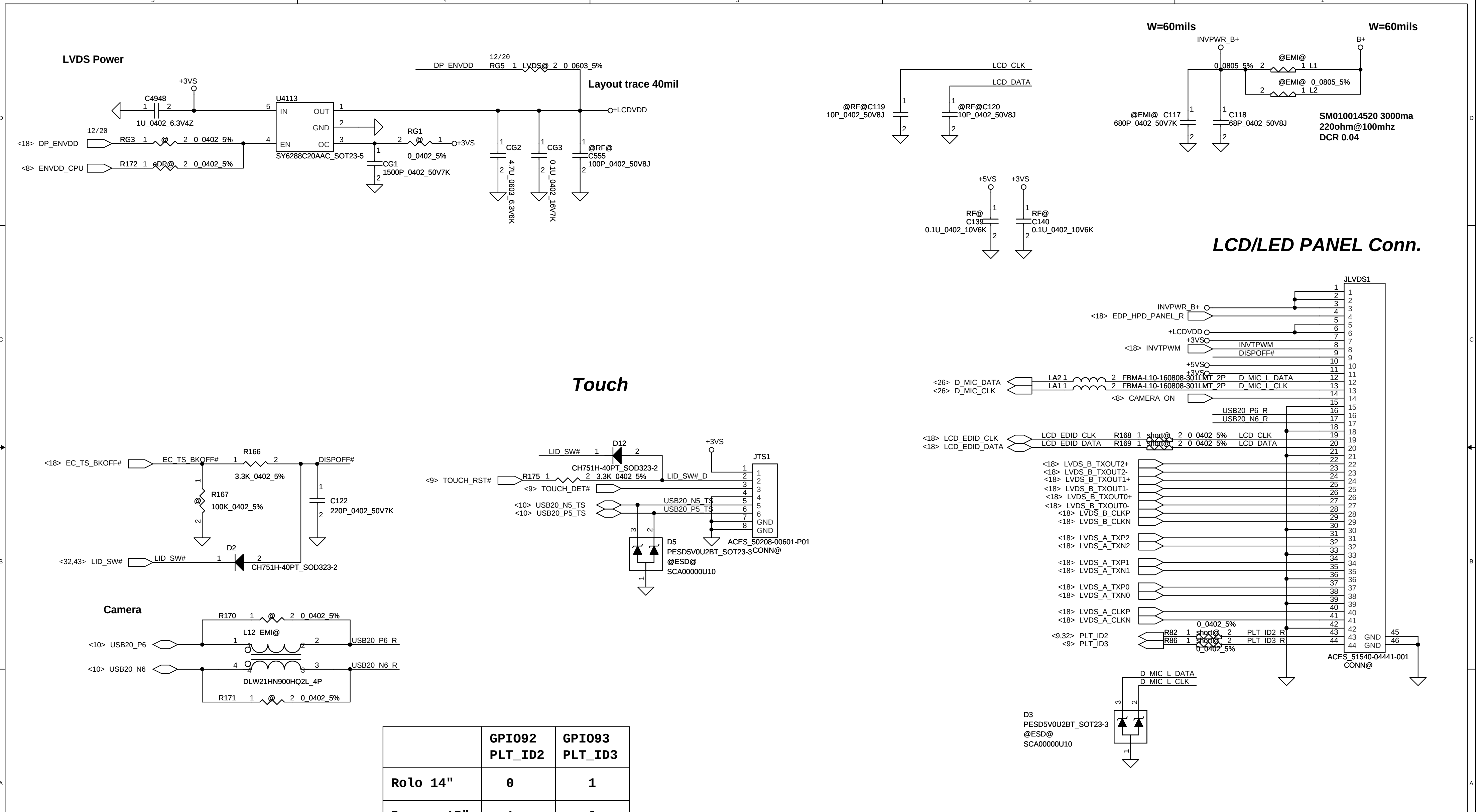
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

Compal Electronics, Inc.

Title: LVDS Translator-RTD2132R

Size | Document Number: LA-B181P | Rev 0.5



	GPIO92 PLT_ID2	GPIO93 PLT_ID3
Rolo 14"	0	1
Reeses 15"	1	0
Raisinet 17"	1	1

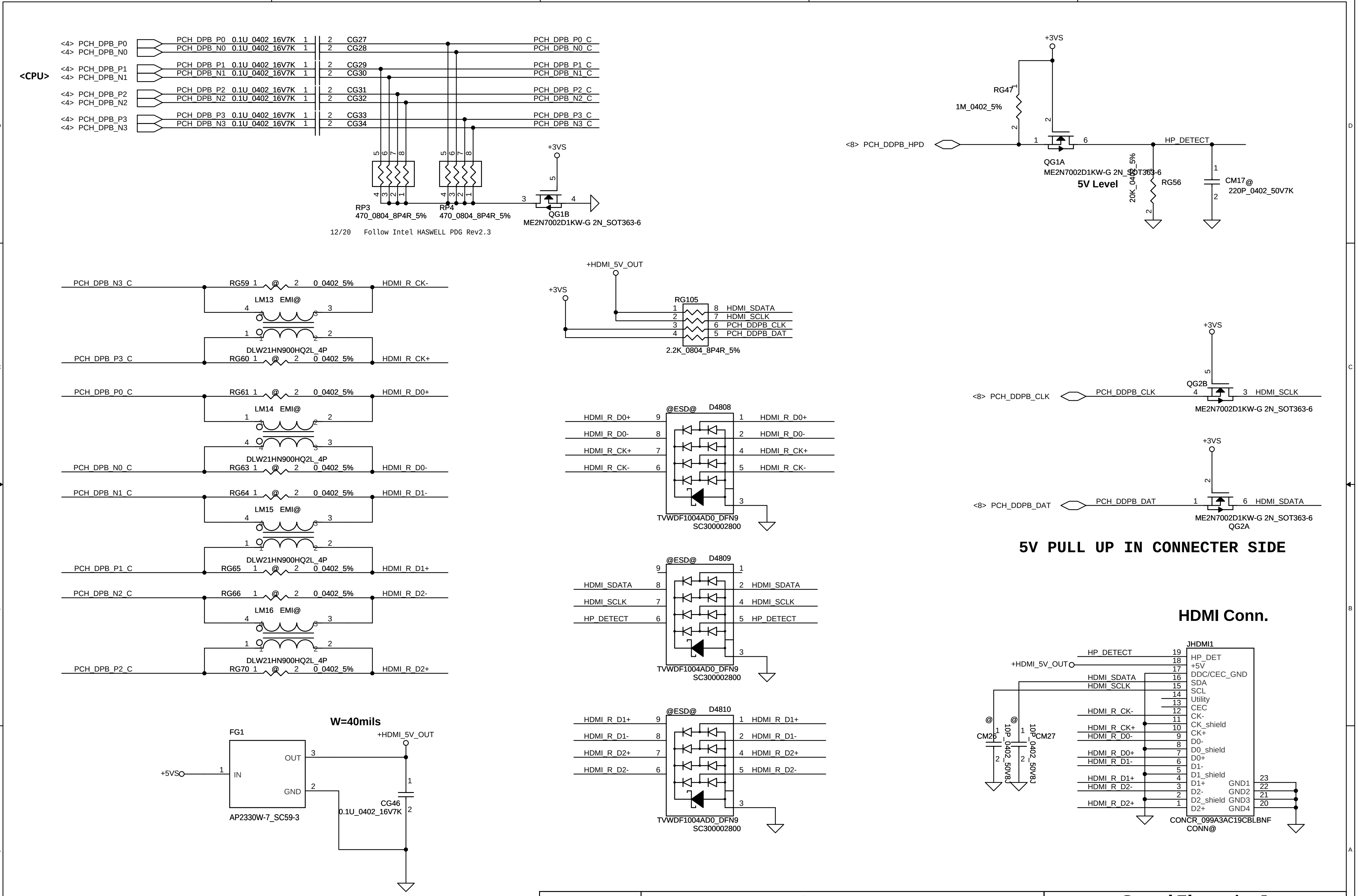
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: LVDS Connector

Size | Document Number: LA-B181P | Rev 0.5

Date: Tuesday, March 25, 2014 |



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

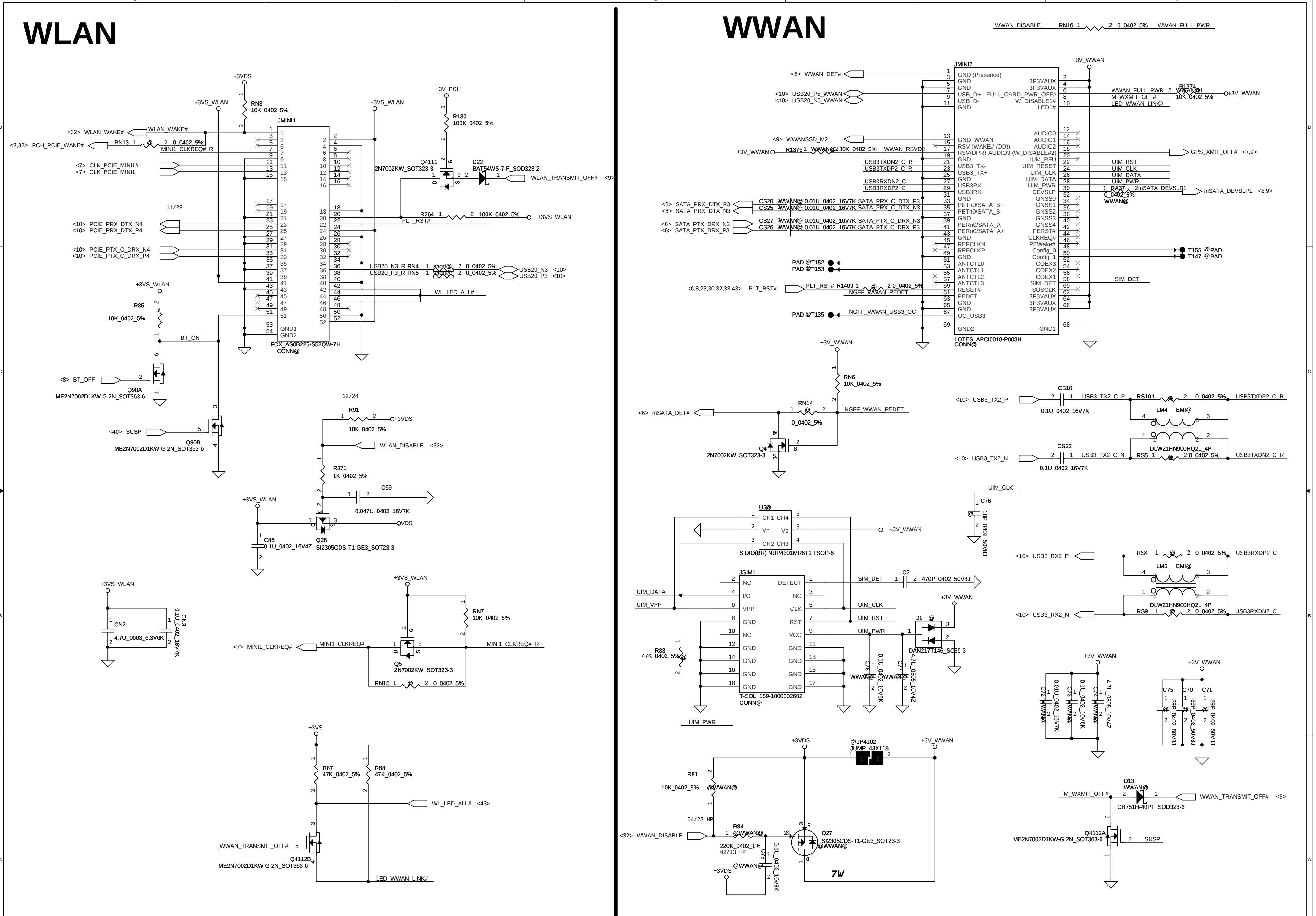
Compal Electronics, Inc.

Title

HDMI Conn/Level shift

Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 20 of 62

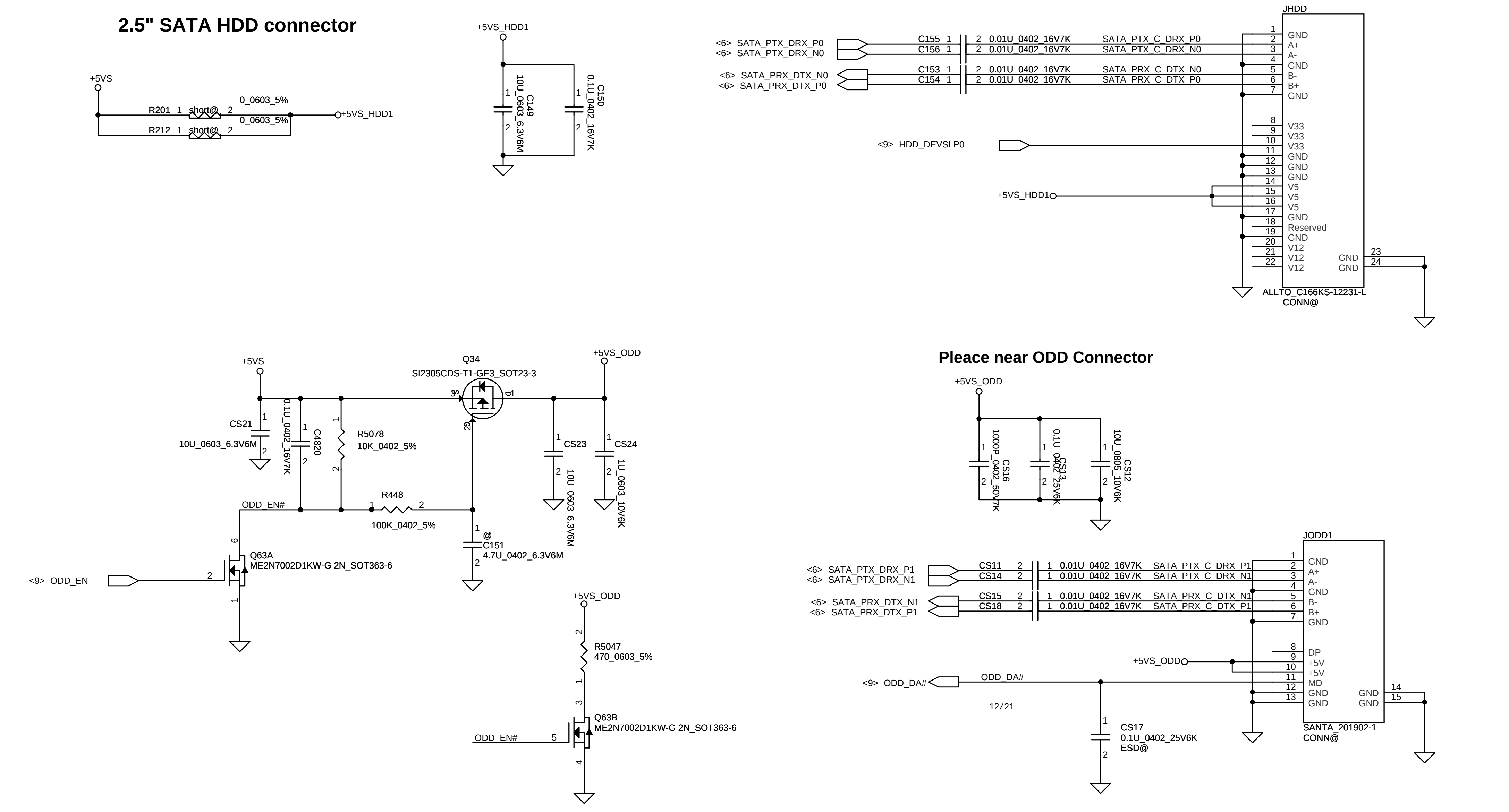


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date 2015/07/08	Title: WLAN

Size | Document Number: LA-B181P | Rev 0.5

2.5" SATA HDD connector

Pleace near ODD Connector



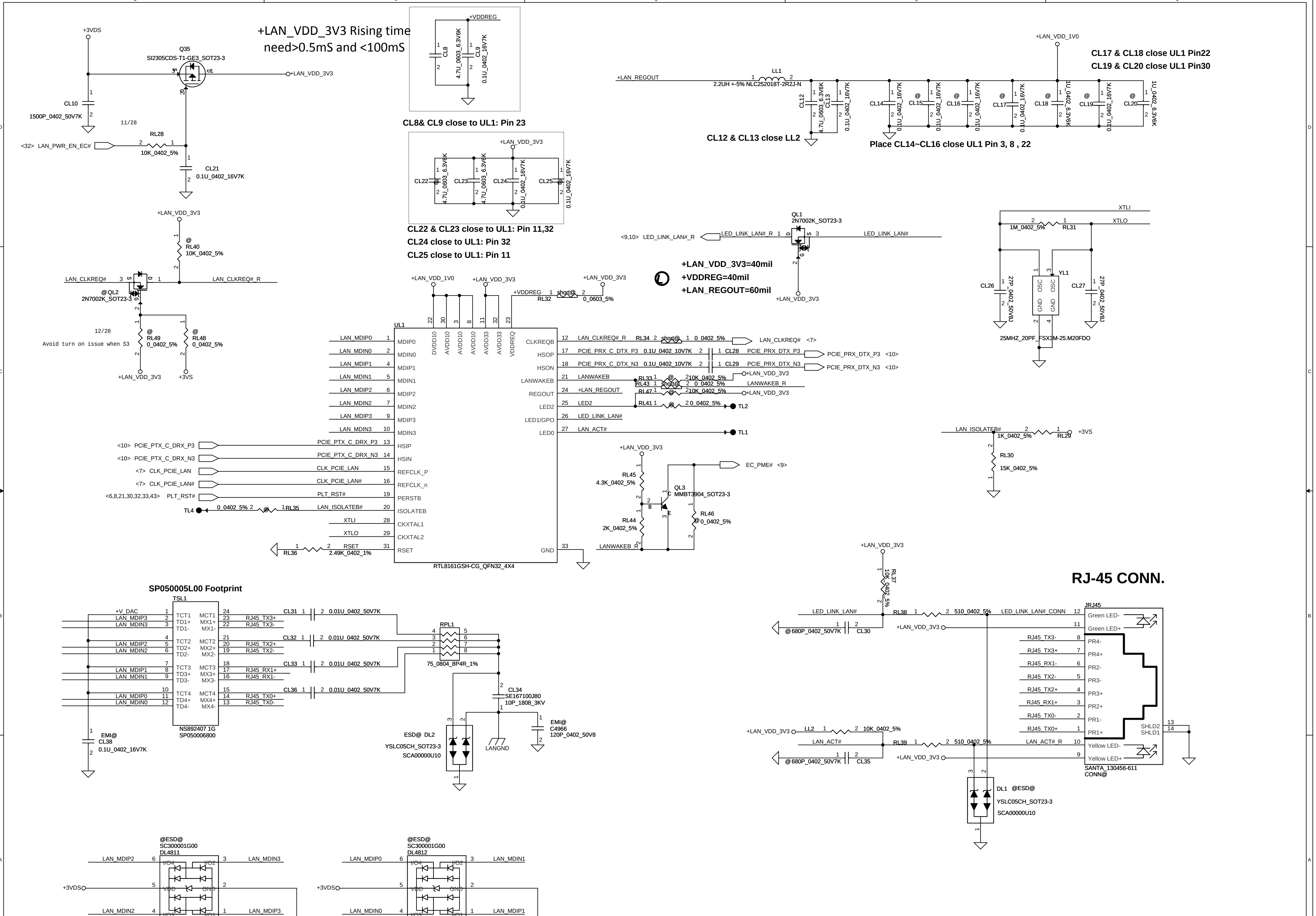
12/20 Customer change GPIO table

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: ODD/SATA Conn

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size	Document Number	Rev
B	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 22 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **LAN RTL8161GSH**

Size | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 23 of 62

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

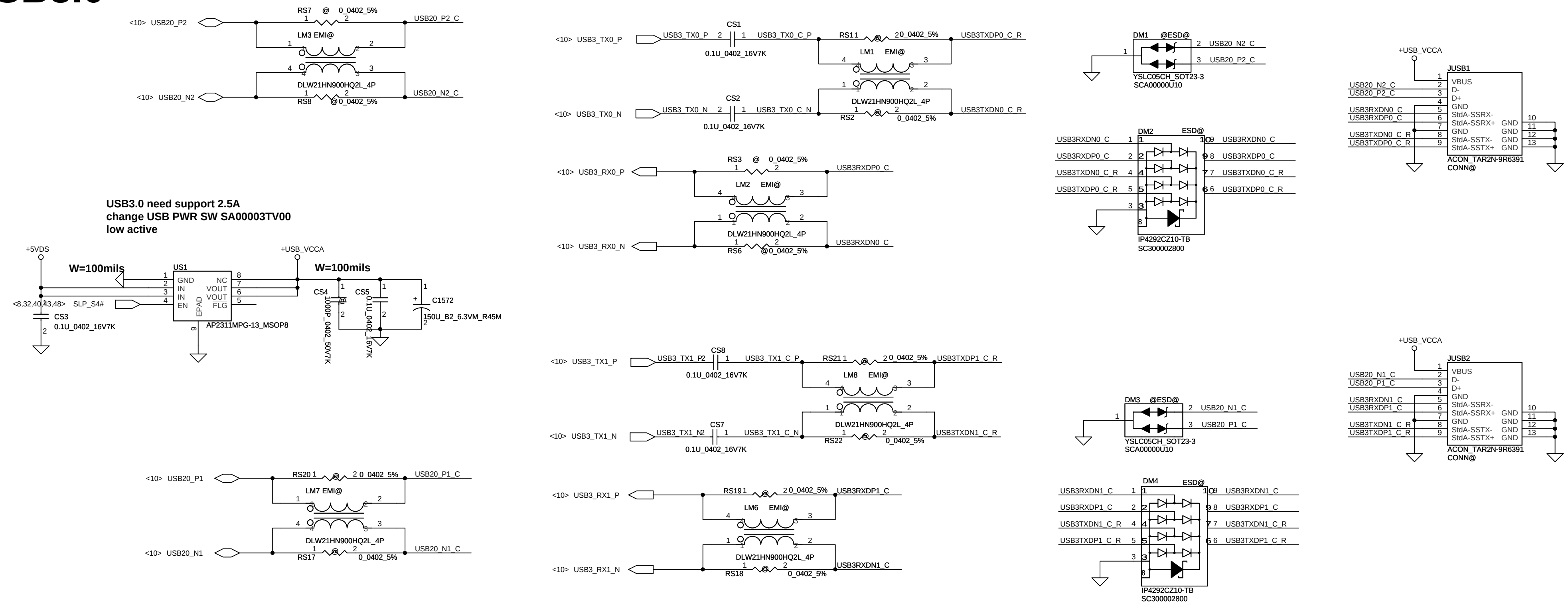
Title

Card Reader RTS5237

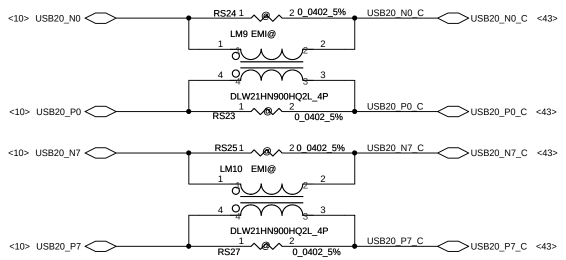
Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 24 of 62

USB3.0



USB2.0



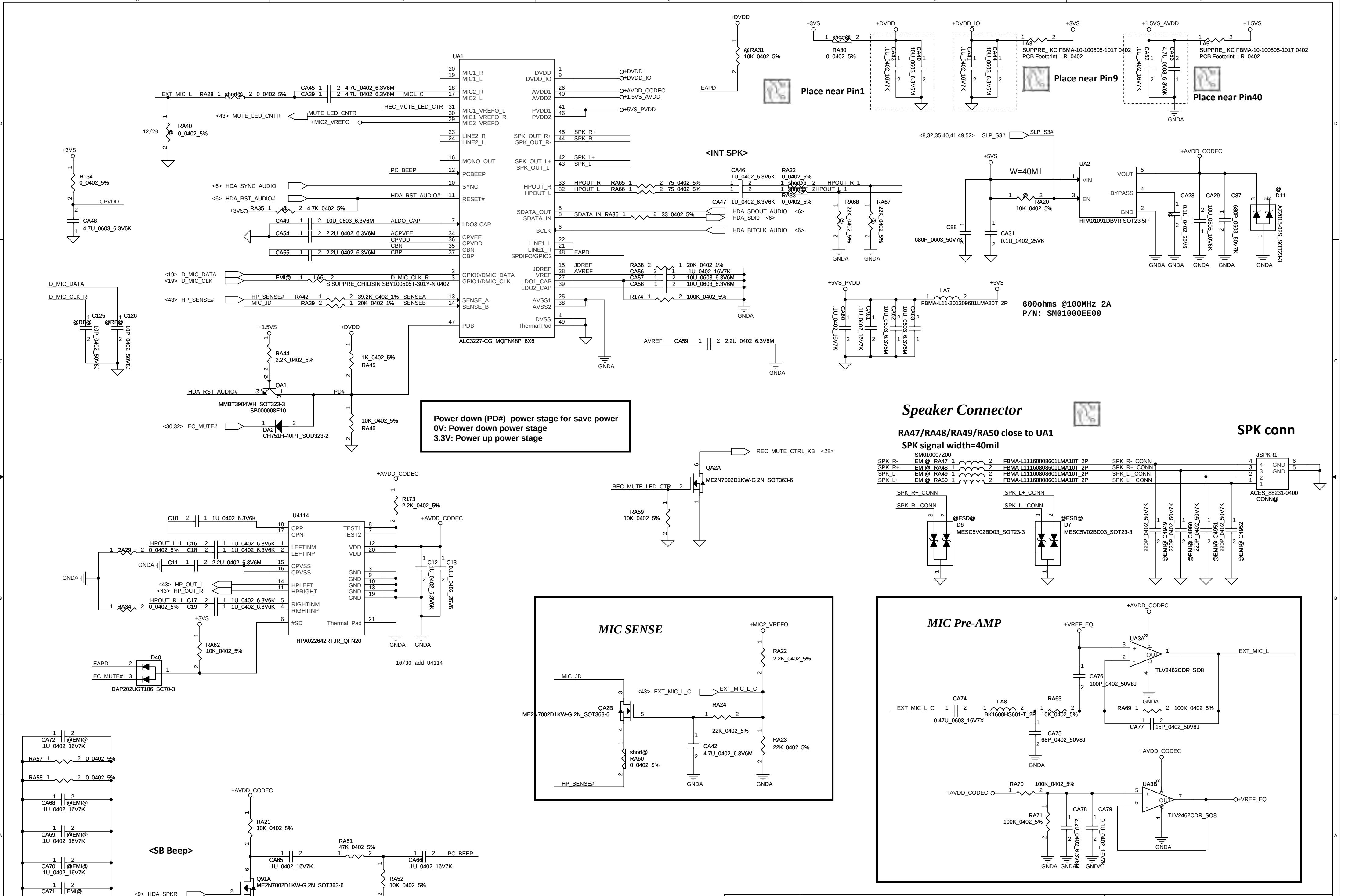
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: USB 3.0

Size: C | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 25 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: AUDIO ALC3227

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 26 of 62

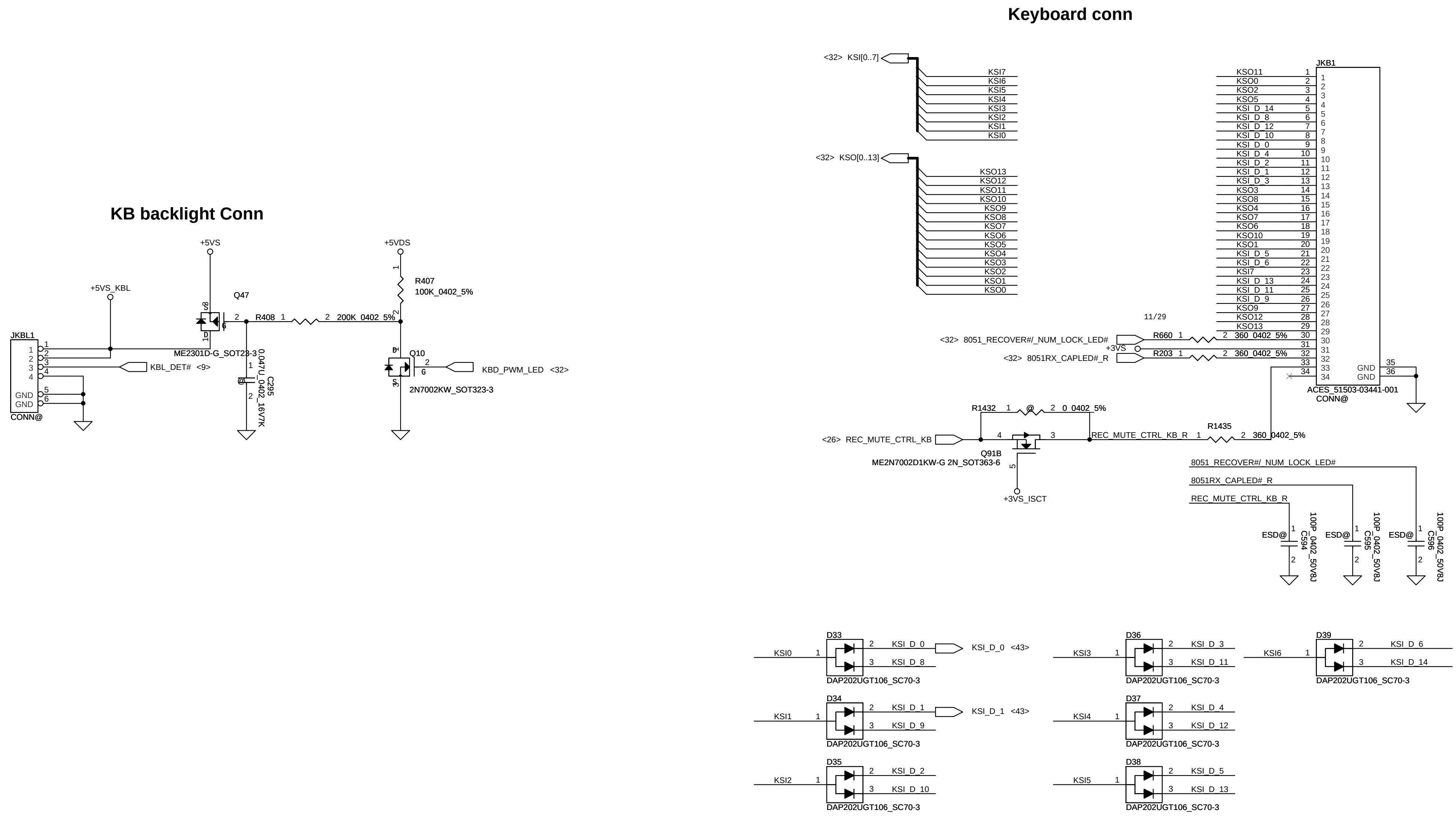
Security Classification	Compal Secret Data		
Issued Date	*2012/03/23*	Deciphered Date	*2012/10/21*

Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

Size	Document Number	Rev
C	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 27 of 62

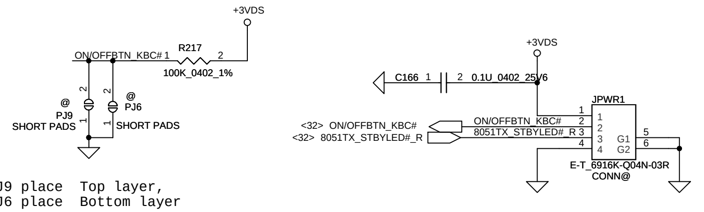


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: KB/TP

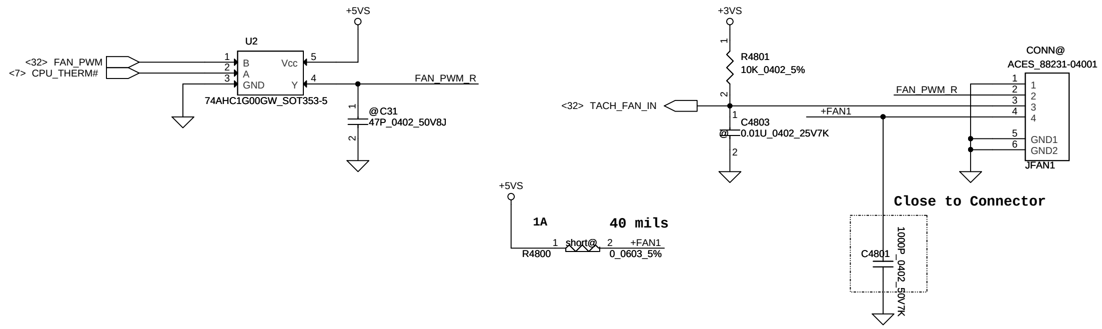
Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014

Power Button Connector



Fan Control Circuit

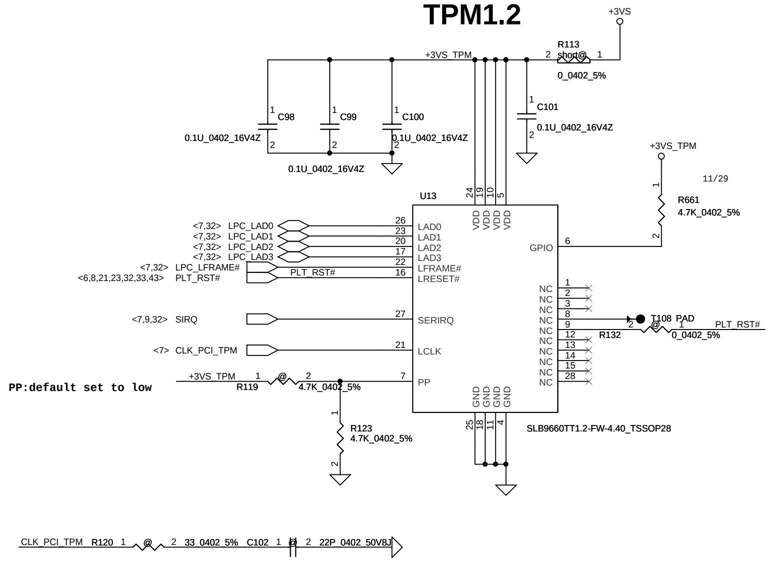


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date 2015/07/08	Title: PWRBTN/FAN

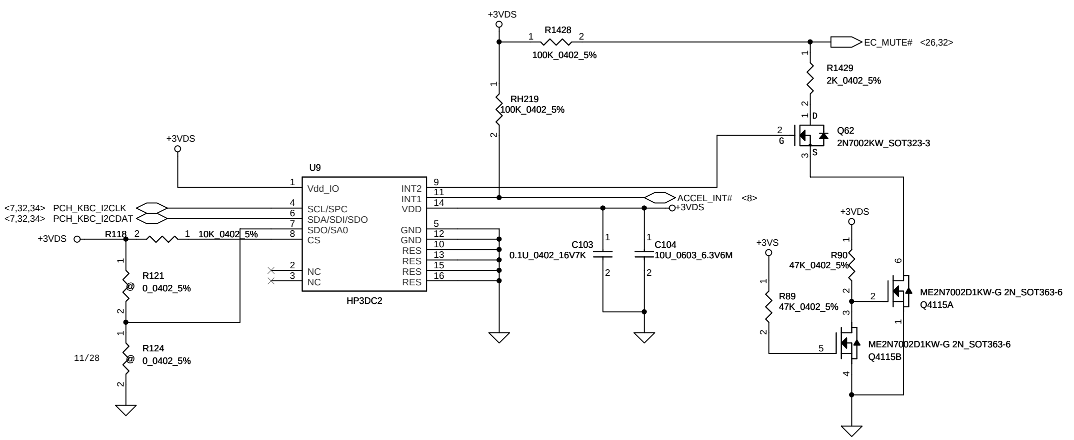
Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014

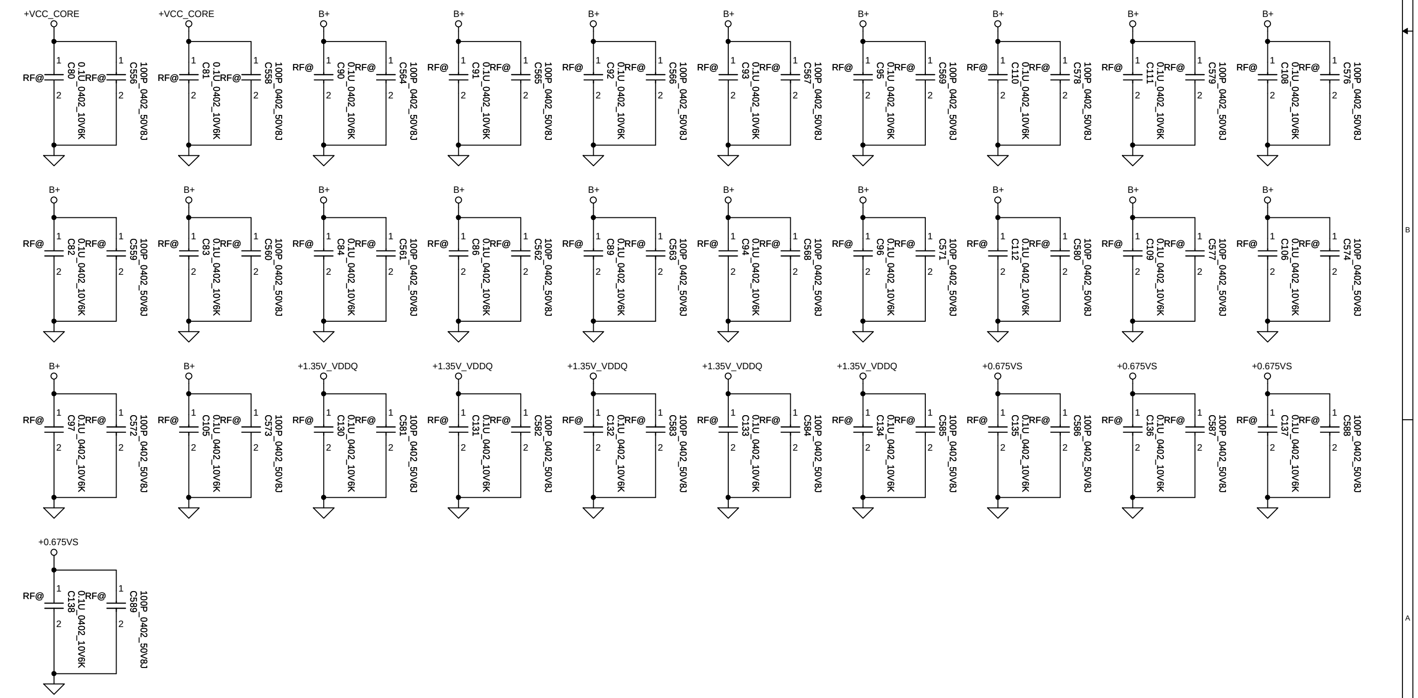
TPM1.2

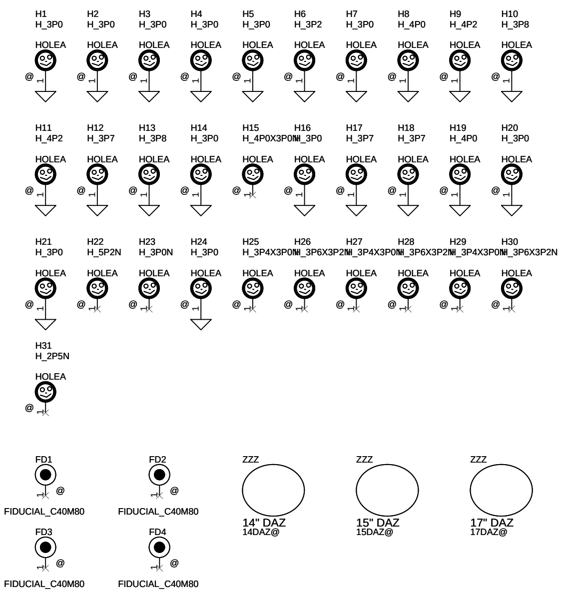


ACCELEROMETER



RF CAP





Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

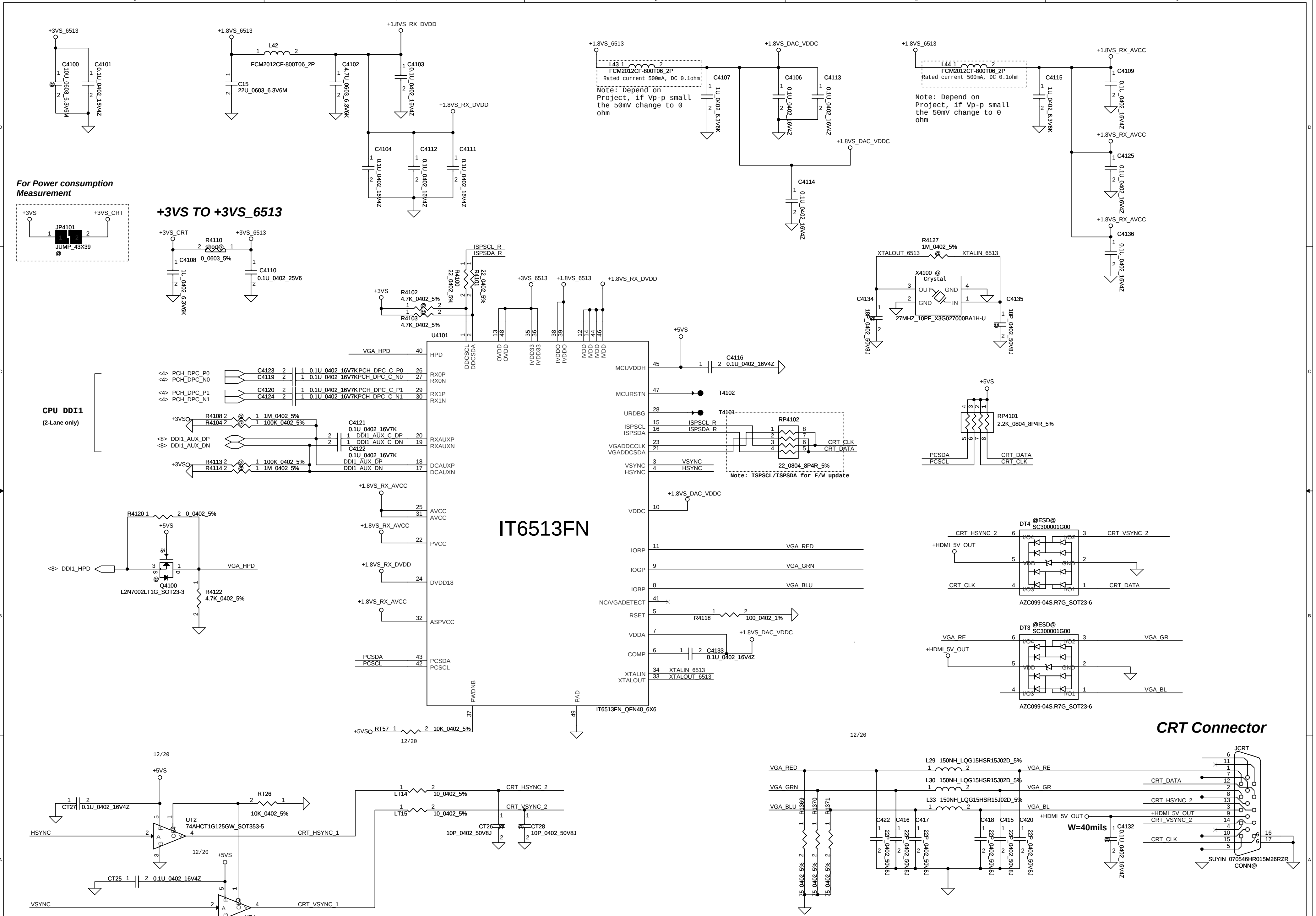
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: *LED/Screw hole*

Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 30 of 62

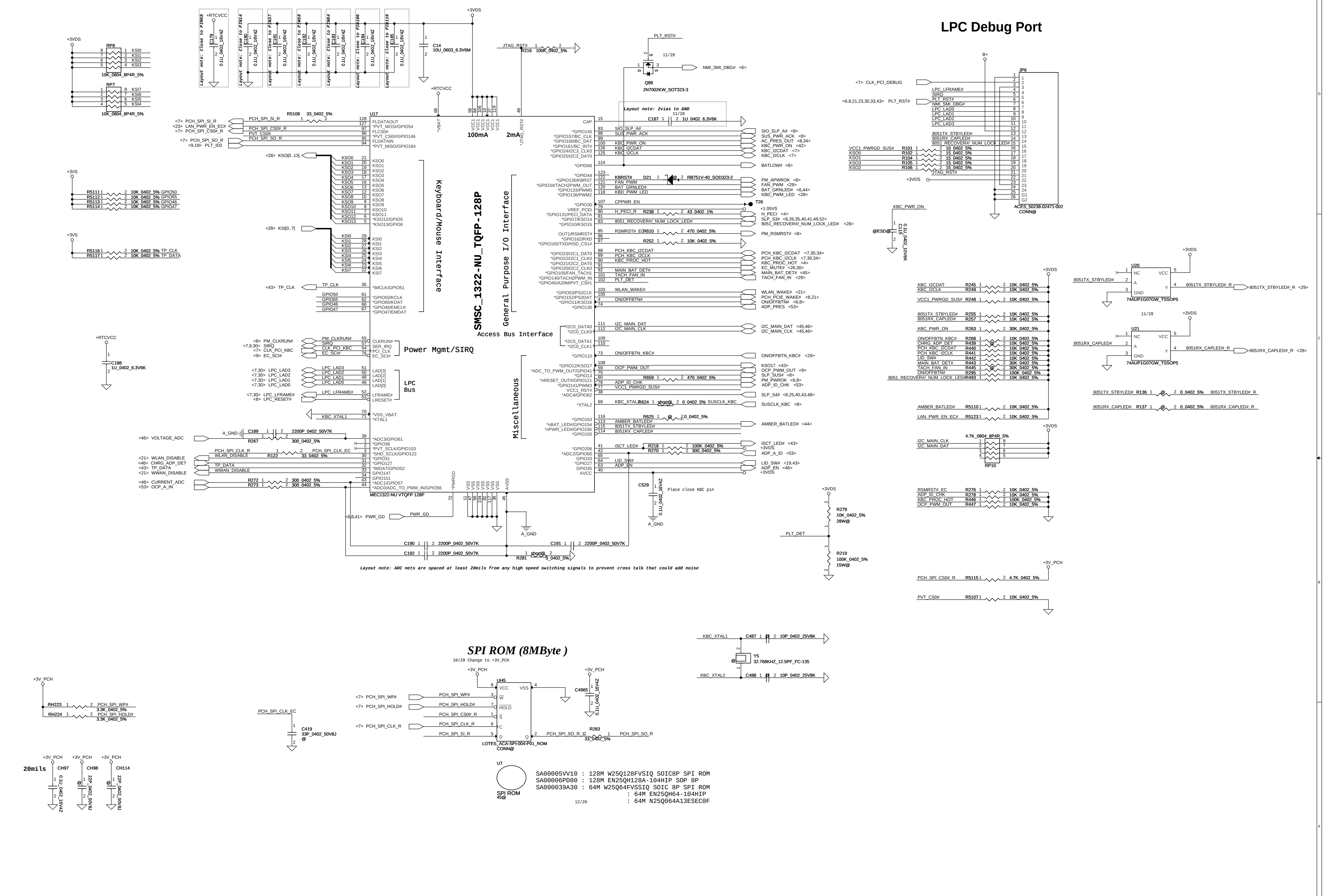


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date	2011/06/29	Title: eDP to CRT

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size	Document Number	Rev
C	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 31 of 62



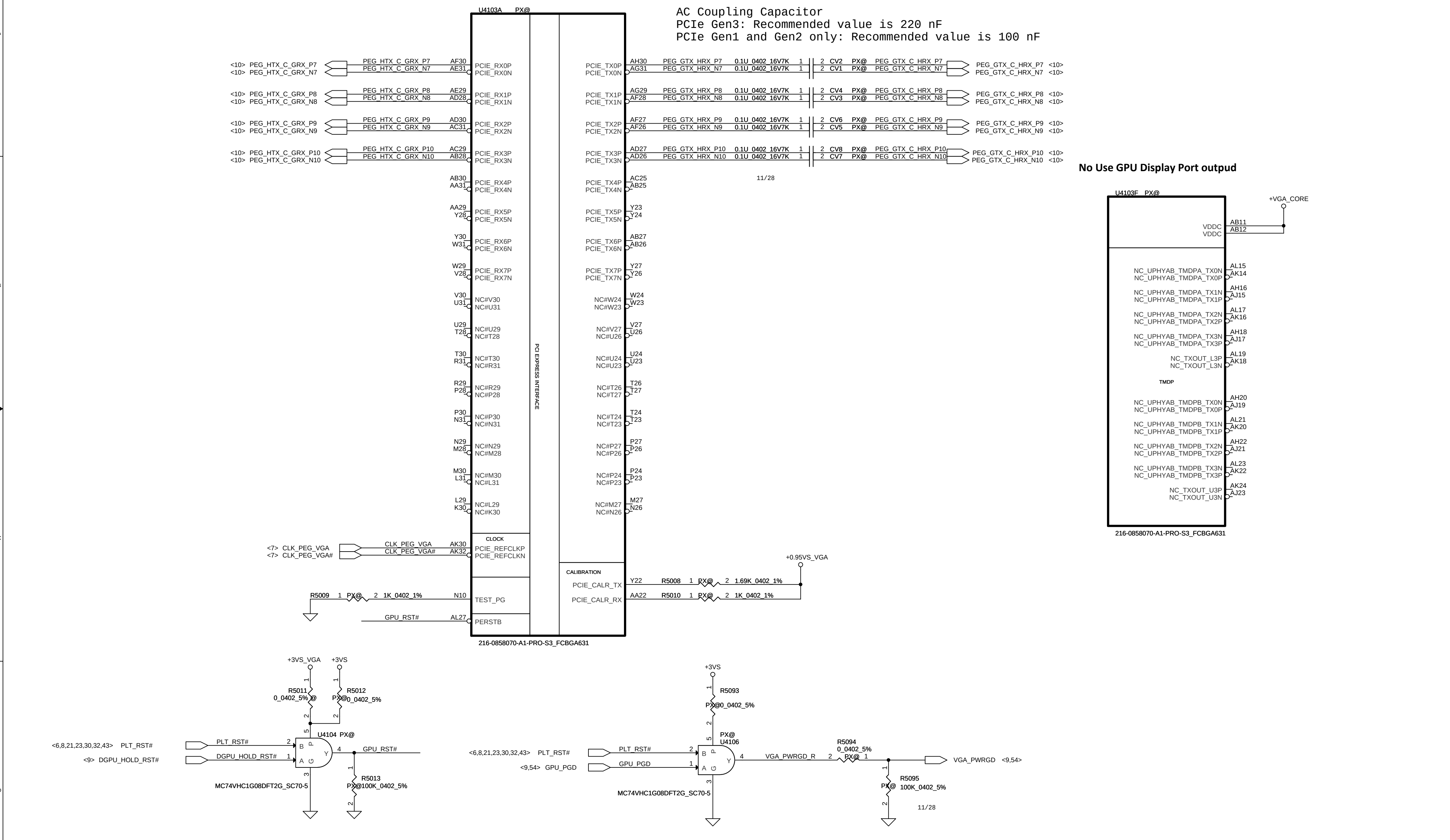
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: EC SMSC_KB1322

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 32 of 62

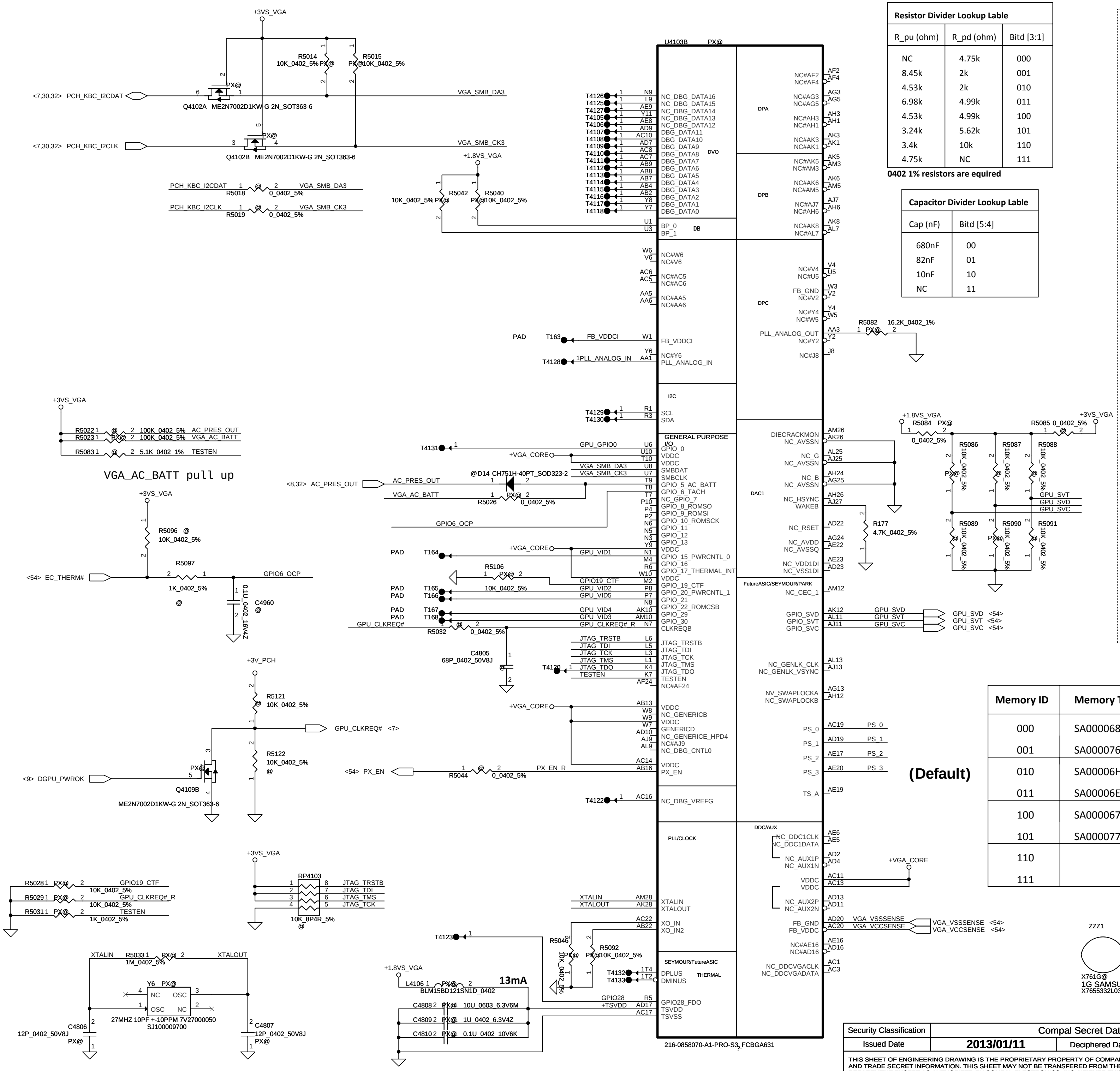


Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **Topaz_PCIE/DP**

Size: Custom | Document Number: **LA-B181P** | Rev: 0.5



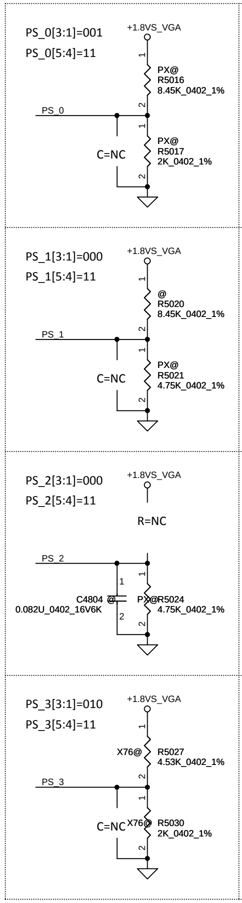
Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :

PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000
PS_1[5:4]=11

Strap Name :

PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11

Strap Name :

PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=010
PS_3[5:4]=11

Strap Name :

PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Memory ID	Memory Type	Configuration	Size	R5027	R5030	X76 P/N
000	SA000068U80	Samsung K4W2G1646Q-BC1A	1GB	NC	4.75K	X7655332L03
001	SA000076P00	Samsung K4W4G1646D-BC1A	2GB	8.45K	2K	X7655332L06
010	SA00006H440	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7655332L01
011	SA00006E800	Hynix H5TC4G63AFR-11C	2GB	6.98K	4.99K	X7655332L04
100	SA000067540	Micron MT41J128M16JT-093G:K	1GB	4.53K	4.99K	X7655332L02
101	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	3.24K	5.62K	X7655332L05
110		Nanya 128x16 NT5CB128M16FP	1GB	3.4K	10K	
111		Nanya 256x16 NT5CB256M16CP	2GB	4.75K	NC	

(Default)

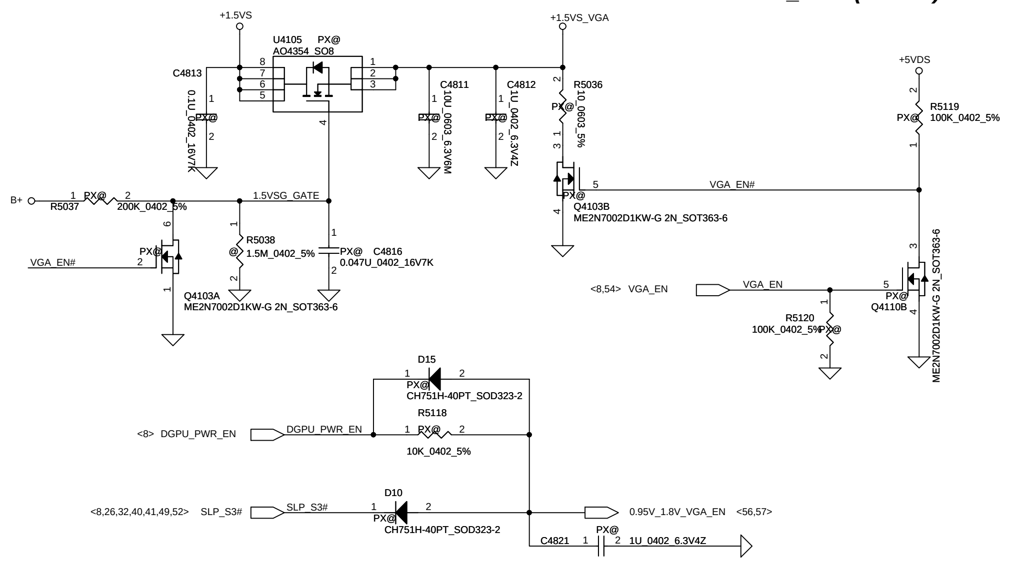
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

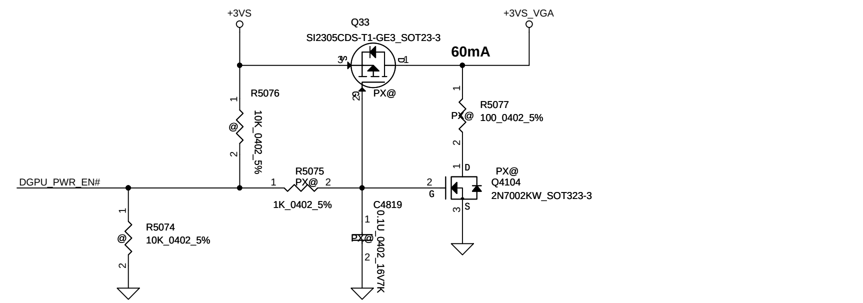
Title: **Topaz_MSIC**

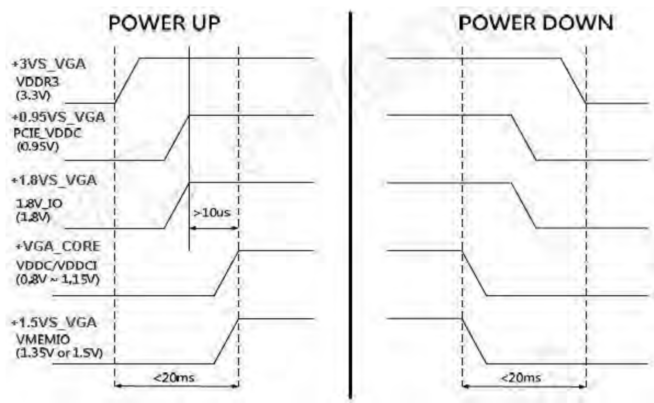
Size: Custom | Document Number: **LA-B181P** | Rev: 0.5

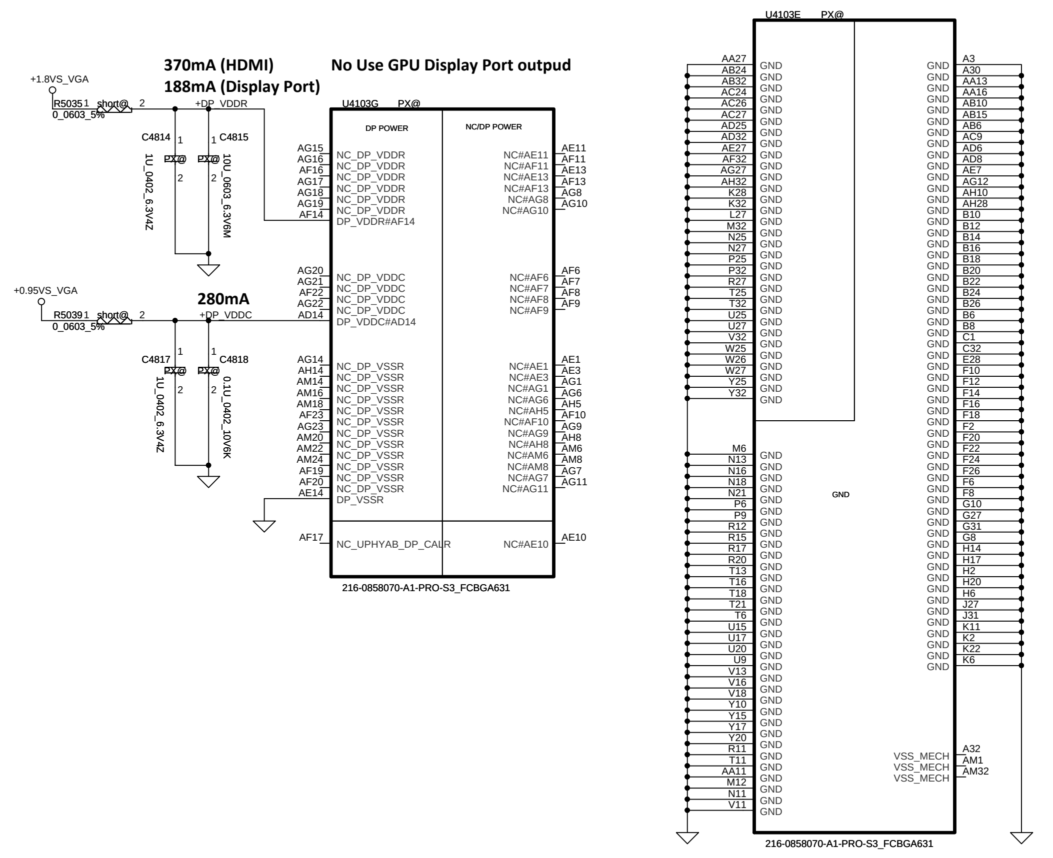
+1.5VS to +1.5VS_VGA (2.096A)

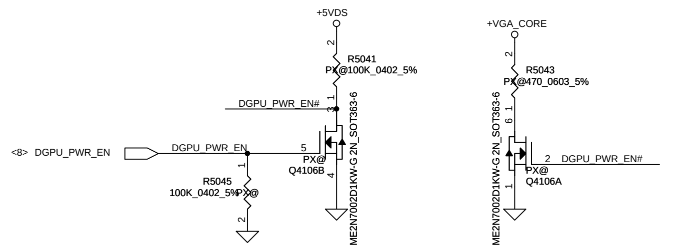


+3VS to +3VS_VGA (25mA)









Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: Topaz_Power/GND

Size: Custom | Document Number: LA-B181P | Rev: 0.5

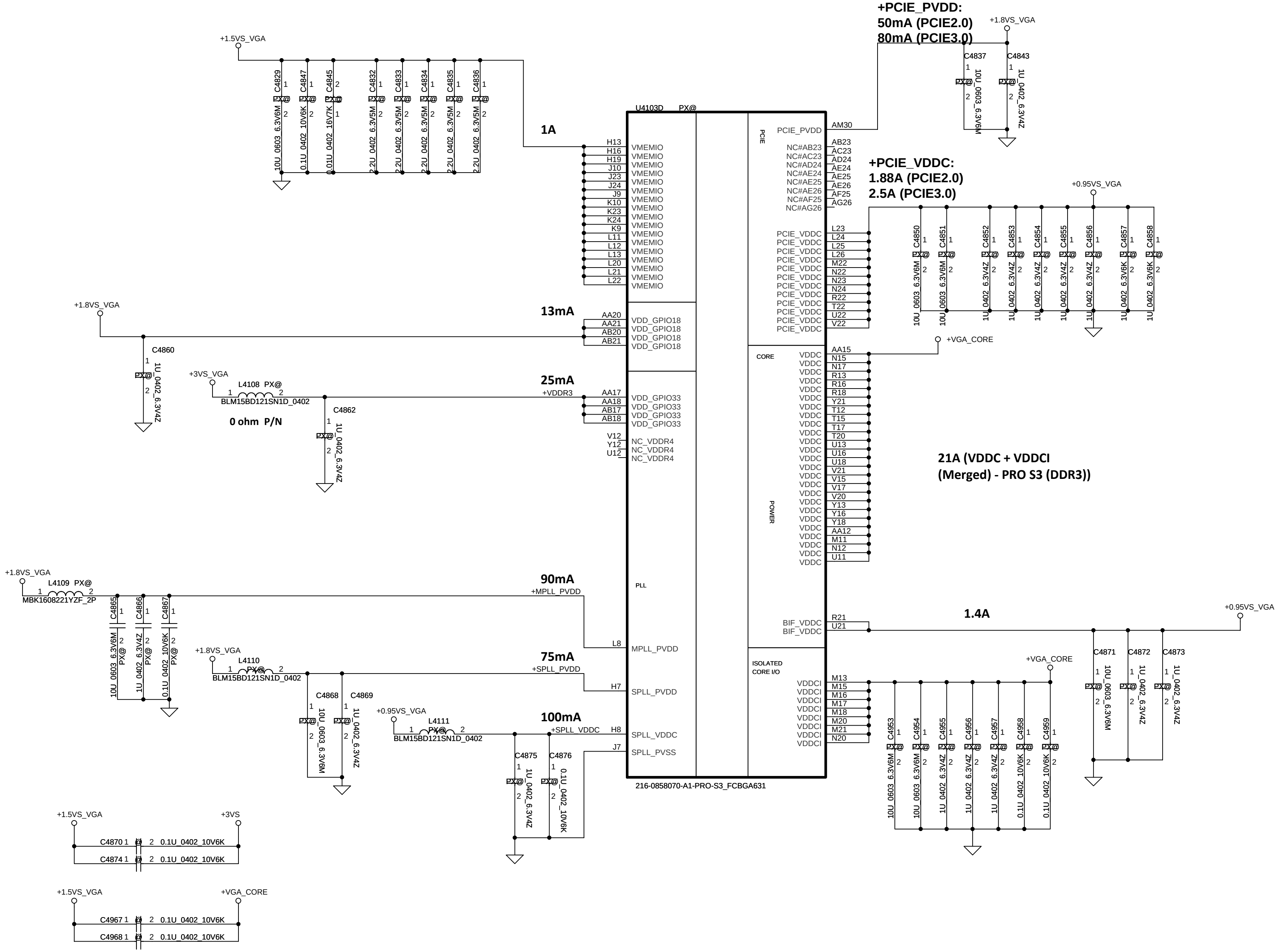
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1

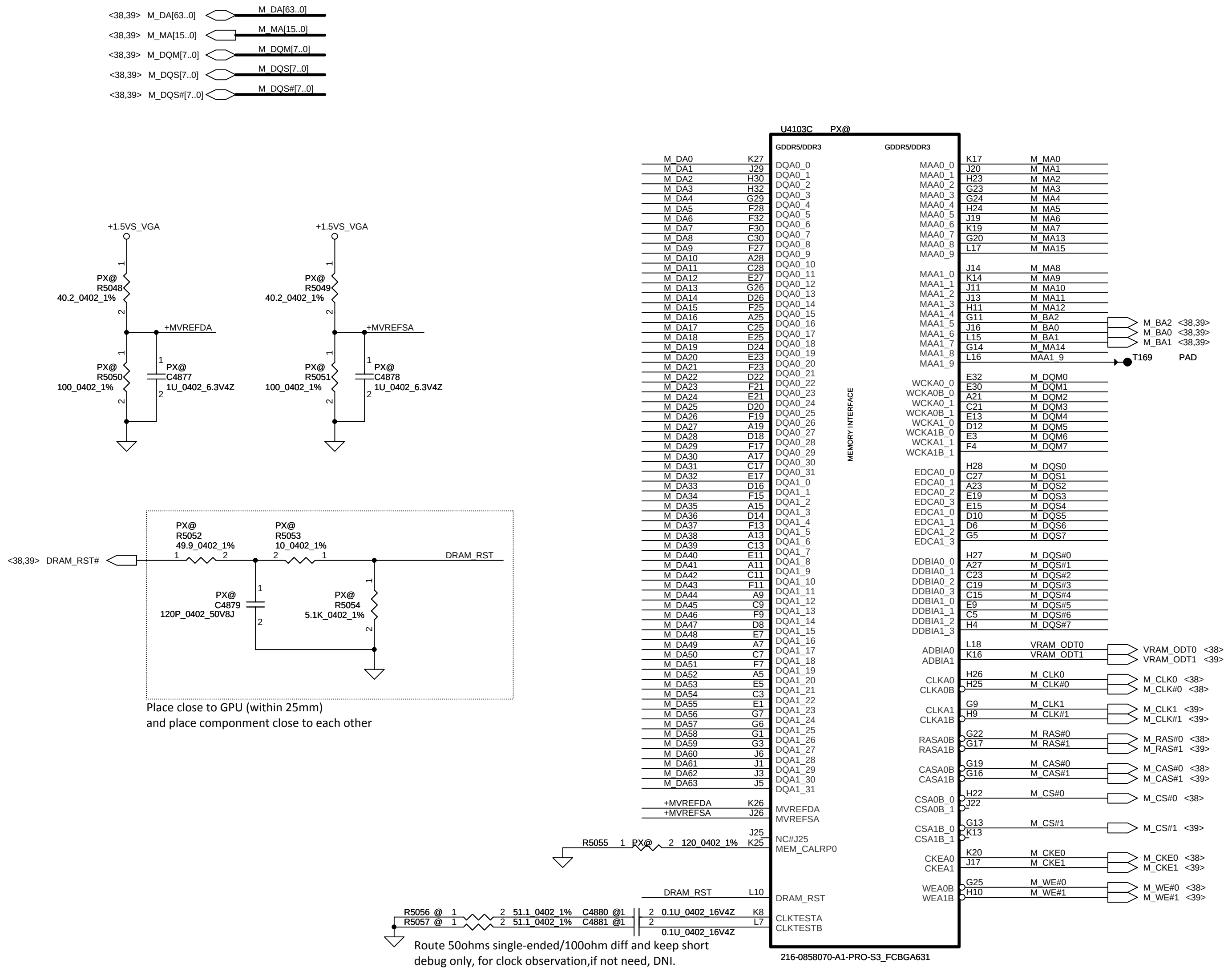


Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **Topaz_Power**

Size: Custom | Document Number: **LA-B181P** | Rev: 0.5



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

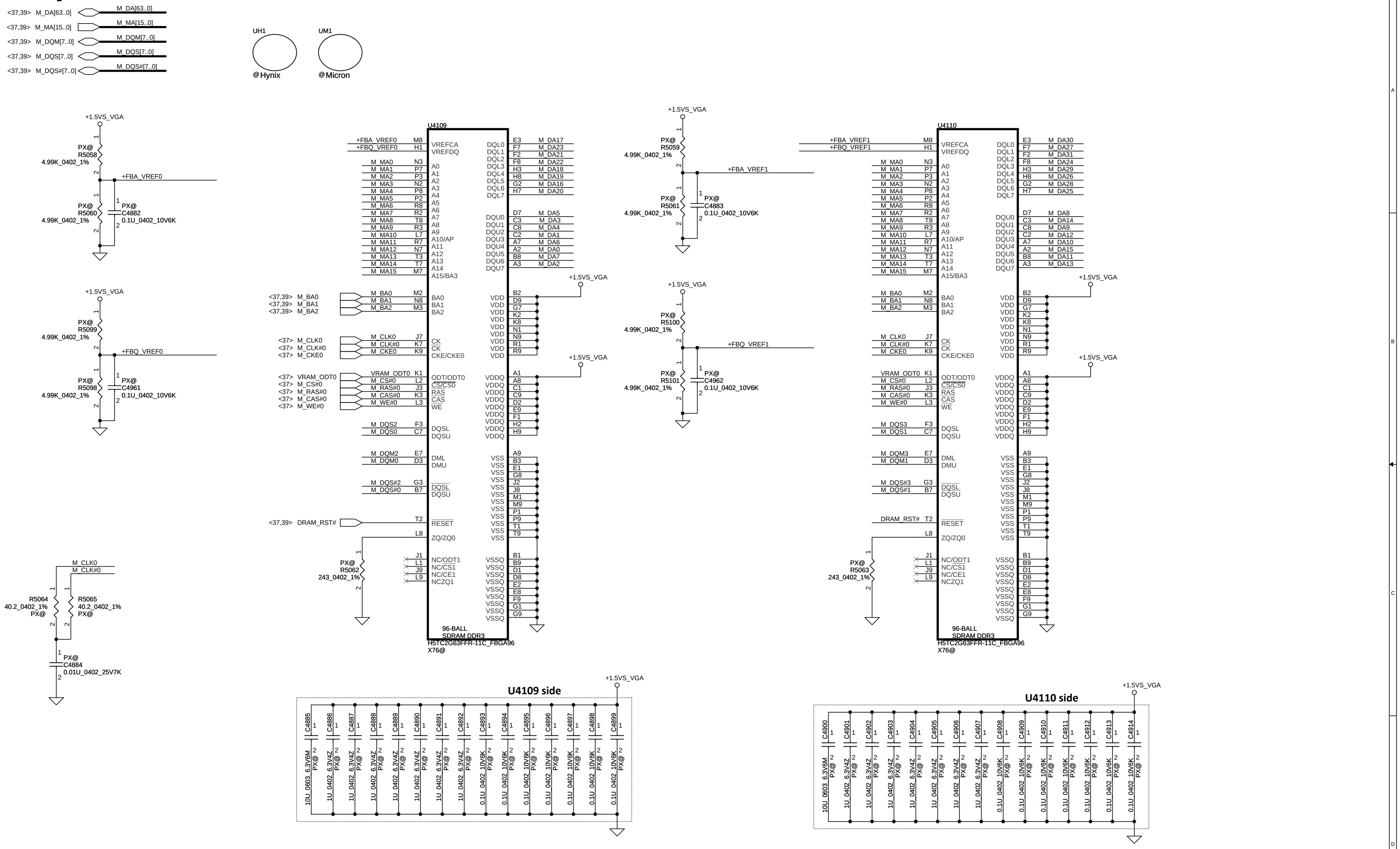
Compal Electronics, Inc.

Title: **Topaz_MEM**

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 37 of 62

Memory Partition A - Lower 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

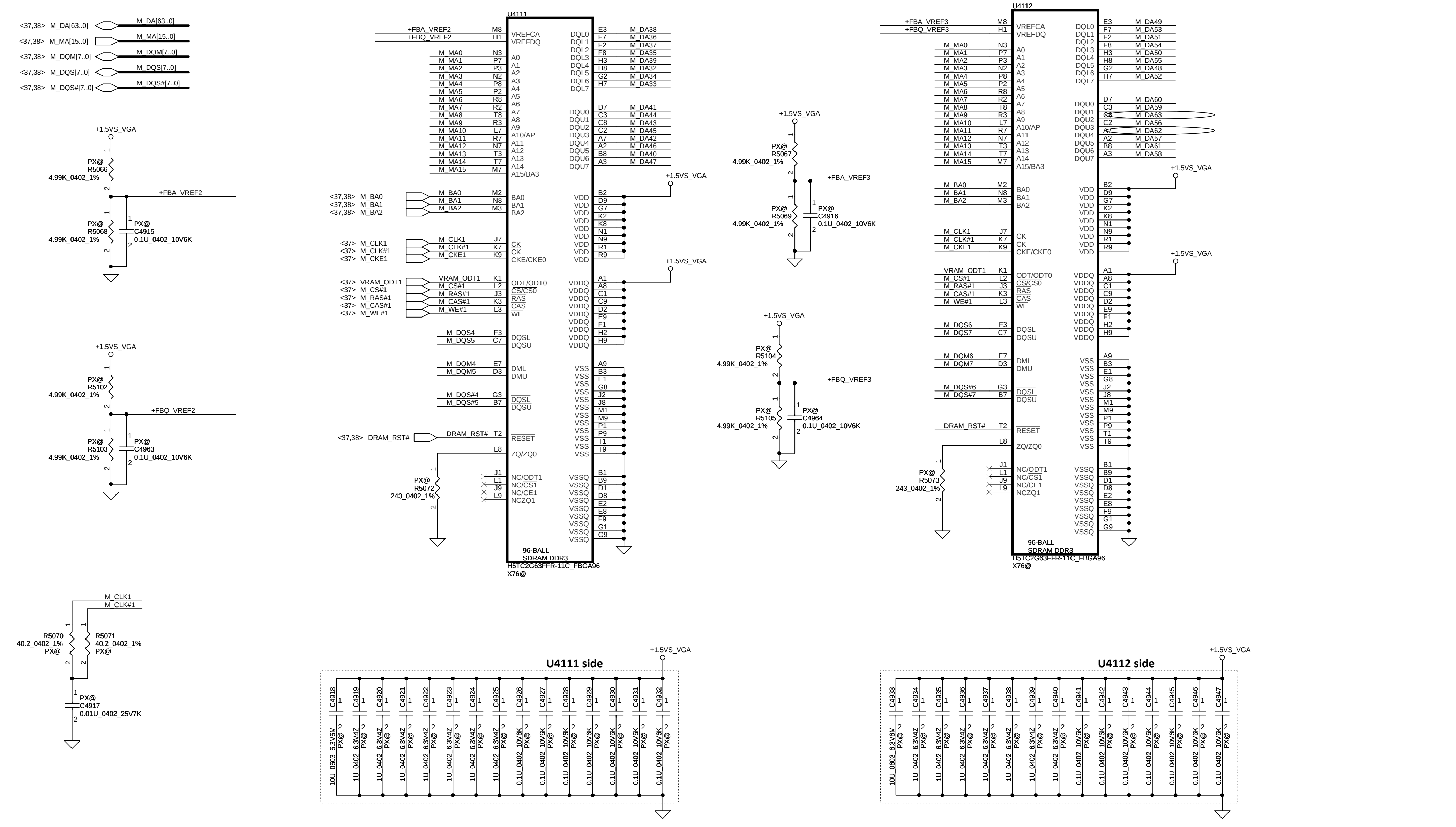
Compal Electronics, Inc.

Title: **Topaz_VRAM A Lower**

Size: Custom | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 38 of 62

Memory Partition A - Upper 32 bits

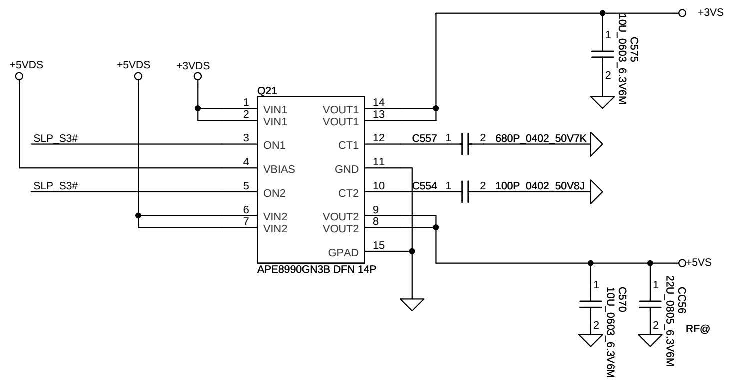


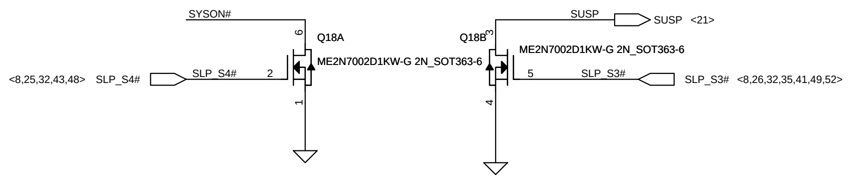
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

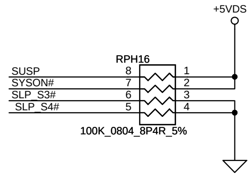
Compal Electronics, Inc.

Title: **Topaz_VRAM A Upper**

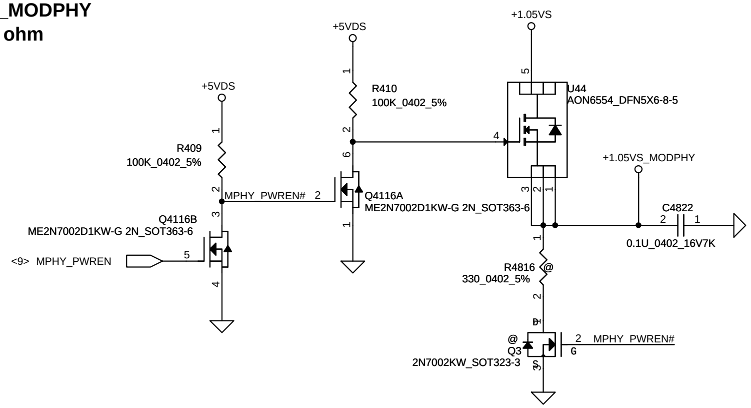
Size: Custom | Document Number: **LA-B181P** | Rev: 0.5



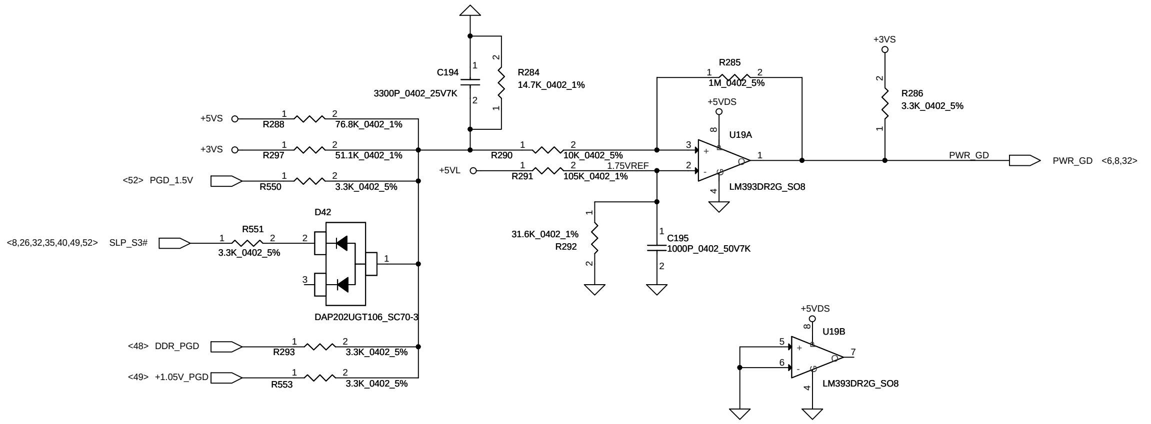




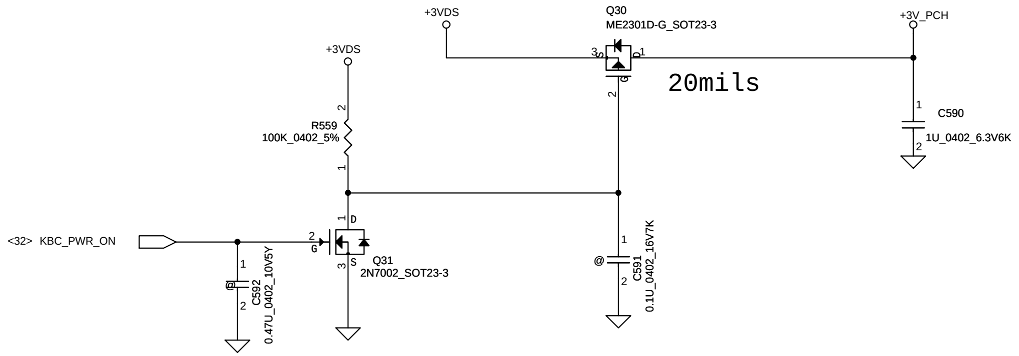
CPU +V1.05DX_MODPHY
Max Rdson <6m ohm
1840mA



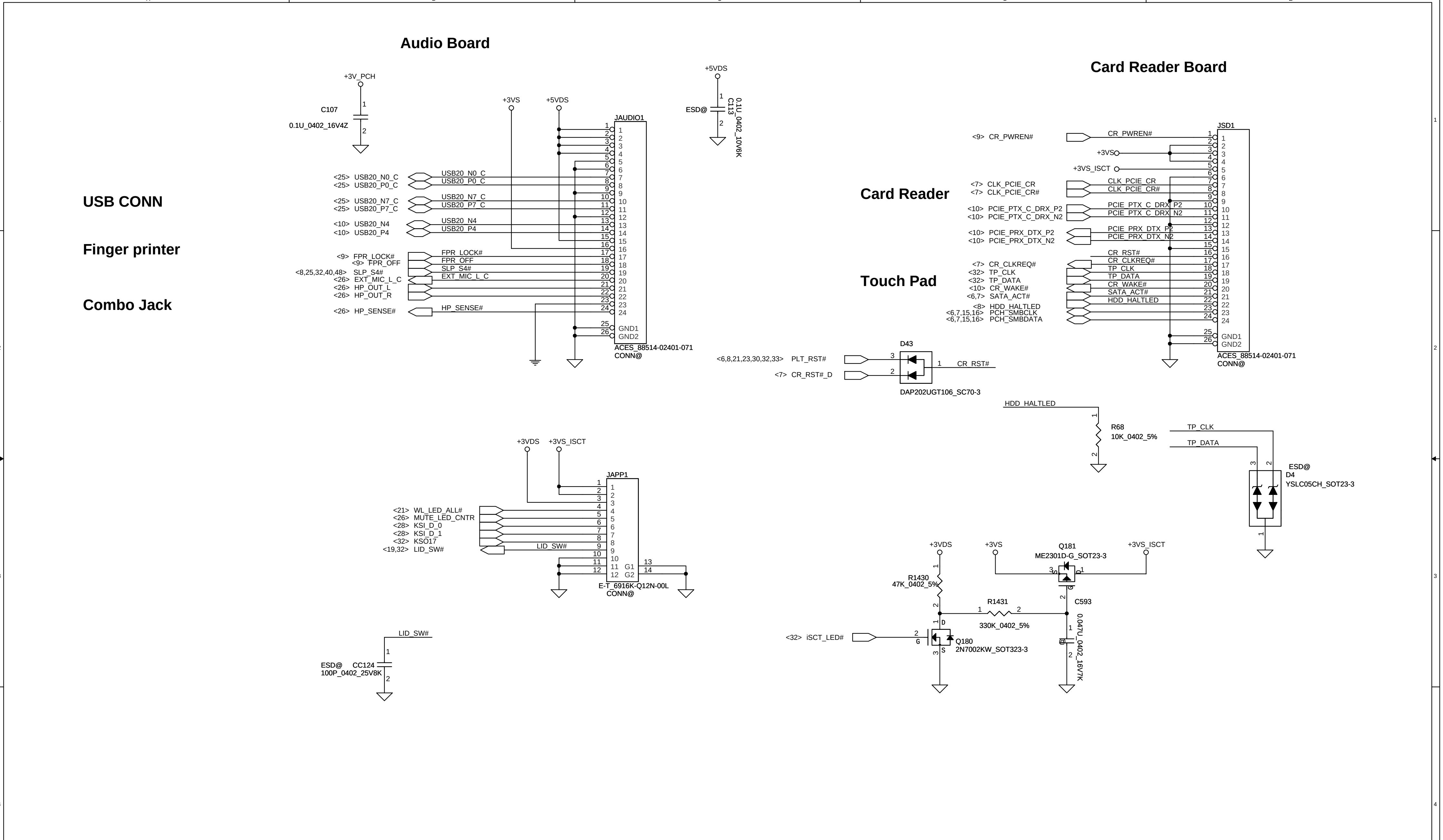
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-B181P; Rev: 0.5
				Date: Tuesday, March 25, 2014; Sheet 40 of 62



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: WAKE and RST-1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: C; Document Number: LA-B181P; Rev: 0.5
			Date: Tuesday, March 25, 2014; Sheet 41 of 62



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: DC DC Device-1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom; Document Number: LA-B181P; Rev: 0.5
				Date: Tuesday, March 25, 2014; Sheet 42 of 62

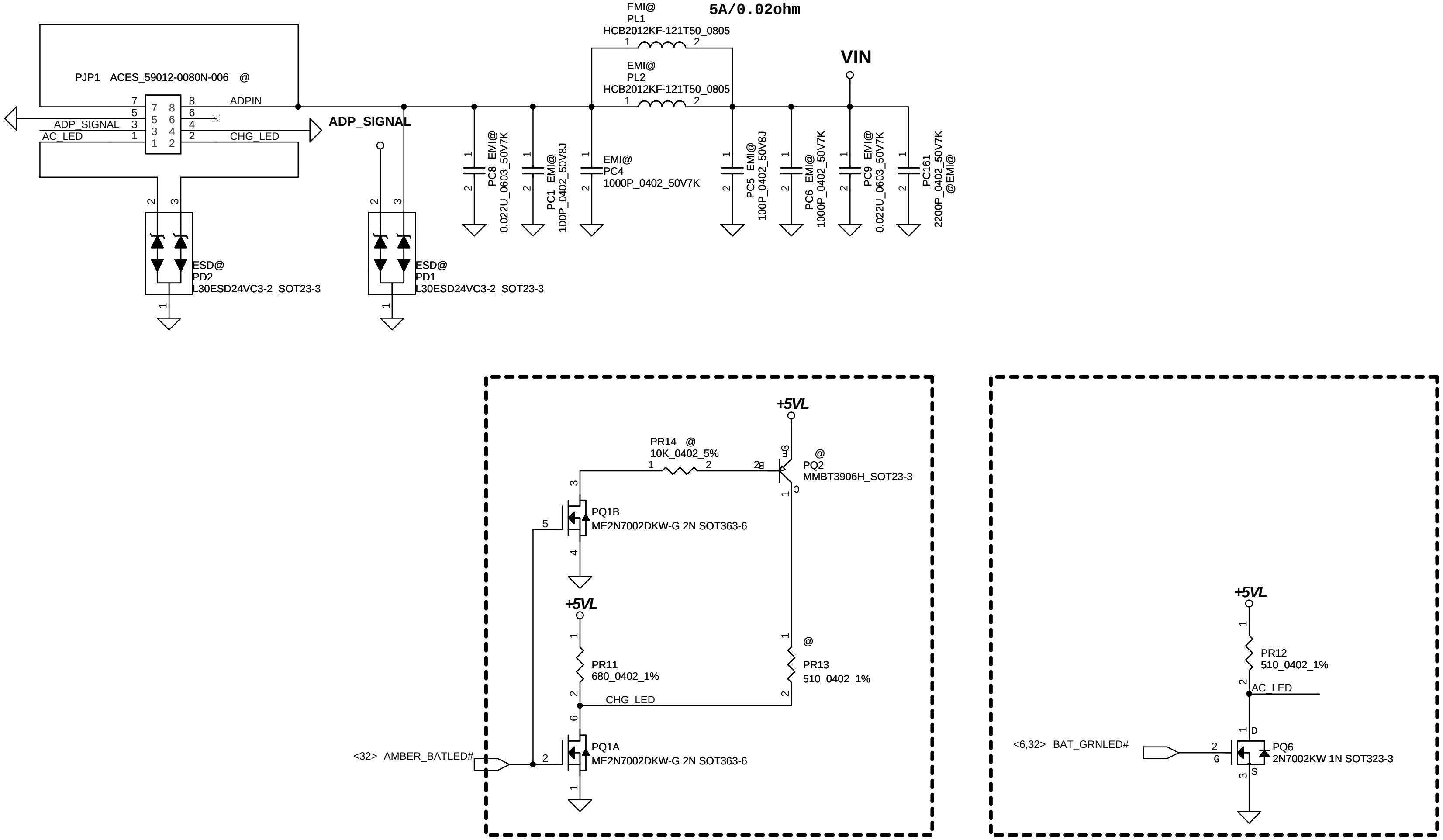


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: DC DC Device-1

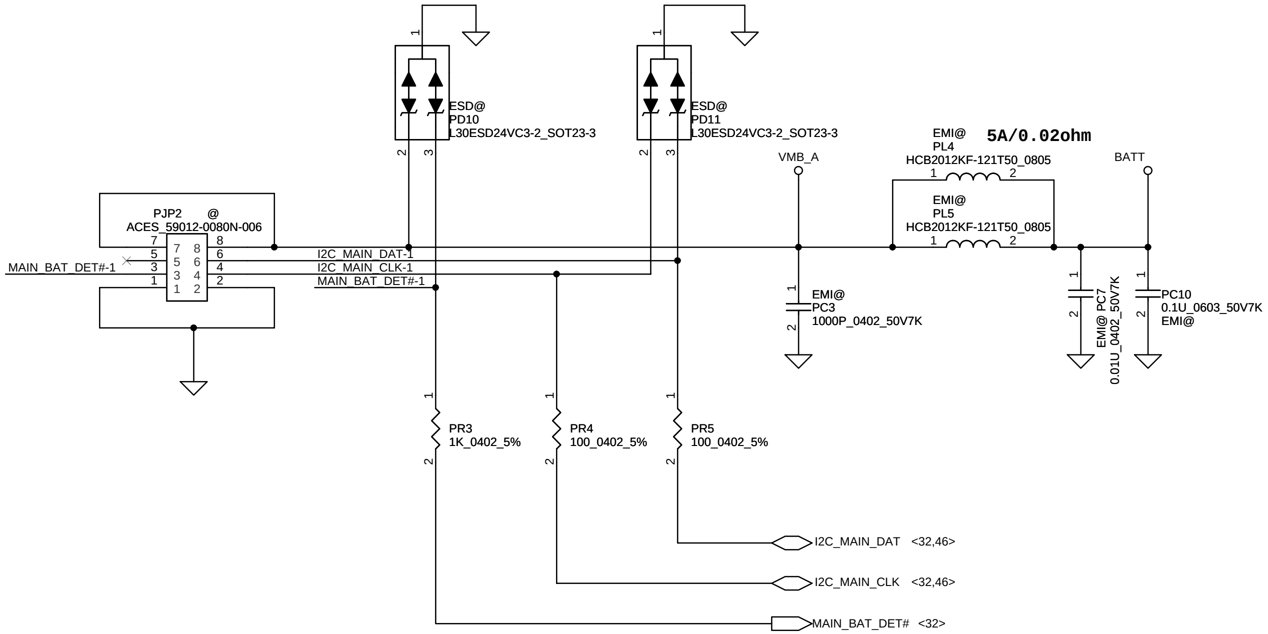
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size	Document Number	Rev
Custom	LA-B181P	0.5

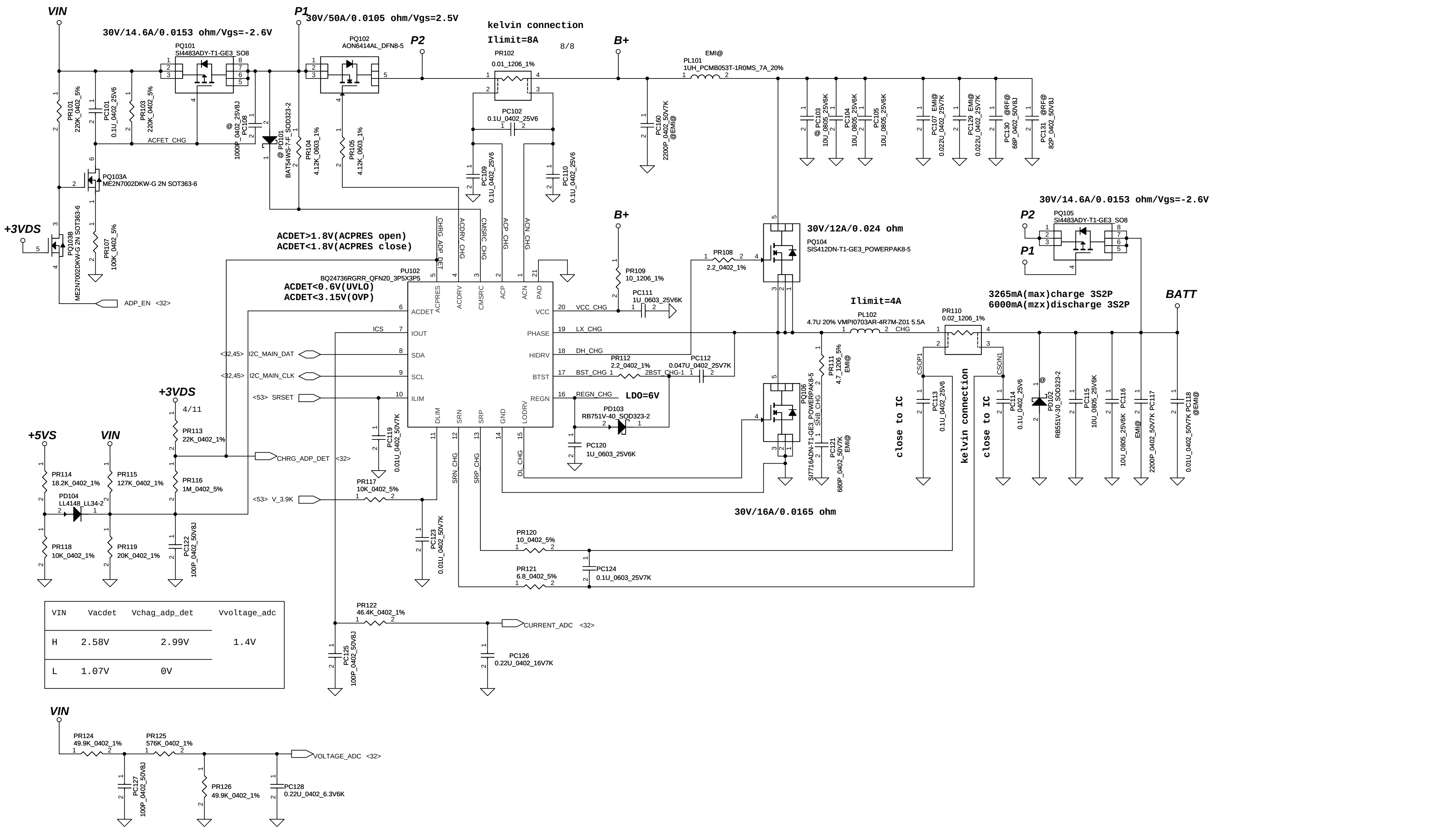
Date: Tuesday, March 25, 2014 — Sheet 43 of 62



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title: DC Conn	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-B181P	Rev: 0.5
				Date: Tuesday, March 25, 2014	Sheet 44 of 62



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title: BATT Conn	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-B181P	Rev 0.5
				Date: Tuesday, March 25, 2014	Sheet 45 of 62



VIN	Vacdet	Vchag_adp_det	Vvoltage_adc
H	2.58V	2.99V	1.4V
L	1.07V	0V	

Ilimit=20*(Vsrp-Vsrn)=20*Ich*Rch
up to Ilimit=1.6V(disable)
R=10m ohm I=8A
R=20m ohm I=4A
fs=750k

Iripple=Vin*D(1-D)/(fs*L),
D=0.5 (worst)
Iripple=1.418A
Isat(L)=Ichg+0.5*Iripple=4+0.5*1.418=4.709A

ILIM>1.6V disable
ILIM<75mV disable
ILIM>105mV enable

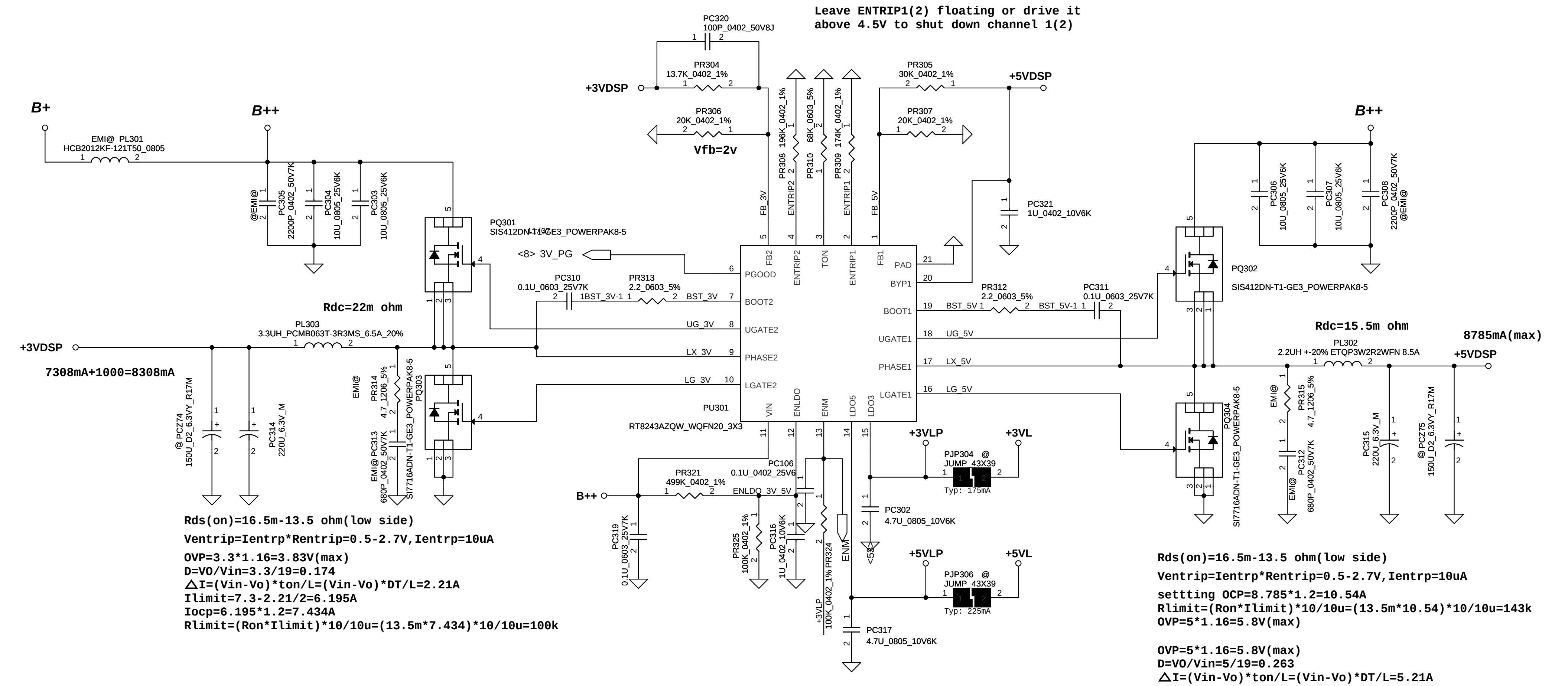
DLIM>1.1V disable
DLIM<870mV disable
DLIM>896mV enable(buck to boost)
default dischager current limit 4.096A

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: LA-B181P | Rev: 0.5



Rds(on)=16.5m-13.5 ohm(low side)
Ventrip=Ientrp*Rentrip=0.5-2.7V,Ientrp=10uA
OVP=3.3*1.16=3.83V(max)
D=VO/Vin=3.3/19=0.174
△I=(Vin-Vo)*ton/L=(Vin-Vo)*DT/L=2.21A
Ilimit=7.3-2.21/2=6.195A
Iocp=6.195*1.2=7.434A
Rlimit=(Ron*Ilimit)*10/10u=(13.5m*7.434)*10/10u=100k

Rds(on)=16.5m-13.5 ohm(low side)
Ventrip=Ientrp*Rentrip=0.5-2.7V,Ientrp=10uA
settting OCP=8.785*1.2=10.54A
Rlimit=(Ron*Ilimit)*10/10u=(13.5m*10.54)*10/10u=143k
OVP=5*1.16=5.8V(max)

OVP=5*1.16=5.8V(max)
D=VO/Vin=5/19=0.263
△I=(Vin-Vo)*ton/L=(Vin-Vo)*DT/L=5.21A
Ilimit=8.785-5.21/2=6.18A
Iocp=6.195*1.2=7.416A
Rlimit=(Ron*Ilimit)*10/10u=(13.5m*7.416)*10/10u=100k

<1>5V=283KHz 3V=330KHz (Vin=6.5 ~ 12v)
<2>5V=321KHz 3V=375KHz (Vin=12 ~ 25v)
(By Rton= 68K ohm)

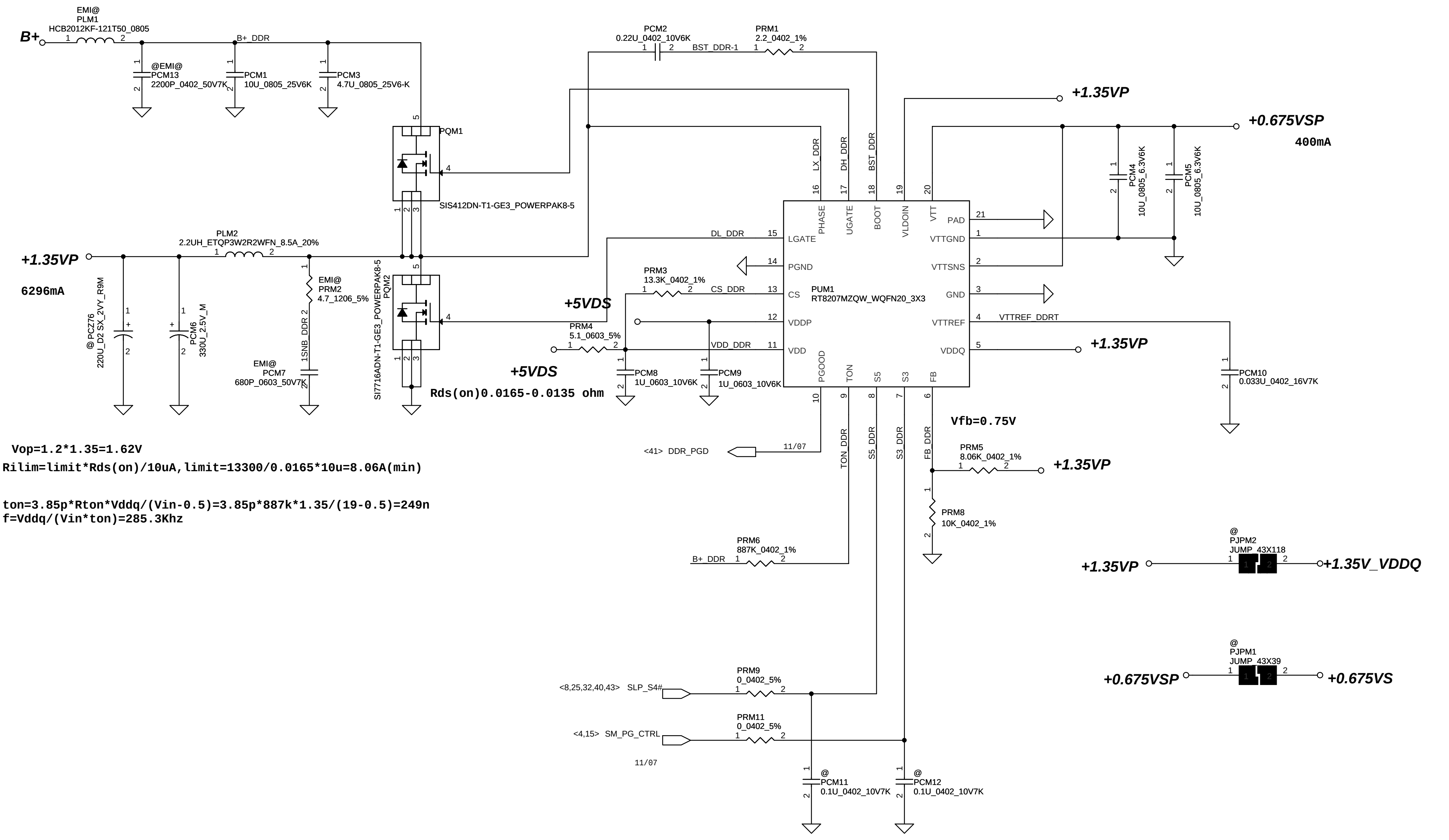
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: 3VDSP/5VDSP

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



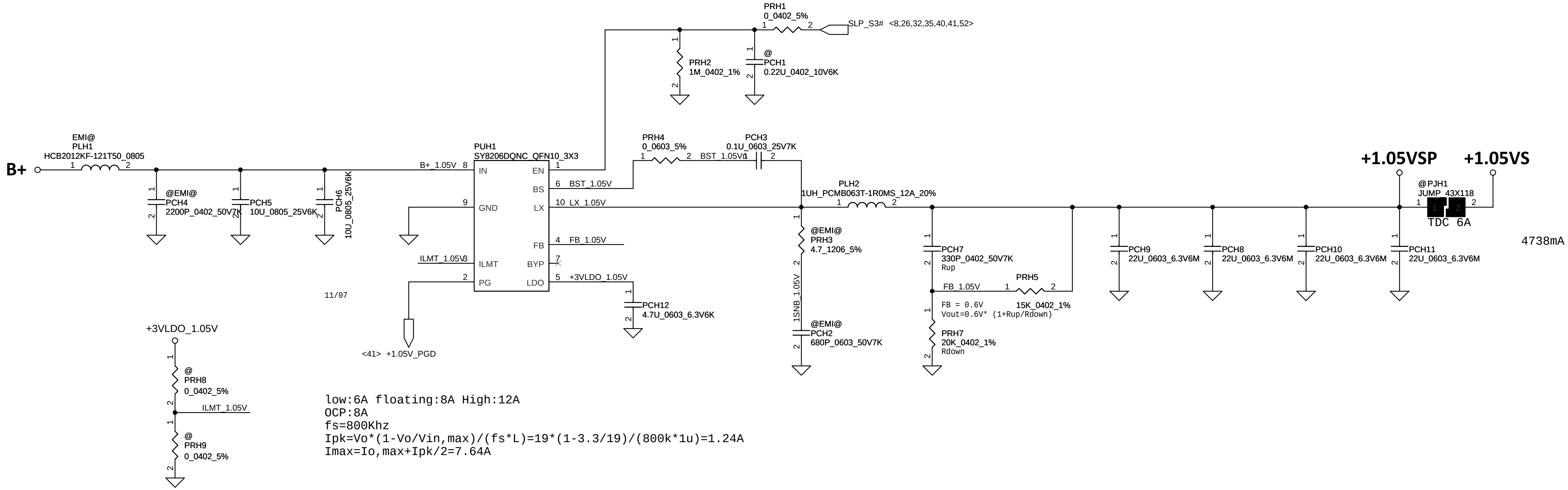
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: **+1.35V/+0.675VS**

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 |



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *+1.05VS*

Size | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 49 of 62

PRZ5:Vo-usr=1.7*(150/(150+9.53))=1.598V
Vusr=540mV
PRZ11:disable OSR&PT,Rosr=150k

PRZ10:setting fs R=150==>1Mhz

Ramp setting:
PRZ9=100K type:160mV
PRZ9>=150K type:40mV

boot voltage setting:
Vb-ram=1V==>2V
Vb-ram=0V==>1.7V
Vb-ram>1.525V==>0V

Iccmax=32A(15w),Iccmax=40A(28w)
IccTDC=10A(15w),IccTDC=16A(28w)
IccDyn=27A(15w),IccDyn=32A(28w)

OCP voatge seeting:
PRZ8=39K ==>18.9mV
Vimon=1.7V

Rp_n=10.74k Rcs(eff)=0.6m ohm
1.7V=10*(1+Rimon/39k)*0.6m*32,Rimon=345k

ALERT goes low,THERM=1.08V
VR_HOT goes low,THERM=1.1V

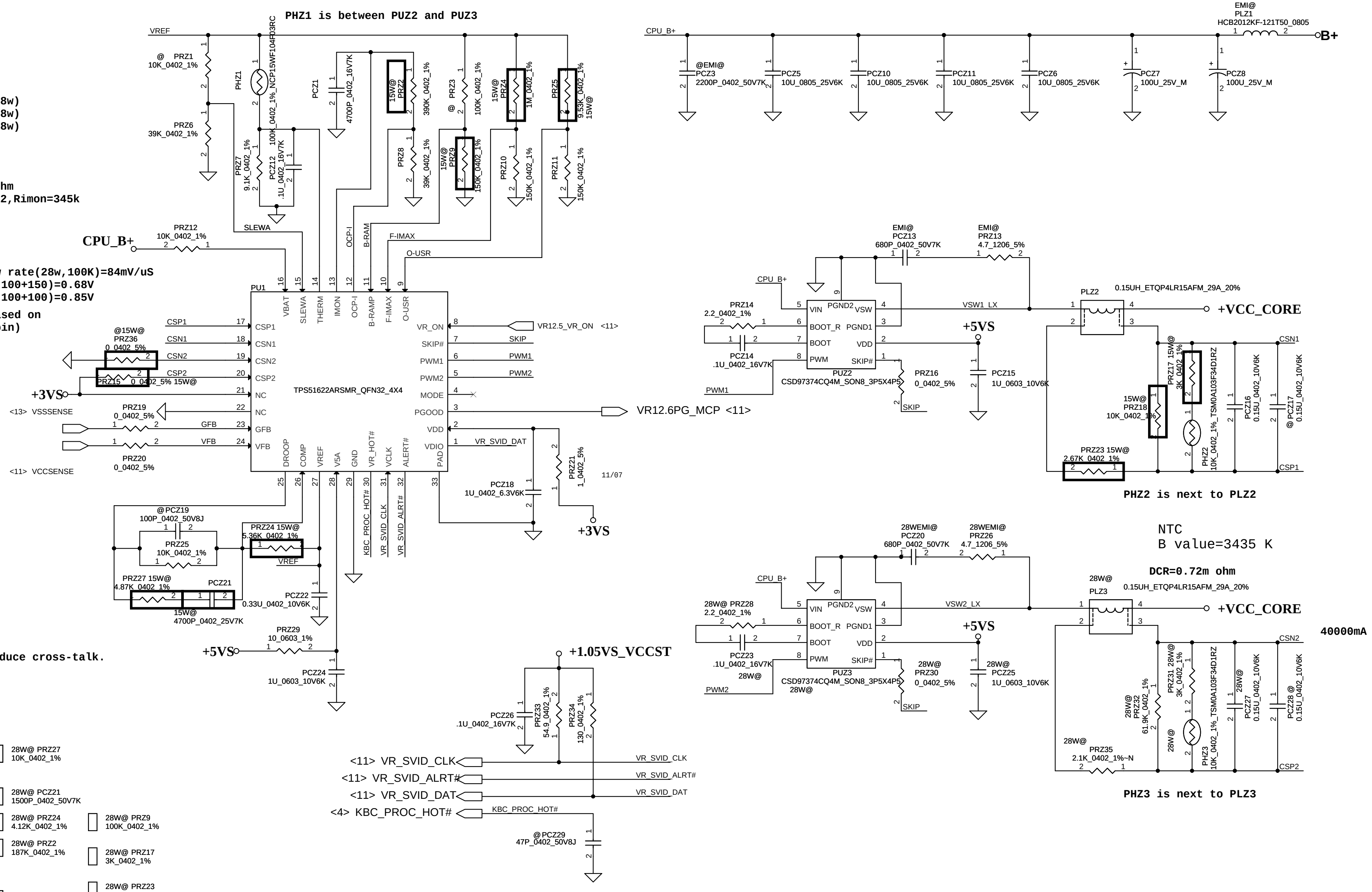
slew rate(15w,150K)=96mV/uS,slew rate(28w,100K)=84mV/uS
address selection(15w):1.7*100/(100+150)=0.68V
address selection(28w):1.7*100/(100+100)=0.85V

On-tome(ton):ON-time is fixed based on
the input voltage (at the VBAT pin)

Vssense and Vccsense need to
be difference pair

Droop:Error amplifier output.

ALERT between VCLK and VDIO to reduce cross-talk.



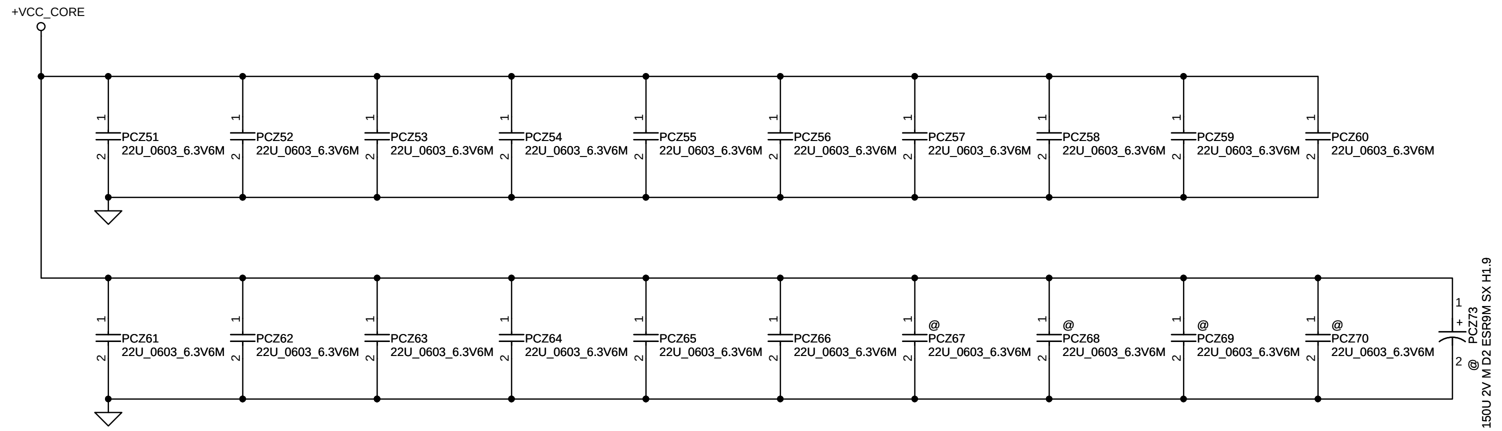
not mount需特別注意(15w@,28w@)

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *+CPU_CORE*

Size | Document Number: LA-B181P | Rev: 0.5



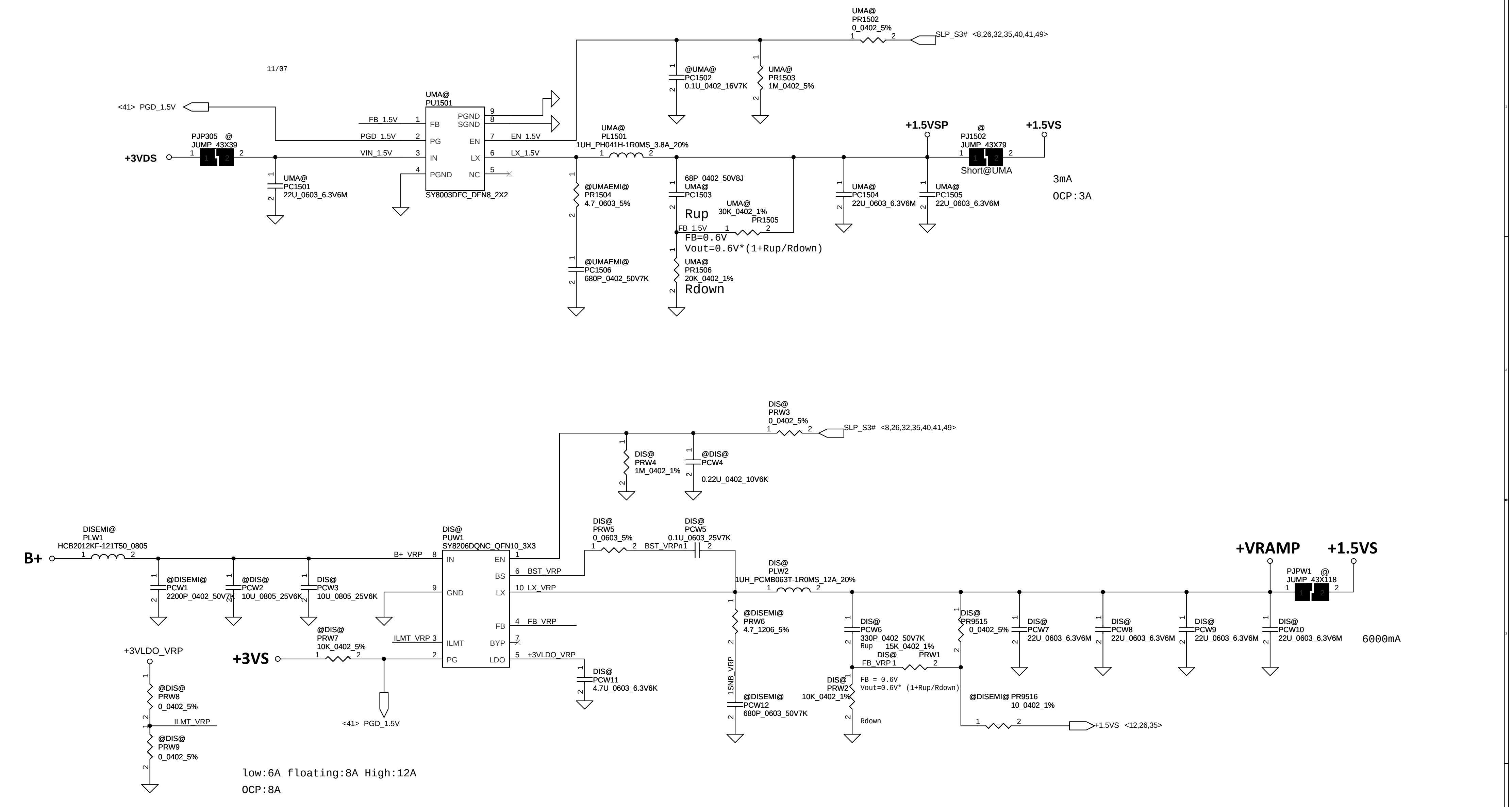
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

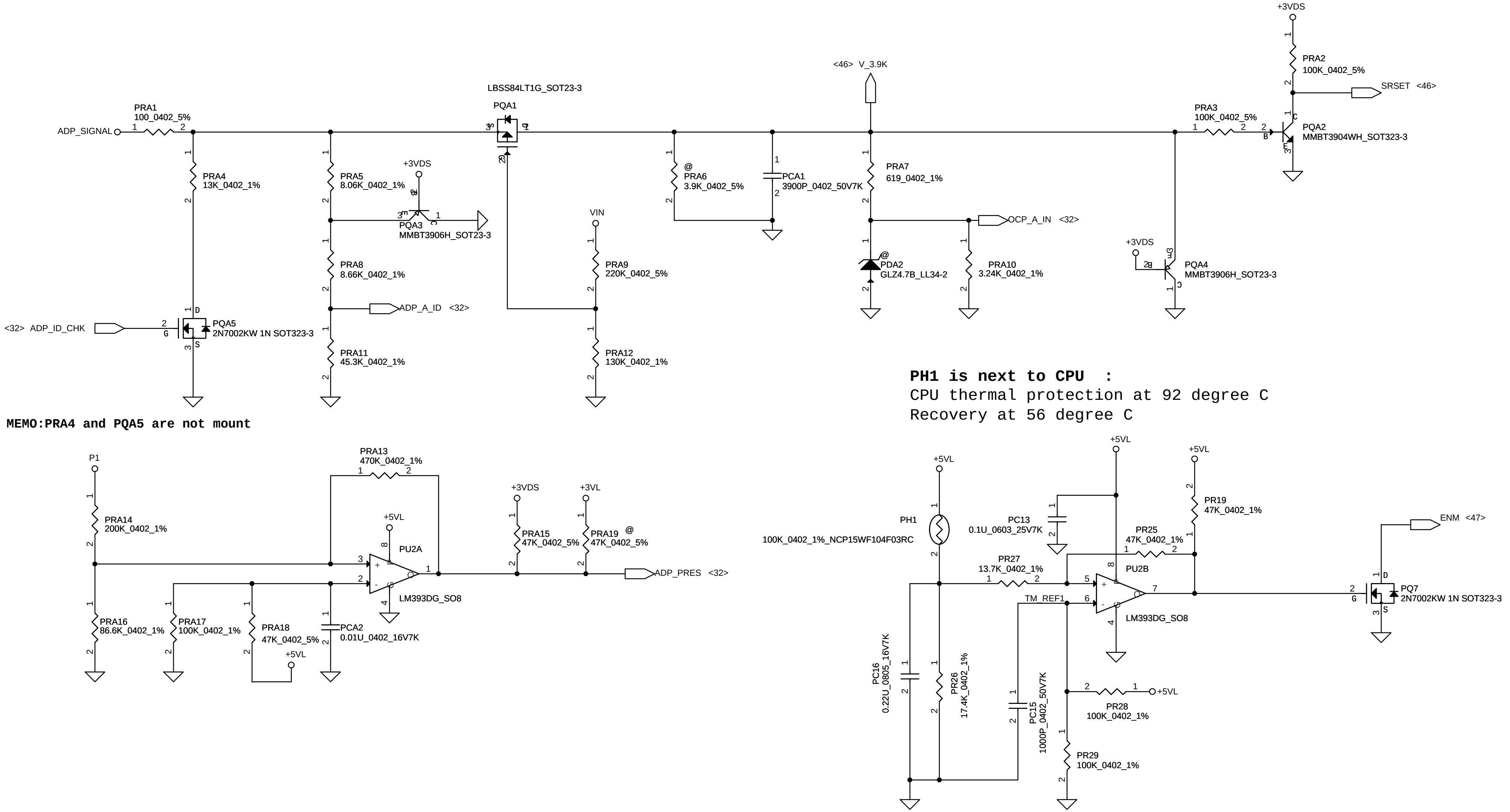
Title: ***PROCESSOR DECOUPLING***

Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 |



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title: +1.5VS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-B181P / Rev 0.5
				Date: Tuesday, March 25, 2014 / Sheet 52 of 62



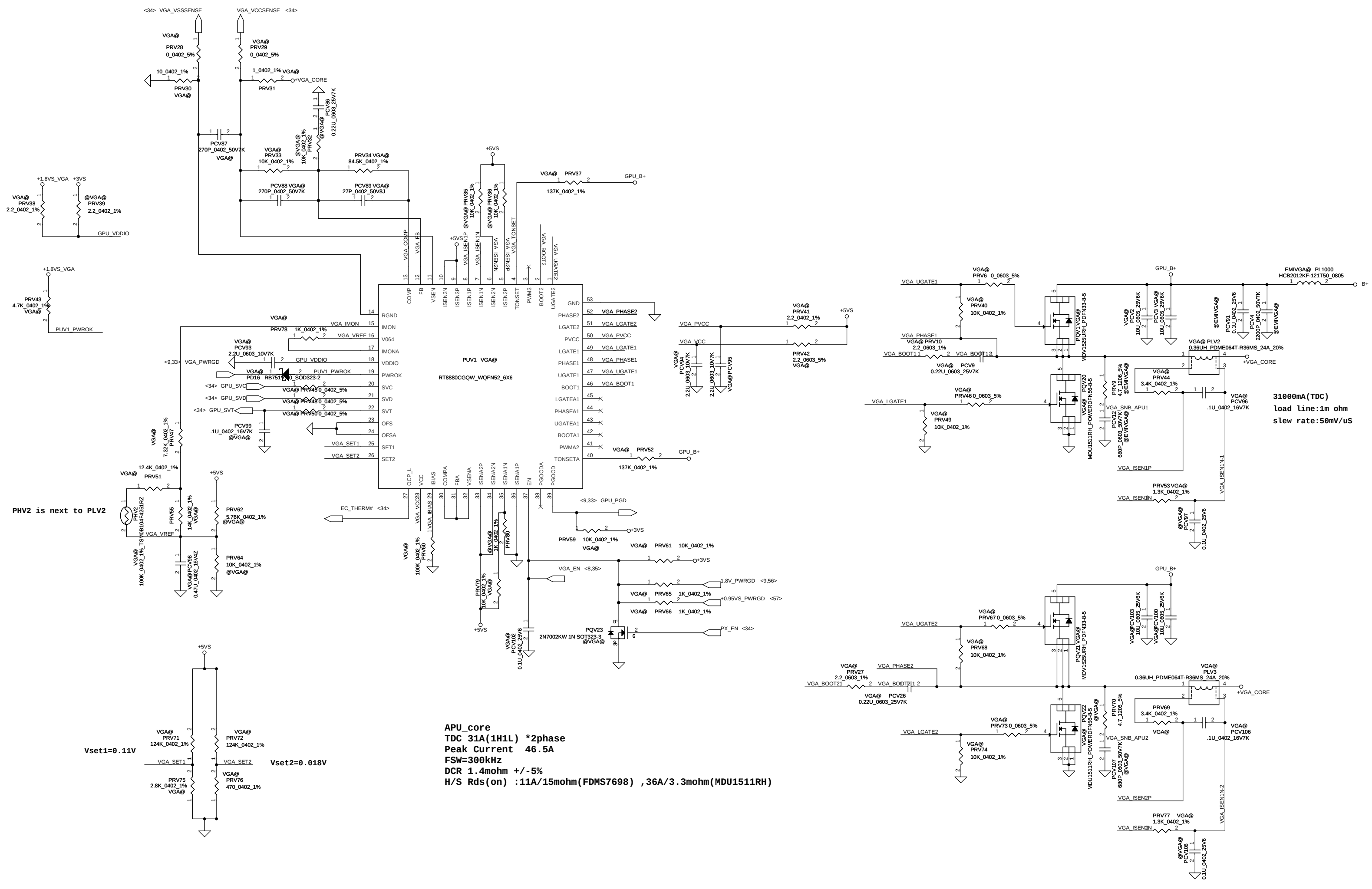
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *ADP_OCP*

Size | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



PHV2 is next to PLV2

Vset1=0.11V

Vset2=0.018V

APU_core
TDC 31A(1H1L) *2phase
Peak Current 46.5A
FSW=300kHz
DCR 1.4mohm +/-5%
H/S Rds(on) :11A/15mohm(FDMS7698) ,36A/3.3mohm(MDU1511RH)

31000mA(TDC)
load line:1m ohm
slew rate:50mV/uS

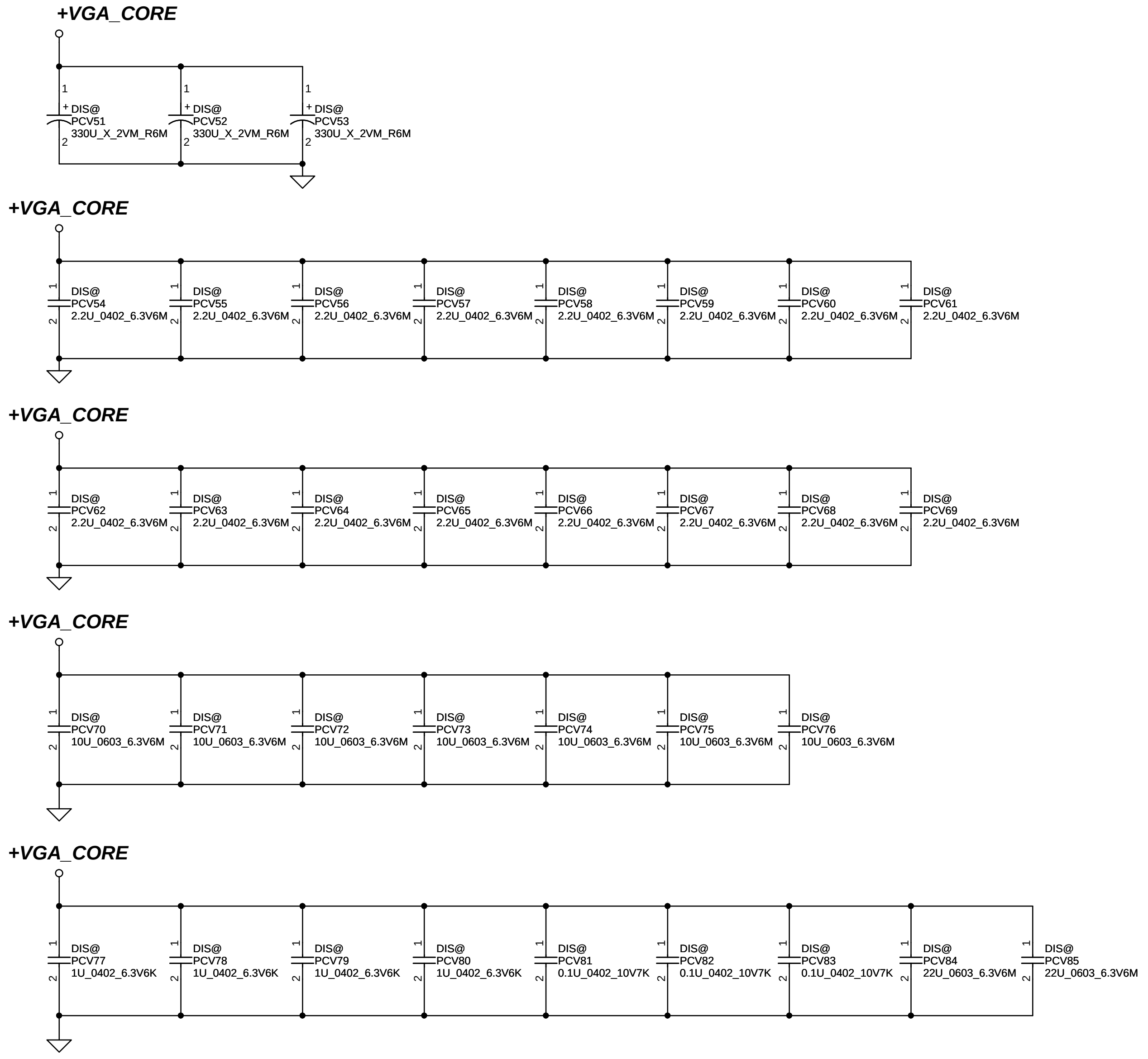
Security Classification	Compal Secret Data		
Issued Date	2013/03/19	Deciphered Date	2013/03/19

Compal Electronics, Inc.

Title: RT8880AGQW

Size / Document Number: LA-B181P — Rev 0.5

Date: Tuesday, March 25, 2014 — Sheet 54 of 62



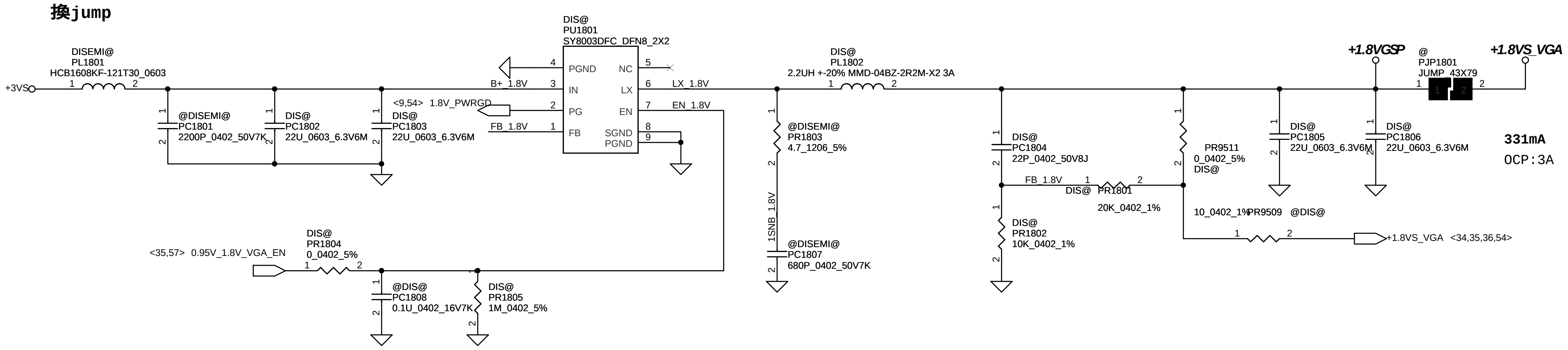
Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *VGA CHIP DECOUPLING*

Size | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 |



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

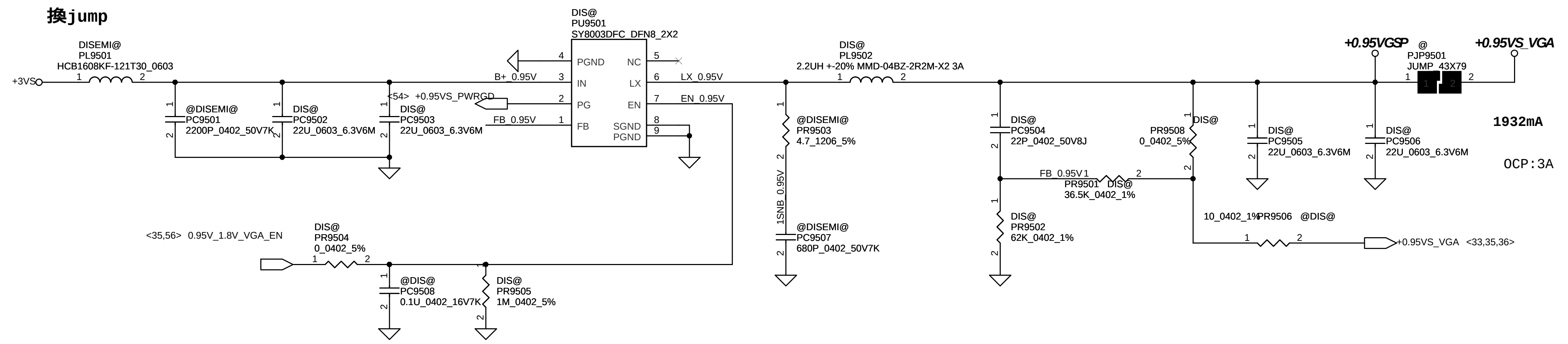
Compal Electronics, Inc.

Title: +1.8VS_VGA

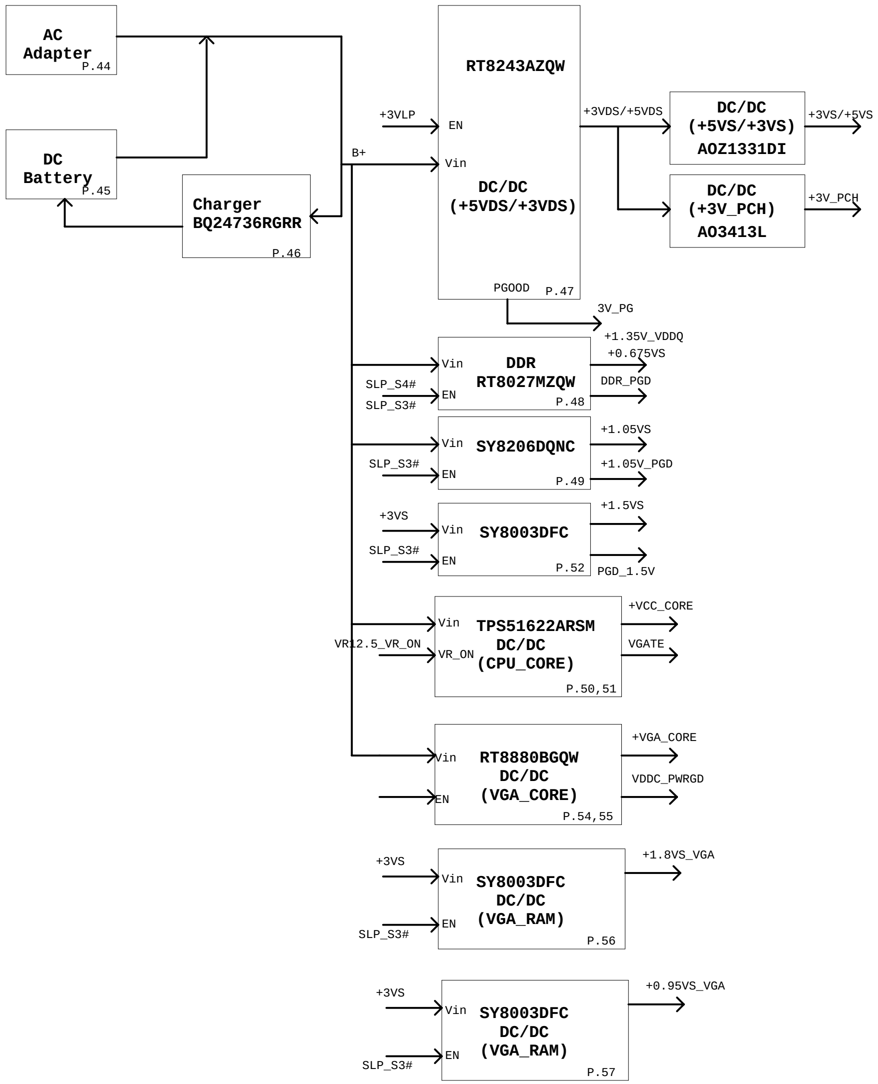
Size: B | Document Number: LA-B181P | Rev: 0.5

Date: |

换jump



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title: +0.95VS_VGA	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B, Document Number LA-B181P	Rev 0.5
				Date:	Sheet 57 of 62

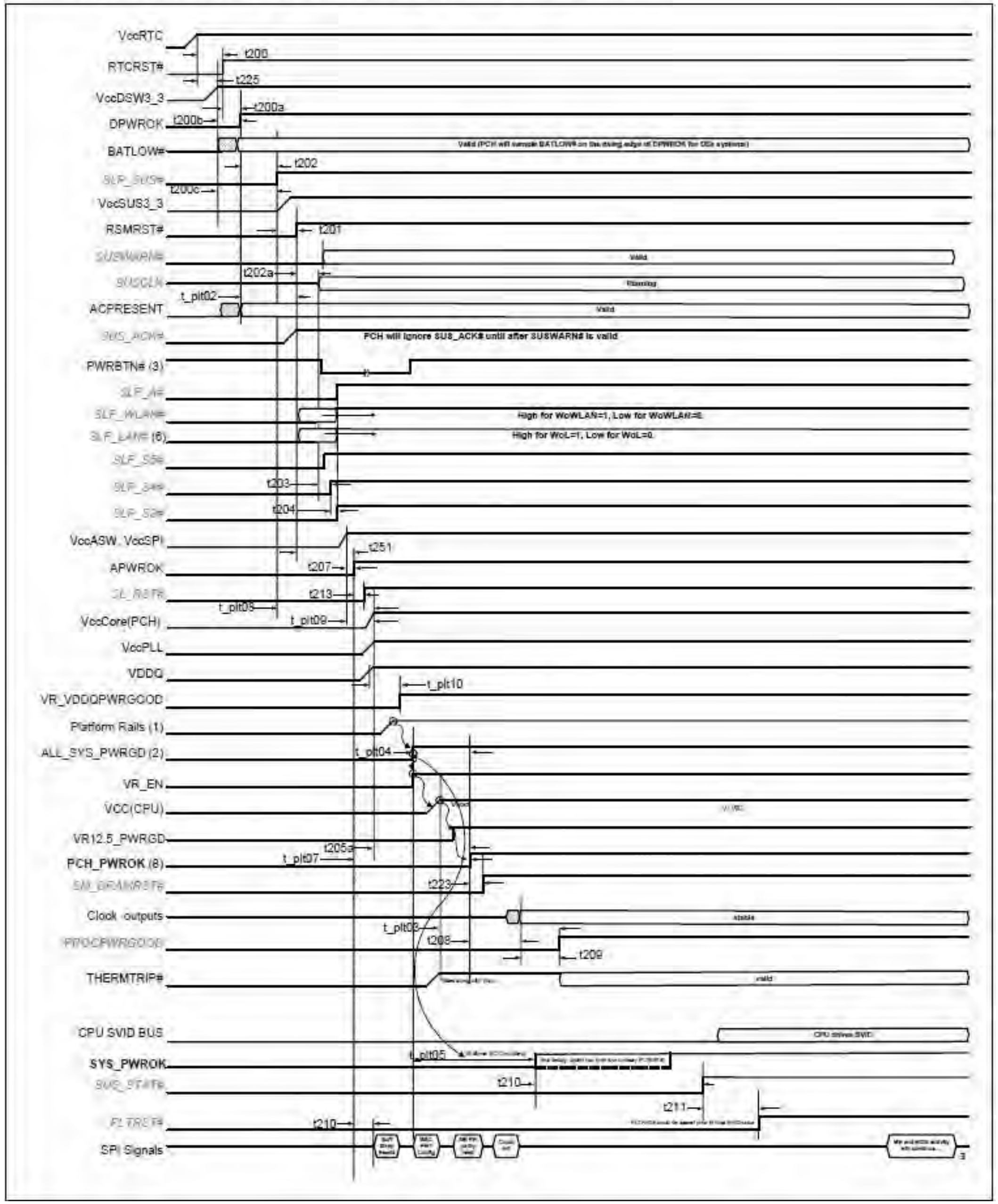


CPU DC/DC TPS51622ARSMR	50~51
INPUTS	OUTPUTS
B+	VCC_VORE
SYSTEM DC/DC RT8243AZQW	47
INPUTS	OUTPUTS
B+	3VDS/5VDS
SYSTEM DC/DC RT8207MZQW	48
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS
SYSTEM DC/DC SY8206DQNC	49
INPUTS	OUTPUTS
B+	1.05VS
SYSTEM DC/DC SY8003DFC	52
INPUTS	OUTPUTS
B+	1.5VS
SYSTEM DC/DC RT8880BGQW	54~55
INPUTS	OUTPUTS
B+	+VGA_CORE
SYSTEM DC/DC SY8003DFC	56
INPUTS	OUTPUTS
B+	+1.8VS_VGA
SYSTEM DC/DC SY8003DFC	57
INPUTS	OUTPUTS
B+	+0.95VS_VGA

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/04/03	Deciphered Date	2014/12/31	Title: Power Block Diagram
				Size / Document Number: LA-B181P / Rev 0.5
				Date: Tuesday, March 25, 2014 / Sheet 58 of 62

Power ON Sequence

Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: Power ON Sequence
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: C; Document Number: LA-B181P; Rev: 0.5
				Date: Tuesday, March 25, 2014; Sheet 59 of 62

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	20131030		Delete 1.PQ307 2.charger air line power circuit 3.change AON7506 to SI7716(PQ106) 4.change NDS0610 to LBSS84L 5.change AON7506 to SI7716 6.change 47U 6.3V to 22U 6.3V (PCH8,PCH9) 7.PR9512 mount	1.customer request 2.customer request 3.customer common part 4.compal change 5.customer common part 6.vender reveiw	DB0 DB0 DB0 DB0
2	20131031		1.10U_0805_25V==>2200p_0402_50V not mount(PC160) 2.PC107,PR111,PC121,PC305,PR314 PC313,PC308,PR315,PC312,PCH4,PCZ3,PRZ13,PCZ13 PCZ20,PCZ26,PCW1,PCV4,PRV70,PCV107 3.change 147K_0402_1% to 237K_0402_1% (PRV34) change 560P_0402_50V7K to 470P_0402_50V7 (PCV88) change 10.7K_0402_1% to 22.6K_0402_1%(PRV47) change 9.76K_0402_1% to 5.6K_0402_1%(PRV51) change 15K_0402_1% to 19.1K_0402_1%(PRV55) change 910K_0402_5% to 20.5K_0402_1%(PRV75) change 910k_0402_1% to 910_0402_1%(PRV53) change 3.48K_0402_1% to 3.4K_0402_1%(PRV69) change 910k_0402_1% to 910_0402_1%(PRV77) 4.remove PR9510,PR9512,PR9514,PR9513 5.remove PC318,PRH10,PRW10,PCW13 6. PRH8,PRW8 not mount 7.22u/0805 6.3V to 22u/0603 6.3V PC1504,PC1501 PC1505,PC1802,PC1803,PC1805,PC1806,PC9502,PC9503, PC9505,PC9506,PCH9,PCH10,PCH11,PCH8 8.0.22U_0402_6.3V6K to 0.22U_0603_50V7K (PC128)	1.EMI feedback 2.EMI feedback 3.power vender feedback 4.power change fb sense 5.for compal module design 6.current limit design	DB0 DB0 DB0 DB1 DB1 DB1 DB1 DB1 DB1 SI1 SI1 SI1
3	20131101		1.remove PRW11	1.HW request	
4	20131112		1.not mount PRW7 2.change 0_0402_1% to 0_0402_5%(PR1502,PR1804, PR9504,PR9508,PR9511,PR9515)	2.AMD request	
5	20131202		1.not mount PRZ36,PRV32 and PCV86 2.PC128 change 0.22U_0603_25V to 0.22U_0402_6.3V6K 3.add PD16,PRV43 4.add PRV45,PRV48,PCV99 and PRV50	1.PWR request 2.PWR request 3. customer request 4.richtek request	SI1 SI1 SI2
					SI2

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: **PIR List**

Size: B | Document Number: **LA-B181P** | Rev: 0.5

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
6	20131210		add PRV78 1K_0402_1% PRV62 5.76K_0402_1% PRV64 10K_0402_1% PRV80 1K_0402_1% PRV79 10K_0402_1% PRV52 137K_0402_1%	RITCHTEK issue request	DB0 DB0 DB0 DB0
	20131221		PRM2 Change 4.7_1206_5% to 0_1206_5% PCM7 Change 680P_0603_50V7K to 1000P_0603_50V7K PR314 not mount==>mount PC313 not mount==>mount PR315 not mount==>mount PC312 not mount==>mount PCZ13 not mount==>mount PRZ13 not mount==>mount PCZ20 not mount==>mount(28W) PRZ26 not mount==>mount(28W)	EMI request	DB0 DB0 DB0 DB1 DB1
	20131226		PRV31 Change 10_0402_1% to 1_0402_1% PRV34 Change 127K_0402_1% to 84.5K_0402_1% PRV47 Change 22.6K_0402_1% to 7.32K_0402_1% PRV51 Change 5.6K_0402_1% to 12.4K_0402_1% PRV55 Change 19.1K_0402_1% to 14K_0402_1% PRV75 Change 20.5K_0402_1% to 2.8K_0402_1% PRV77 Change 910_0402_1% to 1.3K_0402_1% PRV53 Change 910_0402_1% to 1.3K_0402_1% PC128 Change 0.22U_0603_6.3V to 0.22U_0402_6.3V	RITCHTEK issue request	DB1 DB1 DB1 DB1 SI1
	20140102		PRM2 Change 0_1206_5% to 4.7_1206_5% PCM7 Change 1000P_0603_50V7K to 680P_0603_50V7K PUV1 change RT8880BGQW to RT8880CGQW	EMI request RITCHTEK request	SI1 SI1
	20140103		PR14,PQ2 and PR13 are not mount. PR11 Change 330_0402_1% to 680_0402_1%	Customer request	
	20140106		PRV80 mount==>not mount PRV79 not mount==>mount	RITCHTEK issue request	
	20140213		add PC8,PC9 and PC10 mount PR111,PC121,PC107 and PC129 PC107 2200P_0402_50V7K==>0.022_0402 25V PC129 0.1U_0402_50V7K==>0.022_0402_25V	EMC request EMC request	
	20140214		add PC161 2200P_0402_50V7K not mount	EMC request	SI1 SI1 SI2 SI2

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date		Deciphered Date		Title: PIR List
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: B / Document Number: LA-B181P / Rev: 0.5
				Date: Tuesday, March 25, 2014 / Sheet 61 of 62

ZPL40/50/70 from DB to DB-R LA-B181P REV:0.1 -> 0.2 Modify <2013.11.28.~ 2013.12.03>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	11/28	CKT, LAYOUT	6	-Design issue	-Change RC222 pin 1 connection from +3VS to +5VS
0.2	2	11/28	CKT, LAYOUT	7	-Follow CHICLET	-Move TPM LPC CLK from port 0 to port 1
0.2	3	11/28	CKT	8	-DGPU_PWR_EN voltage level uncorrect issue	-Uninstall RC125
0.2	4	11/28	CKT, LAYOUT	9	-DGPU power on sequence	-Change RC121 to 100K and add CC127 to timing delay.
0.2	5	11/28	CKT, LAYOUT	18	-Footprint uncorrect issue	-Modify UT6 footprint to SC70-5
0.2	6	11/28	CKT, LAYOUT	21	-No used.	-Remove CLK_PCI_DEBUG from JMINI1 pin 19
0.2	7	11/28	CKT	23	-Q35 can't turn on issue	-Uninstall RL26
0.2	8	11/28	CKT	30	-Follow HP BIOS code request	-Uninstall R124
0.2	9	11/28	CKT, LAYOUT	32	-Aviod leakage issue.	-Swap Q88 pin 1 and pin 3
0.2	10	11/28	CKT, LAYOUT	32	-Footprint uncorrect issue	-Modify C187 footprint to 0402 package
0.2	11	11/28	CKT, LAYOUT	33	-Design issue	-Swap GPU PEG RX bus P/N signal and CV1~CV8 change to 0.22u
0.2	12	11/29	CKT, LAYOUT	28	-Current limit	-Add R660
0.2	13	11/29	CKT, LAYOUT	30	-Vendor request	-U13 pin 6 add external 4.7K PU to +3VS_TPM
0.2	14	11/29	CKT	32	-Follow CHICLET	-Change R255, R257, and R493 to 10Kohm
						-Delete QC12 and add buffer U20 and U21.
0.2	15	12/02	CKT, LAYOUT	6	-Follow CHICLET	QC8.3 net name from HDA_SDOUT_AUDIO change to HDA_SDOUT
0.2	16	12/02	CKT, LAYOUT	32	-Follow CHICLET	add R101, R102, R104, R105, R106
0.2	17	12/02	CKT, LAYOUT	23	-leakage issue and FAR suggest	1.swap QL2 pin 1 and pin 3 2.Install RL40 3.Reserve 2 resistor (RL48, RL49) connection QL2.2 to +3VS and +LAN_VDD_3V3.
0.2	18	12/02	CKT, LAYOUT	34	-Follow 2013 RRR	-Add D14
0.2	19	12/02	CKT	35	-DGPU power on sequence	-Uninstall R5076, R5074
0.2	20	12/03	CKT, LAYOUT	40	-Follow CHICLET	-change +1.05VS_MODPHY switch circuit

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.2 -> 0.3 Modify <2013.12.04~ 2013.12.17>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	1	12/04	CKT, LAYOUT	29	-Follow 2013 RRR	-update FAN control circuit delete Q4108, R5080 and add U2, C31
0.3	2	12/05	CKT	35	-DGPU power on sequence	-C4816 from 0.01u change to 0.022u
0.3	3	12/05	CKT	9	-DGPU power on sequence	-Change RC121 to 0ohm and uninstall CC127 (BIOS code control timing)
0.3	4	12/05	CKT	10, 33	-For PCIe Gen2	-change CC89, CC90, CC91, CC92, CC93, CC94, CC95, CC96, CV1, CV2, CV3, CV4, CV5, CV6, CV7, CV8 from 0.22u to 0.1u
0.3	5	12/06	CKT	12	-Follow CHICLET	-Change RC174 from 5.11ohm to 0ohm
0.3	6	12/06	CKT	11	-Follow INTEL schematic	-Change RC156 from 110ohm to 130ohm install
0.3	7	12/06	CKT, LAYOUT	29	-Platform ID identify	-add R82, R86
0.3	8	12/06	CKT, LAYOUT	32		-reserve R136, R137 co-lay with U20, U21
0.3	9	12/06	CKT, LAYOUT	40		-reserve R135 co-lay with Q185
0.3	10	12/09	CKT, LAYOUT	43	-No leakage issue	-remove Q57
0.3	11	12/09	CKT	26	-Follow CHICLET	-RA36 from 22ohm change to 33ohm
0.3	12	12/09	CKT, LAYOUT	17	-Follow INTEL schematic	-Install CD52, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.3	13	12/09	CKT, LAYOUT	11	-Follow INTEL schematic	-Re-placement RC154
0.3	14	12/09	CKT, LAYOUT	12	-Follow INTEL schematic	-Add RC183, CC47, RC189, CC75
0.3	15	12/10	CKT, LAYOUT	10	-For WWAN , Touch share USB port	-Add R138, R139
0.3	16	12/10	CKT, LAYOUT	4	-Follow CHICLET	-Add C32
0.3	17	12/11	CKT, LAYOUT	8	-Follow INTEL schematic	-reserve RC330
0.3	18	12/11	CKT, LAYOUT	21	-solve SIM card cann't detect issue	-delete R5079 , Q4107 and add C2
0.3	19	12/13	CKT, LAYOUT	9	-Follow Runt	-R103 change to test point T184
0.3	20	12/13	CKT	8	-solve DGPU power issue	-Install RC125
0.3	21	12/13	CKT, LAYOUT	21	-Follow Runt	-Q90 , Q4113 from two single MOS change to daul MOS (Q90)
0.3	22	12/13	CKT, LAYOUT	22	-ODD power issue	-Add Q63
0.3	23	12/13	CKT, LAYOUT	23	-LAN power issue	-delete JHW1 , RL26
0.3	24	12/13	CKT, LAYOUT	21	-no need	-delete R205 , C292
0.3	25	12/13	CKT	25	-For V drop test	-C1572 from 100u change to 150u
0.3	26	12/13	CKT, LAYOUT	9	-Hp request	-ODD_DA# form GPIO14 change to GPIO3
0.3	27	12/13	CKT, LAYOUT	21	-For GPIO initial status	-add R91
0.3	28	12/14	CKT, LAYOUT	12	-solve power ripple	-add CC77 , CC78 , CC79
0.3	29	12/16	CKT, LAYOUT	9	-reserve for MPHY sequence	-add RC377

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.3 -> 0.4 Modify <2013.12.18~ 2013.12.25>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.4	1	12/20	CKT	9	-Follow HP request	-Install RC272, RC273
0.4	2	12/20	CKT, LAYOUT	15	-Follow Intel PDG	-Remove RD26, Install RD21
0.4	3	12/20	CKT, LAYOUT	16	-Follow Intel PDG	-Unnstall CD52, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.4	4	12/20	CKT, LAYOUT	19	-Follow Vendor request	-Reserve RG5
0.4	5	12/20	CKT	19	-Follow HP request	-Change R82, R86 to 0 ohm
0.4	6	12/20	CKT	20	-Follow Intel PDG	-Change RP3 and RP4 to 470 ohm
0.4	7	12/20	CKT	21	-Compal Request	-Install R91
0.4	8	12/20	CKT, LAYOUT	22	-Customer modify GPIO table.	-Remove Q84, R954. Change JODD1 pin 11 netname to ODD_DA#
0.4	9	12/20	CKT	23	-Prepare leakage issue when S3, S5	-Uninstall RL40, QL2, RL49, RL48 install RL34
0.4	10	12/20	CKT	24	-Vendor Request	-Reserve RA40, U4101 pin 37 add RT57 10K PU to +5VS
0.4	11	12/20	CKT	31	-Vendor Request	-Remove R1363, R1365, R1367, C421, C423, C414, L31, L32, L34, R1364, R1366, and R1368. Modify CRT pi filter
0.4	12	12/20	CKT, LAYOUT	40	-Follow Compal common design	-Modify MPHY Power circuit
0.4	13	12/23	CKT, LAYOUT	30	-Follow RF team request	-Install C80, C556, C81, C558 -Reserve C90, C564, C91, C565, C92, C566, C93, C567, C95, C569, C110, C578, C111, C579, C108, C576, C82, C559, C83, C560, C84, C561, C86, C562, C89, C563, C94, C568, C96, C571, C112, C580, C109, C577, C106, C574, C97, C572, C105, C573, C130, C581, C131, C582, C132, C583, C133, C584, C134, C585, C135, C586, C136, C587, C137, C588, C138, C589
0.4	14	12/24	CKT, LAYOUT		-Follow ESD team request	-Install C113, C127 -Reserve C114, C115, C116, C121, C123, C124, C128, C129

ZPL40/50/70 from SI to PV-1 LA-B181P REV:0.3 -> 0.4 Modify <2014.02.05~2014.>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.5	1	02/05	CKT	21	-Double pull hugh	-RN3 change to @
0.5	2	02/05	CKT	18, 19	-For LVDS SKU	-R163, RG3 change to LVDS@
0.5	3	02/05	CKT	19	-For eDP SKU	-R172 change to eDP@
0.5	4	02/05	CKT	19	-For Lid Switch issue	-R166, R175 change to 3.3K
0.5	5	02/05	CKT, LAYOUT	22	-For ODD issue	-add R448, reserve C151
0.5	6	02/05	CKT, LAYOUT			-1. QA2, QA3 combine to dual mos QA2A, QA2B 2. Q91, Q182 combine to dual mos Q91A, Q91B 3. Q86, Q87 combine to dual mos Q86A, Q86B 4. Q63 change to Q63A, Q63B 5. Q4112, Q4114 combine to dual mos Q4112A, Q4112B
0.5	7	02/10	CKT, LAYOUT	35	-For GPU Power Sequence	-add D15 and move R5075, C4819
0.5	8	02/10	CKT, LAYOUT	28	-Follow ESD team request	-add C594, C595, C596
0.5	9	02/10	LAYOUT	31		-Move U4101 circuit close to JCRT
0.5	10	02/11	CKT, LAYOUT	40	-SLG59M1470VTR is single source issue	-modify U44 circuit
0.5	11	02/12	CKT	33	-Improve VGA_PWRGD signal quality	-R5094 from 8.25K change to 0ohm
0.5	12	02/13	CKT, LAYOUT	11, 19	-Follow RF team request	-add C139, C140, C421
0.5	13	02/14	CKT, LAYOUT		-Follow HP request	-1. FPR_OFF from GPIO11 change to GPIO65 2. change JAUDIO1.16 from +3V_PCH to +3VS 3. disconnect EC pin125 and CPU pinAJ5 rename EC pin125 "PCH_PCIE_WAKE#" to "EC_GPIO25" and add R249 pull up to +3VDS 4. RN13 un-install 5. connector EC pin103 to JMINI1 pin1 (WLAN_WAKE#), JMINI2 pin15 change to NC 6. connector EC pin105 to CPU pinAJ5 (PCH_PCIE_WAKE#) 7. change RN3 pull up power rail from +3VS_WLAN to +3VDS and install RN3 8. add JP4102 between +3VDS and +3V_WWAN