Jedi 15"/17" Schematics
Comet Lake - U/2GB VRAM

2019-06-06

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	*Cover Page*	
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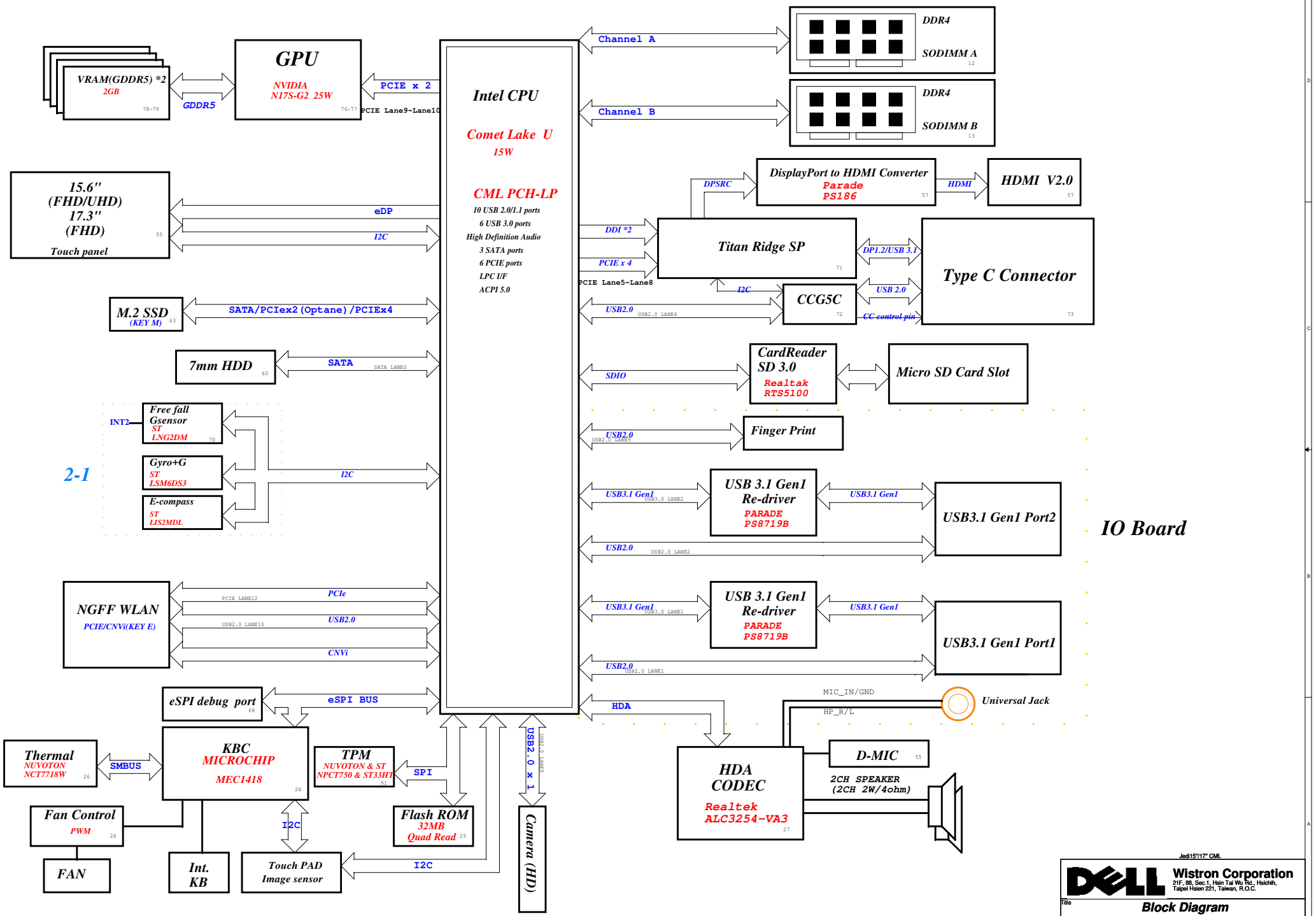
Jedi 15"/17" CPU 15W + GPU 25W Block Diagram

Project code: 4PD0HC010001
PCB P/N: 18806
Revision: A00



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Title: Block Diagram

Size	Document Number	Rev
C	Jedi15"/17" CML	A00

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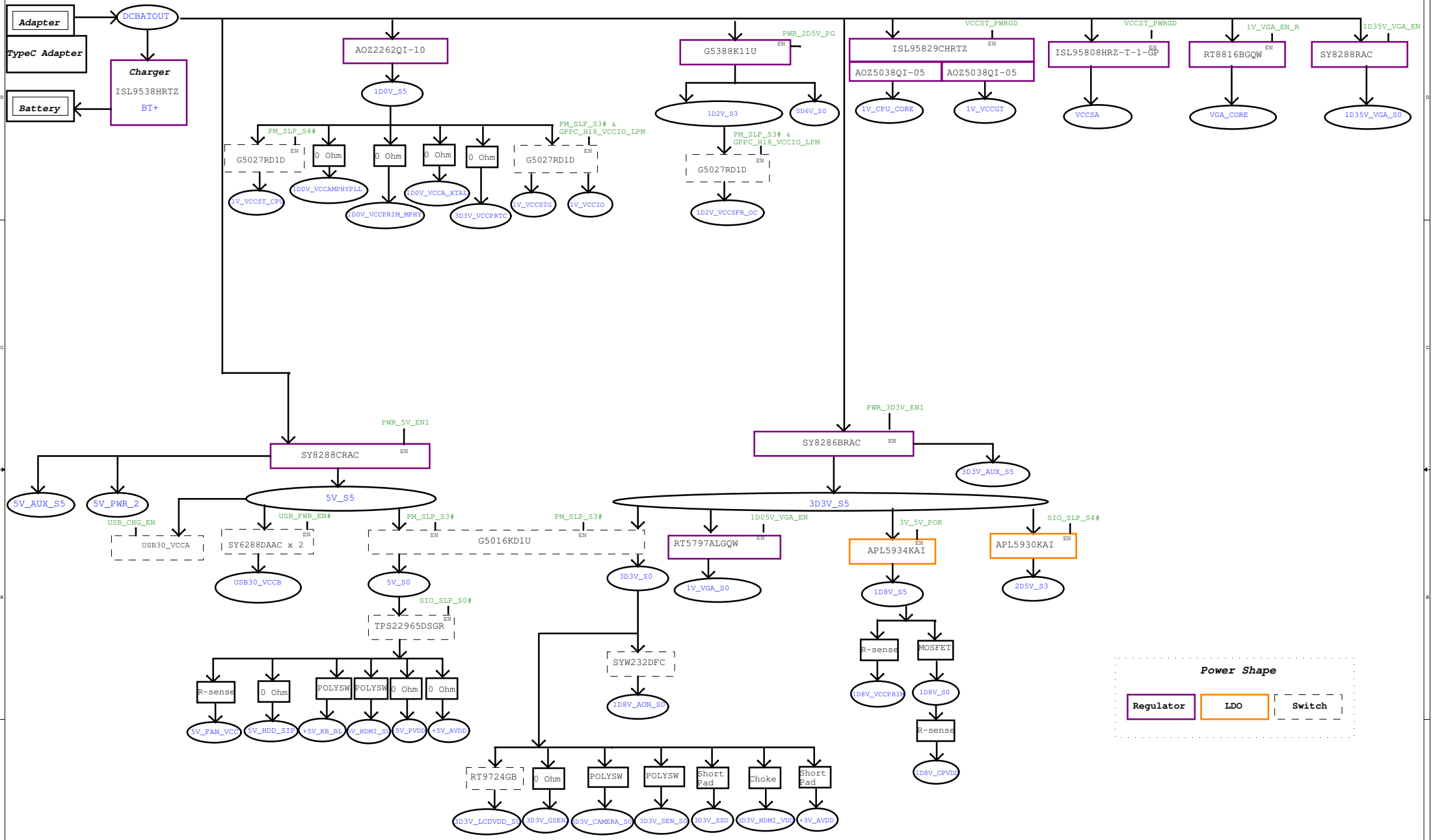

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Title: Power Block Diagram

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A2	Jedi15"/17" CML	A00

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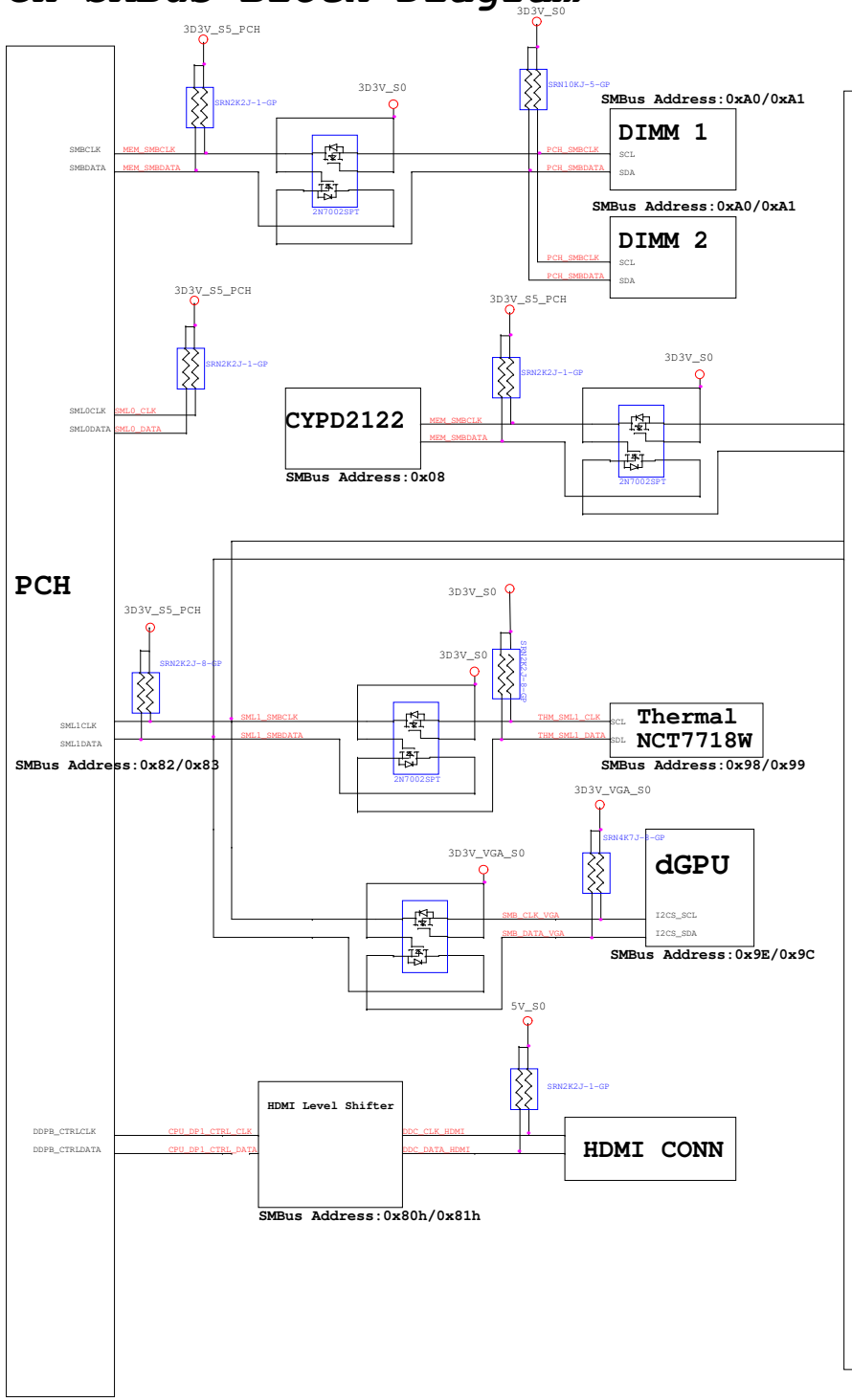
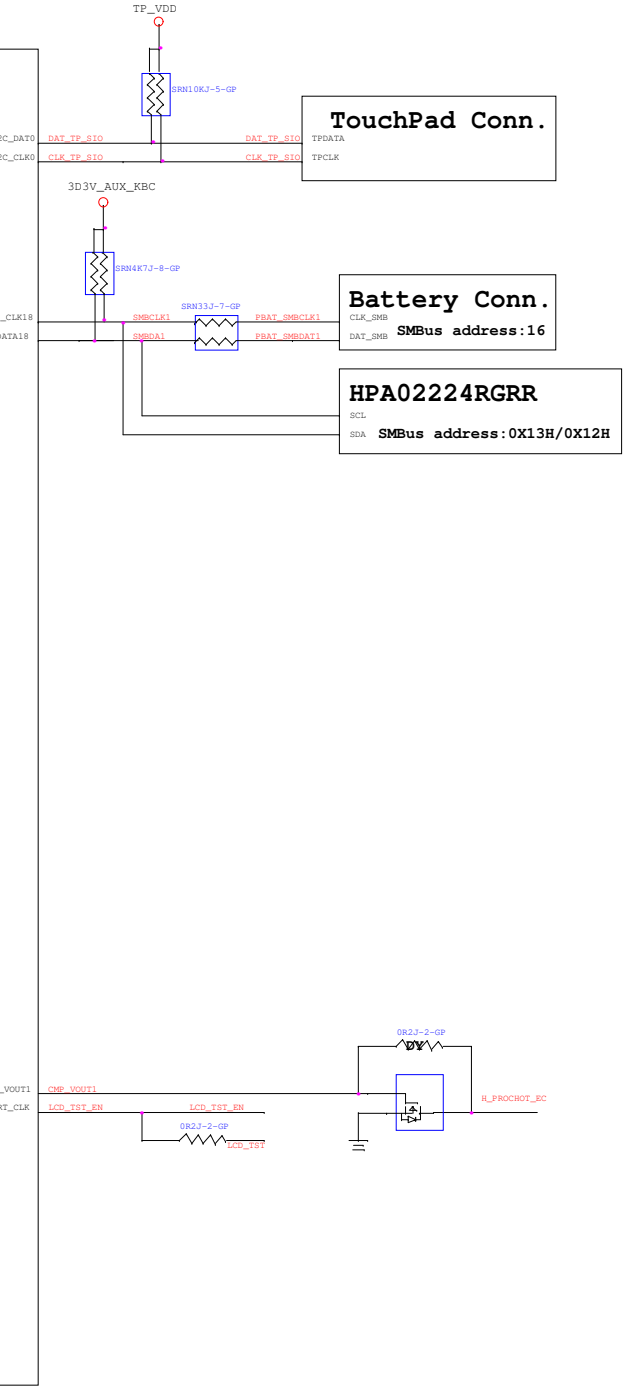
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

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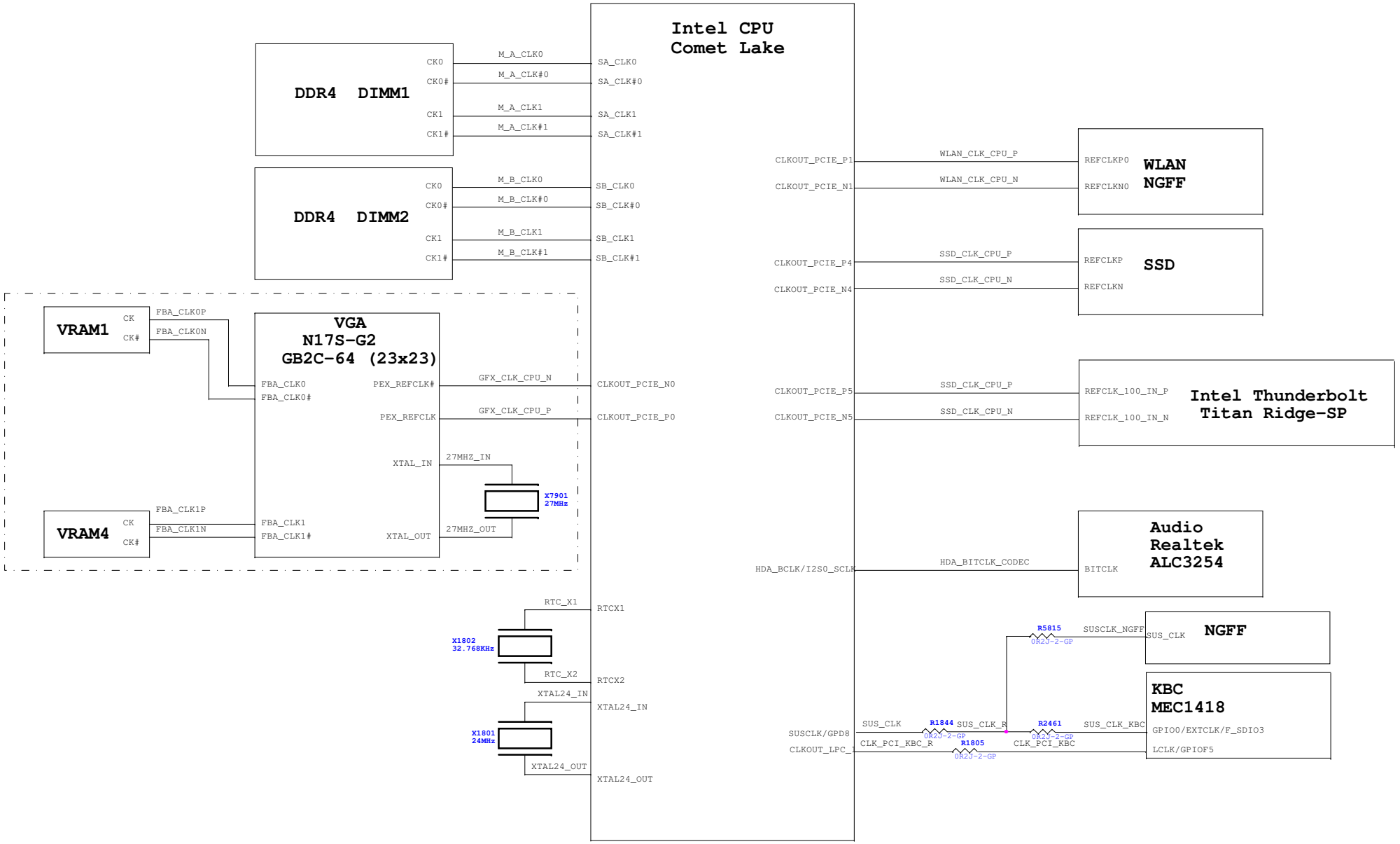
CLK Block Diagram



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Title	CLK Block Diagram	
Size: A2	Document Number: Jedi15"/17" CML	Rev: X01
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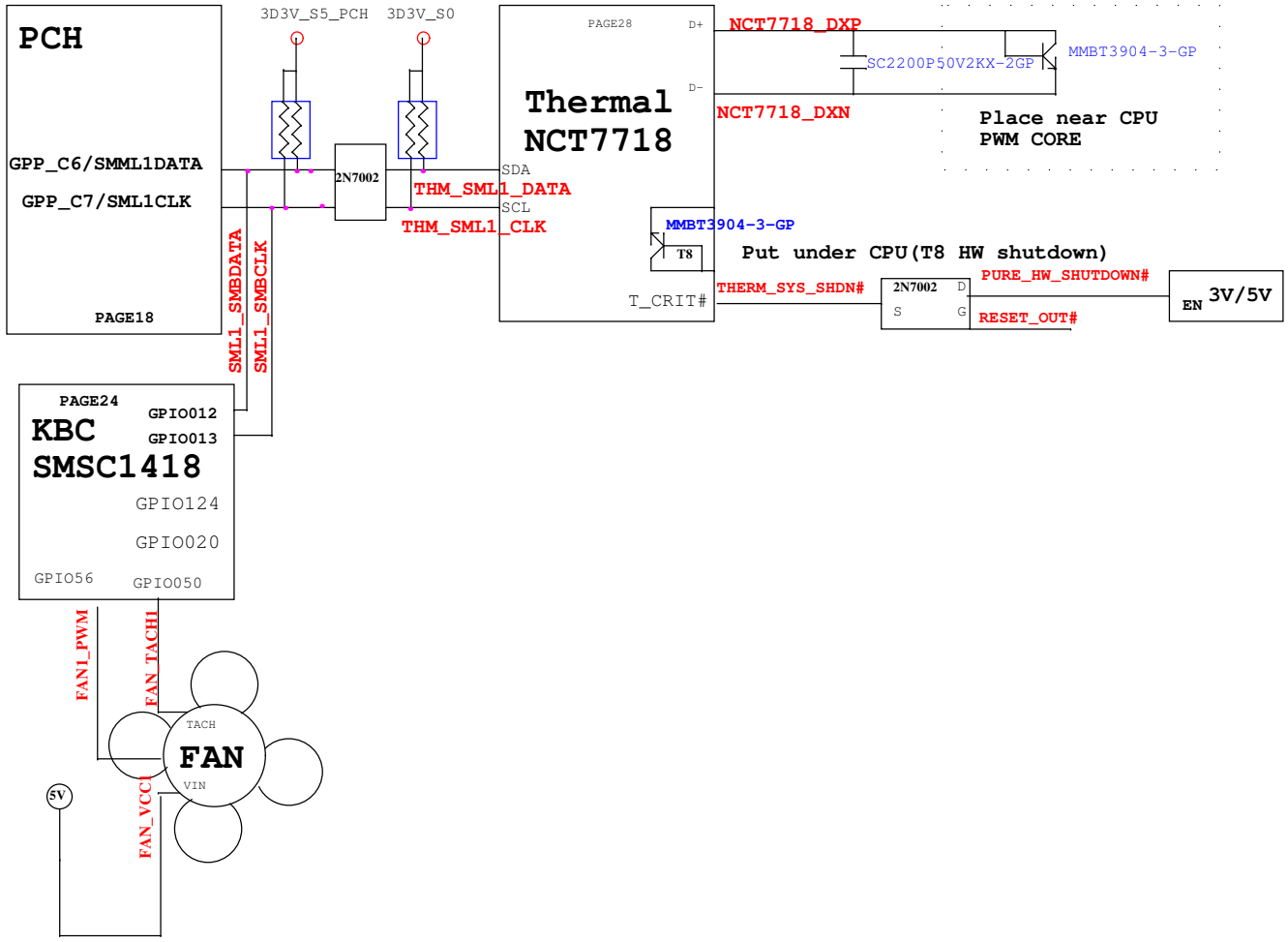
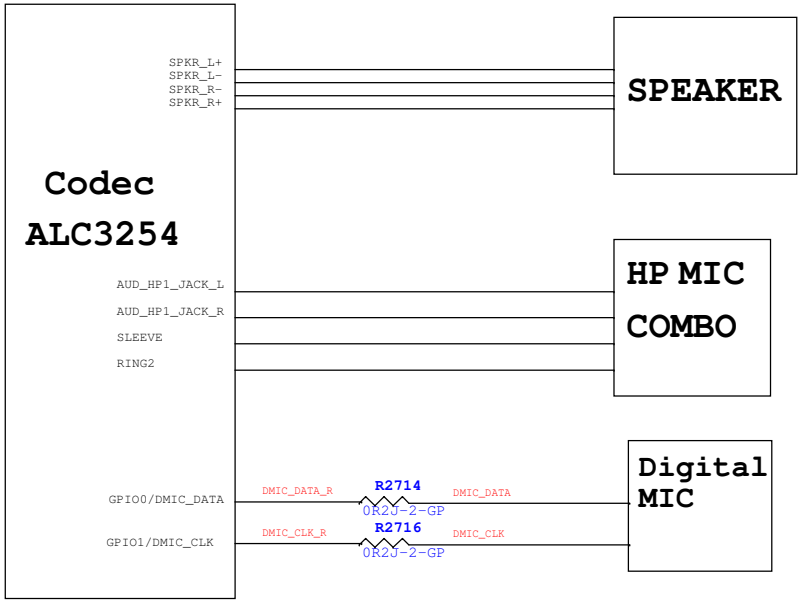
Thermal Block Diagram



Audio Block Diagram



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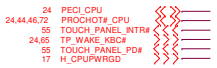
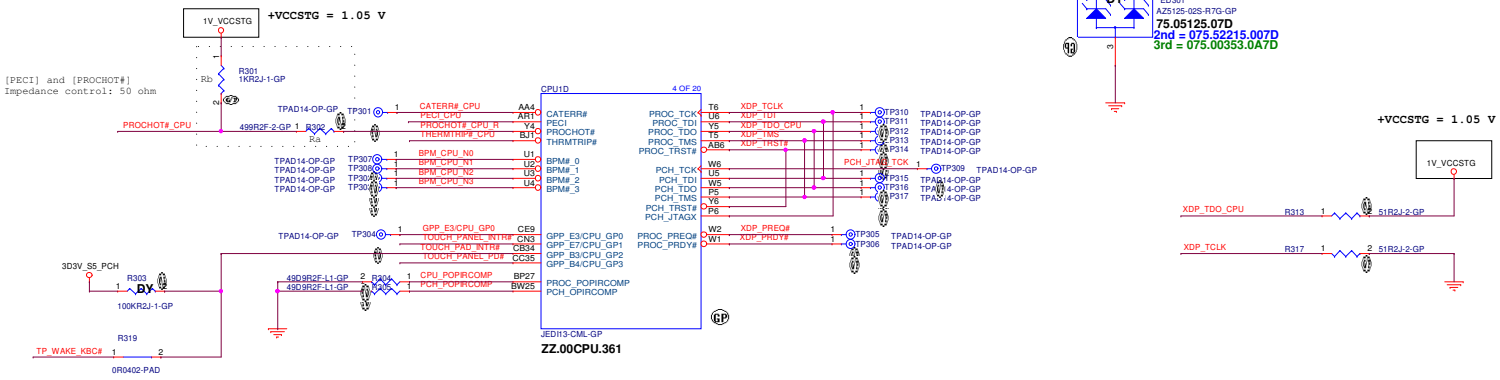
Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Jedi15"/17" CML | Rev: X01

Date: Monday, June 10, 2019 | Sheet 105 of 106

Main Func = CPU





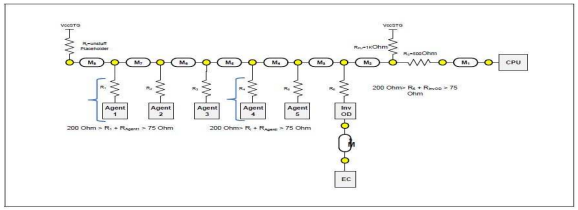


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

Main Func = CPU

DP to TR

71 DP1_DDI_TX_N0
71 DP1_DDI_TX_P0
71 DP1_DDI_TX_N1
71 DP1_DDI_TX_P1
71 DP1_DDI_TX_N2
71 DP1_DDI_TX_P2
71 DP1_DDI_TX_N3
71 DP1_DDI_TX_P3
71 DP1_AUX_CPU_N
71 DP1_AUX_CPU_P
71 DP1_HPD_CPU

71 DP2_DDI_TX_N0
71 DP2_DDI_TX_P0
71 DP2_DDI_TX_N1
71 DP2_DDI_TX_P1
71 DP2_DDI_TX_N2
71 DP2_DDI_TX_P2
71 DP2_DDI_TX_N3
71 DP2_DDI_TX_P3
71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU
71 DP2_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

24 GC6_THM_DIS#

20 IR_CAM_DET#

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

3D3V_S0
RN401 SRN2K2J-5-GP
CPU_DP1_CTRL_CLK
CPU_DP1_CTRL_DATA

3D3V_S0
SRN2K2J-5-GP RN402
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK

eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Port 1

Port 2

DP to TBT

CPU1A 1 OF 20

DP1_DDI_TX_N0 AL5 DDI1_TXN_0
DP1_DDI_TX_P0 AL6 DDI1_TXP_0
DP1_DDI_TX_N1 AJ6 DDI1_TXN_1
DP1_DDI_TX_P1 AJ5 DDI1_TXP_1
DP1_DDI_TX_N2 AF6 DDI1_TXN_2
DP1_DDI_TX_P2 AF5 DDI1_TXP_2
DP1_DDI_TX_N3 AE5 DDI1_TXN_3
DP1_DDI_TX_P3 AE6 DDI1_TXP_3

DP2_DDI_TX_N0 AC4 DDI2_TXN_0
DP2_DDI_TX_P0 AC3 DDI2_TXP_0
DP2_DDI_TX_N1 AC1 DDI2_TXN_1
DP2_DDI_TX_P1 AC2 DDI2_TXP_1
DP2_DDI_TX_N2 AE4 DDI2_TXN_2
DP2_DDI_TX_P2 AE3 DDI2_TXP_2
DP2_DDI_TX_N3 AE1 DDI2_TXN_3
DP2_DDI_TX_P3 AE2 DDI2_TXP_3

EDP_TXN_0 AG4 eDP_TX_CPU_N0
EDP_TXP_0 AG3 eDP_TX_CPU_P0
EDP_TXN_1 AG2 eDP_TX_CPU_N1
EDP_TXP_1 AG1 eDP_TX_CPU_P1
EDP_TXN_2 AJ4 eDP_TX_CPU_N2
EDP_TXP_2 AJ3 eDP_TX_CPU_P2
EDP_TXN_3 AJ2 eDP_TX_CPU_N3
EDP_TXP_3 AJ1 eDP_TX_CPU_P3

EDP_AUX_N AH4 eDP_AUX_CPU_N
EDP_AUX_P AH3 eDP_AUX_CPU_P

DISP_UTILS AM7

DDI1_AUX_N AC7 DP1_AUX_CPU_N
DDI1_AUX_P AC6 DP1_AUX_CPU_P
DDI2_AUX_N AD4 DP2_AUX_CPU_N
DDI2_AUX_P AD3 DP2_AUX_CPU_P
DDI3_AUX_N AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 DP1_HPD_CPU_R
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP2_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 SIO_EXT_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 IR_CAM_DET#
GPP_E17/EDP_HPD/DISP_MISC4 CM7 EDP_HPD_CPU

EDP_BKLTEN CK11 L_BKLT_EN
EDP_VDDEN CG11 EDP_VDD_EN
EDP_BKLTCTL CH11 L_BKLT_CTRL

JEDI13-CML-GP

For TBT

1V_VCCIO
CHECK WHL design guide: DISP_RCOMP
RCOMP SHOULD BE VSS REFERNCE AND SHIELDED
R401 24D9R2F-L-GP
eDP_RCOMP_CPU AM6 DISP_RCOMP

CPU_DP1_CTRL_CLK CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
CPU_DP1_CTRL_DATA CC9 GPP_E19/DPPB_CTRLDATA
CPU_DP2_CTRL_CLK CH4 GPP_E20/DPPC_CTRLCLK
CPU_DP2_CTRL_DATA CH3 GPP_E21/DPPC_CTRLDATA

TPAD14-OP-GP TP402 GPP_E23 CP4 CN4 GPP_E22/DPPD_CTRLCLK GPP_E23/DPPD_CTRLDATA

GC6_THM_DIS# CR26
GPP_H17_STRAP CP26 GPP_H16/DDPF_CTRLCLK GPP_H17/DDPF_CTRLDATA

ZZ.00CPU.361

3D3V_S0
SIO_EXT_SMI# R402 10KR2J-3-GP

3D3V_S5_PCH
R407 10KR2J-3-GP
R408 10KR2J-3-GP
CPU_DP2_HPD_P
Q402 2N7002KDW-1-GP
DP2_HPD_CPU_R
DP2_HPD_CPU
R410 100KR2J-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

3D3V_S5_PCH
R405 10KR2J-3-GP
R406 10KR2J-3-GP
CPU_DP1_HPD_P
Q401 2N7002KDW-1-GP
DP1_HPD_CPU_R
DP1_HPD_CPU
R403 100KR2J-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

Jedi15"/17" CML

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Title: CPU (DDI/EDP)

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

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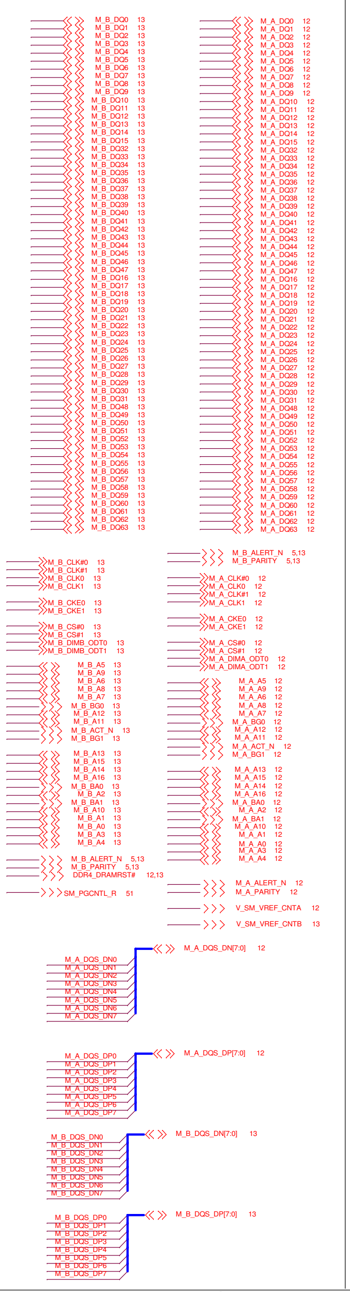
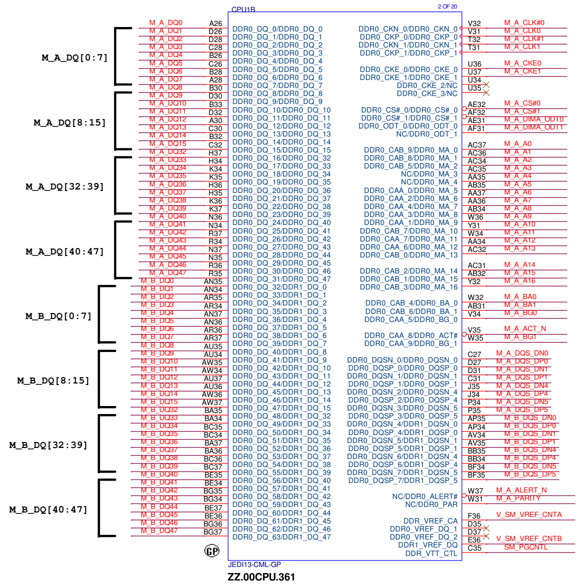
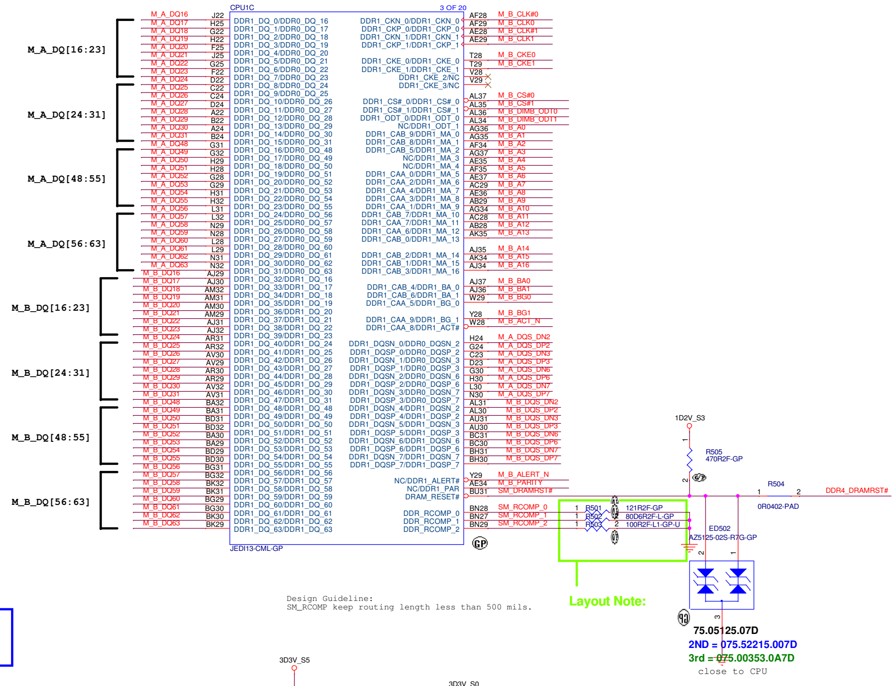
Main Func = CPU

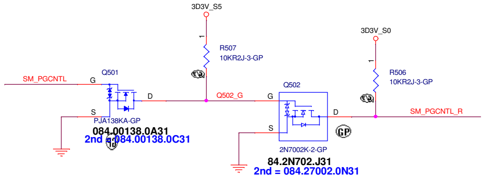
DDR4 ball type: NON-Interleaved Type







DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



PDG: DDR/ODT

4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

Note:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

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Title	CPU (DDR)	
Size: Custom	Document Number: Jedi15"/17" CML	Rev: X01
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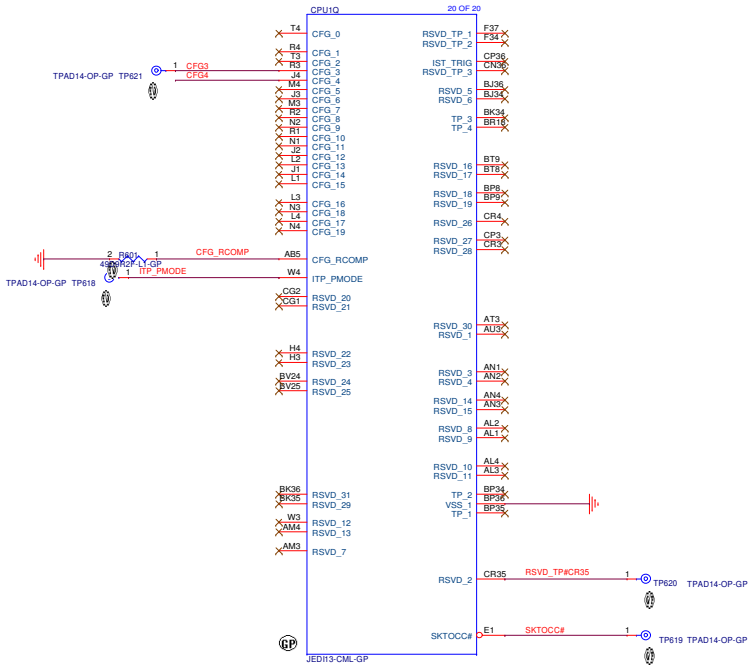
Main Func = CPU

15 CFG3
15 CFG4



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Title: CPU (CFG/IST)

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

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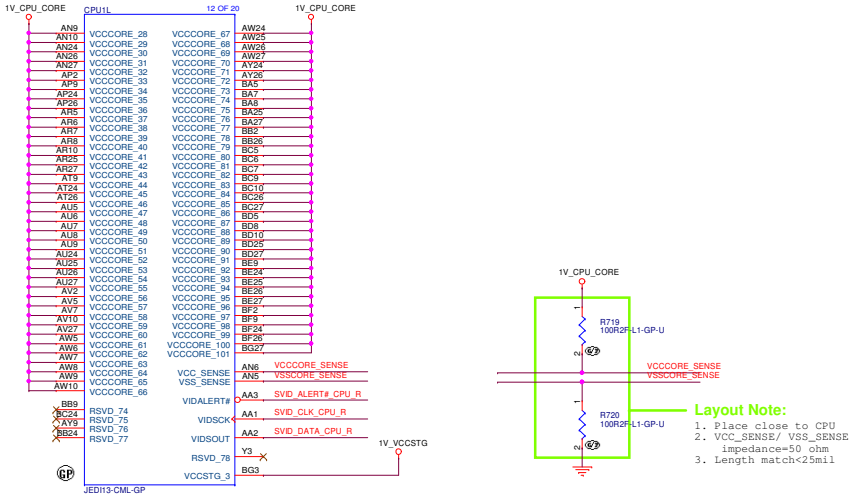
Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU



Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

SVID DATA

SVID CLOCK

SVID ALERT

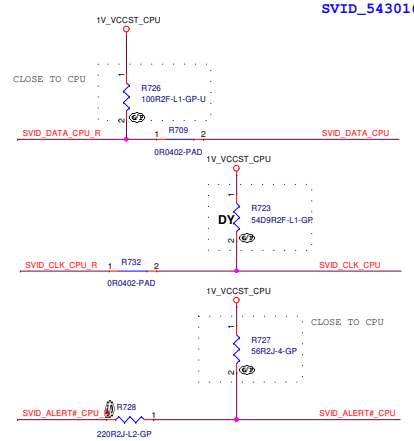


Figure 7-19. Routing Illustration for SVID Topology

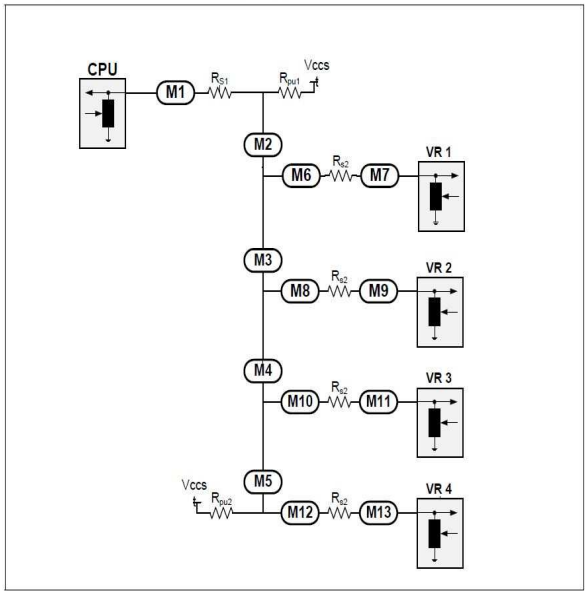
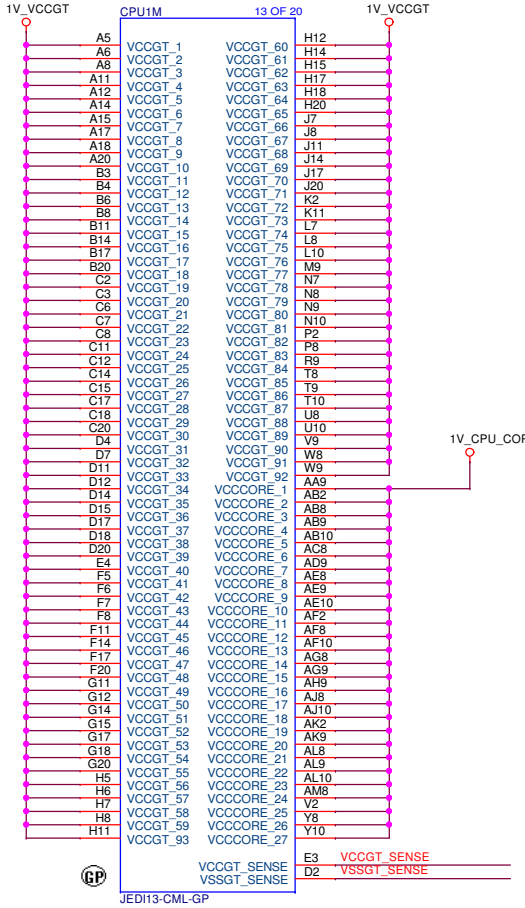


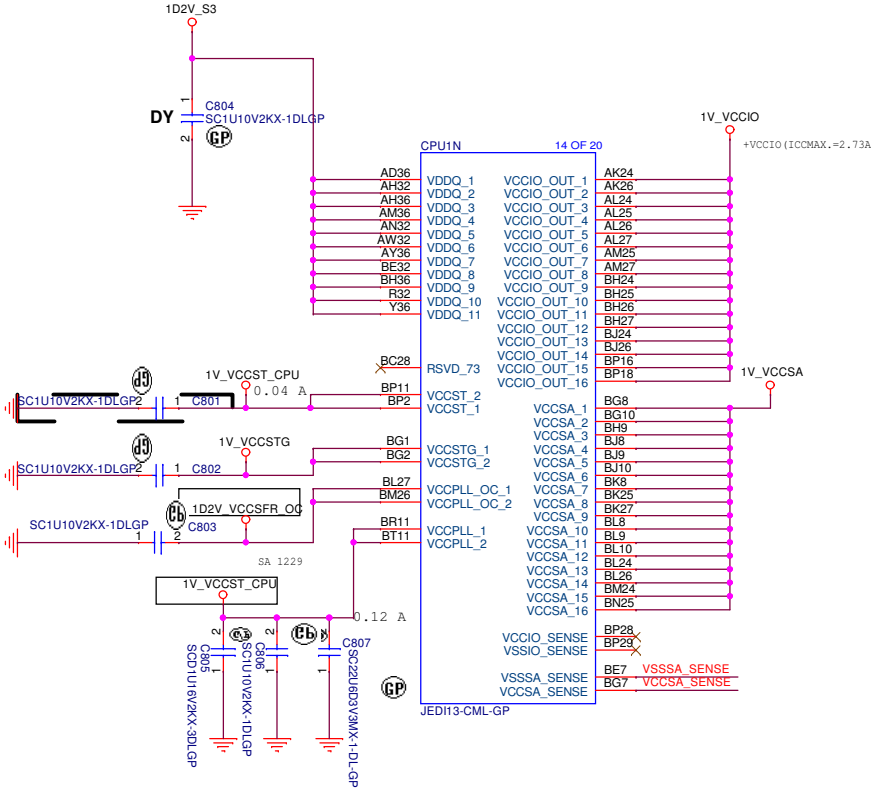
Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

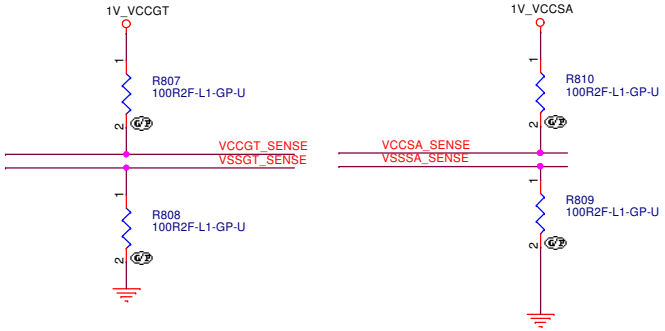
Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

Main Func = CPU

46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE







Jedi15"/17" CML

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Title: CPU (VCCGT/VCCIO/VDDQ/VCCSA)

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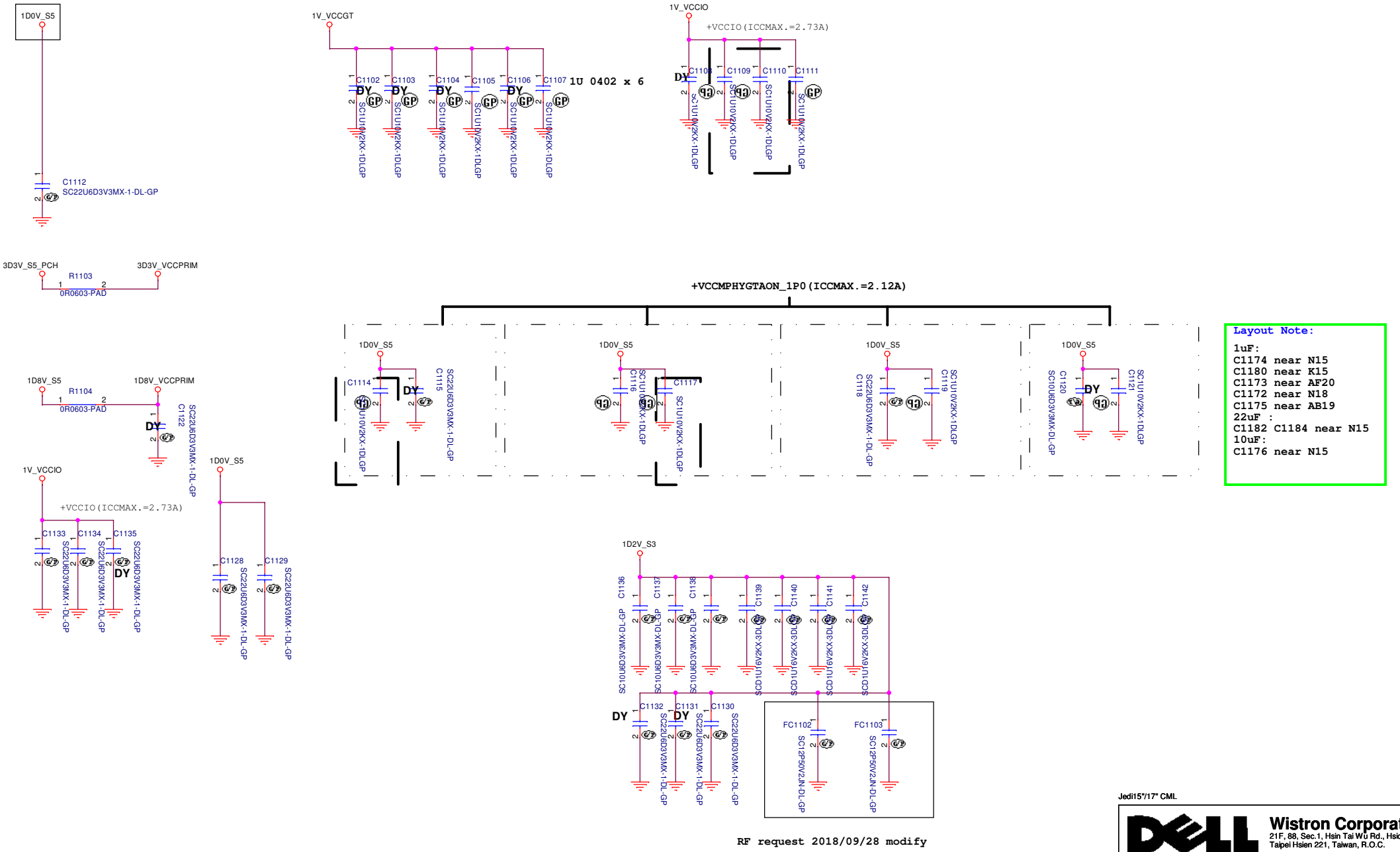
Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

RF request 2018/09/28 modify

Jedi15"/17" CML

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Title: CPU (Power Cap2)

Size	Document Number	Rev
A3	Jedi15"/17" CML	X01

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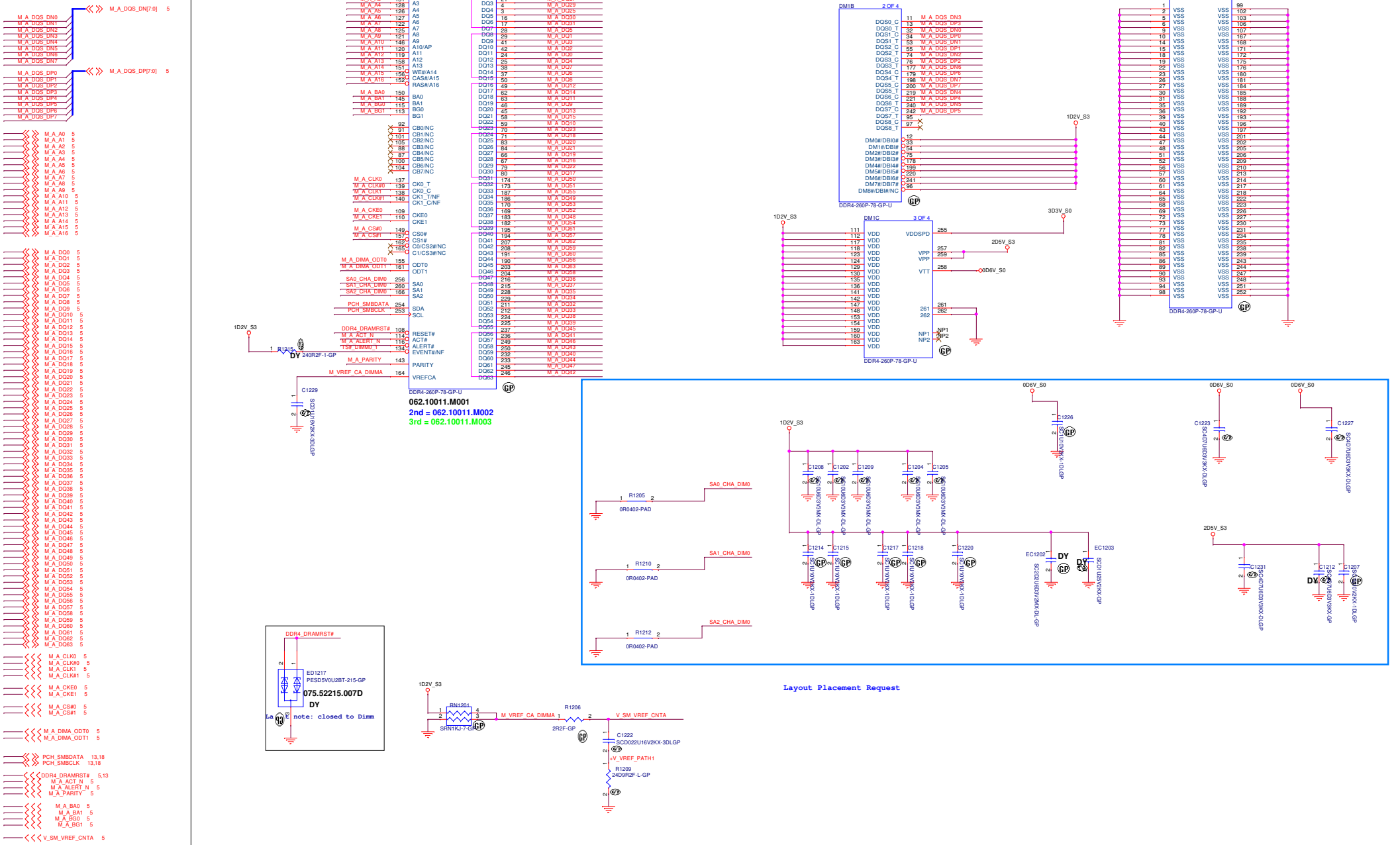
Main Func = MEMORY



Jedi15"/17" CML

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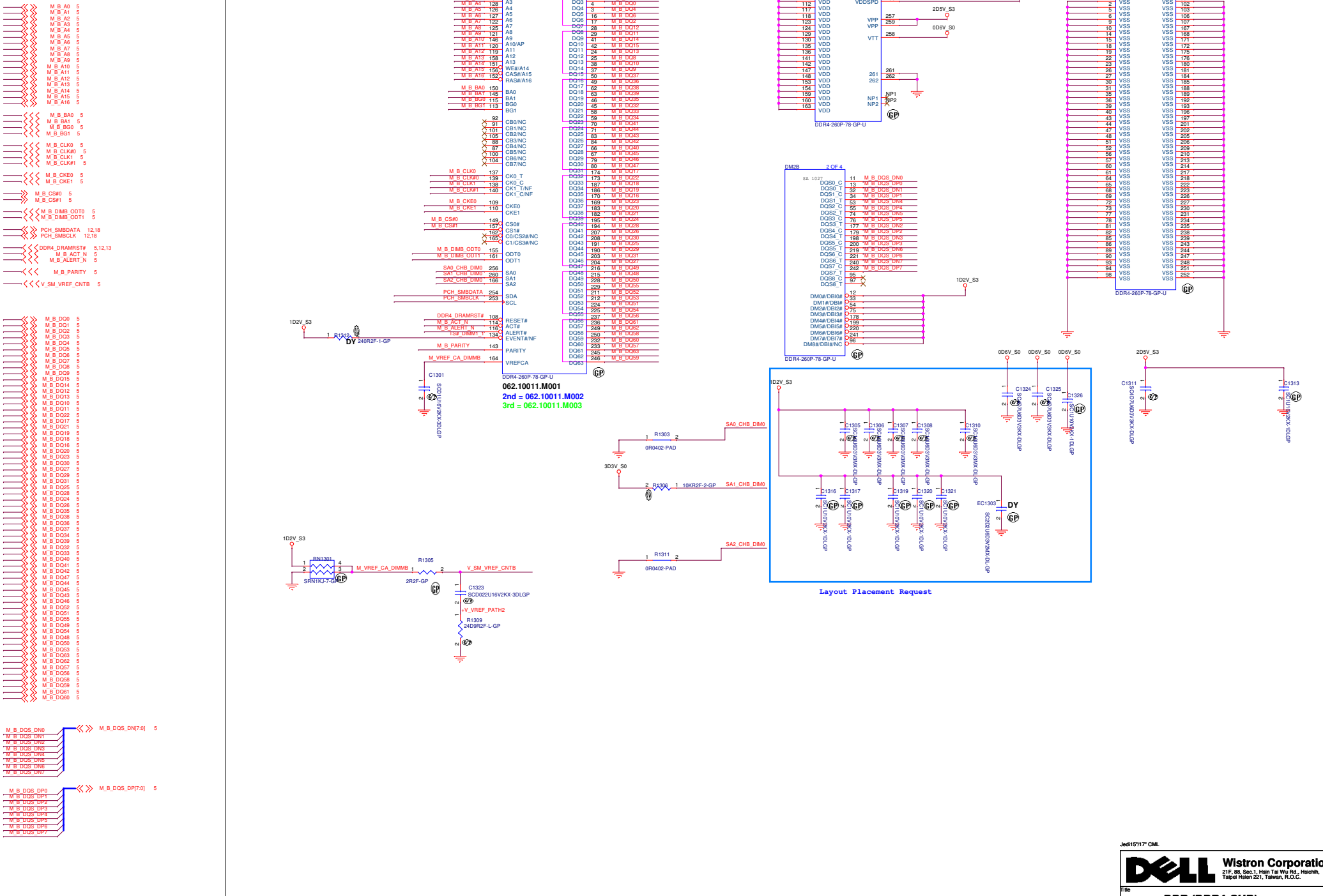
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHA)

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 12 of 106

Main Func = MEMORY



Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 13 of 106

Main Func = PCH

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. The system will use an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 for all FWH cycles targeting the alternate two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit 4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit 685	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. The recommended using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI boot functionality. This is for the SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap will cause SPI cycles to be aborted, but not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

Page 4 RN401 2.2K PU 3.3V_S0

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Page 4 RN403 2.2K PU 3.3V_S0

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

PCH strap pin:

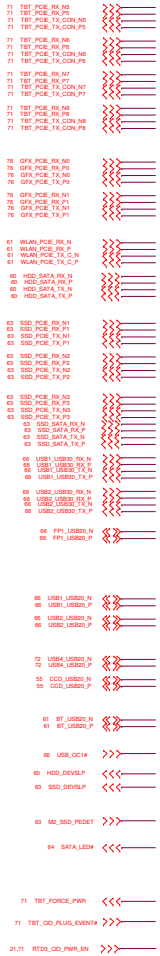
DISPLAY PORT PRESENCE STRAP

Wistron Corporation

CRB (STRAP)

Jedi6th17 CML

Main Func = PCH



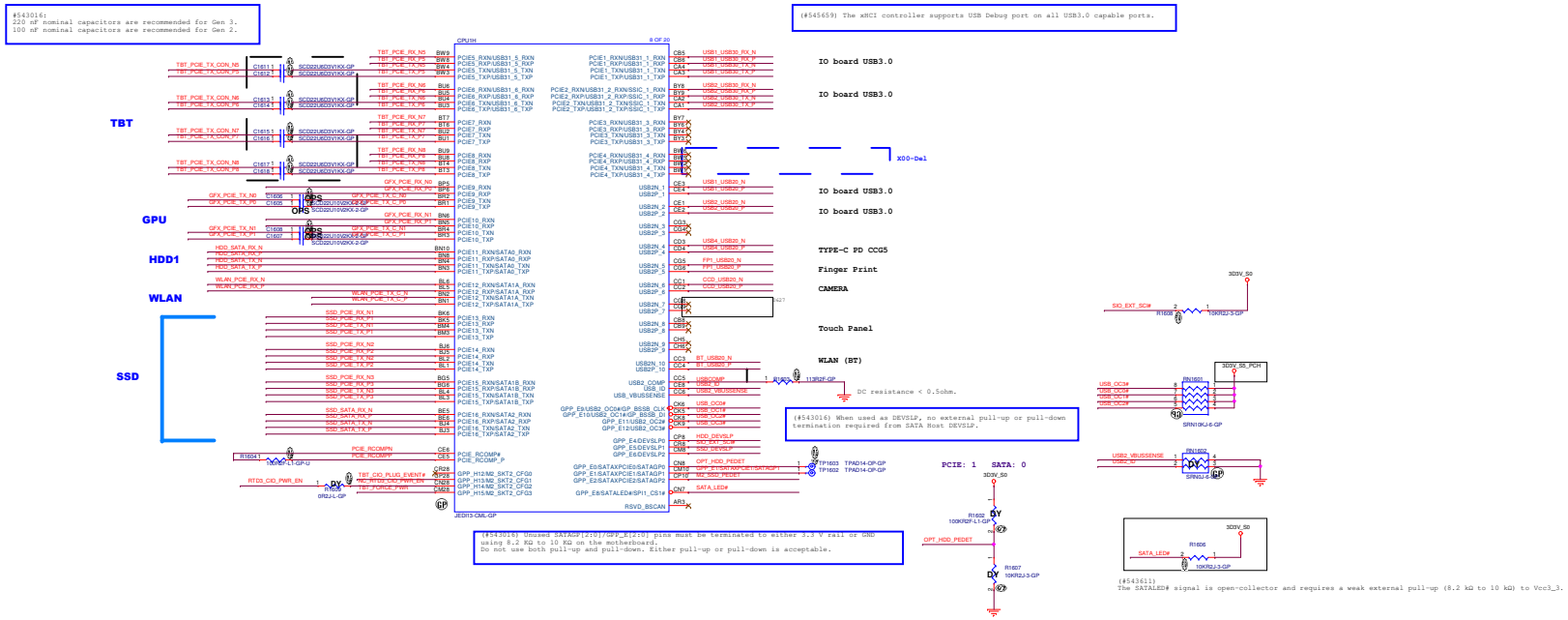
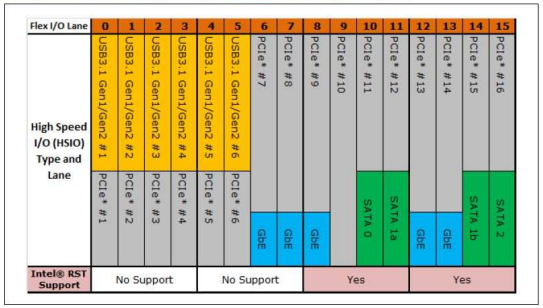


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP



6.3.1 PCH PCI Express* Interface Configuration Details

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

Main Func = PCH

24 SYS_PWROK
24,26 RESET_OUT#
24,40,46 VCCST_PWRGD
24 PCH_RSMRST#
25,45 3V_5V_PWRGD
24,40,91 PM_SLP_S0#
27,40,51,71 PM_SLP_S3#
40,51,66 PM_SLP_S4#
24 SIO_PWRBTN#
43,44 AC_IN#
26,61,63,66,71,76,91 PLTRST#_CPU
3 H_CPUPWRGD
15 INPUT3VSEL
90 PM_RSMRST#
71 PCIE_WAKE#_CPU

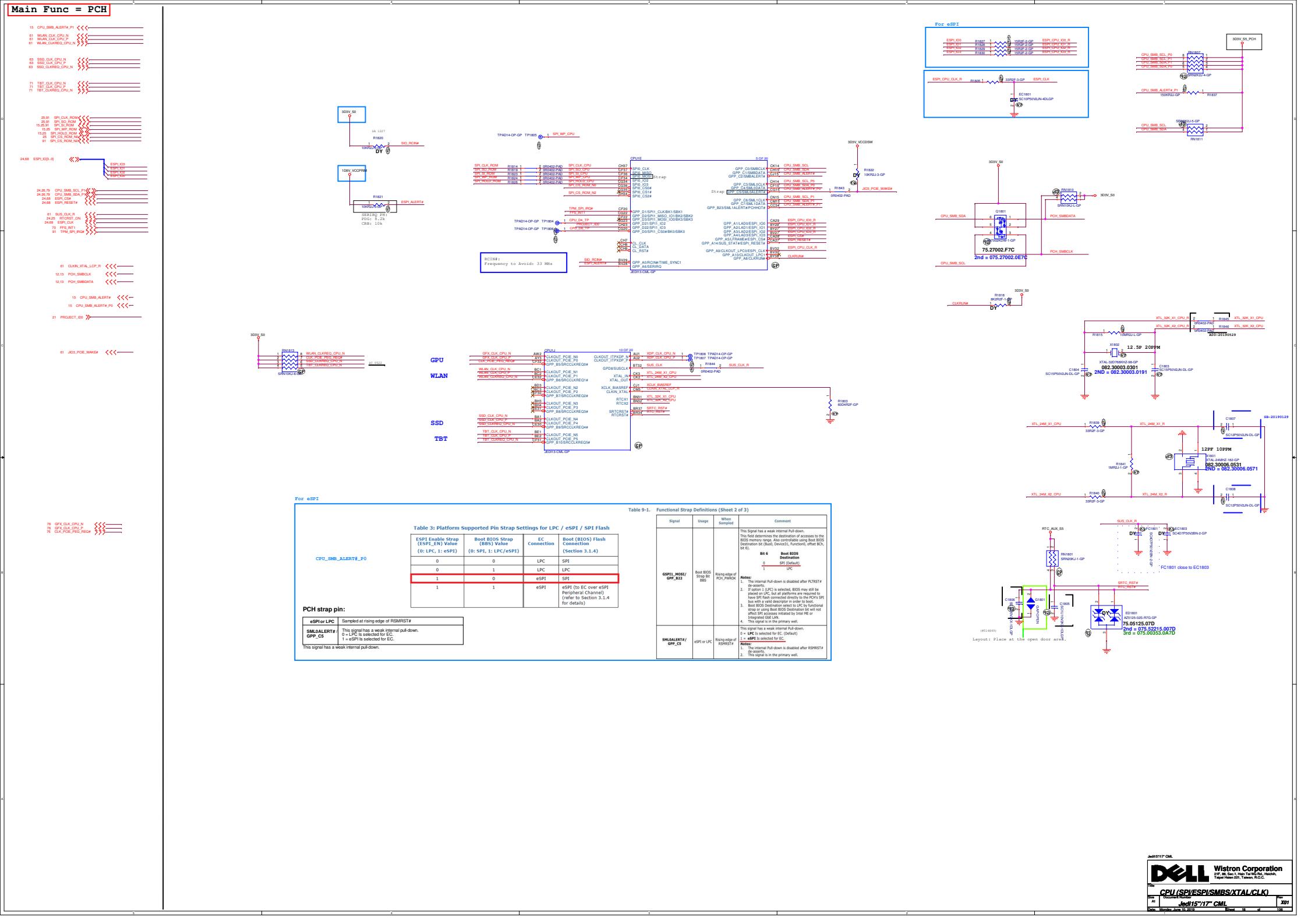
3D3V_VCCDSW
RN1704 SRN10KJ-L-GP
AC_PRESENT
PCIE_WAKE#_CPU
R1722 10KR2J-3-GP
PCH_BATLOW#
R1723 10KR2J-3-GP
DY
RTC_AUX_S5
R1720 330KR2J-L1-GP
#544669 (CRB): 330k.
SM_INTRUDER#
3D3V_VCCPRIM
R1731 100KR2J-3-GP
EXT_PWR_GATE#
3D3V_S5
R1721 10KR2J-3-GP
GPD11:LANPHYPC
GPD11 pull high by Intel PDG1.3 request
#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.
H_CPUPWRGD
R1714 220KR2J-3-GP
RN1703 SRN100KJ-8-GP
PM_RSMRST#
PM_PCH_PWROK
R1712 1_100KR2J-L1-GP
SYS_PWROK
1D8V_VCCPRM
R1738 1_10KR2J-3-GP
ME_SUS_PWR_ACK_R
R1708 0R2J-2-GP
SUSACK#_R
AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us
3D3V_AUX_S5
R1727 100KR2J-1-GP
R1726 10KR2J-3-GP
Q1701 FDT1086X-GP
3V_5V_PCH#
PM_RSMRST#
1KR2J-1-GP R1702
PCH_RSMRST#
3V_5V_PWRGD
075.00138.0A7C
2nd = 075.00138.0E7C
3rd = 075.00139.007C

3D3V_VCCPRIM
R1701 10KR2J-3-GP
CPU1K
11 OF 20
JEDI3-CML-GP
XDP_DBRESET#
PCH_PLTRST#
PM_RSMRST#
H_CPUPWRGD
VCCST_PWRGOOD_R
PROCPWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_LAN#
GPD9/SPI_WLAN#
GPD8/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL
PM_SLP_S0#
PM_SLP_S3#
PM_SLP_S4#
AUX_EN_WOWL
PM_SLP_A#
SIO_PWRBTN#
AC_PRESENT
PCH_BATLOW#
SM_INTRUDER#
EXT_PWR_GATE#
VRALERT#
INPUT3VSEL
TP1709 TPAD14-OP-GP
TP1710 TPAD14-OP-GP
TP1711 TPAD14-OP-GP
TP1712 TPAD14-OP-GP
TP1715 TPAD14-OP-GP
TP1713 TPAD14-OP-GP
TP1714 TPAD14-OP-GP
TP1708 TPAD14-OP-GP
(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.
BATLOW#:
Pull-up required even if not implemented.
AC_PRESENT
EC1707 SCD1U16V2KX-3DLGP

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP
3D3V_S0
R1718 100KR2F-L1-GP
VCCST_PWRGD
VCCST_PWRGD_R
R1717 100KR2F-L1-GP
R1719 47K5R2F-GP
C1711 SCD1U10V2KX-3DLGP
ED1704 AZ5125-02S-R7G-GP
75.05125.07D
2ND = 075.52215.007D
3rd = 075.00353.0A7D
R1722 & EC1708 modify to 100k and 0.01uF at DVT1
PLTRST#_CPU
R1713 0R0402-PAD
PCH_PLTRST#
R1715 100KR2J-1-GP
C1701 SC220P50V2KX-3DLGP
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
XDP_DBRESET#
SYS_PWROK
PCH_RSMRST#
RESET_OUT#
3V_5V_PWRGD
ED1702 AZ5125-02S-R7G-GP
ED1701 AZ5125-02S-R7G-GP
ED1703 AZ5125-02S-R7G-GP
75.05125.07D
2ND = 075.52215.007D
3rd = 075.00353.0A7D
3D3V_AUX_S5
R1737 100KR2J-1-GP
PM_RSMRST#_M
D1701 RB751V-40-GP
AC_IN#
Q1702 2N7002KDW-1-GP
common part
83.R2003.A8M
2ND = 083.52030.008F
75.27002.F7C
2nd = 075.27002.0E7C
Reserve by NON DS3 function 20150413

Jedi15"/17" CML
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (PMU)
Size: A1
Document Number:
Jedi15"/17" CML
Rev: X01
Date: Monday, June 09, 2008
Sheet 17 of 106

Main Func = PCH



Main Func = PCH

61 BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0
55 DMIC_PCH_DATA
55 DMIC_PCH_CLK
15,27 SPKR
27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
68 ME_FWP_SW
27 HDA_SDOUT_CODEC
65 KB_LED_BL_DET
15 HDA_SDOUT_CPU
24,85 DGPU_PWROK

33 SD_SDATA0
33 SD_SDATA1
33 SD_SDATA2
33 SD_SDATA3
33 SD_CMD
33 SD_WP
33 SD_CD_N
33 SD_CLK
33 SD_PWR_EN#

DGPU_PWROK
R1924 100KR2J-1-GP
SA-20181127

3D3V_S5
tTPM
R1910 10KR2J-3-GP
TPM_ID
TPM
R1911 10KR2J-3-GP

CPU1G 7 OF 20
HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST_N_CPU BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
KB_LED_BL_DET CK23 GPP_D23/I2S_MCLK
BL37
BL34 I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
TPAD14-OP-GP TP1903
BT_PCMFRM_RSTN R1923 33R2J-2-GP GPP_H1_SFRM CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
BT_PCMOUT_CLKREQ0 R1922 33R2J-2-GP GPP_H2_CLKREQ0 CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
DMIC_PCH_CLK CP24 GPP_D19/DMIC_CLK0/SNDW4_CLK
DMIC_PCH_DATA CN24 GPP_D20/DMIC_DATA0/SNDW4_DATA
TPM_ID CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
DGPU_PWROK CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA
SPKR CF35 GPP_B14/SPKR
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_1P8_RCOMP
SD_3P3_RCOMP
JEDI13-CML-GP
GPP_G0/SD_CMD CH36 SD_CMD
GPP_G1/SD_DATA0 CL35 SD_SDATA0
GPP_G2/SD_DATA1 CL36 SD_SDATA1
GPP_G3/SD_DATA2 CM35 SD_SDATA2
GPP_G4/SD_DATA3 CN35 SD_SDATA3
GPP_G5/SD_CD# CH35 SD_CD_N
GPP_G6/SD_CLK CK36 SD_CLK
GPP_G7/SD_WP CK34 SD_WP
BW36 SD_PWR_EN#
BY31
CK33 SD_RCOMP
CM34
R1901 1 2 200R2F-L-GP

EC1901 DY HDA_BITCLK_CODEC
SC10P50V2JN-4DLGP

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable *

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

HDA_SYNC_CODEC R1908 1 2 0R0402-PAD HDA_SYNC_CPU

R1920~R1921 need to close for merge prepare

HDA_BITCLK_CODEC R1920 1 0R0402-PAD HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 33R2J-2-GP HDA_SDOUT_CPU
ME_FWP_SW R1909 1 1KR2J-1-GP

HDA_SDOUT_CODEC
EC1903 DY
SC22P50V2JN-4DLGP

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2 | Document Number: Jedi15"/17" CML | Rev: X01
Date: Monday, June 10, 2019 | Sheet 19 of 106

Main Func = PCH

79,86 GC6_FB_EN
55 CPU_I2C_SDA_P1
55 CPU_I2C_SCL_P1
65,66 CPU_I2C_SDA_P0
65,66 CPU_I2C_SCL_P0
55 DBC_PANEL_EN
68 UART_2_CRXD_DTXD
68 UART_2_CTXD_DRXD
24 SIO_EXT_WAKE#
65 KB_DET#
24,66,69 LID_CL_SIO#
55 GSEN_INT1
70 GSEN2_INT1
15,25 RTC_DET#
55,70 CPU_I2C_SDA_ISH0
55,70 CPU_I2C_SCL_ISH0
70 FFS_INT2
91 PIRQA#
21 BOARD_ID2
71 PERST_N_CPU
61 CNV_BRI_RSP
15,61 CNV_RGI_DT_R
61 CNV_BRI_DT_R
61 CNV_RGI_RSP
76 DGPU_HOLD_RST#
79 GPU_EVENT#
86 DGPU_PWR_EN
15 NRB_BIT
15 GPP_B22_GSPI1_MOSI
24 NB_MODE#
24,66,69 LID_CL_SIO_TAB#
24 ISH_TABLE_MODE#
71 TBT_PCIE_WAKE#
4 IR_CAM_DET#

EC2002 DY DGPU_HOLD_RST#
C1KP50V2KX-1DLGP
RN2009 OPS DGPU_HOLD_RST# DGPU_PWR_EN
SRN10KJ-7-GP

1D8V_VCCPRM
R2053 10KR2J-3-GP PIRQA#
DY

3D3V_S0
51KR2J-1-GP R2048 UART_2_CRXD_DTXD
51KR2J-1-GP R2049 UART_2_CTXD_DRXD
DEBUG
10KR2J-3-GP DY R2043 DBC_PANEL_EN
10KR2J-3-GP R2044 FFS_INT2
10KR2J-3-GP R2045 KB_DET#
10KR2J-3-GP R2046 IR_CAM_DET#

3D3V_S5_PCH
10KR2J-3-GP R2041 SIO_EXT_WAKE#

1D8V_S5 SB 0326
R2029 DY 20KR2J-L2-GP CNV_RGI_RSP
R2030 DY 20KR2J-L2-GP CNV_BRI_RSP

GPU_EVENT# R2003 0R0402-PAD GPU_EVENT_MCP#
GC6_FB_EN R2004 0R0402-PAD
PIRQA#
GC6_FB_EN_MCP
VRAM_ID1
NRB_BIT
DBC_PANEL_EN
GPP_B22_GSPI1_MOSI
CNV_RGI_DT_R R2006 33R2J-2-GP
CNV_BRI_DT_R R2007 33R2J-2-GP
CNV_BRI_RSP
CNV_RGI_DT
CNV_BRI_DT
CNV_RGI_RSP
UART_2_CRXD_DTXD
UART_2_CTXD_DRXD
SIO_EXT_WAKE#
KB_DET#
CPU_I2C_SDA_P0
CPU_I2C_SCL_P0
CPU_I2C_SDA_P1
CPU_I2C_SCL_P1
MEM_CONFIG
MEM_CONFIG
MEM_CONFIG
MEM_CONFIG
MEM_CONFIG

CPU1F
GPP_B15/GSPI0_CS0#
GPP_A7/PIRQA#/GSPI0_CS1#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS0#
GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_F5/CNV_BRI_RSP
GPP_F6/CNV_RGI_DT
GPP_F4/CNV_BRI_DT
GPP_F7/CNV_RGI_RSP
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_H4/I2C2_SDA
GPP_H5/I2C2_SCL
GPP_H6/I2C3_SDA
GPP_H7/I2C3_SCL
GPP_H8/I2C4_SDA
GPP_H9/I2C4_SCL
JEDI13-CML-GP

Strap

6 OF 20
GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK DGPU_HOLD_RST#
GPP_D11/ISH_SPI_MISO/GSPI2_MISO TBT_PCIE_WAKE#
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI HTC_DET#
GPP_D5/ISH_I2C0_SDA CPU_I2C_SDA_ISH0
GPP_D6/ISH_I2C0_SCL CPU_I2C_SCL_ISH0
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
GPP_H10/I2C5_SDA/ISH_I2C2_SDA
GPP_H11/I2C5_SCL/ISH_I2C2_SCL
GPP_D13/ISH_UART0_RXD DGPU_PWR_EN
GPP_D14/ISH_UART0_TXD VRAM_ID2
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#
GPP_C12/UART1_RXD/ISH_UART1_RXD BOARD_ID1
GPP_C13/UART1_TXD/ISH_UART1_TXD FFS_INT2
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS# PERST_N_CPU
GPP_A18/ISH_GP0 GSEN_INT1
GPP_A19/ISH_GP1 GSEN2_INT1
GPP_A20/ISH_GP2 ISH_TABLE_MODE#
GPP_A21/ISH_GP3 ISH_ALS_INT#
GPP_A22/ISH_GP4 ISH_KB_DISABLE
GPP_A23/ISH_GP5 LID_CL_SIO_TAB#
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#

TBT CHECK

TP2003 TPAD14-OP-GP

3D3V_S0
RN2007 SRN1KJ-7-GP
CPU_I2C_SDA_ISH0
CPU_I2C_SCL_ISH0

TPAD
Touch panel

1D8V_S5
R2054 10KR2J-3-GP MEM_CONFIG

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

VRAM_ID[2:1] 11: UMA
01: DIS+4G VRAM
00: DIS+2G VRAM

3D3V_S0
R2038 10KR2J-3-GP UMA
VRAM_ID2
R2037 10KR2J-3-GP OPS

3D3V_S0
R2035 10KR2J-3-GP UMA
VRAM_ID1
R2034 10KR2J-3-GP VRAM_ID_2G

3D3V_S0
R2005 10KR2J-3-GP 2IN1
BOARD_ID2
R2008 10KR2J-3-GP DY

3D3V_S0
R2010 10KR2J-3-GP DY
BOARD_ID1
R2009 10KR2J-3-GP WHL-U

ISH_KB_DISABLE
2IN1
G D S
NB_MODE#
Q2001 PJA138KA-GP
084.00138.0A31
2nd = 084.00138.0C31

3D3V_S5
R2050 10KR2J-3-GP
2IN1
NB_MODE#

PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

CNV_BRI_DT
XTAL FREQUENCY SELECTION
1 = 24MHZ
0 = 38.4/19.2MHZ
PCH HAS INTERNAL 20K PD

CNV_RGI_DT
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT
1 = CLKIN_XTAL_LCP
0 = XTAL_IN
PCH HAS INTERNAL 20K PU

Jedi15"/17" CML

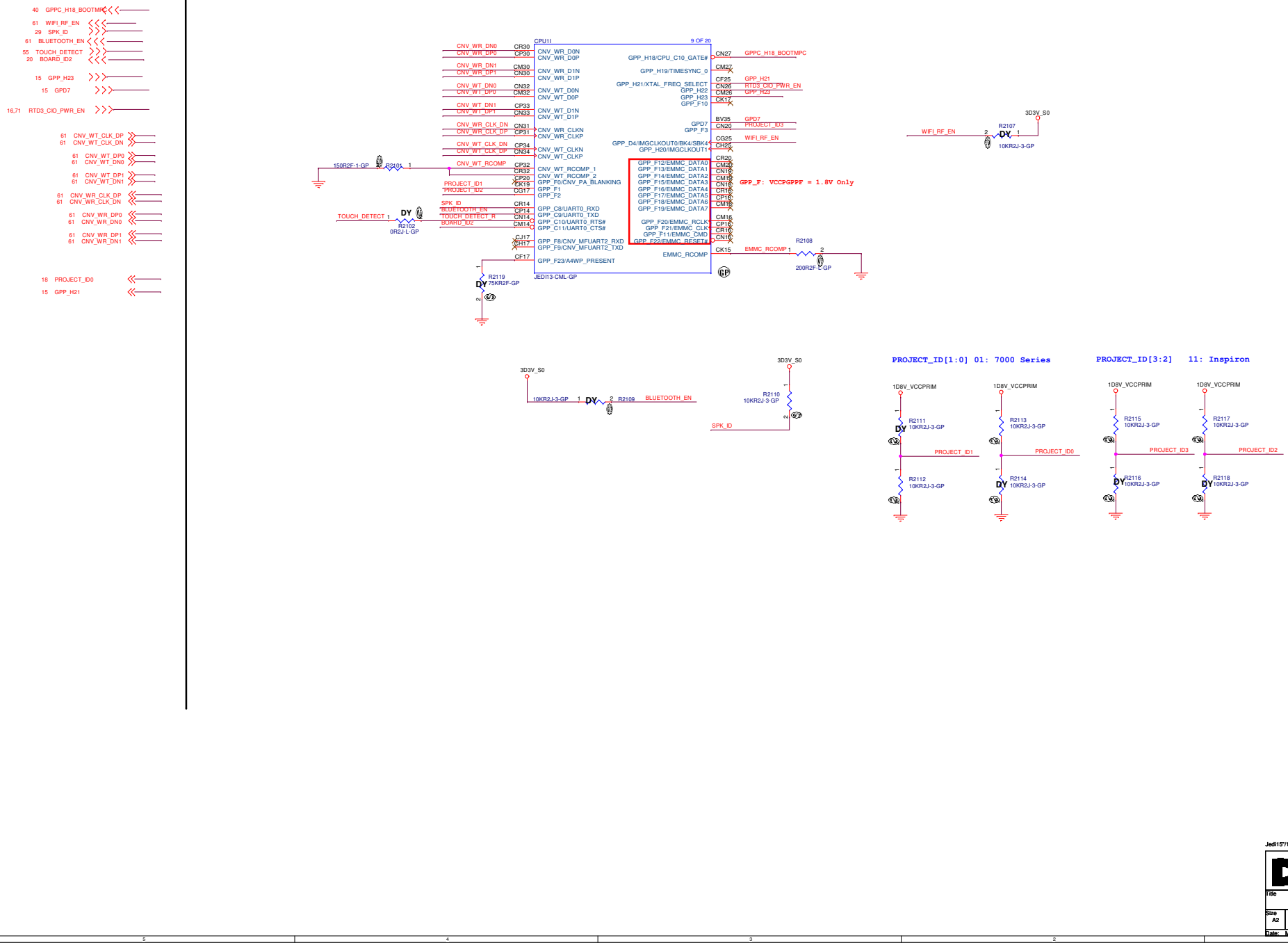
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPSS/ISH)

Size	Document Number	Rev
A2	Jedi15"/17" CML	A00

Date: Monday, June 10, 2019 Sheet 20 of 106

Main Func = PCH



Jedi15"/17" CML

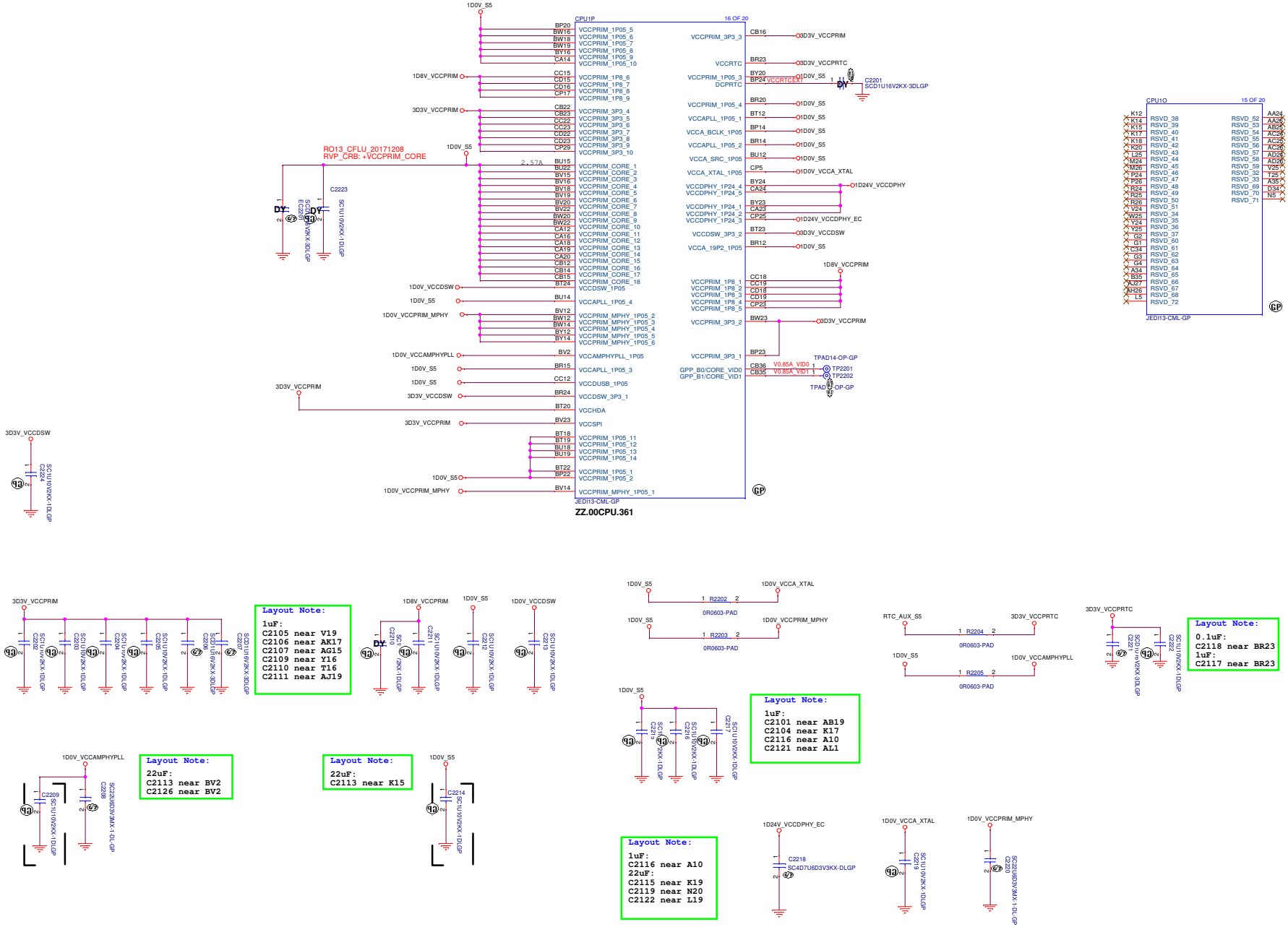
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (EMMC/CNVI)

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 21 of 106

Main Func = PCH



Jedi15"/17" CML

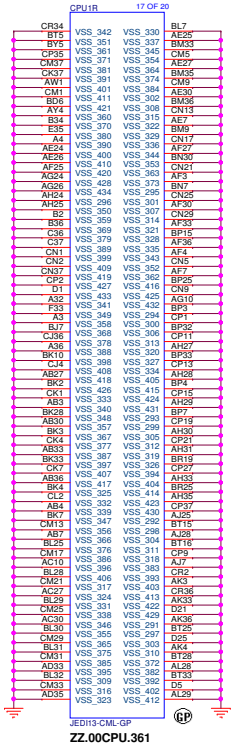
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

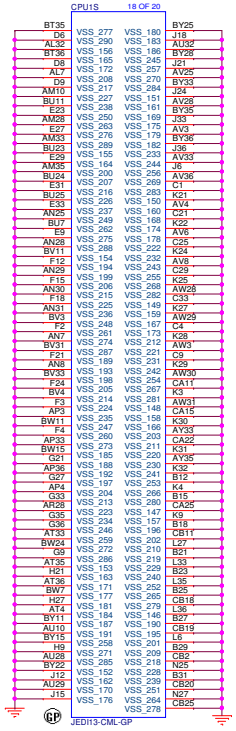
Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 22 of 106

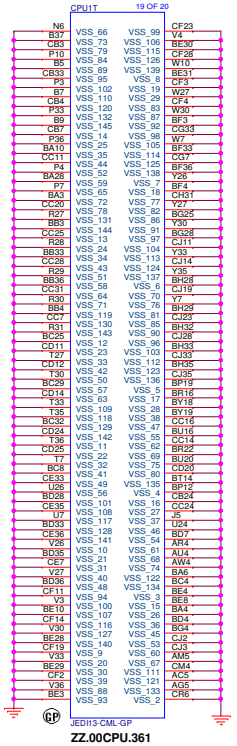
Main Func = PCH



ZZ.00CPU.361



ZZ.00CPU.361



ZZ.00CPU.361

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 23 of 106

Main Func = KBC

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.806
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

MODEL ID

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	TBD	100.0K	10.0K	3
2	TBD	100.0K	17.8K	2.801
3	3x4x13 UMA 2301	100.0K	27.0K	2.598
4	TBD	100.0K	37.4K	2.402
5	TBD	100.0K	49.9K	2.201
6	3x4x17/17UMA 2301	100.0K	64.9K	2.001
7	TBD	100.0K	82.5K	1.806
8	TBD	100.0K	107K	1.594
9	3x4x17/17QC 2301	100.0K	154K	1.299
10	TBD	100.0K	200K	1.1

64.64925.6DL

64.15435.6DL

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

RATTER /CHARGER
CPU/ GPU/ Thermal
TBT

Power Switch Logic(PSL)

For USB TypeC

pull high on CPO side

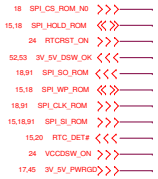
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

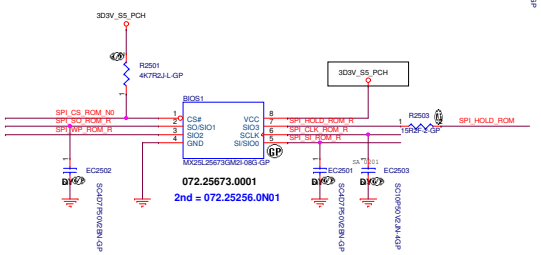
Title: ECI(SMSC 1416)
Size: Document Number: Jedi15"/17" CML
Rev: X01
Date: Monday, June 04, 2012 Sheet 1 of 1

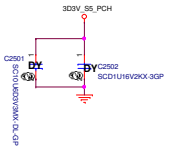
Main Func = SPI Flash

SPI Flash ROM(32M) for PCH

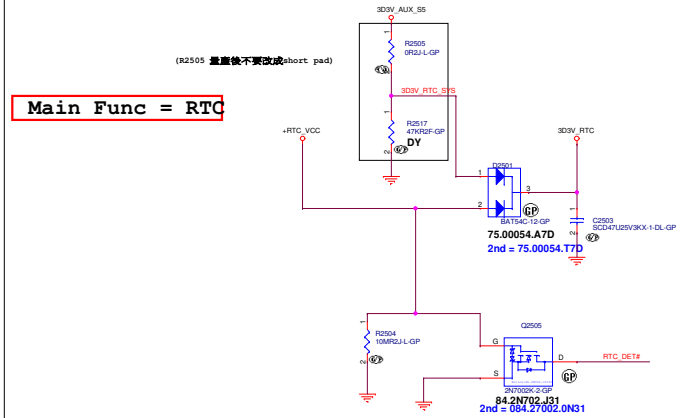
Source	QUAD/DUAL fast read	DUAL fast read	SFDP
072.25128.0B51	O	O	O
072.25127.0001	O	O	O
072.25128.0D61	O	O	O

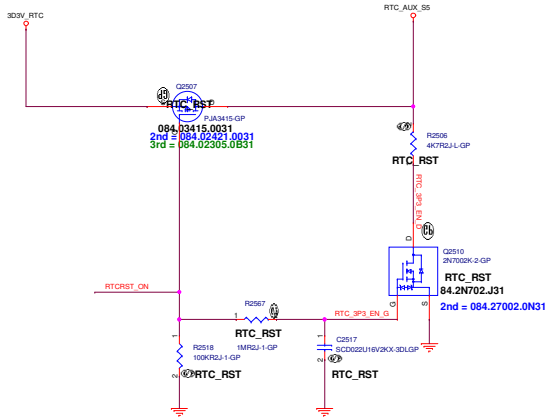


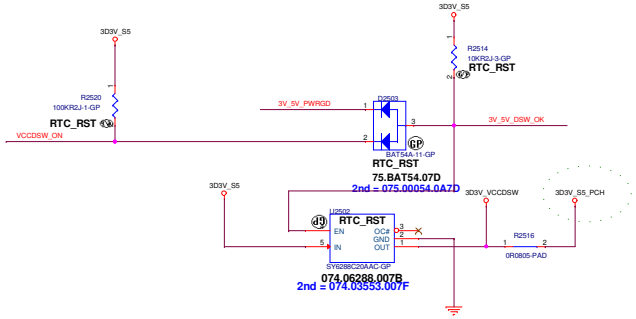




Main Func = RTC







29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

Jedi15"/17" CML

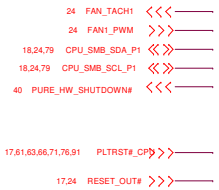
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

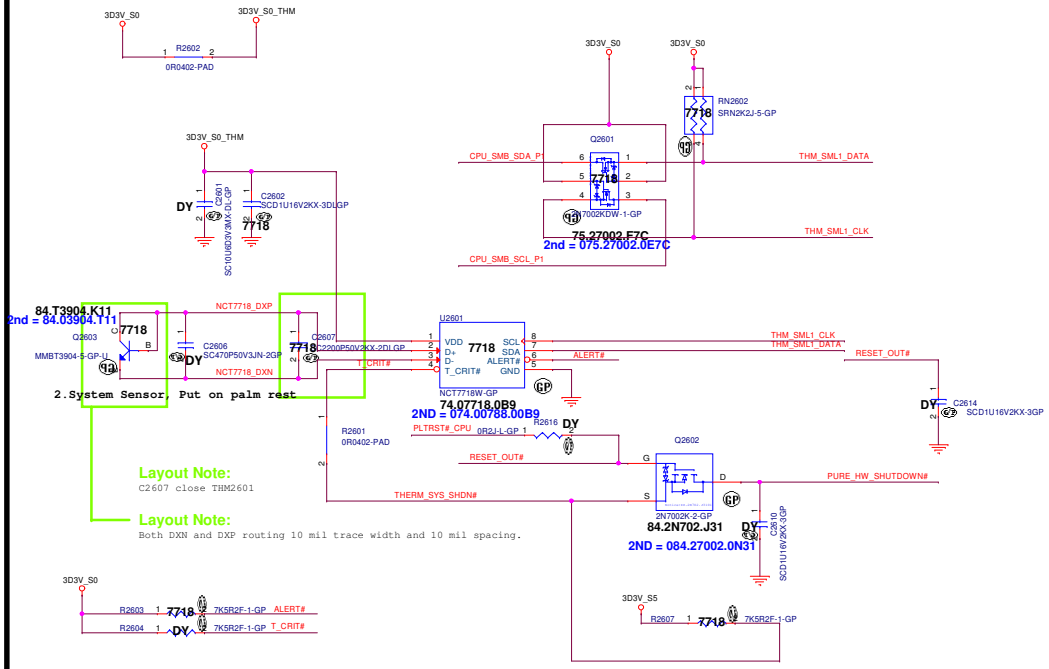
Title: Flash/RTC

Size	Document Number	Rev
Custom	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 25 of 105

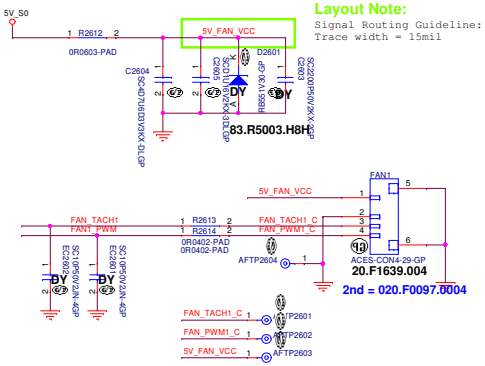
Main Func = Thermal Sensor





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



Jedi15"/17" CML

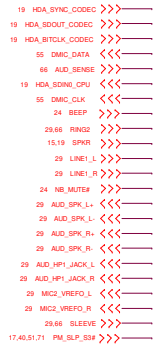
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

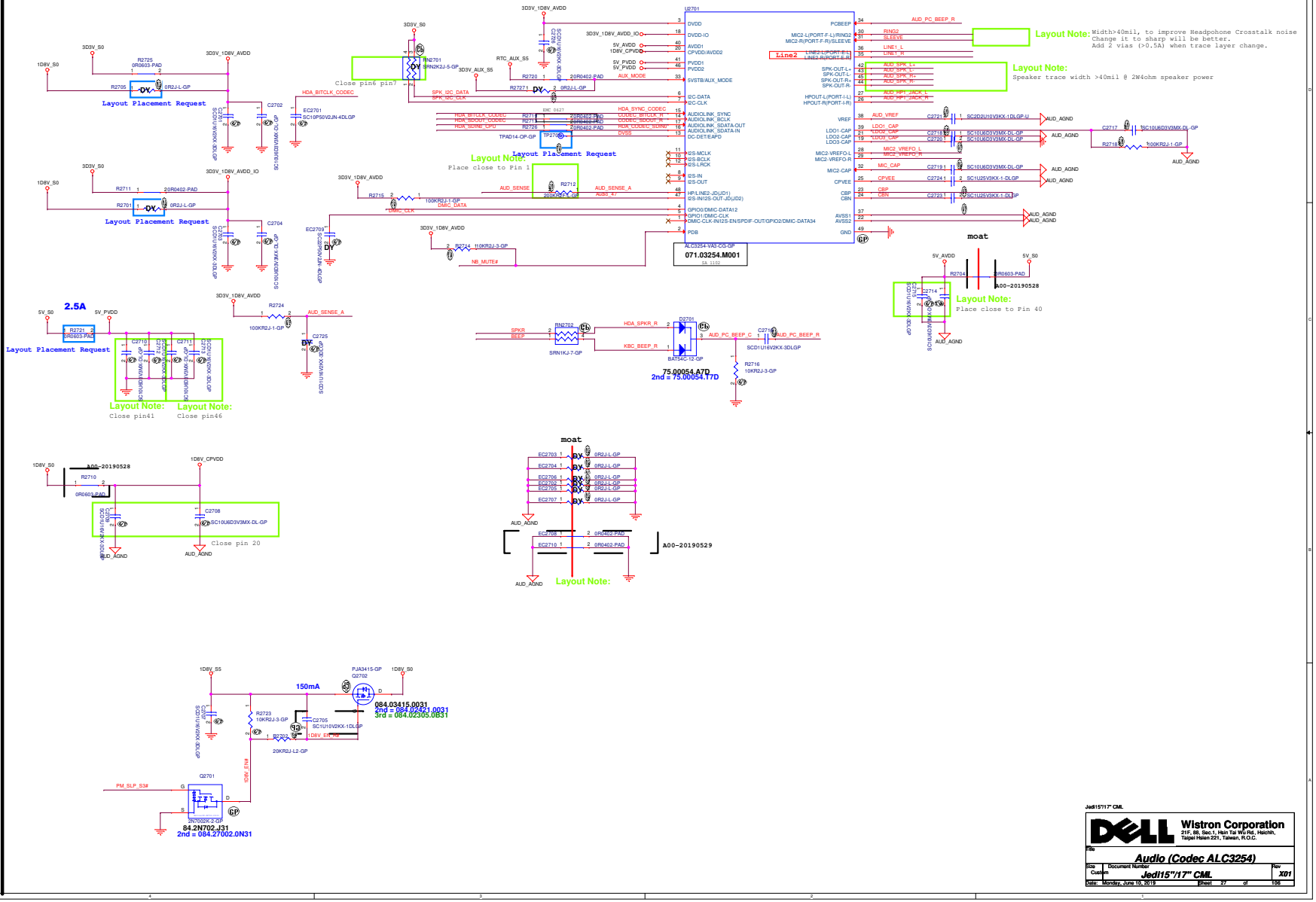
Title: INT IO (Thermal/Fan)

Size: A2 | Document Number: Jedi15"/17" CML | Rev: X01

Date: Monday, June 10, 2019 | Sheet 26 of 106

Main Func = Audio





Main Func = Audio

21 SPK_ID
27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R-
27 AUD_SPK_R+

27 MIC2_VREFO_R
27 MIC2_VREFO_L
27,29,66 RING2
27 LINE1_L

27 LINE1_R

27,29,66 SLEEVE

27 AUD_HP1_JACK_L
27 AUD_HP1_JACK_R

27,66 AUD_SENSE

66 AUD_HP1_JACK_L1
27,29,66 RING2
27,29,66 SLEEVE
66 AUD_HP1_JACK_R1

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

AUD_SPK_L+ — R2919 1 — 20R0402-PAD — AUD_SPK_L+_C
AUD_SPK_L- — R2920 1 — 20R0402-PAD — AUD_SPK_L-_C
AUD_SPK_R- — R2921 1 — 20R0402-PAD — AUD_SPK_R-_C
AUD_SPK_R+ — R2922 1 — 20R0402-PAD — AUD_SPK_R+_C

EC2906 SC1KF50V2KX-1DL0P
EC2905 SC1KF50V2KX-1DL0P
EC2907 SC1KF50V2KX-1DL0P
EC2908 SC1KF50V2KX-1DL0P

SPK1
SPK_ID
ACES-CON6-20-GP-U
20.F1639.006
2nd = 020.F1263.0006

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: FG
0: Veci

AFTP TESTPOINT

AUD_SPK_L-_C — AFTP2901
AUD_SPK_L+_C — AFTP2902
AUD_SPK_R-_C — AFTP2903
AUD_SPK_R+_C — AFTP2904
SPK_ID — AFTP2911

MIC2_VREFO_R
MIC2_VREFO_L
RN2901 SRN2K2J-4GP

Line2 ->
RING2
AUD_HP1_JACK_L — LINE1_L C2901 — LINE1-L_C — R2915 1 — 2 0R0603-PAD — AUD_HP1_JACK_L1
R2918 1 — 20R0402-PAD
SC10U6D3V3MX-DL-GP

Line2 ->
AUD_HP1_JACK_R — LINE1_R C2902 — LINE1-L_R — R2916 1 — 2 0R0603-PAD — AUD_HP1_JACK_R1
R2917 1 — 20R0402-PAD
SC10U6D3V3MX-DL-GP

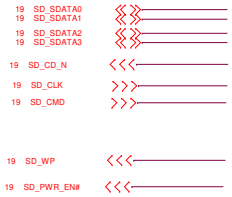
SLEEVE

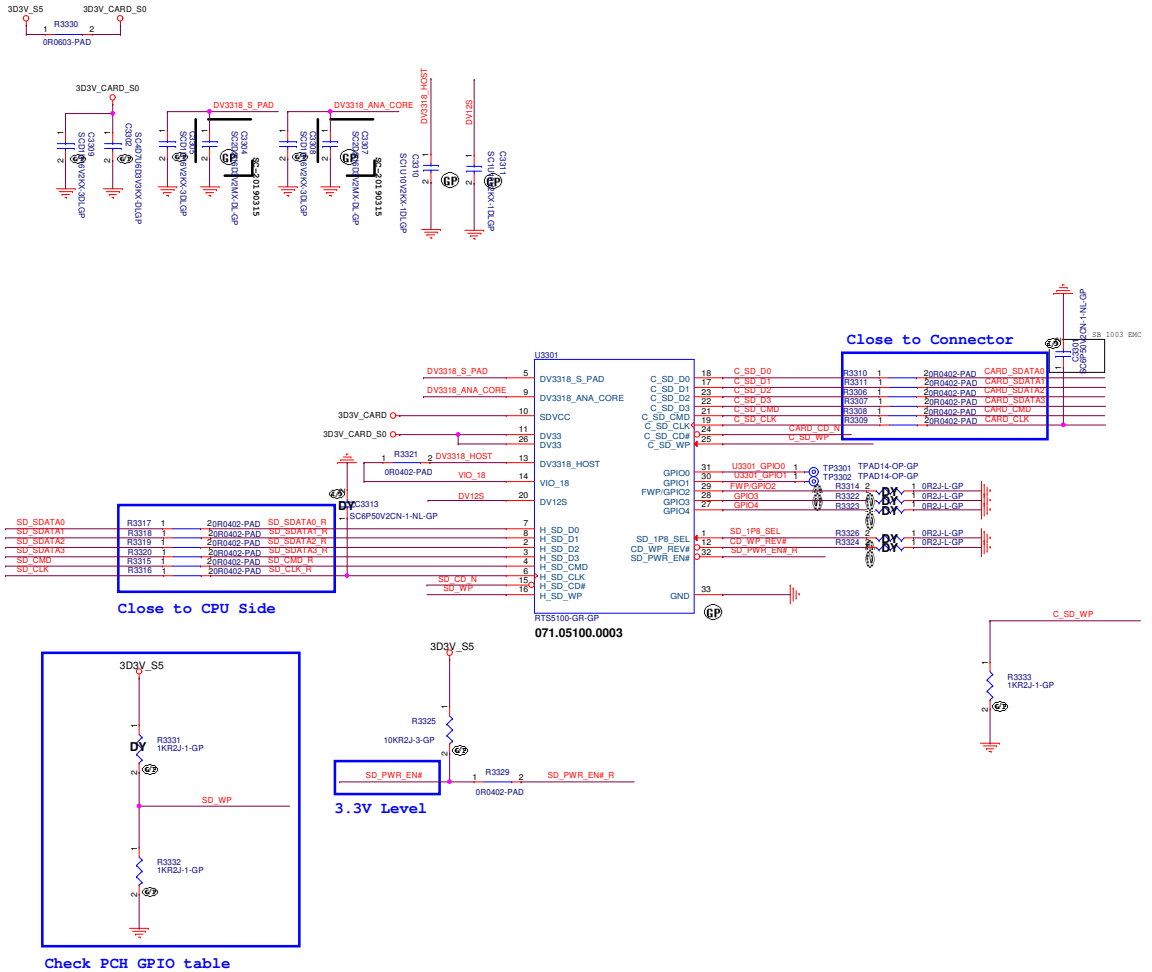
Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A2
Document Number: Jedi15"/17" CML
Rev: A00
Date: Monday, June 10, 2019
Sheet 29 of 106

Main Func = Card Reader





Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader-RTS5100*

Size	Document Number	Rev
A2	*Jedi15"/17" CML*	*A00*

Date: Monday, June 10, 2019 Sheet 33 of 106

Main Func = Power Plane & Sequence

17,27,51,71 PM_SLP_S3#
51 VDDQ_PWRGD
17,24,46 VCCST_PWRGD
45 3V_5V_EN
24 ALWON
26 PURE_HW_SHUTDOWN#
17,51,65 PM_SLP_S4#
52 1D0V_S5_PWRGD
24,53 PRIM_PWRGD
17,25,45 3V_5V_PWRGD
17,24,91 PM_SLP_S0#
21 GPPC_H18_BOOTMFC

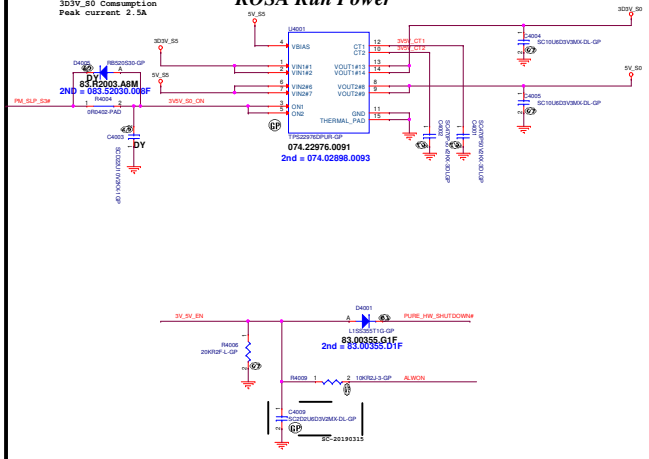
5V_S0

5V_S0 Comsumption
Peak current 5A

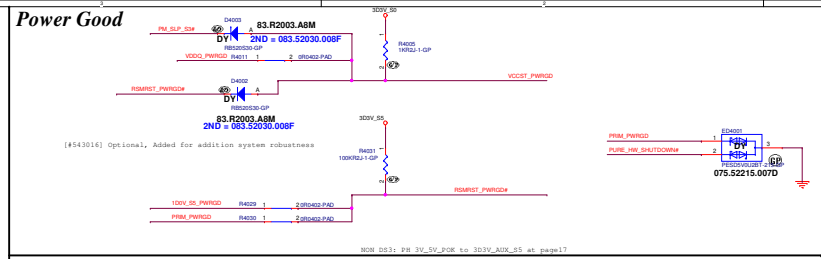
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

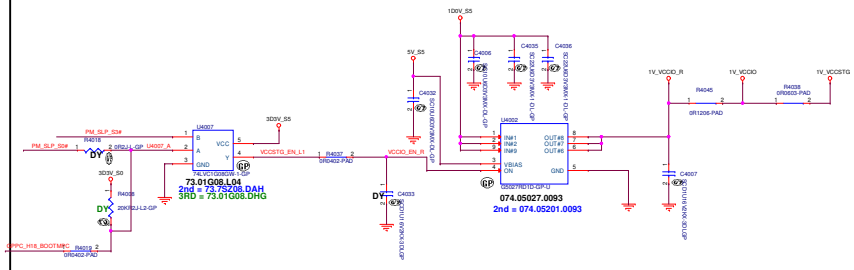
ROSA Run Power



Power Good



+VCCIO/+VCCSTG



EOPIO and EDRAM

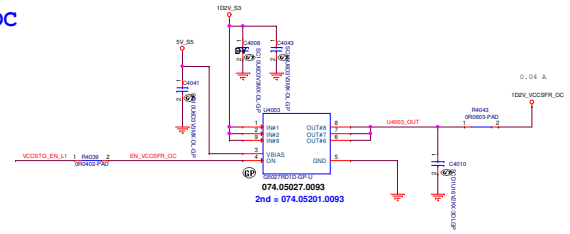
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

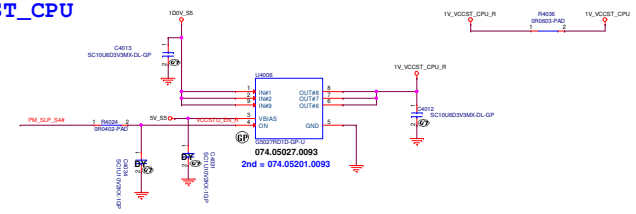
1D2V_VCCSFR_OC



VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

MANAGEMENT RAIL POWER GENERATION

VCCST_CPU



+V1.8S0

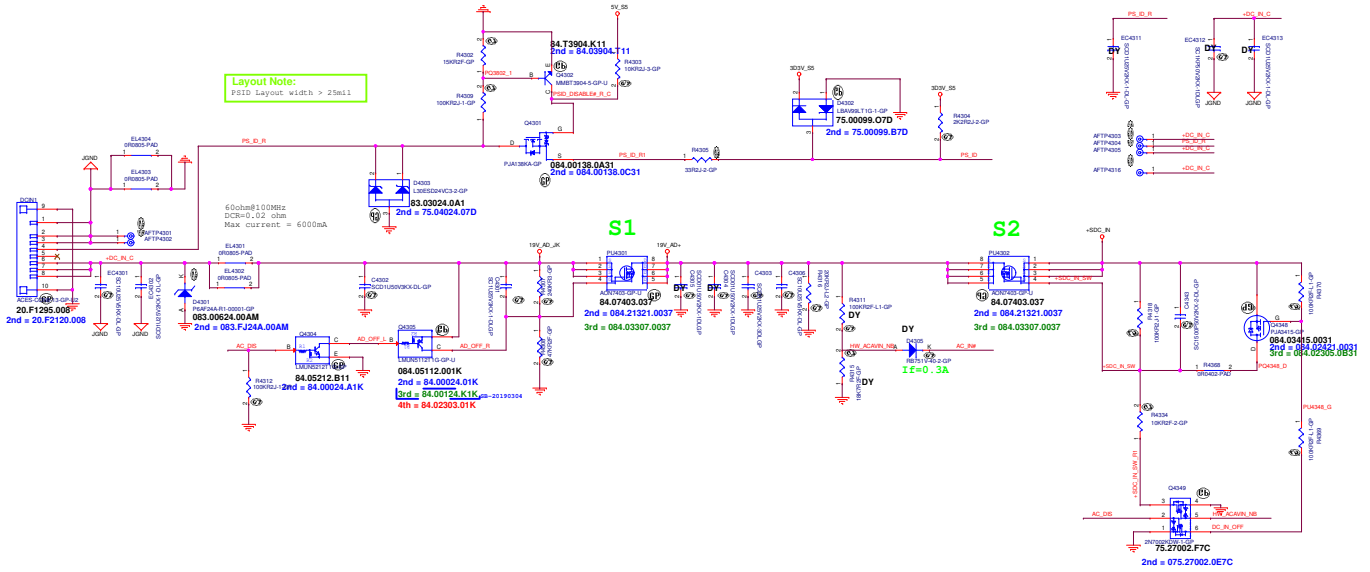
Jedi15"/17" CML

DELL Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

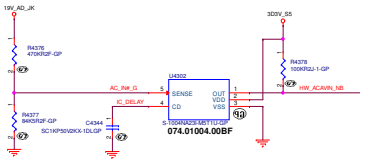
Title: *Sequence (Power Enable)*

Size	Document Number	Rev
A3	Jedi15"/17" CML	X01
Date: Monday, June 18, 2007	Sheet 43 of 106	

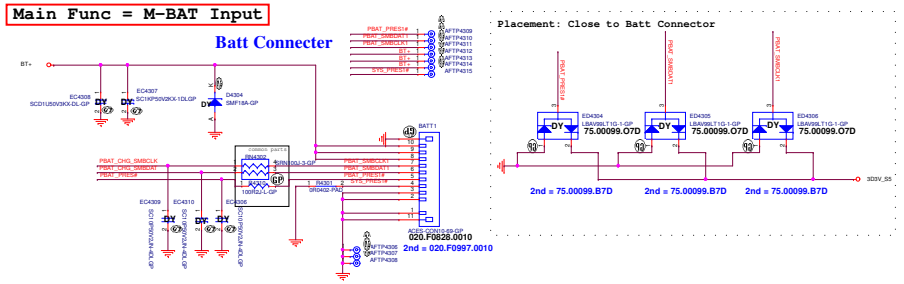
Main Func = ADT Input



Barrel Adapter Piug-in Detect



Main Func = M-BAT Input



Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (ATX/ DC/ BATT Conn)

Size	Document Number	Rev
A1	Jedi15"/17" CML	X01

Date: Monday, June 10, 2013 Sheet 43 of 106

ISL9538H For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

From KSP ACK

10"11.5*4
DCR=6.1~6.8mohm
Idc=15A, Isat=18A

+3D3V_VDD_DCIN

20V>+DC_IN>4.7V

Vout=1.24*(1+(R1/R2))

Vcore_OVP

Trigger Voltage
VDD=4.5V, Vcore > 1.88V
VDD= 5V, Vcore > 2.084V
VDD=5.5V, Vcore > 2.3V

Vsys_UVP

Trigger Voltage
VDD=4.5V, DCBATOUT < 5.39V
VDD= 5V, DCBATOUT < 5.98V
VDD=5.5V, DCBATOUT < 6.58V

Part Reference	Internal LDO (Charger LDO)	External LDO
PC44C3	DY	Stuff
PC44C1	DY	Stuff
PC44C2	DY	Stuff
PR44C7	DY	Stuff
PR44C1	DY	Stuff
PR44C2	DY	Stuff
PR44C3	DY	Stuff
PR44C4	DY	Stuff
PR44C5	DY	Stuff
PR44C6	Stuff	DY
PU44C1	DY	Stuff
PR44A2	64.36535.6DL (365K)	64.24335.6DL (243K)
PR44A3	64.10735.6DL (107K)	64.11035.6DL (110K)
PR44B7	64.16535.6DL (165K)	64.80625.6DL (80.6K)
PR44B1	64.15035.6DL (150K)	64.15035.6DL (150K)

PU +VCCSTG = 1.0 V on CPU side

Barrel Prochot

Follow custormer circuits.

TypeC Prochot

Follow custormer circuits.

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

Wistron Corporation
Power (Charger_ISL9538)
Jedi15"/17" CML
A00

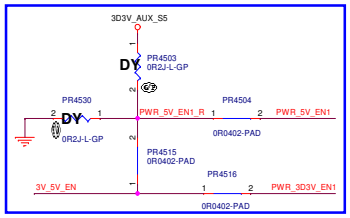
Main Func = PWR.Plane.Regulator_5V

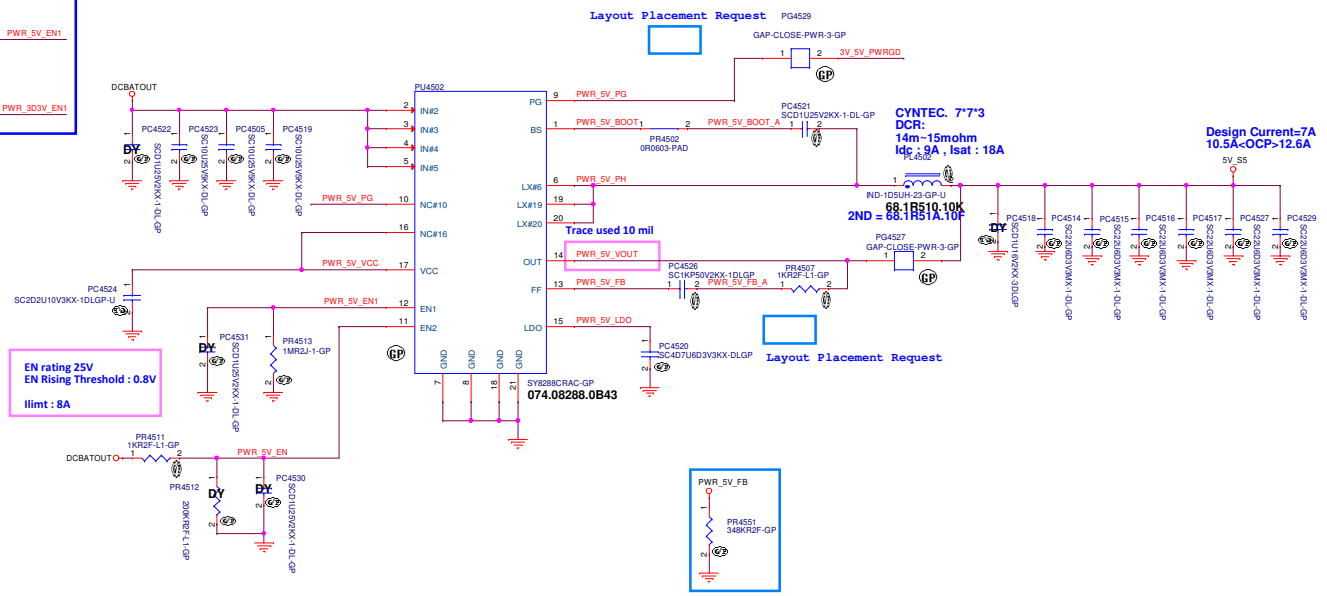
OFFPAGE-Signal

40 3V_5V_EN

17,25,45 3V_5V_PWRGD

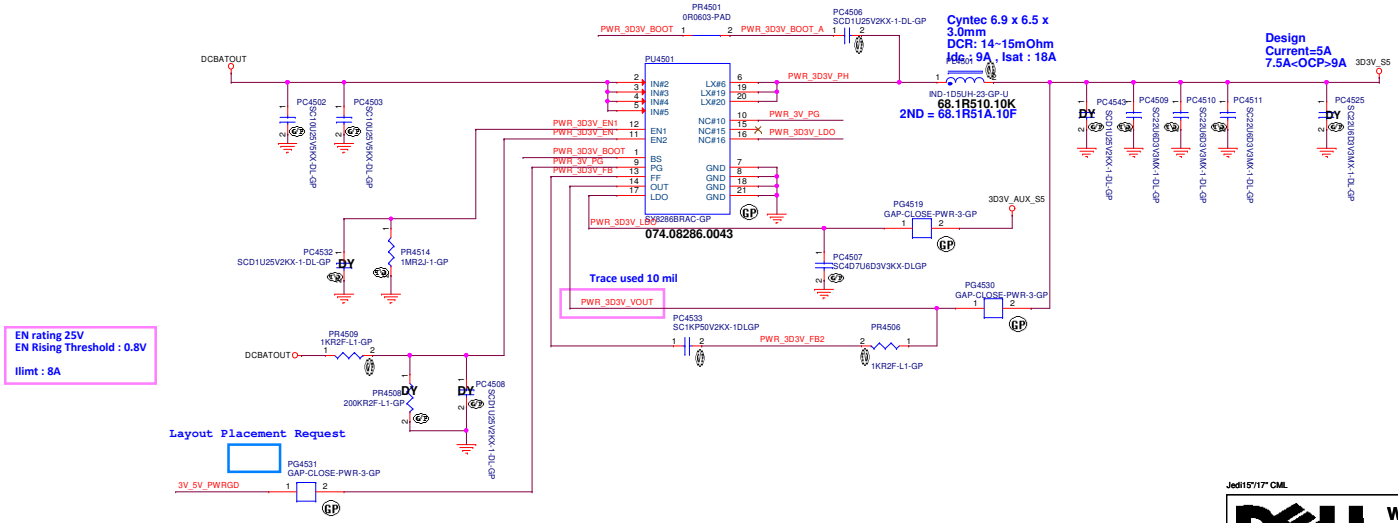
OFFPAGE-GAP





Main Func = PWR.Plane.Regulator_3D3V

17,25,45 3V_5V_PWRGD



Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power (SY8288/8286_5V/3D3V)**

Size	Document Number	Rev
A2	Jedi15"/17" CML	A00

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Main FUNC = CPU_CORE

OFFPAGE

PH on CPU side

3,24,44,72 PROCHOT#_CPU — PROCHOT#_CPU

7 SVID_ALERT#_CPU — SVID_ALERT#_CPU

7 SVID_CLK_CPU — SVID_CLK_CPU

7 SVID_DATA_CPU — SVID_DATA_CPU

VCORE_PG

PH on EE side

17,24,40 VCCST_PWRGD — VCCST_PWRGD

PL on EE side

7 VSSCORE_SENSE — VSSCORE_SENSE

7 VCCCORE_SENSE — VCCCORE_SENSE

PH on EE side

PH on EE side

8 VCCGT_SENSE — VCCGT_SENSE

8 VSSGT_SENSE — VSSGT_SENSE

PL on EE side

PL on EE side

8 VSSSA_SENSE — VSSSA_SENSE

8 VCCSA_SENSE — VCCSA_SENSE

PH on EE side

44 PWR_CORE_PSYS — PWR_CORE_PSYS

EE side Link

SVID Pull High V

1V_VCCST_CPU — PR4601 GAP-CLOSE-PWR-3-GP — PWR_CORE_VCCST

	2 phase	3 phase
PC4655	DY	0.022uF(78.22321.2FLDL)
PR4648	510 (64.51005.6DL)	453 (64.45305.6DL)
PC4635	DY	0.047uF(078.47322.02FD)
PR4660	2.55K(64.25515.6DL)	3.16K(64.31615.6DL)
PR4661	53.6K(64.53625.6DL)	64.9K(64.64925.6DL)
PR4601	1K(64.10015.6DL)	DY
PC4610	0.022U(78.22322.2FLDL)	0.033U(78.33322.2FL)

Jedi15"/17" CML

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Title: POWER (95829_CPUCORE(1/3))

Size: Custom | Document Number: Jedi15"/17" CML | Rev: A00

Date: Monday, June 10, 2019 | Sheet 46 of 106

Main FUNC = CPU_CORE

OFFPAGE

For acoustic noise

DCBATOUT
PT4702
SE33L0J50M0-11-GP
79.33612.20L
2nd = 077.23361.0001

	2 phase	3 phase
PR4722	DY	100K(64.10035.6DL)
PR4751	DY	100K(64.10035.6DL)
PR4724	DY	100K(64.10035.6DL)
PR4752	DY	100K(64.10035.6DL)
PR4730	DY	100K(64.10035.6DL)
PR4753	DY	100K(64.10035.6DL)
PR4731	DY	2.2R(64.2R205.6DL)
PU4703	DY	AOZ5038QI-05-GP(074.05038.0A73)
PC4767	DY	1uF(78.10523.5FLDL)
PC4718	DY	1uF(78.10523.5FLDL)
PC4720	DY	0.22uF(78.22422.2BLDL)
PR4720	DY	2.2R(64.2R205.55L)
PL4705	DY	0.15uH(068.R1510.1171)
PR4729	DY	3.65K(64.36515.6DL)
PR4732	DY	100K(64.10035.6DL)
PR4727	DY	10R(64.10R05.L1L)
PT4704	DY	330uF(79.33719.20C)
PC4735	DY	10uF(078.10612.05BD)
PC4736	DY	10uF(078.10612.05BD)
PC4737	DY	10uF(078.10612.05BD)

CML_U42_Perf
TDC=58A
Iccmax=85A

Cyntec
6.8mm(7.6mm)3.0mm
DCR: 0.8m ohm +/-7%
Ido : 38A , Isat : 48A

068.R1510.1171
2nd = 068.R1510.1141

074.05038.0A73
2nd = 074.00634.0073
3rd = 074.05537.0073

79.33719.20C
2nd = 79.33719.L01

For 3 phase

Jedi15"/17" CML
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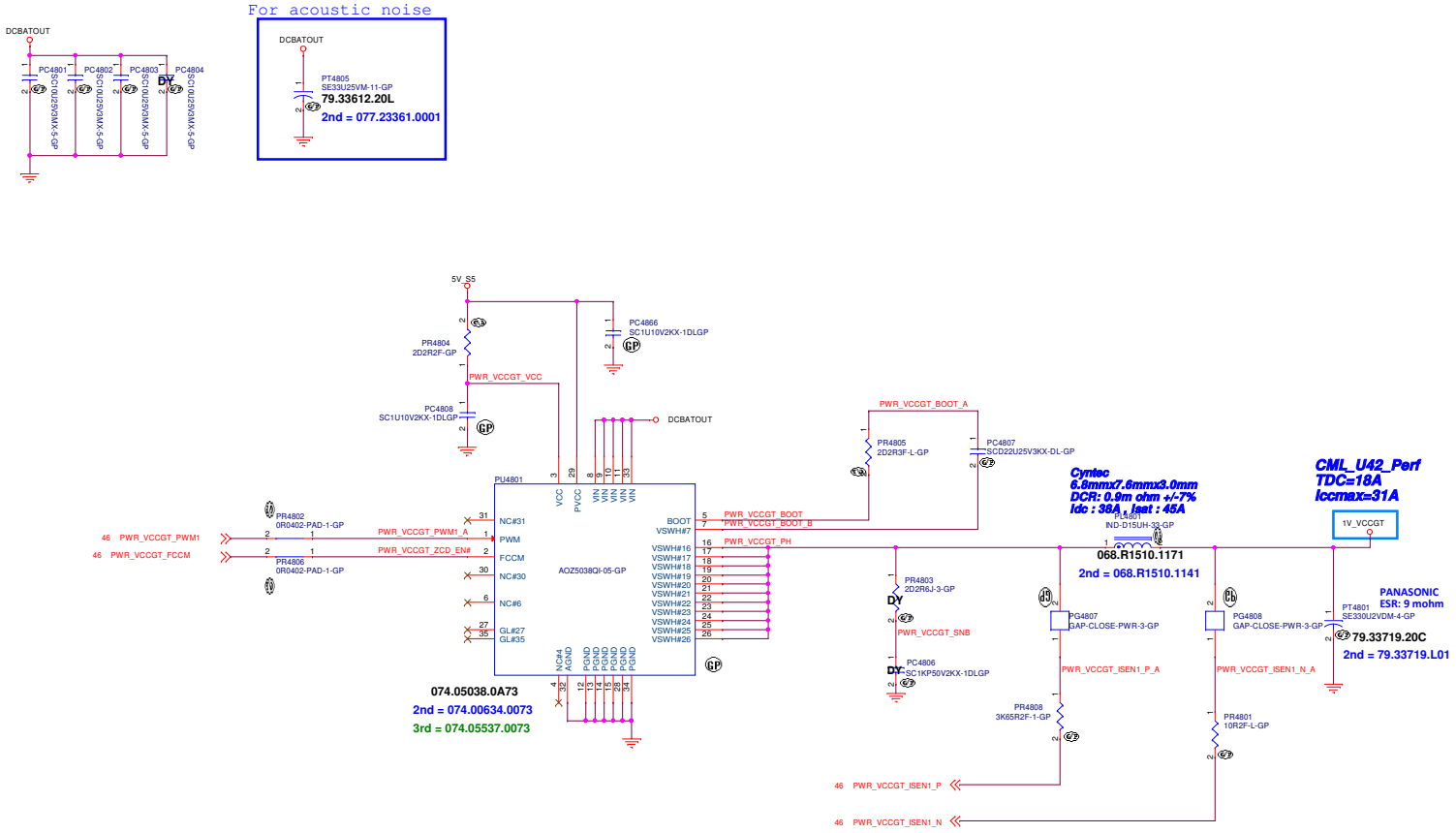
Title: POWER (AOZ5038_CPU_VCORE(2/3))
Size: Custom | Document Number: Jedi15"/17" CML | Rev: A00
Date: Monday, June 10, 2019 | Sheet 47 of 186

Main FUNC = CPU_CORE



Jedi15"/17" CML

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Title: POWER (5038_CPU_VCORE(3/3))

Size	Document Number	Rev
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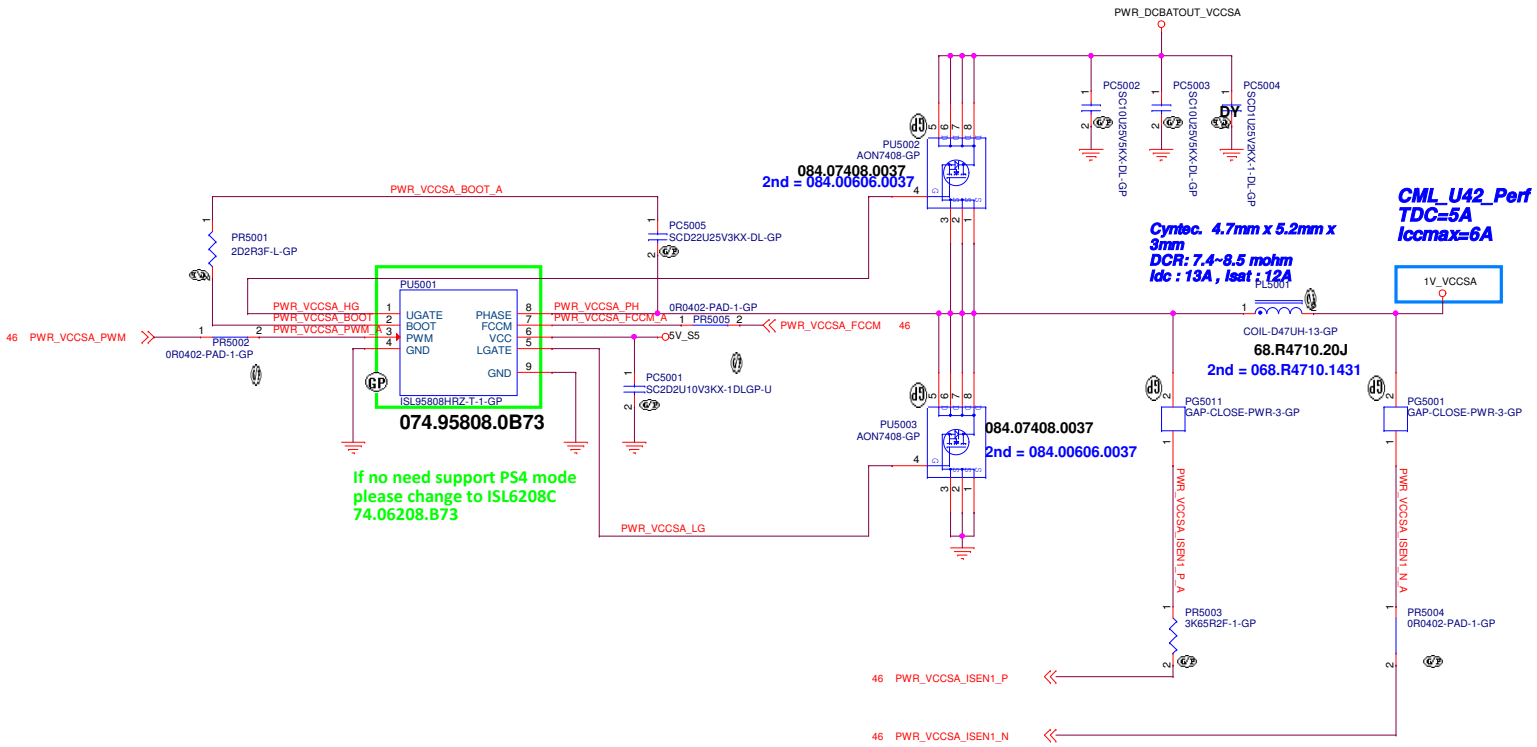
OFFPAGE

DCBATOUT — PG5002 GAP-CLOSE-PWR-3-GP — PWR_DCBATOUT_VCCSA

PG5003 GAP-CLOSE-PWR-3-GP

Main Func = CPU_CORE



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Title	VCCSA	
Size: Custom	Document Number: Jedi15"/17" CML	Rev: A00
Date: Monday, June 10, 2019	Sheet 50 of 106	

Main Func = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

40 VDDQ_PWRGD — EE needs check it!!

51 PWR_2D5V_PG — EE needs check it!!

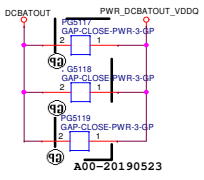
17,27,40,71 PM_SLP_S3#

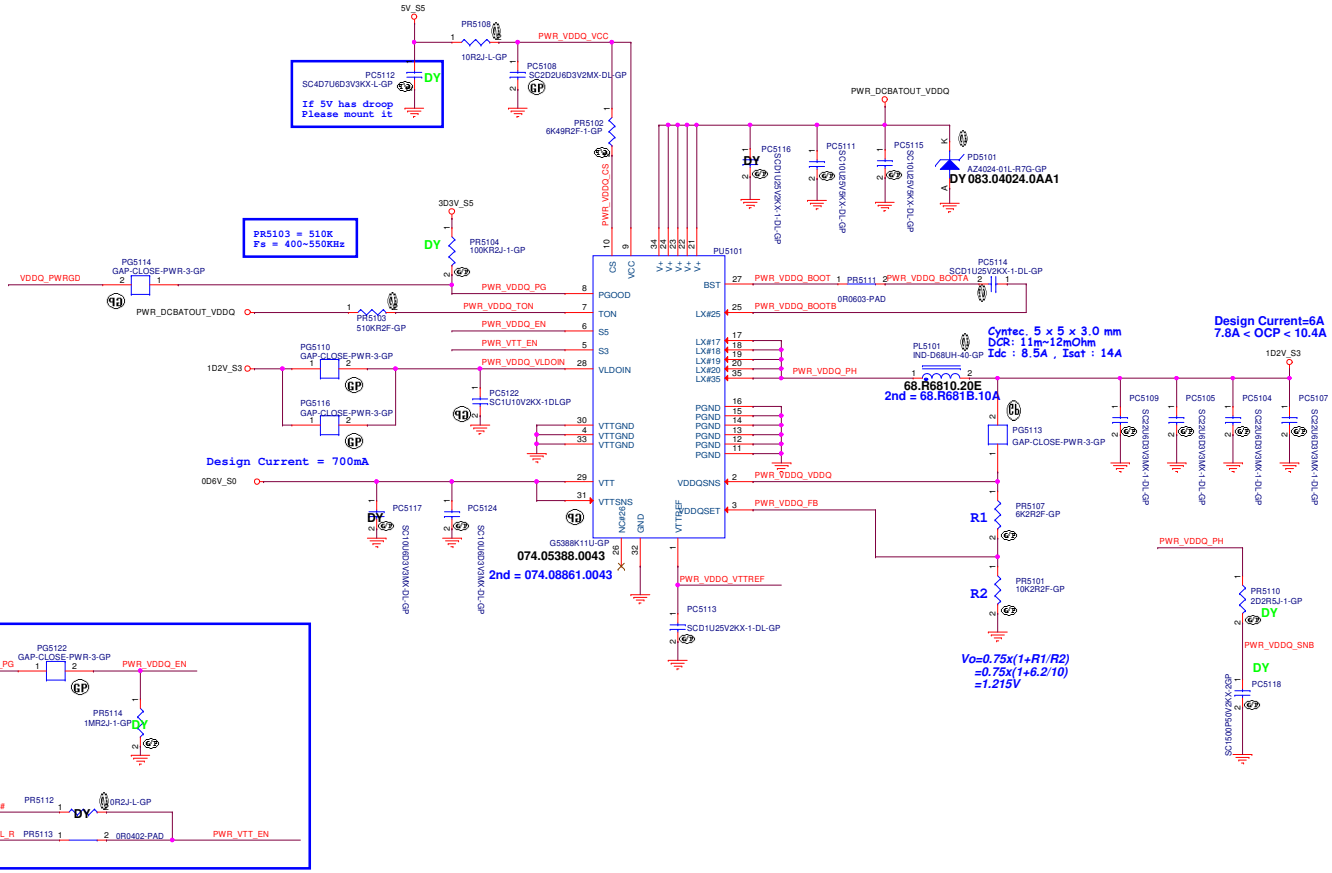
5 SM_PGCNTL_R

51 PWR_2D5V_PG

17,40,66 PM_SLP_S4#

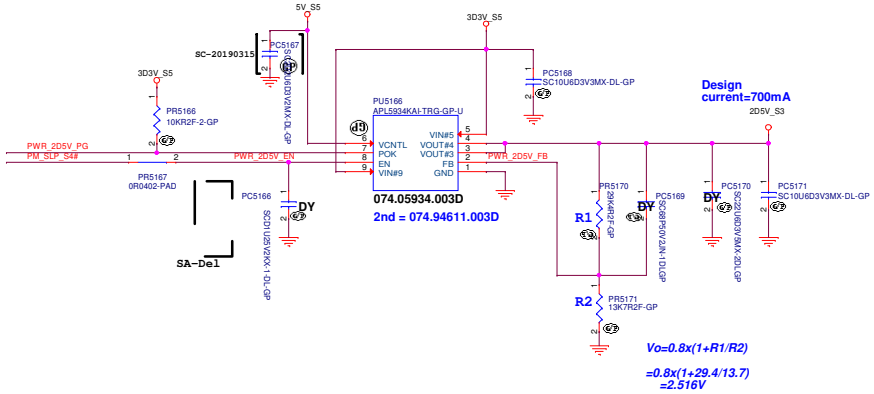
OFFPAGE-GAP





Enable

APL5934 for 2D5V



Jedi15"/17" CML

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Title: Power_(5388_VDDQ/VTT)

Size	Document Number	Rev
A2	Jedi15"/17" CML	A00

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Main Func = PWR.Plane.Regulator_1D0V

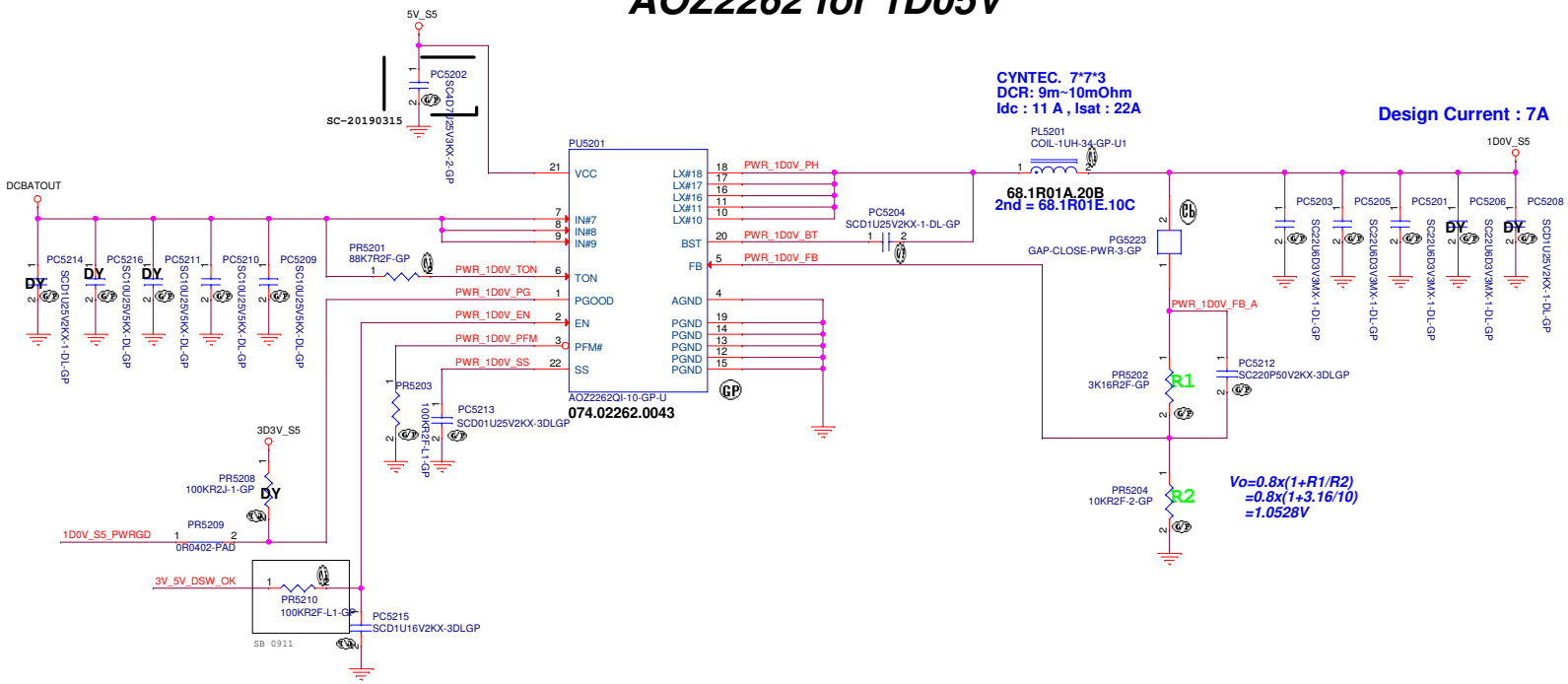
OFFPAGE-Signal

40 1D0V_S5_PWRGD

25,53 3V_5V_DSW_OK

OFFPAGE-GAP

AOZ2262 for 1D05V



Jedi15"/17" CML

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Title: (Reserved)

Size	Document Number	Rev
Custom	Jedi15"/17" CML	A00

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Main Func = 1D8V

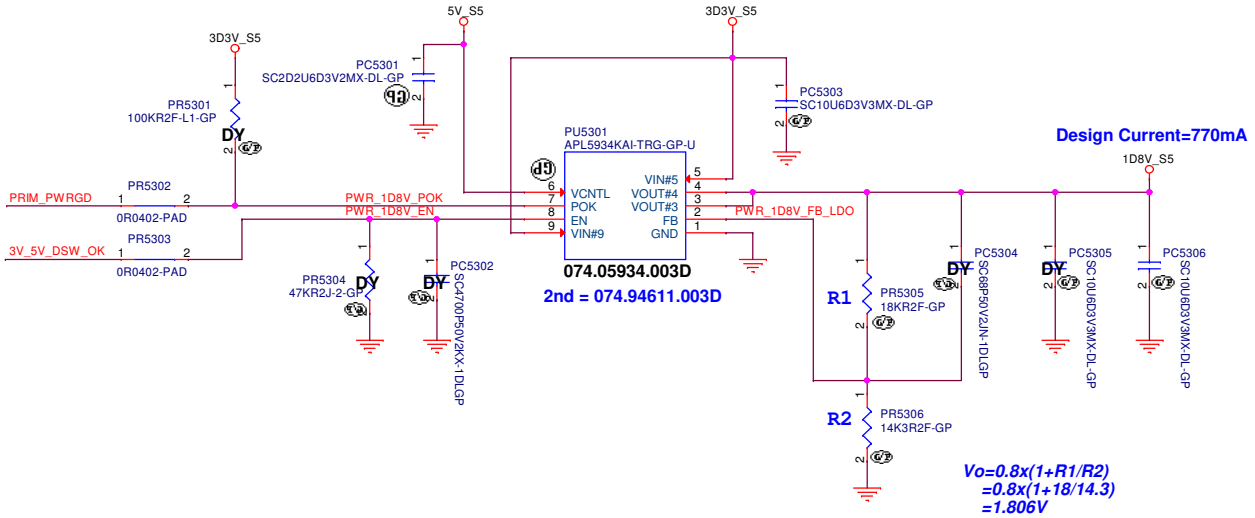
OFFPAGE-Signal

24,40 PRIM_PWRGD

25,52 3V_5V_DSW_OK

OFFPAGE-GAP

APL5934 for 1D8V_S5



Jedi15"/17" CML

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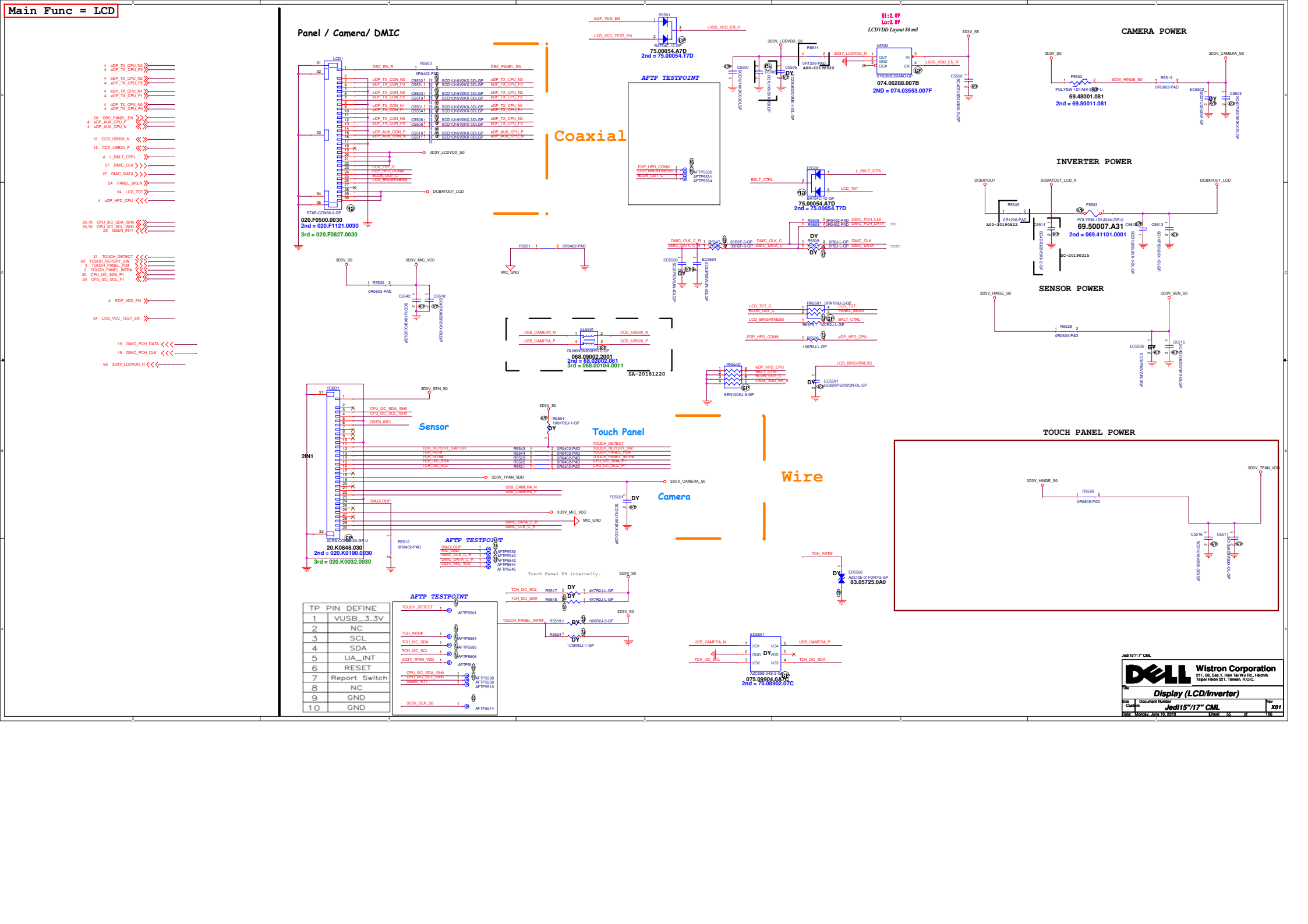
Title: *(Reserved)*

Size	Document Number	Rev
A3	*Jedi15"/17" CML*	*A00*

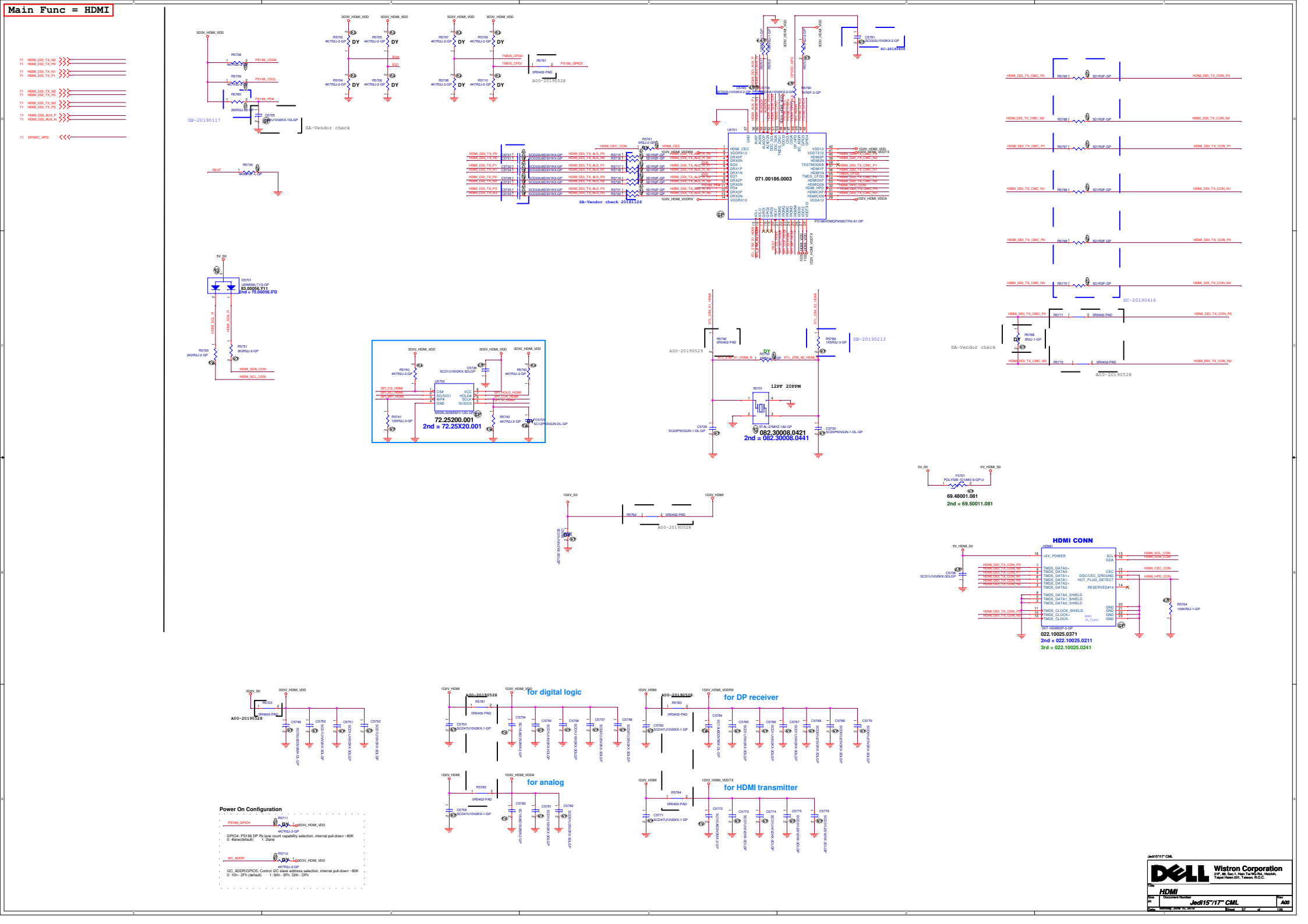
Date: Monday, June 10, 2019 Sheet 53 of 106

Main Func = LCD

Panel / Camera/ DMIC



Main Func = HDMI



Jedi15"/17" CML

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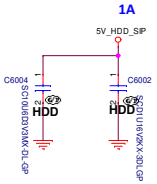
Title: HDMI

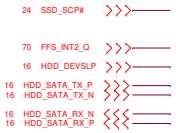
Size	Document Number	Rev
A3	Jedi15"/17" CML	A00

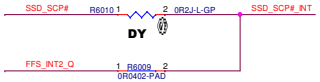
Date: Monday, June 10, 2019 Sheet 57 of 105

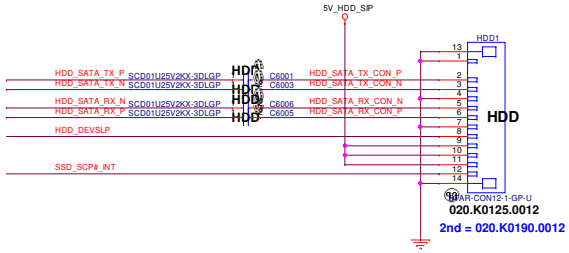
Main Func = HDD



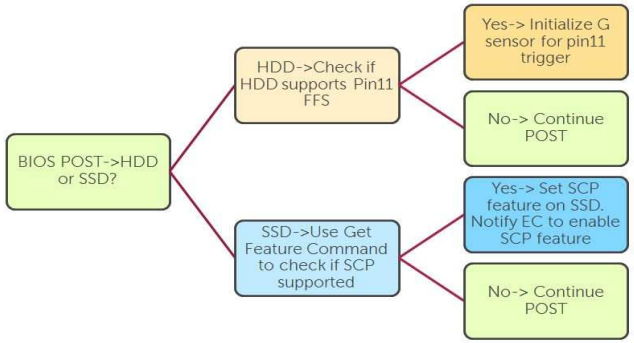
SATA HDD Connector

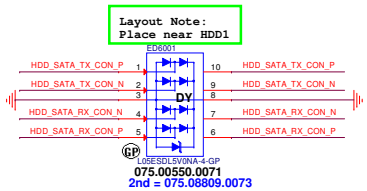






- BIOS today already check whether the device is HDD and whether it supports FFS before enabling sensor chip to trigger pin11. The plan is to add a check on the SSD path to decide if device supports SCP and notify EC whether to support SCP.





Jedi15"/17" CML

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Title: *INT IO (HDD/ODD)*

Size: A2 | Document Number: Jedi15"/17" CML | Rev: X01

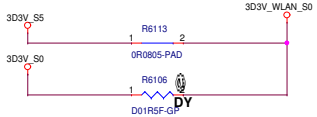
Date: Monday, June 10, 2019 | Sheet 60 of 106

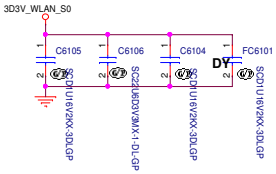
Main Func = WLAN

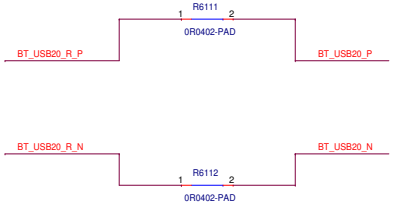
3.3 Peak current consumption

Table 3-4 Peak current consumption

Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply	1360	



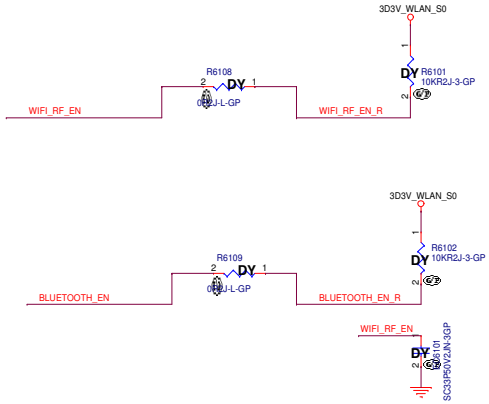


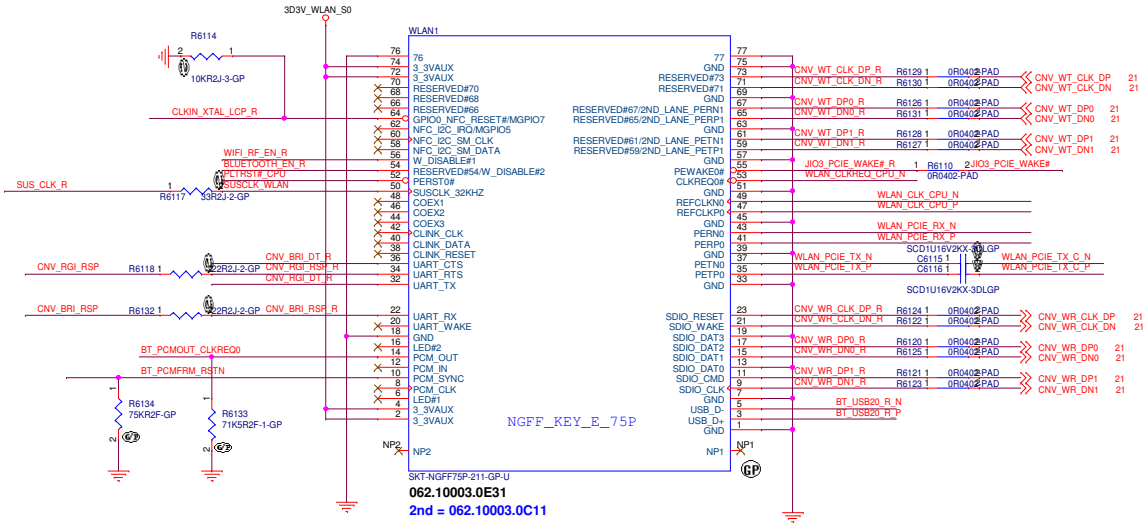


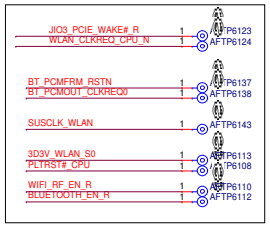
16 BT_USB20_P
16 BT_USB20_N

21 WIFI_RF_EN
16 WLAN_PCIE_TX_C_N
16 WLAN_PCIE_TX_C_P
17,26,63,66,71,76,91 PLTRST# CPU
21 BLUETOOTH_EN
18 WLAN_CLKREQ_CPU_N
18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P
18 CLKIN_XTAL_LCP_R
19 BT_PCMOUT_CLKREQ0
19 BT_PCMFRM_RSTN
18 JIO3_PCIE_WAKE#

18 SUS_CLK_R
20 CNV_RGI_RSP
20 CNV_BRI_RSP
20 CNV_BRI_DT_R
15,20 CNV_RGI_DT_R







Jedi15"/17" CML

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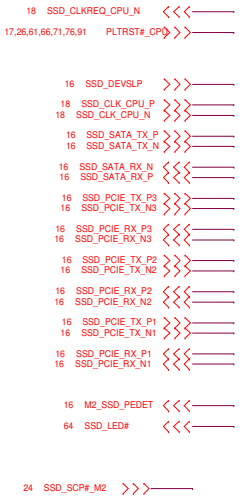
Title: **INT IO (WLAN M.2)**

Size	Document Number	Rev
Custom	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 61 of 106

Main Func = SSD M.2



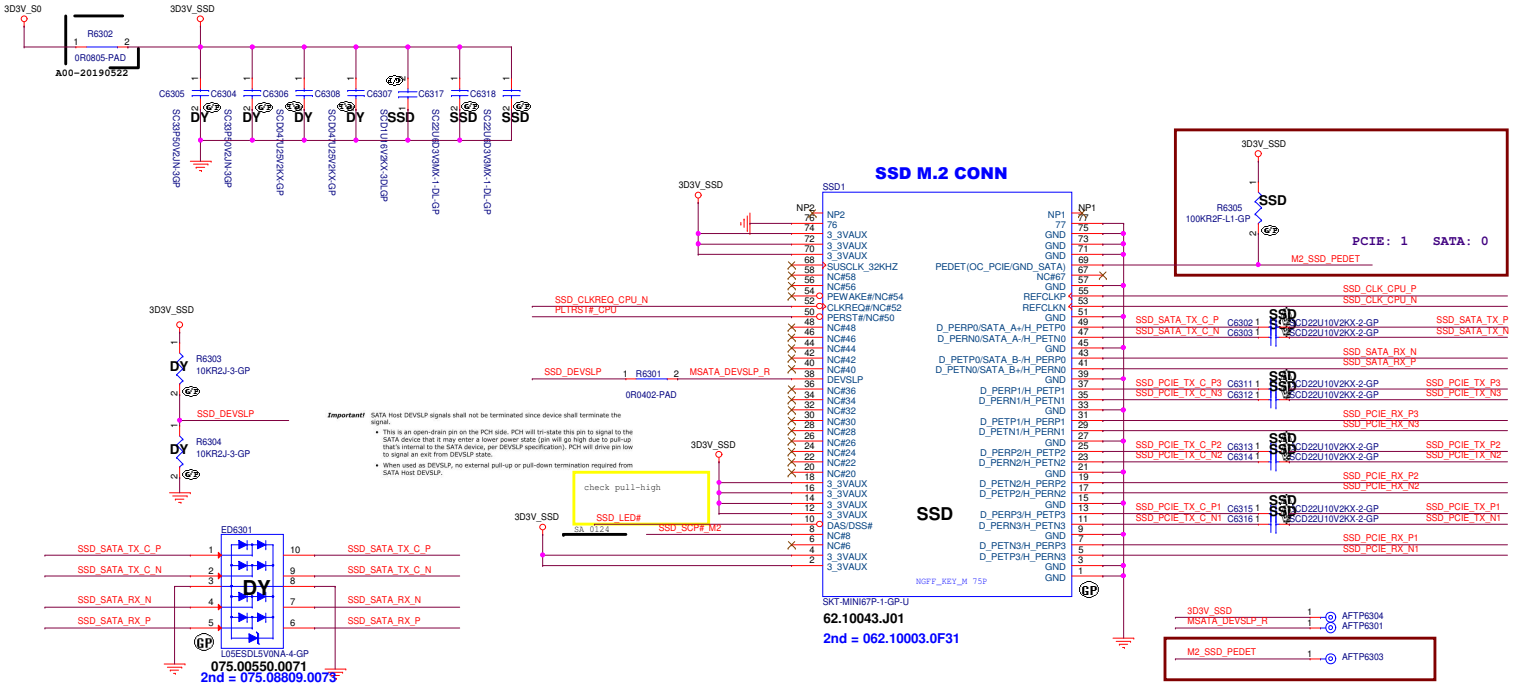


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)

Size	Document Number	Rev
Custom	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 63 of 106

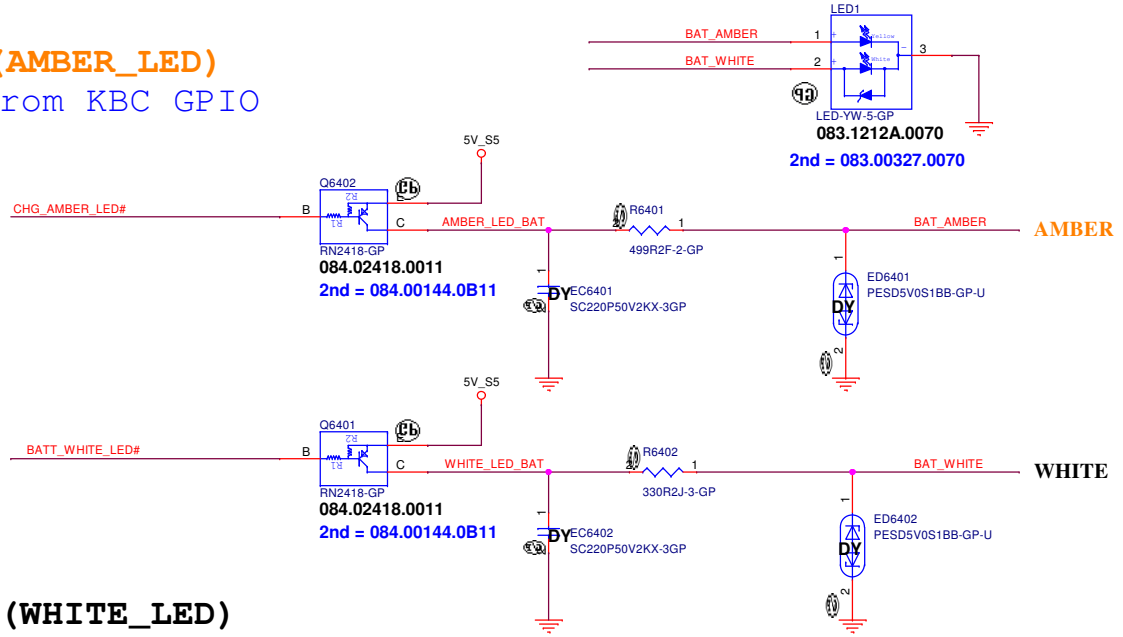
Main Func = Power BTN

24,90 CHG_AMBER_LED#

24 BATT_WHITE_LED#

Battery LED1 (AMBER_LED)

Low actived from KBC GPIO



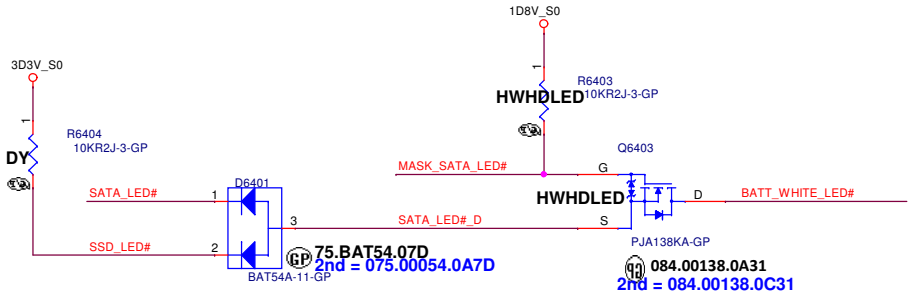
Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

16 SATA_LED#

63 SSD_LED#

24 MASK_SATA_LED#



Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size	Document Number	Rev
A3	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 64 of 106

Main Func = Keyboard

24 KSI[0..7]
24 KSO[0..16]

24 PTP_DIS#
3,24 TP_WAKE_KBC#
24 CLK_TP_SIO
24 DAT_TP_SIO
20,66 CPU_I2C_SCL_P0
20,66 CPU_I2C_SDA_P0
19 KB_LED_BL_DET
20 KB_DET#
24 KB_LED_PWM
24 CAP_LED#_R

AFTP TESTPOINT

5V_KB_BL 1 — AFTP6529
KB_BL_CTRL# 1 — AFTP6530
KB_LED_DET_C 1 — AFTP6538

KB Backlight Power Consumption: 285mA max.

5V_S0 — F6501 POLYSW-1D1A6V-9GP — 5V_KB_BL
C6501 SCD1U16V2KX-3DLGP
69.48001.081
2nd = 69.50011.081
KBBL

5V_KB_BL — KBBL1 ACES-CON4-83-GP
KB_LED_DET_C
KB_BL_CTRL#
020.K0206.0004
2nd = 020.K0345.0004

AFTP6567 — KB_DET# — KB1 ACES-CON30-29-GP
KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0
KSO5 KSO4 KSO7 KSO6 KSO8 KSO3 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10
CAP_LED — AFTP6541
020.K0254.0030
2nd = 20.K0750.030
3rd = 020.K0274.0030

KB_BL_CTRL# — KBBL — Q6501 PJA3402-R1-00001-GP — KB_LED_PWM
R6529 100KR2J-1-GP
084.03402.0031
2nd = 084.02306.0031

KB_LED_BL_DET — R6507 KBBL 51KR2J-1-GP — KB_LED_DET_C
R6508 KBBL 100KR2J-1-GP

CAP LED Control
LOW actived from KBC GPIO

CAP_LED#_R — Q6505 RN2418-GP — 5V_S5
CAP_LED_Q — R6513 — CAP_LED 1KR2J-1-GP
CAP_LED_Q — EC6507 SCS1U50V2KX-4GP
084.02418.0011
2nd = 084.00144.0B11

Main Func = TPAD

3D3V_S0 — R6502 0R0603-PAD — 3D3V_TP_VDD

3D3V_TP_VDD — RN6501 SRN10KJ-5-GP
CLK_TP_SIO — R6514 0R0402-PAD
DAT_TP_SIO — R6515 0R0402-PAD
CPU_I2C_SCL_P0 — R6505 0R0402-PAD — I2C0_SCL_R
CPU_I2C_SDA_P0 — R6506 0R0402-PAD — I2C0_SDA_R
A00-201990528
EC6502 SCS1U50V2KX-4GP
EC6503 SCS1U50V2KX-4GP

EC I2C
CPU I2C

3D3V_TP_VDD — C6505 SCD1U16V2KX-3DLGP
I2C0_SDA_R
I2C0_SCL_R
TP_WAKE_KBC#
PTP_DIS#
TP1 PTWO-CON8-16-GP
AFTP6540
020.K0255.0008
2nd = 020.K0151.0008

AFTP TESTPOINT

3D3V_TP_VDD — AFTP6531
I2C0_SCL_R — AFTP6534
I2C0_SDA_R — AFTP6535
TP_WAKE_KBC# — AFTP6536
PTP_DIS# — AFTP6537

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

5V_S0 — R6510 0R2J-L-GP — 3D3V_TP_VDD
RN6603 SRN2K2J-5-GP
Q6204_G
Q6504 2N7002KDW-1-GP
CPU_I2C_SCL_P0 — I2C0_SCL_R
CPU_I2C_SDA_P0 — I2C0_SDA_R
75.27002.F7C
2nd = 075.27002.0E7C

3D3V_TP_VDD — R6511 10KR2J-3-GP — TP_WAKE_KBC#

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)
Size: Custom | Document Number: Jedi15"/17" CML | Rev: X01
Date: Monday, June 10, 2019 | Sheet 65 of 105

Main Func = IO Connector

20,24,69 LID_CL_SIO#

24,90 KBC_PWRBTN#
17,26,61,63,71,76,91 PLTRST#_CPU
16 USB2_USB20_P
16 USB2_USB20_N
16 USB1_USB20_P
16 USB1_USB20_N

16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P

16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P

17,40,51 PM_SLP_S4#

20,24,69 LID_CL_SIO_TAB#

24 NC_U3_PD#_EC

24 FPR_SCAN#
24 USB_EN#
16 USB_OC1#

16 FP1_USB20_N
16 FP1_USB20_P

27,66 AUD_SENSE

27,29,66 RING2
27,29,66 RING2
27,29,66 RING2
27,29,66 RING2
27,29,66 SLEEVE
27,29,66 SLEEVE
27,29,66 SLEEVE
27,29,66 SLEEVE
29,66 AUD_HP1_JACK_R1
29,66 AUD_HP1_JACK_L1

20,65 CPU_I2C_SDA_P0
20,65 CPU_I2C_SCL_P0

44 PWR_CHG_CSOP_R
44 PWR_CHG_CSON_R

55 3D3V_LCDVDD_R

JOBD1

STAR-CON50-3-GP
020.F1405.0050
2nd = 020.F0285.0050

AFTP TESTPOINT

AFTP6603 AFTP6604 AFTP6605 AFTP6606
AFTP6609 AFTP6610
AFTP6619 AFTP6620 AFTP6621 AFTP6622 AFTP6623 AFTP6624 AFTP6625
AFTP6626 AFTP6627 AFTP6628 AFTP6629 AFTP6630
AFTP6633 AFTP6634
AFTP6635 AFTP6636
AFTP6637 AFTP6638
AFTP6639 AFTP6640

3D3V_S5
R6615 100KR2J-1-GP
LID_CL_SIO_TAB#

KBC_PWRBTN# PLTRST#_CPU
ED6602 ED6603
SC339P50V2JN-3GP

AFTP TESTPOINT
AFTP6601 AFTP6602

FP1_USB20_P FP1_USB20_N
ED6608 ED6607
AZ5725-01FDR7G-GP

USB2_USB20_P USB2_USB20_N
ED6605 ED6606
AZ5725-01FDR7G-GP

E3
HRS-CONN20A-2-GP
20.F1450.020

IN1+ IN1− IN2+ IN2− IN7− IN7+ IN8− IN8+
IN4+ IN4− IN3+ IN3− IN6− IN6+ IN5− IN5+
LCD BACKLIGHT
Panel logic power
CPU Core input
System power source

ED6602
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

ED6604
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

USB1_USB20_P USB1_USB20_N
ED6609 ED6610
AZ5725-01FDR7G-GP

Jedi15"/17" CML

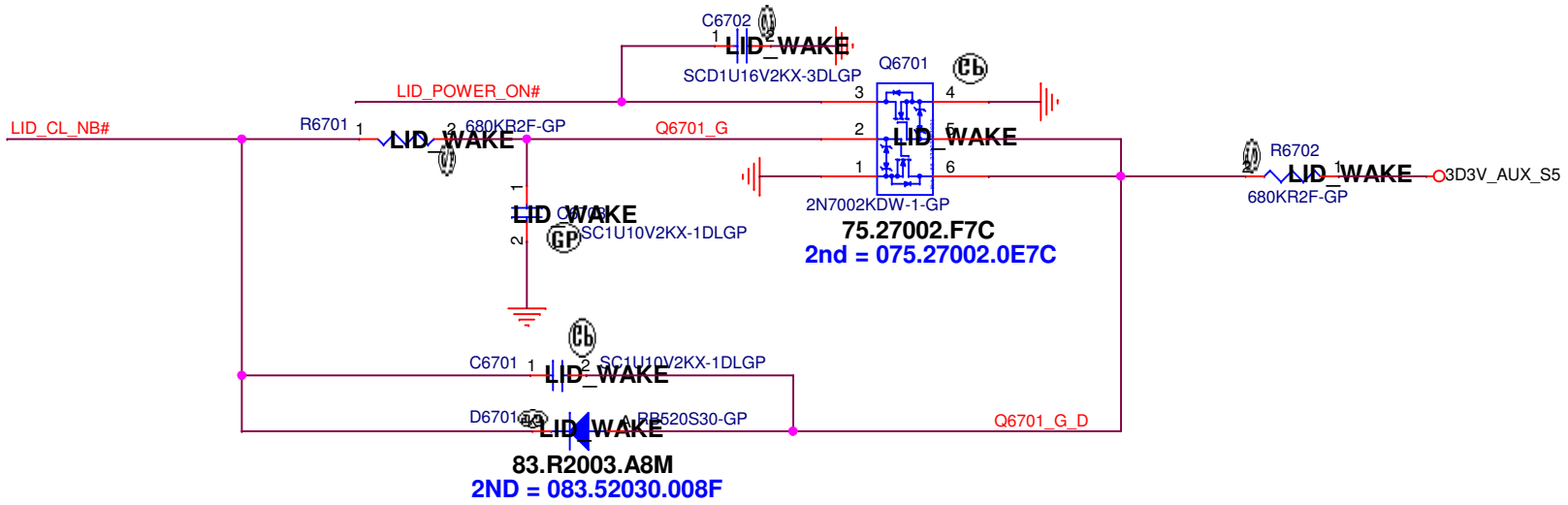
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Tapei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A2
Document Number: Jedi15"/17" CML
Rev: A00
Date: Monday, June 10, 2019
Sheet 66 of 106

Main Func = HALL SENSOR

69 LID_CL_NB#

24 LID_POWER_ON#



Jedi15"/17" CML

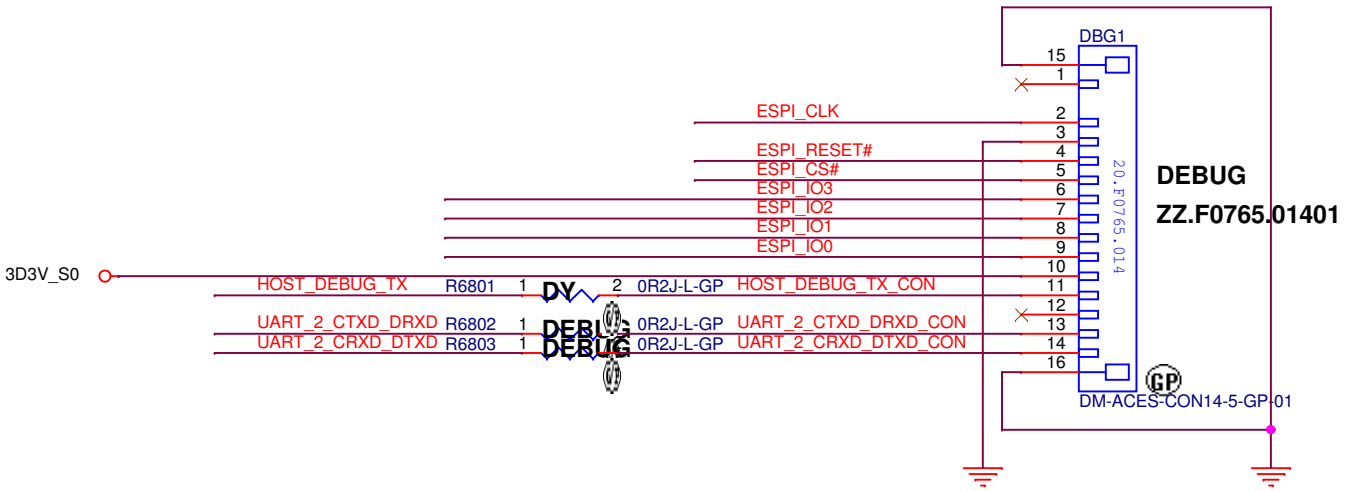
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Lid_Wake*		
Size: A4	Document Number: *Jedi15"/17" CML*	Rev: *A00*
Date: Monday, June 10, 2019	Sheet 67 of 106	

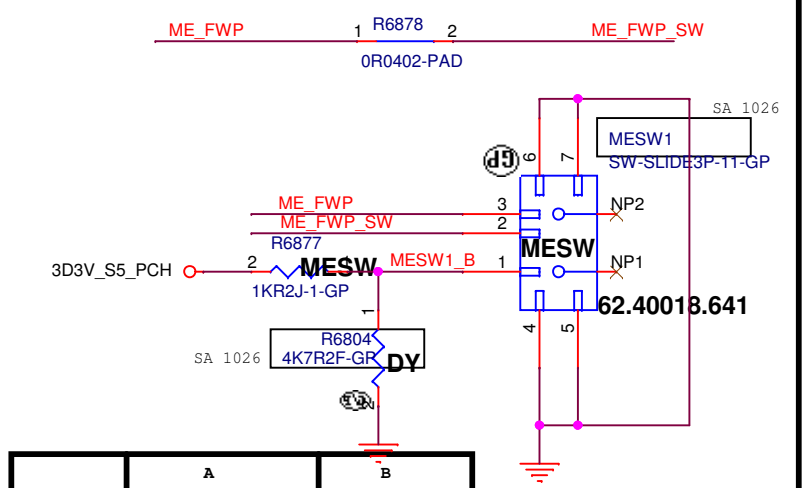
Main Func = Debug

24 HOST_DEBUG_TX
20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD
18,24 ESPI_CLK
18,24 ESPI_RESET#
18,24 ESPI_CS#
18,24 ESPI_IO[3..0]
24 ME_FWP
19 ME_FWP_SW

Debug Connector



Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug (LPC debug)*

Size	Document Number	Rev
A4	*Jedi15"/17" CML*	*X01*

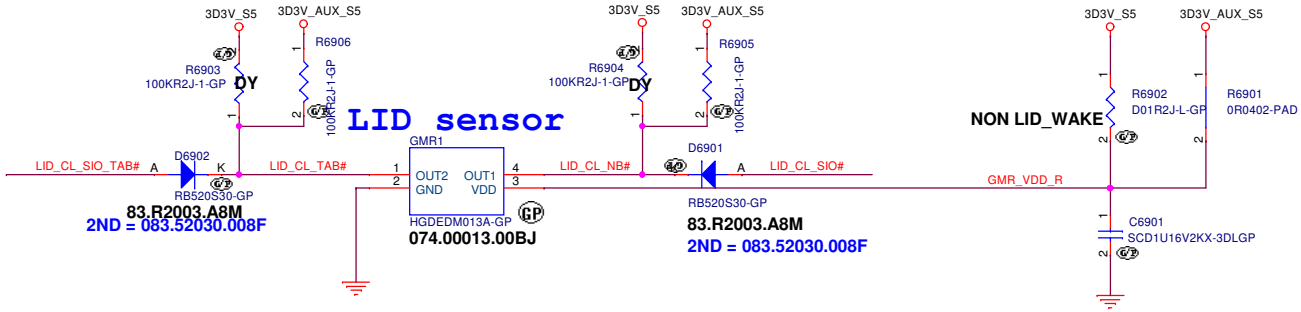
Date: Monday, June 10, 2019 Sheet 68 of 106

Main FUNC = GMR

20,24,66 LID_CL_SIO#

20,24,66 LID_CL_SIO_TAB#

67 LID_CL_NB#



Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

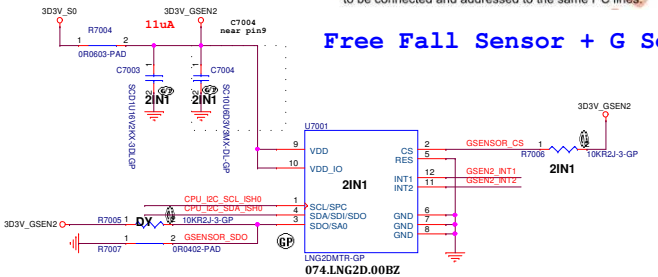
Title		
Sensor (RSVD)		
Size: A3	Document Number: Jedi15"/17" CML	Rev: X01
Date: Monday, June 10, 2019	Sheet 69 of 106	

Main Func = Free Fall Sensor

20,55 CPU_I2C_SCL_ISH0
20,55 CPU_I2C_SDA_ISH0
20 GSEN2_INT1
18 FFS_INT1
20 FFS_INT2
60 FFS_INT2_Q

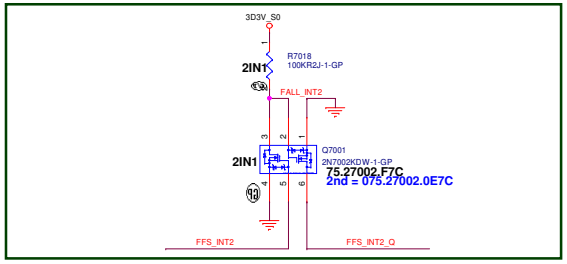
The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U7001



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor (G-sensor)
Size: A2
Document Number: Jedi15"/17" CML
Rev: X01
Date: Monday, June 10, 2019
Sheet 70 of 106

Main Func = TypeC

USB1

MISC & DEBUG

PCIe

DP TBT PORTS

700mA

100mA

GND

Pin E8

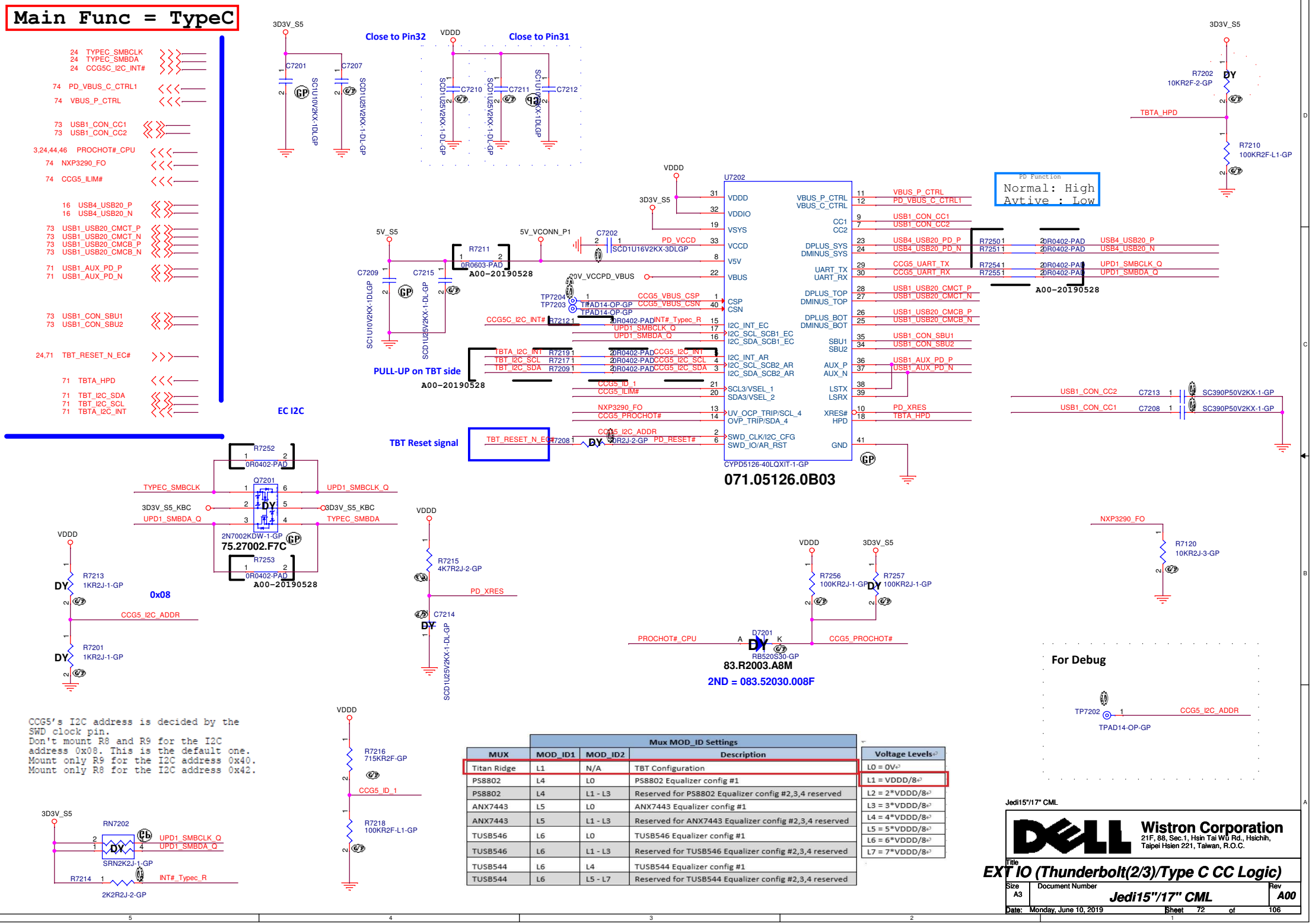
keep traces as short as possible.

SA-for intel review 1123

SA-for intel review 1126

Jedi15"/17" CML	
Wistron Corporation	
EXT IO (Thunderbolt(1/3)/Type C Re-driver)	
Size: A1	Document Number: Jedi15"/17" CML
Rev: A00	
Date: Monday, June 10, 2019	Sheet 71 of 106

Main Func = TypeC



Mux MOD_ID Settings			
MUX	MOD_ID1	MOD_ID2	Description
Titan Ridge	L1	N/A	TBT Configuration
PS8802	L4	L0	PS8802 Equalizer config #1
PS8802	L4	L1 - L3	Reserved for PS8802 Equalizer config #2,3,4 reserved
ANX7443	L5	L0	ANX7443 Equalizer config #1
ANX7443	L5	L1 - L3	Reserved for ANX7443 Equalizer config #2,3,4 reserved
TUSB546	L6	L0	TUSB546 Equalizer config #1
TUSB546	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved
TUSB544	L6	L4	TUSB544 Equalizer config #1
TUSB544	L6	L5 - L7	Reserved for TUSB544 Equalizer config #2,3,4 reserved

Voltage Levels
L0 = 0V
L1 = VDDD/8
L2 = 2*VDDD/8
L3 = 3*VDDD/8
L4 = 4*VDDD/8
L5 = 5*VDDD/8
L6 = 6*VDDD/8
L7 = 7*VDDD/8

Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size	Document Number	Rev
A3	Jedi15"/17" CML	A00

Date: Monday, June 10, 2019 Sheet 72 of 106

Main Func = TypeC

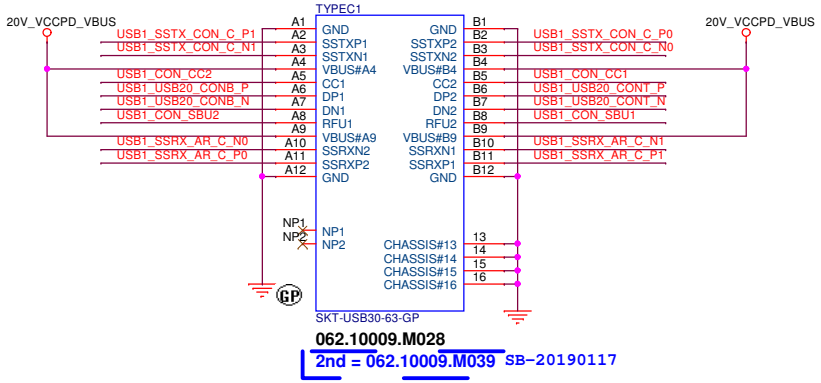
USB1

71 USB1_SSTX_CON_P0
71 USB1_SSTX_CON_N0
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N1
71 USB1_SSRX_AR_P0
71 USB1_SSRX_AR_N0
71 USB1_SSRX_AR_P1
71 USB1_SSRX_AR_N1

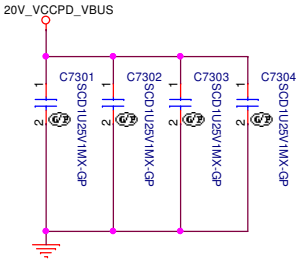
72 USB1_USB20_CMCT_P
72 USB1_USB20_CMCT_N
72 USB1_USB20_CMCB_P
72 USB1_USB20_CMCB_N

72 USB1_CON_CC1
72 USB1_CON_CC2

72 USB1_CON_SBU1
72 USB1_CON_SBU2

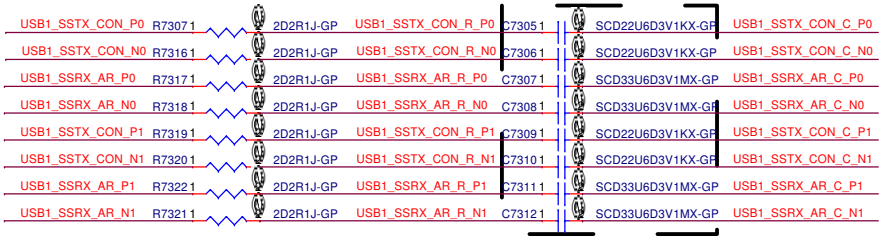


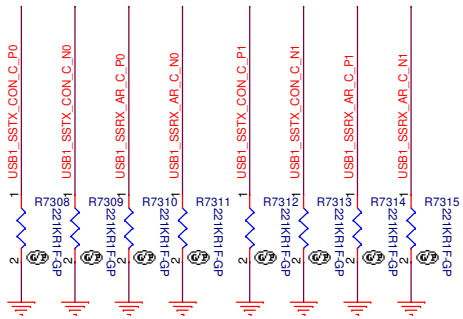
062.10009.M028
2nd = 062.10009.M039 SB-20190117

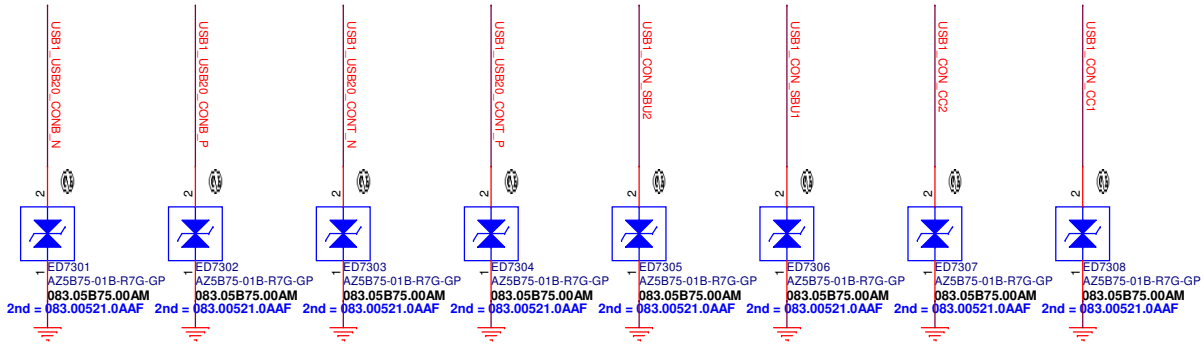


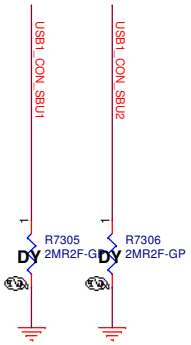
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0011

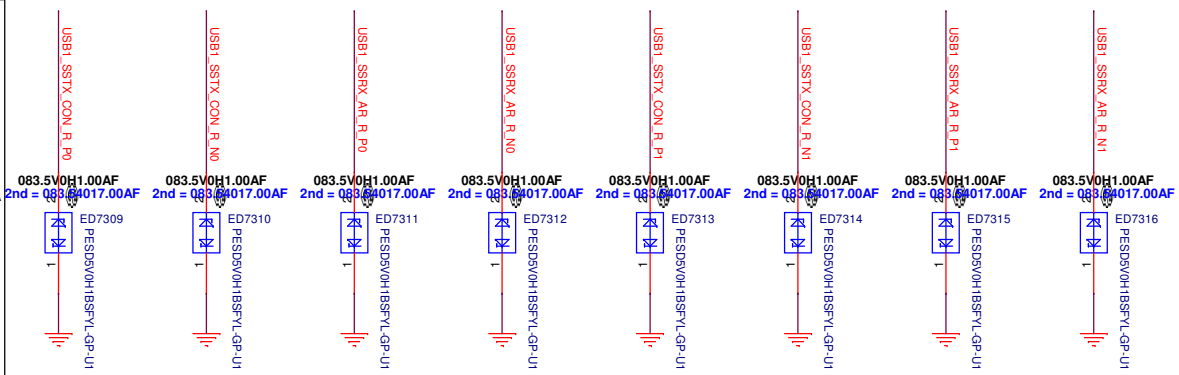
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0011











Jedi15"/17" CML

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size	Document Number	Rev
A3	Jedi15"/17" CML	A00

Date: Monday, June 10, 2019 Sheet 73 of 106

Main FUNC = LPS

CCG5_ILIM#	ILIM
0	1.5A
1	3.3A

72 PD_VBUS_C_CTRL1
72 VBUS_P_CTRL
72 CCG5_ILIM#
44 VCCPD_VBUS_ACK
72 NXP3290_FO
24 TYPEC_DCIN1_EN#

3D3V_S5
R7409 100KR2J-1-GP
VBUS_P_CTRL_Q
Q7409 2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0N31
R7405 100KR2J-1-GP
VBUS_P_CTRL

Form PD control

5V_S5
C7403 SC22U6D3V3MX-1-DL-GP
C7404 SC22U6D3V3MX-1-DL-GP
20V_VCCPD_VBUS
U7403
VBUS#C2 VBUS#D1 VBUS#D2 CAP GND GND GND
VIN#A1 VIN#A2 VCP#B1 VCP#B2 VCP#C1 ILIM EN FO FLT#
NX5P3363UKZ-1GP
074.53363.M001
C7405 SC1U10V2KX-1DLGP
NXP3290CAP
VCP_VBUS
D7401 A K SS3040HE-GP
083.03040.008H
2nd = 083.00330.008H
3rd = 083.00330.0A8H
SB-20190118
NXP3363_ILIM
VBUS_P_CTRL_Q
NXP3290_FO
FLT_NXP3290
R7402 10KR2F-2-GP
R7414 47KR2J-2-GP
3D3V_S5
R7433 24K3R2F-1-GP
R7418 14K3R2F-GP
NXP3363_ILIM_R
Q7411 2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0N31
VDDD
R7434 100KR2J-1-GP
CCG5_ILIM#
R7435 100KR2J-1-GP

layout note:
close to U7419

USB_ADT
U7418 AON7403-GP-U
84.07403.037
2nd = 084.21321.0037
3rd = 084.03307.0037
+SDC_IN
C7401 SC1500P50V2KX-2-DL-GP
R7407 1MR2F-GP
Q7401 PJA3415-GP
084.03415.0031
2nd = 084.02421.0031
3rd = 084.02305.0B31
R7406 100KR2F-L1-GP
R7432 1MR2F-GP
R7403 0R0402-PAD
A00-20190528
LPS_SW_R
LPS_SW_D
R7401 200KR2F-L-GP
R7408 100KR2F-L1-GP
Q7406 PJT138KA-GP
075.00138.0A7C
2nd = 075.00138.0F7C
3rd = 075.00139.007C

3D3V_S5
R7424 100KR2F-L1-GP
VCCPD_VBUS_ACK
U7419 NX20P5090UK-GP
074.20509.007Z
VBUS ACK EN# OVLO VINT GND

Form EC (CY18 add)
Default: High
Avtive : Low
RO13 Shauchi

3D3V_S5
R7427 100KR2F-L1-GP
PD_VBUS_C_EN_B
R7422 1MR2F-GP
TYPEC_DCIN1_EN#
Q7407 PJT138KA-GP
075.00138.0A7C
2nd = 075.00138.0F7C
3rd = 075.00139.007C
R7431 200KR2F-L-GP
R7428 100KR2F-L1-GP

20V_VCCPD_VBUS
R7425 100KR2F-L1-GP
PD_VBUS_C_EN_A
PD_VBUS_C_CTRL1_Q
PD_VBUS_C_CTRL1_R
Q7405 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
VBUS Detect
R7426 100KR2F-L1-GP
R7429 200KR2F-L-GP

3D3V_S5
R7411 100KR2J-1-GP
PD_VBUS_C_CTRL1_Q
Q7410 2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0N31
R7412 100KR2J-1-GP
Device Detect
PD_VBUS_C_CTRL1_A
VBUS_P_CTRL_Q
VBUS_P_CTRL_R
Q7404 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
20V_VCCPD_VBUS
R7423 100KR2F-L1-GP
R7430 200KR2F-L-GP

Form PD control
PD_VBUS_C_CTRL1

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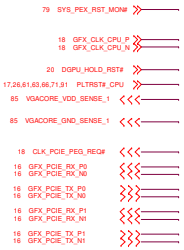
Title: GPU(2/5)DIGITALOUT
Size: Custom | Document Number: Jedi15"/17" CML | Rev: A00
Date: Monday, June 10, 2019 | Sheet 74 of 106

Main Func = dGPU



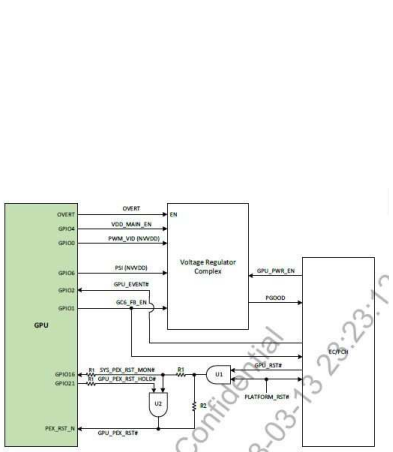


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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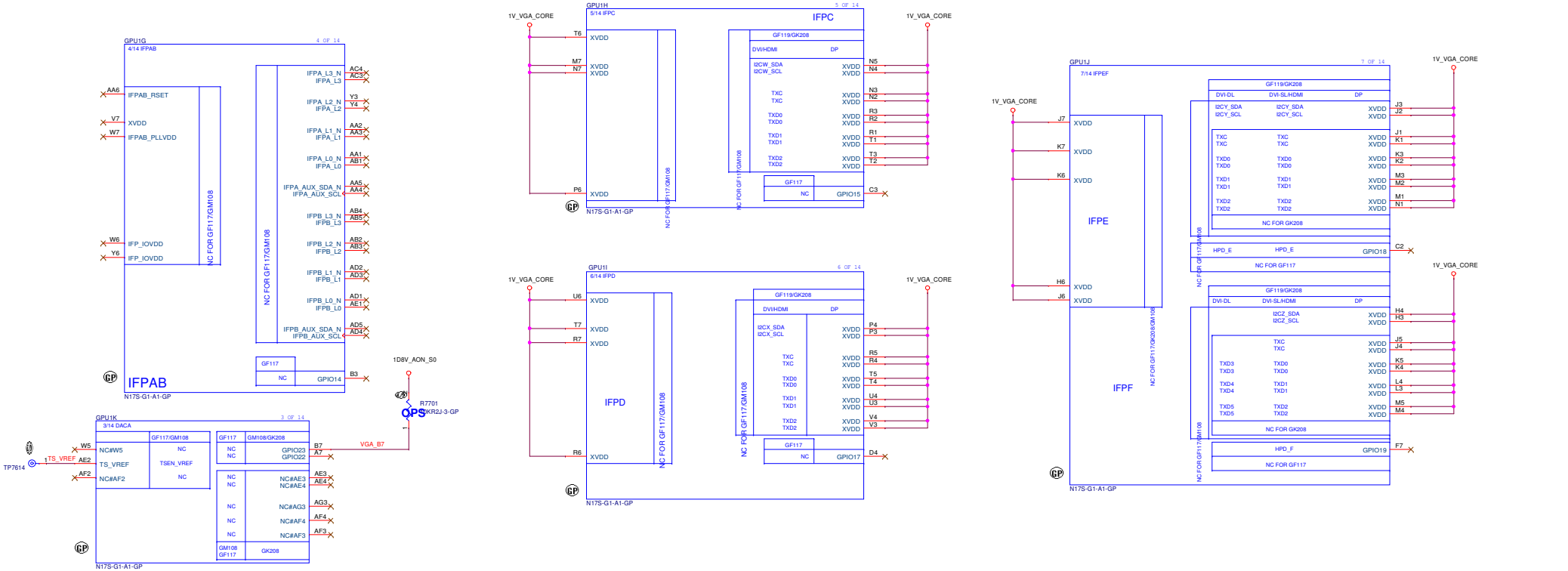
Title: GPU (PEG 1/5)

Size	Document Number	Rev
Custom	Jedi15"/17" CML	X01

Date: Monday, June 10, 2013 Sheet 76 of 100

Main Func = dGPU



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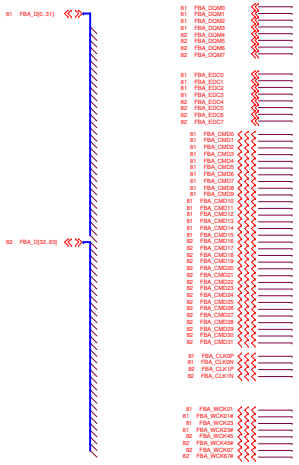
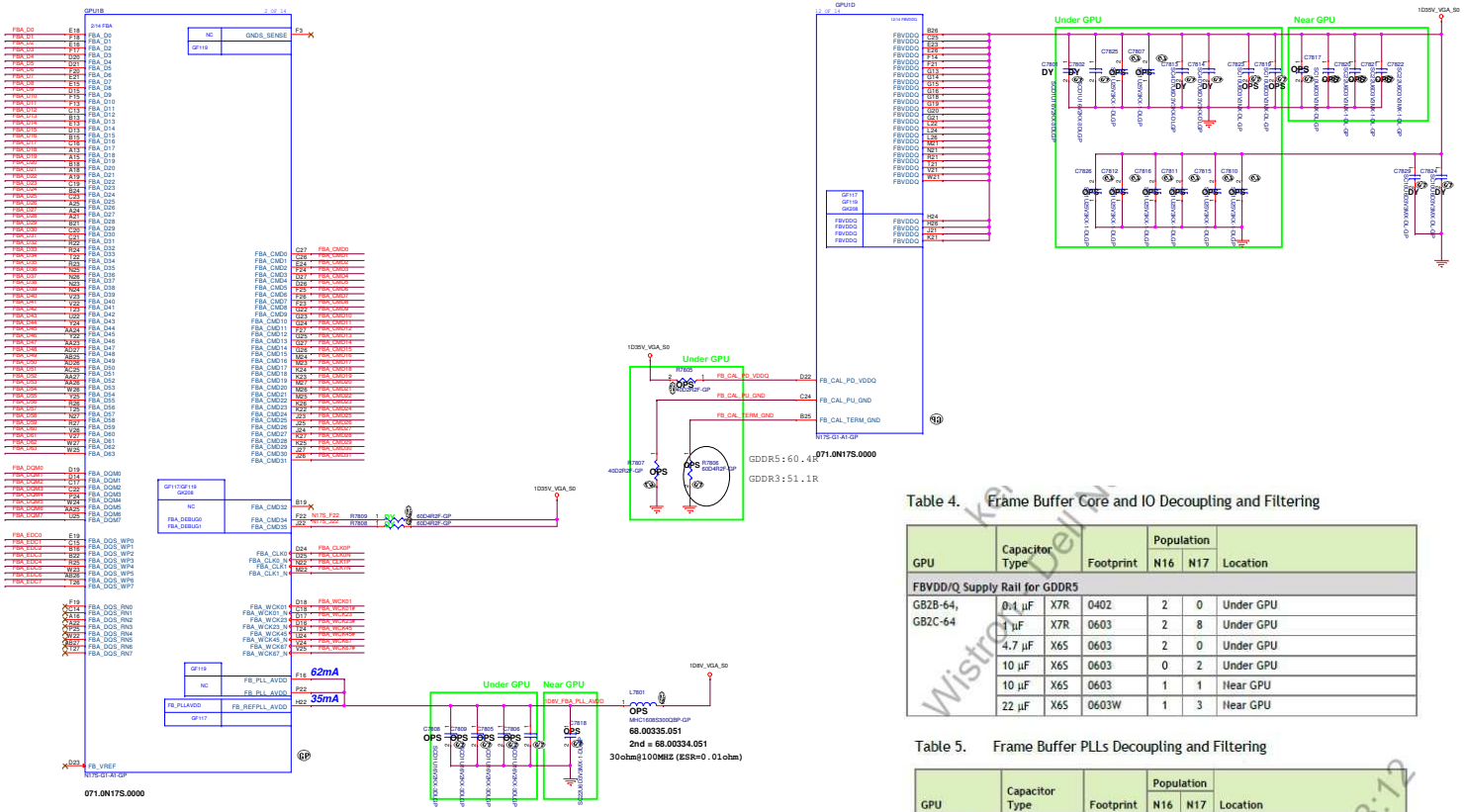
Title: *GPU (DIGITAL 2/5)*

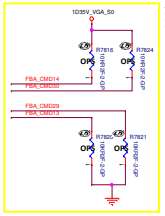
Size	Document Number	Rev
A2	Jedi15"/17" CML	X01

Date: Monday, June 10, 2019 Sheet 77 of 106

Main Func = dGPU







Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type				
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

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Size	Document Number	Rev
A3	Jedi15"/17" CML	X01
Date: Monday, March 31, 2008	Sheet 78 of 96	

Main Func = dGPU

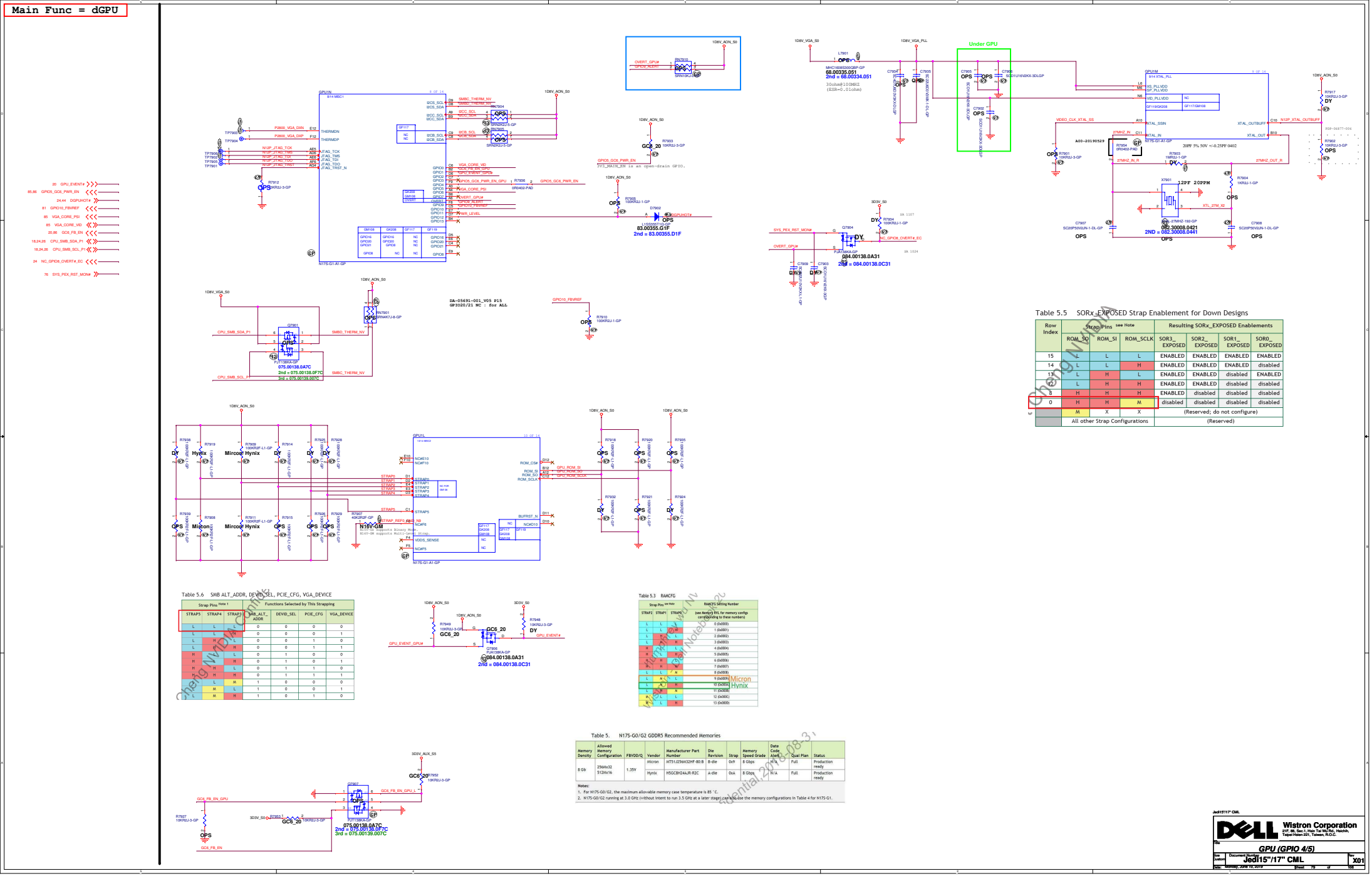

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	M	L	1	0	0	0
L	M	H	1	0	0	1
L	M	H	1	0	1	0

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Strap Number
STRAP2	STRAP1	STRAP0	(see Memory BVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	M	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0xF	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Notes:
1. For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

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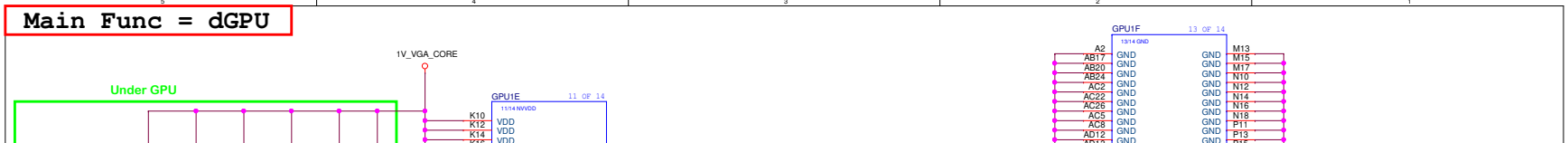
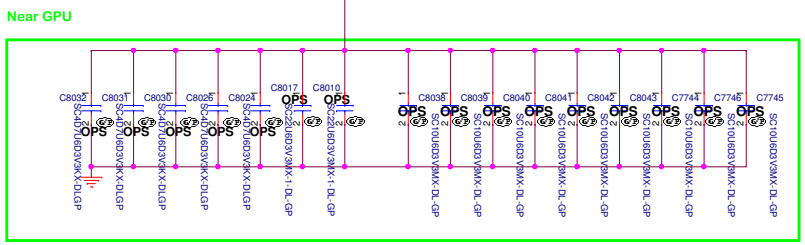
Title: GPU (GPIO 4/5)

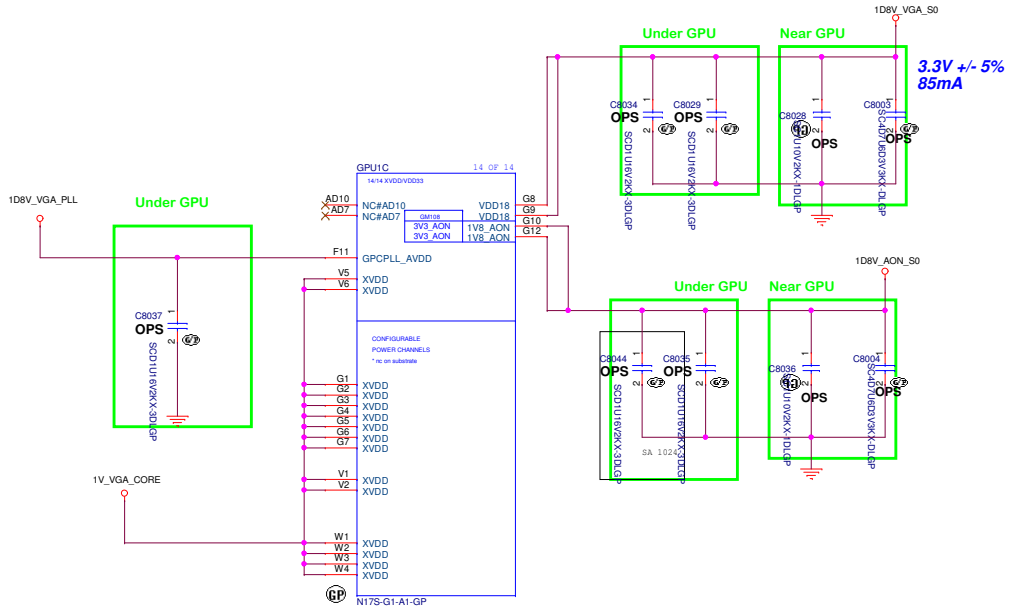
Size: Custom | Document Number: Jed15"/17" CML | Rev: X01

Date: Monday, June 10, 2013 | Sheet 79 of 100

Main Func = dGPU







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Title: *GPU (PWR/GND 5/5)*

Size	Document Number	Rev
Custom	Jedi15"/17" CML	X01

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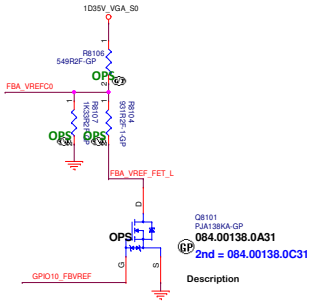
Main FUNC = VRAM

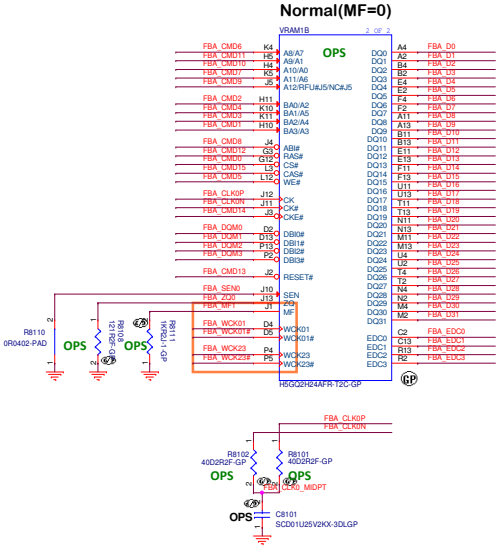
Frame Buffer Patition A-Lower Half



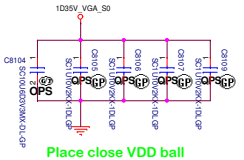
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.675V	High
Termination	70%	0.945V	Low

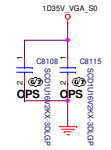
Normal(MF=0)



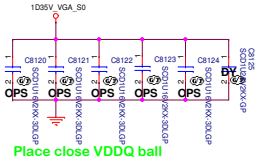
Place close VDD ball



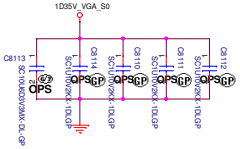
Place close VDD ball



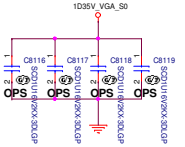
Place close VDD ball



Place close VDDQ ball



Place close VDDQ ball



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Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Jedi15"/17" CML | Rev: A00

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Main FUNC = VRAM

FBA_D[32..63] 78,82

FBA_D[32..63] 78,82

78,82 FBA_CMD22
78,82 FBA_CMD27
78,82 FBA_CMD26
78,82 FBA_CMD23
78,82 FBA_CMD25

78,82 FBA_CMD18
78,82 FBA_CMD20
78,82 FBA_CMD19
78,82 FBA_CMD17

78,82 FBA_CMD24
78,82 FBA_CMD28
78,82 FBA_CMD16
78,82 FBA_CMD31
78,82 FBA_CMD21

78 FBA_CLK1P
78 FBA_CLK1N
78,82 FBA_CMD30

81 FBA_VREFC0

79,81 GPIO10_FBVREF

78,82 FBA_CMD29

FBA_D[32..63] 78,82

FBA_D[32..63] 78,82

78,82 FBA_CMD26
78,82 FBA_CMD23
78,82 FBA_CMD22
78,82 FBA_CMD27
78,82 FBA_CMD25

78,82 FBA_CMD19
78,82 FBA_CMD17
78,82 FBA_CMD18
78,82 FBA_CMD20

78,82 FBA_CMD24
78,82 FBA_CMD31
78,82 FBA_CMD21
78,82 FBA_CMD28
78,82 FBA_CMD16

78,82 FBA_CMD30

78,82 FBA_CMD29

78 FBA_WCK67
78 FBA_WCK67#
78 FBA_WCK45
78 FBA_WCK45#

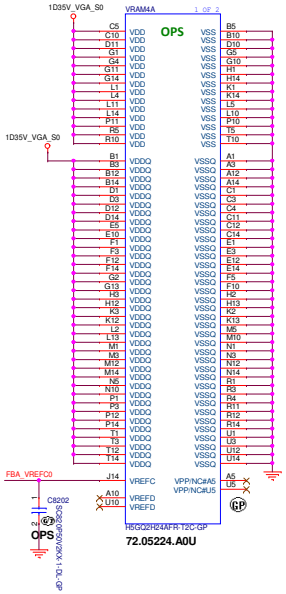
78 FBA_DQM4
78 FBA_DQM5
78 FBA_DQM6
78 FBA_DQM7

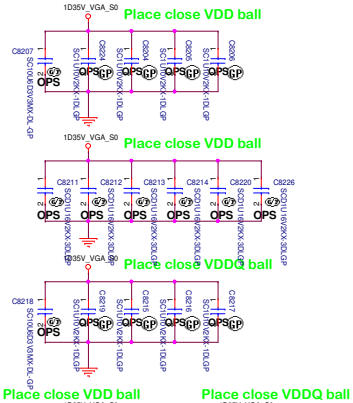
78 FBA_EDC4
78 FBA_EDC5
78 FBA_EDC6
78 FBA_EDC7

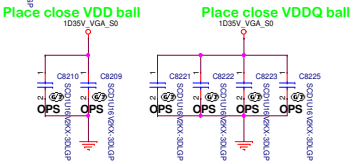
Frame Buffer Patition A-Upper Half

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low







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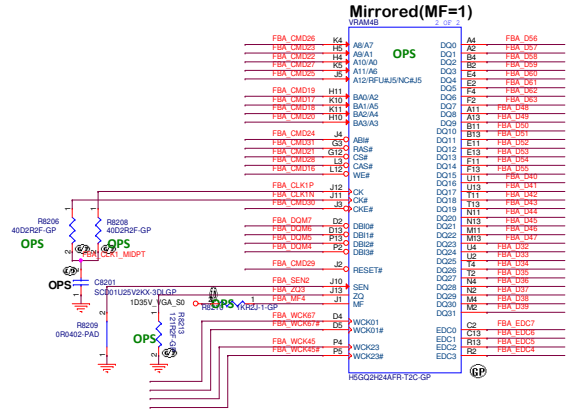

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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Main Func = dGPU

RT8816B For NVVDD

VGA : N17S-G2 / NVVDD
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

need 1.8V

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

Figure 12. GC6 Voltage Regulator Complex Signal Connection

N17S-G1
EDP-Continuous : 30 A
EDP-Peak : 60.1 A

Place Near GPU (NVVDDS)
1X330uF (Poscap) - PT8511 (Page85)

For tuning VGA_CORE sequence.

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Title: VGA Power B
Size: A1
Document Number: Jedi15"/17" CML
Rev: A00
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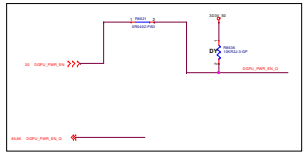
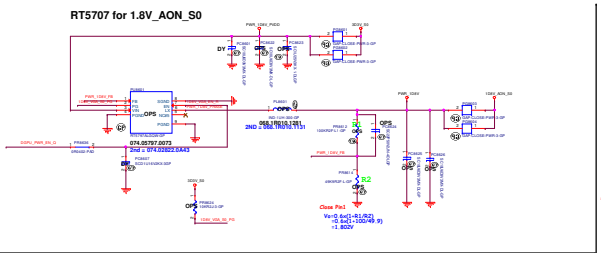
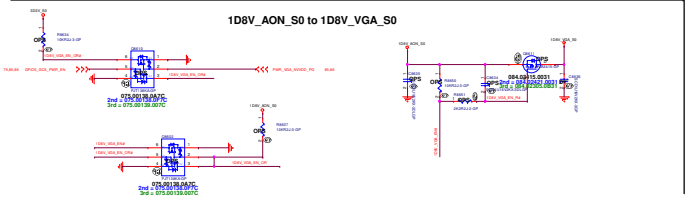
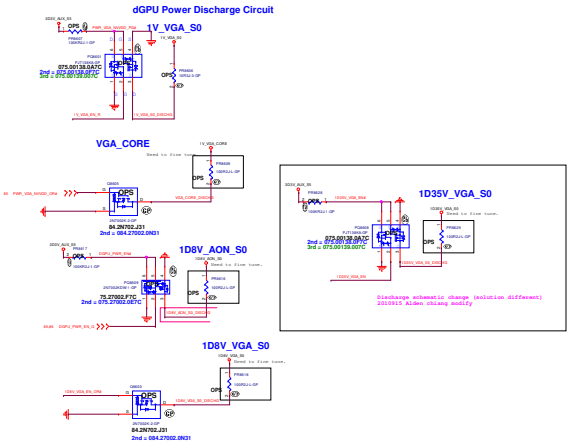
Sheet 85 of 100

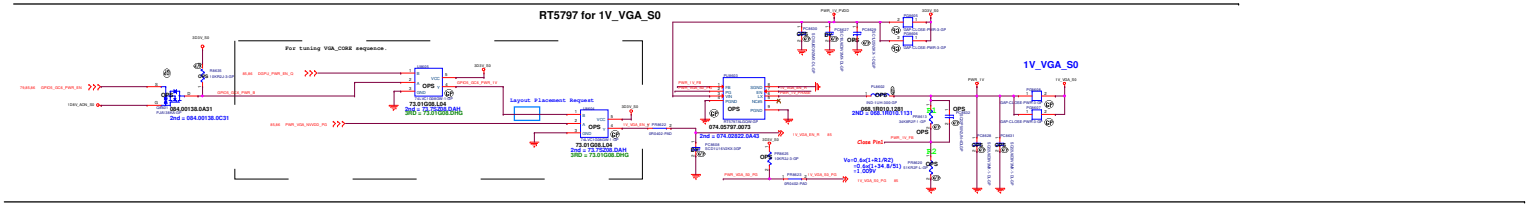
Main Func = dGPU



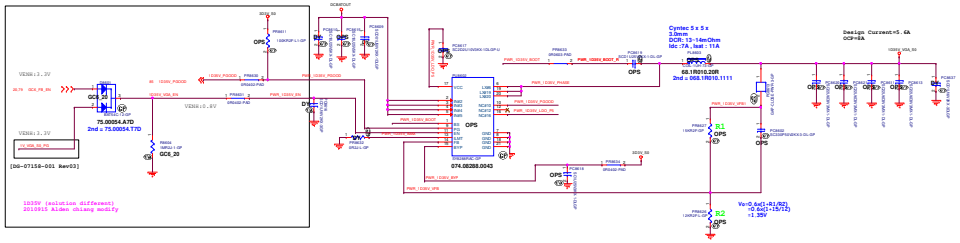








1D35V_VGA_S0



Main Func = UnusedParts

H1 HOLE276R150-GP — ZZ.00PAD.H91
H2 HOLE276R150-GP — ZZ.00PAD.H91
H3 HOLE276R150-GP — ZZ.00PAD.H91
H4 HOLE233R142-GP-U1 — ZZ.00PAD.5S1
H5 HOLE233R142-GP-U1 — ZZ.00PAD.5S1
H6 HOLE233R142-GP-U1 — ZZ.00PAD.5S1
H7 HOLE233R142-GP-U1 — ZZ.00PAD.5S1

WLAN

HS1 STF236R128H128-1-GP — 34.4LO45.001

SB-SPR Del 20190117

H8 HOLE335R178-GP — ZZ.00PAD.7F1
H9 HOLET375B375X375R174-GP — ZZ.00PAD.XQ1

3D3V_S0 — EC8918 EC8919 EC8920 EC8921 EC8926 EC8922 EC8923 EC8924 EC8925 EC8950 — SC1KF50V2KX-1DLGP

5V_S0 — EC8927 EC8928 EC8929 EC8930 EC8954 EC8953 EC8931 EC8932 EC8952 EC8951 — SC1KF50V2KX-1DLGP

+SDC_IN — EC8975 EC8973 EC8974 EC8977 EC8976 EC8978 EC8979 EC8982 EC8980 EC8981 — SC1KF50V2KX-1DLGP

5V_S5 — EC8912 EC8913 EC8914 EC8963 EC8961 EC8962 EC8964 EC8966 EC8965 EC8967 — SC1KF50V2KX-1DLGP

DCBATOUT — EC8908 EC8909 EC8910 EC8911 EC8915 EC8916 EC8917 EC8937 EC8938 EC8939 — SC1KF50V2KX-1DLGP

3D3V_S5 — EC8933 EC8934 EC8935 EC8936 EC8955 EC8957 EC8956 EC8958 EC8959 EC8960 — SC1KF50V2KX-1DLGP

BT+ — EC8971 EC8968 EC8969 EC8970 EC8972 — SC1KF50V2KX-1DLGP

SSID = EMI

Mind the voltage rating of the caps.

1D2V_S3 — EC8940 EC8942 EC8943 EC8944 EC8941 EC8945 EC8949 EC8946 EC8947 EC8948 — SC1KF50V2KX-1DLGP

DCBATOUT — EC8983 EC8984 EC8985 EC8986 EC8987 EC8988 EC8989 EC8990 EC8991 — SC1KF50V2KX-1DLGP

SSID = RF

1D2V_S3 — FC8920 FC8921 FC8922 — SC12P50V2AN-DL-GP

1D2V_S3 — FC8933 FC8934 FC8935 — SC12P50V2AN-DL-GP

DCBATOUT — FC8927 FC8928 FC8929 — SC12P50V2AN-DL-GP

+SDC_IN — FC8960 FC8961 FC8962 FC8963 — SC1KF50V2KX-1GP

1V_VGA_CORE — FC8968 — SC12P50V2JN-DL-GP

1V_CPU_CORE — FC8969 FC8970 — SC12P50V2JN-DL-GP

1V_VCCSA — FC8971 — SC1KF50V2XX-1GP

1V_VCCIO — FC8972 FC8973 — SC12P50V2AN-DL-GP

For GPU

Mind the voltage rating of the caps.

DCBATOUT — FC8951 FC8952 FC8953 FC8954 — SC12P50V2AN-DL-GP

Jedi15"/17" CML

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS (RF/EMI Caps)
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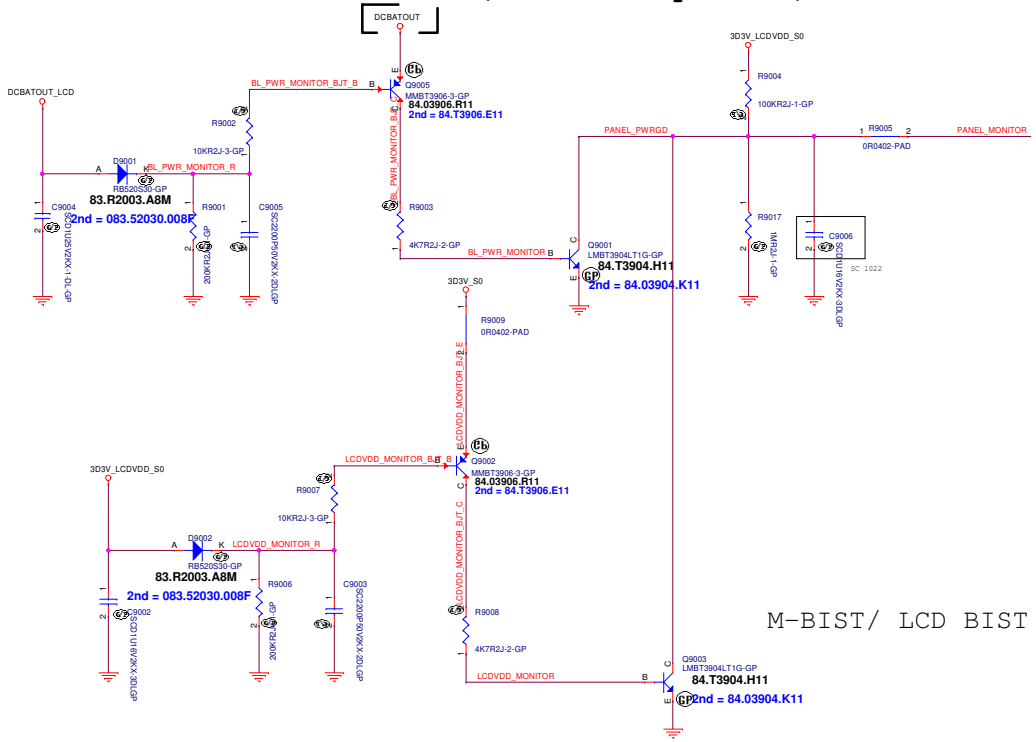
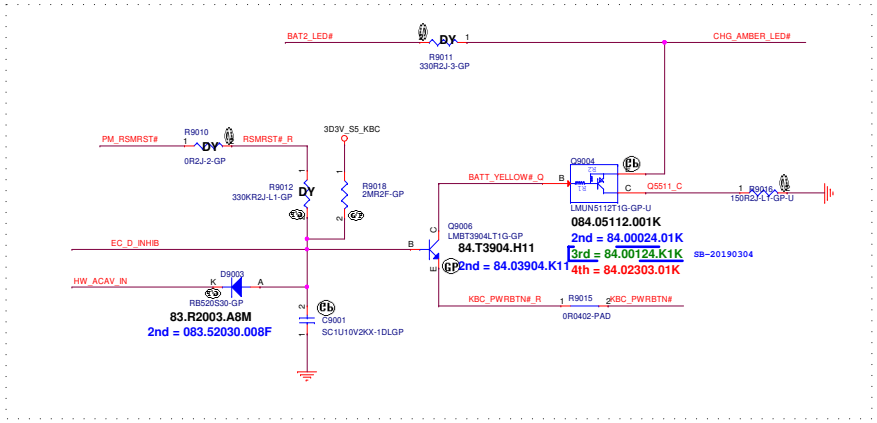
Main FUNC = M-BIST

LCD BIST for G10 (Was test only for G9)



M-BIST for G10 (Proposed schematic)



M-BIST/ LCD BIST -1890201

23,64,90	CHG_AMBER_LED#
24	BAT2_LED#
24,66	KBC_PWRBTN#
17	PM_RSMRST#
24,44	HW_ACAV_IN
24	PANEL_MONITOR
24	EC_D_INHIB
24,64,90	CHG_AMBER_LED#

Jedi15"/17" CML

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Title: M-BIST

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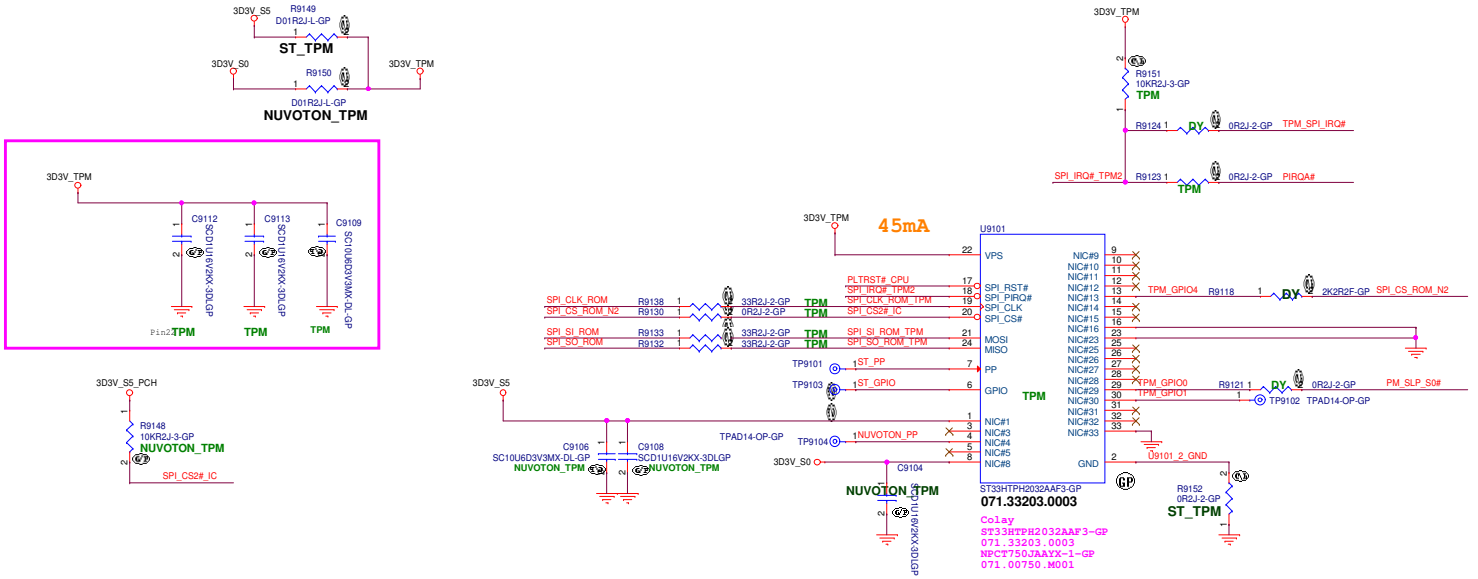
Main Func = TPM

18,25 SPI_SO_ROM
18,25 SPI_CLK_ROM
15,18,25 SPI_SI_ROM
18 SPI_CS_ROM_N2

17,26,61,63,66,71,76 PLTRST#_CPU
17,24,40 PM_SLP_S0#
20 PIRQA#
18 TPM_SPI_IRQ#



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt_L (non TPM)	DY	DY

Jedi15"/17" CML

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM2.0

Size	Document Number	Rev
Custom	Jedi15"/17" CML	A00

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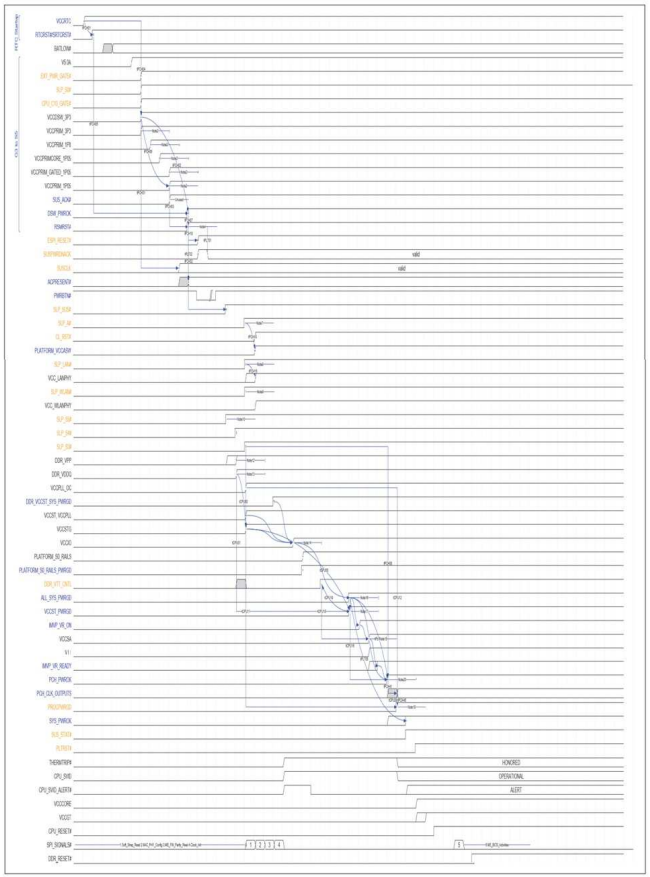
CML-U Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



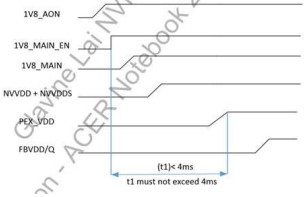
[dGPU] N17S-G2 Power-Up/Down Sequence

Power-Up Sequence

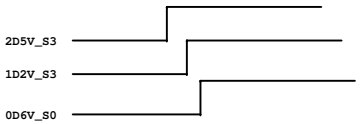
The following power-up sequence is required:

- 1V8_AON → 1V8_MAIN → (NVVDD+ NVVDDS) → PEX_VDD → FBVDD/Q
- All GPU power rails must ramp up after 1V8_AON.
- FBVDD/Q should ramp up after (NVVDD +NVVDDS) and PEX_VDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_VDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_VDD.

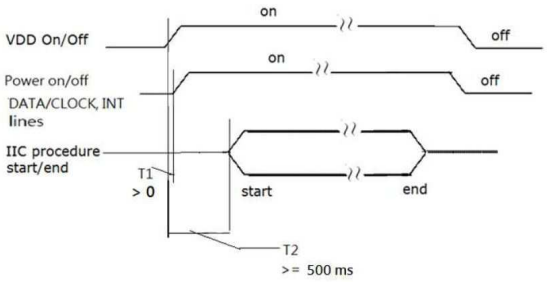


For DDR4 power sequence



[TP] Power-Up Sequence

Power on sequency (IIC interface):



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Title: Power Sequence

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Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER
	X01	01/17	57	R5785 change from 10K to 20K ohm	
	X01	01/17	44	Vcore_OVP & Vsys_UVP circuits DY	
	X01	01/17	89	SPR1 & SPR2 Del	
	X01	01/17	24	R2443 Change to 17.8K Ohm	
	X01	01/24	57	C5727,C5728,C5731-C5735,C5737 Change from 0402 to 0201 size	
	X01	01/24	21	Reserve R2119(75k ohm) pull down	
	X01	01/29	18	C1807 & C1808 Change 15pF to 12pF	
	X01	01/29	71	TBTA_HPD add R7107(0 Ohm)	
	X01	01/29	3~23	Change CPU P/N to ZZ.00CPU.361(Intel CML)	

Jedi15"/17" CML

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Title: *Change History*

Size: A3 | Document Number: *Jedi15"/17" CML* | Rev: *X01*

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