1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
2	0003554845	ENGINEERING RELEASED	2014-12-21

J94 MLB

LAST_MODIFICATION=Sun Dec 21 18:09:31 2014

DRAWING
TITLE=J94 MLB
ARRREV=DRAWING
LAST_MODIFIED=Sun Dec 21 18:09:31 2014

DRAWING TITLE: SCHEM,MLB,J94

Apple Inc.

DRAWING NUMBER: 051-1160 SIZE: D
REVISION: 2.0.0
BRANCH:
PAGE: 1 OF 105
SHEET: 1 OF 73

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DRAWING

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-1160	1	SCH,MLB,J94	SCH	CRITICAL	
820-4274	1	PCBF,MLB,J94	PCB	CRITICAL	
685-00030	1	PCBA,MLB,COMMON PARTS,J94	CMNPTS		MLB_CMNPTS

Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-0889	PCBA,MLB,DEV,J94	DEVELOPMENT,J94_DEVEL
939-00653	PCBA,MLB,DEV,J94,CPU_INT	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:SOCKET,DDR3:HYNIX_8GB_1866,SSD:Y
639-00915	PCBA,MLB,HY,8GB,29NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:HYNIX_8GB_1866,SSD:Y
639-00916	PCBA,MLB,EL,8GB,25NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:ELPIDA_8GB_1866,SSD:Y
639-00917	PCBA,MLB,SA,8GB,23NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:SAMSUNG_8GB_1866,SSD:Y
639-00918	PCBA,MLB,EL,16GB,25NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:ELPIDA_16GB_1866,SSD:Y
639-00919	PCBA,MLB,HY,16GB,25NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:HYNIX_16GB_1866,SSD:Y
639-00920	PCBA,MLB,HY,8GB,29NM,1866,HDD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:HYNIX_8GB_1866,SSD:N
639-00921	PCBA,MLB,EL,8GB,25NM,1866,HDD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:ELPIDA_8GB_1866,SSD:N
639-00922	PCBA,MLB,SA,8GB,23NM,1866,HDD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:SAMSUNG_8GB_1866,SSD:N
639-00923	PCBA,MLB,EL,16GB,25NM,1866,HDD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:ELPIDA_16GB_1866,SSD:N
639-00924	PCBA,MLB,HY,16GB,25NM,1866,HDD,J94	MLB_CMNPTS,ALTERNATE,X403:Y,CPU:BGA,DDR3:HYNIX_16GB_1866,SSD:N
639-00946	PCBA,MLB,X432,HY,8GB,29NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:N,CPU:BGA,DDR3:HYNIX_8GB_1866,SSD:Y
639-00947	PCBA,MLB,X432,EL,16GB,25NM,1866,SSD,J94	MLB_CMNPTS,ALTERNATE,X403:N,CPU:BGA,DDR3:ELPIDA_16GB_1866,SSD:Y
685-00030	PCBA,MLB,COMMON PARTS,J94	J94_COMMON

BOM Groups

BOM GROUP	BOM OPTIONS
J94_COMMON	COMMON,ALTERNATE,J94_PROGPARTS,SMCREG:SUP,XDP,CPUPEG:X8X8,USB_OC_ISO:Y,AUDIO_DP_SNS:Y,CPU_OUT_CAP:H,PP1V2_S3_CAP:H,PP1V05_S0_CAP:H,PPCPU_VDDQ_CAP:H,RTCRST:Y,CPUVCC:3PHASE,SHIELDS
J94_PROGPARTS	SMC:PROG,BOOTROM:PROG,CAMROM:PROG,TBTROM:PROG,ENETROM:PROG
J94_DEVEL	XDP_CONN,TEMPSNSDEV,SAMCONN

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00110	1	CPU,BW,QHPQ,BS,BS,4/3,1.7,45W..8,BGA1364	U0500	CRITICAL	CPU:BGA
998-6122	1	INTERPOSER,BGA1364	U0500	CRITICAL	CPU:SOCKET

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00106	1	IC,LP,PCH,QQB2,9-SER880-D,A0,BS,FCBGA695	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8x8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00185	1	IC,EFI,V0119,J94	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,SERIAL FLASH,64MBIT,3V,8P,WSON,QE=1	U5210	CRITICAL	BOOTROM:BLANK
341S00181	1	IC,SMC-B1,EXTERNAL,(VTBD),POC,J94	U5000	CRITICAL	SMC:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50MIPS,8CPL FW,157BGA	U5000	CRITICAL	SMC:BLANK
341S3778	1	IC,CAMERA,FLASH,V7229,J16	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00164	1	IC,EPROM,T29,FALCON RIDGE,(VTBD),POC,J94	U2890	CRITICAL	TBTROM:PROG
335S0915	1	IC,FLASH,SPI,4MBIT,50MHZ	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET SPI ROM,NVMONYX,V1.15,J16/J16G/J17/J70	U3990	CRITICAL	ENETROM:PROG
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	ENETROM:BLANK

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_8GB_1600	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,RAMCFG4:L,HYNIX_8GB_1600
DDR3:HYNIX_16GB_1600	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,RAMCFG4:L,HYNIX_16GB_1600
DDR3:HYNIX_8GB_1866	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,RAMCFG4:H,HYNIX_8GB_1866
DDR3:HYNIX_16GB_1866	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,RAMCFG4:H,HYNIX_16GB_1866
DDR3:ELPIDA_8GB_1600	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,RAMCFG4:L,ELPIDA_8GB_1600
DDR3:ELPIDA_16GB_1600	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,RAMCFG4:L,ELPIDA_16GB_1600
DDR3:ELPIDA_8GB_1866	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,RAMCFG4:H,ELPIDA_8GB_1866
DDR3:ELPIDA_16GB_1866	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,RAMCFG4:H,ELPIDA_16GB_1866
DDR3:SAMSUNG_8GB_1600	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,SAMSUNG_8GB_1600
DDR3:SAMSUNG_8GB_1866	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,SAMSUNG_8GB_1866

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
998-01027	08	CPU,BRW,4C+3E,65W
338S1247	02	TBT,Falcon Ridge-4c
335S00006	07	IC,SERIAL FLASH,Quad-IO
333S0784	07	HYNIX,32Gb,25nm LPDDR3-1866
333S0786	07	HYNIX,16Gb,29nm LPDDR3-1866
333S0790	07	ELPIDA,32Gb,25nm LPDDR3-1866
333S0792	07	ELPIDA,16Gb,25nm LPDDR3-1866
333S00004	07	SAMSUNG,16Gb,23nm LPDDR3-1866

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S00011		ALL	USB3 diodes
377S0184	377S00011		ALL	USB3 diodes
377S0124	377S0057		ALL	TVS
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
197S0479	197S0478		ALL	12 MHz Cam. Xtal
197S0486	197S0478		ALL	12 MHz Cam. Xtal
107S0251	107S0249		ALL	2mOhm Sense resistor
107S0251	107S0249	SSD:Y	ALL	2mOhm Sense resistor
107S0255	107S0240		ALL	1mOhm Sense resistor
197S0481	197S0480		ALL	25MHz Xtal
197S0343	197S0480		ALL	25MHz Xtal
197S0369	197S0392		ALL	32 KHz PCH Xtal
197S0399	197S0392		ALL	32 KHz PCH Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0860	138S0775	SSD:Y	ALL	Single-source 1uF 402
378S0391	378S0390		ALL	Debug LEDs
341S00016	341S3912		ALL	ENET ROM,ADESTO,V1.15
138S0747	138S0773		ALL	1uF,X6S,402
376S0572	376S0659		ALL	Single P-Ch FET
376S0572	376S0659	SSD:Y	ALL	Single P-Ch FET
376S00001	376S0659		ALL	Single P-Ch FET
376S00001	376S0659	SSD:Y	ALL	Single P-Ch FET
376S0972	376S00075		ALL	Single N-Ch FET
138S1103	138S0719		ALL	CAP,4.7uF,20%,10V,X5R,0402
155S0830	155S0316		ALL	FER BD,600 OHM,0.5A,0603
155S00076	155S0546		ALL	FER BD,600 OHM,300mA,0402
152S1373	152S1876		ALL	IND,PWR,7.8 mohm,13A,7.1x6.5x3mm

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1089	376S1128		ALL	Single N-Ch FET
155S0660	155S0513		ALL	220HM EMI BEAD
155S0694	155S0387		ALL	470OHM EMI BEAD
127S0164	127S0162		ALL	1UF 25V TANT
376S1129	376S0855		ALL	Dual N-Ch FET
376S00074	376S0855		ALL	Dual N-Ch FET
376S1129	376S0855	SSD:Y	ALL	Dual N-Ch FET
376S00074	376S0855	SSD:Y	ALL	Dual N-Ch FET
311S0649	311S0541		ALL	Single AND Gate
107S0375	107S00039		ALL	DDR Sense Res
353S3814	353S3812		ALL	TBT mux
353S4376	353S3384		ALL	HDD OOBv1 comparator
311S00013	311S0508		ALL	Single Driver Buffer OD
371S00019	371S0463		ALL	Rohm Schottky Barrier Diode
138S0746	138S0705		ALL	CAP,CER,X5R,10uF,20%,10V,402
371S00017	371S0749		ALL	DIODE,SCHOTTKY,30V,1A,SOD-323
353S00095	353S3328		ALL	DOC Crossbar
353S00440	353S3052		ALL	USB Power Switch

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0783	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_16GB_1600
333S0784	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_16GB_1866
333S0785	4	IC,SDRAM,29nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_8GB_1600
333S0786	4	IC,SDRAM,29nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_8GB_1866
333S0789	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_16GB_1600
333S0790	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_16GB_1866
333S0791	4	IC,SDRAM,25nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_8GB_1600
333S0792	4	IC,SDRAM,25nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_8GB_1866
333S00003	4	IC,SDRAM,23nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	SAMSUNG_8GB_1600
333S00004	4	IC,SDRAM,23nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	SAMSUNG_8GB_1866

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
N/A	0	1
SAMSUNG	1	0
ELPIDA	1	1

DIE REV	CFG 3
A	0
B	1

SIZE	CFG 2
8GB	0
16GB	1

SPEED	CFG 4
1600	0
1866	1

SYNC_MASTER=J117_TONY SYNC_DATE=05/05/2014

PAGE TITLE

BOM Configuration

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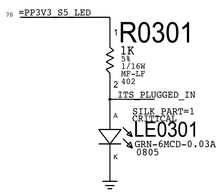
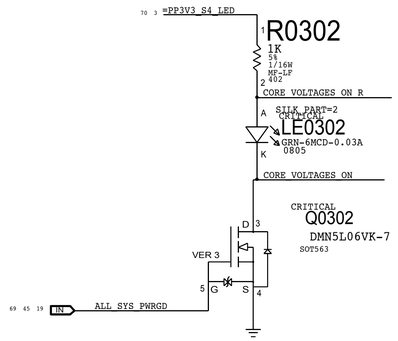
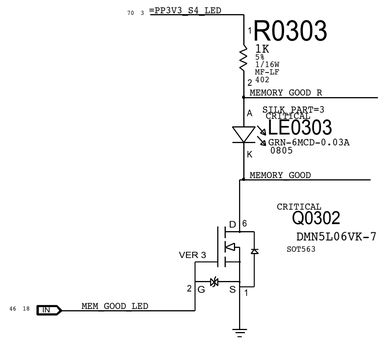
S5 Led



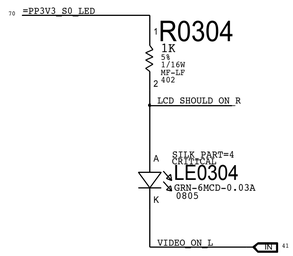
ALL_SYS_PWRGD Led



MEM_GOOD Led



VIDEO ON Led



SYNC_MASTER=J70_GAREN SYNC_DATE=10/22/2013

PAGE TITLE

DEBUG: LEDS

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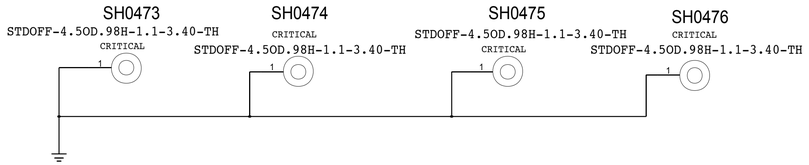
CPU HEATSINK MOUNTING FEATURES

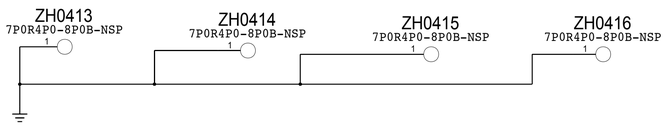


HEATSINK STABILITY MOUNTING FEATURES

APN:860-1532

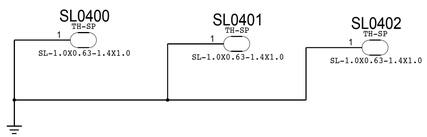
Rear Cover

APN:998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



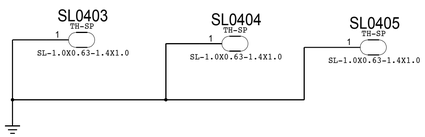
GND Slots for Shield Frame (CPU)

APN:998-3923 (Plated slot, 1mm x 0.63mm)



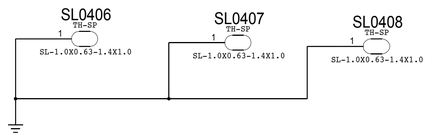
GND Slots for Shield Frame (MEM)

APN:998-3923 (Plated slot, 1mm x 0.63mm)



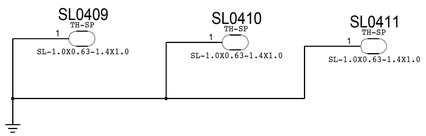
GND Slots for Shield Frame (TBT)

APN:998-3923 (Plated slot, 1mm x 0.63mm)



GND Slots for Shield Frame (USB)

APN:998-3923 (Plated slot, 1mm x 0.63mm)

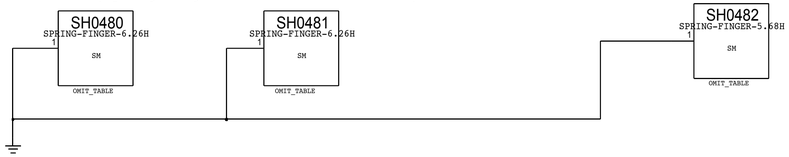


WIRELESS CARD MTG HOLES

APN:998-01406 (Plated holes, 2.1mm inner diameter, 4.3mm top pad, 5.1mm bottom pad)

Display Grounding Springs

APN:870-00886 (Spring Finger 4.2x2.5x6.26 for X403)
APN:870-00909 (Spring Finger 4.2x2.5x5.81 for X432)
APN:870-00887 (Spring Finger 4.2x2.5x5.68 for X403)
APN:870-00908 (Spring Finger 4.2x2.5x5.18 for X432)



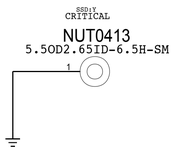
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-00886	2	SPRING FINGER,4.2X2.5X6.26	SH0480,SH0481	CRITICAL	X403:Y
870-00909	2	SPRING FINGER,4.2X2.5X5.81	SH0480,SH0481	CRITICAL	X403:N
870-00887	1	SPRING FINGER,4.2X2.5X5.68	SH0482	CRITICAL	X403:Y
870-00908	1	SPRING FINGER,4.2X2.5X5.18	SH0482	CRITICAL	X403:N

Shield Frames

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-02687	1	FRAME,EMI,SHIELD,CPU,J94	SHIELD_CPU	CRITICAL	SHIELDS
806-02082	1	FRAME,EMI,SHIELD,MEMORY,J94	SHIELD_MEM	CRITICAL	SHIELDS
806-03153	1	FRAME,EMI,SHIELD,USB,J94	SHIELD_USB	CRITICAL	SHIELDS
806-03145	1	FRAME,EMI,SHIELD,MDP,J94	SHIELD_TBT	CRITICAL	SHIELDS

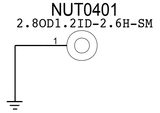
SSD STANDOFF

APN: 860-00198



T29 BUMPER

APN: 860-00201



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE

MECHANICALS: Holes/PD parts

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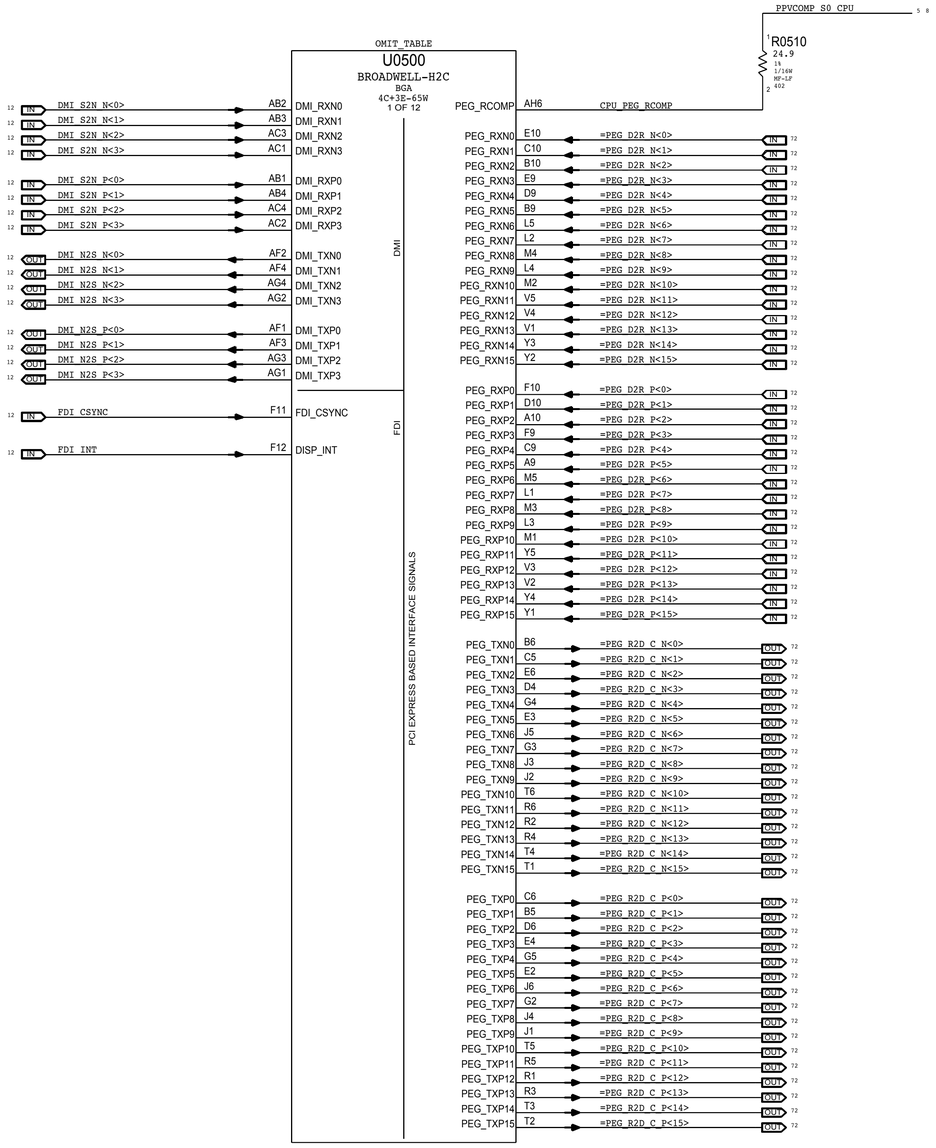

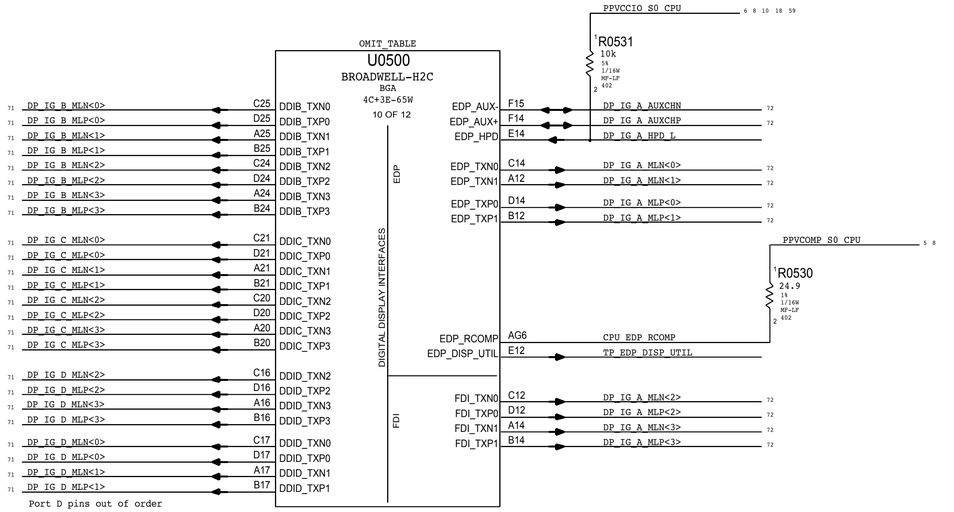

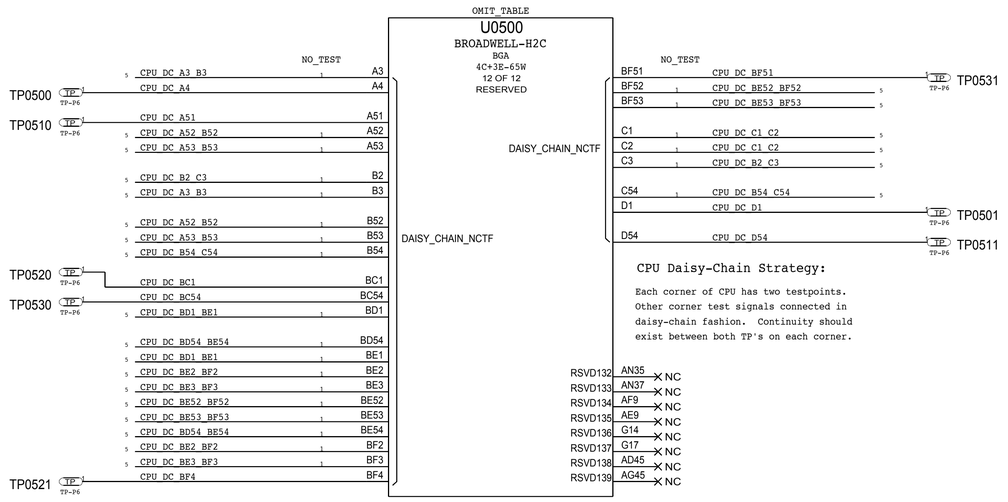

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

CPU & CHIPSET: CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER 051-1160

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SHEET 5 OF 73

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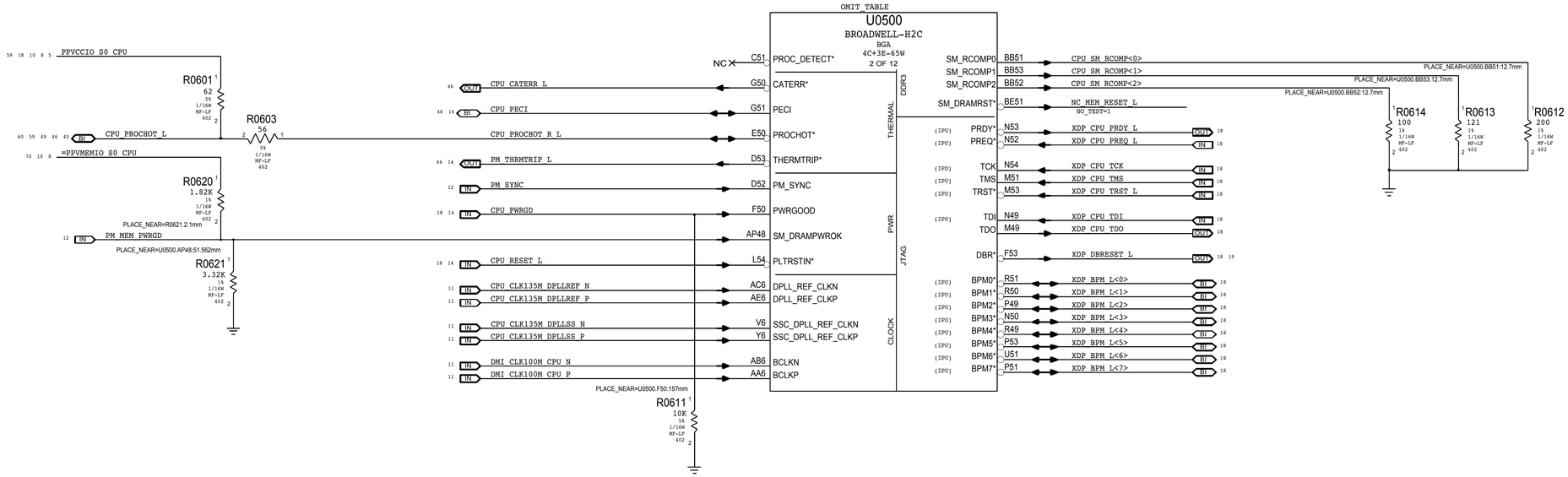
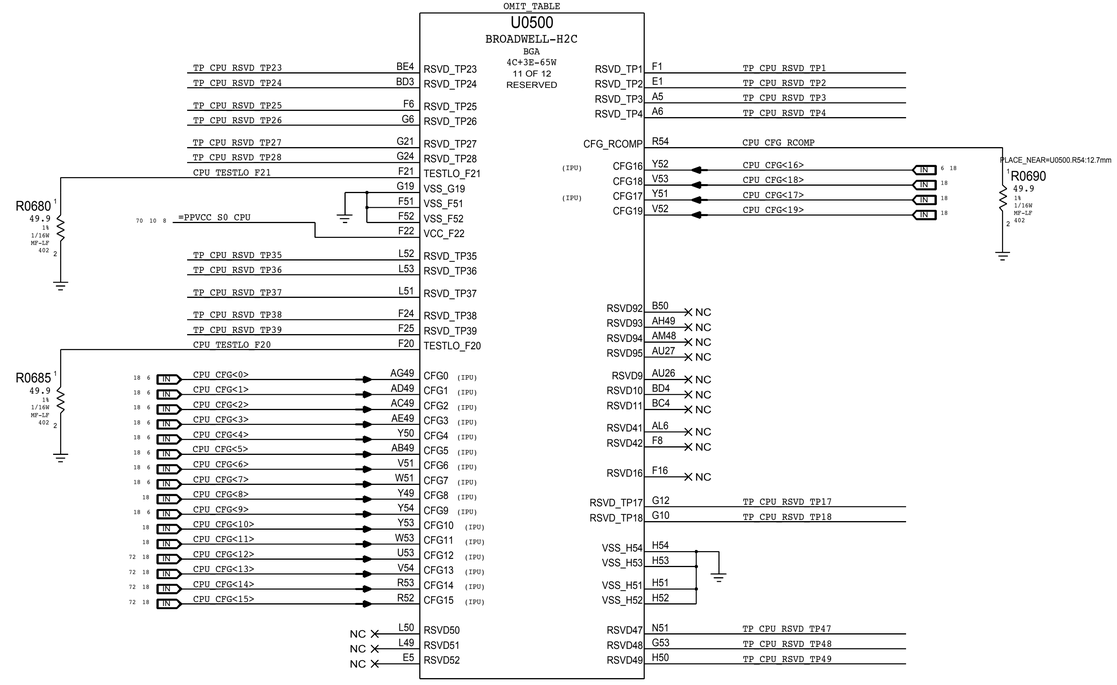
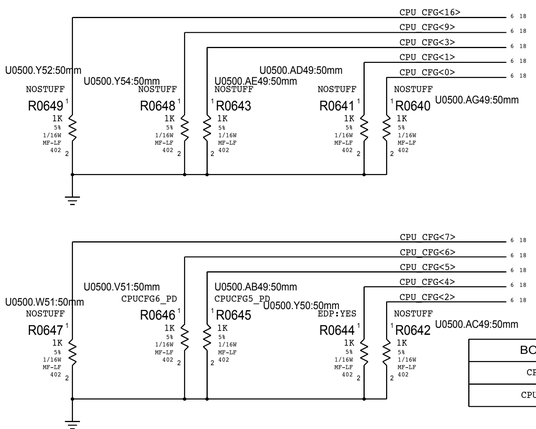





```
CFG [7] :PEG DEFER TRAINING          1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION          11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE          1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL       1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL      1 = NORMAL OPERATION   0 = LANES REVERSED
```

These must be placed within 400pS of U0500 (Intel Doc 479493 Fig. 3-6)



BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=J16_MLB_IG
SYNC_DATE=07/01/2014

PAGE TITLE
CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG

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PAGE 6 OF 105
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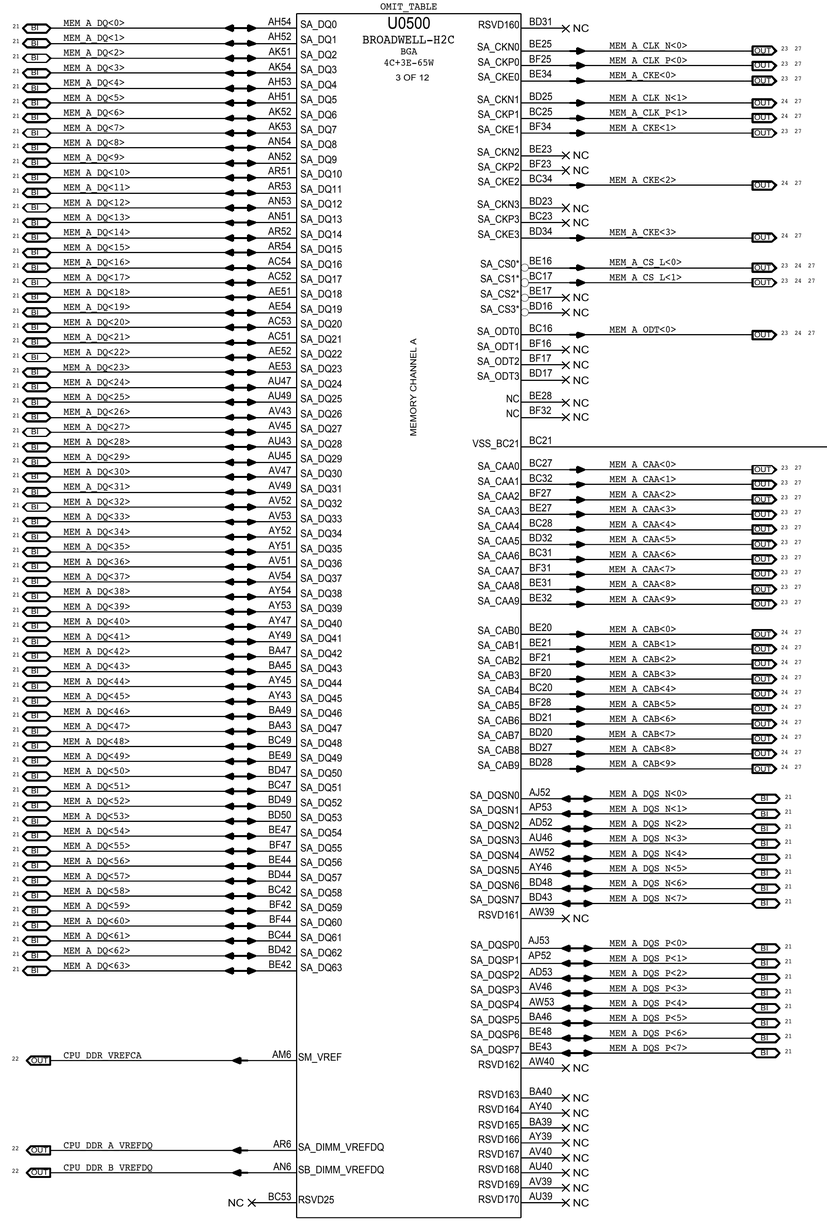

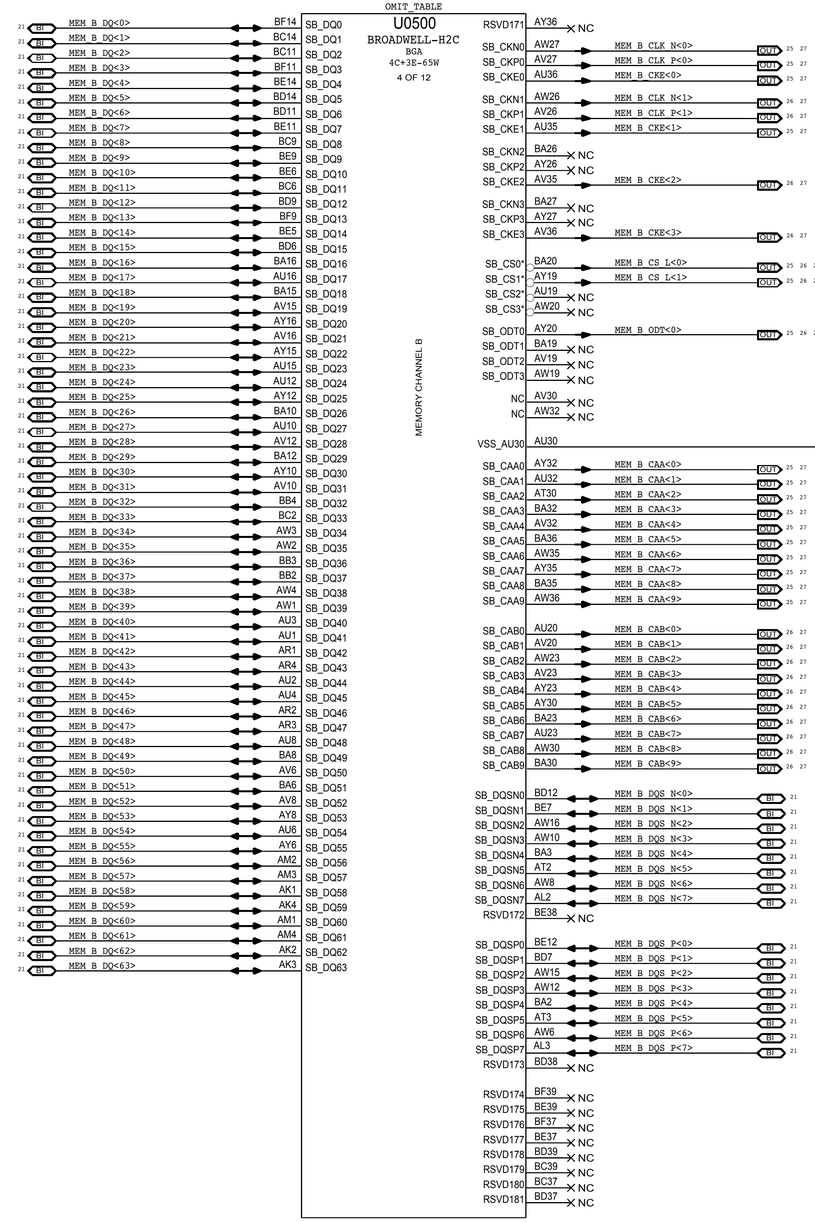

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

CPU & CHIPSET: CPU LPDDR3 Interfaces

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DRAWING NUMBER 051-1160

SIZE D

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PAGE TITLE

CPU & CHIPSET: CPU Power

DRAWING NUMBER	SIZE
051-1160	D

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PAGE: 8 OF 105

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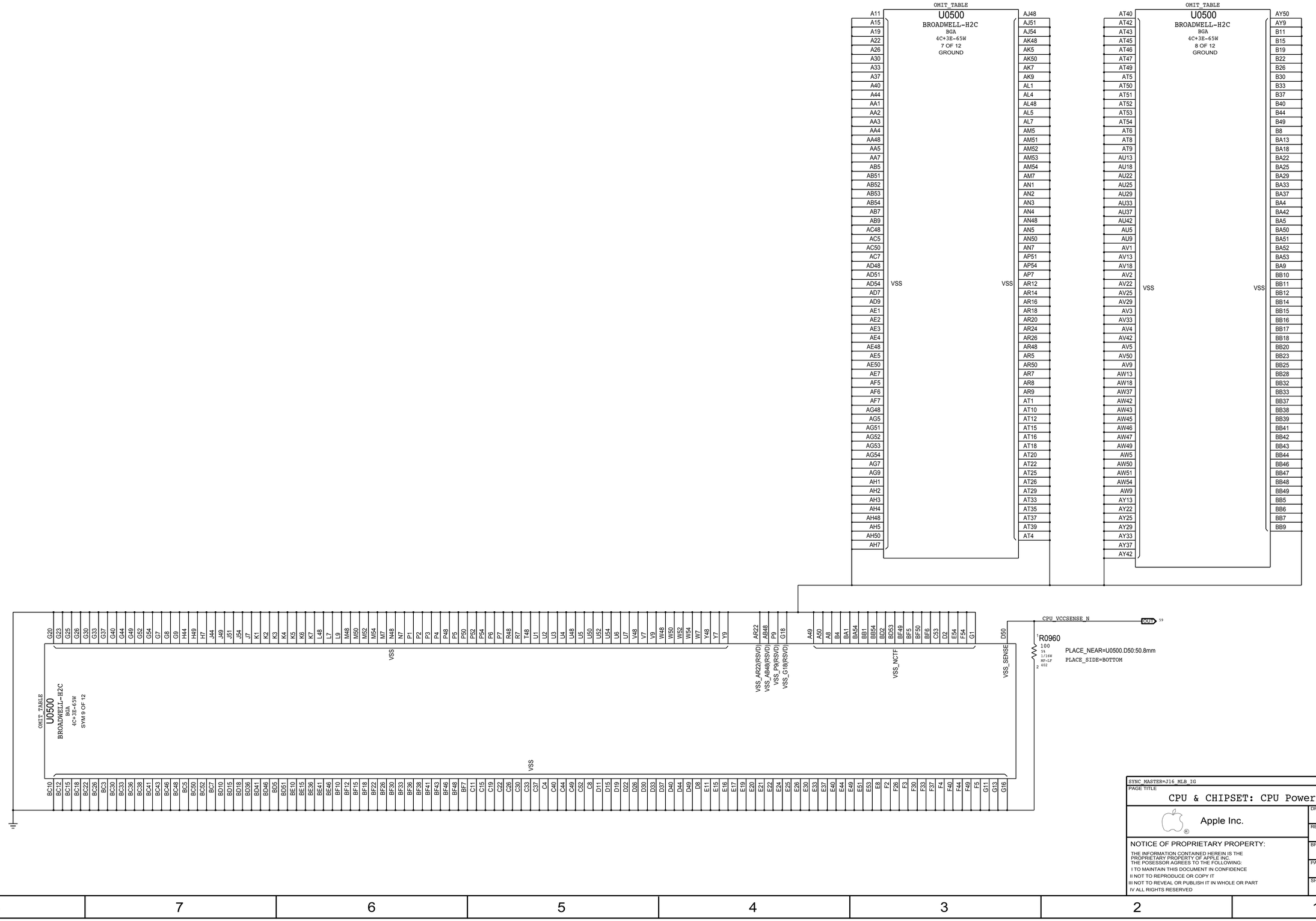

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

CPU & CHIPSET: CPU Power/Ground

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DRAWING NUMBER 051-1160 SIZE D

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

70 8 6 =PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402
C1001 1UF 10% 10V X6S-CERM 0402
C1002 1UF 10% 10V X6S-CERM 0402
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

C1020 10UF 20% 4V X6S 0402
C1021 10UF 20% 4V X6S 0402
C1022 10UF 20% 4V X6S 0402
C1023 10UF 20% 4V X6S 0402

For noise floor mitigation of DP (C1070-C1075):

C1070 1.5PF +/-0.1PF 25V C0G-CERM 0201-1
C1071 1.5PF +/-0.1PF 25V C0G-CERM 0201-1
C1072 1.5PF +/-0.1PF 25V C0G-CERM 0201-1
C1073 1.5PF +/-0.1PF 25V C0G-CERM 0201-1
C1074 1.5PF +/-0.1PF 25V C0G-CERM 0201-1
C1075 1.5PF +/-0.1PF 25V C0G-CERM 0201-1

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 10UF 20% 4V X6S 0402
CRITICAL C1025 10UF 20% 4V X6S 0402
CRITICAL C1026 10UF 20% 4V X6S 0402
CRITICAL C1027 10UF 20% 4V X6S 0402
CRITICAL C1028 10UF 20% 4V X6S 0402
CRITICAL C1029 10UF 20% 4V X6S 0402
CRITICAL C1030 10UF 20% 4V X6S 0402
CRITICAL C1031 10UF 20% 4V X6S 0402
CRITICAL C1032 10UF 20% 4V X6S 0402
CRITICAL C1033 10UF 20% 4V X6S 0402
CRITICAL C1034 10UF 20% 4V X6S 0402
CRITICAL C1035 10UF 20% 4V X6S 0402
CRITICAL C1036 10UF 20% 4V X6S 0402
CRITICAL C1037 10UF 20% 4V X6S 0402
CRITICAL C1038 10UF 20% 4V X6S 0402
CRITICAL C1039 10UF 20% 4V X6S 0402
CRITICAL C1040 10UF 20% 4V X6S 0402
CRITICAL C1041 10UF 20% 4V X6S 0402
CRITICAL C1042 10UF 20% 4V X6S 0402
CRITICAL C1043 10UF 20% 4V X6S 0402
CRITICAL C1044 10UF 20% 4V X6S 0402
CRITICAL C1045 10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 10UF 20% 4V X6S 0402
CRITICAL C1047 10UF 20% 4V X6S 0402
CRITICAL C1048 10UF 20% 4V X6S 0402
CRITICAL C1049 10UF 20% 4V X6S 0402
CRITICAL C1050 10UF 20% 4V X6S 0402
CRITICAL C1051 10UF 20% 4V X6S 0402
CRITICAL C1052 10UF 20% 4V X6S 0402
CRITICAL C1053 10UF 20% 4V X6S 0402
CRITICAL C1054 10UF 20% 4V X6S 0402
CRITICAL C1055 10UF 20% 4V X6S 0402
CRITICAL C1056 10UF 20% 4V X6S 0402
CRITICAL C1057 10UF 20% 4V X6S 0402
CRITICAL C1058 10UF 20% 4V X6S 0402
CRITICAL C1059 10UF 20% 4V X6S 0402
CRITICAL C1060 10UF 20% 4V X6S 0402
CRITICAL C1061 10UF 20% 4V X6S 0402
CRITICAL C1062 10UF 20% 4V X6S 0402
CRITICAL C1063 10UF 20% 4V X6S 0402
CRITICAL C1064 10UF 20% 4V X6S 0402
CRITICAL C1065 10UF 20% 4V X6S 0402
CRITICAL C1066 10UF 20% 4V X6S 0402
CRITICAL C1067 10UF 20% 4V X6S 0402

BULK CAPS ON REGULATOR PAGE

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

70 8 6 =PPVMEMIO_S0_CPU

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603
C1091 10UF 20% 4V X6S-CERM 0603
C1092 10UF 20% 4V X6S-CERM 0603
C1093 10UF 20% 4V X6S-CERM 0603
C1094 10UF 20% 4V X6S-CERM 0603
C1095 10UF 20% 4V X6S-CERM 0603
C1096 10UF 20% 4V X6S-CERM 0603
C1097 10UF 20% 4V X6S-CERM 0603

OMIT_TABLE
CRITICAL
C1078 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0381	1	CAP,AL,POLY,470UF	C1078	CRITICAL	PPCPU_VDDQ_CAP:H
128S0391	1	CAP,AL,POLY,270UF	C1078	CRITICAL	PPCPU_VDDQ_CAP:L

70 19 0 =PP1V05_S0_CPU_VCCST

U0500.D5:25mm
C1098 1UF 10% 10V X6S-CERM 0402
U0500.D5:62.5mm
C1099 4.7UF 10% 25V X5R-CERM 0603

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

59 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 16V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014
PAGE TITLE: CPU & CHIPSET: CPU Decoupling
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SIZE: D
REVISION: 2.0.0
BRANCH:
PAGE: 10 OF 105
SHEET: 10 OF 73

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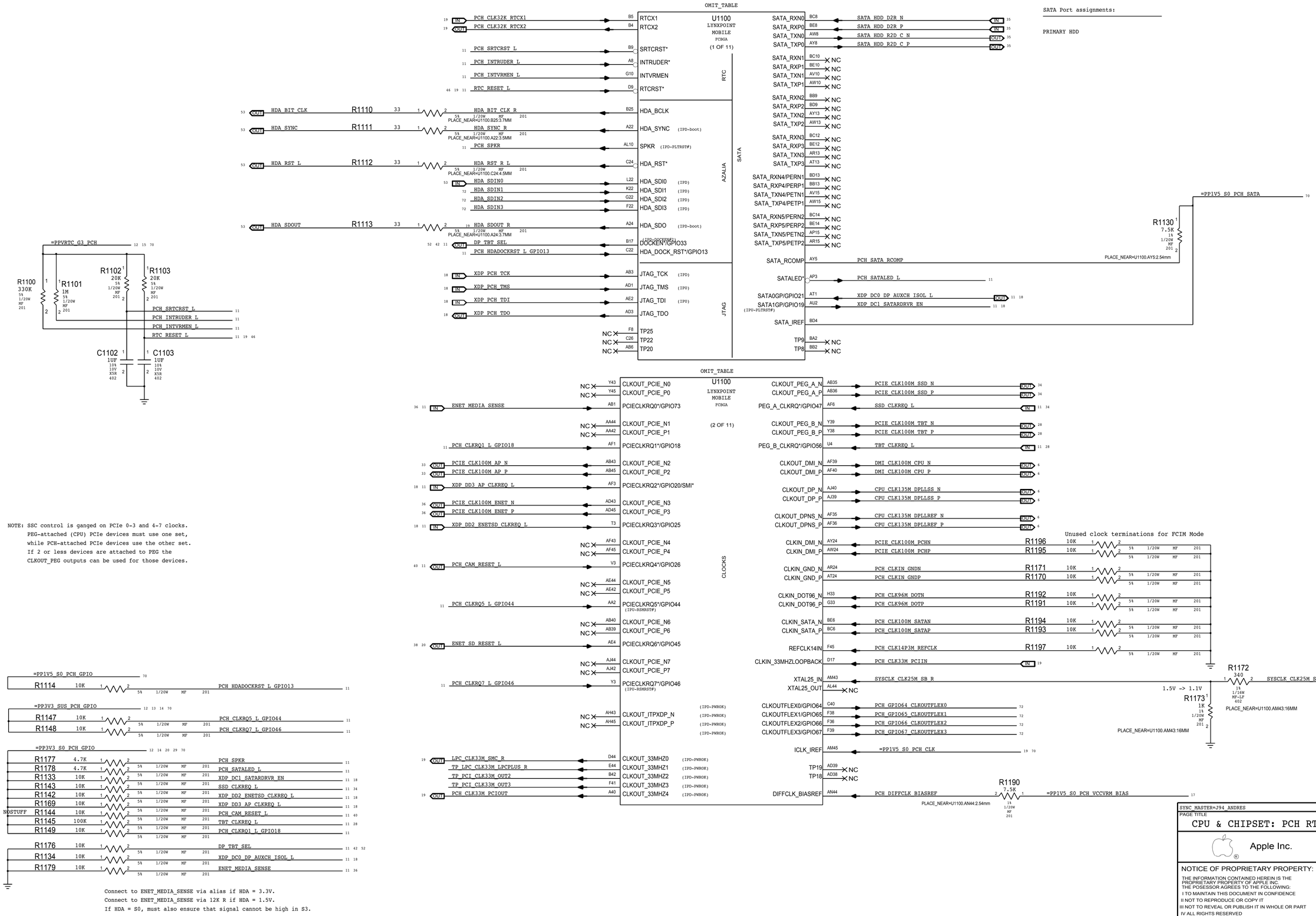

SYNC_MASTER=J94_ANDRES SYNC_DATE=07/09/2014

PAGE TITLE

CPU & CHIPSET: PCH RTC/HDA/JTAG/SATA/CLK

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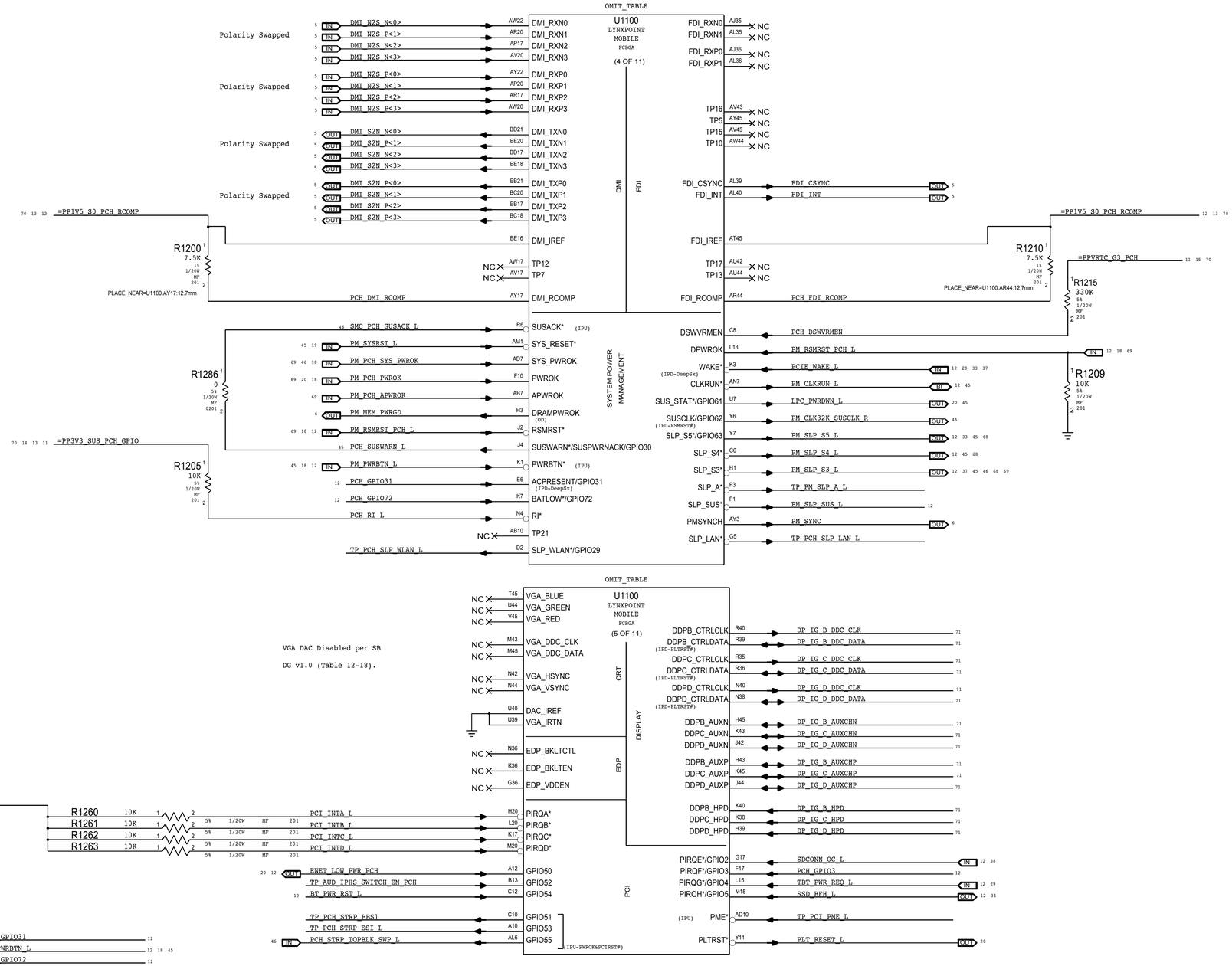

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

CPU & CHIPSET: PCH DMI/FDI/PM/GFX/PCI

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DRAWING NUMBER 051-1160

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OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(9 OF 11)

PCI-E

NC	AW31	PERN1_USB3RN3
NC	AY31	PERP1_USB3RP3
NC	BE32	PETN1_USB3TN3
NC	BC32	PETP1_USB3TP3
NC	AT31	PERN2_USB3RN4
NC	AR31	PERP2_USB3RP4
NC	BD33	PETN2_USB3TN4
NC	BB33	PETP2_USB3TP4
33 IN	AW33	PERN3
33 IN	AY33	PERP3
33 OUT	BE34	PETN3
33 OUT	BC34	PETP3
36 IN	AT33	PERN4
36 IN	AR33	PERP4
36 OUT	BE36	PETN4
36 OUT	BC36	PETP4
NC	AW36	PERN5
NC	AV36	PERP5
NC	BD37	PETN5
NC	BB37	PETP5
NC	AY38	PERN6
NC	AW38	PERP6
NC	BC38	PETN6
NC	BE38	PETP6
NC	AT40	PERN7
NC	AT39	PERP7
NC	BE40	PETN7
NC	BC40	PETP7
NC	AN38	PERN8
NC	AN39	PERP8
NC	BD42	PETN8
NC	BD41	PETP8

AirPort

ENET

USB

USB2N0	B37	USB_EXTA_N	BI 43
USB2P0	D37	USB_EXTA_P	BI 43
USB2N1	A38	USB_EXTC_N	BI 44
USB2P1	C38	USB_EXTC_P	BI 44
USB2N2	A36	NC	
USB2P2	C36	NC	
USB2N3	A34	NC	
USB2P3	C34	NC	
USB2N4	B33	NC	
USB2P4	D33	NC	
USB2N5	F31	NC	
USB2P5	G31	NC	
USB2N6	K31	NC	
USB2P6	L31	NC	
USB2N7	G29	NC	
USB2P7	H29	NC	
USB2N8	A32	USB_EXTB_N	BI 43
USB2P8	C32	USB_EXTB_P	BI 43
USB2N9	A30	USB_EXTD_N	BI 44
USB2P9	C30	USB_EXTD_P	BI 44
USB2N10	B29	USB_CAMERA_N	BI 39
USB2P10	D29	USB_CAMERA_P	BI 39
USB2N11	A28	USB_BT_N	BI 33
USB2P11	C28	USB_BT_P	BI 33
USB2N12	G26	NC	
USB2P12	F26	NC	
USB2N13	F24	NC	
USB2P13	G24	NC	

(IPD)

USB3RN1	AR26	USB3_EXTA_D2R_N	IN 43
USB3RP1	AP26	USB3_EXTA_D2R_P	IN 43
USB3TN1	BE24	USB3_EXTA_R2D_CF_N	OUT 43
USB3TP1	BD23	USB3_EXTA_R2D_CF_P	OUT 43
USB3RN2	AW26	USB3_EXTB_D2R_N	IN 43
USB3RP2	AV26	USB3_EXTB_D2R_P	IN 43
USB3TN2	BD25	USB3_EXTB_R2D_CF_N	OUT 43
USB3TP2	BC24	USB3_EXTB_R2D_CF_P	OUT 43
USB3RN5	AW29	USB3_EXTC_D2R_N	IN 44
USB3RP5	AV29	USB3_EXTC_D2R_P	IN 44
USB3TN5	BE26	USB3_EXTC_R2D_CF_N	OUT 44
USB3TP5	BC26	USB3_EXTC_R2D_CF_P	OUT 44
USB3RN6	AR29	USB3_EXTD_D2R_N	IN 44
USB3RP6	AP29	USB3_EXTD_D2R_P	IN 44
USB3TN6	BD27	USB3_EXTD_R2D_CF_N	OUT 44
USB3TP6	BE28	USB3_EXTD_R2D_CF_P	OUT 44

USBRBIAS*	K24	PCH_USB_RBIAS
USBRBIAS	K26	

PLACE_NEAR=U1100.K24:11.4mm
R1370 22.6 1% 1/20W MF 201

TP24	M33	NC
TP23	L33	NC

OC0*/GPIO59	P3	XDP_DA0_USB_EXTA_OC_L	IN 13 18
OC1*/GPIO40	V1	XDP_DA1_USB_EXTC_OC_L	IN 13 18
OC2*/GPIO41	U2	XDP_DA2_SSD_PWR_EN	OUT 13 18
OC3*/GPIO42	P1	XDP_DA3_PCH_CAM_EXT_BOOT	OUT 13 18
OC4*/GPIO43	M3	XDP_DB0_USB_EXTB_OC_L	IN 13 18
OC5*/GPIO9	T1	XDP_DB1_USB_EXTD_OC_L	IN 13 18
OC6*/GPIO10	N2	XDP_DB2_SSD_SR_EN_L	OUT 13 18
OC7*/GPIO14	M1	XDP_DB3_SDCONN_STATE_CHANGE_L	IN 13 18

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

CAMERA

BT

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

70 12 =PP1V5_S0_PCH_RCOMP

R1300 7.5K 1% 1/20W MF 201

PLACE_NEAR=U1100.BD29:12.7mm

	BE30	PCIE_IREF
NC	BC30	TP11
NC	BB29	TP6
PCH_PCIE_RCOMP	BD29	PCIE_RCOMP

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(3 OF 11)

LPC

45 BI	LPC_AD<0>	R1340 33	LPC_AD_R<0>
45 BI	LPC_AD<1>	R1341 33	LPC_AD_R<1>
45 BI	LPC_AD<2>	R1342 33	LPC_AD_R<2>
45 BI	LPC_AD<3>	R1343 33	LPC_AD_R<3>
45 OUT	LPC_FRAME_L	R1344 33	LPC_FRAME_R_L

LAD0 (IPU)	A20	
LAD1 (IPU)	C20	
LAD2 (IPU)	A18	
LAD3 (IPU)	C18	
LFRAME*	B21	
LDRQ0* (IPU)	D21	72 OUT LPC_DREQ0_L
LDRQ1*/GPIO23 (IPU-LDRQ1#)	G20	20 13 OUT TBT_PWR_EN_PCH
SERIRQ	AL11	45 13 BI LPC_SERIRQ

SMBUS

SMBALERT*/GPIO11	N7	PCH_SMBALERT_L 13
SMBCLK	R10	SMBUS_PCH_CLK OUT 48
SMBDATA	U11	SMBUS_PCH_DATA BI 48
SML0ALERT*/GPIO60	N8	PCH_SML0ALERT_L 13
SML0CLK	U8	SML_PCH_0_CLK OUT 48
SML0DATA	R7	SML_PCH_0_DATA BI 48
SML1ALERT*/PCHHOT*/GPIO74	H6	SSD_RESET_L OUT 20 34
SML1CLK/GPIO58	K6	SML_PCH_1_CLK IN 48
SML1DATA/GPIO75	N11	SML_PCH_1_DATA BI 48

SPI

47 OUT	SPI_CLK_R	SPI_CLK	AJ11
47 OUT	SPI_CS0_R_L	SPI_CS0* (IPU)	AJ7
NC		SPI_CS1* (IPU)	AL7
NC		SPI_CS2* (IPU)	AJ10
47 BI	SPI_MOSI_R	SPI_MOSI (IPD)	AH1
47 BI	SPI_MISO_R	SPI_MISO (IPU)	AH3
47 13 BI	SPI_IO_R<2>	SPI_IO2 (IPU)	AJ4
47 13 BI	SPI_IO_R<3>	SPI_IO3 (IPU)	AJ2

C-LINK

(IPU/IPD)	CL_CLK	AF11	TP_CLINK_CLK
(IPU/IPD)	CL_DATA	AF10	TP_CLINK_DATA
	CL_RST*	AF7	TP_CLINK_RESET_L

TP1	BA45	NC
TP2	BC45	NC
TP4	BE43	NC
TP3	BE44	NC
TD_IREF	AY43	PCH_TD_IREF

R1380 8.2K 1% 1/20W MF 201

=PP3V3_SUS_PCH_GPIO 11 12 14 70

R1360	10K	XDP_DA0_USB_EXTA_OC_L	13 18
R1361	10K	XDP_DA1_USB_EXTC_OC_L	13 18
R1320	10K	XDP_DB0_USB_EXTB_OC_L	13 18
R1321	10K	XDP_DB1_USB_EXTD_OC_L	13 18
R1353	10K	PCH_SMBALERT_L	13
R1354	10K	PCH_SML0ALERT_L	13

=PP3V3_SUS_PCH_VCC_SPI 15 17 70

R1356	1K	SPI_IO_R<2>	13 47
R1357	1K	SPI_IO_R<3>	13 47

=PP3V3_S4_PCH_GPIO 20 43 44 70

R1367	10K	XDP_DB2_SSD_SR_EN_L	13 18
R1369	10K	XDP_DB3_SDCONN_STATE_CHANGE_L	13 18
R1355	10K	XDP_DA2_SSD_PWR_EN	13 18

=PP3V3_S0_PCH 19 70

R1350	10K	LPC_SERIRQ	13 45
R1351	10K	TBT_PWR_EN_PCH	13 20
R1368	10K	XDP_DA3_PCH_CAM_EXT_BOOT	13 18

NOSTUFF

SYNC_MASTER=J94_ANDRES	SYNC_DATE=07/09/2014
PAGE TITLE	CPU & CHIPSET: PCH PCI-E/USB
Apple Inc.	DRAWING NUMBER 051-1160 SIZE D
	REVISION 2.0.0
	BRANCH
	PAGE 13 OF 105
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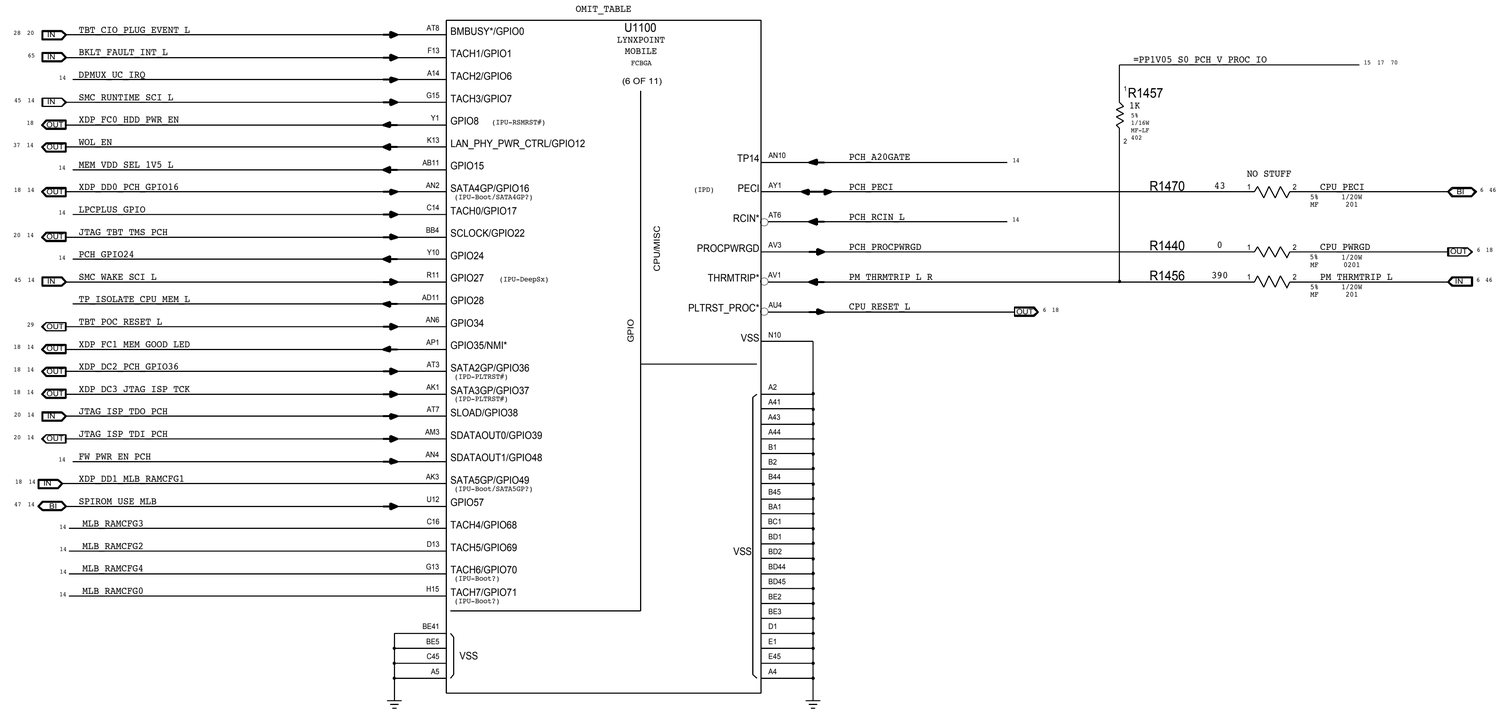
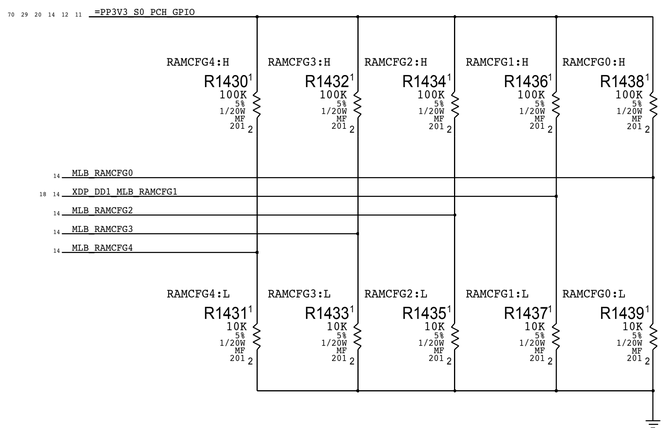
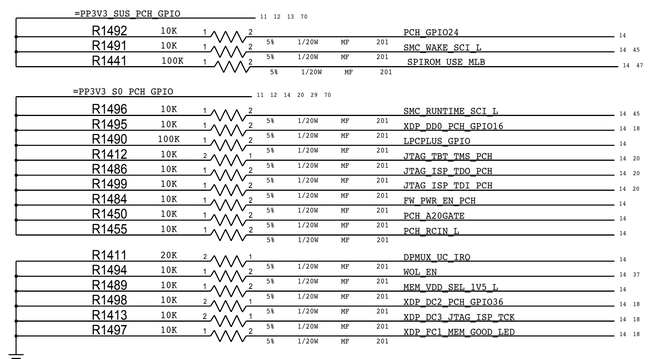


RAM Configuration Straps





SYNC_MASTER=J94_ANDRES SYNC_DATE=07/09/2014

PAGE TITLE

CPU & CHIPSET: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER 051-1160

SIZE D

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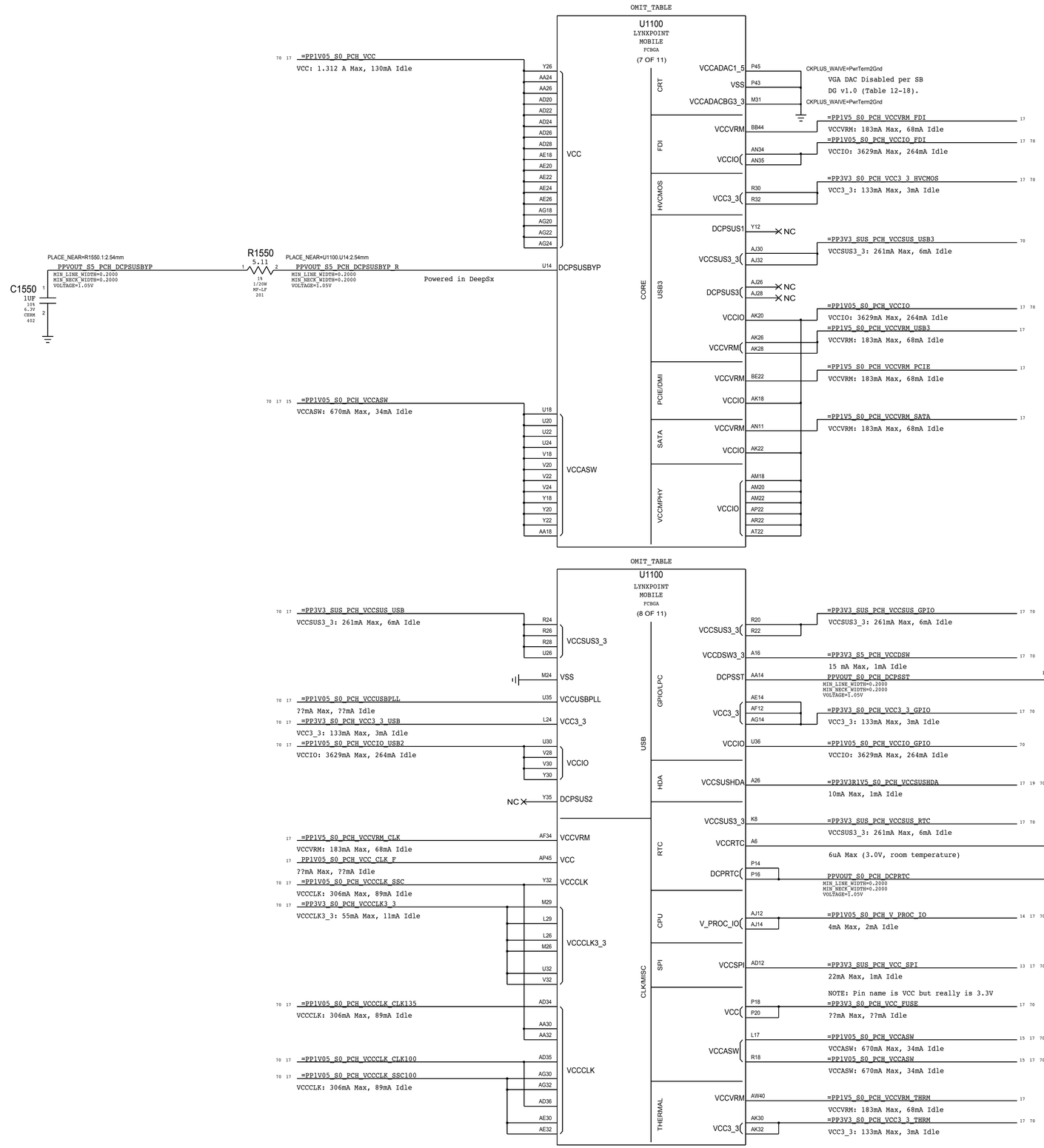

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

CPU & CHIPSET: PCH Power

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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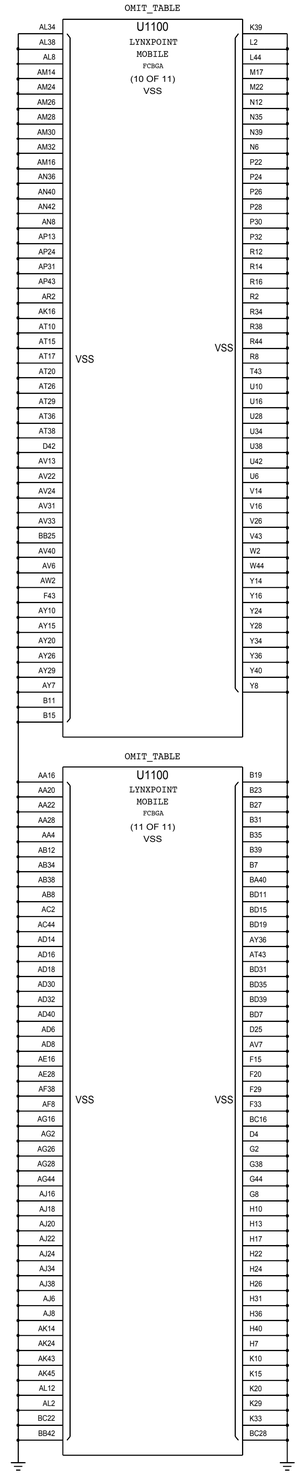

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

CPU & CHIPSET: PCH Grounds

Apple Inc.

DRAWING NUMBER 051-1160

SIZE D

REVISION 2.0.0

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
70 15 =PP3V3_S5_PCH_VCCDSW
C1700 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.A16::2.54mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
70 15 13 =PP3V3_SUS_PCH_VCC_SPI
C1702 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AD12::2.54mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
70 15 =PP3V3_SUS_PCH_VCCSUS_GPIO
C1704 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.R20::2.54mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
70 15 =PP3V3_SUS_PCH_VCCSUS_USB
C1706 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.R26::2.54mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
70 15 =PP3V3_SUS_PCH_VCCSUS_RTC
C1708 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.K8::2.54mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
70 19 15 =PP3V3R1V5_S0_PCH_VCCSUSHDA
C1710 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.A26::2.54mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
70 15 =PP3V3_S0_PCH_VCCCLK3_3
C1720 1UF 20% 10V X5R 0201
C1721 1UF 20% 10V X5R 0201
C1722 1UF 20% 10V X5R 0201
C1723 1UF 20% 10V X5R 0201
BYPASS=U1100.L26::2.54mm
BYPASS=U1100.L29::2.54mm
BYPASS=U1100.M29::2.54mm
BYPASS=U1100.U32::2.54mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_HVCMOS
C1726 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.R30::2.54mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_GPIO
C1728 0.01UF 10% 10V X7R-CERM 0201
BYPASS=U1100.AE14::2.54mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_USB
C1730 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.L24::2.54mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_THRM
C1732 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.AK30::2.54mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
70 15 =PP3V3_S0_PCH_VCC_FUSE
C1734 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.P18::2.54mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
70 =PP1V5_S0_PCH_VCCVRM
183mA Max, 68mA Idle
11 =PP1V5_S0_PCH_VCCVRM_BIAS
15 =PP1V5_S0_PCH_VCCVRM_FDI
15 =PP1V5_S0_PCH_VCCVRM_USB3
15 =PP1V5_S0_PCH_VCCVRM_PCIE
15 =PP1V5_S0_PCH_VCCVRM_SATA
15 =PP1V5_S0_PCH_VCCVRM_CLK
15 =PP1V5_S0_PCH_VCCVRM_THRM
C1740 10UF 20% 10V X5R-CERM 0402-1
BYPASS=U1100.AF34::2.54mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
70 15 =PP1V05_S0_PCH_VCCASW
670mA Max, 34mA Idle
C1750 20UF 20% 4V X5R-CERM 0402
C1751 1.0UF 20% 6.3V X5R 0201-1
C1752 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AA18::2.54mm
BYPASS=U1100.AA18::2.54mm
BYPASS=U1100.AA18::2.54mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
70 15 =PP1V05_S0_PCH_VCC
C1755 10UF 20% 10V X5R-CERM 0402-1
C1756 1.0UF 20% 6.3V X5R 0201-1
C1757 1.0UF 20% 6.3V X5R 0201-1
C1758 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AG18::2.54mm
BYPASS=U1100.AA24::2.54mm
BYPASS=U1100.AD20::2.54mm
BYPASS=U1100.AE18::2.54mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
70 15 =PP1V05_S0_PCH_VCCIO
C1760 10UF 20% 10V X5R-CERM 0402-1
C1761 1.0UF 20% 6.3V X5R 0201-1
C1762 1.0UF 20% 6.3V X5R 0201-1
C1763 1.0UF 20% 6.3V X5R 0201-1
C1764 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AK18::2.54mm
BYPASS=U1100.AK18::2.54mm
BYPASS=U1100.AK22::2.54mm
BYPASS=U1100.AK20::2.54mm
BYPASS=U1100.AM18::2.54mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
70 15 =PP1V05_S0_PCH_VCCUSBPLL
C1770 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1100.U35::2.54mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
70 15 =PP1V05_S0_PCH_VCCIO_FDI
C1772 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AN34::2.54mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
70 15 =PP1V05_S0_PCH_VCCIO_USB2
C1774 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1100.U30::2.54mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
70 15 14 =PP1V05_S0_PCH_V_PROC_IO
C1785 1.0UF 20% 6.3V X5R 0201-1
C1786 0.1UF 10% 6.3V CERM-X5R 0201
C1787 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1100.AJ12::2.54mm
BYPASS=U1100.AJ12::2.54mm
BYPASS=U1100.AJ12::2.54mm

70 =PP1V05_S0_PCH_VCCCLK
??mA Max, ??mA Idle
R1790 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603
PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F 15
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
NO STUFF
C1790 10UF 20% 10V X5R-CERM 0402-1
C1791 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AP45::12.7mm
BYPASS=U1100.AP45::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_SSC100
C1776 1.0UF 20% 6.3V X5R 0201-1
C1777 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AE30::2.54mm
BYPASS=U1100.AG30::2.54mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_CLK100
C1778 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AD35::2.54mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_CLK135
C1780 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AD34::2.54mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_SSC
C1782 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AA30::2.54mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,PF,0 OHM,(0200HM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014
PAGE TITLE
CPU & CHIPSET: PCH Decoupling
Apple Inc.
DRAWING NUMBER 051-1160
SIZE D
REVISION 2.0.0
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Extra BPM Testpoints

XDP_BPM_L<2>	TP1802	
XDP_BPM_L<3>	TP1803	
XDP_BPM_L<4>	TP1804	
XDP_BPM_L<5>	TP1805	
XDP_BPM_L<6>	TP1806	
XDP_BPM_L<7>	TP1807	

CPU Micro2-XDP

59 10 8 6 5 =PPVCCIO_S0_CPU

70 18 =PP1V05_S0_XDP

R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
XDP_CPU_TCK	TCK1	TDI	XDP_CPU_TDI
	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	

998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NC per Intel DPDG.

XDP_CPU_PRESENT_L

R1831 1K 5% 1/16W MF-LF 402

C1804 0.1UF 20% 10V CERM 402

C1800 0.1UF 20% 10V CERM 402

C1801 0.1UF 20% 10V CERM 402

C1806 0.1UF 20% 10V CERM 402

CPU-PCH JTAG Chain Support

To link CPU and PCH JTAG pull ICT_JTAG_EN to 5V (must be in S0)

TP1845 ICT_JTAG_EN

Q1840 DMN5L06VK-7 SOT563

XDP_CPU_TMS — PLACE_NEAR=J1800.57:5.08mm — XDP_CPU_PCH_TMS

TP1840

Q1840 DMN5L06VK-7 SOT563

XDP_CPU_TCK — PLACE_NEAR=J1800.58:5.08mm — XDP_CPU_PCH_TCK

TP1841

Q1842 DMN32D2LFB4 DFN1006B4-3 SYM_VER_3

XDP_CPU_TDO — PLACE_NEAR=J1800.51:5.08mm — XDP_CPU_TDO_PCH_TDI

Q1846 DMN5L06VK-7 SOT563 — XDP_PCH_TMS — PLACE_NEAR=J1850.57:10mm

Q1846 DMN5L06VK-7 SOT563 — XDP_PCH_TCK — PLACE_NEAR=J1850.58:10mm

Q1848 DMN32D2LFB4 DFN1006B4-3 SYM_VER_3 — XDP_PCH_TDI — PLACE_NEAR=J1850.55:5.08mm

R1842 1M 5% 1/20W MF 201

R1841 1M 5% 1/20W MF 201

R1840 1M 5% 1/20W MF 201

R1845 1K 5% 1/20W MF 201

U1830

TPS720105
SON
XDP

70 69 68 67 19 =PP3V3_S5_PWRCTL

C1830 0.1UF 10% 16V X7R-CERM 0402

R1833 150 5% 1/16W MF-LF 402

PM_EN_REG_P1V05_S5

C1832 0.1UF 10% 6.3V CERM-X5R 0201

BIAS, IN, EN, OUT, NC, GND, THRM PAD

PP1V05_S5_LDO

C1831 2.2UF 10% 6.3V X5R 402 XDP

R1805 1K 5% 1/20W MF 201 — CPU_RESET_L

PCH Micro2-XDP

=PP3V3_S5_XDP 70

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM

OBSFN_A0	NC	OBSFN_C0	XDP_FC0_HDD_PWR_EN
OBSFN_A1	NC	OBSFN_C1	XDP_FC1_MEM_GOOD_LED
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_DP_AUXCH_ISOL_L
XDP_DA1_USB_EXTC_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_SATARDRVR_EN
XDP_DA2_SSD_PWR_EN	OBSDATA_A2	OBSDATA_C2	XDP_DC2_PCH_GPIO36
XDP_DA3_PCH_CAM_EXT_BOOT	OBSDATA_A3	OBSDATA_C3	XDP_DC3_JTAG_ISP_TCK
	OBSFN_B0	OBSFN_D0	NC
	OBSFN_B1	OBSFN_D1	NC
XDP_DB0_USB_EXTB_OC_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_PCH_GPIO16
XDP_DB1_USB_EXTD_OC_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_MLB_RAMCFG1
XDP_DB2_SSD_SR_EN_L	OBSDATA_B2	OBSDATA_D2	XDP_DD2_ENETSD_CLKREQ_L
XDP_DB3_SDCONN_STATE_CHANGE_L	OBSDATA_B3	OBSDATA_D3	XDP_DD3_AP_CLKREQ_L
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	
	VCC_OBS_AB	VCC_OBS_CD	
	HOOK2	RESET#/HOOK6	XDP_PM_PCH_PWROK
	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

C1880 0.1UF 20% 10V CERM 402

C1881 0.1UF 20% 10V CERM 402

R1870 1K 5% 1/20W MF 201 — PM_PCH_PWROK

PP1V05_S5_LDO

R1860 51 1% 1/20W MF 201 — XDP_PCH_TDO — J1850.51:2.54mm

R1861 51 1% 1/20W MF 201 — XDP_PCH_TDI — U1100.AE2:35mm

R1862 51 1% 1/20W MF 201 — XDP_PCH_TMS — U1100.AD1:31mm

R1866 51 5% 1/20W MF 201 — XDP_PCH_TCK

SYSTEM SIGNALS / PCH/XDP SIGNALS

OMIT (All 12 R's)

USB_EXTA_OC_L	R1890	SHORT	XDP_DA0_USB_EXTA_OC_L	13 18
USB_EXTC_OC_L	R1893	SHORT	XDP_DA1_USB_EXTC_OC_L	13 18
PCH_CAM_EXT_BOOT	R1895	SHORT	XDP_DA3_PCH_CAM_EXT_BOOT	11 18
USB_EXTB_OC_L	R1880	SHORT	XDP_DB0_USB_EXTB_OC_L	13 18
USB_EXTD_OC_L	R1881	SHORT	XDP_DB1_USB_EXTD_OC_L	13 18
SSD_SR_EN_L	R1887	SHORT	XDP_DB2_SSD_SR_EN_L	13 18
SDCONN_STATE_CHANGE_L	R1897	SHORT	XDP_DB3_SDCONN_STATE_CHANGE_L	13 18
JTAG_ISP_TCK_PCH	R1875	SHORT	XDP_DC3_JTAG_ISP_TCK	14 18
ENETSD_CLKREQ_L	R1882	SHORT	XDP_DD2_ENETSD_CLKREQ_L	11 18
AP_CLKREQ_L	R1883	SHORT	XDP_DD3_AP_CLKREQ_L	11 18
HDD_PWR_EN	R1886	SHORT	XDP_FC0_HDD_PWR_EN	14 18
MEM_GOOD_LED	R1891	SHORT	XDP_FC1_MEM_GOOD_LED	14 18
SSD_PWR_EN	R1892	SHORT	XDP_DA2_SSD_PWR_EN	13 18

Set of PCH-XDP routes must be length matched
to <= 25 ps, as per Intel debug spec.

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).

TDI and TMS are terminated in CPU.

70 18 =PP1V05_S0_XDP

XDP_CPU_TDO	R1820 51	PLACE_NEAR=U0500.N54:12.5MM
XDP_CPU_TCK	R1823 51	PLACE_NEAR=U0500.N54:12.5MM
XDP_CPU_TRST_L	R1824 51	PLACE_NEAR=U0500.M53:12.5MM

CPU & CHIPSET: CPU & PCH XDP

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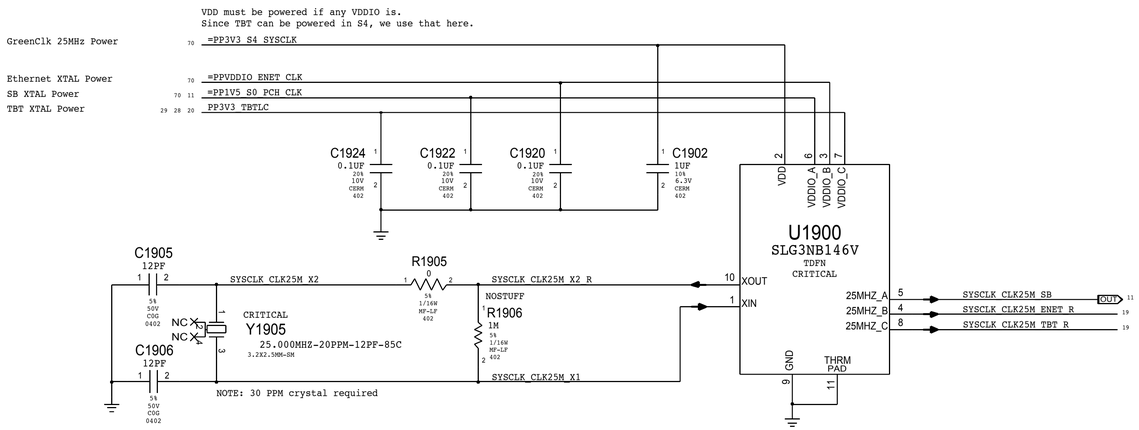
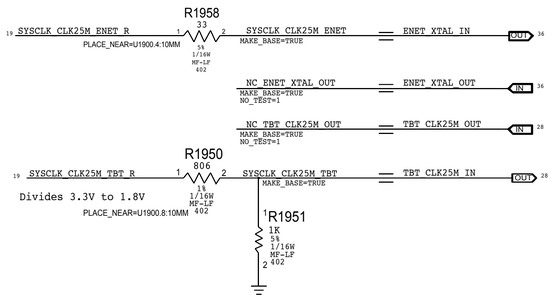
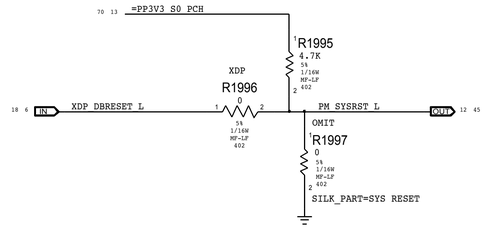
System 25MHz Clock Generator



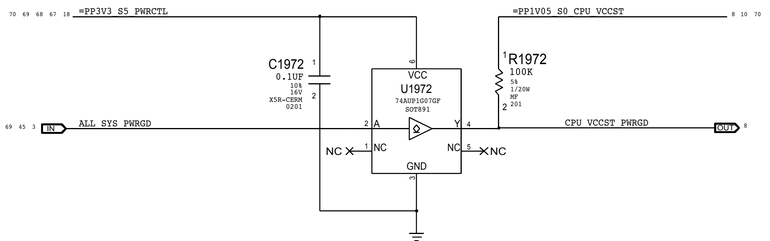
Clock aliases



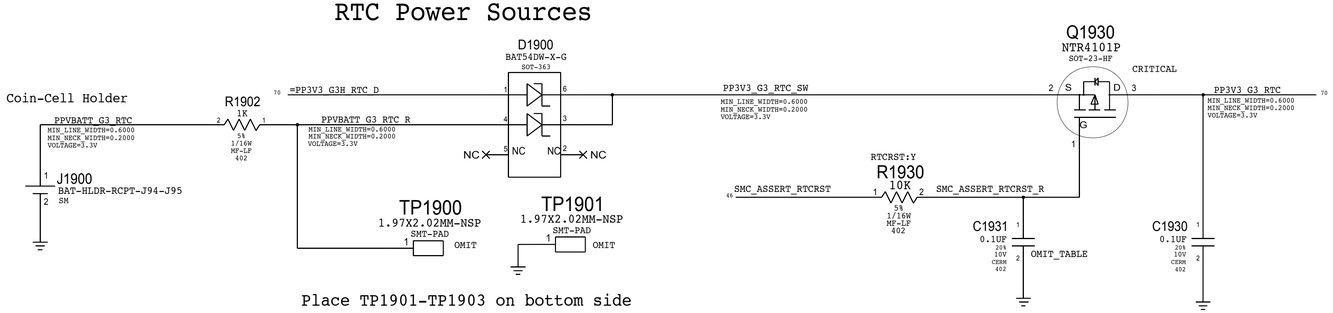
PCH Reset Button



ALL_SYS_PWRGD/CPU_VCCST Level Shifter

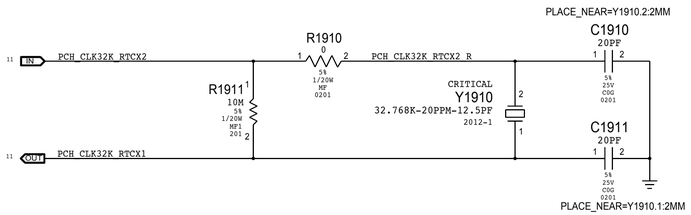


RTC Power Sources

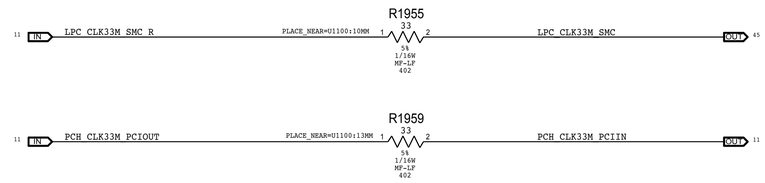


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1059	1	CAP,0.1 UF,402	C1931	RTCRST:Y
116S0090	1	RES,10K ohm,402	C1931	RTCRST:N

PCH RTC Crystal

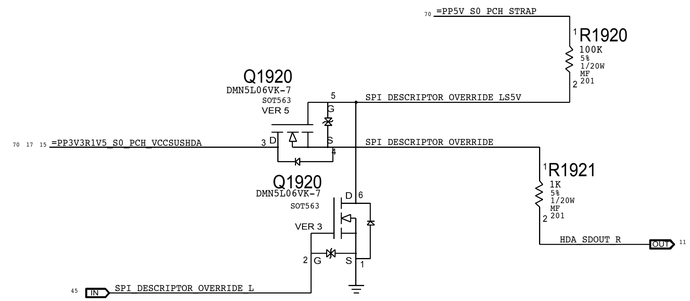


Clock series termination



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



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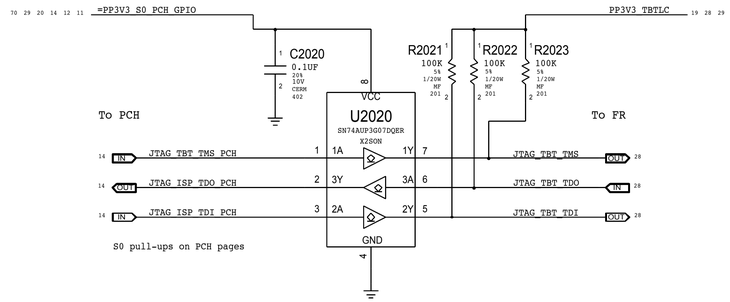
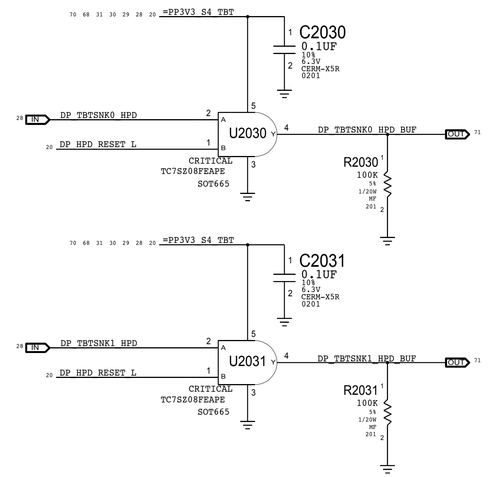
Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH



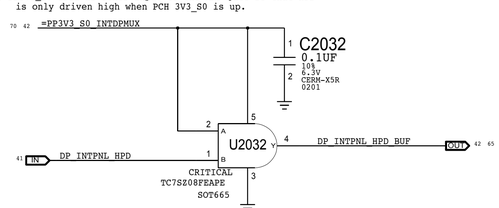
Falcon Ridge HPD Isolation

NOTE: PLT_RESET_L used as other input to the AND gate so that HPD is only driven high to the PCH in S0.



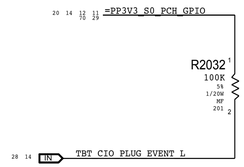
Internal Display HPD Isolation

NOTE: PP3V3_S0 used as other input to the AND gate so that HPD is only driven high when PCH 3V3_S0 is up.

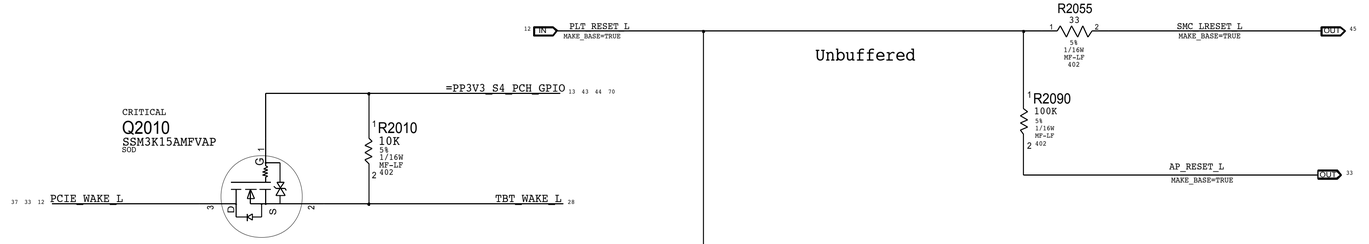


Falcon Ridge Support

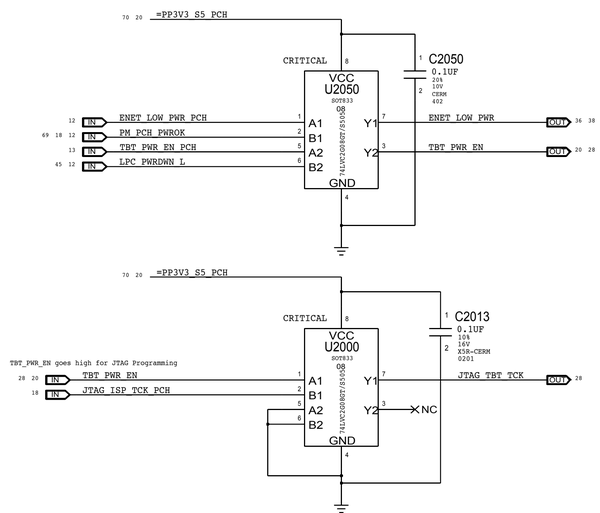
FR output is open-drain, no isolation necessary



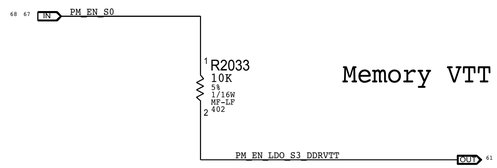
Platform Reset Connections



GPIO Glitch Prevention



Memory VTT Enable



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PAGE TITLE

CPU & CHIPSET: Project-Specific Chipset Support

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Memory Bit/Byte Swizzle

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DRAM: DDR3 Signal Aliases

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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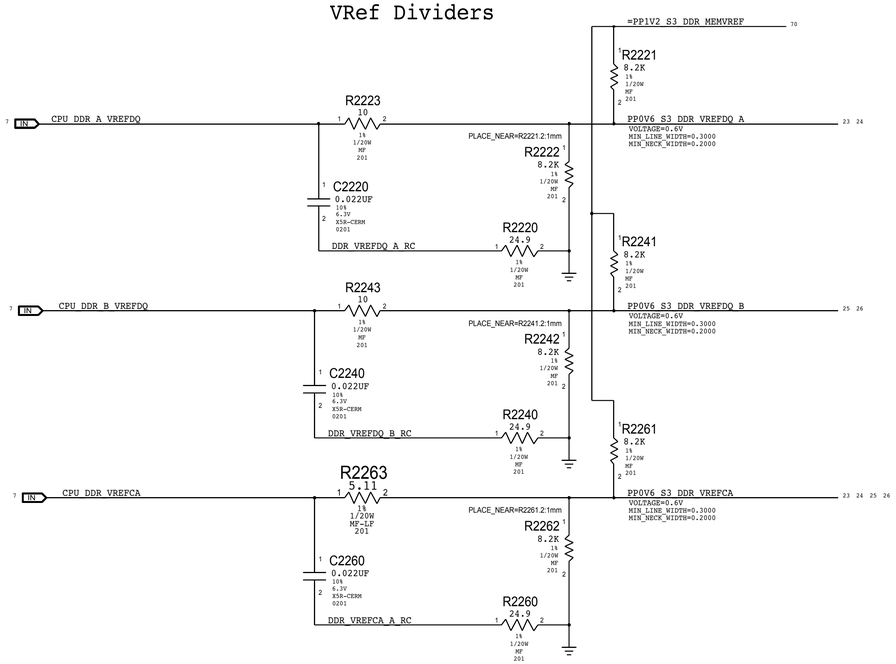
VRef Dividers



SYNC_MASTER=J117_ANDRES SYNC_DATE=02/27/2014

PAGE TITLE

DRAM: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

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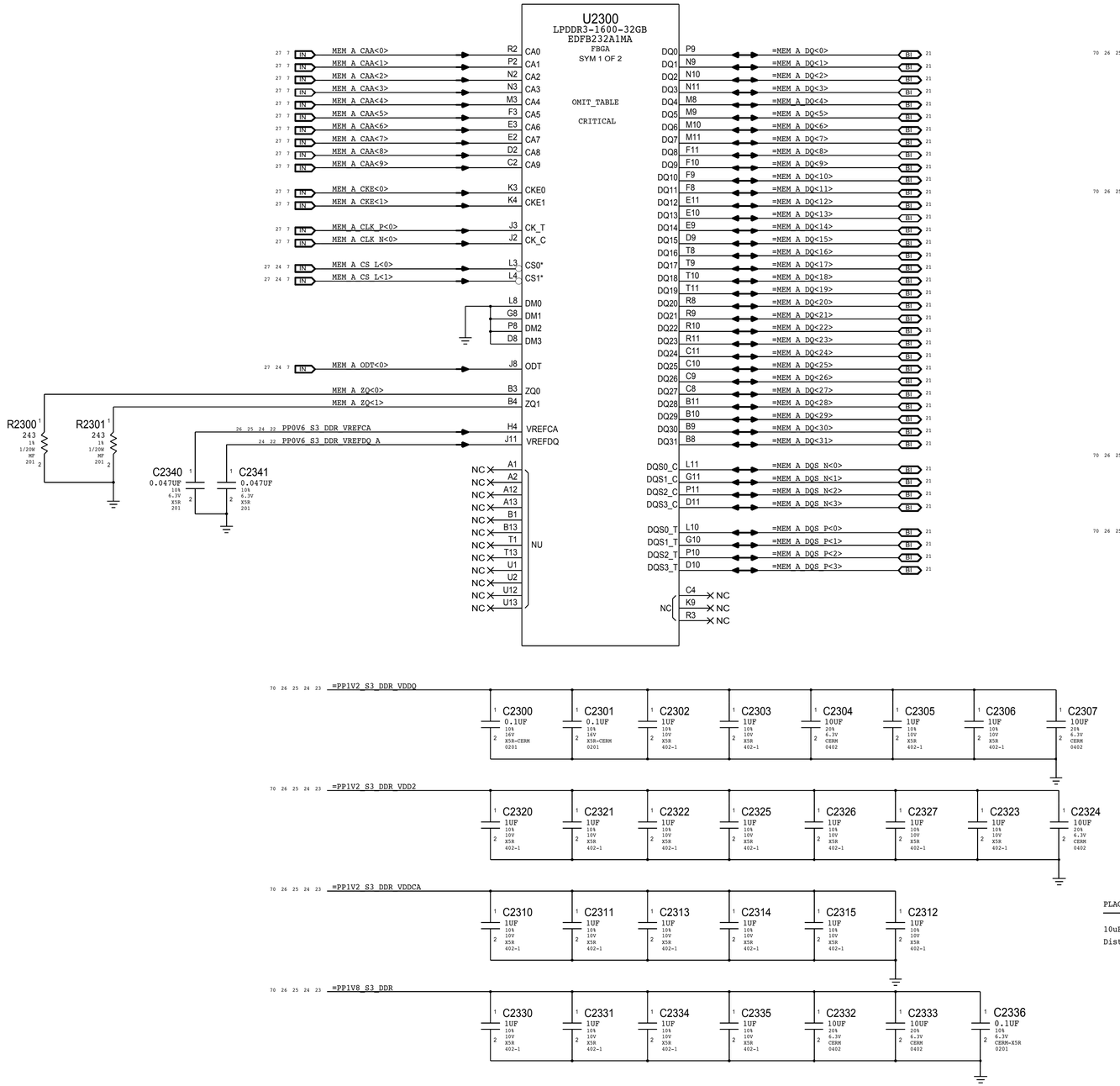
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

DRAM: LPDDR3 Channel A (0-31)

Apple Inc.

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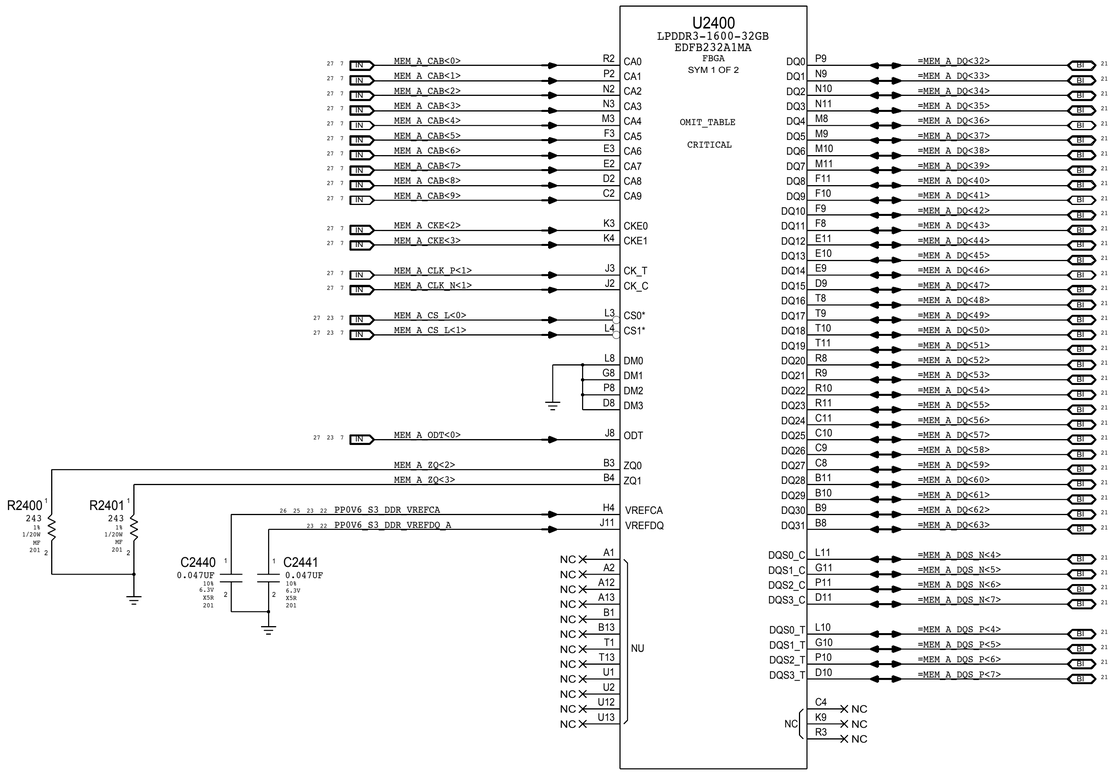
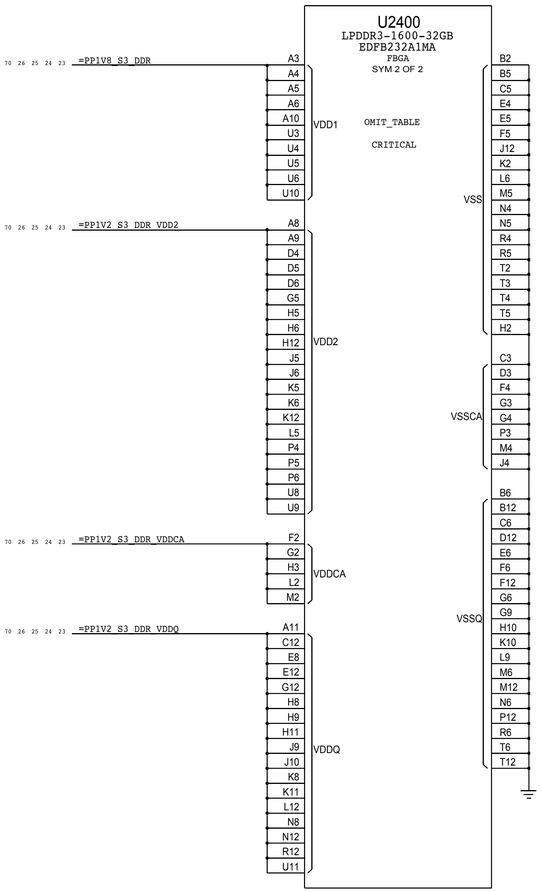
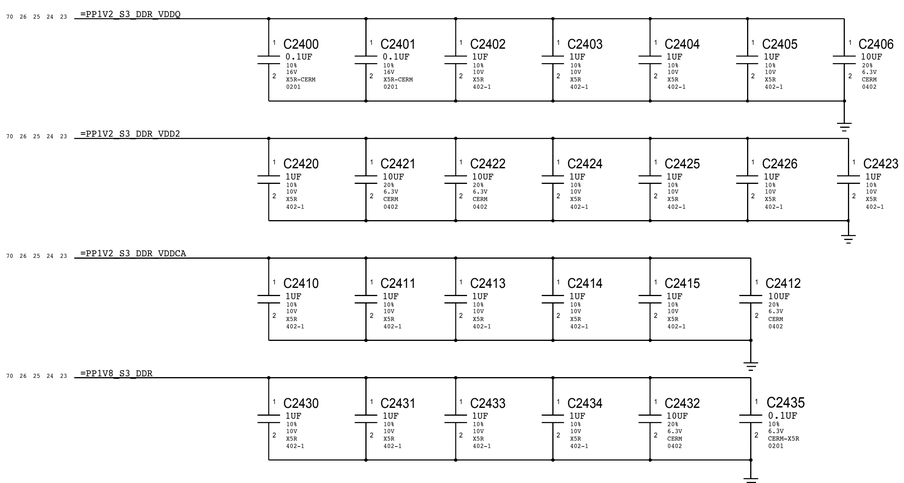
LPDDR3 CHANNEL A (32-63)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB	SYNC_DATE=09/03/2013
PAGE TITLE: DRAM: LPDDR3 Channel A (32-63)	
Apple Inc.	DRAWING NUMBER: 051-1160
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	REVISION: 2.0.0
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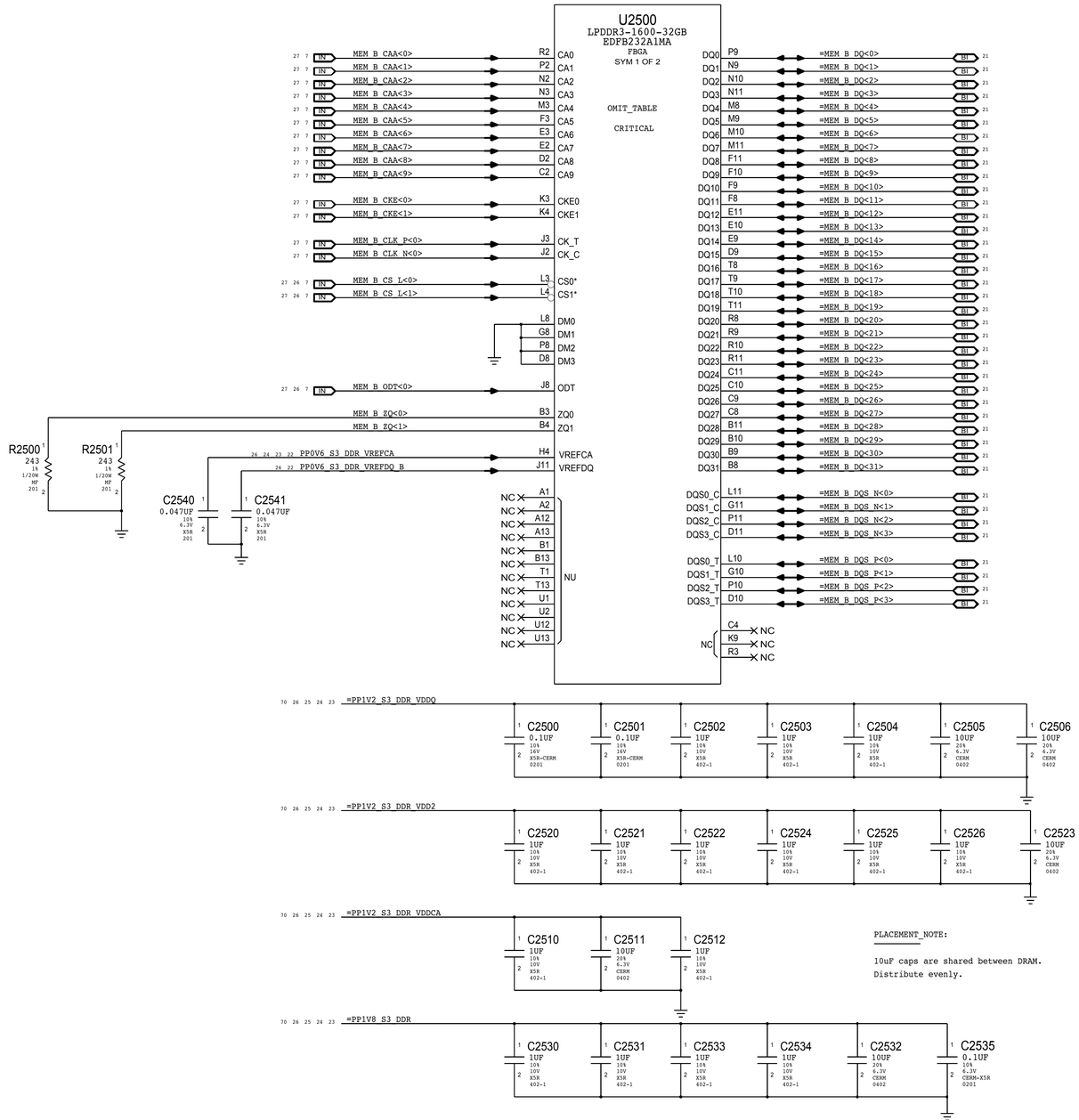
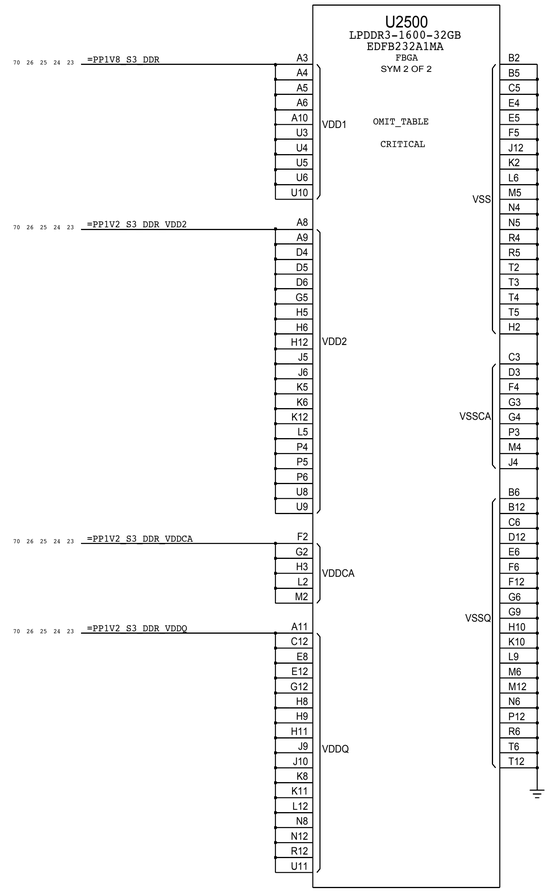
LPDDR3 CHANNEL B (0-31)





PLACEMENT_NOTE:

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Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

DRAM: LPDDR3 Channel B (0-31)

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

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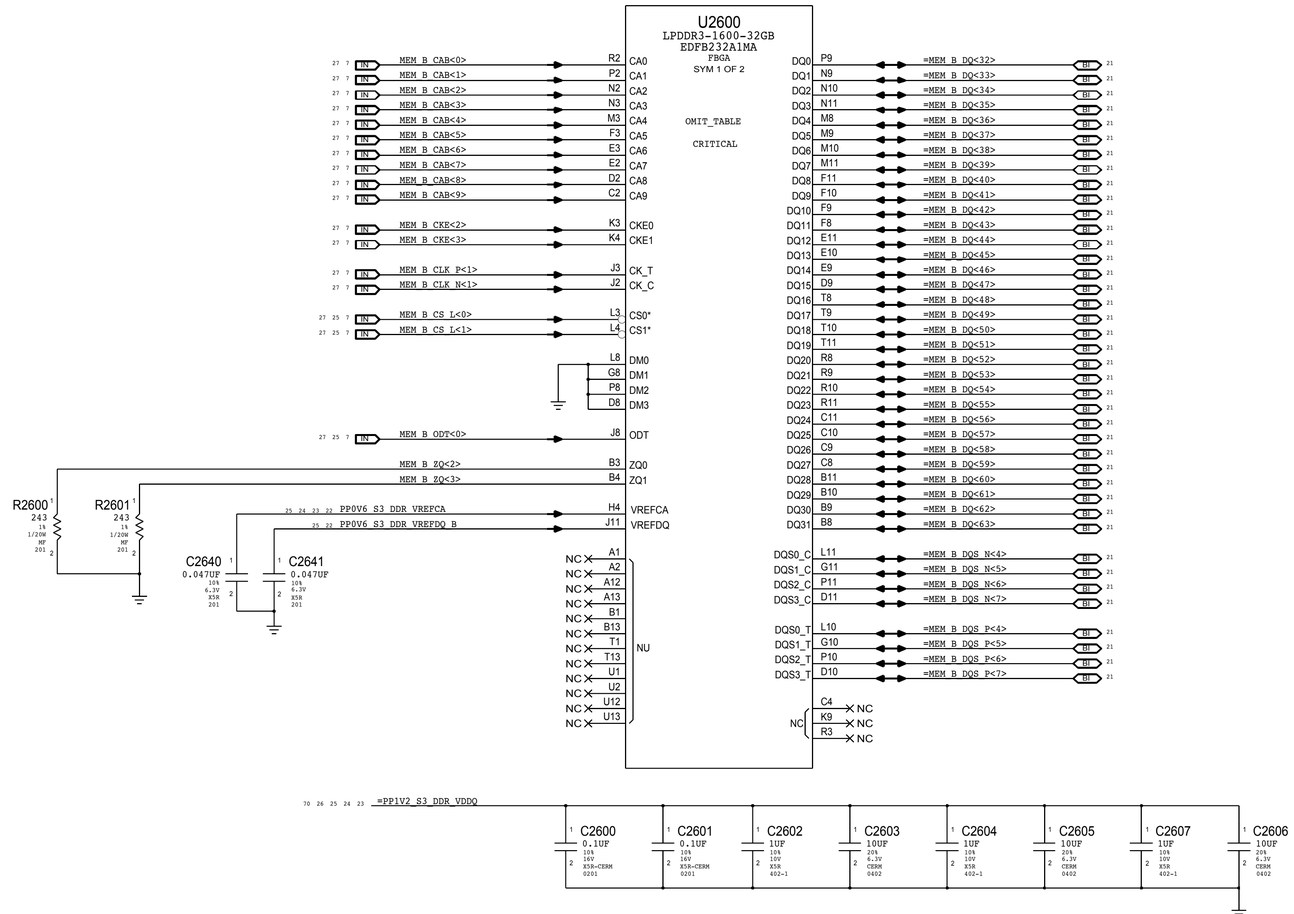
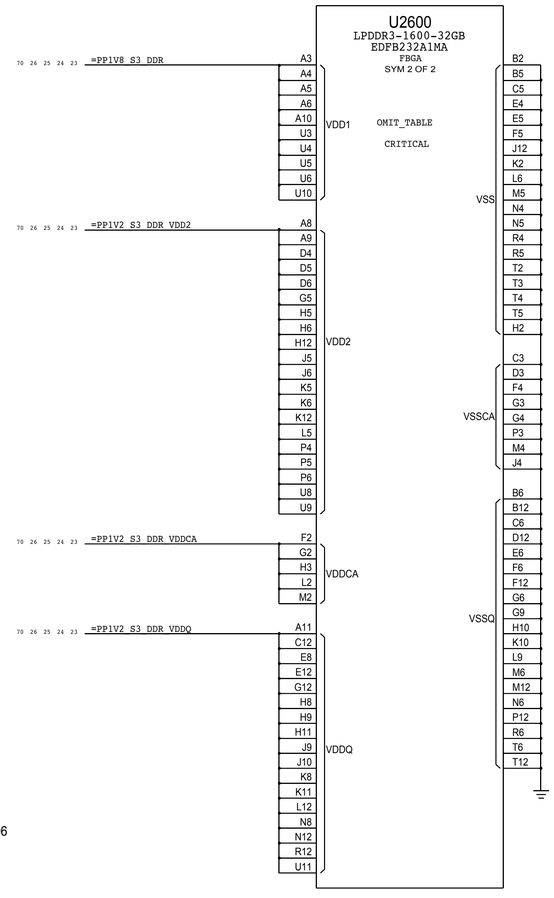
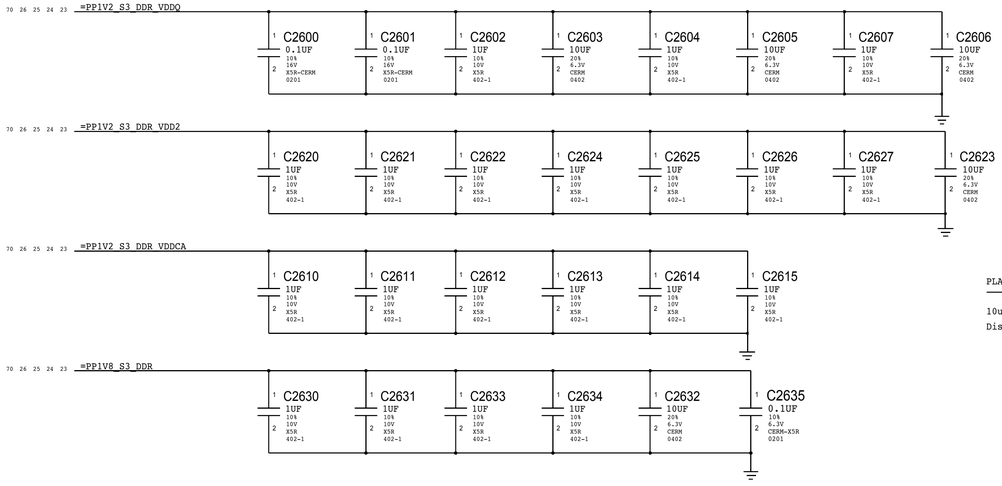
LPDDR3 CHANNEL B (32-63)







PLACEMENT_NOTE:

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Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

DRAM: LPDDR3 Channel B (32-63)

Apple Inc.

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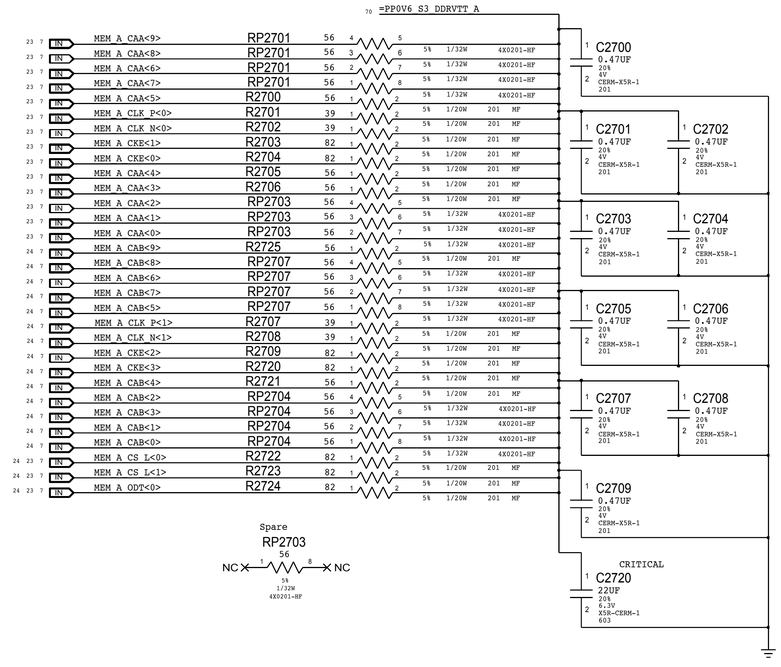
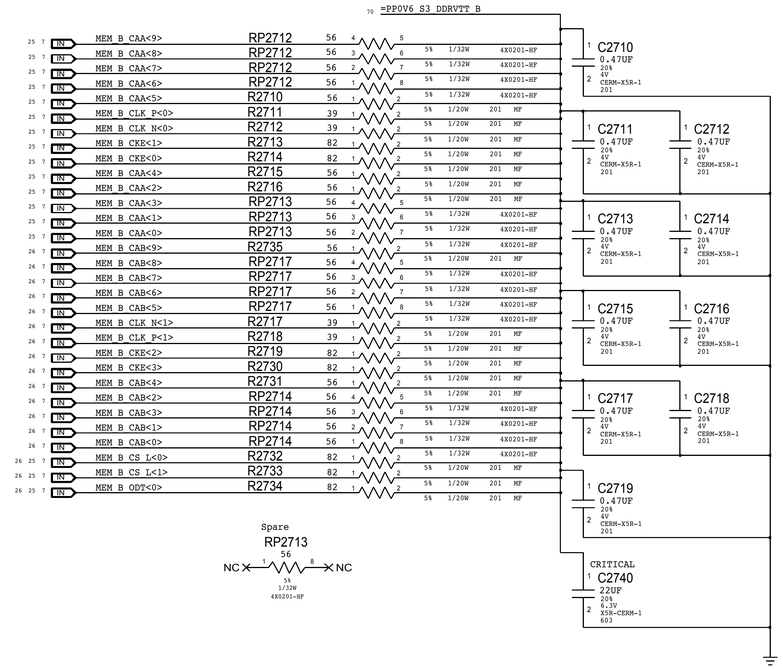
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC_MASTER=J41_MLB	SYNC_DATE=09/03/2013
PAGE TITLE	DRAM: LPDDR3 Termination
Apple Inc.	DRAWING NUMBER 051-1160 SIZE D
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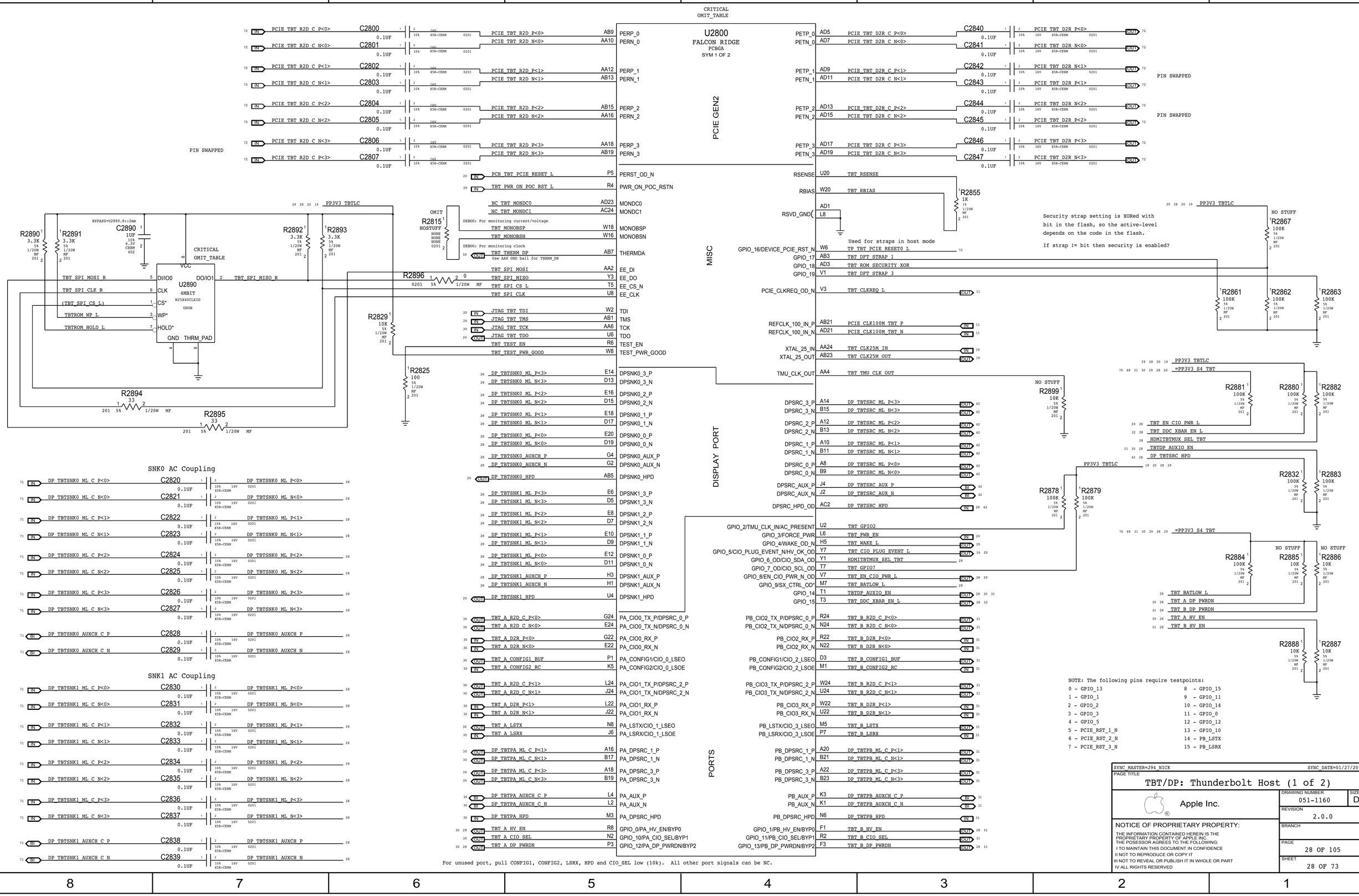

SYNC_MASTER=J94_NICK SYNC_DATE=01/27/2014

PAGE TITLE

TBT/DP: Thunderbolt Host (1 of 2)

Apple Inc.

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U2950

Part	SLG5AP304V
Type	Load Switch
R(on) @ 1.05V	7.8 mOhm Typ 9.6 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch

Internal switch not functional on RR.

=PP3V3_S4_TBT

C2940 1.0UF 20% 6.3V X5R 0201-1

PP1V05_TBT

U2940 SLG5AP304V TDFN CRITICAL

VDD, GND, D, S, CAP, ON

TBT_CIO_FET_CAP

TBT_EN_CIO_PWR

PP3V3_TBTLC

R2945 100K 5% 1/20W MF 201

C2941 0.0022UF 10% 50V CERM 402

Q2945 DMN5L06VK-7 SOT563

VER 3

=PP3V3_S0_PCH_GPIO

Pull-up (S0) on PCH page

TBT_PWR_REQ_L

TBT_EN_CIO_PWR_L

Q2945 DMN5L06VK-7 SOT563

PP1V05_TBTRDV

MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V

700 mA EDP

C2900 C2901 C2902 C2903 C2904 C2905 C2906 1.0UF 20% 6.3V X5R 0201-1

PP1V05_TBTCIO

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V

1200 mA EDP

C2930 C2931 C2932 1.0UF 20% 6.3V X5R 0201-1

U2800

FALCON RIDGE
FCBGA
SYM 2 OF 2

VCC1P0_CIO

VCC1P0_RDV_DECAP

VCC

SVR input to RR - 1100 mA EDP

POC input to RR - 150 mA EDP

VCC3P3

Isolated to reduce noise from SVR

PP1V05_TBT

MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V

C2910 C2911 1.0UF 20% 6.3V X5R 0201-1

SVR_VCC1P0

VCC3P3_LC

PP3V3_TBTLC

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
VOLTAGE=3.3V

100 mA EDP

C2970 1.0UF 20% 6.3V X5R 0201-1

VCC3P3_RDV_DECAP

=PP3V3_S4_TBT

3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A

PLACE_NEAR=C2952:1:3mm

C2950 C2951 C2952 C2953 10UF 20% 6.3V CERM-X5R 0402-1

XW2960

CRITICAL

L2920 680NH-30%-3.6A-35MOHM SM

1900 mA EDP

P1V05TBT_SW

MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE
SWITCH_MODE=TRUE

C2923 C2922 C2921 C2920 10UF 20% 6.3V CERM-X5R 0402-1

SVR_IND

SVR_AMON

NC

CRITICAL

D2920L SOD-323 NSR1020MW2T1G

PP3V3_TBTRDV

MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V

25 mA EDP

C2980 C2981 1.0UF 20% 6.3V X5R 0201-1

PP3V3_S4_TBT_F

MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V

C2960 C2961 1.0UF 20% 6.3V X5R 0201-1

A2, B1, and C2 are the ground current pins for A4, A6, and B3.
They should be routed as a shape to the annode of D2920.

GND

VSS

TBT "POC" Power-up Reset

=PP3V3_S4_TBT

SMC_DELAYED_PWRGD

=PP3V3_S0_PCH_GPIO

TBT_POC_RESET_L

Q2995 DMN32D2LFB4 DFN1006B4-3

SYM_VER_3

R2995 100K 5% 1/20W MF 201

R2990 100K 5% 1/20W MF 201

R2992 100K 5% 1/20W MF 201

C2995 330PF 10% 16V X7R 0201

R2991 24.9K 1% 1/20W MF 201

U2990 TPS3895ADRY USON

VCC, ENABLE, SENSE, GND, SENSE_OUT, CT

TBTPOCRST_MR_L

TBTPOCRST_SENSE

TBTPOCRST_CT

TBT_PWR_ON_POC_RST_L

Push-pull output

C2990 0.1UF 10% 25V X5R 402

C2991 0.001UF 10% 50V X7R-CERM 0402

Vth = 2.508V nominal

Delay = 4.04ms nominal

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=J70_NICK SYNC_DATE=01/12/2014

PAGE TITLE

TBT/DP: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-1160
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

For 12V systems:

I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A

	Min	Max
IV3P3	1040mA	1155mA
IHVS0/S3	1060mA	1180mA (12W minimum)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0398	128S0220		ALL	3.3V INPUT CAP

70 =PP3V3_S4_TBTAPWRSW
70 =PPHV_SW_TBTAPWRSW
18.9V Max

C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM-1 603
C3281 0.1UF 20% 10V CERM 402
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 50V X7R 603-1

U3210 CD3211A1RGP QFN

19	V3P3	V3P3OUT	18 NC
20			
6		OUT	12
7	VHV		14
16	ENHVU	FAULTZ	4
5	EN	ISET_V3P3	8
11	HV_EN	ISET_S0	10
17	S0	ISET_S3	9
	GND	THRM PAD	21

68 IN =TBTAPWRSW_EN
28 IN TBT_A_HV_EN
68 31 IN =TBT_S0_EN

PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=15V
C3211 0.1UF 10% 50V X7R 603-1

R3210 35.7K 1% 1/20W MF 201
R3211 35.7K 1% 1/20W MF 201
R3212 36.5K 1% 1/16W MF-LF 402

70 68 31 29 28 20 =PP3V3_S4_TBT

C3220 0.1UF 10% 6.3V CERM-X5R 0201
C3221 0.1UF 10% 6.3V CERM-X5R 0201

GND_VOID=TRUE (Both C's)

POLARITY SWAPPED

28 OUT TBT_A_D2R_P<1>	C3277 0.47UF 20% 4V CERM-X5R-1 201	TBT_A_D2R_C_N<1>	GND_VOID=TRUE	7 TB-
28 OUT TBT_A_D2R_N<1>	C3276 0.47UF 20% 4V CERM-X5R-1 201	TBT_A_D2R_C_P<1>	GND_VOID=TRUE	8 TB+
28 IN DP_TBTPA_AUXCH_C_N	C3230 0.1UF 10% 6.3V CERM-X5R 0201	DP_TBTPA_AUXCH_N		1 AUX-
28 IN DP_TBTPA_AUXCH_C_P	C3231 0.1UF 10% 6.3V CERM-X5R 0201	DP_TBTPA_AUXCH_P		2 AUX+
		32 IN DP_TBTPA_DDC_DATA		4 DDC_DAT
		32 IN DP_TBTPA_DDC_CLK		5 DDC_CLK
		28 OUT TBT_A_CONFIG1_BUF		16 CA_DETOUT
28 IN DP_TBTPA_ML_C_P<1>	C3232 0.22UF 20% X5R 0201	DP_TBTPA_ML_P<1>		11 DP+
28 IN DP_TBTPA_ML_C_N<1>	C3233 0.22UF 20% X5R 0201	DP_TBTPA_ML_N<1>		10 DP-
		28 IN TBT_A_LSTX		14 LSTX
		28 OUT TBT_A_LSRX		13 LSRX
		28 OUT DP_TBTPA_HPD		12 HPDOUT

VDD
CRITICAL
U3220 CBTL05024 HVQFN24-COMBO

TB_ENA	15	TBT_A_CIO_SEL IN 28
AUXIO_EN	24	TBTDP_AUXIO_EN IN 28 31
DP_PD	6	TBT_A_DP_PWRDN IN 28
AUXIO-	23	GND_VOID=TRUE TBT_A_D2R1_AUXDDC_N 30
AUXIO+	22	TBT_A_D2R1_AUXDDC_P 30
		GND_VOID=TRUE TBT: RX_1
CA_DET	18	TBT_A_CONFIG1_RC 30
DPMLO+	19	DP_A_LSX_ML_P<1> 30
DPMLO-	20	DP_A_LSX_ML_N<1> 30
		TBT: LSX_A_R2P/P2R (P/N)
HPD	17	TBT_A_HPD 30

GND_THMPAD
9 21 25

Thunderbolt Connector A

L3200 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=15V

C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402

TBTACONN_20_RC
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V

R3201 12 5% 1/20W MF 201

TBTACONN_1_C
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V
(0-18.9V)

C3205 0.01UF 10% 25V X5R-CERM 0201

TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
DP: Lane 0 TBT: TX_0

GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<0> IN 28
TBT_A_R2D_C_N<0> IN 28

GND_VOID=TRUE
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201

TBTACONN_7_C
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V
(0-18.9V)

C3206 0.01UF 10% 25V X5R-CERM 0201

DP_A_LSX_ML_P<1> 30
DP_A_LSX_ML_N<1> 30
DP: Lane 1

TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
DP: Lane 2 TBT: TX_1

GND_VOID=TRUE (Both C's)
POLARITY SWAPPED
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_N<1> IN 28
TBT_A_R2D_C_P<1> IN 28

GND_VOID=TRUE
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201

470k R's for ESD protection
on AC-coupled signals.

CRITICAL
J3200 DUAL-MDP-K70 F-ANG-TH PORT A

HPD	2	GND0	1
CONFIG1	4	ML_LANE0P	3
CONFIG2	6	ML_LANE0N	5
GND2	8	GND1	7
ML_LANE3P	10	ML_LANE1P	9
ML_LANE3N	12	ML_LANE1N	11
GND4	14	GND3	13
AUX_CHP	16	ML_LANE2P	15
AUX_CHN	18	ML_LANE2N	17
DP_PWR	20	RETURN	19

SHLD: 46 45 44 43 42 41
SHLD: 65 52 51 50 49 48 47

J70:514-0824 / J78:514-0831

POLARITY SWAPPED
GND_VOID=TRUE (Both C's)

28 OUT TBT_A_D2R_N<0>	C3274 0.47UF	TBT_A_D2R_C_P<0>	
28 OUT TBT_A_D2R_P<0>	C3275 0.47UF	TBT_A_D2R_C_N<0>	

TBT: RX_0

GND_VOID=TRUE
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=1
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=1

POLARITY SWAPPED

28 IN DP_TBTPA_ML_C_N<3>	C3278 0.22UF	DP_TBTPA_ML_P<3>	R3278 470K 5% 1/20W MF 201
28 IN DP_TBTPA_ML_C_P<3>	C3279 0.22UF	DP_TBTPA_ML_N<3>	R3279 470K 5% 1/20W MF 201

TBT: Terminated
DP: Lane 3

30 TBT_A_D2R1_AUXDDC_P
30 TBT_A_D2R1_AUXDDC_N
TBT: RX_1

30 TBT_A_HPD
30 TBT_A_CONFIG1_RC
28 OUT TBT_A_CONFIG2_RC

R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R 0201
C3295 330PF 10% 16V X7R 0201
R3241 100K 5% 1/20W MF 201

C3202 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J70_NICK SYNC_DATE=10/16/2013
PAGE TITLE: TBT/DP: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D
REVISION 2.0.0
BRANCH
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

For 12V systems:

I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A

	Min	Max
IV3P3	1040mA	1155mA
IHVS0/S3	1060mA	1180mA (12W minimum)

70 =PP3V3_S4_TBTBPWRSW

CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C3380 22UF 20% 6.3V X5R-CERM-1 603
C3381 0.1UF 20% 10V CERM 402

70 =PPHV_SW_TBTBPWRSW
18.9V Max

C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 50V X7R 603-1

CRITICAL U3310 CD3211A1RGP QFN

19	V3P3	V3P3OUT	18
20			NC
6		OUT	12
7	VHV		14
16	ENHVU	FAULTZ	4
5	EN	ISET_V3P3	8
11	HV_EN	ISET_S0	10
17	S0	ISET_S3	9
	GND	THRM PAD	21

PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=15V
C3311 0.1UF 10% 50V X7R 603-1

68 30 IN =TBT_S0_EN
28 IN TBT_B_HV_EN
68 IN =TBTBPWRSW_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3

R3310 35.7K 1% 1/20W MF 201
R3311 35.7K 1% 1/20W MF 201
R3312 36.5K 1% 1/16W MF-LF 402

70 68 30 29 28 20 =PP3V3_S4_TBT

C3320 0.1UF 10% 6.3V CERM-X5R 0201
C3321 0.1UF 10% 6.3V CERM-X5R 0201

VDD
CRITICAL U3320 CBTL05024 HVQFN24-COMBO

GND_VOID=TRUE
(Both C's)

28 OUT TBT_B_D2R_P<1> — C3377 0.47UF 20% 4V CERM-X5R-1 201 — POLARITY SWAPPED — TBT_B_D2R_C_N<1> — GND_VOID=TRUE — 7 TB-
28 OUT TBT_B_D2R_N<1> — C3376 0.47UF 20% 4V CERM-X5R-1 201 — TBT_B_D2R_C_P<1> — GND_VOID=TRUE — 8 TB+
28 BI DP_TBTPB_AUXCH_C_N — C3330 0.1UF 10% 6.3V CERM-X5R 0201 — DP_TBTPB_AUXCH_N — 1 AUX-
28 BI DP_TBTPB_AUXCH_C_P — C3331 0.1UF 10% 6.3V CERM-X5R 0201 — DP_TBTPB_AUXCH_P — 2 AUX+
32 BI DP_TBTPB_DDC_DATA — 4 DDC_DAT
32 IN DP_TBTPB_DDC_CLK — 5 DDC_CLK
28 OUT TBT_B_CONFIG1_BUF — 16 CA_DETOUT
28 IN DP_TBTPB_ML_C_P<1> — C3332 0.22UF 20% X5R 0201 — DP_TBTPB_ML_P<1> — 11 DP+
28 IN DP_TBTPB_ML_C_N<1> — C3333 0.22UF 20% X5R 0201 — DP_TBTPB_ML_N<1> — 10 DP-
28 IN TBT_B_LSTX — 14 LSTX
28 OUT TBT_B_LSRX — 13 LSRX
28 OUT DP_TBTPB_HPD — 12 HPDOUT

TB_ENA	15		TBT_B_CIO_SEL IN 28
AUXIO_EN	24		TBTDP_AUXIO_EN IN 28 30
DP_PD	6		TBT_B_DP_PWRDN IN 28
AUXIO-	23	GND_VOID=TRUE	TBT_B_D2R1_AUXDDC_N 31
AUXIO+	22		TBT_B_D2R1_AUXDDC_P 31
CA_DET	18	GND_VOID=TRUE TBT: RX_1	TBT_B_CONFIG1_RC 31
DPMLO+	19		DP_B_LSX_ML_P<1> 31
DPMLO-	20		DP_B_LSX_ML_N<1> 31
		TBT: LSX_B_R2P/P2R (P/N)	
HPD	17		TBT_B_HPD 31

GND_THMPAD
3 21 25

Thunderbolt Connector B

L3300 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=15V

C3300 0.01UF 10% 50V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_20_RC
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V

R3301 5K 1/20W MF 201

TBTBCONN_1_C
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V

C3305 0.01UF 10% 25V X5R-CERM 0201

(0-18.9V)
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
DP: Lane 0 TBT: TX_0

GND_VOID=TRUE
(Both C's)
C3370 0.22UF 20% X5R 0201 — TBT_B_R2D_C_P<0> IN 28
C3371 0.22UF 20% X5R 0201 — TBT_B_R2D_C_N<0> IN 28
GND_VOID=TRUE R3370 470K 5% 1/20W MF 201
GND_VOID=TRUE R3371 470K 5% 1/20W MF 201

CRITICAL
J3200 DUAL-MDP-K70 F-ANG-TH

HPD	22	GND0	21
CONFIG1	24	ML_LANE0P	23
CONFIG2	26	ML_LANE0N	25
GND2	28	GND1	27
ML_LANE3P	30	ML_LANE1P	29
ML_LANE3N	32	ML_LANE1N	31
GND4	34	GND3	33
AUX_CHP	36	ML_LANE2P	35
AUX_CHN	38	ML_LANE2N	37
DP_PWR	40	RETURN	39

SHLD 50 57 56 55 54 53
PORT B SHLD 65 64 63 62 61 60 59

C3306 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_7_C
MIN_LINE_WIDTH=0.3800
MIN_NECK_WIDTH=0.2000
VOLTAGE=18.9V

(0-18.9V)
DP_B_LSX_ML_P<1> 31
DP_B_LSX_ML_N<1> 31
DP: Lane 1

GND_VOID=TRUE
(Both C's)
POLARITY SWAPPED
C3372 0.22UF 20% X5R 0201 — TBT_B_R2D_C_N<1> IN 28
C3373 0.22UF 20% X5R 0201 — TBT_B_R2D_C_P<1> IN 28
GND_VOID=TRUE R3372 470K 5% 1/20W MF 201
GND_VOID=TRUE R3373 470K 5% 1/20W MF 201

TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
DP: Lane 2 TBT: TX_1

470k R's for ESD protection
on AC-coupled signals.

POLARITY SWAPPED
GND_VOID=TRUE
(Both C's)
C3374 0.47UF 20% 4V CERM-X5R-1 201 — 28 OUT TBT_B_D2R_N<0> — TBT_B_D2R_C_P<0>
C3375 0.47UF 20% 4V CERM-X5R-1 201 — 28 OUT TBT_B_D2R_P<0> — TBT_B_D2R_C_N<0>

GND_VOID=TRUE R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=1
GND_VOID=TRUE R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=1

TBT: RX_0

C3379 0.22UF 20% X5R 0201 — 28 IN DP_TBTPB_ML_C_P<3> — DP_TBTPB_ML_P<3>
C3378 0.22UF 20% X5R 0201 — 28 IN DP_TBTPB_ML_C_N<3> — DP_TBTPB_ML_N<3>
TBT: Terminated

R3378 470K 5% 1/20W MF 201
R3379 470K 5% 1/20W MF 201
DP: Lane 3

31 TBT_B_D2R1_AUXDDC_P
31 TBT_B_D2R1_AUXDDC_N
TBT: RX_1

J70:514-0824 / J78:514-0831

28 OUT TBT_B_HPD
31 TBT_B_CONFIG1_RC
28 OUT TBT_B_CONFIG2_RC

R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R 0201
C3395 330PF 10% 16V X7R 0201
R3341 100K 5% 1/20W MF 201

C3302 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J70_NICK	SYNC_DATE=10/16/2013
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DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.

70 =PP3V3_S0_DP

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

R3485 100K 5% 1/20W MF 201

C3480 0.1UF 20% 10V CERM 402

U3400
TSD810224
QFN
CRITICAL

	ENA		
30 OUT / BI DP_TBTPA_DDC_CLK / DP_TBTPA_DDC_DATA	INA+ / INA-	OUTA1+ / OUTA1-	R3451 2.2K 1% 1/20W MF 201
		OUTA0+ / OUTA0-	R3452 2.2K 1% 1/20W MF 201 → DP_TBTSNK1_DDC_CLK / DP_TBTSNK1_DDC_DATA → IN / BI 71
	SAI	SAO	
	ENB		
31 OUT / 31 BI DP_TBTPB_DDC_CLK / DP_TBTPB_DDC_DATA	INB+ / INB-	OUTB1+ / OUTB1-	R3453 2.2K 1% 1/20W MF 201
		OUTB0+ / OUTB0-	R3454 2.2K 1% 1/20W MF 201 → DP_TBTSNK0_DDC_CLK / DP_TBTSNK0_DDC_DATA → IN / BI 71
TBT_DDC_XBAR_EN	SBI	SBO	
	GND	THRM PAD	

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

Q3400
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

28 IN TBT_DDC_XBAR_EN_L

SYNC_MASTER=J70_TONY	SYNC_DATE=09/13/2013
PAGE TITLE: TBT/DP: DDC Crossbar	
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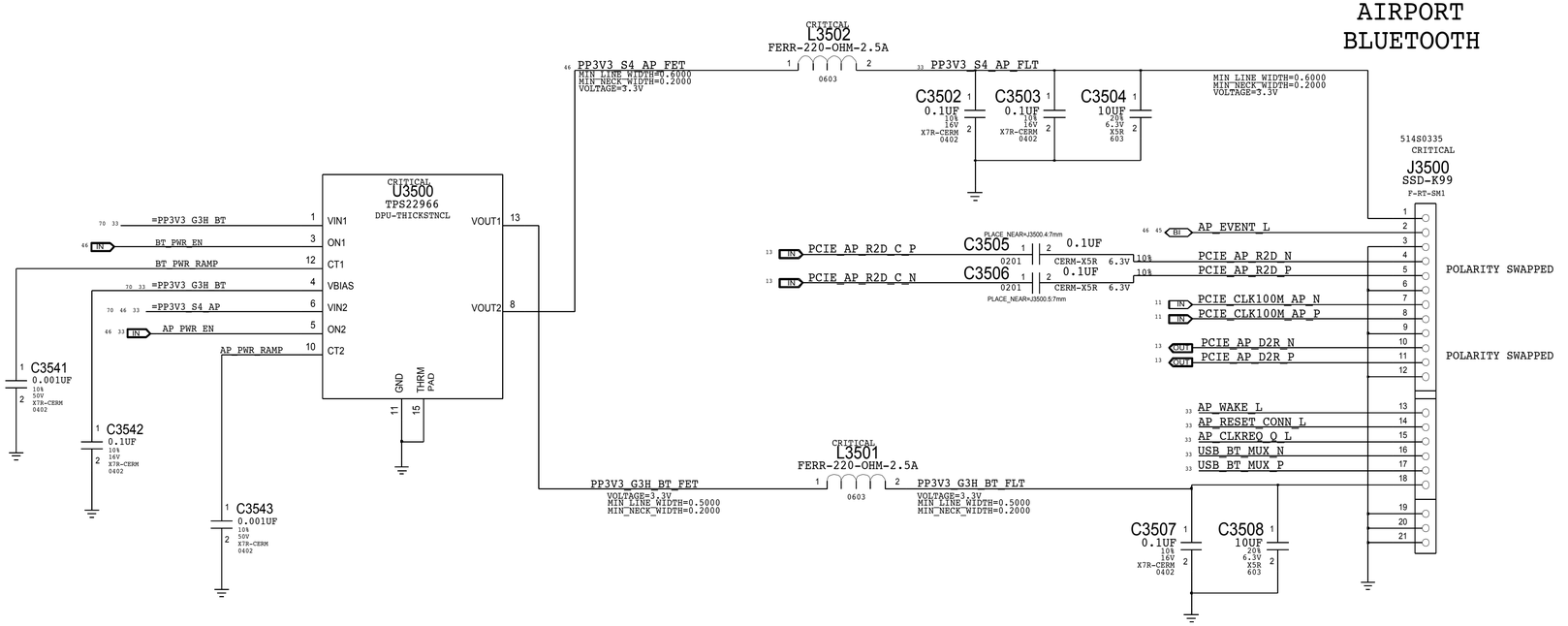
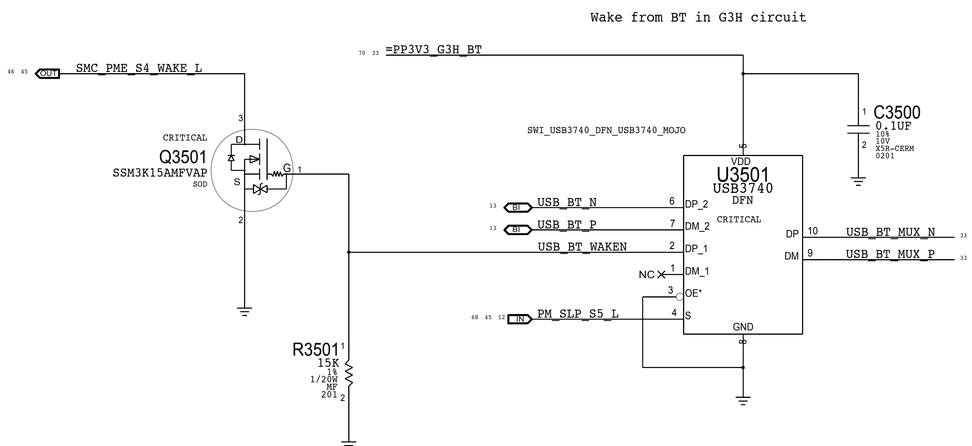
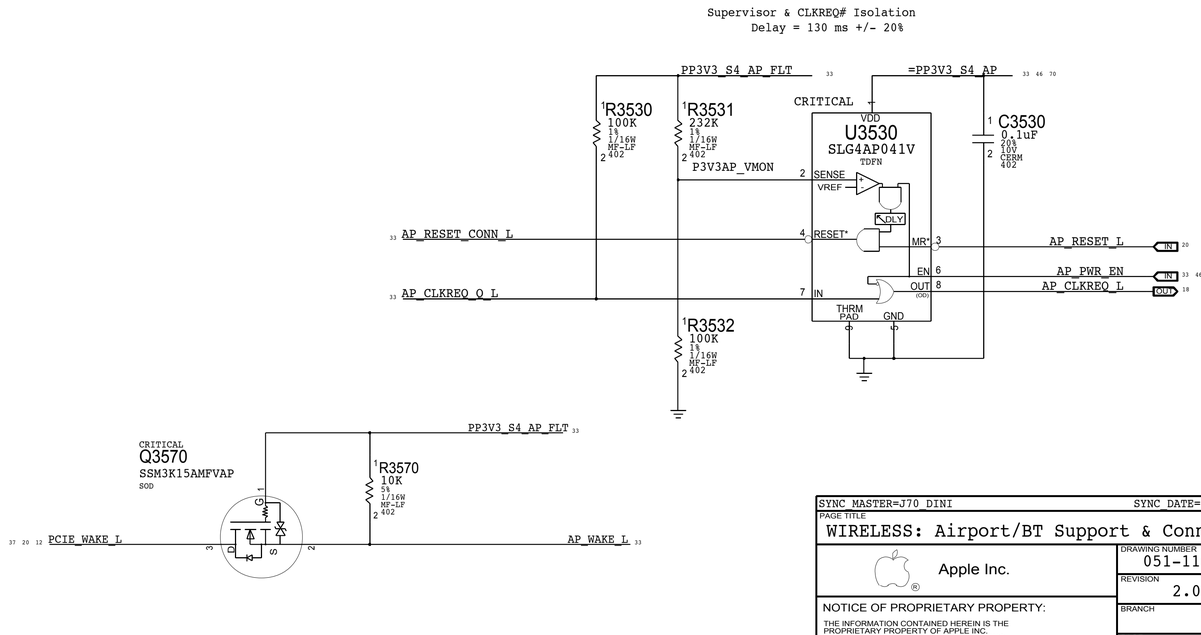
AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22966
AP SLEW RATE	1185 us
BT SLEW RATE	1185 us
Equation	0.32*Ct + 13.7







SYNC_MASTER=J70_DINI	SYNC_DATE=10/08/2013
PAGE TITLE	WIRELESS: Airport/BT Support & Connector
Apple Inc.	DRAWING NUMBER 051-1160 · SIZE D
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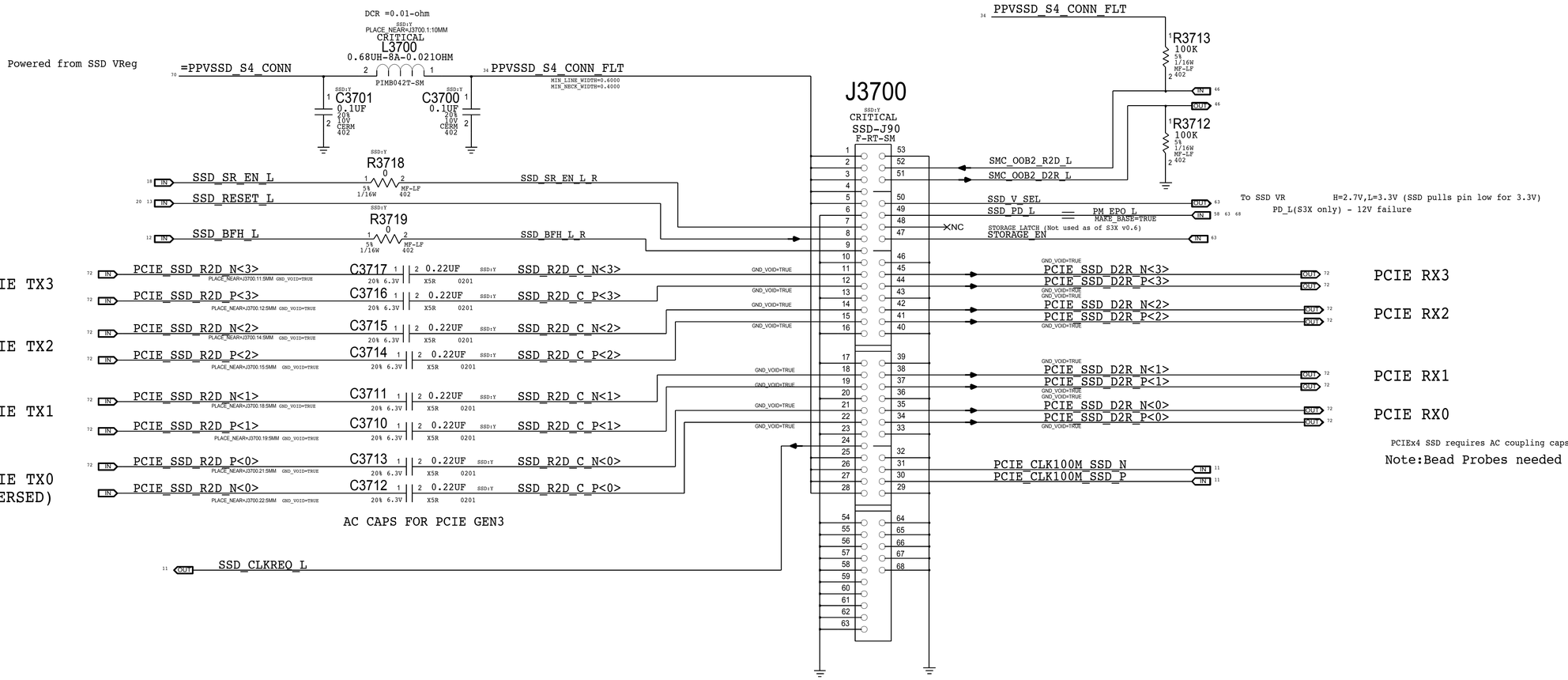

SYNC_MASTER=J94_ANDRES	SYNC_DATE=07/09/2014
PAGE TITLE: SSD: SSD Connector	
Apple Inc.	DRAWING NUMBER: 051-1160 SIZE: D
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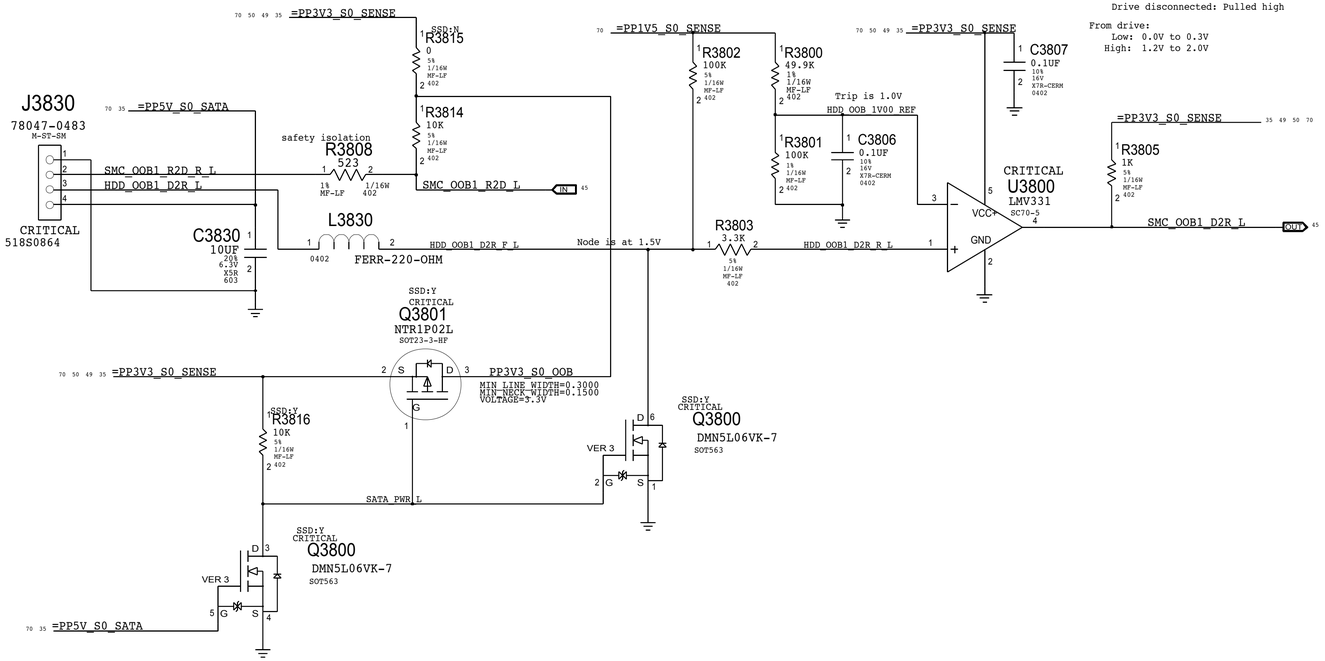
HDD POWER/OOB CONNECTOR

HDD Out-of-Band Temperature Sensing



Notes:

Drive active: Valid signal protocol

Drive asleep: HDD drives HDD_OOB_TEMP low

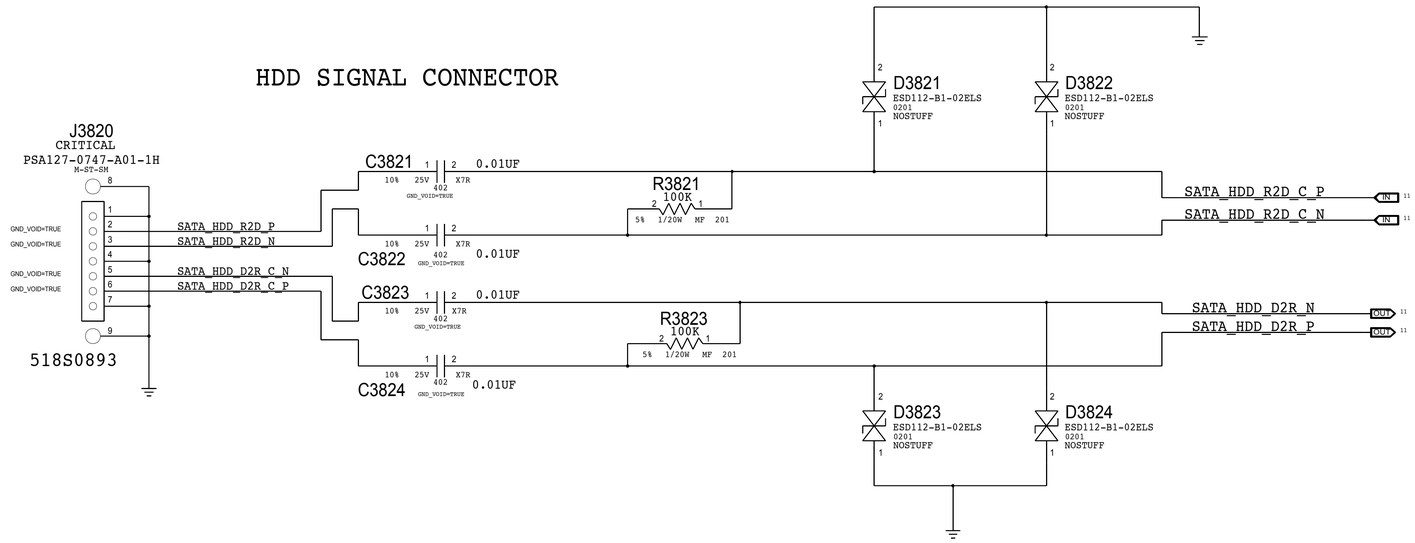
Drive disconnected: Pulled high

From drive:

Low: 0.0V to 0.3V

High: 1.2V to 2.0V

HDD SIGNAL CONNECTOR



SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE	HDD: HDD Connector
Apple Inc.	DRAWING NUMBER 051-1160 SIZE D
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

70 37 36 =PP3V3_ENET_PHY

281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
36 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 37

=ENET_SR_VFB 37

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 37

396mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
PP1V2_ENET_PHY_AVDDL
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

AVDDH 42 48 | BIASVDDH 37 | XTALVDDH 17 | VDDO 7 20 35 62 | SR_VDD 14 | SR_VDDP 15 | SR_LX 16 | SR_VFB 13 | AVDDL 39 45 51 | PCIE_PLLVDDL 29 32 | GPHY_PLLVDDL 36 | VDDC 35 61

70 =PP3V3_S0_ENET

R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U3900 BCM57766C0KMLG QFN-8X8

13 OUT PCIE_ENET_D2R_N — C3950 0.1UF 10% 16V X5R-CERM 0201 — ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPD-ENET)
13 OUT PCIE_ENET_D2R_P — C3951 0.1UF 10% 16V X5R-CERM 0201 — PCIE_ENET_D2R_C_N — 27 PCIE_TXD_N; PCIE_ENET_D2R_C_P — 28 PCIE_TXD_P
13 IN PCIE_ENET_R2D_C_P — C3955 0.1UF 10% 16V X5R-CERM 0201 — PCIE_ENET_R2D_P — 33 PCIE_RXD_P; PCIE_ENET_R2D_N — 34 PCIE_RXD_N
13 IN PCIE_ENET_R2D_C_N — C3956 0.1UF 10% 16V X5R-CERM 0201 — 11 IN PCIE_CLK100M_ENET_P — 31 PCIE_REFCLK_P; 11 IN PCIE_CLK100M_ENET_N — 30 PCIE_REFCLK_N
38 IN ENET_RESET_L — 11 PERST* (IPD)
18 OUT ENETSD_CLKREQ_L — 12 CLKREQ* (OD)
37 OUT =ENET_WAKE_L (See note) — 3 WAKE* (OD)
38 20 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)
SMB_ENET_SCL — 6 SMB_CLK
SMB_ENET_SDA — 10 SMB_DATA (IPD-ENETM)
36 ENET_SCLK — 66 SCLK_SPD1000LED*
36 ENET_MISO — 64 SI/EEDATA
36 ENET_MOSI — 65 SO_LINKLED*
36 ENET_CS_L — 63 CS*/EECLK (IPU)
NC — 2 SPD100LED*/SERIAL_DO (OD)
37 OUT ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
19 IN ENET_XTAL_IN — 18 XTALI
19 OUT ENET_XTAL_OUT — 19 XTALO
ENET_RDAC — 38 RDAC
(NO IPU OR IPD-ENET) THRM_PAD 69

R3965 1.24K 1% 1/16W MF-LF 402

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata. (IPU-ENET)

TRD0_P 40 ENETCONN_MDI_P<0> BI 37
TRD0_N 41 ENETCONN_MDI_N<0> BI 37
TRD1_P 44 ENETCONN_MDI_P<1> BI 37
TRD1_N 43 ENETCONN_MDI_N<1> BI 37
TRD2_P 46 ENETCONN_MDI_P<2> BI 37
TRD2_N 47 ENETCONN_MDI_N<2> BI 37
TRD3_P 50 ENETCONN_MDI_P<3> BI 37
TRD3_N 49 ENETCONN_MDI_N<3> BI 37

PP3V3R1V8_ENET_LR_OUT MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3R1V8_CR_VDDIO 36
C3980 4.7UF 20% 6.3V X5R-CERM1 402
C3981 0.1UF 10% 16V X5R-CERM 0201
C3982 0.1UF 10% 16V X5R-CERM 0201

(IPD) GPIO_0/CR_ACT_LED* 5 NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 — ENET_MEDIA_SENSE OUT 11
(IPx-ENET) SD_DETECT 1 — ENET_SD_DETECT_L IN 38

CR_CMD 26 ENET_SD_CMD — R3961 33 5% 1/20W MF 201 — SDCONN_CMD IN 38
CR_CLK 21 ENET_SD_CLK — R3979 33 5% 1/20W MF 201 — SDCONN_CLK OUT 38
(IPx-ENET) CR_DATA0 25 ENET_CR_DATA<0> — R3971 33 — SDCONN_DATA<0> BI 38
CR_DATA1 24 ENET_CR_DATA<1> — R3972 33 — SDCONN_DATA<1> BI 38
CR_DATA2 23 ENET_CR_DATA<2> — R3973 33 — SDCONN_DATA<2> BI 38
CR_DATA3 22 ENET_CR_DATA<3> — R3974 33 — SDCONN_DATA<3> BI 38
CR_DATA4 52 ENET_CR_DATA<4> — R3975 33 — SDCONN_DATA<4> BI 38
CR_DATA5 53 ENET_CR_DATA<5> — R3976 33 — SDCONN_DATA<5> BI 38
CR_DATA6 54 ENET_CR_DATA<6> — R3977 33 — SDCONN_DATA<6> BI 38
CR_DATA7 55 ENET_CR_DATA<7> — R3978 33 — SDCONN_DATA<7> BI 38
(IPU-ENET) MS_INS* 59 NC — No MS (Memory Stick) Insert feature needed.
(IPU-ENET) CR_LED*/CR_BUS_PWR 60 ENET_CR_PWREN OUT 38 — Control signal to light LED or control SD bus power.
(IPU-ENET) CR_WP* 57 — SDCONN_WP IN 38
(IPU-ENET) SR_DISABLE 68 ENET_SR_DISABLE — R3981 1K 5% 1/16W MF-LF 402 (See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

70 37 36 =PP3V3_ENET_PHY

U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC 8 — C3990 0.1UF 10% 16V X5R-CERM 0201
36 ENET_SCLK — SCK 2
36 ENET_CS_L — CS* 4
WP* 5
RESET* 3
GND 7
SI 1 — ENET_MOSI 36
SO 8 — ENET_MISO 36
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J70_GAREN SYNC_DATE=09/19/2013

PAGE TITLE
ETHERNET: PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D
REVISION 2.0.0
BRANCH
PAGE 39 OF 105
SHEET 36 OF 73

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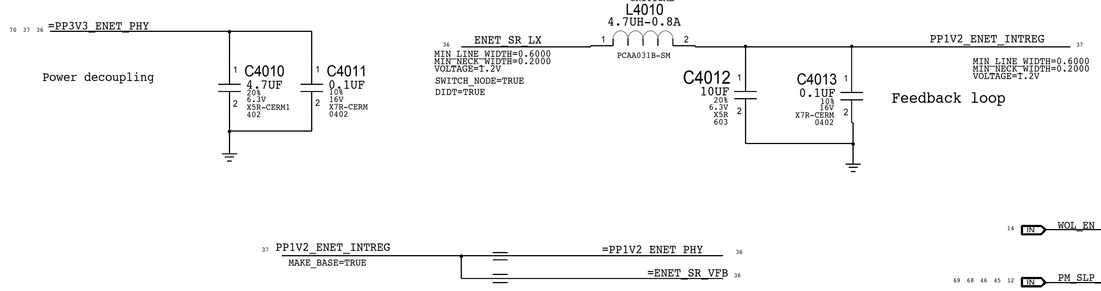
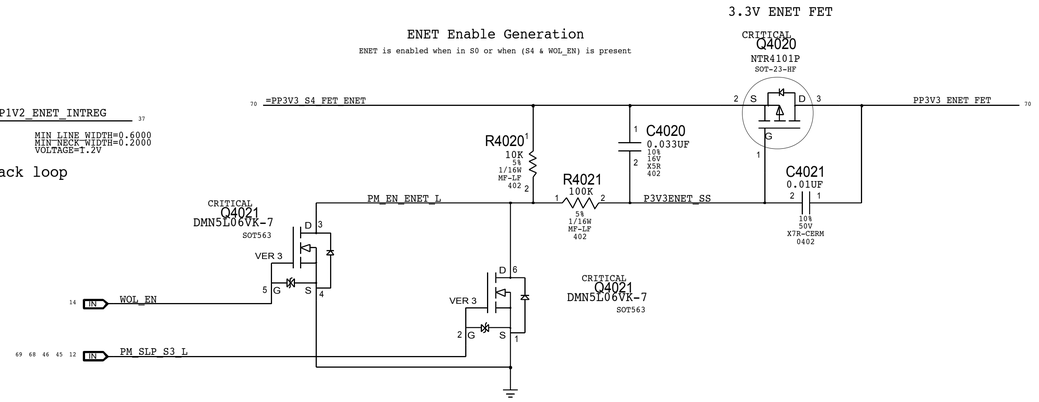
CAESAR IV 1.2V INT.VR CMPTS

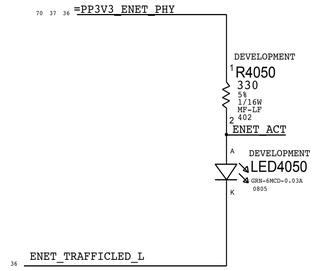


ENET Enable Generation

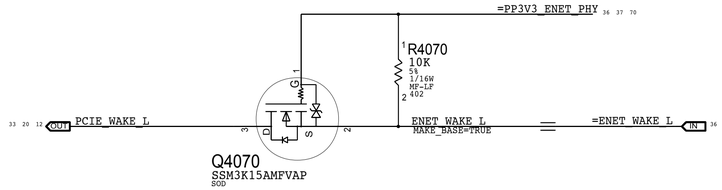
ENET is enabled when in S0 or when (S4 & WOL_EN) is present

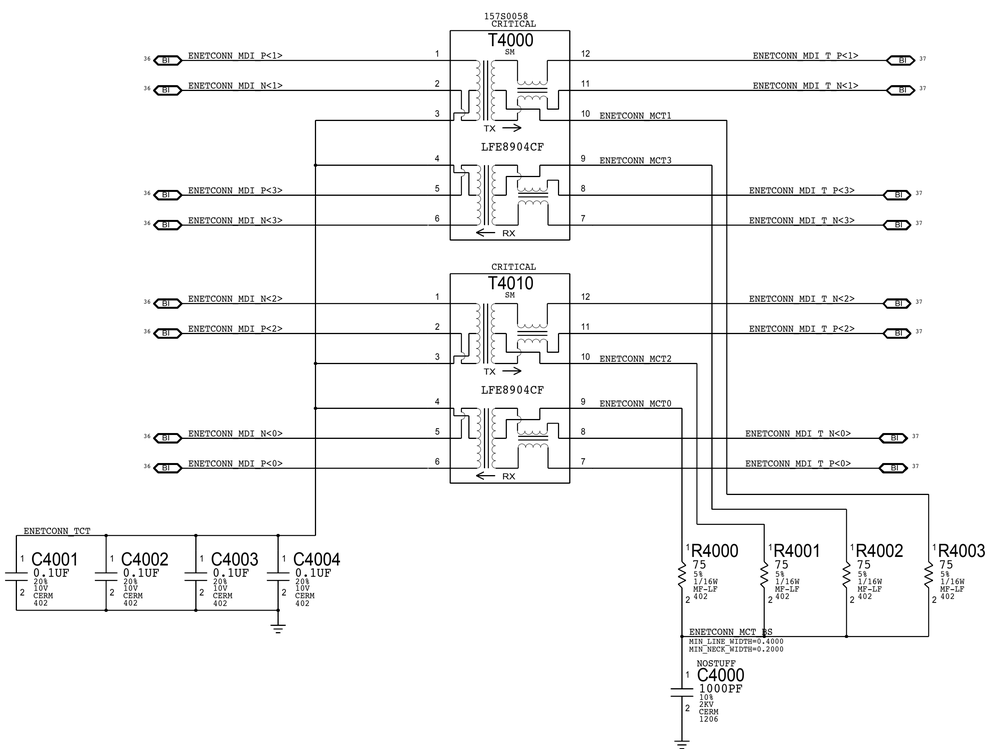


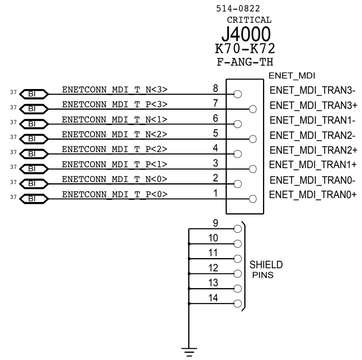
CAESAR IV ACTIVITY LED



CAESAR IV WAKE# ISOLATION







SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE

ETHERNET: Ethernet Support & Connector

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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PAGE 40 OF 105

SHEET 37 OF 73

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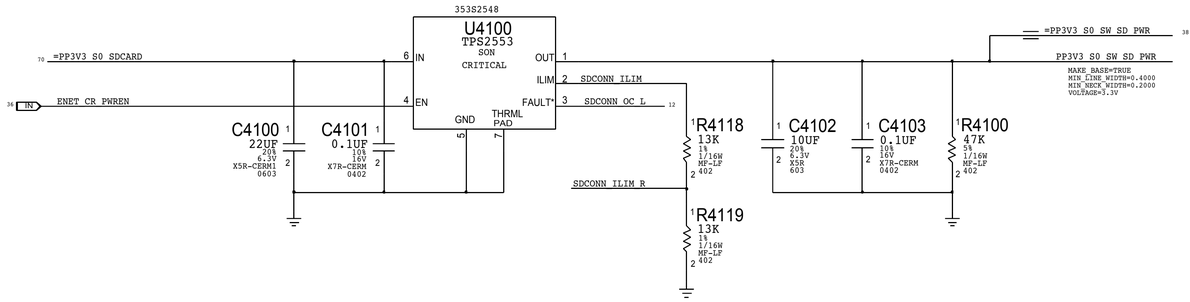
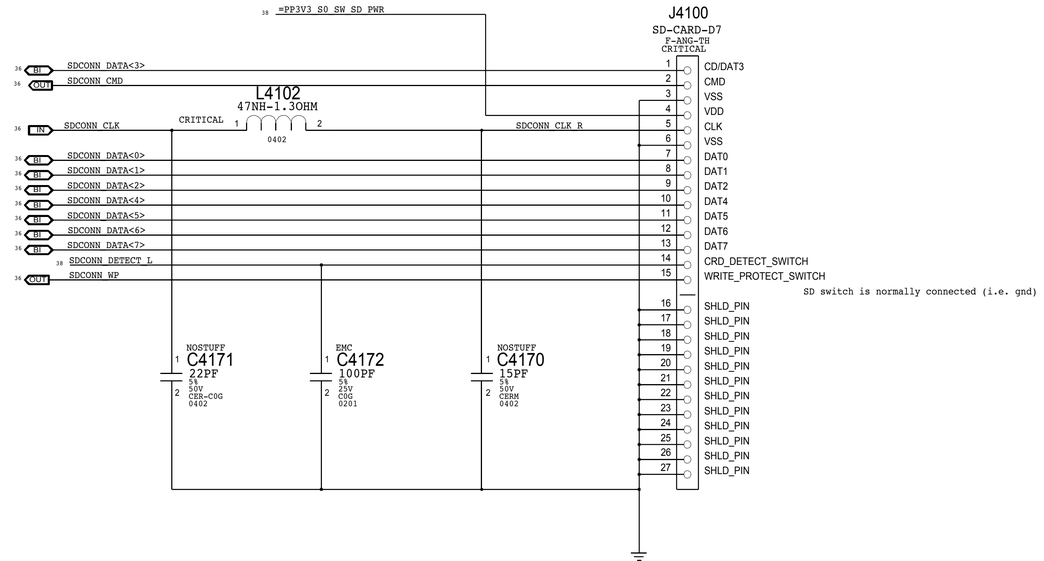
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

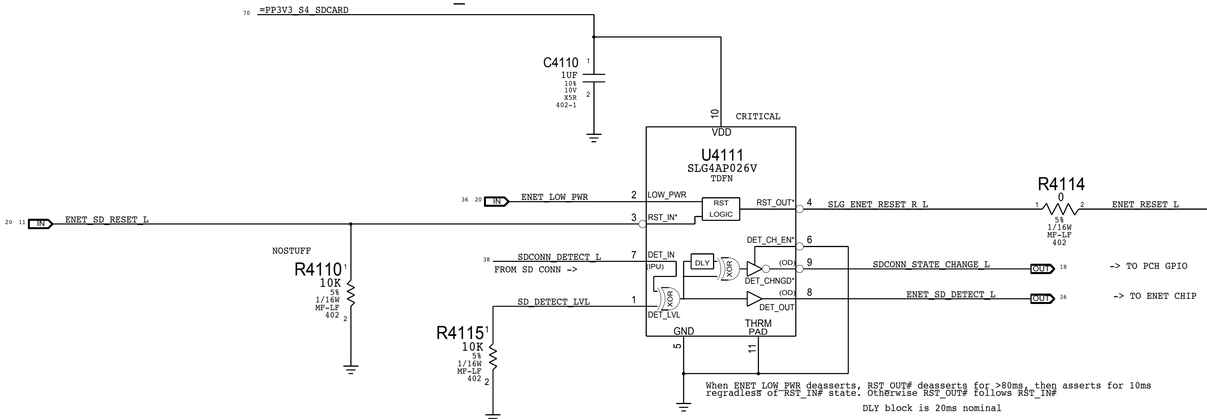


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J70_GAREN	SYNC_DATE=09/23/2013
PAGE TITLE: SD CARD: SD Reader Connector	
Apple Inc.	DRAWING NUMBER: 051-1160 SIZE: D
	REVISION: 2.0.0
	BRANCH:
	PAGE: 41 OF 105
	SHEET: 38 OF 73

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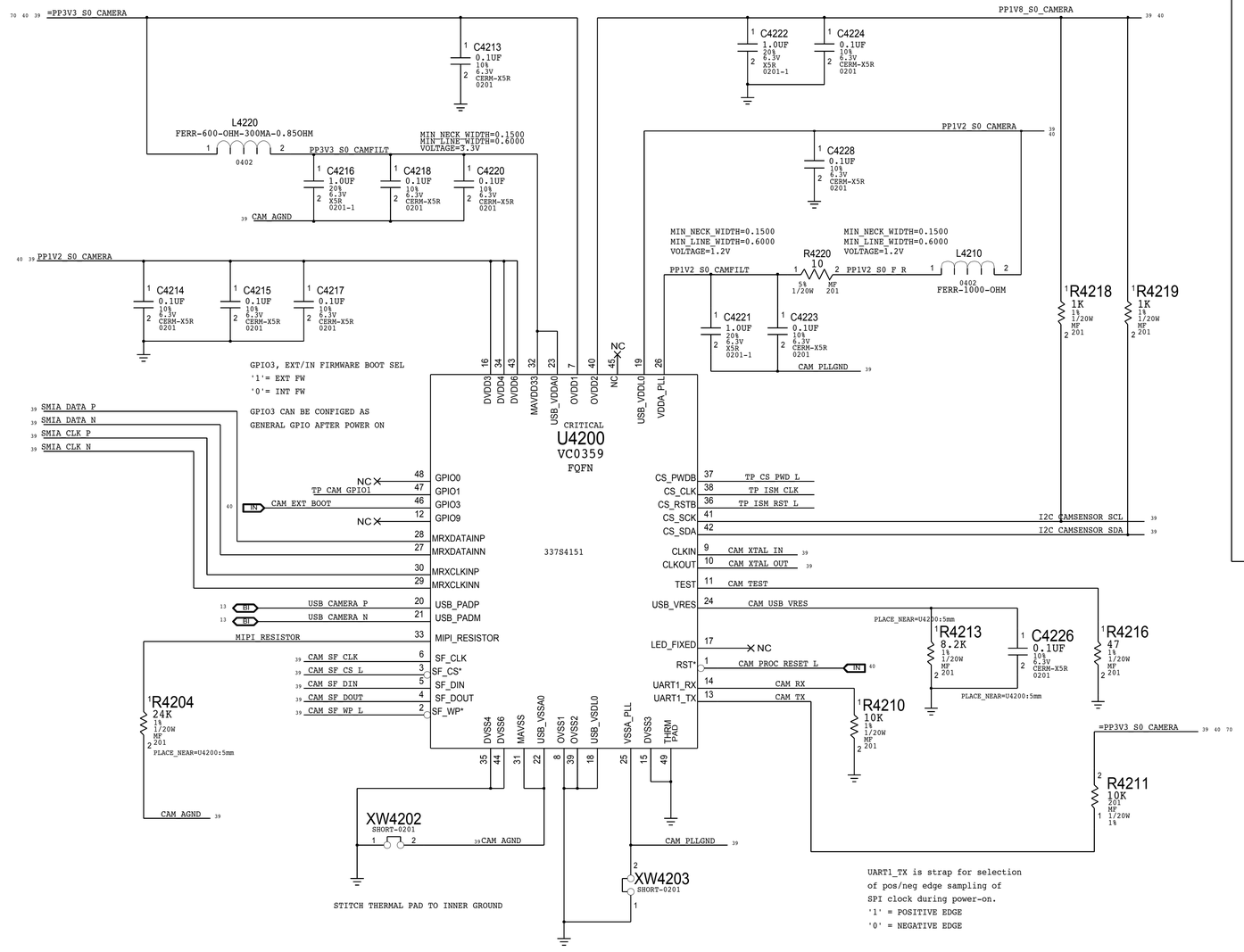
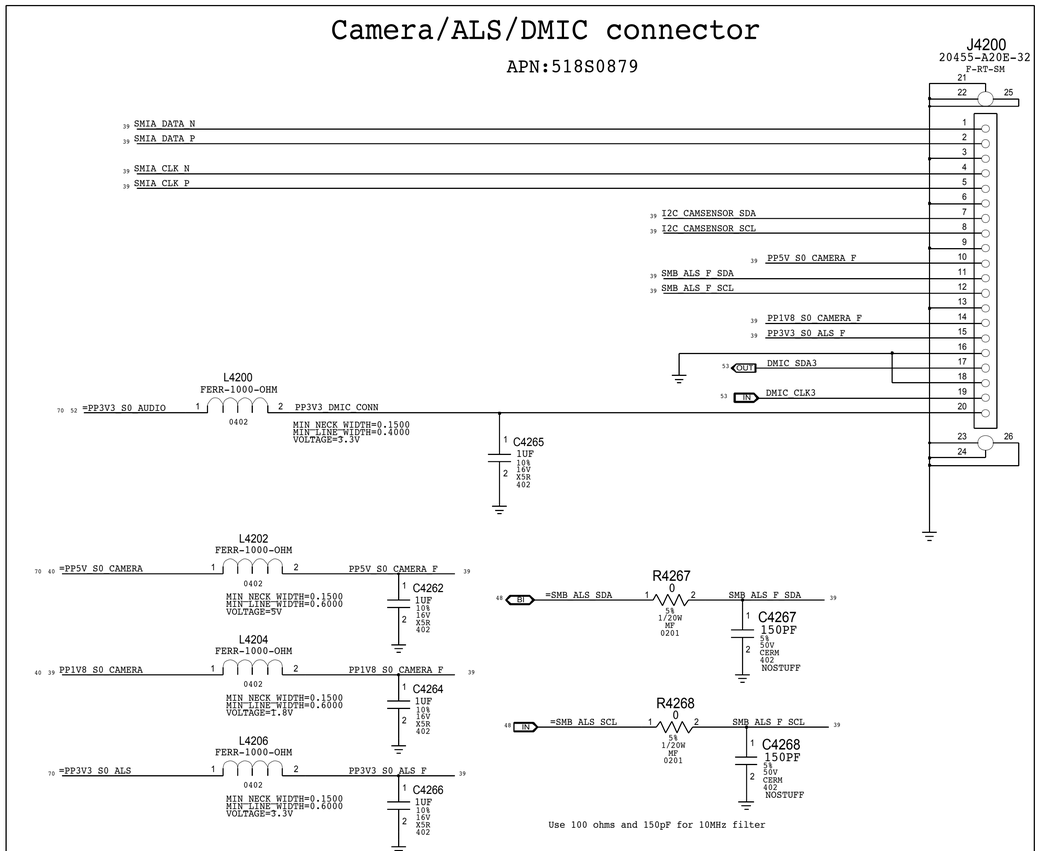
USB CAMERA CONTROLLER

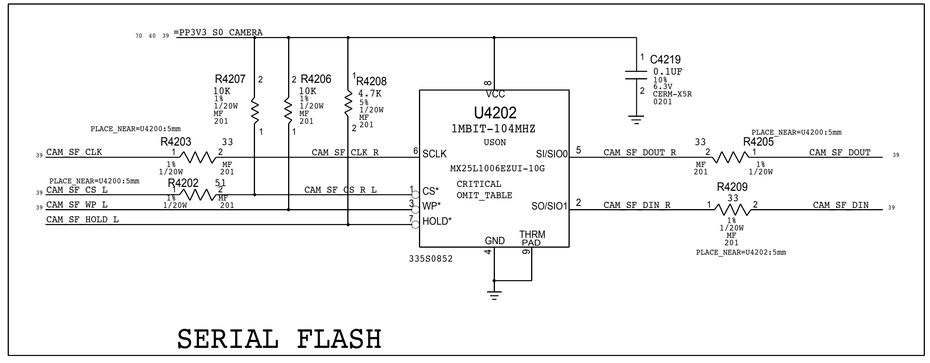


Camera/ALS/DMIC connector

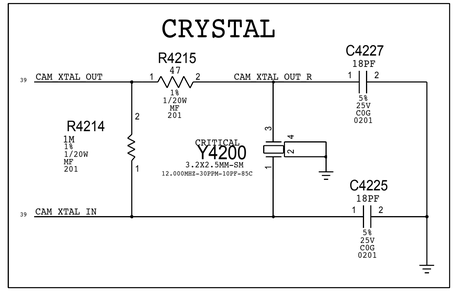
APN:518S0879



SERIAL FLASH



CRYSTAL



SYNC_MASTER=J70_GAREN	SYNC_DATE=02/05/2014
PAGE TITLE: CAMERA: Camera Controller	
Apple Inc.	DRAWING NUMBER: 051-1160 SIZE: D
	REVISION: 2.0.0
	BRANCH:
	PAGE: 42 OF 105
	SHEET: 39 OF 73

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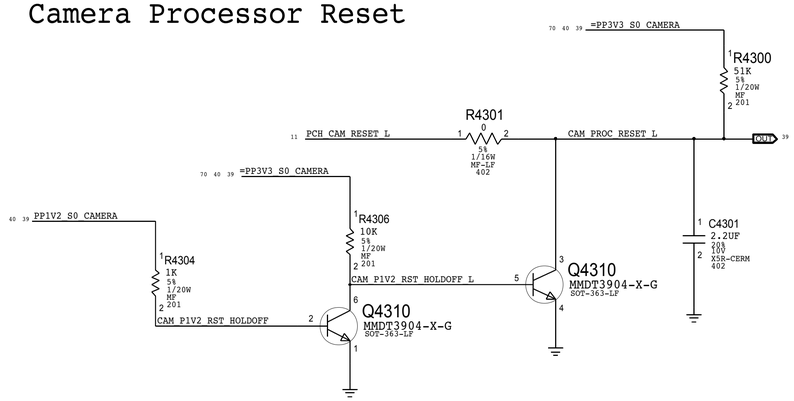
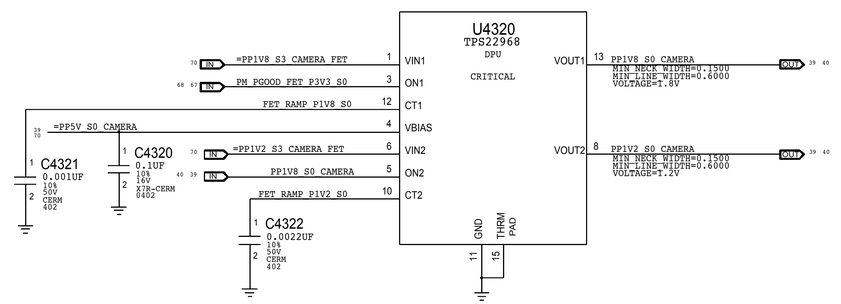
Camera Processor Reset



Camera Processor ExtBoot Cntl

1.8V S0 and 1.2V S0 Load Switch

POWER SEQUENCE
3.3V => 1.8V => 1.2V
Enable 1.8V camera rail when 3.3V S0 rail is on
Enable 1.2V camera rail when 1.8V S0 rail is on



Capacitor Values Found Using
Slew Rate(us/V) = 0.32*CT(pF) + 13.7

Rise Times:
1.8V S0 -- 1000 pF -- 600 us
1.2V S0 -- 2200 pF -- 861 us

SYNC_MASTER=J70_GAREN SYNC_DATE=10/24/2013

PAGE TITLE
CAMERA: Camera Controller Support

Apple Inc.

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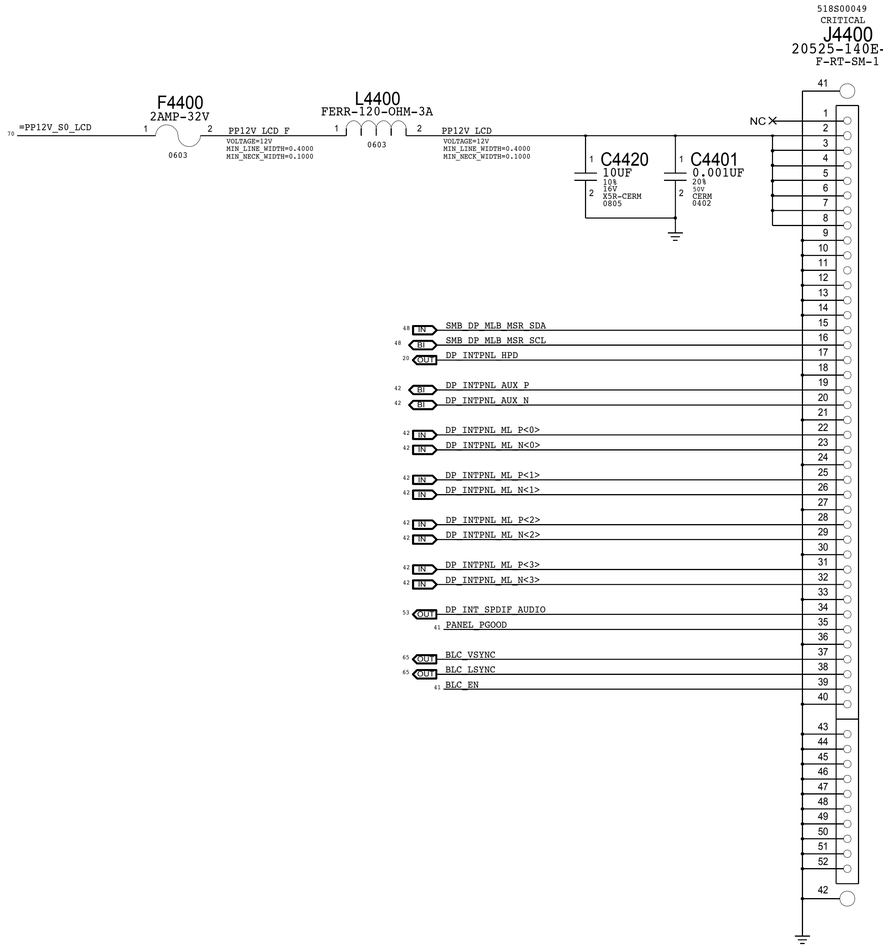
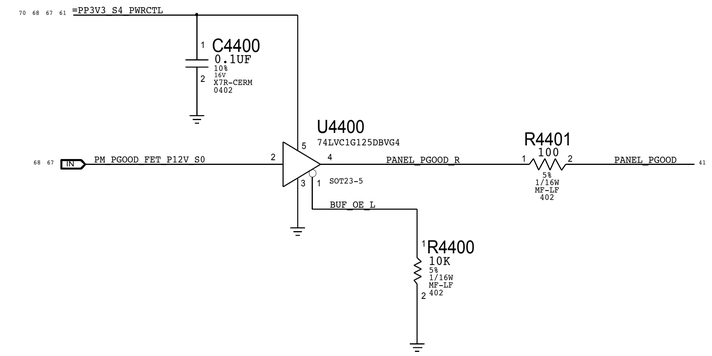
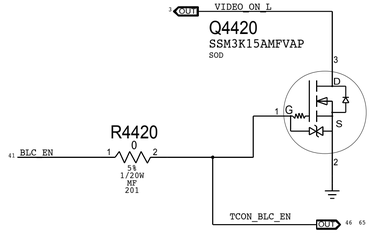
Internal DP Connector





X403 Config



SYNC_MASTER=J94_NICK SYNC_DATE=06/23/2014

PAGE TITLE

DISPLAY: Internal DP Support

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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SHEET 41 OF 73

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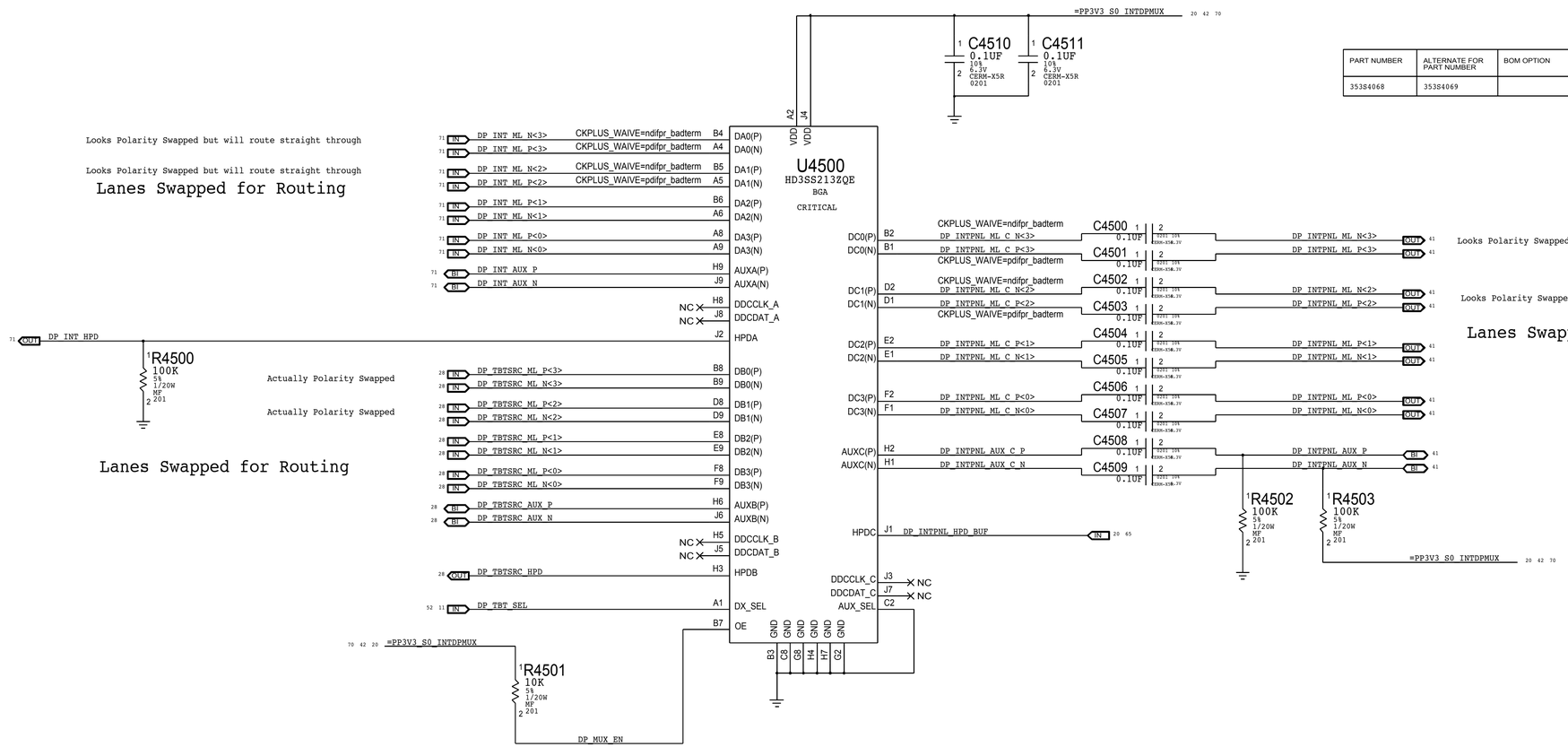
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4068	353S4069		U4500	NXP TDM Mux



SYNC MASTER=J94_NICK	SYNC DATE=06/23/2014
PAGE TITLE	DISPLAY: Internal DP MUXing
Apple Inc.	DRAWING NUMBER 051-1160 SIZE D
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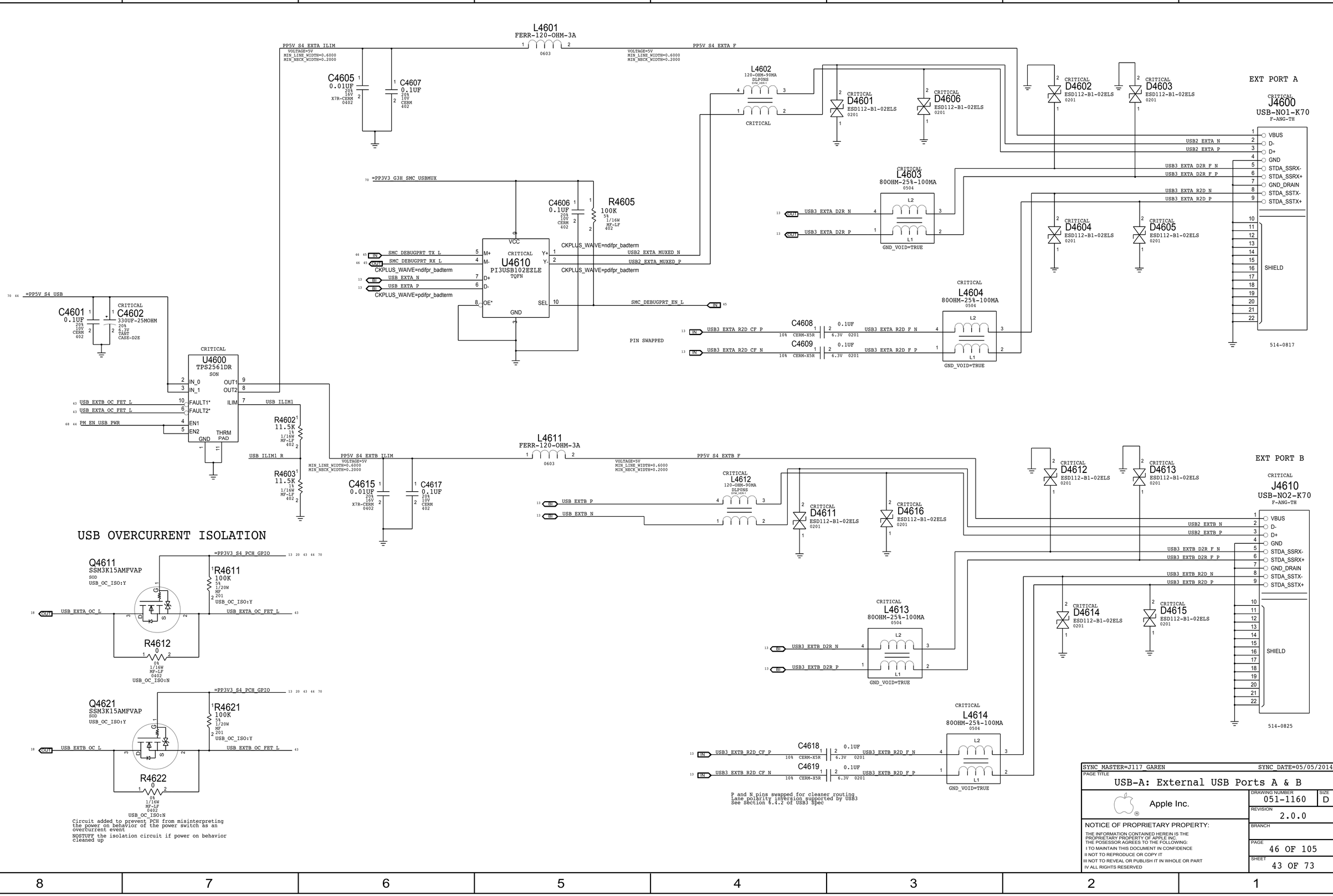
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
PP5V_S4_EXTA_F
C4605 0.01UF 20% 16V X7R-CERM 0402
C4607 0.1UF 20% 10V CERM 402
L4602 120-OHM-90MA DLP0NS
CRITICAL
D4601 ESD112-B1-02ELS 0201
D4606 ESD112-B1-02ELS 0201
D4602 ESD112-B1-02ELS 0201
D4603 ESD112-B1-02ELS 0201
EXT PORT A
J4600 USB-NO1-K70 F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_D2R_F_N
USB3_EXTA_D2R_F_P
USB3_EXTA_R2D_N
USB3_EXTA_R2D_P
=PP3V3_G3H_SMC_USBMUX
C4606 0.1UF 20% 10V CERM 402
R4605 100K 5% 1/16W MF-LF 402
VCC
U4610 PI3USB102EZLE TQFN
GND
SEL
OE*
M+
M-
D+
D-
Y+
Y-
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
USB_EXTA_N
USB_EXTA_P
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SMC_DEBUGPRT_EN_L
L4603 80OHM-25%-100MA 0504
L4604 80OHM-25%-100MA 0504
GND_VOID=TRUE
C4608 0.1UF 10% CERM-X5R 6.3V 0201
C4609 0.1UF 10% CERM-X5R 6.3V 0201
PIN SWAPPED
=PP5V_S4_USB
C4601 0.1UF 20% 10V CERM 402
C4602 330UF-25MOHM 20% 6.3V TANT CASE-D2E
U4600 TPS2561DR SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
GND
THRM PAD
OUT1
OUT2
ILIM
USB_EXTB_OC_FET_L
USB_EXTA_OC_FET_L
PM_EN_USB_PWR
USB_ILIM1
R4602 11.5K 1% 1/16W MF-LF 402
R4603 11.5K 1% 1/16W MF-LF 402
USB_ILIM1_R
PP5V_S4_EXTB_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
C4615 0.01UF 20% 16V X7R-CERM 0402
C4617 0.1UF 20% 10V CERM 402
L4611
FERR-120-OHM-3A
0603
PP5V_S4_EXTB_F
L4612 120-OHM-90MA DLP0NS
D4611 ESD112-B1-02ELS 0201
D4616 ESD112-B1-02ELS 0201
D4612 ESD112-B1-02ELS 0201
D4613 ESD112-B1-02ELS 0201
EXT PORT B
J4610 USB-NO2-K70 F-ANG-TH
USB_EXTB_P
USB_EXTB_N
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_D2R_F_N
USB3_EXTB_D2R_F_P
USB3_EXTB_R2D_N
USB3_EXTB_R2D_P
L4613 80OHM-25%-100MA 0504
L4614 80OHM-25%-100MA 0504
C4618 0.1UF 10% CERM-X5R 6.3V 0201
C4619 0.1UF 10% CERM-X5R 6.3V 0201
D4614 ESD112-B1-02ELS 0201
D4615 ESD112-B1-02ELS 0201
514-0825
USB OVERCURRENT ISOLATION
Q4611 SSM3K15AMFVAP SOD
Q4621 SSM3K15AMFVAP SOD
USB_OC_ISO:Y
R4611 100K 5% 1/20W MF 201
R4621 100K 5% 1/20W MF 201
R4612 0 0% 1/16W MF-LF 0402
R4622 0 0% 1/16W MF-LF 0402
USB_OC_ISO:N
=PP3V3_S4_PCH_GPIO
USB_EXTA_OC_L
USB_EXTB_OC_L
Circuit added to prevent PCH from misinterpreting the power on behavior of the power switch as an overcurrent event
NOSTUFF the isolation circuit if power on behavior cleaned up
P and N pins swapped for cleaner routing
Lane polarity inversion supported by USB3
See Section 6.4.2 of USB3 Spec
SYNC_MASTER=J117_GAREN
SYNC_DATE=05/05/2014
PAGE TITLE
USB-A: External USB Ports A & B
Apple Inc.
DRAWING NUMBER 051-1160
SIZE D
REVISION 2.0.0
BRANCH
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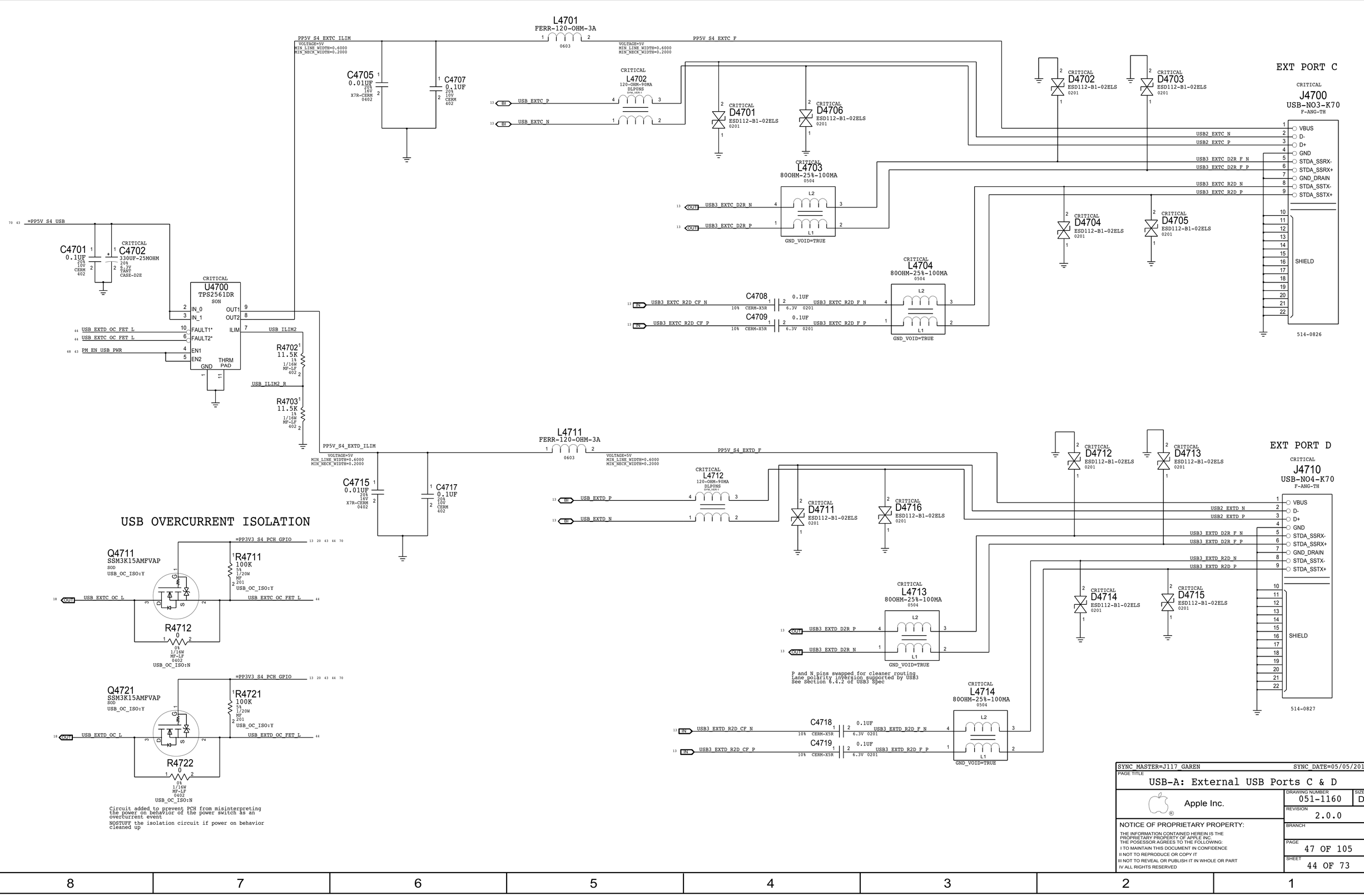
L4701
FERR-120-OHM-3A
0603
PP5V_S4_EXTC_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
PP5V_S4_EXTC_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
C4705
0.01UF
20%
16V
X7R-CERM
0402
C4707
0.1UF
20%
10V
CERM
402
CRITICAL
L4702
120-OHM-90MA
DLP0NS
SYM_VER=1
USB_EXTC_P
USB_EXTC_N
CRITICAL
D4701
ESD112-B1-02ELS
0201
CRITICAL
D4706
ESD112-B1-02ELS
0201
CRITICAL
D4702
ESD112-B1-02ELS
0201
CRITICAL
D4703
ESD112-B1-02ELS
0201
EXT PORT C
CRITICAL
J4700
USB-NO3-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0826
USB2_EXTC_N
USB2_EXTC_P
USB3_EXTC_D2R_F_N
USB3_EXTC_D2R_F_P
USB3_EXTC_R2D_N
USB3_EXTC_R2D_P
CRITICAL
L4703
80OHM-25%-100MA
0504
L2
L1
GND_VOID=TRUE
USB3_EXTC_D2R_N
USB3_EXTC_D2R_P
CRITICAL
D4704
ESD112-B1-02ELS
0201
CRITICAL
D4705
ESD112-B1-02ELS
0201
CRITICAL
L4704
80OHM-25%-100MA
0504
C4708
0.1UF
10% CERM-X5R 6.3V 0201
C4709
0.1UF
10% CERM-X5R 6.3V 0201
USB3_EXTC_R2D_CF_N
USB3_EXTC_R2D_CF_P
USB3_EXTC_R2D_F_N
USB3_EXTC_R2D_F_P
=PP5V_S4_USB
C4701
0.1UF
20%
10V
CERM
402
CRITICAL
C4702
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
CRITICAL
U4700
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
GND
THRM PAD
OUT1
OUT2
ILIM
USB_EXTD_OC_FET_L
USB_EXTC_OC_FET_L
PM_EN_USB_PWR
USB_ILIM2
R4702
11.5K
1%
1/16W
MF-LF
402
USB_ILIM2_R
R4703
11.5K
1%
1/16W
MF-LF
402
L4711
FERR-120-OHM-3A
0603
PP5V_S4_EXTD_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
PP5V_S4_EXTD_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
C4715
0.01UF
20%
16V
X7R-CERM
0402
C4717
0.1UF
20%
10V
CERM
402
CRITICAL
L4712
120-OHM-90MA
DLP0NS
SYM_VER=1
USB_EXTD_P
USB_EXTD_N
CRITICAL
D4711
ESD112-B1-02ELS
0201
CRITICAL
D4716
ESD112-B1-02ELS
0201
CRITICAL
D4712
ESD112-B1-02ELS
0201
CRITICAL
D4713
ESD112-B1-02ELS
0201
EXT PORT D
CRITICAL
J4710
USB-NO4-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0827
USB2_EXTD_N
USB2_EXTD_P
USB3_EXTD_D2R_F_N
USB3_EXTD_D2R_F_P
USB3_EXTD_R2D_N
USB3_EXTD_R2D_P
CRITICAL
L4713
80OHM-25%-100MA
0504
L2
L1
GND_VOID=TRUE
USB3_EXTD_D2R_P
USB3_EXTD_D2R_N
CRITICAL
D4714
ESD112-B1-02ELS
0201
CRITICAL
D4715
ESD112-B1-02ELS
0201
P and N pins swapped for cleaner routing
Lane polarity inversion supported by USB3
See section 6.4.2 of USB3 Spec
CRITICAL
L4714
80OHM-25%-100MA
0504
C4718
0.1UF
10% CERM-X5R 6.3V 0201
C4719
0.1UF
10% CERM-X5R 6.3V 0201
USB3_EXTD_R2D_CF_N
USB3_EXTD_R2D_CF_P
USB3_EXTD_R2D_F_N
USB3_EXTD_R2D_F_P
USB OVERCURRENT ISOLATION
Q4711
SSM3K15AMFVAP
SOD
USB_OC_ISO:Y
=PP3V3_S4_PCH_GPIO
R4711
100K
5%
1/20W
MF
201
USB_OC_ISO:Y
USB_EXTC_OC_L
USB_EXTC_OC_FET_L
R4712
0
0%
1/16W
MF-LF
0402
USB_OC_ISO:N
Q4721
SSM3K15AMFVAP
SOD
USB_OC_ISO:Y
=PP3V3_S4_PCH_GPIO
R4721
100K
5%
1/20W
MF
201
USB_OC_ISO:Y
USB_EXTD_OC_L
USB_EXTD_OC_FET_L
R4722
0
0%
1/16W
MF-LF
0402
USB_OC_ISO:N
Circuit added to prevent PCH from misinterpreting the power on behavior of the power switch as an overcurrent event
NOSTUFF the isolation circuit if power on behavior cleaned up
SYNC_MASTER=J117_GAREN
SYNC_DATE=05/05/2014
PAGE TITLE
USB-A: External USB Ports C & D
Apple Inc.
DRAWING NUMBER
051-1160
SIZE
D
REVISION
2.0.0
BRANCH
PAGE
47 OF 105
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44 OF 73
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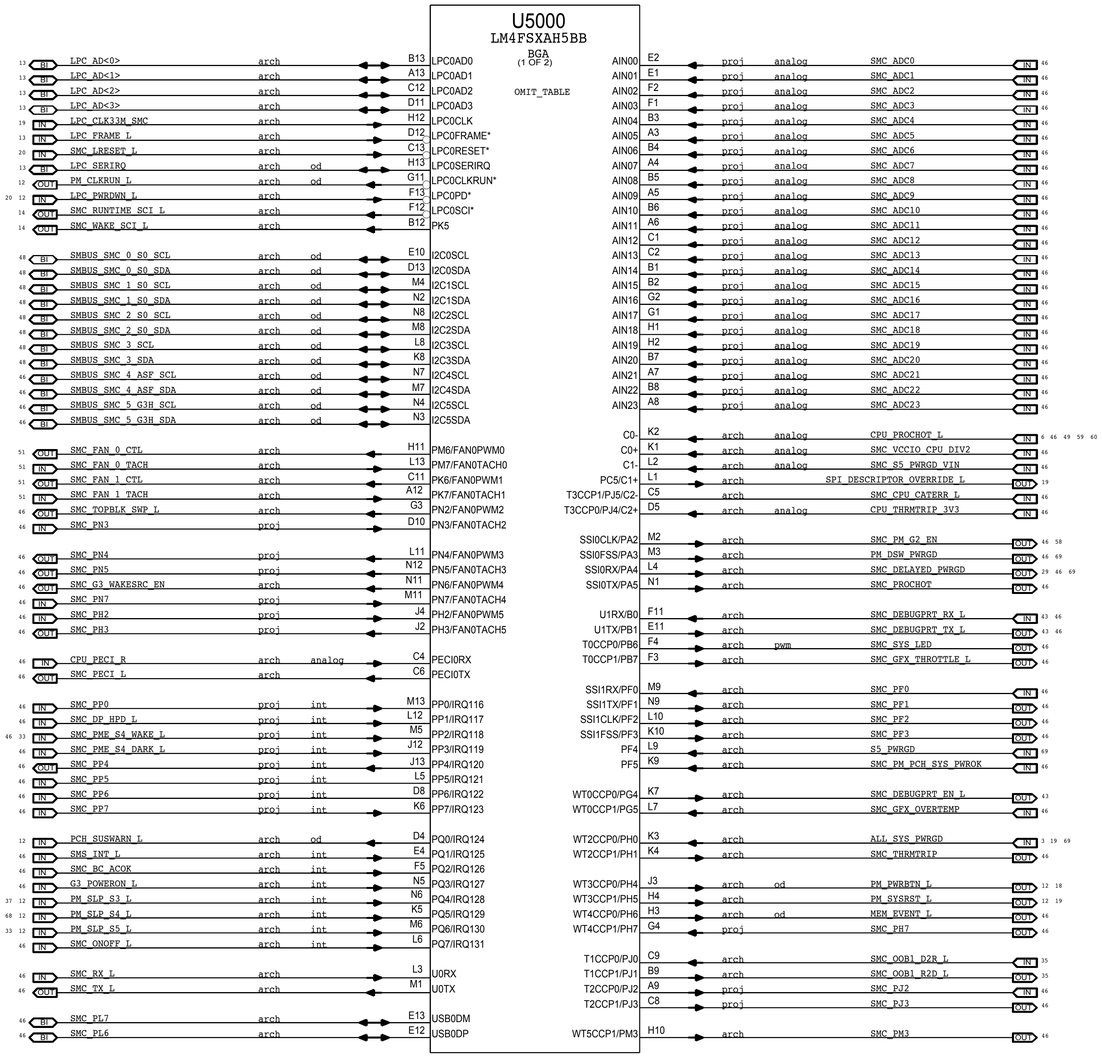
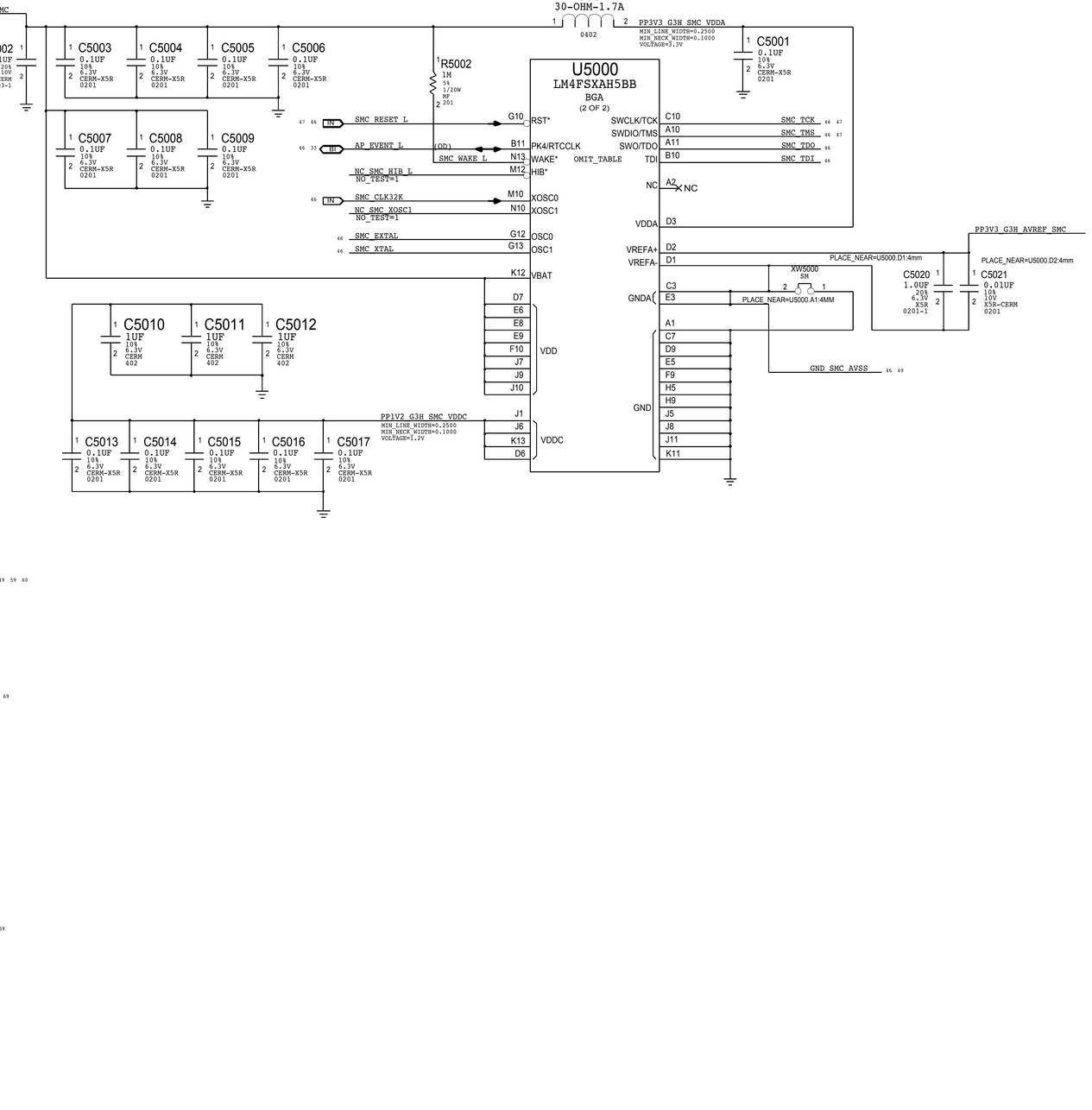
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





SYNC_MASTER=J70_NICK	SYNC_DATE=09/24/2013
PAGE TITLE: SMC: SMC Controller	
Apple Inc.	DRAWING NUMBER 051-1160 · SIZE D
	REVISION 2.0.0
	BRANCH
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SMC Supervisor and AVREF Supply

R5102 47 5% 1/16W MF-LF 402 — =PP3V3_G3H_SMC → PP3V42_G3H_SMC_SPVSR (MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.42V)

C5102 4.7UF 20% 6.3V X5R-CERM1 402

R5105 100K 5% 1/16W MF-LF 402 — =PP3V3_G3H_SMC

=PPVIN_G3H_SMCVREF

U5100 VREF-3.3V-VDET-3.0V DFN SN0903049
- V+ (1), VIN (3)
- NC, MR1* (ipu) (6)
- NC, MR2* (ipu) (7)
- RESET* (5) → SMC_RESET_L OUT 45 47
- DELAY (4) ← SMC_MANUAL_RST_L
- CRITICAL
- REFOUT (8) → PP3V3_G3H_AVREF_SMC (MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.1500, VOLTAGE=3.3V)
- GND (2), THRM PAD (9) → GND_SMC_AVSS (MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.1500, VOLTAGE=0V)

C5100 0.47UF 10% 6.3V CERM-X5R 402

C5101 0.01UF 10% 16V X7R-CERM 0402

C5105 1UF 20% 10V X5R-CERM 0603-1

C5106 0.01UF 10% 16V X7R-CERM 0402

NOSTUFF C5103 1000PF 5% 25V CERM 0402

Note: IPU are pulled to VIN rail

Power Button

=PP3V3_G3H_SMC → R5120 10K 5% 1/20W MF 201

DEVELOPMENT J5120 NTC020-AK1J-B260T (1 SM 2)

SMC_ONOFF_L OUT 45 (MAKE_BASE=TRUE)

PWR_BTN OUT 58

(3, 4)

SMC Controlled RTC Reset

To absorb current from discharging RTC Reset CAP

CRITICAL Q5199 SSM3K15AMFVAP SOD

RTC_RESET_L_R ← R5194 330 5% 1/16W MF-LF 402 ← RTC_RESET_L OUT 11 19

SMC_ASSERT_RTCRST 46 19

R5199 10K 5% 1/16W MF-LF 402

NOSTUFF C5199 1.0UF 20% 6.3V X5R-CERM 0402

Comparator Reference

=PP1V05_S0_SMC → R5130 10K 1% 1/16W MF-LF 402 (PLACE_NEAR=U5000.K1:5MM)

SMC_VCCIO_CPU_DIV2 OUT 45

R5131 10K 1% 1/16W MF-LF 402 (PLACE_NEAR=U5000.K1:5MM)

C5131 0.1UF 10% 16V X7R-CERM 0402 (PLACE_NEAR=U5000.K1:3.5MM)

SMC control for AirPort power

=PP3V3_S4_AP → R5142 100K 5% 1/20W MF 201

SMC_WIFI_PWR_EN 46 → AP_PWR_EN OUT 33 (MAKE_BASE=TRUE)

AC/DC Burst Mode Enable

=PP3V3_S5_SMC → R5140 10K 5% 1/20W MF 201

=PP3V3_S4_SMC → R5141 10K 5% 1/20W MF 201

Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

BURSTMODE_EN_L OUT 58 64

CRITICAL Q5140 DMN5L06VK-7 SOT563 (VER 3)

ACDC_BURST

CRITICAL Q5140 DMN5L06VK-7 SOT563 (VER 3)

ACDC_BURST_EN_L 46

=PP3V3_S5_SMC → C5140 0.1UF 10% 6.3V CERM-X5R 0201

U5140 CRITICAL TC7SZ08FEAPE SOT665

PM_SLP_S3_L 69 68 45 37 12 IN → PM_SLP_S3_BUF_L 4

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H
SMC_ADC1	ISNS_P12VG3H
SMC_ADC2	VSNS_P3V3S5
SMC_ADC3	ISNS_P3V3S5
SMC_ADC6	VSNS_P1V2_S3_DDR
SMC_ADC7	ISNS_P1V2_S3_DDR
SMC_ADC8	VSNS_P5VS4
SMC_ADC9	ISNS_P5VS4
SMC_ADC10	VSNS_CPUVCC
SMC_ADC11	ISNS_CPUVCC
SMC_ADC20	VSNS_P3V3_SSD
SMC_ADC21	ISNS_SSDS0

(MAKE_BASE=TRUE)

Unused ADC Channels

SMC_ADC4	NC_VSNS_PVDDQS0	NO_TEST=1
SMC_ADC5	NC_ISNS_PVDDQS0	NO_TEST=1
SMC_ADC12	NC_VSNS_GPUCORE_ALT	NO_TEST=1
SMC_ADC13	NC_ISNS_GPUCORE_ALT	NO_TEST=1
SMC_ADC14	NC_VSNS_HDDS0	NO_TEST=1
SMC_ADC15	NC_ISNS_HDDS0	NO_TEST=1
SMC_ADC16	NC_SMC_ADC16	NO_TEST=1
SMC_ADC17	NC_SMC_ADC17	NO_TEST=1
SMC_ADC18	NC_VSNS_P1V05S0_PCH	NO_TEST=1
SMC_ADC19	NC_ISNS_P3V3S4_AP	NO_TEST=1
SMC_ADC22	NC_SMC_ADC22	NO_TEST=1
SMC_ADC23	NC_SMC_ADC23	NO_TEST=1

(MAKE_BASE=TRUE)

Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L 46
SMC_PJ3	SMC_OOB2_R2D_L 34
SMC_PJ2	SMC_OOB2_D2R_L 34
SMC_PP0	SMC_ACDC_ID 58
SMC_PH2	SMC_ASSERT_RTCRST 19 46
SMC_PL6	SMC_WIFI_PWR_EN 46
SMC_PH3	SMC_PCH_SUSACK_L 12
SMC_PN3	TCON_BLC_EN 41 65
SMC_PH7	MEM_GOOD_LED 3 18
TP for ACC68S_1I ZPB re-intstated	
SMC_PL7	BT_PWR_EN 33 46
SMC_PM3	PSU_OCP_ACTIVE 49

(MAKE_BASE=TRUE)

Unused Project-specific

SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	NO_TEST=1
SMC_PN4	NC_SMC_PN4	NO_TEST=1
SMC_PP4	NC_SMC_S4_WAKESRC_EN	NO_TEST=1
SMC_PN7	NC_SMC_PN7	NO_TEST=1
SMC_PP5	NC_SMC_PP5	NO_TEST=1
SMC_PP6	NC_SMC_PP6	NO_TEST=1
SMC_PP7	NC_SMC_PP7	NO_TEST=1
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	NO_TEST=1
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	NO_TEST=1
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	NO_TEST=1
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	NO_TEST=1
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	NO_TEST=1
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	NO_TEST=1
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	NO_TEST=1
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	NO_TEST=1
MEM_EVENT_L	NC_MEM_EVENT_L	NO_TEST=1
SMC_PF0	NC_SPI_SMC_MISO	NO_TEST=1
SMC_PF1	NC_SPI_SMC_MOSI	NO_TEST=1
SMC_PF2	NC_SPI_SMC_CLK	NO_TEST=1
SMC_PF3	NC_SPI_SMC_CS_L	NO_TEST=1

(MAKE_BASE=TRUE)

Platform Thermal Control

PECI Support

Level-shifter that allows SMC to drive PECI

Place this circuit near the Tee point to minimize reflections

=PP1V05_S0_SMC → CRITICAL Q5135 SSM3K15AMFVAP SOD

SMC_PECI_L IN 45 → R5135 0 5% 1/16W MF-LF 402 → SMC_PECI_L_R

OMIT R5136 NOSTUFF NONE NONE NONE 402

CPU_PECI_R 45 → R5138 43 5% 1/16W MF-LF 402 → CPU_PECI BI 6 14

R5137 330 5% 1/16W MF-LF 402

NOSTUFF C5137 47PF 5% 50V CER 0402

PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT

CRITICAL Q5125 SSM3K15AMFVAP SOD

CPU_PROCHOT_L BI 6 45 49 59 60 → C5125 47PF 5% 50V CER 0402

SMC_PROCHOT IN 45

Wire OR'd with CPU

PM_THRMTRIP_L IN 14 6

CRITICAL Q5123 SSM3K15AMFVAP SOD

This allows SMC to shutdown system.

=PP3V3_S5_SMC 70 46 → R5128 10K 5% 1/20W MF 201 → CPU_THRMTRIP_3V3 OUT 45

R5127 3.3K 5% 1/20W MF 201 — CPU_TT_OC_L

CRITICAL Q5127 BC846BLP DFN1006H4-3

SMC_THRMTRIP IN 45 → R5126 10K 5% 1/20W MF 201

This passes CPU's TRHMTRIP to SMC so shutdown reason can be recorded.

SMC 32KHz Clock

PM_CLK32K_SUSCLK_R IN 12 → R5160 51 5% 1/20W MF 201 → SMC_CLK32K OUT 45

PLACE_NEAR=U1100.Y6:10MM

SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal

CRITICAL Y5165 3.2X2.5MM-8M 12.000MHZ-30PPM-10PF-85C

SMC_EXTAL 45

NOSTUFF R5166 1M 5% 1/16W MF-LF 402

R5165 0 5% 1/16W MF-LF 402

SMC_XTAL_R → SMC_XTAL 45

C5165 12PF 5% 50V C0G 0402

C5166 12PF 5% 50V C0G 0402

Arch Pull Up/Down

R5148 0 5% 1/20W MF 0201 — PM_PCH_SYS_PWROK IN 69 18 12 → SMC_PM_PCH_SYS_PWROK OUT 45

R5149 0 5% 1/20W MF 0201 — CPU_CATERR_L IN 6 → SMC_CPU_CATERR_L OUT 45

R5154 1K 5% 1/20W MF 201 — SMC_TOPBLK_SWP_L IN 46 45 → PCH_STRP_TOPBLK_SWP_L OUT 12

=PP3V3_S0_SMC 70 → R5171 1K 5% 1/20W MF 201 — SMC_TOPBLK_SWP_L 46 45

=PP3V3_G3H_SMC 70 51 46 45

G3_POWERON_L 45	R5176	10K	1/20W MF 201
SMC_BC_ACOK 45	R5178	100K	1/20W MF 201
SMC_SYS_LED 45 (NOSTUFF)	R5179	100K	1/20W MF 201
SMS_INT_L 45	R5180	10K	1/20W MF 201
SMC_PME_S4_WAKE_L 45 33	R5181	10K	1/20W MF 201

PP3V3_S4_AP_FET 33

AP_EVENT_L 45 33	R5185	10K	1/20W MF 201
SMC_G3_WAKESRC_EN 45	R5118	100K	1/20W MF 201
BT_PWR_EN 46 33	R5119	100K	1/20W MF 201
SMC_DELAYED_PWRGD 69 45 29	R5186	100K	1/16W MF-LF 402
PM_DSW_PWRGD 69 45	R5184	100K	1/16W MF-LF 402
SMC_PM_G2_EN 58 45	R5187	100K	1/20W MF 201

Note:

Serial/JTAG Interface Pull-ups

=PP3V3_G3H_SMC 70 51 46 45

SMC_TX_L 45	R5190	10K	1/20W MF 201
SMC_RX_L 45	R5191	100K	1/20W MF 201
SMC_DEBUGPRT_TX_L 45 43	R5192	20K	1/20W MF 201
SMC_DEBUGPRT_RX_L 45 43	R5193	20K	1/20W MF 201
SMC_TCK 47 45	R5195	10K	1/20W MF 201
SMC_TDI 45	R5196	10K	1/20W MF 201
SMC_TDO 45	R5197	10K	1/20W MF 201
SMC_TMS 47 45	R5198	10K	1/20W MF 201

SYNC_MASTER=J70_NICK	SYNC_DATE=01/15/2014
PAGE TITLE	SMC: SMC Support
Apple Inc.	DRAWING NUMBER 051-1160
	SIZE D
	REVISION 2.0.0
	BRANCH
	PAGE 51 OF 105
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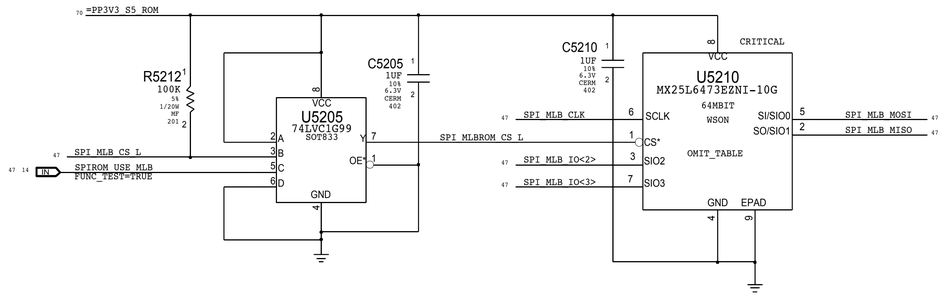
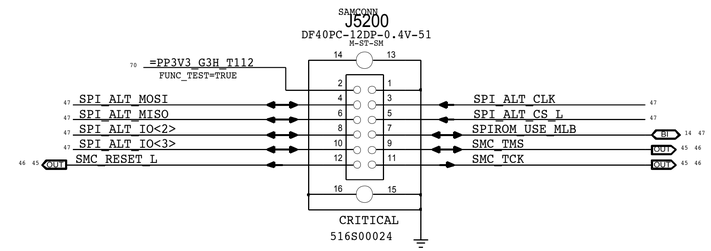
SPI BootROM

Quad_IO Mode (Mode 0 & 3) supported
SPI Freq: 50MHz for PCH, 20 MHz for SMC

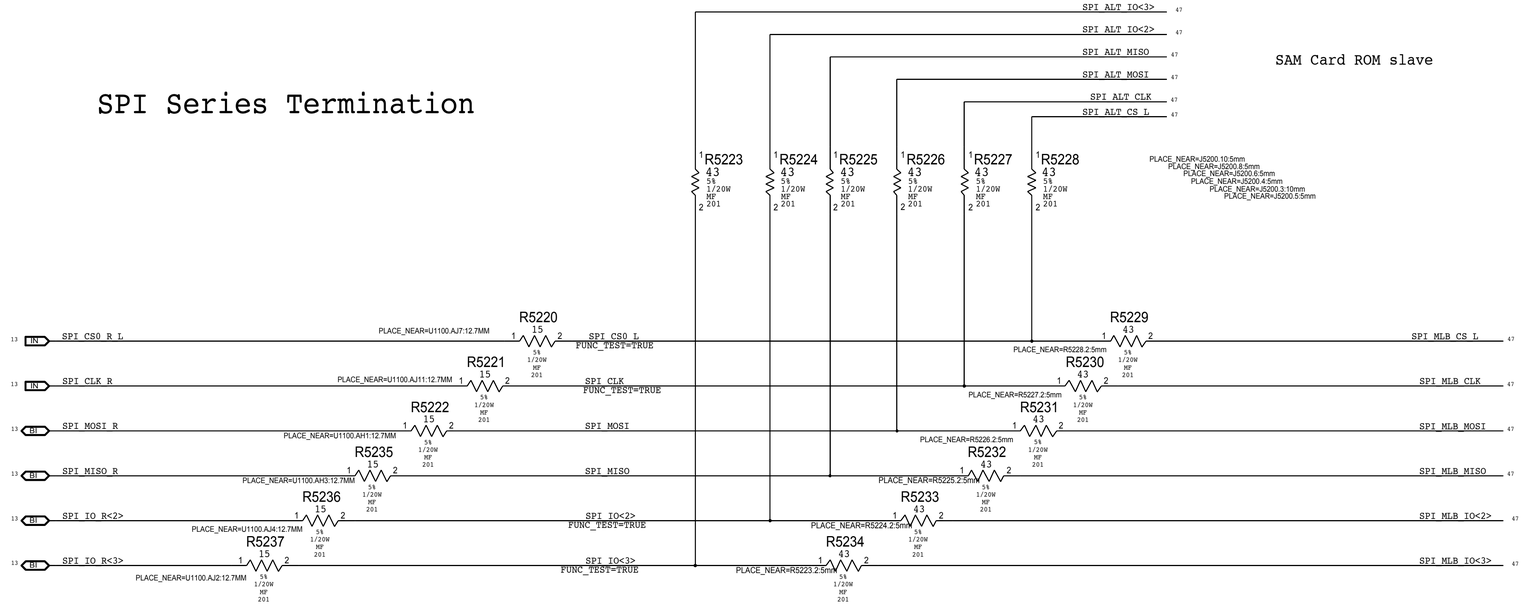


SPI+SWD SAM Connector



SPI Series Termination

SAM Card ROM slave



SYNC MASTER=J117 TONY SYNC DATE=05/05/2014

PAGE TITLE
CPU & CHIPSET: SPI and Debug Connector

Apple Inc.

DRAWING NUMBER 051-1160
SIZE D
REVISION 2.0.0
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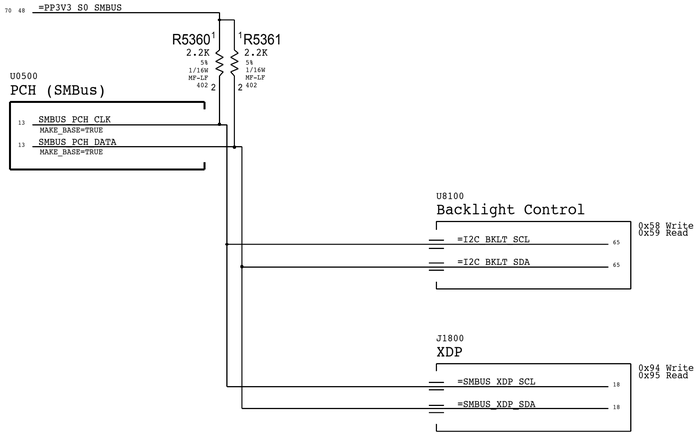
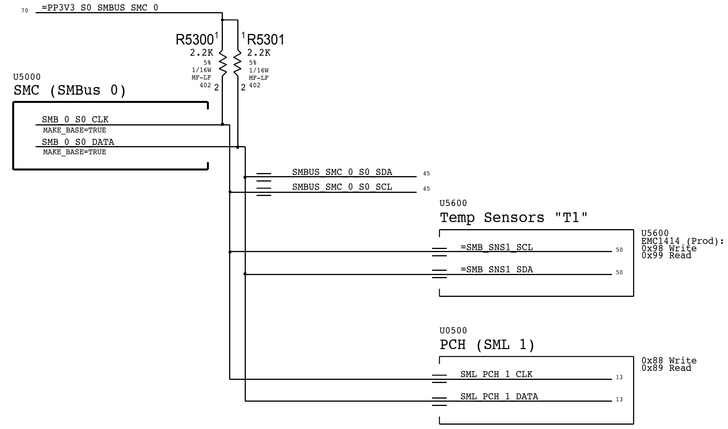
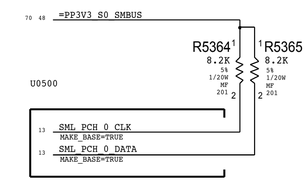
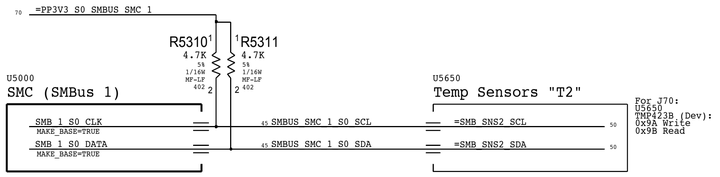
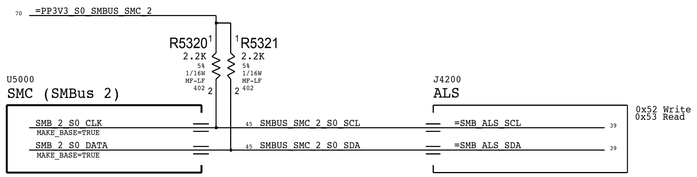


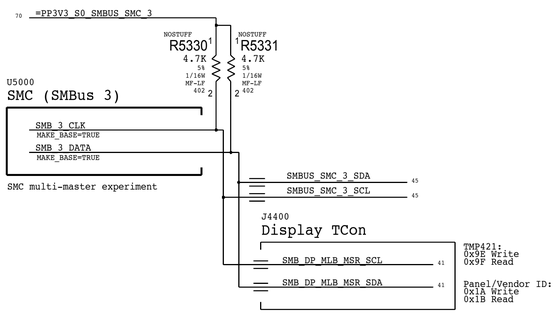




Unused PCH SM Link







SMC multi-master experiment

Line Legend

- Master
- Slave
- Mux

SYNC_MASTER=J70_NICK	SYNC_DATE=02/14/2014
PAGE TITLE: SMC: SMBus Connections	
Apple Inc.	DRAWING NUMBER: 051-1160 SIZE: D
	REVISION: 2.0.0
	BRANCH:
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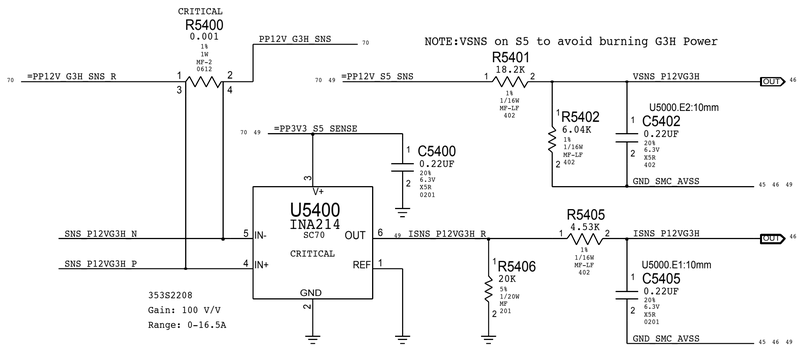
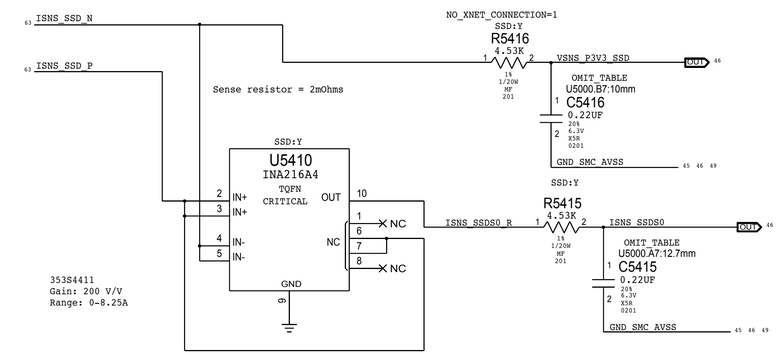
12V G3H (VD2R:ADC0/ID2R:ADC1)

AC/DC lowside sense (System total)



SSD S0 (IH1R:ADC21/VH1R:ADC20)

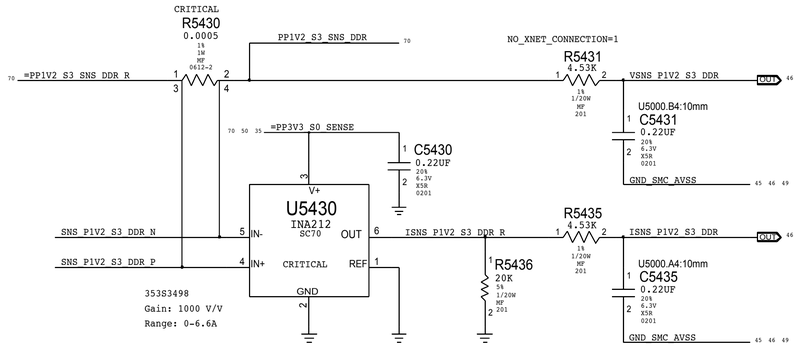
I-sense / V-sense for SSD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13280304	2	CAP,0.22UF,201	C5415,C5416	SSD:Y
11780201	2	RES,0 OHM,201	C5415,C5416	SSD:N

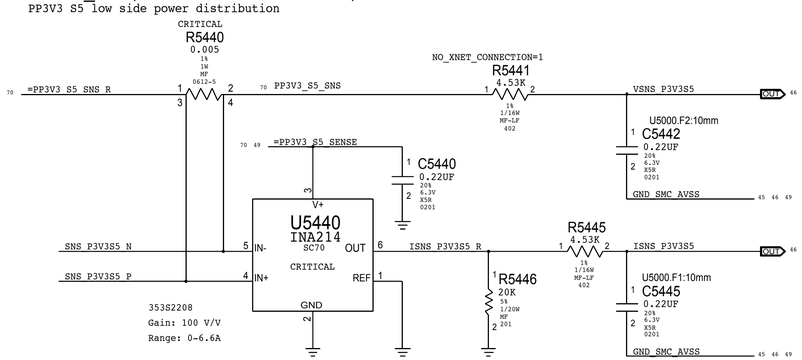
VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for DDR



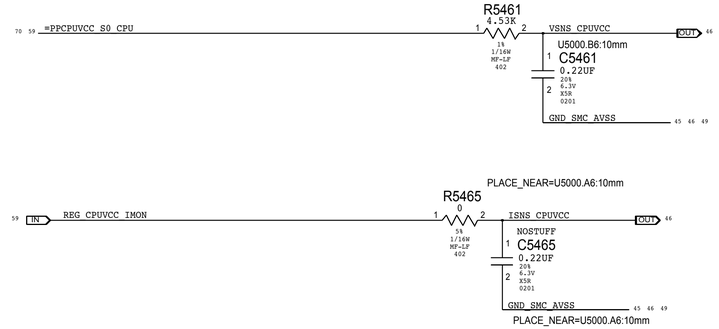
PP3V3_S5 (VR35:ADC2/IR35:ADC3)

PP3V3 S5 low side power distribution



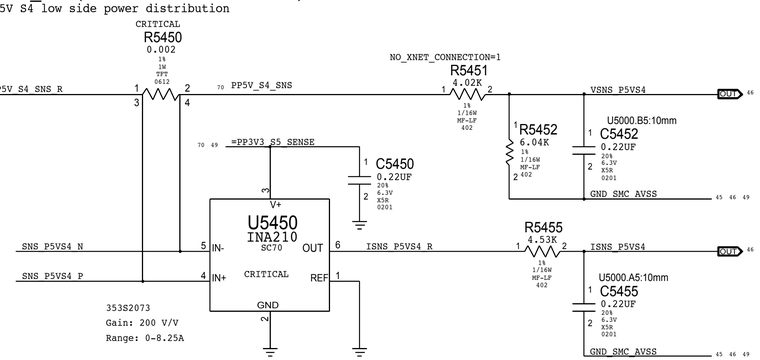
CPU Core (VC0C:ADC10/IC0C:ADC11)

Voltage sense and IMON amp (VC0C, IC0C)

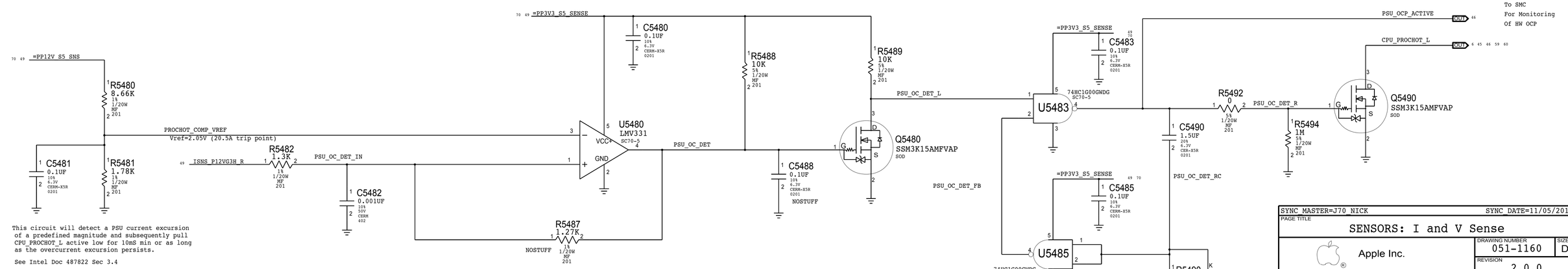


PP5V_S4 (VR54:ADC8/IR54:ADC9)

PP5V S4 low side power distribution



Fast Response PSU Overcurrent Protection



This circuit will detect a PSU current excursion of a predefined magnitude and subsequently pull CPU_PROCHOT_L active low for 10mS min or as long as the overcurrent excursion persists.

See Intel Doc 487822 Sec 3.4

SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

PAGE TITLE: SENSORS: I and V Sense

Apple Inc.

DRAWING NUMBER: 051-1160 SIZE: D

REVISION: 2.0.0

BRANCH:

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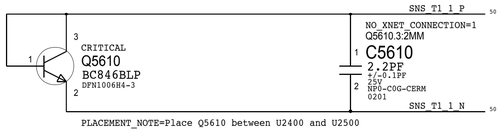
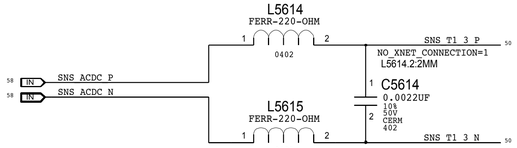
Temperature Sensor T1

LPDDR3 Proximity

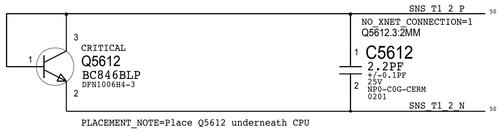


PLACEMENT_NOTE=Place Q5610 between U2400 and U2500

AC/DC Diode on supply

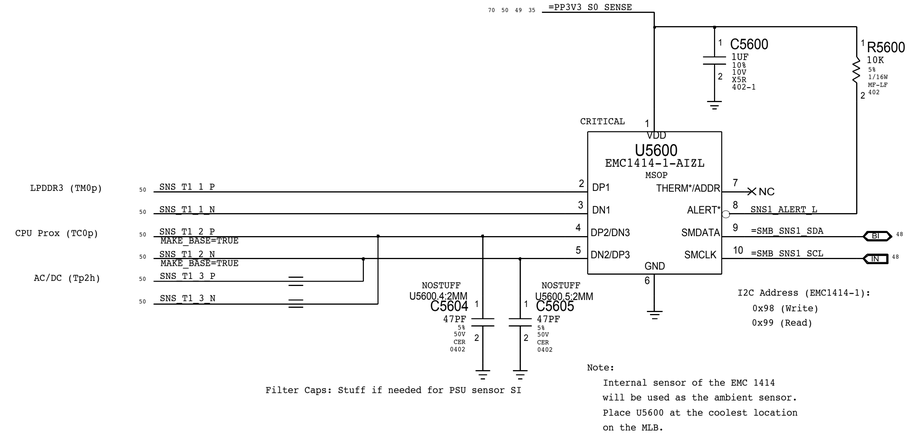


CPU Proximity



PLACEMENT_NOTE=Place Q5612 underneath CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

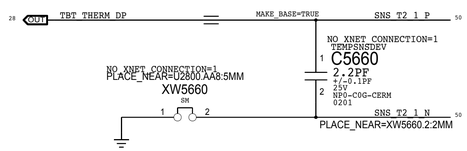


Filter Caps: Stuff if needed for PSU sensor SI

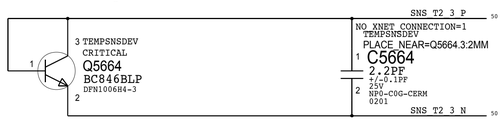
Note:
Internal sensor of the EMC 1414
will be used as the ambient sensor.
Place U5600 at the coolest location
on the MLB.

Temperature Sensor T2

TBT On Die

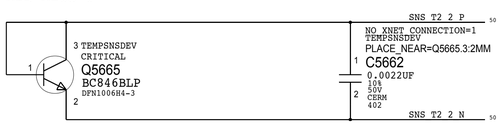


BLC Proximity

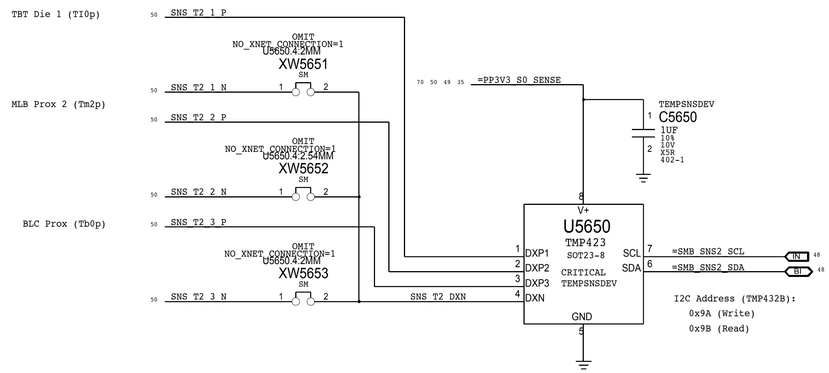


PLACEMENT_NOTE=Place Q5664 near BLC controller

MLB Misc 0



PLACEMENT_NOTE=PLACE Q5665 near CPU



I2C Address (TMP432B):
0x9A (Write)
0x9B (Read)

SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

PAGE TITLE
SENSORS: Temperature Sense

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D
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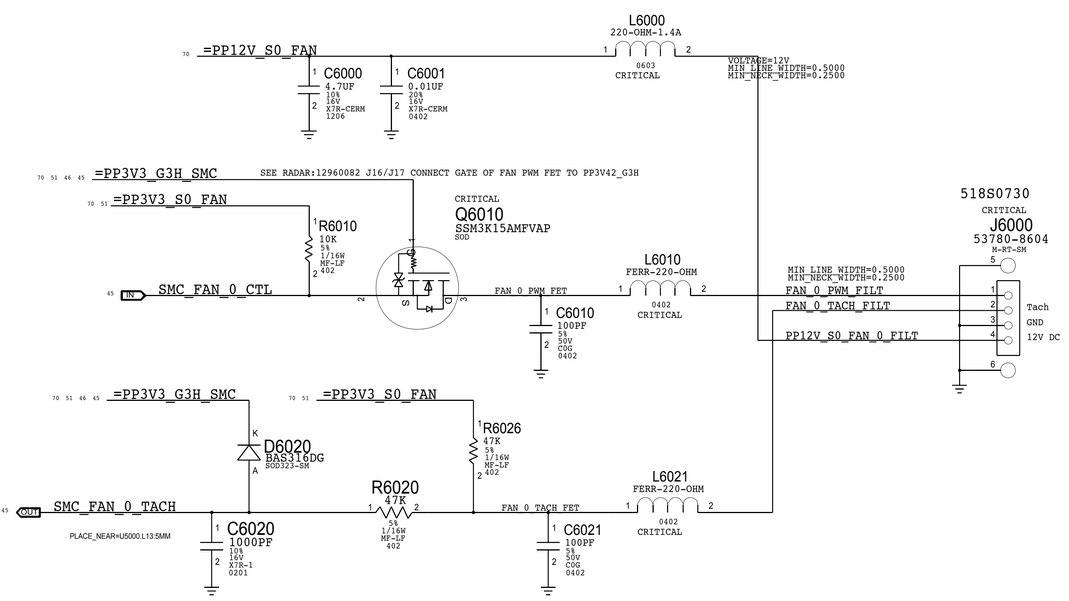
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Protol Fan Tach instability.

SMC Fan 1 (Unused)

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
FAN: System Fan Connector

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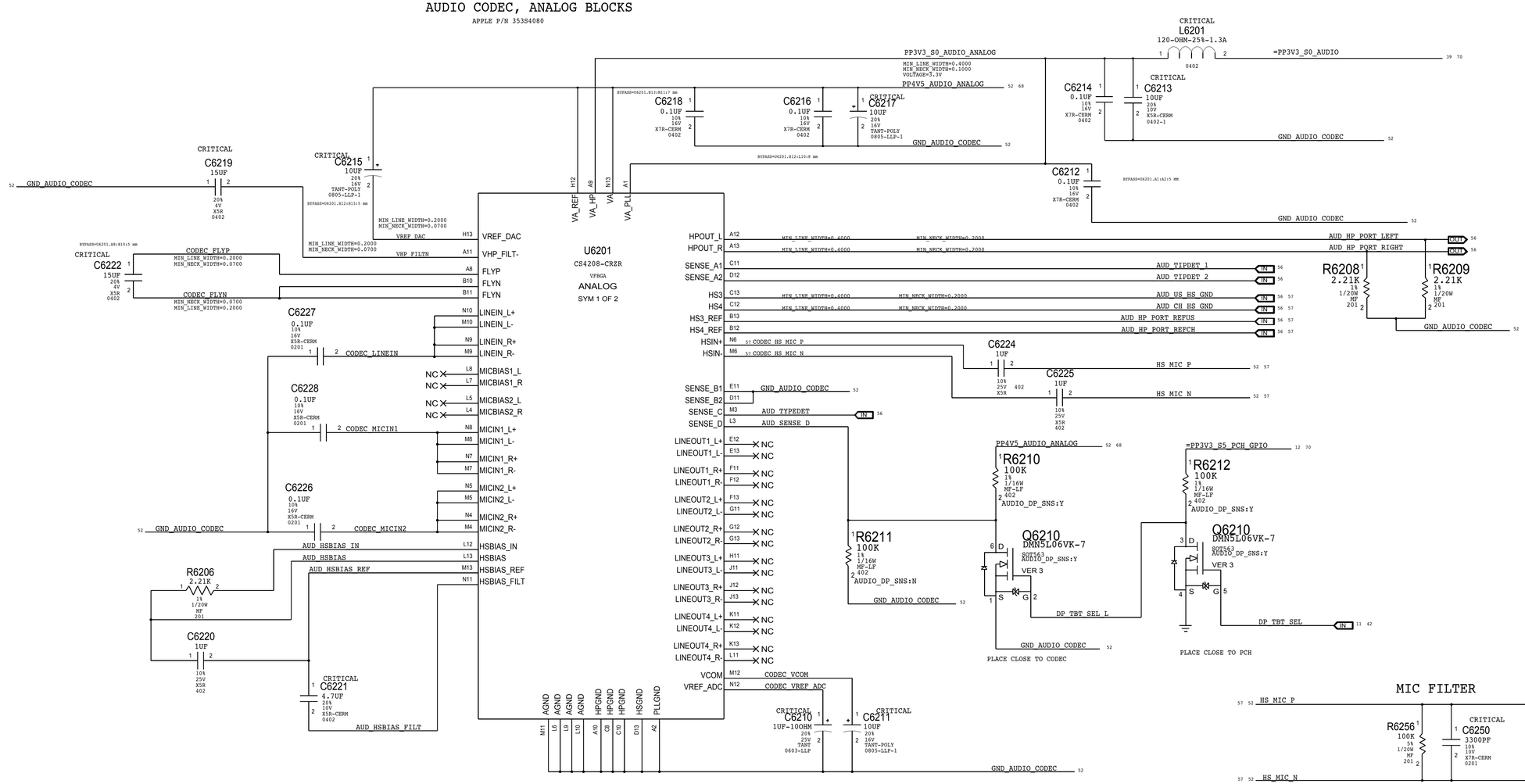
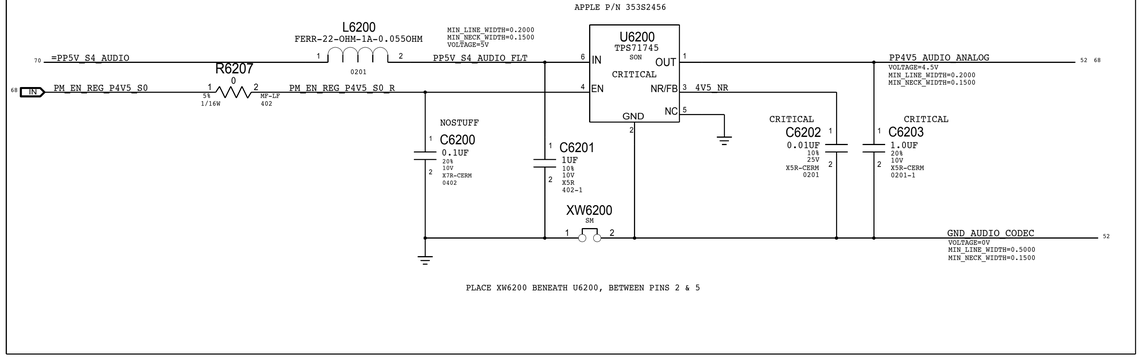
AUDIO CODEC, ANALOG BLOCKS

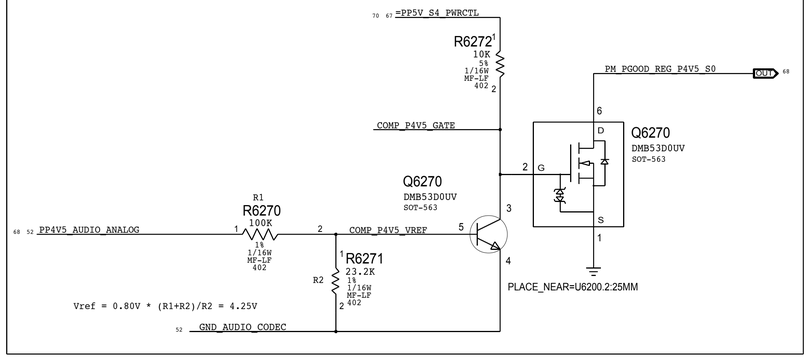
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC



4.5V COMPARATOR



SYNC_MASTER=J117_GAREN	SYNC_DATE=05/05/2014
PAGE TITLE	AUDIO: Codec (Analog)
Apple Inc.	DRAWING NUMBER 051-1160 · SIZE D
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AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.050HM
0201

=PP1V5_S0_AUDIO_DIG → PP1V5_S0_AUDIO_DIG_FILT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.5V

C6300 4.7UF 20% 4V X5R-1 402
C6301 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.J2:J1:13 mm
C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.E1:F1:11 mm

=PP3V3_S0_AUDIO_DIG
BYPASS=U6201.G1:F1:12 mm
C6303 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.K1:K3:6 mm
C6304 0.1UF 10% 6.3V CERM-X5R 0201
C6305 10UF 20% 10V X5R-CERM 0402-1
C6306 10UF 20% 10V X5R-CERM 0402-1
BYPASS=U6201.A7:E3:6 mm
C6307 0.1UF 10% 6.3V CERM-X5R 0201

=PP3V3_S0_AUDIO_DIG
R6358 1K 1% 1/16W MF-LF 402
R6359 1K 1% 1/16W MF-LF 402
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201
R6326 47.0K 1% 1/16W MF-LF 402
R6327 47.0K 1% 1/16W MF-LF 402

CODEC_SDA
CODEC_SCL

SPKR_AMP_SD
SPKR_AMP_FAULT
AUD_CONN_SPKR_VENDOR_ID_LEFT
AUD_CONN_SPKR_VENDOR_ID_RIGHT
DFET_OPENUS
DFET_OPENCH

R6340 0 5% 1/20W MF 0201
R6341 0 5% 1/20W MF 0201
R6342 22 5% 1/20W MF 201
R6343 0 5% 1/20W MF 0201

HDA_BIT_CLK
HDA_BIT_CLK_PORT
HDA_SYNC
HDA_SYNC_PORT
HDA_SDIN0
CS4208_HDA_SDOUT0_R
NC_CS4208_HDA_SDOUT1
HDA_SDOUT
HDA_SDOUT_PORT
HDA_RST_L

R6350 33 1% 1/20W MF 201
R6351 33 1% 1/20W MF 201
R6352 33 1% 1/20W MF 201
R6353 33 1% 1/20W MF 201

MCLKA_SPKR_LEFT
SCLKA_SPKR_LEFT
LRCLKA_SPKR_LEFT
SDOUTA_SPKR_LEFT

R6360 33 1% 1/20W MF 201
R6361 33 1% 1/20W MF 201
R6362 33 1% 1/20W MF 201
R6363 33 1% 1/20W MF 201

MCLKB_SPKR_RIGHT
SCLKB_SPKR_RIGHT
LRCLKB_SPKR_RIGHT
SDOUTB_SPKR_RIGHT

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

J2	VD	
E1	VL_HD	
A7	VL_SP	
G1	VL_LF	
K1	VL_DM	
H3	GPIO0	
H2	GPIO1	
H1	GPIO2	
C4	GPIO3	
C5	GPIO4	
C7	GPIO5	
C9	GPO0	NC
B9	GPO1	NC
F2	BCLK	
E2	SYNC	
D1	SDI0	
C1	SDI1	
D2	SDO0	
C2	SDO1	
C3	SDO2	
B1	SDO3	
D3	RST*	
A5	MCLK_A	
B2	SCLK_A	
B4	LRCK_A	
A3	SDOUT_A	
B3	SDIN_A	
A6	MCLK_B	
B6	SCLK_B	
B5	LRCK_B	
B8	SDOUT_B	
A4	SDIN_B	
C6	SDA	
B7	SCL	
G3	SPDIF_IN	CS4208_SPDIF_IN
G2	SPDIF_OUT	CS4208_SPDIF_OUT
N3	DMIC_SDA0	
N2	DMIC_SCL0	NC
N1	DMIC_SDA1	
M1	DMIC_SCL1	NC
M2	DMIC_SDA2	
L1	DMIC_SCL2	NC
K2	DMIC_SDA3	DMIC_SDA3_R
L2	DMIC_SCL3	DMIC_CLK3_R
F6	NC	
F7	NC	
F8	NC	
G6	NC	
G7	NC	
G8	NC	
H6	NC	
H7	NC	
H8	NC	
J1	DGND	
F1	LGND	
E3	LGND	
F3	LGND	
J3	LGND	
K3	LGND	

R6302 0 5% 1/20W MF 0201
DP_INT_SPDIF_AUDIO → IN 41

R6330 33 5% 1/16W MF-LF 402
SPDIF_OUT_JACK → OUT 56

R6333 0 5% 1/20W MF 0201
DMIC_SDA3 → IN 39

R6332 75 1% 1/16W MF-LF 402
DMIC_CLK3 → OUT 39

PAGE TITLE
AUDIO: Codec (Digital)

Apple Inc.

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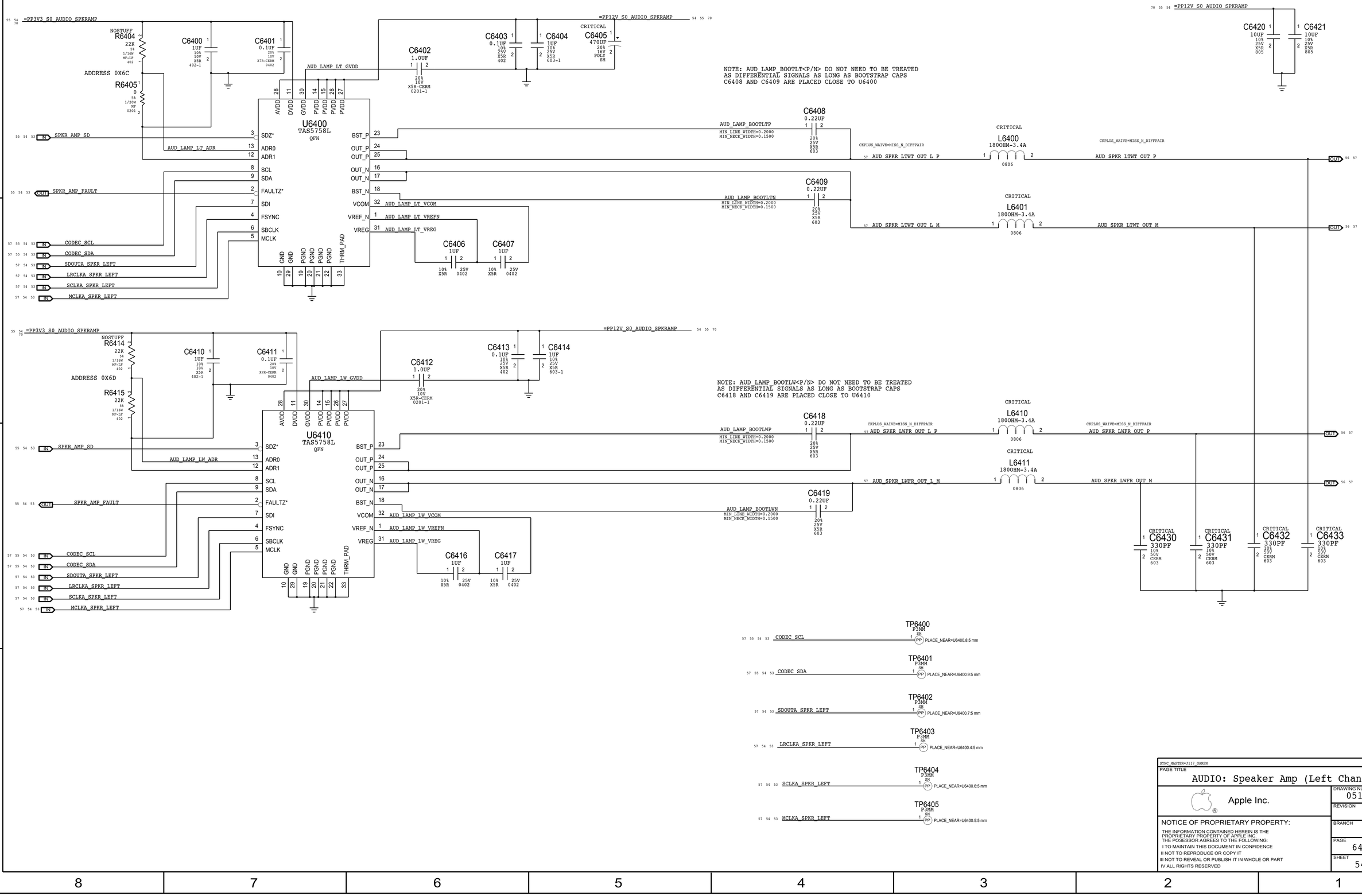
2X MONO SPEAKER AMPLIFIERS (TAS5758L)

APN: TBD

GAIN = TBD

SPEAKER AMPLIFIERS - LEFT CHANNEL



SYNC_MASTER=J117_CAREN SYNC_DATE=05/05/2014

PAGE TITLE

AUDIO: Speaker Amp (Left Channel)

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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2X MONO SPEAKER AMPLIFIERS (TAS5758L)

APN: TBD

GAIN = TBD

SPEAKER AMPLIFIERS - RIGHT CHANNEL

=PP3V3_S0_AUDIO_SPKRAMP

=PP12V_S0_AUDIO_SPKRAMP

R6504 22K 5% 1/16W MF-LF 402

ADDRESS 0X6E

NOSTUFF R6505 22K 5% 1/16W MF-LF 402

C6500 1UF 10% 10V X5R 402-1

C6501 0.1UF 20% 10V X7R-CERM 0402

C6502 1.0UF 20% 10V X5R-CERM 0201-1

C6503 0.1UF 10% 25V X5R 402

C6504 1UF 10% 25V X5R 603-1

CRITICAL C6505 470UF 20% 16V POLY SM

C6520 10UF 10% 25V X5R 805

C6521 10UF 10% 25V X5R 805

AUD_RAMP_RT_GVDD

U6500 TAS5758L QFN

28	AVDD	BST_P	23
11	DVDD	OUT_P	24
30	GVDD	OUT_P	25
14	PVDD	OUT_N	16
15	PVDD	OUT_N	17
26	PVDD	BST_N	18
27	PVDD	VCOM	32 (AUD_RAMP_RT_VCOM)
3	SDZ*	VREF_N	1 (AUD_RAMP_RT_VREFN)
13	ADR0	VREG	31 (AUD_RAMP_RT_VREG)
12	ADR1		
8	SCL		
9	SDA		
2	FAULTZ*		
7	SDI		
4	FSYNC		
6	SBCLK		
5	MCLK		
10, 29	GND		
19, 20, 21, 22	PGND		
33	THRM_PAD		

AUD_RAMP_RT_ADR

SPKR_AMP_SD (IN)

SPKR_AMP_FAULT (OUT)

CODEC_SCL (IN)

CODEC_SDA (IN)

SDOUTB_SPKR_RIGHT (IN)

LRCLKB_SPKR_RIGHT (IN)

SCLKB_SPKR_RIGHT (IN)

MCLKB_SPKR_RIGHT (IN)

C6506 1UF 10% 10V X5R 0402

C6507 1UF 10% 10V X5R 0402

NOTE: AUD_LAMP_BOOTRT<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6508 AND C6509 ARE PLACED CLOSE TO U6500

AUD_RAMP_BOOTRTP

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

C6508 0.22UF 20% 25V X5R 603

CKPLUS_WAIVE=MISS_N_DIFFPAIR

AUD_SPKR_RTWT_OUT_L_P

CRITICAL L6500 180OHM-3.4A 0806

AUD_SPKR_RTWT_OUT_P (OUT)

AUD_RAMP_BOOTRTN

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

C6509 0.22UF 20% 25V X5R 603

AUD_SPKR_RTWT_OUT_L_M

CRITICAL L6501 180OHM-3.4A 0806

AUD_SPKR_RTWT_OUT_M (OUT)

=PP3V3_S0_AUDIO_SPKRAMP

=PP12V_S0_AUDIO_SPKRAMP

R6514 0 5% 1/20W MF 0201

ADDRESS 0X6F

NOSTUFF R6515 22K 5% 1/16W MF-LF 402

C6510 1UF 10% 10V X5R 402-1

C6511 0.1UF 20% 10V X7R-CERM 0402

C6512 1.0UF 20% 10V X5R-CERM 0201-1

C6513 0.1UF 10% 25V X5R 402

C6514 1UF 10% 25V X5R 603-1

AUD_RAMP_RW_GVDD

U6510 TAS5758L QFN

28	AVDD	BST_P	23
11	DVDD	OUT_P	24
30	GVDD	OUT_P	25
14	PVDD	OUT_N	16
15	PVDD	OUT_N	17
26	PVDD	BST_N	18
27	PVDD	VCOM	32 (AUD_RAMP_RW_VCOM)
3	SDZ*	VREF_N	1 (AUD_RAMP_RW_VREFN)
13	ADR0	VREG	31 (AUD_RAMP_RW_VREG)
12	ADR1		
8	SCL		
9	SDA		
2	FAULTZ*		
7	SDI		
4	FSYNC		
6	SBCLK		
5	MCLK		
10, 29	GND		
19, 20, 21, 22	PGND		
33	THRM_PAD		

AUD_RAMP_RW_ADR

SPKR_AMP_SD (IN)

SPKR_AMP_FAULT (OUT)

CODEC_SCL (IN)

CODEC_SDA (IN)

SDOUTB_SPKR_RIGHT (IN)

LRCLKB_SPKR_RIGHT (IN)

SCLKB_SPKR_RIGHT (IN)

MCLKB_SPKR_RIGHT (IN)

C6516 1UF 10% 10V X5R 0402

C6517 1UF 10% 10V X5R 0402

NOTE: AUD_LAMP_BOOTRW<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6518 AND C6519 ARE PLACED CLOSE TO U6510

AUD_RAMP_BOOTRWP

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

C6518 0.22UF 20% 25V X5R 603

CKPLUS_WAIVE=MISS_N_DIFFPAIR

AUD_SPKR_RWFR_OUT_L_P

CRITICAL L6510 180OHM-3.4A 0806

AUD_SPKR_RWFR_OUT_P (OUT)

AUD_RAMP_BOOTRWN

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

C6519 0.22UF 20% 25V X5R 603

AUD_SPKR_RWFR_OUT_L_M

CRITICAL L6511 180OHM-3.4A 0806

AUD_SPKR_RWFR_OUT_M (OUT)

CRITICAL C6530 330PF 10% 50V CERM 603

CRITICAL C6531 330PF 10% 50V CERM 603

CRITICAL C6532 330PF 10% 50V CERM 603

CRITICAL C6533 330PF 10% 50V CERM 603

TP6500 P3MM SM — CODEC_SCL — PLACE_NEAR=U6510.8:5 mm

TP6501 P3MM SM — CODEC_SDA — PLACE_NEAR=U6510.9:5 mm

TP6502 P3MM SM — SDOUTB_SPKR_RIGHT — PLACE_NEAR=U6510.7:5 mm

TP6503 P3MM SM — LRCLKB_SPKR_RIGHT — PLACE_NEAR=U6510.4:5 mm

TP6504 P3MM SM — SCLKB_SPKR_RIGHT — PLACE_NEAR=U6510.6:5 mm

TP6505 P3MM SM — MCLKB_SPKR_RIGHT — PLACE_NEAR=U6510.5:5 mm

SYNC_MASTER=J117_GAREN

SYNC_DATE=05/05/2014

PAGE TITLE

AUDIO: Speaker Amp (Right Channel)

Apple Inc.

DRAWING NUMBER 051-1160

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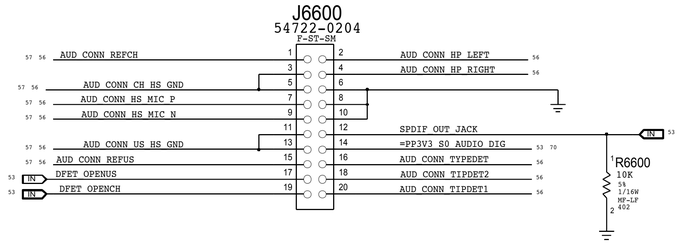
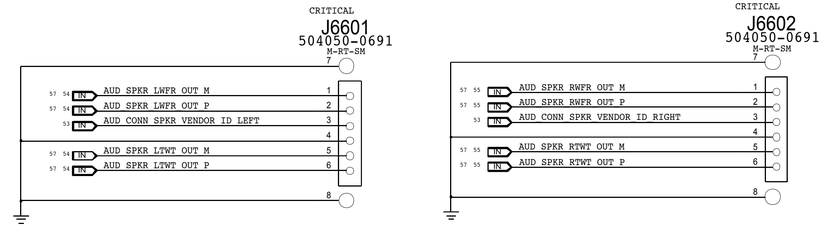
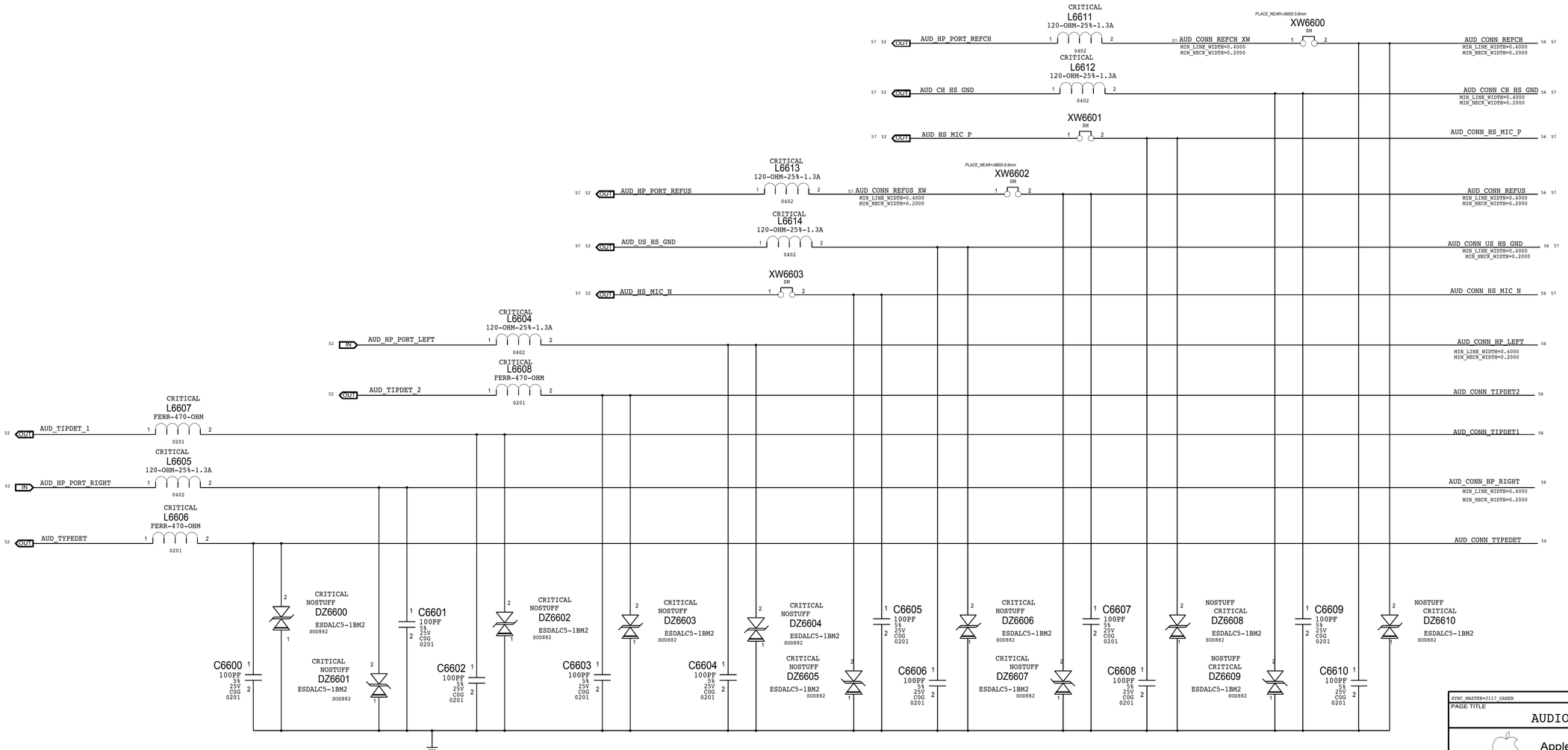
SPEAKER CONNECTOR





Reversed Phases 1 & 2 and 5 & 6 on J6601 and J6602 Ref J16



ESD DIODES (DZ6600 -> DZ6610) NOW NOSTUFF - MAY BE ADDED FOLLOWING ESD TESTING

SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2016

PAGE TITLE

AUDIO: Jack Translators

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR_INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO_ISO	*	0.1 MM	?
SPKROUT_ISO	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
AUDIODIFF_2MM	*	Y	0.2 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	AUDIO_ISO
SPKROUT	*	*	SPKROUT_ISO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SPEAKER OUTPUTS				
T205 AUDIO_DIFFPAIR	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	55 56
T203 AUDIO_DIFFPAIR	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RWFR_OUT_M	55 56
T220	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_P	55
T219	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_M	55
T333 AUDIO_DIFFPAIR	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	55 56
T332 AUDIO_DIFFPAIR	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RTWT_OUT_M	55 56
T330	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_P	55
T331	SPKROUT_DIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_M	55
T337 ?	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	54 56
T336 ?	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LWFR_OUT_M	54 56
T334	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_P	54
T335	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_M	54
T341 AUDIO_DIFFPAIR	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	54 56
T340 ?	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LTWT_OUT_M	54 56
T338	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_P	54
T339	SPKROUT_DIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_M	54
HEADSET MIC				
T345 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	AUD_CONN_HS_MIC_P	56
T346 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	AUD_CONN_HS_MIC_N	56
T250 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	AUD_HS_MIC_P	52 56
T255 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	AUD_HS_MIC_N	52 56
T374 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	HS_MIC_P	52
T375 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	HS_MIC_N	52
T343 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	CODEC_HS_MIC_P	52
T342 AUDIO_DIFFPAIR	AUDIO_DIFF	AUDIO	CODEC_HS_MIC_N	52
T354		AUDIO	AUD_CONN_CH_HS_GND	56
T356		AUDIO	AUD_CONN_US_HS_GND	56
T168		AUDIO	AUD_CH_HS_GND	52 56
T169		AUDIO	AUD_US_HS_GND	52 56
T352		AUDIO	AUD_CONN_REFCH	56
T353		AUDIO	AUD_CONN_REFUS	56
T371		AUDIO	AUD_CONN_REFCH_XW	56
T370		AUDIO	AUD_CONN_REFUS_XW	56
T372		AUDIO	AUD_HP_PORT_REFCH	52 56
T373		AUDIO	AUD_HP_PORT_REFUS	52 56

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CODEC SCL & SDA				
T358			CODEC_SCL	53 54 55
T359			CODEC_SDA	53 54 55
TDM				
T360		?	MCLKA_SPKR_LEFT	53 54
T361		?	SCLKA_SPKR_LEFT	53 54
T362		?	LRCLKA_SPKR_LEFT	53 54
T363		?	SDOUTA_SPKR_LEFT	53 54
T378			MCLKA_SPKR_LEFT_R	53
T379			SCLKA_SPKR_LEFT_R	53
T380			LRCLKA_SPKR_LEFT_R	53
T377			SDOUTA_SPKR_LEFT_R	53
T364		?	MCLKB_SPKR_RIGHT	53 55
T365		?	SCLKB_SPKR_RIGHT	53 55
T367		?	LRCLKB_SPKR_RIGHT	53 55
T366		?	SDOUTB_SPKR_RIGHT	53 55
T375			MCLKB_SPKR_RIGHT_R	53
T376			SCLKB_SPKR_RIGHT_R	53
T382			LRCLKB_SPKR_RIGHT_R	53
T381			SDOUTB_SPKR_RIGHT_R	53

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

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AUDIO: Speaker ID

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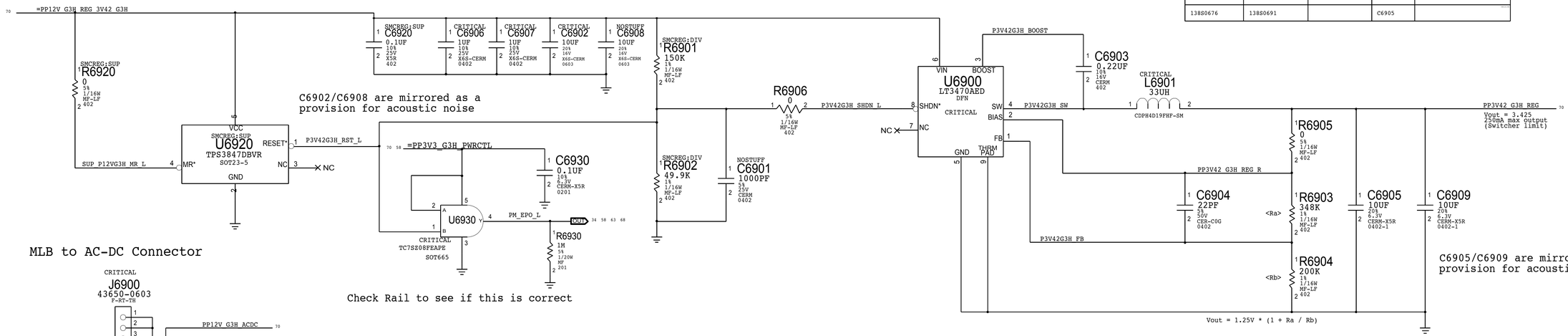
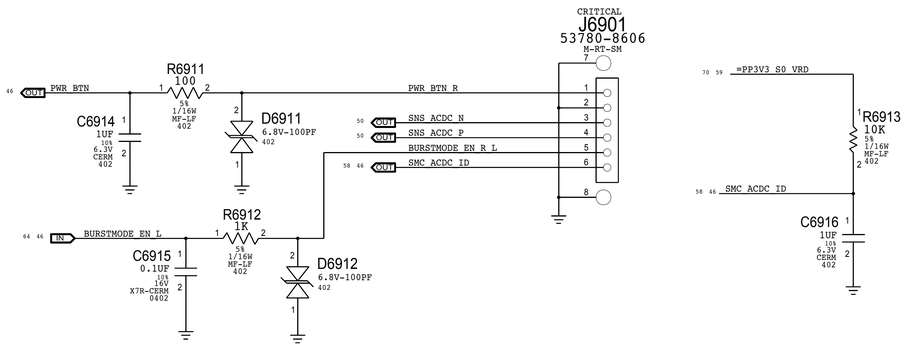
3.425V "G3Hot" Regulator

Switching freq: 409 kHz = 13.5 / L6901

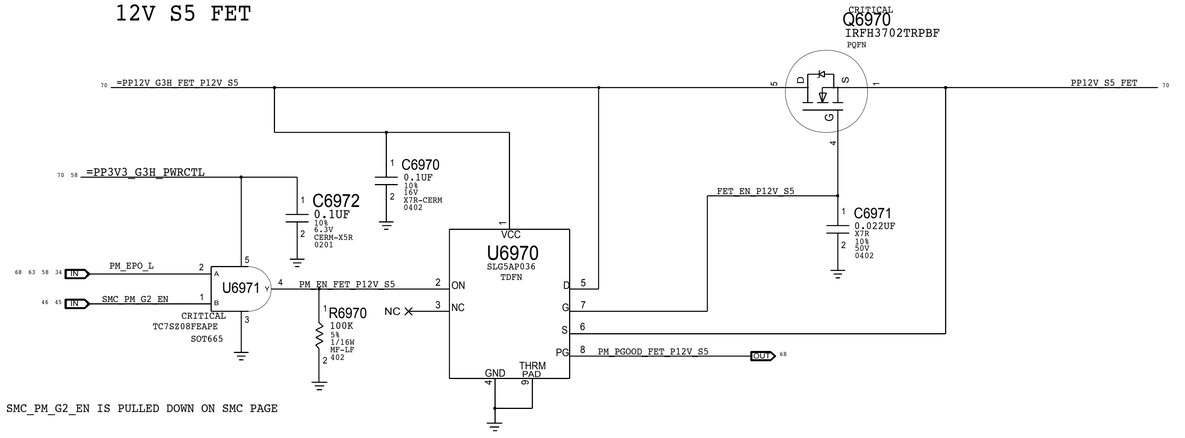
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6905	



MLB to AC-DC Supplemental Signal Connector



12V S5 FET



SYNC_MASTER=J117_ANDRES	SYNC_DATE=03/24/2014
PAGE TITLE: PLATFORM POWER: Connectors / VReg G3Hot	
Apple Inc.	DRAWING NUMBER: 051-1160 · SIZE: D
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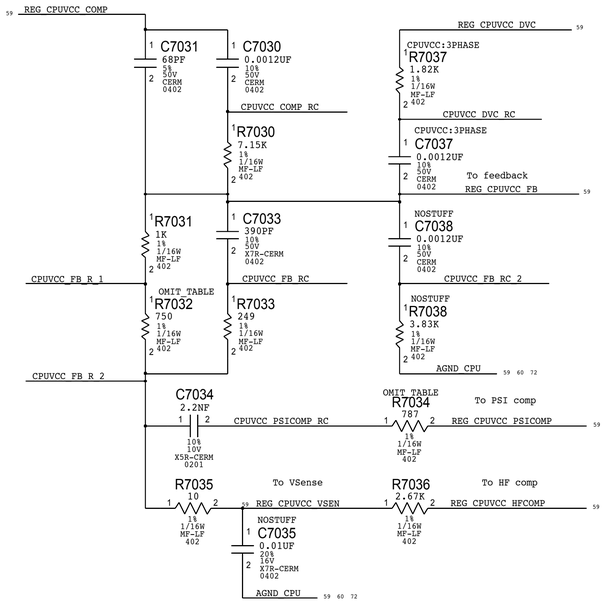
CPU VCC S0 Regulator

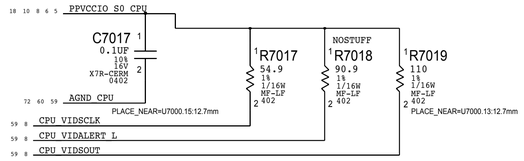
OC trip point: 114 A

Switching freq: 403 kHz = 5 E10 / R7003

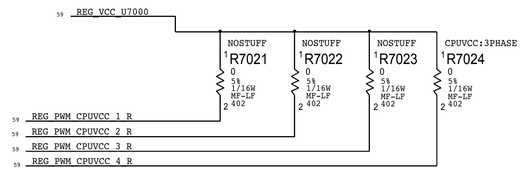
Compensation and feedback

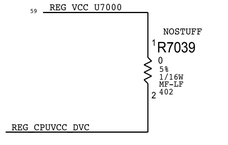


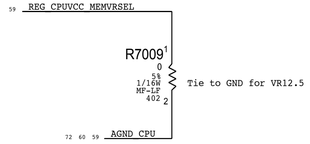
Pull-ups 1

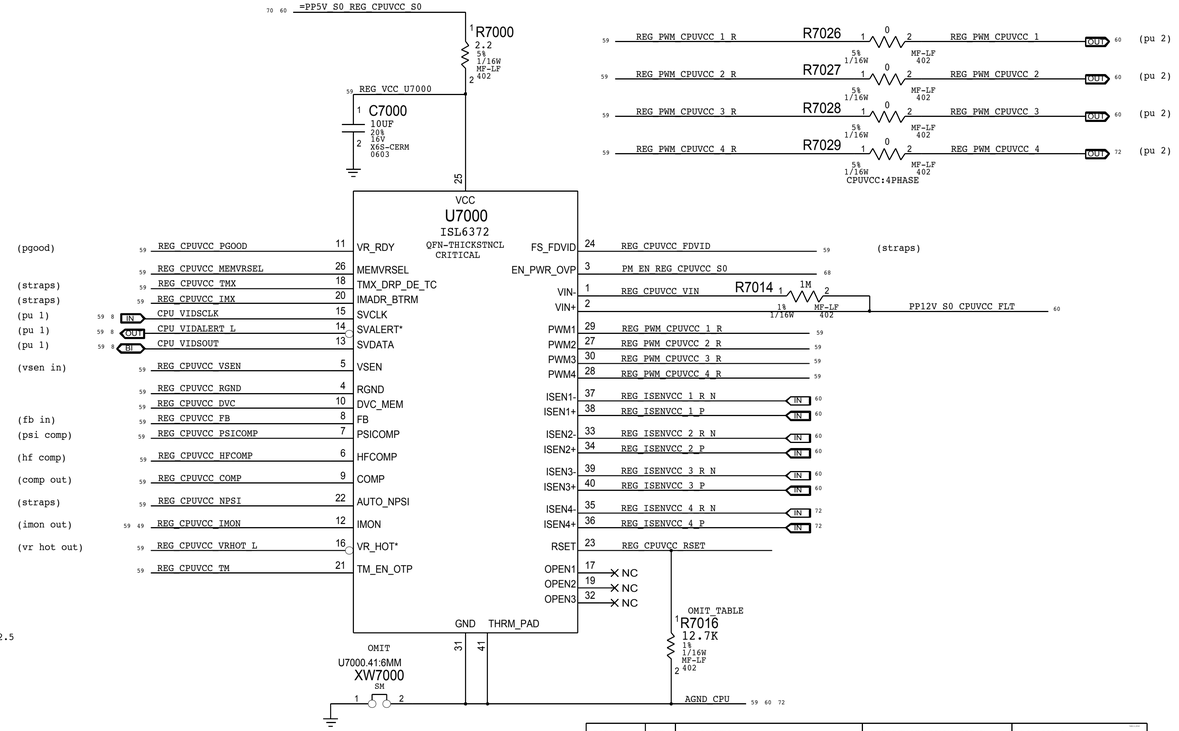


Pull-ups 2



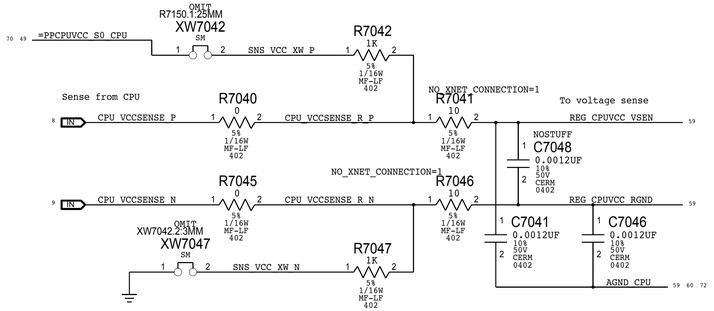




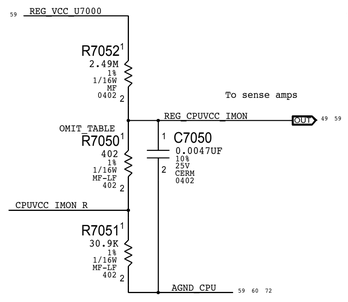


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0324	1	RES,12.7K,402	R7016	CPUVCC:3PHASE
114S0316	1	RES,10.2K,402	R7016	CPUVCC:4PHASE

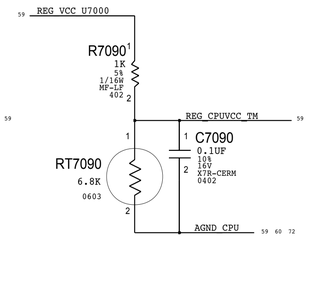
Voltage sense input



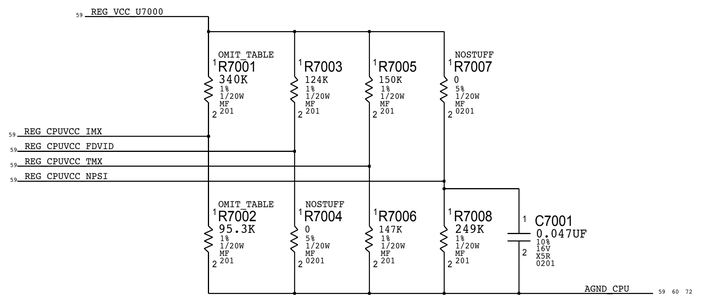
IMON output



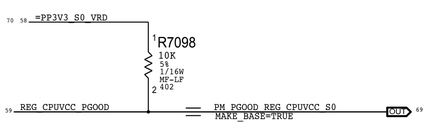
Temp measurement



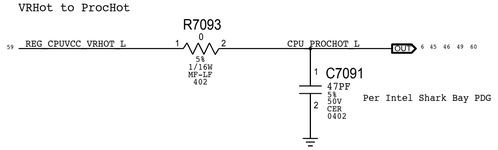
Straps



Power goods



VRHot to ProcHot



J16: 3PHASE
J17: 4PHASE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0311	1	RES,340K,201	R7001	CPUVCC:3PHASE
118S0116	1	RES,158K,201	R7001	CPUVCC:4PHASE
118S0575	1	RES,95.3K,201	R7002	CPUVCC:3PHASE
118S0380	1	RES,44.2K,201	R7002	CPUVCC:4PHASE
114S0206	1	RES,750 OHM,402	R7032	CPUVCC:3PHASE
114S0210	1	RES,825 OHM,402	R7032	CPUVCC:4PHASE
114S0208	1	RES,787 OHM,402	R7034	CPUVCC:3PHASE
114S0189	1	RES,499 OHM,402	R7034	CPUVCC:4PHASE
114S0179	1	RES,402 OHM,402	R7050	CPUVCC:3PHASE
114S0184	1	RES,453 OHM,402	R7050	CPUVCC:4PHASE

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

PAGE TITLE

PLATFORM POWER: VReg CPU VCC Cntl

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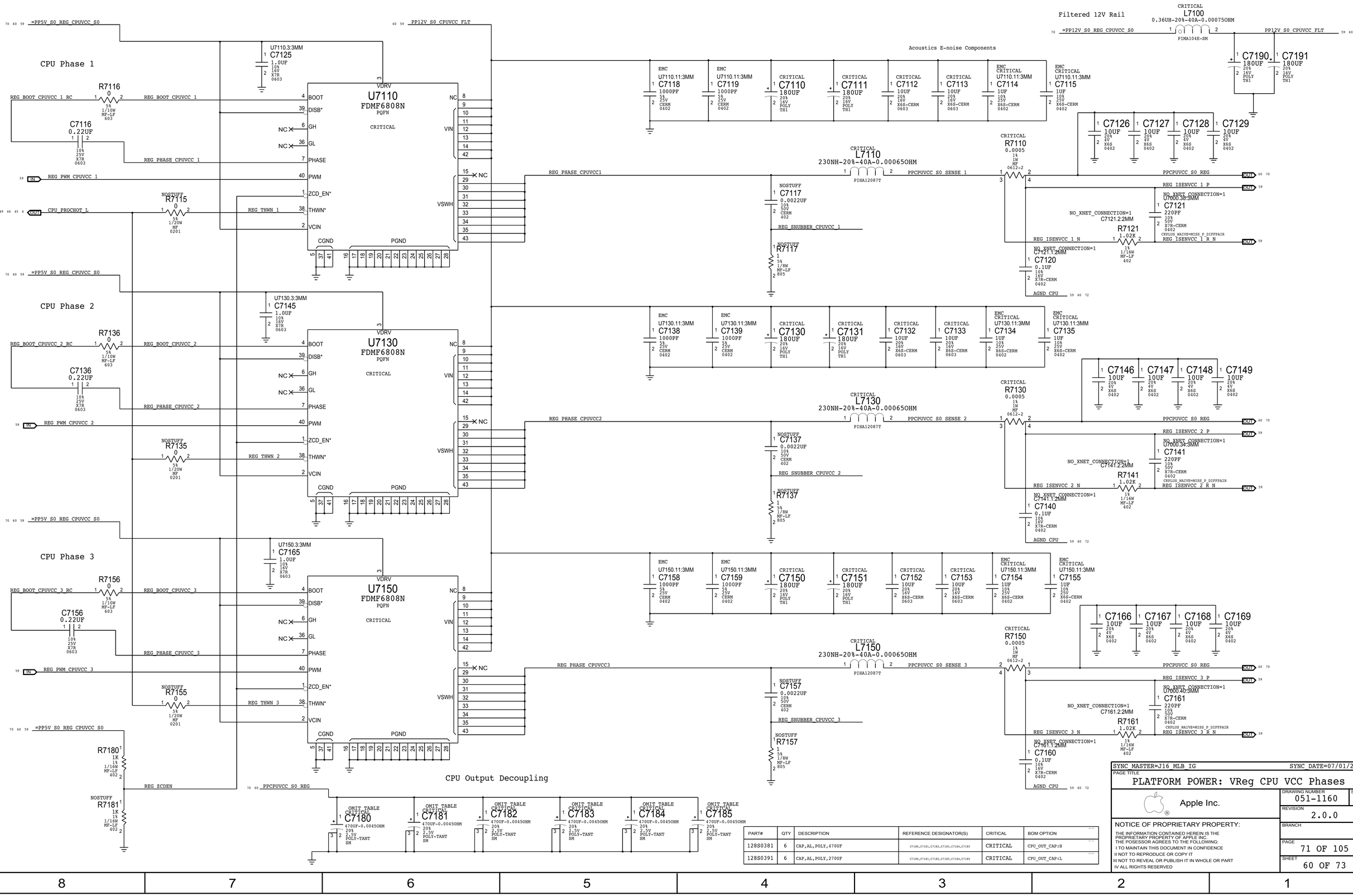

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0381	6	CAP,AL,POLY,470UF	C7180,C7181,C7182,C7183,C7184,C7185	CRITICAL	CPU_OUT_CAP:H
128S0391	6	CAP,AL,POLY,270UF	C7180,C7181,C7182,C7183,C7184,C7185	CRITICAL	CPU_OUT_CAP:L

SYNC_MASTER=J16_MLB_IG SYNC_DATE=07/01/2014

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PLATFORM POWER: VReg CPU VCC Phases

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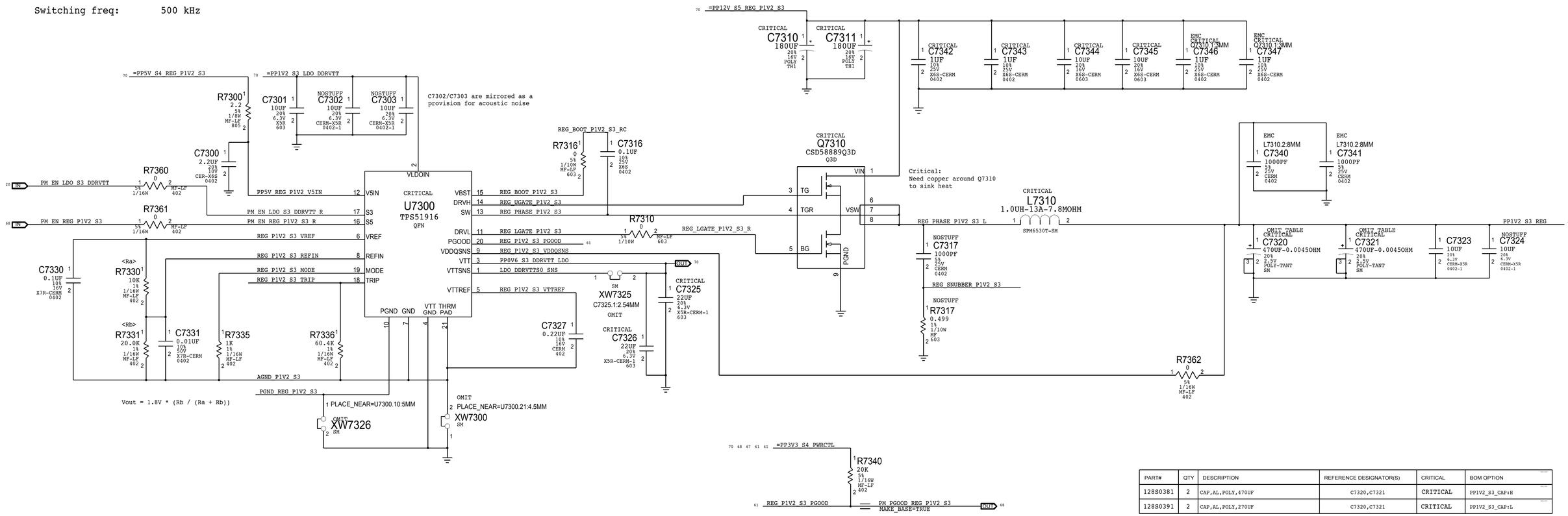
VDDQ 1.2V S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{\text{R7336}}{\text{8 E5 * Rds(Q7310)}} + \frac{0.65625}{\text{L7310 * f(switch)}}$

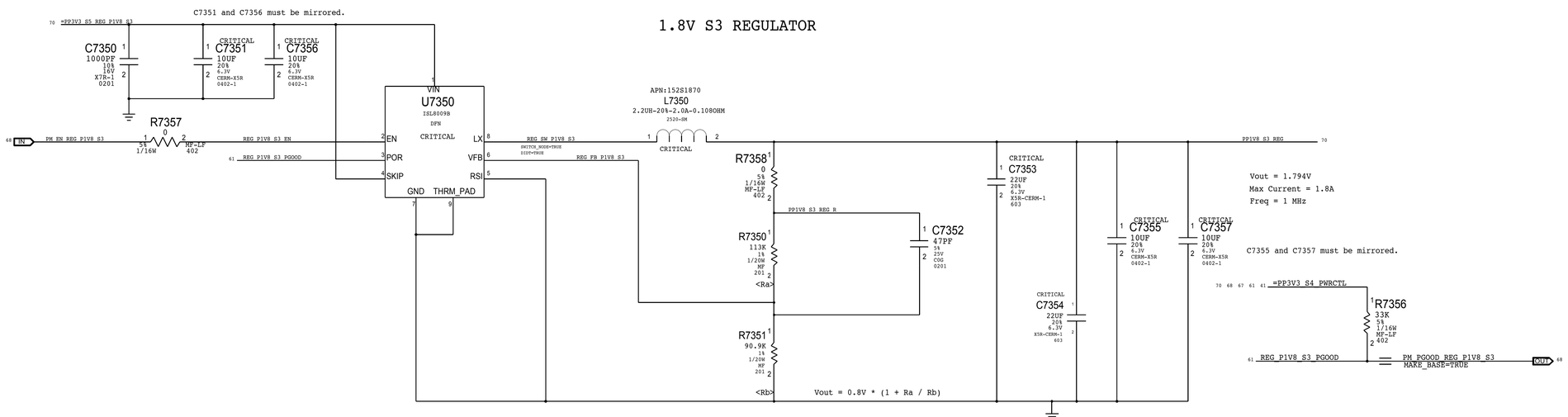
3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0381	2	CAP,AL,POLY,470UF	C7320,C7321	CRITICAL	PP1V2_S3_CAP:H
128S0391	2	CAP,AL,POLY,270UF	C7320,C7321	CRITICAL	PP1V2_S3_CAP:L

1.8V S3 REGULATOR



SYNC_MASTER=J70_ROSSANA SYNC_DATE=09/12/2013

PAGE TITLE: PLATFORM POWER: VReg VDDQ S3 / 1.8V S3

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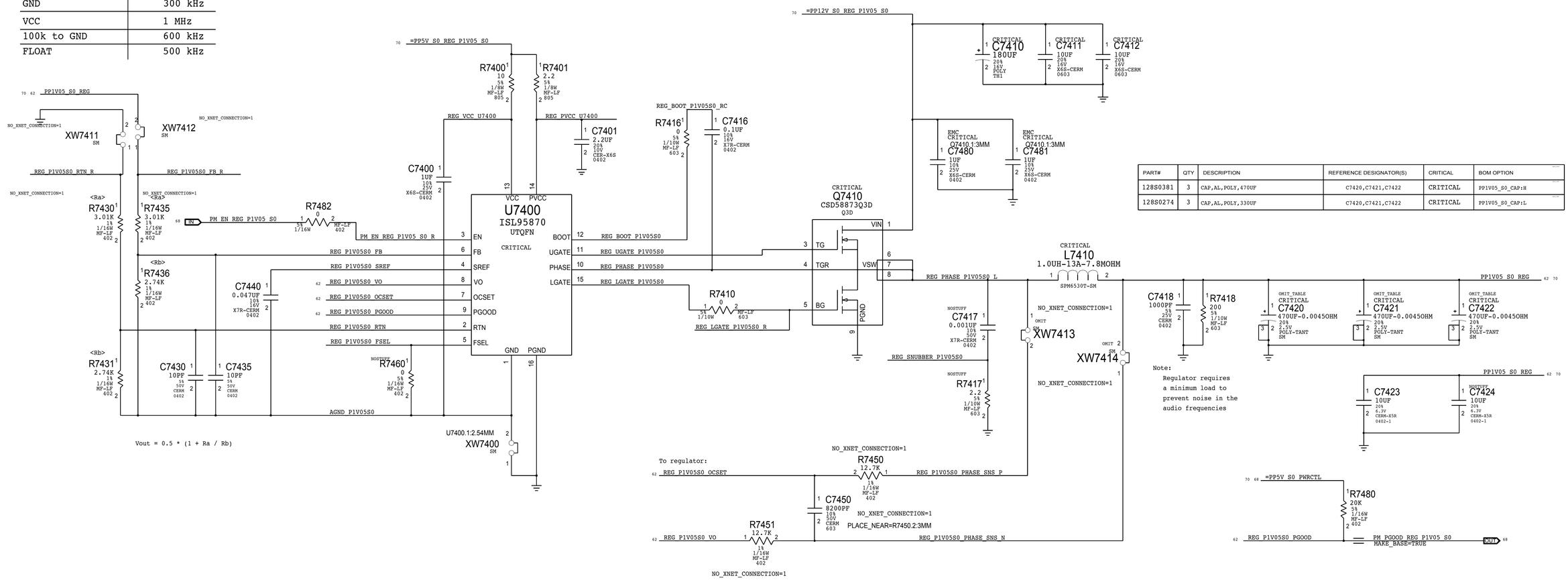
PCH (1.05V) S0 REGULATOR

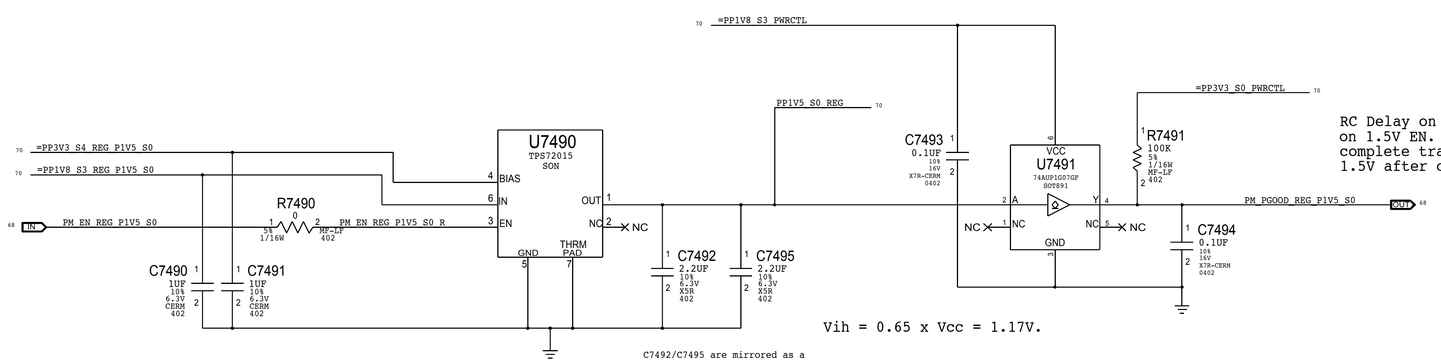
Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{\text{R7450} * 8.5\ \text{E-6}}{\text{DCR(L7410)}}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0381	3	CAP,AL,POLY,470UF	C7420,C7421,C7422	CRITICAL	PP1V05_S0_CAP:H
128S0274	3	CAP,AL,POLY,330UF	C7420,C7421,C7422	CRITICAL	PP1V05_S0_CAP:L

1.5V S0 REGULATOR



RC Delay on 1.5V PGOOD must be longer than delay on 1.5V EN. This allows for rail voltage to complete transition from Vih min (1.17V) to 1.5V after output shifts to OD.

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: PLATFORM POWER: VREG 1V05 S0 / 1V5 S0

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PAGE TITLE

PLATFORM POWER: VREG SSD 3V3/2V7

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3.3V S5 Regulator

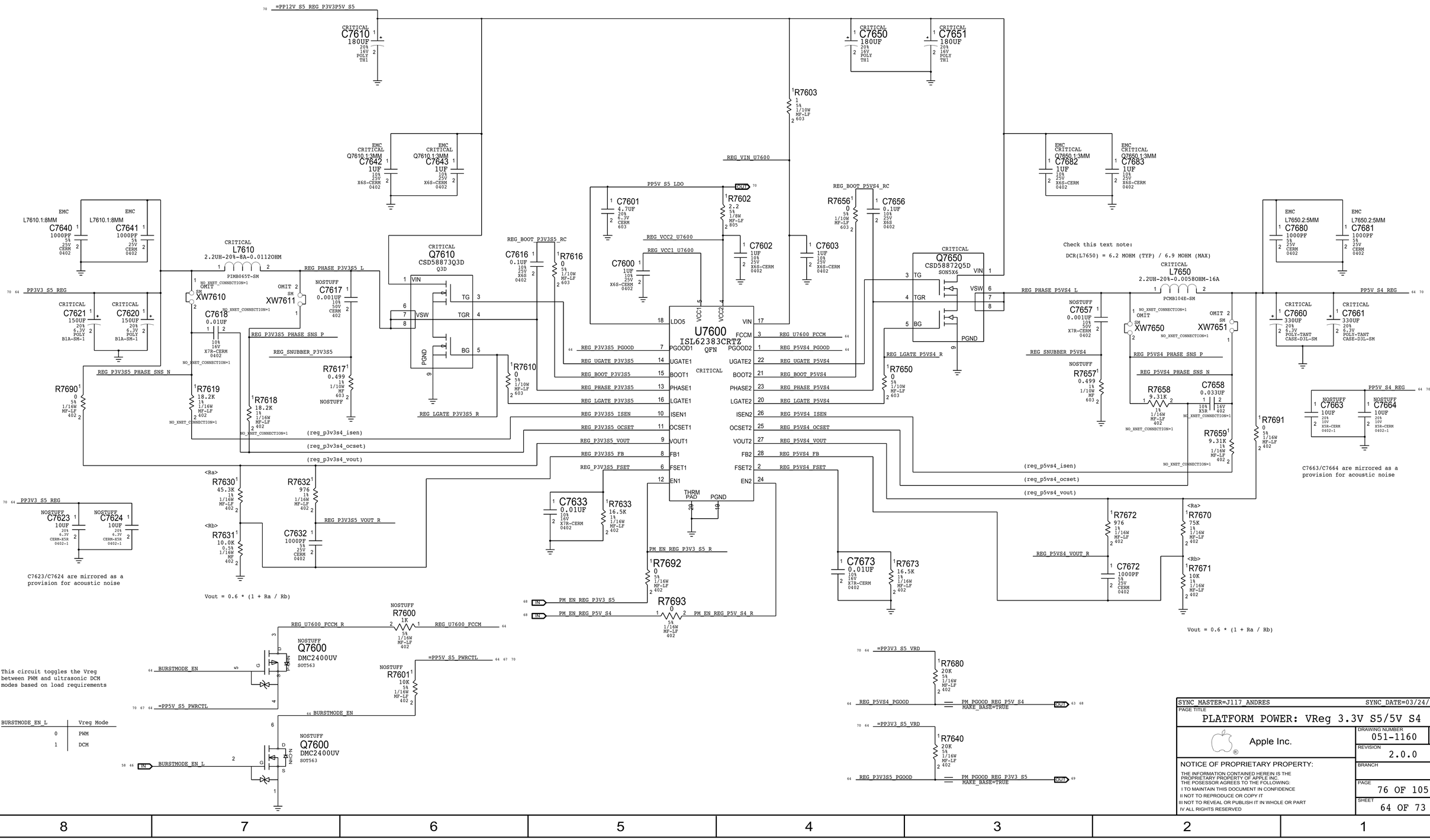
OC trip point: 12.5 A = R7618 * 10 E-6 / DCR(L7610)

Switching freq: 356 kHz = 1 / 170 E-12 * R7633

5V S4 Regulator

OC trip point: 14.1 A = R7658 * 10 E-6 / DCR(L7650)

Switching freq: 356 kHz = 1 / 170 E-12 * R7673



SYNC MASTER=J117 ANDRES SYNC DATE=03/24/2014

PAGE TITLE: PLATFORM POWER: VReg 3.3V S5/V S4

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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PAGE 76 OF 105

SHEET 64 OF 73

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OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program

PP12V_S0_BKLT_PWR
D8103 SOD-323 SBR130S3
C8140 1000PF 5% 25V CERM 0402
C8141 1000PF 5% 25V CERM 0402
C8102 CRITICAL 10UF 10% 25V X7R-CERM 1206-1
C8103 CRITICAL 10UF 10% 25V X7R-CERM 1206-1
C8114 CRITICAL 100UF 20% 35V ELEC 6.3X11-TH
PLACE C8114 NEAR HIGHER FREQUENCY CAPS

OMIT_TABLE L8100 33UH-20%-10A-0.0351OHM IHLP6767GZ-IHLP4040DZ11-SM
BKLT_PHASE
D8101 POWERDI5-TO277A PDS5100H
NOSTUFF R8123 4.7 5% 1/10W MF-LF 603
BKLT_SNUBBER
NOSTUFF C8113 100PF 5% 100V C0G-CERM 0603
BKLT_GATE_R
Q8120 IRF6643TRPBF DIRECTFET-MZ
BKLT_SNSN_R
R8119 0 5% 1/8W MF-LF 805
R8102 0.03 1% 2W MF 2512-LF
R8114 20 5% 1/8W MF-LF 805
R8113 887K 1% 1/16W MF-LF 402
R8112 330K 1% 1/8W MF 0402
XW8109 SHORT-1206
C8110 1000PF 10% 100V X7R-CERM 0603
R8104 887K 1% 1/16W MF-LF 402
R8103 330K 1% 1/8W MF 0402
C8111 1000PF 10% 100V X7R-CERM 0603

OMIT_TABLE C8119 100PF 5% 100V C0G-CERM 0603
C8106 2.2UF 10% 100V X7S-CERM 1206
C8108 2.2UF 10% 100V X7S-CERM 1206
C8109 CRITICAL 15UF 20% 100V ELEC TH-COMBO
C8118 CRITICAL 15UF 20% 100V ELEC TH-COMBO
C8120 100PF 5% 100V C0G-CERM 0603
BKLT_BOOST

BKLT_PHASE
Q8121 IRF6645PBF DIRECTFET-SJ
BKLT_GATE_R
BKLT_SNSP_R

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1078	138S0810		C8106, C8108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0648	371S0694		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8211 TO Q8216	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR
126-0312	126-0306		C8114	BLC INPUT CAP

PP3V3_S0_BKLT_VDDIO
PP5V_S0_BKLT_VDDD
PP5V_S0_BKLT_VDDA
OMIT_TABLE
PP12V_S0_BKLT_FILT

U8100 LP8565A13RWC WQFN

BKLT_SHUTDOWN	39	SD	
	40	UVLO_OVP	
=I2C_BKLT_SDA	9	SDA	
=I2C_BKLT_SCL	8	SCL	
DP_INTPNL_HPD_BUF_R	2	HPD	
TCON_BLC_EN	3	BL_EN	
BKLT_FAULT_INT_R_L	12	INT	
BLC_VSYNC_R	10	BRT_SYNC	
BKLT_PWM_IN	7	PWM	
BLC_LSYNC_R	11	SYNC	
BKLT_PLL_FILT	43	FILTER	
BKLT_ANG_TEST	32	ANALOG_TEST	
BKLT_DIG_TEST	1	DIGITAL_TEST	
PP12V_S0_BKLT_PWR_R	38	VING	
BKLT_GD_RAIL	37	BST_GD_RAIL	
BKLT_NC_TEST	13	NC	

BST_GD	36	BKLT_GATE	
BST_ISENSE_P	34	BKLT_SNSP	
BST_ISENSE_N	33	BKLT_SNSN	
BST_FB	31	BKLT_BST_FB	
BST_SHORT_FB	30	BKLT_BST_SHORT_FB	
LED1_HDR	14	BKLT_VSEN1	IN
LED1_GD	15	BKLT_GD1	OUT
LED1_R	16	BKLT_ISEN1_Q	IN
LED2_HDR	17	BKLT_VSEN2	IN
LED2_GD	18	BKLT_GD2	OUT
LED2_R	19	BKLT_ISEN2_Q	IN
LED3_HDR	20	BKLT_VSEN3	IN
LED3_GD	21	BKLT_GD3	OUT
LED3_R	22	BKLT_ISEN3_Q	IN
LED4_HDR	24	NC	
LED4_GD	25	NC	
LED4_R	26	NC	
LED5_HDR	29	NC	
LED5_GD	27	NC	
LED5_R	28	NC	
LED6_HDR	44	NC	
LED6_GD	45	NC	
LED6_R	46	NC	
LED7_HDR	47	BKLT_VSEN4	IN
LED7_GD	48	BKLT_GD4	OUT
LED7_R	49	BKLT_ISEN4_Q	IN
LED8_HDR	51	BKLT_VSEN5	IN
LED8_GD	52	BKLT_GD5	OUT
LED8_R	53	BKLT_ISEN5_Q	IN
LED9_HDR	54	BKLT_VSEN6	IN
LED9_GD	55	BKLT_GD6	OUT
LED9_R	56	BKLT_ISEN6_Q	IN

VDDIO	4	GNDA	41
VDDD	5	GNDD	6
VDDA	42	LED_GND1	23
		LED_GND2	50
		GND_BST_GD	35
		THRM PAD	57

BKLT_PLL_FILT
C8115 330PF 5% 50V C0G 402
R8111 270K 5% 1/16W MF-LF 402
D8102 SOD-323 BAT54XV2T1
C8116 4700PF 10% 50V X7R-CERM 0402
BKLT_PLL_FILT_R
BKLT_GNDA
X403:N R8100 0 5% 1/16W MF-LF 402

BKLT_GD_RAIL
C8145 0.1UF 10% 25V X6S 0402 NOSTUFF
C8117 0.1UF 10% 25V X6S 0402
BKLT_GND_BST_GD

R8125 0 5% 1/16W MF-LF 402
BKLT_SNSP
C8130 1000PF 10% 100V X7R 603 NOSTUFF NO_XNET_CONNECTION=1
BKLT_SNSN
R8191 0 5% 1/16W MF-LF 402
BKLT_SNSP_R
BKLT_SNSN_R

C8121 470PF 5% 100V CER-COG 0603
C8122 470PF 5% 100V CER-COG 0603
C8123 470PF 5% 100V CER-COG 0603
C8124 470PF 5% 100V CER-COG 0603
C8125 470PF 5% 100V CER-COG 0603
C8126 470PF 5% 100V CER-COG 0603
BKLT_BOOST
LED_RETURN_1_FB
LED_RETURN_2_FB
LED_RETURN_3_FB
LED_RETURN_4_FB
LED_RETURN_5_FB
LED_RETURN_6_FB

R8138 1 5% 1/16W MF-LF 402
PP12V_S0_BKLT_PWR
PP12V_S0_BKLT_PWR_R
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8142 1UF 10% 25V X7R 0603
C8143 0.01UF 10% 16V X7R-CERM 0402
C8144 0.1UF 10% 16V X7R-CERM 0402
BKLT_GND_BST_GD

XW8105 BKLT_GNDA
XW8106 BKLT_GNDD
XW8108 BKLT_GND_BST_GD

R8137 1 5% 1/16W MF-LF 402
=PP5V_S0_BKLT
PP5V_S0_BKLT_VDDA
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8137 22UF 20% 10V X5R-CERM 0603
C8138 0.01UF 10% 16V X7R-CERM 0402
C8139 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDA

R8131 1 5% 1/16W MF-LF 402
=PP5V_S0_BKLT
PP5V_S0_BKLT_VDDD
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8131 22UF 20% 10V X5R-CERM 0603
C8132 0.01UF 10% 16V X7R-CERM 0402
C8133 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDD

R8134 1 5% 1/16W MF-LF 402
=PP3V3_S0_BKLT
PP3V3_S0_BKLT_VDDIO
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0850
C8134 1UF 10% 25V X7R 0603
C8135 0.01UF 10% 16V X7R-CERM 0402
C8136 0.1UF 10% 16V X7R-CERM 0402
BKLT_GNDD

=PP3V3_S0_BKLT
R8124 4.7K 5% MF 1/20W 201
R8172 0 5% 1/16W MF-LF 402
BKLT_FAULT_INT_R_L
BKLT_FAULT_INT_L

R8106 200K 1% MF 1/20W 201 DP_INTPNL_HPD_BUF_R
R8105 100K 5% MF 1/20W 201 TCON_BLC_EN
R8107 10K 5% MF 1/20W 201 BKLT_PWM_IN
R8121 10K 5% MF 1/20W 201 NOSTUFF BLC_VSYNC_R
R8120 10K 5% MF 1/20W 201 NOSTUFF BLC_LSYNC_R
BKLT_GNDD

X403:Y
R8173 0 5% MF-LF 1/16W 402 DP_INTPNL_HPD_BUF
R8170 0 5% MF-LF 1/16W 402 BLC_VSYNC
R8171 0 5% MF-LF 1/16W 402 BLC_LSYNC

R8180 10K 5% MF 1/20W 201 BKLT_ANG_TEST
R8181 10K 5% MF 1/20W 201 BKLT_DIG_TEST
R8182 10K 5% MF 1/20W 201 BKLT_NC_TEST
BKLT_GNDA

=PP12V_S0_BKLT
F8100 6AMP-32V 0603-1
PP12V_BKLT_SNS
R8132 CRITICAL 0.005 1% 1/4W MF 1206-1
PP12V_BKLT_FUSED
FB8108 CRITICAL 160-OHM-6A 1206
PP12V_S0_BKLT_FILT

Q8119 FDMS6681Z POWER56
PP12V_S0_BKLT_PWR
C8171 NOSTUFF 0.1UF 10% 25V X6S 0402
R8101 NOSTUFF 330K 1% 1/8W MF 0402
C8101 0.01UF 10% 16V X7R-CERM 0402
BKLT_EN_DIV

Q8101 SSM3K15AMFVAP SOD NOSTUFF
BKLT_EN_L
R8133 NOSTUFF 147K 1% 1/16W MF-LF 402
R8122 0 5% 1/16W MF-LF 402
TCON_BLC_EN
BKLT_SHUTDOWN

SYNC_MASTER=MLB_CTO
SYNC_DATE=05/14/2014
PAGE TITLE
DISPLAY: LCD Backlight Driver 1
Apple Inc.
DRAWING NUMBER 051-1160
SIZE D
REVISION 2.0.0
BRANCH
PAGE 81 OF 105
SHEET 65 OF 73

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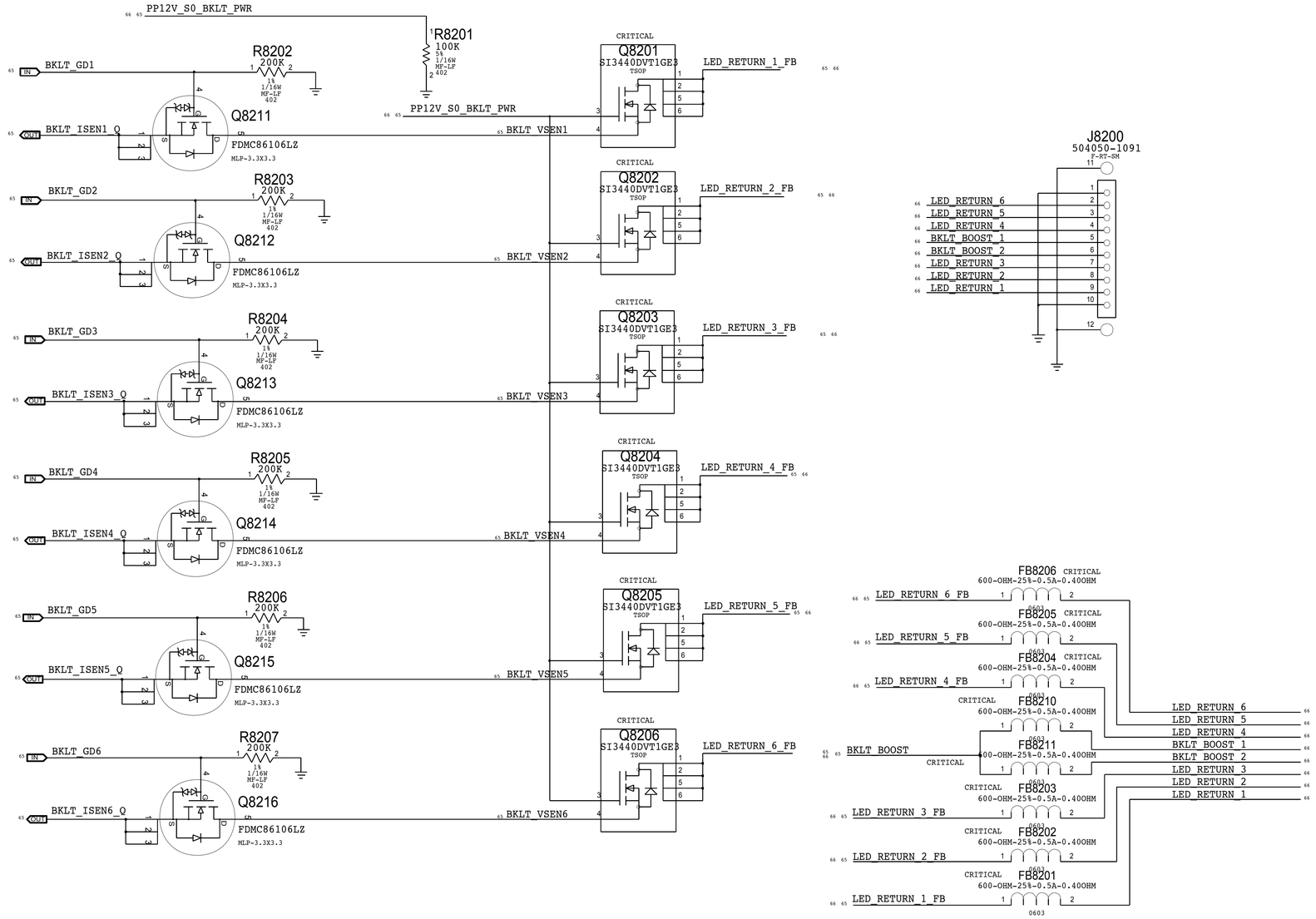
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	
126-0190	2	BOOST POLYMER OUTPUT CAP	C8109, C8118	CRITICAL	
353S00341	1	IC,PB565A110,LED BCKLGHT CTRL,TKT QFN56	U8100	CRITICAL	X403:Y
353S00336	1	IC,PB565A108,LED BCKLGHT CTRL,TKT QFN56	U8100	CRITICAL	X403:N

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



SYNC_MASTER=MLB_CTO SYNC_DATE=05/14/2014

PAGE TITLE

DISPLAY: LCD Backlight Driver 2

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

REVISION 2.0.0

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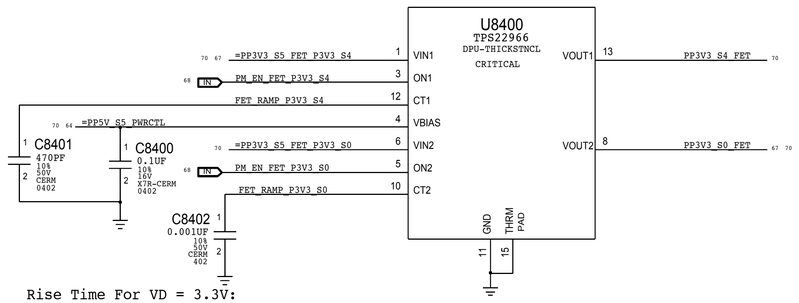
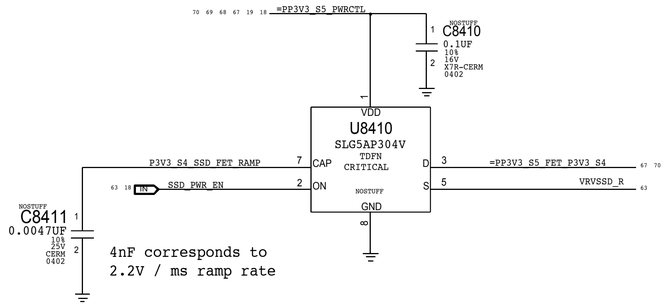
3.3V S4/S0 FET

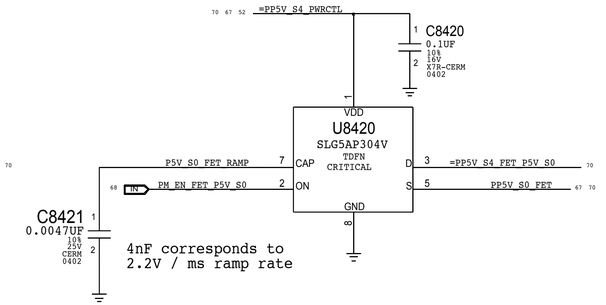


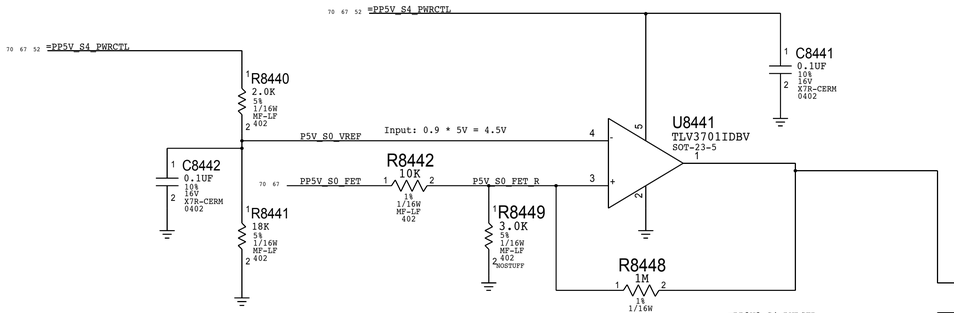
Rise Time For VD = 3.3V:
470 pF -- 603 us
1000 pF -- 1185 us

3V3 S4 SSD

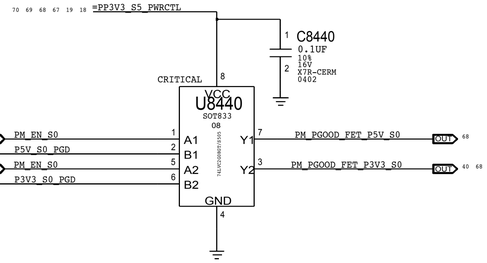


5V S0 FET

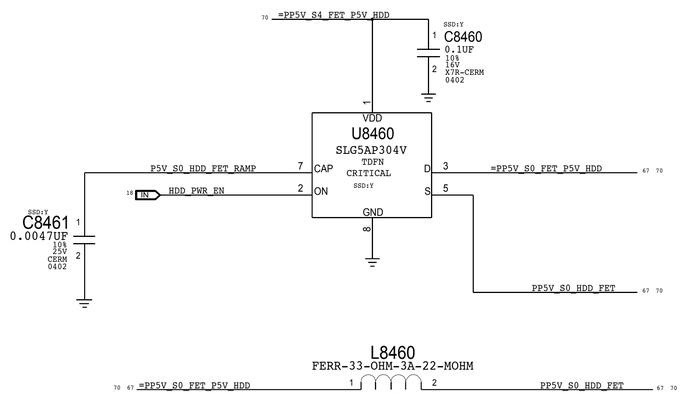




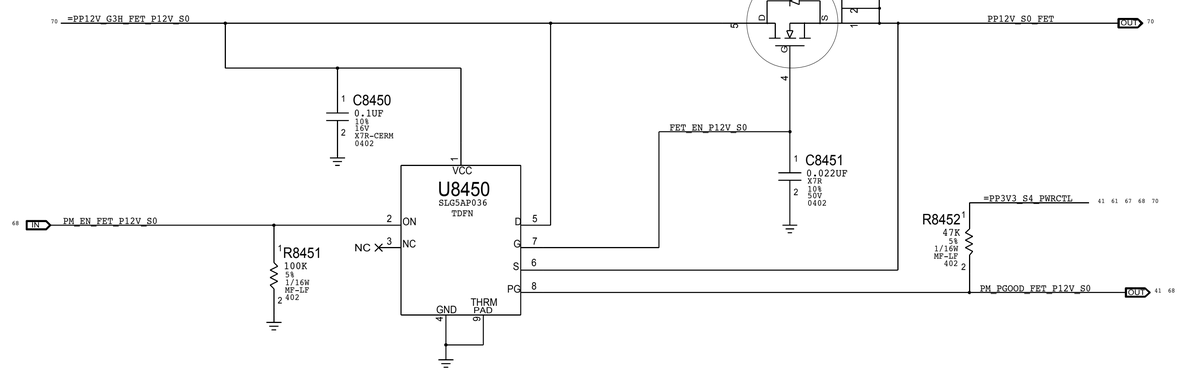
5V / 3V3 S0 PGOODs



5V HDD FET



12V S0 FET



SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE: PLATFORM POWER: PM FETs/LDOs	
Apple Inc.	DRAWING NUMBER 051-1160 · SIZE D
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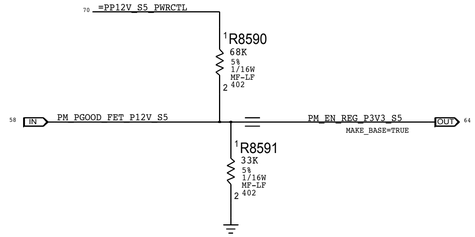
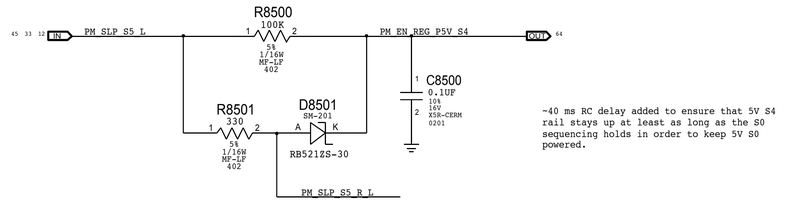
S5 Enable

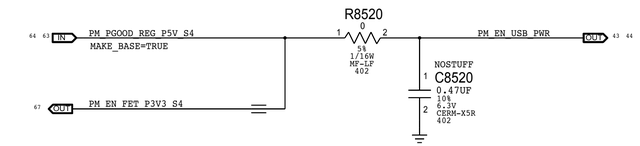


S4 Enables

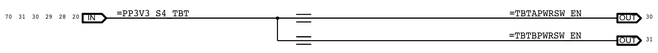


~40 ms RC delay added to ensure that 5V S4 rail stays up at least as long as the S0 sequencing holds in order to keep 5V S0 powered.

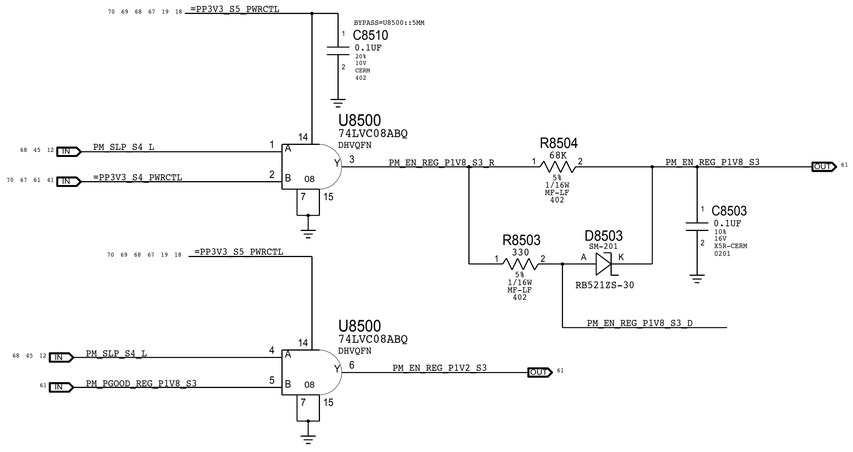
S4 USB Enable



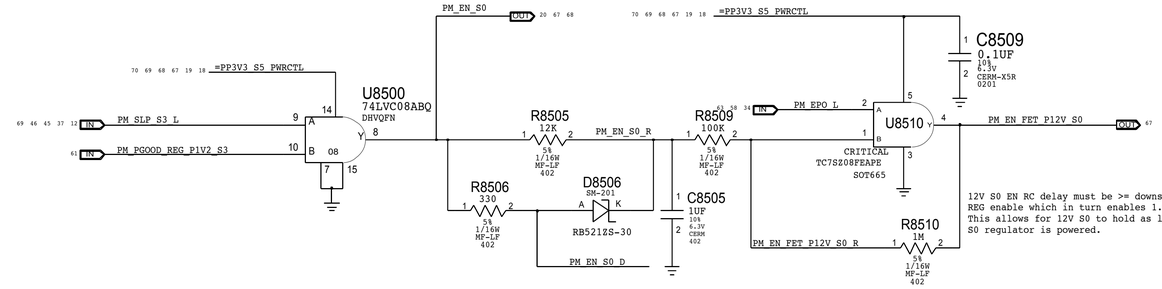
S4 TBT Port Enable



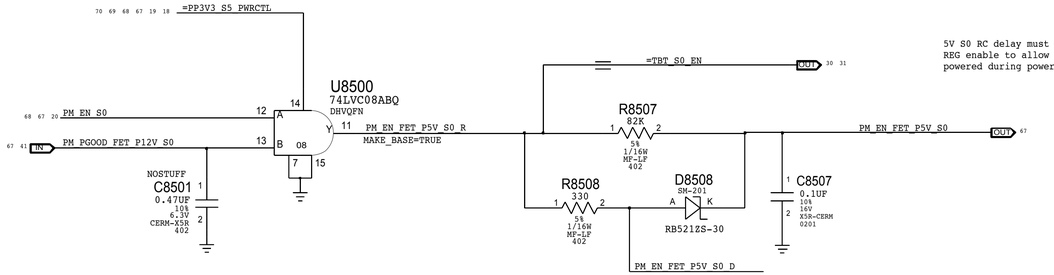
S3 Enables



S0 Enables

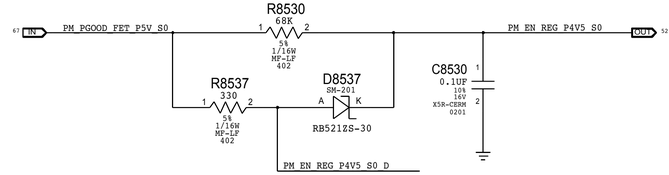


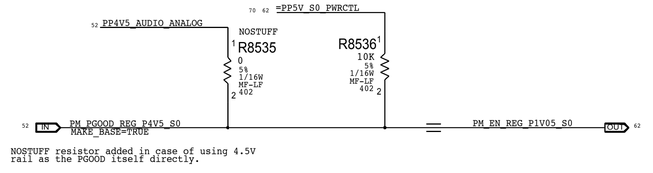
12V S0 EN RC delay must be >= downstream delay on 4.5V REG enable which in turn enables 1.05V S0. This allows for 12V S0 to hold as long as 1.05V S0 regulator is powered.



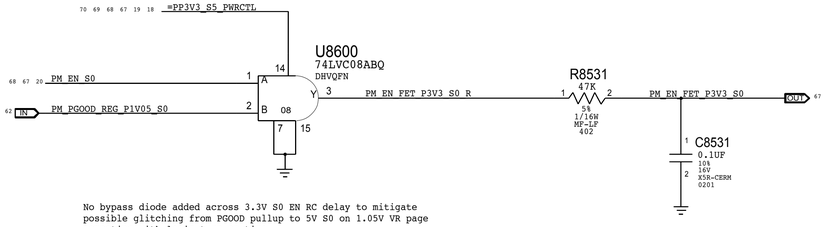
5V S0 RC delay must be >= downstream delay on 4.5V REG enable to allow for 4.5V regulator to remain powered during power down sequence.

Audio + PCH Sequencing Requirements:
4.5V -> 1.05V -> 3.3V -> 1.5V -> ALL SYS GOOD

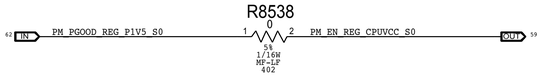


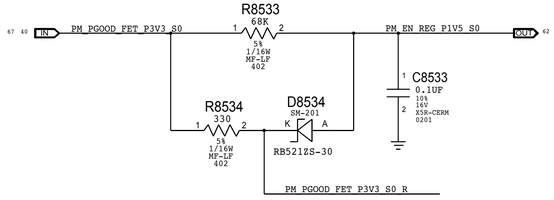


NOSTUFF resistor added in case of using 4.5V rail as the PGOOD itself directly.



No bypass diode added across 3.3V S0 EN RC delay to mitigate possible glitching from PGOOD pullup to 5V S0 on 1.05V VR page competing with logic turn on time.





SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

PLATFORM POWER: PM Regulator Enables

Apple Inc.

DRAWING NUMBER 051-1160 SIZE D

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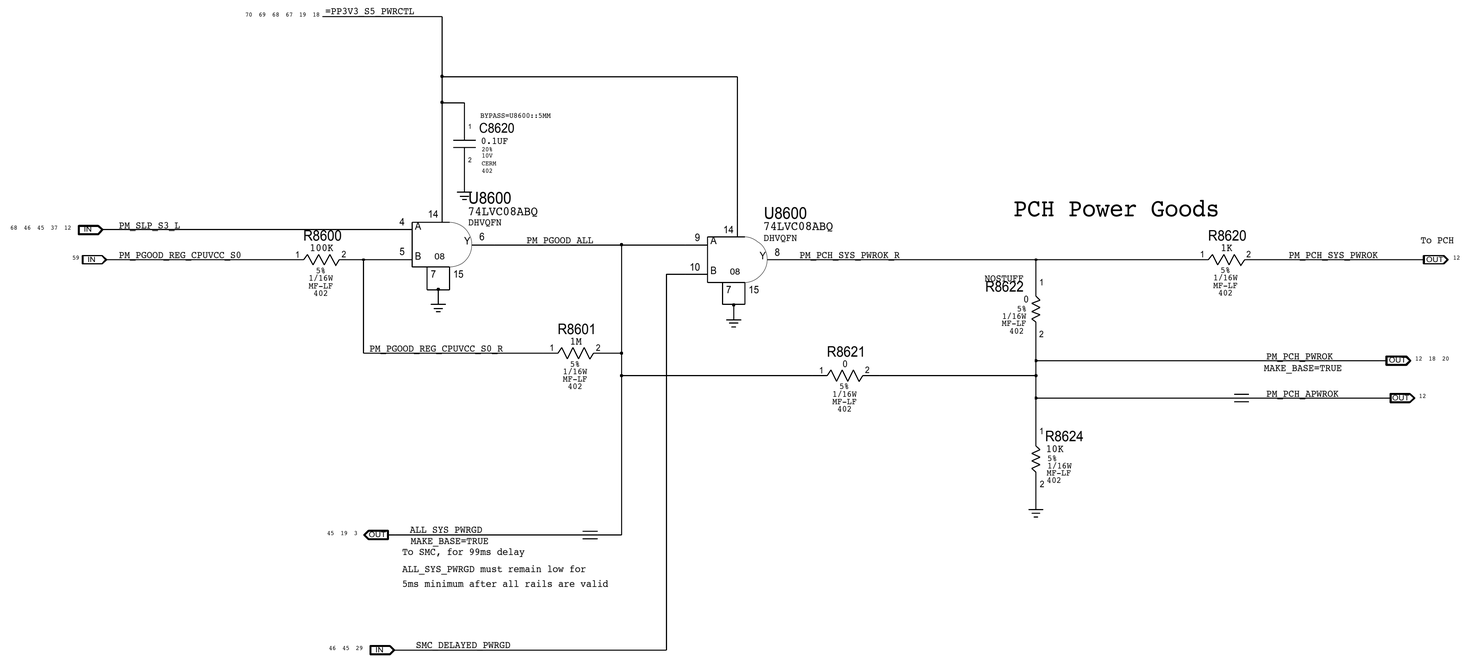
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation



PCH Power Goods

Resume Reset

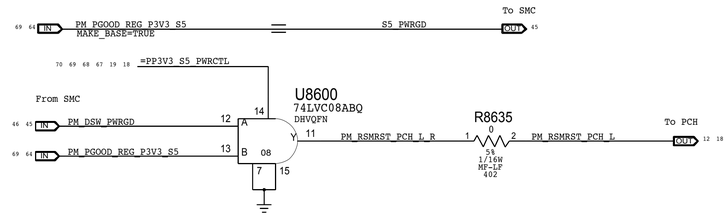
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J70 design does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



Rail definitions

Platform: All processor non-Core and non-Graphics (5V, 3.3V, 1.5V, 1.05V for PCH/TBT/GPU)
Uncore: 1.8V and 1.2V for DDR3

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

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PLATFORM POWER: PM Power Good

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G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC — 19
- =PPVRTC_G3_PCH — 11 12 15

G3H Rails

PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC — 58
- =PP12V_G3H_SNS_R — 49

PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS — 49
- =PP12V_G3H_REG_3V42_G3H — 58
- =PP12V_G3H_FET_P12V_S5 — 58
- =PP12V_G3H_FET_P12V_S0 — 67
- =PP12V_G3H_SSD — 63

PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG — 58
- =PP3V3_G3H_BT — 33
- =PP3V3_G3H_SMC — 45 46 51
- =PP3V3_G3H_RTC_D — 19
- =PPVIN_G3H_SMCVREF — 46
- =PP3V3_G3H_SMC_USBMUX — 43
- =PP3V3_G3H_T112 — 47
- =PP3V3_G3H_PWRCTL — 58

Ground/Common

GND\G (MAKE_BASE=TRUE)

S5 Rails

Enabled when system has AC and is in S5

PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET — 58
- =PP12V_S5_REG_P3V3P5V_S5 — 64
- =PP12V_S5_REG_P1V2_S3 — 61
- =PPHV_SW_TBTAPWRSW — 30
- =PPHV_SW_TBTBPWRSW — 31
- =PP12V_S5_SNS — 49
- =PP12V_S5_PWRCTL — 68

PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO — 64
- =PP5V_S5_PWRCTL — 64 67

PP3V3_S5_SRC (MAKE_BASE=TRUE)
- PP3V3_S5_REG — 64
- =PP3V3_S5_SNS_R — 49

PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_SNS — 49
- =PP3V3_S5_FET_P3V3_S4 — 67
- =PP3V3_S5_FET_P3V3_S0 — 67
- =PP3V3_S5_PWRCTL — 18 19 67 68 69
- =PP3V3_S5_VRD — 64
- =PP3V3_S5_LED — 3
- =PP3V3_SUS_PCH_VCCSUS_GPIO — 15 17
- =PP3V3_S5_PCH_VCCDSW — 15 17
- =PP3V3_SUS_PCH_VCC_SPI — 13 15 17
- =PP3V3_SUS_PCH_VCCSUS_RTC — 15 17
- =PP3V3_SUS_PCH_VCCSUS_USB — 15 17
- =PP3V3_SUS_PCH_VCCSUS_USB3 — 15
- =PP3V3_S5_PCH — 20
- =PP3V3_S5_ROM — 47
- =PP3V3_S5_SENSE — 49
- =PP3V3_S5_SMC — 46
- =PP3V3_S4_TBTAPWRSW — 30
- =PP3V3_S4_TBTBPWRSW — 31
- =PP3V3_SUS_PCH_GPIO — 11 12 13 14
- =PP3V3_S5_PCH_GPIO — 12 52
- =PP3V3_S5_REG_P1V8_S3 — 61
- =PP3V3_S5_XDP — 18
- =PP3V3_S5_SSDCTL — 63

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4_SRC (MAKE_BASE=TRUE)
- PP5V_S4_REG — 64
- =PP5V_S4_SNS_R — 49

PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_SNS — 49
- =PP5V_S4_REG_P1V2_S3 — 61
- =PP5V_S4_FET_P5V_S0 — 67
- =PP5V_S4_PWRCTL — 52 67
- =PP5V_S4_USB — 43 44
- =PP5V_S4_AUDIO — 52
- =PP5V_S4_FET_P5V_HDD — 67
- =PP5V_S4_SSD — 63

PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET — 67
- =PP3V3_S4_FET_ENET — 37
- =PP3V3_S4_PWRCTL — 41 61 67 68
- =PP3V3_S4_LED — 3
- =PP3V3_S4_PCH_GPIO — 13 20 43 44
- =PP3V3_S4_SDCARD — 38
- =PP3V3_S4_SMC — 46
- =PP3V3_S4_TBT — 20 28 29 30 31 68
- =PP3V3_S4_AP — 33 46
- =PP3V3_S4_REG_P1V5_S0 — 62
- =PP3V3_S4_SYSCLK — 19

S3 Rails

Enabled when system is in run or sleep

PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET — 37
- =PP3V3_ENET_PHY — 36 37
- =PPVDDIO_ENET_CLK — 19

PP1V8_S3 (MAKE_BASE=TRUE)
- PP1V8_S3_REG — 61
- =PP1V8_S3_DDR — 23 24 25 26
- =PP1V8_S3_CAMERA_FET — 40
- =PP1V8_S3_PWRCTL — 62
- =PP1V8_S3_REG_P1V5_S0 — 62

PP1V2_S3 (MAKE_BASE=TRUE)
- PP1V2_S3_REG — 61
- =PP1V2_S3_SNS_DDR_R — 49

PP1V2_S3_DDR (MAKE_BASE=TRUE)
- PP1V2_S3_SNS_DDR — 49
- =PP1V2_S3_LDO_DDRVTT — 61
- =PP1V2_S3_DDR_MEMVREF — 22
- =PP1V2_S3_DDR_VDD2 — 23 24 25 26
- =PP1V2_S3_DDR_VDDCA — 23 24 25 26
- =PP1V2_S3_DDR_VDDQ — 23 24 25 26
- =PPVMEMIO_S0_CPU — 6 8 10
- =PP1V2_S3_CAMERA_FET — 40

PP0V6_S3_DDRVTT (MAKE_BASE=TRUE)
- PP0V6_S3_DDRVTT_LDO — 61
- =PP0V6_S3_DDRVTT_A — 27
- =PP0V6_S3_DDRVTT_B — 27

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET — 67
- =PP12V_S0_REG_CPUVCC_S0 — 60
- =PP12V_S0_REG_P1V05_S0 — 62
- =PP12V_S0_AUDIO_SPKRAMP — 54 55
- =PP12V_S0_BKLT — 65
- =PP12V_S0_FAN — 51
- =PP12V_S0_LCD — 41

PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET — 67
- =PP5V_S0_REG_CPUVCC_S0 — 59 60
- =PP5V_S0_REG_P1V05_S0 — 62
- =PP5V_S0_BKLT — 65
- =PP5V_S0_FET_P5V_HDD — 67
- =PP5V_S0_CAMERA — 39 40
- =PP5V_S0_PWRCTL — 62 68
- =PP5V_S0_PCH_STRAP — 19

PP5V_S0_HDD (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET — 67
- =PP5V_S0_SATA — 35

PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET — 67
- =PP3V3_S0_VRD — 58 59
- =PP3V3_S0_AUDIO — 39 52
- =PP3V3_S0_AUDIO_DIG — 53 56
- =PP3V3_S0_AUDIO_SPKRAMP — 54 55
- =PP3V3_S0_DP — 32
- =PP3V3_S0_ENET — 36
- =PP3V3_S0_FAN — 51
- =PP3V3_S0_INTDPMUX — 20 42
- =PP3V3_S0_LED — 3
- =PP3V3_S0_PCH — 13 19
- =PP3V3_S0_PCH_VCC3_3_GPIO — 15 17
- =PP3V3_S0_SDCARD — 38
- =PP3V3_S0_SENSE — 35 49 50
- =PP3V3_S0_SMBUS — 48
- =PP3V3_S0_SMBUS_SMC_0 — 48
- =PP3V3_S0_SMBUS_SMC_1 — 48
- =PP3V3_S0_SMBUS_SMC_2 — 48
- =PP3V3_S0_SMBUS_SMC_3 — 48
- =PP3V3_S0_SMC — 46
- =PP3V3_S0_BKLT — 65
- =PP3V3_S0_PCH_GPIO — 11 12 14 20 29
- =PP3V3_S0_CAMERA — 39 40
- =PP3V3_S0_ALS — 39
- =PP3V3_S0_PWRCTL — 62
- =PP3V3_S0_PCH_VCC3_3_THRM — 15 17
- =PP3V3_S0_PCH_VCCCLK3_3 — 15 17
- =PP3V3_S0_PCH_VCC3_3_HVCMOS — 15 17 70
- =PP3V3_S0_PCH_VCC_FUSE — 15 17
- =PP3V3_S0_PCH_VCC3_3_USB — 15 17
- =PP3V3_S0_PCH_VCC3_3_HVCMOS — 15 17 70
- =PP3V3_S0_RSTBUF — 20

PP1V5_S0 (MAKE_BASE=TRUE)
- PP1V5_S0_REG — 62
- =PP1V5_S0_SENSE — 35
- =PP1V5_S0_PCH_VCCVRM — 17
- =PP1V5_S0_AUDIO_DIG — 53
- =PP1V5_S0_PCH_RCOMP — 12 13
- =PP1V5_S0_PCH_SATA — 11
- =PP1V5_S0_PCH_CLK — 11 19
- =PP1V5_S0_PCH_GPIO — 11
- =PP3V3R1V5_S0_PCH_VCCSUSHDA — 15 17 19

PP1V05_S0 (MAKE_BASE=TRUE)
- PP1V05_S0_REG — 62
- =PP1V05_S0_PCH_VCC — 15 17
- =PP1V05_S0_PCH_VCCASW — 15 17
- =PP1V05_S0_PCH_VCCCLK — 17
- =PP1V05_S0_PCH_VCCIO_USB2 — 15 17
- =PP1V05_S0_PCH_VCCIO — 15 17
- =PP1V05_S0_PCH_VCCIO_FDI — 15 17
- =PP1V05_S0_PCH_VCCUSBPLL — 15 17
- =PP1V05_S0_SMC — 46
- =PP1V05_S0_XDP — 18
- =PP1V05_S0_PCH_VCCCLK_CLK100 — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK135 — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC100 — 15 17
- =PP1V05_S0_PCH_VCCIO_GPIO — 15
- =PP1V05_S0_PCH_V_PROC_IO — 14 15 17
- =PP1V05_S0_CPU_VCCST — 8 10 19

PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)
- PPCPUVCC_S0_REG — 60
- =PPCPUVCC_S0_CPU — 49 59
- =PPVCC_S0_CPU — 6 8 10

PPVSSD_S4 (MAKE_BASE=TRUE)
- PPVSSD_S4_REG — 63
- =PPVSSD_S4_CONN — 34

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Power Aliases

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Display Aliases

20	DP_TBTSNK0_HPD_BUF MAKE_BASE=TRUE	=	DP_IG_B_HPD	12
28	DP_TBTSNK0_ML_C_P<3..0> MAKE_BASE=TRUE	=	DP_IG_B_MLP<3..0>	5
28	DP_TBTSNK0_ML_C_N<3..0> MAKE_BASE=TRUE	=	DP_IG_B_MLN<3..0>	5
28	DP_TBTSNK0_AUXCH_C_P MAKE_BASE=TRUE	=	DP_IG_B_AUXCHP	12
28	DP_TBTSNK0_AUXCH_C_N MAKE_BASE=TRUE	=	DP_IG_B_AUXCHN	12
32	DP_TBTSNK0_DDC_DATA MAKE_BASE=TRUE	=	DP_IG_B_DDC_DATA	12
32	DP_TBTSNK0_DDC_CLK MAKE_BASE=TRUE	=	DP_IG_B_DDC_CLK	12
20	DP_TBTSNK1_HPD_BUF MAKE_BASE=TRUE	=	DP_IG_C_HPD	12
28	DP_TBTSNK1_ML_C_P<3..0> MAKE_BASE=TRUE	=	DP_IG_C_MLP<3..0>	5
28	DP_TBTSNK1_ML_C_N<3..0> MAKE_BASE=TRUE	=	DP_IG_C_MLN<3..0>	5
28	DP_TBTSNK1_AUXCH_C_P MAKE_BASE=TRUE	=	DP_IG_C_AUXCHP	12
28	DP_TBTSNK1_AUXCH_C_N MAKE_BASE=TRUE	=	DP_IG_C_AUXCHN	12
32	DP_TBTSNK1_DDC_DATA MAKE_BASE=TRUE	=	DP_IG_C_DDC_DATA	12
32	DP_TBTSNK1_DDC_CLK MAKE_BASE=TRUE	=	DP_IG_C_DDC_CLK	12
42	DP_INT_HPD MAKE_BASE=TRUE	=	DP_IG_D_HPD	12
42	DP_INT_ML_P<3..0> MAKE_BASE=TRUE	=	DP_IG_D_MLP<3..0>	5
42	DP_INT_ML_N<3..0> MAKE_BASE=TRUE	=	DP_IG_D_MLN<3..0>	5
	TP_DP_INT_DDC_DATA MAKE_BASE=TRUE	=	DP_IG_D_DDC_DATA	12
	TP_DP_INT_DDC_CLK MAKE_BASE=TRUE	=	DP_IG_D_DDC_CLK	12
42	DP_INT_AUX_P MAKE_BASE=TRUE	=	DP_IG_D_AUXCHP	12
42	DP_INT_AUX_N MAKE_BASE=TRUE	=	DP_IG_D_AUXCHN	12

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Signal Aliases

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CPU Reserved

18 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12> 59 60
MAKE_BASE=TRUE

PCH GPIO

11 PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
MAKE_BASE=TRUE NO_TEST=1

11 PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
MAKE_BASE=TRUE NO_TEST=1

11 PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
MAKE_BASE=TRUE NO_TEST=1

11 PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3
MAKE_BASE=TRUE NO_TEST=1

Unused IG Display

5 DP_IG_A_MLP<3..0> — NC_DP_IG_A_MLP<3..0>
MAKE_BASE=TRUE NO_TEST=1

5 DP_IG_A_MLN<3..0> — NC_DP_IG_A_MLN<3..0>
MAKE_BASE=TRUE NO_TEST=1

5 DP_IG_A_AUXCHP — NC_DP_IG_A_AUXCHP
MAKE_BASE=TRUE NO_TEST=1

5 DP_IG_A_AUXCHN — NC_DP_IG_A_AUXCHN
MAKE_BASE=TRUE NO_TEST=1

PCH PCI

13 LPC_DREQ0_L — NC_LPC_DREQ0_L
MAKE_BASE=TRUE NO_TEST=1

PCH Miscellaneous

11 HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=1

11 HDA_SDIN2 — NC_HDA_SDIN2
MAKE_BASE=TRUE NO_TEST=1

11 HDA_SDIN3 — NC_HDA_SDIN3
MAKE_BASE=TRUE NO_TEST=1

Unused Thunderbolt Aliases

28 TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L
MAKE_BASE=TRUE NO_TEST=1

Unused VREG Aliases

59 REG_PWM_CPUVCC_4 — NC_REG_PWM_CPUVCC_4
MAKE_BASE=TRUE NO_TEST=1

59 REG_ISENVCC_4_P — NC_REG_ISENVCC_4P
MAKE_BASE=TRUE NO_TEST=1

59 REG_ISENVCC_4_R_N — AGND_CPU 59 60
MAKE_BASE=TRUE

SSD Signals Through PEG

5 =PEG_D2R_P<3..0> — PCIE_SSD_D2R_P<3..0> 34
MAKE_BASE=TRUE

5 =PEG_D2R_N<3..0> — PCIE_SSD_D2R_N<3..0> 34
MAKE_BASE=TRUE

5 =PEG_R2D_C_P<3..0> — PCIE_SSD_R2D_P<3..0> 34
MAKE_BASE=TRUE

5 =PEG_R2D_C_N<3..0> — PCIE_SSD_R2D_N<3..0> 34
MAKE_BASE=TRUE

Thunderbolt Signals Through PEG

5 =PEG_D2R_P<11..8> — PCIE_TBT_D2R_P<3..0> 28
MAKE_BASE=TRUE

5 =PEG_D2R_N<11..8> — PCIE_TBT_D2R_N<3..0> 28
MAKE_BASE=TRUE

5 =PEG_R2D_C_P<11..8> — PCIE_TBT_R2D_C_P<3..0> 28
MAKE_BASE=TRUE

5 =PEG_R2D_C_N<11..8> — PCIE_TBT_R2D_C_N<3..0> 28
MAKE_BASE=TRUE

Unused PEG Lanes

5 =PEG_D2R_P<7> — NC_PEG_D2R_P_7
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<6> — NC_PEG_D2R_P_6
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<5> — NC_PEG_D2R_P_5
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<4> — NC_PEG_D2R_P_4
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<7> — NC_PEG_D2R_N_7
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<6> — NC_PEG_D2R_N_6
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<5> — NC_PEG_R2D_N_5
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<4> — NC_PEG_R2D_N_4
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<15> — NC_PEG_D2R_P_15
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<14> — NC_PEG_D2R_P_14
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<13> — NC_PEG_R2D_P_13
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_P<12> — NC_PEG_R2D_P_12
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<15> — NC_PEG_D2R_N_15
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<14> — NC_PEG_D2R_N_14
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<13> — NC_PEG_R2D_N_13
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_D2R_N<12> — NC_PEG_R2D_N_12
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<7> — NC_PEG_R2D_C_P_7
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<6> — NC_PEG_R2D_C_P_6
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<5> — NC_PEG_R2D_C_P_5
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<4> — NC_PEG_R2D_C_P_4
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<7> — NC_PEG_R2D_C_N_7
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<6> — NC_PEG_R2D_C_N_6
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<5> — NC_PEG_R2D_C_N_5
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<4> — NC_PEG_R2D_C_N_4
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<15> — NC_PEG_R2D_C_P_15
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<14> — NC_PEG_R2D_C_P_14
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<13> — NC_PEG_R2D_C_P_13
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_P<12> — NC_PEG_R2D_C_P_12
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<15> — NC_PEG_R2D_C_N_15
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<14> — NC_PEG_R2D_C_N_14
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<13> — NC_PEG_R2D_C_N_13
MAKE_BASE=TRUE NO_TEST=1

5 =PEG_R2D_C_N<12> — NC_PEG_R2D_C_N_12
MAKE_BASE=TRUE NO_TEST=1

SYNC_MASTER=J94_ANDRES SYNC_DATE=07/09/2014

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Unused Signal Aliases

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