MS-7869 Version : 1.0

CPU :

Intel Haswell Processor

System Chipset :

Intel Lynx Point Chipset

On Board Chipset :

VRM 12.5 --ISL95816HRZ 3 Phase
Gigabit LAN-RTL8111GA
HDA Codec -- Realtek ALC662-VD
Super I/O -- NCT5537D
SPI Flash 64Mb

Main Memory :

2 Channel DDR III * 2 (Max 8GB)

Expansion Slot :

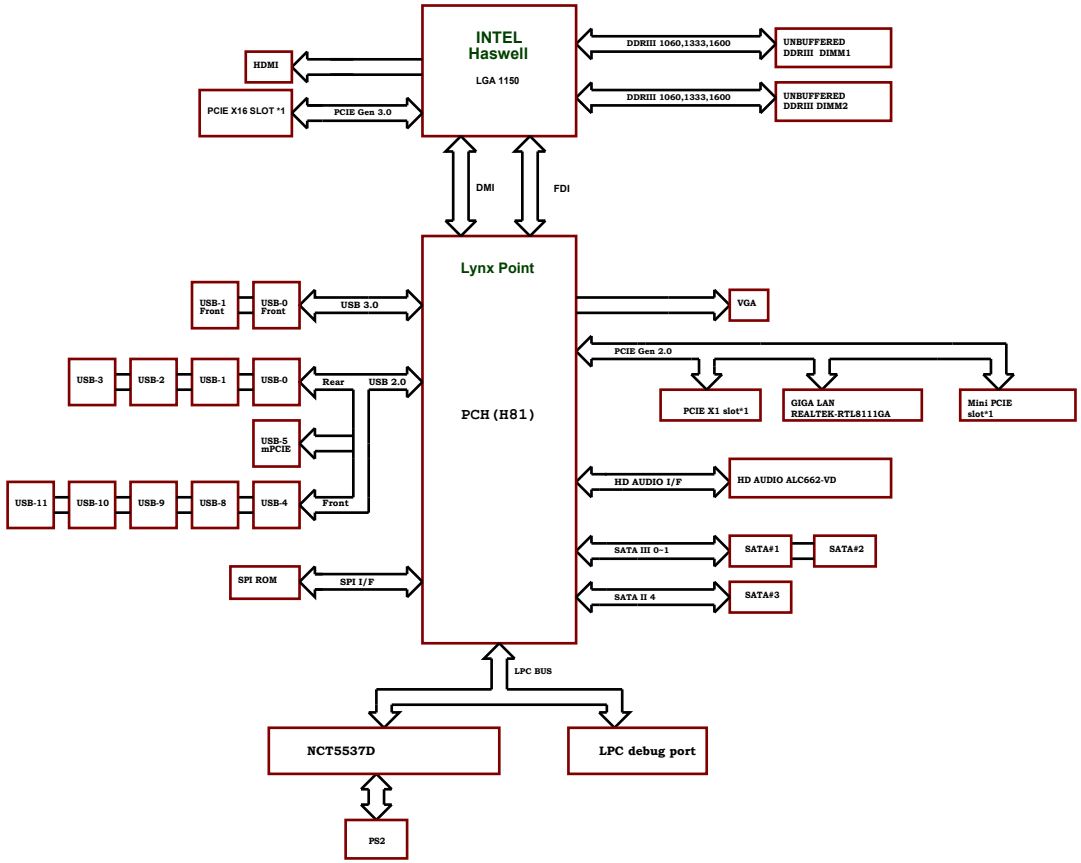
PCI Express x16 Slot * 1
PCI Express x1 Slot * 1
Mini PCIE Slot * 1

MSI MICRO-START INT'L CO.,LTD

Title: Cover Sheet

Size: | Document Number: Acer SharkBay | Rev: 1.0

Date: | Sheet 1 of 35

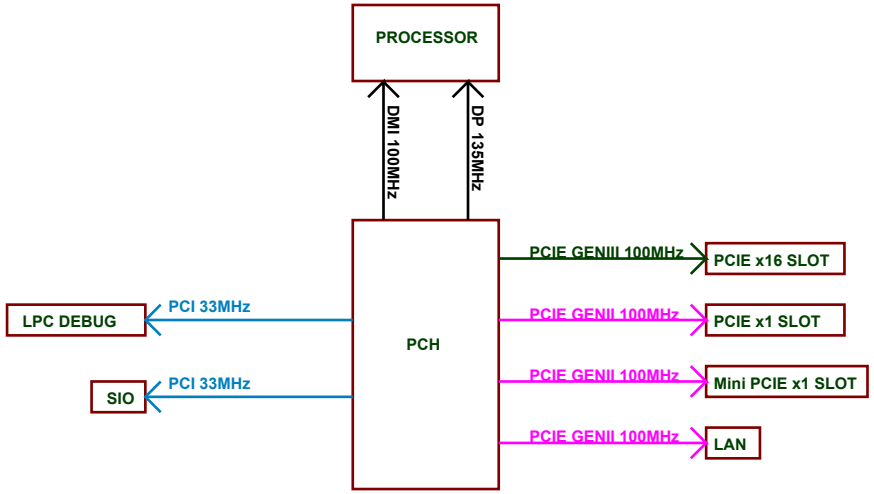


MSI
MICRO-START INT'L CO.,LTD

Title: Block Diagram

Size	Document Number	Rev
	Acer SharkBay	1.0

Date: Thursday, July 11, 2013 Sheet 2 of 34

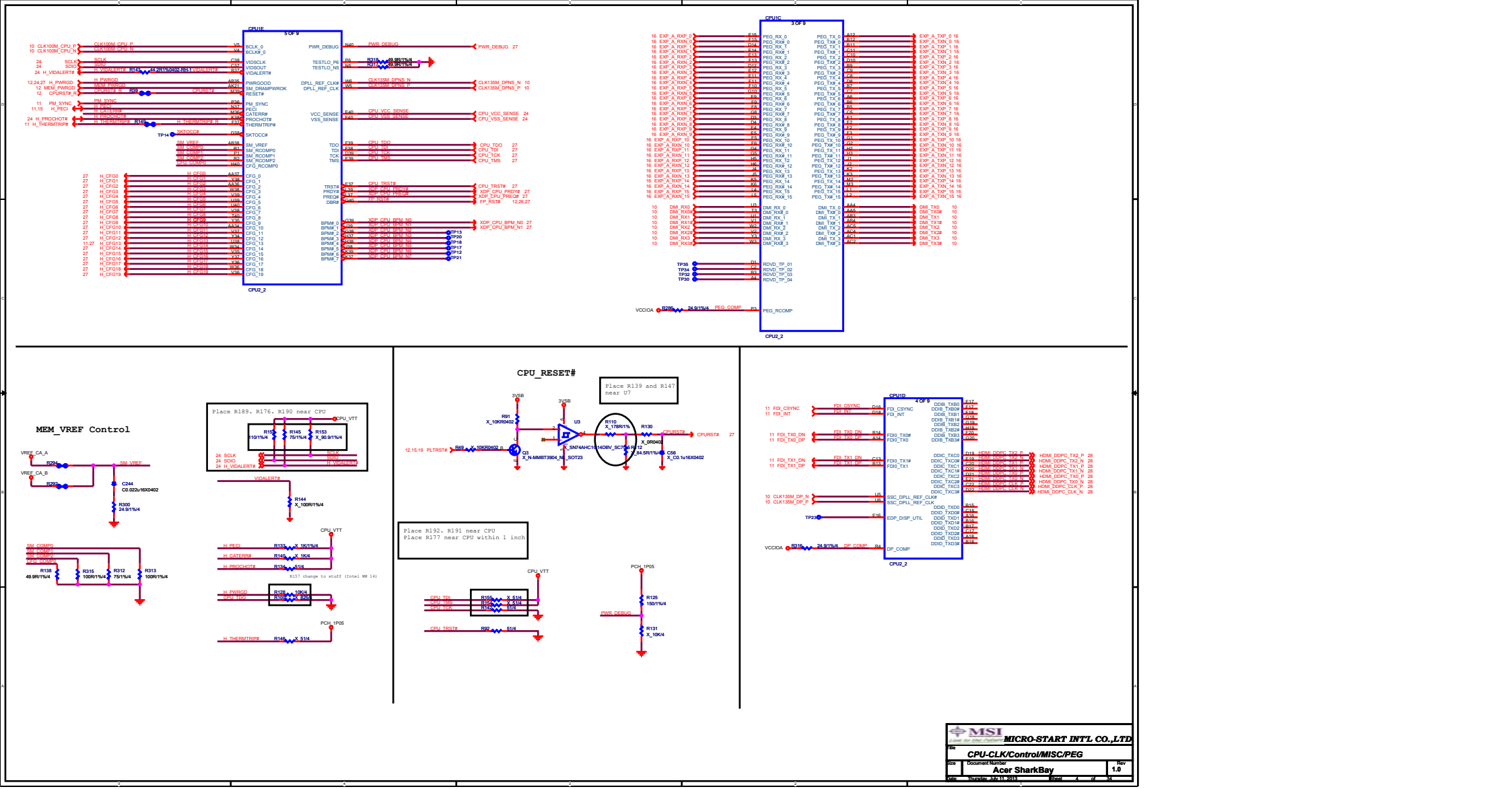


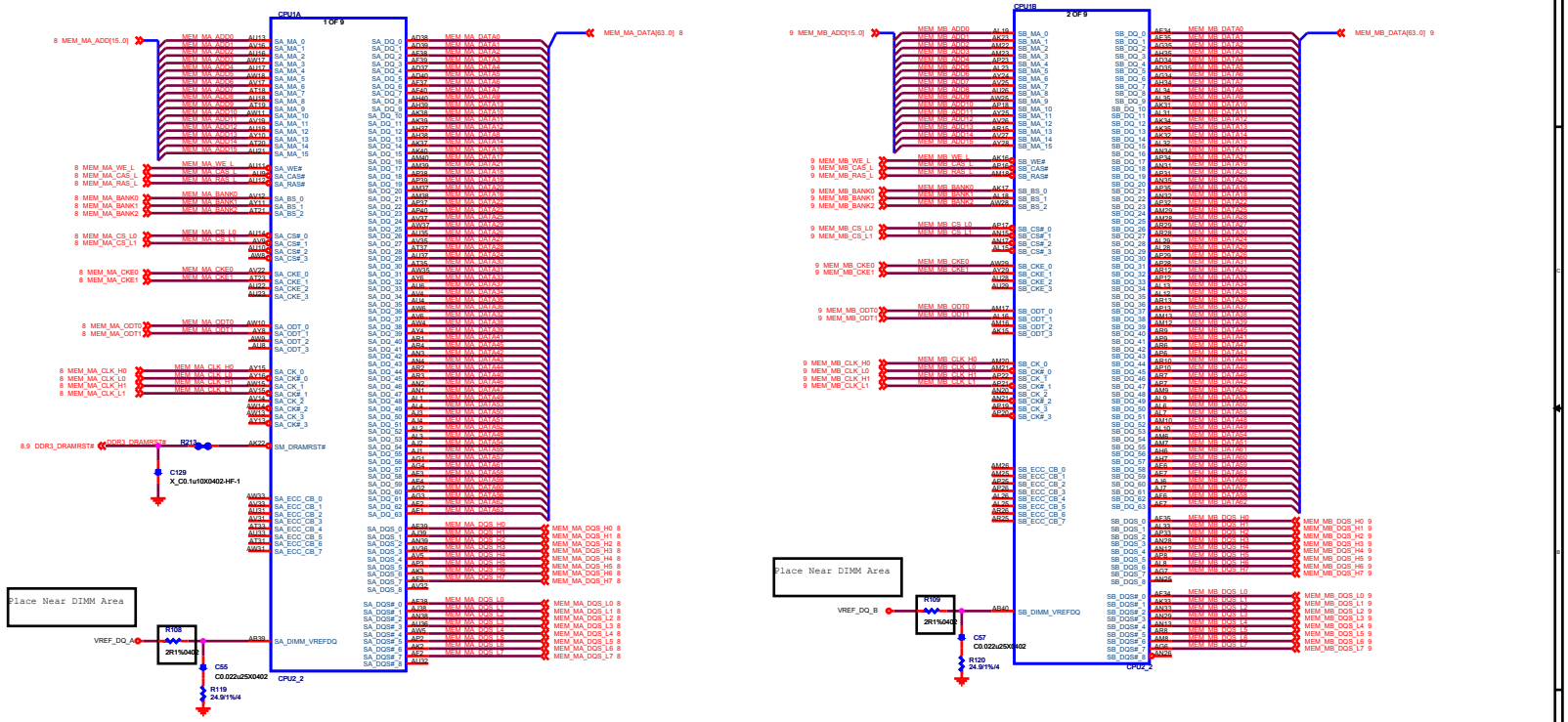
MSI MICRO-STAR INT'L CO.,LTD

Title: Clock Distribution

Size | Document Number: Acer SharkBay | Rev: 1.0

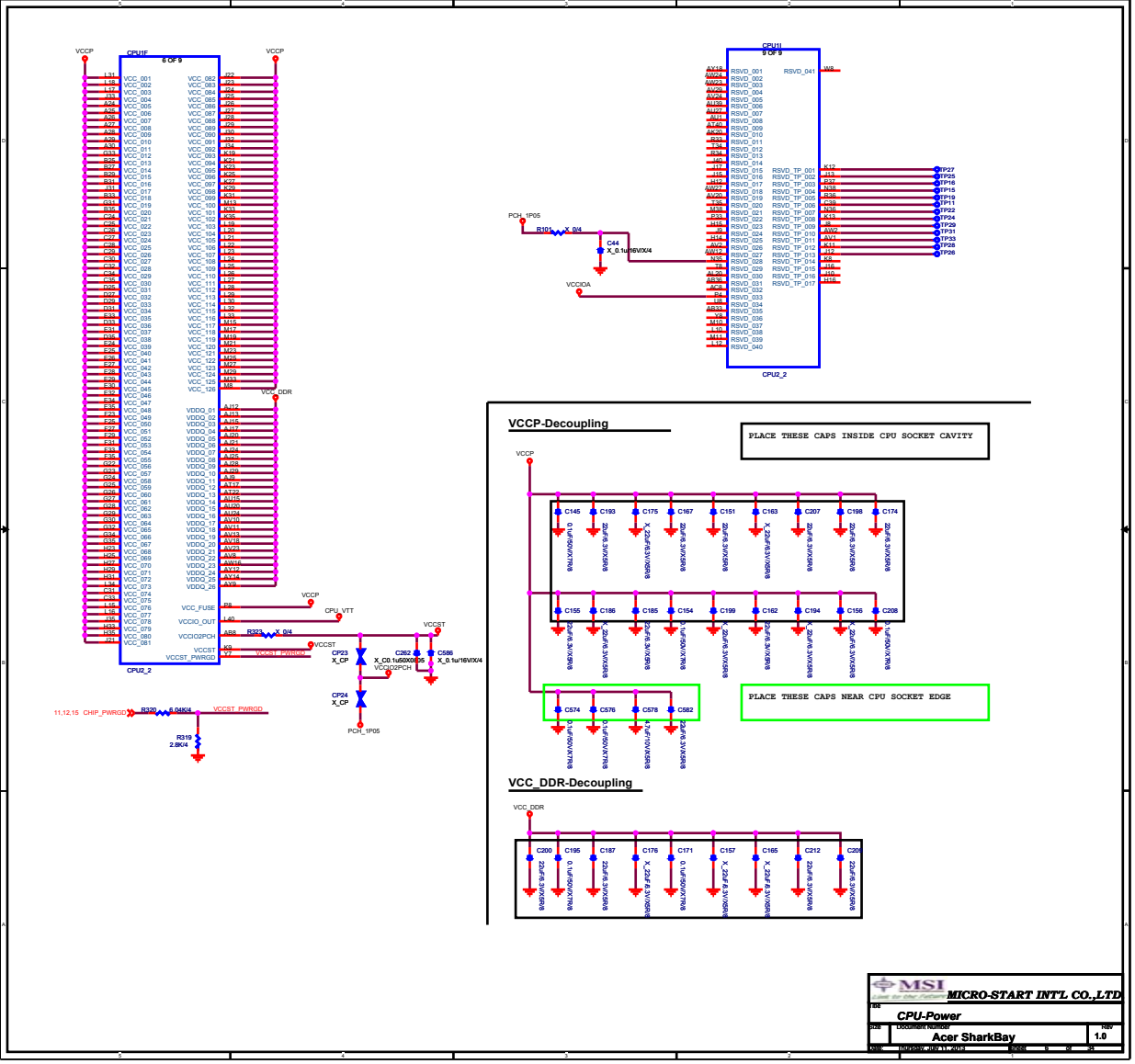
Date: Thursday, July 11, 2013 | Sheet 5 of 34

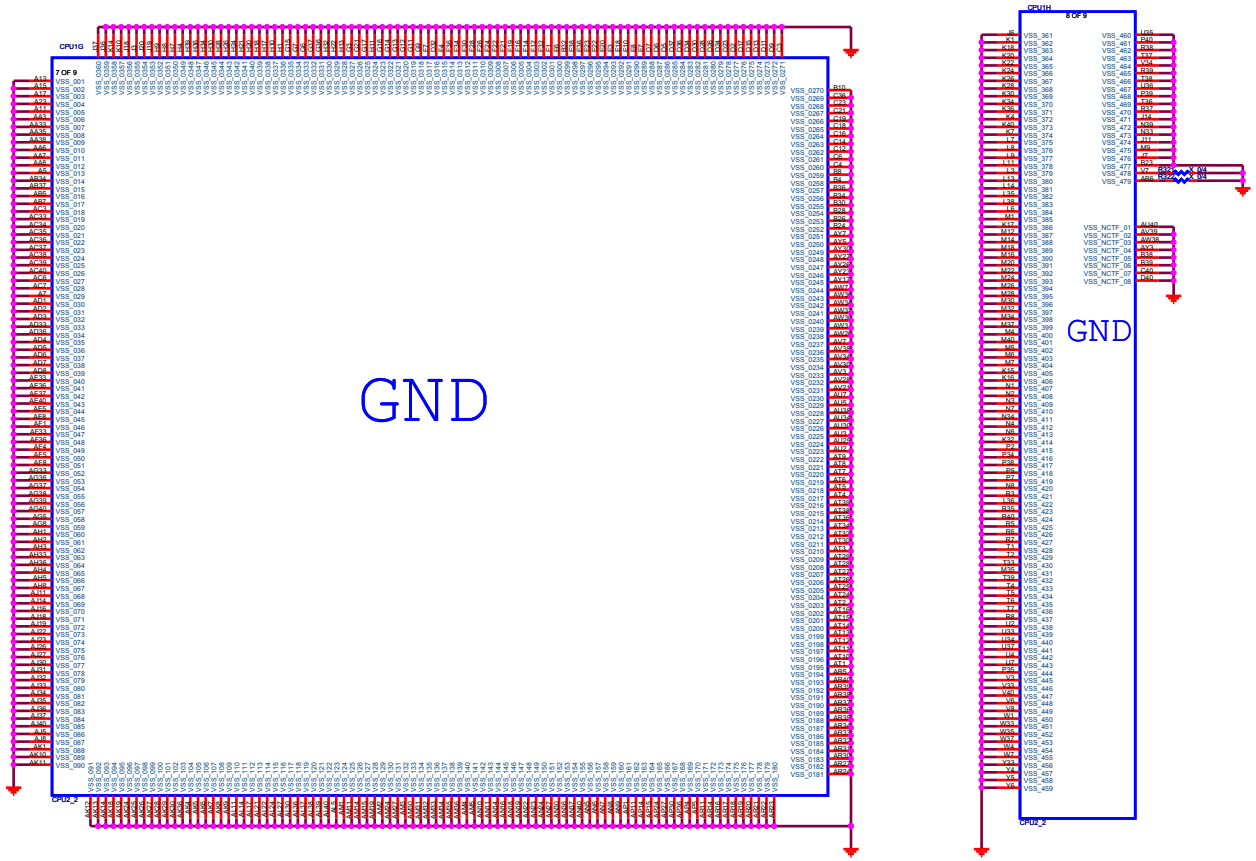

CPU1E
5 OF 9
CPU2_2
CPU1C
3 OF 9
CPU2_2
MEM_VREF Control
Place R189、R176、R190 near CPU
CPU_RESET#
Place R139 and R147 near U7
Place R192、R191 near CPU
Place R177 near CPU within 1 inch
CPU1D
4 OF 9
CPU2_2
MSI
MICRO-START INT'L CO.,LTD
CPU-CLK/Control/MISC/PEG
Acer SharkBay
1.0
Thursday, July 11, 2013



MSI — MICRO-START INT'L CO.,LTD

File	CPU-Memory	
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 5 of 34	


CPU1F
6 OF 9
CPU2_2
CPU1I
9 OF 9
CPU2_2
VCCP
VCC_DDR
CPU_VTT
VCCST
VCCST_PWRGD
CHIP_PWRGD
PCH_1P05
VCCIO2DA
VCCIO2PCH
R319
2.8K/4
R320
5.04K/4
R323
X_0/4
R105
X_0/4
C44
X_0.1u/16V/X4
CP23
X_CP
CP24
X_CP
C262
X_C0.1u/50X0D05
C586
X_0.1u/16V/X4
VCCP-Decoupling
PLACE THESE CAPS INSIDE CPU SOCKET CAVITY
PLACE THESE CAPS NEAR CPU SOCKET EDGE
VCC_DDR-Decoupling
MICRO-START INT'L CO.,LTD
CPU-Power
Acer SharkBay
1.0



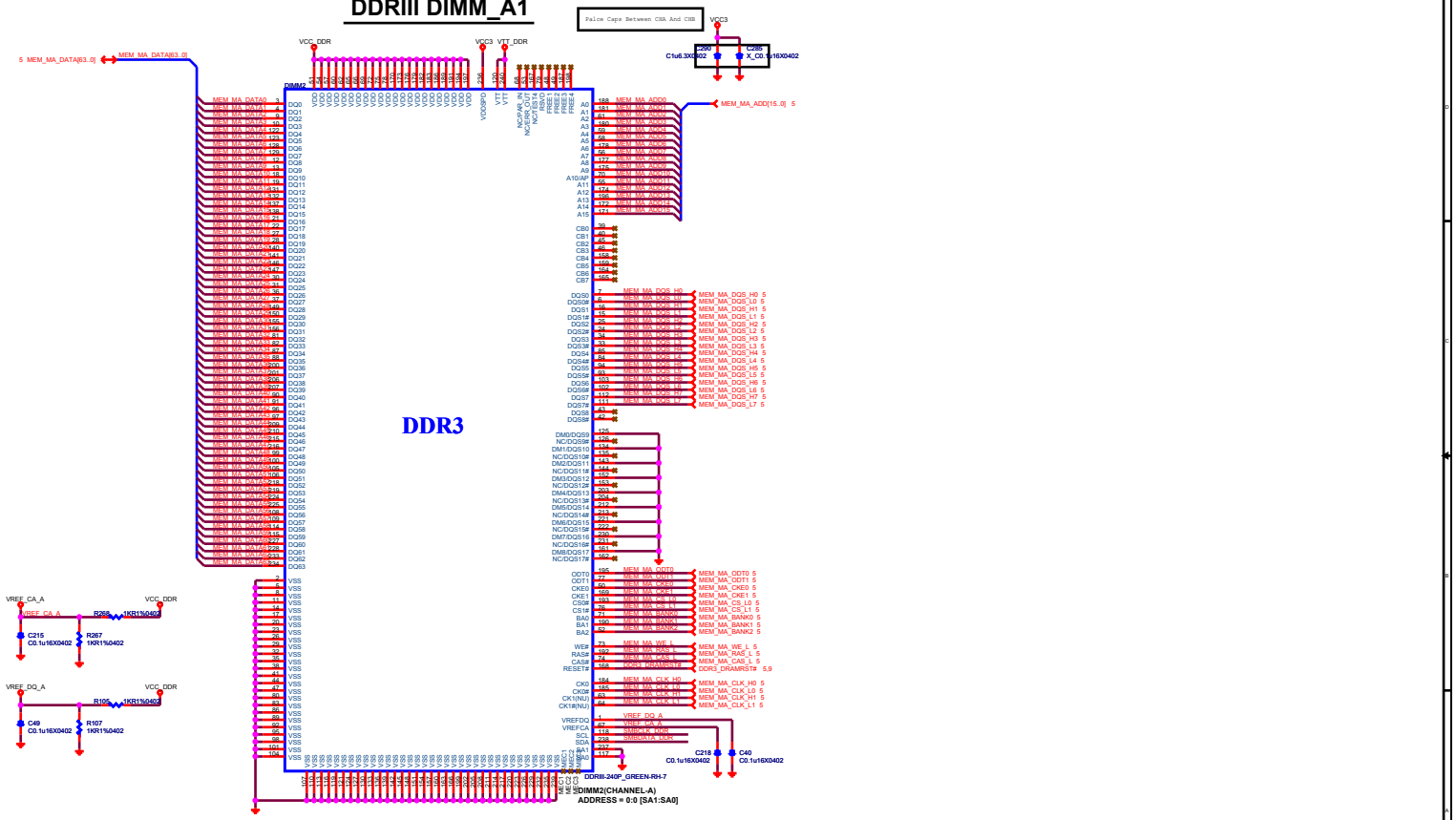
MSI MICRO-START INT'L CO.,LTD

Title: CPU-GND

Size	Document Number	Rev
	Acer SharkBay	1.0

Date: Thursday, June 11, 2015 Sheet 7 of 38

DDRIII DIMM_A1



DDR3

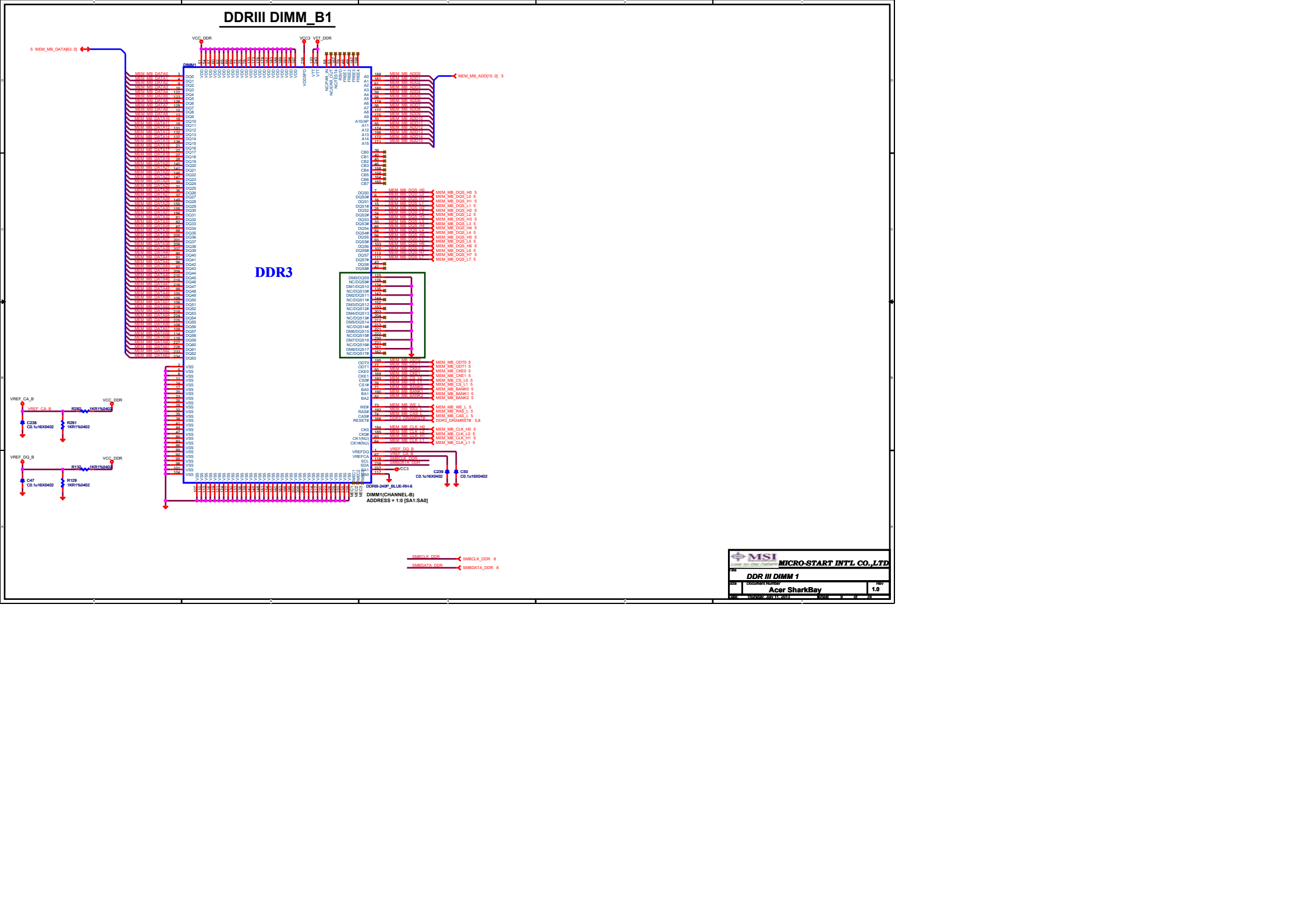
MSI MICRO-START INT'L CO.,LTD

File: DDR III DIMM 2

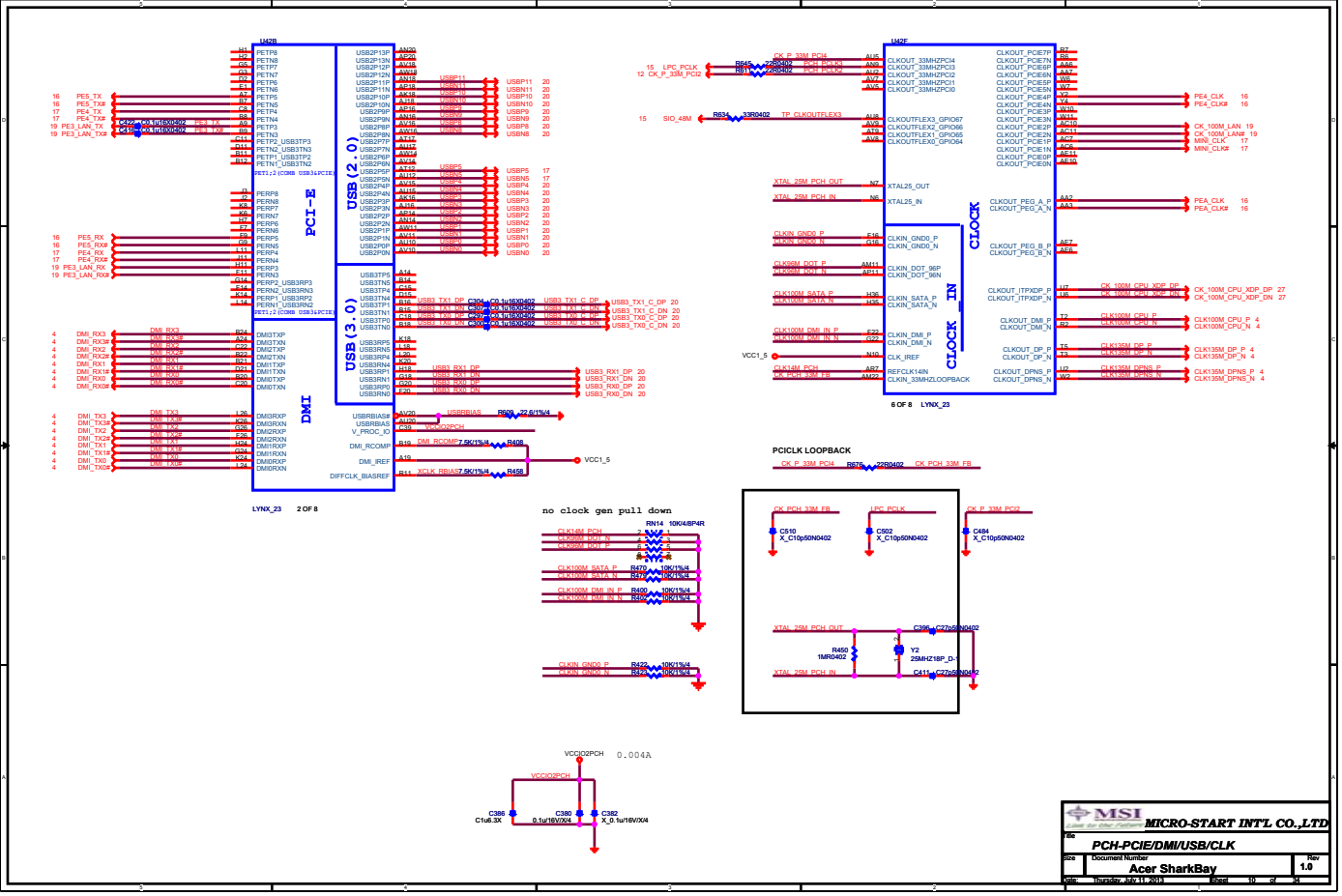
Size	Document Number	Rev
	Acer SharkBay	1.0

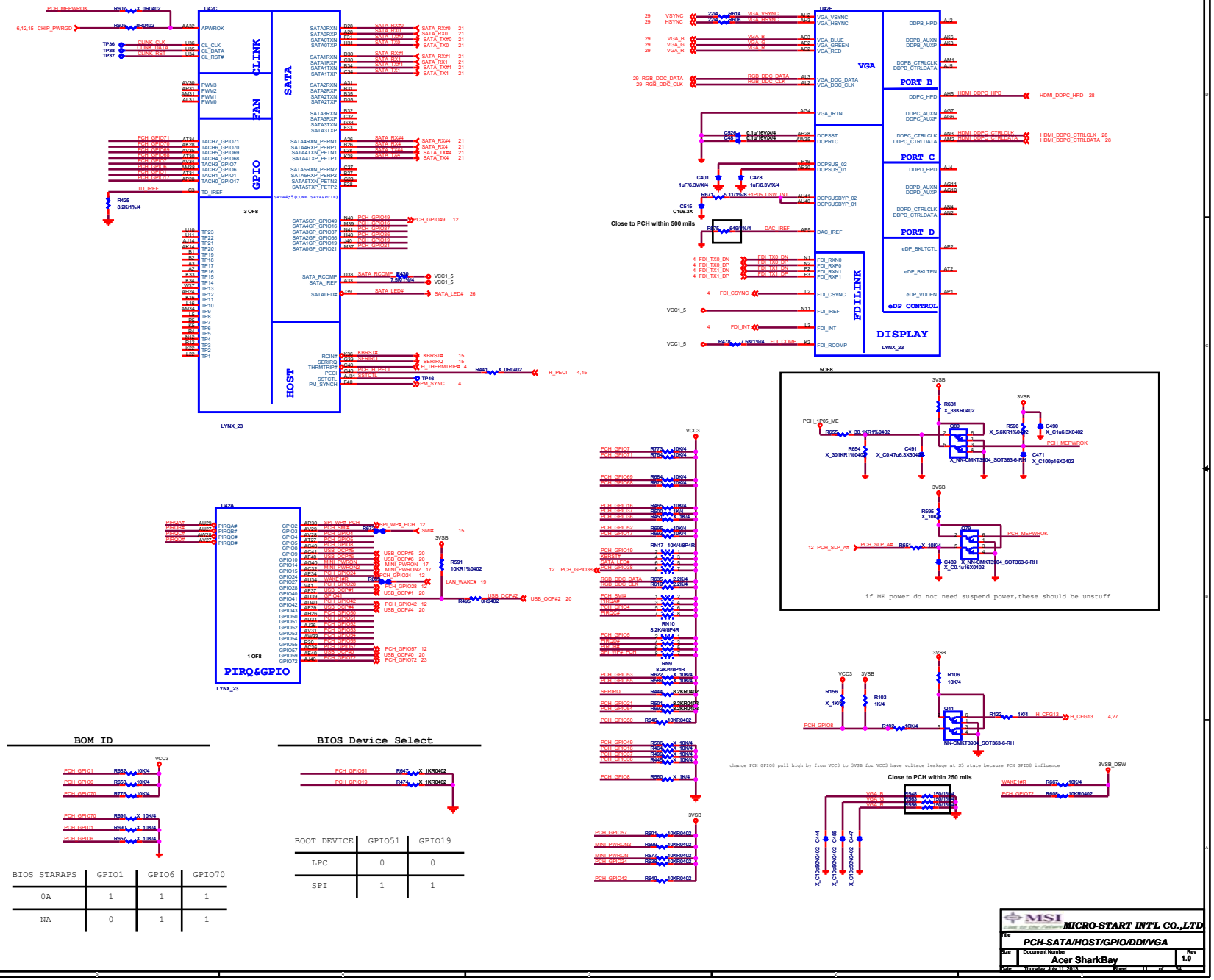
Date: Thursday, July 11, 2013 Sheet 8 of 34

DDRIII DIMM_B1



MSI	MICRO-START INT'L CO.,LTD	
Title	DDR III DIMM 1	
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 9 of 34	


PCI-E
USB (2, 0)
USB (3, 0)
DMI
CLOCK
CLOCK IN
LYNX_23 2 OF 8
6 OF 8 LYNX_23
PCICLK LOOPBACK
no clock gen pull down
MICRO-START INT'L CO.,LTD
PCH-PCIE/DMI/USB/CLK
Acer SharkBay
Thursday, July 11, 2013



BOM ID

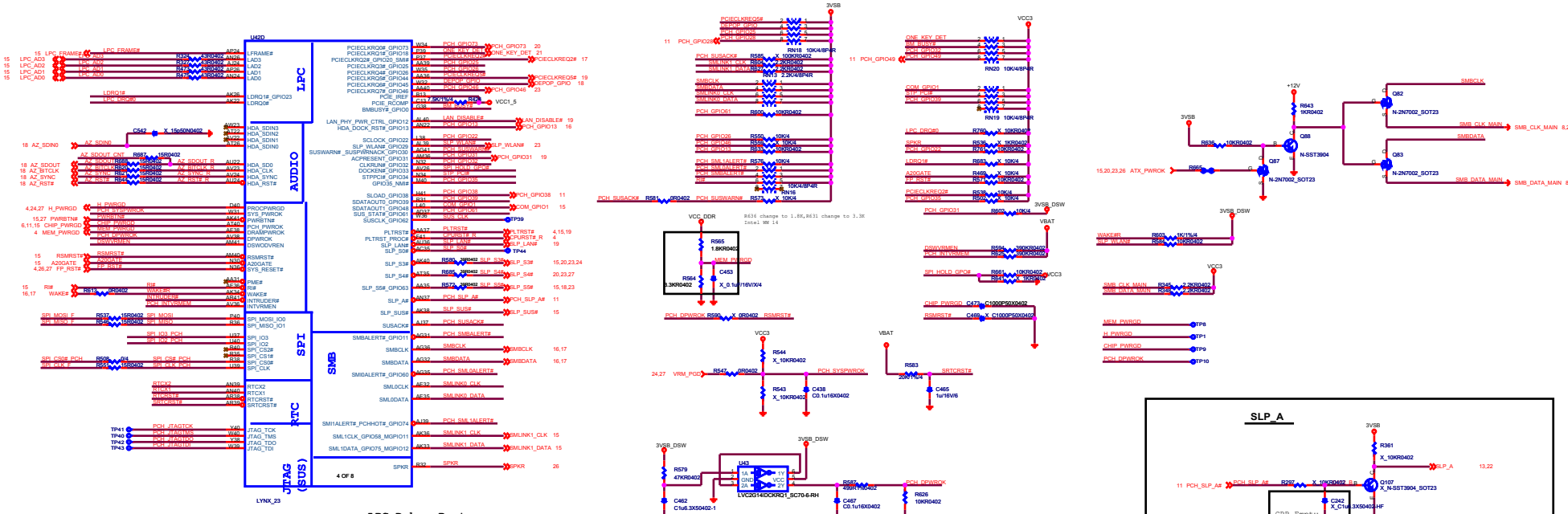
BIOS STARAPS	GPIO1	GPIO6	GPIO70
0A	1	1	1
NA	0	1	1

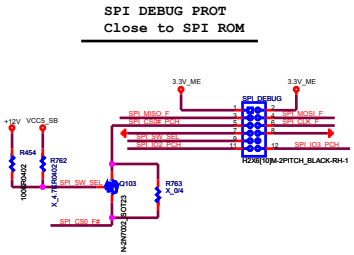
BIOS Device Select

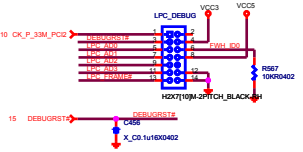
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

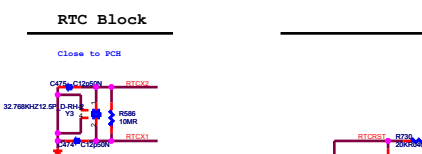
MSI MICRO-START INT'L CO.,LTD

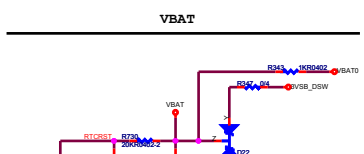
File	PCH-SATA/HOST/GPIO/DDI/VGA	
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 11 of 34	

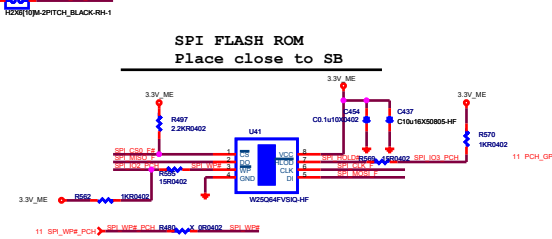


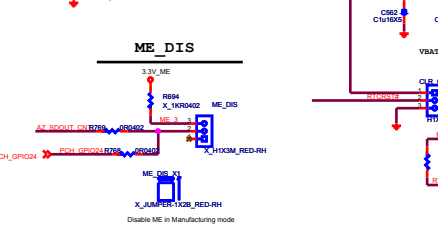


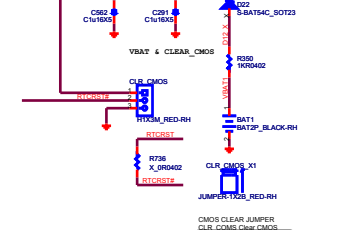






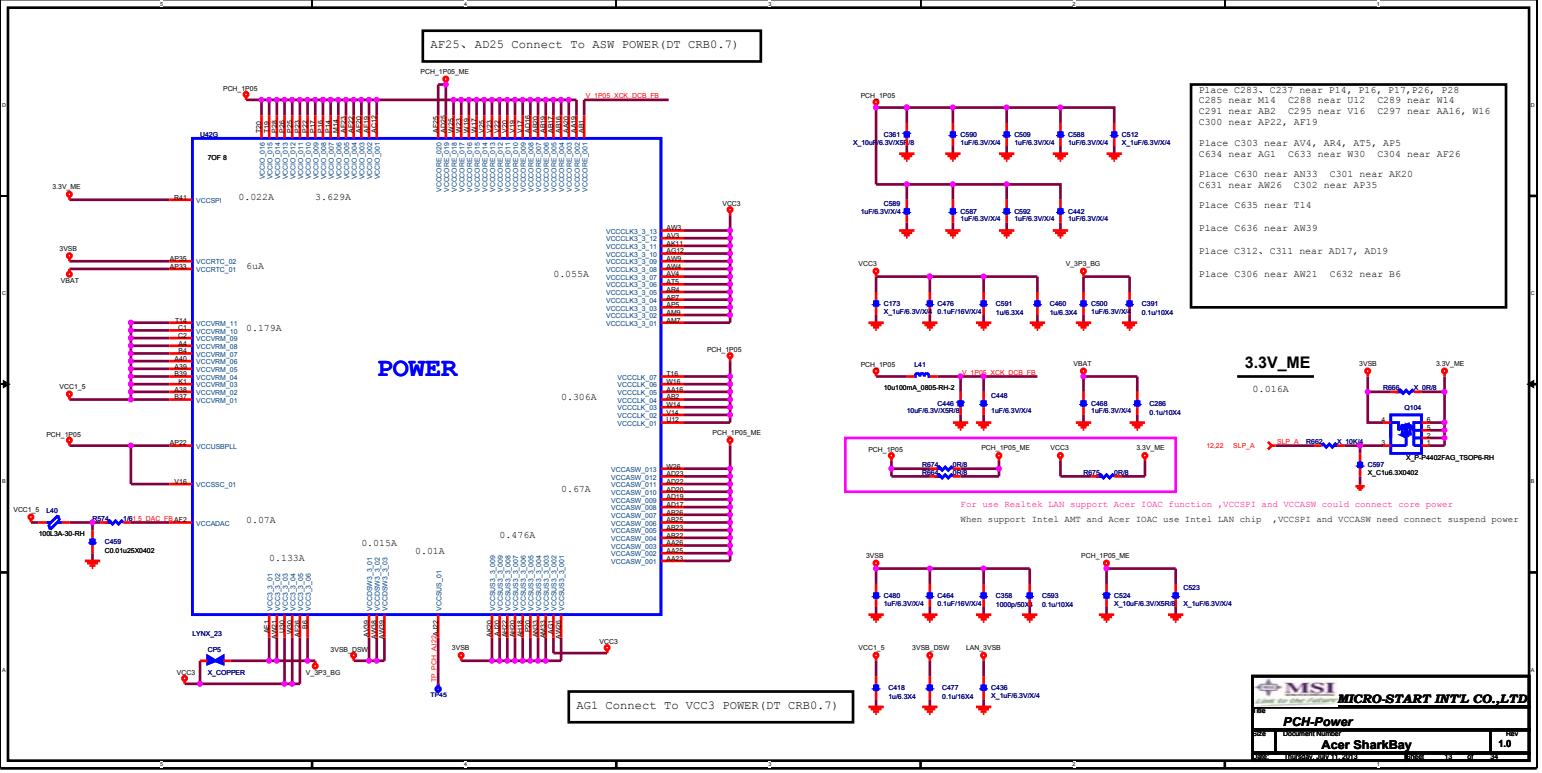






HDA_SDO is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal input can be tied to a jumper which connects the input to power through an external pull up (1K?%) ONLY. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

MSI	MICRO-START INT'L CO.,LTD	
Title	PCH-SMB/LPC/AUDIO/RTC	
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, April 11, 2013	Sheet 14 of 48	



Place C283、C237 near P14, P16, P17,P26, P28
C285 near M14 C288 near U12 C289 near W14
C291 near AB2 C295 near V16 C297 near AA16, W16
C300 near AP22, AP19

Place C303 near AV4, AR4, AT5, AP5
C634 near AG1 C633 near W30 C304 near AF26

Place C630 near AN33 C301 near AK20
C631 near AW26 C302 near AP35

Place C635 near T14

Place C636 near AW39

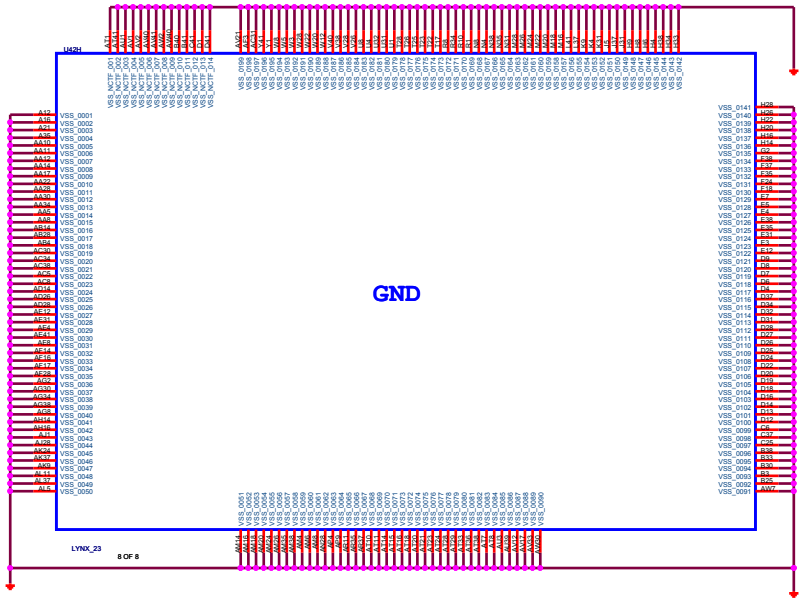
Place C312、C311 near AD17, AD19

Place C306 near AW21 C632 near B6

3.3V_ME
0.016A

For use Realtek LAN support Acer IOAC function ,VCCSPI and VCCASW could connect core power
When support Intel AMT and Acer IOAC use Intel LAN chip ,VCCSPI and VCCASW need connect suspend power

MICRO-START INTL CO.,LTD		
Title: PCH-Power		
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 13 of 34	

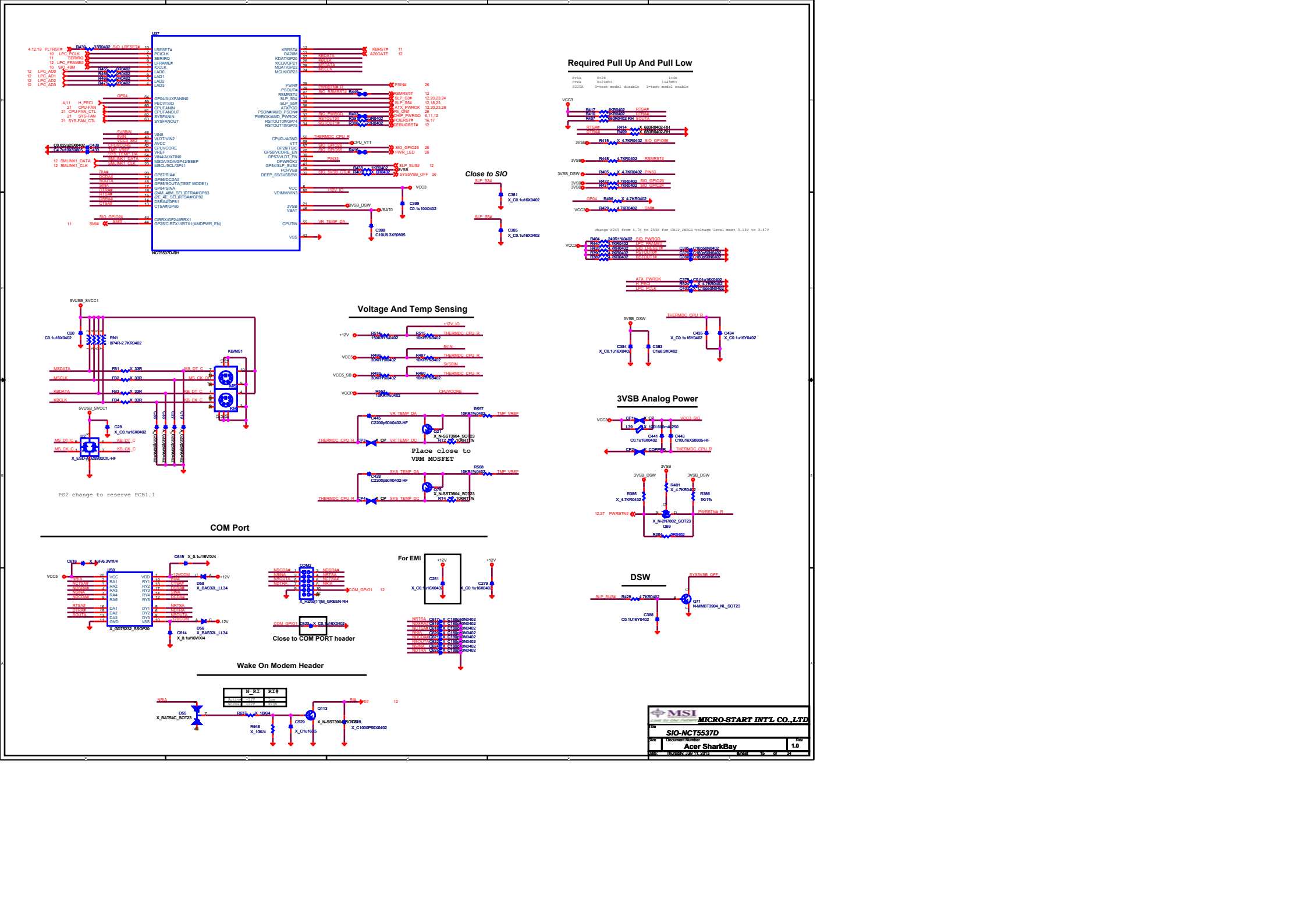


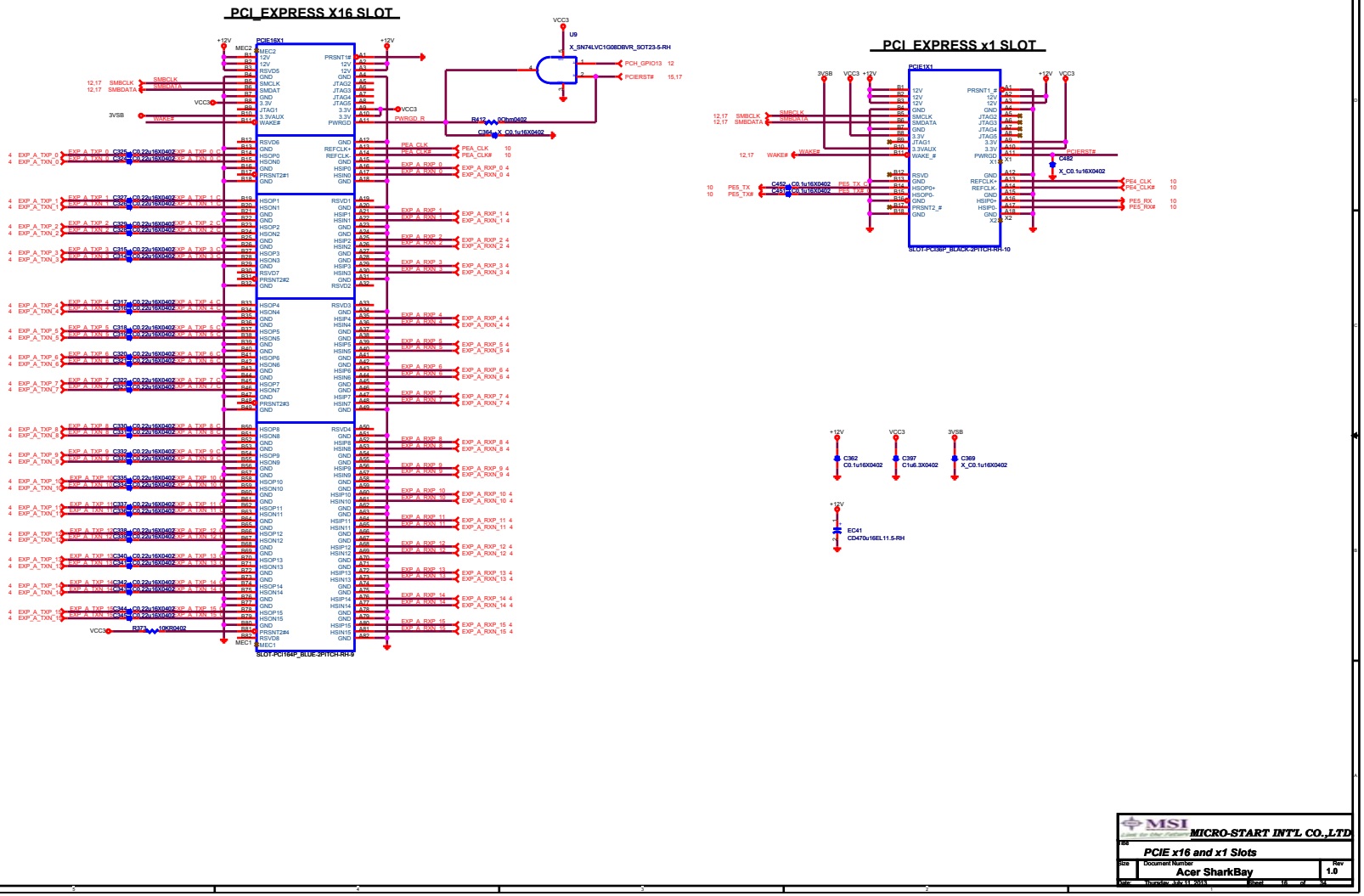
MICRO-START INT'L CO.,LTD

Title: PCH-GND

Size: | Document Number: Acer SharkBay | Rev: 1.0

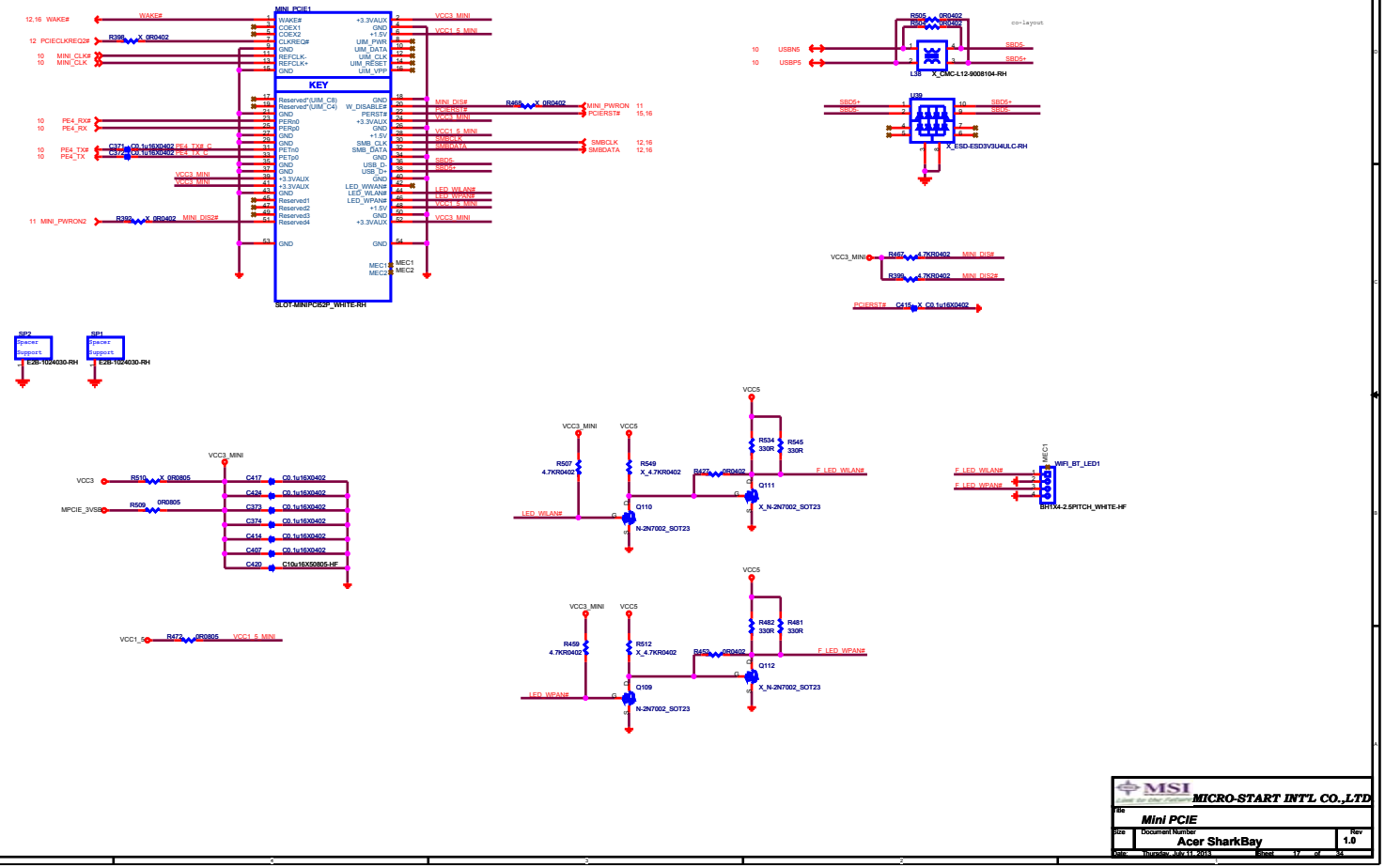
Date: | Tuesday, June 11, 2013 | Sheet 13 of 34


Required Pull Up And Pull Low
Close to SIO
Voltage And Temp Sensing
Place close to
VRM MOSFET
3VSB Analog Power
PS2 change to reserve PCB1.1
COM Port
Close to COM PORT header
For EMI
DSW
Wake On Modem Header
MICRO-START INT'L CO.,LTD
SIO-NCT5537D
Acer SharkBay
1.0



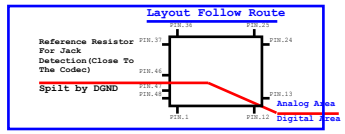
MSI	MICRO-START INT'L CO.,LTD	
Title: PCIE x16 and x1 Slots		
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 16 of 34	

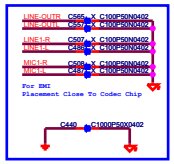
Half-size Mini PCIE Card

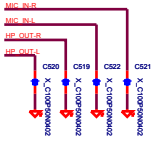


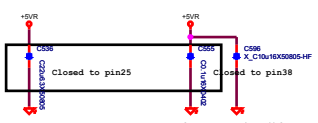
MSI	MICRO-START INT'L CO.,LTD		
Title	Mini PCIE		
Size	Document Number: Acer SharkBay		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 17 of 34		

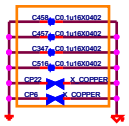
Azalia Codec -ALC662

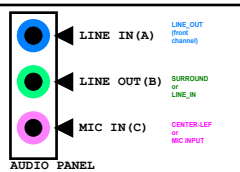




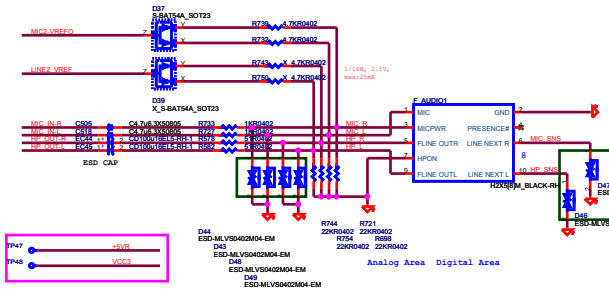






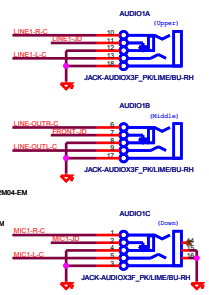


Front Audio Jack

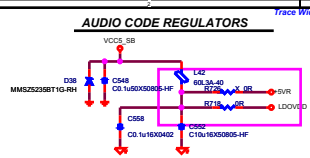


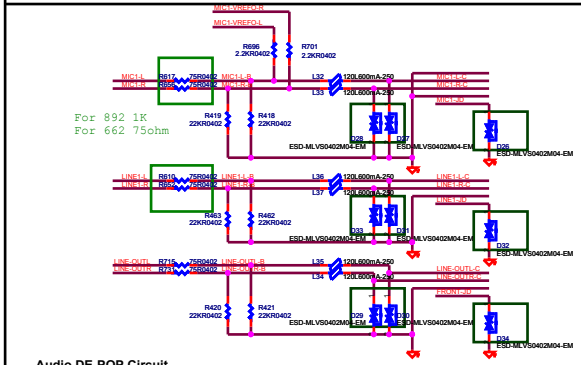
EMC Request

3 Jack

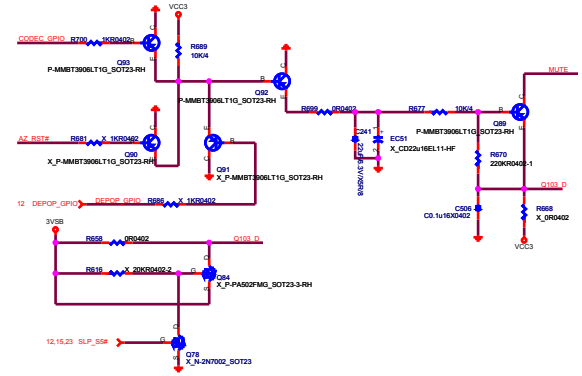


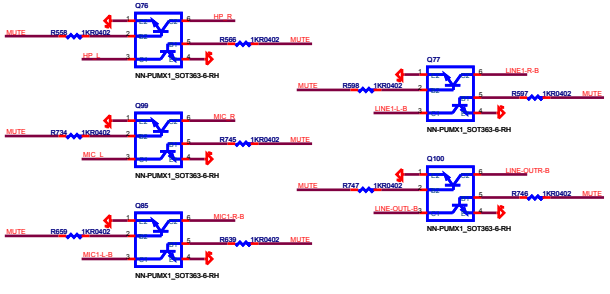
AUDIO CODE REGULATORS



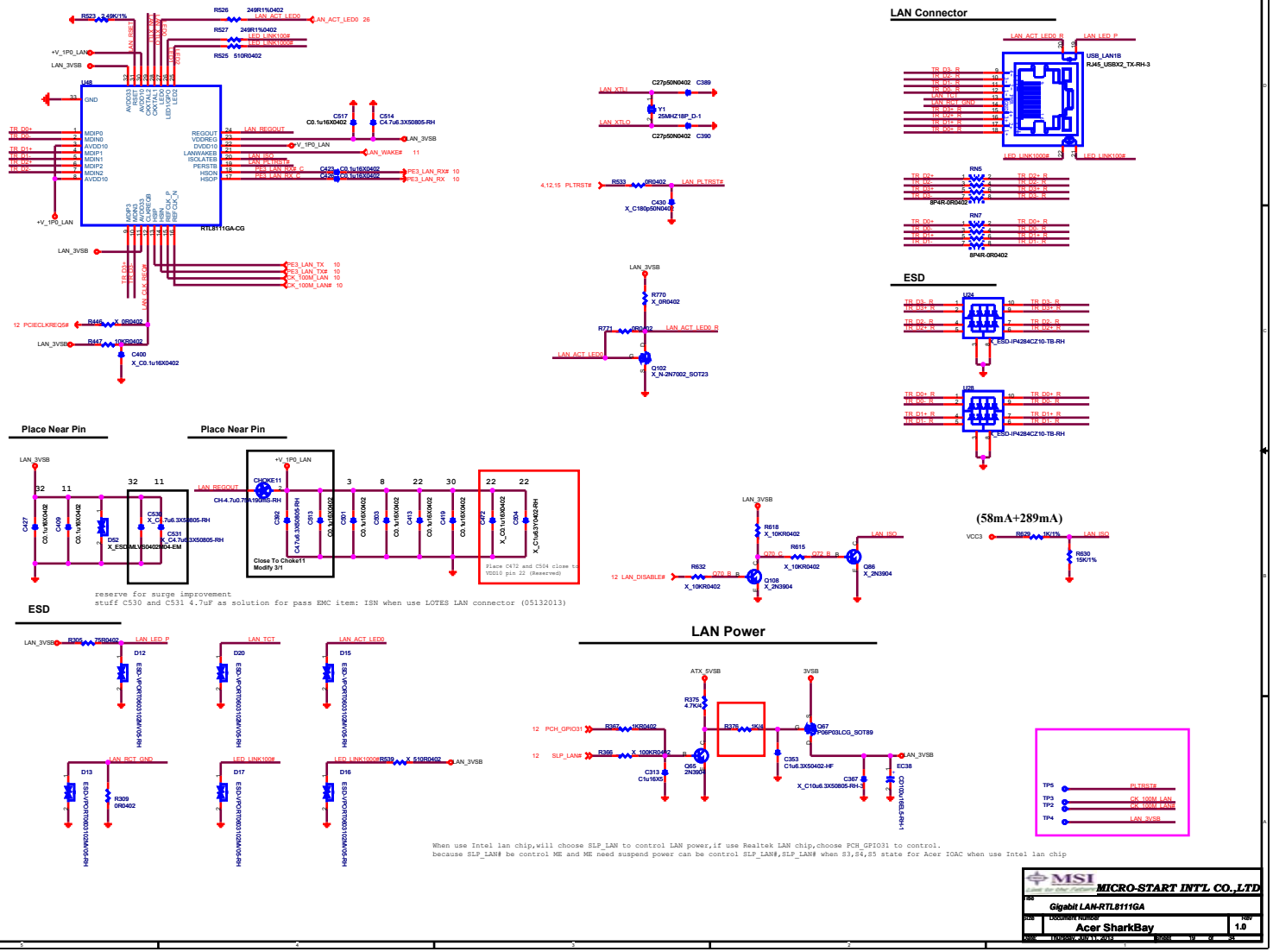


Audio DE-POP Circuit

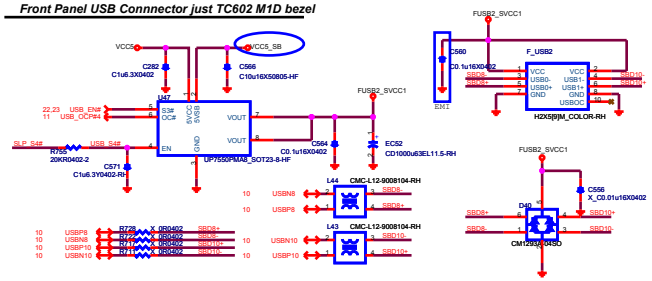




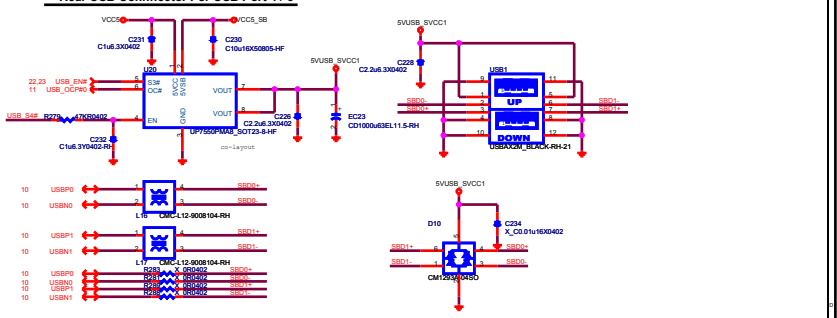
MSI MICRO-START INT'L CO.,LTD		
Title: Audio Codec-ALC892 Co-lay ALC662-VD		
Size: Custom	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, May 31, 2012	Sheet 18 of 34	


LAN Connector
ESD
Place Near Pin
Place Near Pin
ESD
LAN Power
(58mA+289mA)
reserve for surge improvement
stuff C530 and C531 4.7uF as solution for pass EMC item: ISN when use LOTES LAN connector (05132013)
When use Intel lan chip,will choose SLP_LAN to control LAN power,if use Realtek LAN chip,choose PCH_GPIO31 to control.
because SLP_LAN# be control ME and ME need suspend power can be control SLP_LAN#,SLP_LAN# when S3,S4,S5 state for Acer IOAC when use Intel lan chip
MICRO-START INT'L CO.,LTD
Gigabit LAN-RTL8111GA
Acer SharkBay
1.0

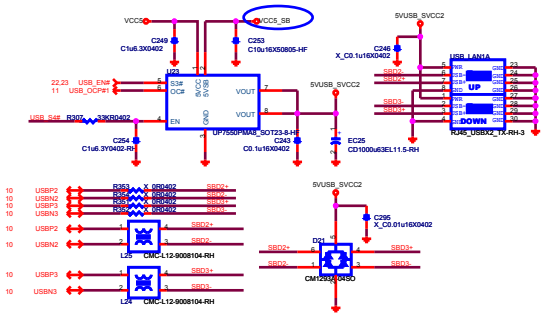
Front Panel USB Connnector just TC602 M1D bezel



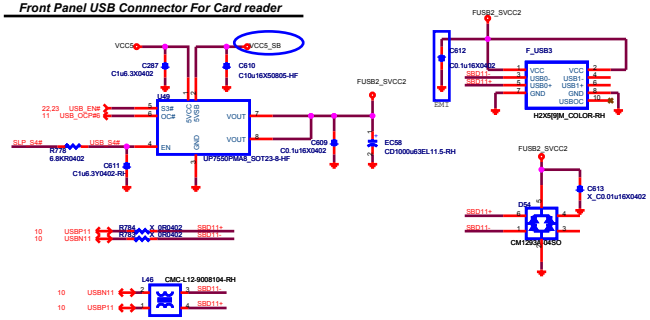
Rear USB Connnector For USB Port 4 / 5

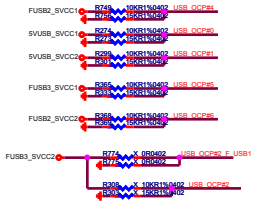


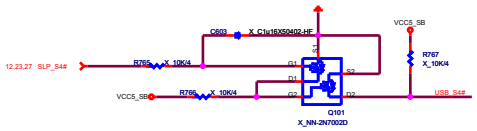
Rear USB Connnector For USB Port 8 / 9



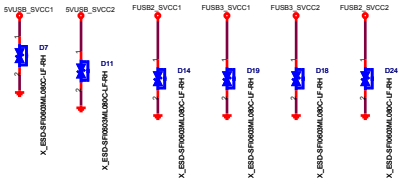
Front Panel USB Connnector For Card reader





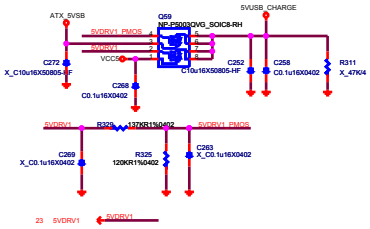


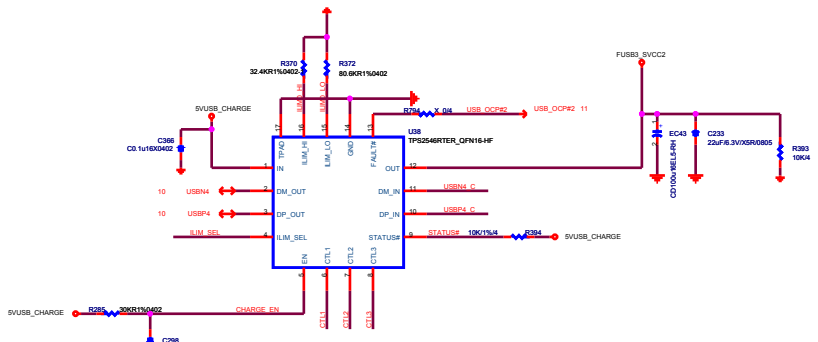
Reserve ESD protection diode on USB front header 5V_Dual power.



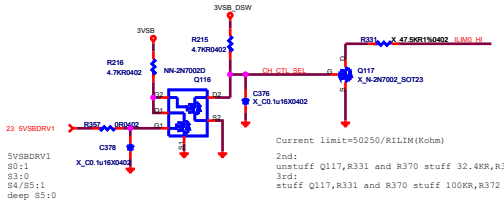
FRONT USB3.0 With Charge

NOTE:
Because of TC602 M1D bezel just support USB2.0 Port, so it will be stuff F_USB2 and unstuff F_USB1 ;
if not use TC602 M1D bezel, it will be stuff F_USB1 and unstuff F_USB2.
But will be stuff all for validate first,later choose one.





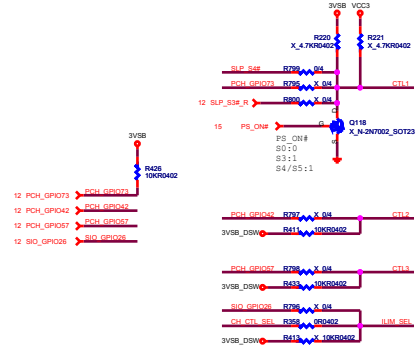
Control PIN



5VSBDRV1
S0:1
S3:0
S4/S5:1
deep S5:0

Current limit=50250/RILIM(Kohm)

2nd:
unstuff Q117,R331 and R370 stuff 32.4KR,R372 stuff 80.6KR
3rd:
stuff Q117,R331 and R370 stuff 100KR,R372 stuff 32.4KR



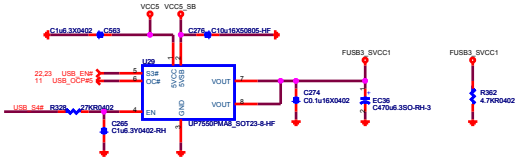
Default(2nd)	CTL1	CTL2	CTL3	ILIM_SEL
CDP(S0)	1	1	1	1
SDP(S3)	1	1	1	0
DCP(S4/S5)	0	1	1	1

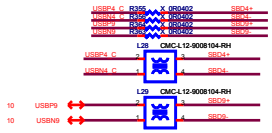
Stuff:R799,R411,R433,R358
Unstuff:Q118,R220,R795,R797,R798,R796,R413,Q117,R331,R800,R221

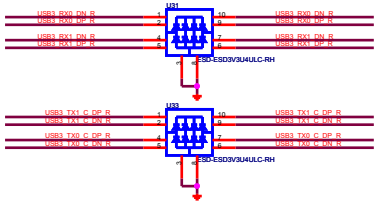
Reserve(3rd)	CTL1	CTL2	CTL3	ILIM_SEL
CDP(S0)	1	1	1	1
SDP(S3)	0	1	1	1
DCP(S4/S5)	0	1	1	1

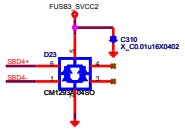
Stuff:Q118,R220,R411,R433,R413
Unstuff:R799,R795,R797,R798,R796,R358,R800,R221

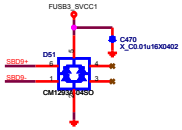
S0 DCP: not support
CDP: 1.5A
SDP: 0.5A others not support
S3 SDP:0.5A(support wake) 0111 or 1110
S4 DCP:1.5A
S5 DCP:1.5A



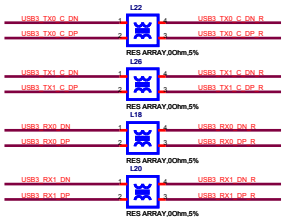


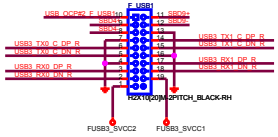






*co-lay R3C-0000012-****





Pin 1 should provide 1.5A charge when power state at S0/S4/S5.

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Title: Front / Rear USB Connectors

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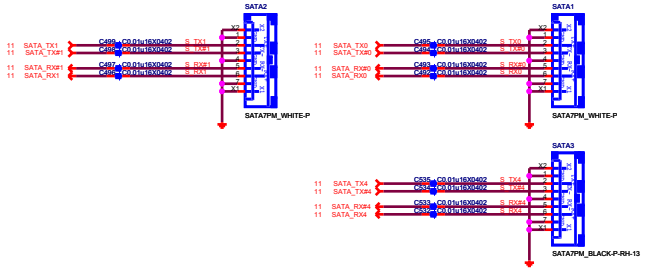
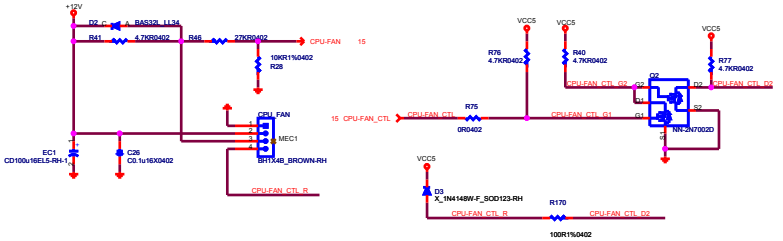
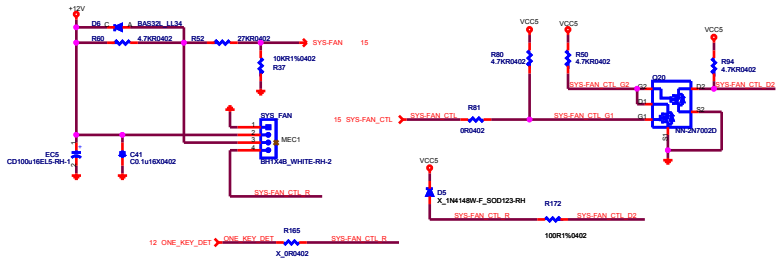
SATA Connector



CPU Fan



System Fan



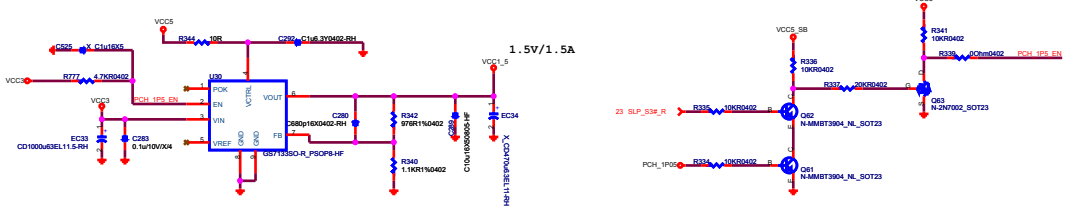
MICRO-START INTL CO.,LTD

File: SATA / FAN

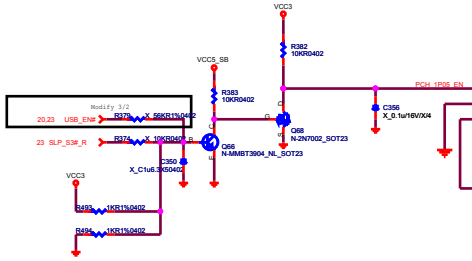
Size | Document Number: Acer SharkBay | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 21 of 34

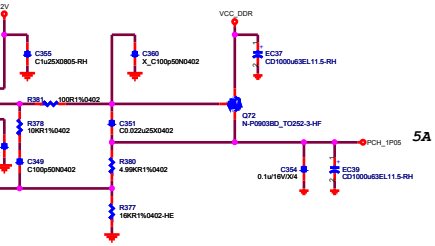
1.5V Power



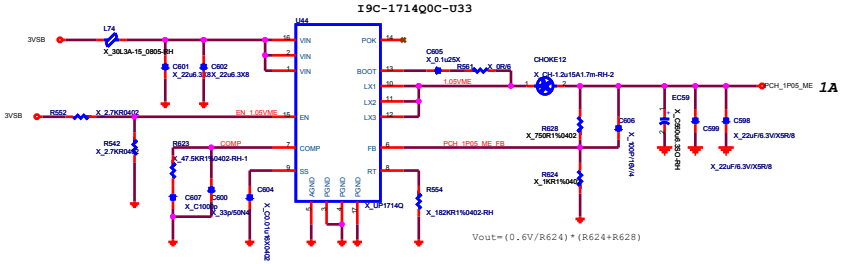
PCH Core Power Control



PCH Core Power



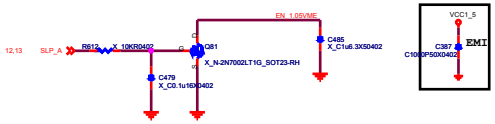
PCH ME Power



For use Realtek LAN support Acer IOAC function ,VCCSPI and VCCASW could connect core power

When support Intel AMT and Acer IOAC use Intel LAN chip ,VCCSPI and VCCASW need connect suspend power

PCH ME Power Control



MICRO-START INTL CO.,LTD

Title: PCH & ME Core Power		
Size	Document Number: Acer SharkBay	Rev: 1.0
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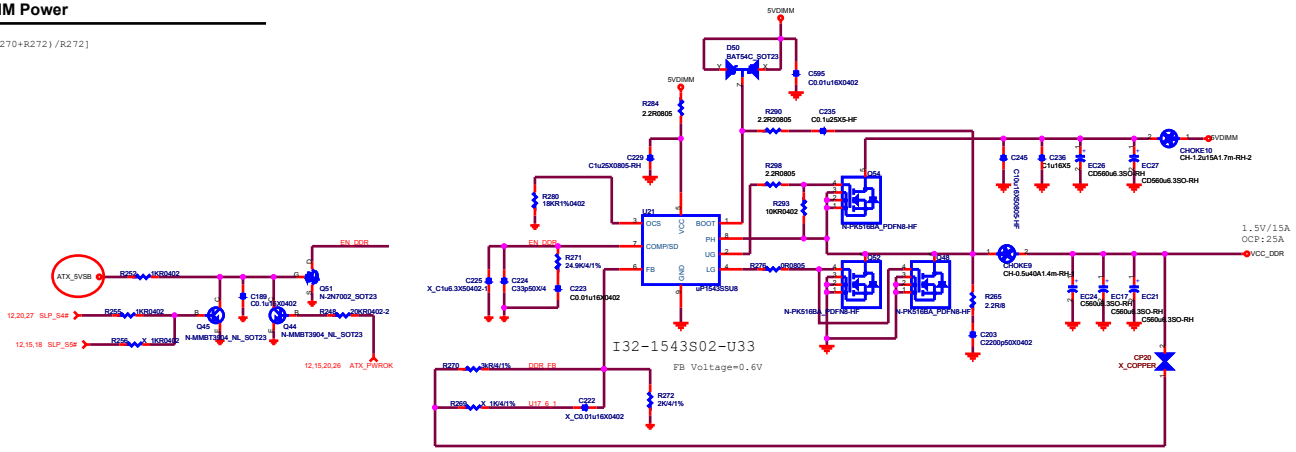
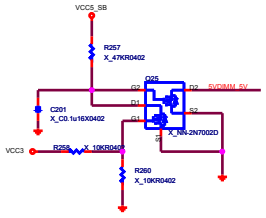
DDRIII DIMM Power

Vout = 0.6[(R270+R272)/R272]

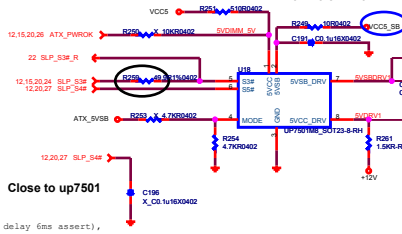




reserve some power supply VCC3 delay long time after VCC5 .
the chip U7501 5VDRV1 work when VCC5 ready(when VCC5 up to 4.2V and 5VDRV1 delay 6ms assert),
but VCC3 not ready and let 3VSB sequence fail

DDRIII Regulator Power Source

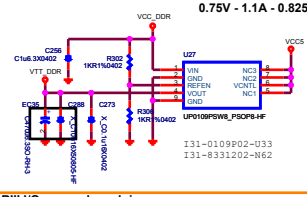
5V - 5.8A - 29W



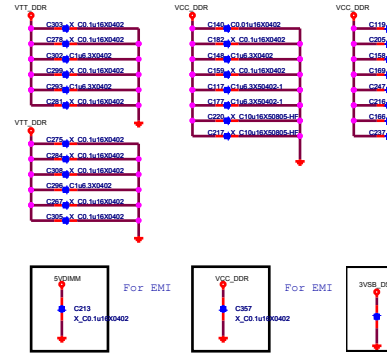
Close to up7501

DDRIII Termination Power

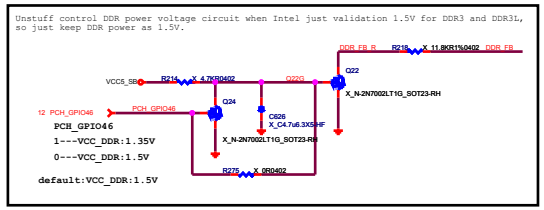
0.75V - 1.1A - 0.825W



DDRIII I/O power decoulping caps.

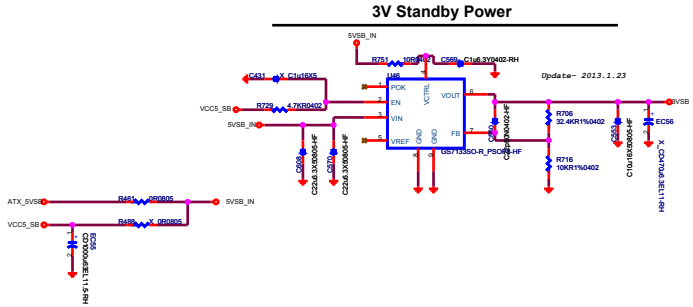


Unstuff control DDR power voltage circuit when Intel just validation 1.5V for DDR3 and DDR3L,
so just keep DDR power as 1.5V.



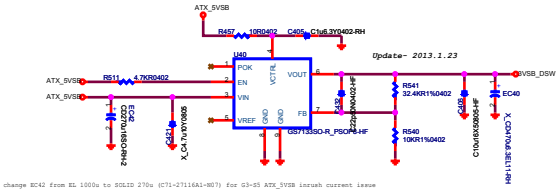
The processor supports two channels of
DDR3/DDR3L @ 1.5V with a maximum of two UDIMMs per channel.

3V Standby Power



Deep Sx Power

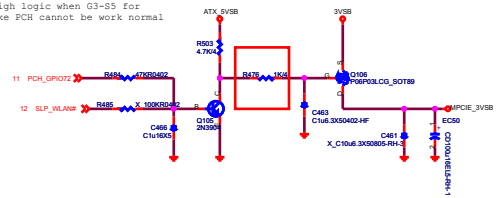
Vout=0.8*(R461+R449)/R461=3.392 V



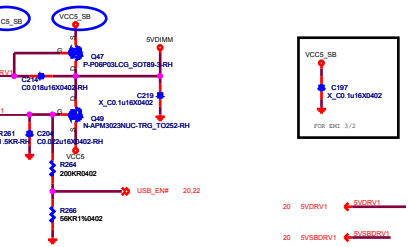
change EC42 from EL 1000u to SOLID 270u (C71-27116A1-H07) for G3-S5 ATX_5VSB inrush current issue

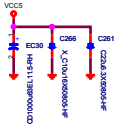
MPCIE Power

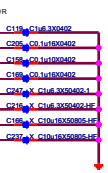
PCH_GPIO72 need keep high logic when G3-S5 for
if keep low will be make PCH cannot be work normal



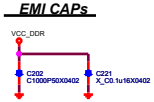
When use Intel lan chip,will choose SLP_WLAN# to control MINIPCIE power,if use Realtek LAN chip,choose PCH_GPIO72 to control.
because SLP_WLAN# be control and ME need suspend power can be control SLP_LAN#,SLP_WLAN# when S3,S4,S5 state for Acer IOAC when use Intel lan chip







EMI CAPs



For EMI

MSI
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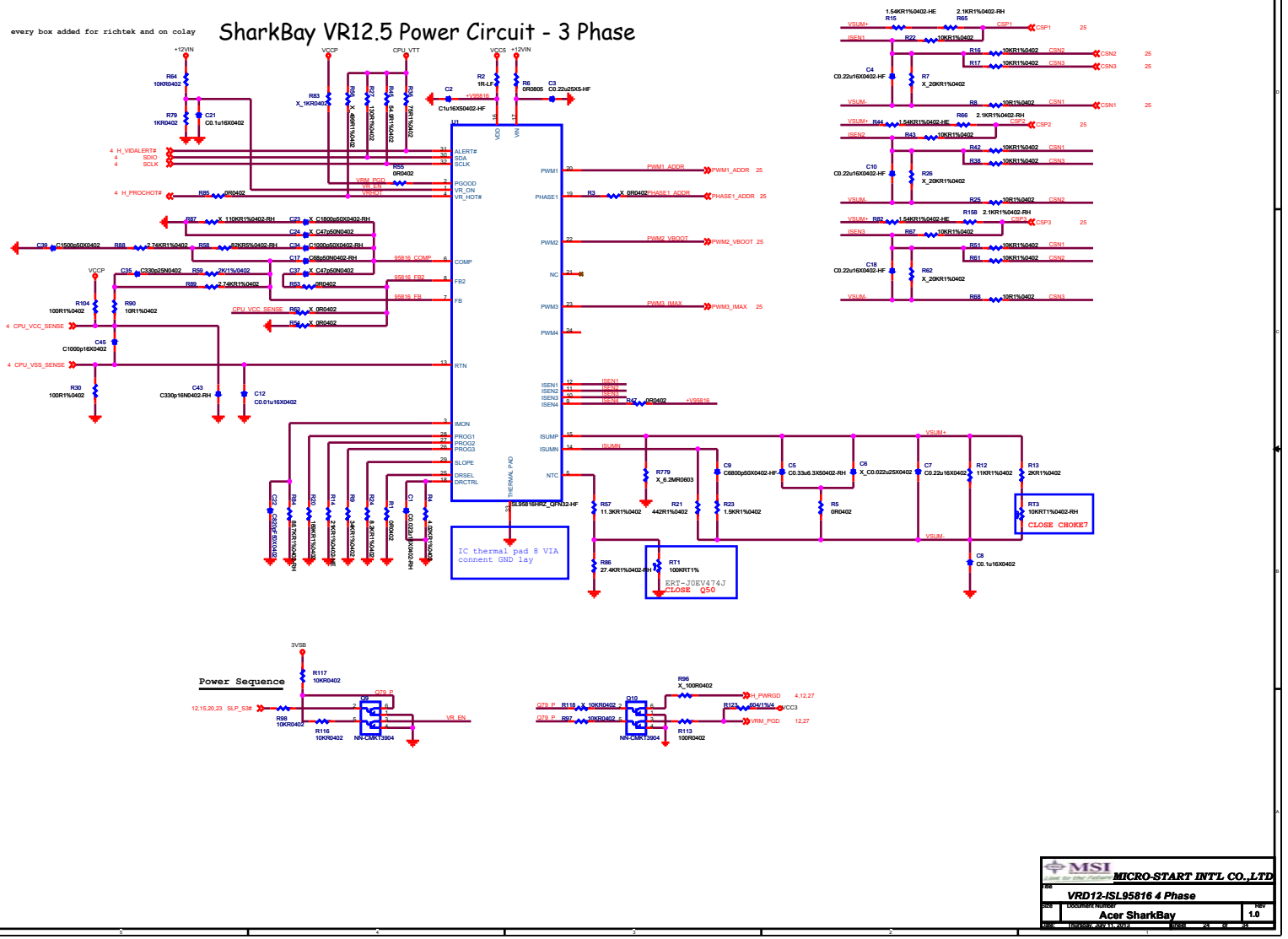
DDR Power

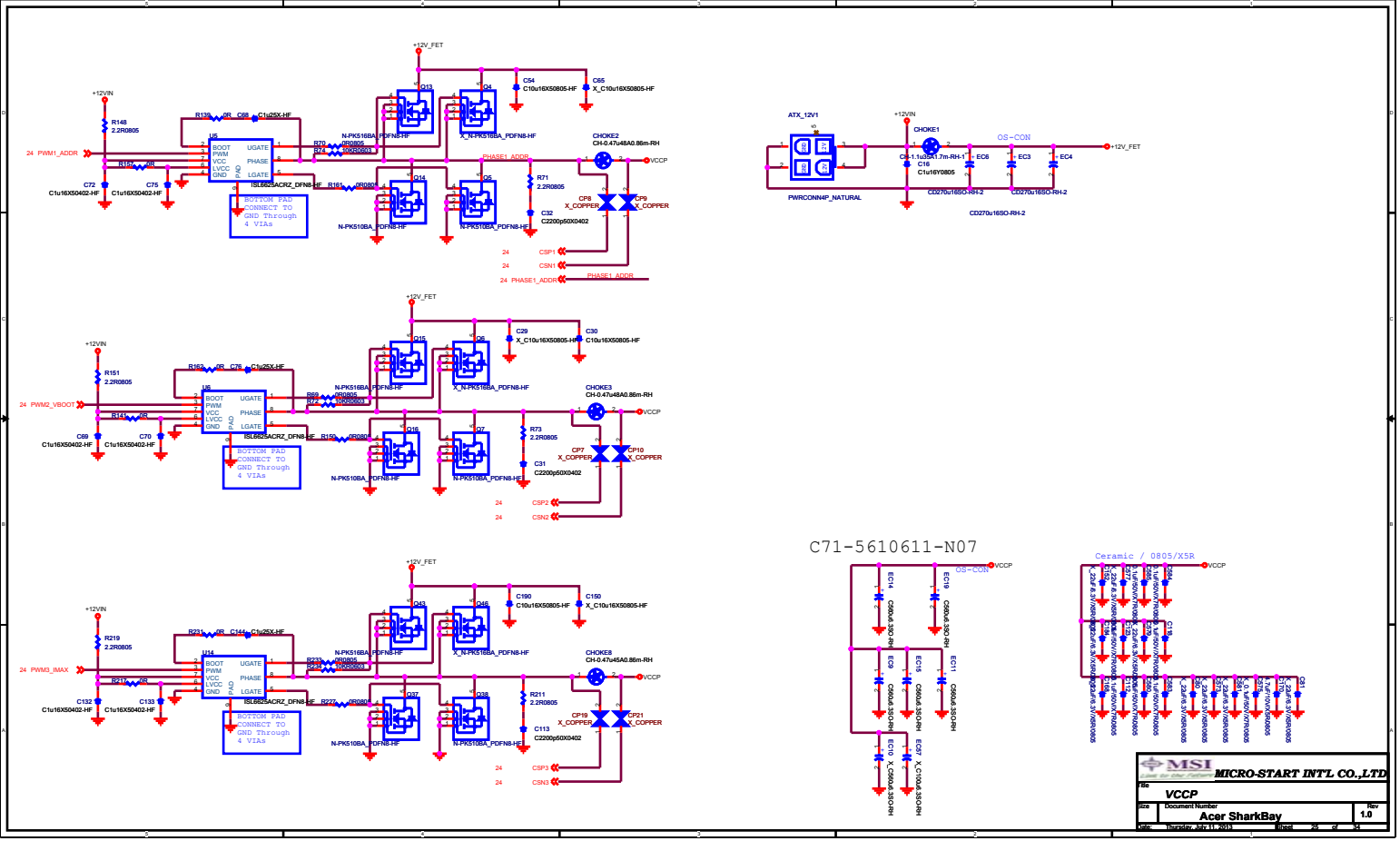
Acer SharkBay

1.0

every box added for richtek and on colay

SharkBay VR12.5 Power Circuit - 3 Phase





C71-5610611-N07

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File: VCCP		
Size	Document Number: Acer SharkBay	Rev: 1.0
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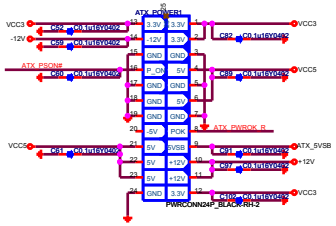
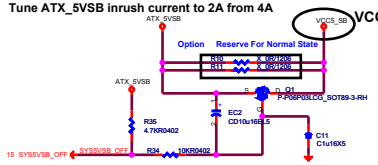
12 Pin ATX Power Connector



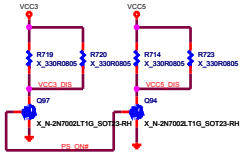
5VSB Power Switch

Tune ATX_5VSB inrush current to 2A from 4A

VCC5_SB Trace Width 80mils

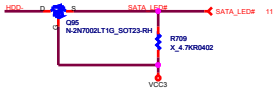


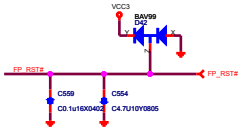
VCC3、VCC5 Discharge Schematic

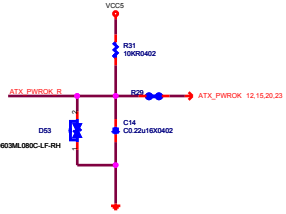


Acer Front Panel Connector

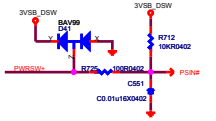
HDD LED





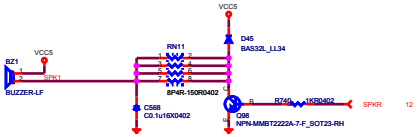


Power Button

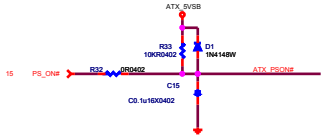


Power LED

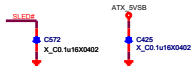
Buzzer Circuit



ATX Power On



Cap For EMI



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Title: ATX/F_Panel/EMI/LED

Size	Document Number	Rev
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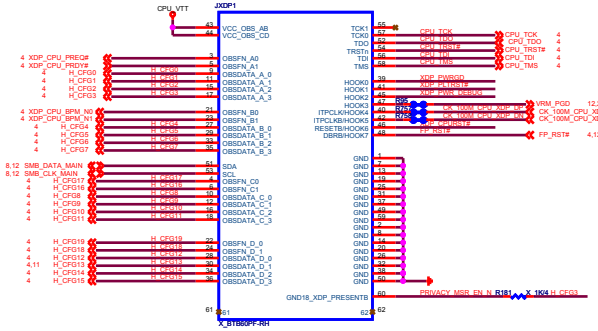
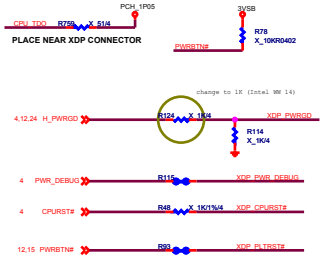
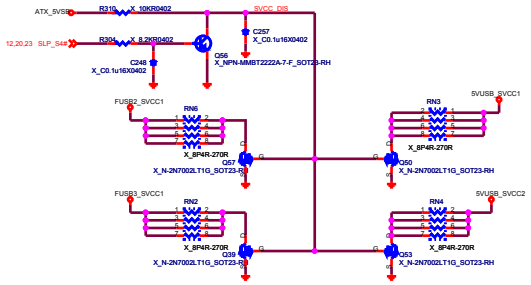
Reserve debug port 5020





NOTE:MP JXDP1 remove and footprint change to 2X30_XDP_CONN_T for printing ink cover

USB power discharge circuit



NOTE:FUSB2_SVCC2 need reserve discharge circuit if have leakage

MSI MICRO-START INT'L CO.,LTD

Title: CPU/PCH XDP&USB PW-Discharge

Size	Document Number	Rev
	Acer SharkBay	1.0

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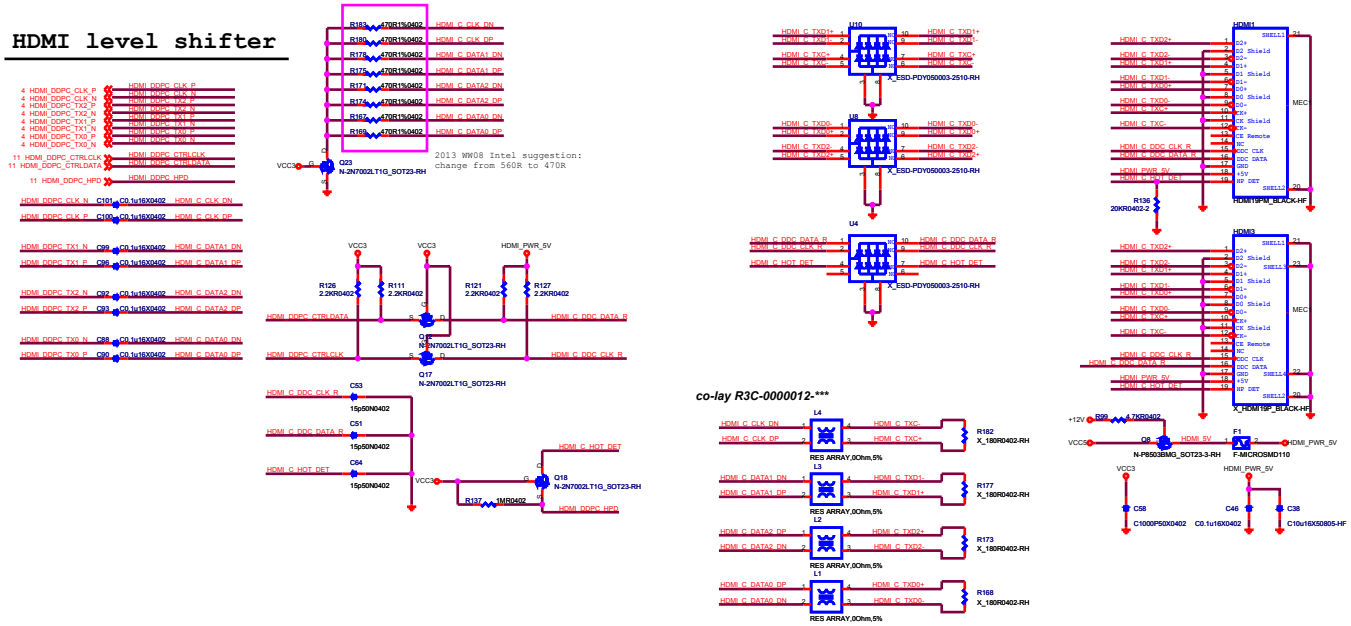
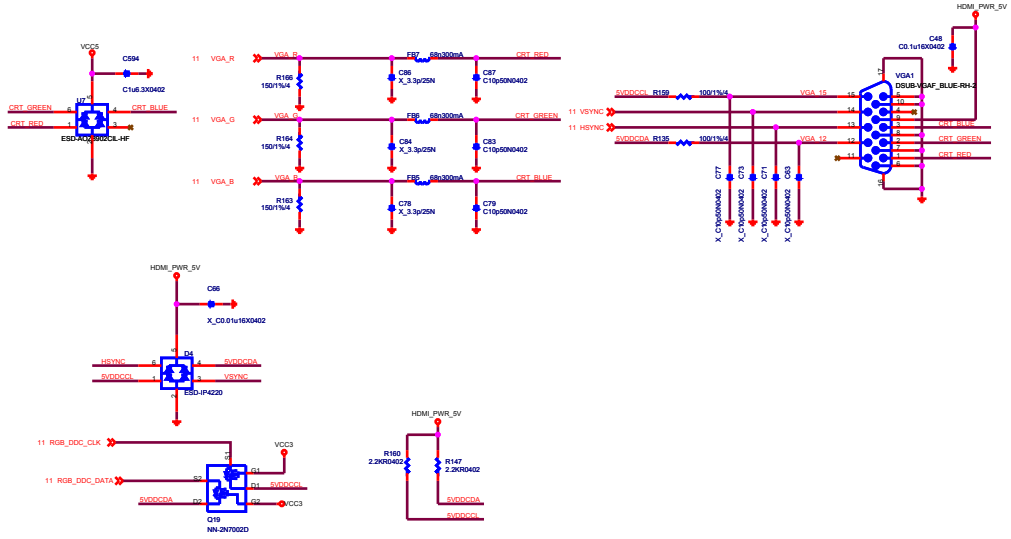
HDMI level shifter



co-lay R3C-0000012-***

MSI	MICRO-START INT'L CO.,LTD	
Title: HDMI		
Size	Document Number: Acer SharkBay	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 28 of 34	



MSI MICRO-STAR INT'L CO.,LTD

Title: VGA

Size: Document Number: Acer SharkBay Rev: 1.0

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Manual Parts

PCB

PCB

P31-0786910-G37
P31-0786910-E48

XU1_X2
X_CPU RETENTION BACKPLATE

U3_X1
MEC1
MEC2
HS-0401634-RH

XU1_X1
CPU SOCKET

CPU_PLATE

Simulation

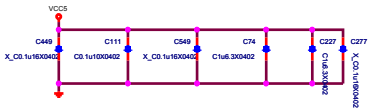
SIP1
SIP2
X_PIN1*2
X_PIN1*2

VBAT-S1
BAT-BCR2032P-RH

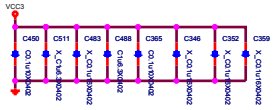
BIOS_ROM

M31-25Q6443-W03
M31-25L6452-M24

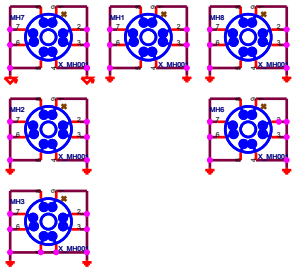
For EMI



For Moat CAP



Mounting Holes



Optics Orientation Holes

Optical Fiducial Marks-120

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Manual & Option Parts

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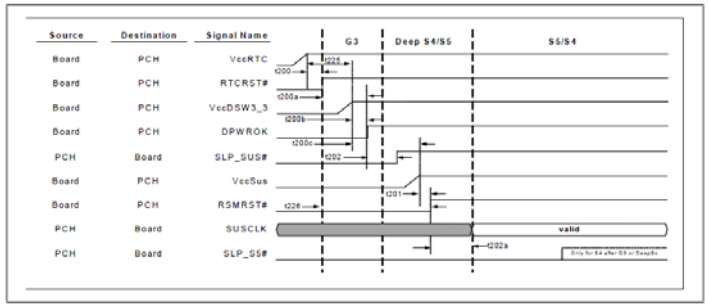
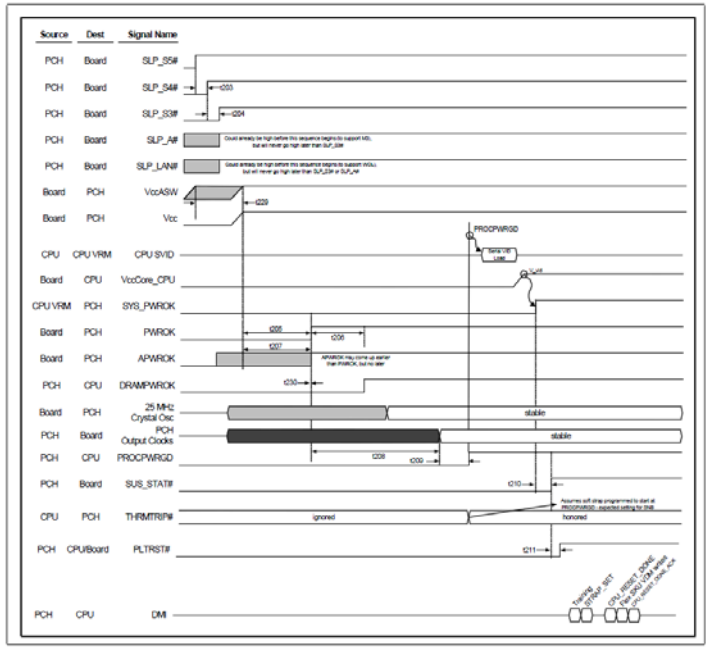
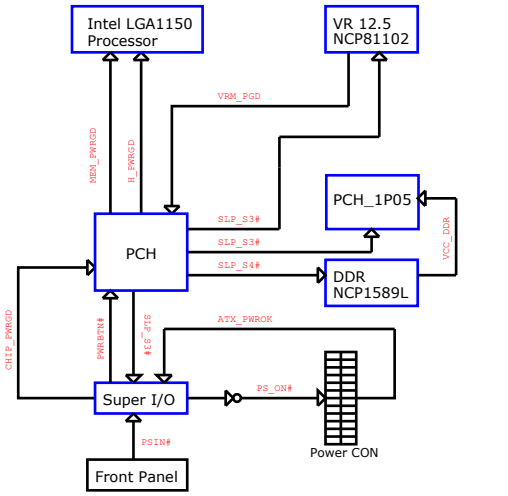
G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



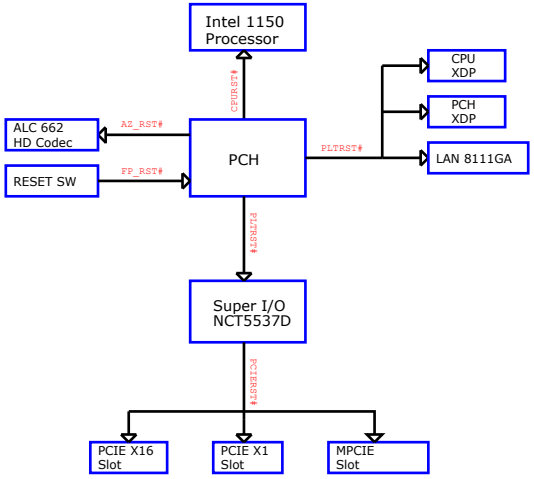
S5 to S0 Timing Diagram



PWROK MAP



RESET MAP



G3-S5

- 3VSB_DSW
- PCH_DPWROK
- SLP_SUS#
- /SYS5VSB_OFF
- 5VSB
- 3VSB
- RSMRST#

S5-S0

- 12V
- 5V
- 3.3V
- 5VDRV1
- VCC1_5REF
- DDR_EN
- VCC1_5
- VCC_DDR
- PCH_1P05
- CHIP_PWRGD
- MEM_PWRGD
- H_PWRGD
- VCCCP
- PCH_SYSPWROK
- SUS_STAT#
- PLTRST#

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Reset/Pwrok/PON

Acer SharkBay

Rev 1.0

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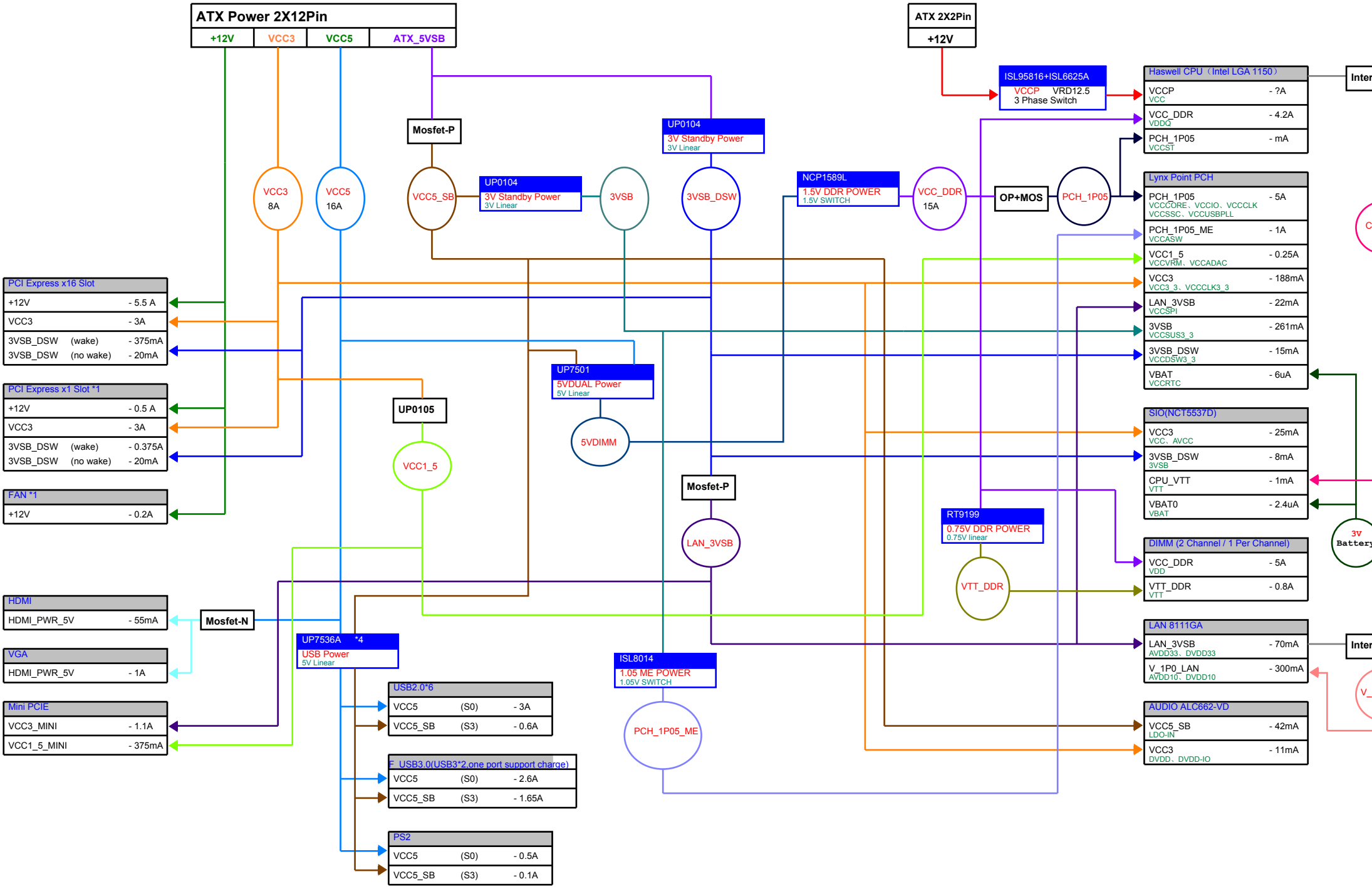


Figure 32-2. Platform Power Map

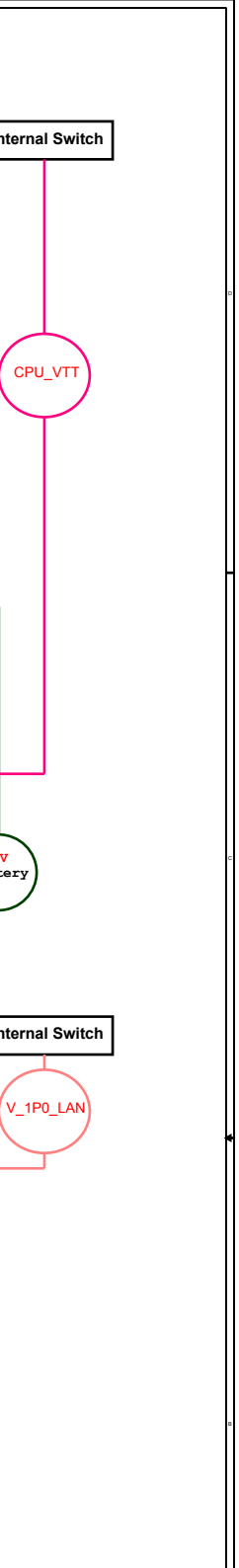
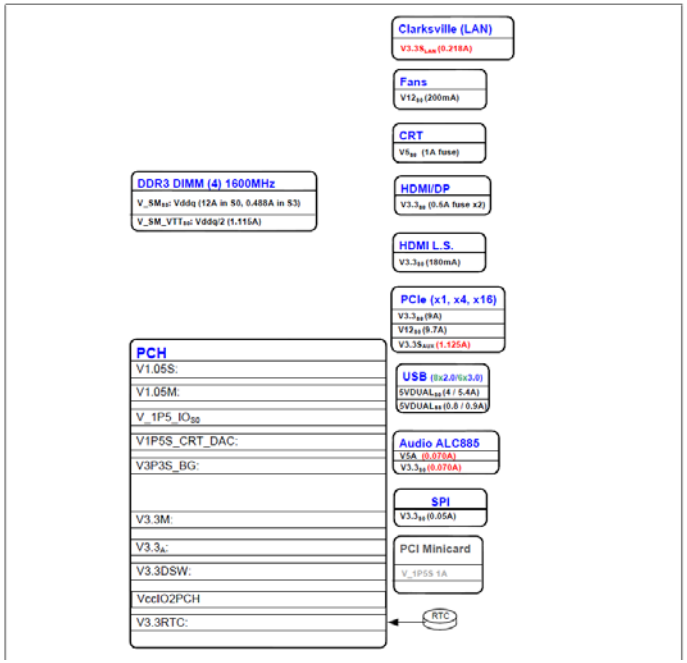

nternal Switch
CPU_VTT
nternal Switch
V_1P0_LAN

Figure 32-2. Platform Power Map



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wer Map

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PCH

GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BMBUSY#	I/O	Main	3.3V	GPI	BM_BUSY#
GPIO[1]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO1
GPIO[2]	PIRQE#	I/O	Main	5V	GPI	SPI_WP#_PCH
GPIO[3]	PIRQF#	I/O	Main	5V	GPI	SMI#
GPIO[4]	PIRQG#	I/O	Main	5V	GPI	PCH_GPIO4
GPIO[5]	PIRQH#	I/O	Main	5V	GPI	PCH_GPIO5
GPIO[6]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO6
GPIO[7]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO7
GPIO[8]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO8
GPIO[9]	OC5#	I/O	Resume	3.3V	Native	USB_OCP#5
GPIO[10]	OC6#	I/O	Resume	3.3V	Native	USB_OCP#6
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	PCH_SMBALERT#
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	Native	LAN_DISABLE#
GPIO[13]	Unmuxed	I/O	Resume	3.3V	GPI	PCH_GPIO13
GPIO[14]	OC7#	I/O	Resume	3.3V	Native	MINI_PWRON
GPIO[15]	Unmuxed	I/O	Resume	3.3V	GPO	MINI_PWRON2
GPIO[16]	SATA4GP	I/O	Main	3.3V	GPI	PCH_GPIO16
GPIO[17]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO17
GPIO[18]	PCIECLKRQ1#	I/O	Main	3.3V	Native	ONE_KEY_DET
GPIO[19]	SATA1GP	I/O	Main	3.3V	GPI	PCH_GPIO19
GPIO[20]	PCIECLKRQ2#	I/O	Main	3.3V	Native	PCIECLKREQ2#
GPIO[21]	SATA0GP	I/O	Main	3.3V	GPI	PCH_GPIO21
GPIO[22]	SCLOCK	I/O	Main	3.3V	GPI	PCH_GPIO22
GPIO[23]	LDRQ1#	I/O	Main	3.3V	Native	LDRQ1#
GPIO[24]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO24
GPIO[25]	Unmuxed	I/O	Resume	3.3V	Native	PCH_GPIO25
GPIO[26]	Unmuxed	I/O	Resume	3.3V	Native	PCH_GPIO26
GPIO[27]	Unmuxed	I/O	DSW	3.3V	GPI	LAN_WAKE#
GPIO[28]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO28
GPIO[29]	SLP_WLAN#	I/O	Resume	3.3V	Native	SLP_WLAN#
GPIO[30]	SUS_PWRDN_ACK/SUS_WARN#	I/O	Resume	3.3V	GPI	PCH_SUSWARN#
GPIO[31]	Unmuxed	I/O	DSW	3.3V	GPI	PCH_GPIO31
GPIO[32]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO32
GPIO[33]	HDA_DOCK_EN#	I/O	Main	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	STP_PCI	I/O	Main	3.3V	GPI	STP_PCI#
GPIO[35]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO35
GPIO[36]	SATA2GP	I/O	Main	3.3V	GPI	PCH_GPIO36

PCH

GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name
GPIO[37]	SATA3GP	I/O	Main	3.3V	GPI	PCH_GPIO37
GPIO[38]	SLOAD	I/O	Main	3.3V	GPI	PCH_GPIO38
GPIO[39]	SDATAOUT0	I/O	Main	3.3V	GPI	PCH_GPIO39
GPIO[40]	OC1#	I/O	Resume	3.3V	Native	USB_OCP#1
GPIO[41]	OC2#	I/O	Resume	3.3V	Native	USB_OCP#2
GPIO[42]	OC3#	I/O	Resume	3.3V	Native	PCH_GPIO42
GPIO[43]	OC4#	I/O	Resume	3.3V	Native	USB_OCP#4
GPIO[44]	PCIECLKRQ5#	I/O	Resume	3.3V	Native	PCIECLKREQ5#
GPIO[45]	PCIECLKRQ6#	I/O	Resume	3.3V	Native	DEPOP_GPIO
GPIO[46]	PCIECLKRQ7#	I/O	Resume	3.3V	Native	PCH_GPIO46
GPIO[48]	SDATAOUT1	I/O	Main	3.3V	GPI	COM_GPIO1
GPIO[49]	SATA5GP	I/O	Main	3.3V	GPI	PCH_GPIO49
GPIO[50]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO50
GPIO[51]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO51
GPIO[52]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO52
GPIO[53]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO53
GPIO[54]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO54
GPIO[55]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO55
GPIO[57]	Unmuxed	I/O	Resume	3.3V	GPI	PCH_GPIO57
GPIO[58]	SML1CLK#	I/O	Resume	3.3V	Native	SMLINK1_CLK
GPIO[59]	OC0#	I/O	Resume	3.3V	Native	USB_OCP#0
GPIO[60]	SML0ALERT#	I/O	Resume	3.3V	Native	PCH_SML0ALERT#
GPIO[61]	SUS_STAT#	I/O	Resume	3.3V	Native	PCH_GPIO61
GPIO[62]	SUSCLK	I/O	Resume	3.3V	Native	SUS_CLK
GPIO[63]	SLP_S5#	I/O	Resume	3.3V	Native	SLP_S5#
GPIO[64]	CLKOUTFLEX0	I/O	CORE	3.3V	Native	NC
GPIO[65]	CLKOUTFLEX1	I/O	CORE	3.3V	Native	NC
GPIO[66]	CLKOUTFLEX2	I/O	CORE	3.3V	Native	NC
GPIO[67]	CLKOUTFLEX3	I/O	CORE	3.3V	Native	SIO_48M
GPIO[68]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO68
GPIO[69]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO69
GPIO[70]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO70
GPIO[71]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO71
GPIO[72]	Unmuxed	I/O	DSW	3.3V	Native	PCH_GPIO72
GPIO[73]	PCIECLKRQ0#	I/O	Resume	3.3V	Native	PCH_GPIO73
GPIO[74]	SML1ALERT#	I/O	Resume	3.3V	Native	PCH_SML1ALERT#
GPIO[75]	SML1DATA	I/O	Resume	3.3V	Native	SMLINK1_DATA

SIO(NCT5537D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO4	GP04	Input	reserve pull high
GPIO20	KBDATA	Input	Keyboard data in
GPIO21	KBCLK	Output	keyboard clcok out
GPIO22	MSDATA	Input	Mouse data in
GPIO23	MSCLK	Output	Mouse clcok out
GPIO24	SIO_GPIO24	Output	pull high
GPIO25	SMI#	Input	SIO SMI# generation

DDR-III DIMM Config

DEVICE	ADDRESS(SA1:SA0)	CLOCK
DIMM 1	10	MEM_MB_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 2	00	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1

GPIO25	SMI#	Input	SIO SMI# generation
GPIO26	NC	NC	NC
GPIO41	SMLINK1_CLK	Output	SM bus link
GPIO42	SMLINK1_DATA	Output	SM bus link
GPIO54	SLP_SUS#	Input	DSW signal which received from PCH
GPIO56	PWR_LED	Output	LED drive signal which shows the system state
GPIO57	NC	NC	NC

SIO(NCT5537D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO75	RSTOUT0#	Output	PCIE reset signal
GPIO76	RSTOUT1#	Output	LPC_Debug card reset signal
GPIO80	CTSA#	Input	COM port signal
GPIO81	DSRA#	Input	COM port signal
GPIO82	RTSA#	Output	COM port signal
GPIO83	DTRA#	Output	COM port signal
GPIO84	SINA	Input	COM port signal
GPIO85	SOUTA	Output	COM port signal
GPIO86	DCDA#	Input	COM port signal
GPIO87	RIA#	Input	COM port signal

Ver.0B history (changed to 0B from 0A)

1. Power solution
<1>VRM
R53 /R61 /R81 /R50 /R52 /R65 Change to NC
R89 Change to 3.48K;R24 Change to 8.2K ;C7 Change to 0.22UF;R58 Change to 82k
<2>VCCM
C224 Change to 470P;R271 Change to 2.43K,
CHOKE9 Change to 0.5u/40A(P/N:L04-05A7211-L65)
<3>5V
R207 Change to 25.5K;R218 Change to 21K
EC8/ EC13 Change to 560u(P/N:C71-5610611-M07)
<4>3V
R214 Change to 19.1K;R215 Change to 13K
EC16 Change to 560u *2 (Add 1pcs) P/N:C71-5610611-M07
2. CPU loading
RT1 Change to 100K ohm(PN: R51-0104713-M05)
R57 Change to 11.3k ohm(P/N: R11-1132712-W08)
3. Add D50,For Memory power
4. For card reader,(USB2.0 signal) USB 6 /7 and USB 10 /11 by Swap
5. Audio
<1>Stuff R698,R721
<2>Reserve C596
<3>R617,R636 Change to 75 Ohm
<4> Stuff R698; Reserve R668
6. VCC_DDR power change to upi534
7. R169/R167/R174/R171/R175/R178/R180/R183 680 Ohm Change to 560 Ohm
8. Reserve SLP_S4# To U35.8
9. Front USB3.0 header, RX+/RX- and TX+/TX- modify signal
10. Front USB3.0 header,DP pin Change to Reserve
11. USB power discharge circuit Change to Reserve
12. MLCC SIZE, C11-2267315-M09(0603) Change to C11-2267014-M09(0805)
13. LAN Connector ,pin21 and pin22 Swap
14. R103 change to Reserve,For VCC3 Leakage voltage
15. Add jumper setting. For BIOS_WP
16. LAN Power. PCH_GPIO31 Stuff. SLP_LAN# Reserve
17. R446 and R447 Change to Reserve. Add R764(10K). For LAN_3VSB Leakage voltage
18. Reserve SLP_S4# delay circuit. U26 and U29 EN pin use USB_S4# control (page20)
19. Stuff EC31
20. ME jumper. Reserve GPIO72 control
21. Reserve LAN_ACT_LED3 1.
22. unmounts R413 , mount R360. For GPIO57 pull low
23. CHANGE CB Add 0 ohm RESISTOR , R772
24. R764 size 0402 Change to 0603. P/N: R11-0103033-W08.
25. Front USB3.0 header,DP pin Change to Reserve
26. R772 un-mount, R761 stuff

Ver.1.1 history (changed to 1.1 from 1.0)

1. F_USB2 protect diode modify Power separate,
Picture 1(old V1.0) change to Picture 2(new V1.1)
Picture 1(old V1.0)

Picture 2(new V1.1)

2. ATX_POWER1 change to P/N: N93-12M0091-M06. For the positioning column

3. F_USB3.0 header,P/N (Vendor P/N) : N32-2101091-M06 (BH20NQ3BAFJ14) change to
P/N (Vendor P/N) : N32-2101151-M06 (BH20NQ3GAFL14)
4. Modify BOM. Remove BIOS write protect and CIR header
5. Modify BOM. Add Rear DP port

Ver.1.0 history (changed to 1.0 from 0B)

1. LPC bus. PCH side Fales resistance change to 43 ohm ;
SIO side Fales resistance change to 0 ohm
2. SPI_DEBUG change to P/N: N31-2071101-M04
3. System fan 3pin change to 4pin
3. VGA port N51-15F0871-M06 Factories have reported : processing length pin problems exist; V1.0 change to
P/N: N51-15F0801-M06
4. Switch power high/low side Footprint change to SOT669_COLAY
5. USB3.0 BOX HEADER modify
N31-2101211-M06 change to N32-2101091-M06
6. For Acer IOAC function modify
7. BIOS ROM
B85 ROM:16M size; P/N: N31-2512853-W03
Z87 ROM:8M size; P/N: N31-25Q6433-W03
8. SATA4
B85 ROM:BLACK; P/N: N5N-07M2081-L06
Z87 ROM: WHITE; N5N-07M1881-L06
9. ME_DIS , change Reserve PCH_GPIO24
10. Power solution
CORE
R84=115K
U1/ ISL95816, Pin15 (ISUMP Pin) Add 4.7M ohm to GND

GSB
R280=17.4K
R271=24.9K
(OCP=35.7A)

VCC3
R215=10K
R214=31.6K
(OCP=25.44A)

VCC5
R218=15K
R207=16K
(OCP=41A)
11. SIO NCT5533D/NCT5537D Cancel Co-lay; stuff NCT5537D
12. In deep S5 support USB charge, power modify to ATX_5VSB
Modify charge spec S3 state support DCP mode
13. USB_OC#2 modify

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