LV115 Schematics
Skylake-U

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: LV115 SKL-U	Rev: -1
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Project code:
LV115SK:4PD08B010001
LV114SK:4PD08A010001
PCB P/N: 15277/15309
Revision: SA
IO Board:

LV115/LV114 SKL-U Block Diagram

32.768KHz 24MHz

X7901 27MHz

25MHz

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

DDR4 SO-DIMM x1 13 — DDR4 1866/2133MHz Channel A
DDR4 MD x4 pcs 14 — DDR4 1866/2133MHz Channel B
Left side USB 3.0 SKT x2 — USB3.0 x 2
Right side USB 2.0 SKT x — USB2.0 x 1

Intel CPU
Skylake U
28W (UMA only)
15W (UMA&DIS)

SKL PCH-LP
10 USB 2.0/1.1 ports
6 USB 3.0 ports
High Definition Audio
3 SATA ports
6 PCIE ports
LPC I/F
ACPI 5.0

SM Bus, PEG x4 — AMD GPU EXO Pro S3 18W 76~80 — VRAM x4 GDDR3 / 1.5V 900MHz 81~84
PCIe x 1 — LAN 10/100/1000 RealTek RTL8111H 30 — RJ45 Conn.
PCIe x 1, USB2.0 x 1 — NGFF WLAN W/ Bluetooth COMBO 61
SATA(Gen3) x 1 — HDD 60
SATA(Gen2) x 1 — ODD 61
LPC BUS — LPC Debug Port 65
SPI — Flash ROM 16MB 25
SMBUS — Thermal NUVOTON NCT7718W 26
SMBUS — 1ST Battery
KBC NPCE285 24
PS2 — Clickpad 62
PWM — Int. KB
PWM — FAN 26
I2C

14.0"/15.6" (FHD) — eDP
HDMI V1.4b 57 — HDMI
CRT — Travis — eDP
Camera (HD) 52 — USB2.0 x 1
D-MIC
2CH SPEAKER (2CH 2W/4ohm)
Universal Jack — MIC_IN/GND, HP_R/L 29
HDA CODEC Realtek ALC3240 27 — HDA
SD Card Slot SDR50 SSD/MMC — CardReader — USB2.0 x 1

PCB	Halogen PN	No Halogen PN
LV115SK MB	15277	15309
LV115SK BTN BD	15902	15939
LV115SK AUDIO IO BD	15903	15940
LV115SK ODD BD	15904	15941

CHARGER BQ24780RUYR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51275CRUKR 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5

CPU Core Power NCP81208MNTXG 46~50
NCP81382MNTXG x 2
NCP81382MNTXG(23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+V_VCCGTUS_VR (23e only)
DCBATOUT	+VCCSA_VR

DDR3L SUS TPS51716RUKR 51

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU VCCIO 0.975V RT8068AZQWID 52

INPUTS	OUTPUTS
3D3V_S5	+VCCIO_VR

CPU VCCPRIM_CORE 0.95V TPS22961DNYT 52

INPUTS	OUTPUTS
3D3V_S5	VCCPRIM_CORE

CPU DCDC-V1D00A AOZ1268QI 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V TLV70215DBVR 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V RT9025-25ZSP 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 G5016KD1U 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

VCCSTG M5938ARD1U

INPUTS	OUTPUTS
1D0V_S5	+V1.00DX 40

VCCST M5938ARD1U

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU 40

EOPIO/EDRAM (23e) TPS22961DNYT 52

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA G5016KD1U 86

INPUTS	OUTPUTS
3D3V_S0 3D3V_S0	+V_EDRAM_VR +V_EOPIO_VR

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Title: Block Diagram
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Main Func = CPU

(Blanking)

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Title: Reserved

Size: A3 | Document Number: LV115 SKL-U | Rev: -1

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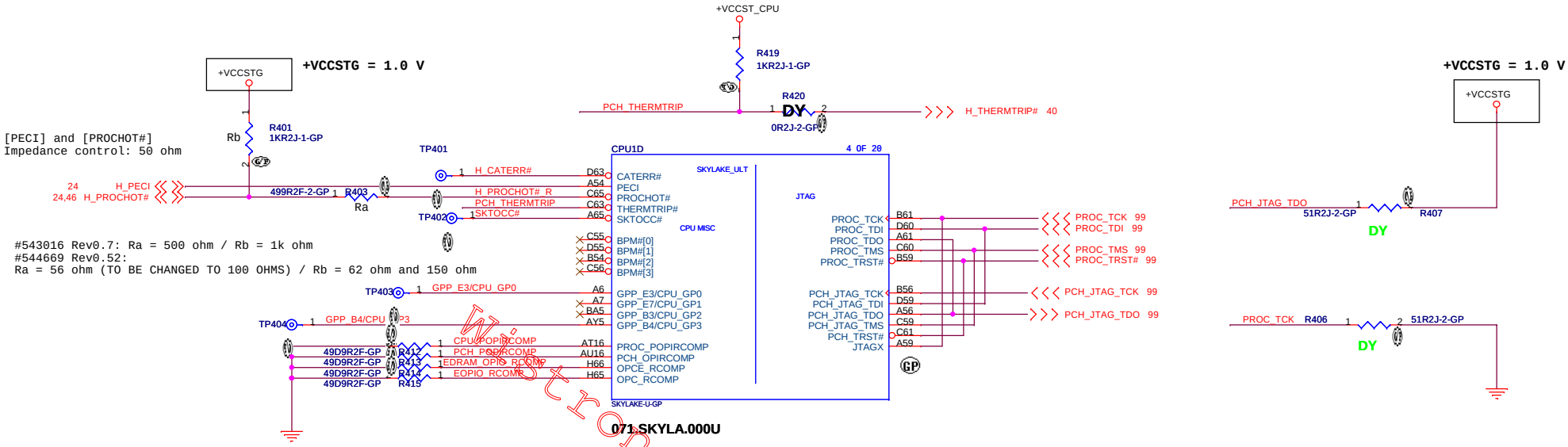
Main Func = CPU

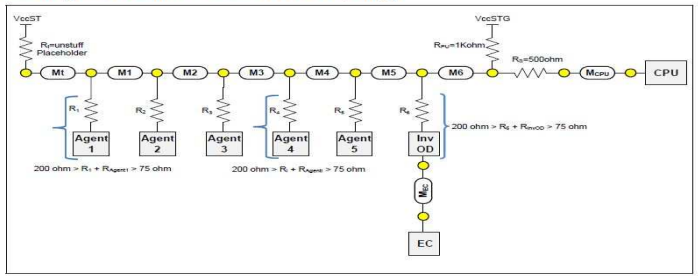


071.SKYLA.000U

CPU BOM CTRL

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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Title: CPU (JTAG/CPU SIDE BAND)

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Main Func = CPU

DDR4 ball type: Interleaved Type

M_A_BG1
M_VREF_DQ_DIMM0
Reserve Testpoint only

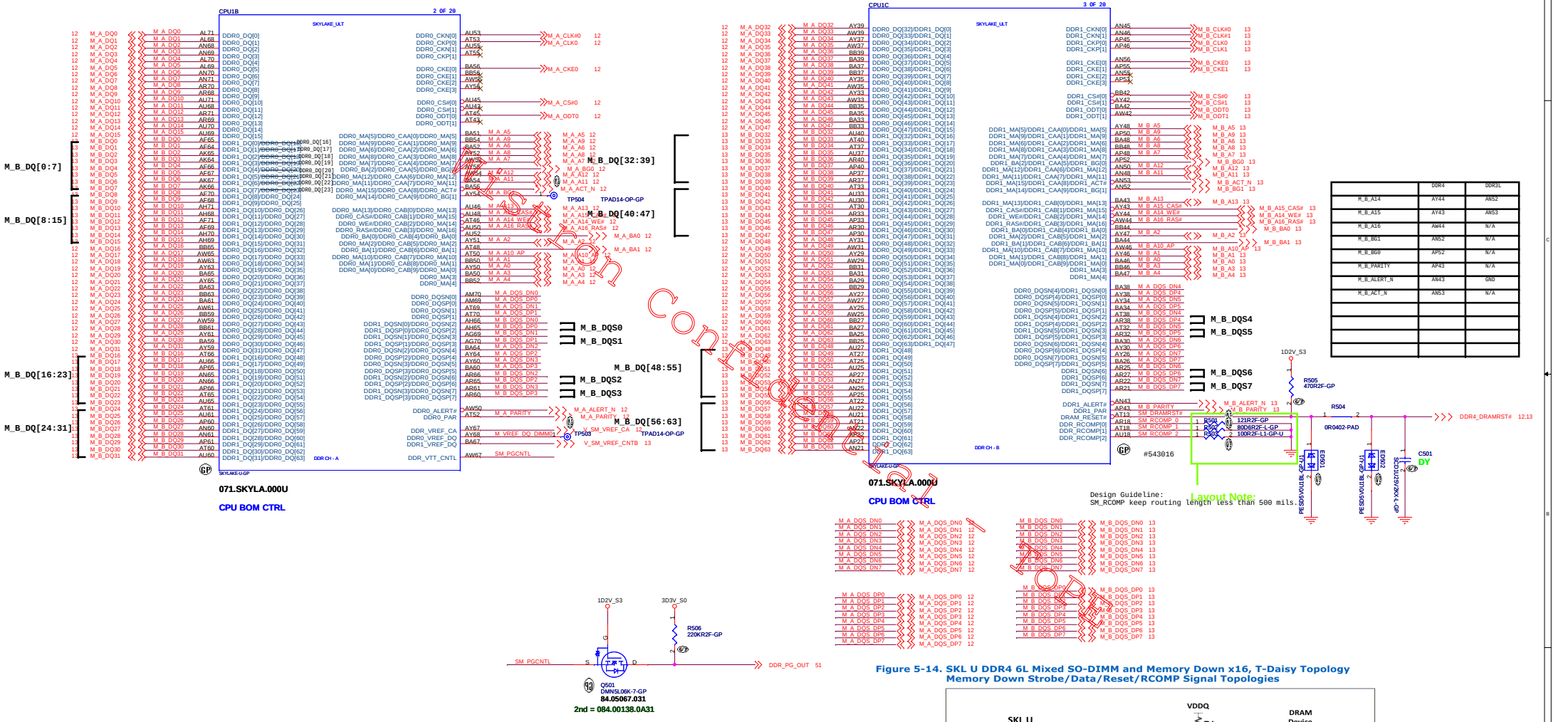
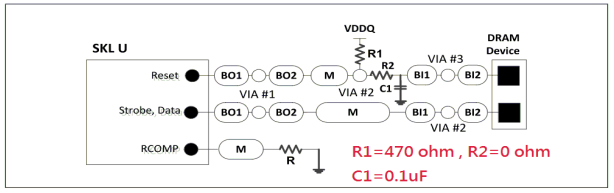


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



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Title: CPU (DDR)

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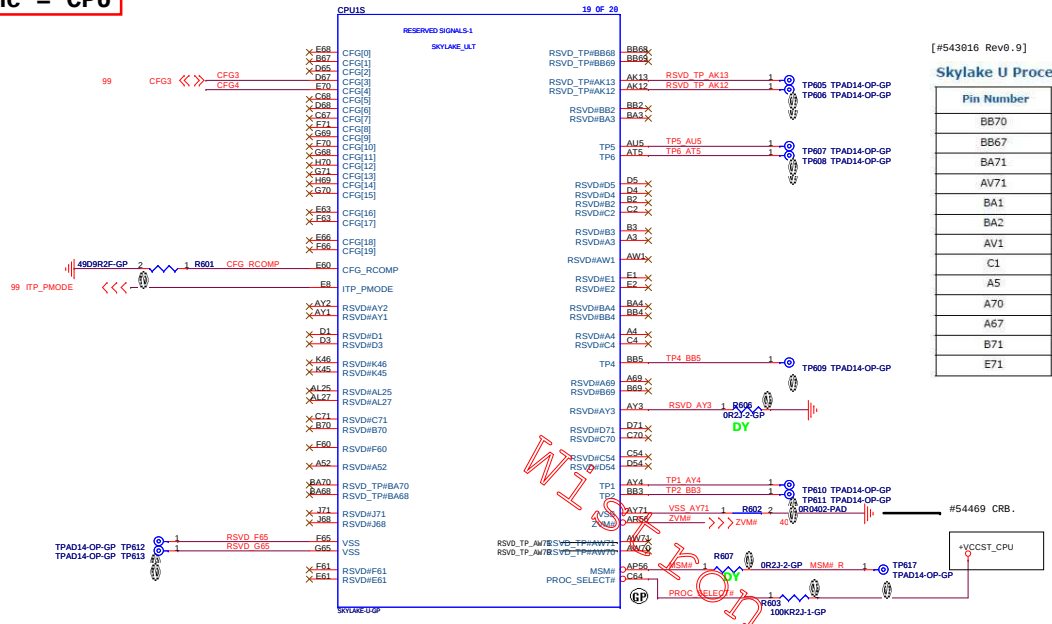
Main Func = CPU

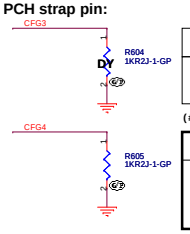


[#543016 Rev0.9]

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

PCH strap pin: **071.SKYLA.000U** **CPU BOM CTRL**



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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Title: CPU (RESERVED)
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Main Func = CPU

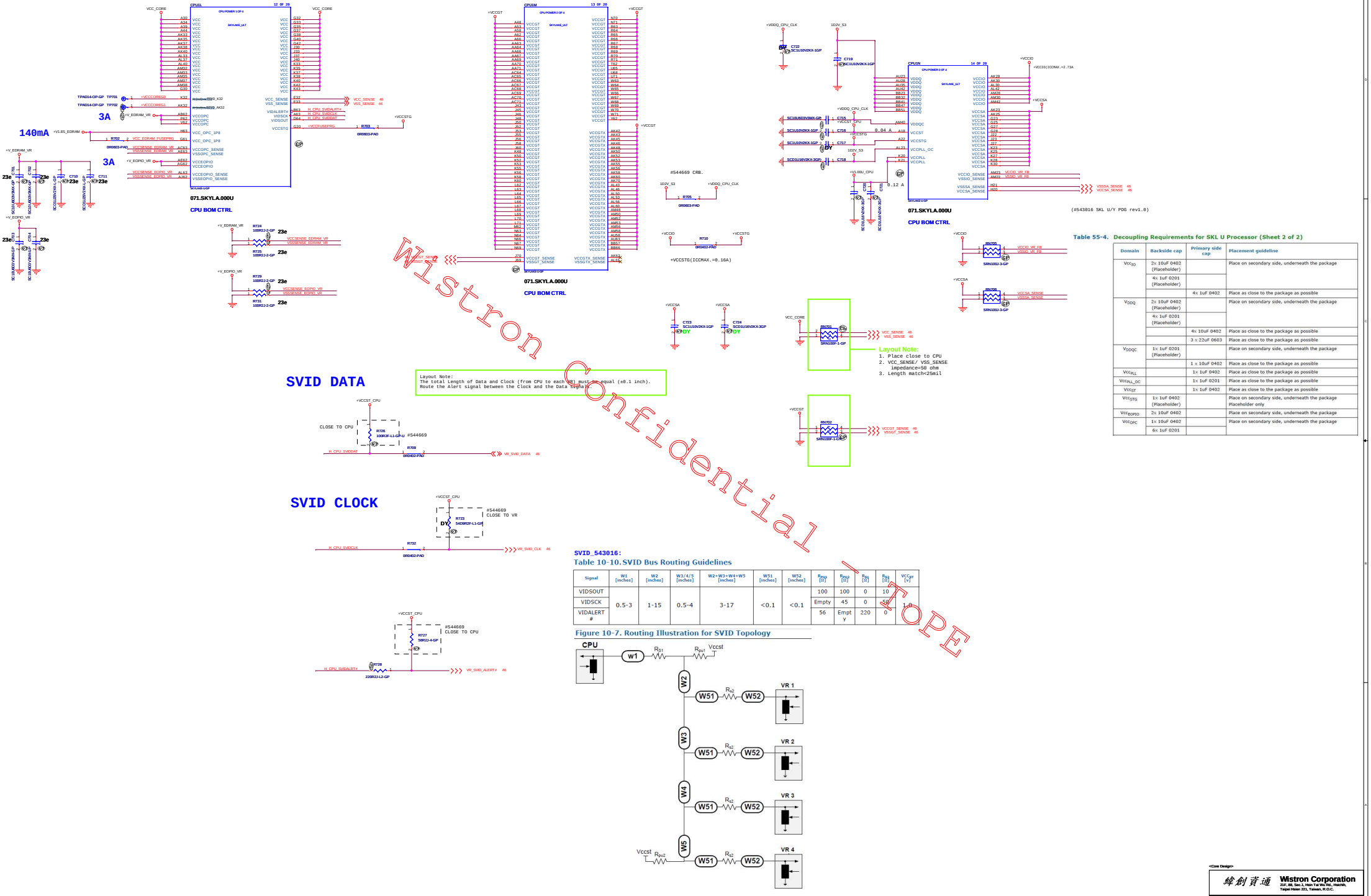

Table 55-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
V_{CCIO}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 1uF 0402	Place as close to the package as possible
V_{DDQ}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 10uF 0402	Place as close to the package as possible
		3 x 22uF 0603	Place as close to the package as possible
V_{DDQC}	1x 1uF 0201 (Placeholder)		Place on secondary side, underneath the package
		1 x 10uF 0402	Place as close to the package as possible
V_{CCPLL}		1x 1uF 0402	Place as close to the package as possible
V_{CCPLL_OC}		1x 1uF 0201	Place as close to the package as possible
V_{CCST}		1x 1uF 0402	Place as close to the package as possible
V_{CCSTG}	1x 1uF 0402 (Placeholder)		Place on secondary side, underneath the package Placeholder only
$V_{CCEOPIO}$	2x 10uF 0402		Place on secondary side, underneath the package
$V_{CCEOPIC}$	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

SVID_543016:

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU0} [Ω]	R_{PU1} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{BT} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	56	
VIDALERT#							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology

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Title: CPU(VCC_CORE)

Size: A1 | Document Number: LV115 SKL-U | Rev: -1

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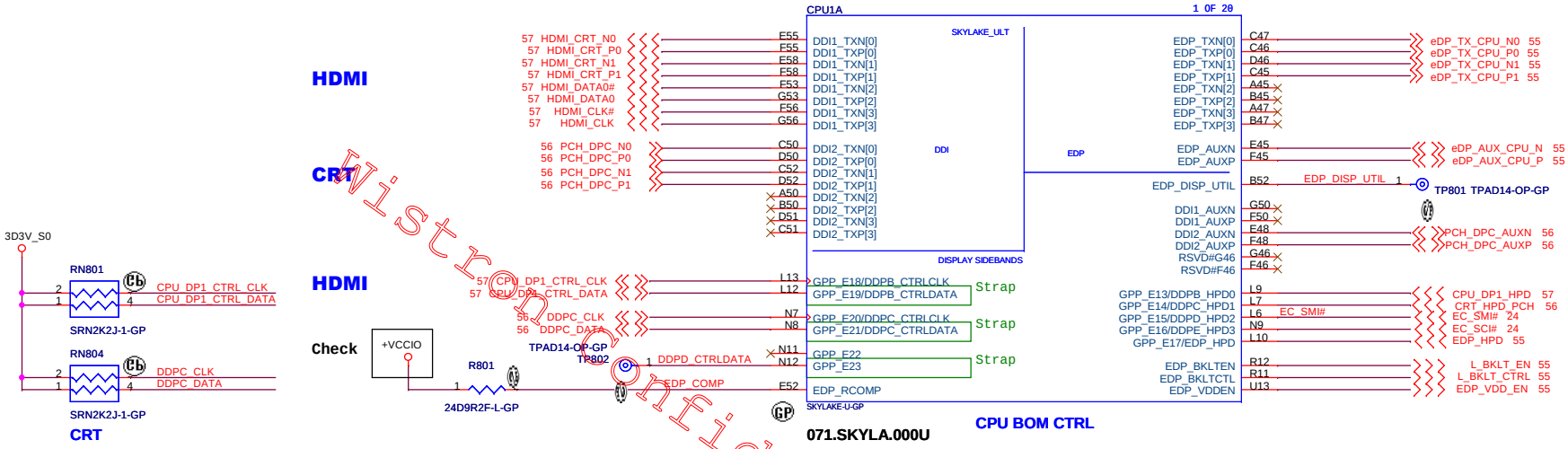
Main Func = CPU



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

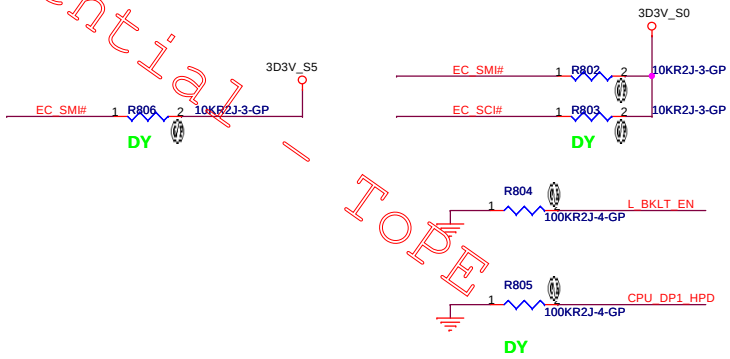
(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.



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Title: CPU_(DISPLAY)

Size: A3 | Document Number: LV115 SKL-U | Rev: -1

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Main Func = CPU

(Blanking)

<Core Design>

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Title: (Reserved)CPU

Size: A3 | Document Number: LV115 SKL-U | Rev: -1

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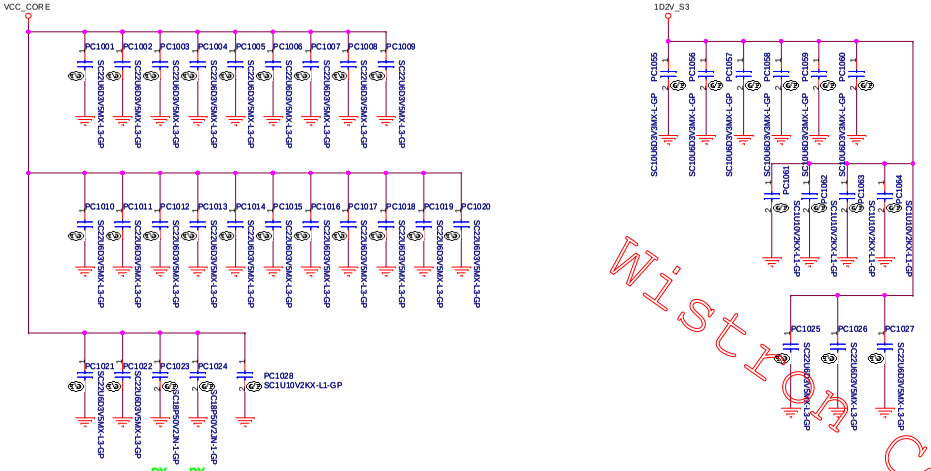
Main Func = CPU

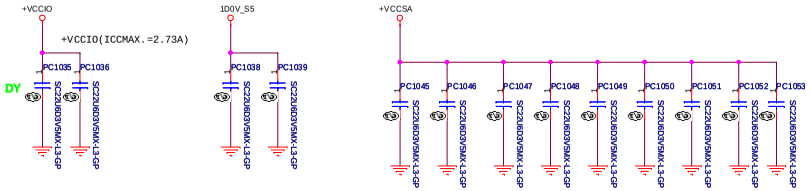
(#543016 PDG)

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A



VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

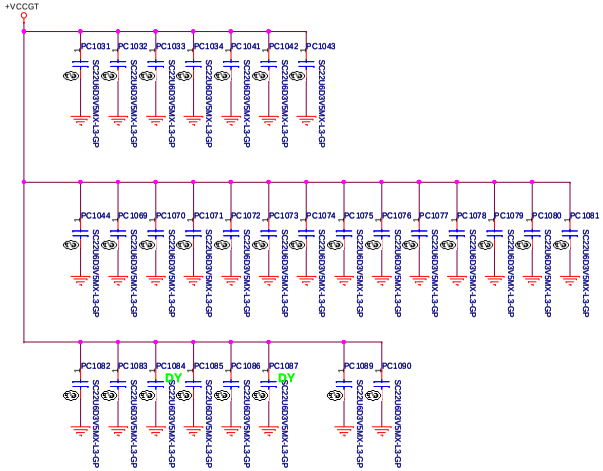


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 10uF 0201		

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Title: CPU (Power CAP1)

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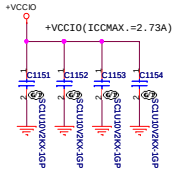
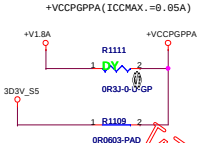
Main Func = CPU

UNSLICED GT

VCCIO



PCH DERIVED RAILS



GTUS

20141114 Alden

+V_VCCGTUS_VR can merge to +VCCGT

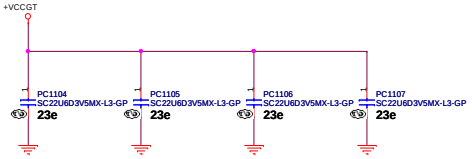
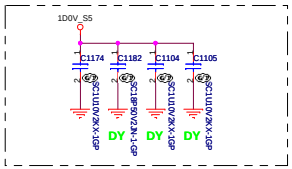
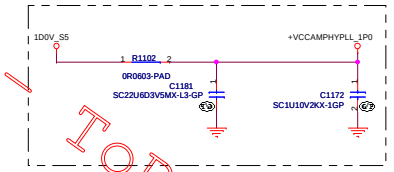
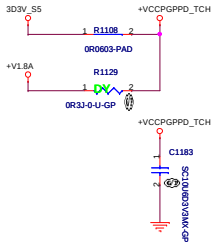


Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		
		(6.3V)[4]	
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible







<Core Design>

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Title: CPU (Power CAP2)

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Main Func = DDR4 On Board with Single Rank

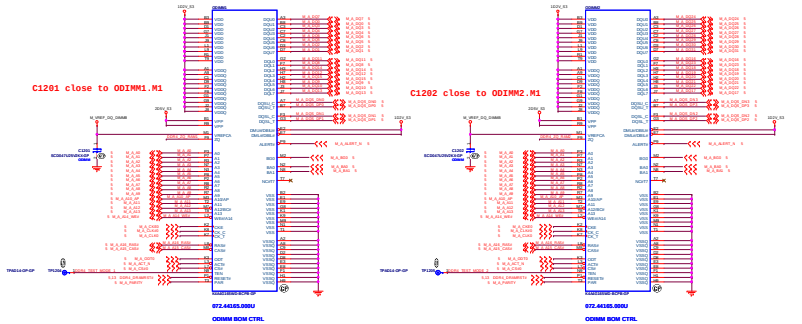


Figure 5-15. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down CLK/CTRL/CKE/CMD Signals Double-T Topology

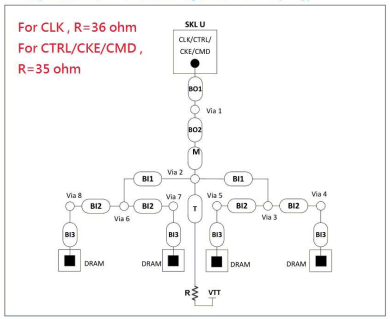
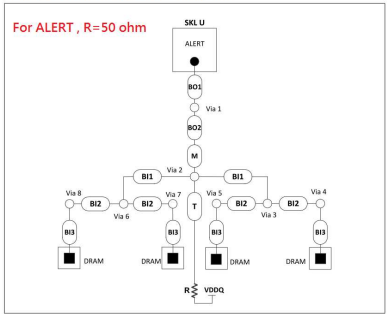


Figure 5-16. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down ALERT Signal Double-T Topology



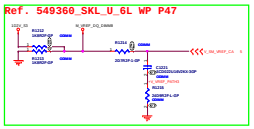
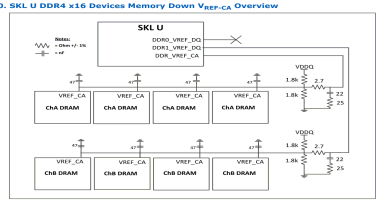
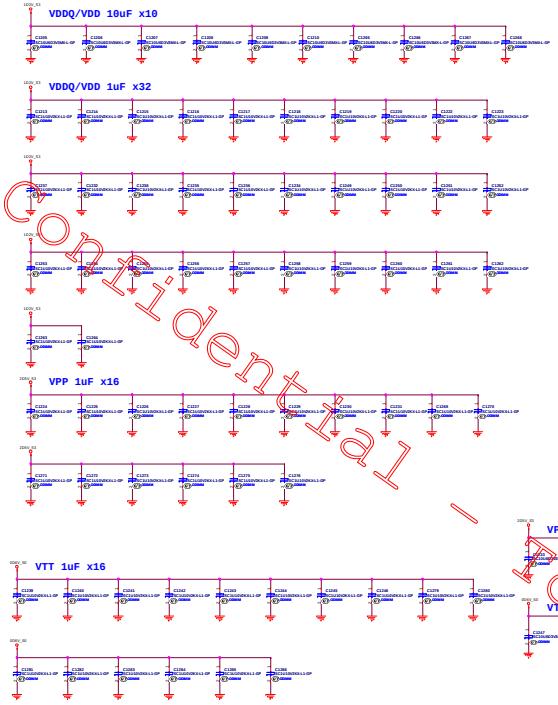


Figure 5-20. SKL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview



DDR4 On Board RAM Power Decouple Cap



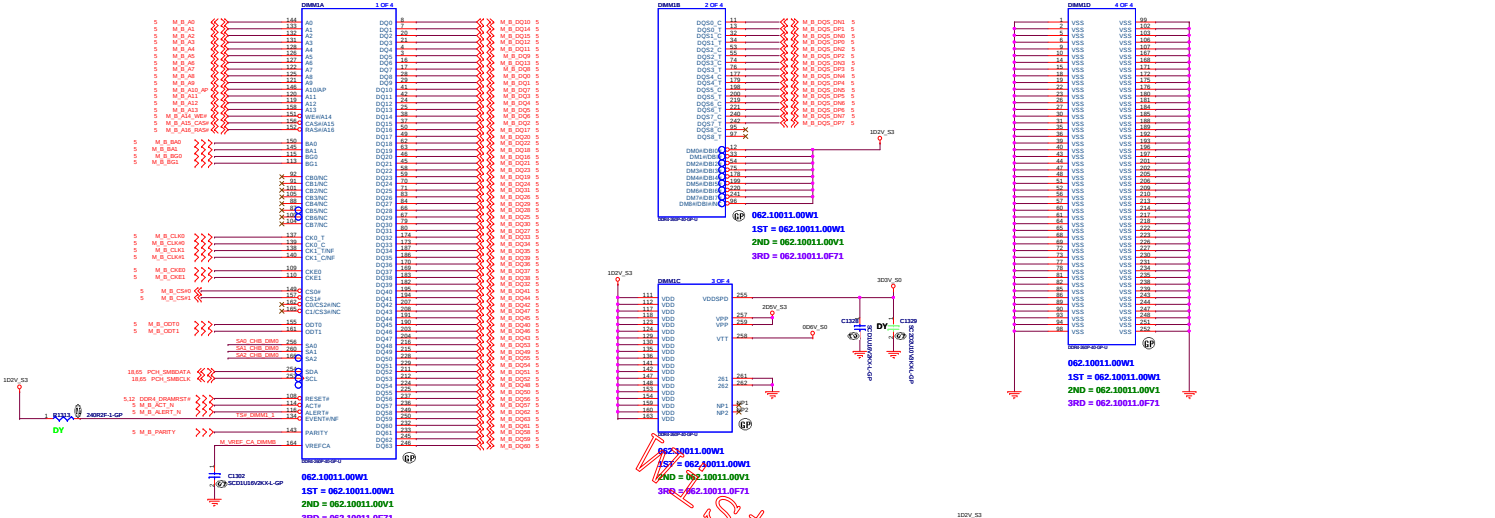
LV115 use 1ch memory down , only need half of Caps

4.23.5 SKL-U DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-55. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty × µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	



20151007 Change DIMM1 SKT PN

Ref. 549360_SKL_U_6L WP P47

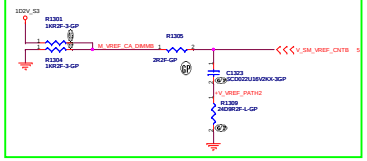
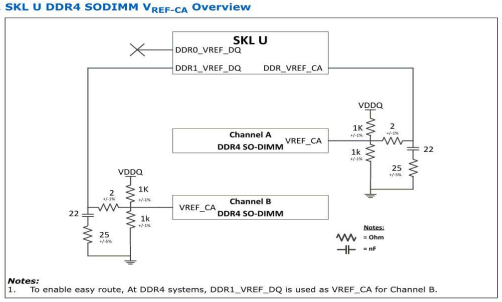


Figure 5-19. SKL U DDR4 SODIMM V_{REF-CA} Overview



Notes:

1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

(Blanking)

<Core Design>

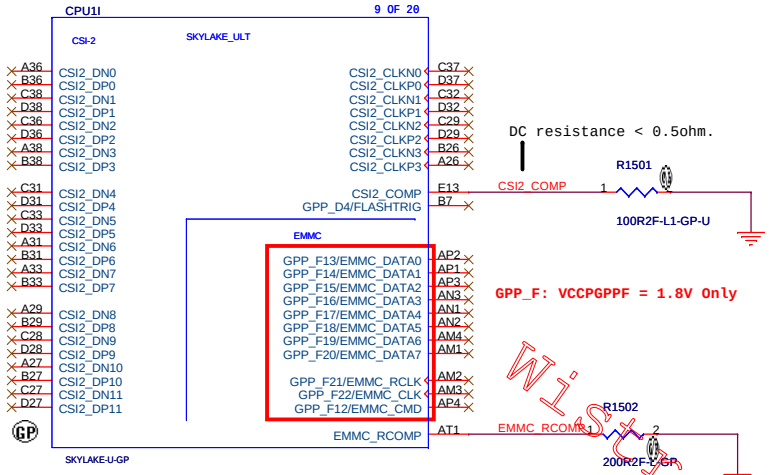
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)SODIMM3_SODIMM4

Size	Document Number	Rev
A4	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 14 of 102

Main Func = PCH



071.SKYLA.000U

CPU BOM CTRL

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

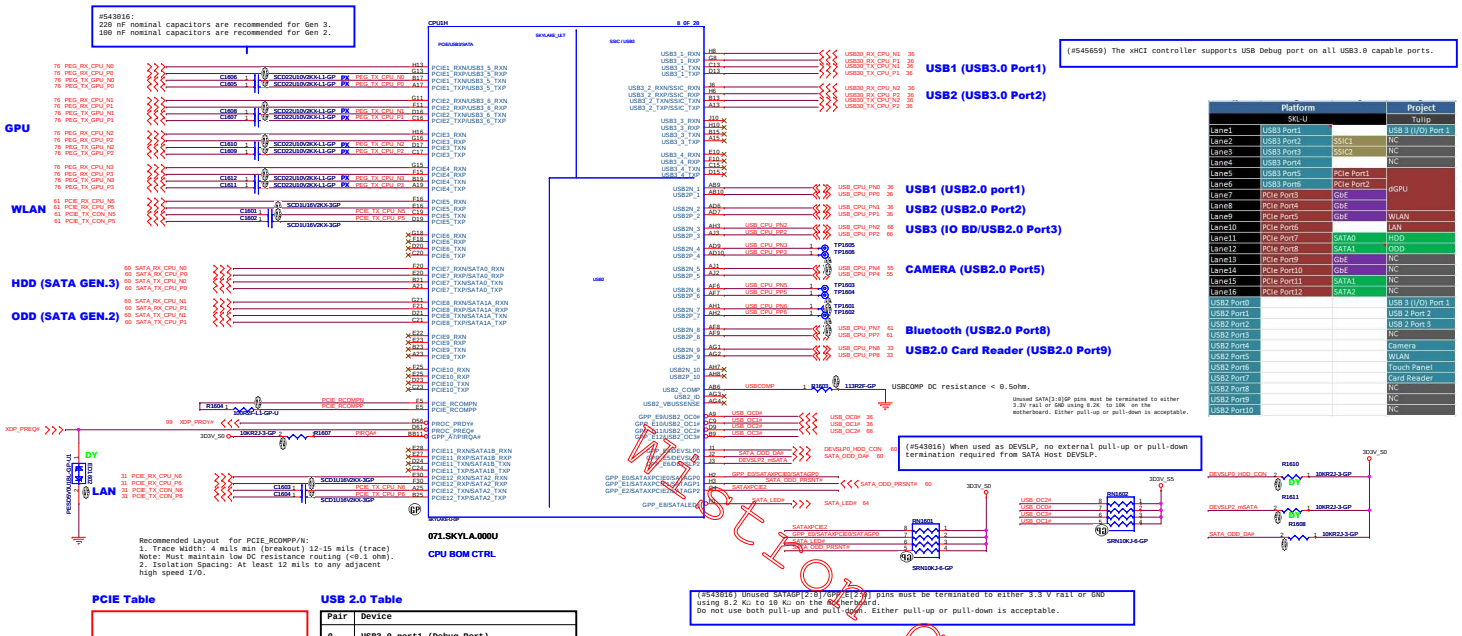
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CS-2/EMMC)

Size: A3 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 15 of 102

Main Func = PCH



(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

Platform SKL-U			Project Tulip
Lane1	USB3 Port1		USB 3 (I/O) Port 1
Lane2	USB3 Port2	SSIC1	NC
Lane3	USB3 Port3	SSIC2	NC
Lane4	USB3 Port4		NC
Lane5	USB3 Port5	PCIe Port1	
Lane6	USB3 Port6	PCIe Port2	dGPU
Lane7	PCIe Port3	GbE	
Lane8	PCIe Port4	GbE	
Lane9	PCIe Port5	GbE	WLAN
Lane10	PCIe Port6		LAN
Lane11	PCIe Port7	SATA0	HDD
Lane12	PCIe Port8	SATA1	ODD
Lane13	PCIe Port9	GbE	NC
Lane14	PCIe Port10	GbE	NC
Lane15	PCIe Port11	SATA1	NC
Lane16	PCIe Port12	SATA2	NC
USB2 Port0			USB 3 (I/O) Port 1
USB2 Port1			USB 2 Port 2
USB2 Port2			USB 2 Port 3
USB2 Port3			NC
USB2 Port4			Camera
USB2 Port5			WLAN
USB2 Port6			Touch Panel
USB2 Port7			Card Reader
USB2 Port8			NC
USB2 Port9			NC
USB2 Port10			NC

Recommended Layout for PCIE_RCOMPP/N:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

PCIE Table

Port	Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	WLAN	
6	N/A	
7	N/A	SATA0 (HDD)
8	N/A	SATA1 (ODD)
9	N/A	
10	N/A	
11	N/A	
12	LAN	

USB 2.0 Table

Pair	Device
0	USB3.0 port1 (Debug Port)
1	USB2.0 Port2
2	USB2.0 Port3 (IOBD)
3	
4	CAMERA
5	
6	
7	Bluetooth
8	USB2.0 Card Reader
9	

20151024 Modify PCIE/USB2.0 Mapping Table

Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

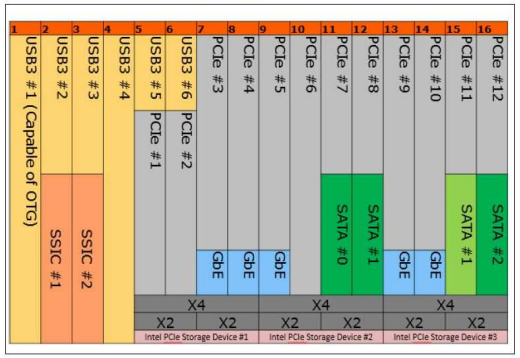


Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Main Func = PCH

3D3V_S5
R1709 10KR2J-3-GP AC_PRESENT
RN1701 SRN10KJ-5-GP SIO_PWRBTN# PCH_WAKE#
R1723 10KR2J-3-GP PCH_BATLOW#
RTC_AUX_S5
R1730 1MR2J-1-GP SM_INTRUDER#
R1733 10KR2J-3-GP PM_RSMRST#
ED1701 PESD5V0U1BL-GP-U1
R1732 8K2R2F-1-GP PM_PCH_PWROK
R1717 10KR2J-3-GP SYS_PWROK
DY

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.
H_CPUPWRGD
AFTP1702
ED1703 PESD5V0U1BL-GP-U1
R1735 10KR2J-3-GP
24,31,79 PCH_WAKE#

3D3V_S0 3D3V_S5
R1711 10KR2J-3-GP
R1701 3KR2J-2-GP DY
24,31,40,61,68,76 PLT_RST#
R1713 33R2J-2-GP PCH_PLTRST#
R1715 47KR2J-2-GP
C1701 SC100P50V2JN-3GP DY
ED1704 PESD5V0U1BL-GP-U1
0R2J-2-GP R1705
40 H_THERMTRIP_EN
60D4R2F-GP R1734
H_VCCST_PWRGD_R
24 SYS_PWROK
40 PCH_PWROK
R1706 0R0402-PAD PM_RSMRST#
R1704 0R0402-PAD
20,24 ME_SUS_PWR_ACK_R
3D3V_S5 R1707 10KR2J-3-GP

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

CPU1K 11 OF 20
SYSTEM POWER MANAGEMENT
SKYLAKE_ULT
PCH_PLTRST# XDP_DBRESET# PM_RSMRST# H_CPUPWRGD H_VCCST_PWRGD SYS_PWROK PCH_PWROK PM_PCH_PWROK PCH_DPWROK ME_SUS_PWR_ACK_R SUSACK# R PCH_WAKE# GPD2/LAN_WAKE#
GPP_B13/PLTRST# SYS_RESET# RSMRST#
PROCPWRGD VCCST_PWRGD
SYS_PWROK PCH_PWROK DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK GPP_A15/SUSACK#
WAKE# GPD2/LAN_WAKE# GPD11/LANPHYPC GPD7/RSVD#AT15
SKYLAKE-U-GP

GPP_B12/SLP_S0# GPD4/SLP_S3# GPD5/SLP_S4# GPD10/SLP_S5#
SLP_SUS# SLP_LAN# GPD9/SLP_WLAN# GPD6/SLP_A#
GPD3/PWRBTN# GPD1/ACPRESENT GPD0/BATLOW#
GPP_A11/PME# INTRUDER#
GPP_B11/EXT_PWR_GATE# GPP_B2/VRALERT#
SIO_SLP_S0# SIO_SLP_S3# SIO_SLP_S4# SIO_SLP_S5# SIO_SLP_SUS# SIO_SLP_LAN# SIO_SLP_A# AC_PRESENT PCH_BATLOW# PME# SM_INTRUDER# EXT_PWR_GATE# GPP_B2/VRALERT#
TP1709 TP1703 TP1710 TP1704 TP1705 TP1706 TP1707 TP1708

SIO_SLP_S3# TP1701

[543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

3D3V_S5
R1731 20KR2J-L2-GP EXT_PWR_GATE#

BATLOW#:
Pull-up required even if not implemented.

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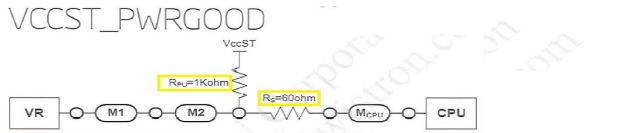
3D3V_S5
C1702 SC1U10V2KX-3GP +VCCST_CPU
Dis-wire with XDP_PM_RSMRST_PWRGD_XDP
U1701 74LVC1G07GW-GP 73.01G07.0HG
R1722 1KR2J-1-GP
24,40 ALL_SYS_PWRGD
H_VCCST_PWRGD_R
EC1708 SC1U10V2KX-3GP
R1718 200KR2F-L1-GP
R1719 47KR2F-GP
EC1709 SC1U10V2KX-3GP

VCCST_PWRGD / HWM201:



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

XDP_DBRESET# SYS_PWROK PLT_RST# PCH_PWROK
EC1706 EC1702 EC1703 EC1704 SC10P50V2KX-1GP
ED1702 PESD5V0U1BL-GP-U1 DY

DY
ME_SUS_PWR_ACK_R R1708 0R2J-2-GP SUSACK# R
3D3V_AUX_KBC
R1727 100KR2J-1-GP
R1726 10KR2J-3-GP
Q1701 2N7002KDW-GP
3V_5V_POK#
PM_RSMRST# R1702 1KR2J-1-GP
3V_5V_POK_C R1728 0R0402-PAD
3V_5V_POK 45,54
PCH_RSMRST# 24
EC1711 EC1712 SC1U10V2KX-3GP
84.2N702.A3F
2nd = 075.063D1.007C

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: LV115 SKL-U | Rev: -1
Date: Monday, April 25, 2016 | Sheet 17 of 102

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SMLOALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PLACE WITHIN 1.1 INCH OF PCH

(#543816)Optional, can be left as OPEN/No-Connect.

add Circuit for NFC

RCIN#:
Frequency to Avoid: 33 MHz

SERIRQ PH:
PDG: 8.2k
CRB: 10k

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GPU
WLAN
LAN

Check Clock Mapping

Memory Down Strap

0=L, 1=H

RAMID	MD_ID3	MD_ID2	MD_ID1	MD_ID0	LENOVO PN	VENDOR PN	WISTRON PN	VENDOR	Density
0	0	0	0	0				SAMSUNG	1GB
1	0	0	0	1				MICRON	1GB
2	0	0	1	0				HYNIX	1GB
3	0	0	1	1				SAMSUNG	2GB
4	0	1	0	0				MICRON	2GB
5	0	1	0	1				HYNIX	2GB
6	0	1	1	0	SM30K11219	K4A8G165WB-BCPB	072.4B165.000U	SAMSUNG	4GB
7	0	1	1	1	SM30K59892	MT40A512M16HA-083E:A	072.4U512.0A0U	MICRON	4GB
8	1	0	0	0	SM30K59899	H5AN8G6NAFR-TFC	N/A	HYNIX	4GB
9	1	0	0	1					
10	1	0	1	0					
11	1	0	1	1					
12	1	1	0	0					
13	1	1	0	1					
14	1	1	1	0					
15	1	1	1	1					

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)
Size: A3 | Document Number: LV115 SKL-U | Rev: -1
Date: Monday, April 25, 2016 | Sheet 18 of 102

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	* 0 = Port C is not detected. 1 = Port C is detected.

These two signals have weak internal pull-down.

PCH strap pin:

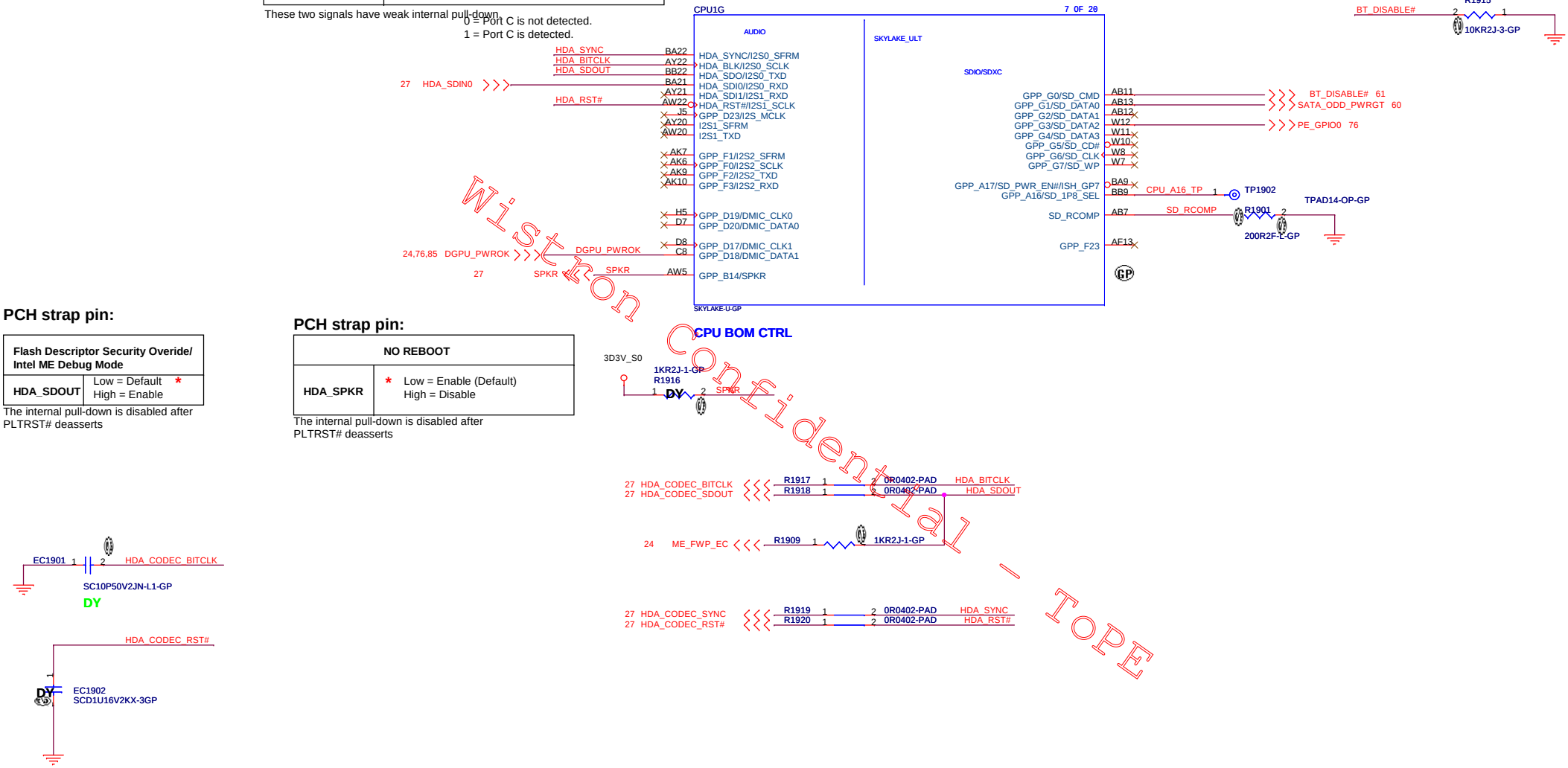
Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (AUDIO/SDIO/SDXC)	
Size A3	Document Number LV115 SKL-U	Rev -1
Date: Monday, April 25, 2016	Sheet 19 of 102	

Main Func = PCH

20151013 Change VIDEO_THERM_ALERT# PIN to GPP_B20

20151013 ADD R2041 to Connect DGPU_PWR_EN and PE_GPIO1

PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

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CPU BOM CTRL

ON BOARD RAM STUFF

ON BOARD RAM DY

DIMM SKT STUFF

DIMM SKT DY

CPU_28W

CPU_15W

<Core Design>

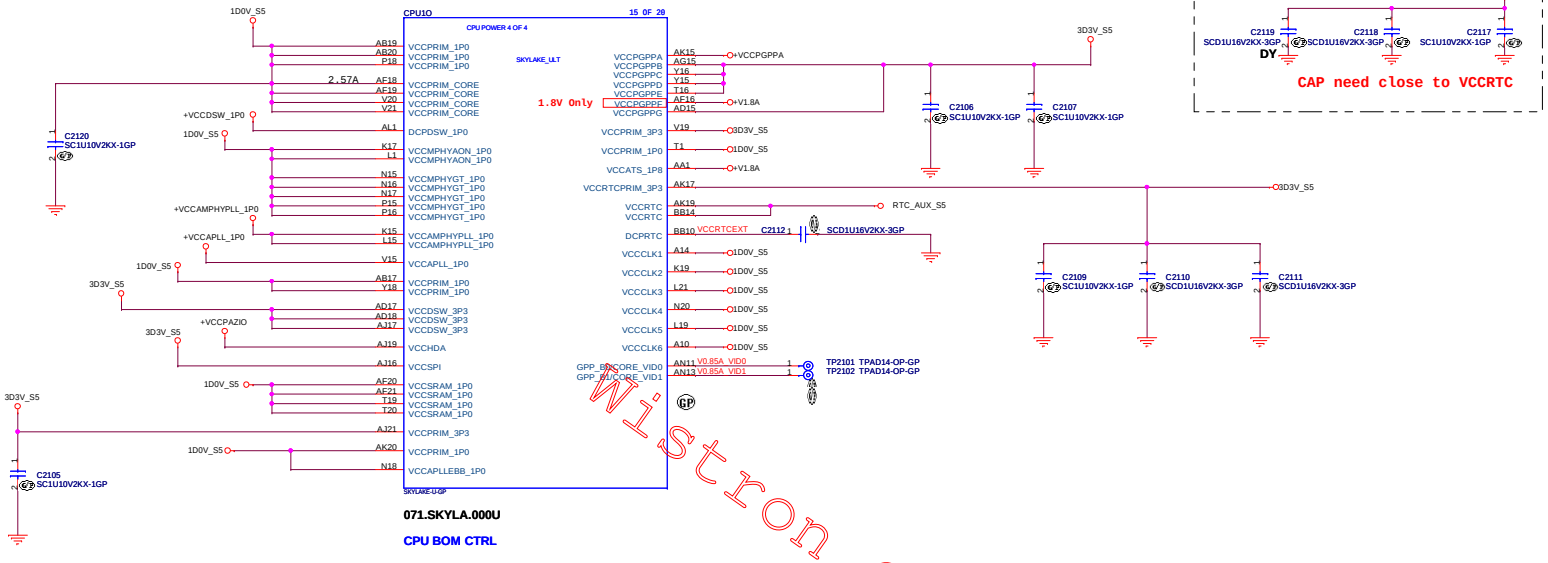
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

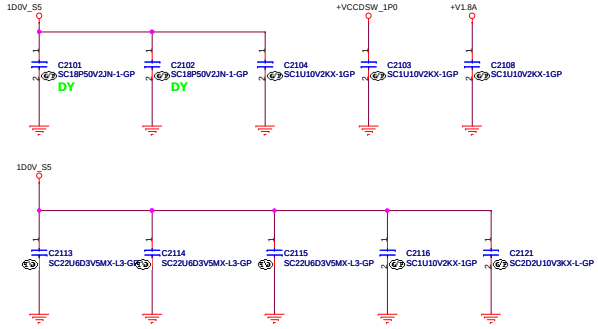
Title: CPU (LPSS/ISH)

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 20 of 102

Main Func = PCH





<Core Design>

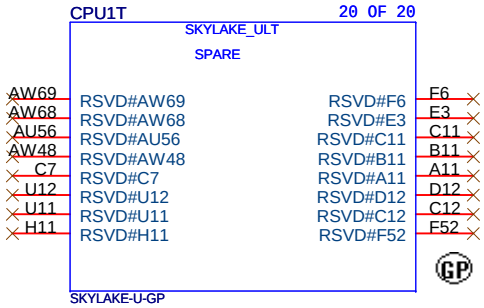
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 21 of 102

Main Func = PCH



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CPU BOM CTRL

<Core Design>

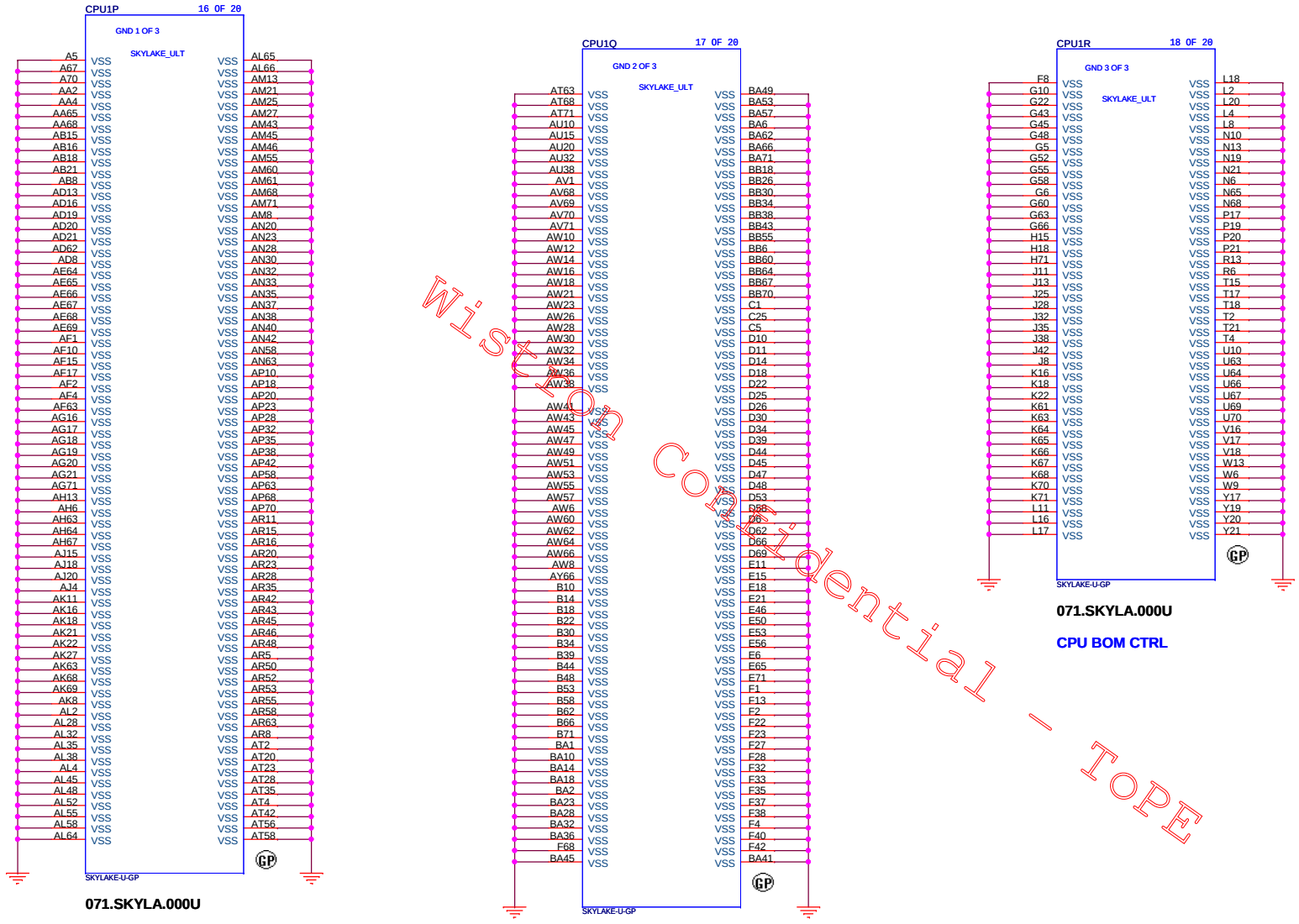
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	**LV115 SKL-U**	**-1**

Date: Monday, April 25, 2016 Sheet 22 of 102

Main Func = PCH



071.SKYLA.000U

CPU BOM CTRL

071.SKYLA.000U

CPU BOM CTRL

071.SKYLA.000U

CPU BOM CTRL

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_(VSS)*

Size	Document Number	Rev
A3	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 23 of 102

SSID = KBC

Model_ID_BOM Ctrl

MODEL ID

BOM Ctrl_Model

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LV115 Intel skylake	100.0K	10.0K 64.10025.6DL	3.0V
LV114 Intel skylake	100.0K	20.0K 64.20025.1DL	2.75V
NA	100.0K	33.0K 64.33025.1DL	2.48V
NA	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

PCB VERSION

BOM Ctrl_VER

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
SE	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

SPEC: ADT PWR Detection Function V1 3

DELTA Model:ADP65FD BB-PD03 ADP

PIN 3 PIN 1 PIN 2

	SIGNAL
PIN 1	287~ohm(1% TOLERANCE)
PIN 3	------
PIN 2	

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.109V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.234V < ID <= 0.663V	45W

SA

Prevent BIOS data loss solution

84.T3906.A11
1ST = 84.T3906.A11
2nd = 84.T3906.E11

74.03809.07B

NPCE285G

Thermal VD

BATTERY / CHARGER ---->

TP---->

20150724 Need check DGPUHOT

Modified 20151007
Delete DS3 Relative Components

06/16 MAX R1717 DY

Reserved AOAC

071.00285.0A0G

6/18 U2403 Change Part Number to 71.00285.0A0G (285P)

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils.. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Locate resistors R2415 and R2417 close to the U2401.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
PWM Signal :
1. If unused, select alternative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

< ----06/26 LT41 USB_CHAR_SEL

KBC PWR supply at PSL mode.

< ----06/26 Viber Del TPM

< ----06/24 ADD IT8320

R2472 close to Pin103

2013/9/12
GPIO83/SOUT_CR & GPIO87/SIN_CR
Need reserved TP for Debug

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

84.02130.031
2nd = 84.00102.031

84.2N702.231
2ND = 84.2N702.031
3rd = 84.2N702.W31

EC_GPIO47 High Active

84.2N702.231
2ND = 84.2N702.031
3rd = 84.2N702.W31

EC GPIO PH

EC GPIO PL

KBB_DEFINE1_R use MODEL_ID to Define Lenovo Key:
LV115: "Fast Forward" Key
LV114: "Delete" Key

(Debug Card Side)

(Main Board Side)

3.3V_S5

KBC

TX
RX
GND

(RX) (reserved)
(RX)
(TX)
(TX) (reserved)

LF15V Note:
(1) R21= DY R2458(E51_TXD)
(2) R13= DY R2451(E51_RXD)

Nuvoton KBC PSL Logic

Table 11. PSL Operation States

Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

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NPCE285

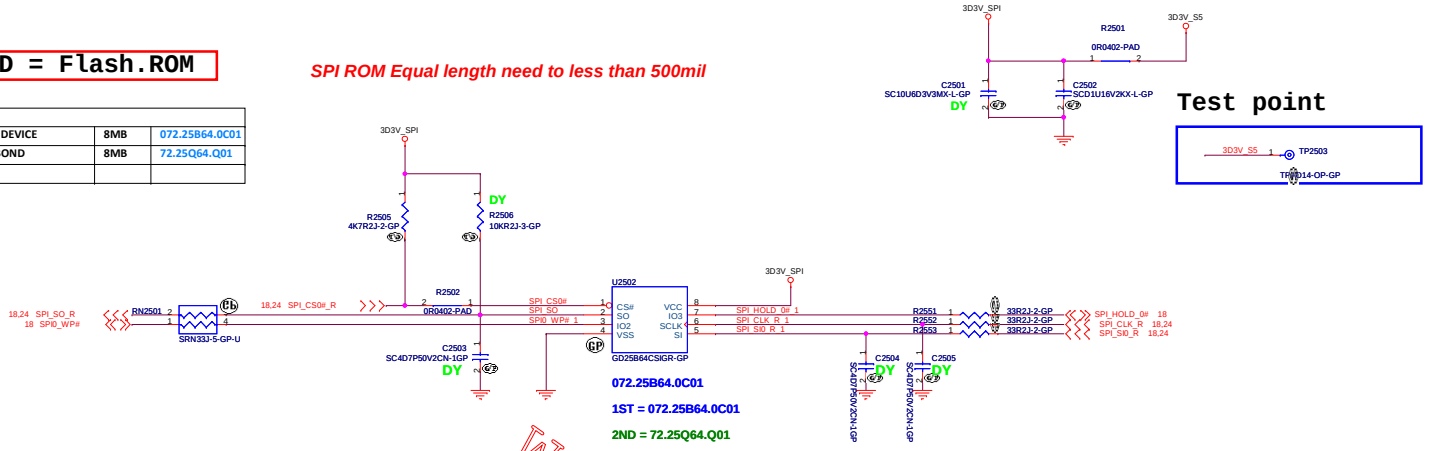
LV115 SKL-U

-1

SSID = Flash.ROM

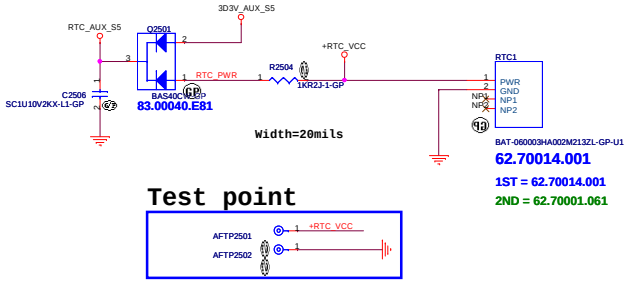
SPI ROM Equal length need to less than 500mil

U2502			
1ST	GIGA DEVICE	8MB	072.25B64.0C01
2ND	WINBOND	8MB	72.25Q64.Q01
3RD			

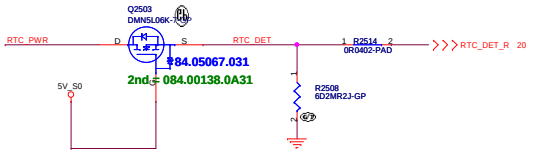


SSID = RBATT

SSID = RBATT



High Detect
Need to Check whether to PD in PCH Side



<Core Design>

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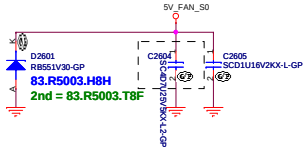
Title: Flash(KBC+PCH)/RTC

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 25 of 102

Main Func = Thermal Sensor

Layout 15 mil

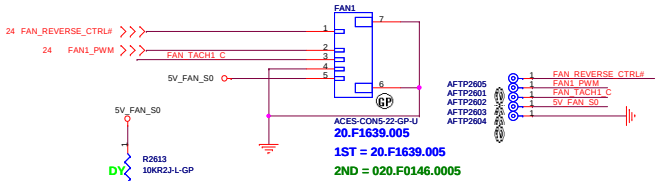


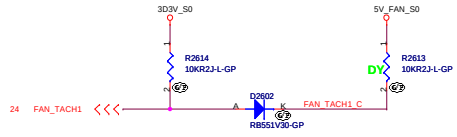
07/31 C2604 Change part number 78.47523.5BL to 78.47522.L4L, 值為4.uF, 0805, 不同的是25V

ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

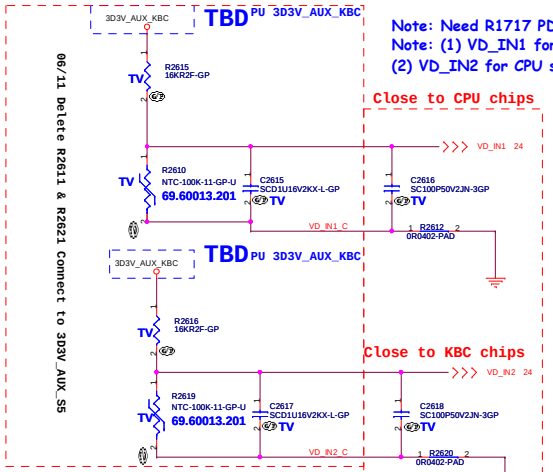
T_CRIT temperature strapping point





2.System Sensor, Put on palm rest

Close to Thermal sensor

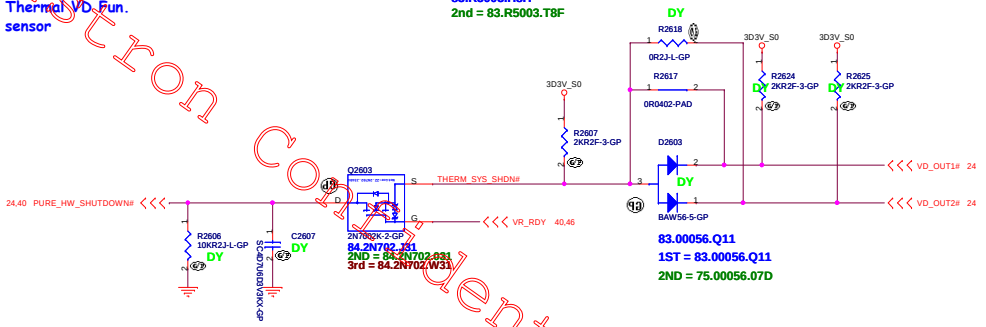


Close to CPU chips

Close to KBC chips

Note: Need R1717 PD: Enable Thermal VD Fun.
Note: (1) VD_IN1 for System sensor
(2) VD_IN2 for CPU sensor

T8=85 degree



Thermal config

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY
D2603	ASM	DY
R1717	ASM	DY

<Core Design>
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Title: THERMAL NCT7718W/Fan
Size: A2 | Document Number: LV115 SKL-U | Rev: -1
Date: Monday, April 25, 2016 | Sheet 26 of 102

Current > 2A

MOAT

MOAT

MOAT

MOAT

MOAT 20151024 modify

Tied at one point only under Codec or near the Codec

Near AVDD1 and AVDD2 power source input

SA_ESD

Place close to pin1

Place close to pin8

Place close to pin26

ERN2701 SET 22 ohm in SA

R2708 power should follow DVDD (pin1) power rail.
If DVDD=3.3V, R7 power source should be change to 3.3V

RING2/SLEEVE Trace width must > 40mils

SPK 4Ω 40mils

Place close to Pin 26

UAJ-Microphone

place close audio codec

Analog

Digital

Place close to pin 1

Place close to pin 9

EC_Mute#

U2701

ALC3240-VA3-CG-GP

071.03240.0A03

REALTEK
ALC3240
(Include Thermal pad)
QFN40 (5x5)

Wistron Confidential

TOP

FAE
HDA_RST#_CODEC:
High=1.8V
Low=0V
this signal might cause AUD_SD# always low when R2710=0ohm
You should add level shift on HDA_RST#_CODEC signal when Codec PIN9 DVDDIO= 1.5V.

83.00056.Q11

1ST = 83.00056.Q11

2ND = 75.00056.07D

<Core Design>

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Title: Audio Codec ALC3234

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 27 of 102

<Core Design>

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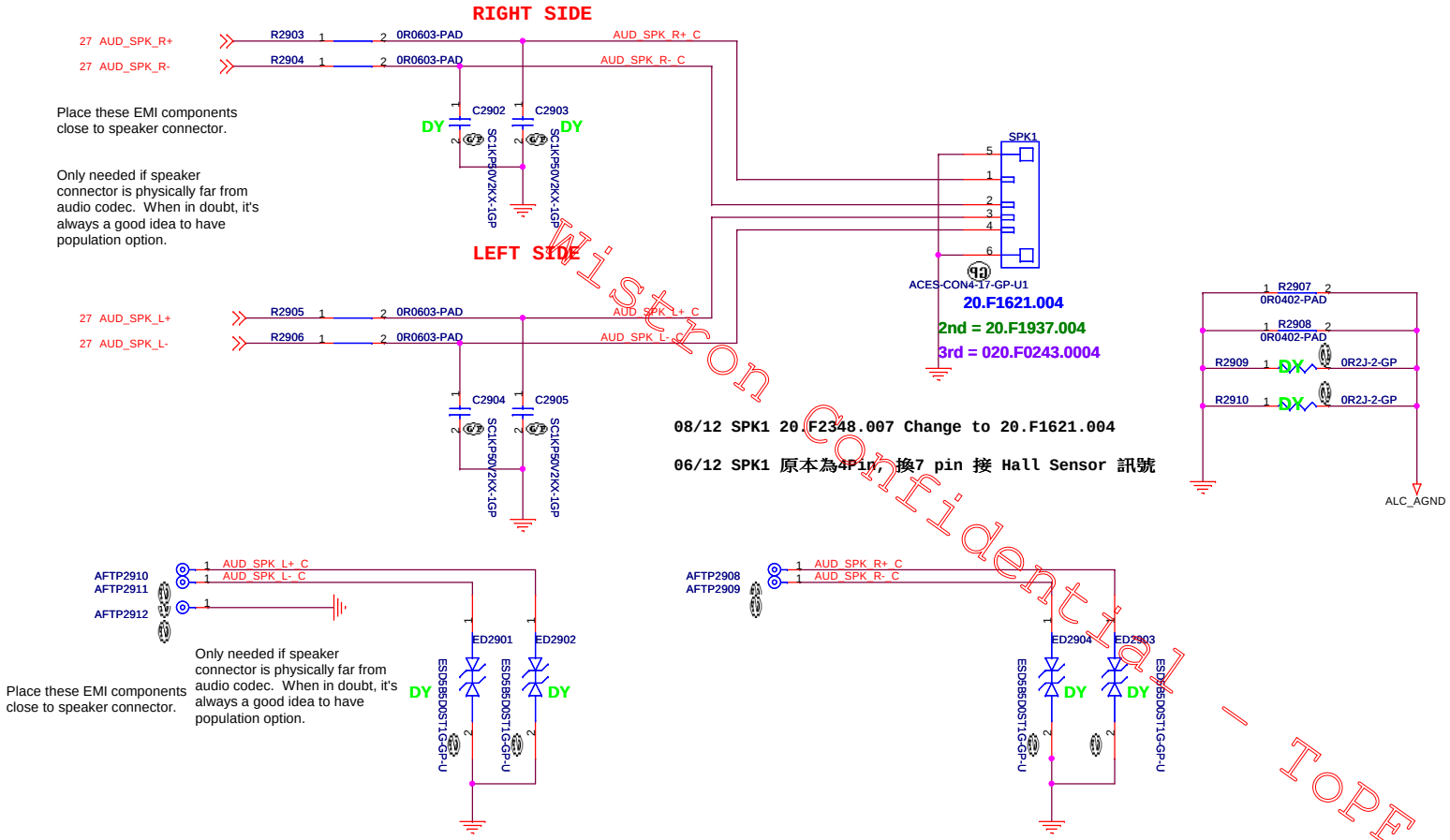
Title

Reserved

Size	Document Number	Rev
A1	LV115 SKL-U	-1

Date: Monday, April 20, 2015 Sheet 28 of 102

INTERNAL STEREO SPEAKERS



<Core Design>

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Title: Audio IO

Size: A3 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 29 of 102

Main Func = Audio

(Blanking)

<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A4	LV115 SKL-U	-1

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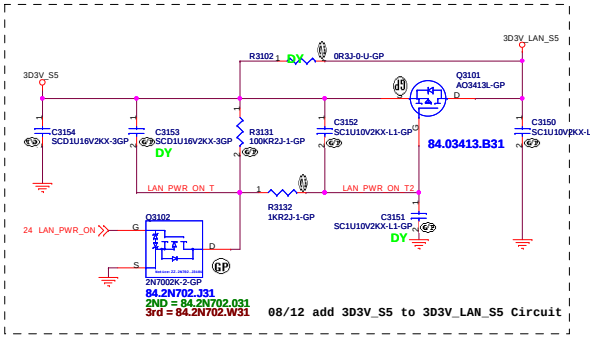
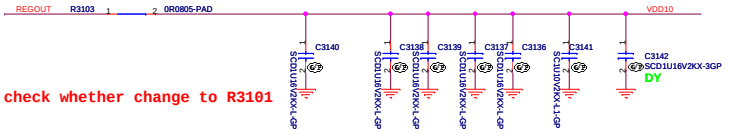




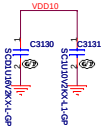
Need check whether change to R3101

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C3138 to C3141 close to each VDD10 pin-- 3, 8, 22, 30

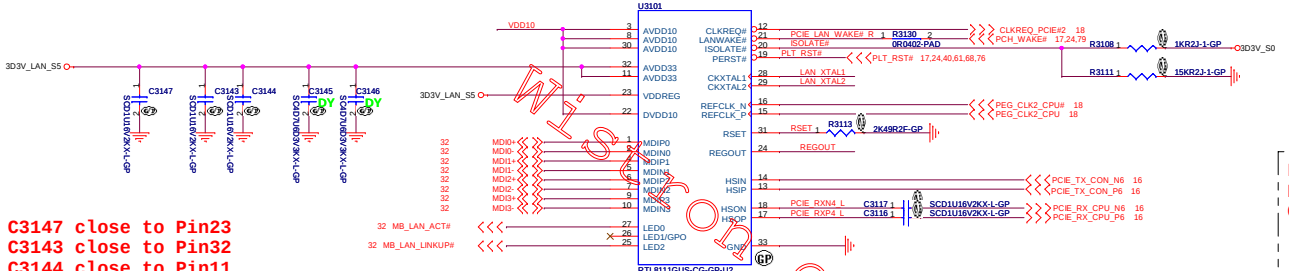
For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C20 and C21 close to each VDD10 pin-- 22 (Reserved)

C3138 close to Pin3 , C3139 close to Pin8
C3140 close to Pin30,C3136 close to Pin22

For RTL8111G(S) Series/ RTL8111GUS Series/ RTL8111H(S) Series/
RTL8106EUS Series/ RTL8107E(S) Series/ RTL8118AS Series
C3132,C3133 close to Pin22



For RTL8106E Series
C3130,C3131 close to Pin30



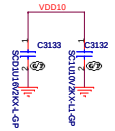
71.08111.W03

BOM CHANGE TO RTL8111H:SC50H01259

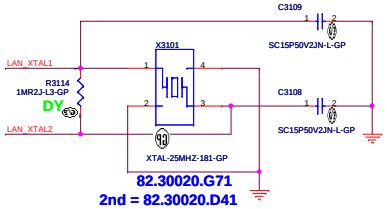
LAN_BOM_CTRL

C3147 close to Pin23
C3143 close to Pin32
C3144 close to Pin11

For RTL8111G(S) Series/ RTL8111GUS Series/ RTL8111H(S) Series/
RTL8106EUS Series/ RTL8107E(S) Series/ RTL8118AS Series
C3132,C3133 close to Pin22



25MHz XTAL



Crystal 27MHz			
MAIN	HASONIC	82.30020.G71	78.15034.L1L
2ND	HARMONY	82.30020.D41	78.18034.1FL

LAN and Transformer Config:

LAN/Transformer	

<Core Design>
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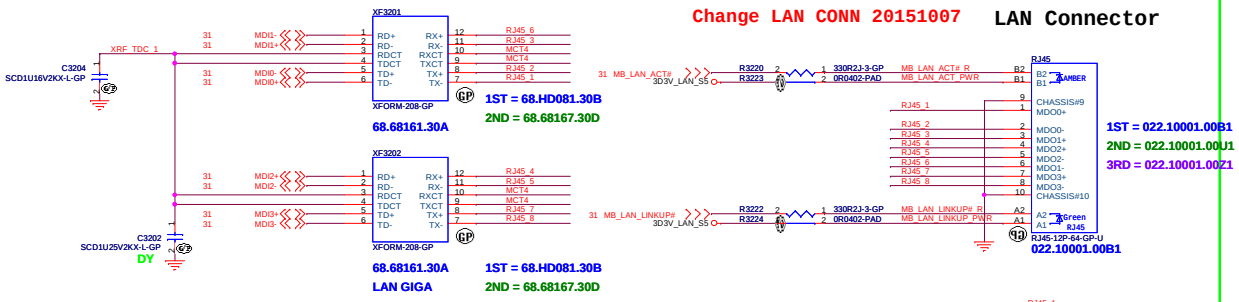
Taipei Hsien 221, Taiwan, R.O.C.

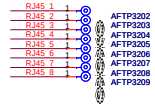
Title: LAN_RTL8111

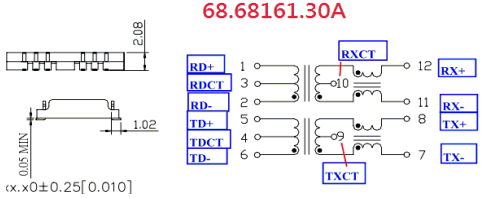
Size	Document Number	Rev
A2	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 31 of 102

10/100M/1000M Lan Transformer



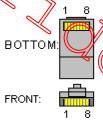




RJ45 Pin define

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BI_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BI_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BI_DB+
4	Not connected or BiDirectional	n/c	n/c	BI_DC+
5	Not connected or BiDirectional	n/c	n/c	BI_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BI_DB-
7	Not connected or BiDirectional	n/c	n/c	BI_DD+
8	Not connected or BiDirectional	n/c	n/c	BI_DD-

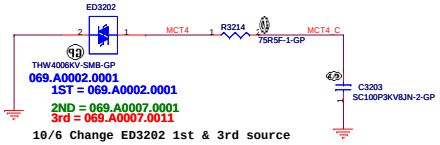
The connector is 8 pin RJ45 (8P8C) male

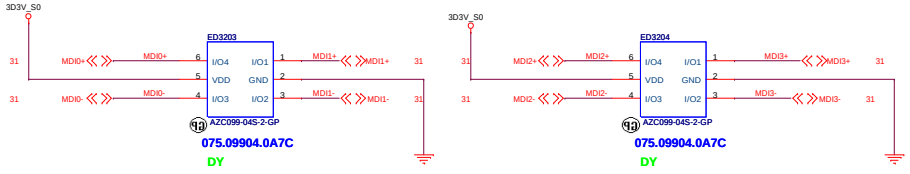


The associated connector is 8 pin RJ45 (8P8C) female

10/100/1000 LAN surge circuit

For test stuff





<Core Design>

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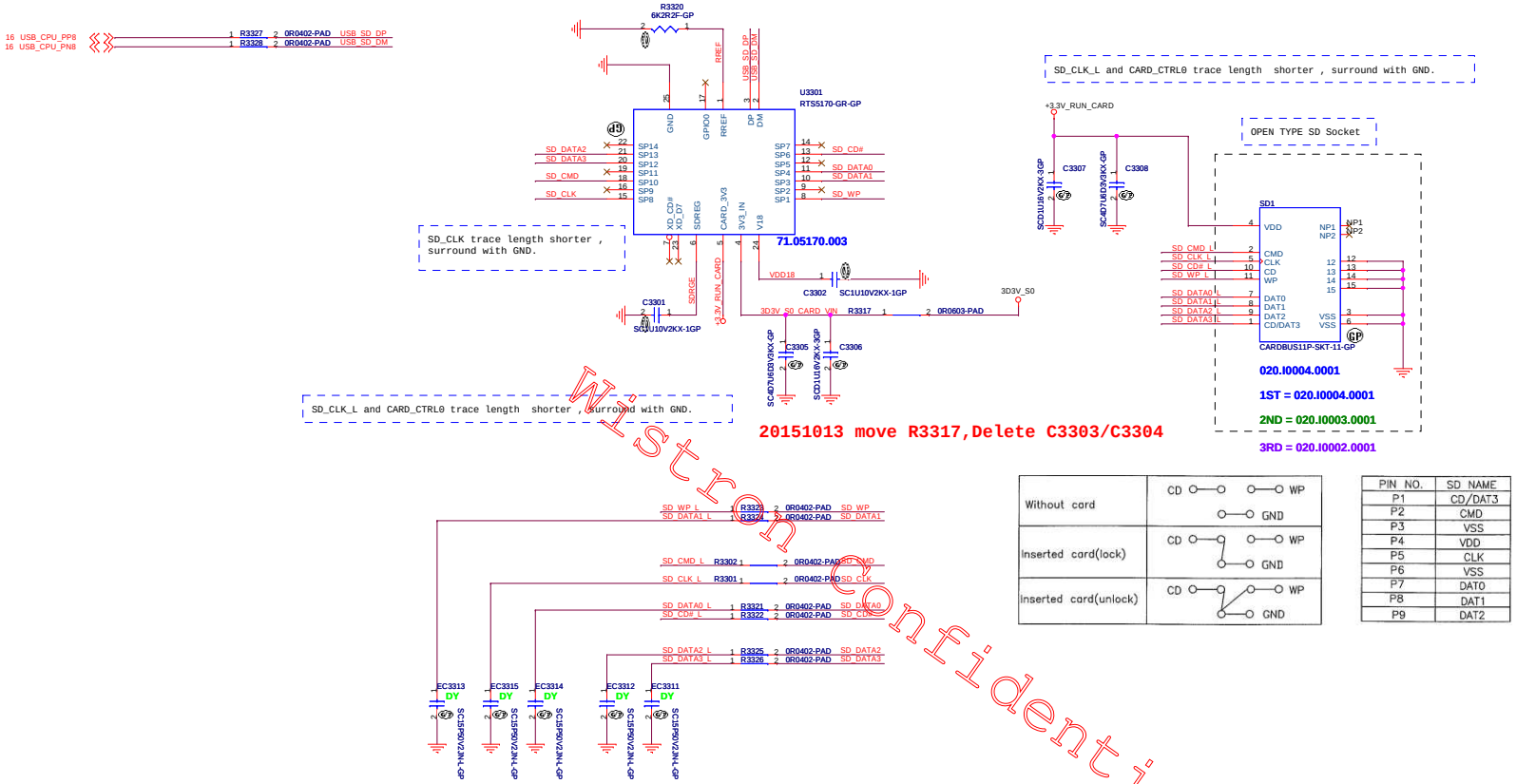
Title: RJ45&Transformer
Size: A2 | Document Number: LV115 SKL-U | Rev: -1
Date: Monday, April 25, 2016 | Sheet 32 of 102

Card Reader RTS5170



PIN_NO.	SD_NAME
P1	CD/DAT3
P2	CMD
P3	VSS
P4	VDD
P5	CLK
P6	VSS
P7	DAT0
P8	DAT1
P9	DAT2

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 33 of 102

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Charger

Size	Document Number	Rev
Custom	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 34 of 102

<Core Design>

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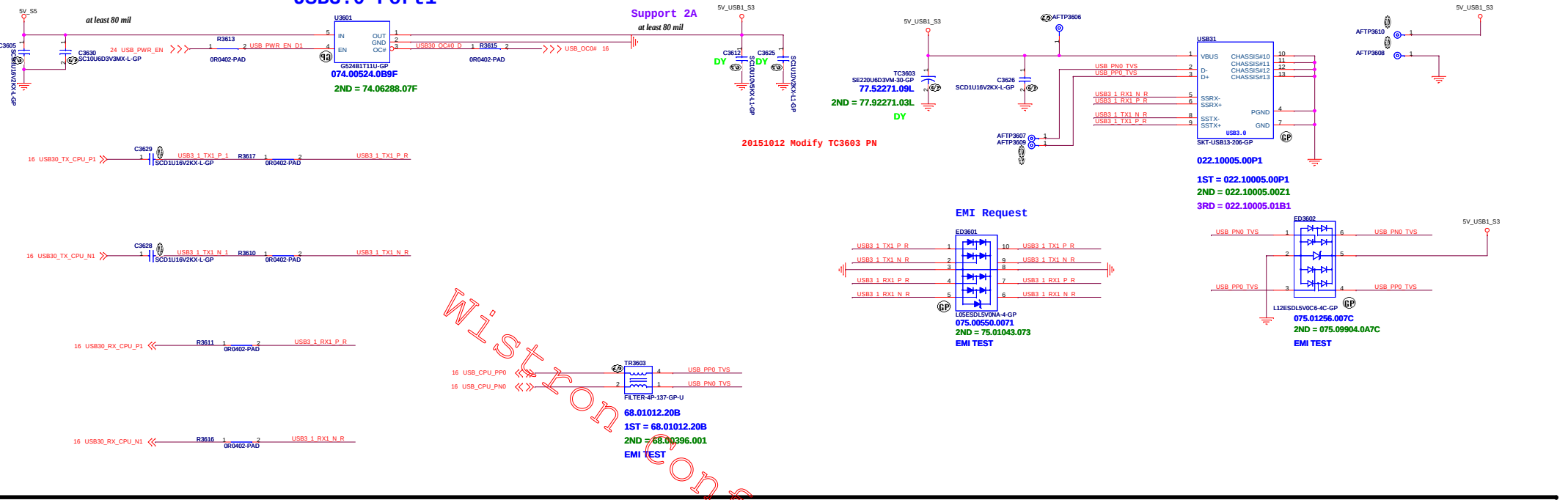
Title
Reserved

Size	Document Number	Rev
A3	LV115 SKL-U	-1

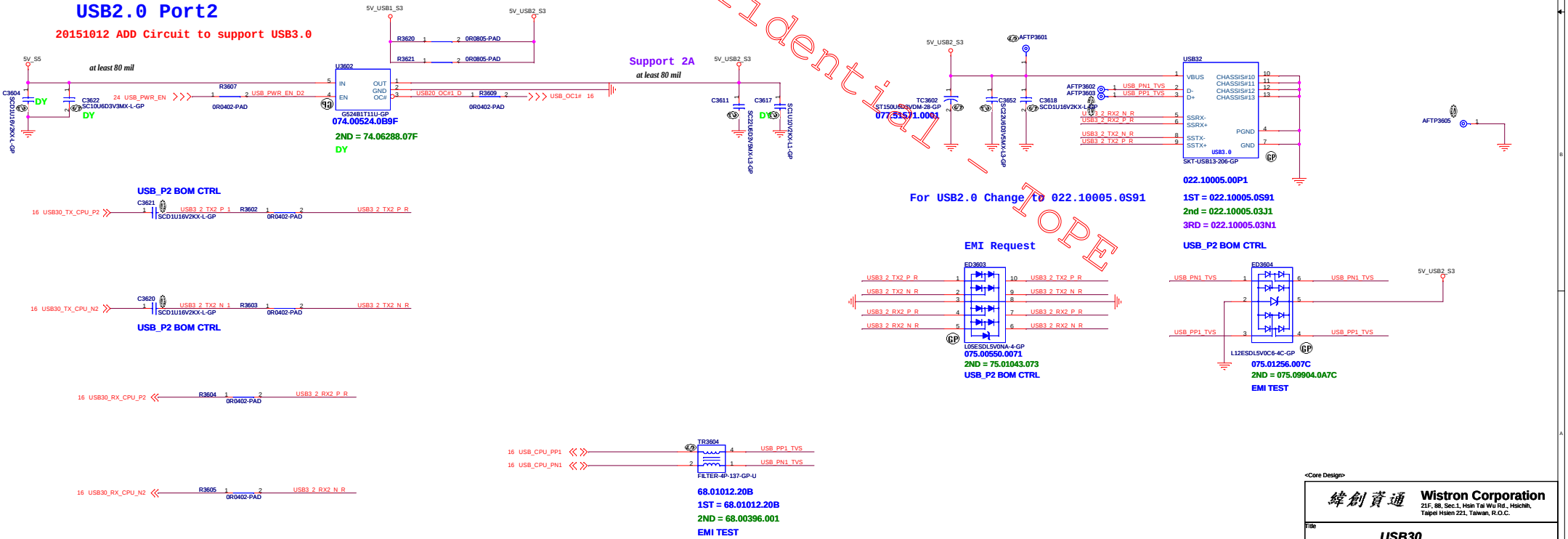
Date: Monday, April 25, 2016 Sheet 35 of 102

USB3.0 Port1



USB2.0 Port2

20151012 ADD Circuit to support USB3.0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size	Document Number	Rev
A2	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 36 of 102

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 37 of 102

Main Func = USB3.0 Port1

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 38 of 102

Main Func = USB3.0 Port1

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

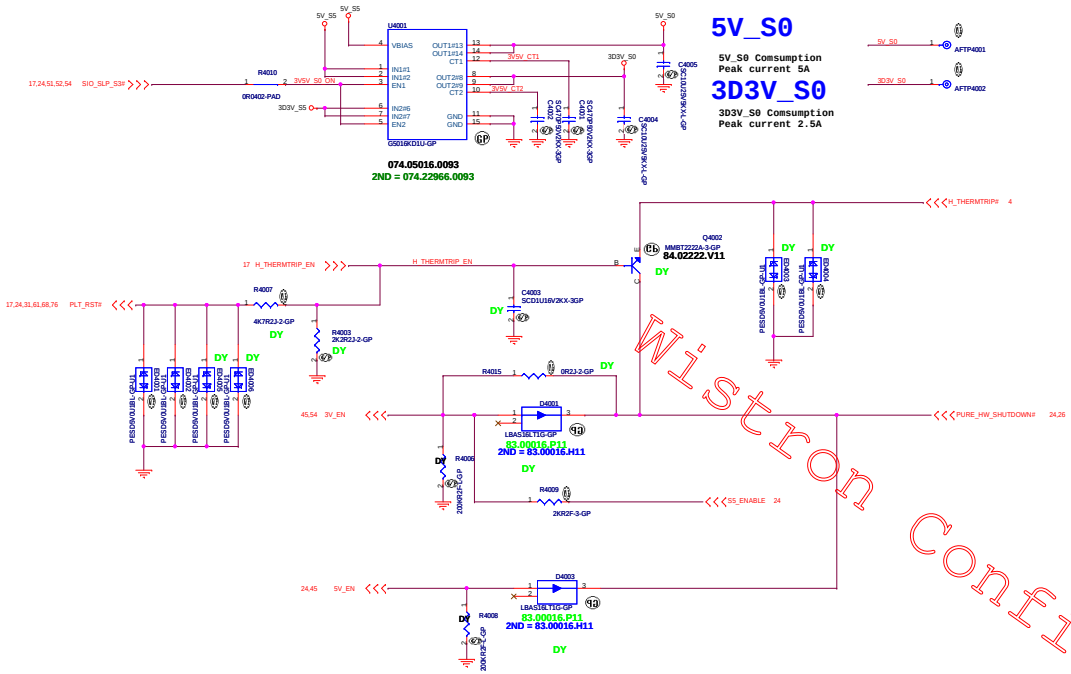
Title: ***Reserved***

Size	Document Number	Rev
A4	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 39 of 102

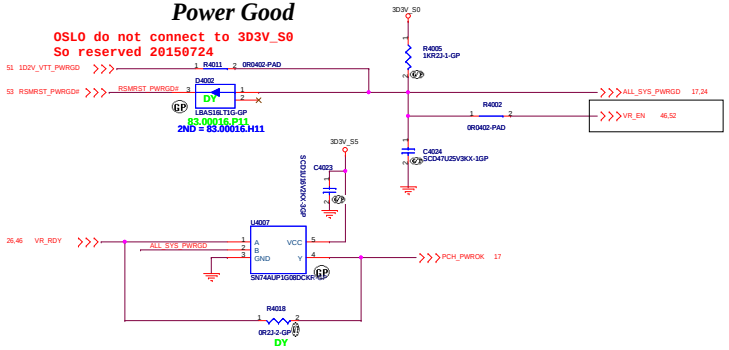
Main Func = Power Plane & Sequence

ROSA Run Power



Power Good

OSLO do not connect to 3D3V_S0
So reserved 20150724



VCCSTG

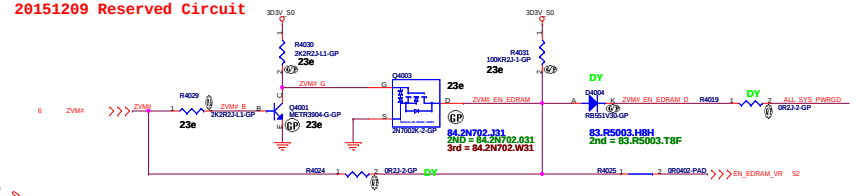
20151007 Delete Reserved Circuit
Power Source Keep VCCIO (R710)

+VCCSTG(ICCMAX.=0.16A)

VCCSTG should only ramp up equal to or after VCCST.

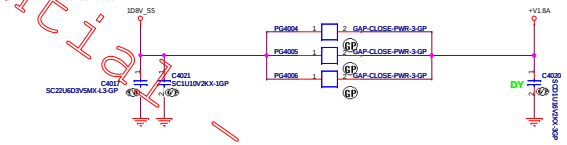
GT3 Low Power Circuit (ZVM)

20151209 Reserved Circuit

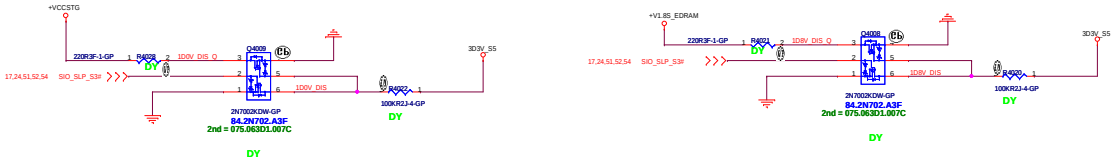


V1.8A

Need to Check



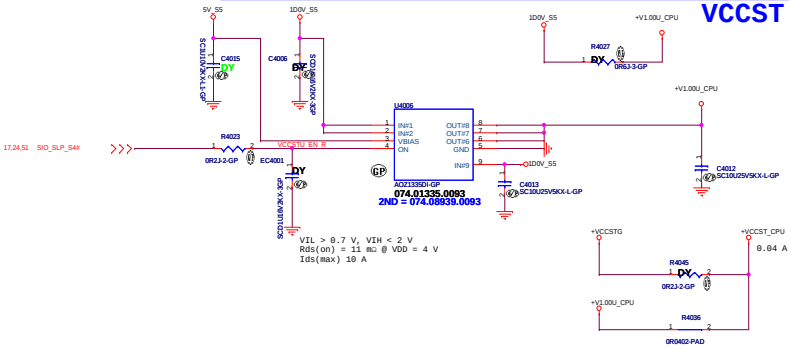
Discharge circuit



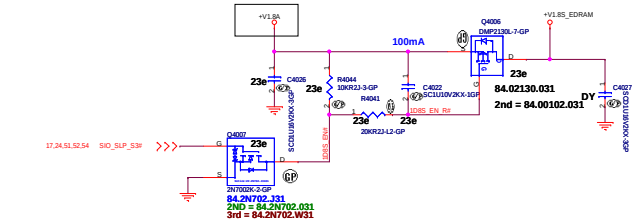
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST



V1.8S



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane EN Sequence

Size: Custom | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 40 of 102

Main Func = Power Plane & Sequence

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(1/2)+DS3*

Size	Document Number	Rev
A4	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 41 of 102

Main Func = DIMM1
Main Func = DIMM2

VREF CIRCUITRY

<Core Design>

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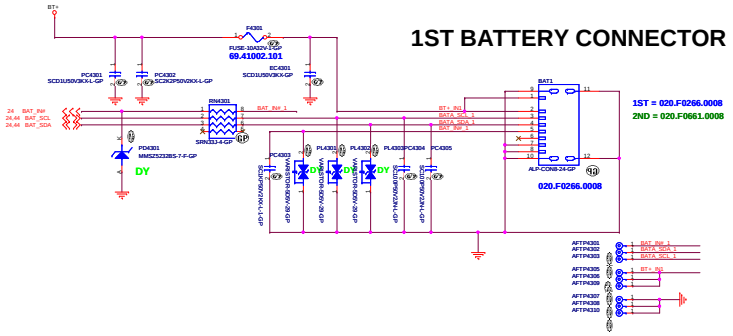
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Connected_Standby(2/2)*	
Size: A3	Document Number: LV115 SKL-U	Rev: -1
Date: Monday, April 25, 2016	Sheet 42 of 102	

1ST BATTERY CONNECTOR



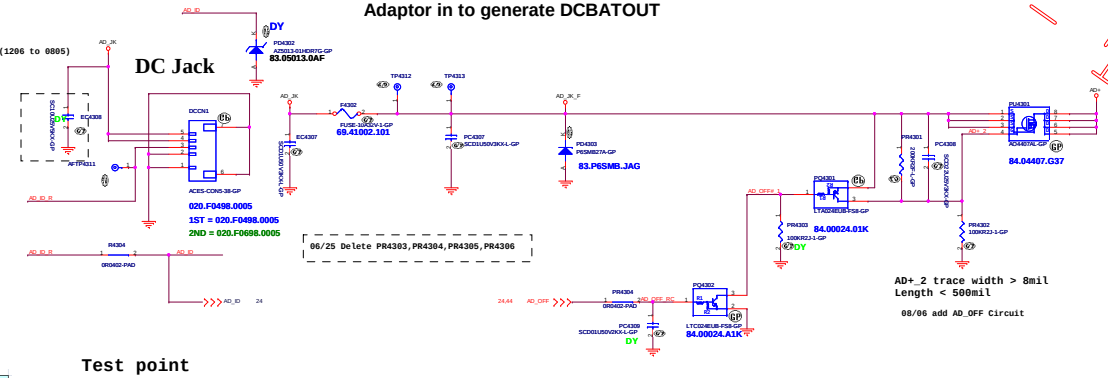
Connector Pin Alignment(Vendor：Suyin,Aces)

Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

08/01 EC4308 Change part number 78.10622.L5L to 78.10622.51L(1206 to 0805)

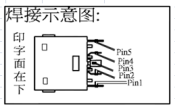
Adaptor in to generate DCBATOUT

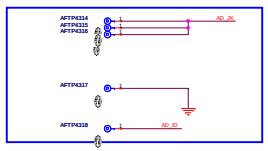


Test point

MB_Side		Cable
		Max. Current
Pin 1	AD_JK_F	UL10064AWG28# (3A)
Pin 2	AD_JK_F	UL10064AWG28# (3A)
Pin 3	AD_ID	UL10064AWG28# (3A)
Pin 4	GND	UL10064AWG26# (3.8A)
Pin 5	GND	UL10064AWG26# (3.8A)

焊接示意图:





<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: DCIN & BATT Com
Size: A1 | Document Number: LV115 SKL-U | Rev: -1
Date: Monday, April 25, 2016 | Sheet 43 of 102

SSID = Charger

20151230 Power Team update Table

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
45w	51K 64.51025.6DL	100K
65w	120K 64.12035.6DL	100K
		100K
		100K

20151012 Modify PU4401 PN 84.08131.037
1ST = 84.08131.037
2ND = 84.07403.037

20151012 Modify PU4402 PN
84.08131.037
1ST = 84.08131.037
2ND = 84.07403.037

Id= -10A
Qg= -22nC
Rdson=14~22mohm

STOP_CHG# connects to KBC

ADT BOM CTRL

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31

84.00412.037
1ST = 84.00412.037
2ND = 084.03319.0A37

83.1R003.N8F

74.02224.073

Charger Current=1.4~3.6A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CHARGER
Size: A2 | Document Number: LV115 SKL-U | Rev: -1
Date: Monday, April 25, 2016 | Sheet 44 of 102

08/20 add 5V_EN

12/18 PR4501,PR4502 Change to Short PAD

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(上綠漆)

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(上綠漆)

Design Current=3.1A
OCP <6.2A

Design Current=6.4A
OCP < 12.8A

20151012 Modify TC4501 PN

20151012 Modify TC4503 PN

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

ASM_RES_PAD_DY

<Core Design>

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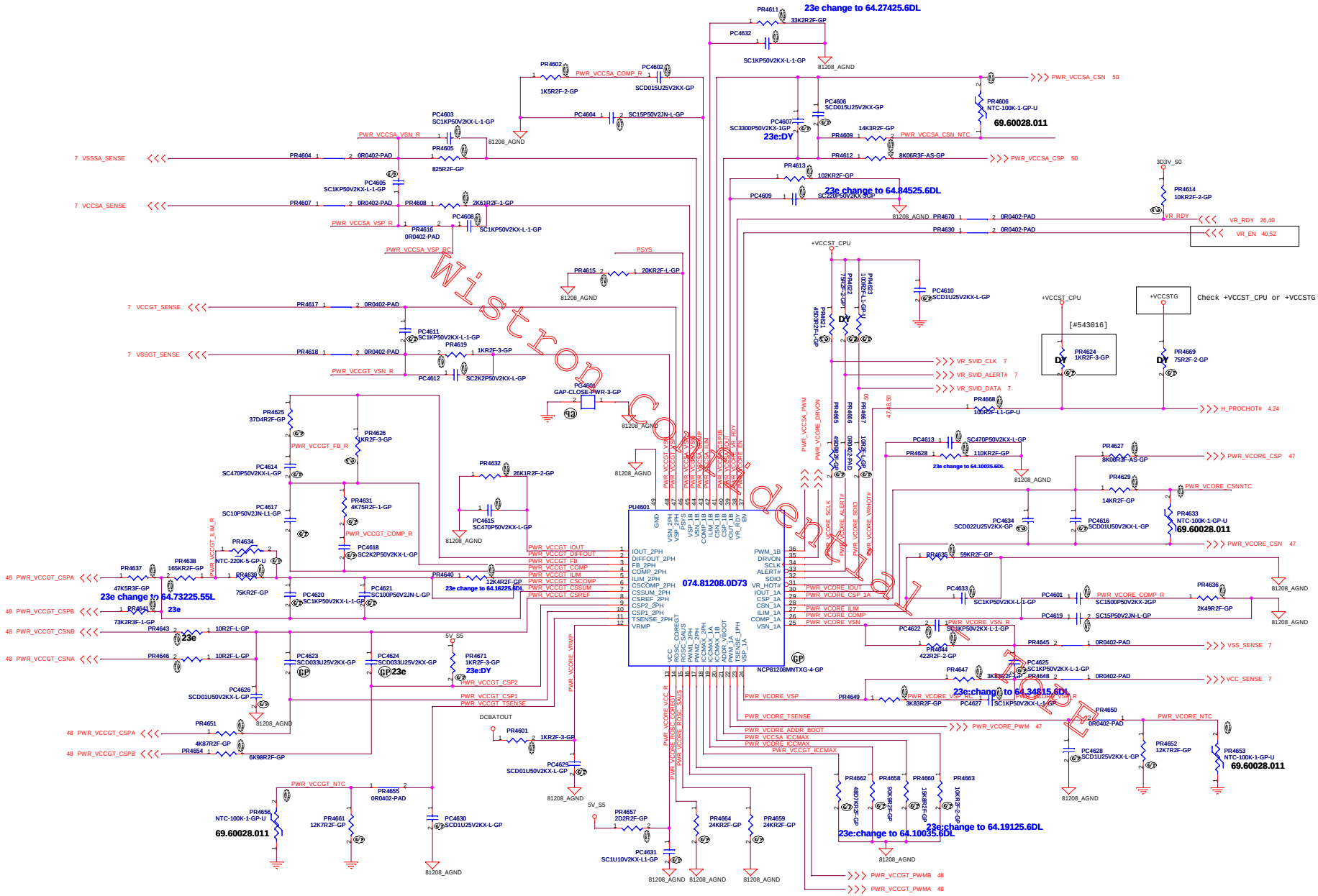
Taipei Hsien 221, Taiwan, R.O.C.

Title: SYN256 5V/3D3V

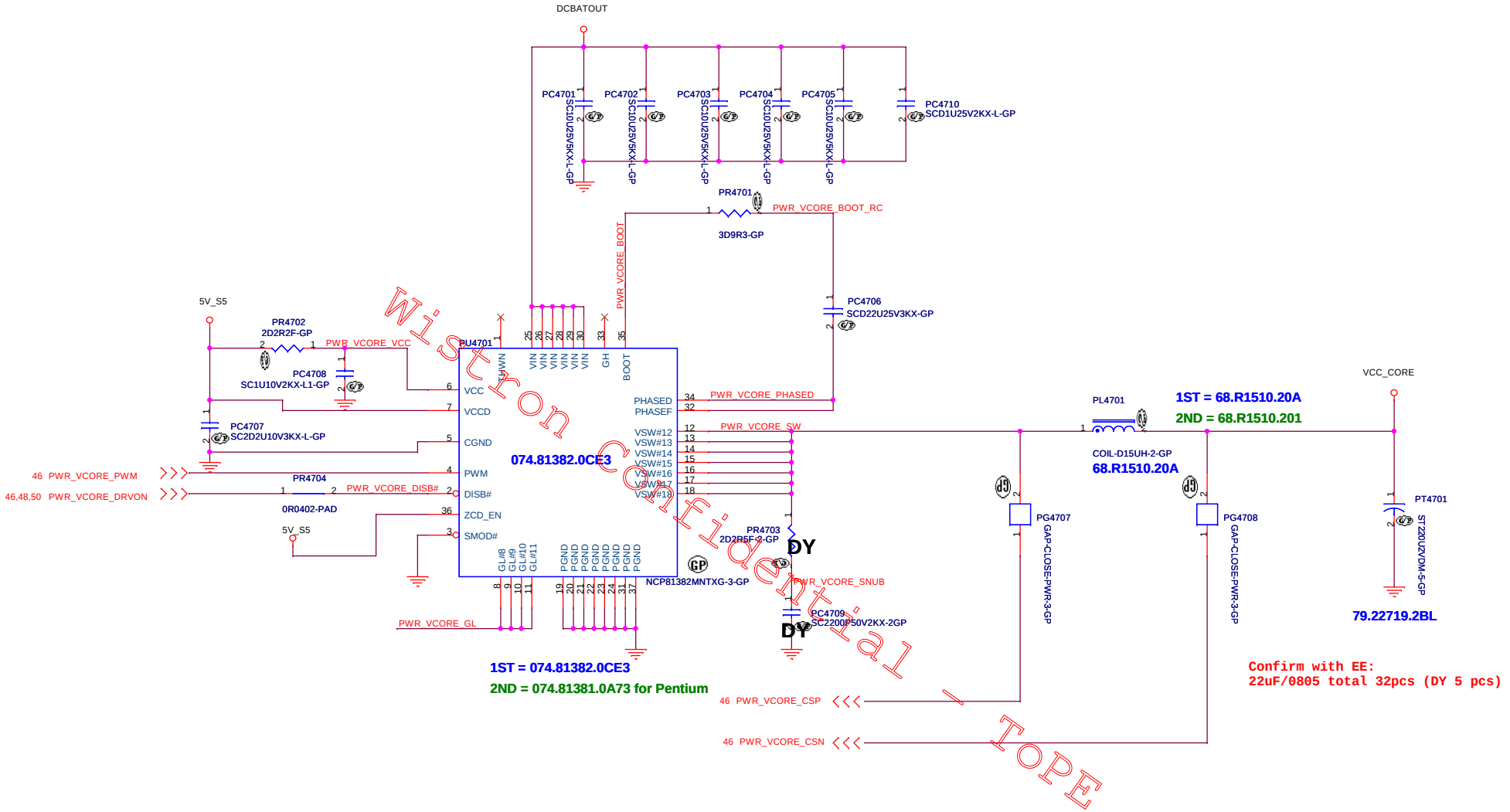
Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 45 of 102

Main Func = CPU_CORE



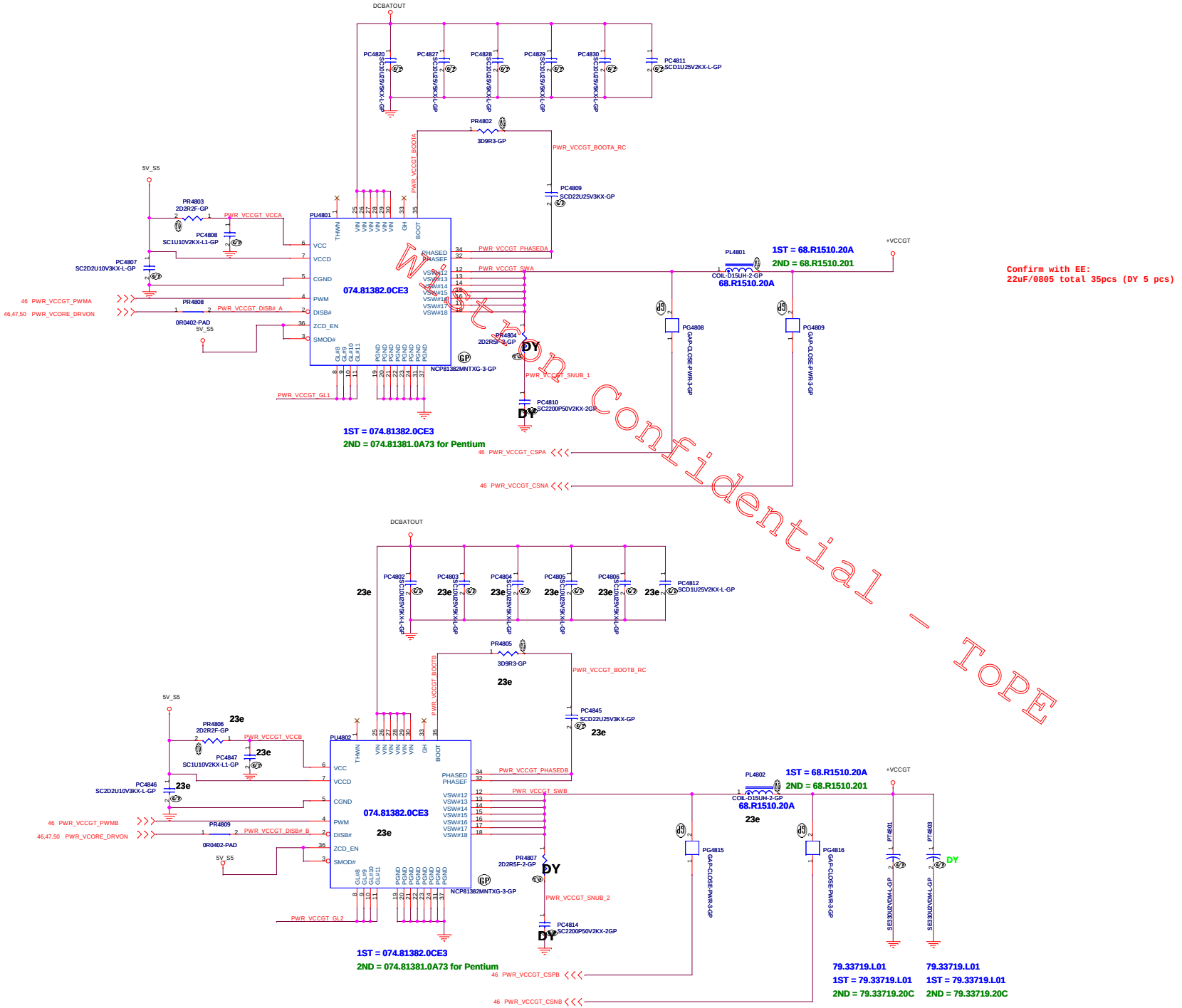
Main Func = CPU_CORE



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_VCORE(2/3)		
Size: A3	Document Number: LV115 SKL-U	Rev: -1
Date: Monday, April 25, 2016	Sheet 47 of 102	

Main Func = CPU_CORE



Confirm with EE:
22uF/0805 total 35pcs (DY 5 pcs)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCCGT3/3)

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 48 of 102

<Core Design>

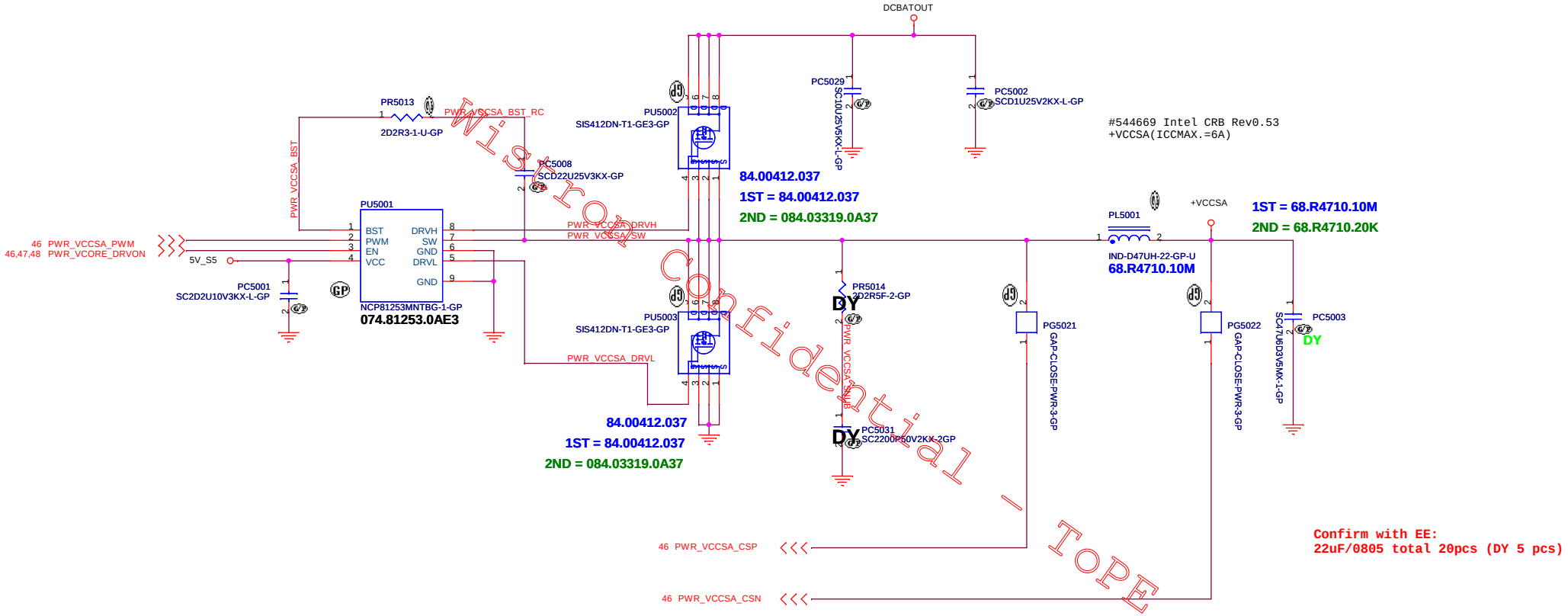
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCCGTUS

Size	Document Number	Rev
A2	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 49 of 102

Main Func = CPU_CORE



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCCSA

Size: A3 | Document Number: LV115 SKL-U | Rev: -1

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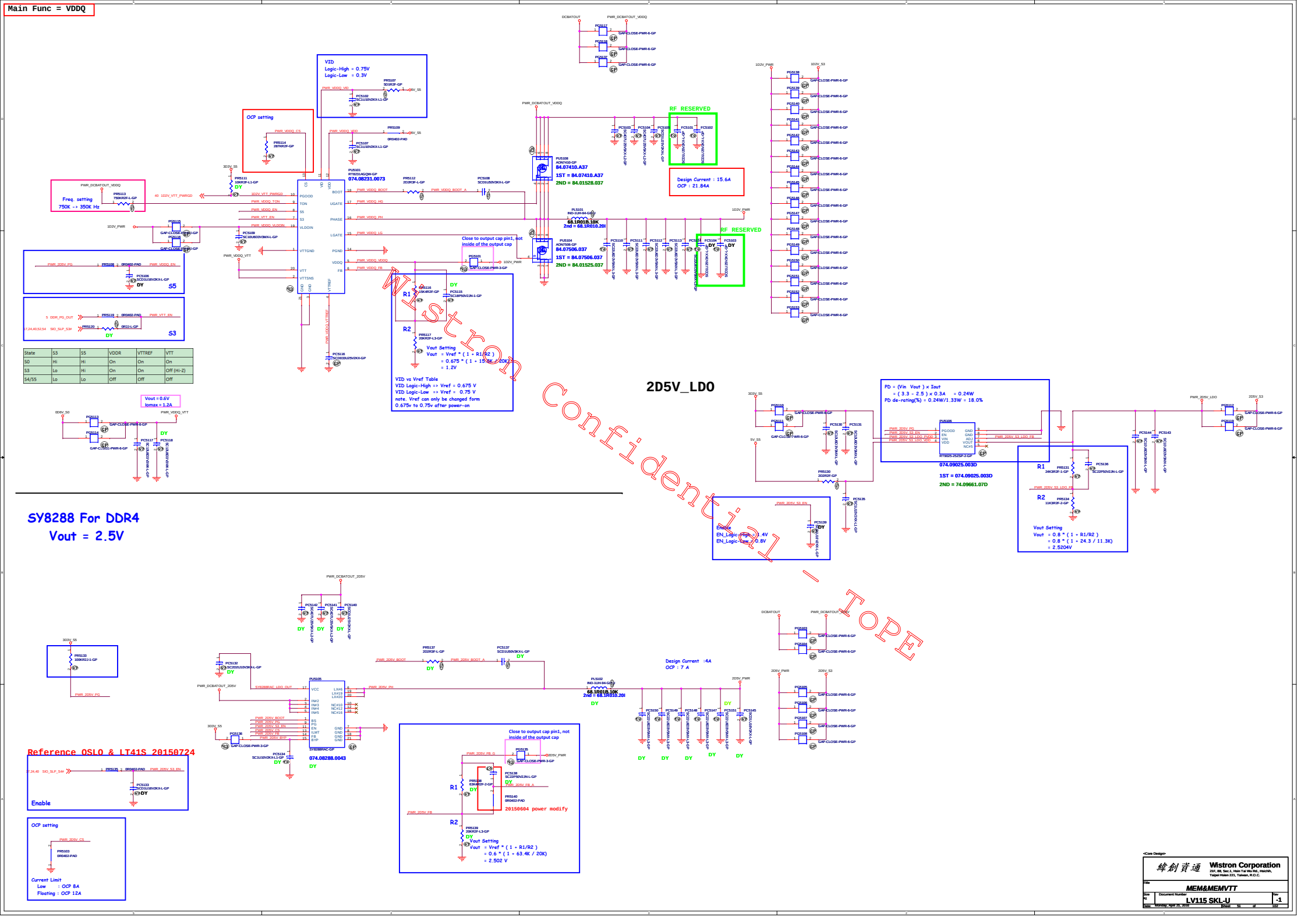
Main Func = VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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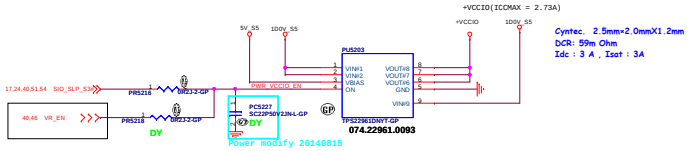
MEM&MEMVTT

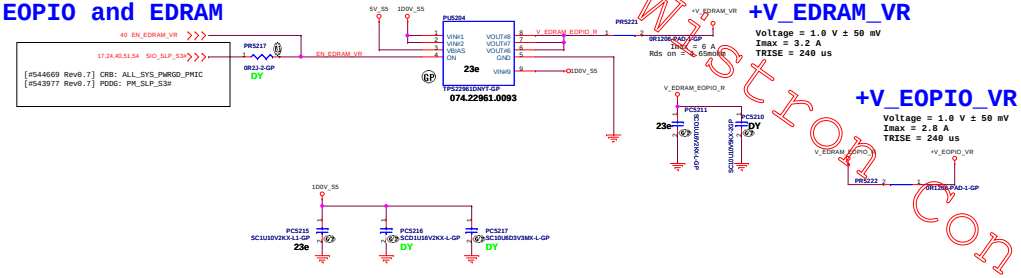
LV115 SKL-U

-1

VCCIO



EOPIO and EDRAM



+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

<Core Design>

Wistron Corporation
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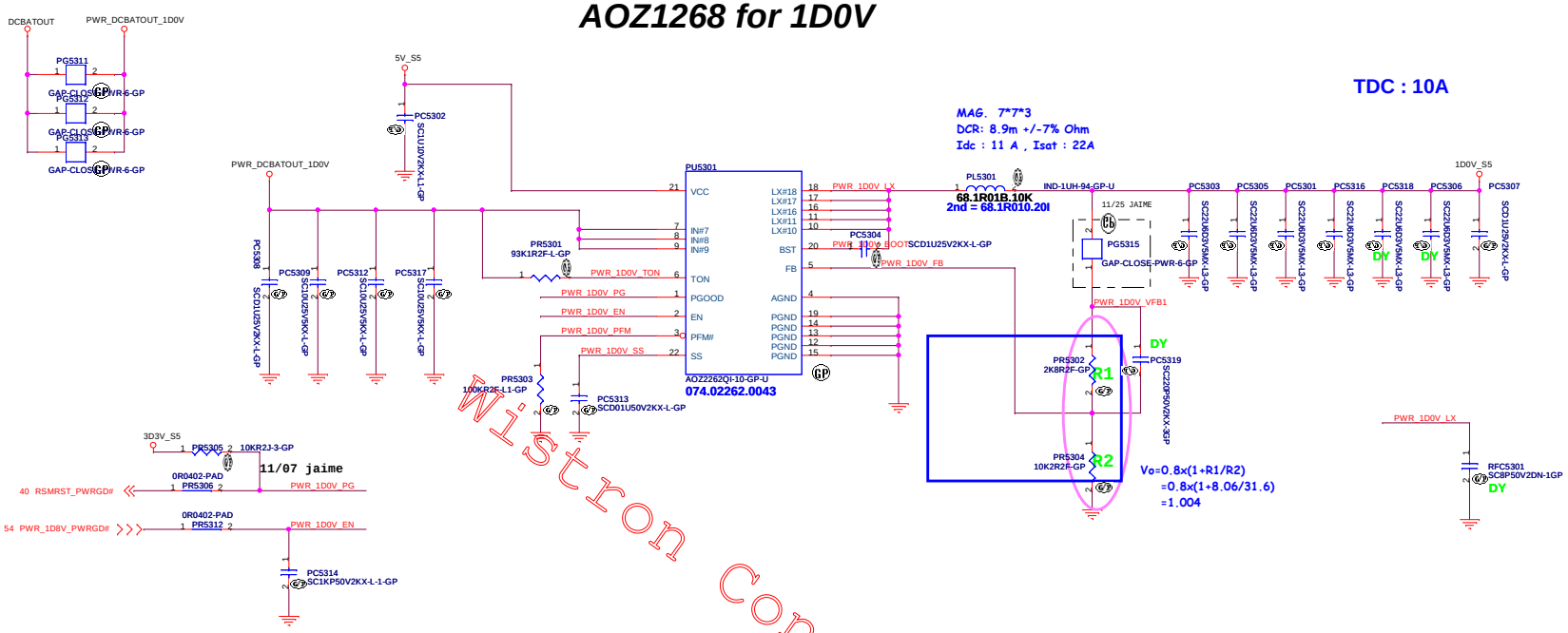
Title: DCDC-0D975V_VCCIO

Size: Custom | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 52 of 102

Main Func = 1D0V

AOZ1268 for 1D0V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC-V1D00A

Size: Custom | Document Number: LV115 SKL-U | Rev: -1

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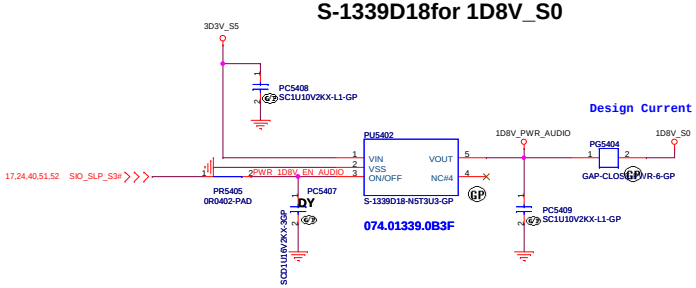
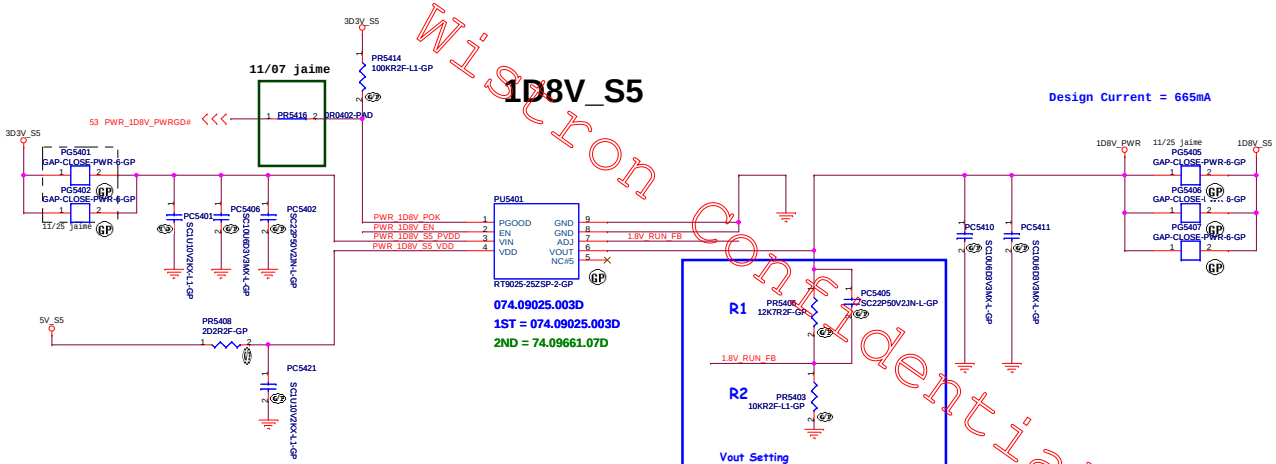
Main Func = 1D5V

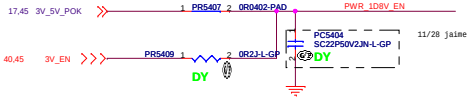
S-1339D18for 1D8V_S0



1D8V_S5

11/07 jaime





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC V1D8V

Size	Document Number	Rev
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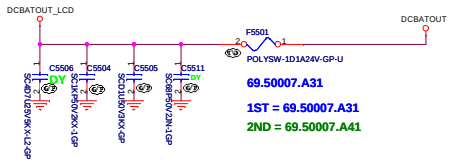
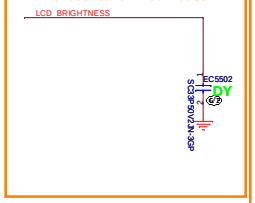
SSID = VIDEO

INVERTER POWER



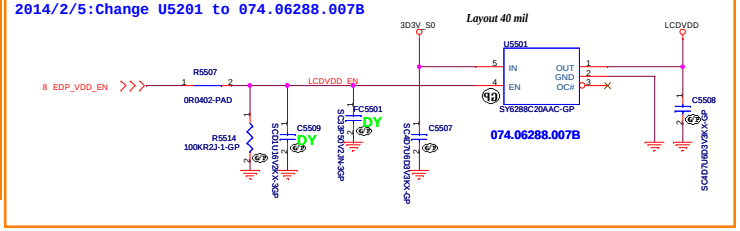
Close to eDP connector



SSID = VIDEO

LCD POWER (Do Not use SW 74.09724.09F)

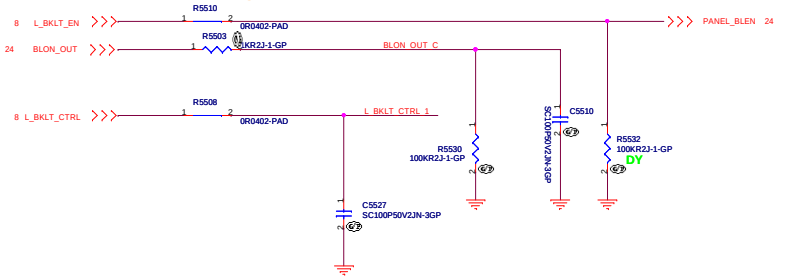
2014/2/5:Change U5201 to 074.06288.007B



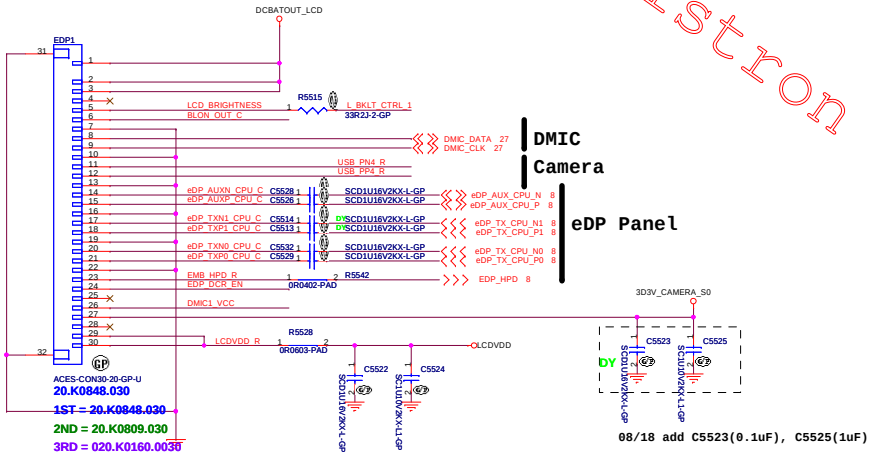
eDP Device

Item	Device
1	eDP Panel
2	Camera
3	DMIC
4	
5	
6	

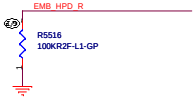
Panel BL brightness/Power En/BL En



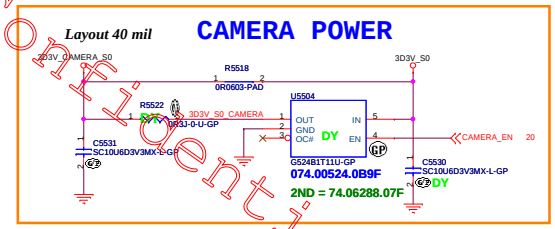
eDP connector

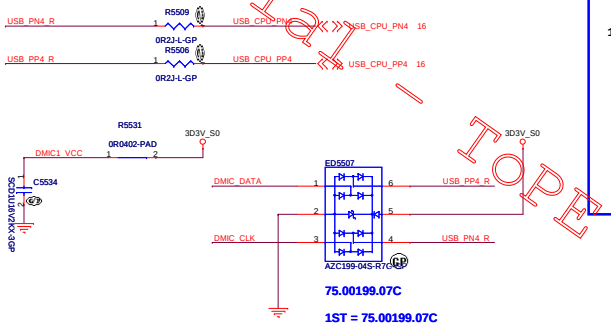


08/18 add C5523(0.1uF), C5525(1uF)

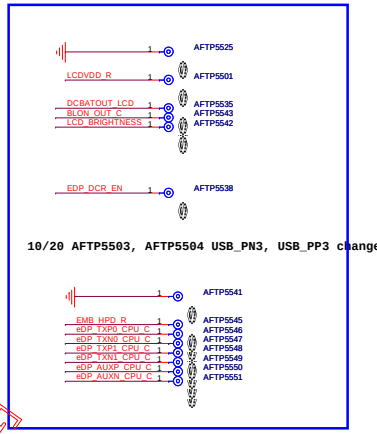


CAMERA POWER





Test point



10/20 AFTP5503, AFTP5504 USB_PN3, USB_PP3 change to USB_PN3_R, USB_PP3_R

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

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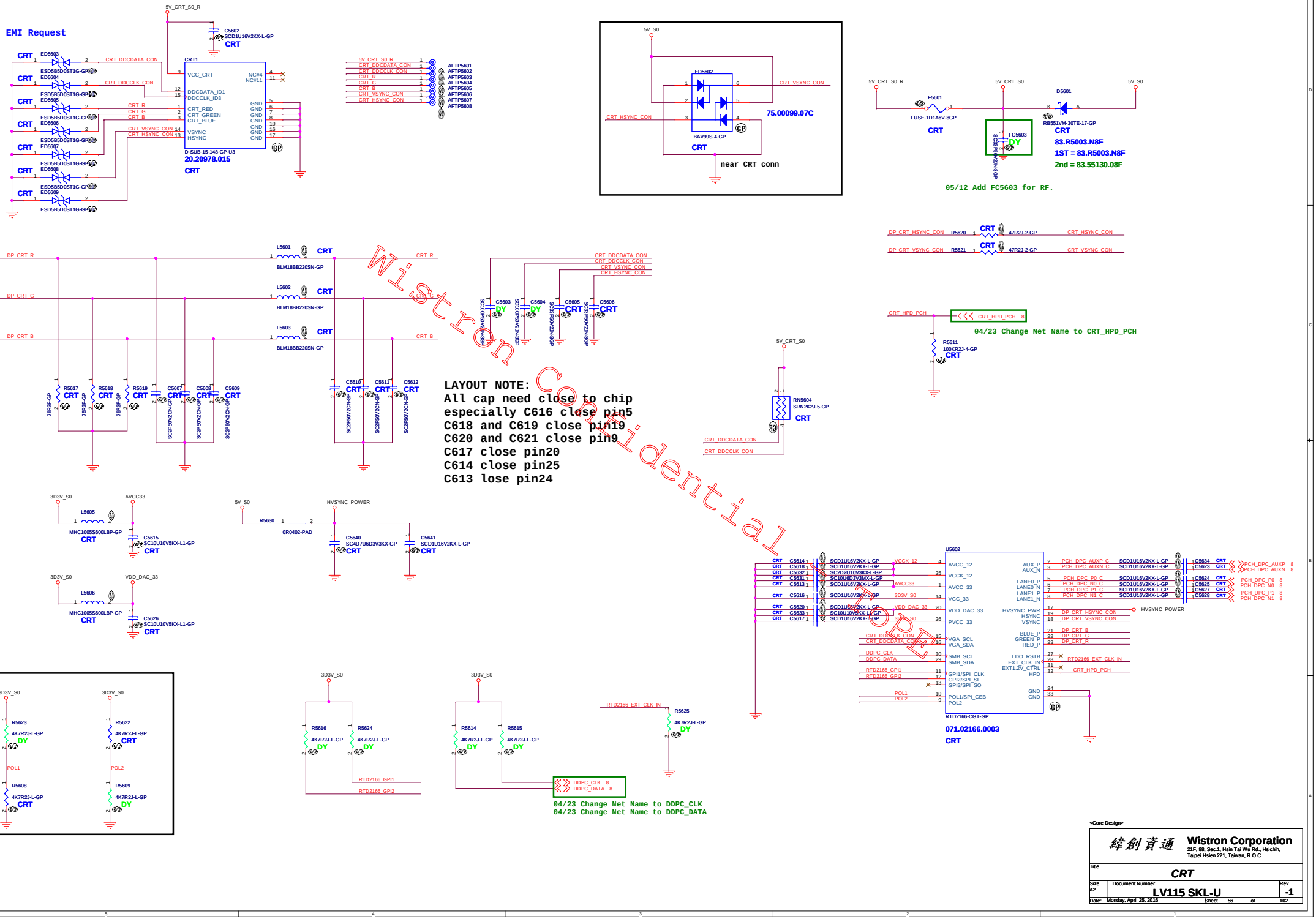
EMI Request
5V_CRT_S0_R
C5602
SCD1U16V2KX-L-GP
CRT
CRT1
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
GND
D-SUB-15-148-GP-U3
20.20978.015
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
CRT_VSYNC_CON
CRT_HSYNC_CON
ESD5B5D0ST1G-GP
AFTP5601
AFTP5602
AFTP5603
AFTP5604
AFTP5605
AFTP5606
AFTP5607
AFTP5608
5V_S0
ED5602
BAV99S-4-GP
75.00099.07C
near CRT conn
F5601
FUSE-1D1A6V-8GP
D5601
RB551VM-30TE-17-GP
FC5603
83.R5003.N8F
1ST = 83.R5003.N8F
2nd = 83.55130.08F
05/12 Add FC5603 for RF.
DP_CRT_R
DP_CRT_G
DP_CRT_B
L5601
L5602
L5603
BLM18BB220SN-GP
R5617
R5618
R5619
C5607
C5608
C5609
C5610
C5611
C5612
C5603
C5604
C5605
C5606
DP_CRT_HSYNC_CON
DP_CRT_VSYNC_CON
R5620
R5621
47R2J-2-GP
CRT_HPD_PCH
R5611
100K2J-4-GP
04/23 Change Net Name to CRT_HPD_PCH
RN5604
SRN2K2J-5-GP
LAYOUT NOTE:
All cap need close to chip
especially C616 close pin5
C618 and C619 close pin19
C620 and C621 close pin9
C617 close pin20
C614 close pin25
C613 lose pin24
Wistron Confidential
3D3V_S0
AVCC33
L5605
MHC1005S600LBP-GP
C5615
SC10U10V5KX-L1-GP
VDD_DAC_33
L5606
C5626
HVSYNC_POWER
R5630
0R0402-PAD
C5640
SC4D7U6D3V3KX-GP
C5641
SCD1U16V2KX-L-GP
U5602
RTD2166-CGT-GP
071.02166.0003
R5623
R5622
4K7R2J-L-GP
POL1
POL2
R5608
R5609
R5616
R5624
R5614
R5615
R5625
RTD2166_GPI1
RTD2166_GPI2
RTD2166_EXT_CLK_IN
DDPC_CLK
DDPC_DATA
04/23 Change Net Name to DDPC_CLK
04/23 Change Net Name to DDPC_DATA
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT
Size
A2
Document Number
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Rev
-1
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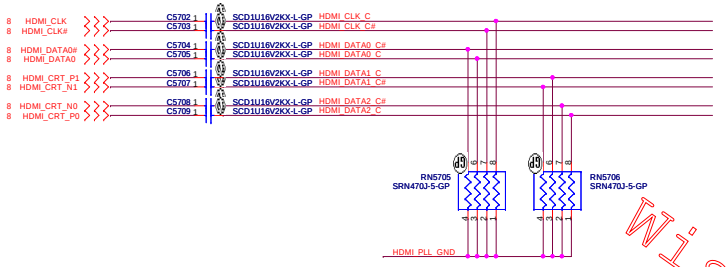
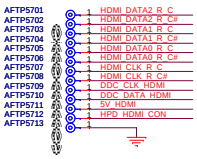
SSID = VIDEO

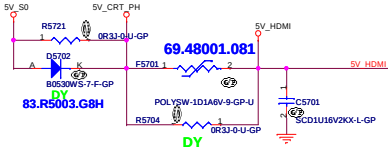
HDMI CONNECTOR

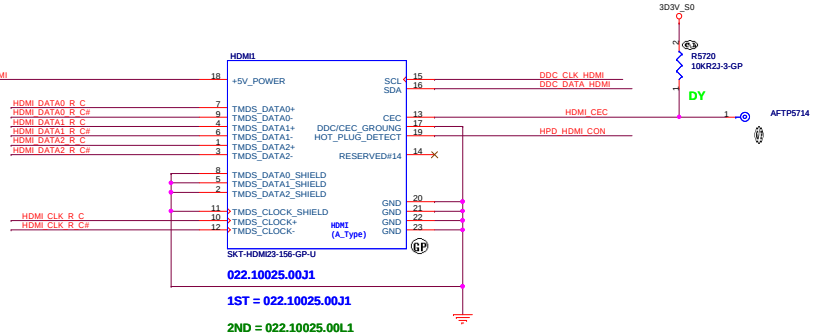
HDMI Passive Level Shifter

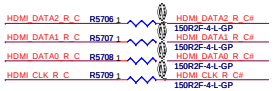
Close to HDMI Connector





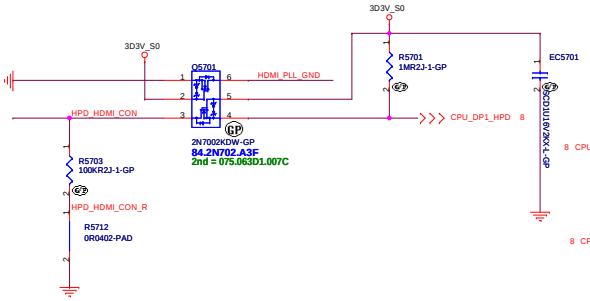


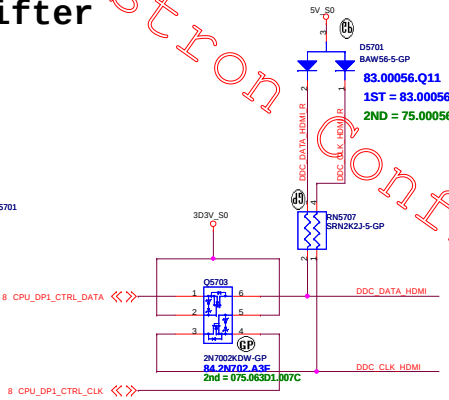


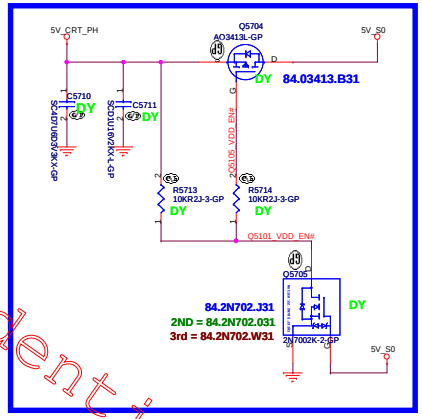


ESD STUFF OPTION
ESD STUFF OPTION
ESD STUFF OPTION
ESD STUFF OPTION

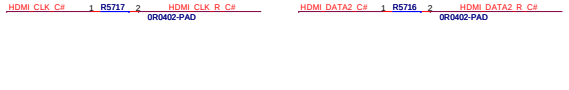
HDMI DDC Passive Level Shifter

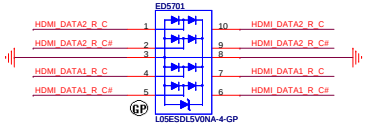


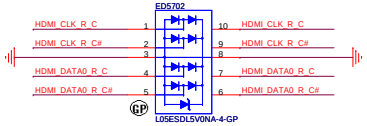


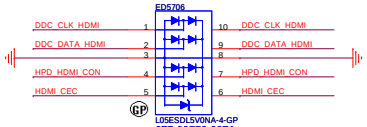


07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31



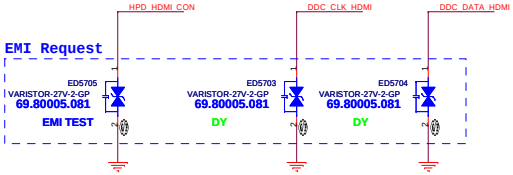






HDMI A type pin define (Total: 19pin)

Pin	Pin定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: A2
Document Number: LV115 SKL-U
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Date: Monday, April 25, 2016
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DP

Size: A1 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 58 of 102

<Core Design>

緯創資通 **Wistron Corporation**
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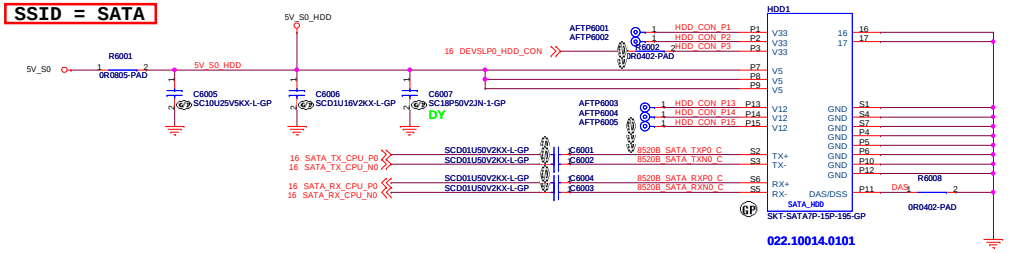
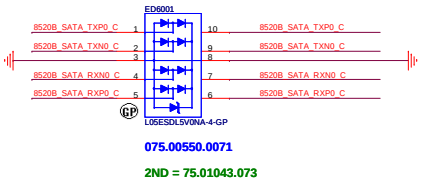
Title: ***Demultiplexer***

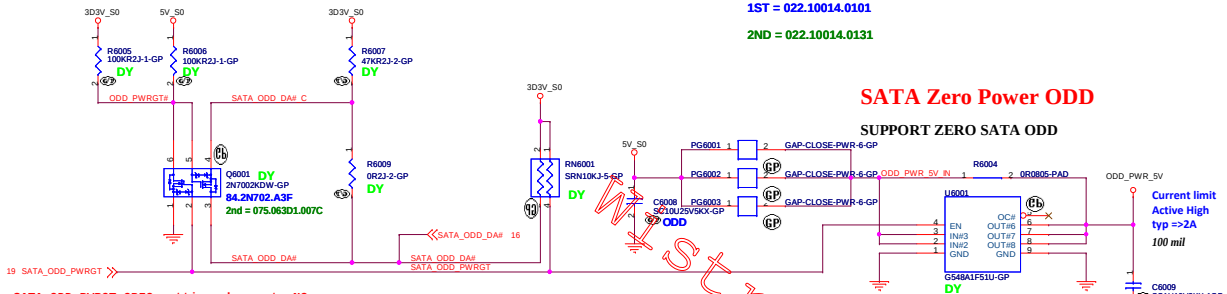
Size	Document Number	Rev
A2	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 59 of 102

SSID = SATA







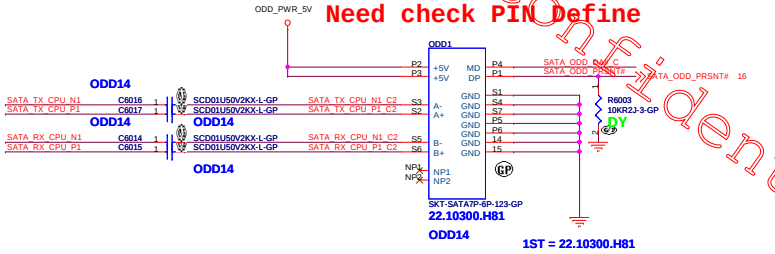
SATA Zero Power ODD

SUPPORT ZERO SATA ODD

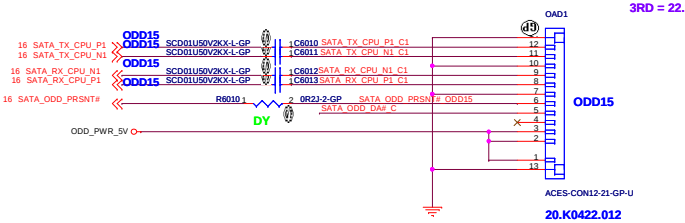
SATA_ODD_PWRGT GPIO setting change to NC
2016/4/21

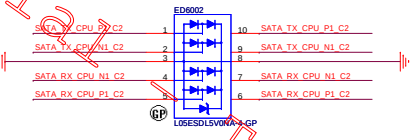
2015/10/3
Change Switch IC to 74.00548.A79

Need check PIN Define



1ST = 22.10300.H81
2ND = 22.10300.H31
3RD = 22.10300.H61





<Core Design>

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Title: SATA IF HDD/ODD

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

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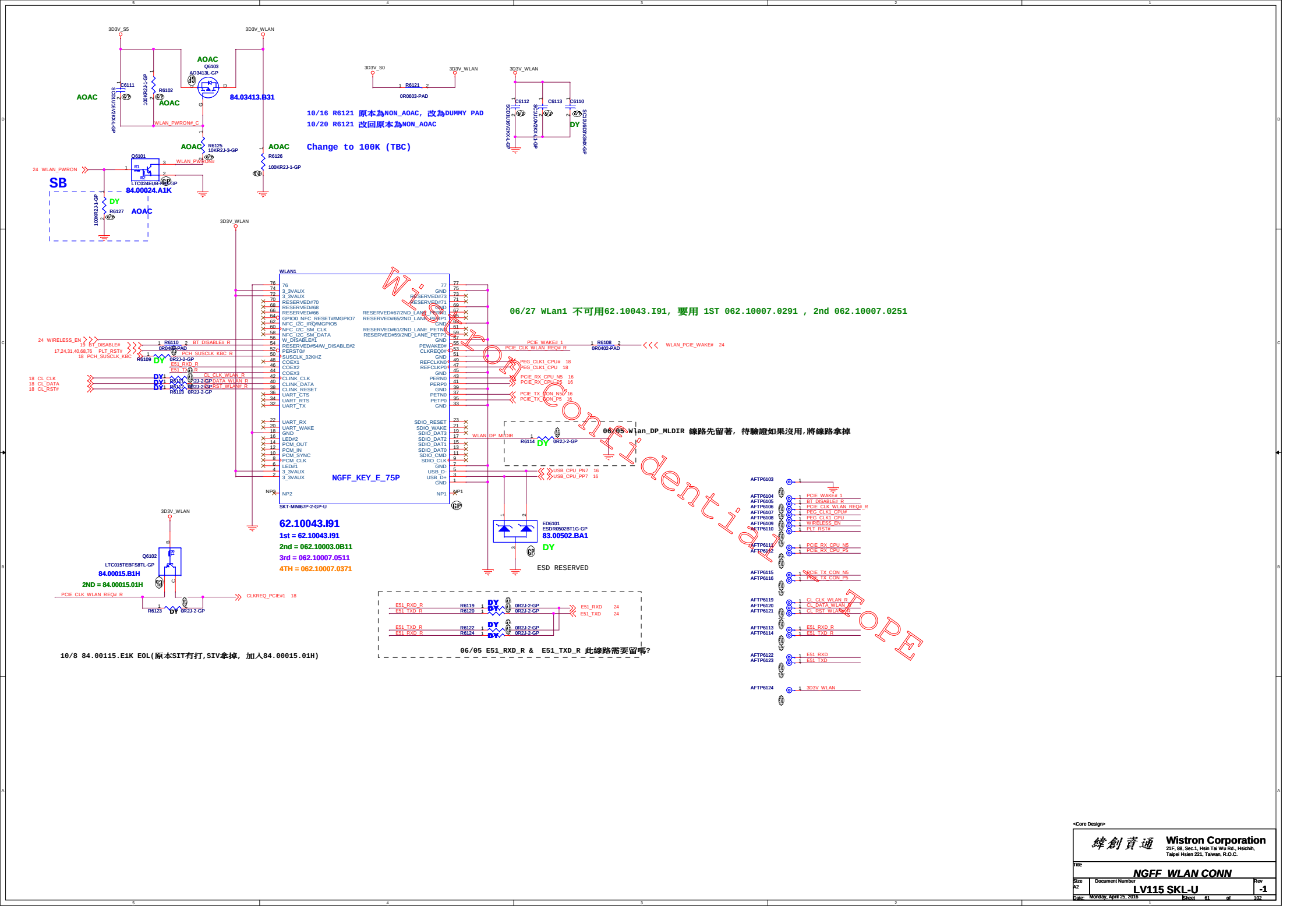

<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 61 of 102

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<Core Design>

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Title

RESERVED

Size	Document Number	Rev
A4	LV115 SKL-U	-1

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
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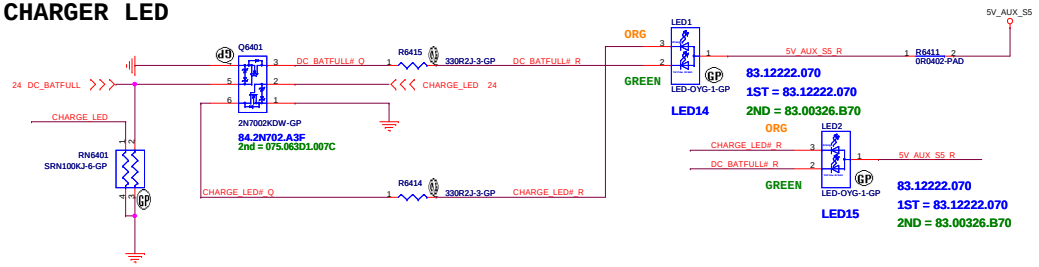
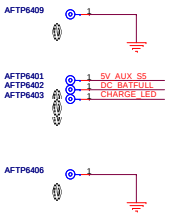
Test point

CHARGER LED

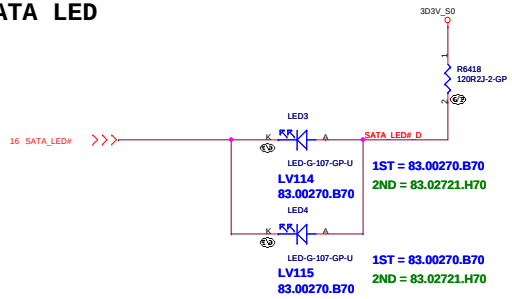


Forward Current	I_F	S2:25 G6:25	mA

Chip		Emitted Color	Resin Color
Type	Material		
S2	AlGaInP	Brilliant Orange	Water Clear
G6	AlGaInP	Brilliant Yellow Green	



SATA LED



<Core Design>

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Title: LED Board&Power Button

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

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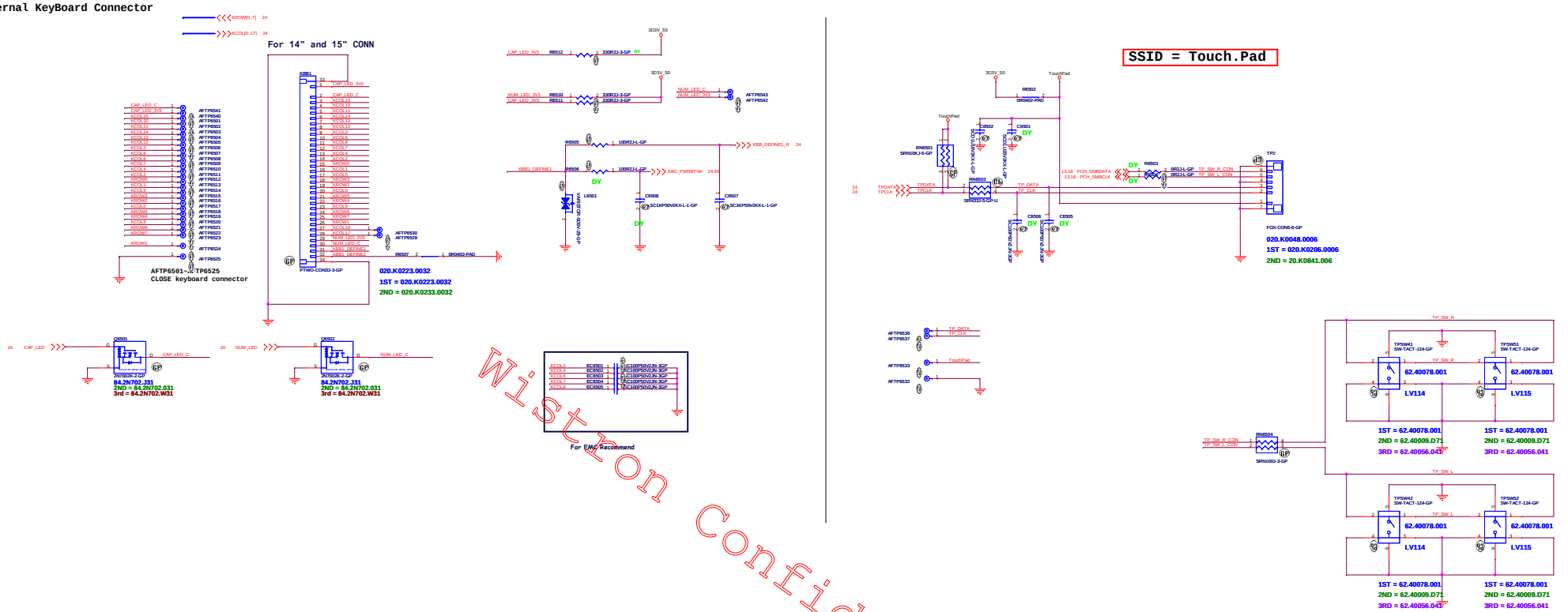
Internal KeyBoard Connector



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Key Board&Touch Pad

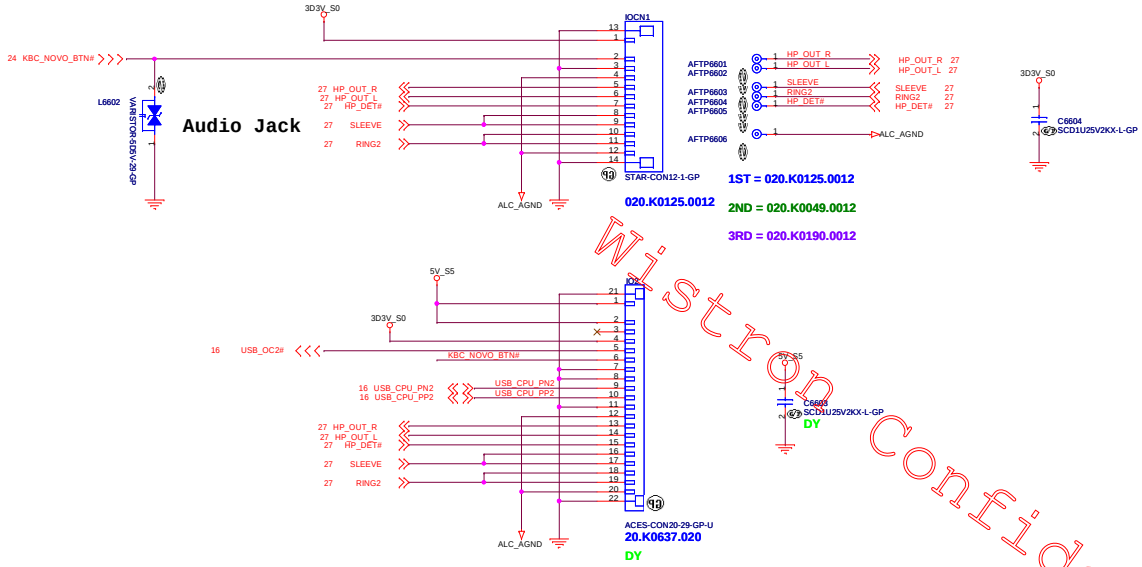
LV115 SKL-U

-1

IO BD Device

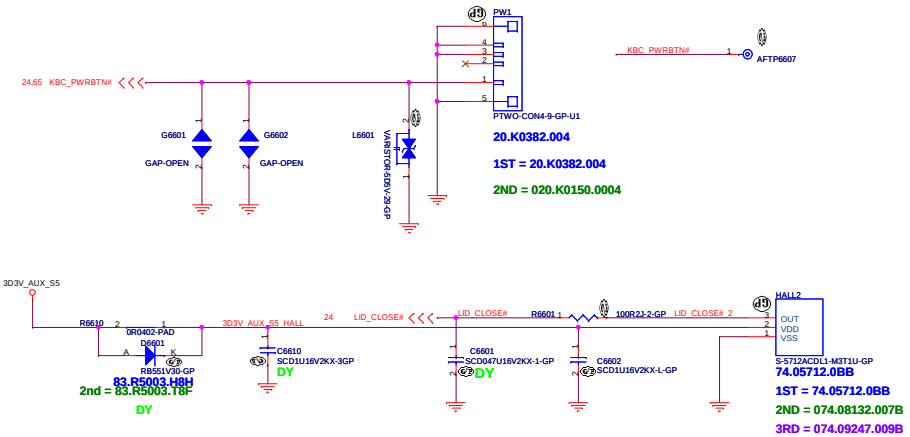
Item	Device
1	
2	
3	
4	

IO BD connector



PWR BTN BD connector

Modified Pin Define and PN 20151208



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board Connector*

Size	Document Number	Rev
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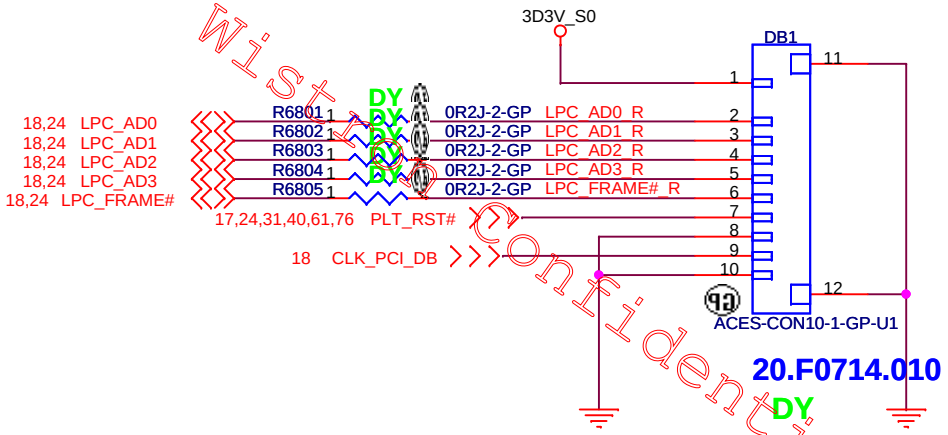
Main Func = Debug

Debug Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug connector*

Size	Document Number	Rev
A4	LV115 SKL-U	-1

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: G Sensor

Size	Document Number	Rev
A3	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 70 of 102

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	LV115 SKL-U	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A3	LV115 SKL-U	-1

Date: Monday, April 25, 2016 Sheet 72 of 102

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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A3	LV115 SKL-U	-1

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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A3	LV115 SKL-U	-1

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<Core Design>

緯創資通 Wistron Corporation
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Title: ***Reserved***

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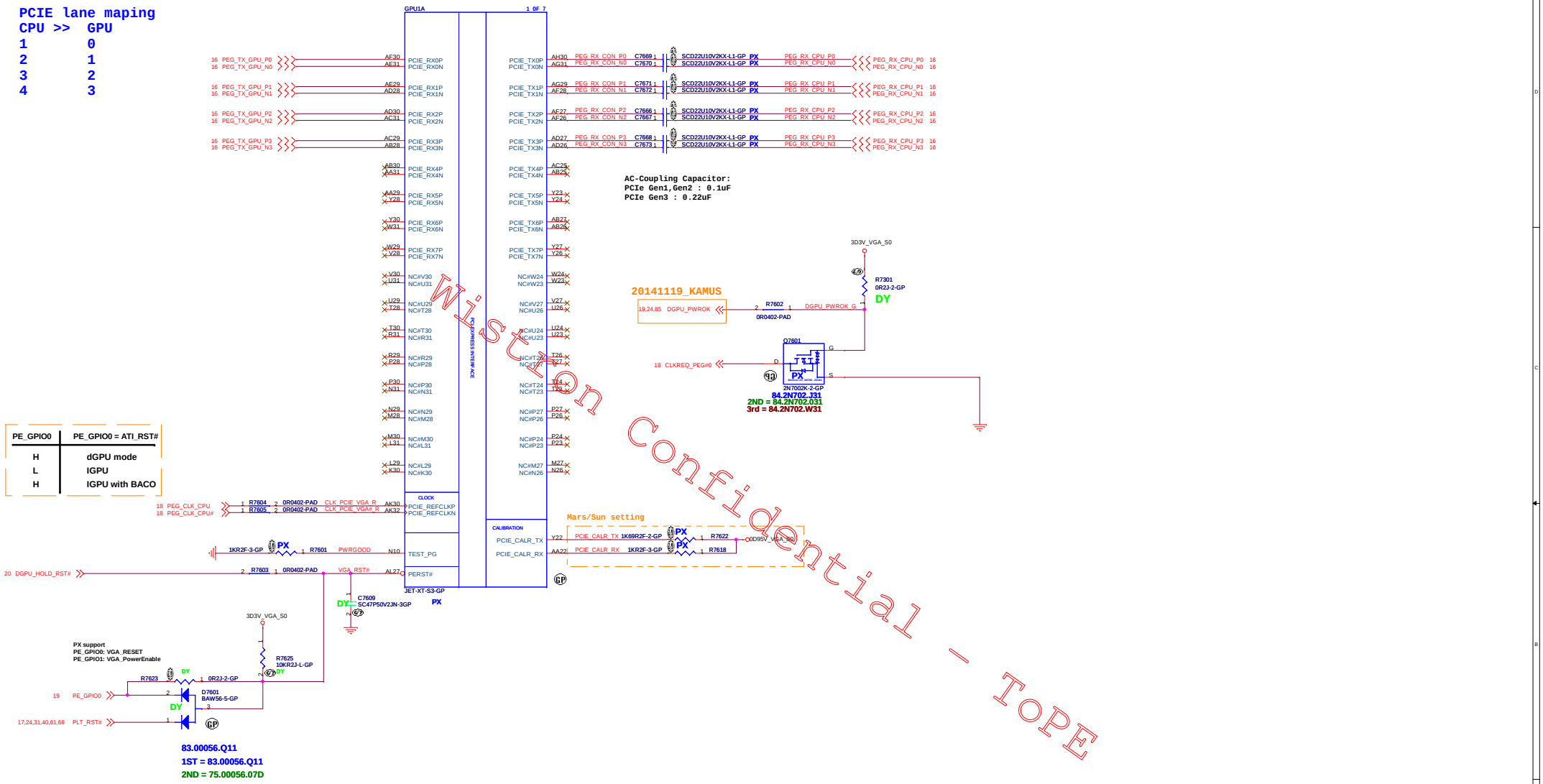
PCIE lane maping

CPU >>	GPU
1	0
2	1
3	2
4	3



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5) PEG

Size	Document Number	Rev
A2	LV115 SKL-U	-1

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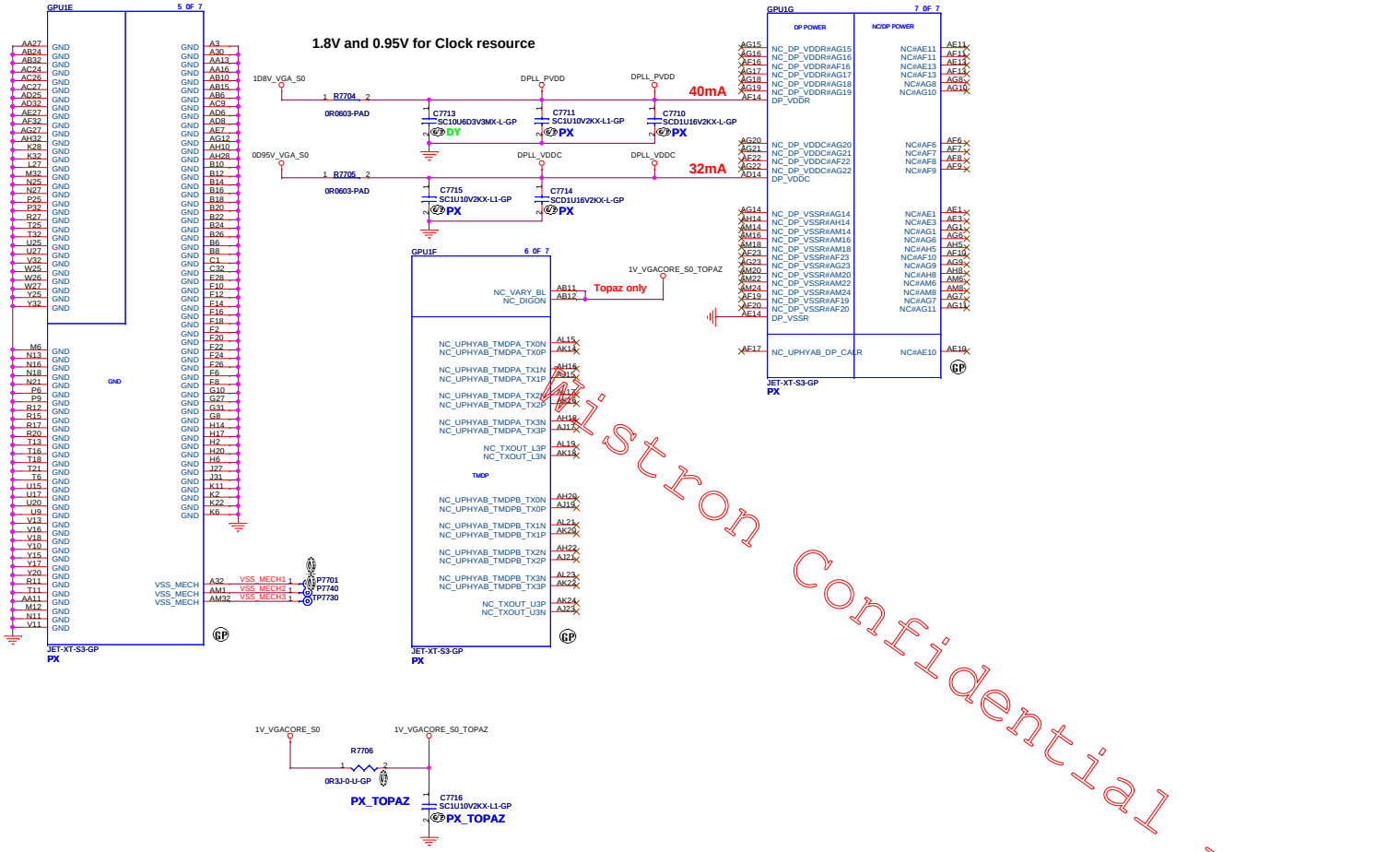

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (2/5) DIGITALOUT

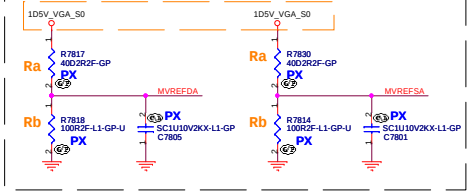
Size: A2 | Document Number: LV115 SKL-U | Rev: -1

Date: Monday, April 25, 2016 | Sheet 77 of 102

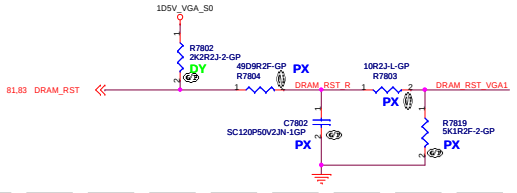
Please MVREF drivers and Caps close to ASIC

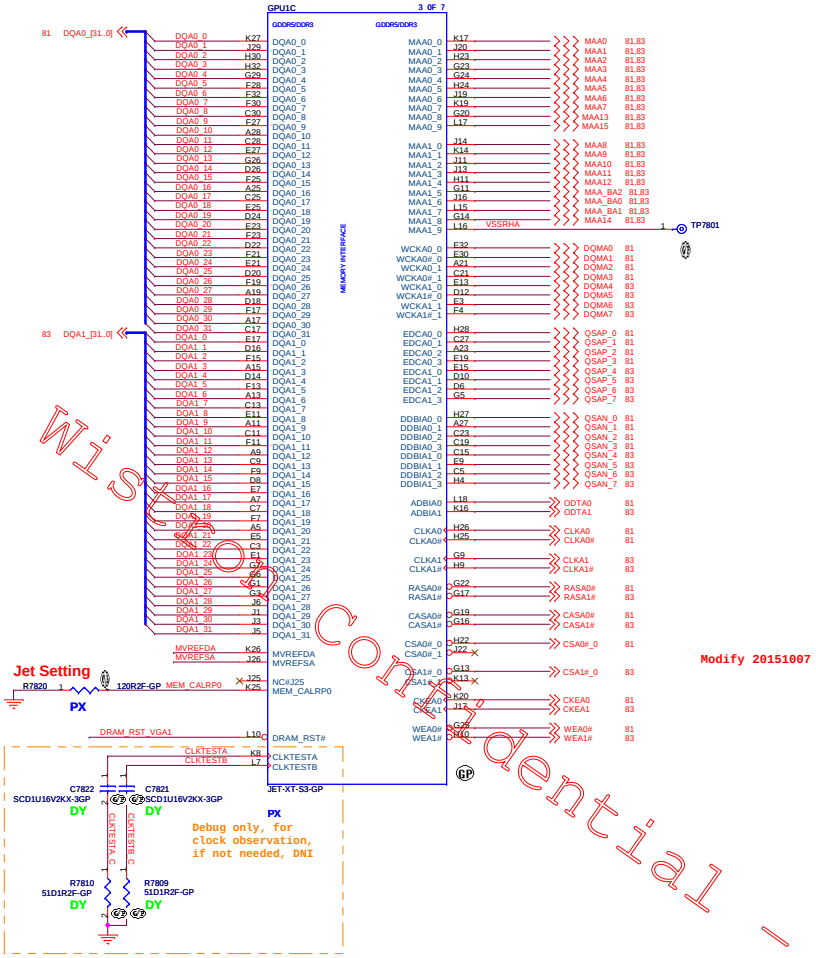
DDR3/GDDR3 Memory Stuff Option(JET/TOPAZ)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5





Jet Setting

Modify 20151007

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5) VRAM I/F

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

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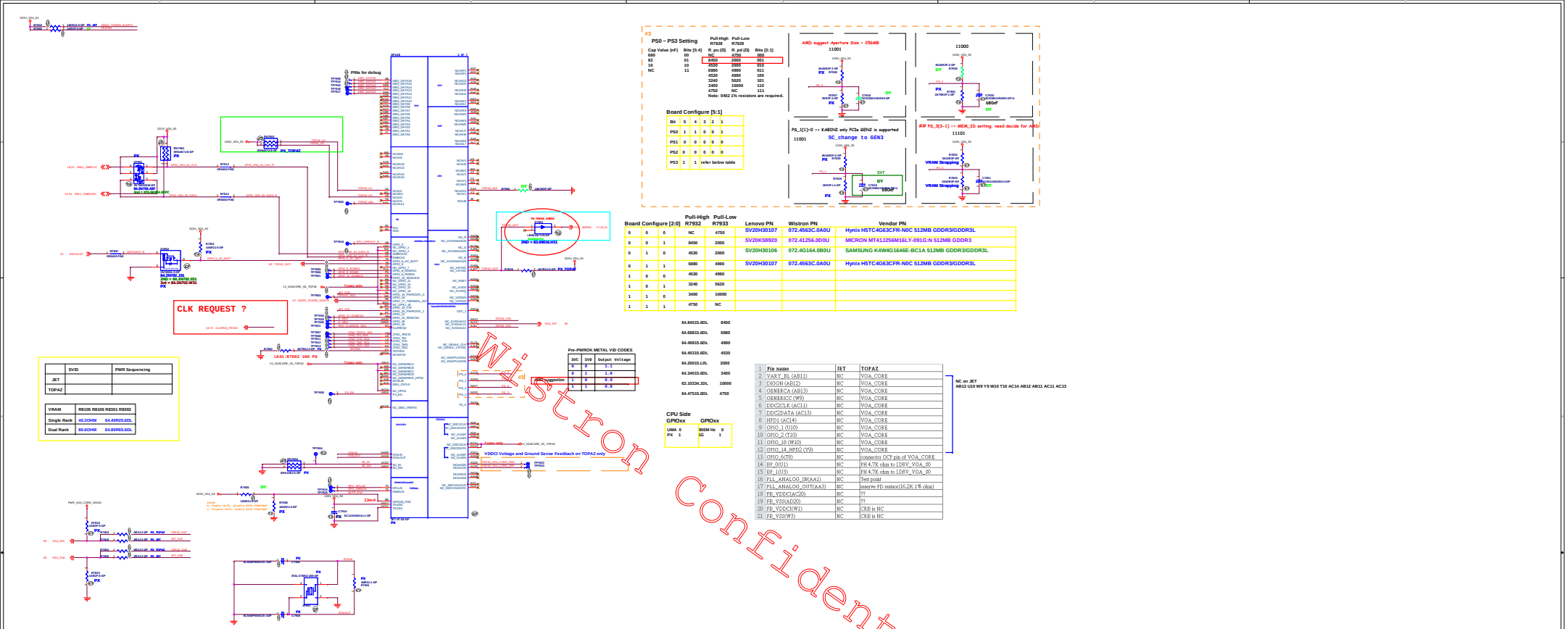

PS0 – PS3 Setting

Cap Value (nF)	Bits [5:4]	Pull-High R7928 R_pu (Ω)	Pull-Low R7929 R_pd (Ω)	Bits [3:1]
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6080	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

Note: 0402 1% resistors are required.

Board Configure [5:1]

Bit	5	4	3	2	1
PS0	1	1	0	0	1
PS1	0	0	0	0	0
PS2	0	0	0	0	0
PS3	1	1	refer below table		

Board Configure [2:0]

			Pull-High R7932	Pull-Low R7933	Lenovo PN	Wistron PN	Vendor PN
0	0	0	NC	4750	SV20H30107	072.4563C.0A0U	Hynix H5TC4G63CFR-N0C 512MB GDDR3/GDDR3L
0	0	1	8450	2000	SV20K59920	072.41256.0D0U	MICRON MT41J256M16LY-091G:N 512MB GDDR3
0	1	0	4530	2000	SV20H30106	072.4G164.0B0U	SAMSUNG K4W4G1646E-BC1A 512MB GDDR3/GDDR3L
0	1	1	6080	4990	SV20H30107	072.4563C.0A0U	Hynix H5TC4G63CFR-N0C 512MB GDDR3/GDDR3L
1	0	0	4530	4990			
1	0	1	3240	5620			
1	1	0	3400	10000			
1	1	1	4750	NC			

	SVID	PWR Sequencing
JET		
TOPAZ		

VRAM	R8105 R8106 R8301 R8302
Single Rank	40.2OHM 64.40R25.6DL
Dual Rank	80.6OHM 64.80R65.6DL

64.84515.6DL	8450
64.69815.6DL	6980
64.49915.6DL	4990
64.45315.6DL	4530
64.20015.L0L	2000
64.34015.6DL	3400
63.10334.1DL	10000
64.47515.6DL	4750

CPU Side GPIOxx

GPIOxx		GPIOxx	
UMA	0	900M Hz	0
PX	1	XG	1

	Pin name	JET	TOPAZ
1	VARY_BL (AB11)	NC	VGA_CORE
2	DIOOM (AB12)	NC	VGA_CORE
3	GENERICA (AB13)	NC	VGA_CORE
4	GENERICC (W9)	NC	VGA_CORE
5	DDC2CLK (AC11)	NC	VGA_CORE
6	DDC2DATA (AC13)	NC	VGA_CORE
7	HPD1 (AC14)	NC	VGA_CORE
8	GPIO_1 (U10)	NC	VGA_CORE
9	GPIO_2 (T10)	NC	VGA_CORE
10	GPIO_18 (W10)	NC	VGA_CORE
11	GPIO_I4_HPD2 (Y9)	NC	VGA_CORE
12	GPIO_0(T8)	NC	connector OCP pin of VGA_CORE
13	BP_0(U1)	NC	PH 4.7K ohm to 1D6V_VGA_IO
14	BP_1(U3)	NC	PH 4.7K ohm to 1D6V_VGA_IO
15	PLL_ANALOG_IN(AA1)	NC	Test point
16	PLL_ANALOG_OUT(AA3)	NC	reserve FD resistor(16.2K 1% ohm)
17	FB_VDDCI(AC20)	NC	??
18	FB_VSS(AD20)	NC	??
19	FB_VDDCI(W1)	NC	CRB is NC
20	FB_VSRW(W3)	NC	CRB is NC

NC on JET
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13

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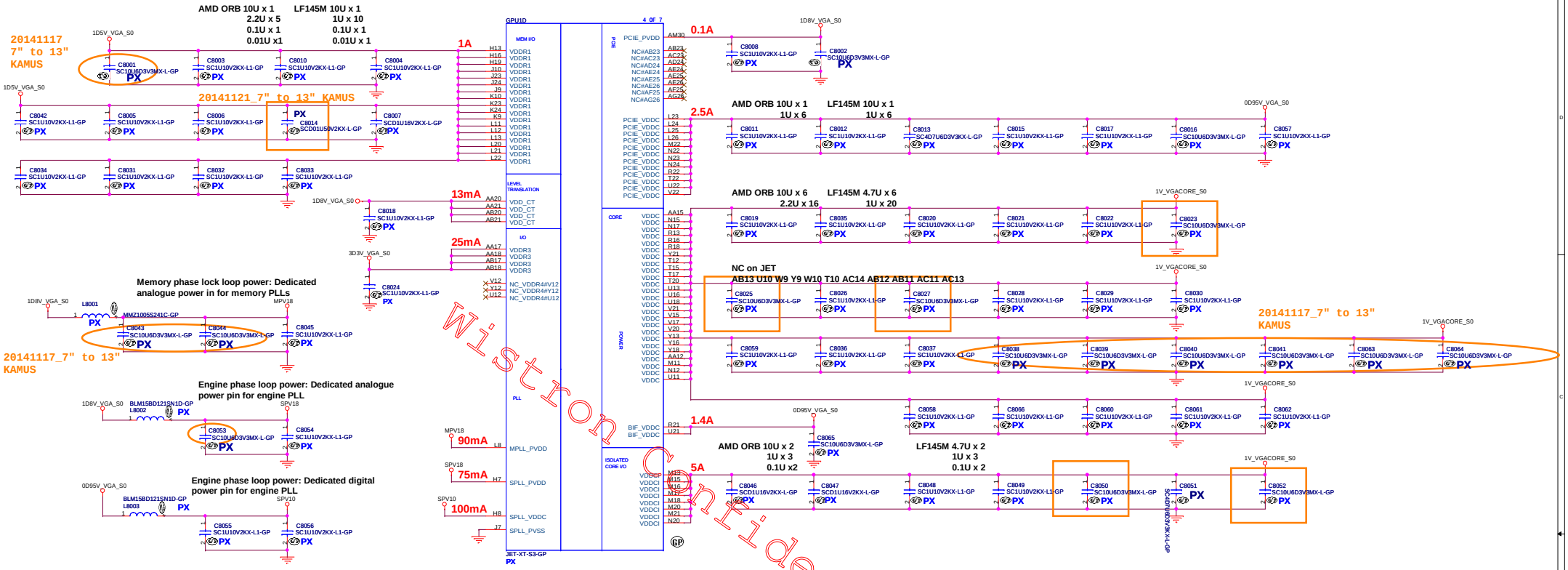
GPU (4/5) GPIOSTRAP

LV115 SKL-U

-1



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Title: GPU (5/5) PWR/GND

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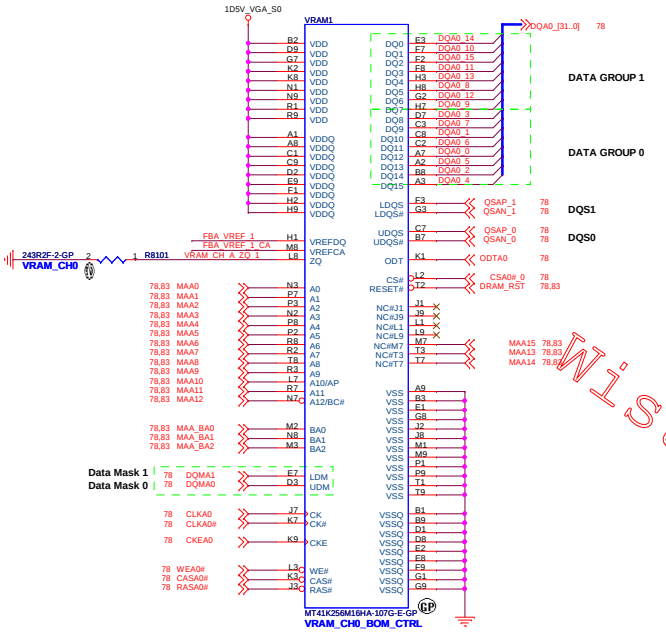
Channel 0 DATA0:15



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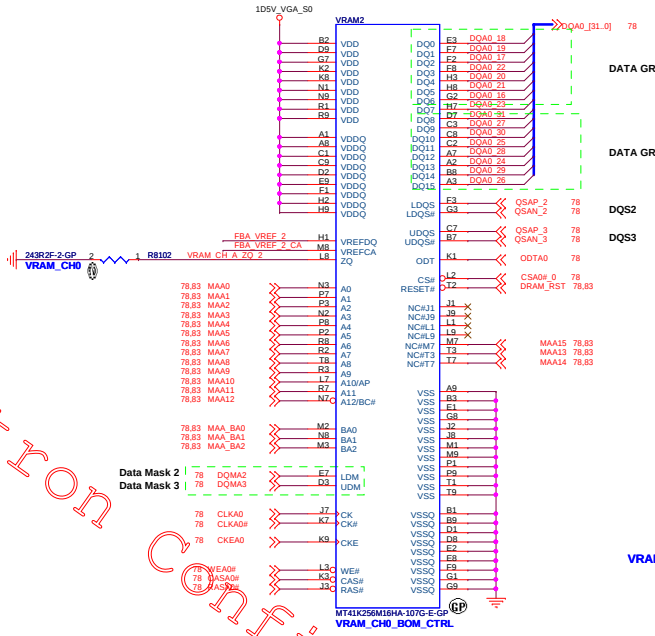

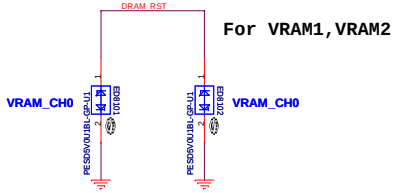

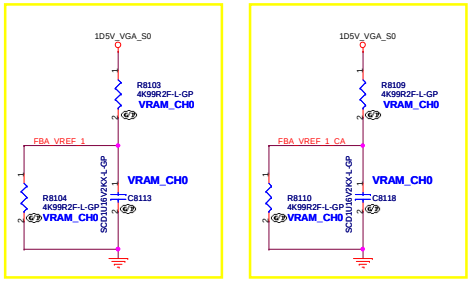

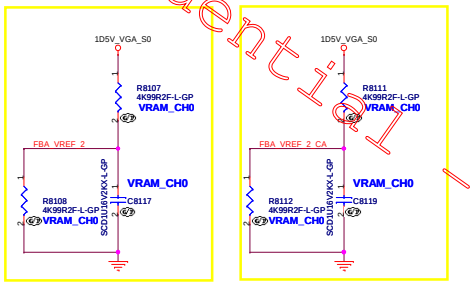

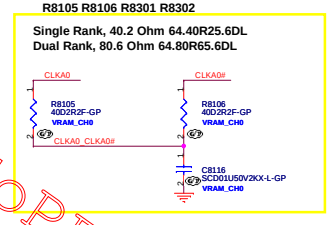

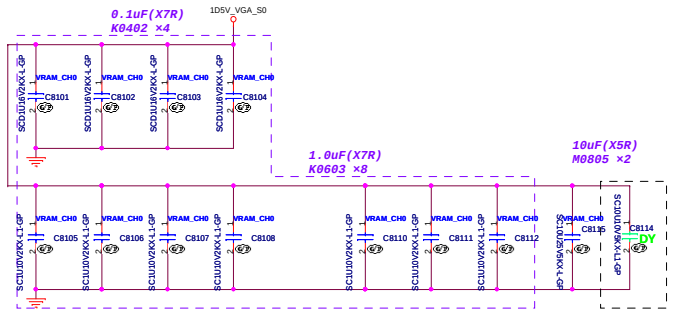

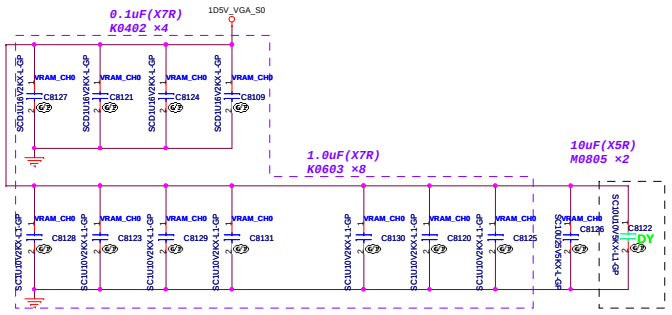

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Title: ***VRAM3,4 (2/4)***

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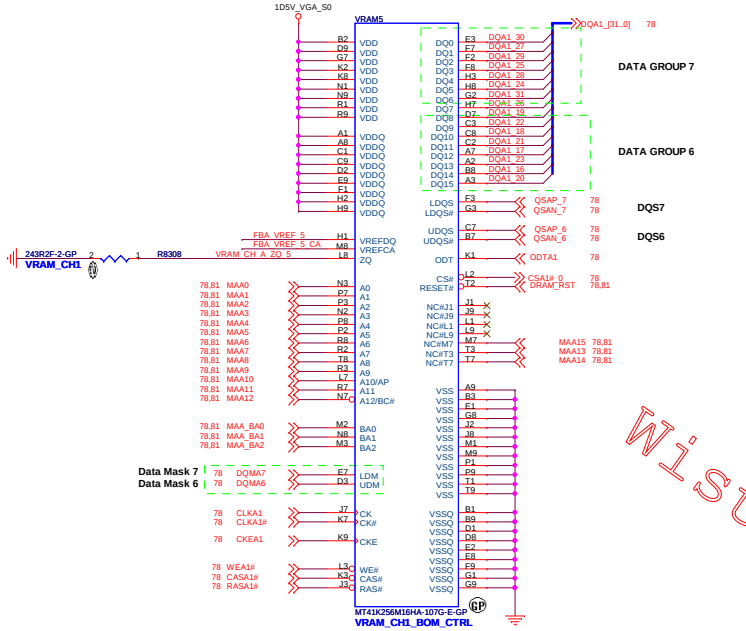

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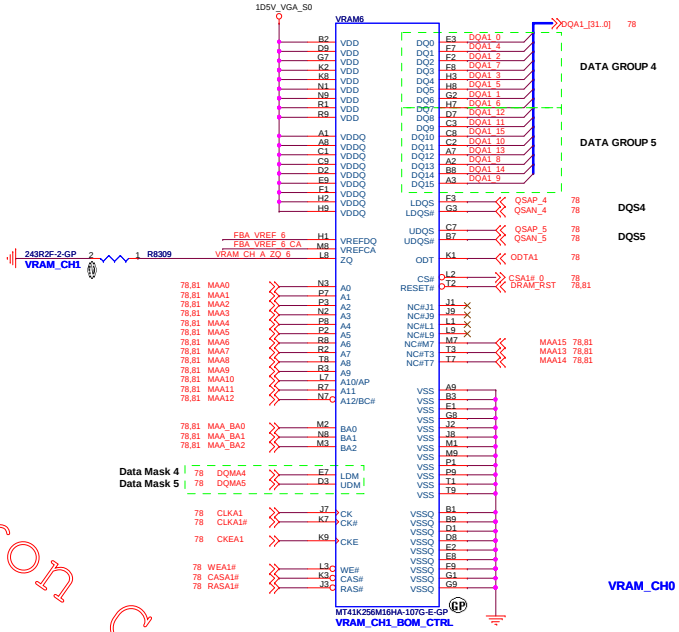

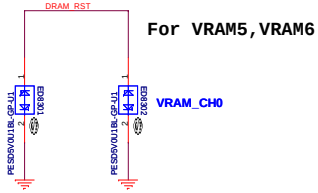

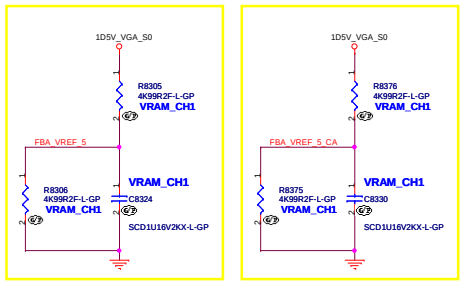

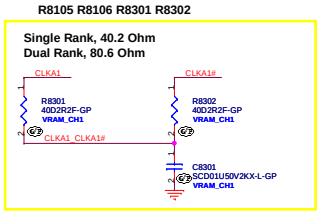

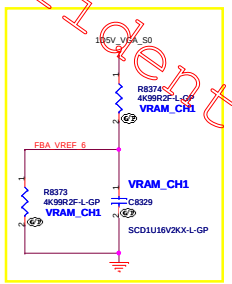

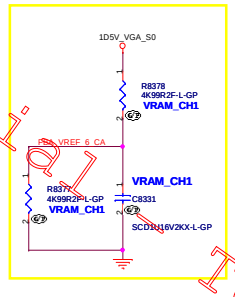

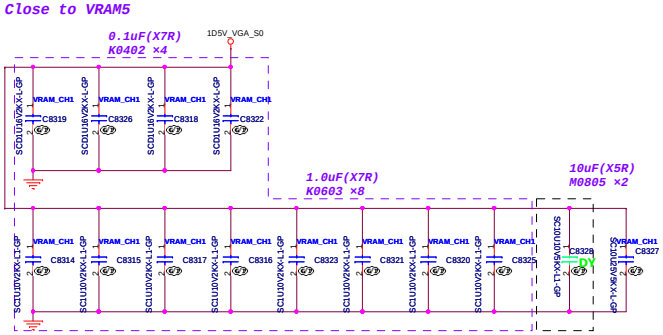

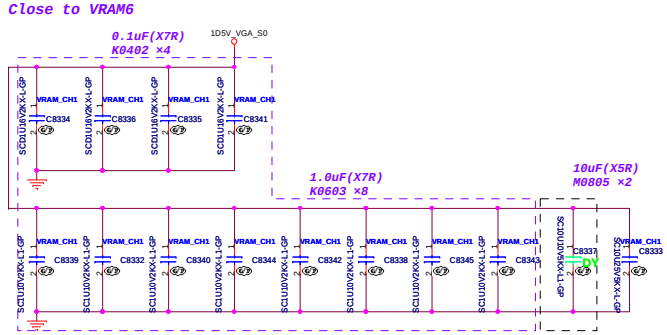

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Title: VRAM5,6 (3/4)

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Title: ***VRAM7,8 (4/4)***

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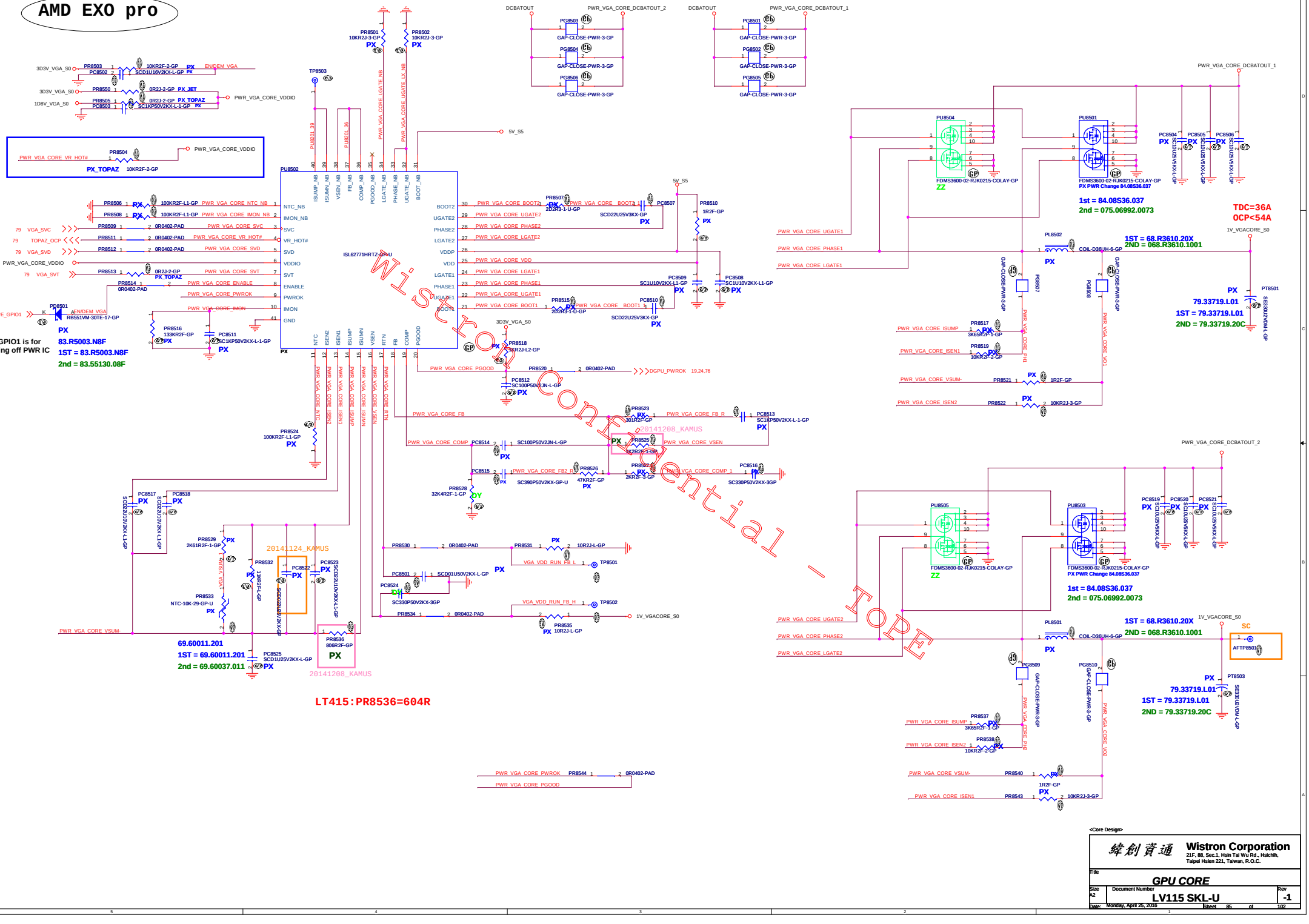
AMD EXO pro


PU8502
ISL62771HRTZ-GP-U
PU8504
PU8501
PU8505
PU8503
PE_GPIO1 is for turning off PWR IC
PX
83.R5003.N8F
1ST = 83.R5003.N8F
2nd = 83.55130.08F
69.60011.201
1ST = 69.60011.201
2nd = 69.60037.011
20141124_KAMUS
20141208_KAMUS
LT415:PR8536=604R
TDC=36A
OCP<54A
1ST = 84.08S36.037
2nd = 075.06992.0073
1ST = 68.R3610.20X
2ND = 068.R3610.1001
79.33719.L01
1ST = 79.33719.L01
2ND = 79.33719.20C
FDMS3600-02-RJK0215-COLAY-GP
ZZ
PX PWR Change 84.08S36.037
Wistron Confidential - Top
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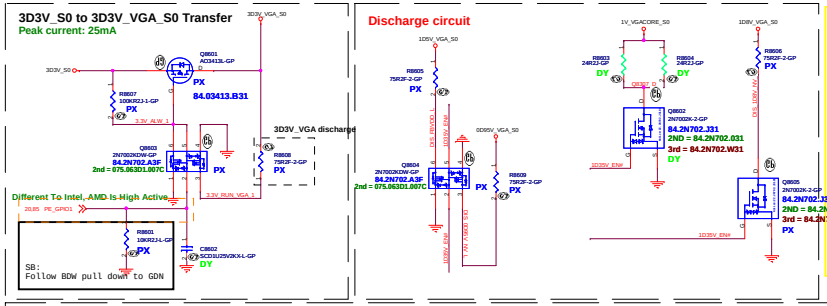
GPU CORE
LV115 SKL-U
Monday, April 25, 2016

20151106 need Add MOS to Control 1D35V_EN# IN SB version



GPU PWR Sequencing
3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

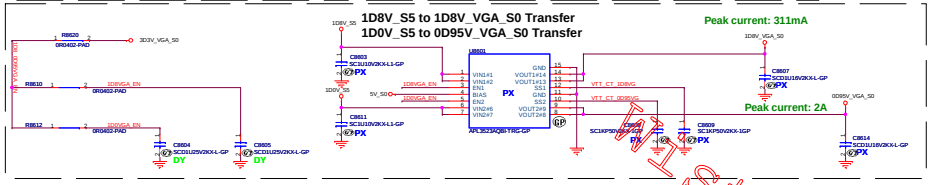
=> 1D35V_VGA_S0

=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

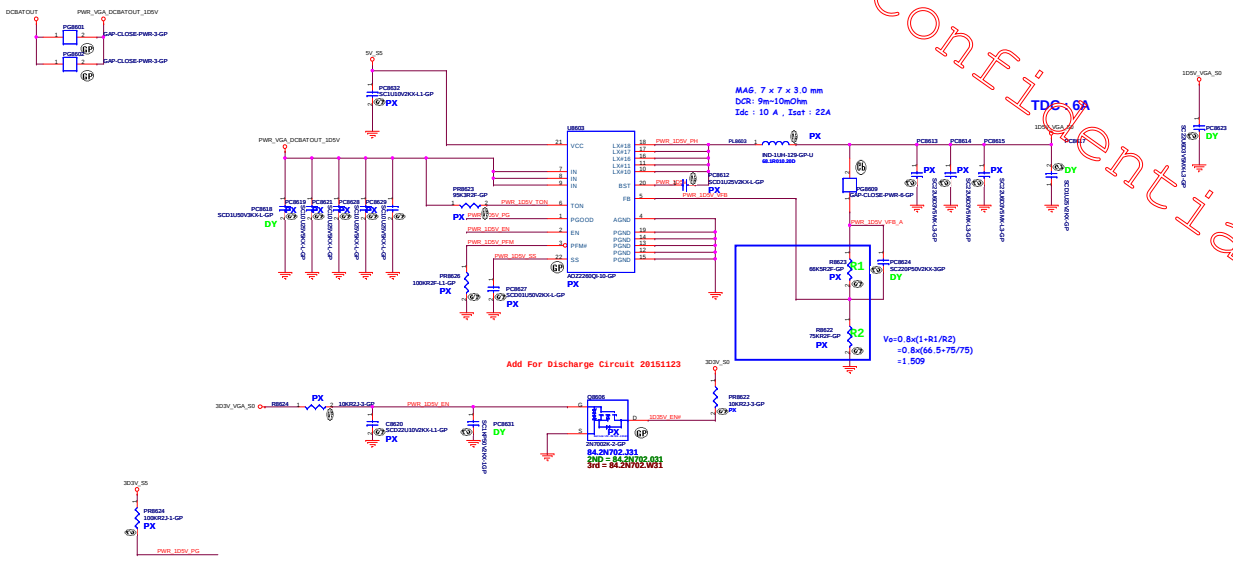
It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



NN30331A for VGA_1D5V(For VRAM DDR3)

Reference OSLO 1D5V_VGA_S0



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Title: ***Reserved***

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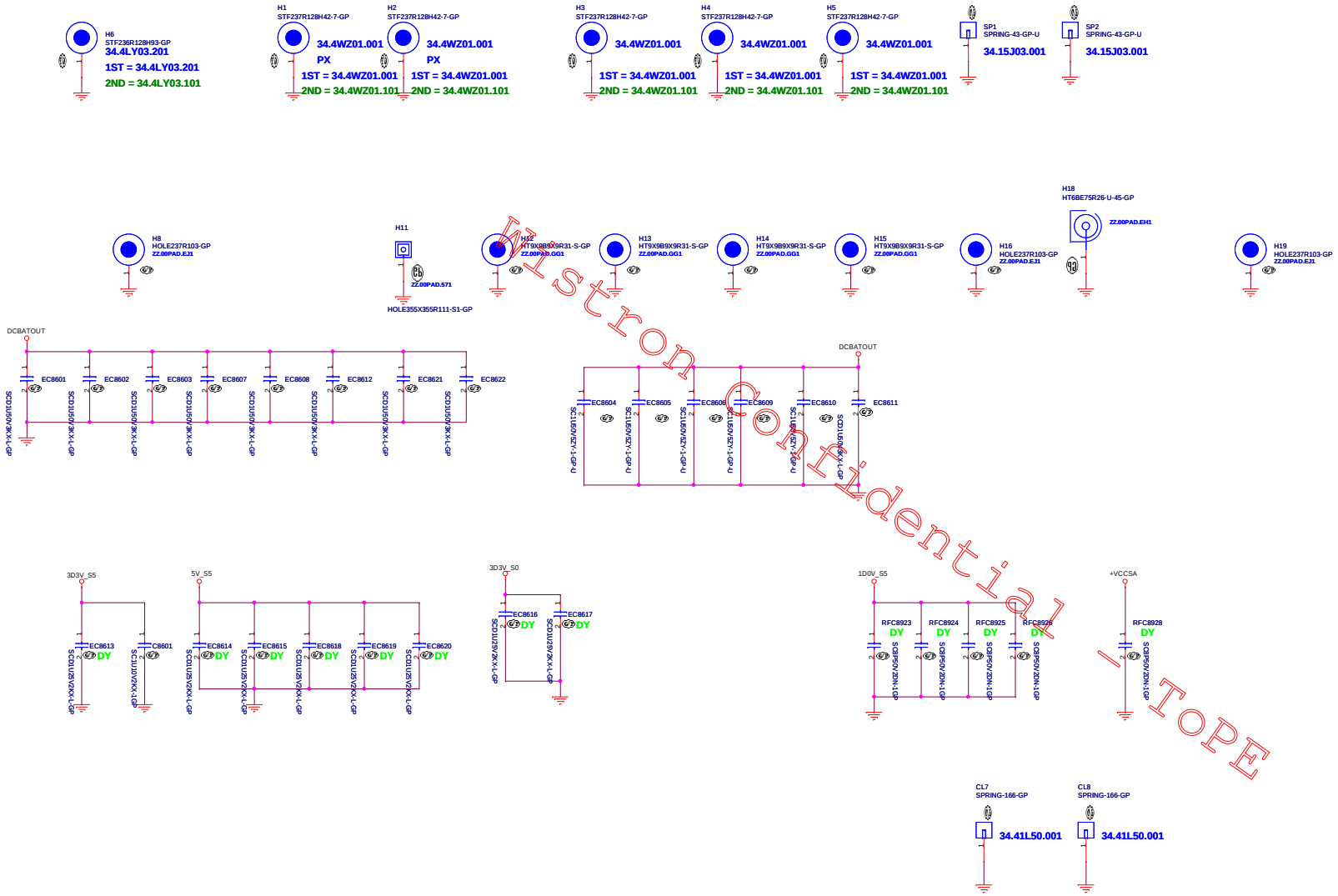

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Title: ***UNUSED PARTS/EMI Capacitors***

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Title: *NFC (Reserved)*

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Title: ***TPM***

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SSID = Finger Print

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Title

Finger Print

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Title: ***Reserved***

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Title: ***LAN SWITCH***

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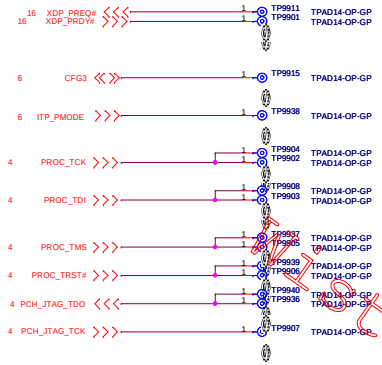

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Title: Reserved

Size: A2 | Document Number: LV115 SKL-U | Rev: -1

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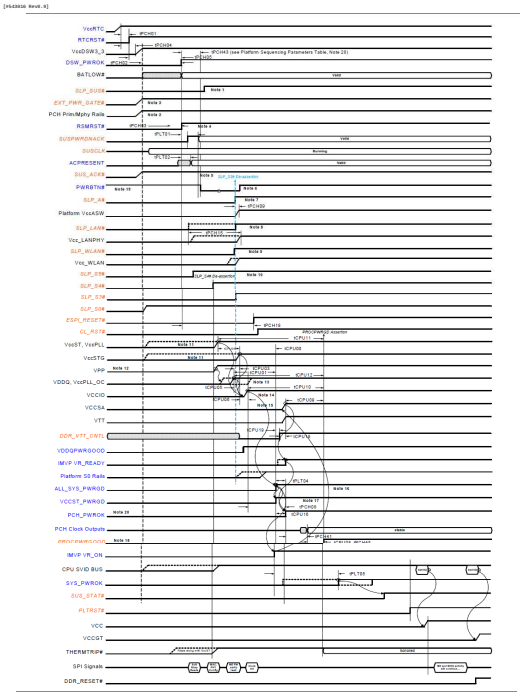
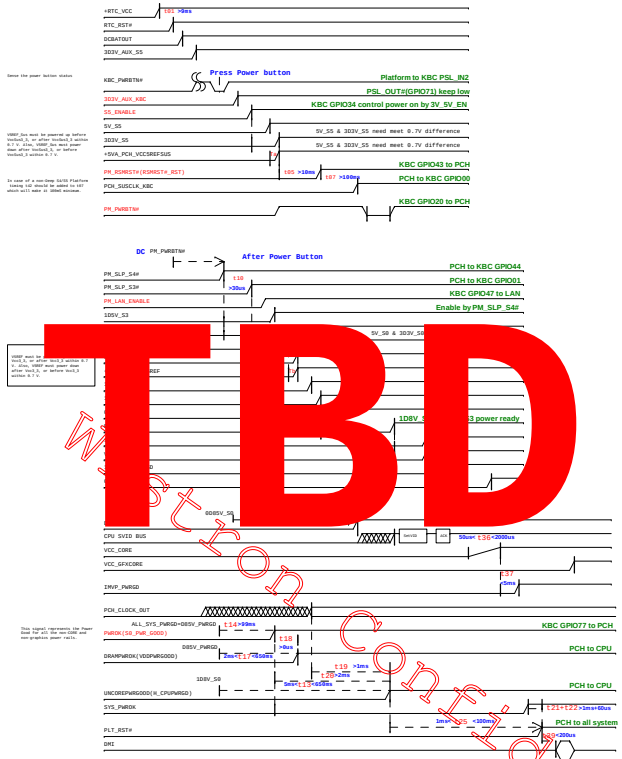
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

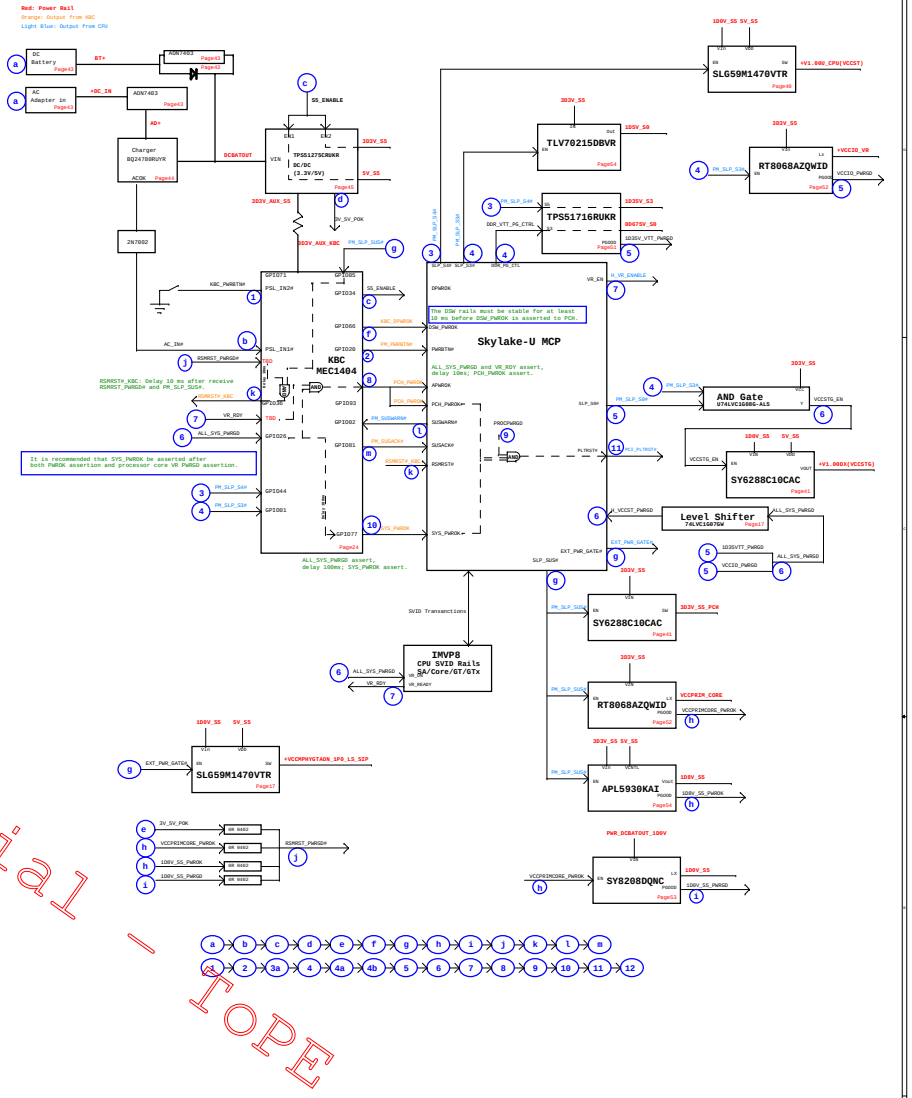


(DC mode)

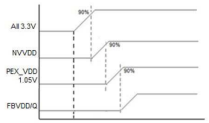
Red Words: Controlled by EC GPIO



Skylake POWER UP SEQUENCE DIAGRAM



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:

- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

POWER SEQUENCE
LV11S SKL-U

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Title: **Power Block Diagram**

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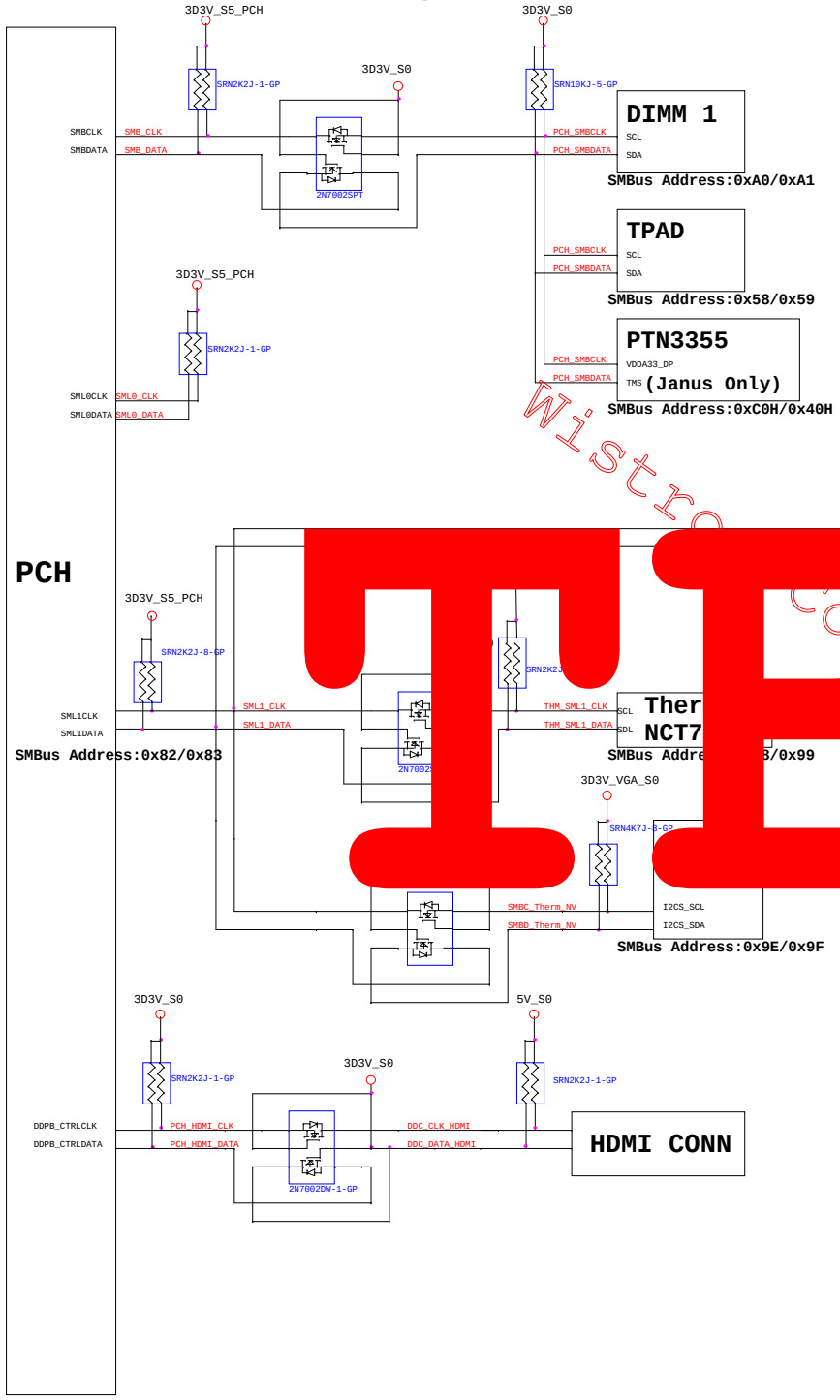
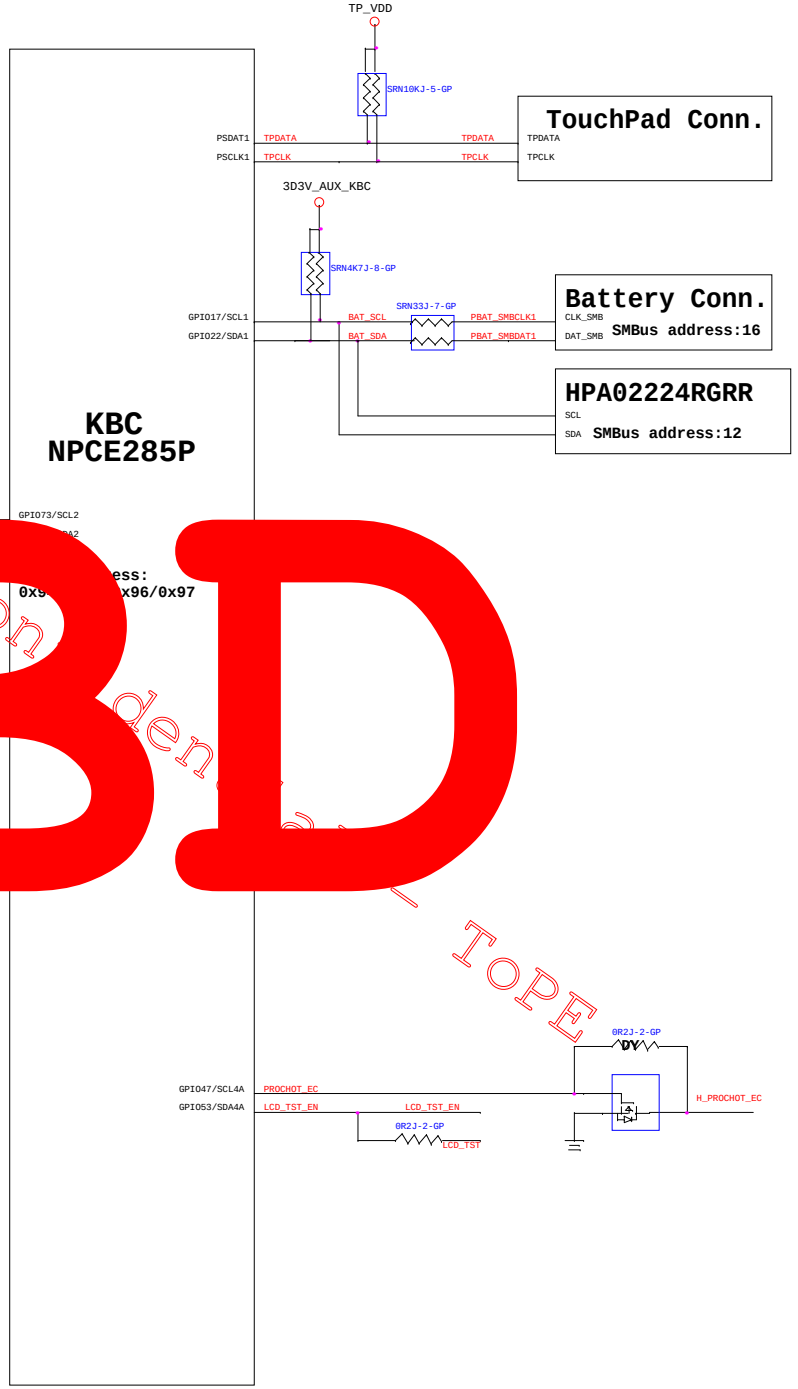
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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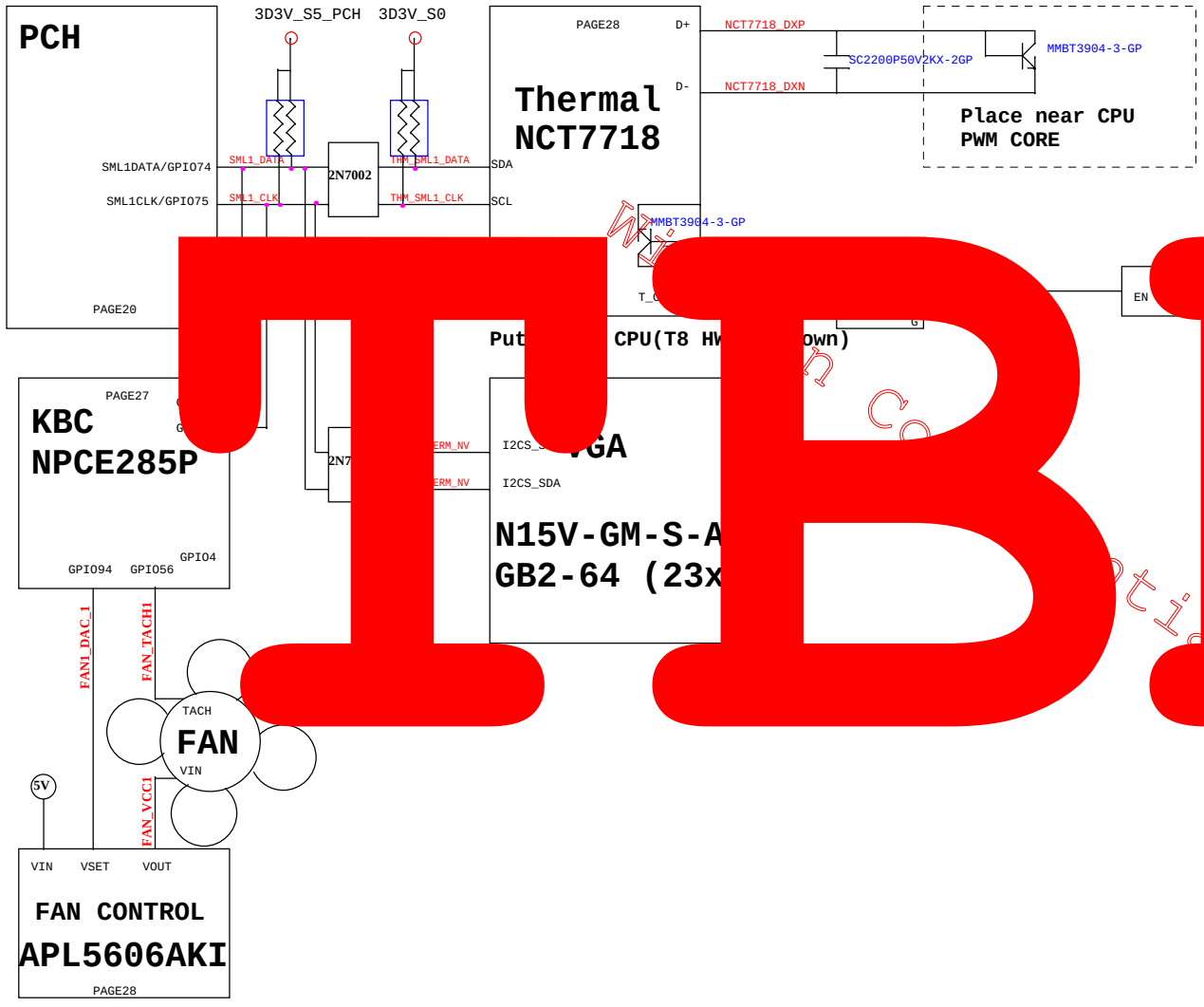
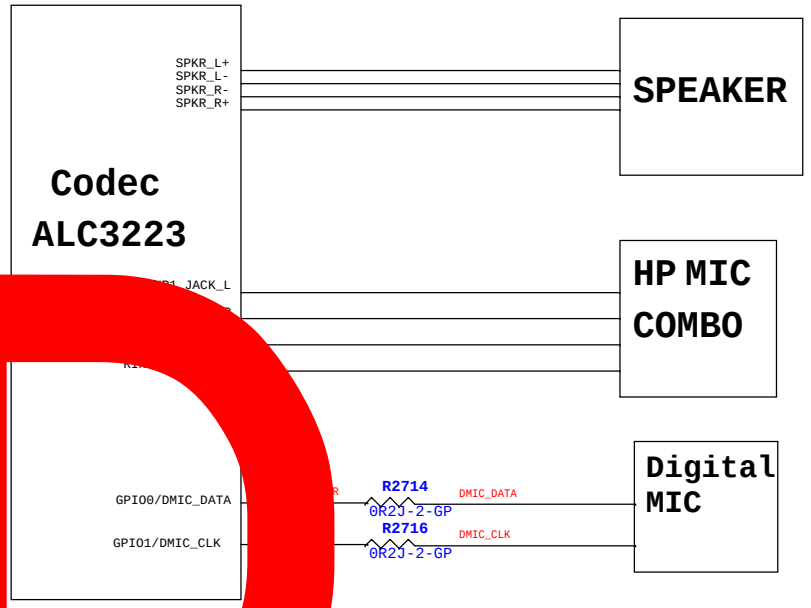
Thermal Block Diagram



Audio Block Diagram



TBD

<Core Design>

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