PCI-EXPRESS EDGE CONNECTOR

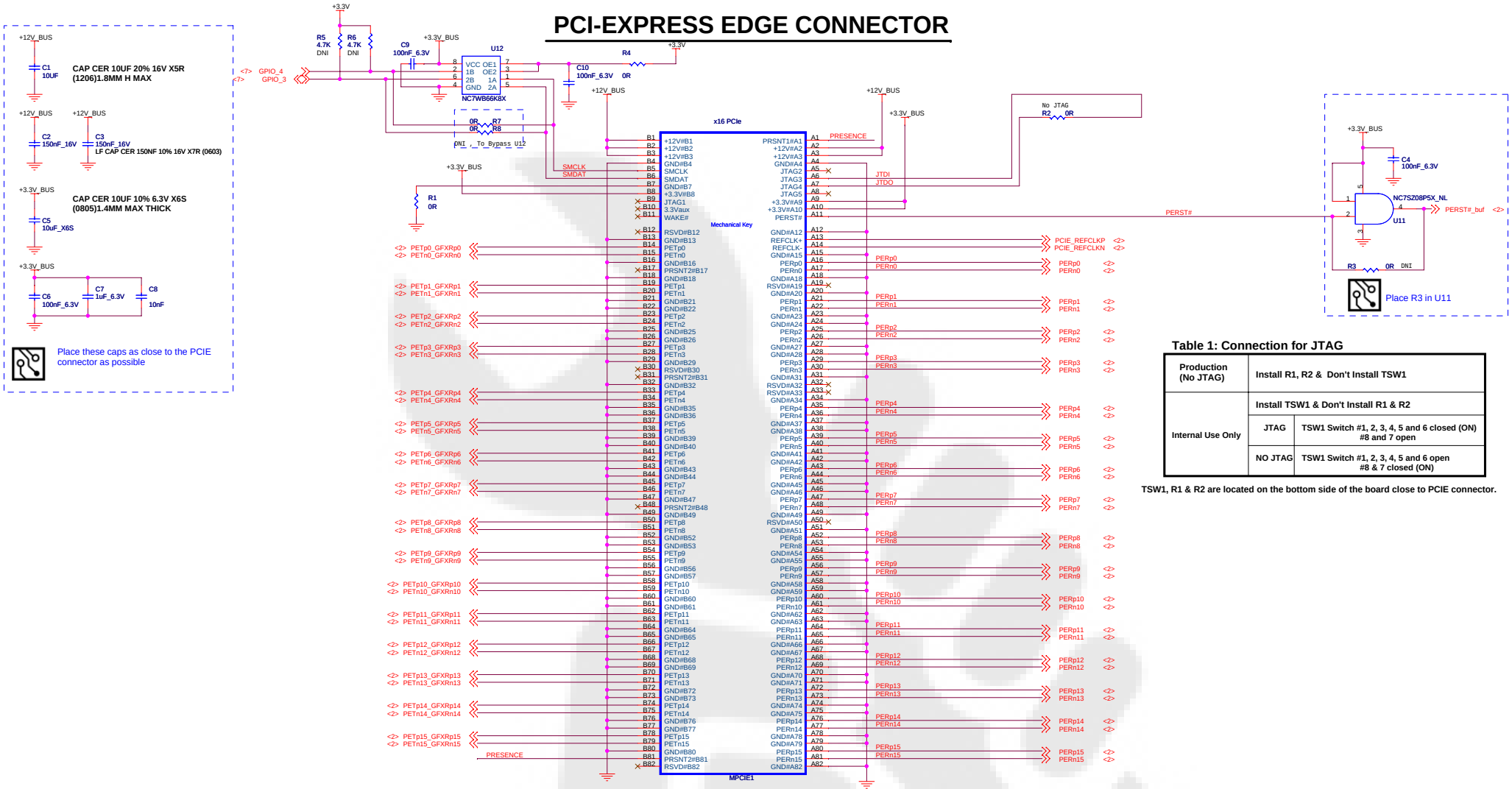

Table 1: Connection for JTAG

Production (No JTAG)	Install R1, R2 & Don't Install TSW1	
Internal Use Only	Install TSW1 & Don't Install R1 & R2	
	JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 closed (ON) #8 and 7 open
	NO JTAG	TSW1 Switch #1, 2, 3, 4, 5 and 6 open #8 & 7 closed (ON)

TSW1, R1 & R2 are located on the bottom side of the board close to PCIE connector.

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY

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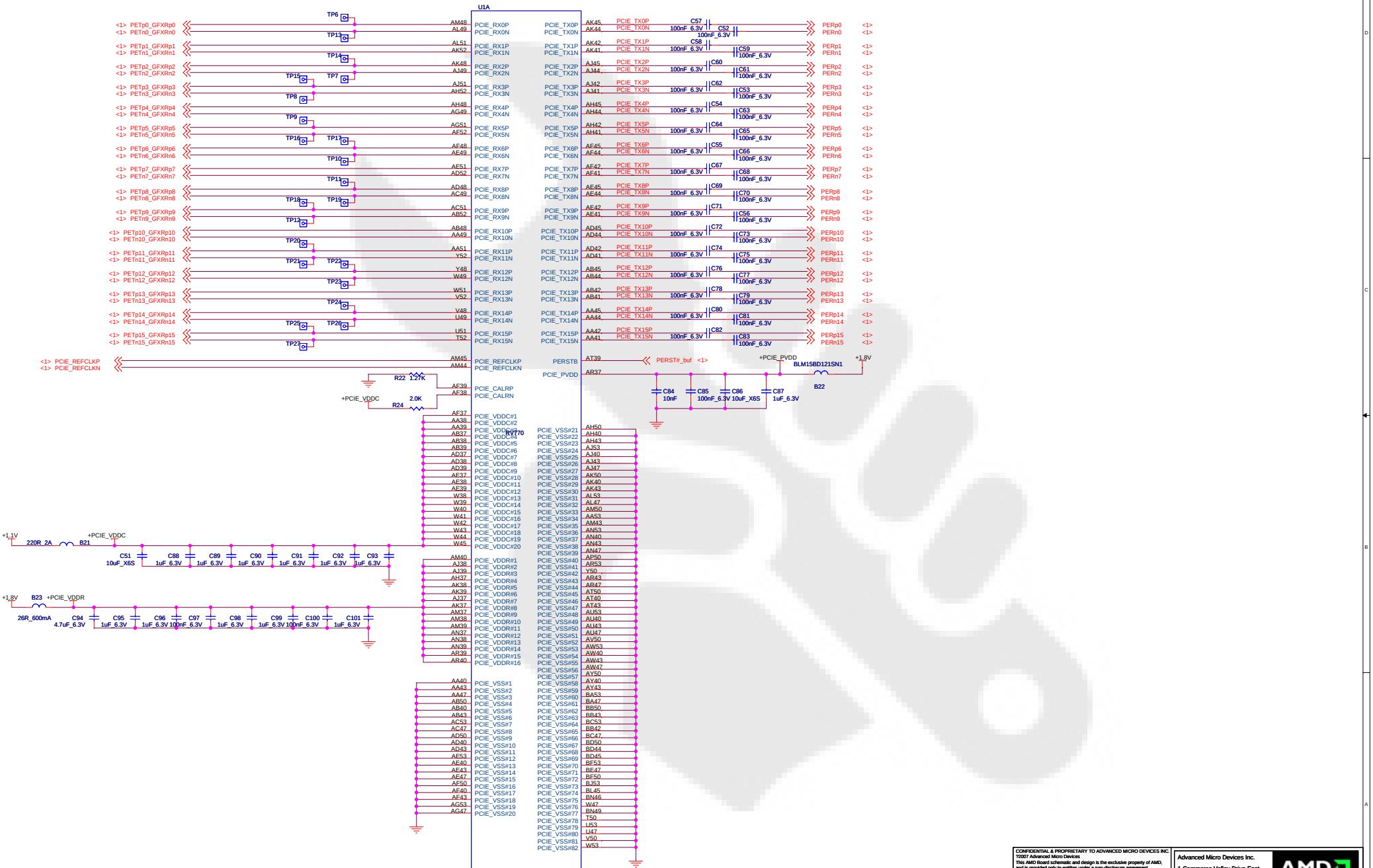
Doc No: 105-B50102-00

NOTE: some of the PCIE testpoints will
be available trought via on traces.



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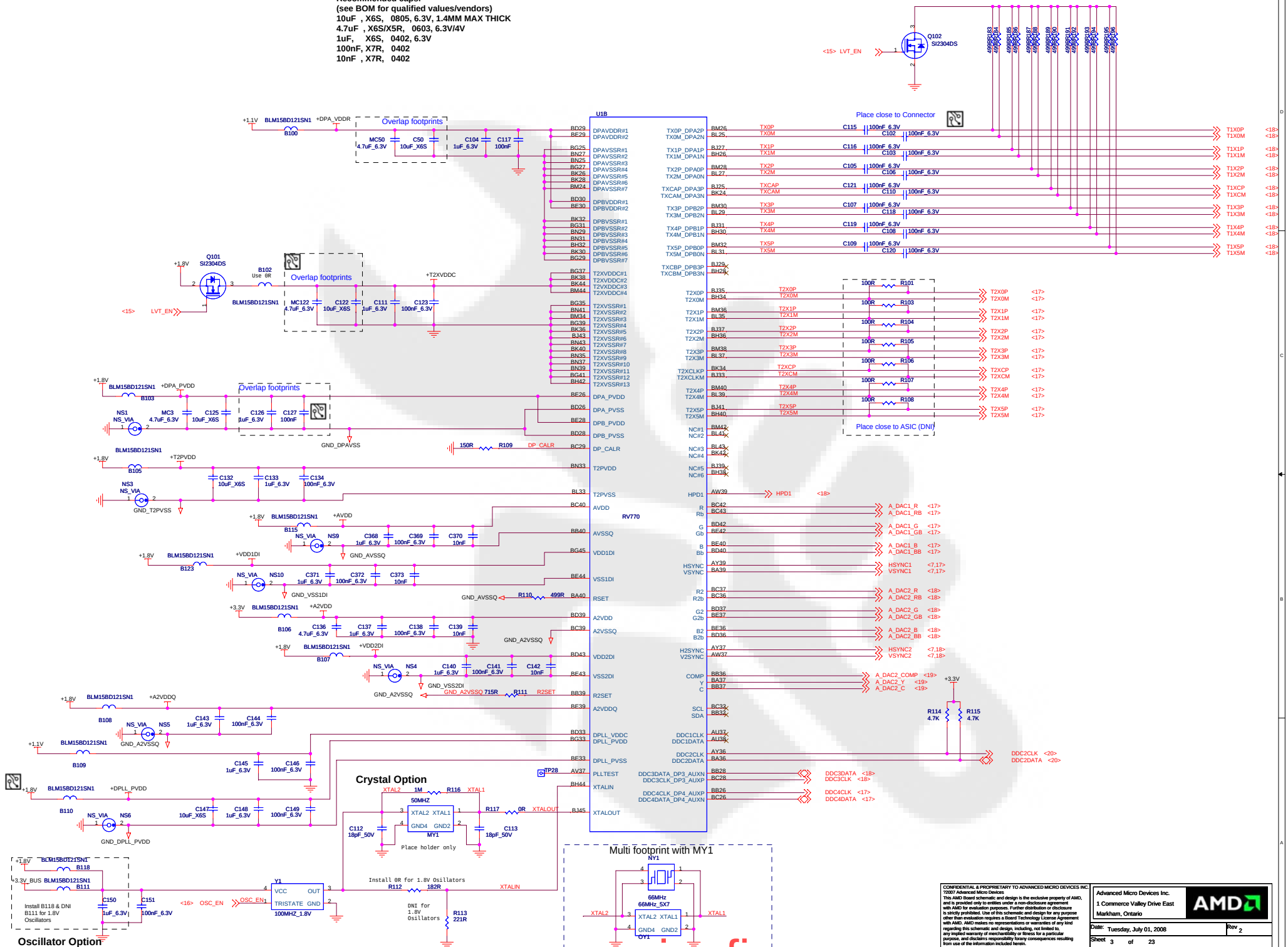
Recommended caps:
(see BOM for qualified values/vendors)
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK
4.7uF , X6S/X5R, 0603, 6.3V/4V
1uF, X6S, 0402, 6.3V
100nF, X7R, 0402
10nF , X7R, 0402



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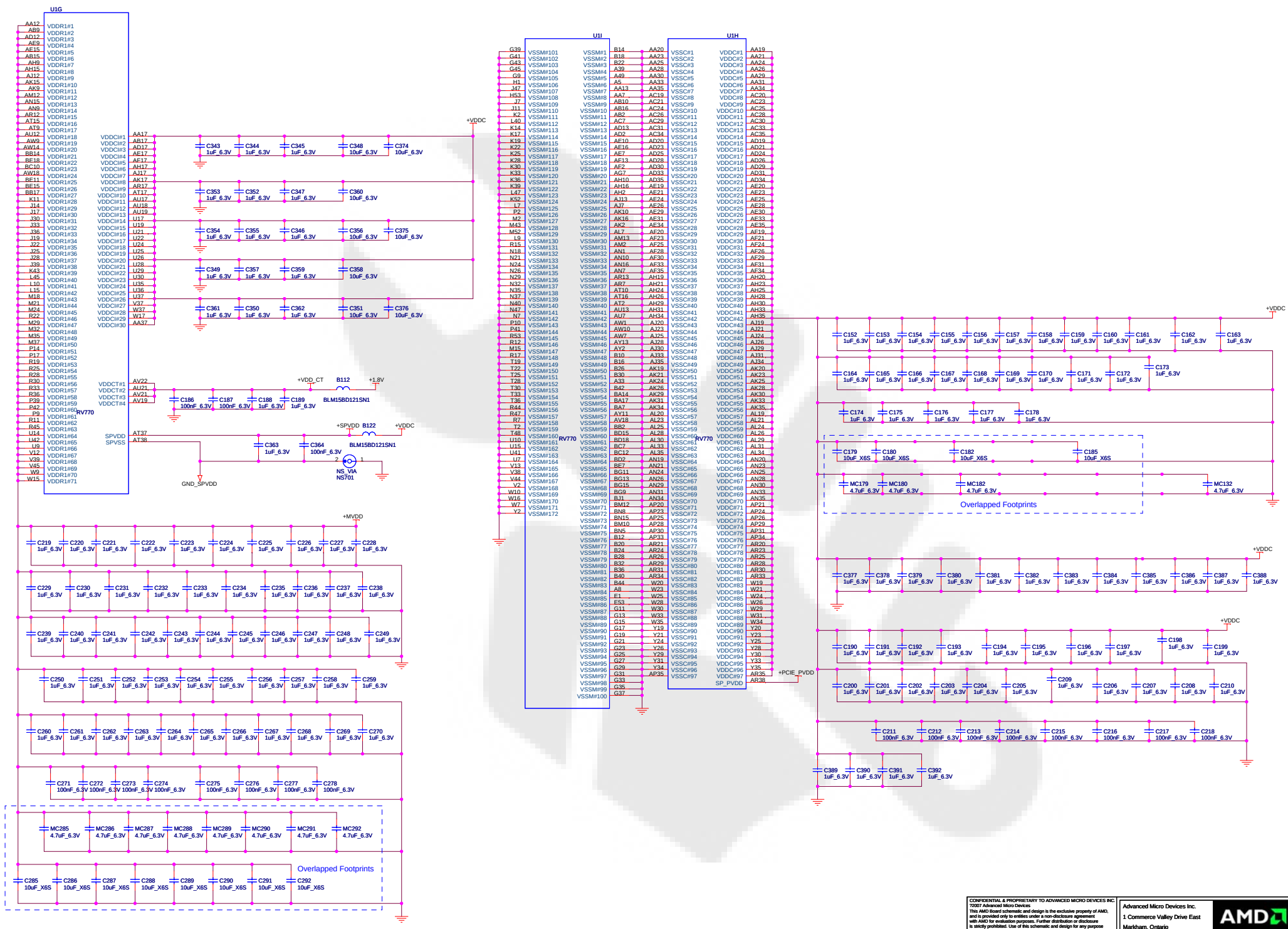

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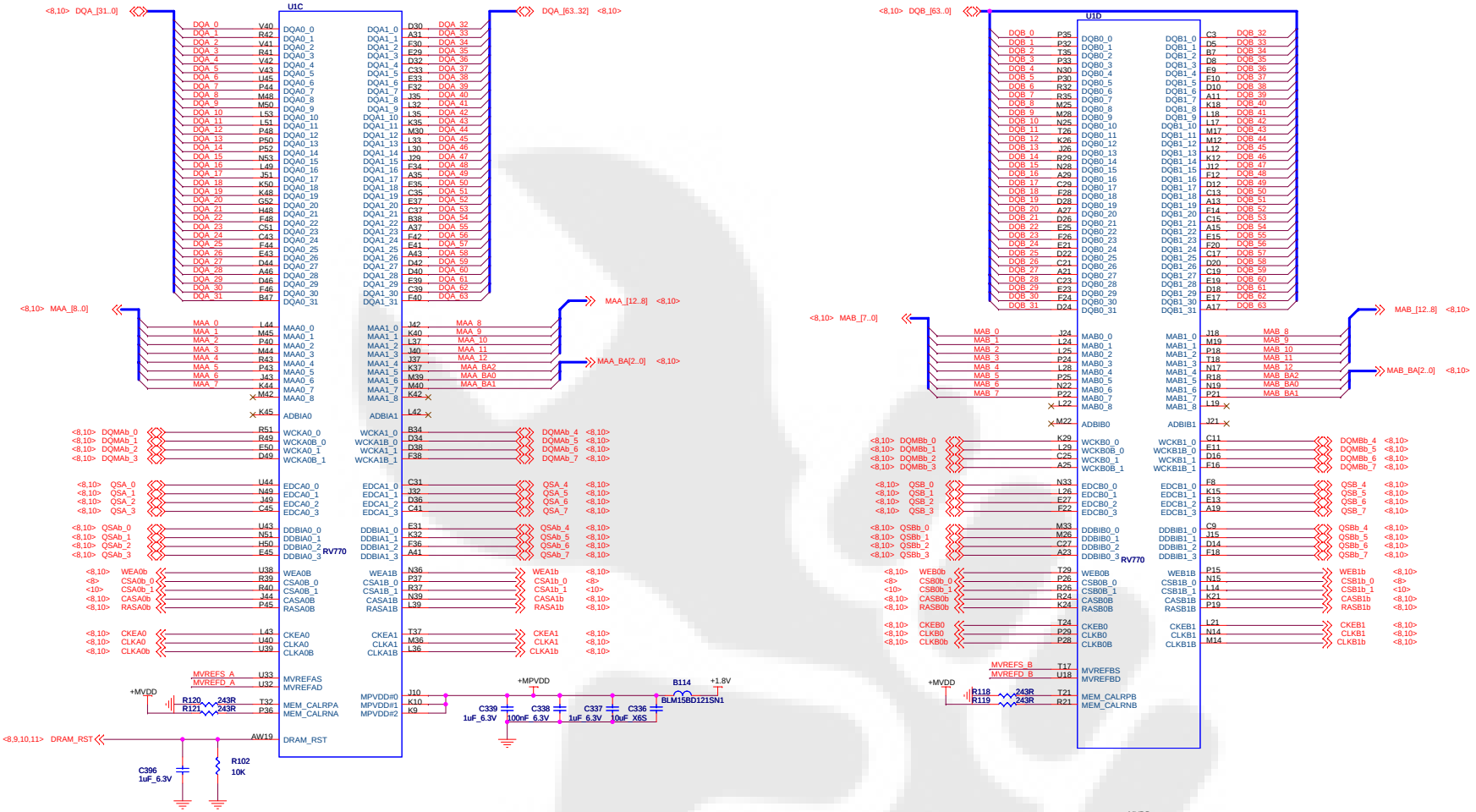

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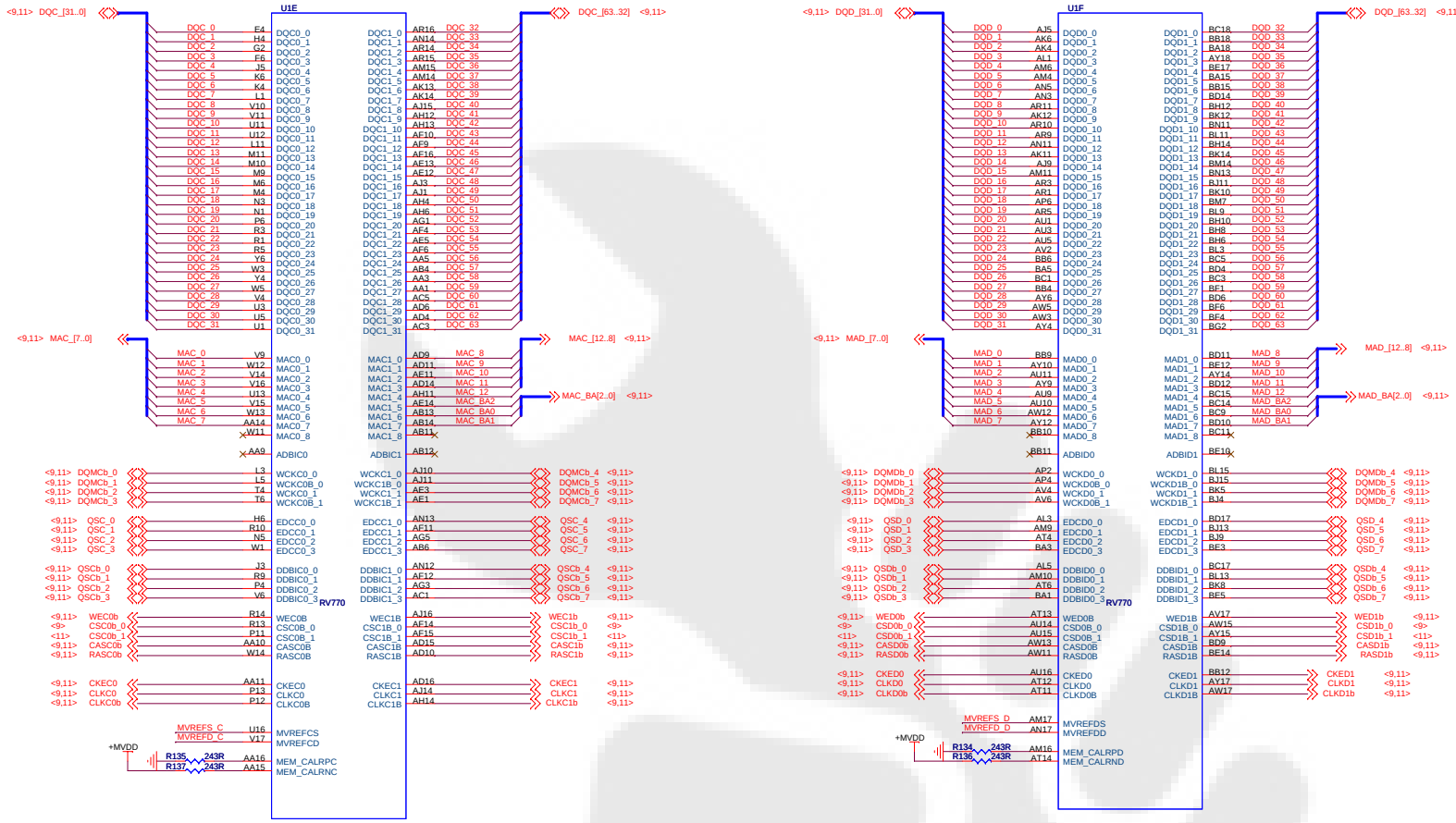

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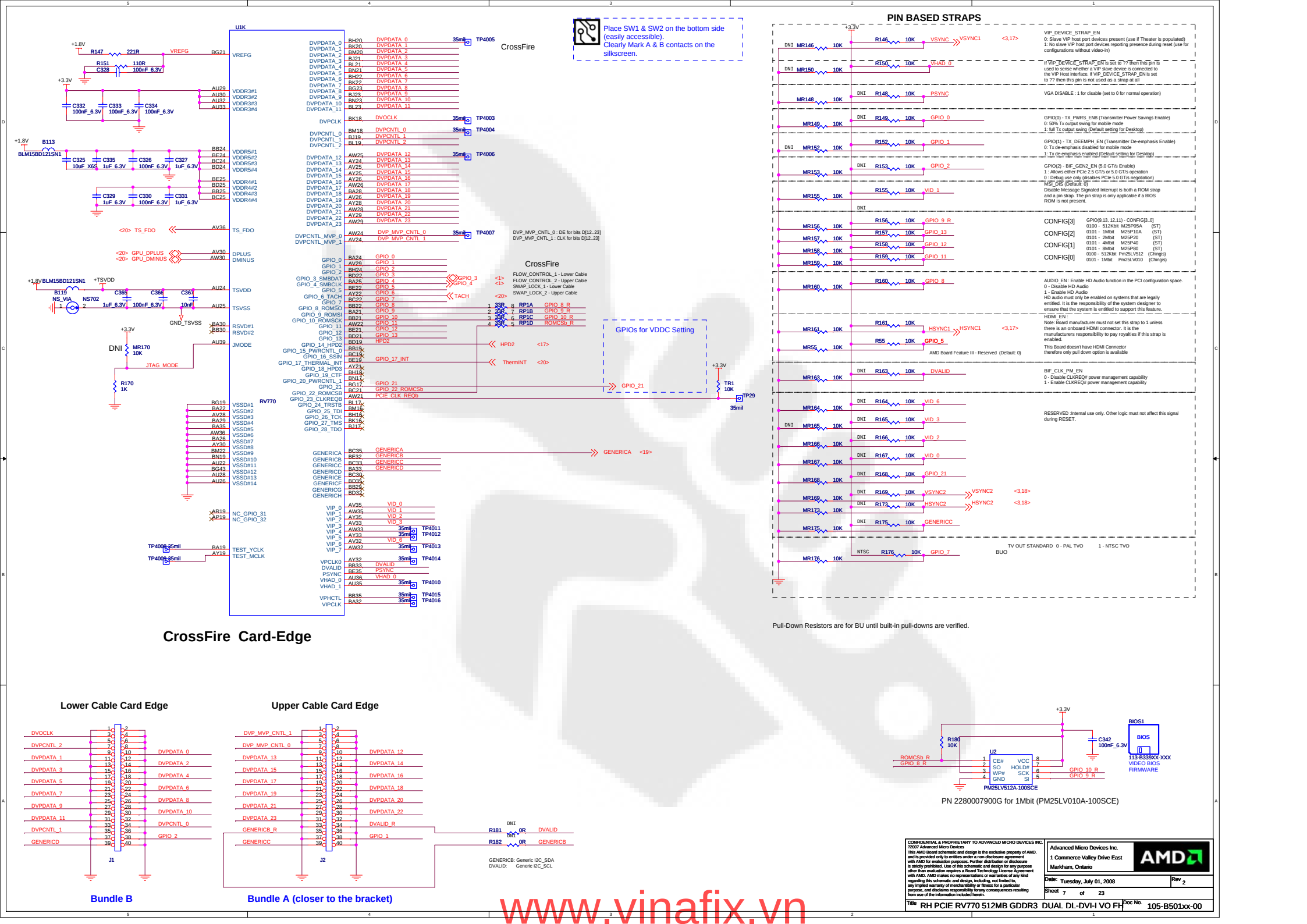
U1K
RV770
CrossFire
Place SW1 & SW2 on the bottom side (easily accessible).
Clearly Mark A & B contacts on the silkscreen.
GPIOs for VDDC Setting
PIN BASED STRAPS
Pull-Down Resistors are for BU until built-in pull-downs are verified.
CrossFire Card-Edge
Lower Cable Card Edge
Upper Cable Card Edge
Bundle B
Bundle A (closer to the bracket)
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)
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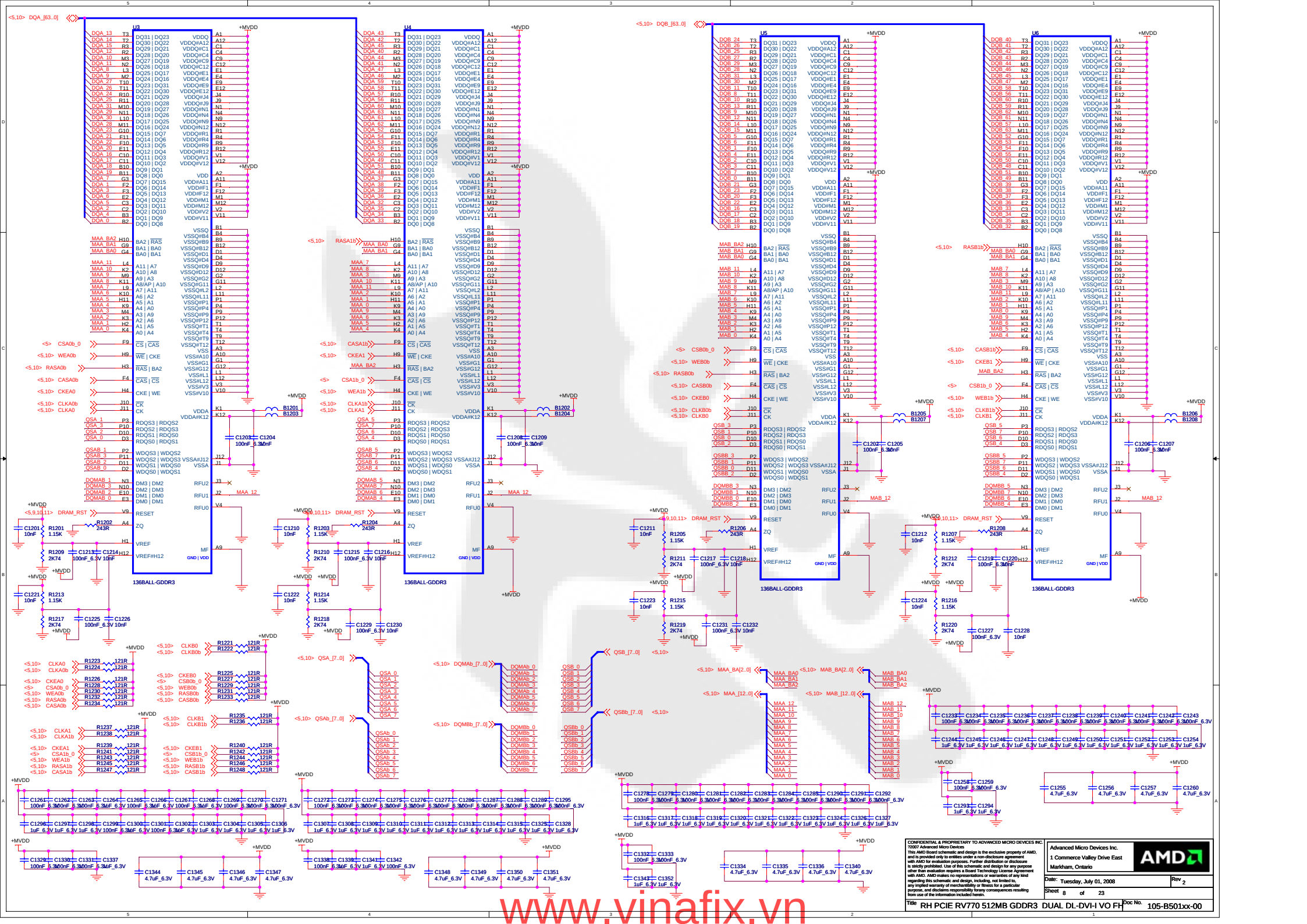
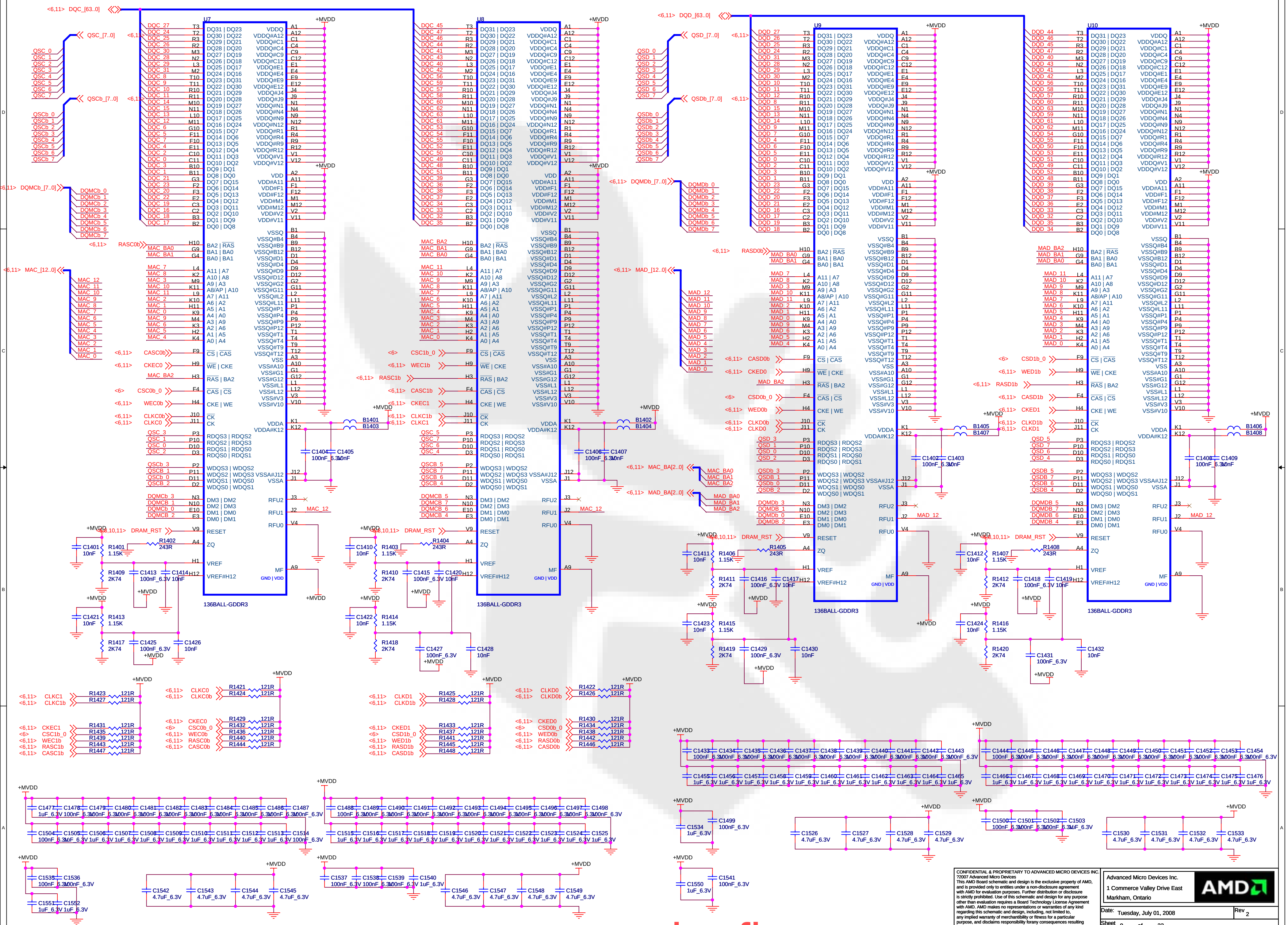
RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FH
105-B501xx-00
www.vinafix.vn





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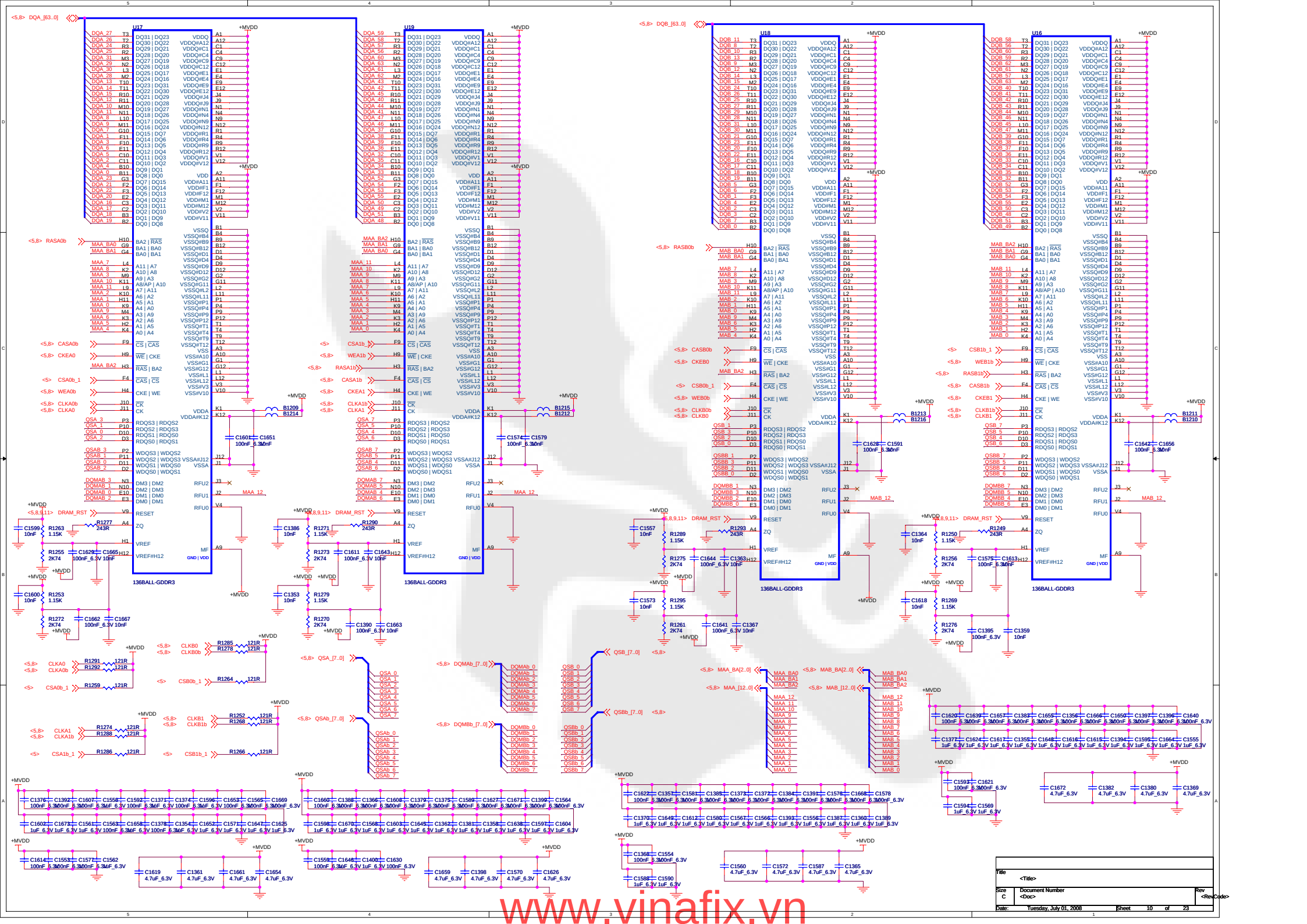

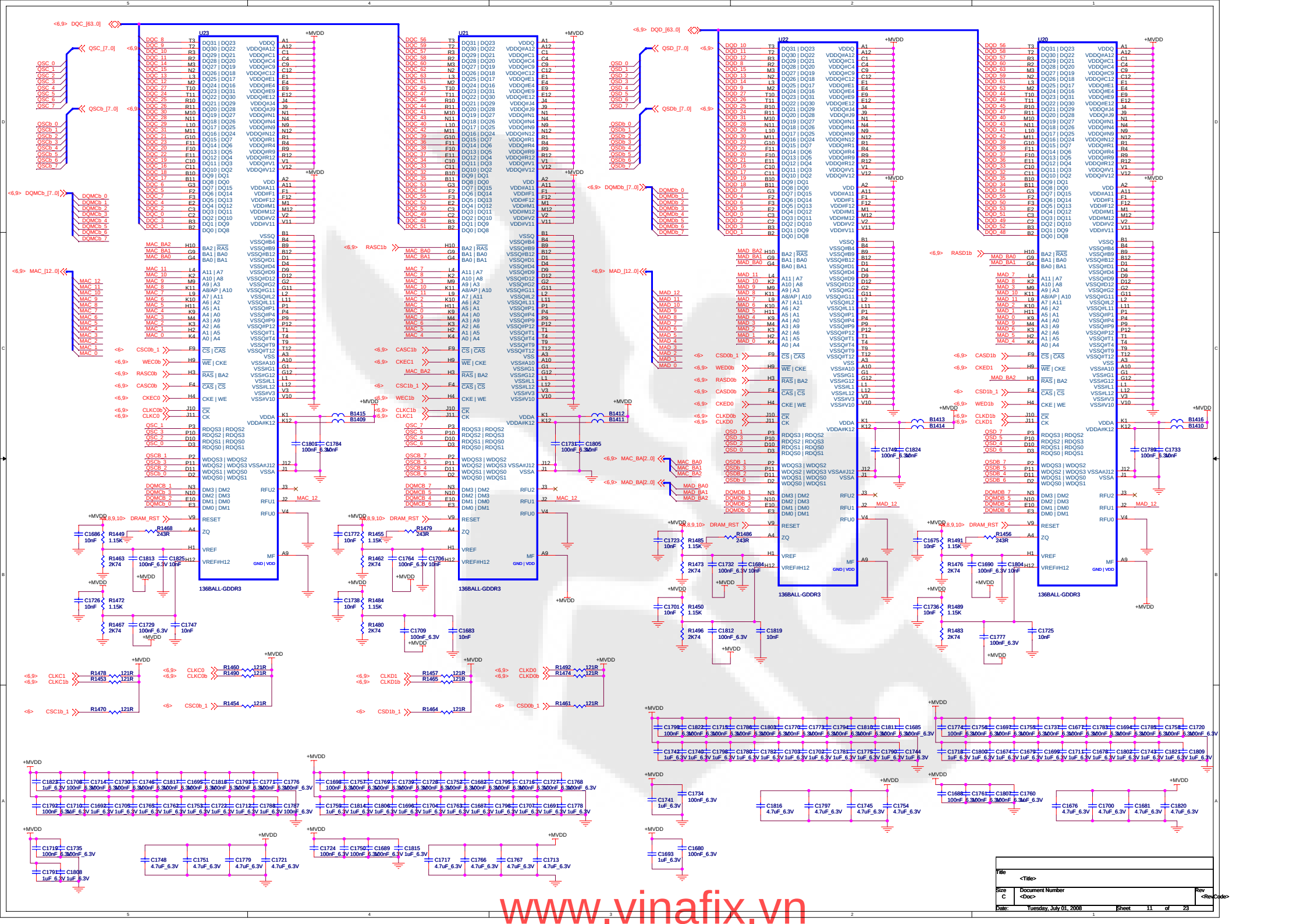
U23
U21
U22
U20
136BALL-GDDR3
DQC_[63..0]
DQD_[63..0]
QSC_[7..0]
QSD_[7..0]
QSCb_[7..0]
QSDb_[7..0]
DQMCb_[7..0]
DQMDb_[7..0]
MAC_[12..0]
MAD_[12..0]
RASC1b
RASD1b
CSC0b_1
CSD0b_1
WEC0b
WED0b
RASC0b
RASD0b
CASC0b
CASD0b
CKEC0
CKED0
CLKC0b
CLKD0b
CLKC0
CLKD0
CASC1b
CASD1b
CKEC1
CKED1
CSC1b_1
CSD1b_1
WEC1b
WED1b
CLKC1b
CLKD1b
CLKC1
CLKD1
MAC_BA[2..0]
MAD_BA[2..0]
DRAM_RST
MAC_12
MAD_12
+MVDD
GND | VDD
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Title
<Title>
Size C
Document Number <Doc>
Rev <RevCode>
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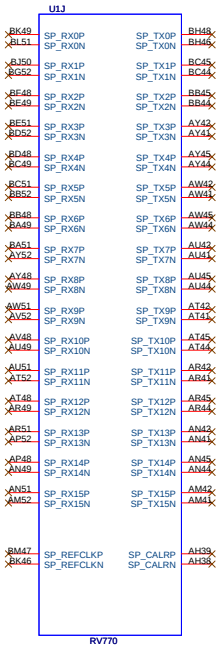

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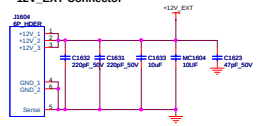
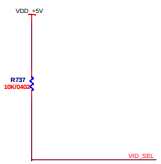
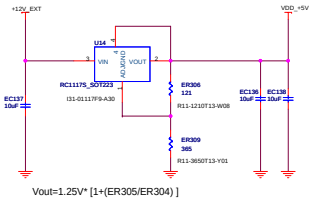
Install AR47 for Disable PWM3 function

+VDDC=0.8 * (1+ (AR49 / AR82))

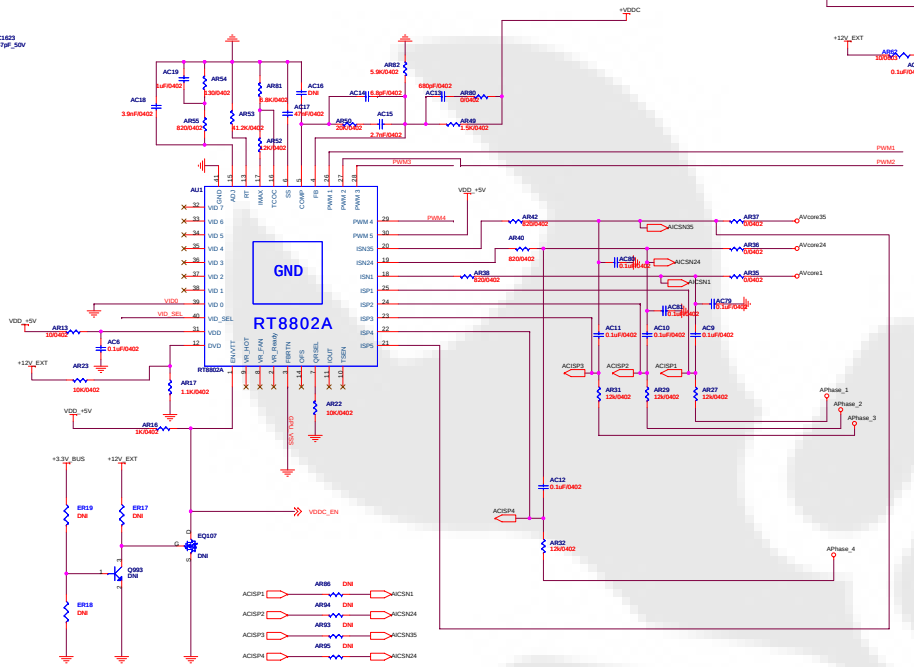
12V_EXT Connector

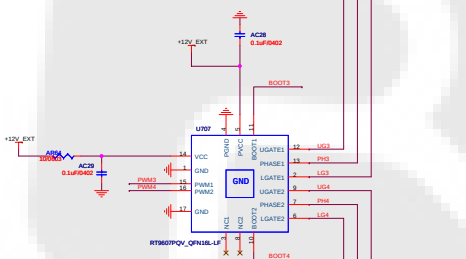


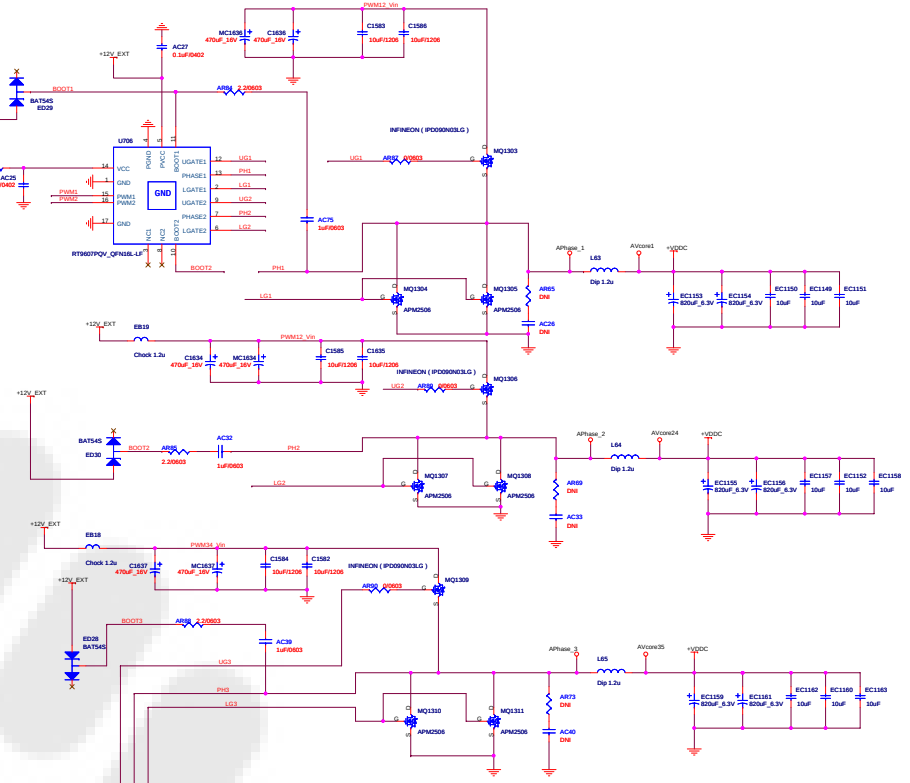




Vout=1.25V* [1+(ER305/ER304)]







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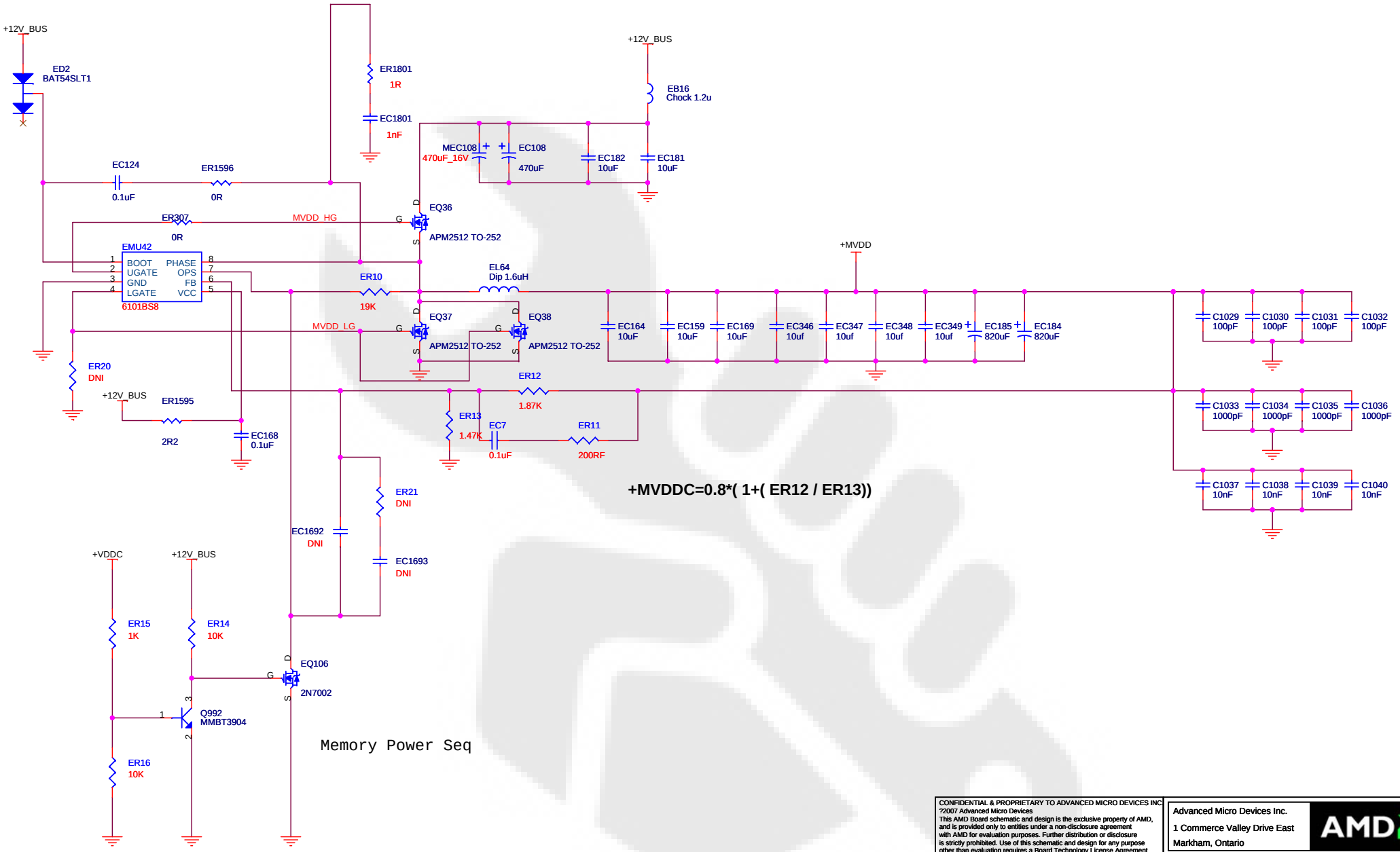

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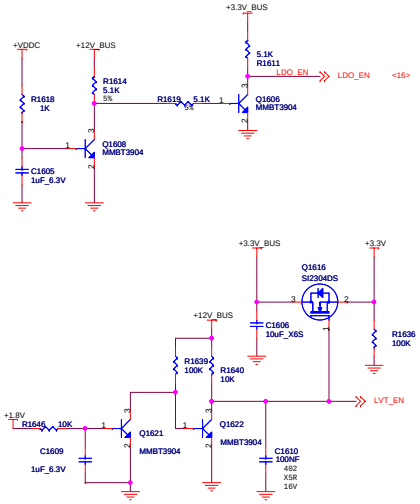
Power up Sequencing



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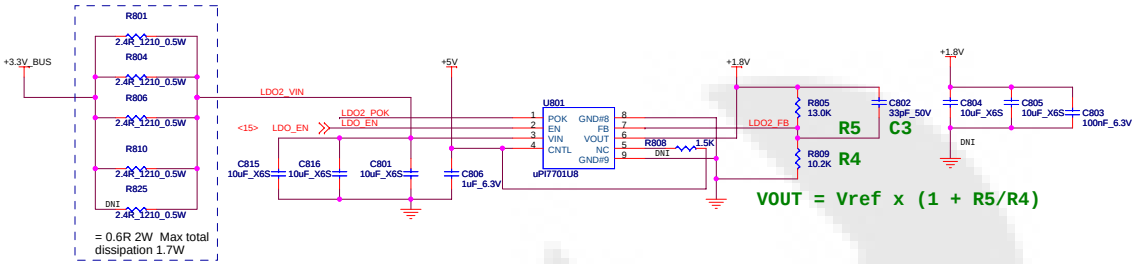
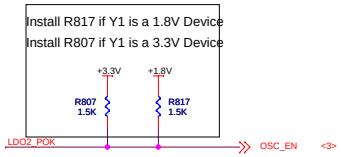
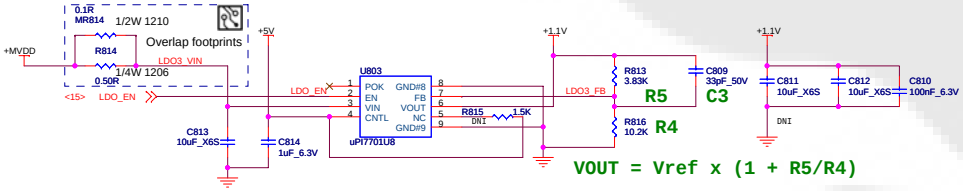
Regulators for +5V, +5V_VESA and +5V_VESA2

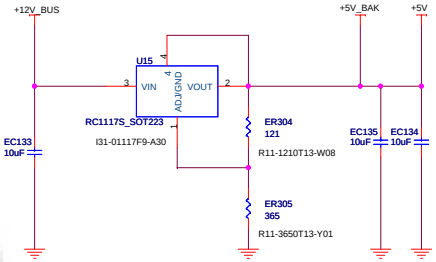
LDO #2: Vin = 2.5V to 3.6V MAX Vout = +1.8V +/- 3% Iout = 1.7A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling



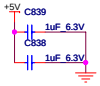


LDO #3: Vin = +1.50V to 2.1VMAX Vout = +1.1V +/- 3% Iout = Up to 1.3A (TBV) RMS MAX
PCB: Min 70mm sq. copper area for cooling





Vout=1.25V* [1+(ER305/ER304)]



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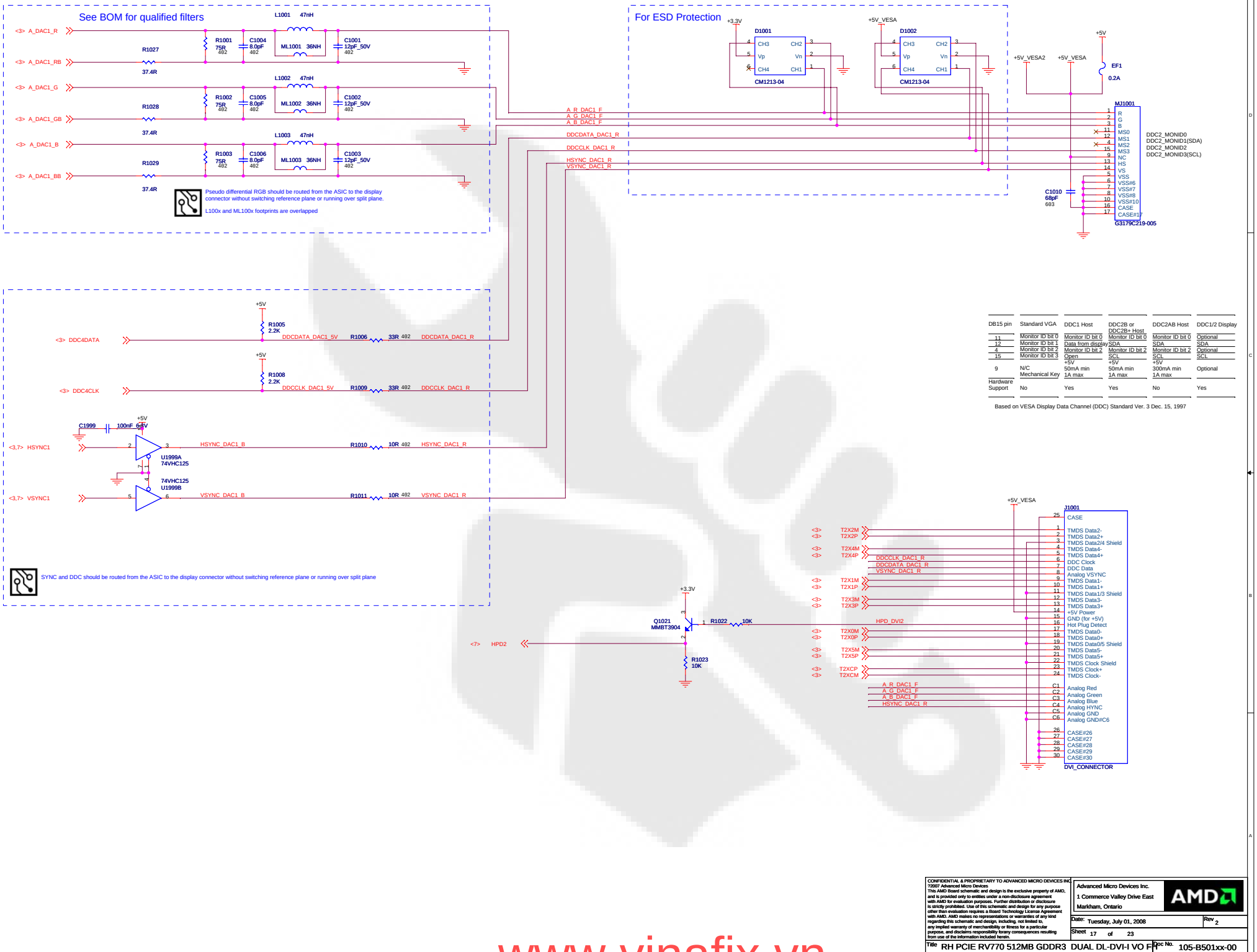

DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min 1A max	+5V 50mA min 1A max	+5V 300mA min 1A max	Optional
Hardware Support	Mechanical Key	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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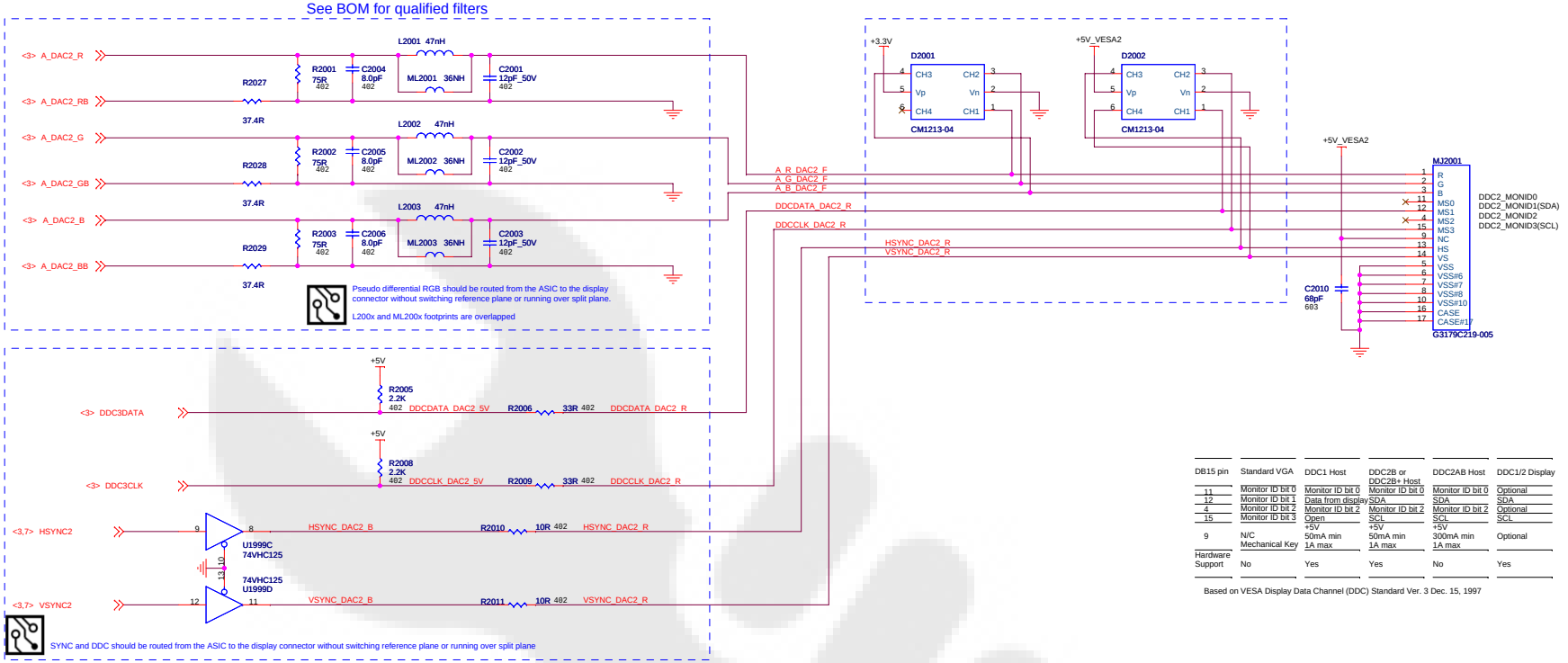
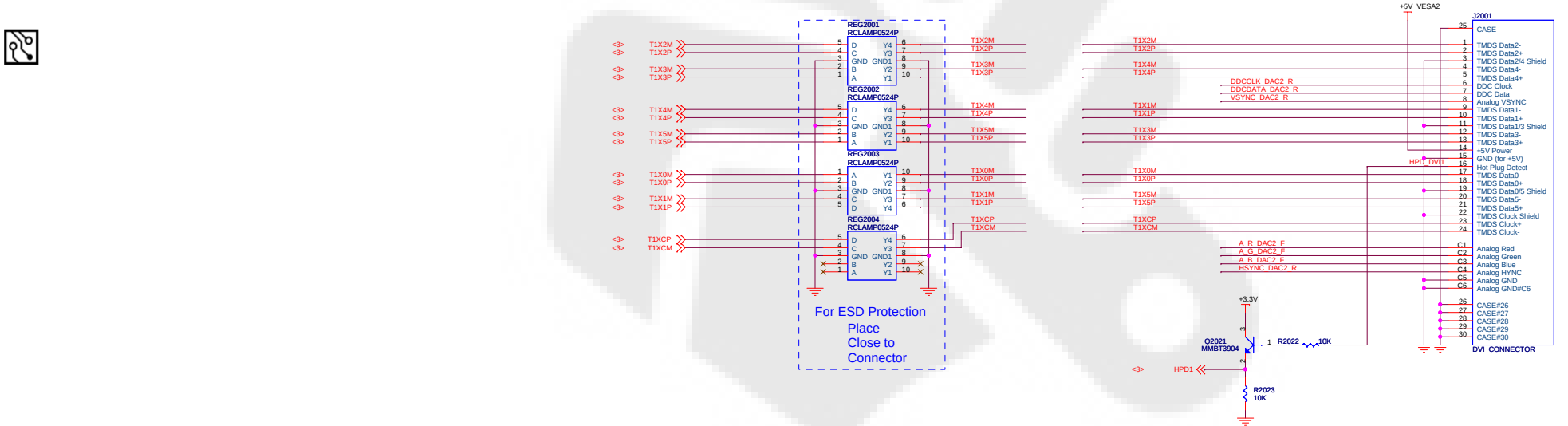
See BOM for qualified filters



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997



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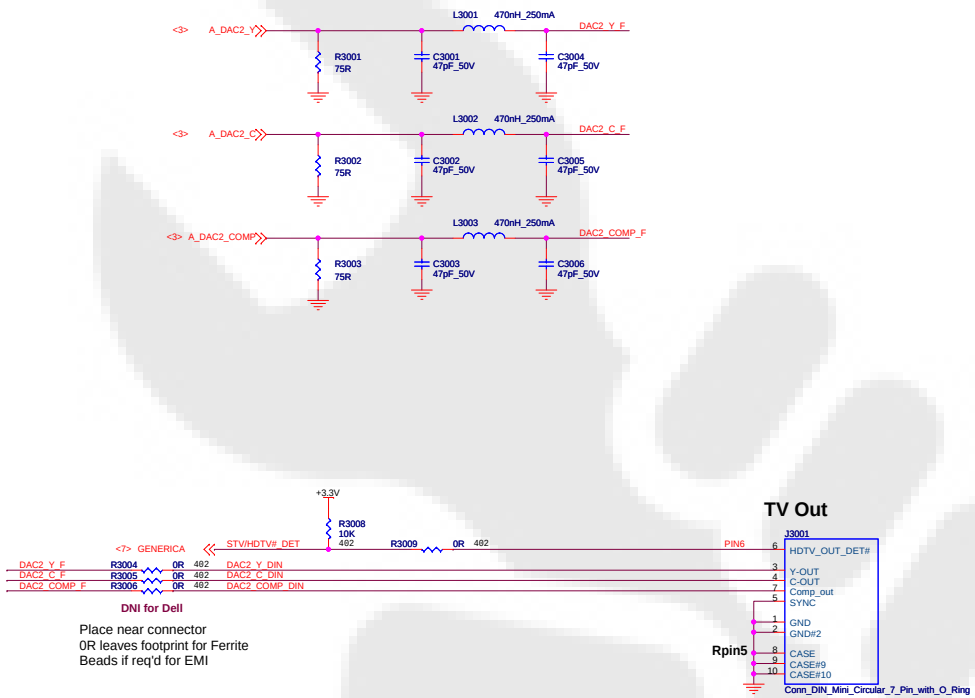

- 4-pin Svideo MiniDIN P/N 6070001000G

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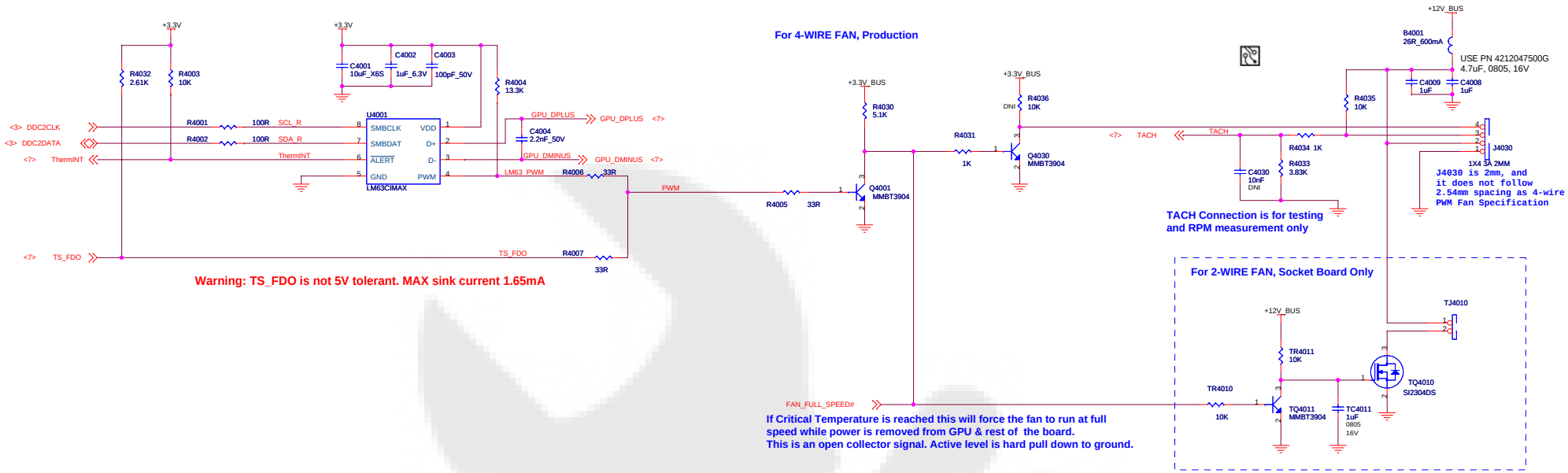

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ASSY-SCREW2
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW1
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW4
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

ASSY-SCREW3
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>

MT1
MT_Hole_0.136 TM 5.5 BM 7.0

PCB1
PCB
109-B33931-00A

ASSY1
ANTISTATIC BAG
6_X_11

BKT1
BRACKET
80200386B0G

ASSY-SCREW5
SCREW
SCREW

BKT1: DS, DVI - DIN - DVI

BKT2
BRACKET
8020038600G

SK1
Socket_RV770

VDDC1

MVDD1

TPC1

IOT1

PCIE 12V/3.3V Power up Bonding support

FM1 SW_FB
FM2 SW_FB
FM3 SW_FB
FM4 SW_FB
FM5 SW_FB
FM6 SW_FB

J7 impedence
J4 impedence
J5 impedence
J8 impedence

J3 X_PIN1*2
J6 X_PIN1*2
J9 X_PIN1*2
J11 X_PIN1*2

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Title	Schematic No.	Date:
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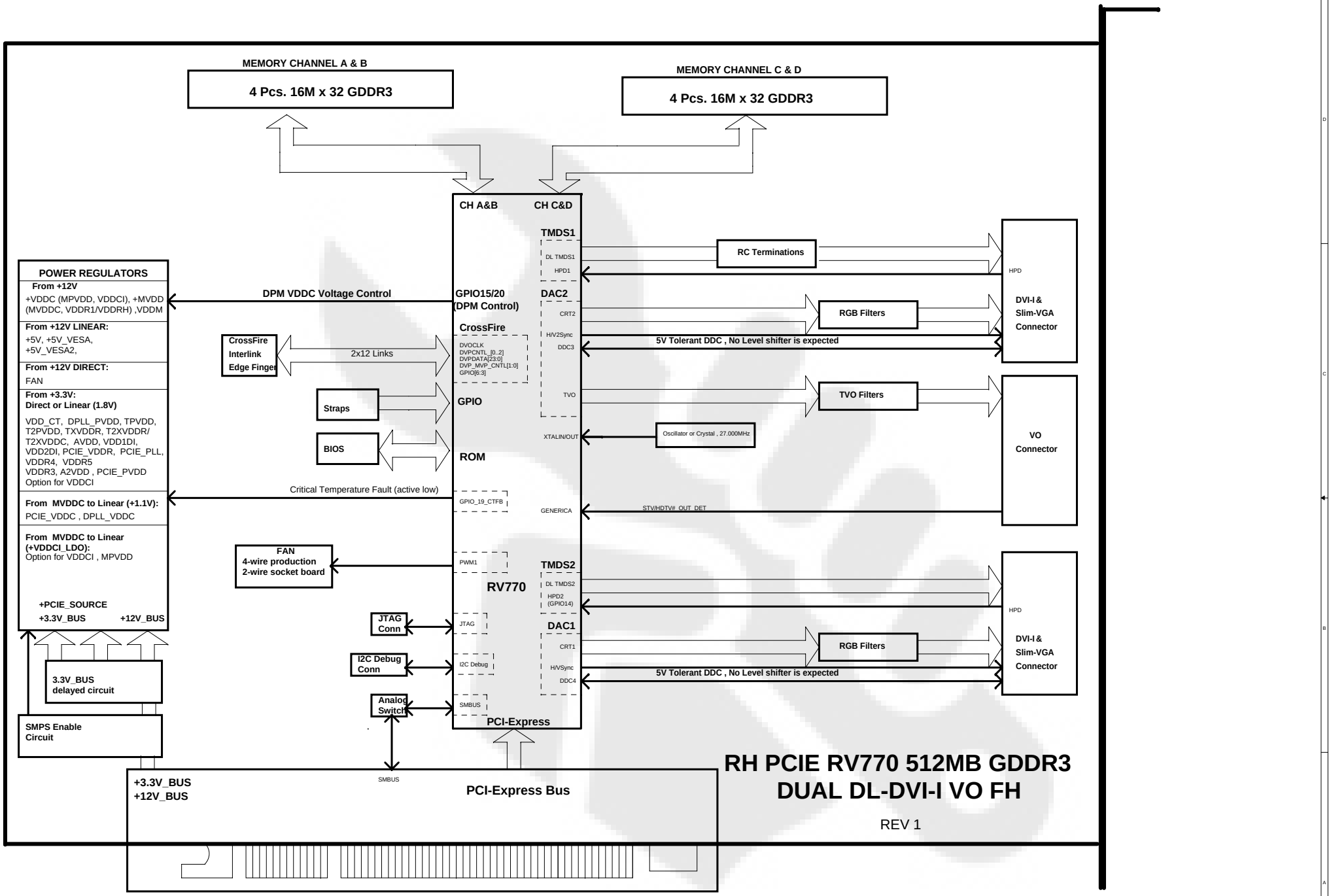
REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI , ? please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	07/10/11	Initial design for RV770 GDDR3
1	00B	08/02/25	Improvement: 1) Add 1 uF CAP on memory reset, Pg5 2) MVDDC current leakage board workaround; Pg13 3) MVDD Themal Protection, Pg 13 4) Improvement on Hot Plug protection Pg13 5) 12V_BUS & 12V_EXT Input Switch Circuit Page 13
2	00	08/03/27	1.Correct PTC comparator power connection. 2. Add Fuse NF1200 on page 13



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