

# Compal Confidential

## ZRMAA/ZEMAA Schematics Document

Haswell ULT with DDR3L

nVIDIA N14P-GV2 (Dual Rank)

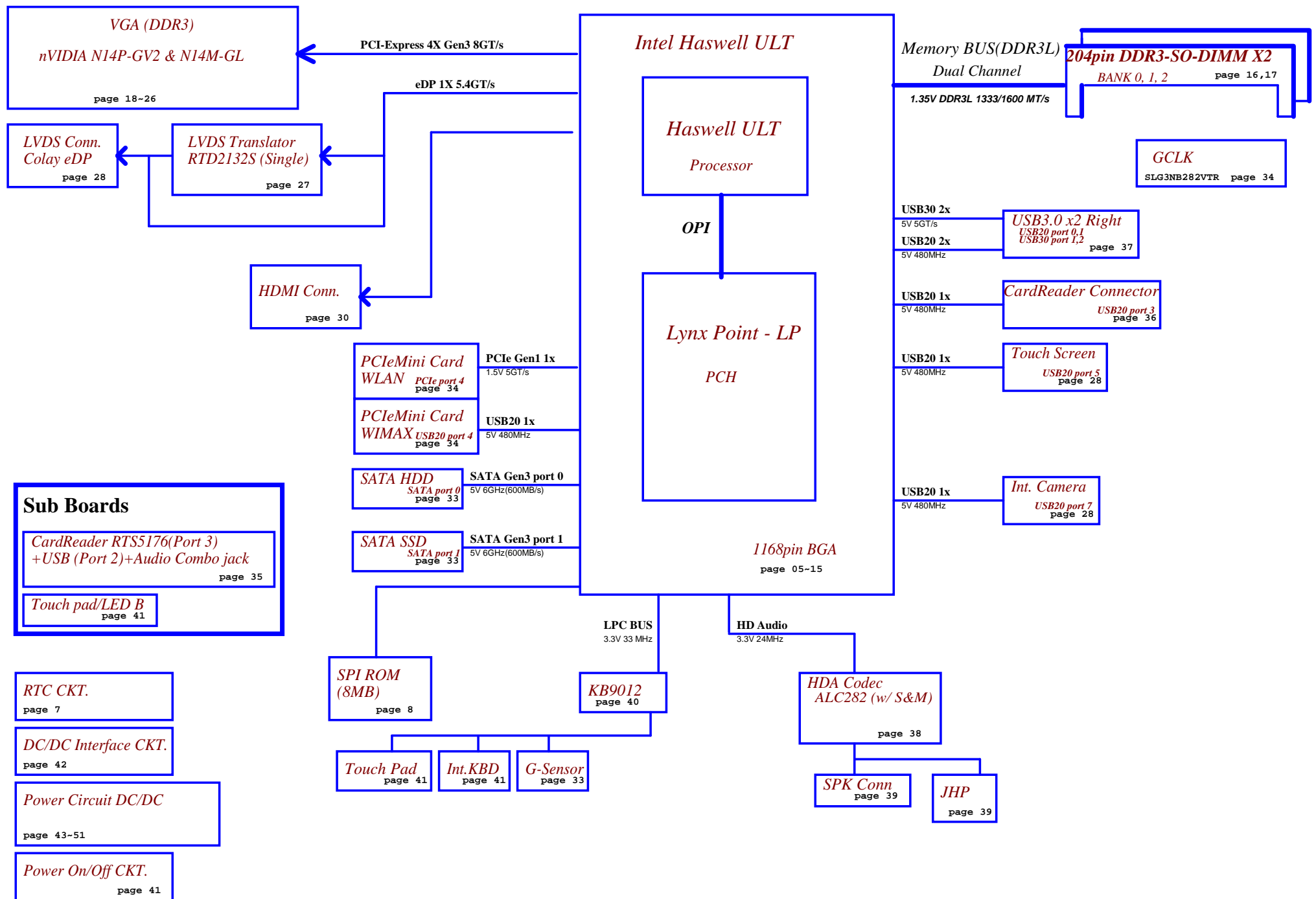
nVIDIA N14M-GL

# LA-A481P REV 0.1 Schematic

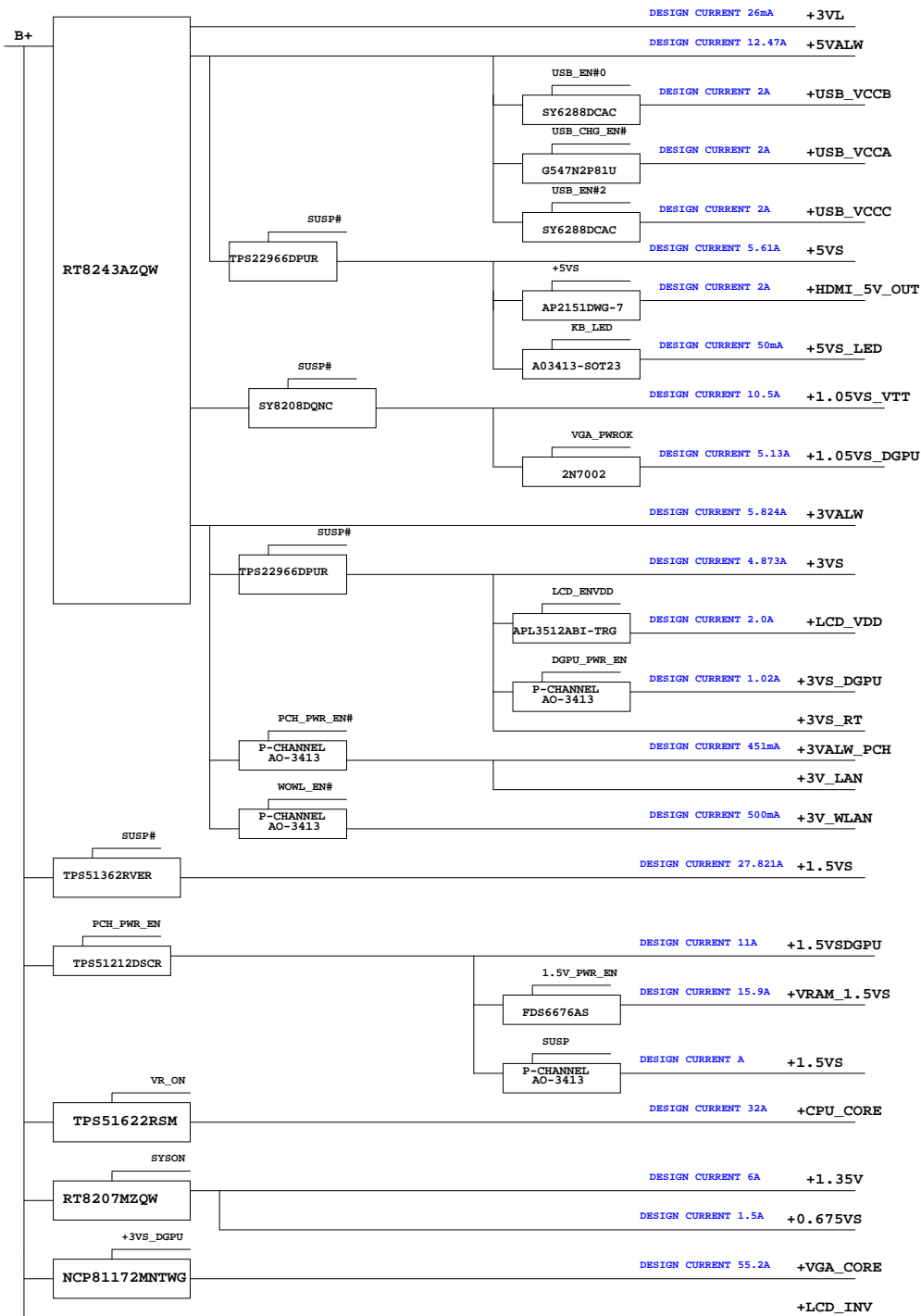
Intel Processor (Haswell)

2013-02-22 Rev 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	ZRMAA/ZEMAA	Rev 0.1
				Date	Sunday, April 07, 2013	Sheet 1 of 49



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				ZRMAA/ZEMAA	0.1
				Date: Sunday, April 07, 2013	Sheet 2 of 49



Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> <i>Power Map</i>	
Issued Date		Deciphered Date			
2012/10/25		2013/10/05		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	ZRMMAA/ZEMAA
				Date	Sunday, April 07, 2013
				Sheet	3 of 48
				Rev	0.1

# Voltage Rails ( O MEANS ON X MEANS OFF )

power plane \ State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW +VSB	+1.35V	+5VS +3VS +1.8VS_CRT +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +1.05VS_VTT
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

## PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

## EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

Power	Device	HEX	Address
-------	--------	-----	---------

## EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

Platform	SKU	CPU	PCH	VGA
				nVIDIA N13P-GL (N13PGL@)

## BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

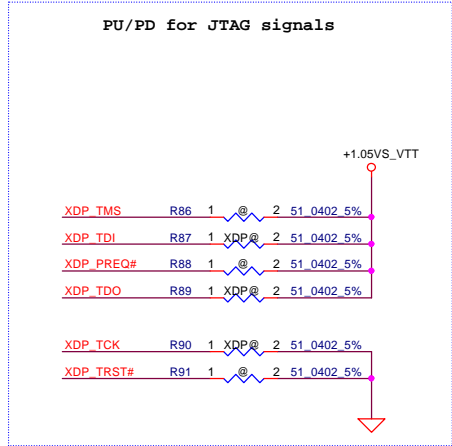
Function						
description						
explain						
BTO						

Function						
description						
explain						
BTO						

Function		
description		
explain		
BTO		

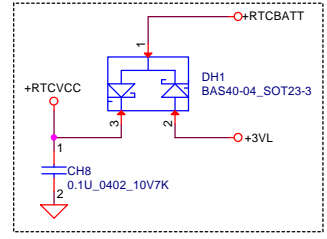
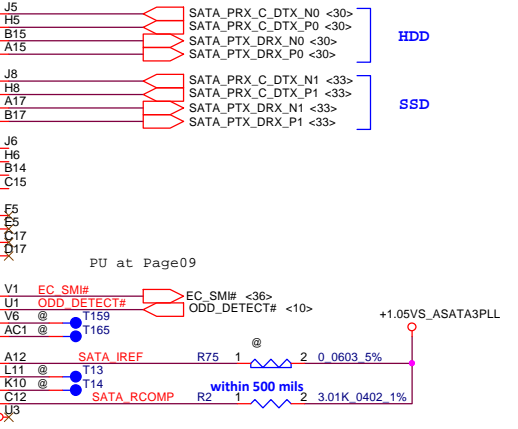
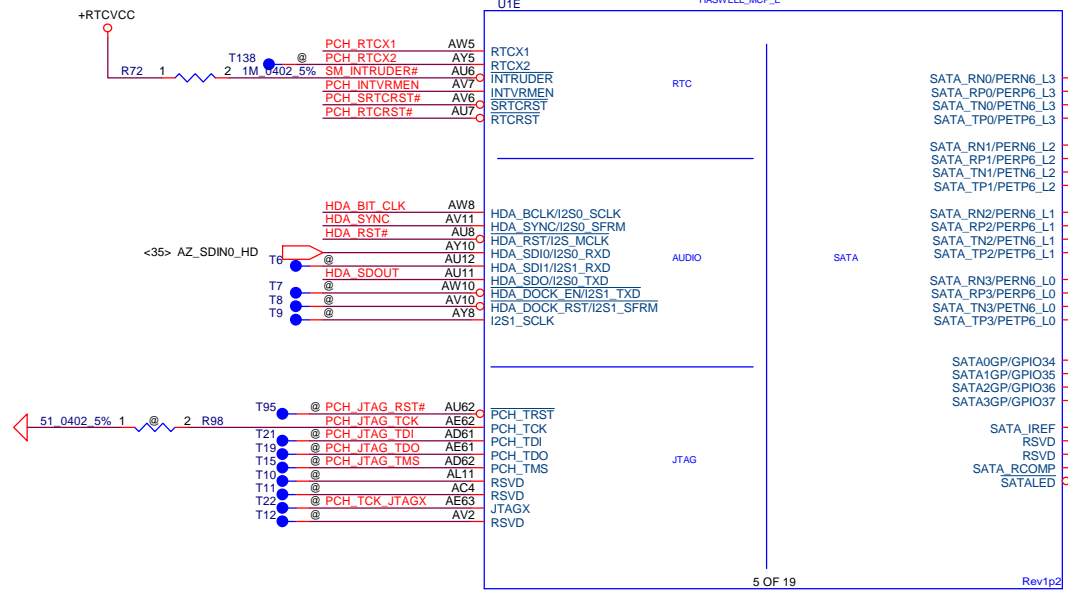
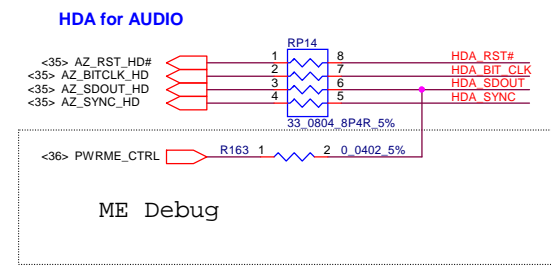
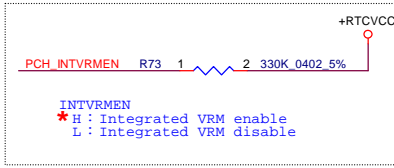
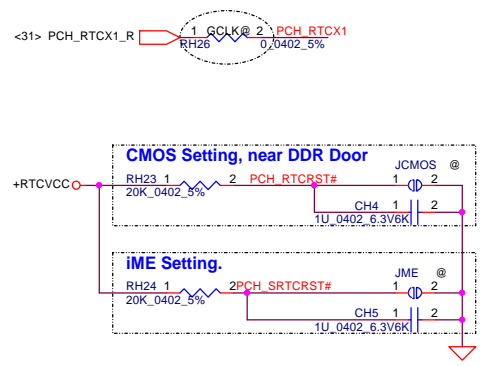
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Notes List		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	ZRMAA/ZEMAA	Rev 0.1
				Date:	Sunday, April 07, 2013	Sheet 4 of 49

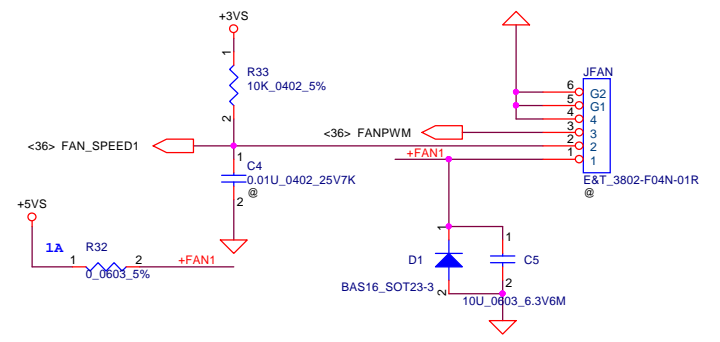


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>HSW MCP(1/11) DDI,MSIC,XDP</b>	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number <b>ZRMAA/ZEMAA</b>
				Date: Sunday, April 07, 2013	Sheet 5 of 49
					Rev 0.1

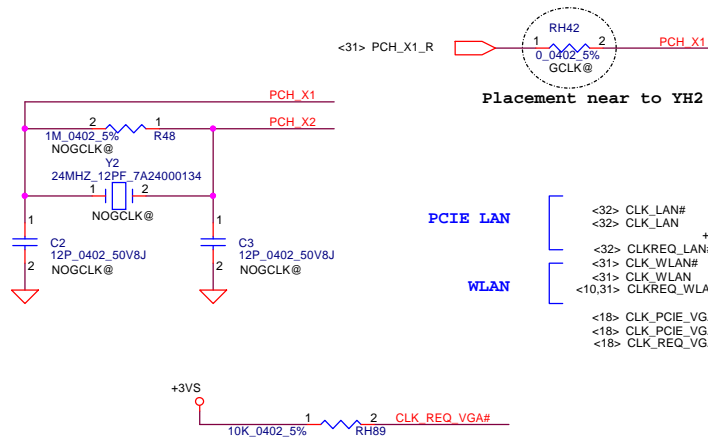




## FAN Control Circuit



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2012/07/10		Deciphered Date	
2013/07/10		Title		HSW MCP(3/11) RTC,SATA,XDP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size Custom		Document Number	
Date:		Sunday, April 07, 2013		Sheet 7 of 49	
				Rev 0.1	



PCIE LAN  
WLAN

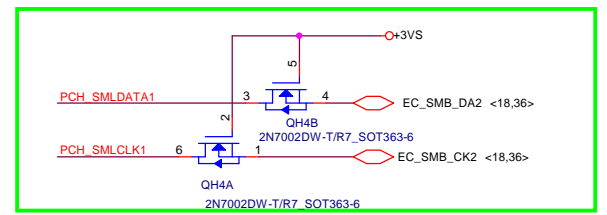
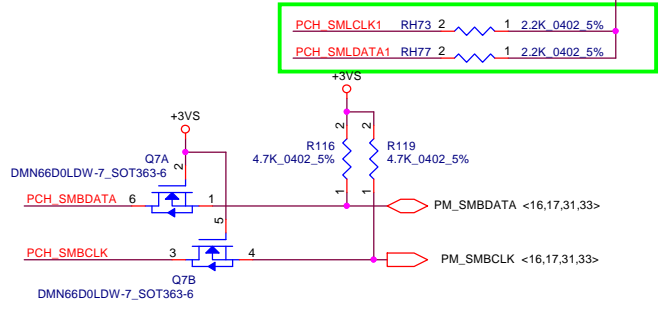
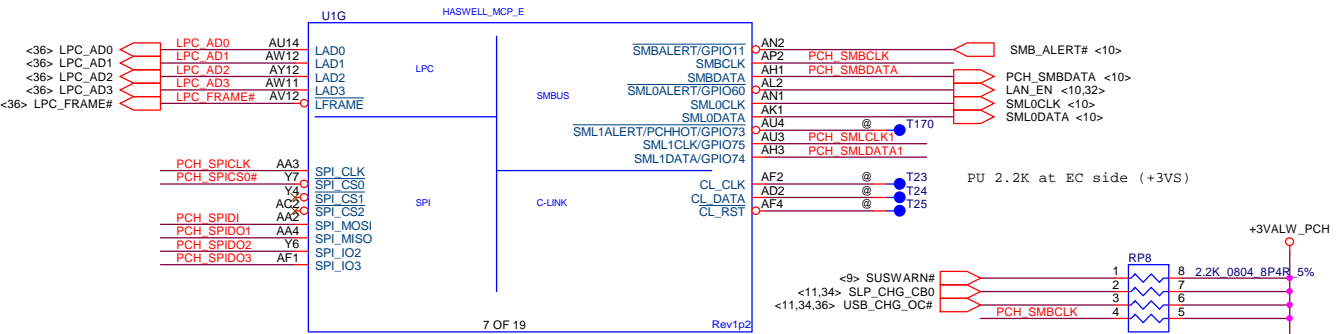
- <32> CLK\_LAN#
- <32> CLK\_LAN
- <32> CLKREQ\_LAN#
- <31> CLK\_WLAN#
- <31> CLK\_WLAN
- <10,31> CLKREQ\_WLAN#
- <18> CLK\_PCIE\_VGA#
- <18> CLK\_PCIE\_VGA
- <18> CLK\_REQ\_VGA#

- <36> LPC\_AD0
- <36> LPC\_AD1
- <36> LPC\_AD2
- <36> LPC\_AD3
- <36> LPC\_FRAME#

- PCH SPICLK
- PCH SPICS0#
- PCH SPIDI
- PCH SPIDO1
- PCH SPIDO2
- PCH SPIDO3

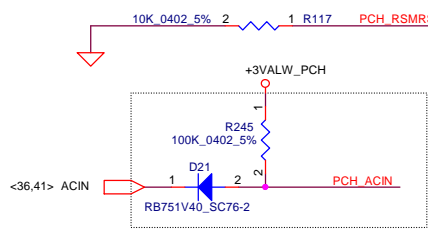
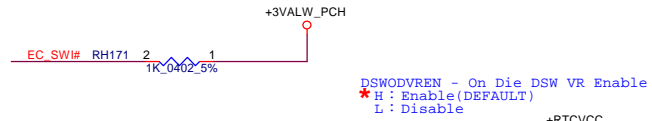
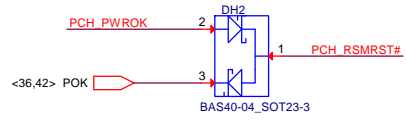
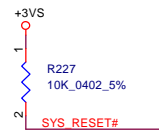


Socket: SP07000F500/SP07000H900  
Please place UH3 close to U1 CPU,  
Please place RH66, RH67, RH68 near UH3



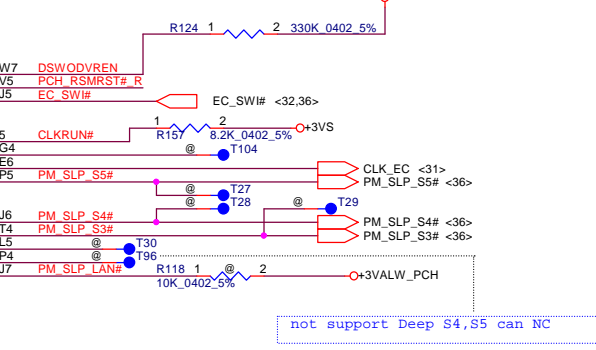
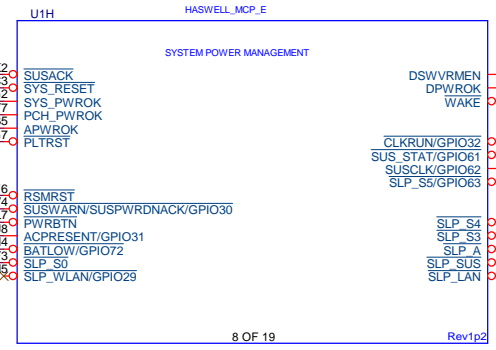
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	HSW MCP(4/11) CLK,SPI,SMBUS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	ZRMAA/ZEMAA	0.1
				Date:	Sunday, April 07, 2013	Sheet 8 of 49





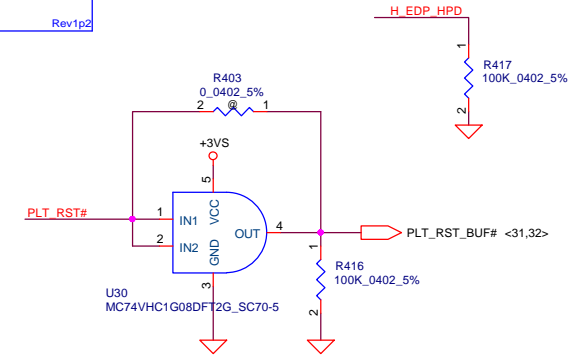
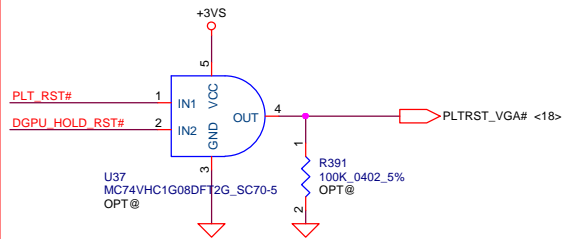
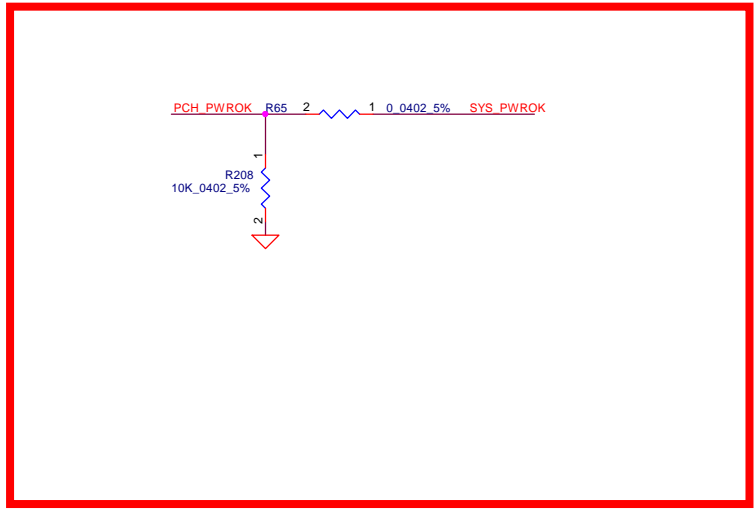
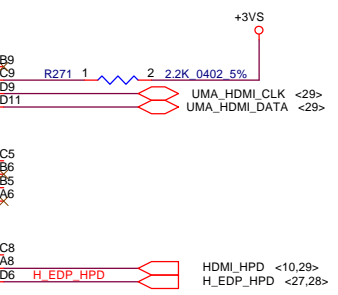
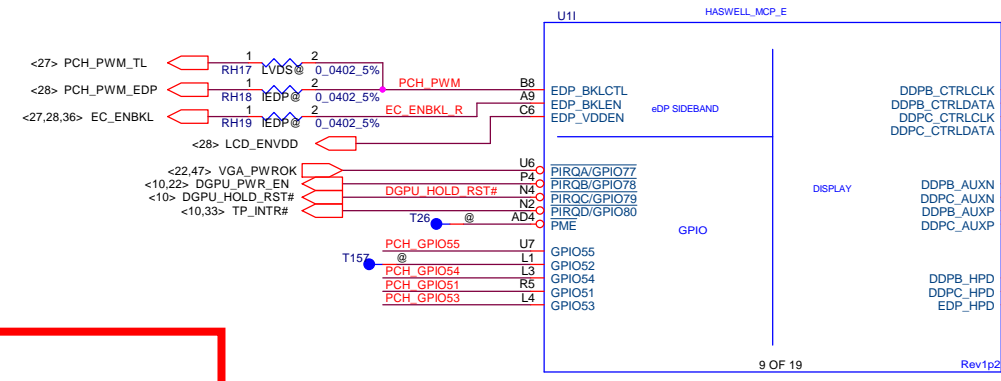
Note for PCH\_ACIN: Deep Sx need use EC GPIO for ACPRESENT function

**Need to Check**



DDPB\_CTRLDATA: Port B Detected  
DDPC\_CTRLDATA: Port C Detected

\* 1: Port B or C is detected  
0: Port B or C is not detected  
(Have internal PD)

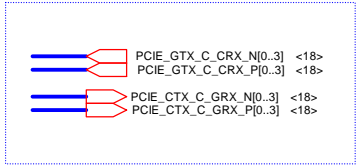


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				Date:	Document Number
				Sheet	9 of 49

**Compal Electronics, Inc.**  
**HSW MCP(5/11) PM,GPIO,DDI**

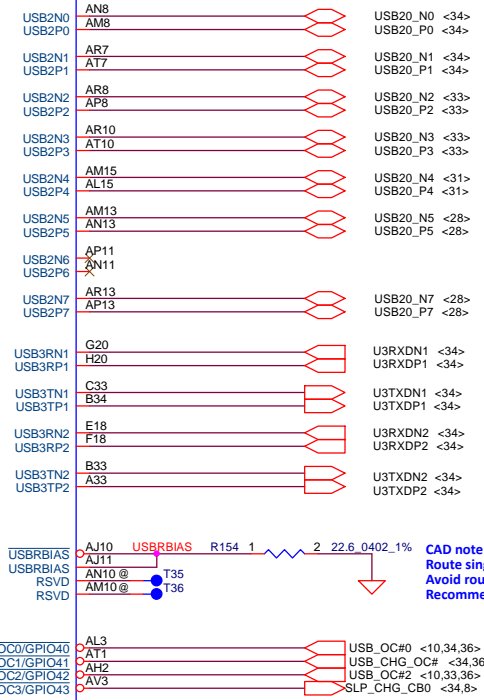
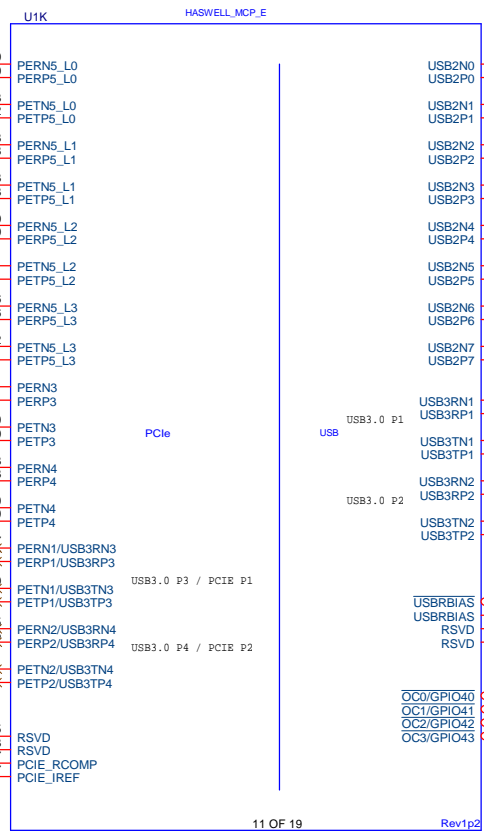
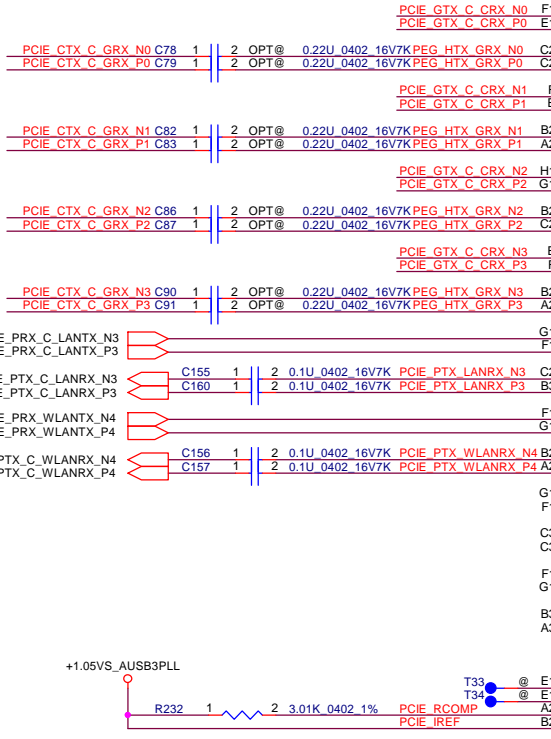
Document Number: **ZRMAA/ZEMAA**  
Rev: 0.1  
Date: Sunday, April 07, 2013



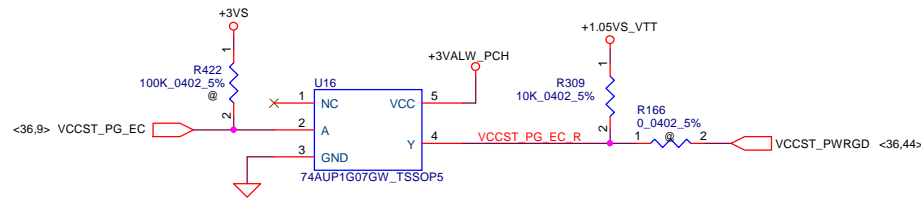


PCIE LAN

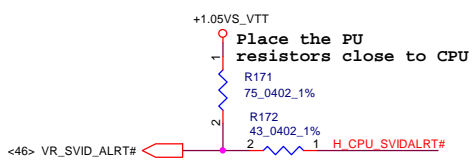
WLAN



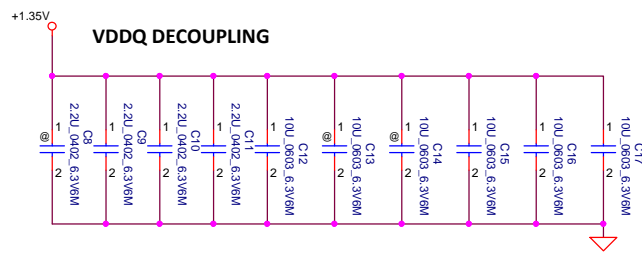
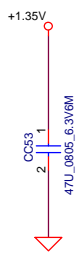
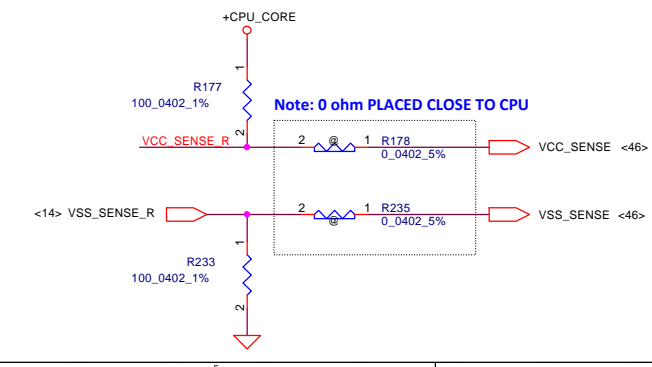
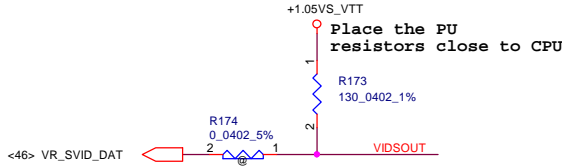
USB-Right1  
USB-Right2  
USB-Left1  
CardReader  
WiMAX / BT  
Touch Screen  
Camera  
CAD note:  
Route single-end 50-ohms and max 450-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils  
USB-Right Rear  
USB-Right Front  
USB-Left



### SVID ALERT



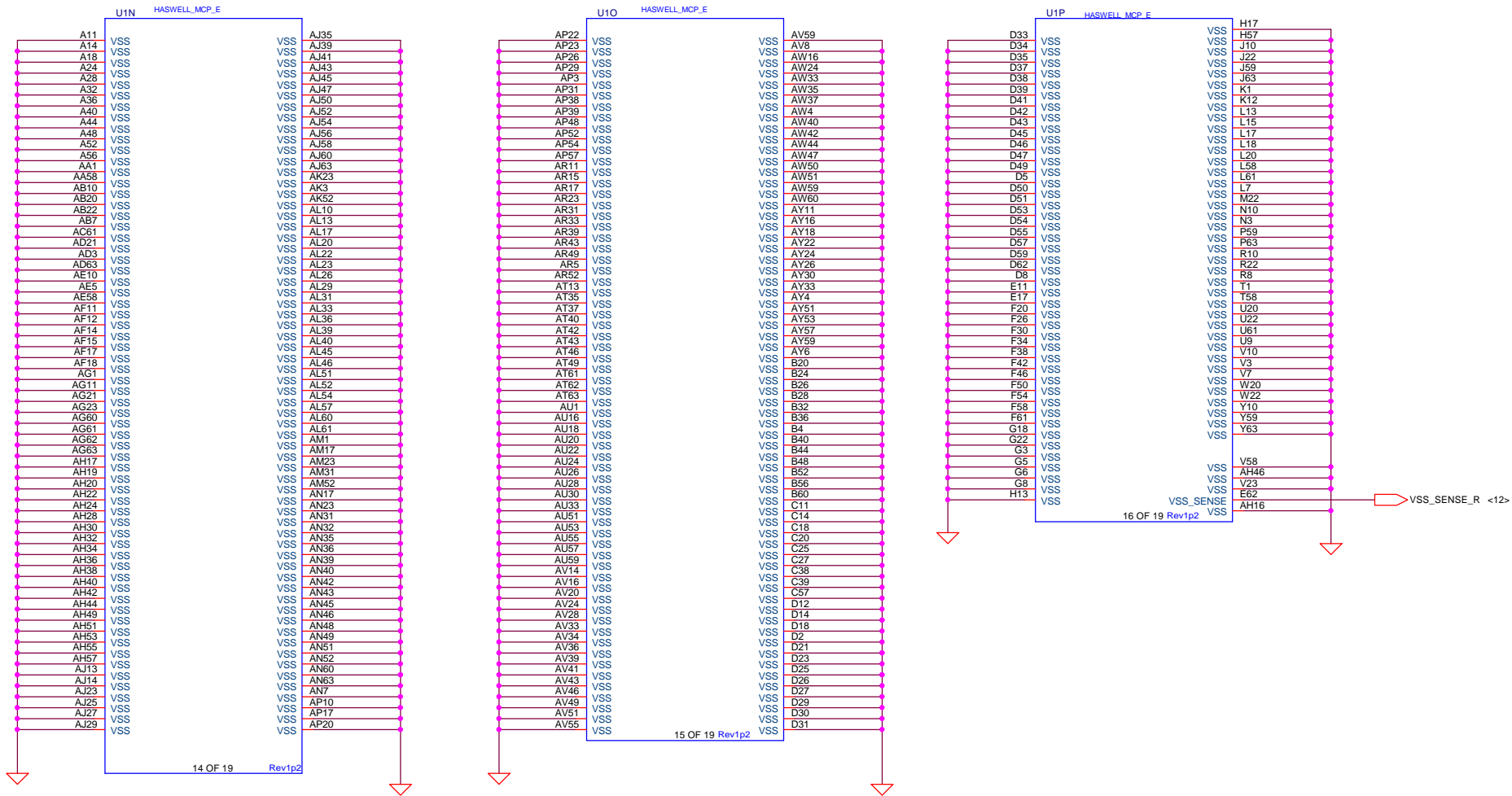
### SVID DATA



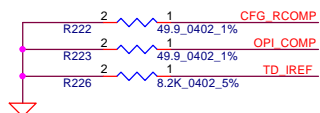
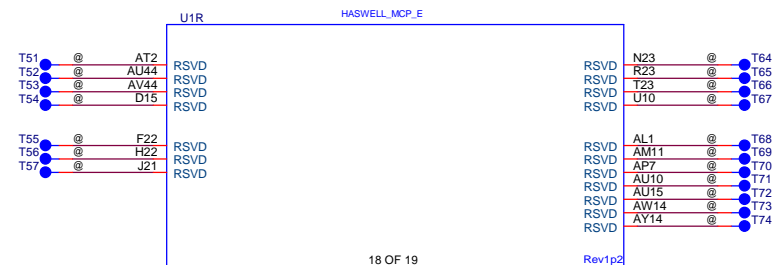
+1.35V : 470UF/2V/7343 \*2  
 10UF/6.3V/0603 \* 6  
 2.2UF/6.3V/0402 \* 4

Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/07/10		Deciphered Date		2013/07/10		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						HSW MCP(8/11) Power					
						Size		Document Number		Rev	
						Custom		ZRMMA/ZEMAA		0.1	
						Date:		Sunday, April 07, 2013		Sheet 12 of 49	



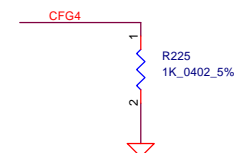


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2012/07/10	Deciphered Date	2013/07/10	Title
				HSW MCP(10/11) GND	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number				Rev
Custom	ZRMAA/ZEMAA				0.1
Date:		Sunday, April 07, 2013		Sheet	14 of 49



The diagram shows a circuit connection for the CFG3 pin. A purple line labeled 'CFG3' at the top connects to a resistor labeled 'R224 1K\_0402\_1%' and 'Q2'. The resistor is represented by a zigzag line with terminals '1' and '2'. Terminal '1' is connected to the CFG3 line, and terminal '2' is connected to a ground symbol (a triangle with a circle inside).

Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

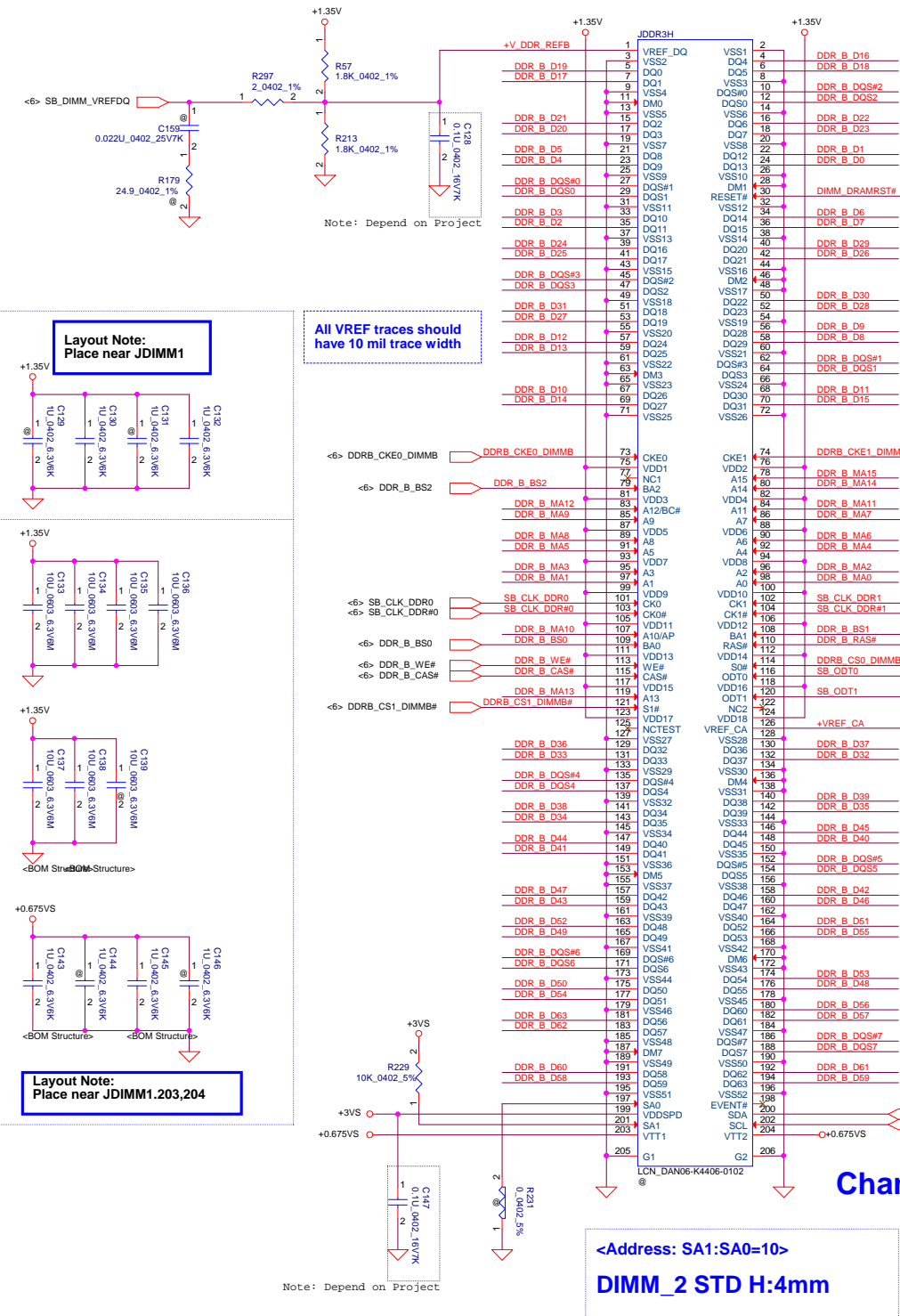


Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>HSW MCP(11/11) RSVD</b>	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number <b>ZRMAA/ZEMAA</b>
				Date: Sunday, April 7, 2013	Sheet 15 of 49
				Rev	0.1





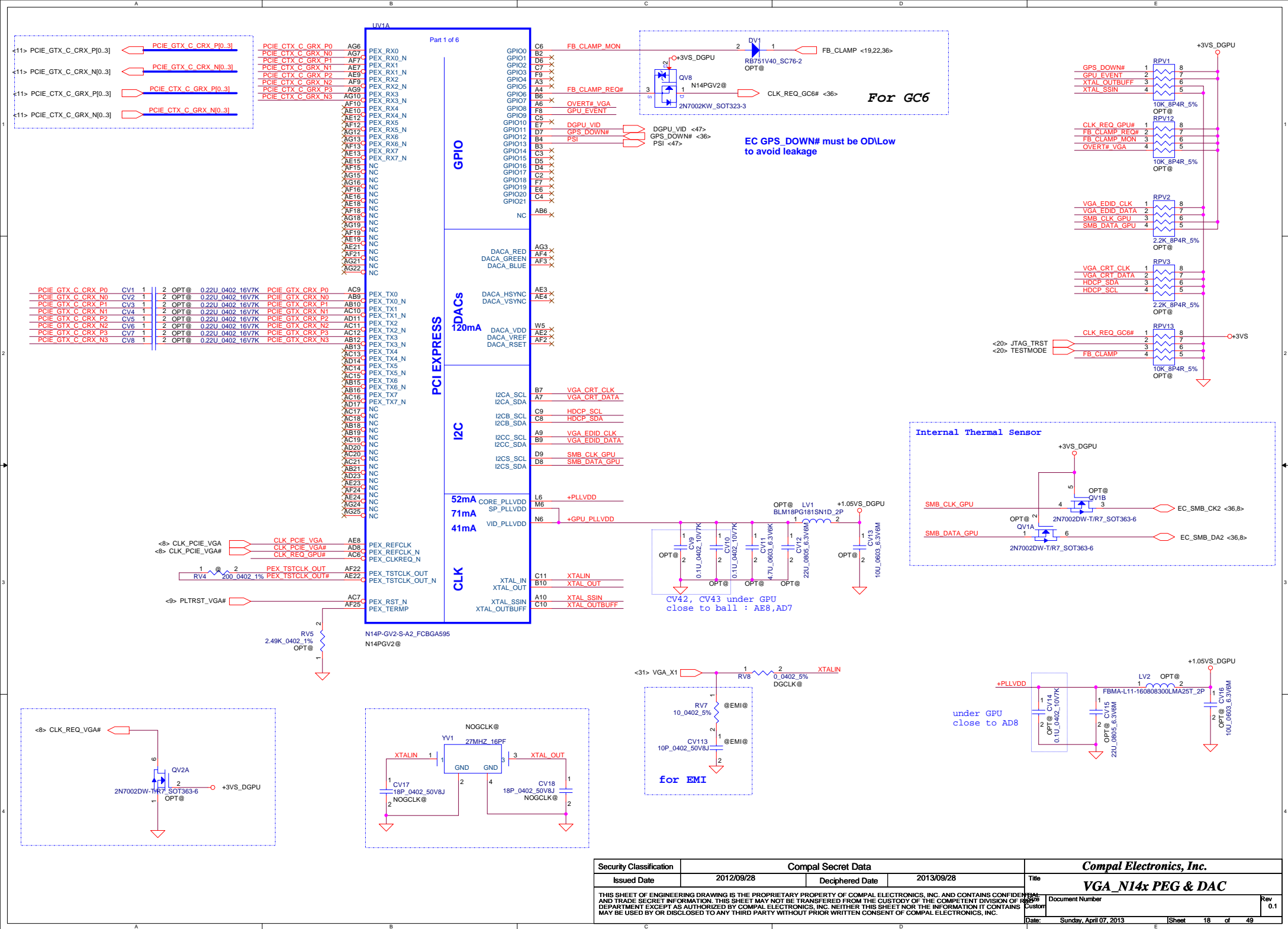


DDR3 SO-DIMM B  
Reverse Type  
H=9.0mm

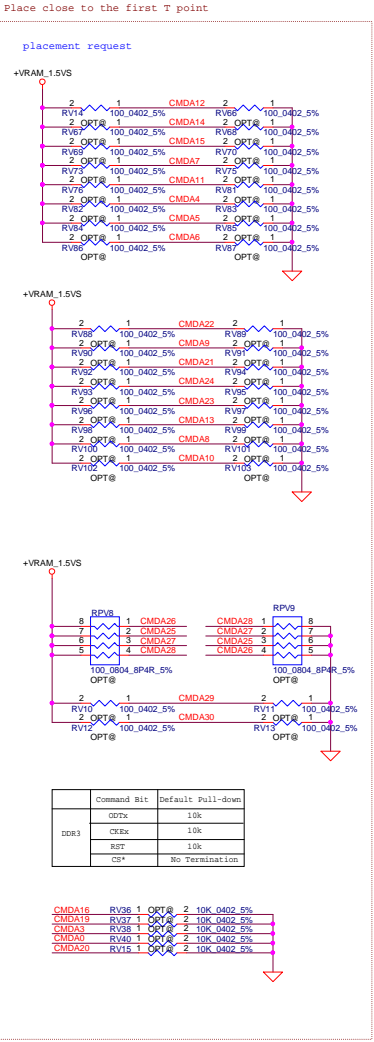
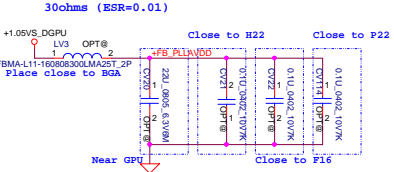
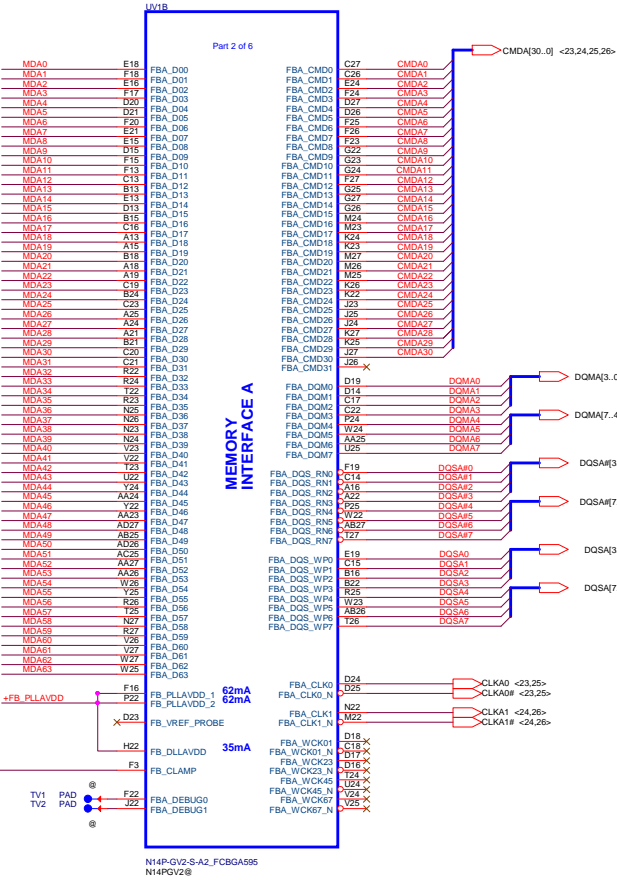
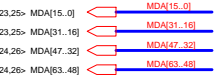
DDR_B_DQ5# [0.7]	<6>
DDR_B_DQ5 [0.7]	<6>
DDR_B_DQ [0.63]	<6>
DDR_B_MA [0.15]	<6>
DIMM_DRAMRST#	<16,5>
DDR_B_D6	
DDR_B_D7	
DDR_B_D29	
DDR_B_D26	
DDR_B_D30	
DDR_B_D28	
DDR_B_D9	
DDR_B_D8	
DDR_B_DQ5#1	
DDR_B_DQ5#1	
DDR_B_D11	
DDR_B_D15	
DDR_B_CKE0_DIMMB	<6>
DDR_B_BS2	
DDR_B_MA12	
DDR_B_MA9	
DDR_B_MA8	
DDR_B_MA5	
DDR_B_MA3	
DDR_B_MA1	
SB_CLK_DDR0	
SB_CLK_DDR#0	
DDR_B_MA10	
DDR_B_BS0	
DDR_B_WE#	
DDR_B_CAS#	
DDR_B_MA13	
DDR_B_CS1_DIMMB#	
DDR_B_D36	
DDR_B_D33	
DDR_B_DQ5#4	
DDR_B_DQ5#4	
DDR_B_D38	
DDR_B_D34	
DDR_B_D35	
DDR_B_D44	
DDR_B_D41	
DDR_B_D47	
DDR_B_D43	
DDR_B_D52	
DDR_B_D49	
DDR_B_DQ5#6	
DDR_B_DQ5#6	
DDR_B_D50	
DDR_B_D54	
DDR_B_D63	
DDR_B_D62	
DDR_B_D60	
DDR_B_D60	
PM_SMBDATA	<16,31,33,8>
PM_SMBCLK	<16,31,33,8>

Channel B

<Address: SA1:SA0=10>  
DIMM\_2 STD H:4mm



VRAM Interface



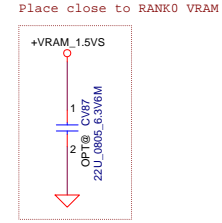
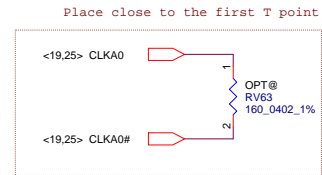
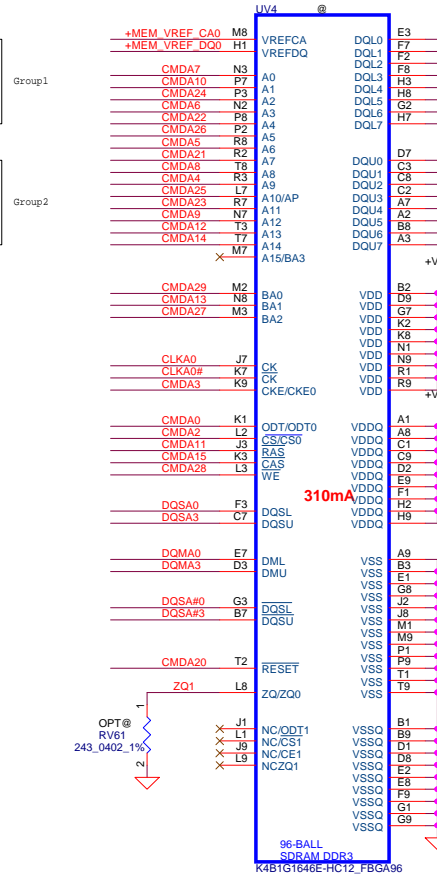
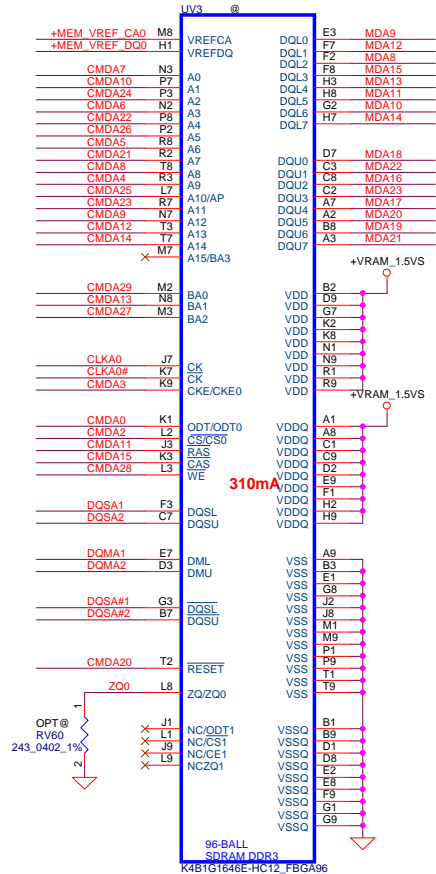
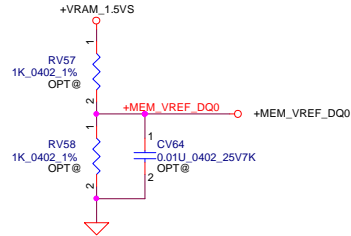
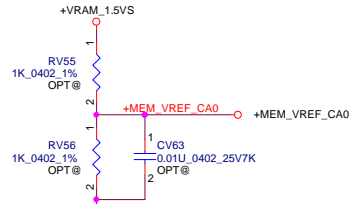
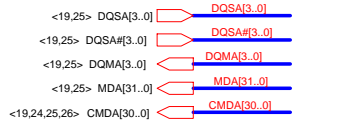
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/28	Deciphered Date	2013/09/28	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Document Number	Rev
Date			Sunday, April 07, 2013	19 of 49







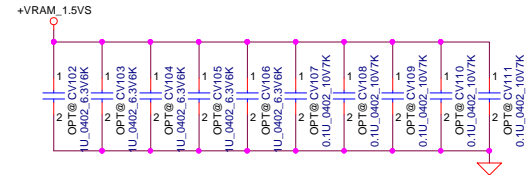
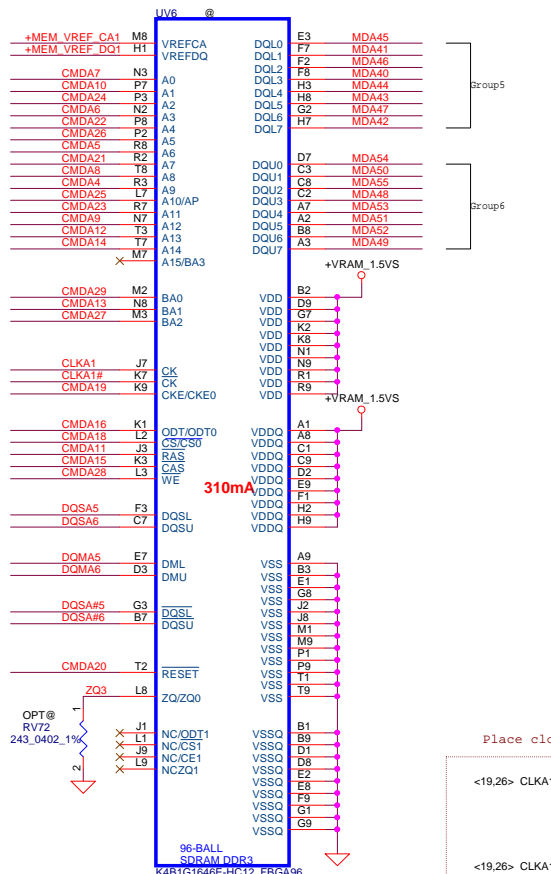
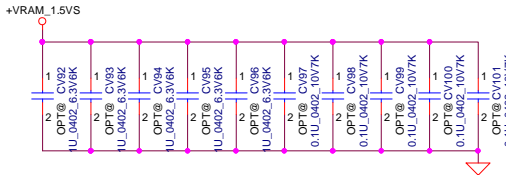
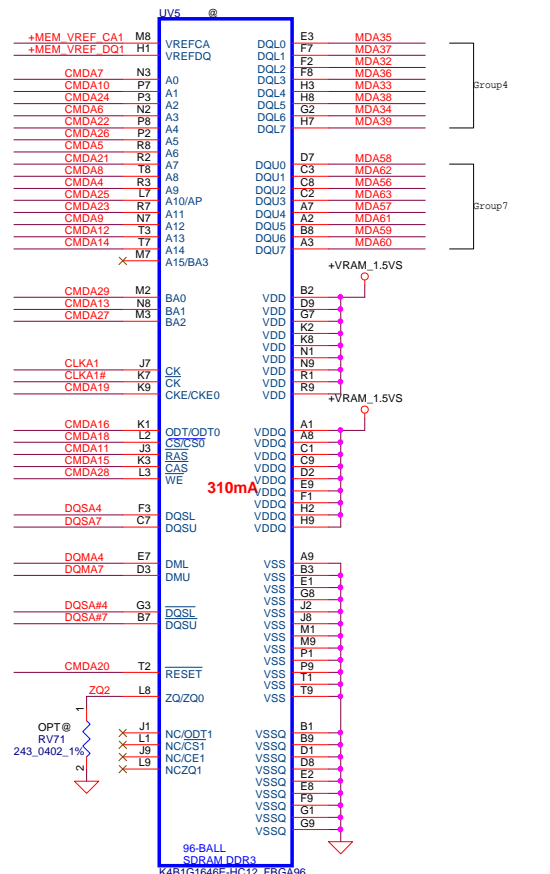
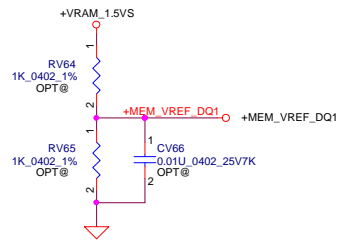
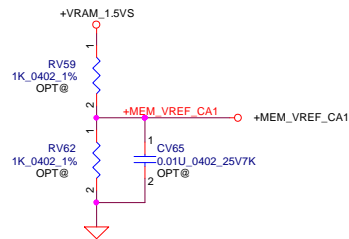
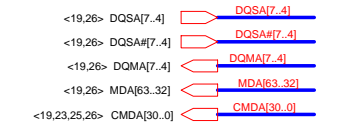
# RANK 0 [31...0] VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

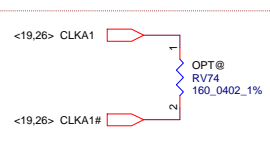


# RANK 0 [63...32] VRAM DDR3 Chips

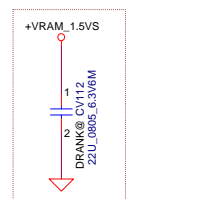


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Place close to the first T point

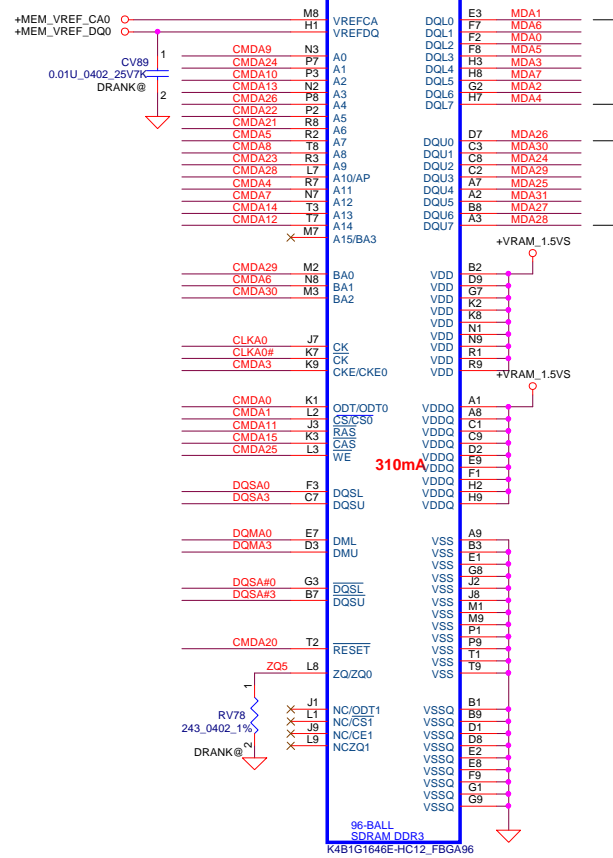
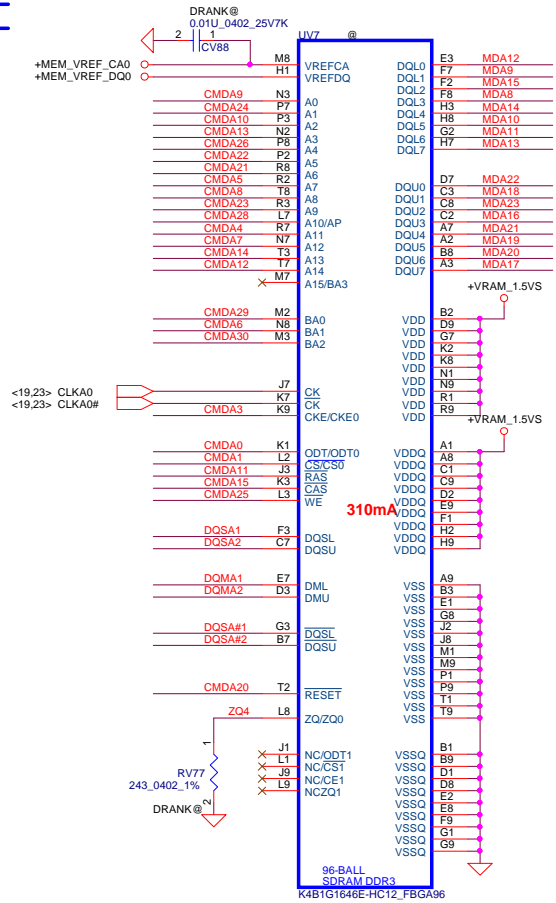
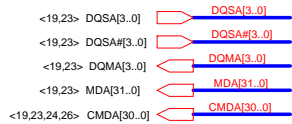


Place close to RANK1 VRAM





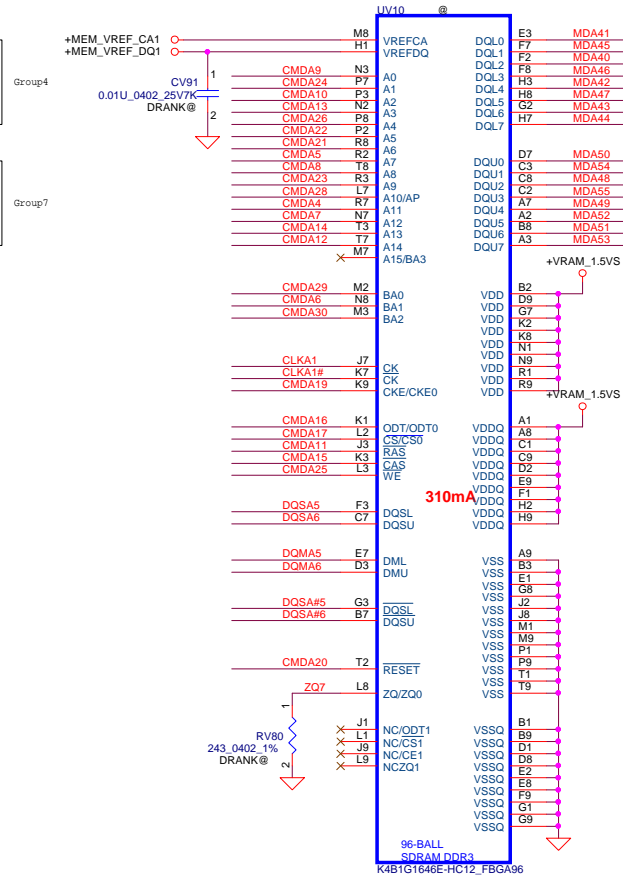
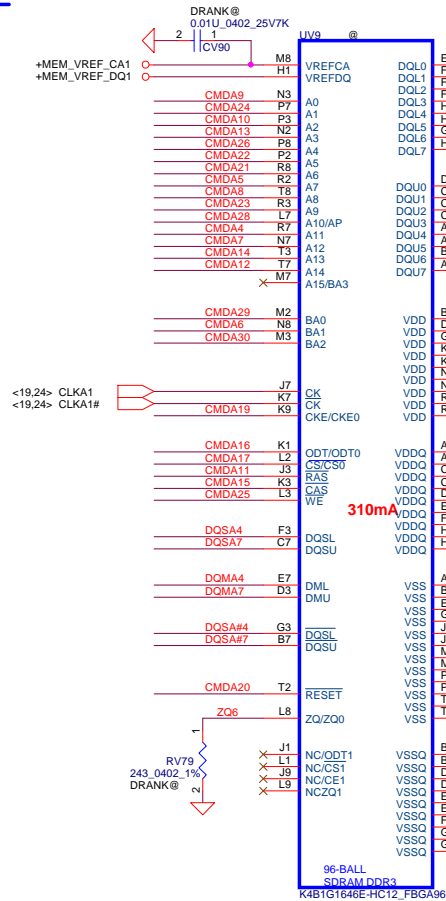
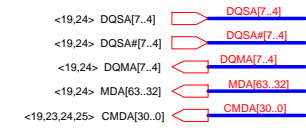
## RANK 1 [31...0]



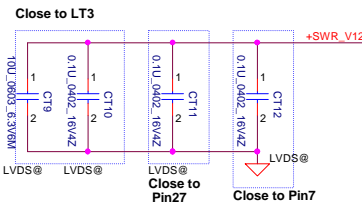
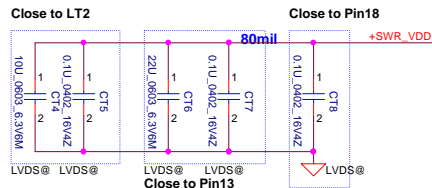
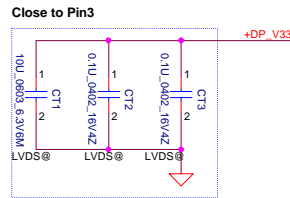
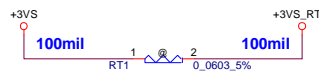
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/09/28	Deciphered Date	2013/09/28	Title	VGA N14x VRAM RANK 1L	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT TO ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc Number	Rev	
				Custom	0.1	
Date:		Sunday, April 07, 2013		Sheet	25	of 49

## RANK 1 [63...32]



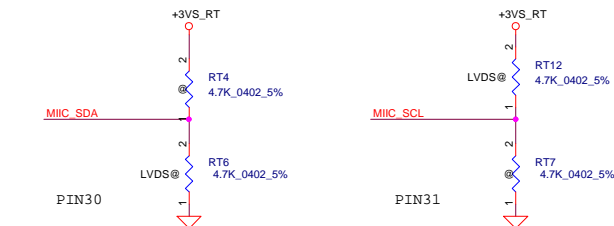
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



## Mode Configure

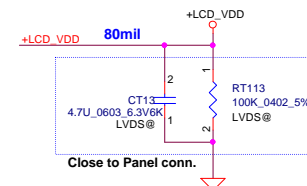
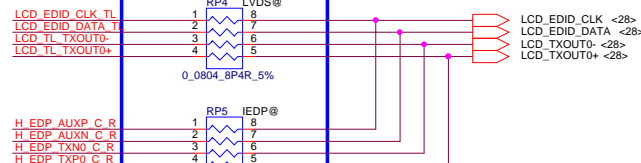
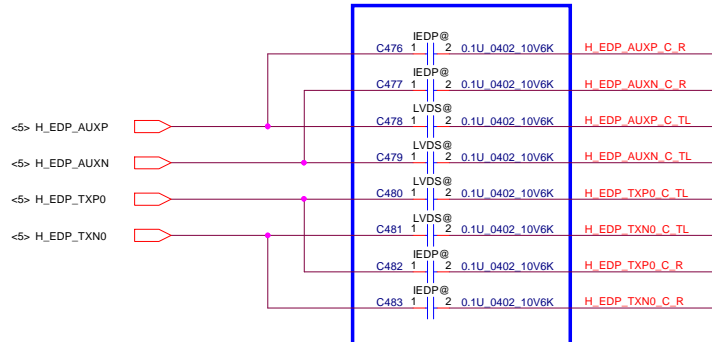
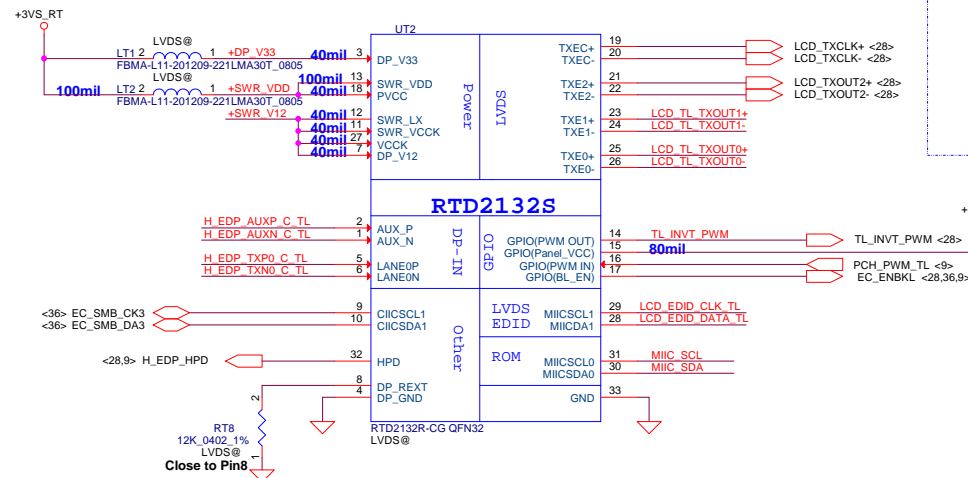
※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.  
BP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.  
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >



## SWR / LDO Mode select

※LDO mode is adopted as default power regulator mode.  
Also can implement SWR mode by add inductor.



Place co-lay Resistor back to back on TOP and BOT

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

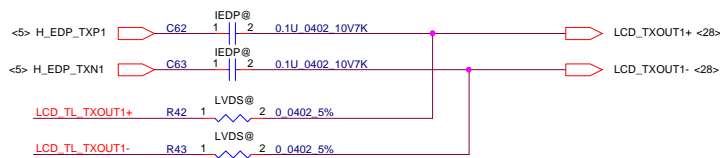
\* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

\* Version R has internal level shifter, remove level shifter circuit on AMD platform

## Different between 2132S and 2132R

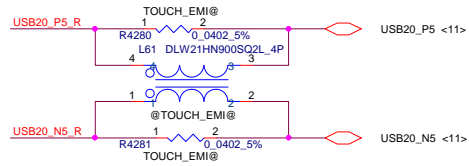
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter



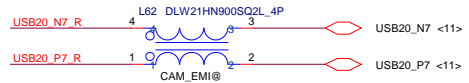
Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date
2013/06/30		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		<p>Document Number</p> <p>ZRMAA/ZEMAA</p> <p>Rev 0.1</p> <p>Date: Sunday, April 07, 2013</p> <p>Sheet 27 of 49</p>

## LVDS Translator - RTD2132S

BTO : TOUCH\_EMI@

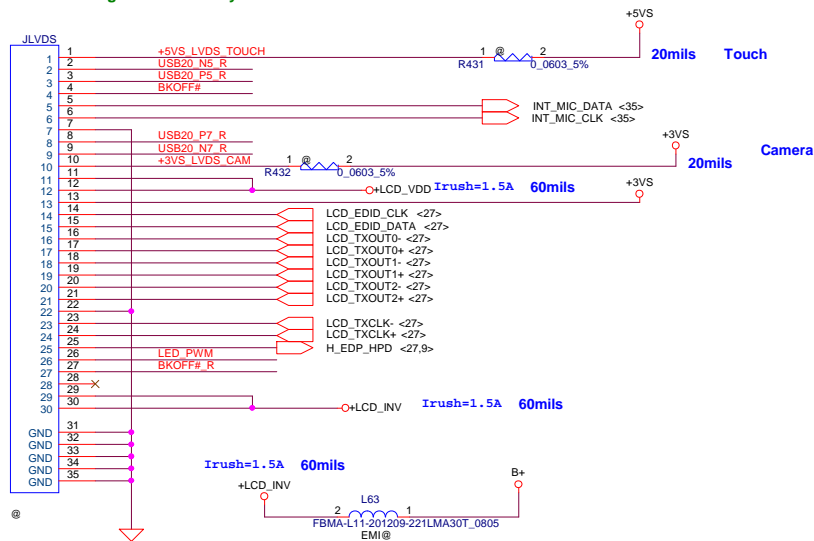


EMI request - Close to JEDP connector

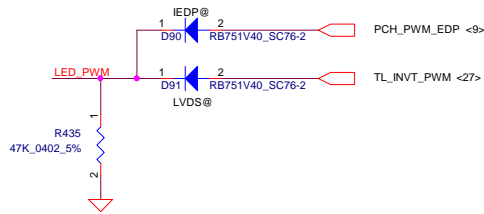
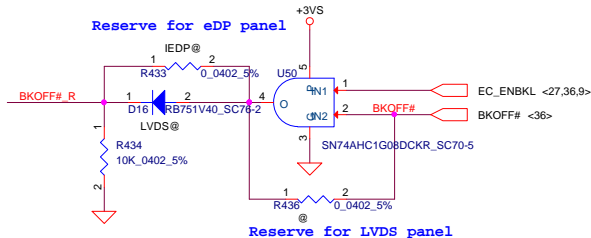
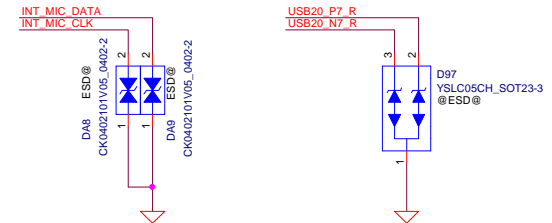
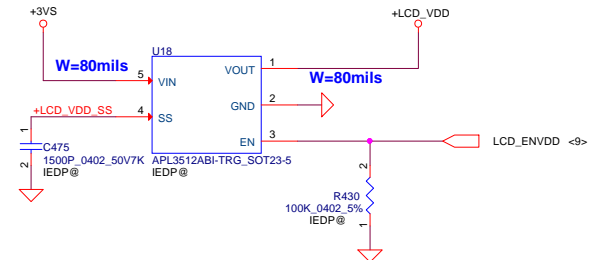


## LVDS colay eDP cable

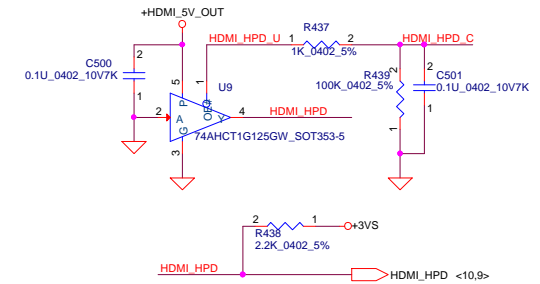
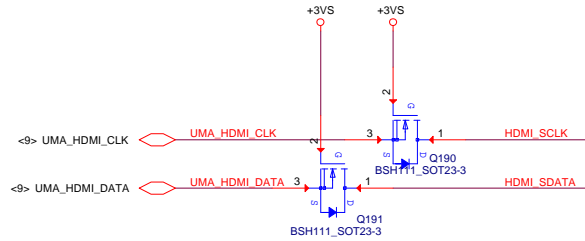
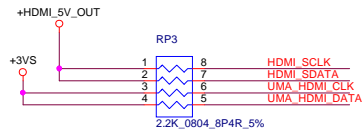
Pin define will be change after ME ready



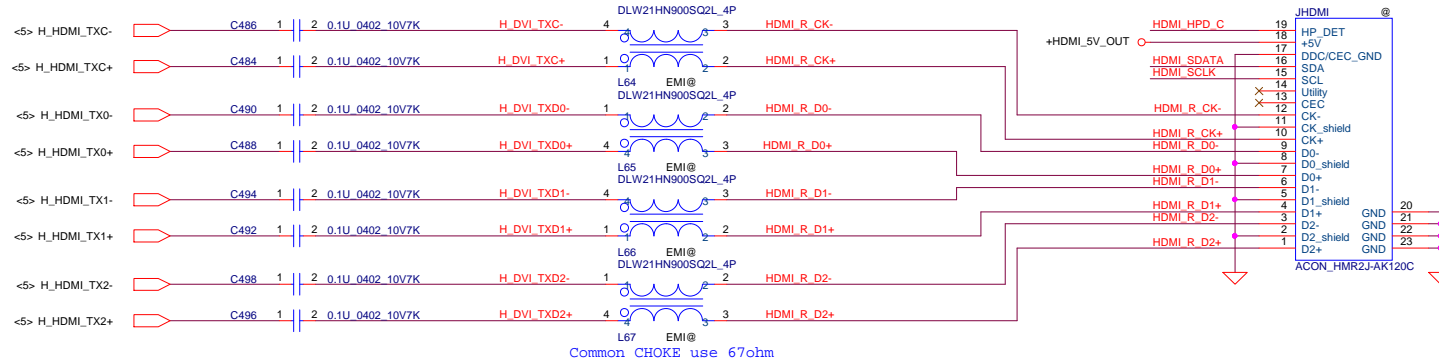
## LCD POWER CIRCUIT (For EDP panel only)



Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2012/04/19		Deciphered Date		2015/04/19		Title					
								LVDS					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.													
Document Number ZRM/AA/ZEMAA													
						Date: Sunday, April 07, 2013		Sheet 28 of 49					



## HDMI Connector



HDMI Royalty

ZZZ HDM145@

RO0000003HM

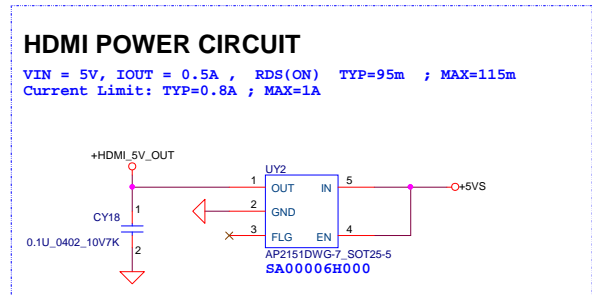
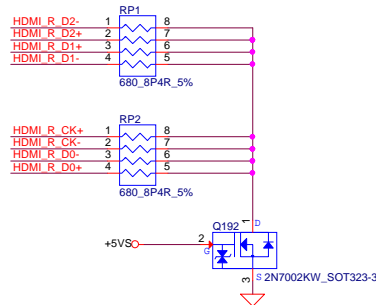
HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HM

HDMI W/Logo: RO0000002HM

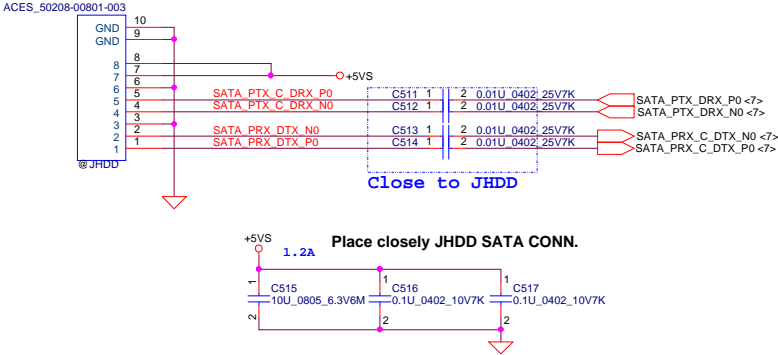
HDMI W/Logo + HDCP: RO0000003HM

please manually load  
this virtual material to 45@ BOM



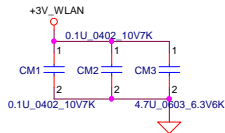
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI Conn.		
				Document Number		
				ZRM00006H000		
				Rev		
				0.1		
				Date: Sunday, April 07, 2013		
				Sheet 29 of 49		

SATA HDD Conn.



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HDD/Gsensor
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				ZRMAA/ZEMAA	0.1
				Date: Sunday, April 07, 2013	Sheet 30 of 49

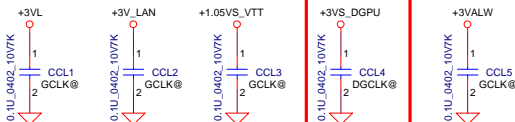
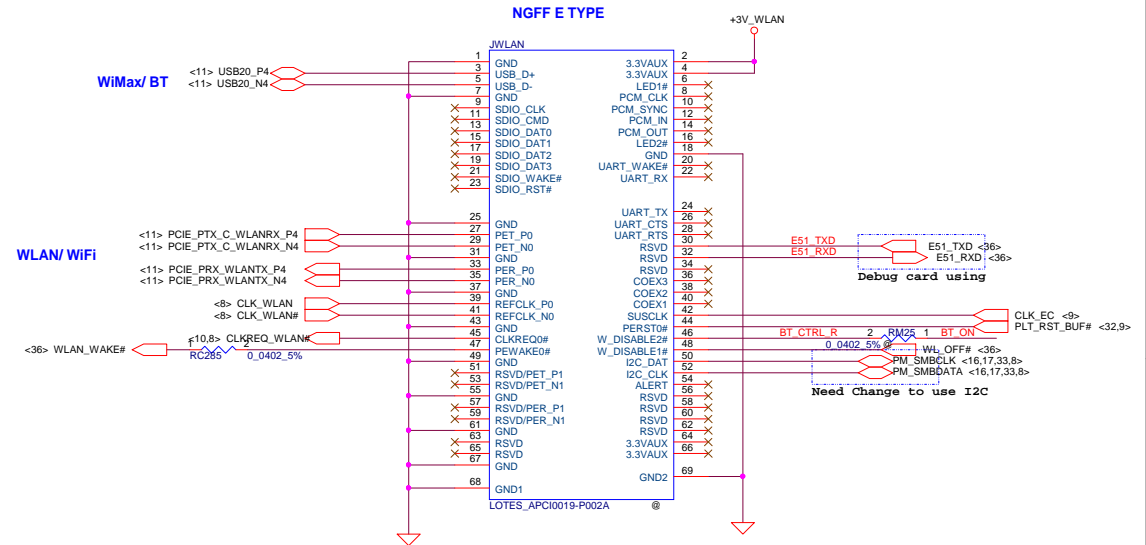
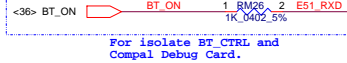
Slot 1 Half PCIe Mini Card-WLAN



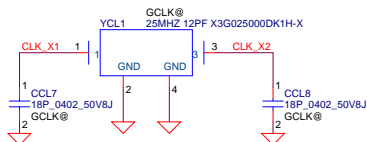
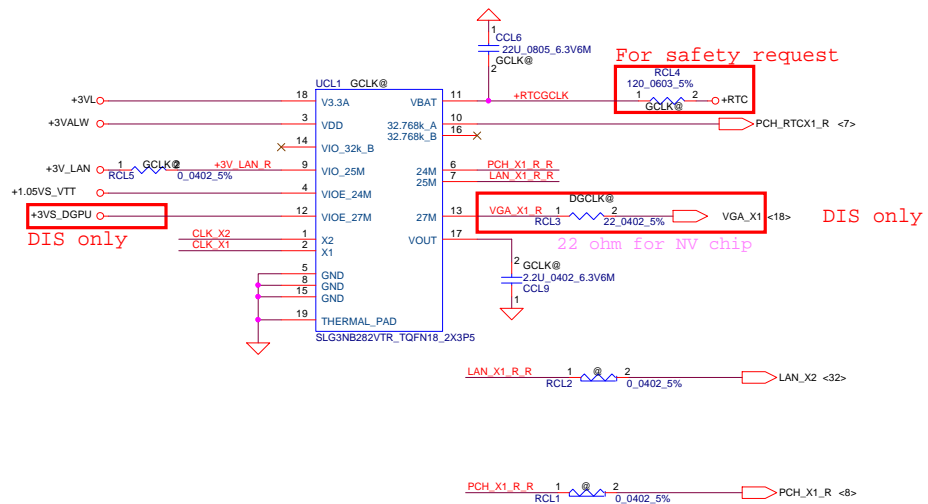
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

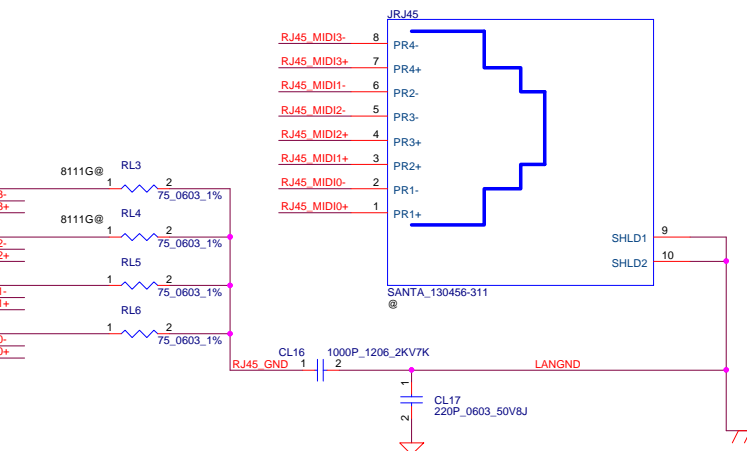
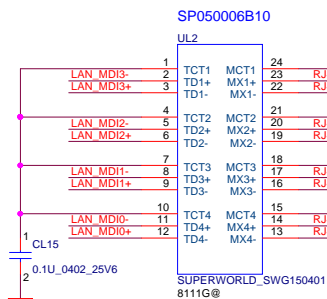
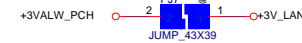
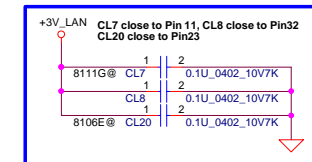
From EC



DIS only



## UL1



LAN	WOL	LAN_EN		ISOLATED	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

\*  
S3: after SUSP# assert low over 100ms  
S4/S5: after SYSON assert low over 100ms

3VS

RL24 2

1 10K 0402 5%

LANCLK\_REQ#

<10,8> LAN\_EN

<8> CLKREQ\_LAN#

LANCLK\_REQ#

QL53  
2N7002KW SOT23-3

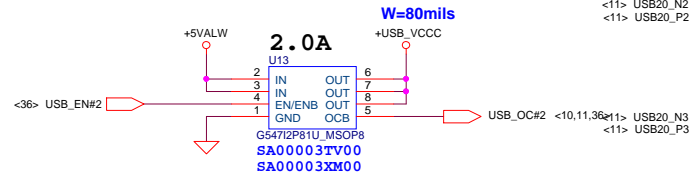
	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PCle-LAN-RTL8105E</b>	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF REGISTRATION DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				<b>ZRMAA/ZEMAA</b> Date: Sunday, April 07, 2013	0.1

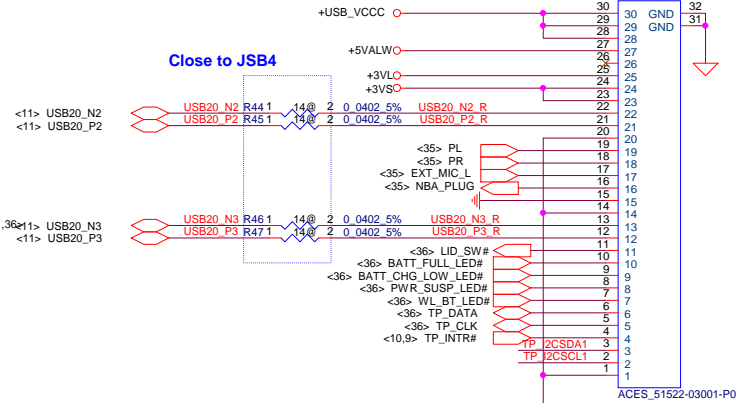


# Small board Conn

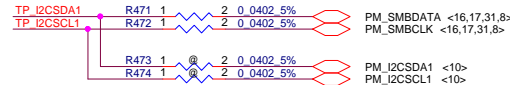
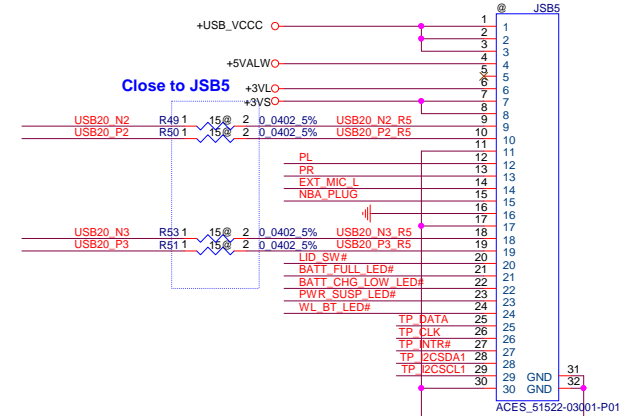
## Left USB 2.0 x 1



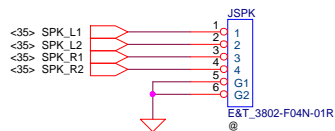
## Close to JSB4



## Close to JSB5

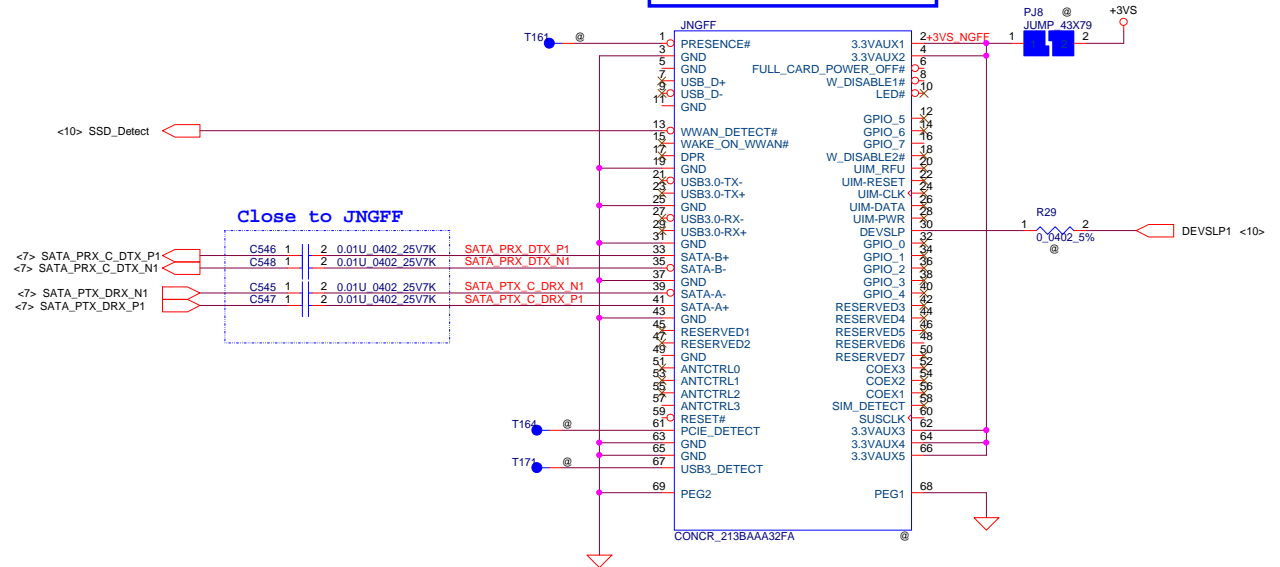


## SPK Conn.

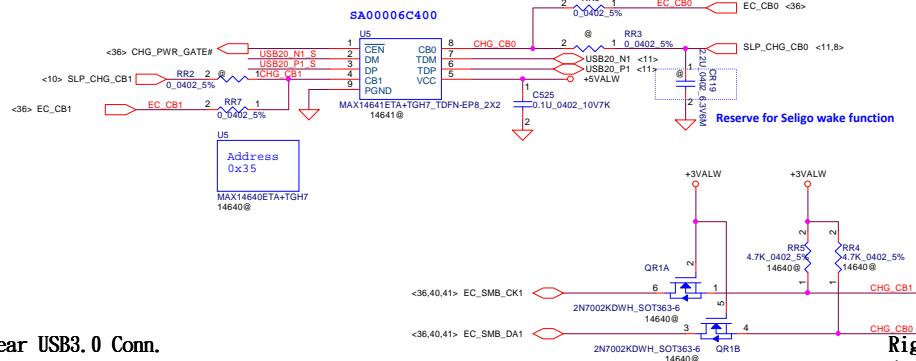


## NGFF SSD B Type connector

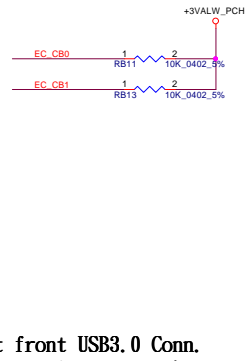
P/N:SP071212280



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	<b>USB-CardReader Genesys GL834L</b>		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		
				Size Custom	Document Number	Rev
				ZRMAA/ZEMAA		0.1
				Date:	Sunday, April 07, 2013	Sheet 33 of 49



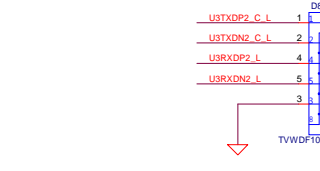
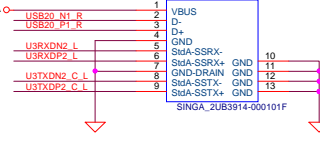
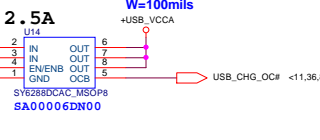
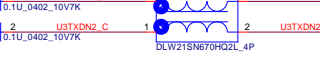
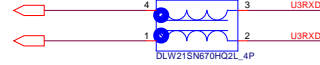
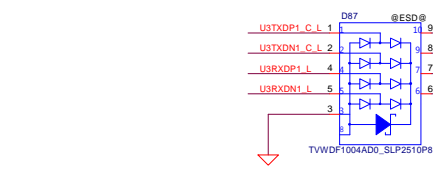
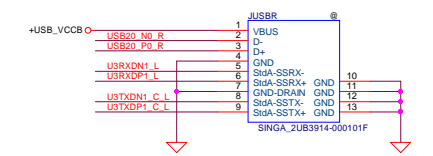
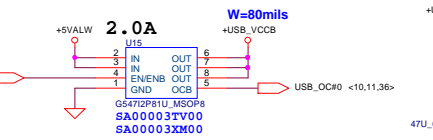
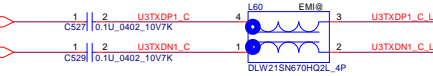
Right rear USB3.0 Conn.

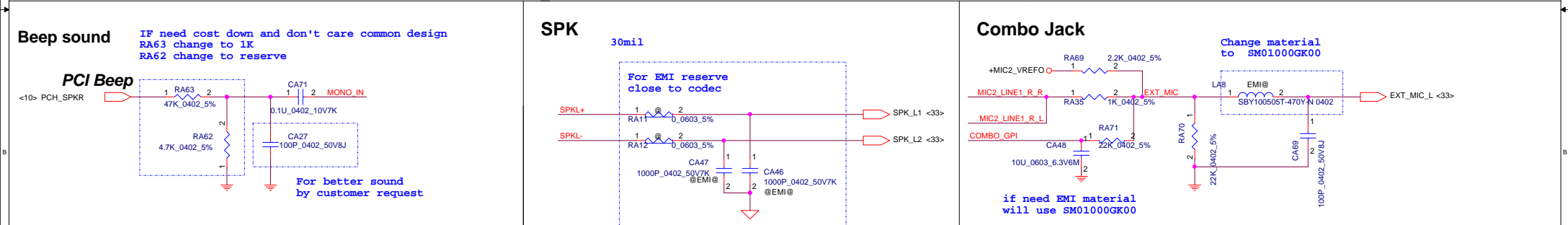


Right front USB3.0 Conn.  
(Support S&C function)

## USB Sleep & Charge

State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM, including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode. DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.





# SPK

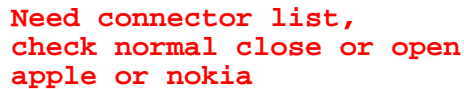
30mil

For EMI reserve  
close to codec

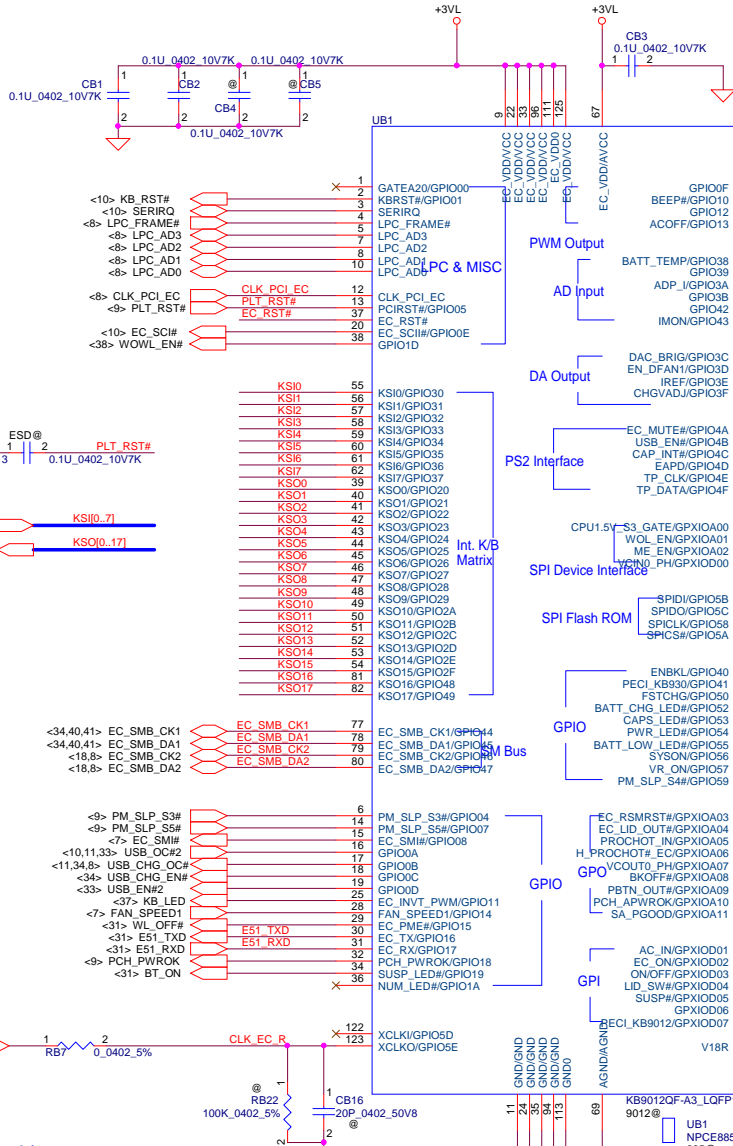
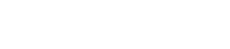
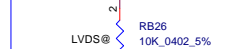
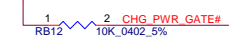
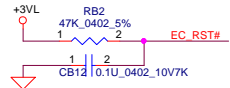
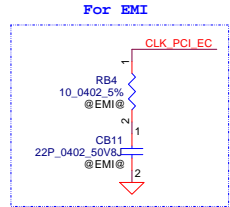
SPKL+ 1 2 RA11 0.0603\_5% SPKL- 1 2 RA12 0.0603\_5% SPKR+ 1 2 RA13 0.0603\_5% SPKR- 1 2 RA14 0.0603\_5%

CA47 1000P\_0402\_50V7K @EMI@ CA46 1000P\_0402\_50V7K @EMI@ CA45 1000P\_0402\_50V7K @EMI@

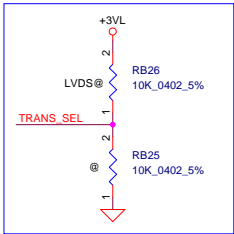
SPK\_L1 <33> SPK\_L2 <33> SPK\_R1 <33> SPK\_R2 <33>



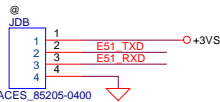
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2012/07/25	Deciphered Date	2013/07/25	Title	<b>Cover Sheet</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Part Number Customer	Document Number Revision	Rev 0.1
				Date:	Sunday, April 07, 2013	Sheet 35 of 49



Signal pull high is default status (ROM only mode).  
If signal pull low, EC will send translator code to chip.(EP mode)

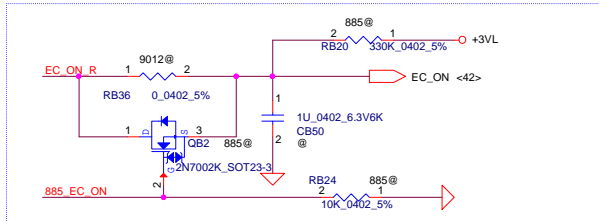


**EC DEBUG port**

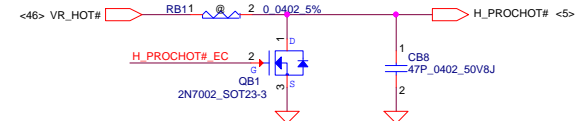


**Voltage Comparator Pins FOR 9012 A3**

VCIN0 pin109	VCIN1 pin102	>1.2V	<1.2V
VCOUT0 pin104		HIGH (default)	LOW
VCOUT1 pin103		HIGH	LOW (default)



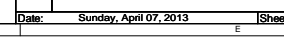
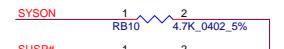
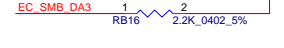
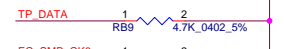
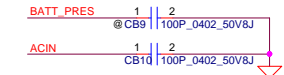
For KB9012 EC\_ON low pulse work around



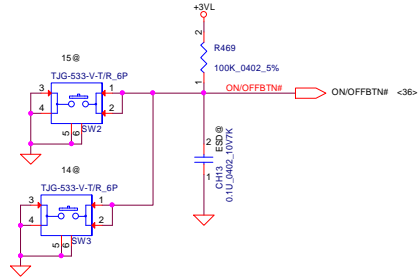
Reserve this signal to EC by SW demand  
2011/10/18a

VCIN0\_PH connect to power portion (9012 only)

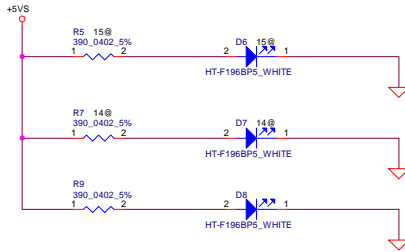
PROCHOT\_IN connect to power portion (9012 only)



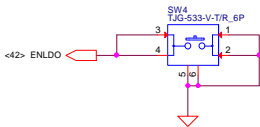
Power Button



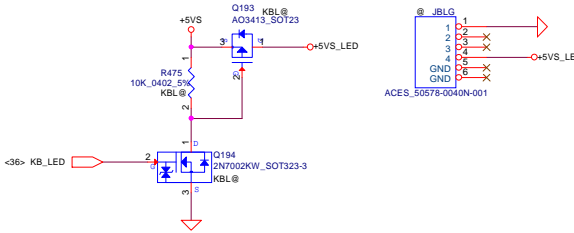
POWER LED



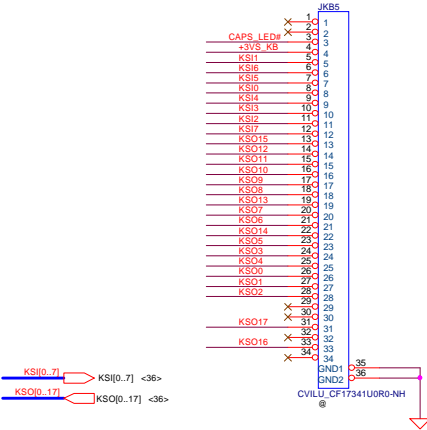
Battery Reset



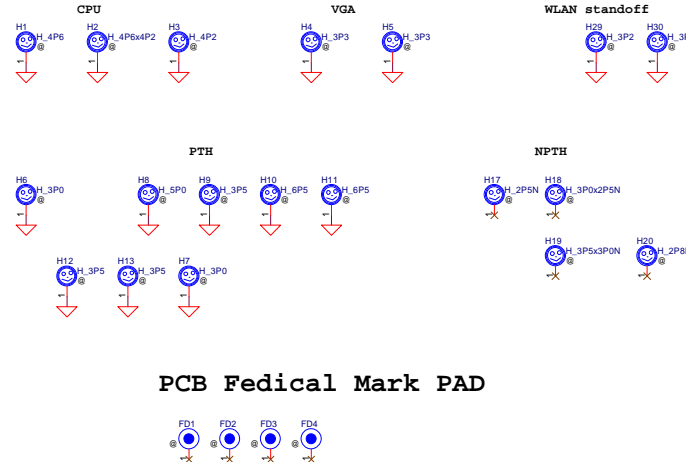
Keyboard LED



15 " KEYBOARD CONN.



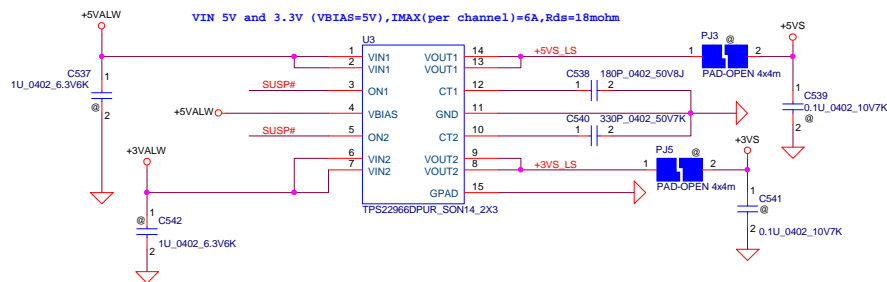
Screw Hole



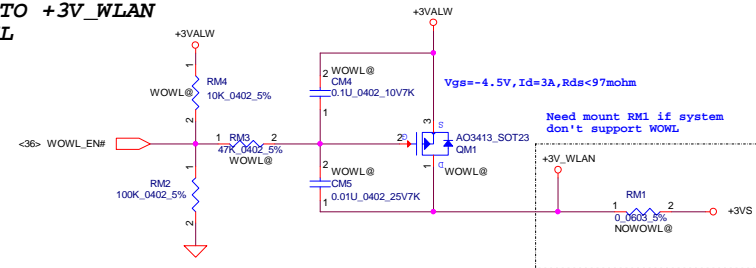
PCB Federal Mark PAD



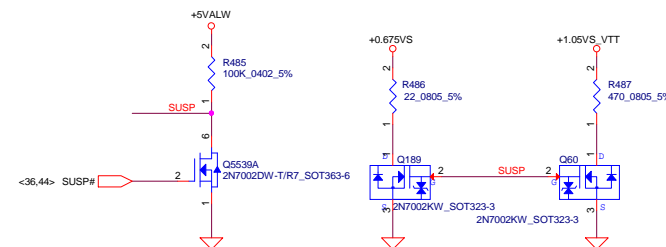
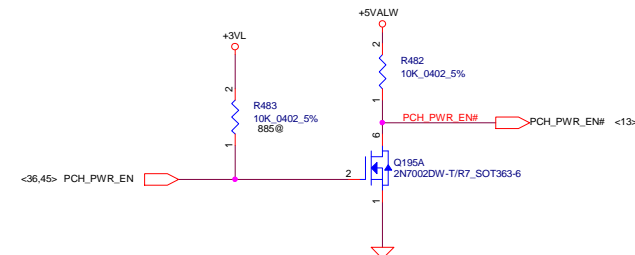
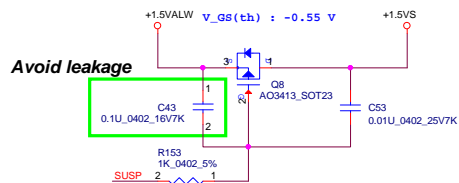
**+3VALW TO +3VS**  
**+5VALW TO +5VS**  
**Load Switch**



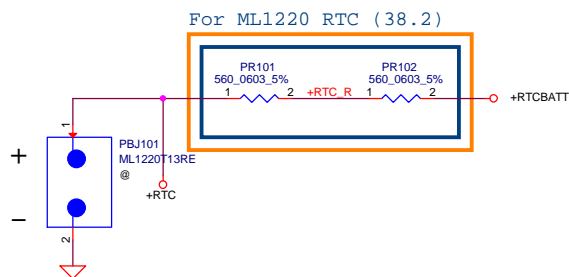
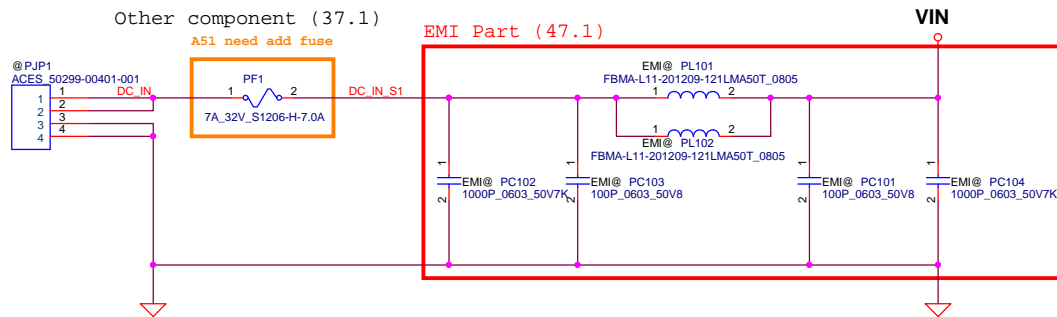
**+3VALW TO +3V\_WLAN**  
**for WOWL**



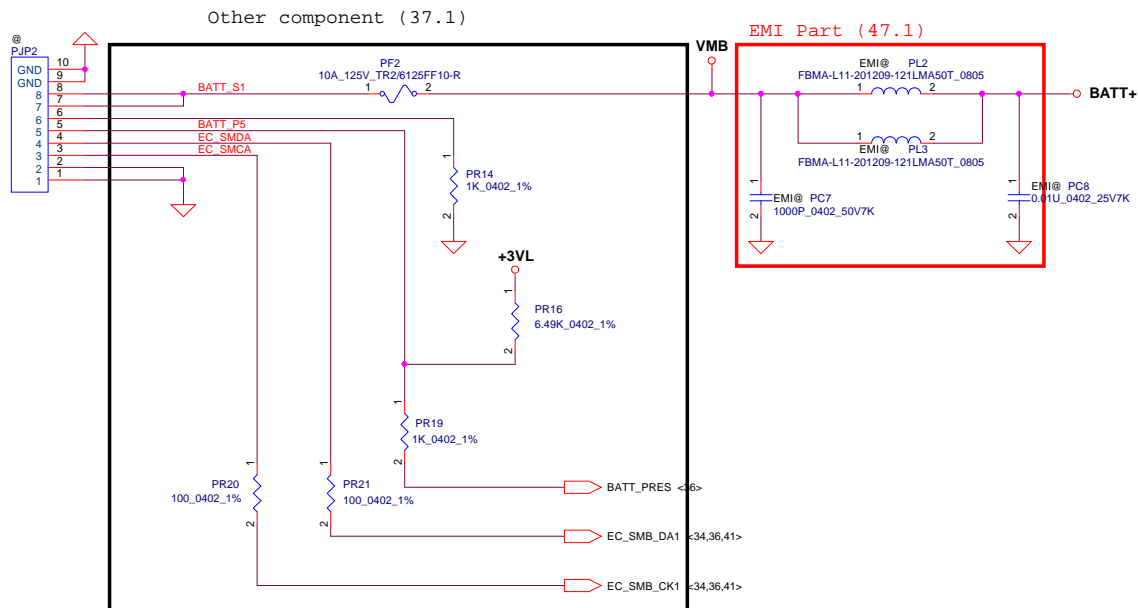
**+1.5VALW to +1.5VS**



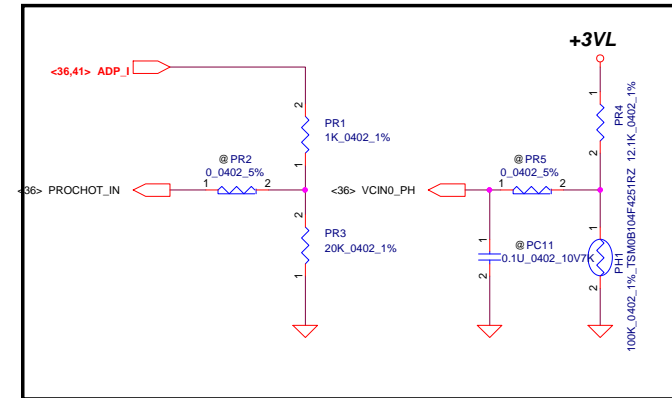
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	DC-DC INTERFACE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RA&S DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	ZRMAA/ZEMAA
				Date	Sunday, April 07, 2013
				Sheet	38 of 49
				Rev	0.1



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date	Title <b>DCIN</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RADEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number	<b>ZRMAA</b>	
		Date:	Sheet 39 of 49	Rev 0.1



OTP (39.7)



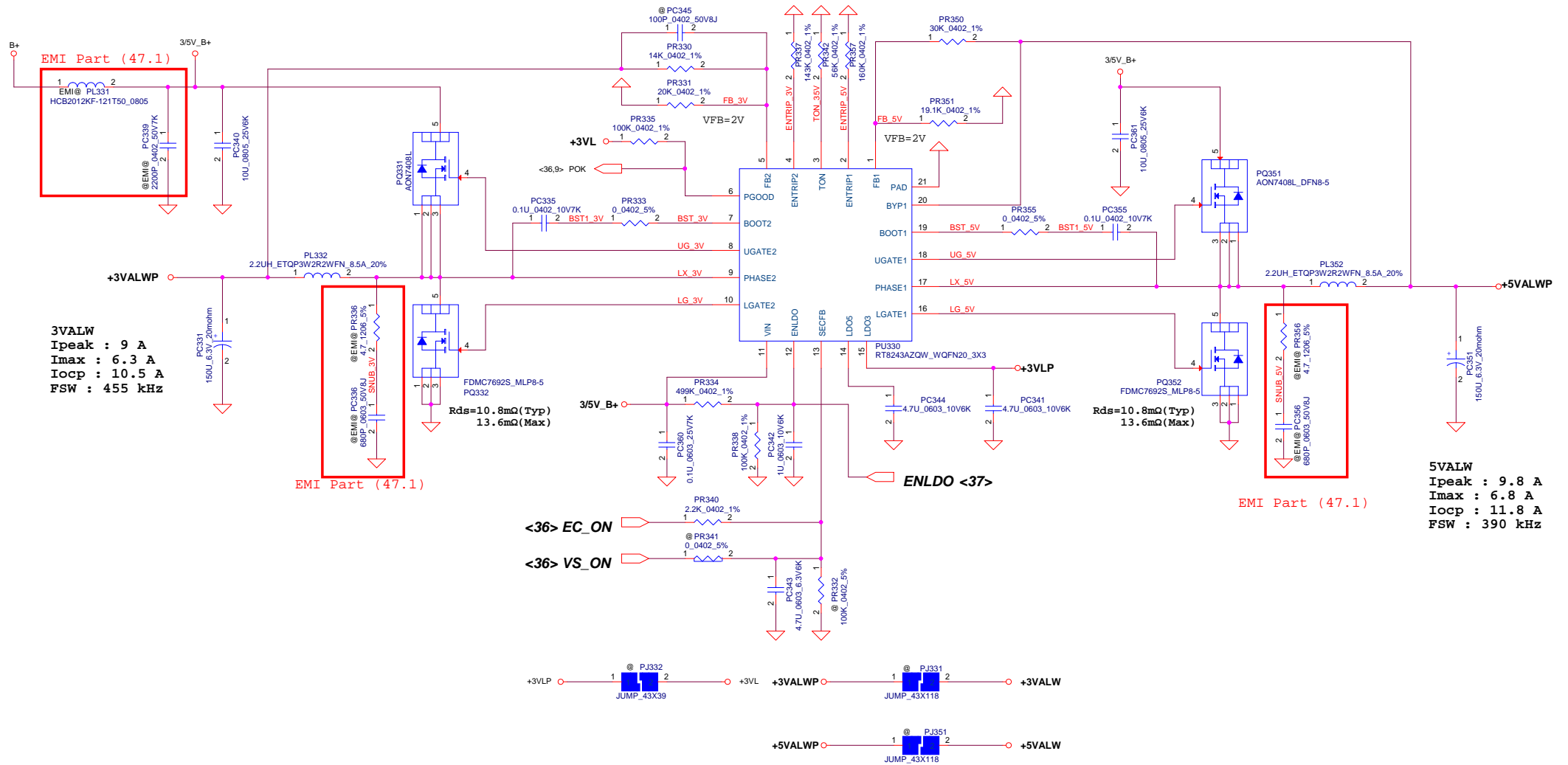
	Initial	Recovery
45W UMA	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C



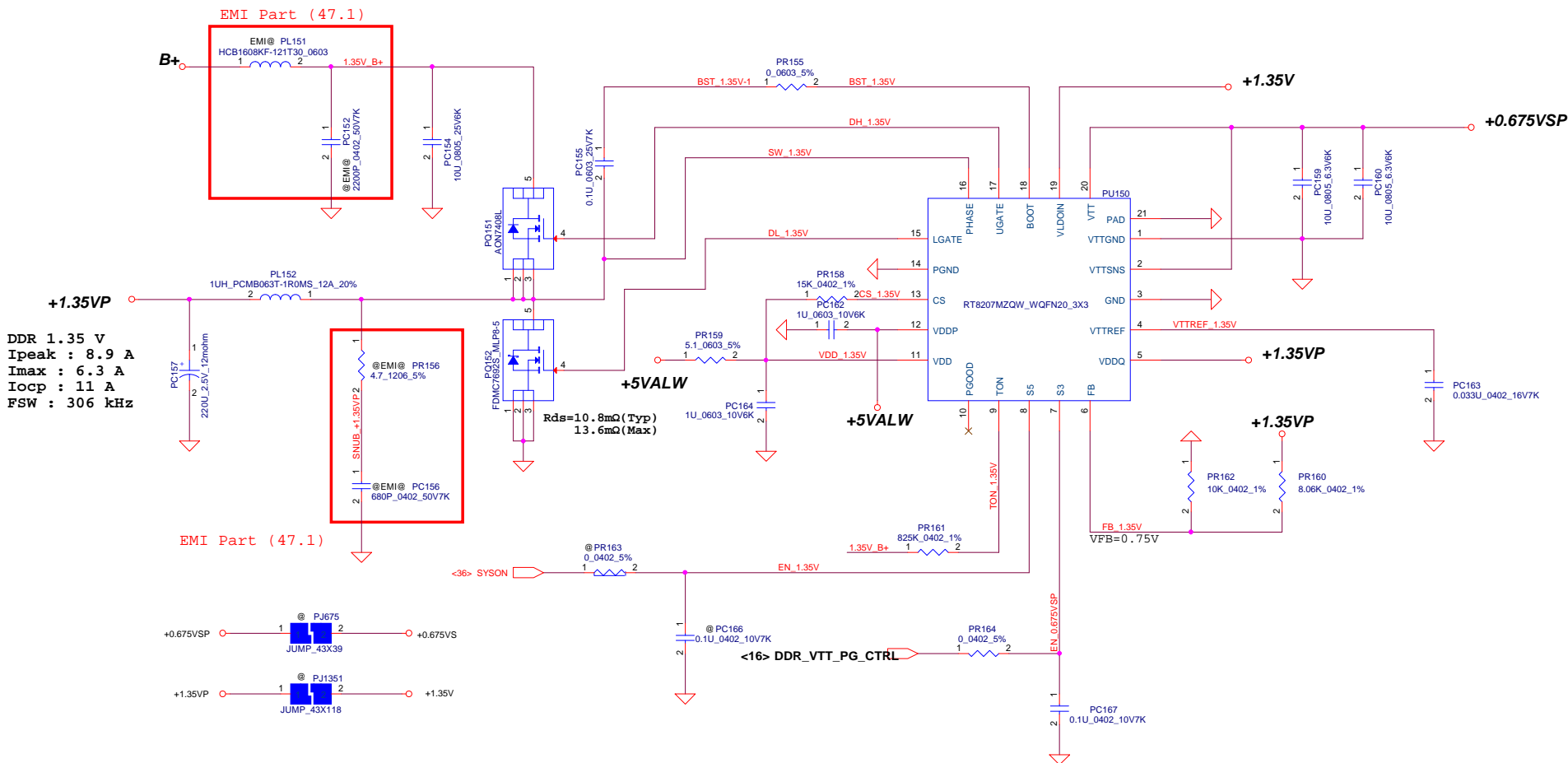
Charger controller (40.1), Support component (40.2)



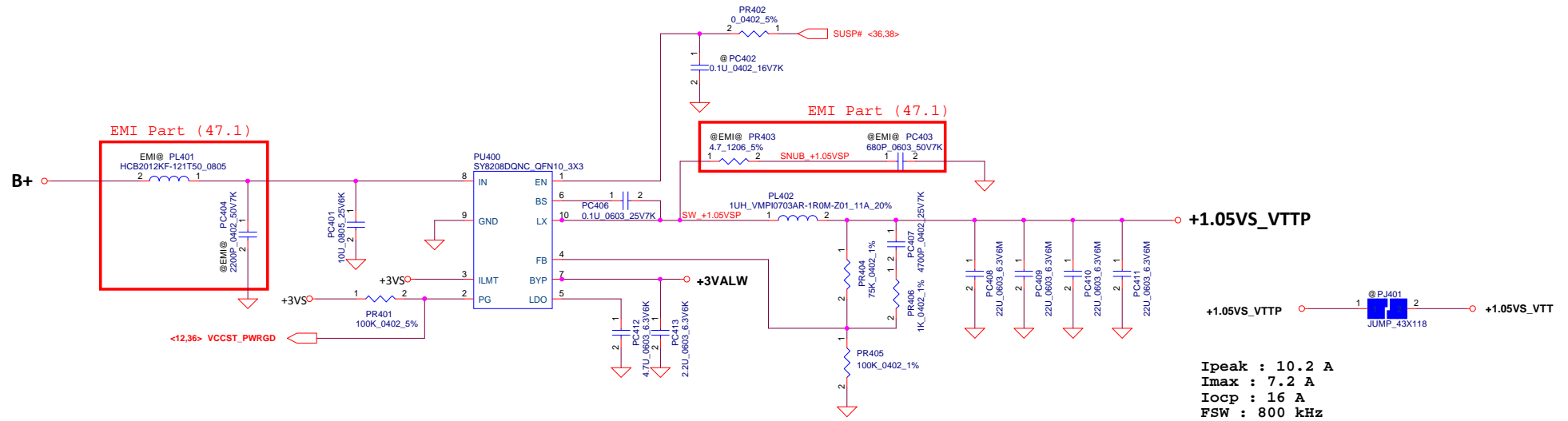


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		Deciphered Date		Title			
				3VALW/5VALW			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size		Rev	
				Document Number		0.1	
				ZRMMA			
Date:				Sheet		42 of 49	

# DDR controller (35.3), Support component (35.4)

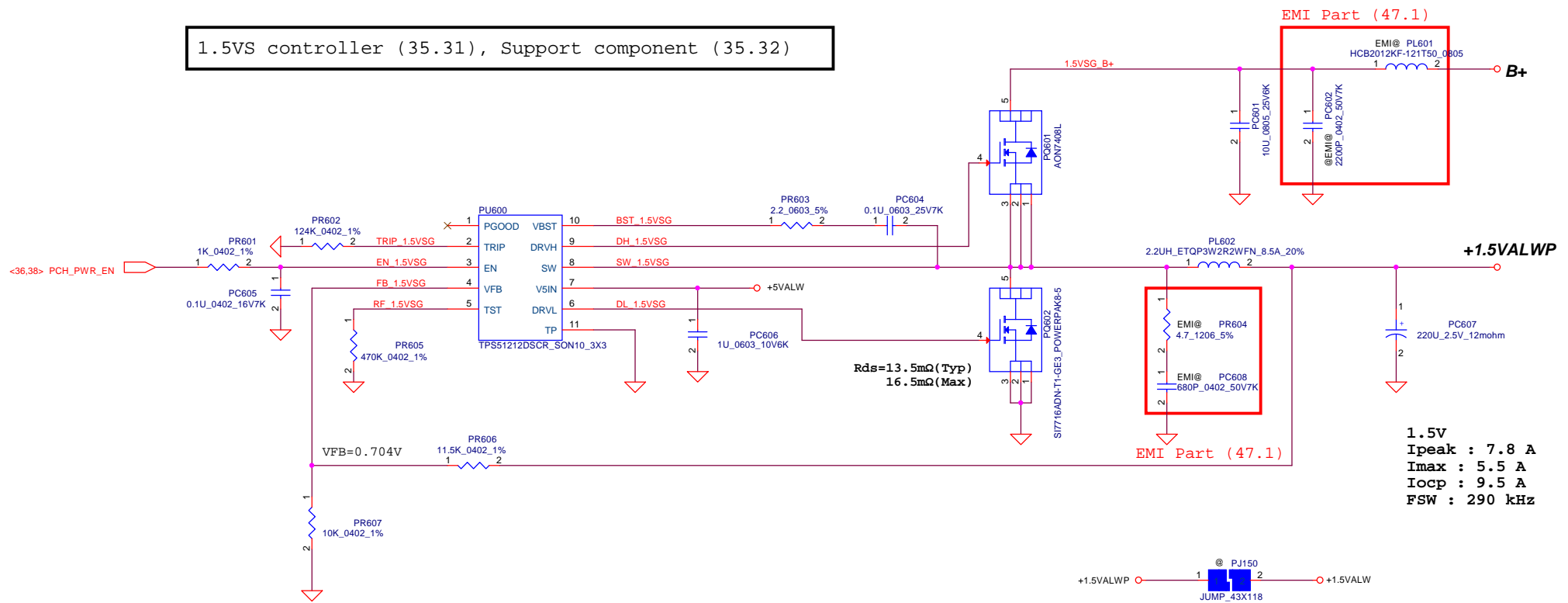


1.05VCCP controller (35.5), Support component (35.6)



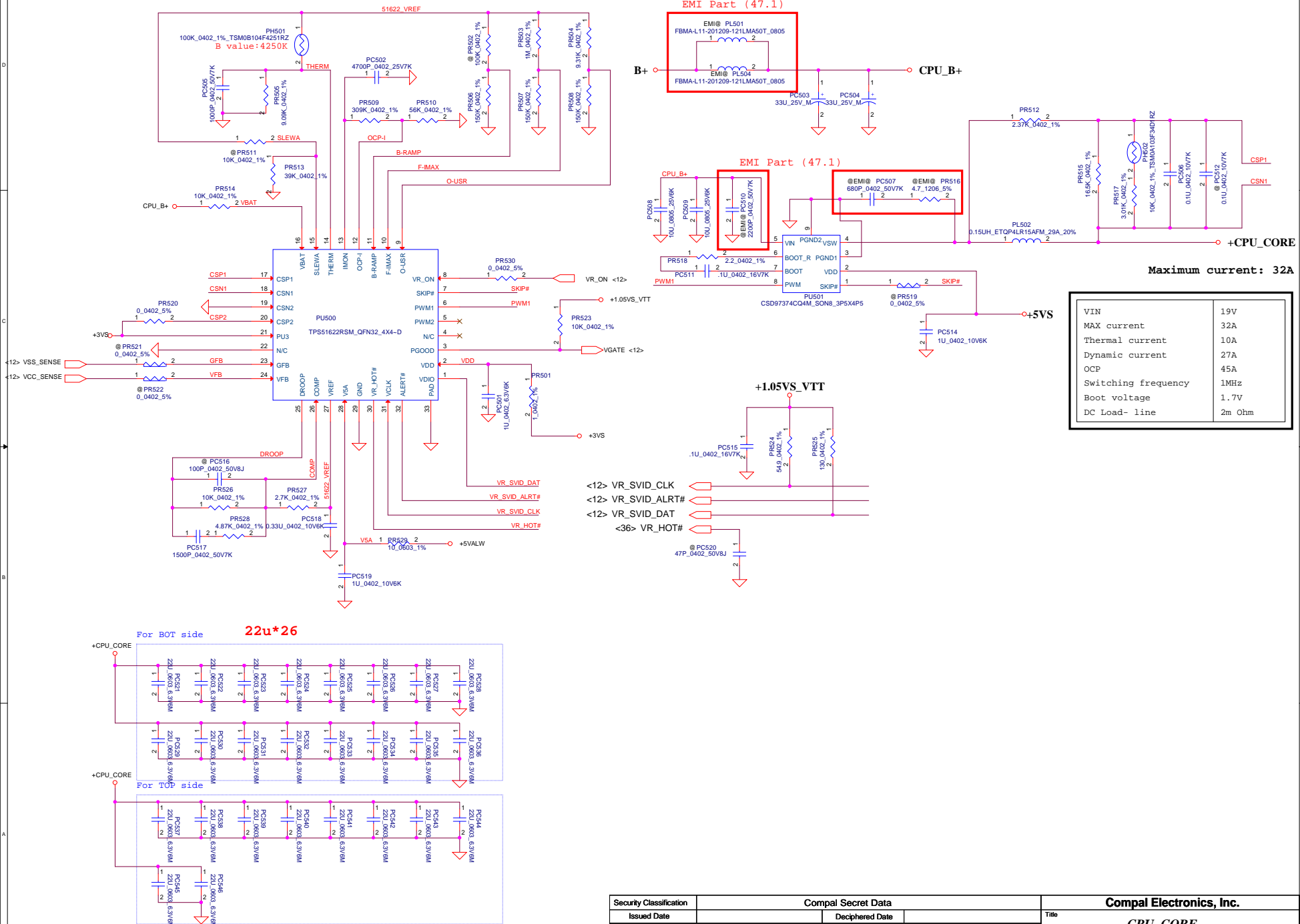
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Title			Document Number	Rev
+1.05VS_VCCP			ZRMAA	0.1
Date:		Sheet	44	of 49

1.5VS controller (35.31), Support component (35.32)



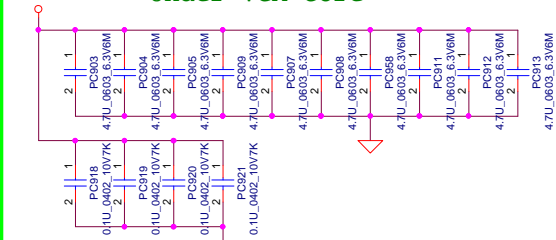
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date:	
				Sheet	45 of 49

+VCC\_CORE controller (36.1), Support component (36.3)  
driver(36.2), decoupling cap(36.4)

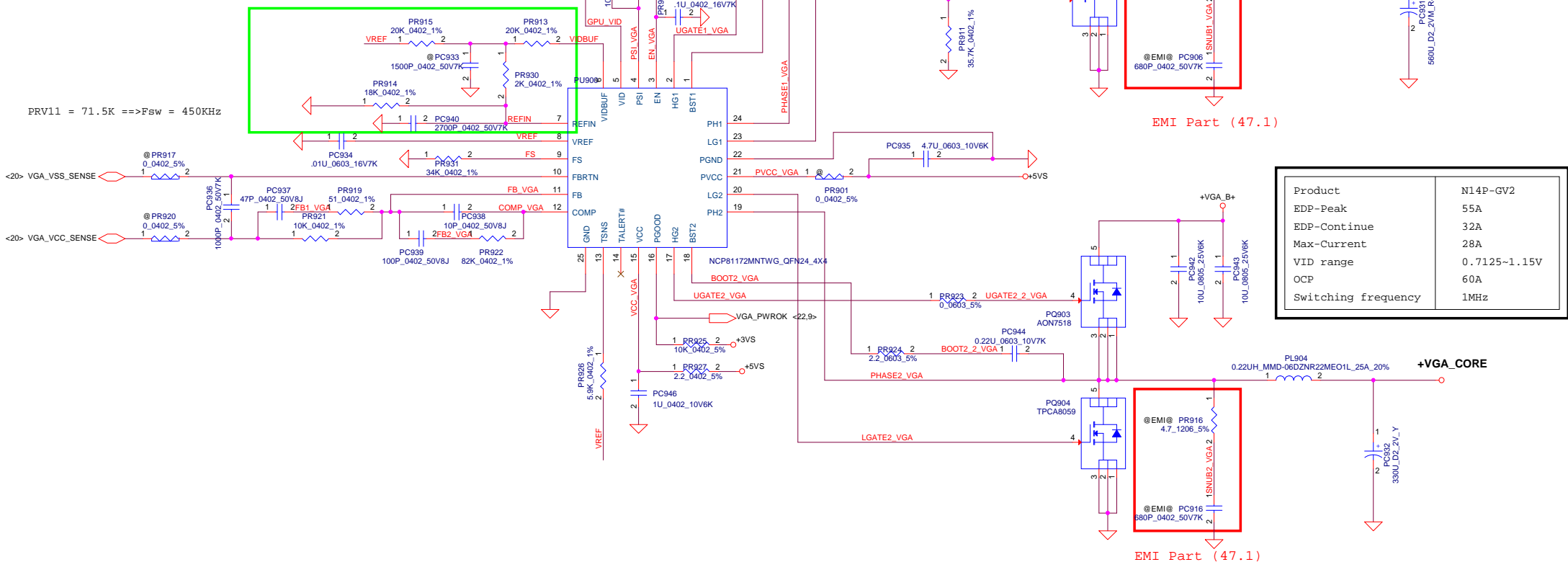


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	CPU CORE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number			Rev	0.1
	ZRMMA				
Date:				Sheet	46 of 49

## GB4-128 package



PRV11 = 71.5K ==>Fsw = 450KHz



Product	N14P-GV2
EDP-Peak	55A
EDP-Continue	32A
Max-Current	28A
VID range	0.7125~1.15V
OCP	60A
Switching frequency	1MHz

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		Deciphered Date		Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>VGA CORE</b>		
				Size	Document Number	Rev
				<b>ZRMAA</b>		
Date:				Sheet	47	of 49

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size	Document Number	Rev
			ZRMAA	0.1

# PW R PIR (Product Improve Record)

## VSKTA LA-9865P Schematic Change List

Item	Time (When)	Page (W Here)	Location / Discription ( How / W hat)	Request (W ho)	Reson (W hy)
1	EVT--2012/11/28		Add / PC101, PC103, PC102, PC104, PC7, PC8, PL151, PC181, PL2, PC3, PL101, PL102, PL331, PL401, PL601, PL501, PL901	EMI	EMI request
2	EVT--2012/11/28	P50-PWR-CPU_CORE	Value change / PR529, PR520, PR528, PR503, PR507, PR515, PR527, PR509, PR510, PR504, PC516, PL502, PC543, PC544, PC545, PC546, PC514, PC519	PW R	TPS51622 for 15W CPU setting
3	EVT--2012/11/28	P48-PWR-1.05VS_VCCP/1.8VSP	Value change / PR407, PR401, PR404, PR405, PC404, PC405	PW R	For TPS51362 design change
4	EVT--2012/11/28	P46-PWR-1.35VP/0.675VSP	Short pad reserve / PR163	PW R	
5	EVT--2012/11/28	P47-PWR-3VALW /5VALW	PC351 reserve / PC352 mount	PW R	ME limitation
6	EVT--2012/11/28	P50-PWR-CPU_CORE	PC504 reserve	PW R	ME limitation
7	EVT--2012/11/28	P44-PWR-BATTERY CONN / OTP	PF2 change vendor	PW R	for cost down plan
8	EVT--2012/11/29	P46-PWR-1.35VP/0.675VSP	change material / PL152	PW R	For design change
9	DVT-2012/12/13	P43-PWR-DCIN	modify PBJ101 footprint	PW R	for comm footprint
10	DVT-2012/12/13	P44-PWR-BATTERY CONN / OTP	modify PR20, PR21 pin define	PW R	for layout module request
11	DVT-2012/12/13	P46-PWR-1.35VP/0.675VSP	change PR160 to 8.06K	PW R	for output voltage level
12	DVT-2012/12/13	P46-PWR-1.35VP/0.675VSP	modify PL152, PC155, PR164 pin define	PW R	for layout module request
13	DVT-2012/12/13	P47-PWR-3VALW /5VALW	del PC331, PC351	PW R	ME limitation
14	DVT-2012/12/13	P47-PWR-3VALW /5VALW	modify PL332, PR337, PR342, PR357 pin define	PW R	for layout module request
15	DVT-2012/12/13	P47-PWR-3VALW /5VALW	modify the VS_ON direction	PW R	input signal
16	DVT-2012/12/13	P48-PWR-1.05VS_VCCP/1.8VSP	change the 1.8VSP EN to 6511_PWR_EN	PW R	for High enable
17	DVT-2012/12/13	P48-PWR-1.05VS_VCCP/1.8VSP	modify PR401, PC402, PR182 pin define	PW R	for layout module request
18	DVT-2012/12/13	P49-PWR-1.5VALW P	change PR603 to 0ohm	PW R	VBST resistor
19	DVT-2012/12/13	P49-PWR-1.5VALW P	modify PR602, PR606, PL601 pin define	PW R	for layout module request
20	DVT-2012/12/13	P50-PWR-CPU_CORE	change the B+ EMI bead	PW R	ME limitation
21	DVT-2012/12/13	P50-PWR-CPU_CORE	modify PC516, PR526, PR527, PC517, PR529, PR512, PR516, PR518, PR534, PR536, PR530, PR524 pin define	PW R	for layout module request
22	DVT-2012/12/13	P51-PWR-VGA_CORE	PR912/add 10K ohm	PW R	pull high +3VS_DGPU
23	DVT-2012/12/13	P51-PWR-VGA_CORE	PC934 change to 0.01u	PW R	VREF pull down cap
24	DVT-2012/12/13	P51-PWR-VGA_CORE	modify PL901, PR908, PR907, PR901, PR923, PR924, PR927, PC946, PR913, PR915, PR914, PR904, PR928, PR931, PR932, PR909 pin define	PW R	for layout module request
25	PVT-2013/01/25	P47-PWR-3VALW /5VALW	change PC332, PC352, PR409 location to PC331, PC351, PR335	PW R	common change
26	PVT-2013/01/25	P46-PWR-1.35VP/0.675VSP	change PL152 value from 1uH to 0.68uH	PW R	for design change
27	PVT-2013/01/25	P46-PWR-1.35VP/0.675VSP	change PC157 to 390uF 5*5.7	PW R	layout request
28	PVT-2013/01/25	P51-PWR-VGA_CORE	change PC934 part number	PW R	common change
29	PVT-2013/02/04	P50-PWR-CPU_CORE	PC529, 531, 533, 534, 535, 537 reserve PC505 0.1uF change to 10nF PR527 4.99k change to 2.7k PR509 374k change to 309k PC506 0.15u change to 0.1u PR510 39k change to 56k	PW R	for TPS51622 date code 2BI design change
30	PVT-2013/02/04	P51-PWR-VGA_CORE	PC947 330u reserve	PW R	for cost down plan
31	PVT-2013/02/04	P51-PWR-VGA_CORE	PL903, 904 change PN	PW R	common change
32	PVT-2013/02/04	P49-PWR-1.5VALW P	net name change from 1.5VALW_EN to PCH_PWR_EN	HW	for common design change
33	PVT-2013/02/07	P49-PWR-1.5VALW P	PR604 PC608 mount PR603 change from 0ohm to 2.2ohm	EMI	EMI request
34	PVT-2013/02/07	P49-PWR-1.5VALW P	PL602 change from 4.7u to 2.2u	PW R	For design change
35	PVT-2013/02/07	P48-PWR-1.05VS_VCCP/1.8VSP	PL402 change PN from RX00 (H1.8) to 5K80 (H3.0)	PW R	change Material for useful height

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
				PIR (PWR)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size	Document Number	Rev	
			ZRMAA	0.1	
Date: Sunday, April 07, 2013		Sheet 48 of 49			



# HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2013/xx/xx

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	03/04	36	Add EC_SMB_CK3、EC_SMB_DA3、RB135、RB136	Vendor request for LVDS Translator
2	03/04	27	Add EC_SMB_CK3、EC_SMB_DA3	Vendor request for LVDS Translator
3	03/04	31	Change JWLAN connector	For WLAN
4	03/04	31	Change JHDMI connector	For HDMI
5	03/04b	30	Change JHDD pin define	For HDD
6	03/04b	33	Delete DEVSLP0	For HDD
7	03/04b	37	ADD R5、D6、R7、D7	For Power LED
8	03/05A	07	Change FAN connector	For FAN
9	03/05A	16、17	Change DDR net order	For DDR
10	03/05A	33	Change JHP connector	For Small board
11	03/05B	19	Change RV4、RV5、RV6、RV7、RV8、RV9	For Layout placement
12	03/06A	19	Delete RV108、RV109、RV110、RV111、RV104、RV105、RV106、RV107	For Layout placement
13	03/06A	19	ADD RPV8、RPV9	For Layout placement
14	03/06A	06	Update DDR pin for DDR interleave routing	For DDR
15	03/06B	33	Change JHP to JSB4 and Add JSB5	For Small board
16	03/06B	33	ADD R44、R45、R46、R47	For Small board
17	03/06B	33	Change JKB to JKB4、ADD JKB5	For Keyboard
18	03/07A	16、17	Change JDDR3S、JDDR3R	For DDR
19	03/11A	33	Change JNGFF connector	For NGFF SSD
20	03/11A	34	Change JUSBR、JUSEF connector	For NGFF SSD
21	03/11A	37	Modify Hole	For Dummy
22	03/11B	35	ADD RA5、Q5539B for Combo Jack Normal Close	For Audio
23	03/11B	07	Change JSPK	For Speaker
24	03/12A	30	Swap JHDD pin define	For HDD
25	03/12A	29	Swap L64、L65、L66、L67	For HDMI
26	03/12A	37	Change D6、D7 material and Add D8、R19	For 14" 15" LED
27	03/12A	37	Add SW3 for 14"	For Power Button
28	03/12B	37	Add H18、H19 Delete H7、H14、H15	For Hole
29	03/12C	37	Change CCL2 and RCL5 @ to GCLK@	For Green clock
30	03/12C	37	Delete E51_TXD(RB27)、E51_RXD	For WLAN
31	03/12D	31	Change JWLAN to NGFF E type	For WLAN
32	03/13A	37	ADD KSO17、KSO16 for 15" keyboard	For keyboard
33	03/13A	36	Change TRANS_SEL to pin75、CHG_PWR_GATE# to pin89	For keyboard
34	03/13A	36	ADD KSO17、KSO16 for 15" keyboard	For keyboard
35	03/13A	36	Delete BT_ON Pin34	For WLAN
36	03/13A	17、6	Change DDR to no interleave routing	For DDR
37	03/13B	36	Change LAN_WAKE# from UB1.108 to UB1.71	For EC
38	03/13B	36	Change WAKE# to EC_SWI# and connect to UB1.108	For EC
39	03/13B	34	Swap L60、L56、L71、L72	For DDR3
40	03/13B	37	Delete Q196	For WLAN LED
41	03/13B	35	Delete CA54、CA56	For Audio
42	03/13B	35	Swap JSPK	For Audio
43	03/14A	34	Swap LR7、LR8	For USB
44	03/14A	16、17	Swap JDDR3R、JDDR3S	For DDR
45	03/14B	33	Swap R44、R45、R46、R47	For Small board
46	03/14B	36	ADD JDB for EC debug	For Debug
47	03/14B	18	Change XTAL_OUTBUFF、XTAL_SSIN to RPV1.3、RPV1.4	For VGA
50	03/14B	18	Change SMB_CLK_GPU、SMB_DATA_GPU to RPV2.3、RPV2.4	For VGA
51	03/14B	16、17	JDDR3R、JDDR3S to JDDR3H、JDDR3L	For DDR
52	03/14B	31、36	ADD BT_ON	For WLAN
53	03/14B	36	EC_SMB_CK3、EC_SMB_DA3 change use 2.2K	For LVDS SM Bus
54	03/14B	10	Delete R307、R220	For Audio sleep & music
55	03/15A	5、10、37	Change CH7,D98,D99 BOM config from @ESD@ to ESD@ for ESD's request.	

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HW-PIR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev	0.1
				Date	Sunday, April 07, 2013	Sheet 49 of 49

[www.s-manuals.com](http://www.s-manuals.com)