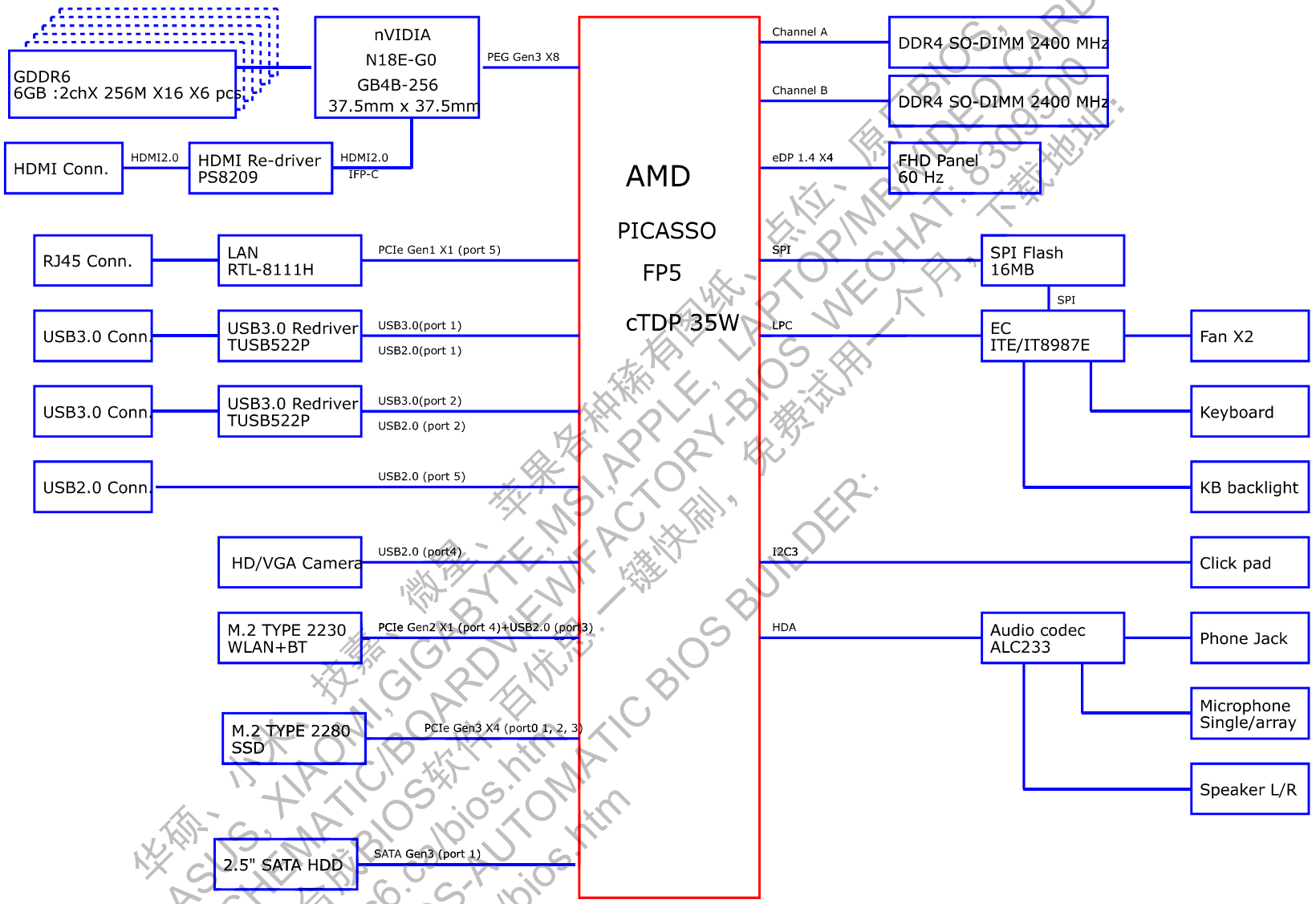
FX505DU Block Diagram



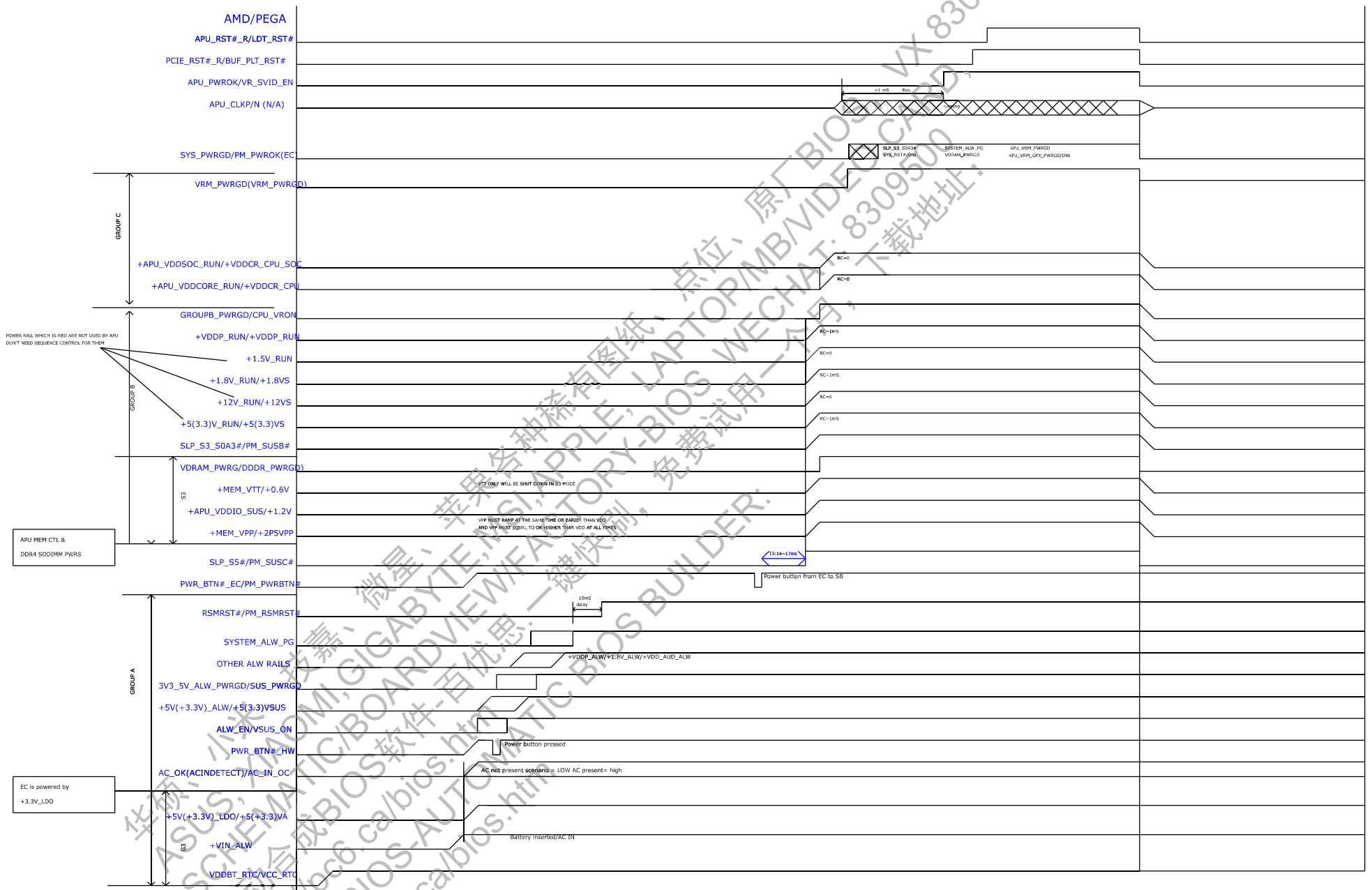
Power

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

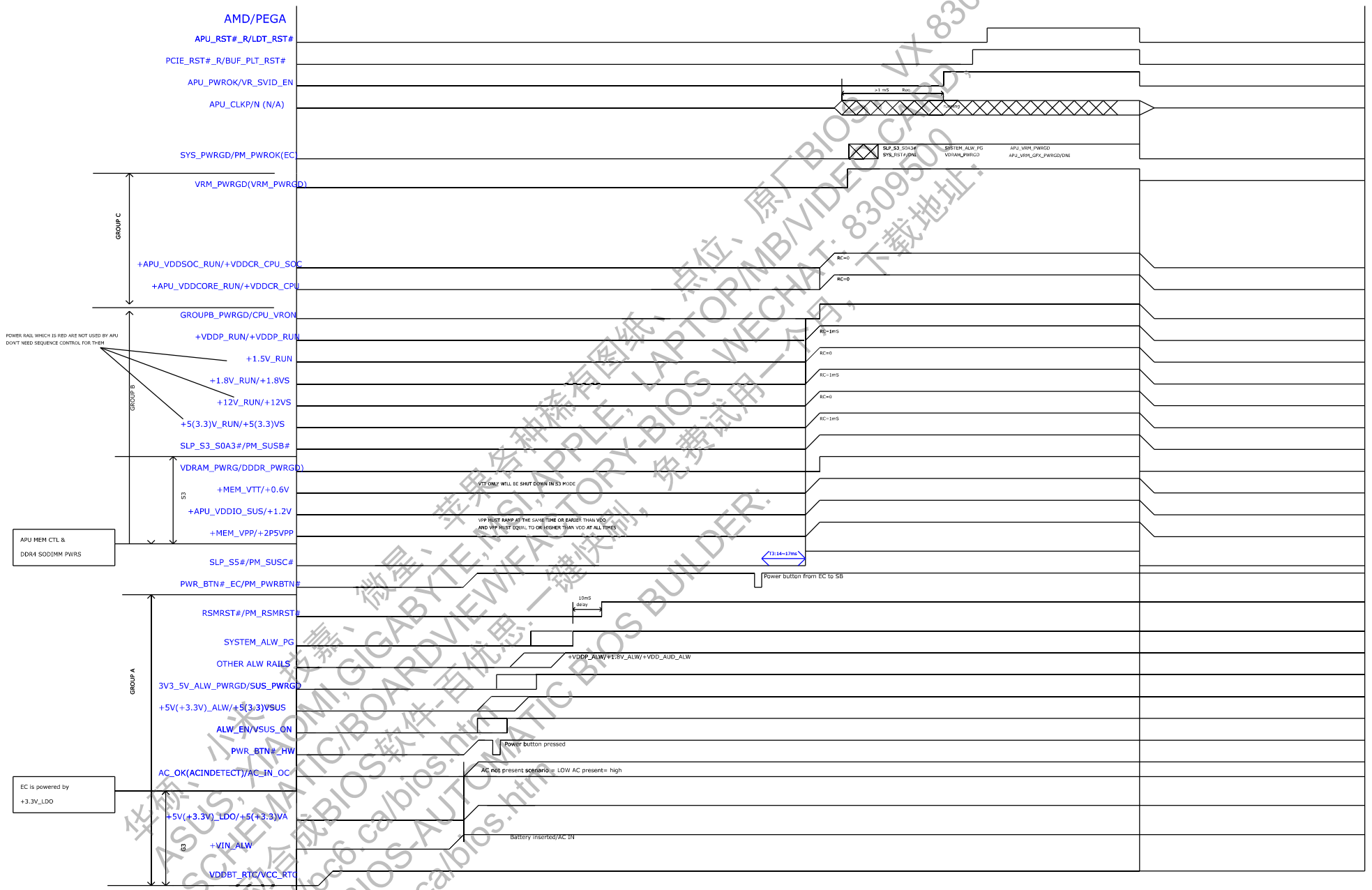
Title : Block Diagram
Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.1

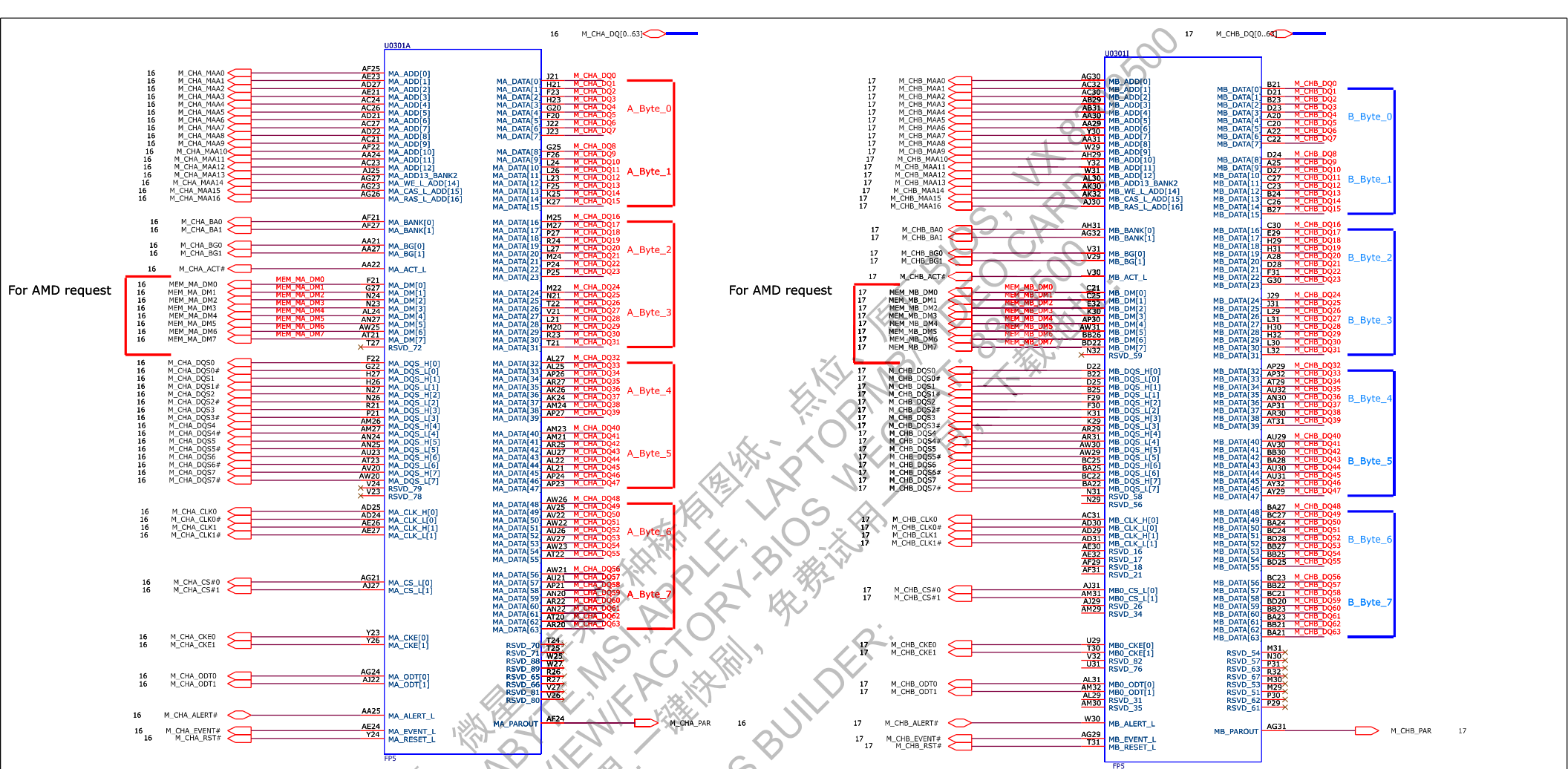
Date: Tuesday, March 12, 2019 Sheet 1 of 99



PEGATRON Title : Option
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD Engineer: Johnson Huang
Size C | Project Name FX505DU | Rev 1.1
Date: Tuesday, March 12, 2019 Sheet 2 of 72



PEGATRON Title : Option
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD Engineer: Johnson Huang
Size C | Project Name FX505DU | Rev 1.1
Date: Tuesday, March 12, 2019 Sheet 2 of 72



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

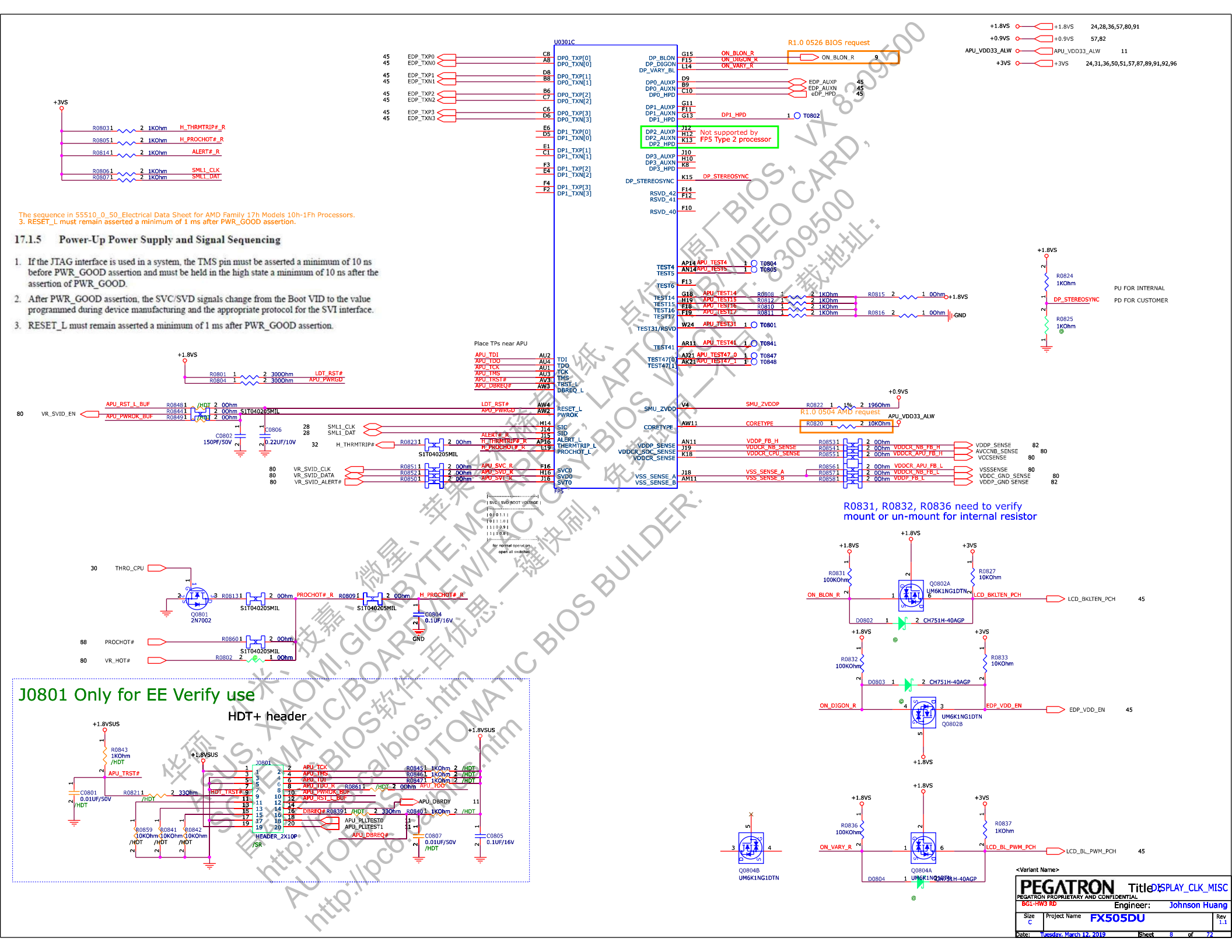
Title: MEM & PCIE I_F

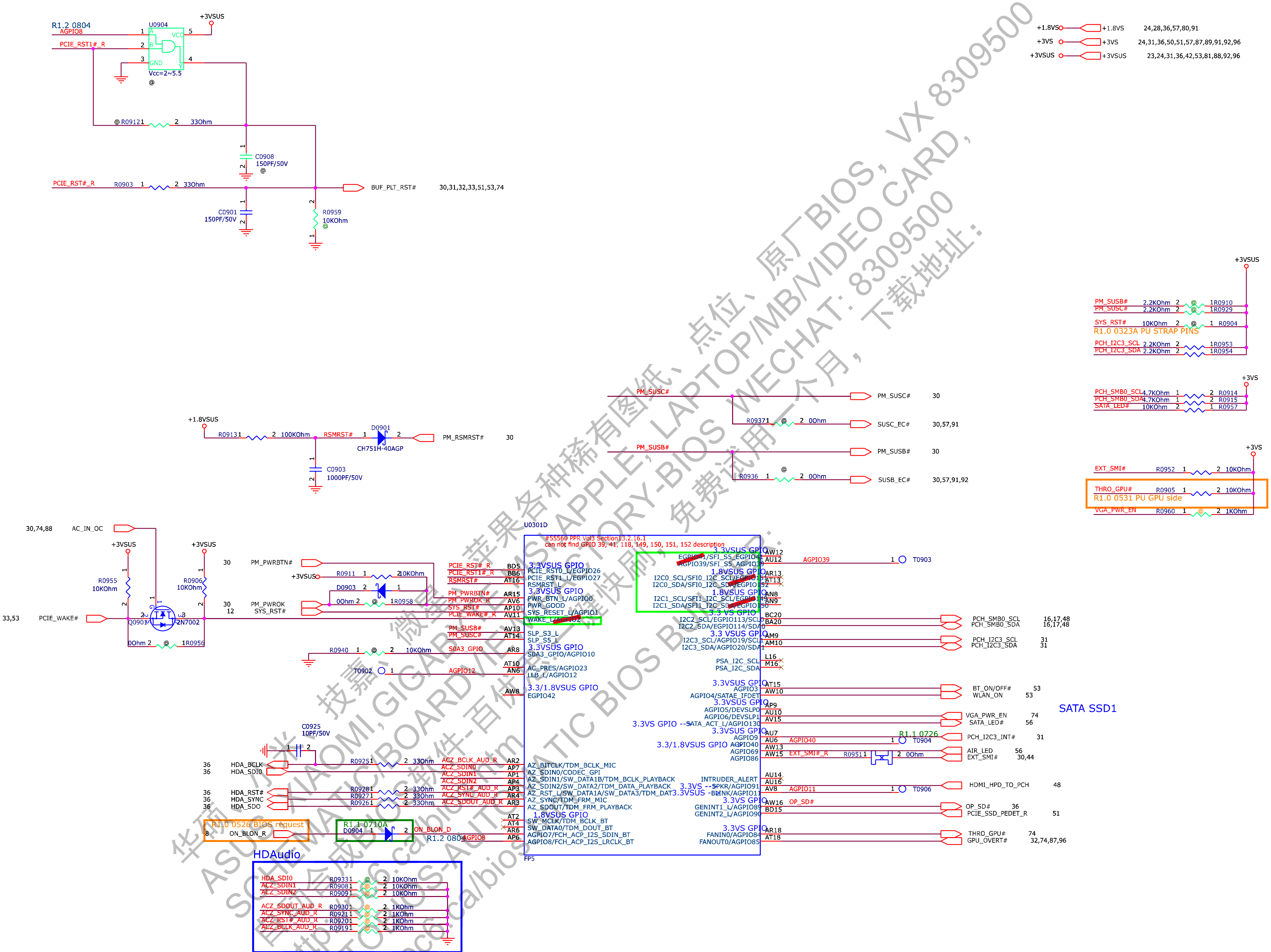
BG1-HW3 RD

Engineer:

Size	Project Name	Rev
C		1.1

Date: Tuesday, March 12, 2019 | Sheet 7 of 72


The sequence in 55510_0_50_Electrical Data Sheet for AMD Family 17h Models 10h-1Fh Processors.
3. RESET_L must remain asserted a minimum of 1 ms after PWR_GOOD assertion.
17.1.5 Power-Up Power Supply and Signal Sequencing
1. If the JTAG interface is used in a system, the TMS pin must be asserted a minimum of 10 ns before PWR_GOOD assertion and must be held in the high state a minimum of 10 ns after the assertion of PWR_GOOD.
2. After PWR_GOOD assertion, the SVC/SVD signals change from the Boot VID to the value programmed during device manufacturing and the appropriate protocol for the SVI interface.
3. RESET_L must remain asserted a minimum of 1 ms after PWR_GOOD assertion.
R1.0 0526 BIOS request
Not supported by FP5 Type 2 processor
Place TPs near APU
R1.0 0504 AMD request
R0831, R0832, R0836 need to verify mount or un-mount for internal resistor
J0801 Only for EE Verify use
HDT+ header
PU FOR INTERNAL
PD FOR CUSTOMER
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: DISPLAY_CLK_MISC
BG1-HW3 RD
Engineer: Johnson Huang
Size C
Project Name FX505DU
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 8 of 72



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: GEVENT_GPIO_SD_AZ

BG1-HW3 RD

Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.1

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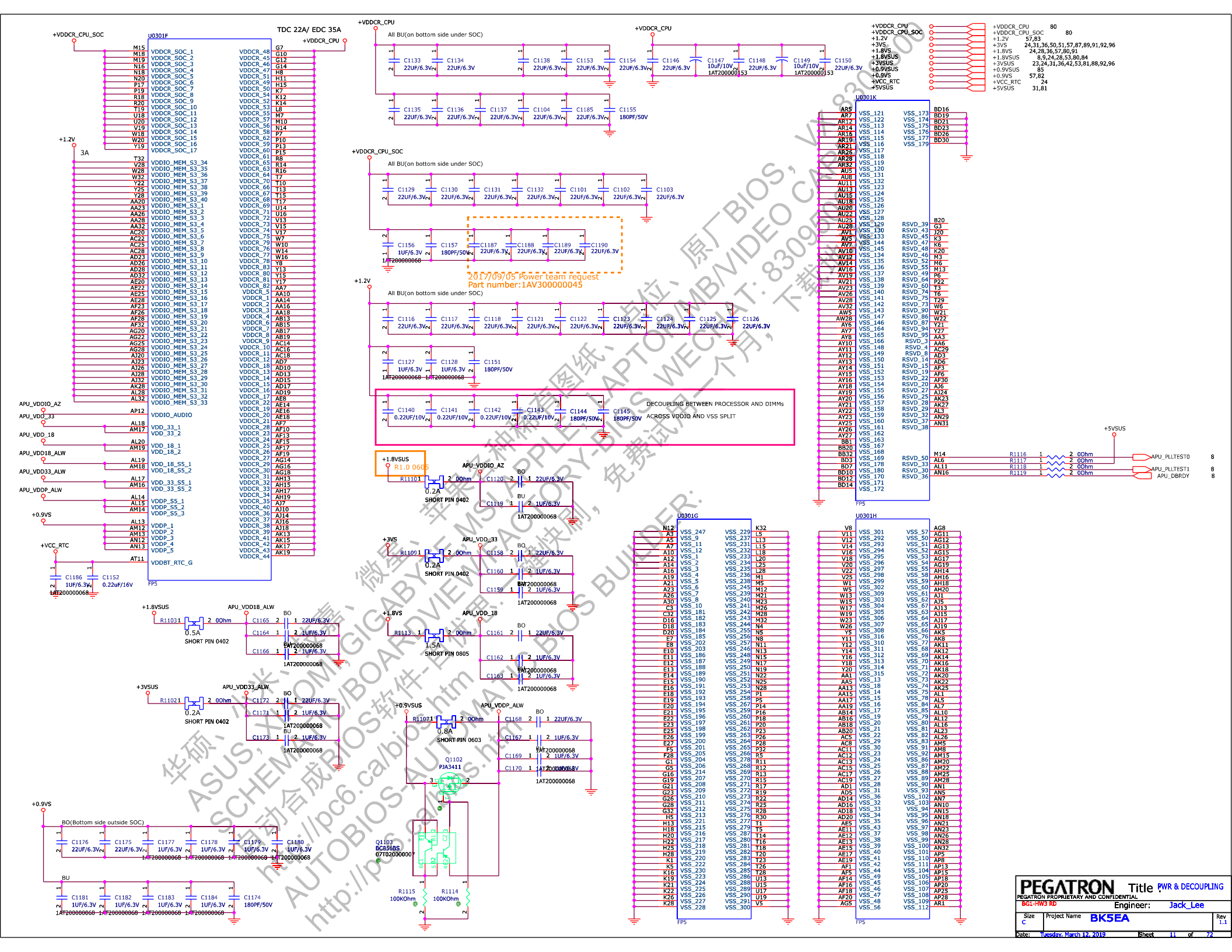
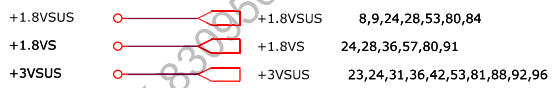
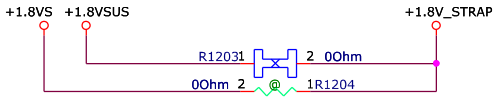
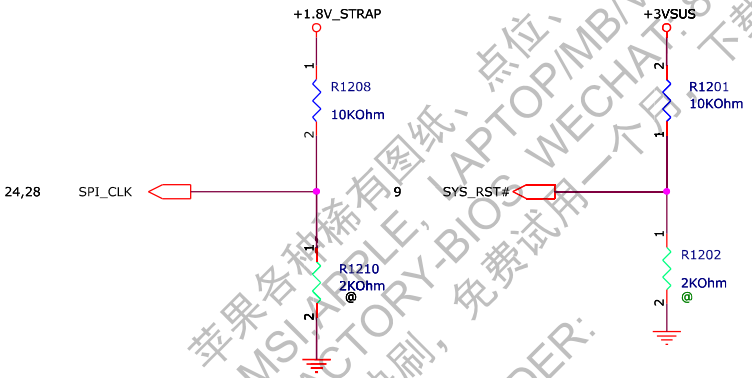

TDC 22A/ EDC 35A
U0301F
U0301K
U0301G
U0301H
+VDDCR_CPU_SOC
+VDDCR_CPU
+1.2V
3A
+3VSUS
+1.8VSUS
+0.9VSUS
+VCC_RTC
+5VSUS
APU_VDDIO_AZ
APU_VDD_33
APU_VDD_18
APU_VDD18_ALW
APU_VDD33_ALW
APU_VDDP_ALW
All BU(on bottom side under SOC)
BO(Bottom side outside SOC)
BU
DECOUPLING BETWEEN PROCESSOR AND DIMMs
ACROSS VDDIO AND VSS SPLIT
2017/09/05 Power team request
Part number:1AV300000045
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PWR & DECOUPLING
Engineer: Jack_Lee
BG1-HW3 RD
Project Name BK5EA
Size C
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 11 of 72





STRAP PINS



STRAP	FUNCTION	DEFINITION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : STRAPS, SOCKET, HS

BG1-HW3 RD

Engineer: Johnson Huang

Size	Project Name	Rev
B	FX505DU	1.1

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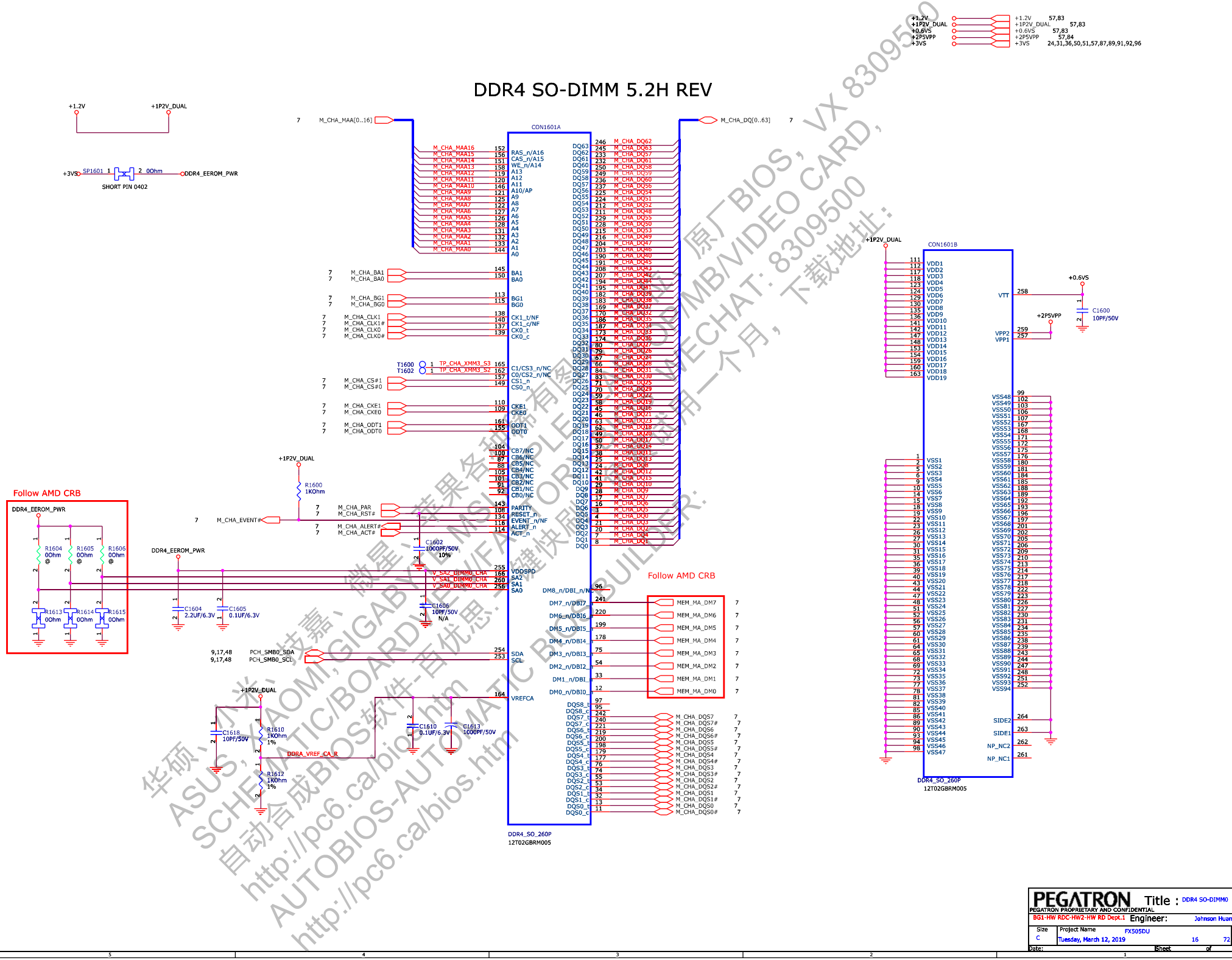
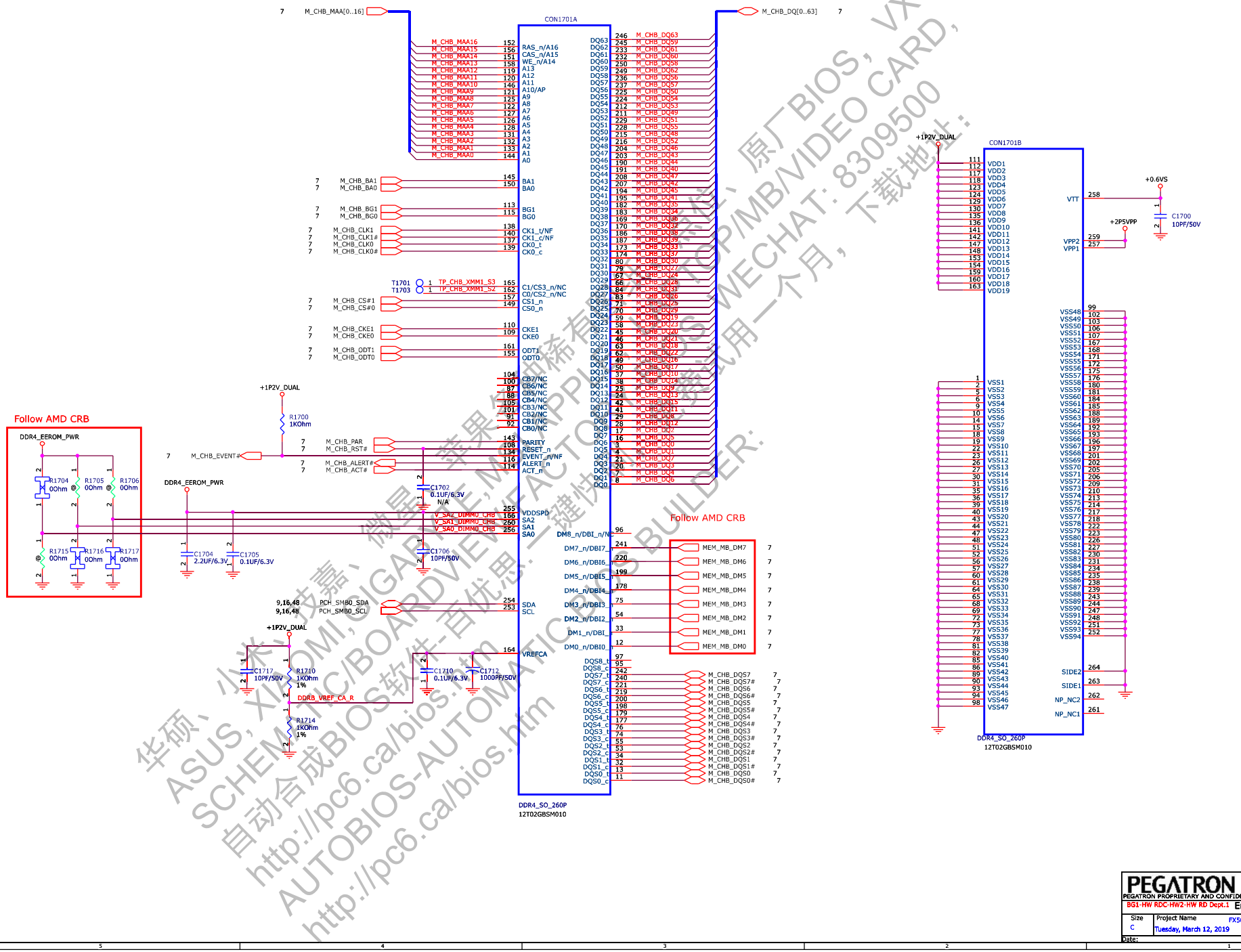
DDR4 SO-DIMM 5.2H REV

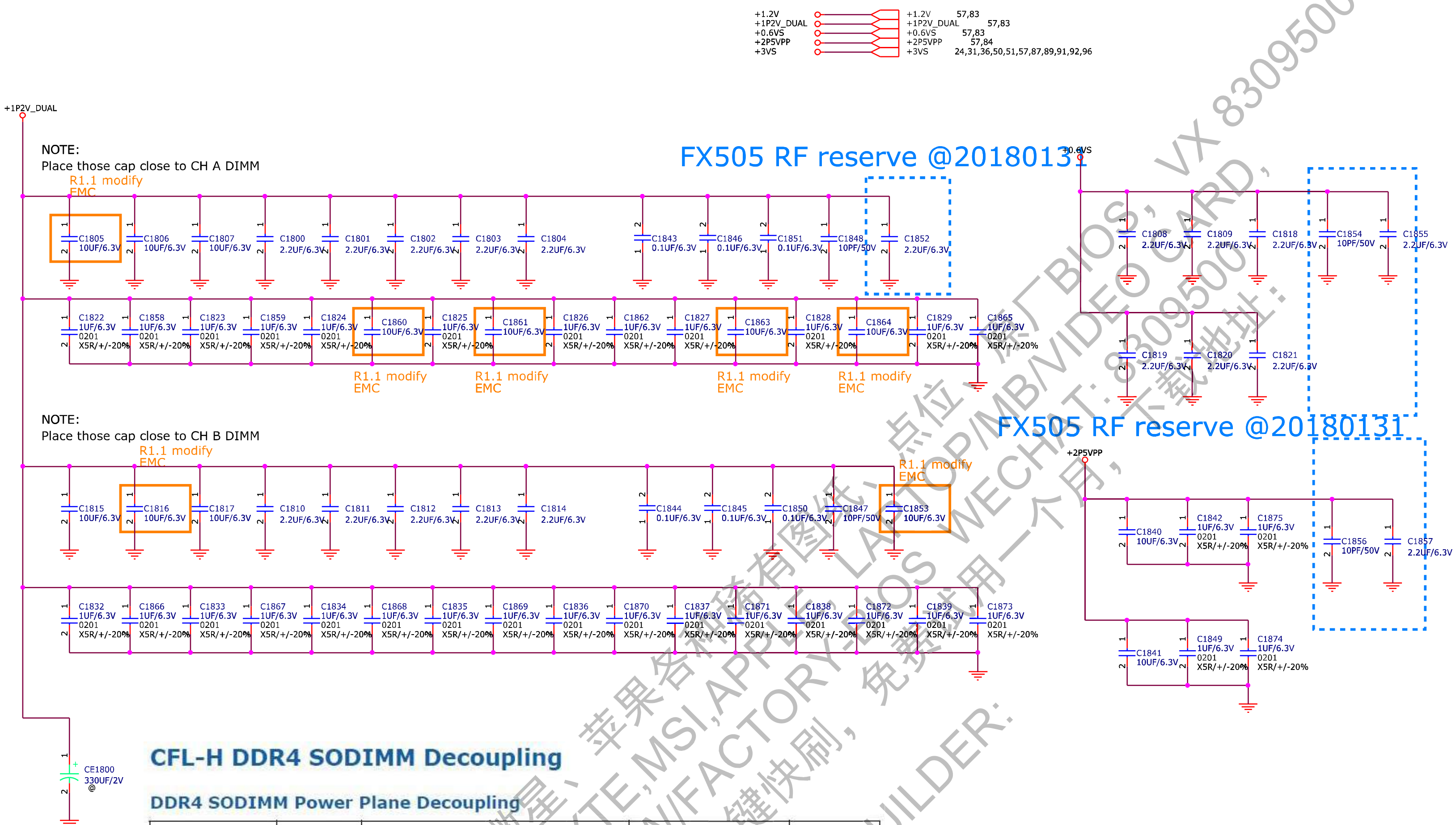


PEGATRON	Title : DDR4 SO-DIMM0		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: Johnson Huang		
Size: C	Project Name: FX505DU		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet 16 of 72		

DDR4 SO-DIMM 5.2H STD



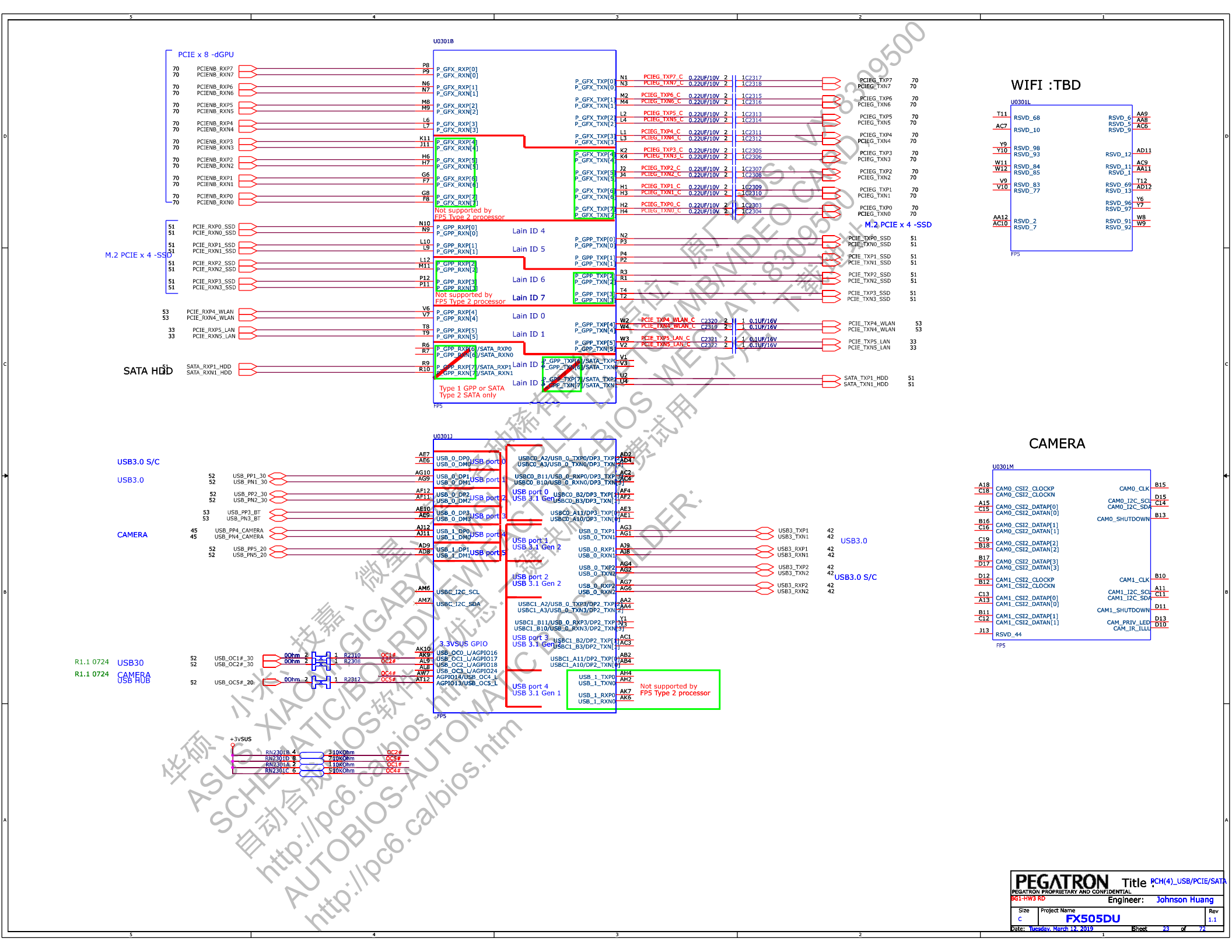
PEGATRON Title : DDR4 SO-DIMM1
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size C | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 17 of 72

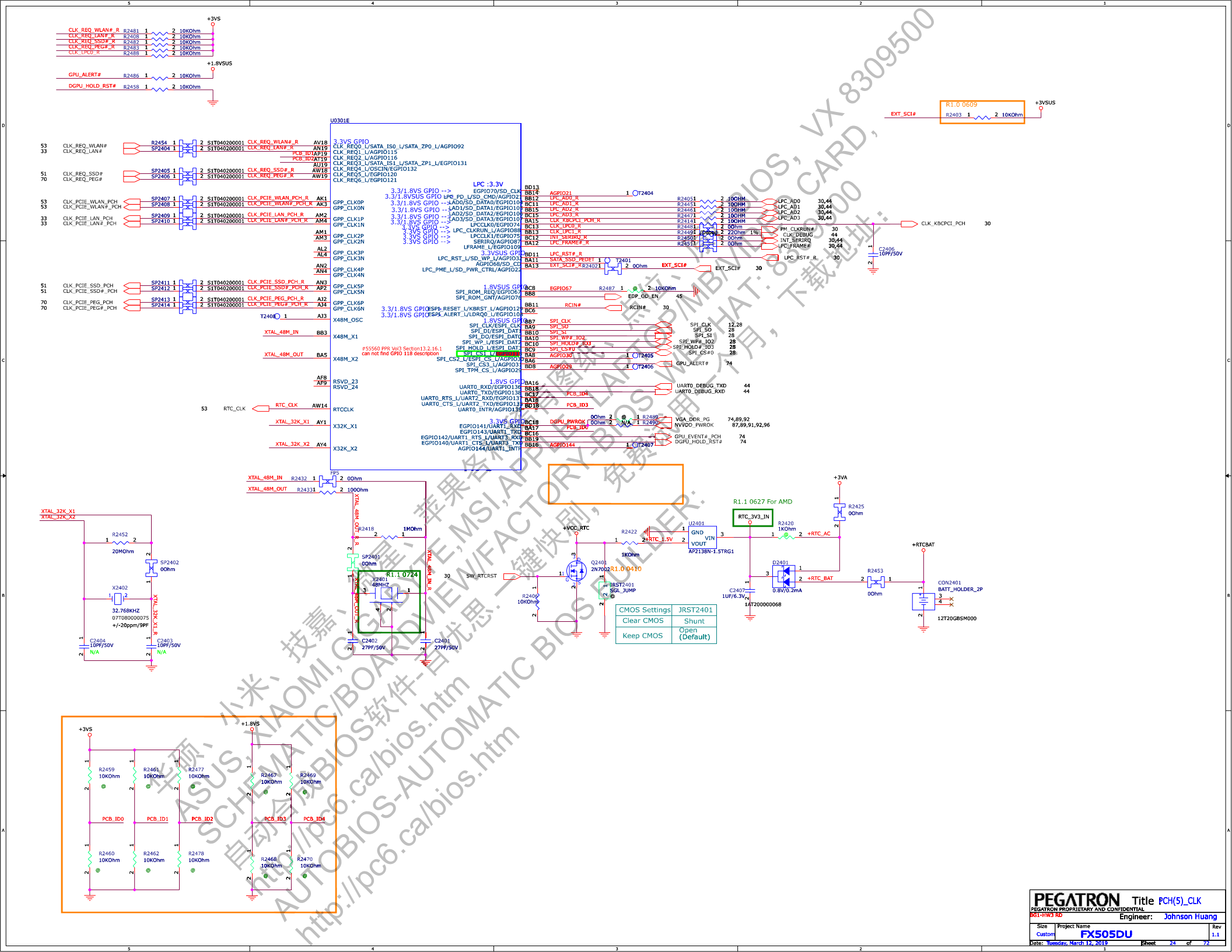


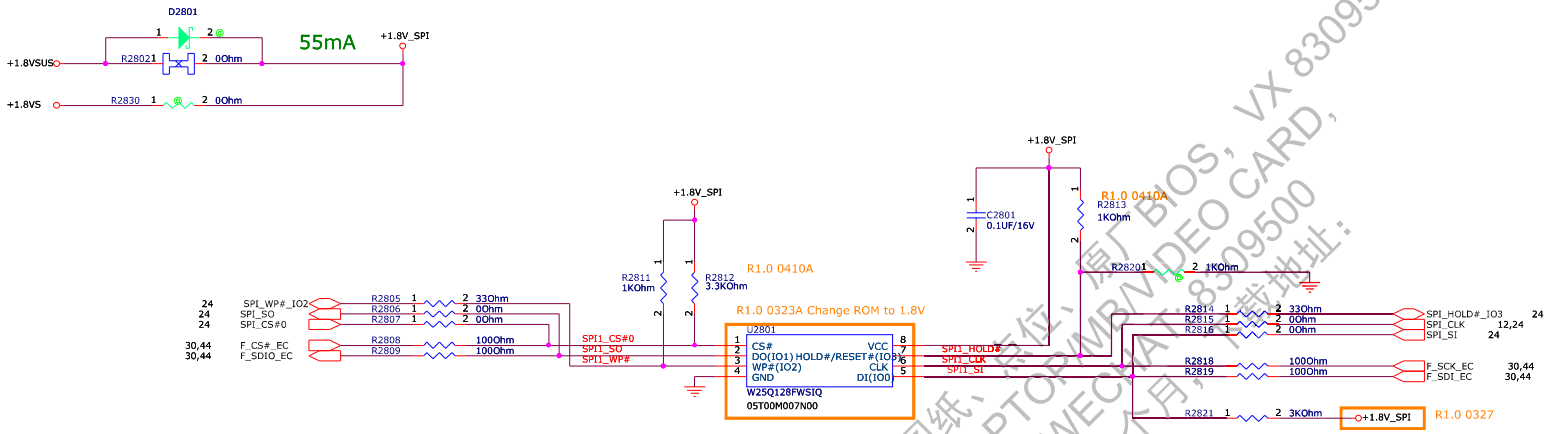
CFL-H DDR4 SODIMM Decoupling

DDR4 SODIMM Power Plane Decoupling

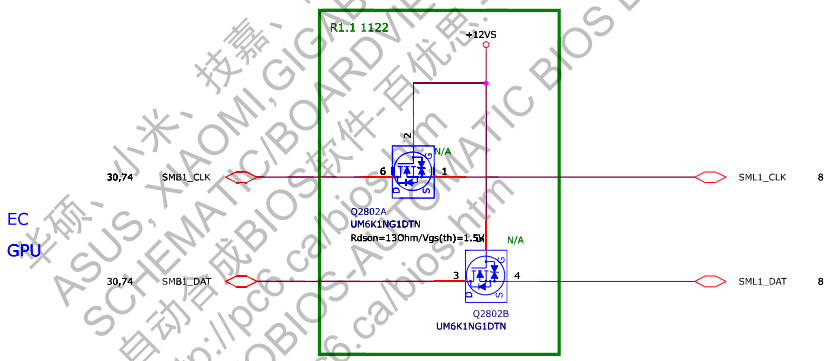
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	


PCIE x 8 -dGPU
M.2 PCIE x 4 -SSD
SATA HDD
WIFI :TBD
M.2 PCIE x 4 -SSD
CAMERA
USB3.0 S/C
USB3.0
CAMERA
USB30
CAMERA
USB HUB
R1.1 0724
R1.1 0724
Not supported by FP5 Type 2 processor
Type 1 GPP or SATA
Type 2 SATA only
Not supported by FP5 Type 2 processor
3.3VSUS GPIO
+3VSUS
PEGATRON
Title : PCH(4)_USB/PCIE/SATA
PEGATRON PROPRIETARY AND CONFIDENTIAL
SG1-HW3 RD
Engineer: Johnson Huang
Size C
Project Name FX505DU
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 23 of 72

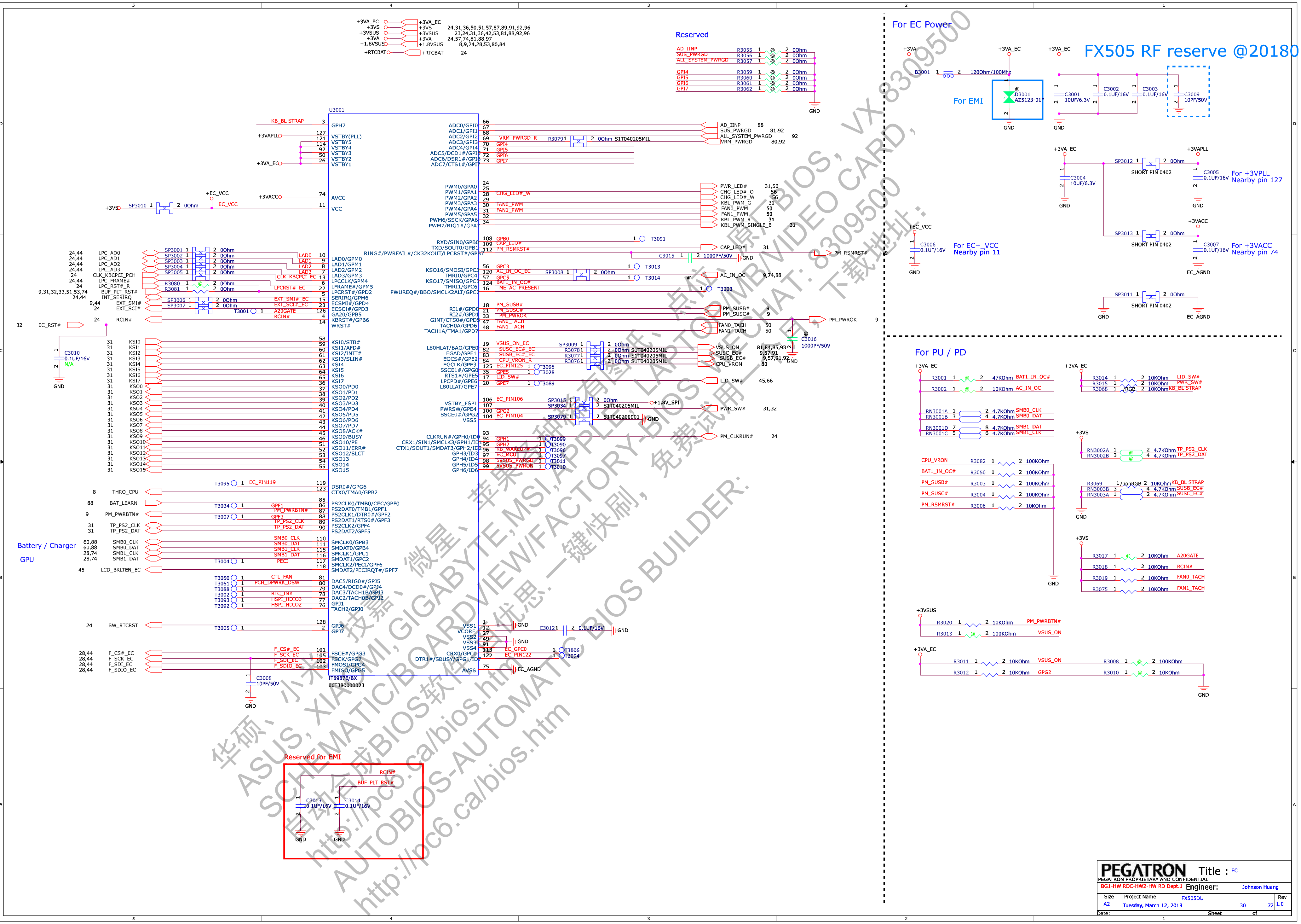

U0301E
LPC :3.3V
3.3V GPIO
1.8VSUS GPIO
CMOS Settings
Clear CMOS
Keep CMOS
JRST2401
Shunt
Open
(Default)
PEGATRON
Title PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Johnson Huang
Project Name FX505DU
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 24 of 72

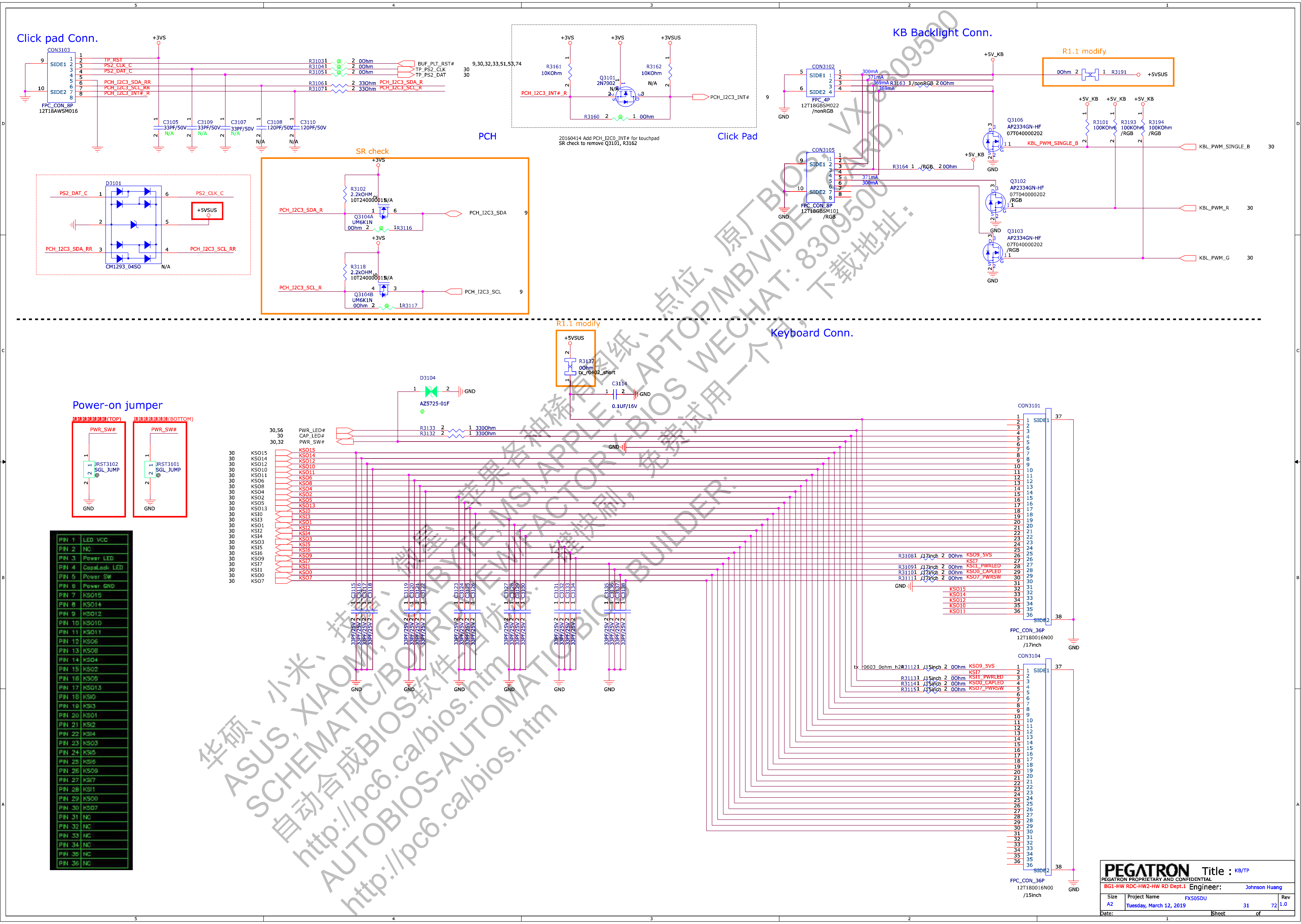


PCH SMBus

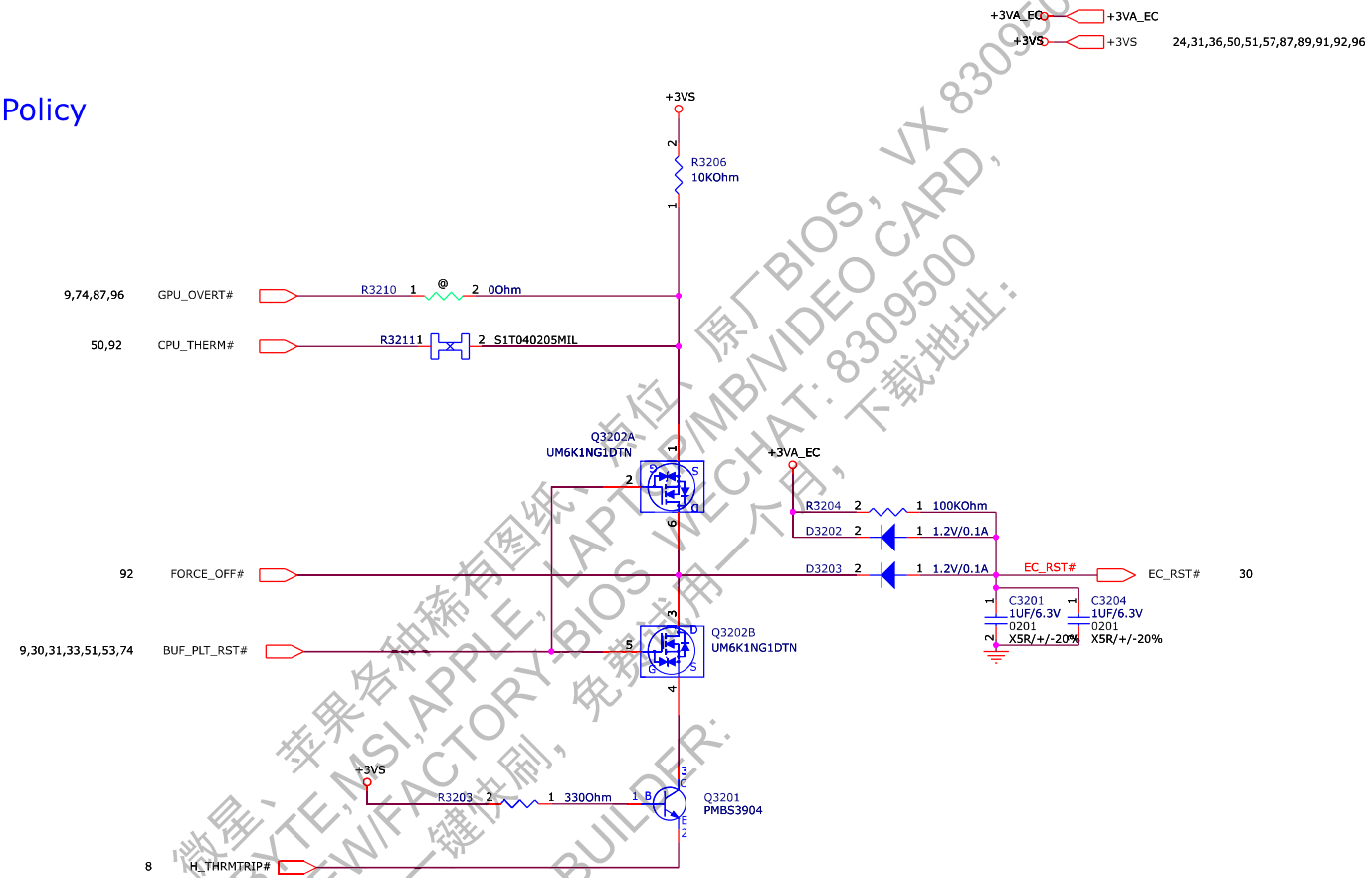


PEGATRON Title : PCH(9)_SPI_SMB
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD Engineer: Johnson Huang
Size: Custom | Project Name: FX505DU | Rev: 1.1
Date: Tuesday, March 12, 2019 | Sheet 28 of 72

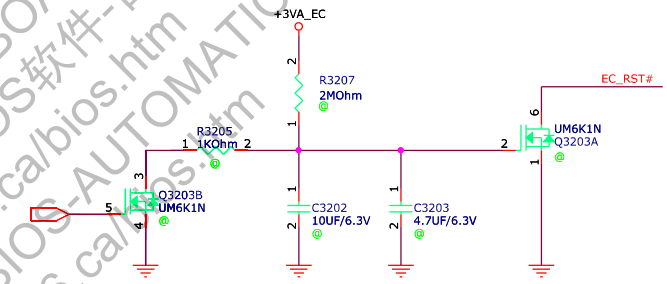




Thermal Policy

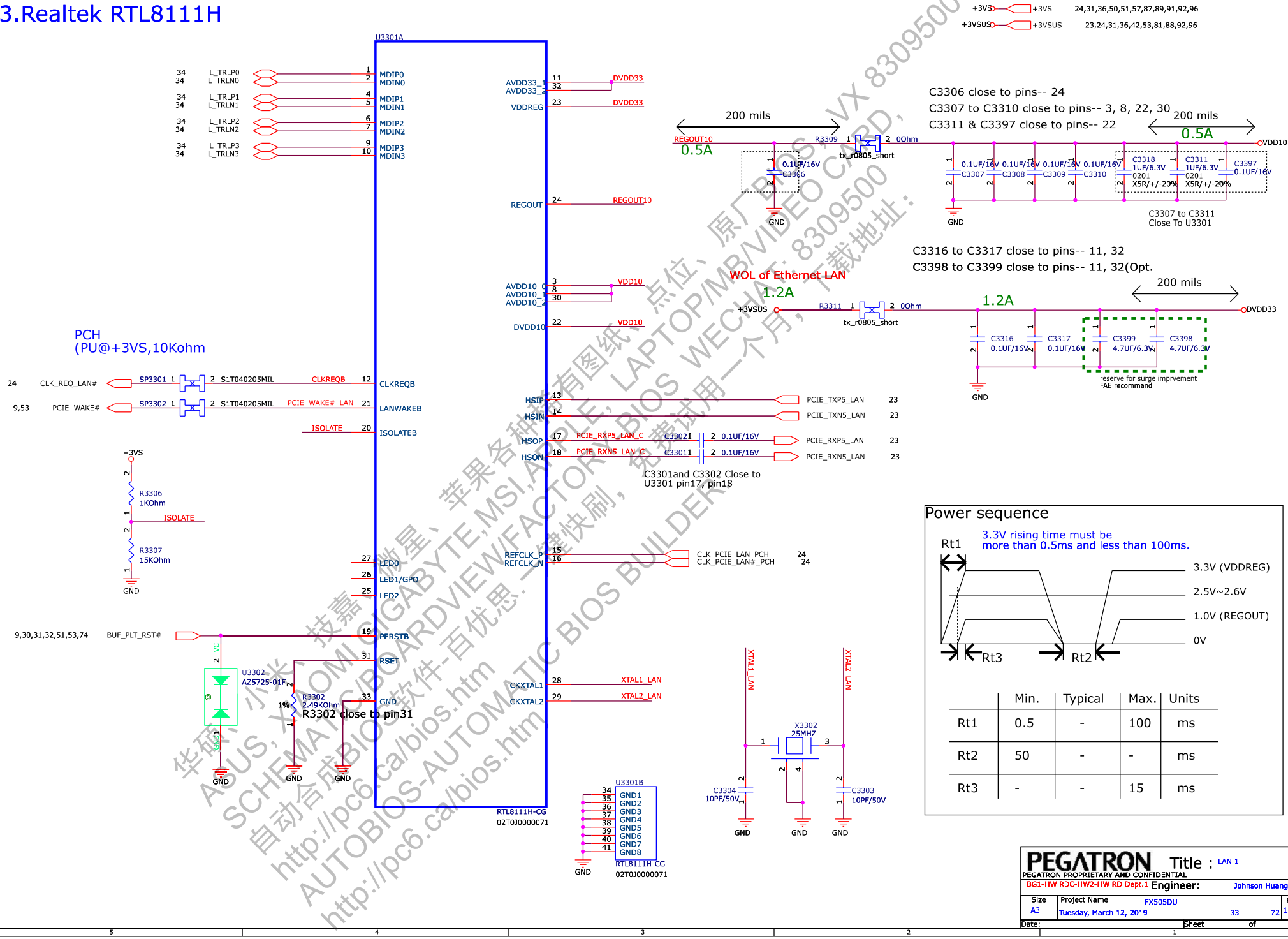


EC reset



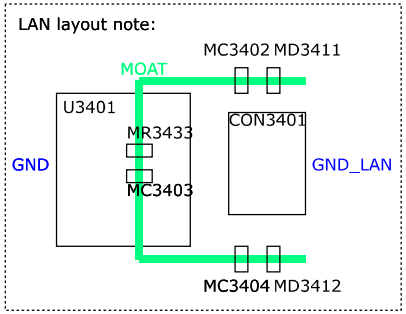
PEGATRON Title : RST
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size A3 | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 32 of 72

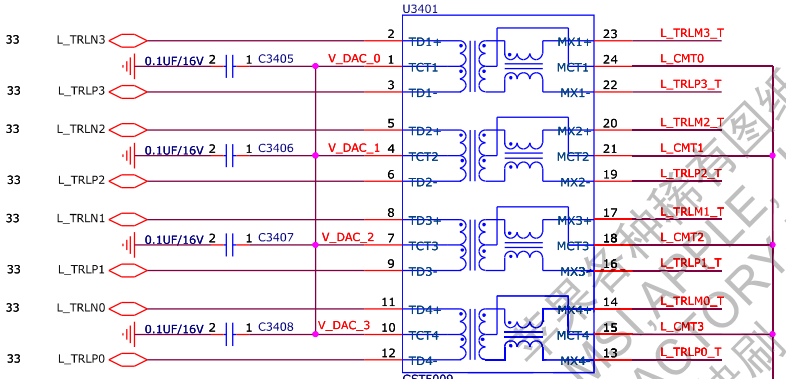
33.Realtek RTL8111H

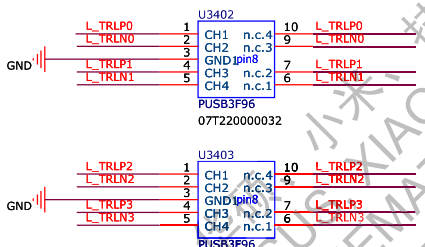


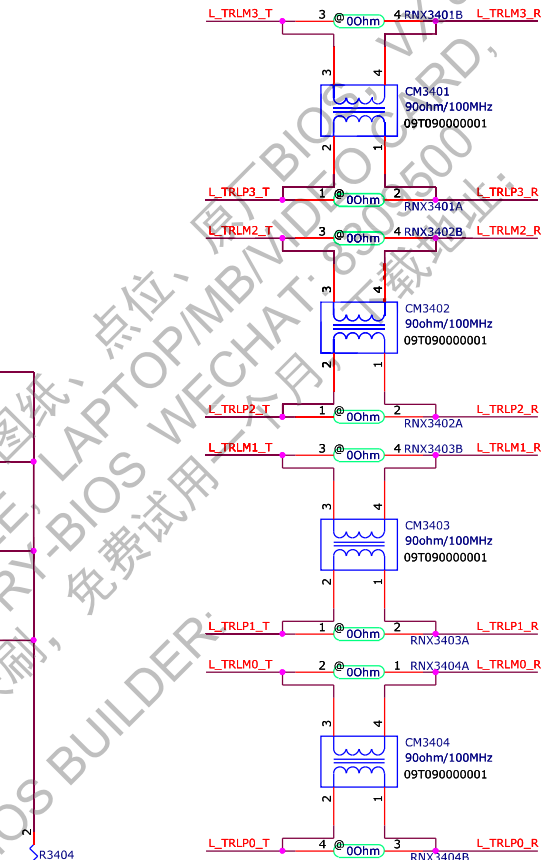
PEGATRON	Title : LAN 1			
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG1-HW RDC-HW2-HW RD Dept.1	Engineer:	Johnson Huang		
Size	Project Name	FX505DU		Rev
A3	Tuesday, March 12, 2019	33	72	1.0
Date:		Sheet	of	

34.Transformer/RJ45

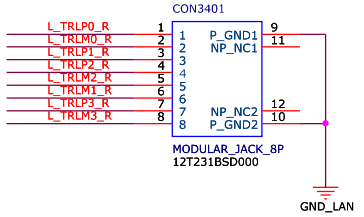


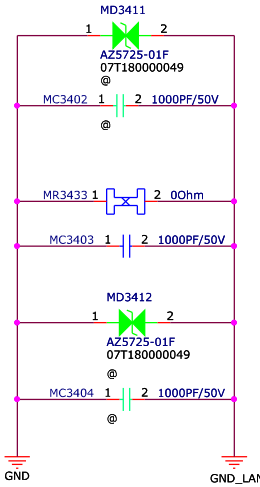






RJ45



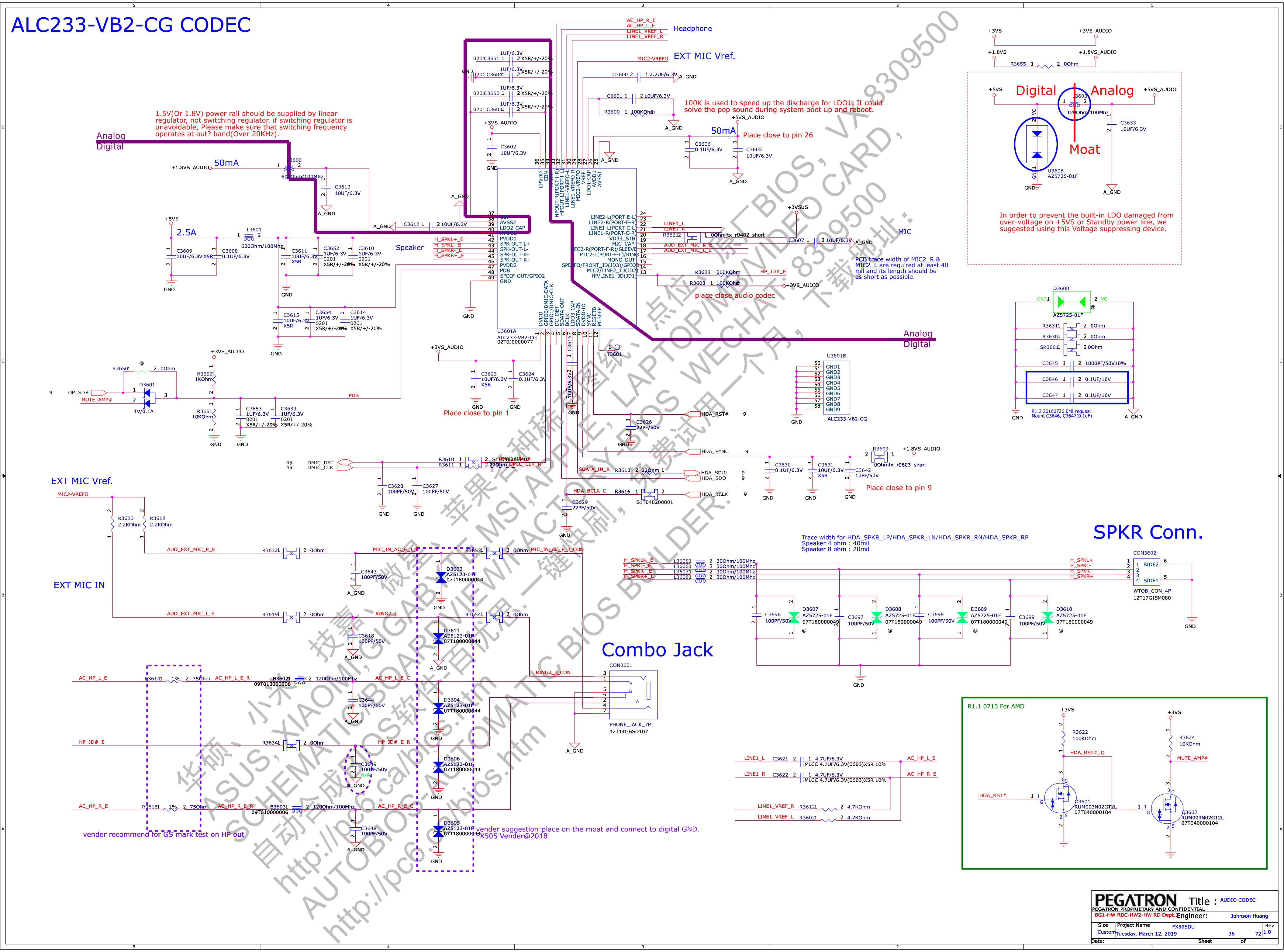


PEGATRON Title : LAN 2

PEGATRON PROPRIETARY AND CONFIDENTIAL

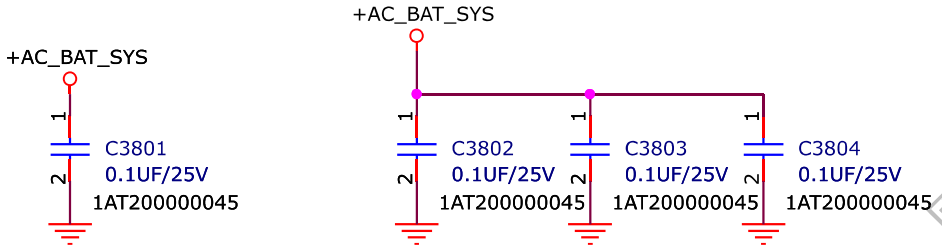
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name		Rev
A3	FX505DU		1.0
Date: Tuesday, March 12, 2019	Sheet 34	of 72	

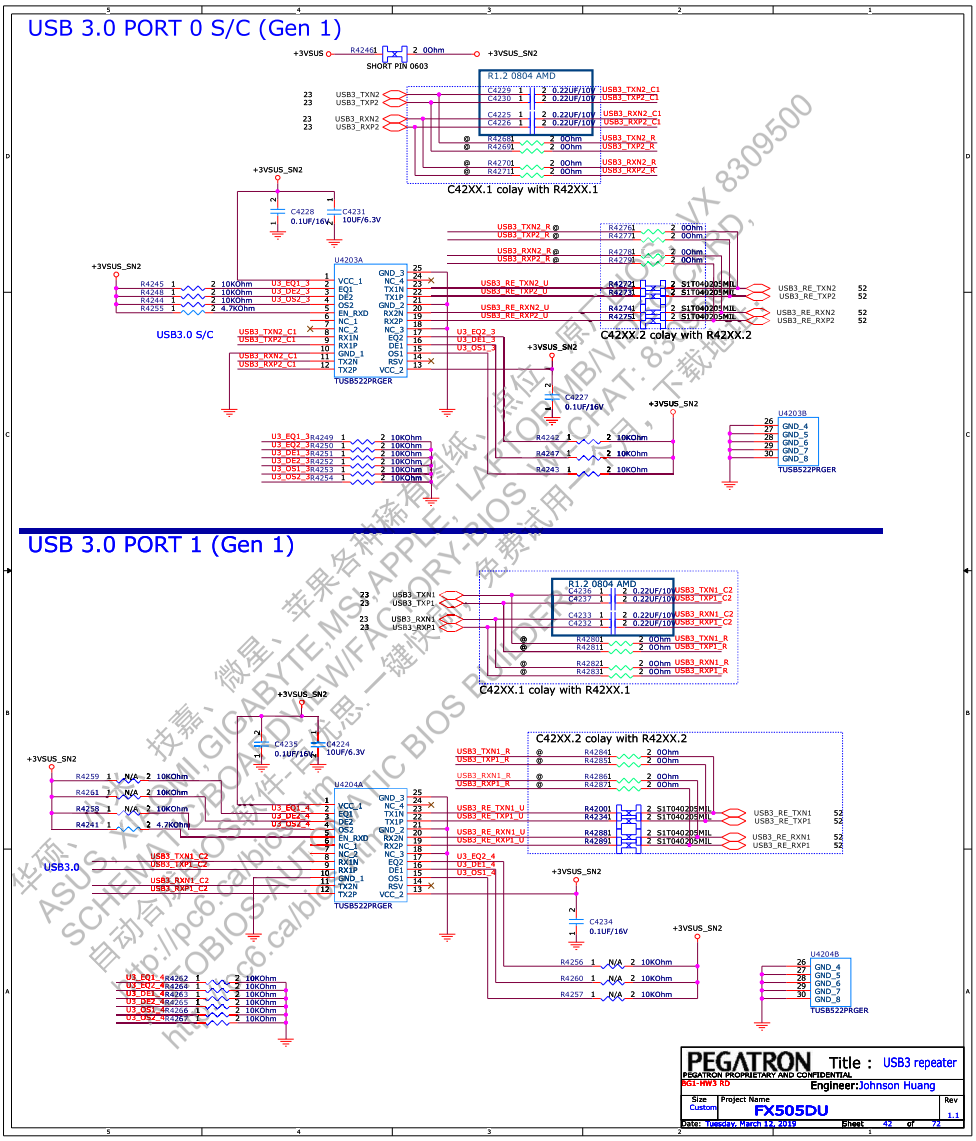


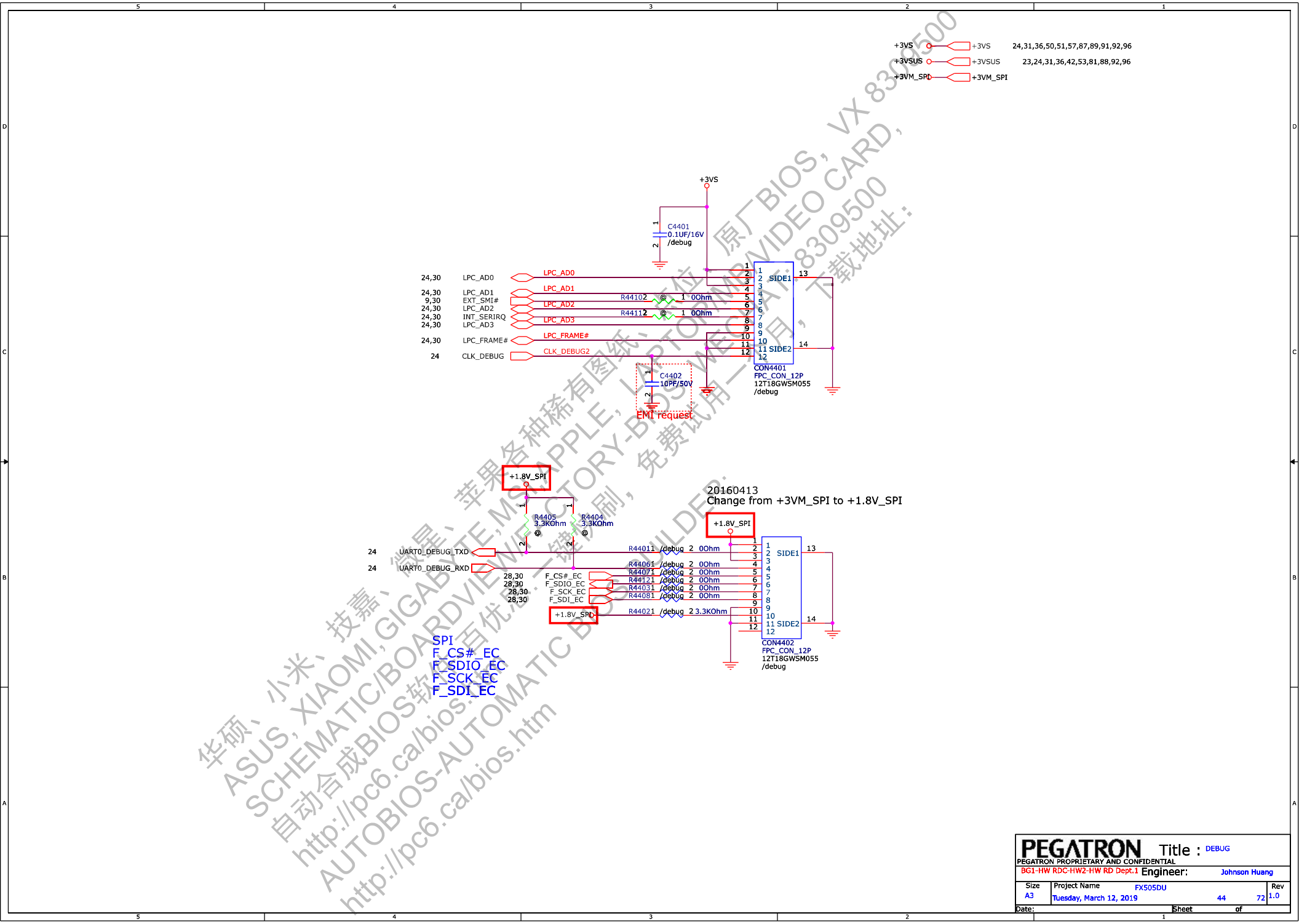
ALC233-VB2-CG CODEC
Headphone
EXT MIC Vref.
1.5V(Or 1.8V) power rail should be supplied by linear regulator, not switching regulator. if switching regulator is unavoidable, Please make sure that switching frequency operates at out? band(Over 20KHz).
Analog
Digital
50mA
2.5A
Speaker
100K is used to speed up the discharge for LDO1. It could solve the pop sound during system boot up and reboot.
Place close to pin 26
MIC
PCB trace width of MIC2_R & MIC2_L are required at least 40 mil and its length should be as short as possible.
place close audio codec
Place close to pin 1
Place close to pin 9
Digital
Analog
Moat
In order to prevent the LDO damaged from over-voltage on +5VS or Standby power line, we suggested using this Voltage suppressing device.
R1.2 20160726 EMI request Mount C3646, C3647(0.1uF)
EXT MIC Vref.
EXT MIC IN
SPKR Conn.
Trace width for HDA_SPKR_LP/HDA_SPKR_LN/HDA_SPKR_RN/HDA_SPKR_RP
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil
Combo Jack
vender recommend for GS mark test on HP out
vender suggestion:place on the moat and connect to digital GND.
FX505 Vender@2018
R1.1 0713 For AMD
U3601A ALC233-VB2-CG
U3601B ALC233-VB2-CG
CON3601 PHONE_JACK_7P
CON3602 WTOB_CON_4P
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : AUDIO CODEC
BG1-HW RDC-HW2-HW RD Dept.
Engineer: Johnson Huang
Project Name FX505DU
Size Custom
Tuesday, March 12, 2019
Sheet 36 of 72
Rev 1.0

+AC_BAT_SYS +AC_BAT_SYS 80,81,82,83,84,88,97



Title <Title>		
Size A	Document Number FX505DU	Rev 1.1
Date: Tuesday, March 12, 2019	Sheet 38 of 72	

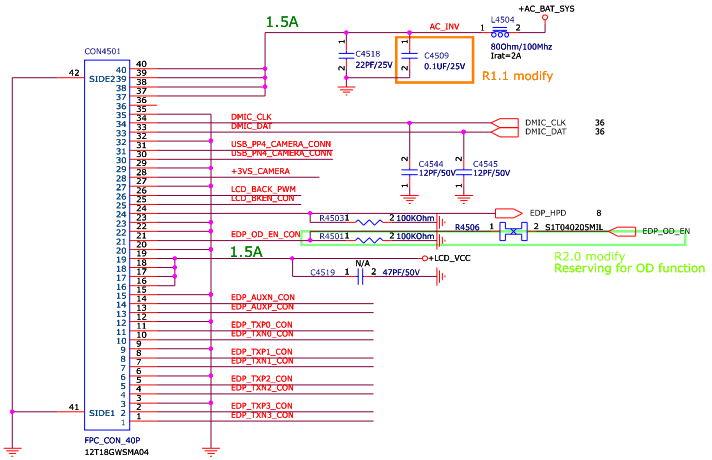

USB 3.0 PORT 0 S/C (Gen 1)
C42XX.1 colay with R42XX.1
C42XX.2 colay with R42XX.2
USB3.0 S/C
TUSB522PRGER
USB 3.0 PORT 1 (Gen 1)
C42XX.1 colay with R42XX.1
C42XX.2 colay with R42XX.2
USB3.0
TUSB522PRGER
PEGATRON
Title : USB3 repeater
PEGATRON PROPRIETARY AND CONFIDENTIAL
SG1-MW3 RD
Engineer:Johnson Huang
Size
Custom
Project Name
FX505DU
Rev
1.1
Date: Tuesday, March 12, 2019
Sheet 42 of 72



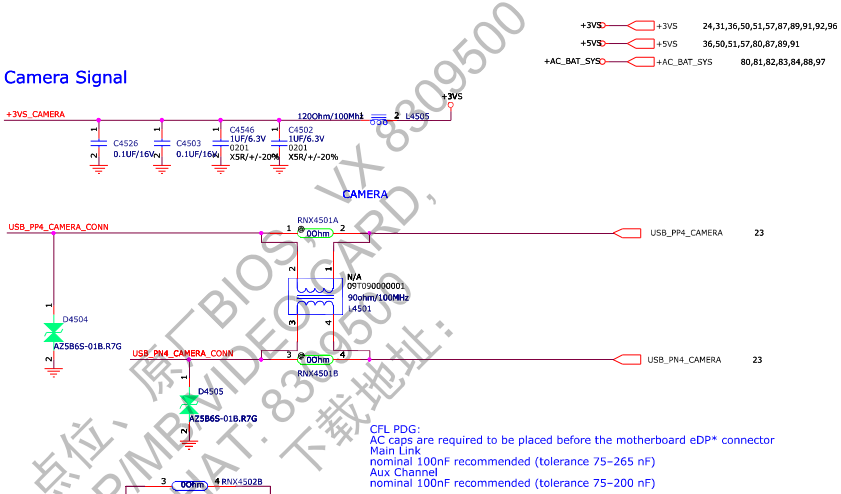
PEGATRON Title : DEBUG
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 44 of 72	

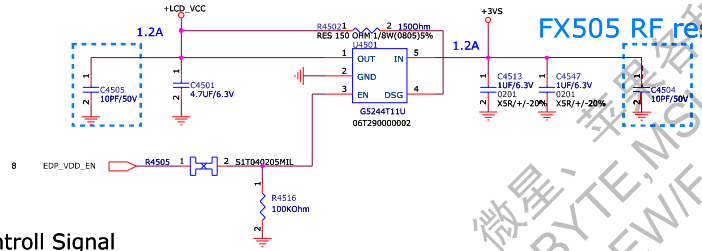
eDP Conn.



Camera Signal

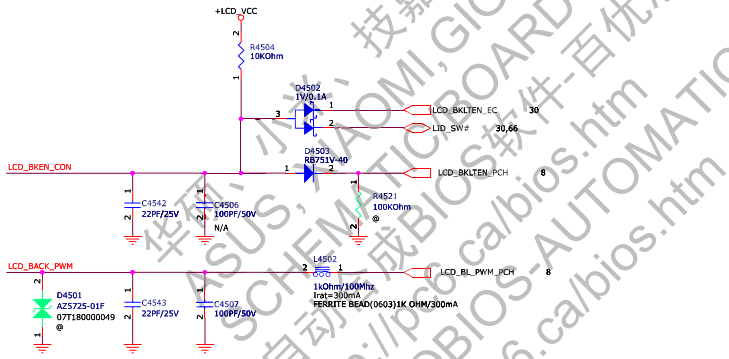


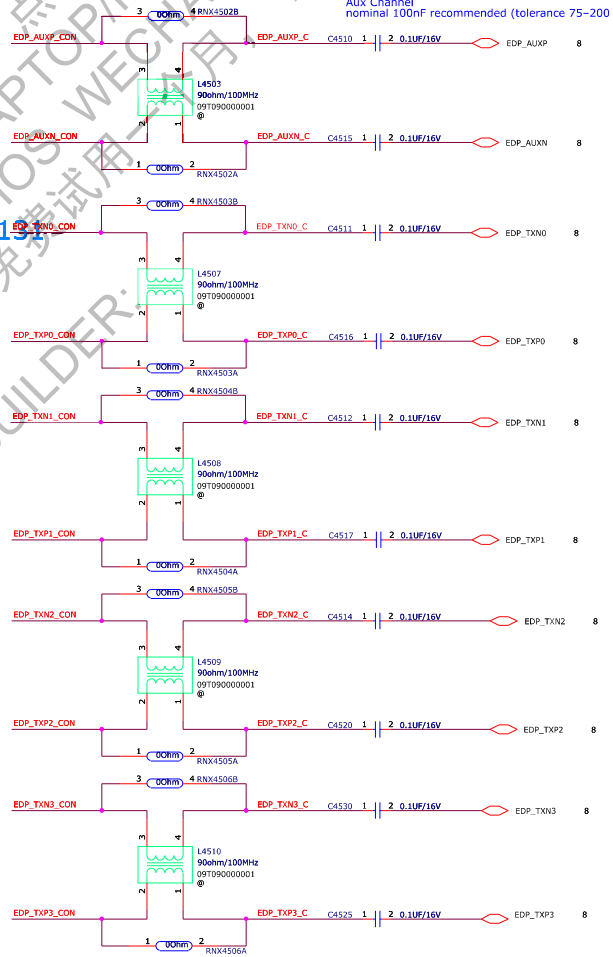
LCD VDDEN / +LED_VCC



FX505 RF reserve @20180131

Controll Signal





+3VS	+3VS	24,31,36,50,51,57,87,89,91,92,96
+5VS	+5VS	36,50,51,57,80,87,89,91
+AC_BAT_SYS	+AC_BAT_SYS	80,81,82,83,84,88,97

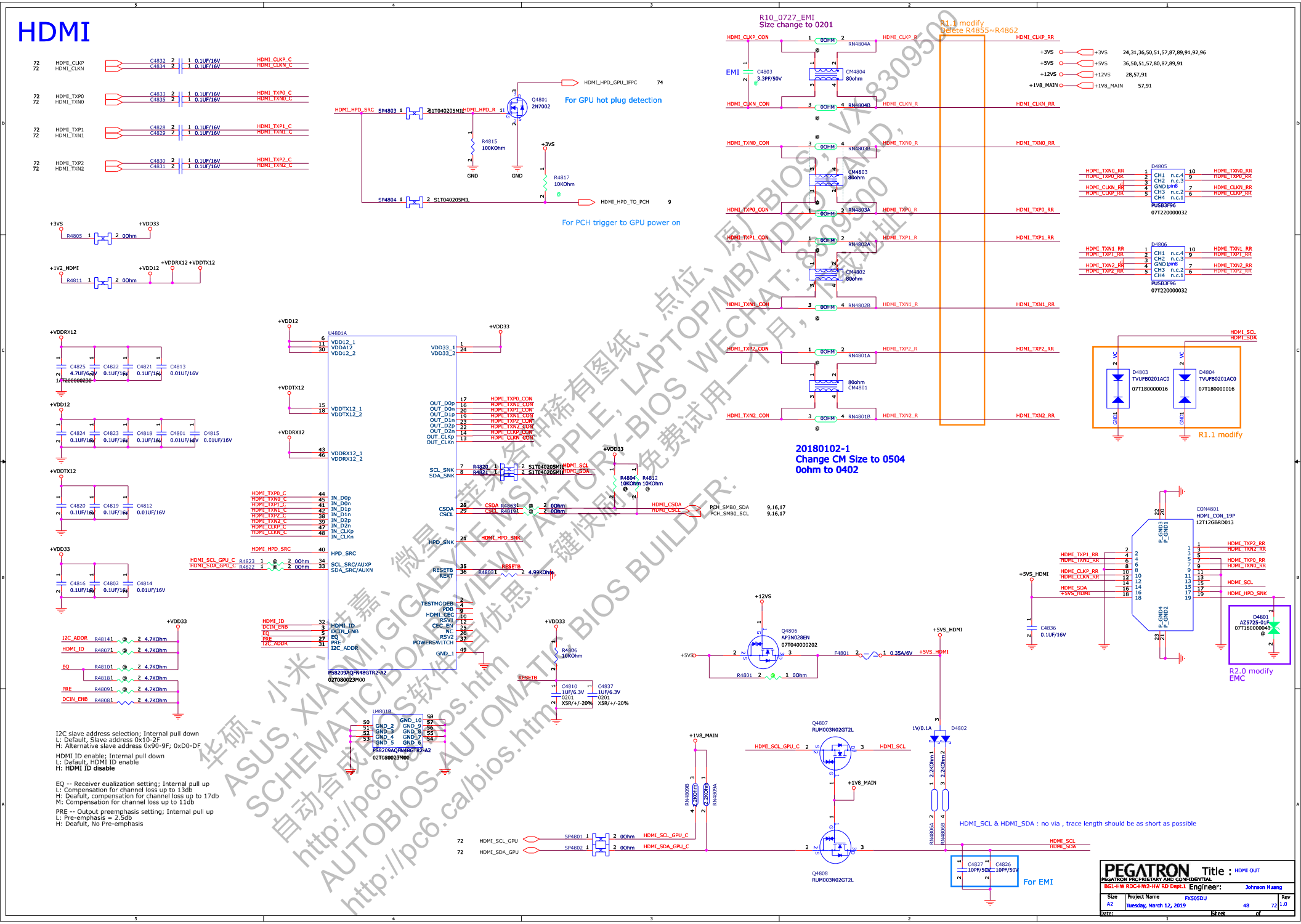
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : EDP/MIC

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A2	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 45 of 72	

HDMI

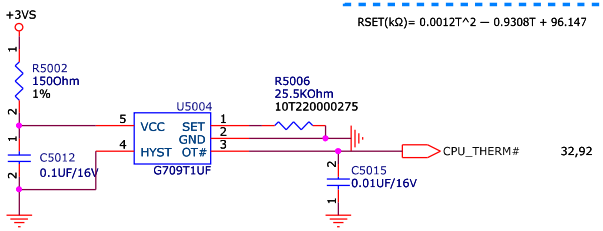


PEGATRON	Title : HDMI OUT		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: Johnson Huang		
Size: A2	Project Name: FX505DU		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet: 48 of 72		

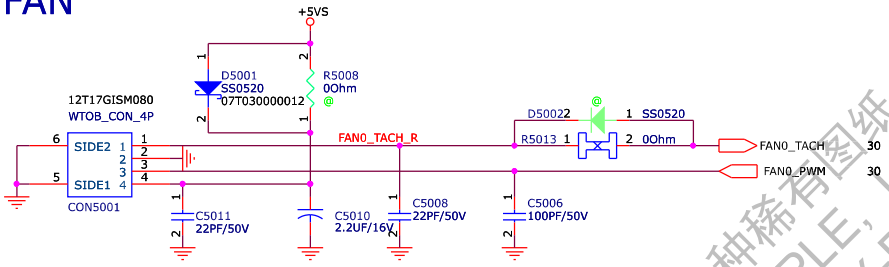
CPU Thermal Sensor

temperature set=85 C

RSET(kΩ)= 0.0012T^2 – 0.9308T + 96.147

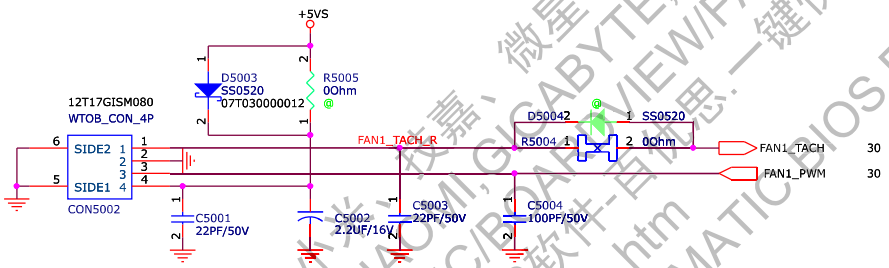


CPU FAN

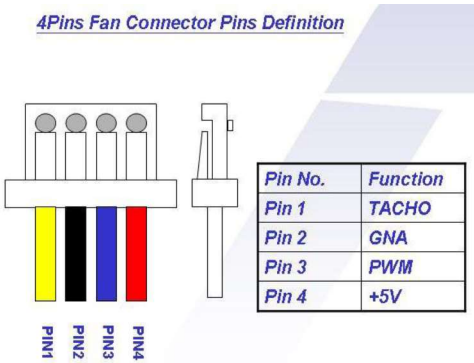


EC(PU@+3VS,10Kohm

GPU FAN



EC(PU@+3VS,10Kohm



Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

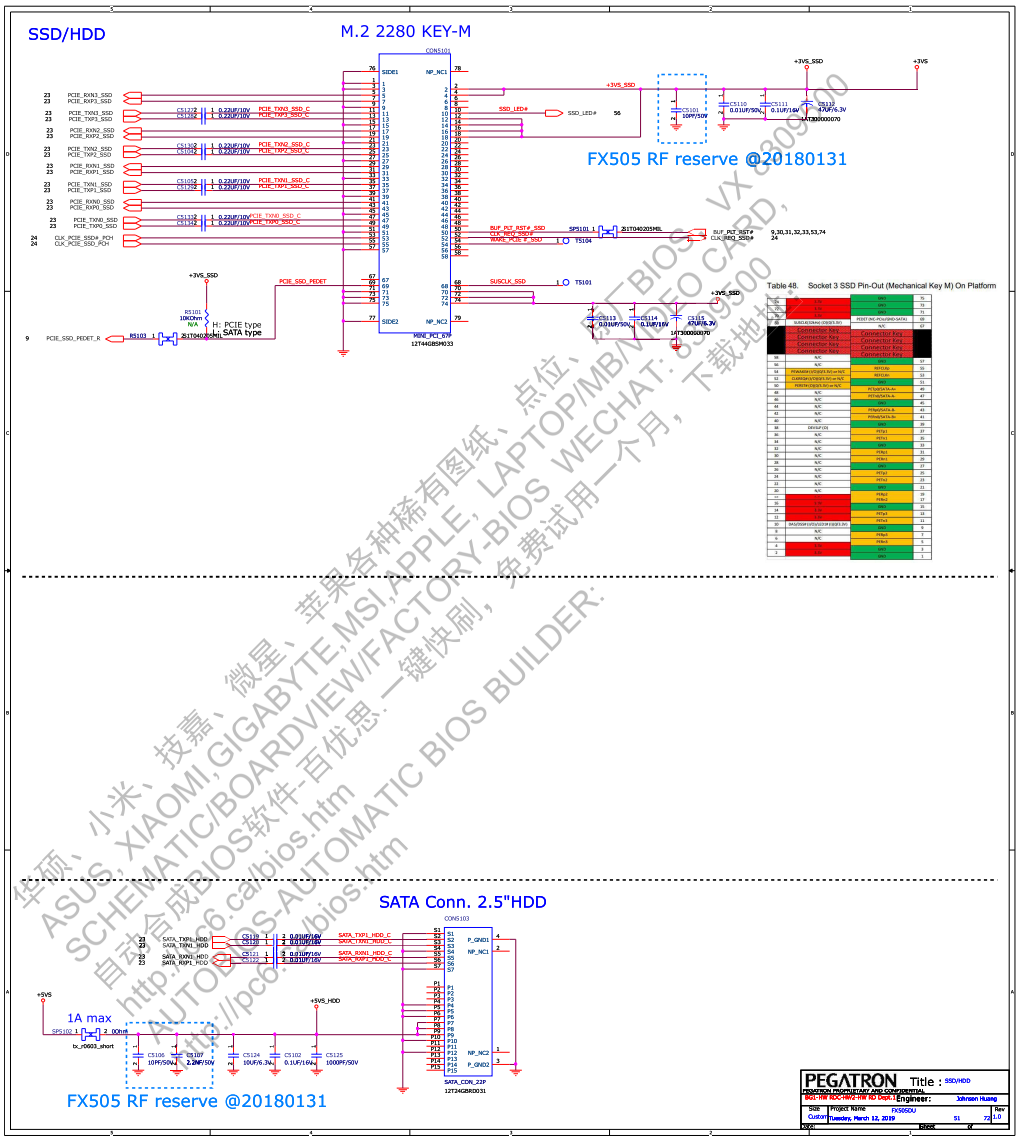
PEGATRON Title : FAN/THERMAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

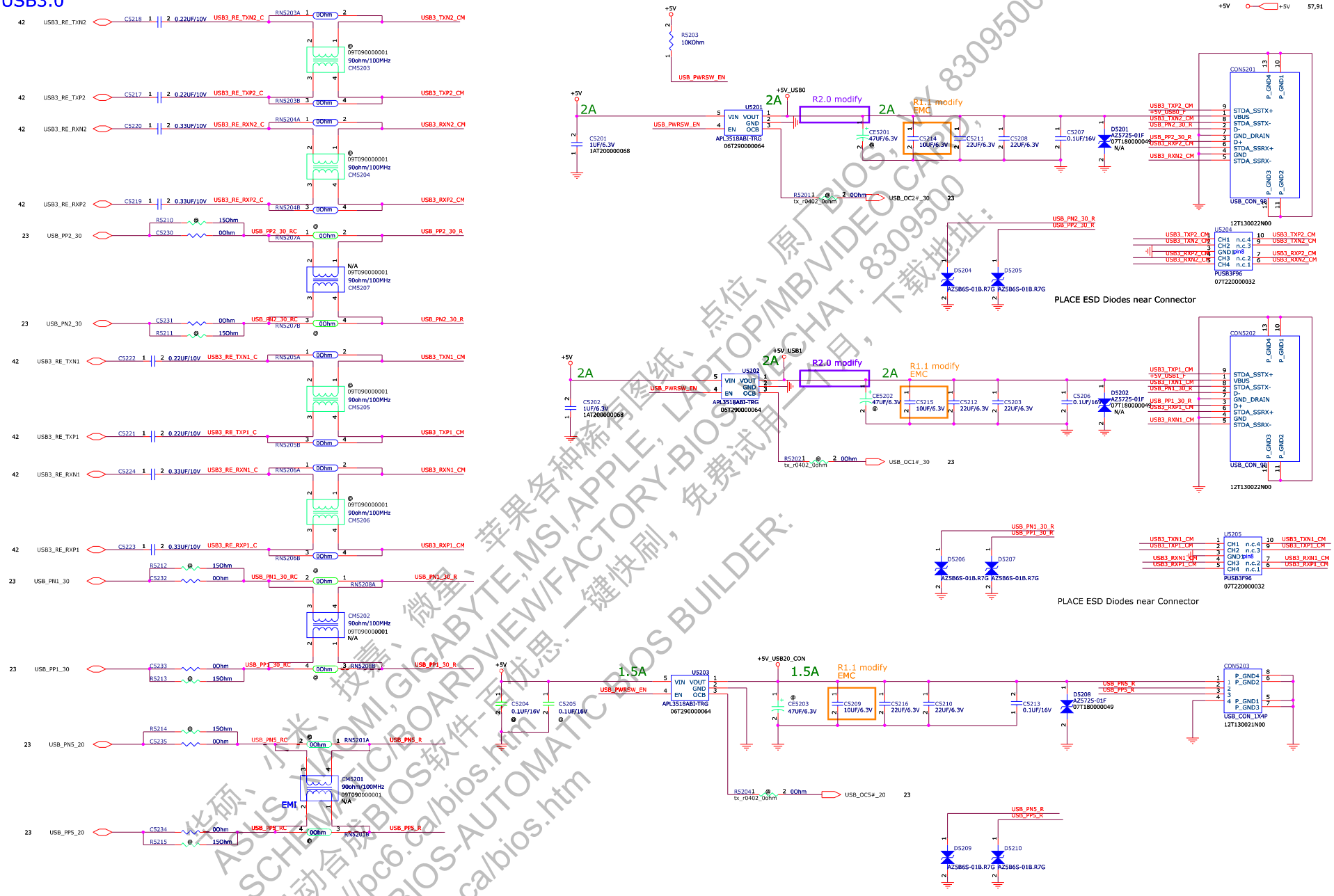
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0

Date: Tuesday, March 12, 2019 Sheet 50 of 72



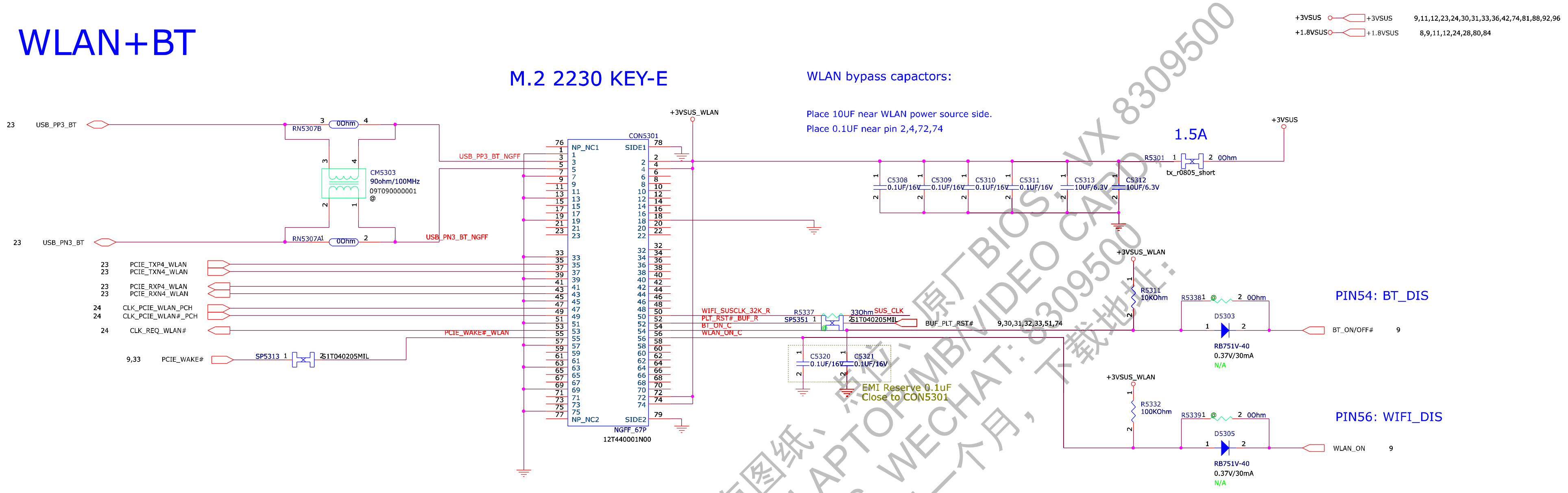
52.USB3.0



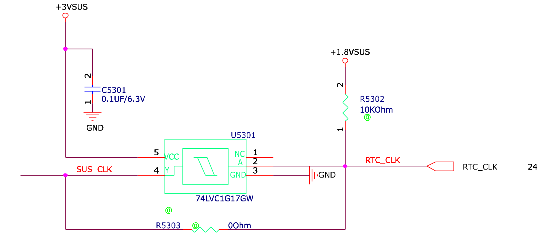
PEGATRON	Title : USB 3CAK		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: Johnson Huang		
Size: A2	Project Name: FX505GE		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet: 52 of 72		

WLAN+BT

M.2 2230 KEY-E



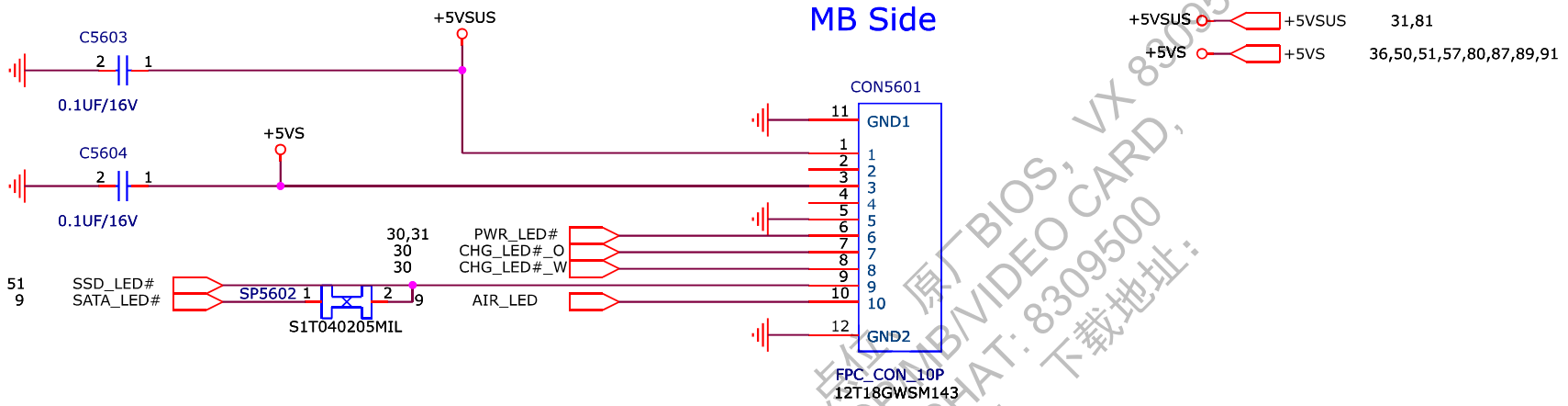
WLAN_SUS_CLK Update



Pin	Standard M.2 Key E	LcP Signals
74	+V3P3A	
72	+V3P3A	
70	PEWake1# (IO)(0/3.3V)	
68	CLKREQ1# (IO)(0/3.3V)	
66	PERST1# (O)(0/3.3V)	
64	RESERVED	REFCLKO (I)(1V@38.4MHz)
62	ALERT# (I)(0/1.8)	A4WP_IRQ#
60	I2C_CLK (O)(0/1.8V)	A4WP_I2C_CLK
58	I2C_DATA (IO)(0/1.8)	A4WP_I2C_DATA
56	W_DISABLE1# (O)(0/3.3V)	
54	W_DISABLE2# (O)(0/3.3V)	
52	PERST0# (O)(0/3.3V)	
50	SUSCLK(32kHz) (O)(0/3.3V)	C_P32K (3.3V Tolerant)
48	COEX_TXD (O)(0/1.8V)	
46	COEX_RXD (O)(0/1.8V)	
44	COEX3 (IO)(0/1.8V)	
42	CLink CLK	
40	CLink DATA	
38	CLink RESET (O)(0/3.3V)	
36	LPSS UART RTS (O)(0/1.8V)	/ BRI_DT (MUX'd in PCH/SoC)
34	LPSS UART CTS (I)(0/1.8V)	/ RGI_RSP (MUX'd in PCH/SoC)
32	LPSS UART Tx (O)(0/1.8V)	/ RGI_DT (MUX'd in PCH/SoC)
E	Connector Key	
	Connector Key	
	Connector Key	
	Connector Key	
22	LPSS UART Rx (I)(0/1.8V)	/ BRI_RSP (MUX'd in PCH/SoC)
20	UART Wake# (I)(0/3.3V)	
18	GND	GND/LNA_EN (LcP Production)
16	LED2# (I)(OD)	
14	PCM_OUT (O)(0/1.8V)	/ CLKREQ0 (MUX'd in PCH/SoC)
12	PCM_IN (I)(0/1.8V)	
10	PCM_SYNC (OI)(0/1.8V)	/RF_RESET_B (MUX'd in PCH/SoC)
8	PCM_CLK (OI)(0/1.8V)	
6	LED1# (I)(OD)	
4	+V3P3A	
2	+V3P3A	

LcP Signals	Standard M.2 Key E	Pin
GND		75
WT_CLKP	REFCLKN1	73
WT_CLKN	REFCLKP1	71
GND		69
WT_D0P	PERn1	67
WT_D0N	PERp1	65
GND		63
WT_D1P	PETn1	61
WT_D1N	PETp1	59
GND		57
PEWake0# (IO)(0/3.3V)		55
CLKREQ0# (IO)(0/3.3V)		53
GND		51
REFCLKN0		49
REFCLKP0		47
GND		45
PERn0		43
PERp0		41
GND		39
PETn0		37
PETp0		35
GND		33
Connector Key		E
Connector Key		
Connector Key		
Connector Key		
WGR_CLKP	SDIO Reset#(O)(0/1.8V)	23
WGR_CLKN	SDIO Wake#(I)(0/1.8V)	21
GND	SDIO DAT3(IO)(0/1.8V)	19
WGR_D0P	SDIO DAT2(IO)(0/1.8V)	17
WGR_D0N	SDIO DAT1(IO)(0/1.8V)	15
GND	SDIO DAT0(IO)(0/1.8V)	13
WGR_D1P	SDIO CMD(IO)(0/1.8V)	11
WGR_D1N	SDIO CLK(O)(0/1.8V)	9
GND		7
USB_D-		5
USB_D+		3
GND		1

PEGATRON Title : WLAN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size A2 | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 53 of 72



Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF

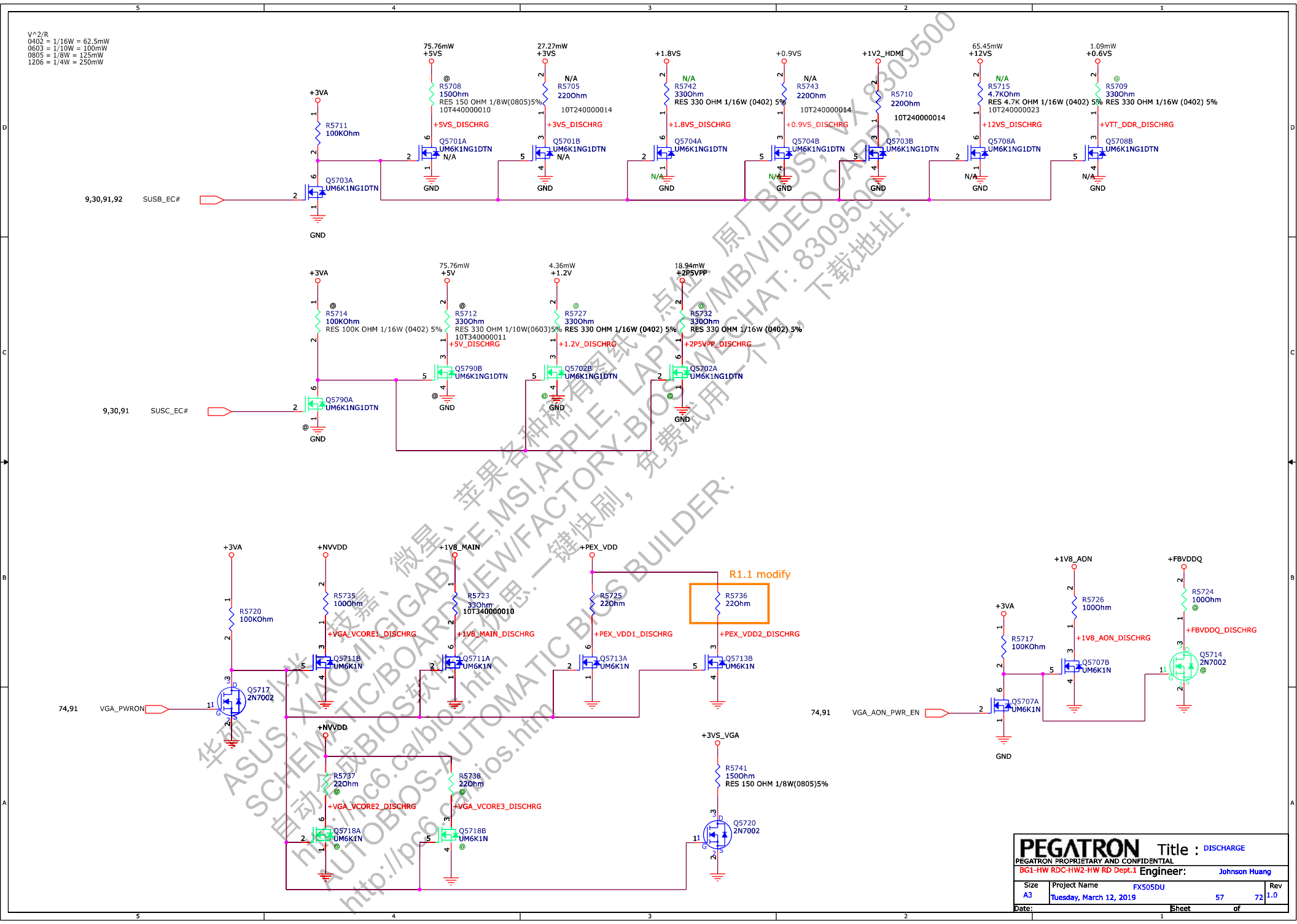
Charger LED

PCB/ID LOCATION

HDD LED

PEGATRON Title : LED
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept. Engineer: Johnson Huang

Size	Project Name		Rev
A4	FX505DU		1.0
Date: Tuesday, March 12, 2019	Sheet 56	of 72	


V^2/R
0402 = 1/16W = 62.5mW
0603 = 1/10W = 100mW
0805 = 1/8W = 125mW
1206 = 1/4W = 250mW
+3VA
R5711
100KOhm
75.76mW
+5VS
R5708
150Ohm
RES 150 OHM 1/8W(0805)5%
10T440000010
+5VS_DISCHRG
Q5701A
UM6K1NG1DTN
N/A
GND
27.27mW
+3VS
N/A
R5705
220Ohm
10T240000014
+3VS_DISCHRG
Q5701B
UM6K1NG1DTN
+1.8VS
N/A
R5742
330Ohm
RES 330 OHM 1/16W (0402) 5%
+1.8VS_DISCHRG
Q5704A
UM6K1NG1DTN
+0.9VS
N/A
R5743
220Ohm
10T240000014
+0.9VS_DISCHRG
Q5704B
UM6K1NG1DTN
+1V2_HDMI
R5710
220Ohm
10T240000014
Q5703B
UM6K1NG1DTN
65.45mW
+12VS
N/A
R5715
4.7KOhm
RES 4.7K OHM 1/16W (0402) 5%
10T240000023
+12VS_DISCHRG
Q5708A
UM6K1NG1DTN
1.09mW
+0.6VS
R5709
330Ohm
RES 330 OHM 1/16W (0402) 5%
+VTT_DDR_DISCHRG
Q5708B
UM6K1NG1DTN
Q5703A
UM6K1NG1DTN
9,30,91,92
SUSB_EC#
+3VA
R5714
100KOhm
RES 100K OHM 1/16W (0402) 5%
75.76mW
+5V
R5712
330Ohm
RES 330 OHM 1/10W(0603)5%
10T340000011
+5V_DISCHRG
Q5790B
UM6K1NG1DTN
4.36mW
+1.2V
R5727
330Ohm
RES 330 OHM 1/16W (0402) 5%
+1.2V_DISCHRG
Q5702B
UM6K1NG1DTN
18.94mW
+2P5VPP
R5732
330Ohm
RES 330 OHM 1/16W (0402) 5%
+2P5VPP_DISCHRG
Q5702A
UM6K1NG1DTN
Q5790A
UM6K1NG1DTN
9,30,91
SUSC_EC#
+3VA
R5720
100KOhm
+NVVDD
R5735
100Ohm
+VGA_VCORE1_DISCHRG
Q5711B
UM6K1N
+1V8_MAIN
R5723
33Ohm
10T340000010
+1V8_MAIN_DISCHRG
Q5711A
UM6K1N
+PEX_VDD
R5725
220Ohm
+PEX_VDD1_DISCHRG
Q5713A
UM6K1N
R1.1 modify
R5736
22Ohm
+PEX_VDD2_DISCHRG
Q5713B
UM6K1N
Q5717
2N7002
74,91
VGA_PWRON
+NVVDD
R5737
22Ohm
@
+VGA_VCORE2_DISCHRG
Q5718A
UM6K1N
R5738
22Ohm
@
+VGA_VCORE3_DISCHRG
Q5718B
UM6K1N
+3VS_VGA
R5741
150Ohm
RES 150 OHM 1/8W(0805)5%
Q5720
2N7002
+1V8_AON
R5726
100Ohm
+1V8_AON_DISCHRG
Q5707B
UM6K1N
+FBVDDQ
R5724
100Ohm
@
+FBVDDQ_DISCHRG
Q5714
2N7002
@
+3VA
R5717
100KOhm
Q5707A
UM6K1N
74,91
VGA_AON_PWR_EN
GND
PEGATRON
Title : DISCHARGE
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size A3
Project Name FX505DU
Rev 1.0
Tuesday, March 12, 2019
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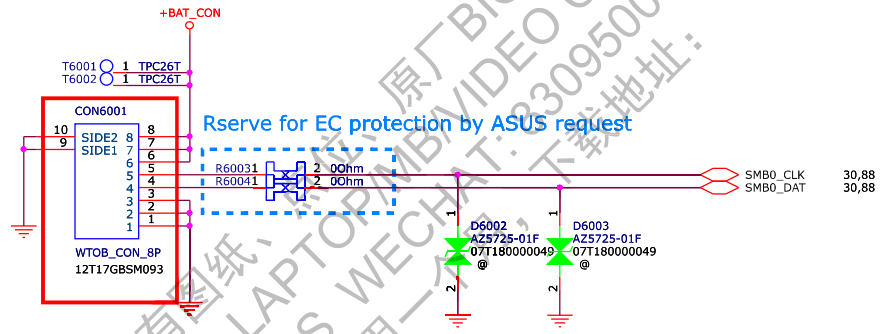
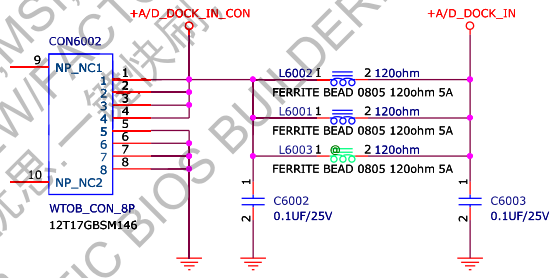
72
Date:
Sheet
of

Battery Conn.



ABBA assign: 1217-01UG0AS(1217-017L000), doesn't include 1217-01EG000 (the same pool)

AC in Conn.



FX505DD/DT N17P/N18P Adaptor: 120W (6.32A)
FX505DU N18E-G0 Adaptor: 180W (9.23A)

PEGATRON Title : BAT/AC IN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 60 of 99	

65.NUT,Screw hole,Tooling hole

M.2 SSD NUT:

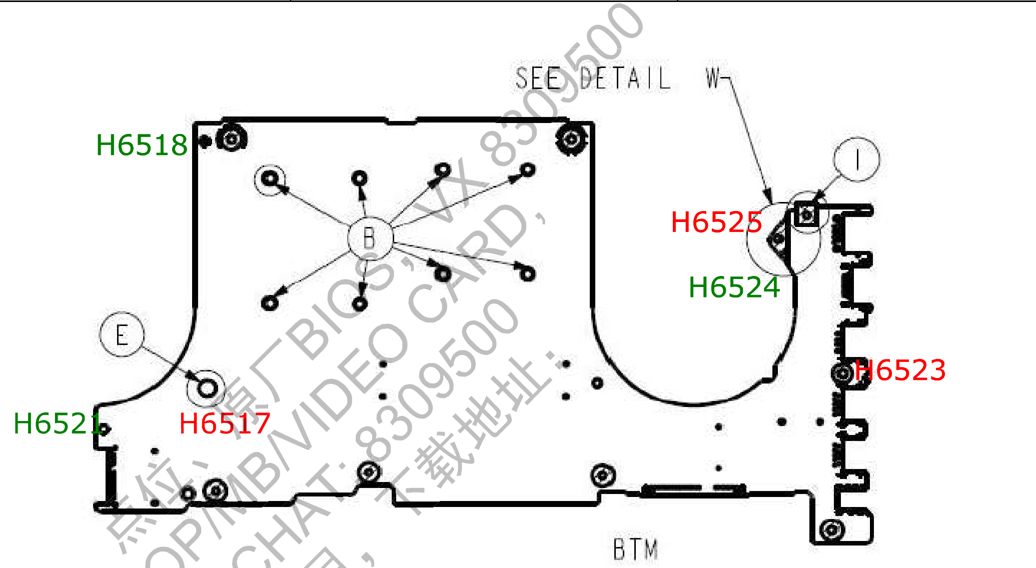
H6522
GND CT236B176D146

Tooling hole

drill 3*3.5
H6518 1 O138x118DO138x118N
H6521 1 O138x118DO138x118N

drill 1.7
H6524 1 C67D67N

drill 2.2*1.7
H6526 1 O87X67DO87X67N



Screw hole

B group:
CPU GPU bracket hole

H6501 1 CT303CB185D146
H6502 1 CT303CB185D146
H6503 1 CT303CB185D146
H6504 1 CT303CB185D146
GND

H6505 1 CT303CB185D146
H6506 1 CT303CB185D146
H6507 1 CT303CB185D146
H6508 1 CT303CB185D146
GND

E:
TOP: phi 7 drill 6
BOT: phi 7 drill 6

H6517 1 C276D236
GND

D group:

H6510 C315D118
1 P_GND — GND

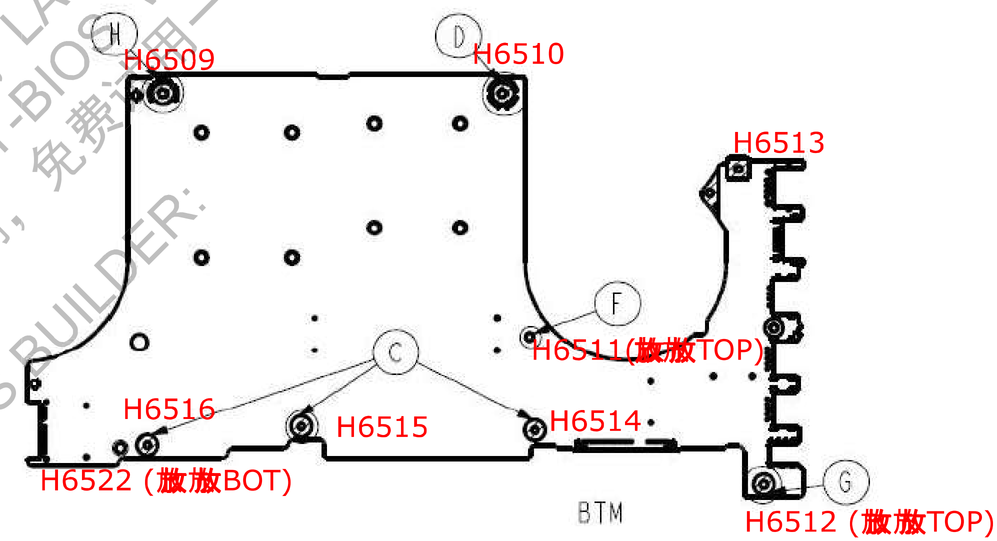
Pin	Name	Name	Pin
2			49
3	NP_NC_1	NP_NC_48	48
4	NP_NC_2	NP_NC_47	47
5	NP_NC_3	NP_NC_46	46
6	NP_NC_4	NP_NC_45	45
7	NP_NC_5	NP_NC_44	44
8	NP_NC_6	NP_NC_43	43
9	NP_NC_7	NP_NC_42	42
10	NP_NC_8	NP_NC_41	41
11	NP_NC_9	NP_NC_40	40
12	NP_NC_10	NP_NC_39	39
13	NP_NC_11	NP_NC_38	38
14	NP_NC_12	NP_NC_37	37
15	NP_NC_13	NP_NC_36	36
16	NP_NC_14	NP_NC_35	35
17	NP_NC_15	NP_NC_34	34
18	NP_NC_16	NP_NC_33	33
19	NP_NC_17	NP_NC_32	32
20	NP_NC_18	NP_NC_31	31
21	NP_NC_19	NP_NC_30	30
22	NP_NC_20	NP_NC_29	29
23	NP_NC_21	NP_NC_28	28
24	NP_NC_22	NP_NC_27	27
25	NP_NC_23	NP_NC_26	26
	NP_NC_24	NP_NC_25	

F:
TOP: phi 8 drill 3
BOT: phi 4 drill 3

H6511 1 CT315CB157D118
GND

C group:
TOP: phi 8 drill 2.5
BOT: phi 8 drill 2.5

H6514 1 C315D98 S1T1XDCCUY00
H6515 1 C315D98 S1T1XDCCUY00
H6516 1 C315D98 S1T1XDCCUY00
GND



Near Audio Jack
TOP: square 8
BOT: phi 8 drill 3

H6512 1 RT315X335B315D118
B_GND

R65011 1 2 0Ohm
R65021 1 2 0Ohm
B_GND A_GND

H group:

H6509 C315D118
1 P_GND — GND

Pin	Name	Name	Pin
2			20
3	NP_NC1	NP_NC19	21
4	NP_NC2	NP_NC20	22
5	NP_NC3	NP_NC21	23
6	NP_NC4	NP_NC22	24
7	NP_NC5	NP_NC23	25
8	NP_NC6	NP_NC24	26
9	NP_NC7	NP_NC25	27
10	NP_NC8	NP_NC26	28
11	NP_NC9	NP_NC27	29
12	NP_NC10	NP_NC28	30
13	NP_NC11	NP_NC29	31
14	NP_NC12	NP_NC30	32
15	NP_NC13	NP_NC31	33
16	NP_NC14	NP_NC32	34
17	NP_NC15	NP_NC33	35
18	NP_NC16	NP_NC34	36
19	NP_NC17	NP_NC35	37
	NP_NC18	NP_NC36	

I group:
TOP: square8*8.5 drill 2.5
BOT: square8*8.5 drill 2.5

H6513 1 R315X335D98
GND

TOP: phi 7 drill 3
BOT: phi 7 drill 3

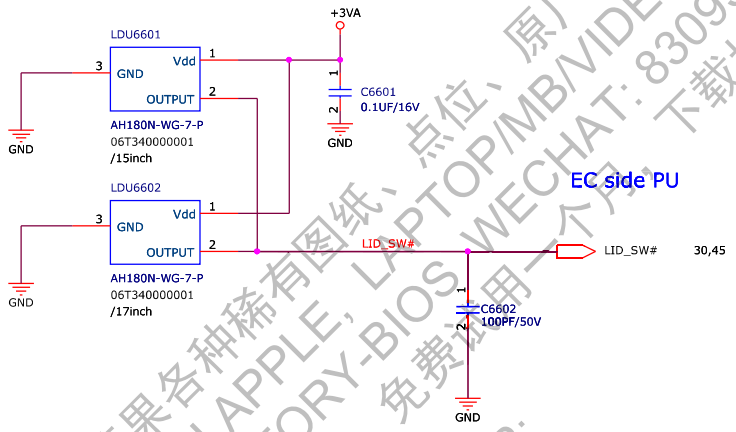
H6523 1 C276D118
GND

TOP: phi 3 drill 2.5
BOT: phi 3 drill 2.5

H6525 1 C118D98
GND

Title : NUT/HOLE
Engineer: Johnson Huang
Size: Custom | Project Name: FX505DU | Rev: 1.0
Date: Tuesday, March 12, 2019 | Sheet 65 of 72

Hall sensor



+3VA +3VA 24,57,74,81,88,97

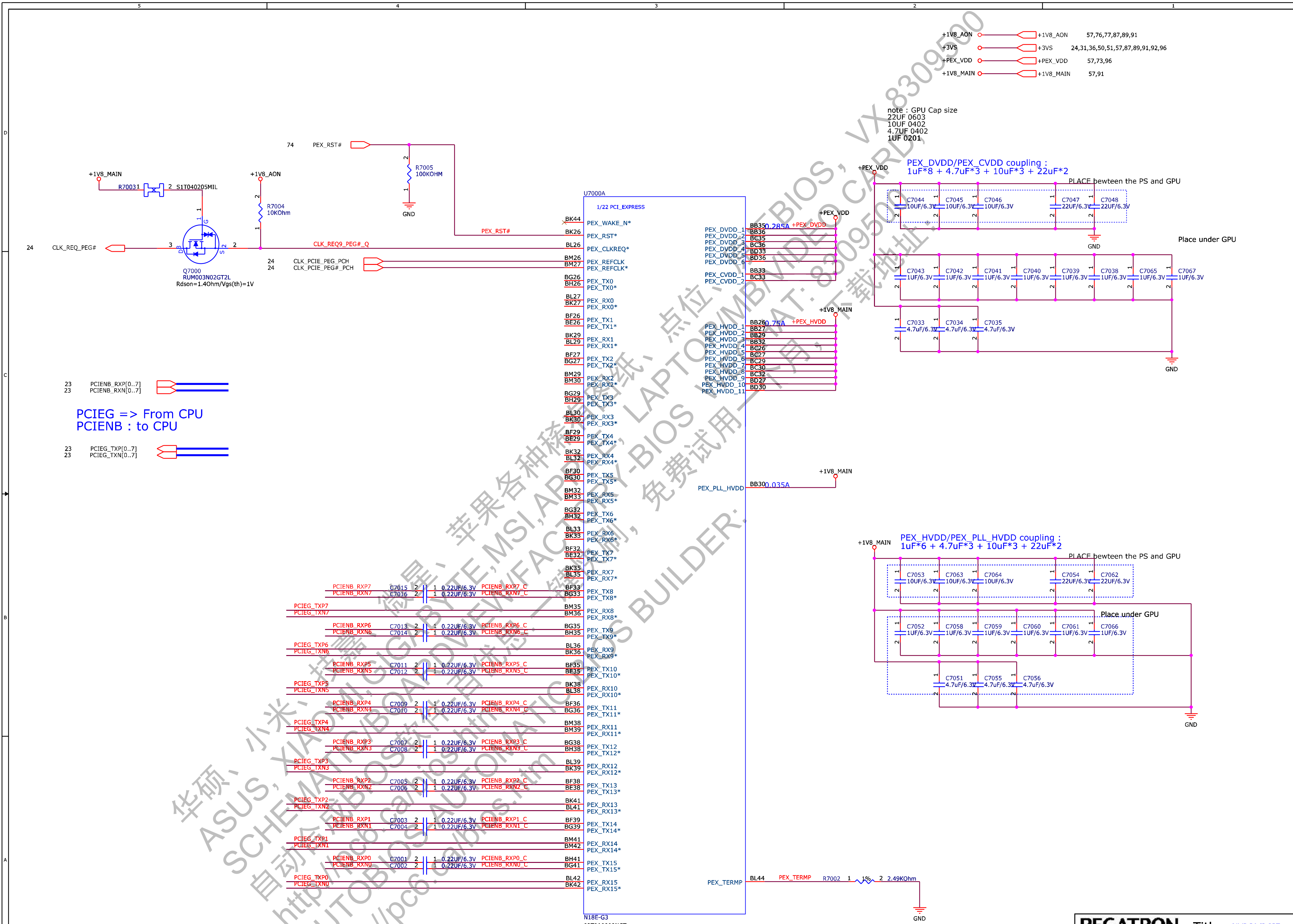
PEGATRON Title : TO DB

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0

Date: Tuesday, March 12, 2019 Sheet 66 of 72



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : NVDIA/PCIE
BG1-HW RD Div.2-HW RD Dept.2
Engineer: Johnson Huang
Size C
Project Name FX505DU
Rev 1.0
Date: Tuesday, March 12, 2019
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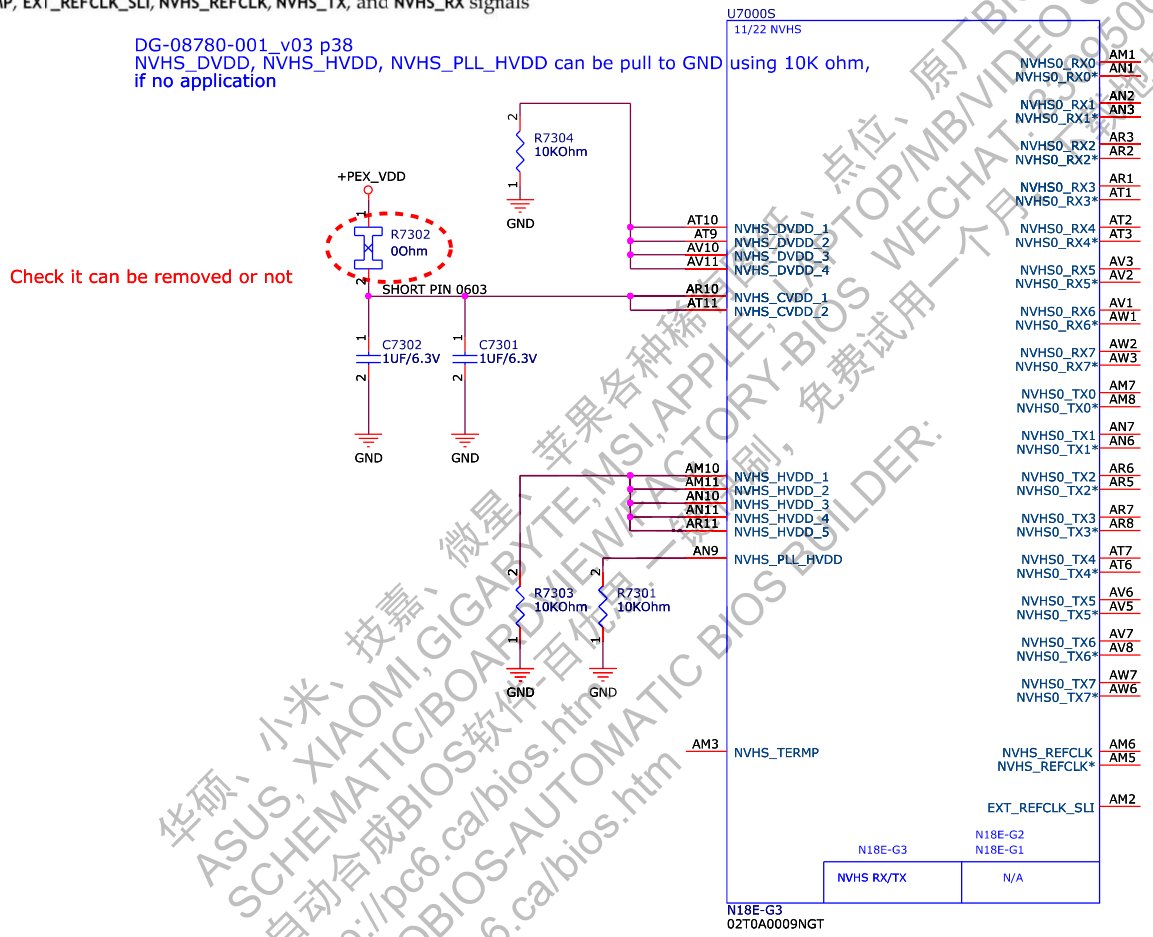
NVLINK

- N18E GPU does not support NVLink and SLI.
- Pull down **NVHS_DVDD**, **NVHS_CVDD**, **NVHS_HVDD**, and **NVHS_PLL_HVDD** rails to **GND** with 10 K resistor
- Do not use any decoupling or filtering capacitor for **NVHS_DVDD**, **NVHS_CVDD**, **NVHS_HVDD**, or **NVHS_PLL_HVDD** rails
- Leave **NVHS_TERMP**, **EXT_REFCLK_SLI**, **NVHS_REFCLK**, **NVHS_TX**, and **NVHS_RX** signals floating (**NC**).

DG-08780-001_v03 p38
NVHS_DVDD, NVHS_HVDD, NVHS_PLL_HVDD can be pull to GND using 10K ohm, if no application

Check it can be removed or not



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : NVDIA/Multi-use IO

BG1-HW RD Div.2-HW RD Dept.2 Engineer: Johnson Huang

Size	Project Name	Rev
B	FX505DU	1.0

Date: Tuesday, March 12, 2019 Sheet 73 of 99

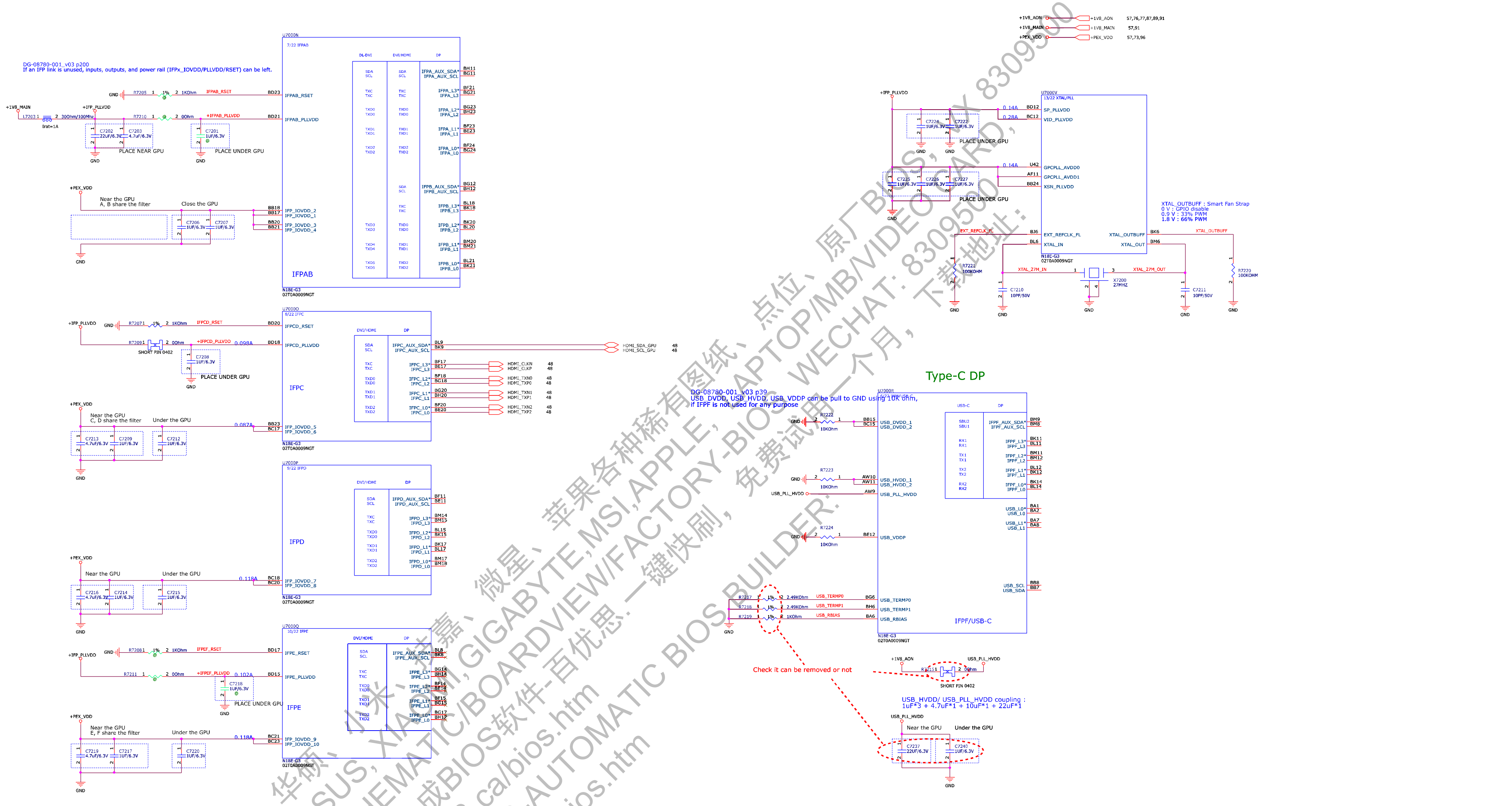


Table 10.5 HDMI Power Rails

Power Rails	Voltage	Maximum Current Draw
IFPA_IOVDD	1.0 V ± 5%	~87 mA
IFPB_IOVDD	1.0 V ± 5%	~87 mA
IFPC_IOVDD	1.0 V ± 5%	~87 mA
IFPD_IOVDD	1.0 V ± 5%	~87 mA
IFPE_IOVDD	1.0 V ±5%	~87 mA
IFPF_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 5%	~98 mA
IFPCD_PLLVDD	1.8 V ± 5%	~98 mA
IFPEF_PLLVDD	1.8 V ± 5%	~98 mA

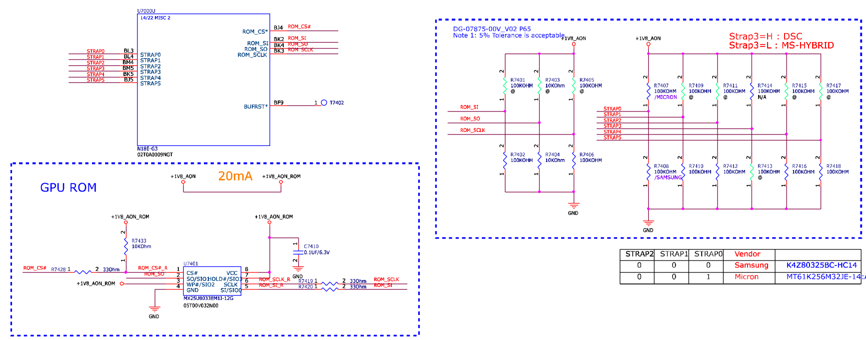
Table 10.1 Standard Configurations

Link	Description
GB4-256 Standard Mode	
Link AB	DVI (Dual Link)
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link with IFPF)
Link F	DisplayPort/eDP, DVI (Dual Link with IFPE)
GB4-256 Split Mode AB	
Link A	DisplayPort, HDMI, DVI (Single Link or Dual Link)
Link B	DisplayPort/eDP, DVI (Single Link or Dual Link)
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link EF	Not Connected
GB4-256 Split Mode EF	
Link AB	Not Connected
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link)
Link F	DisplayPort/eDP, DVI (Single Link or Dual Link)

1. Only four independent display heads supported.

Table 10.10 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFPA_IOVDD	1.0 V ± 5%	~118 mA
IFPB_IOVDD	1.0 V ± 5%	~118 mA
IFPC_IOVDD	1.0 V ± 5%	~118 mA
IFPD_IOVDD	1.0 V ± 5%	~118 mA
IFPE_IOVDD	1.0 V ± 5%	~118 mA
IFPF_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA



STRAP2	STRAP1	STRAP0	Vendor	
0	0	0	Samsung	K4Z80325BC-HC14
0	0	1	Micron	MT61K256M32JE-14:A

Table 11.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 11.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Note: The ternary strap pins listed in the STRAP columns must be pulled to one of thr... voltage levels. "L" means Low level (GND). "M" means Middle level (0.9V). "H" means

Table 11.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

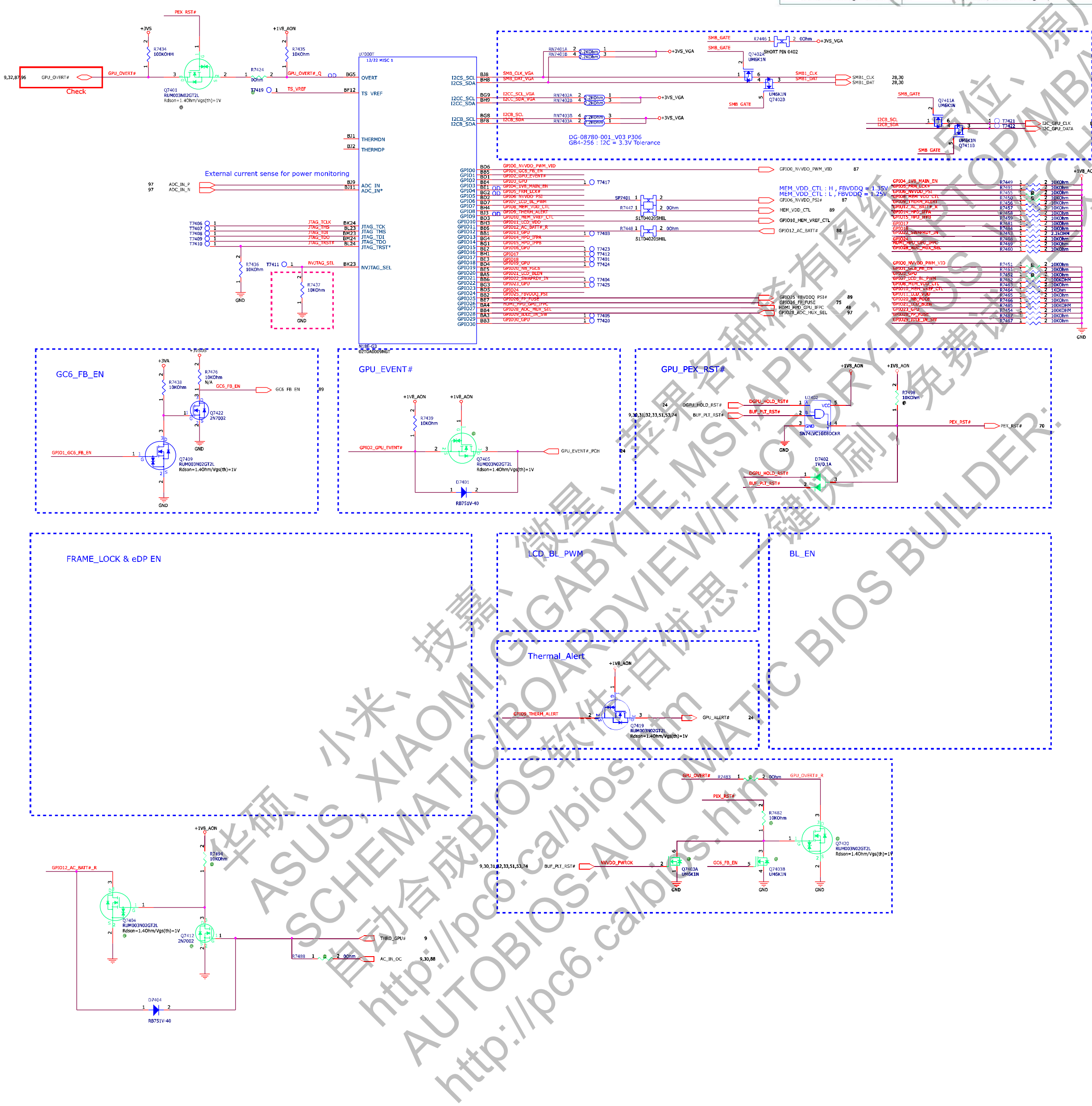
+1V8_AON	+1V8_AON	57,76,77,87,89,91
+1V8_MAIN	+1V8_MAIN	57,91
+3VSUS	+3VSUS	23,24,31,36,42,53,81,88,92,96
+3VS_VGA	+3VS_VGA	57,91,97
+3VS	+3VS	24,31,36,50,51,57,87,89,91,92,96

Table 11.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

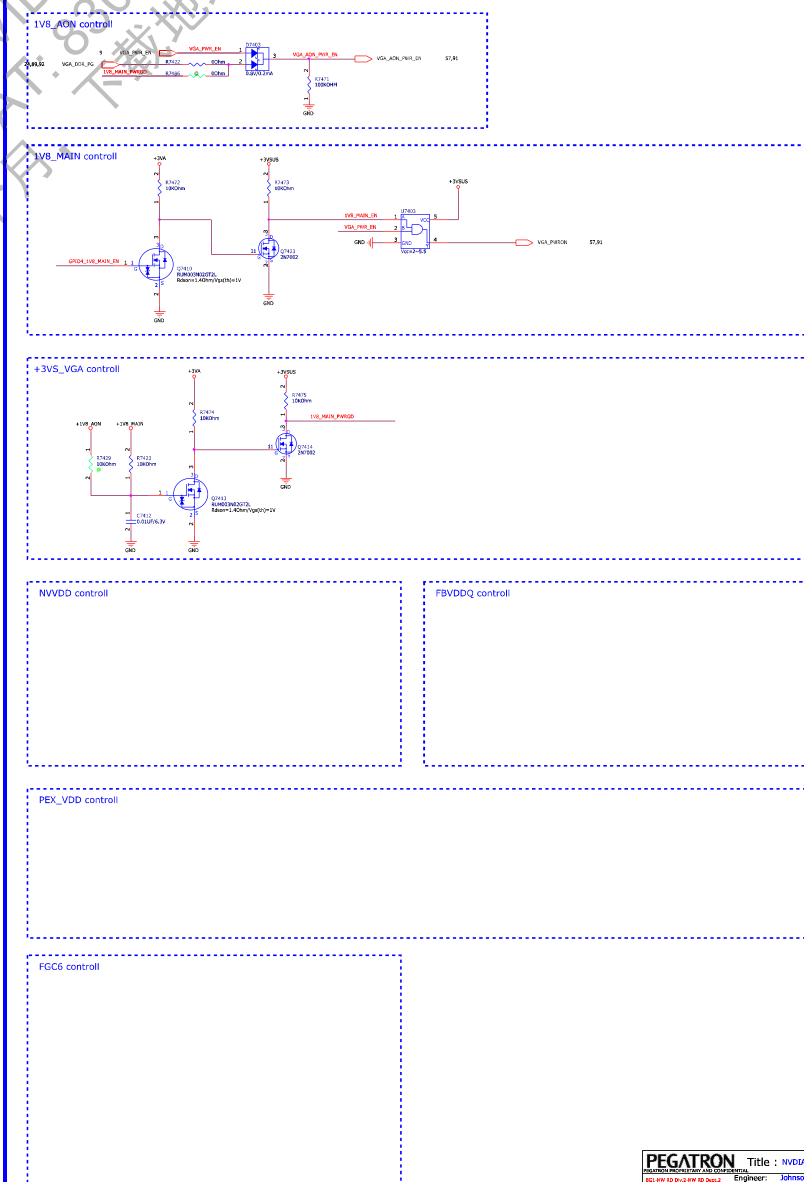
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
H	L	M	Reserved			
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	H				
M	H	M				
H	M	M				
M	M	M				

Table 11.4 FS_OVERT* Strap Enablement

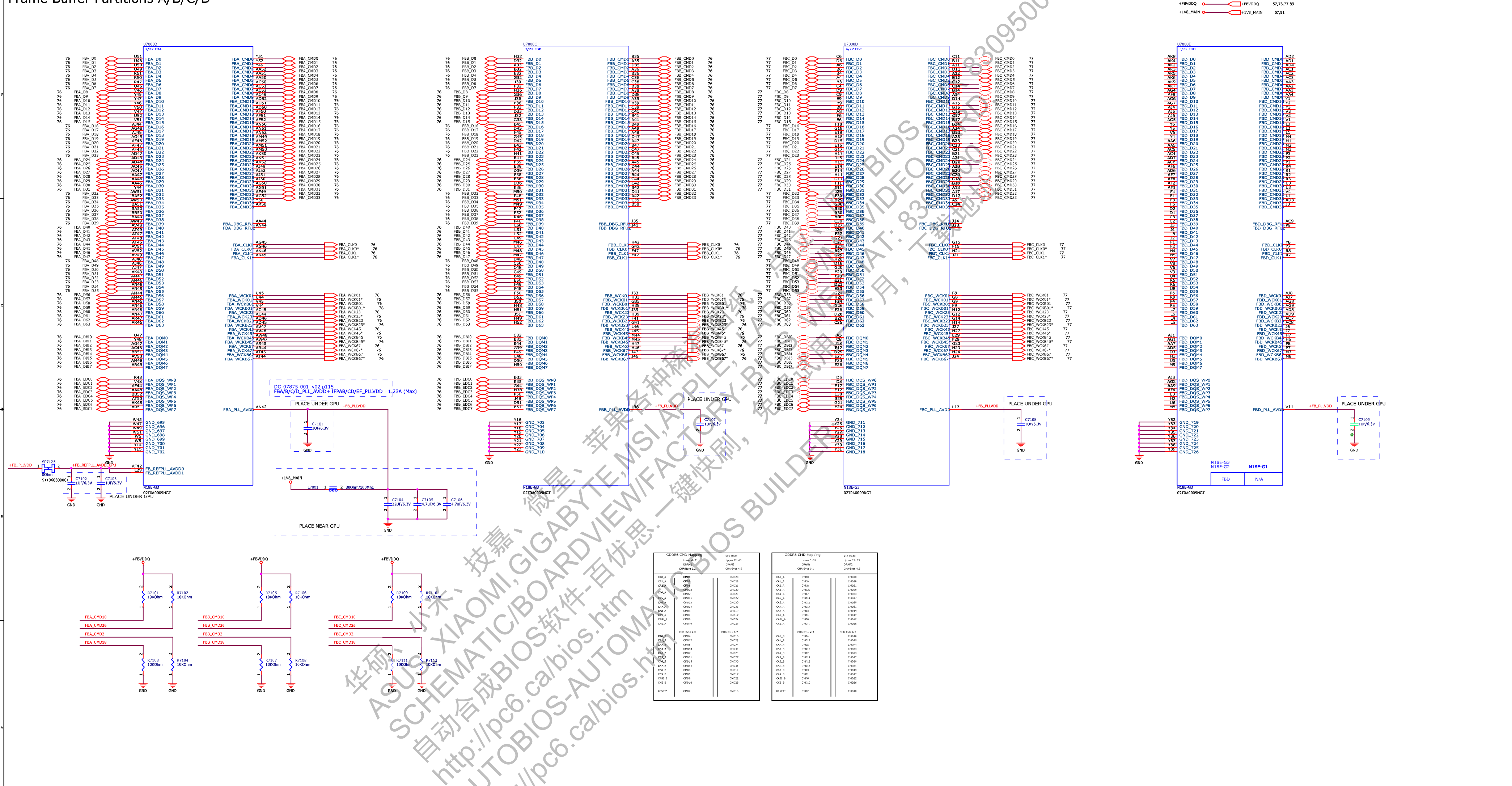
Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)



NV power sequence

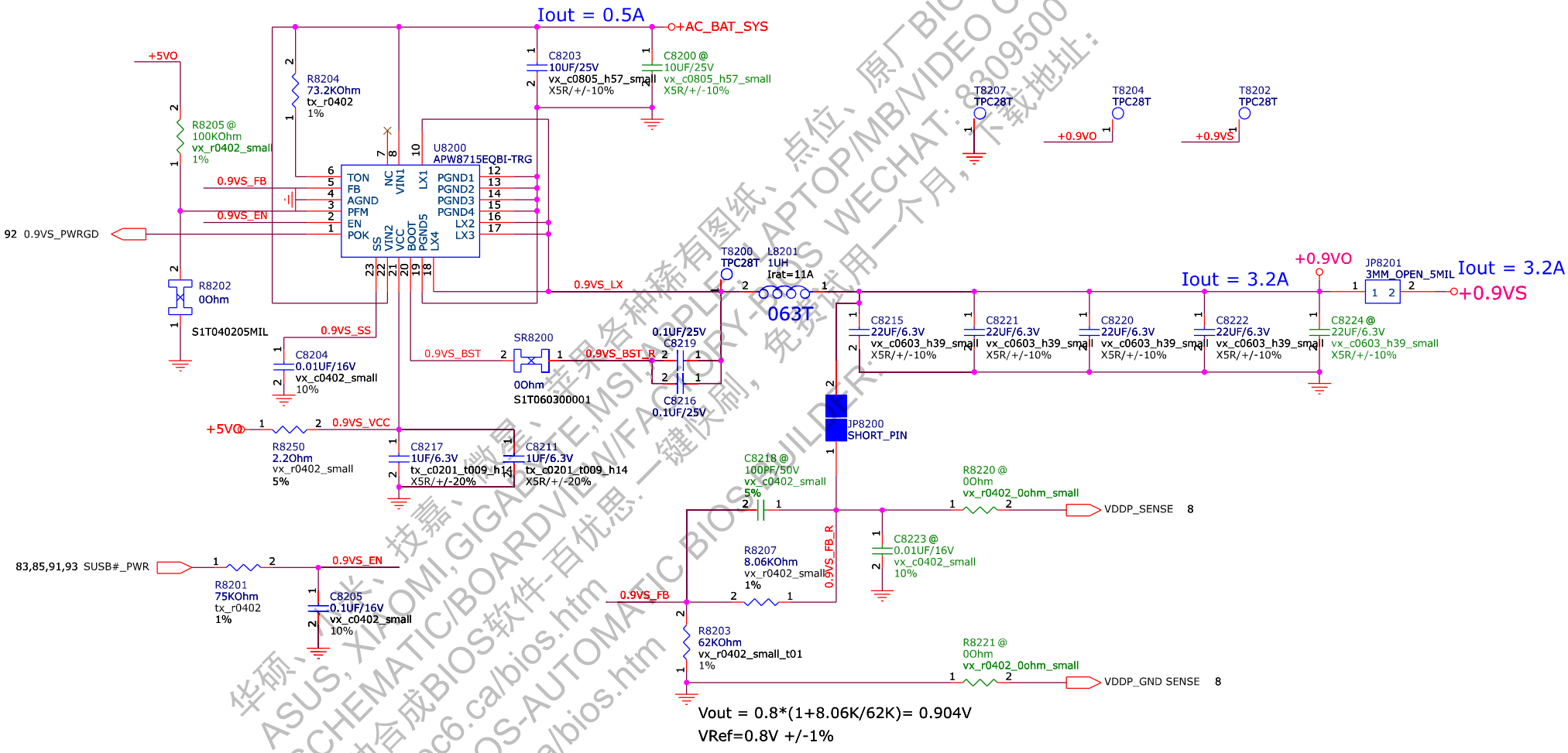


Frame Buffer Partitions A/B/C/D



PEGATRON	Title : NVDIA/BUFFERA/B		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RD Div.2-HW RD Dept.2	Engineer: Johnson Huang		
Size: Custom	Project Name: FX505DU		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet 71 of 99		

0.9VS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : +0.9VS

Engineer: Wayne_Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

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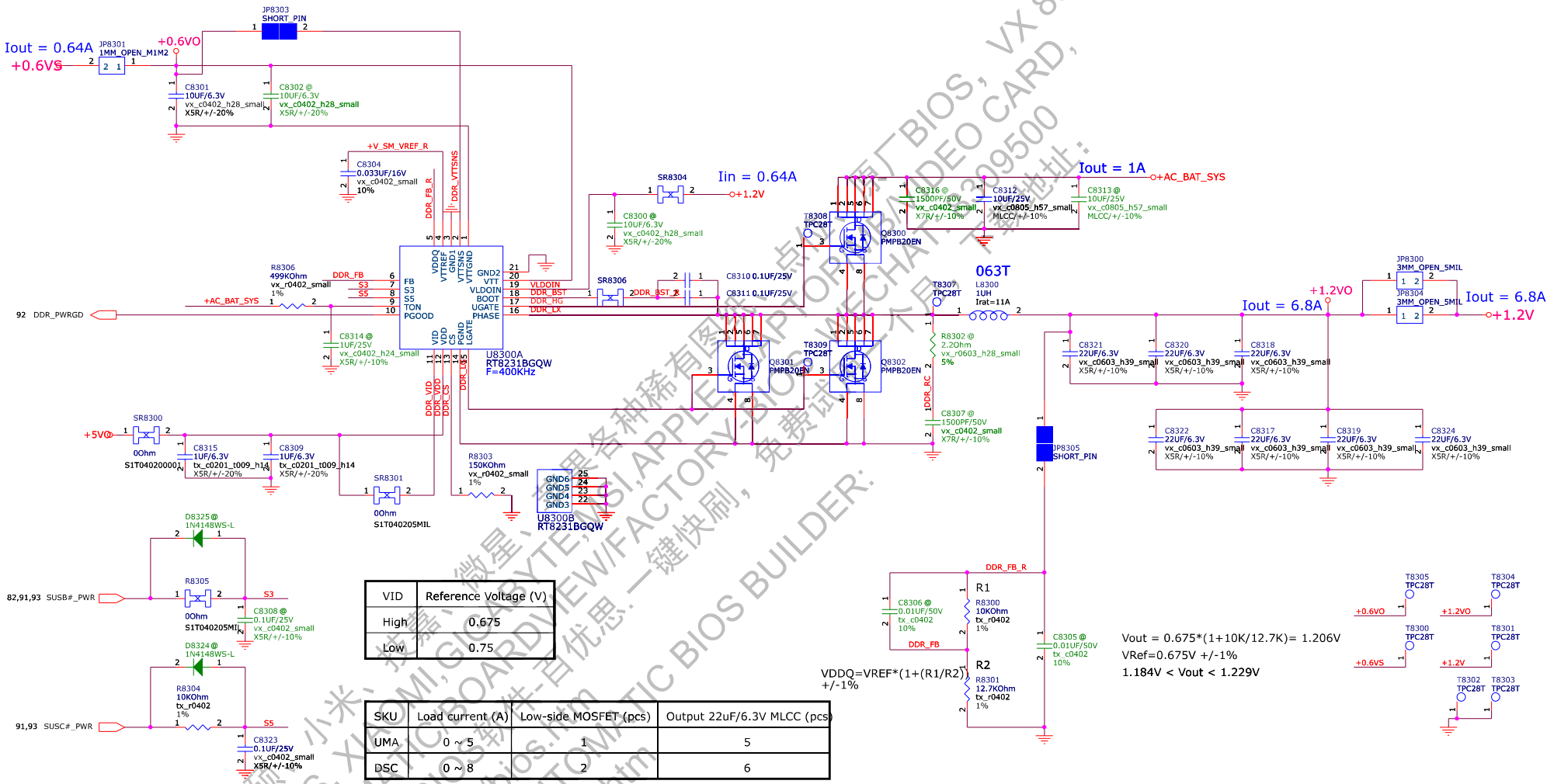
DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

<Variant Name>

PEGATRON
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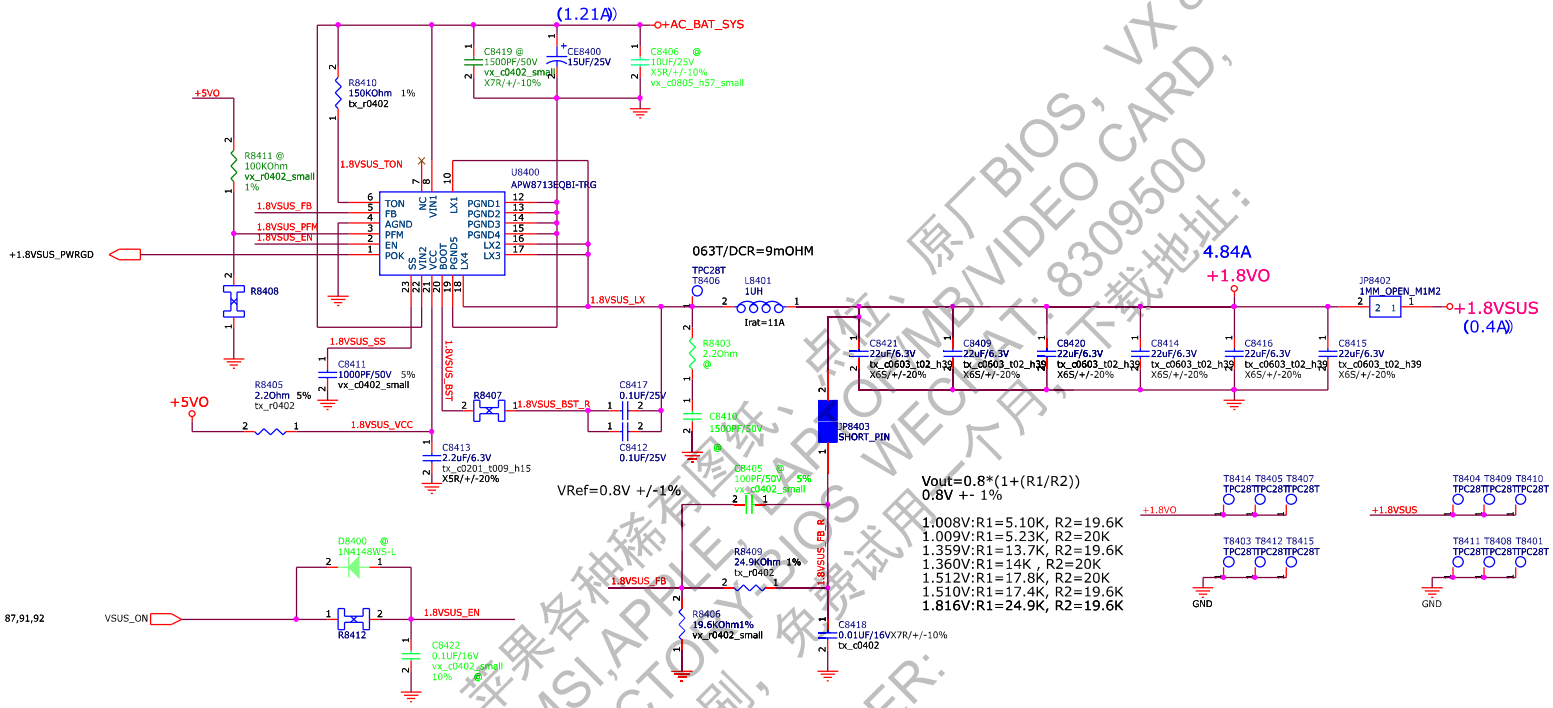
Title : POWER_DDR & VTT

Engineer: Wayne_Sung

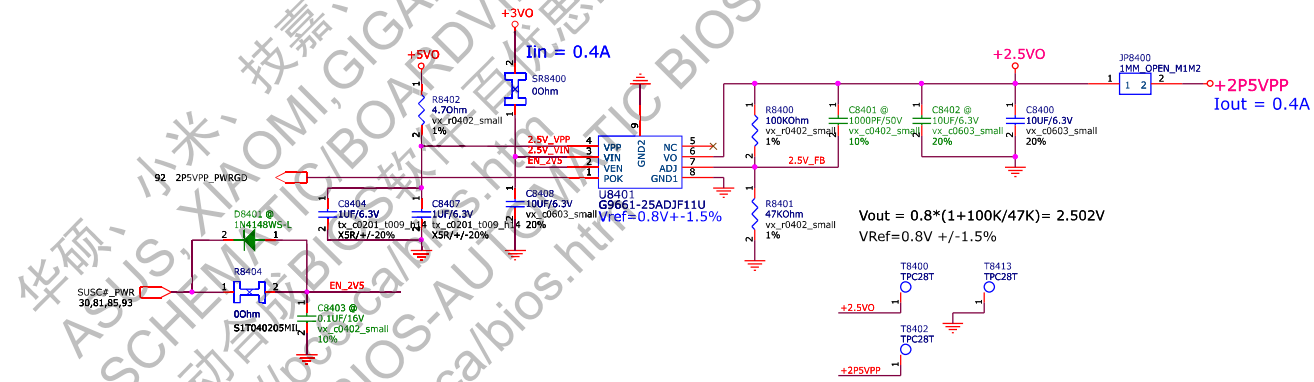
Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 83 of 97

1.8VSUS POWER SUPPLY

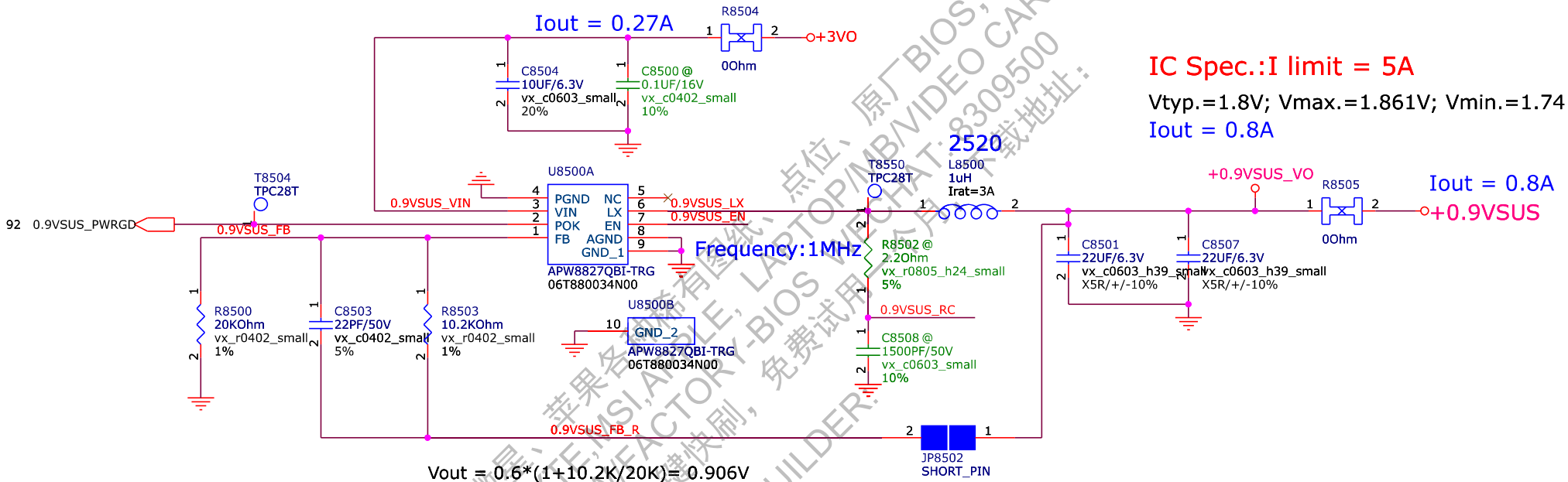


2.5VO POWER SUPPLY



PEGATRON Title : POWER_+1.8VSUS_2.5V
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp. Engineer: Wayne Sung
Size C | Project Name FX505AN | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 84 of 97

0.9VSUS POWER SUPPLY



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_0.9VSUS

Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

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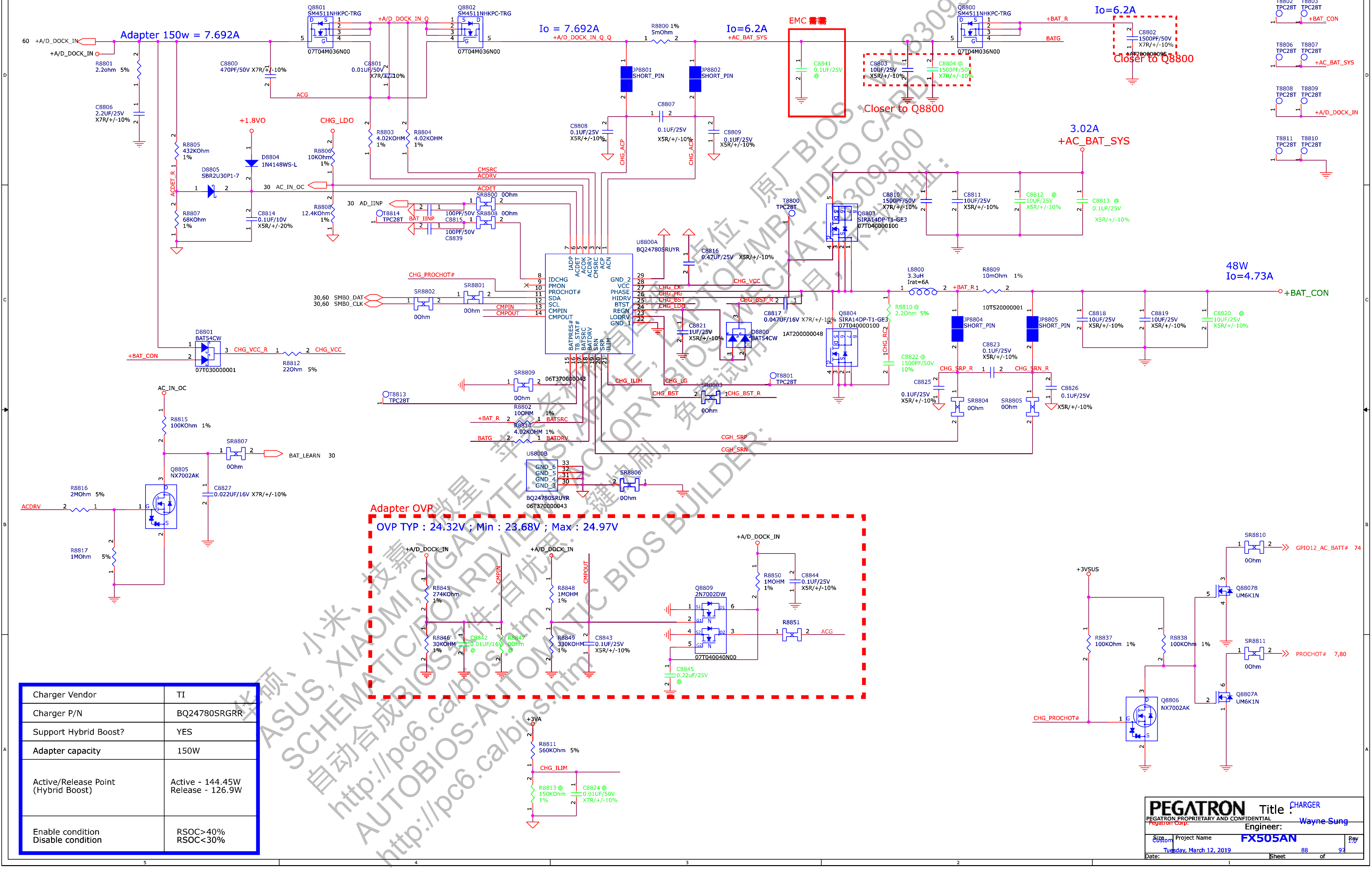
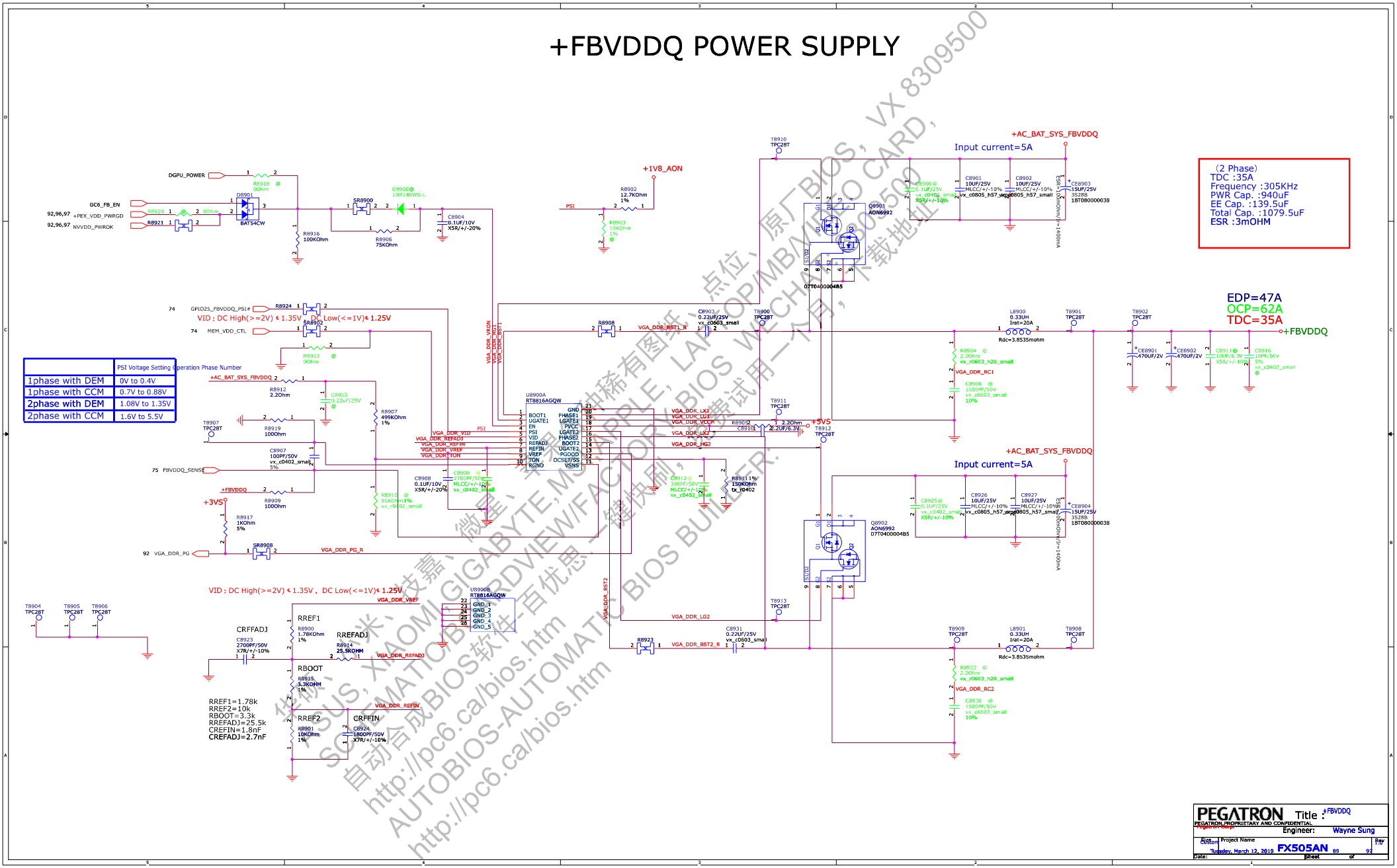
BATTERY CHARGER



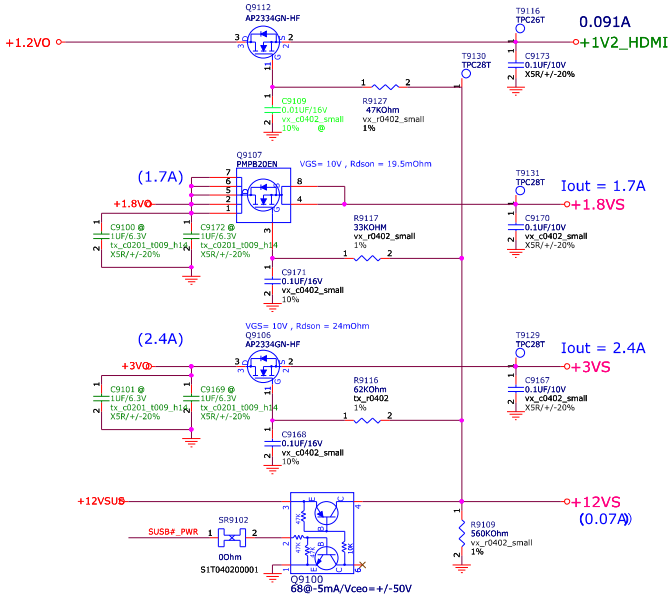
Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	150W
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W
Enable condition Disable condition	RSOC>40% RSOC<30%

PEGATRON Title : CHARGER
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.
Engineer: Wayne Sung
Size Custom Project Name FX505AN Rev 1.0
Date: Tuesday, March 12, 2019 Sheet 88 of 97

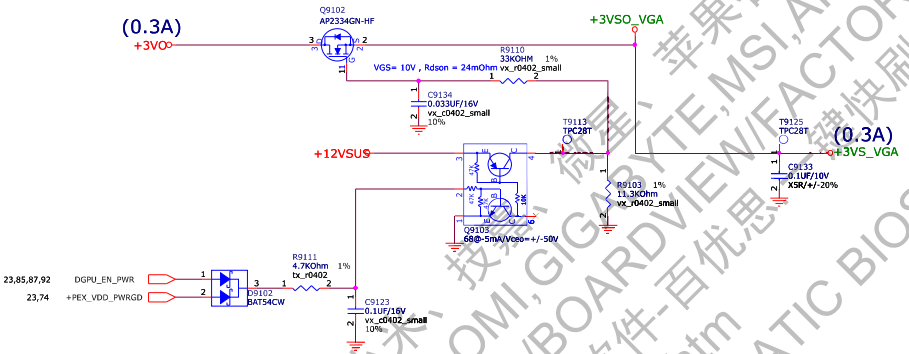
+FBVDDQ POWER SUPPLY

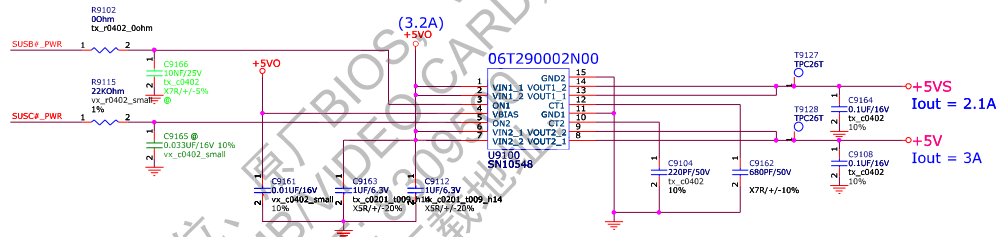


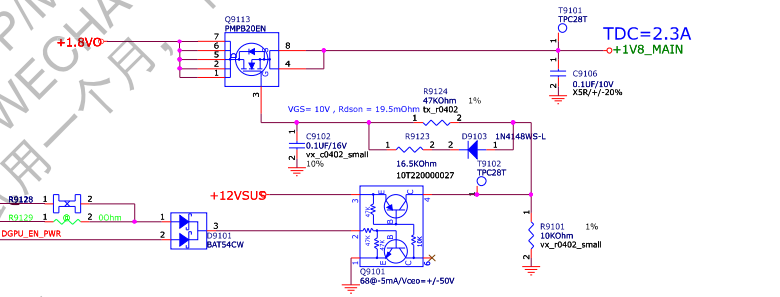
LOAD SWITCH

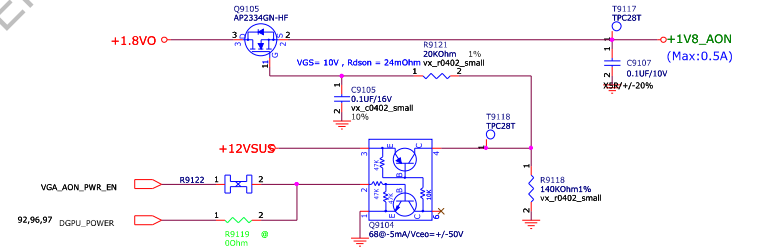


DSC_VGA_PWR POWER

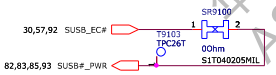




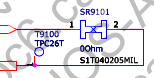




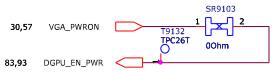
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control

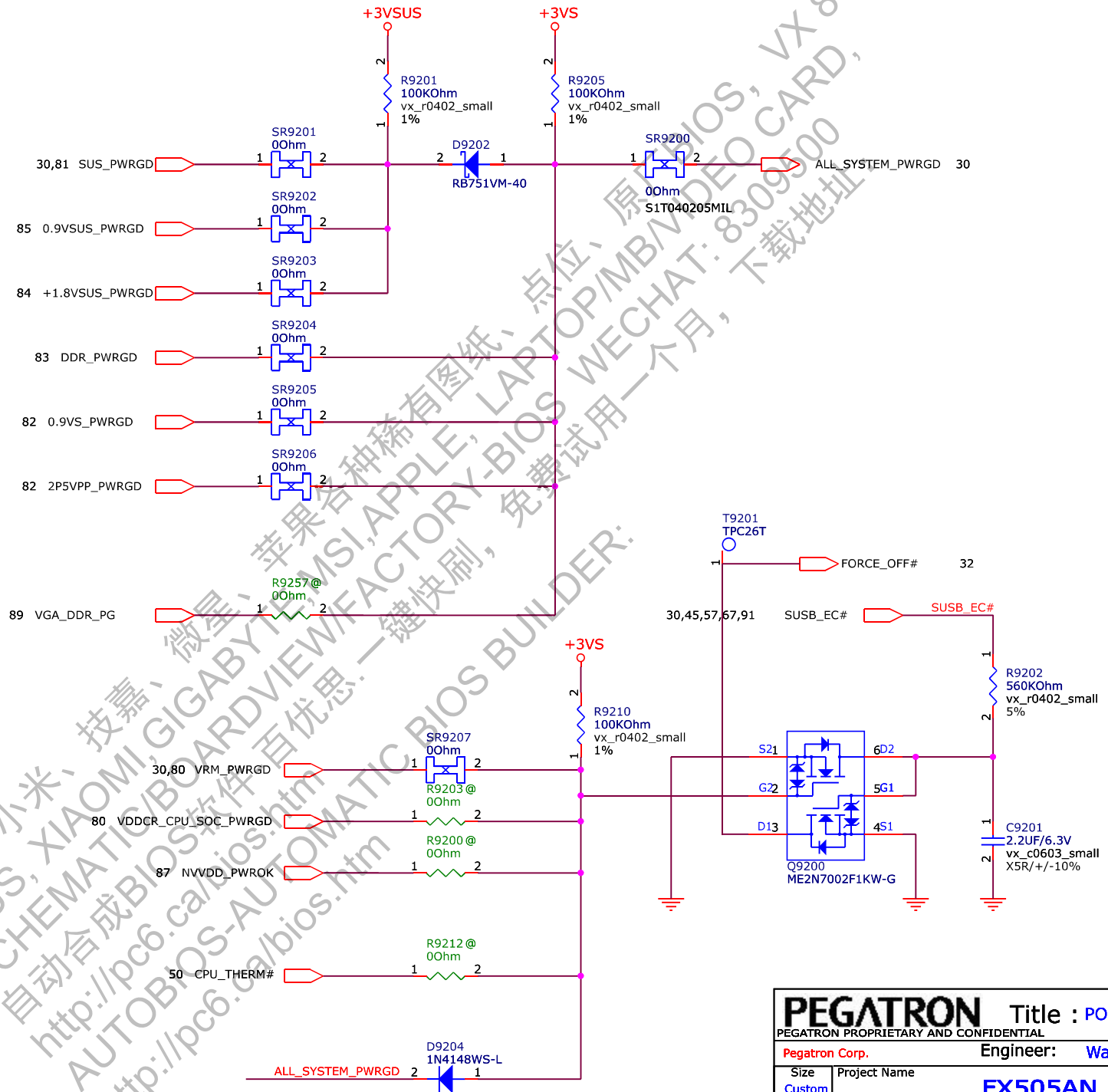


DSC_VGA_PWR POWER Control



PEGATRON Title : POWER_LOAD SWITCH
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp. Engineer: Wayne Sung
Size A2 | Project Name FX505AN | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 91 of 97

POWER GOOD DETECTER



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Pegatron Corp. Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 92 of 97

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,88,89

+BAT_CON → +BAT_CON 60,88

+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 56,66,81

+3VA → +3VA 11,28,30,56,57,60,66,81,88

+5VO → +5VO 81,83,85,89,91

+3VO → +3VO 81,84,85,89,91

+2.5VO → +2.5VO 83

+1.8VO → +1.8VO 84,85,91

+1.8VO_VGA → +1.8VO_VGA 83

+1.2VO → +1.2VO 83

+0.9VO → +0.9VO 83

+0.9VSUS_VO → +0.9VSUS_VO83

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91

+5VSUS → +5VSUS 52,66,81

+3VSUS → +3VSUS 8,9,11,12,28,30,31,36,51,81,92

+1.8VSUS → +1.8VSUS 9,11,28,80,84,89

+0.9VSUS → +0.9VSUS 83

+12VS → +12VS 28,31,48,91

+5VS → +5VS 30,31,36,48,50,51,56,57,61,80,91

+3VS → +3VS 8,9,10,11,12,16,17,28,30,31,36,37,40,45,48,50,51,53,56,57,61,62,64,66,91,92

+1.8VS → +1.8VS 8,9,11,28,31,44,48,57,80,89,91

+0.6VS → +0.6VS 16,17,57,83

+3V → +3V 31,44,57,64,66,91

+1.2V → +1.2V 7,11,16,17,57,83

+2P5VPP → +2P5VPP 83

+1.8VS_VGA → +1.8VS_VGA 83

+1.35VS_VGA → +1.35VS_VGA 83

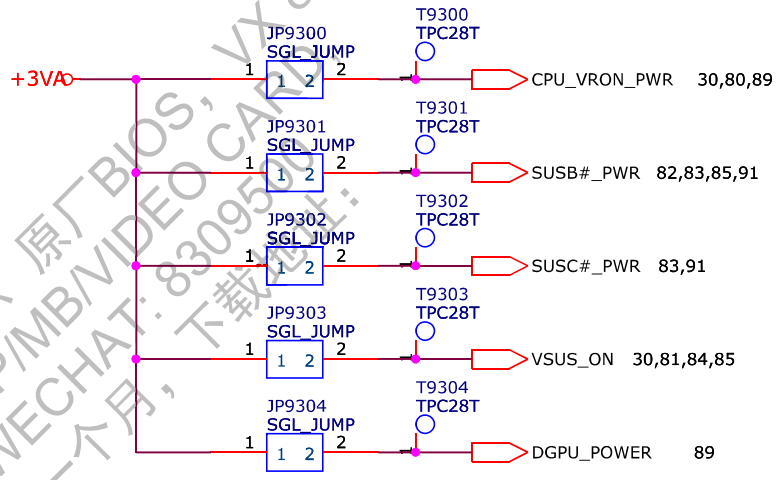
+VDDCI_VGA → +VDDCI_VGA 11,80,89

+VDDC_VGA → +VDDC_VGA 11,80,89

+VDDCR_CPU_SOC → +VDDCR_CPU_SOC 11,80

+VDDCR_CPU → +VDDCR_CPU 11,80

FOR POWER TEST



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

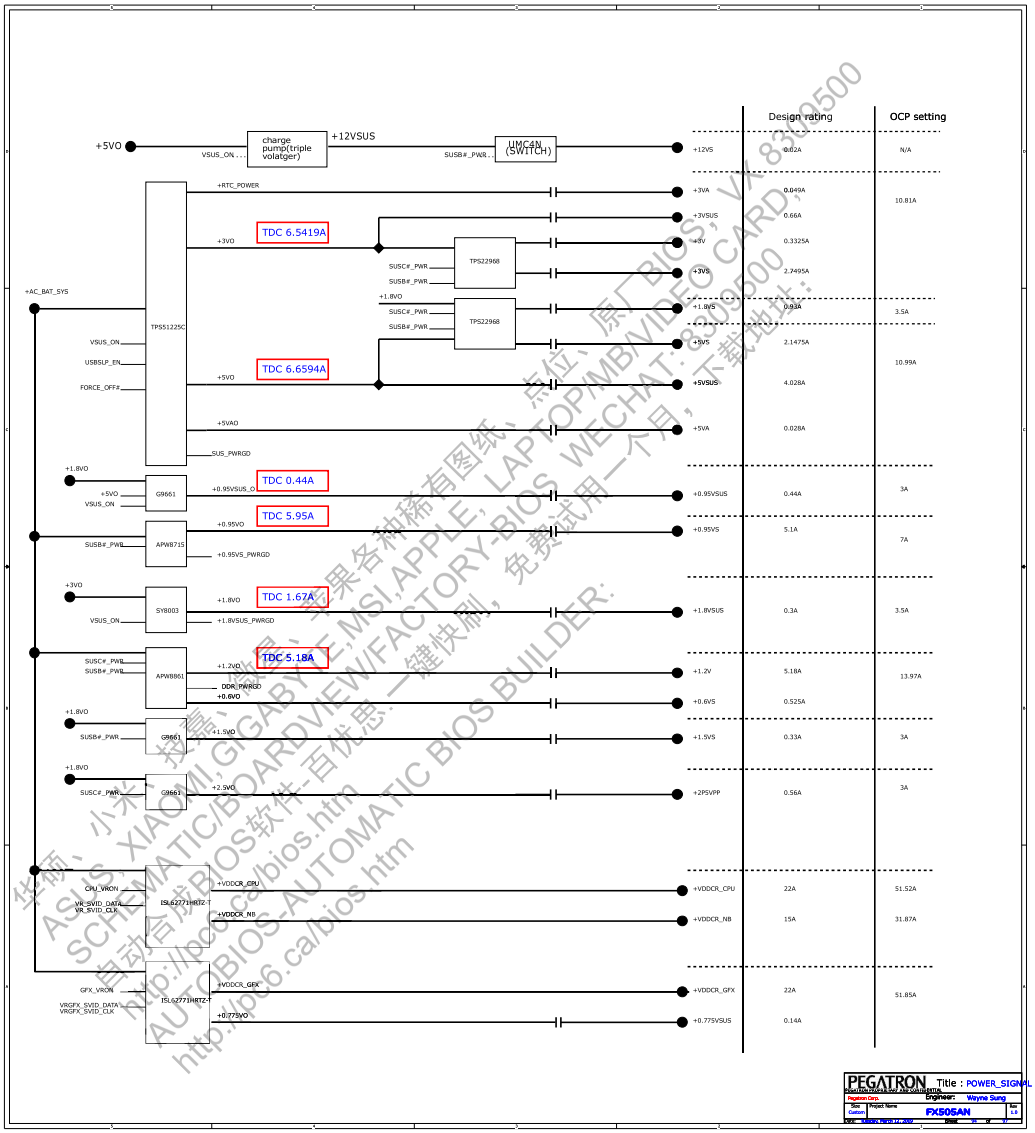
Title : POWER_SIGNAL

Pegatron Corp.

Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 93 of 97


+5VO
charge pump(triple volatger)
+12VSUS
VSUS_ON
SUSB#_PWR
UMC4N (SWITCH)
Design rating
OCP setting
+12VS
0.62A
N/A
+RTC_POWER
+3VA
0.049A
+3VSUS
0.66A
10.81A
+3VO
TDC 6.5419A
+3V
0.3325A
SUSC#_PWR
SUSB#_PWR
TPS22968
+3VS
2.7495A
+1.8VO
+1.8VS
0.03A
3.5A
+AC_BAT_SYS
TPS51225C
VSUS_ON
USBSLP_EN
FORCE_OFF#
+5VO
TDC 6.6594A
+5VS
2.1475A
10.99A
+5VSUS
4.028A
+5VAO
+5VA
0.028A
SUS_PWRGD
+1.8VO
+5VO
VSUS_ON
G9661
+0.95VSUS_O
TDC 0.44A
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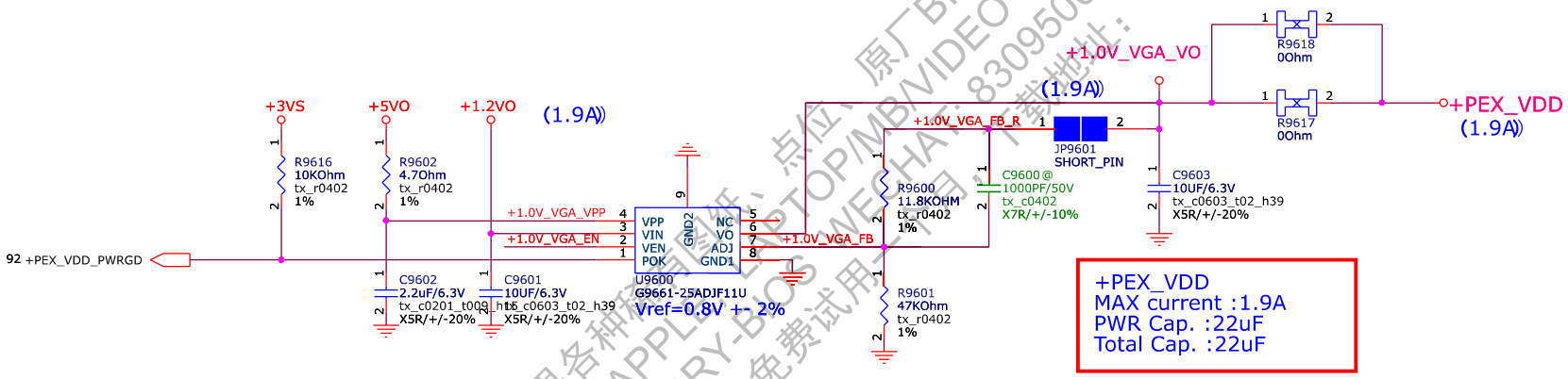
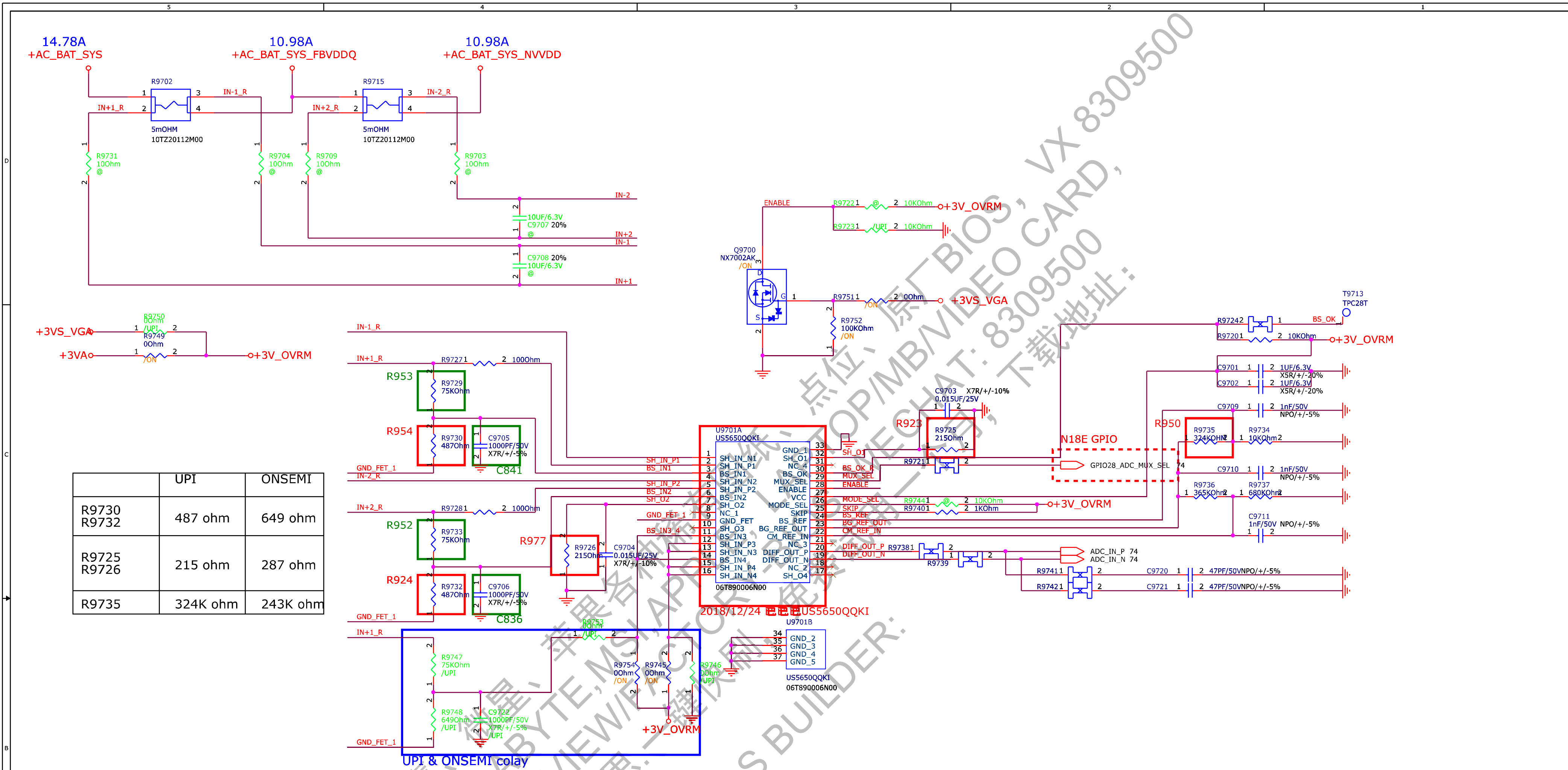
3A
TDC 5.95A
+0.95VO
+0.95VS
5.1A
7A
SUSB#_PWR
APW8715
+0.95VS_PWRGD
+3VO
+1.8VO
TDC 1.67A
+1.8VSUS
0.3A
3.5A
VSUS_ON
SY8003
+1.8VSUS_PWRGD
SUSC#_PWR
SUSB#_PWR
TDC 5.18A
+1.2V
5.18A
13.97A
APW8861
DDR_PWRGD
+0.6VO
+0.6VS
0.525A
+1.8VO
SUSB#_PWR
G9661
+1.5VO
+1.5VS
0.33A
3A
+1.8VO
SUSC#_PWR
G9661
+2.5VO
+2PSVPP
0.56A
3A
CPU_VRON
VR_SVID_DATA
VR_SVID_CLK
ISL62771HRTZ-T
+VDDCR_CPU
+VDDCR_CPU
22A
51.52A
+VDDCR_NB
+VDDCR_NB
15A
31.87A
GFX_VRON
VRGFX_SVID_DATA
VRGFX_SVID_CLK
ISL62771HRTZ-T
+VDDCR_GFX
+VDDCR_GFX
22A
51.85A
+0.775VO
+0.775VSUS
0.14A
PEGATRON
Title : POWER_SIGNAL
Engineer: Wayne Sung
Project Name
FX505AN

+PEX_VDD POWER SUPPLY



PEGATRON	Title :	+PEX_VDD	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer:	Wayne Sung	
Pegatron Corp.			
Size: B	Project Name: FX505AN		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet: 96	of: 97	



	UPI	ONSEMI
R9730 R9732	487 ohm	649 ohm
R9725 R9726	215 ohm	287 ohm
R9735	324K ohm	243K ohm

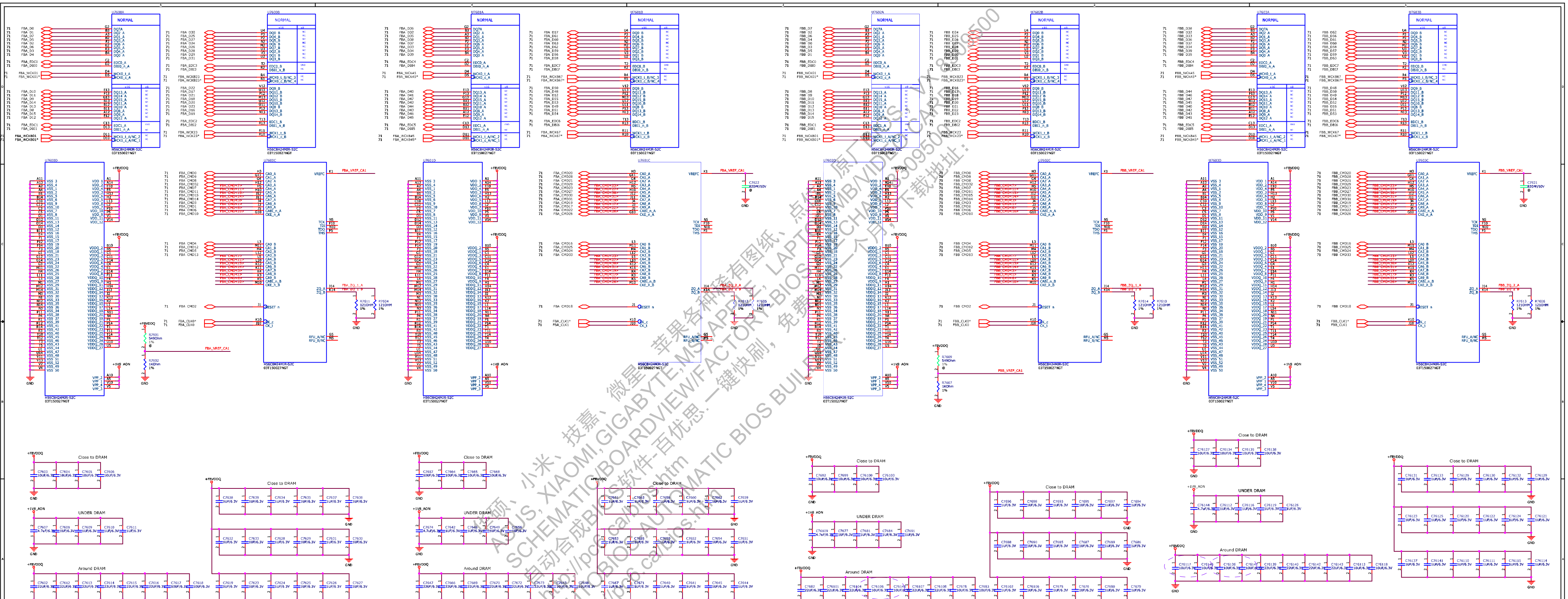
Table 13. Power Monitoring with OnSemi OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
115W to 130W	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
100W to 110W	649 Ω	221 Ω	243 kΩ	75 kΩ	1.0 nF
75W to 90W	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
70W or lower	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

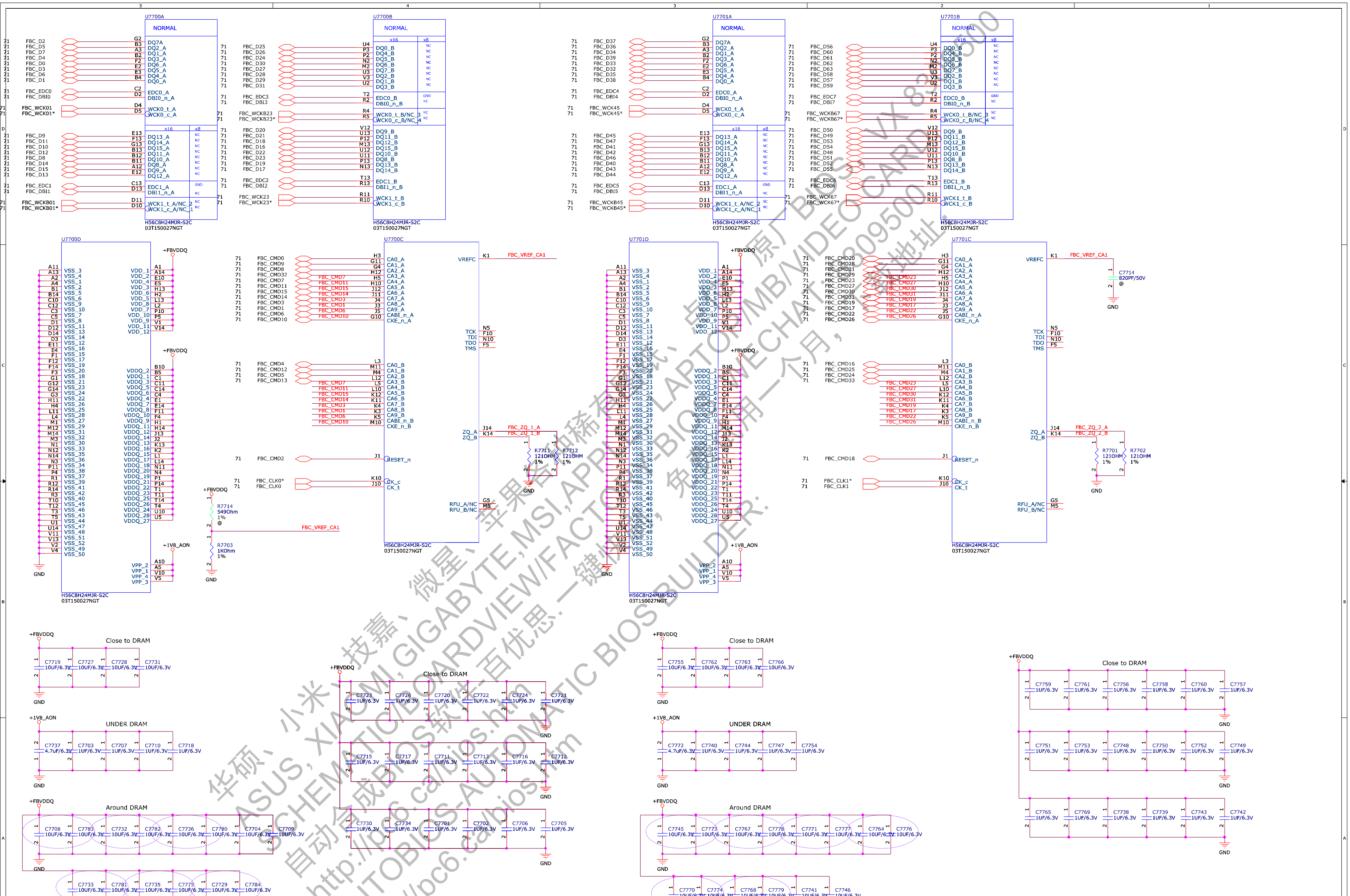
Table 14. Power Monitoring with uPI OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	487 Ω	127 Ω	324 kΩ	75 kΩ	1.0 nF
115W to130W	487 Ω	143 Ω	324 kΩ	75 kΩ	1.0 nF
100W to 110W	487 Ω	165 Ω	324 kΩ	75 kΩ	1.0 nF
75W to 90W	487 Ω	215 Ω	324 kΩ	75 kΩ	1.0 nF
70W or lower	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.
Title : +NVVDDS
Engineer: Wayne Sung
Size C | Project Name FX505AN | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 97 of 97



PEGATRON	Title : GDDR6 256M X32bit_A		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RD Div.2-HW RD Dept.2	Engineer: Johnson Huang		
Size: Custom	Project Name: FX505DU		Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet 76 of 99		



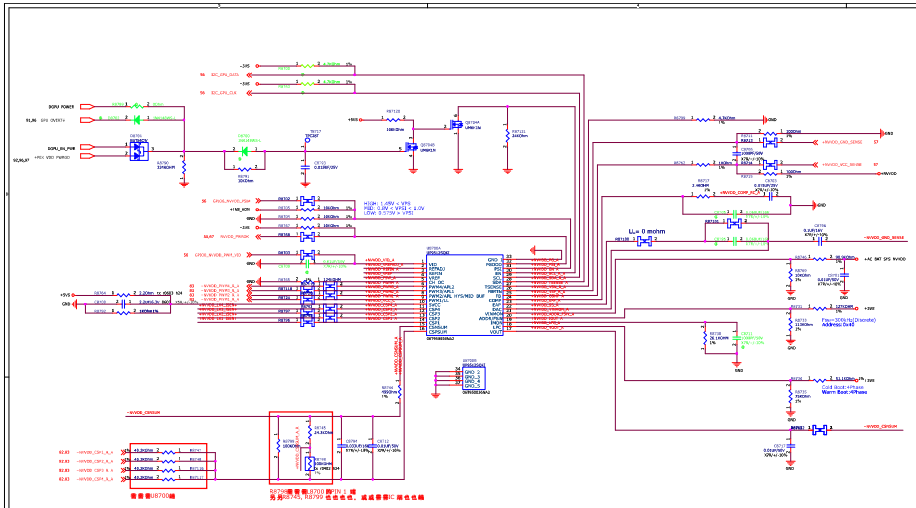
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: GDDR6 256M X32bit_C

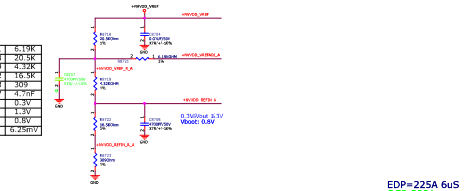
BG1-HW RD Div.2-HW RD Dept.2 — Engineer: Johnson Huang

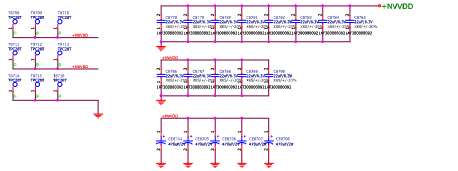
Size: Custom | Project Name: FX505DU | Rev: 1.0

Date: Tuesday, March 12, 2019 | Sheet 77 of 99

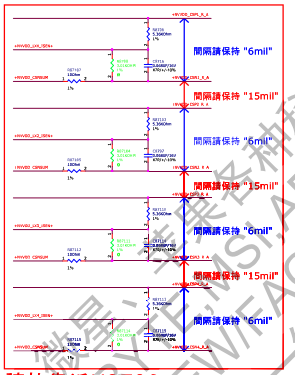


R8721	6.19K
R8718	20.5K
R8719	4.32K
R8722	16.5K
R8723	309
C8707	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

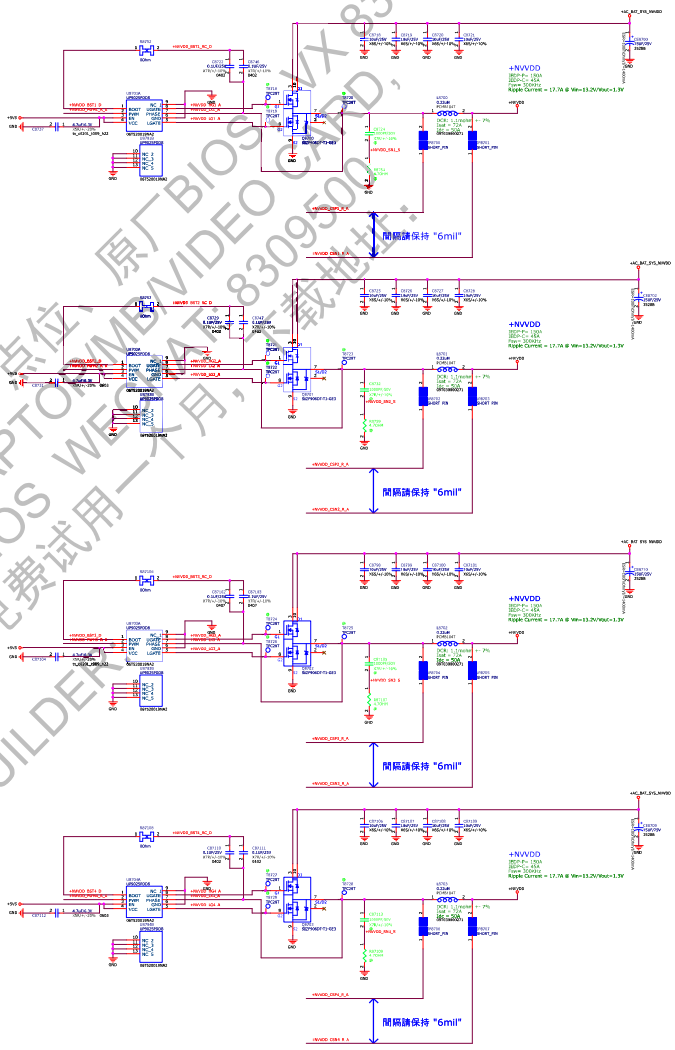


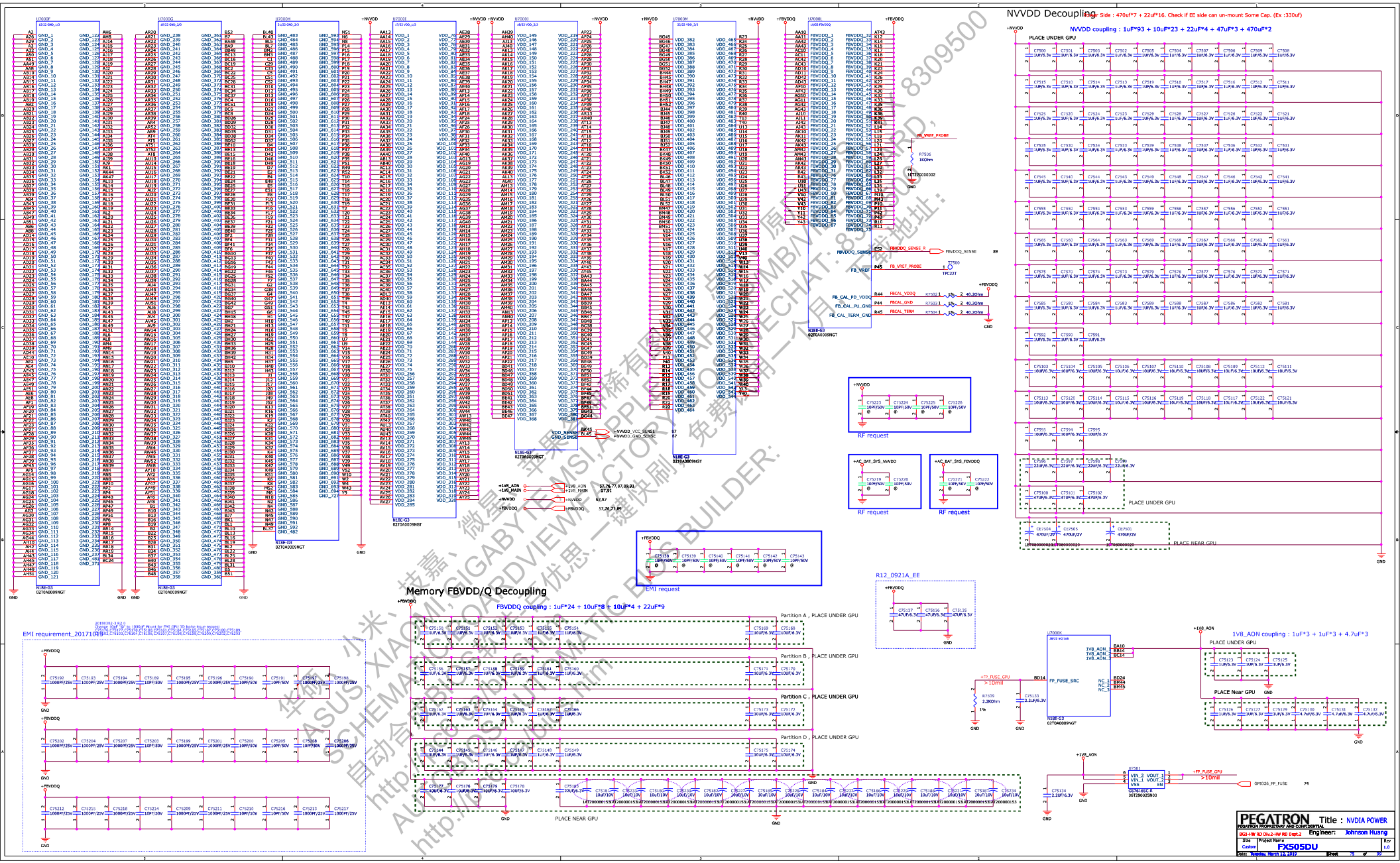


EDP=225A 6uS
OCP:20A
TDC=80A



請放靠近U8700




NVVDD Decoupling
NVVDD coupling : 1uF*93 + 10uF*23 + 22uF*4 + 47uF*3 + 470uF*2
PLACE UNDER GPU
Memory FBVDD/Q Decoupling
FBVDDQ coupling : 1uF*24 + 10uF*8 + 10uF*4 + 22uF*9
Partition A , PLACE UNDER GPU
Partition B , PLACE UNDER GPU
Partition C , PLACE UNDER GPU
Partition D , PLACE UNDER GPU
PLACE NEAR GPU
EMI requirement_20171019
EMI request
RF request
1V8_AON coupling : 1uF*3 + 1uF*3 + 4.7uF*3
PLACE Near GPU
PEGATRON
Title : NVDIA POWER
Engineer: Johnson Huang
Project Name
FX505DU
Rev 1.0
Tuesday, March 13, 2018