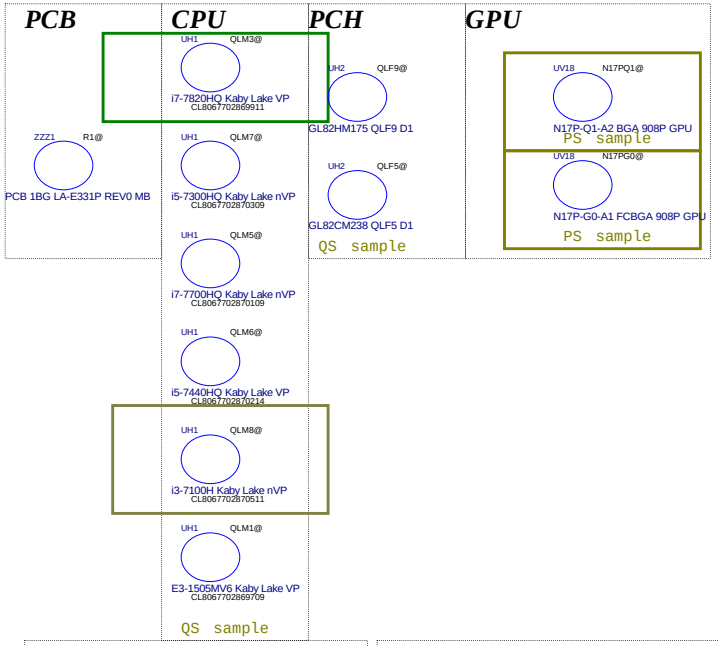
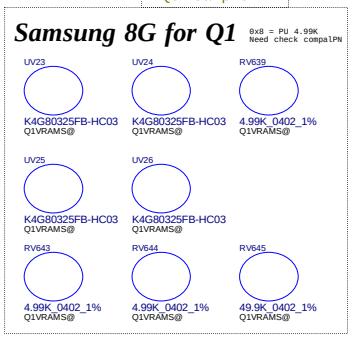
MODEL NAME : CAM00
CAM01

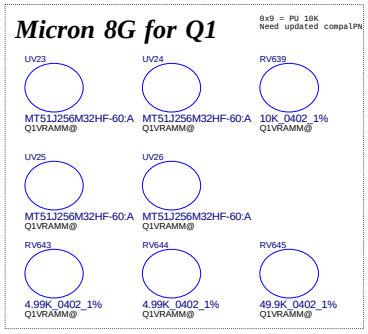
PCB NO : LA-E331P

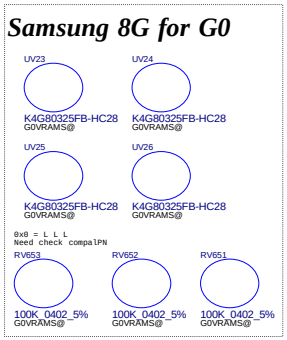
BOM P/N :

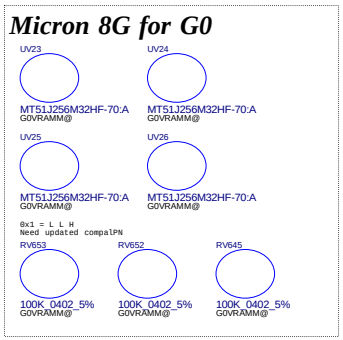
Dell/Compal Confidential

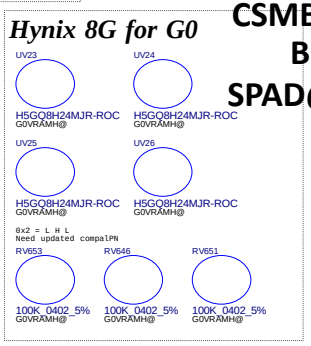












Schematic Document

Berlinetta MLK (KABY LAKE-H)

2016-10-26

Rev: 1.0 (A00)

@ : Nopop Component

@SPAD@ : Nopop Component 0 Ohm Short-PAD

XDP@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

TPM@ : TPM funct i on

EMC@ : Pop of EMI parts

Q1VRAMS@ : Samsung GDDR5 for Q1-GPU

Q1VRAMM@ : Micron GDDR5 for Q1-GPU

G0VRAMS@ : Samsung GDDR5 for G0-GPU

G0VRAMM@ : Micron GDDR5 for G0-GPU

G0VRAMH@ : Hynix GDDR5 for G0-GPU

BreakDown@ : for measure power consumpt i on

Q1@ : GPU N16PQ1 & N17PQ1

G0@ : GPU N17PG0

UMA@ / DIS@ : UMA/DIS

CSMB@ :G0

BC@ : Q1

SPAD@ : Nopop Component 0 Ohm Short-PAD for NPI test require

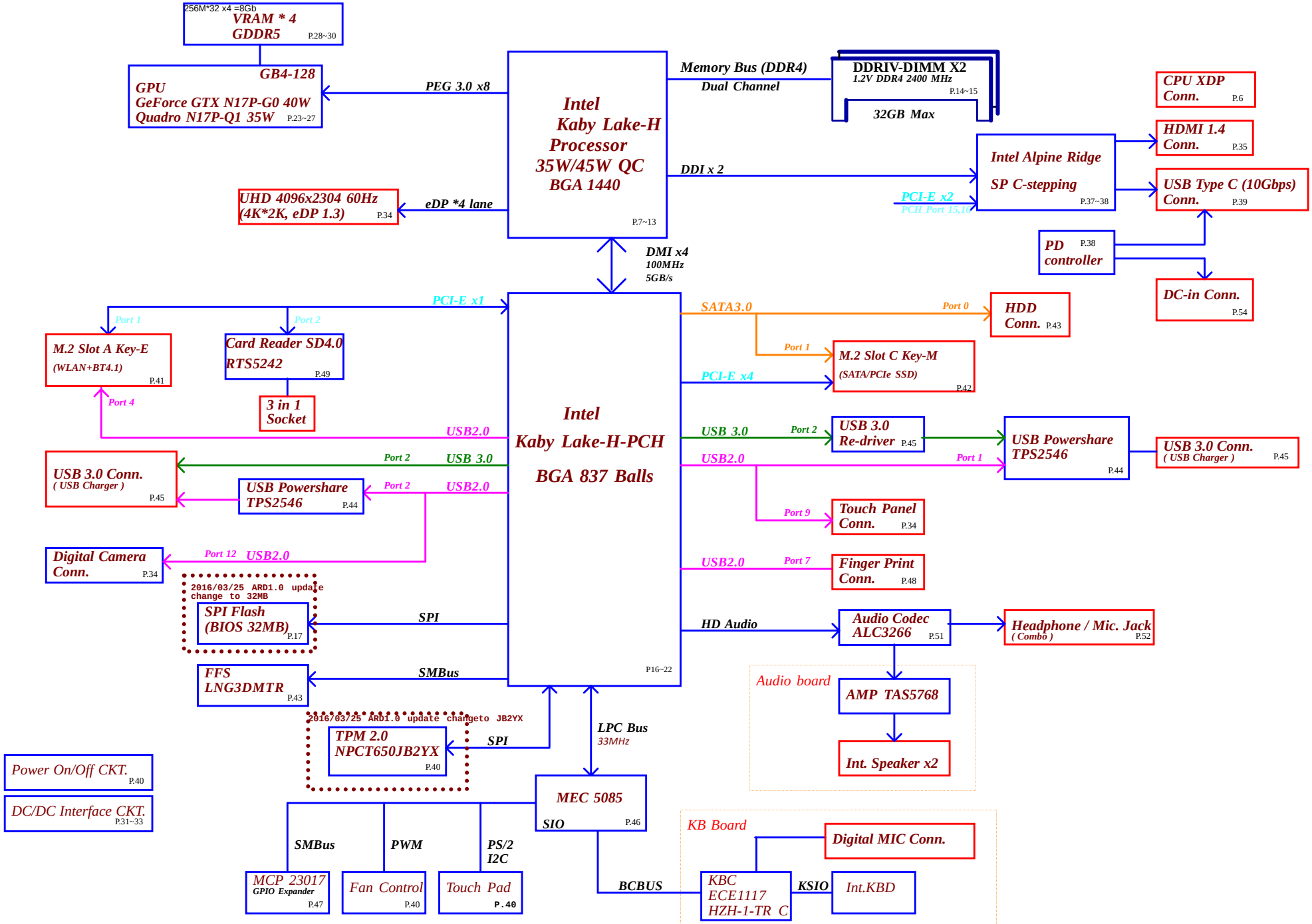
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: Cover Page

Size | Document Number: LA-E331P | Rev: 0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 1 of 75

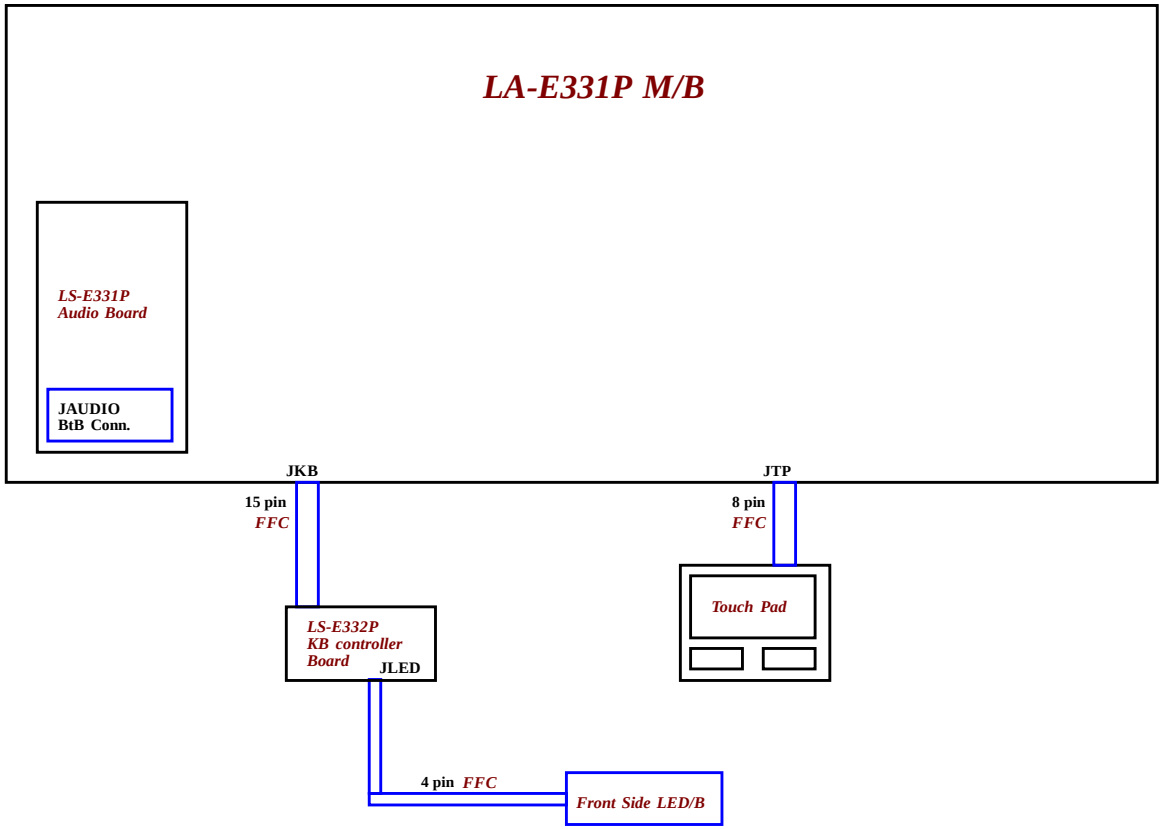


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: LA-E331P		Rev: 0.1(000)
Date: Wednesday, October 26, 2016	Sheet 2 of 75		

Compal Confidential

Project Code : CAM00
File Name :



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DB block diagram**

Size	Document Number	Rev
		0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 3 of 75

Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION
Lane 1	NGFF-1 WLAN + BT
Lane 2	CARD READER
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	Alpine Ridge
Lane 16	Alpine Ridge

USB3	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0A	SSD
1A	N/A
N/A	N/A
N/A	N/A
0B	None
1B	HDD
2	None
3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Symbol Note :

: means Digital Ground : means Analog Ground

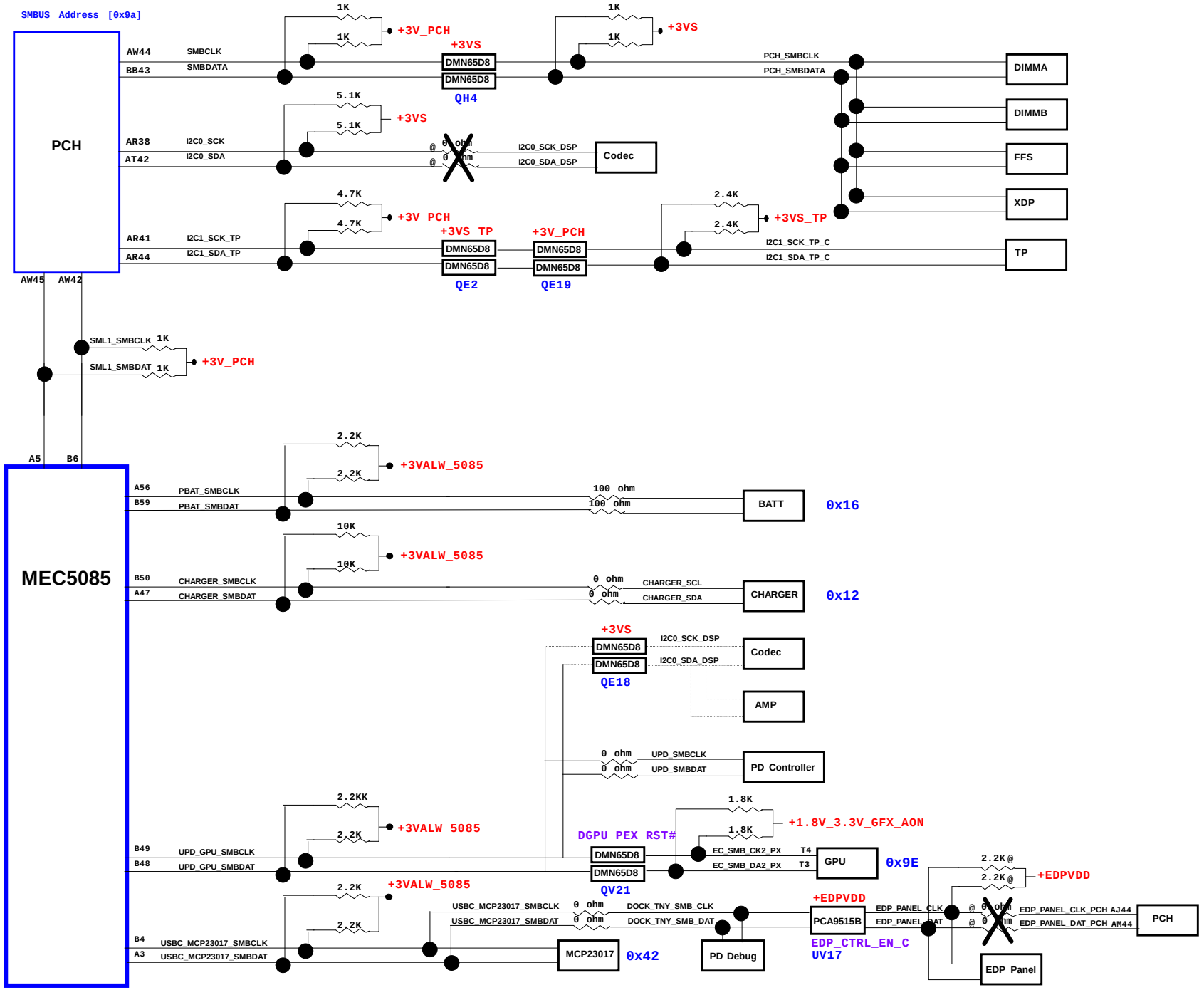
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 4 of 75



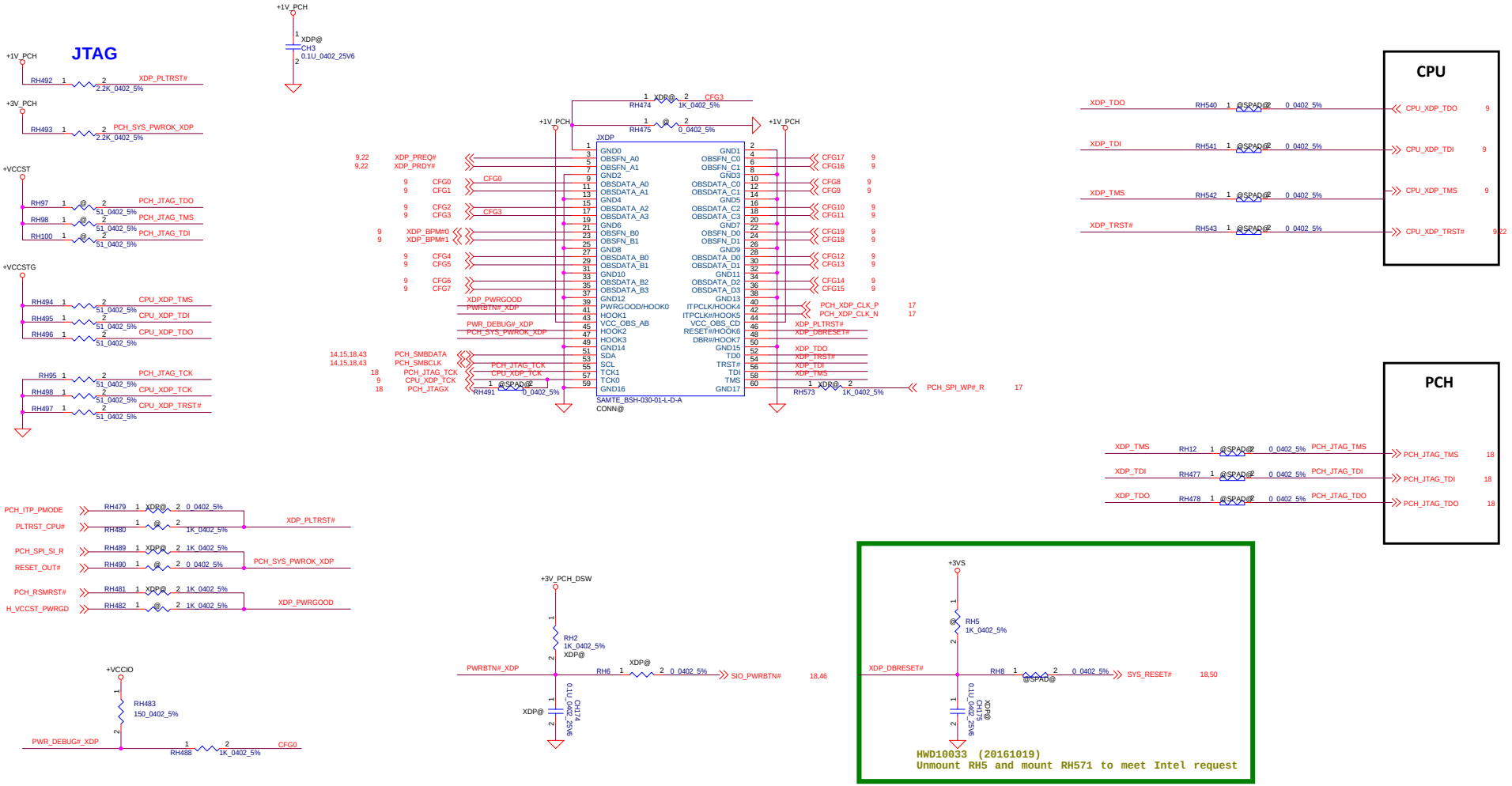
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
Custom		0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 5 of 75



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **XDP CONN**

Size	Document Number	Rev
		0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 6 of 75

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

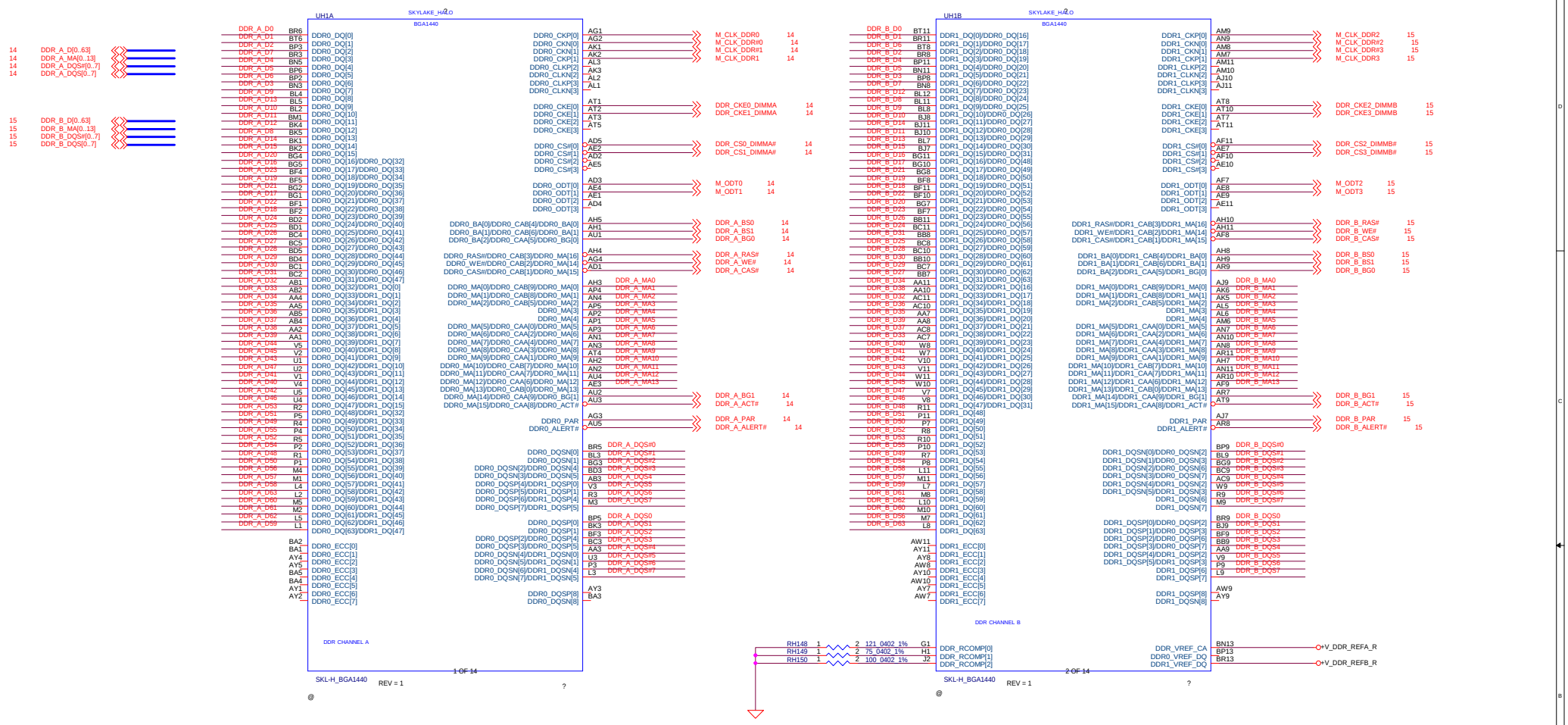
Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
C		0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 7 of 75

Interleave



Security Classification	Compal Secret Data
Issued Date	2011/08/25
Deciphered Date	2012/07/25

Title: **PROCESSOR(3/7) DDRIII**

Size	Document Number	Rev
C		0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 8 of 75

CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

CFG0 — RH183 1K_0402_5%

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG2 — RH184 1K_0402_5%

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 — RH185 1K_0402_5%

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5 — RH186 1K_0402_5%
CFG6 — RH187 1K_0402_5%

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG7 — RH188 1K_0402_5%

+VCCST

H_THERMTRIP#_R — RH163 1K_0402_5%
XDP_PREQ# — RH156 51_0402_5%
H_VCCST_PWRGD — RH164 1K_0402_5%
VR_SVID_DATA — RH151 100_0402_5%
VR_SVID_ALERT# — RH152 56.2_0402_1%
H_CATERR# — RH570 49.9_0402_1%

+VCCSTG

H_PROCHOT# — RH165 1K_0402_5%

UH1E SKYLAKE_H2 BGA1440

BCLKP / BCLKN ← PCH_CPU_BCLK_P / PCH_CPU_BCLK_N
PCI_BCLKP / PCI_BCLKN ← PCH_CPU_PCIBCLK_P / PCH_CPU_PCIBCLK_N
CLK24P / CLK24N ← CPU_24MHZ_P / CPU_24MHZ_N
VIDALERT# ← VR_SVID_ALERT#_R (RH153 220_0402_5%)
VIDSCK ← VR_SVID_CLK
VIDSOUT ← VR_SVID_DATA
PROCHOT# ← H_PROCHOT#_R (RH158 499_0402_1%)
DDR_VTT_CNTL ← DDR_VTT_PG_CTRL
VCCST_PWRGD ← VCCST_PWRGD_CPU (RH154 60.4_0402_1%)
PROCPWRGD ← PLTRST_CPU#
RESET# ← H_PM_SYNC_R
PM_SYNC ← H_PM_DOWN_R
PM_DOWN ← H_PM_DOWN (RH155 20_0402_5%, RH190 0_0402_5%)
PECI ← H_PECI
THERMTRIP# ← H_THERMTRIP#_R
SKTOCC# ← PROC_DETECT# (RH519 0_0402_5%)
PROC_SELECT# → GND
CATERR# ← H_CATERR#
CFG_RCOMP → RH59 49.9_0402_1%
CFG[0:19] → CFG0 6 … CFG19 6
BPM#[0:3] → XDP_BPM#0 6 … XDP_BPM#1 6
PROC_TDO / PROC_TDI / PROC_TMS / PROC_TCK → CPU_XDP_TDO / CPU_XDP_TDI / CPU_XDP_TMS / CPU_XDP_TCK 6
PROC_TRST# → CPU_XDP_TRST# 6,22
PROC_PREQ# → XDP_PREQ# 6,22
PROC_PRDY# → XDP_PRDY# 6,22

5 OF 14
SKL-H_BGA1440
REV = 1

+1.2V_DDR

UC1 74AUP1G07GW_TSSOP5 (VCC, NC, A, Y, GND)
CH197 0.1U_0402_10V7K
DDR_VTT_PG_CTRL

+3VS

RH525 220K_0402_5%
SM_PG_CTRL

UH1K SKYLAKE_H2 BGA1440

PAD-D T39–T90 → RSVD_TP / RSVD / VSS
PCH_TRIGGER / CPU_TRIGGER → PCH_TRIGGER_R / CPU_TRIGGER_R (RH167 30_0402_5%, RH192 30_0402_5%)
PROC_TRIGIN / PROC_TRIGOUT

11 OF 14
SKL-H_BGA1440
REV = 1

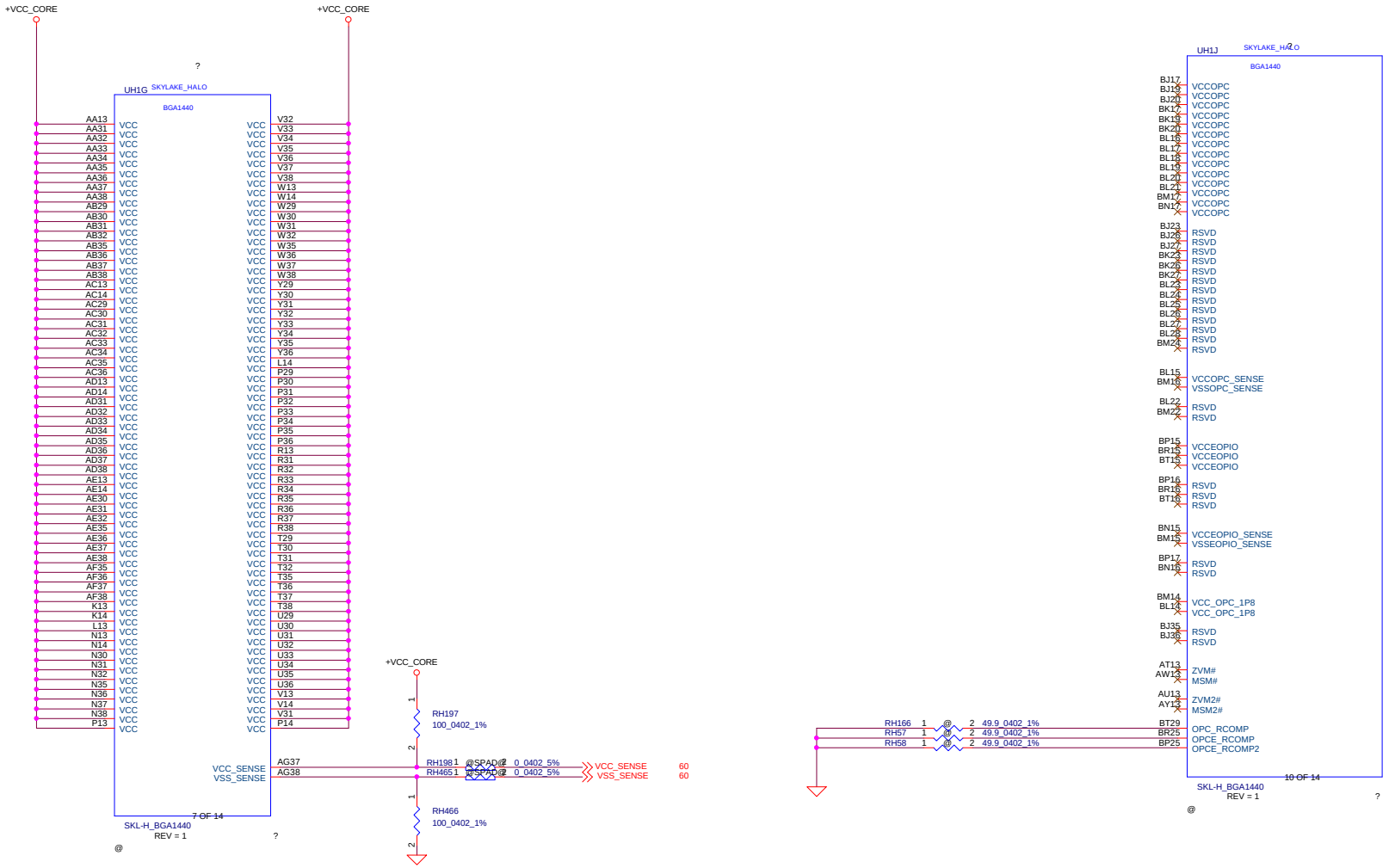
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
C		0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 9 of 75

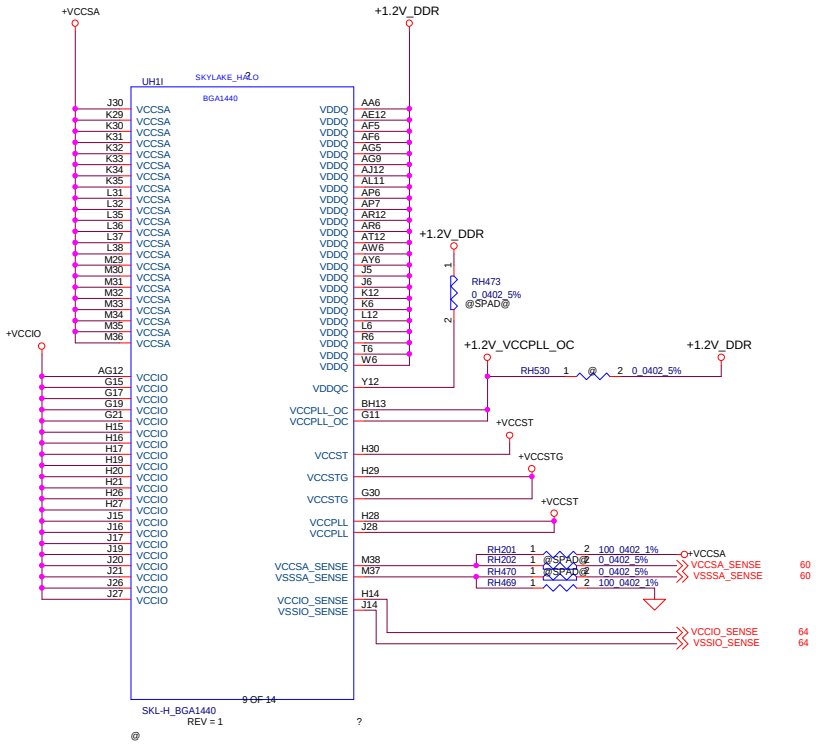


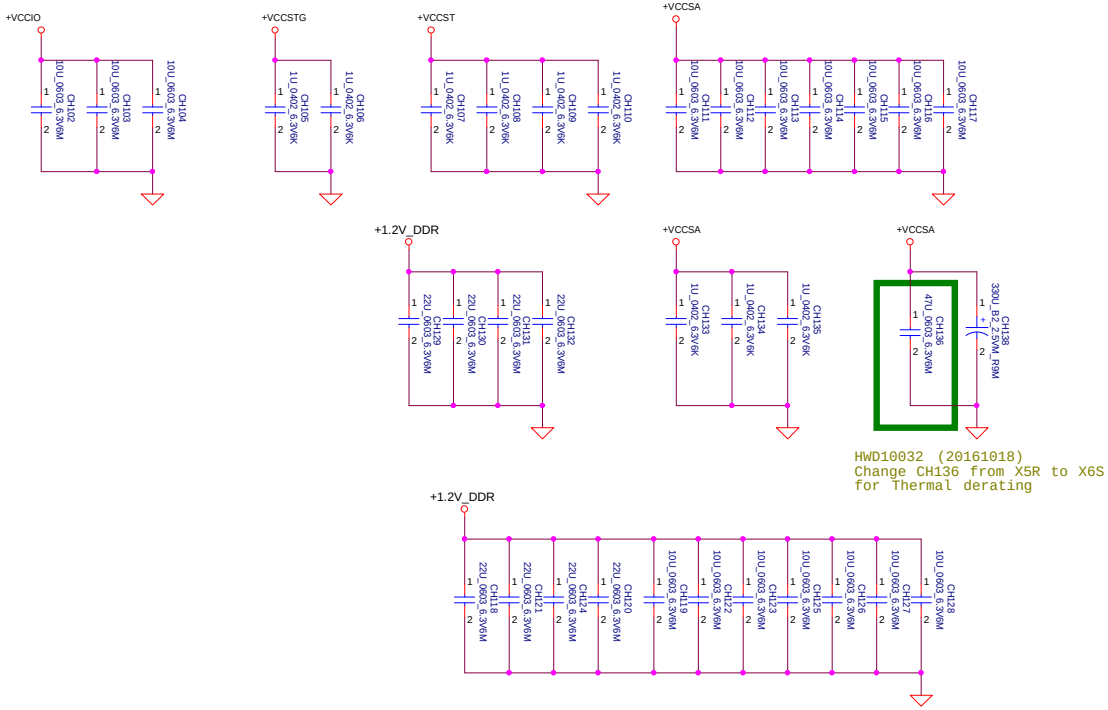
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(5/7) PWR,BYPASS**

Size	Document Number	Rev
Custom		0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 10 of 75





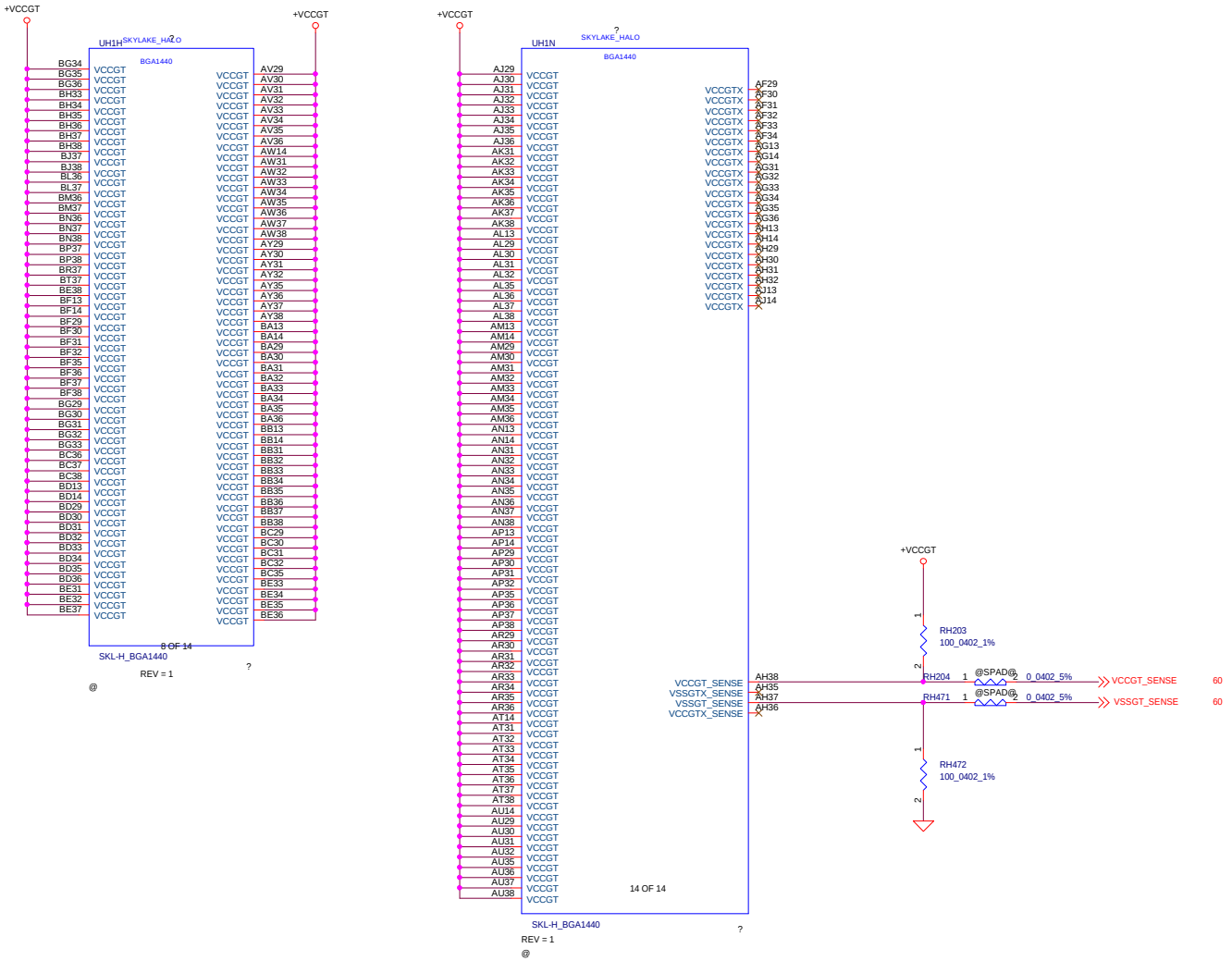
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PROCESSOR(6/7) PWR**

Size	Document Number	Rev
Custom		0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 11 of 75



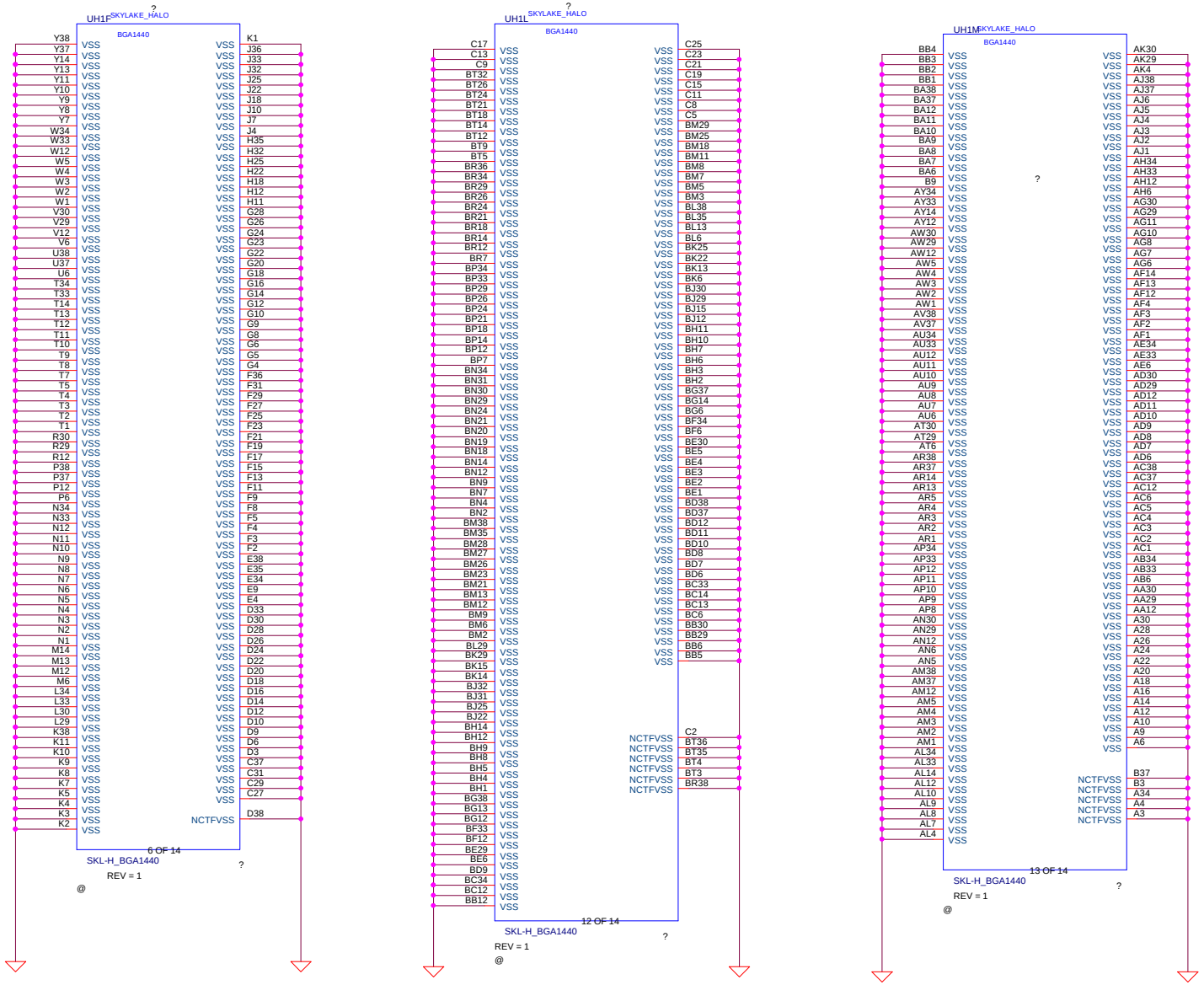
Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
Custom		0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 12 of 75



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PROCESSOR(7/7) VSS**

Size	Document Number	Rev
Custom		0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 13 of 75

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

8 DDR_A_D[0..63]
8 DDR_A_MA[0..13]
8 DDR_A_DQS#[0..7]
8 DDR_A_DQS[0..7]

+2.5V_MEM
CD9 10U_0603_6.3V6M
CD10 10U_0603_6.3V6M
CD3 1U_0402_6.3V6K
CD4 1U_0402_6.3V6K

+0.6VS
CD12 1U_0402_6.3V6K
CD13 10U_0603_6.3V6M
CD14 10U_0603_6.3V6M
CD15 10U_0603_6.3V6M

+3VS
CD16 1U_0402_6.3V6K
CD17 2.2U_0402_6.3V6M

+1.2V_DDR
CD1 1U_0402_6.3V6K
CD2 1U_0402_6.3V6K
CD75 1U_0402_6.3V6K
CD74 1U_0402_6.3V6K
CD77 1U_0402_6.3V6K
CD76 1U_0402_6.3V6K
CD79 1U_0402_6.3V6K
CD78 1U_0402_6.3V6K

+1.2V_DDR
CD5 10U_0603_6.3V6M
CD6 10U_0603_6.3V6M
CD7 10U_0603_6.3V6M
CD8 10U_0603_6.3V6M
CD70 10U_0603_6.3V6M
CD71 10U_0603_6.3V6M
CD72 10U_0603_6.3V6M
CD73 10U_0603_6.3V6M
CD11 220U_D7_2VM_R6M

JDIMM1
JP7
BELLW_SD-80886-1021
CONN@

+1.2V_DDR
DDR_A_D5 DDR_A_D1 DDR_A_DQS#0 DDR_A_DQS0 DDR_A_D7 DDR_A_D3 DDR_A_D13 DDR_A_D9 DDR_A_D15 DDR_A_D10 DDR_A_D21 DDR_A_D17 DDR_A_DQS#2 DDR_A_DQS2 DDR_A_D23 DDR_A_D19 DDR_A_D29 DDR_A_D25 DDR_A_D30 DDR_A_D26

+1.2V_DDR
DDR_A_D4 DDR_A_D0 DDR_A_D6 DDR_A_D2 DDR_A_D12 DDR_A_D8 DDR_A_DQS#1 DDR_A_DQS1 DDR_A_D14 DDR_A_D11 DDR_A_D20 DDR_A_D16 DDR_A_D22 DDR_A_D18 DDR_A_D28 DDR_A_D24 DDR_A_DQS#3 DDR_A_DQS3 DDR_A_D31 DDR_A_D27

8 DDR_CKE0_DIMMA → DDR_CKE0_DIMMA
8 DDR_A_BG1 → DDR_A_BG1
8 DDR_A_BG0 → DDR_A_BG0
DDR_A_MA12 DDR_A_MA9 DDR_A_MA8 DDR_A_MA6 DDR_A_MA3 DDR_A_MA1
8 M_CLK_DDR0 → M_CLK_DDR0
8 M_CLK_DDR#0 → M_CLK_DDR#0
DDR_A_PAR → DDR_A_PAR
8 DDR_A_BS1 → DDR_A_BS1
DDR_CS0_DIMMA# → DDR_CS0_DIMMA#
8 DDR_A_WE# → DDR_A_WE#
M_ODT0 → M_ODT0
8 DDR_CS1_DIMMA# → DDR_CS1_DIMMA#
M_ODT1 → M_ODT1

DDR4_DRAMRST# → DDR4_DRAMRST#
DDR_CKE1_DIMMA → DDR_CKE1_DIMMA 8
DDR_A_ALERT# → DDR_A_ACT# 8, DDR_A_ALERT# 8
DDR_A_MA11 DDR_A_MA7 DDR_A_MA5 DDR_A_MA4 DDR_A_MA2
M_CLK_DDR1 → M_CLK_DDR1 8, M_CLK_DDR#1 8
DDR_A_MA0 DDR_A_MA10
DDR_A_BS0 → DDR_A_BS0 8, DDR_A_RAS# 8
DDR_A_CAS# → DDR_A_CAS# 8, DDR_A_MA13

+V_DDR_REFA
DIMM_CHA_SA2
CD18 1U_0402_6.3V6K

+1.2V_DDR
DDR_A_D37 DDR_A_D33 DDR_A_DQS#4 DDR_A_DQS4 DDR_A_D38 DDR_A_D34 DDR_A_D44 DDR_A_D40 DDR_A_D46 DDR_A_D42 DDR_A_D52 DDR_A_D49 DDR_A_DQS#6 DDR_A_DQS6 DDR_A_D55 DDR_A_D51 DDR_A_D61 DDR_A_D56 DDR_A_D62 DDR_A_D58 PCH_SMBCLK

+1.2V_DDR
DDR_A_D39 DDR_A_D35 DDR_A_D45 DDR_A_D41 DDR_A_DQS#5 DDR_A_DQS5 DDR_A_D47 DDR_A_D43 DDR_A_D53 DDR_A_D48 DDR_A_D54 DDR_A_D50 DDR_A_D60 DDR_A_D57 DDR_A_DQS#7 DDR_A_DQS7 DDR_A_D63 DDR_A_D59 PCH_SMBDATA DIMM_CHA_SA0 DIMM_CHA_SA1 +0.6VS

+3VS +2.5V_MEM → 6,15,18,43 PCH_SMBCLK
PCH_SMBDATA → 6,15,18,43

All VREF traces should have 10 mil trace width

+3VS
RD1 0_0402_5% @
RD2 0_0402_5% @
RD3 0_0402_5% @
DIMM_CHA_SA0
DIMM_CHA_SA1
DIMM_CHA_SA2
RD28 0_0402_5% @SPAD@
RD29 0_0402_5% @SPAD@
RD30 0_0402_5% @SPAD@

+1.2V_DDR
RD35 470_0402_1%
DDR4_DRAMRST# → 15 DDR4_DRAMRST#
RD31 0_0402_5% @SPAD@
H_DRAMRST# 18
CD69 1U_0402_6.3V6K

+V_DDR_REFA_R
20mil
RH484 1 2 2_0402_1%
+V_DDR_REFA
CH101 0.022U_0402_25V7K
RH211 24.9_0402_1%

+1.2V_DDR
RH206 1K_0402_1%
RH209 1K_0402_1%

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.
Title: DDRIII DIMMA
Size: | Document Number: LA-E331P | Rev: 0.1(000)
Date: Wednesday, October 26, 2016 | Sheet 14 of 75

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMMB

8 DDR_B_D[0..63]
8 DDR_B_MA[0..13]
8 DDR_B_DQS#[0..7]
8 DDR_B_DQS[0..7]

JDIMM2
JP7

All VREF traces should have 10 mil trace width

BELLW_SD-80886-1021
CONN@

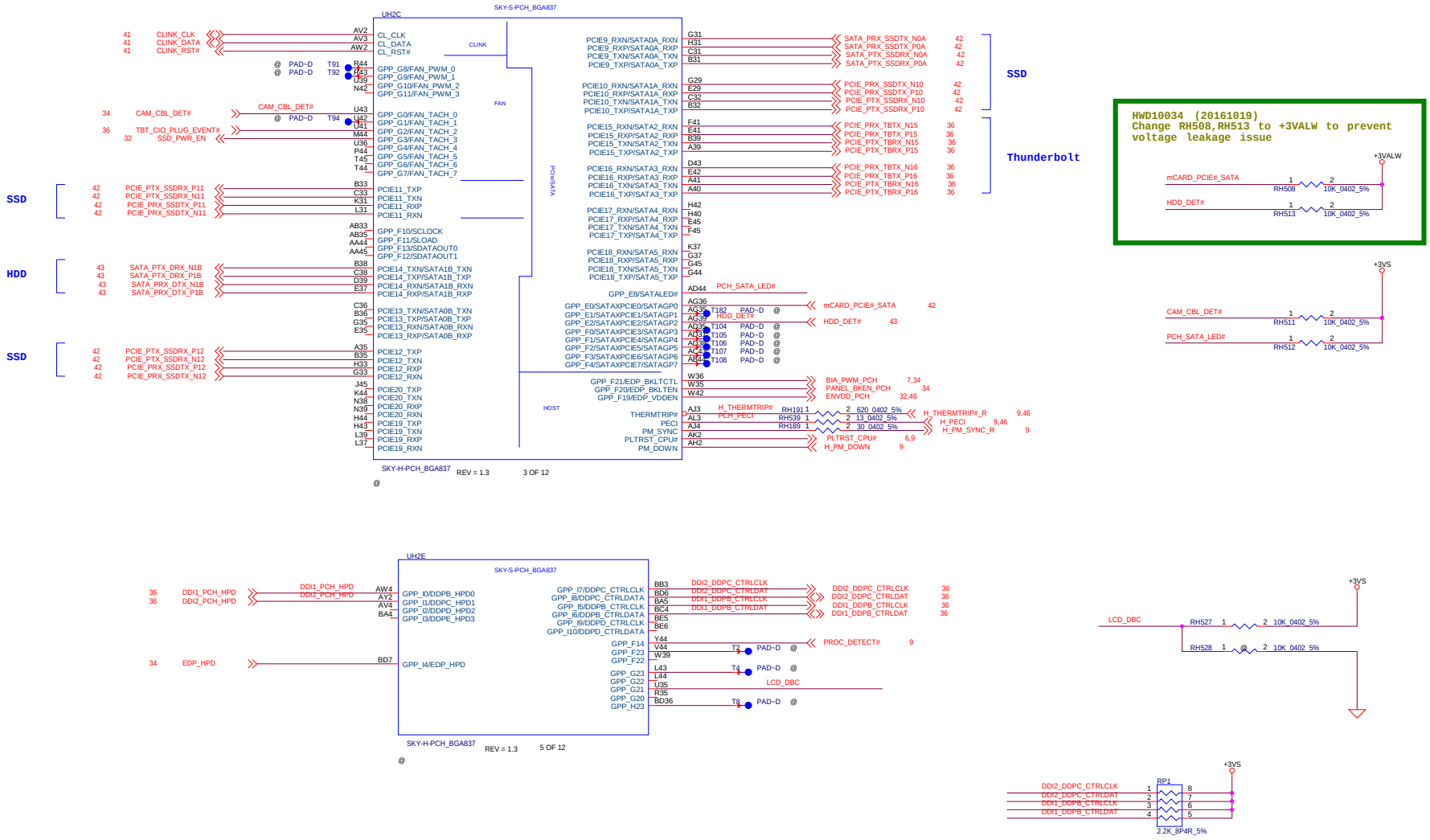
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 15 of 75



HWD10034 (20161019)
Change RH508,RH513 to +3VALW to prevent voltage leakage issue

PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 16 of 75

RTC CRYSTAL

Max Crystal
ESR = 50k Ohm.

EMI10005 (20161003)
Change RA96/RA97 from 0 ohm
to 33 ohm for panel fliker issue

SPI ROM FOR ME (32MByte)

20160 0420 follow Avandotor and Dino 2 MLK same part

HWD10036 (20161019)
Change 0ohm to short pad

Close PR313

Follow Beaver Creek

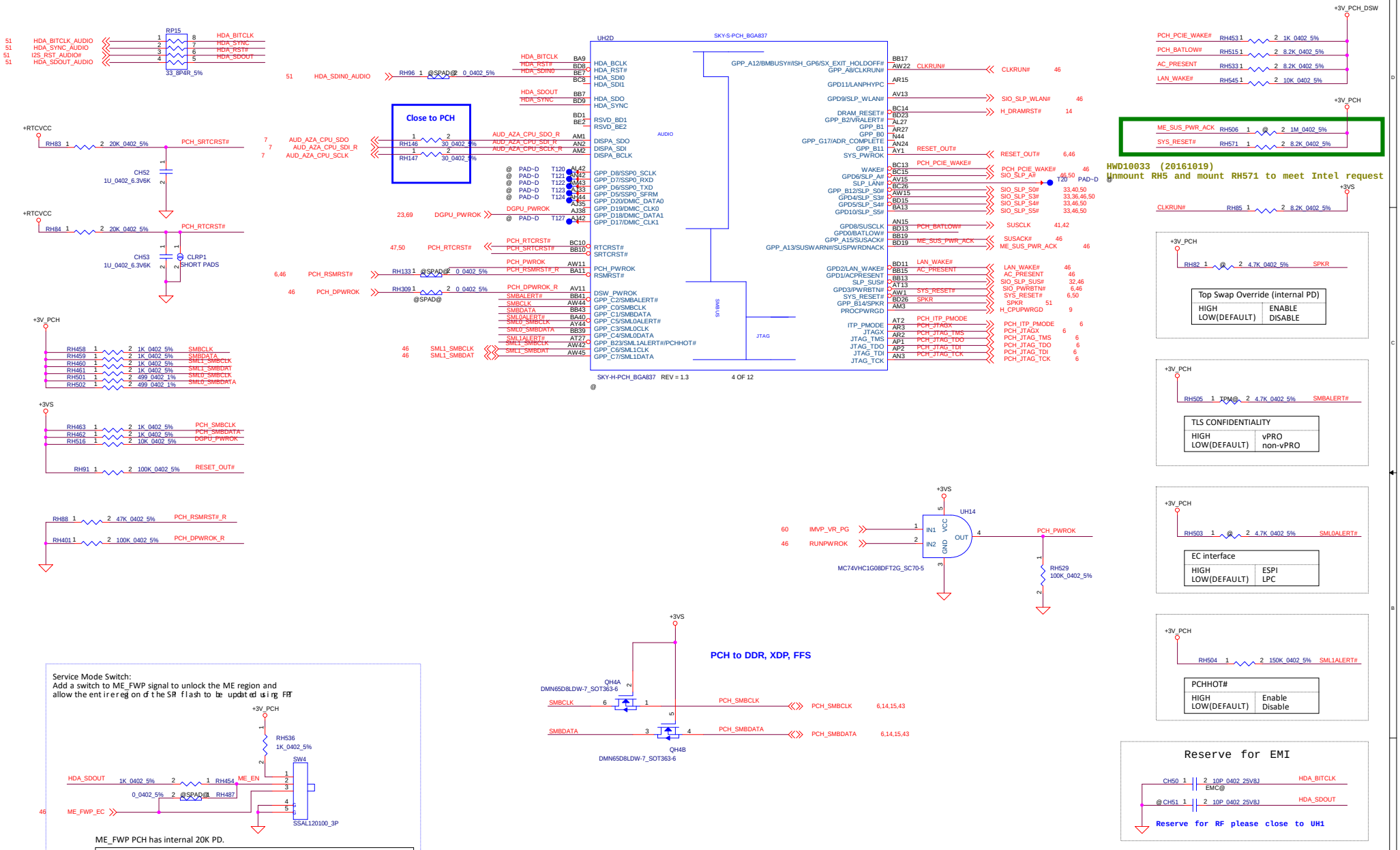
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (2/8) SMBUS, CLK, SPI, LPC

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 17 of 75



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

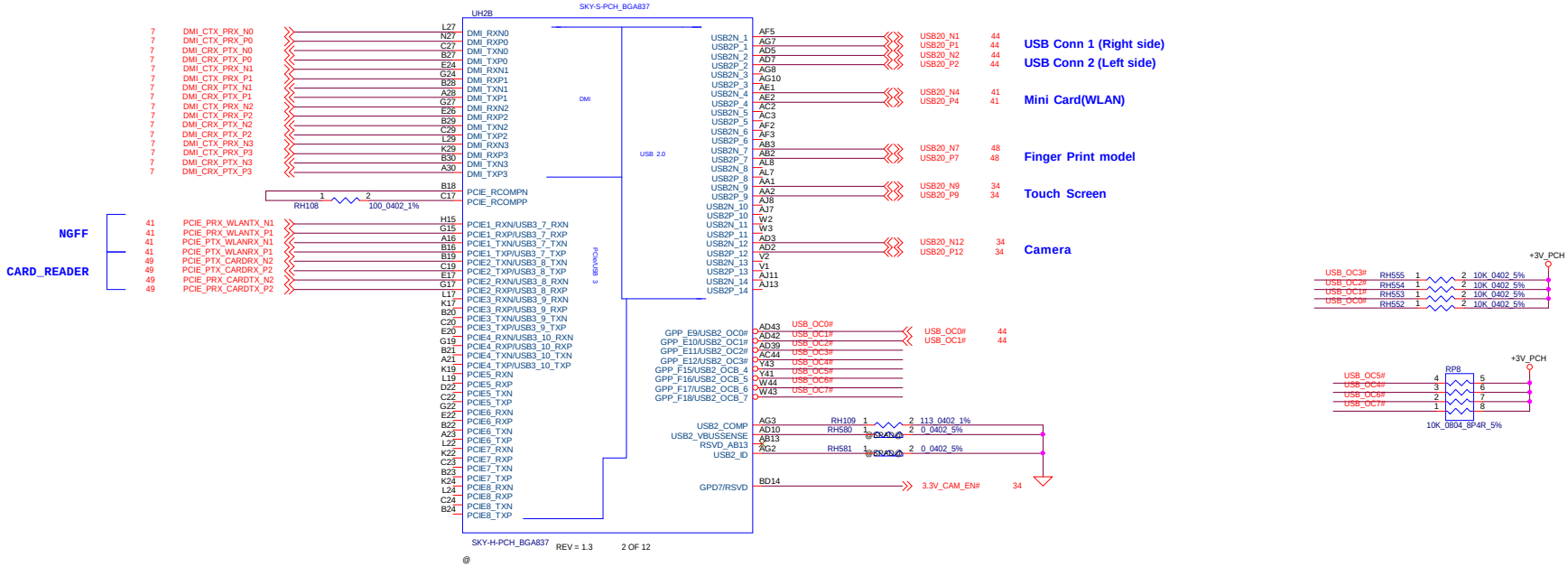
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

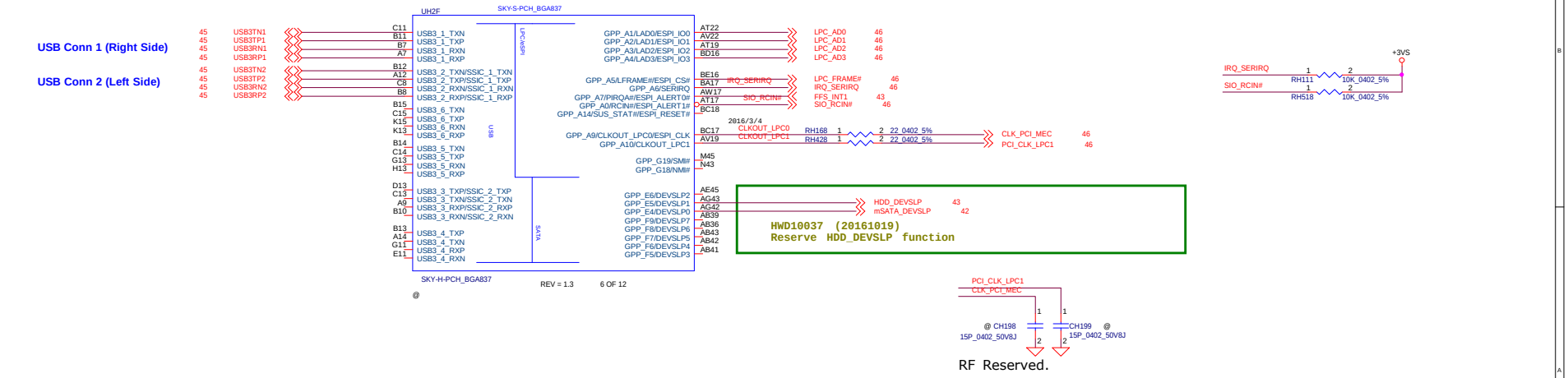
Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 18 of 75





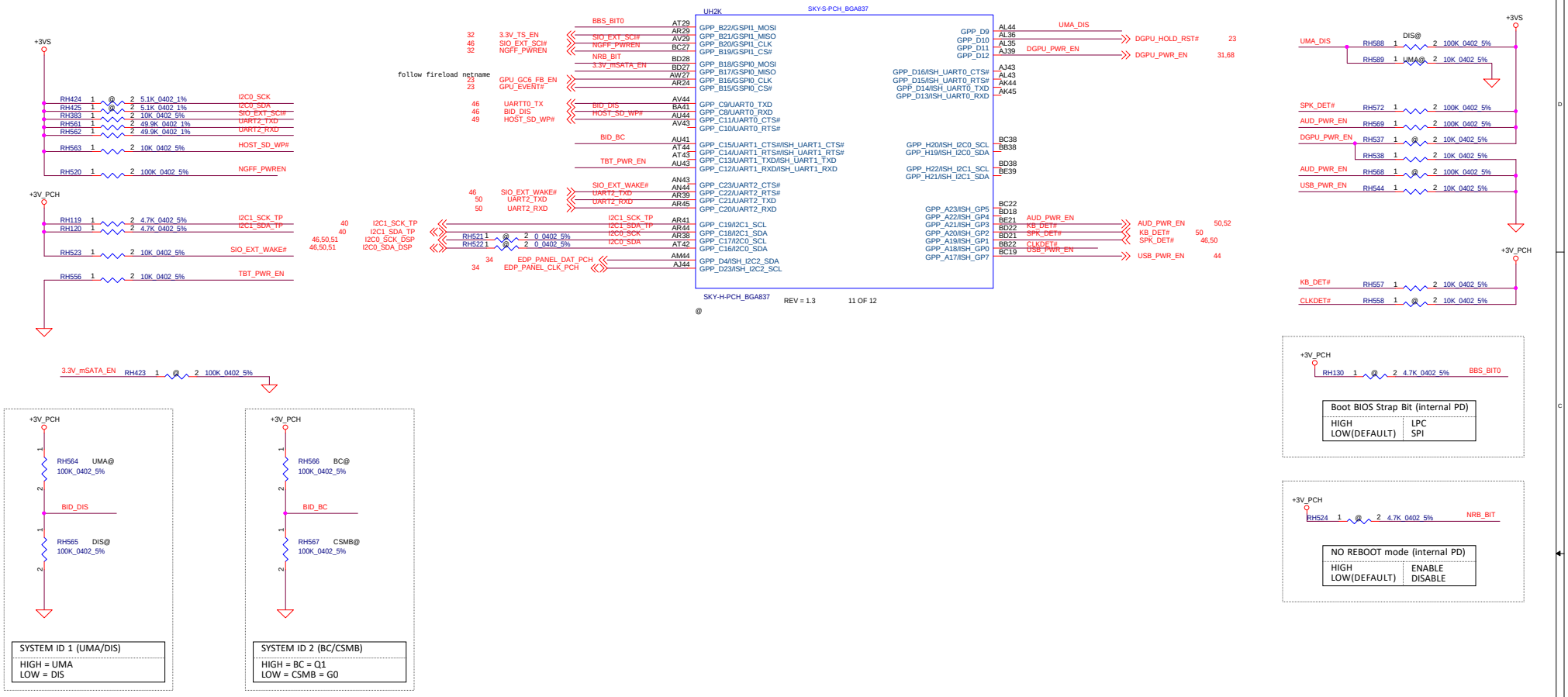
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 Sheet 19 of 75



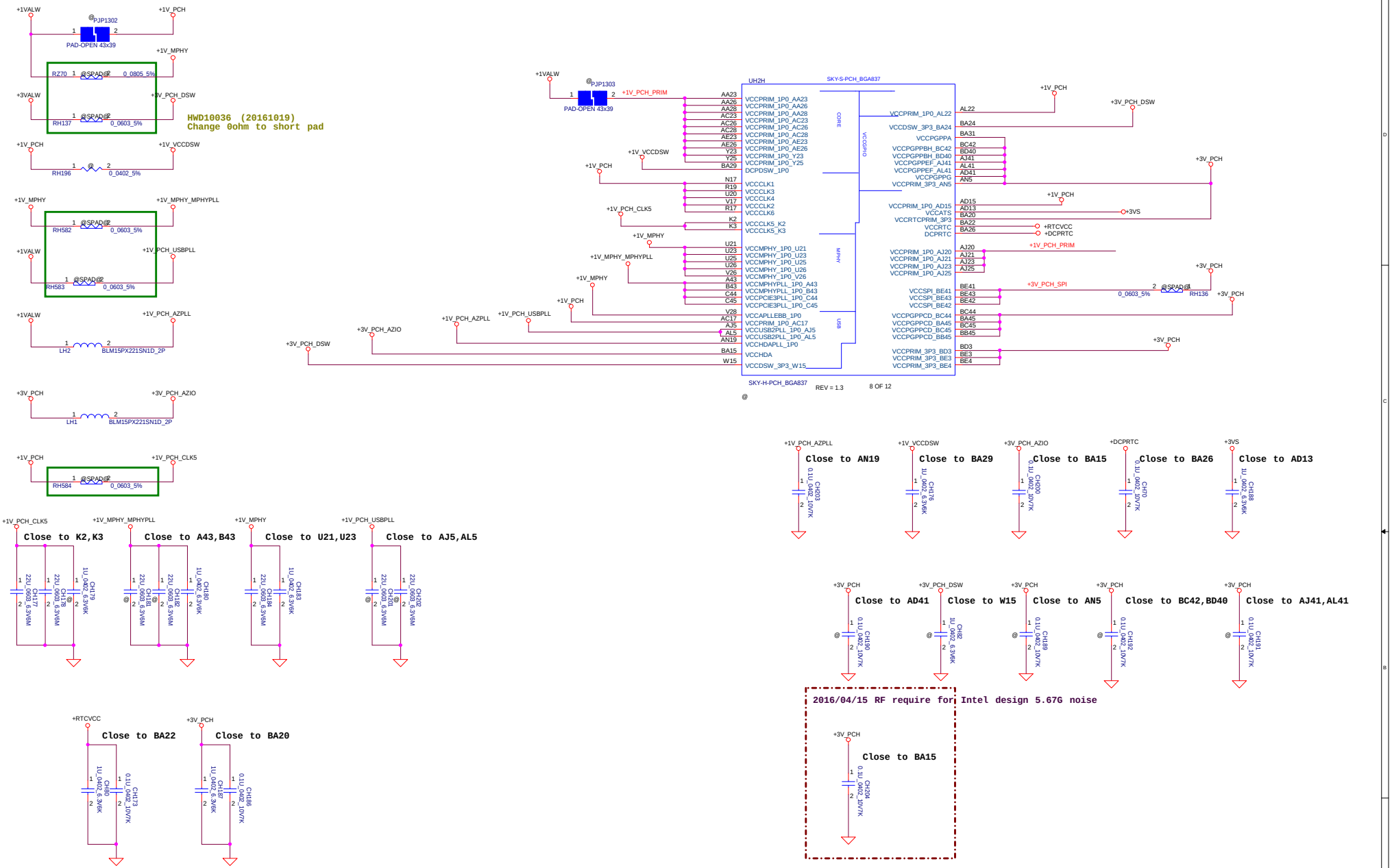
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (5/8) GPIO, CPU, MISC**

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 Sheet 20 of 75



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

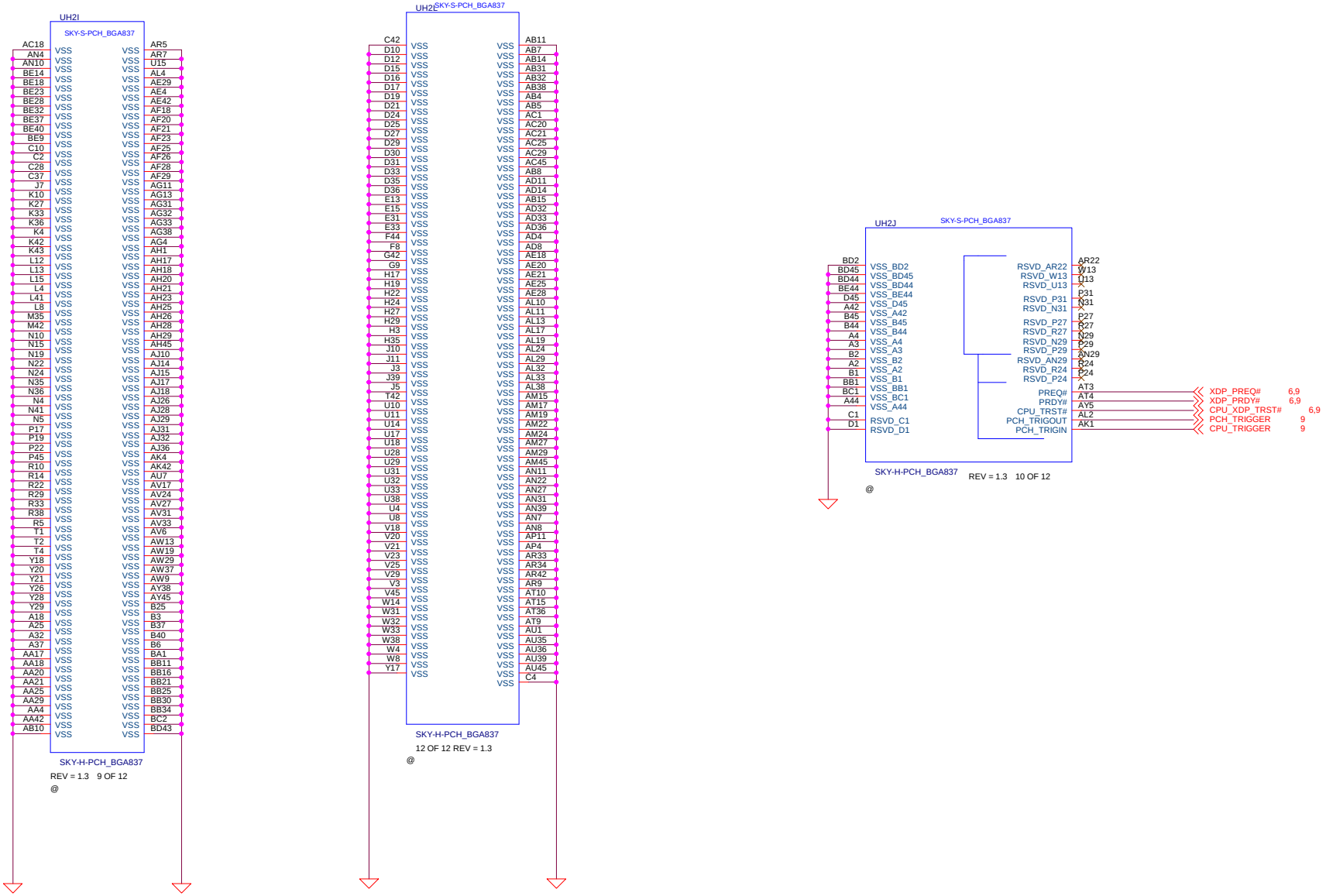
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 21 of 75

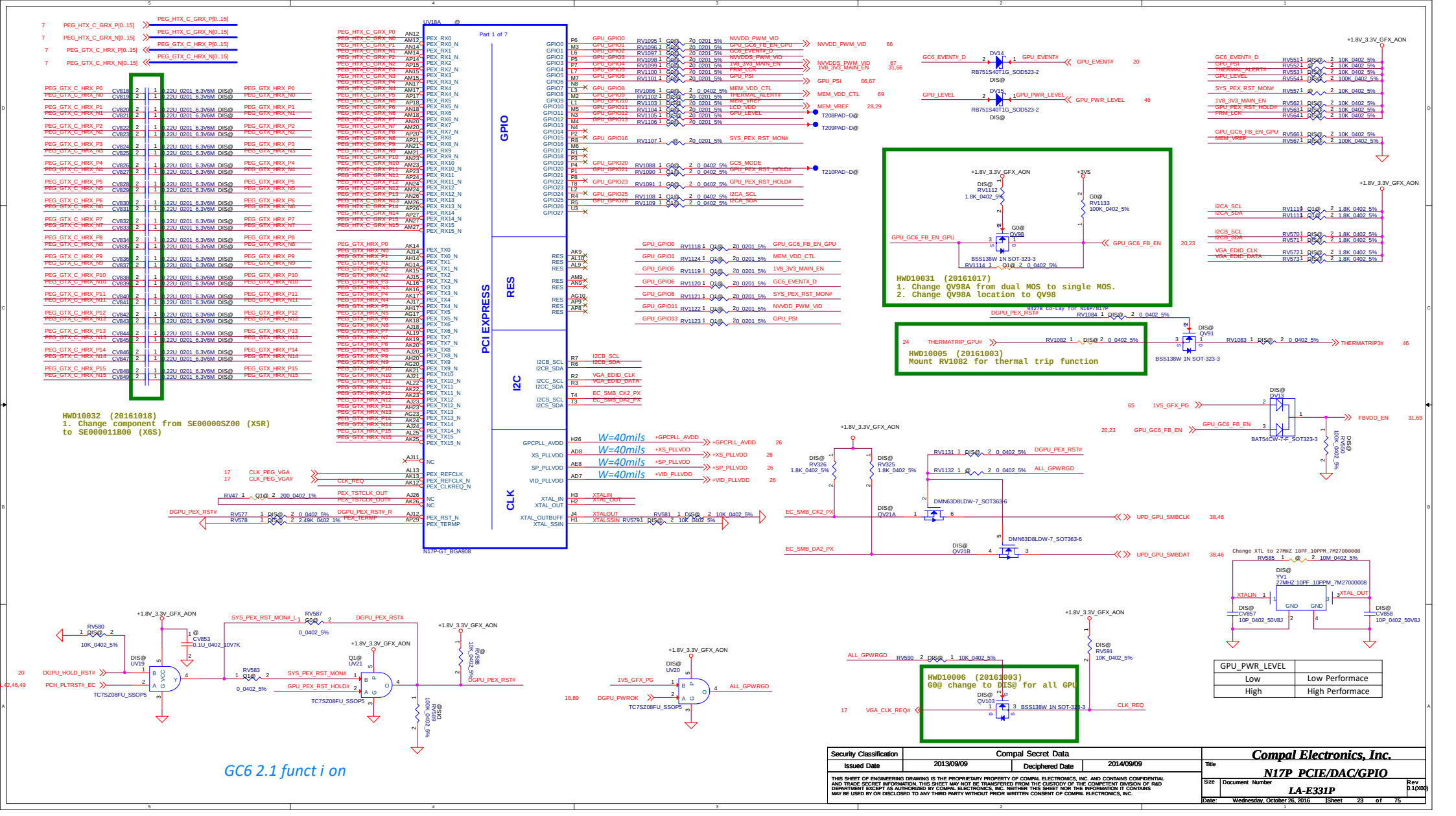


Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-E331P	0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 22 of 75



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

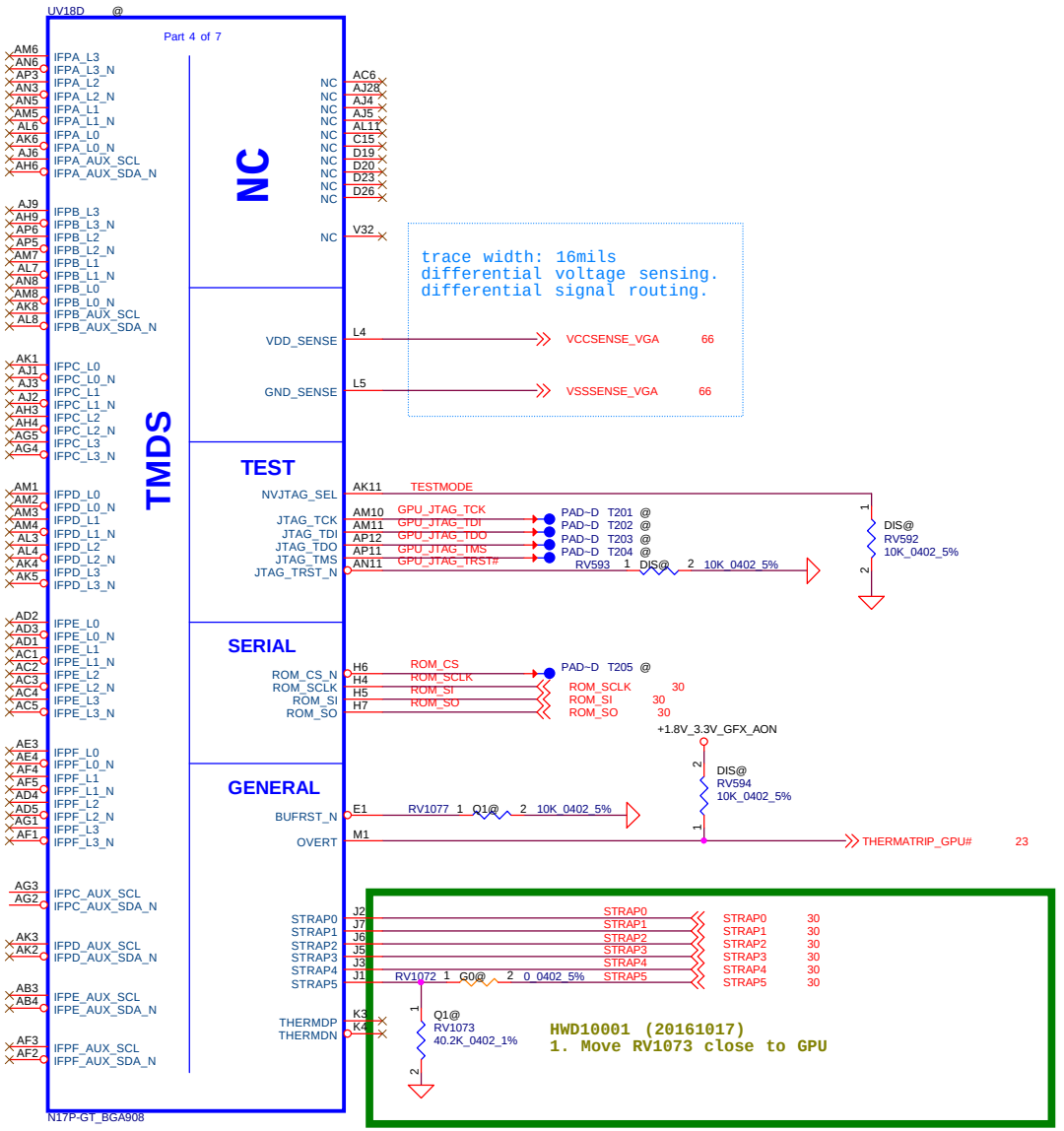
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **N17P PCIE/DAC/GPIO**

Size	Document Number	Rev
	LA-E331P	0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 23 of 75



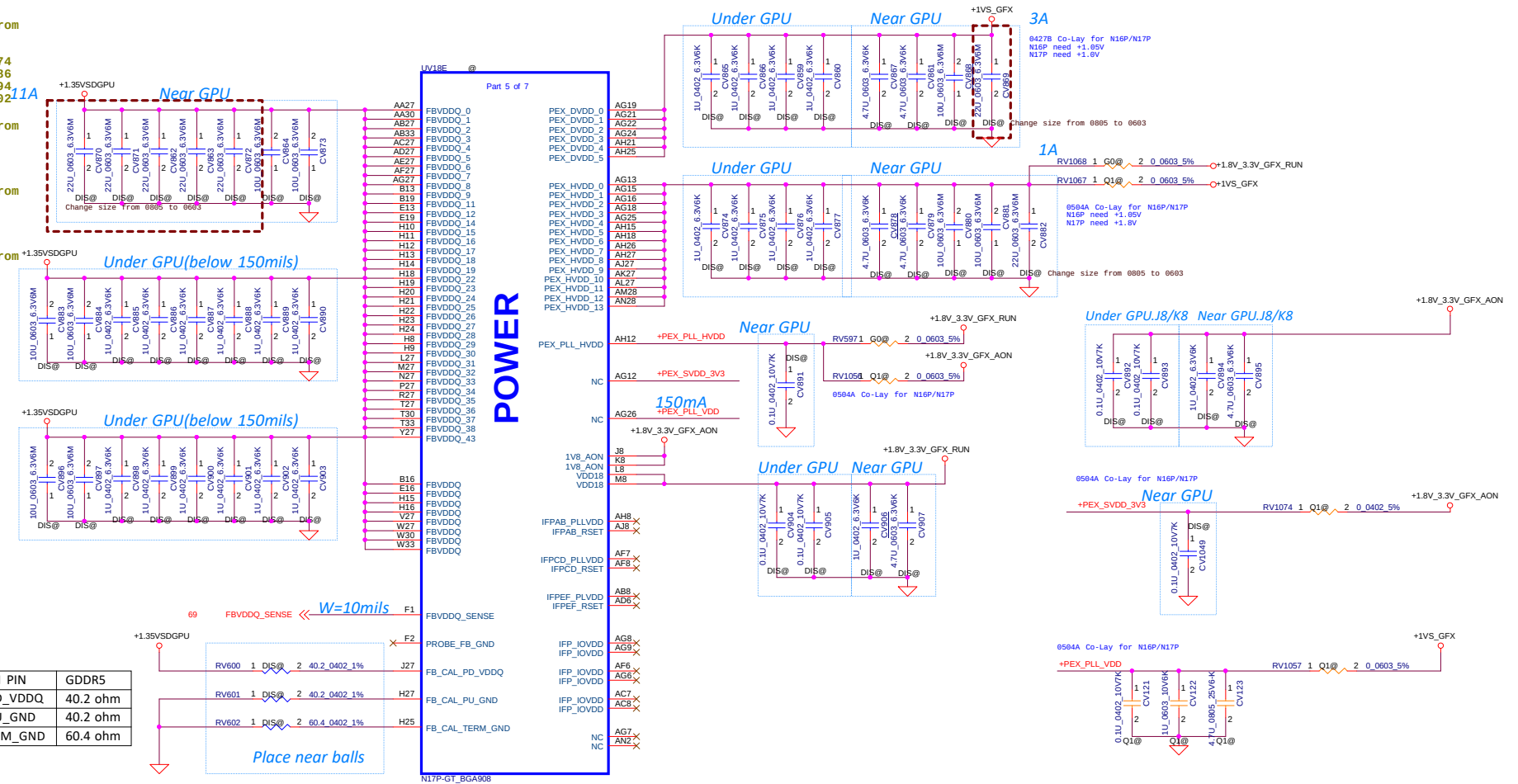
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **N17P_eDP/HDMI/mDP**

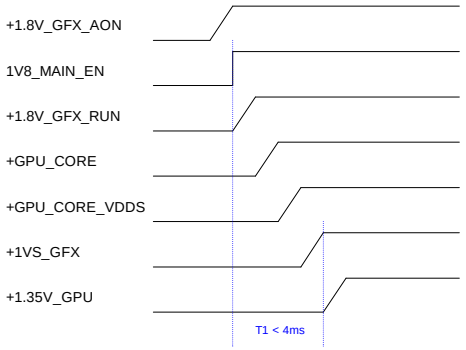
Size	Document Number	Rev
	LA-E331P	0.1(X00)
Date: Wednesday, October 26, 2016	Sheet 24 of 75	

HWD10032 (20161018)
1. Change below component from SE000000K80 (X5R) to E00001EP00 (X7R) CV859,CV860,CV865,CV866,CV874 CV875,CV876,CV877,CV885,CV886 CV887,CV888,CV889,CV890,CV894 CV898,CV899,CV900,CV901,CV902 CV903
2. Change below component from SE000005T80 (X5R) to SE000010T00 (X6S) CV864,CV873,CV880,CV881 CV883,CV884,CV896,CV897
3. Change below component from SE00000M000 (X5R) to SE00001CA00 (X6S) CV863,CV869,CV870,CV872 CV882,CV924
4. Change below component from SE107475K80 (X5R) to SE00000G300 (X6S) CV878,CV879,CV895



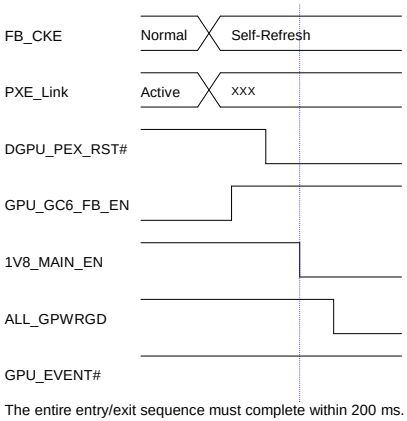
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

GPU Power Up Sequence



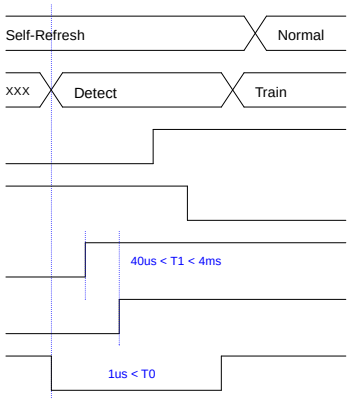
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

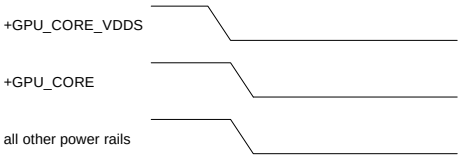


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



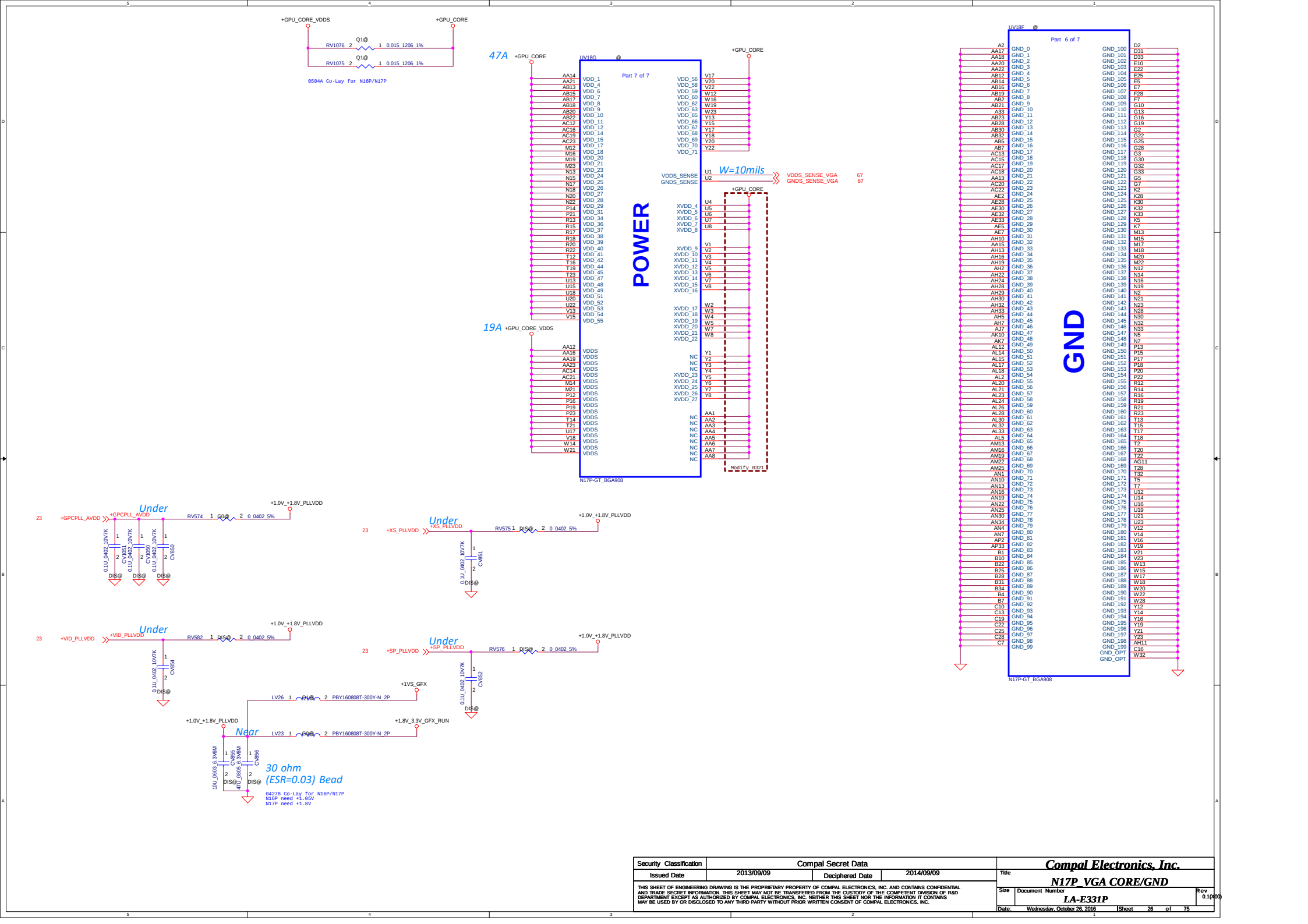
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: N17P_Power

Size | Document Number: LA-E331P | Rev: 0.1(100)

Date: Wednesday, October 26, 2016 | Sheet 25 of 75



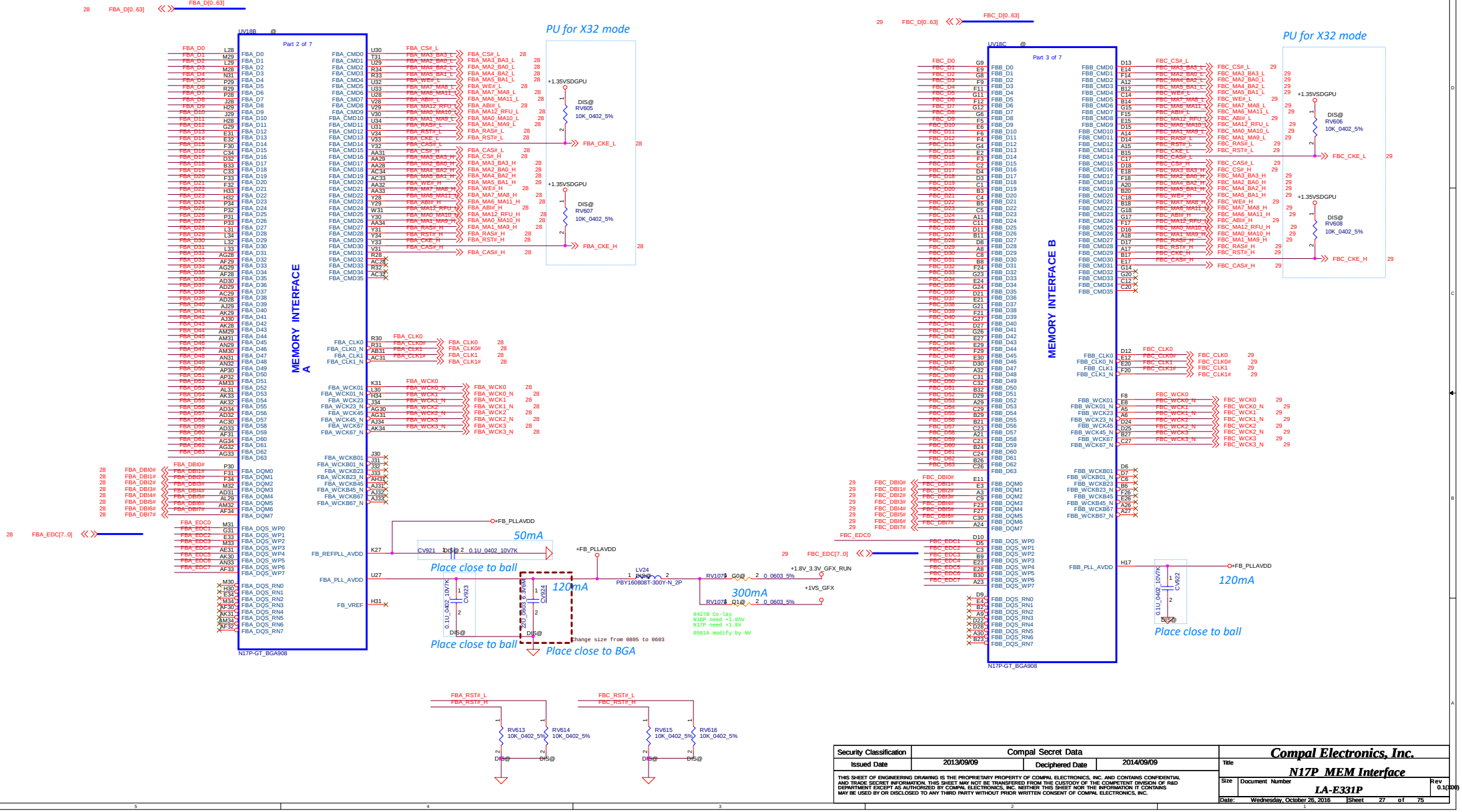
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: N17P_VGA CORE/GND

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 Sheet 26 of 75



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **N17P MEM Interface**

Size: | Document Number: **LA-E331P** | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 27 of 75

Memory Partition A- Lower 32 bits

MF=0

MF=1

MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable

W=16mils

Under DRAM

Close to DRAM

Around DRAM

Change size from 0805 to 0603

170-BALL SGRAM GDDR5

K4G80325FB-HC03_FBGA170-D

Security Classification	Compal Secret Data	
Issued Date	2013/09/09	Deciphered Date 2014/09/09

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

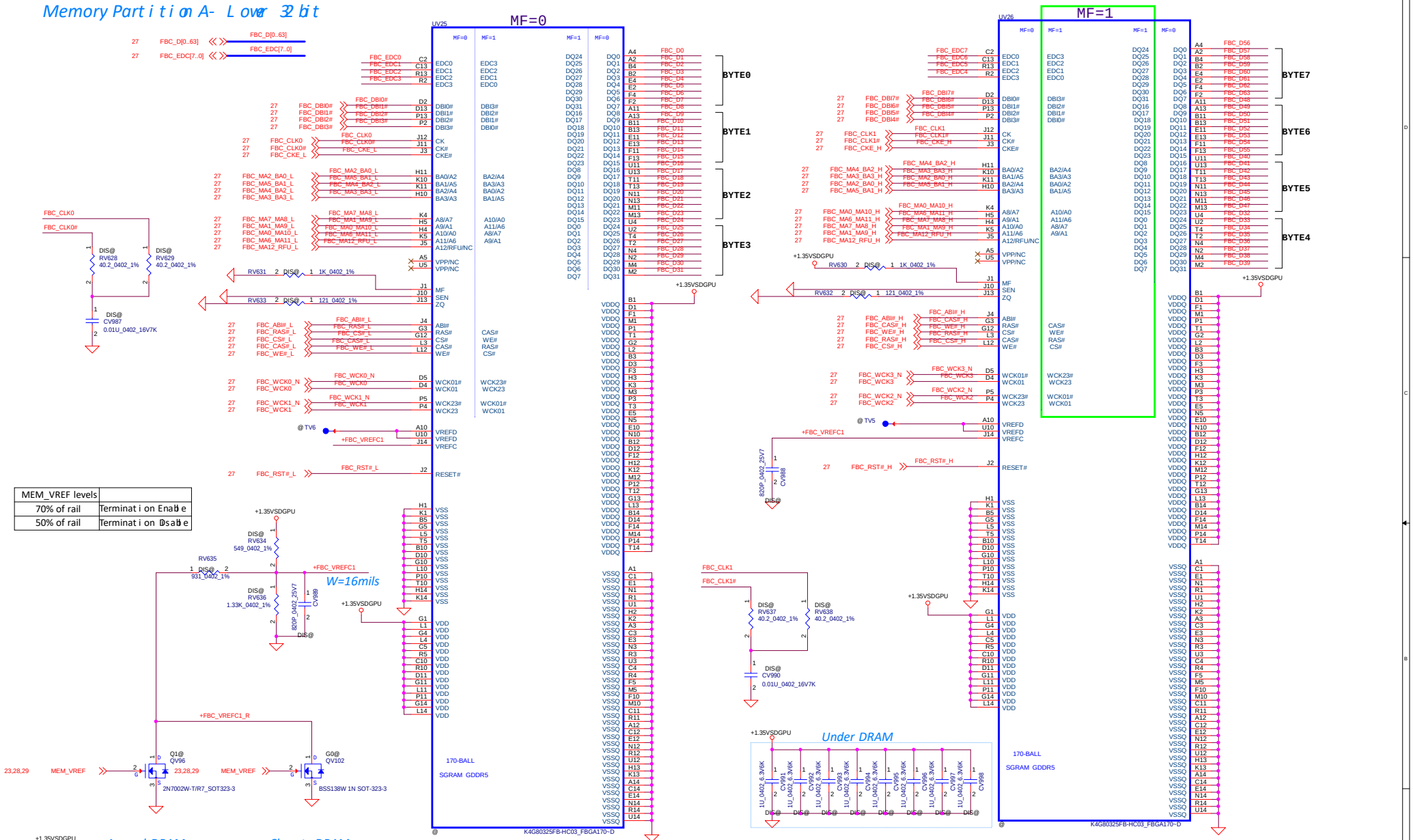
Compal Electronics, Inc.

Title: N17P_GDDR5_A

Size: | Document Number: LA-E331P | Rev: 0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 28 of 75

Memory Partition A- Lower 32bit



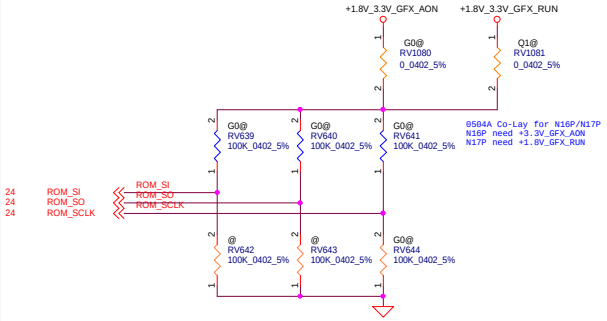
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

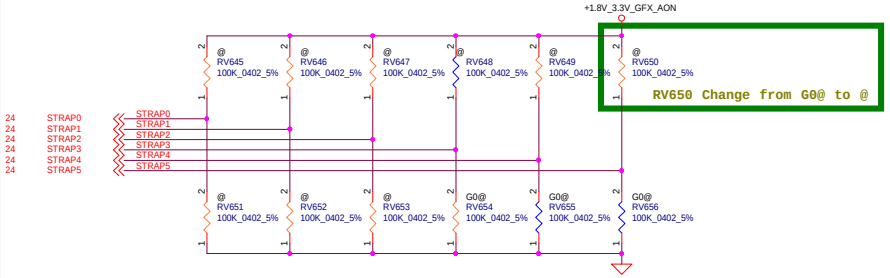
Compal Electronics, Inc.

Title: N17P_GDDR5_B

Size: | Document Number: LA-E331P | Rev: 0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 29 of 75





SMB_ALT_ADDR	State
Low	Single GPU
High	Dual GPU

DEVID_SEL	State
Low	Original Device ID
High	Re-brand Device ID

PCIE_CFG	State
Low	Normal signal swing
High	Reduce the signal amplitude

VGA_DEVICE	State
Low	3D Device
High	VGA Device

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000 SAMSUNG	0000
10.0 kΩ	1001 MICRON	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 4. N17P-Q1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

Notes:
1. For N17P-Q1, the maximum allowable memory case temperature is 85 °C.

Table 1. N16P-Q3 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade(Gbps)	Qual Freq (MHz)	Date Code Alert	Qual Plan	ETA
8 Gb	256Mx32[2]	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	5 Gbps	2500	N/A	Full	Done
			Micron	MT51J256M32HF-60:A	A-die	0x9	5 Gbps	2500	N/A	Full	Done

Notes:
1. For N16P-Q3, the maximum allowable memory case temperature is 85 °C.
2. 8 Gb is supported in ×32 configuration only (no ×16 support planned).

N17P-G0/-G1 GDDR5 MEMORY RVL

NVIDIA recommends the following GDDR5 memories for use in conjunction with notebook designs using N17P-G0/-G1 GPUs.

Table 1. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.5V/ 1.5V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	0x0	3500	N/A	Production candidate
				Micron	MT51J256M32HF-70:A	A-die	0x1	3500	N/A	Production candidate
				Hynix	H5GQ8H24MJR-R0C	M-die	0x2	3500	N/A	Post-production candidate

Note:
1. For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
2. N17P-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

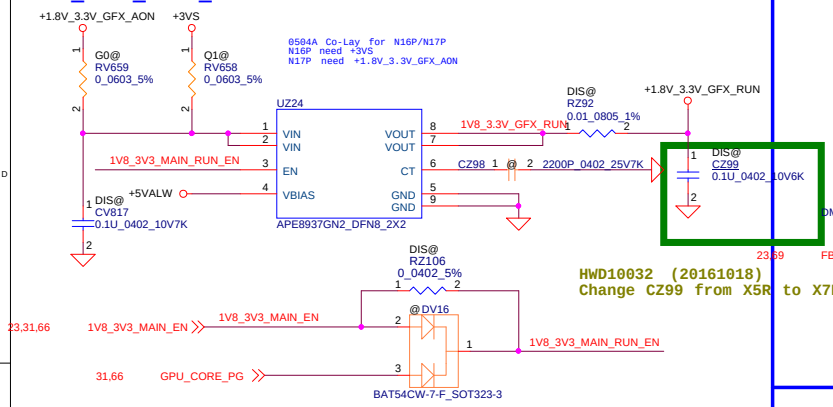
Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

Berlinetta MLK			
Straps	(N17P-Q1)		(N17P-G0)
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL.	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0) , DEVIE_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0) , VGA_DEVICE(0)
STRAP5	Unused	"L"	

Compal Electronics, Inc.
Title: N17P_MISC
Size: C Document Number: LA-E331P Rev: 0.1(X00)
Date: Wednesday, October 26, 2016 Sheet 30 of 75

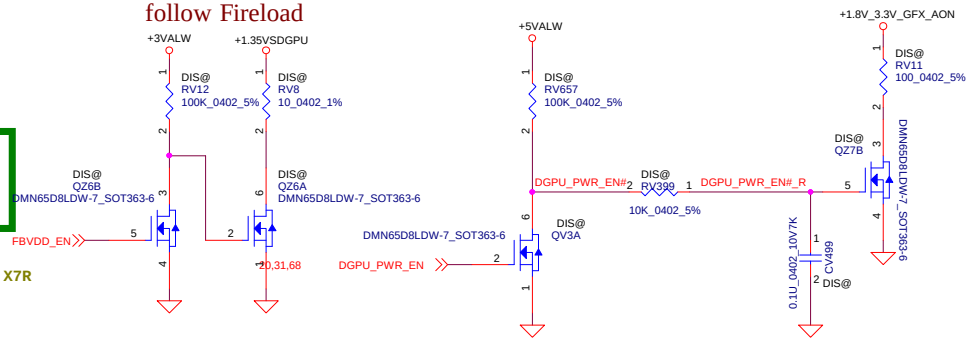
+1.8V_3.3V_GFX_RUN



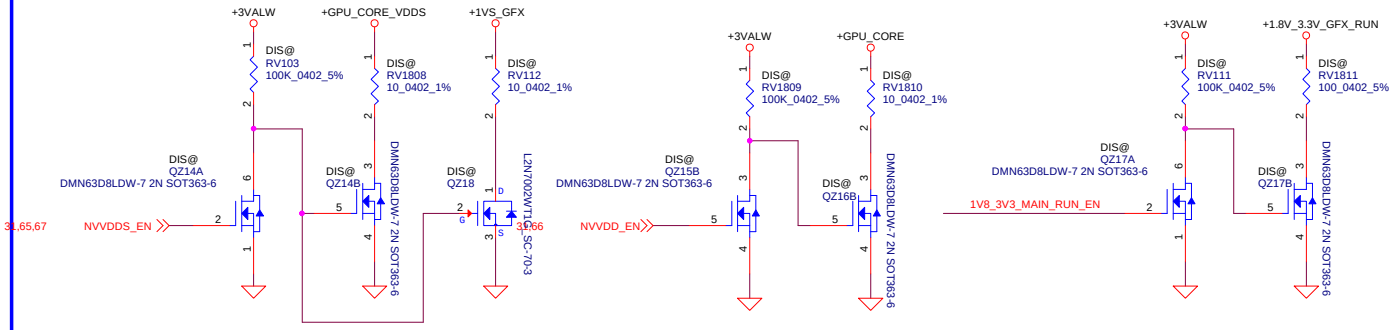
HWD10032 (20161018)
Change CZ99 from X5R to X7R

Discharge

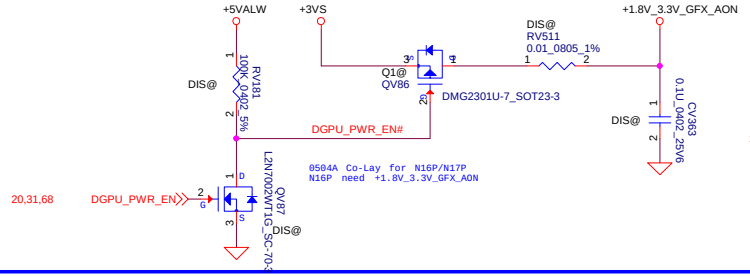
follow Fireload



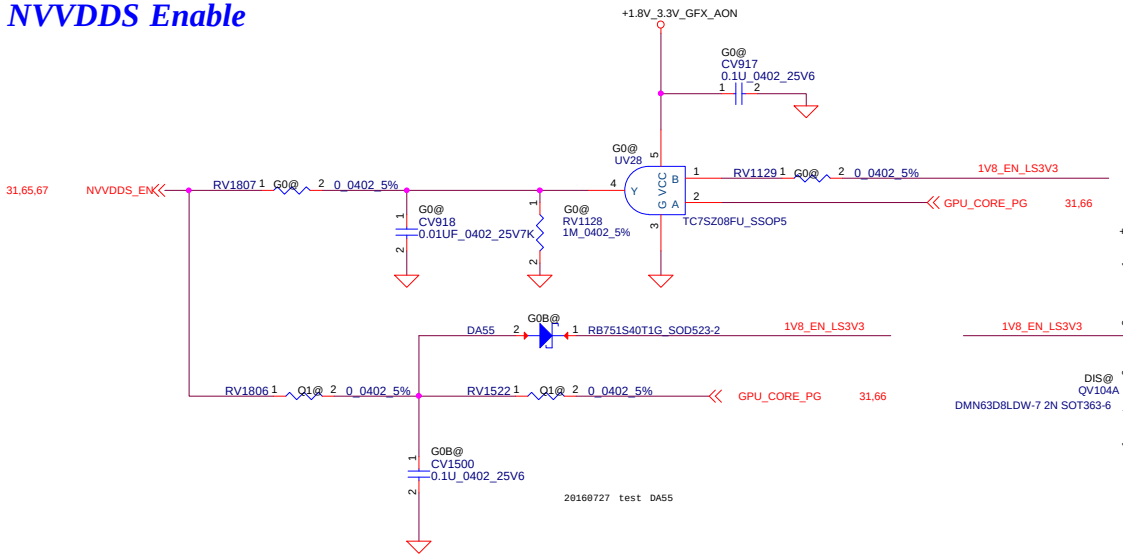
20160727 follow fireload

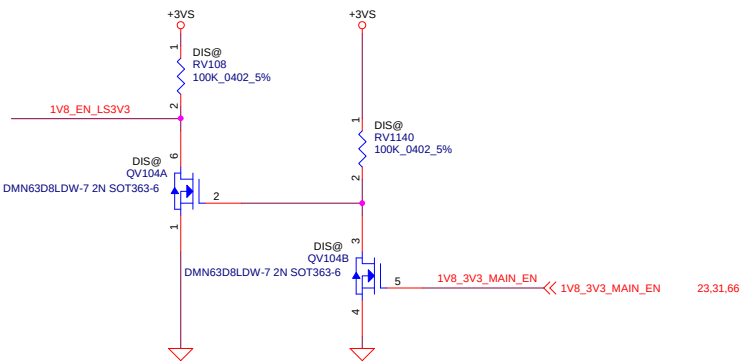


+3VS to +1.8V_3.3V_GFX_AON

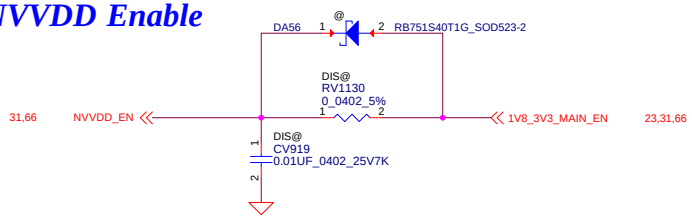


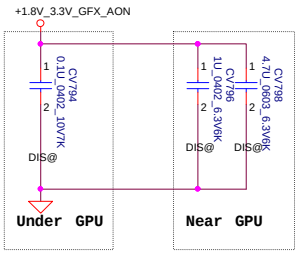
NVVDDS Enable





NVVDD Enable





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

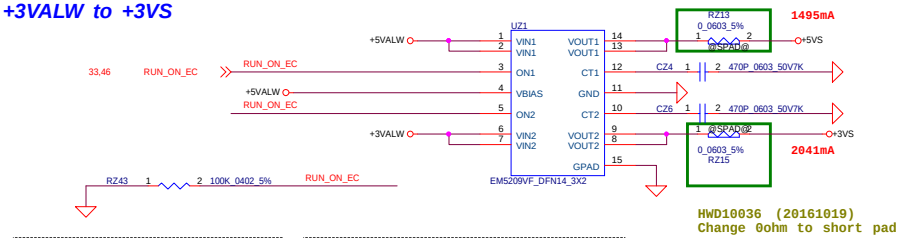
Compal Electronics, Inc.

Title: **GPU DC/DC interface**

Size	Document Number	Rev
		0.1(X00)

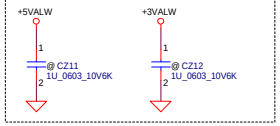
Date: Wednesday, October 26, 2016 Sheet 31 of 75

+5VALW to +5VS
+3VALW to +3VS

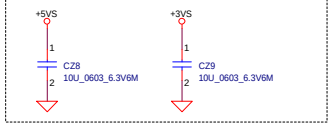


HWD10036 (20161019)
Change 0ohm to short pad

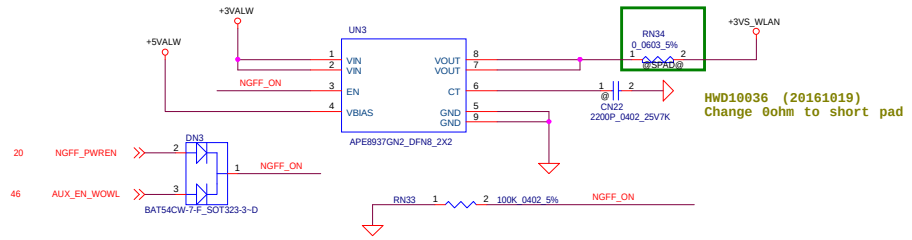
Close UZ4



Close UZ4



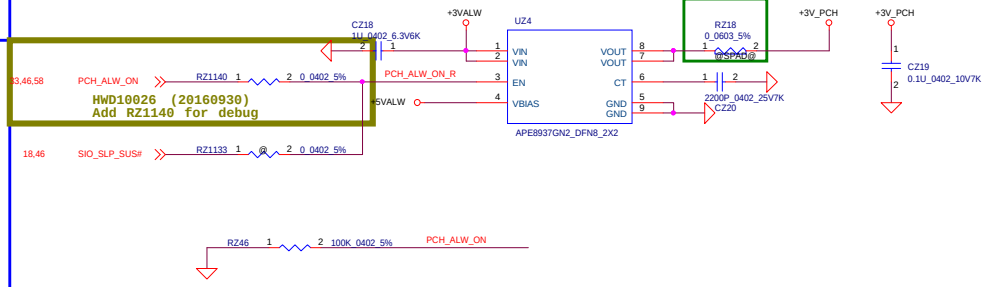
WLAN Load Switch



HWD10036 (20161019)
Change 0ohm to short pad

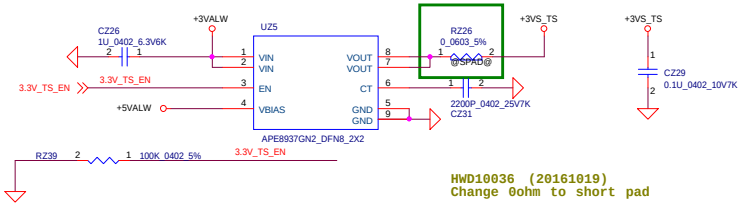
+3VALW to +3V_PCH

HWD10036 (20161019)
Change 0ohm to short pad

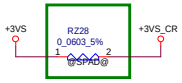


HWD10026 (20160930)
Add RZ1140 for debug

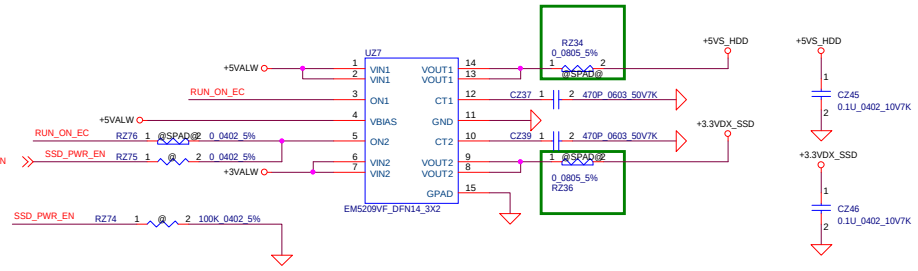
Touch Screen Load Switch & Card Reader



HWD10036 (20161019)
Change 0ohm to short pad

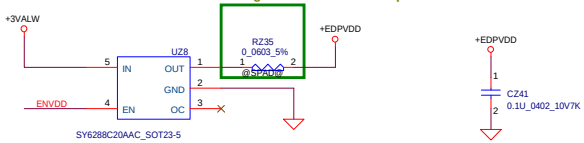


HDD, SSD Load Switch

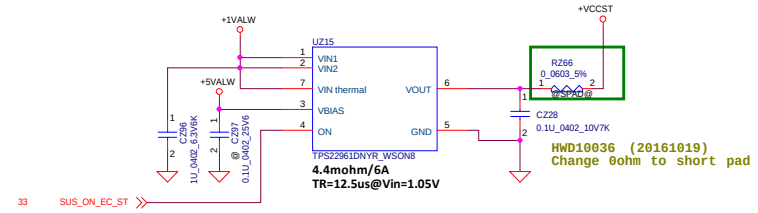


eDP & Camera Load Switch

HWD10036 (20161019)
Change 0ohm to short pad



+VCCST Load Switch

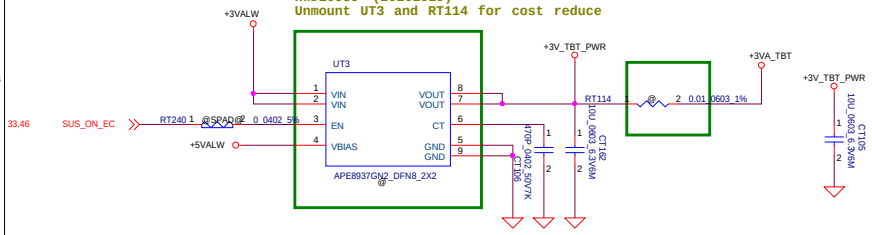


4.4mohm/6A
TR=12.5us@Vin=1.05V

HWD10036 (20161019)
Change 0ohm to short pad

Alpine Ridge(TBT) Load Switch

HWD10039 (20161019)
Unmount UT3 and RT114 for cost reduce



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

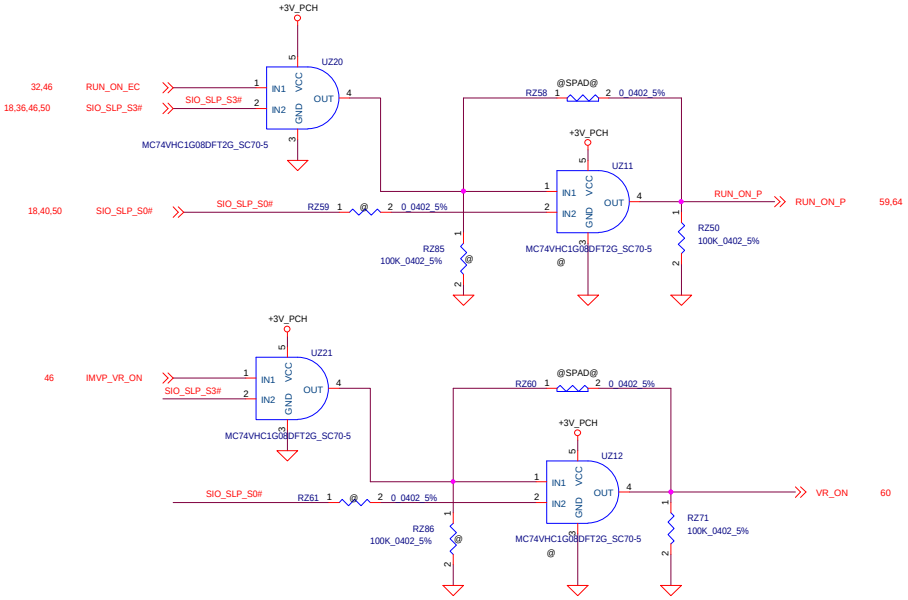
Title: SYS DC/DC Interface

Size | Document Number: LA-E331P | Rev: 0.1(000)

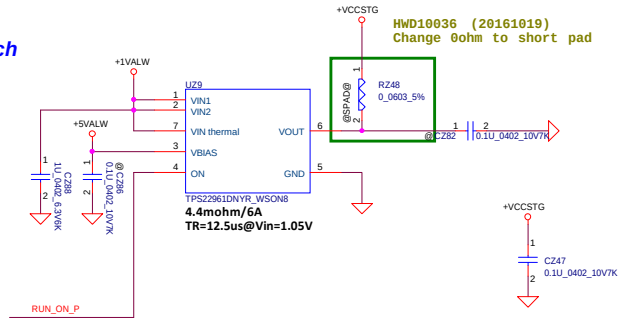
Date: Wednesday, October 26, 2016 | Sheet 32 of 75

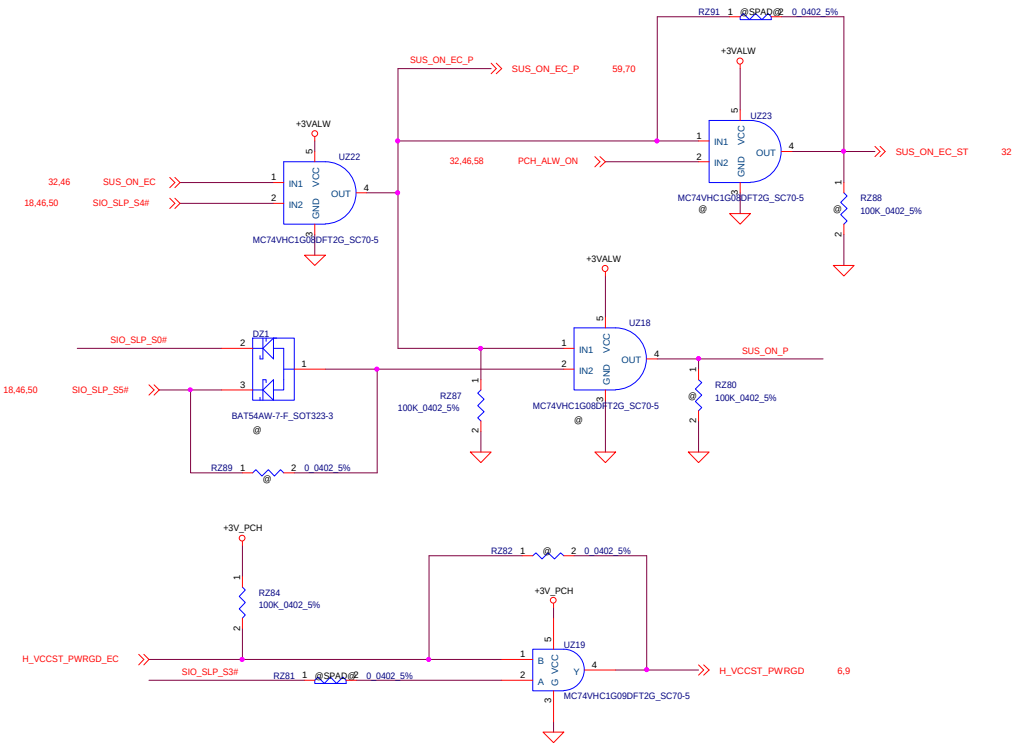
DDR4 VPP Load Switch

20160623 delete DDR4 VPP load switch change to PW p70

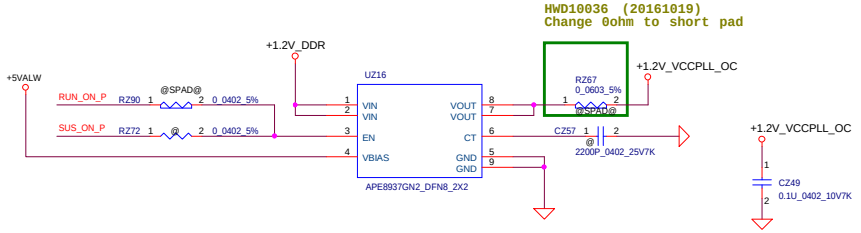


+VCCSTG Load Switch





+VCCPLL_OC Load Switch



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

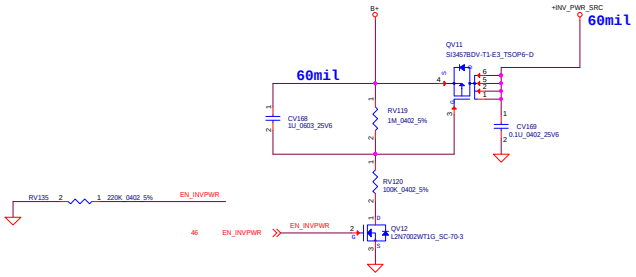
Compal Electronics, Inc.

Title: **EC ENE-KB9012/ KC3810**

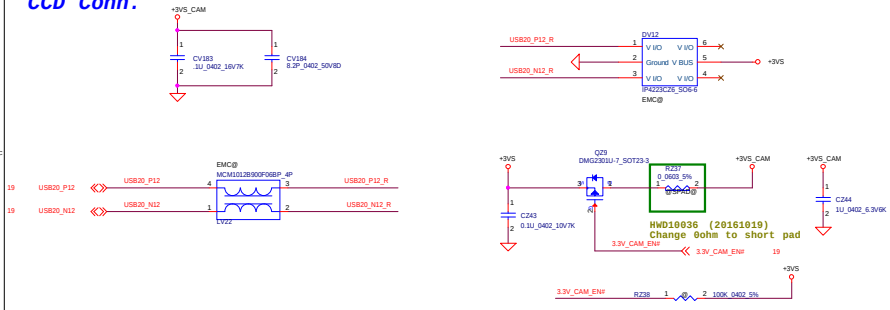
Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 33 of 75

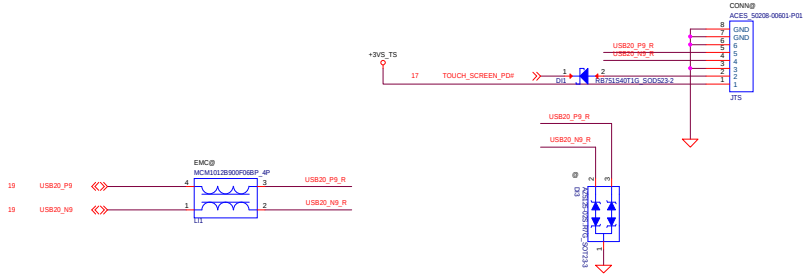
LCD backlight PWR CTRL



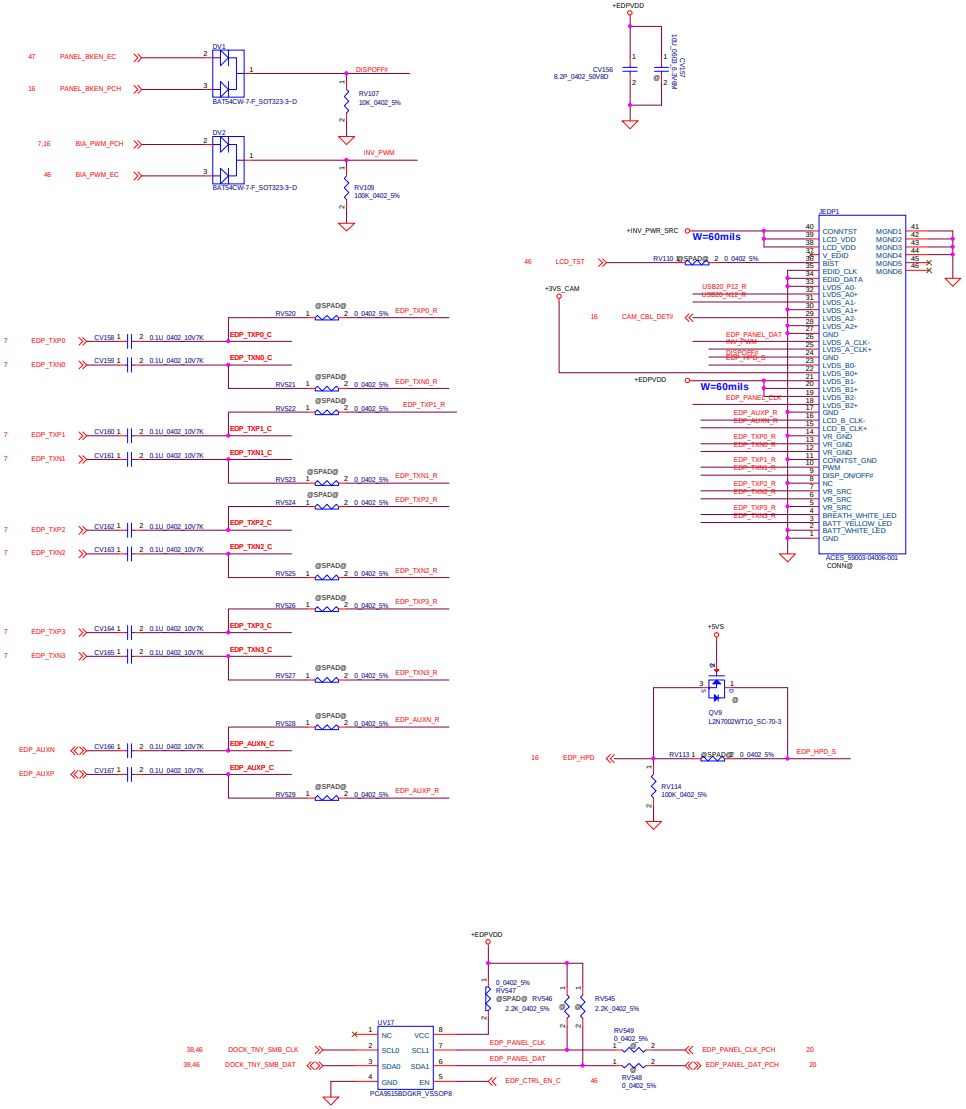
CCD Conn.



Touch Screen Conn.



eDP & TS Conn.

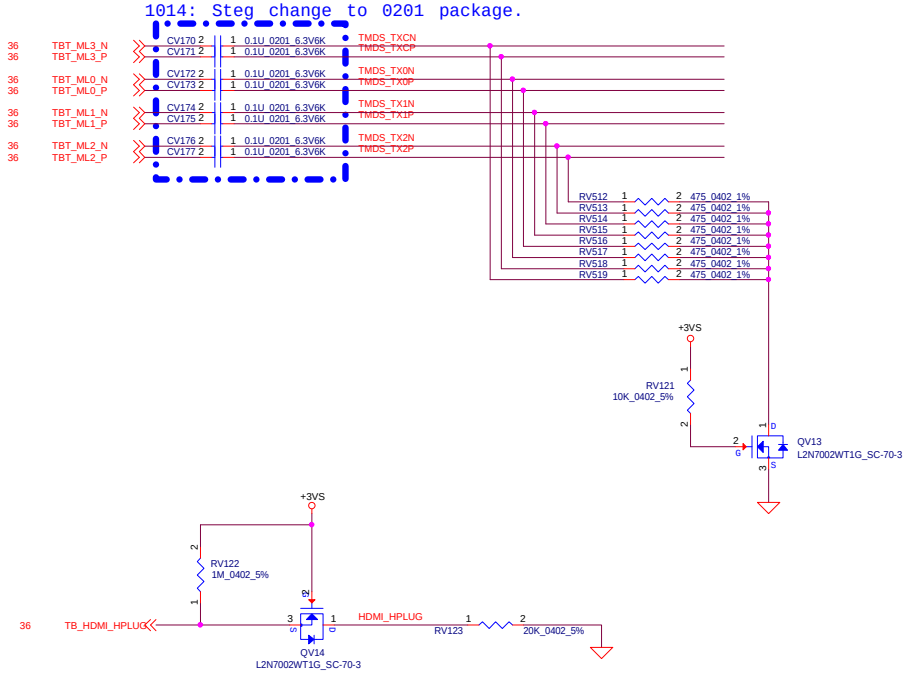


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: eDP /TS conn.			
Size:	Document Number: LA-E331P		Rev: 0.1(XX)
Date: Wednesday, October 26, 2016		Sheet 34 of 75	

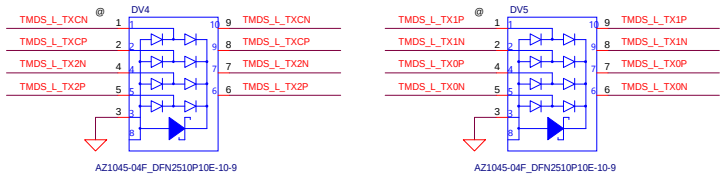
HDMI Active Level Shift(ALS type)

1014: Steg change to 0201 package.

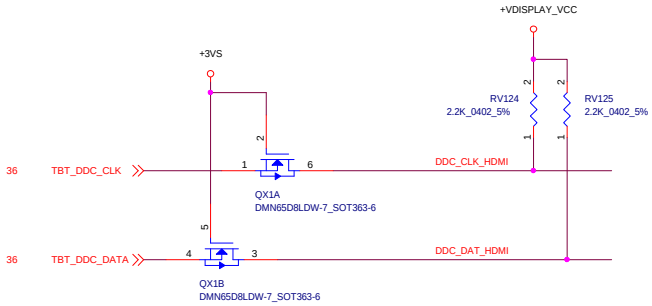


Place between ESD and CM-Choke

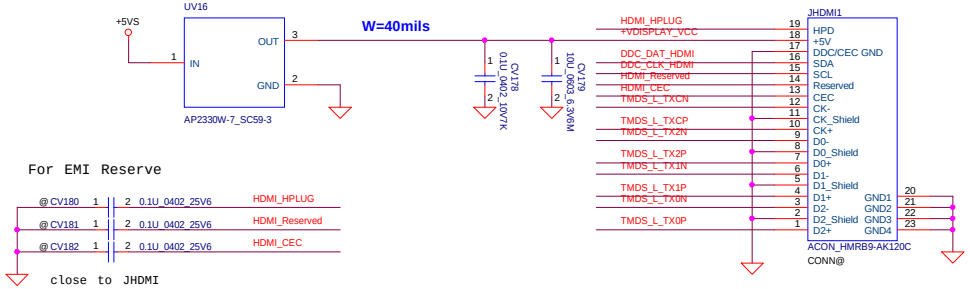
Place close to JHDMI1



HDMI DDC



HDMI conn



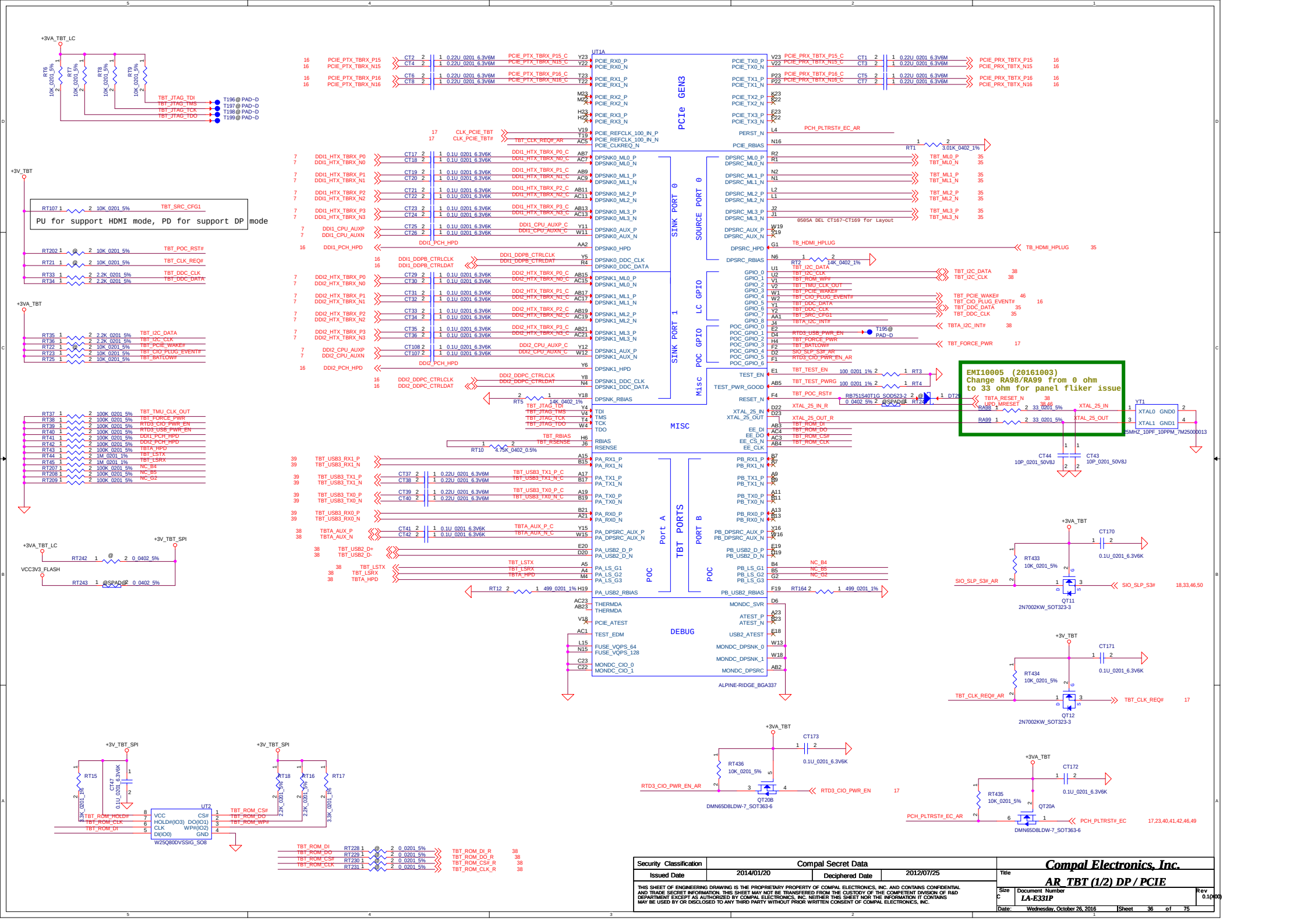
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: HDMI

Size: Custom | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 35 of 75



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2012/07/25

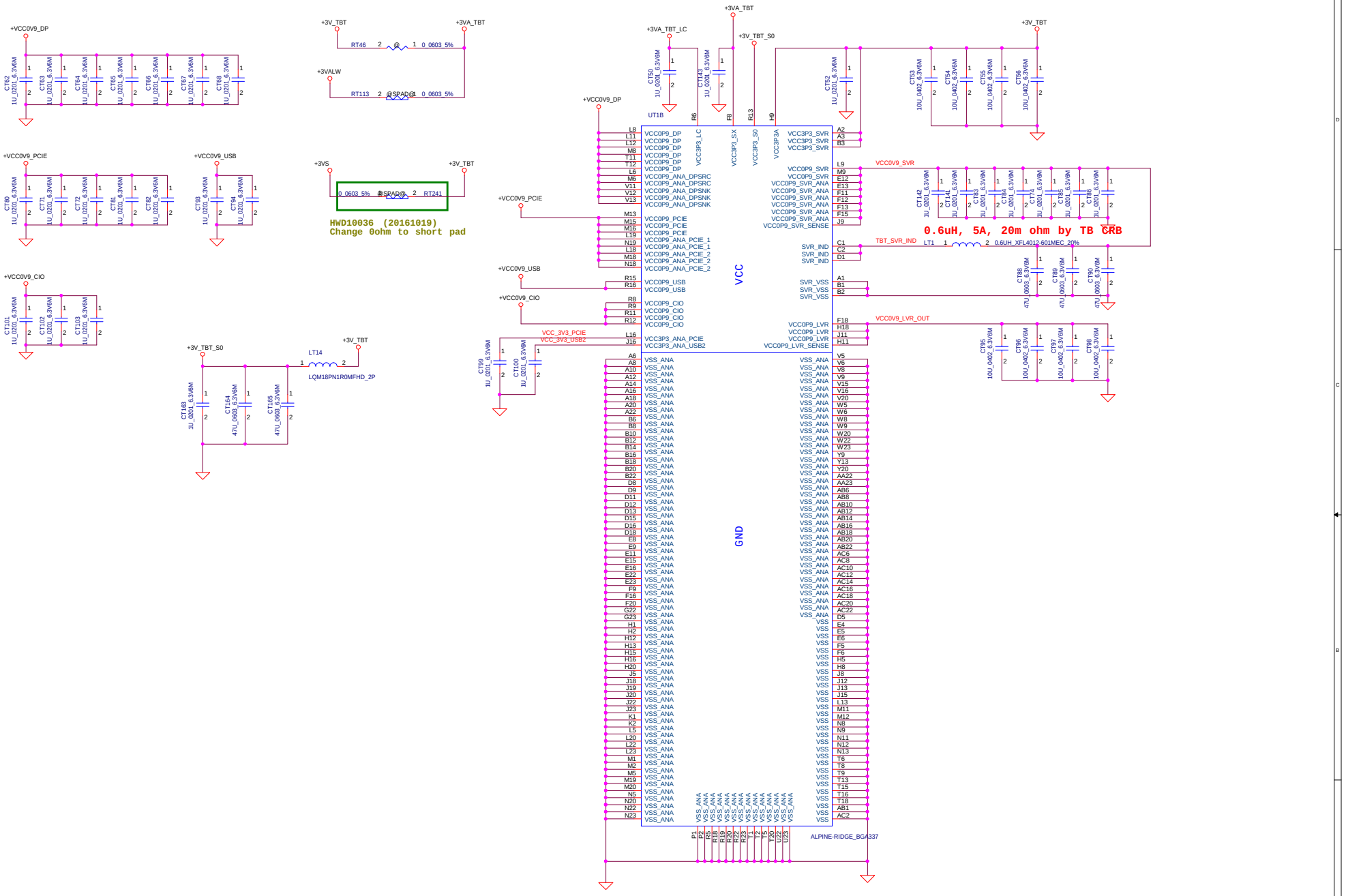
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **AR_TBT (1/2) DP / PCIE**

Size	Document Number	Rev
C	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 36 of 75



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2012/07/25

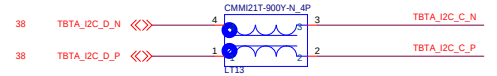
Compal Electronics, Inc.

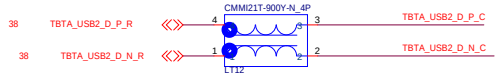
Title: AR_TBT (2/2) PWR / GND

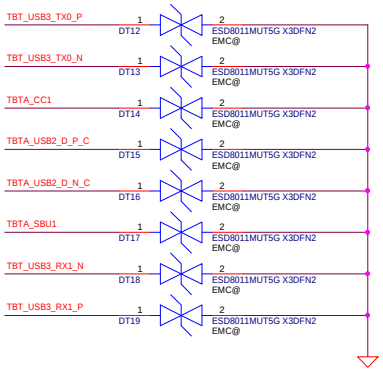
Size	Document Number	Rev
C	LA-E331P	0.1(000)

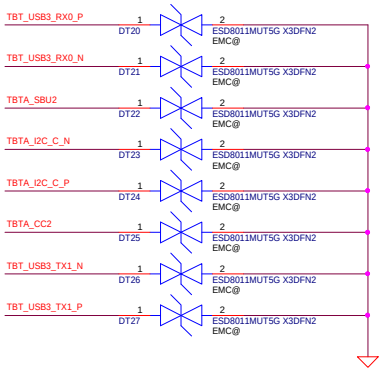
Date: Wednesday, October 26, 2016 | Sheet 37 of 75

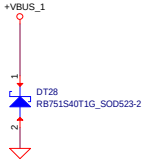
+5VALW
VCC5V0_SYS
RT165 1 @SPAD@2 0 0805 5%
VCC5V0_SYS
CT147 22U_0603_6.3V6M
CT148 22U_0603_6.3V6M
CT149 22U_0603_6.3V6M
CT150 22U_0603_6.3V6M
+3V_VC
CT161 10U_0402_6.3V6M
TBTA_LDO_BMC
CT144 2.2U_0402_6.3V6M
VCC3V3_TBT_SX
CT145 1U_0201_6.3V6M
VCC3V3_FLASH
CT146 10U_0402_6.3V6M
VCC1V8A_TBTA_LDO
CT151 2.2U_0402_6.3V6M
VCC1V8D_TBTA_LDO
CT152 2.2U_0402_6.3V6M
PP_HV
CT155 4.7U_0603_25V6K
+VBUS_1
CT153 1U_0603_25V6
+3VA_TBT
RT167 1 2 10K_0201_5% TBTA_I2C_INT#
VCC3V3_FLASH
RT168 1 2 3.3K_0201_1% PD_EE_CS#
RT169 1 2 3.3K_0201_1% PD_EE_DO
RT170 1 2 3.3K_0201_1% PD_EE_WP#
RT171 1 2 3.3K_0201_1% PD_HOLD#
RT432 1 2 100K_0201_5% TBTA_AUX_N
RT431 1 2 100K_0201_5% TBTA_AUX_P
0504A modify By Intel
PP_HV
RT1092 1 2 0_0603_5%
VCC5V0_SYS
+3VALW
RT1095 1 2 0_0402_5%
+3V_VC
RT1094 1 @ 2 0_0402_5%
UT4
PP_HV
PP_CABLE
VDDIO
VIN_3V3
36 TBT_I2C_DATA
36 TBT_I2C_CLK
36 TBTA_I2C_INT#
I2C_SDA1
I2C_SCL1
I2C_IRQ1_N
UPD_SMBDAT
UPD_SMBCLK
I2C_SDA2
I2C_SCL2
46 PD_I2C_ALERT#
I2C_IRQ2_N
PD_EE_CLK
PD_EE_DI
PD_EE_DO
PD_EE_CS#
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS_N
36 TBT_USB2_D+
36 TBT_USB2_D-
USB_RP_P
USB_RP_N
36 TBTA_AUX_P
36 TBTA_AUX_N
AUX_P
AUX_N
@ PAD~D T193
@ PAD~D T194
SWD_CLK
SWD_DATA
RT430 1 2 1M_0201_1%
UART_TX
UART_RX
36 TBT_LSTX
36 TBT_LSRX
LSTX/R2P
LSRX/P2R
VCC3V3_FLASH
RT226 1 2 10K_0201_5%
RT227 1 2 10K_0201_5%
DEBUG_CTL1
DEBUG_CTL2
34,46 DOCK_TNY_SMB_CLK
34,46 DOCK_TNY_SMB_DAT
RT184 1 @SPAD@2 0_0402_5% TBTA_DEBUG1
RT185 1 @SPAD@2 0_0402_5% TBTA_DEBUG2
DEBUG1
DEBUG2
TBT_LSTX
TBT_LSRX
RT233 1 @ 20_0201_5%
RT232 1 @ 20_0201_5%
TBTA_DEBUG3_LSTX
TBTA_DEBUG4_LSRX
DEBUG3
DEBUG4
I2C_ADDR
RT187 10K_0201_5%
RT188 100K_0201_5%
RT190 0_0402_5%
@SPAD@
TPS65982D_BGA96
TBTA_HRESET
RT429 100K_0402_5%
TBTA_HRESET might be connected to EC or PCH to allow TPS65982 FW load
0505A modify By TI
0506A DEL QT21 /RT1094
0501A modify By TI
SENSEP
SENSEN
HV_GATE1
HV_GATE2
T191 PAD~D @
T192 PAD~D @
VBUS
TBTA_VBUS_L
LT11 EMC@ HCB2012KF-121T50_2P
CT157 1U_0603_25V6
DT10 AZ4024-02S_SOT23-3-D EMC@
+VBUS_1
@ DT174 1U_0603_25V6
close to +VBUS_1
VOUT_3V3
LDO_3V3
LDO_1V8A
LDO_1V8D
LDO_BMC
VCC3V3_TBT_SX
VCC3V3_FLASH
VCC1V8A_TBTA_LDO
VCC1V8D_TBTA_LDO
TBTA_LDO_BMC
C_CC1
C_CC2
CT160 220P_0402_50V7K
CT159 220P_0402_50V7K
TBTA_CC1 39
TBTA_CC2 39
RPD_G1
RPD_G2
C_USB_TP
C_USB_TN
TBTA_USB2_D_P_R 39
TBTA_USB2_D_N_R 39
C_USB_BP
C_USB_BN
TBTA_I2C_D_P 39
TBTA_I2C_D_N 39
C_SBU1
C_SBU2
TBTA_PD_SBU1
TBTA_PD_SBU2
RT176 1 @SPAD@2 0_0402_5%
RT177 1 @SPAD@2 0_0402_5%
TBTA_SBU1 39
TBTA_SBU2 39
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
RT178 1 @SPAD@2 0_0402_5%
RT437 1 2 1M_0201_1%
EN_PD_HV 55
RT181 1 @SPAD@2 0_0402_5%
TBTA_HPD 36
RT182 1 @SPAD@2 0_0402_5%
PWR_BTN_DOCK1#
TBT_CONFIG
T185 PAD~D @
T187 PAD~D @
T200 PAD~D @
MRESET
RESET_N
BUSPOWER_N
R_OSC
SS
RT245 1 @ 2 0_0201_5%
RT186 1 2 100K_0201_5%
UPD_MRESET 36,46
TBTA_RESET_N 36
RT189 1 @ 2 0_0402_5%
VCC3V3_FLASH
RT246 1 @ 2 0_0402_5%
VCC1V8A_TBTA_LDO
RT199 1 2 0_0402_5%
RT191 15K_0402_0.1%
CT158 0.22U_0402_10V6K
+3VA_TBT
RT194 100K_0402_5%
PWR_BTN_DOCK1#
QV89 L2N7002WT1G_SC-70-3
RT195 1 @SPAD@2 0_0402_5%
PWR_TB_DOCK# 46
the PD RST will keep low,
it will let PD work abnormal.[Ex. Type-c adapter plug in]
HRESET | D6 | Digital I/O | Hi-Z | Active high hardware reset input. Assertion will cause a reboot sequence. Ground pin when HRESET functionality will not be used.
c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design.
When 82D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).
LDO_3V3
ADC
CONFIG
R1 1%
R2 1%
If External SPI Connected use "Infinite Retry" Setting by pulling CONFIG (GPIO 8) to LDO_3V3
Figure 78. Factory Configuration Resistor Divider
Table 13. Factory Device Configuration Selection
DIV = R2/(R1+R2) (1)
DIV_min | DIV_max | Factory Device Configuration | Description
0.70 | 1.00 | 7 | Infinite boot retry from Flash to Host I/F cycles.
VCC3V3_FLASH
RT1093 10K_0402_1%
TBT_CONFIG
RT183 100K_0402_1%
36 TBT_ROM_CLK_R
36 TBT_ROM_DI_R
36 TBT_ROM_DO_R
36 TBT_ROM_CS#_R
RT210 1 @ 2 0_0201_5% PD_EE_CLK
RT211 1 @ 2 0_0201_5% PD_EE_DI
RT212 1 @ 2 0_0201_5% PD_EE_DO
RT213 1 @ 2 0_0201_5% PD_EE_CS#
VCC3V3_FLASH
UT5
PD_HOLD#
PD_EE_CLK
PD_EE_DI
VCC
/HOLD/IO3
CLK
DI/IO0
/CS
DO/IO1
/WP/IO2
GND
PD_EE_CS#
PD_EE_DO
PD_EE_WP#
W25Q32FVSSIQ_SO8
23,46 UPD_GPU_SMBDAT
RT200 1 @SPAD@2 0_0402_5% UPD_SMBDAT
23,46 UPD_GPU_SMBCLK
RT201 1 @SPAD@2 0_0402_5% UPD_SMBCLK
Security Classification: Compal Secret Data
Issued Date: 2011/08/25
Deciphered Date: 2012/07/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title: PCH (7/8) PWR
Size: Document Number: LA-E331P
Rev: 0.1(000)
Date: Wednesday, October 26, 2016
Sheet 38 of 75

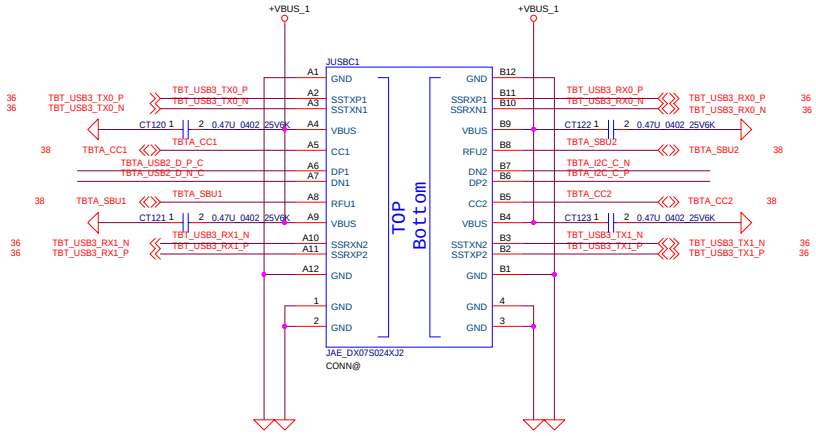












Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2012/07/25

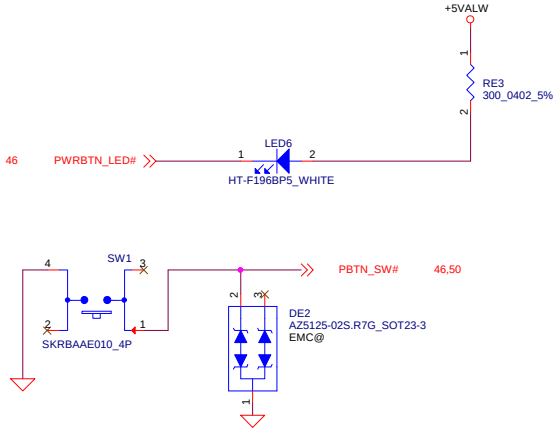
Compal Electronics, Inc.

Title: **PD USB TYPE-C**

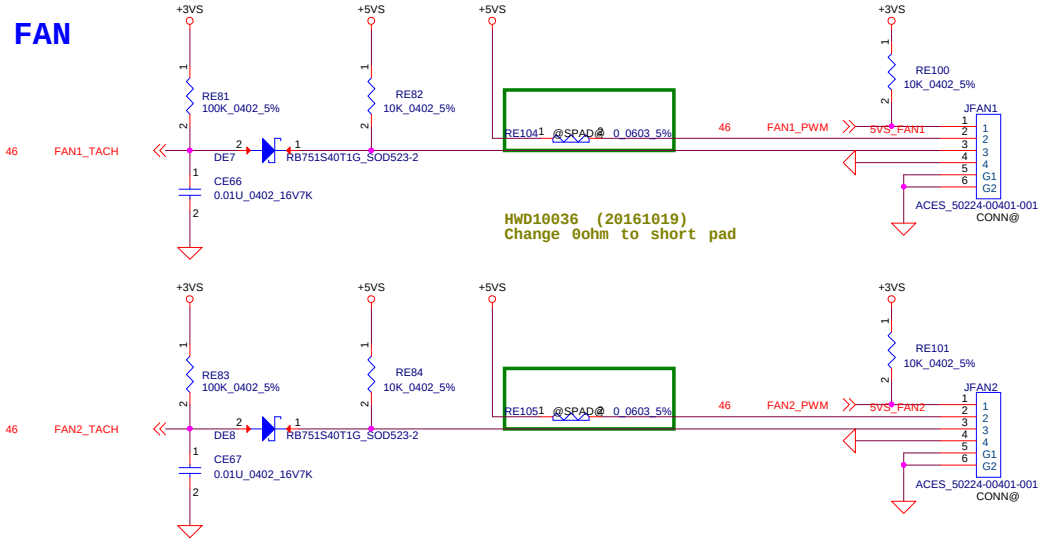
Size	Document Number	Rev
C	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 39 of 75

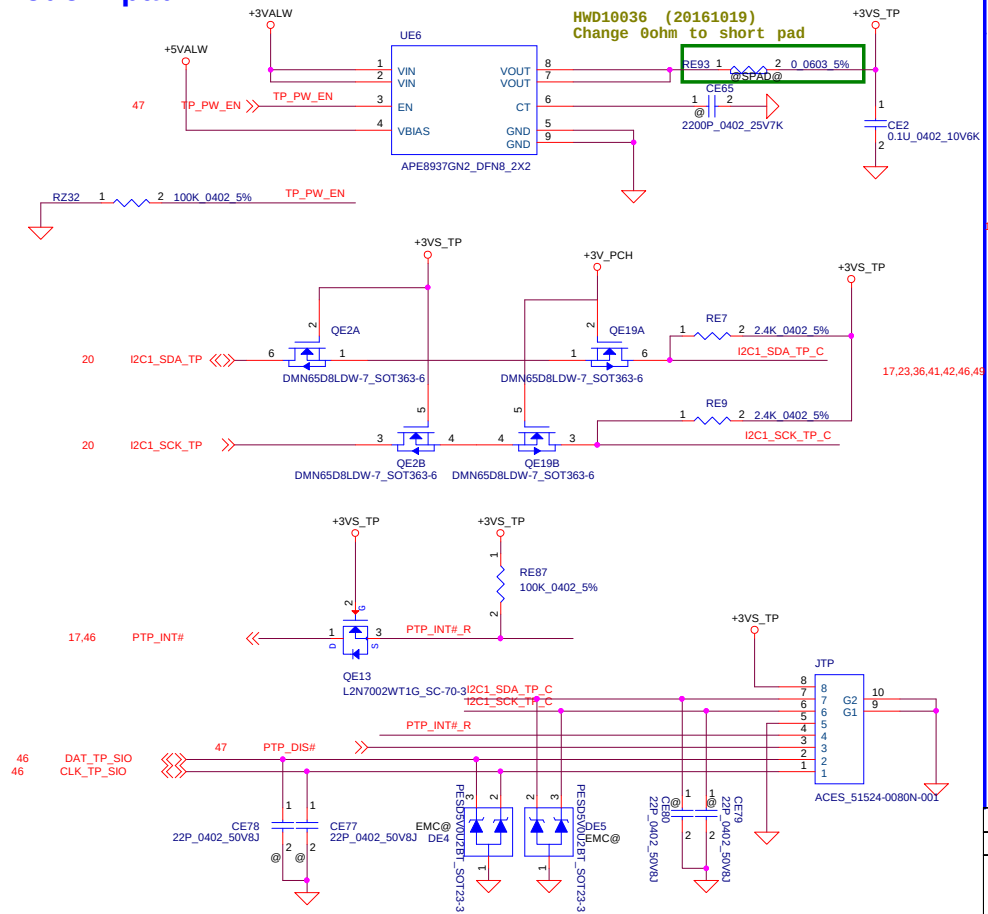
Power Button and LED



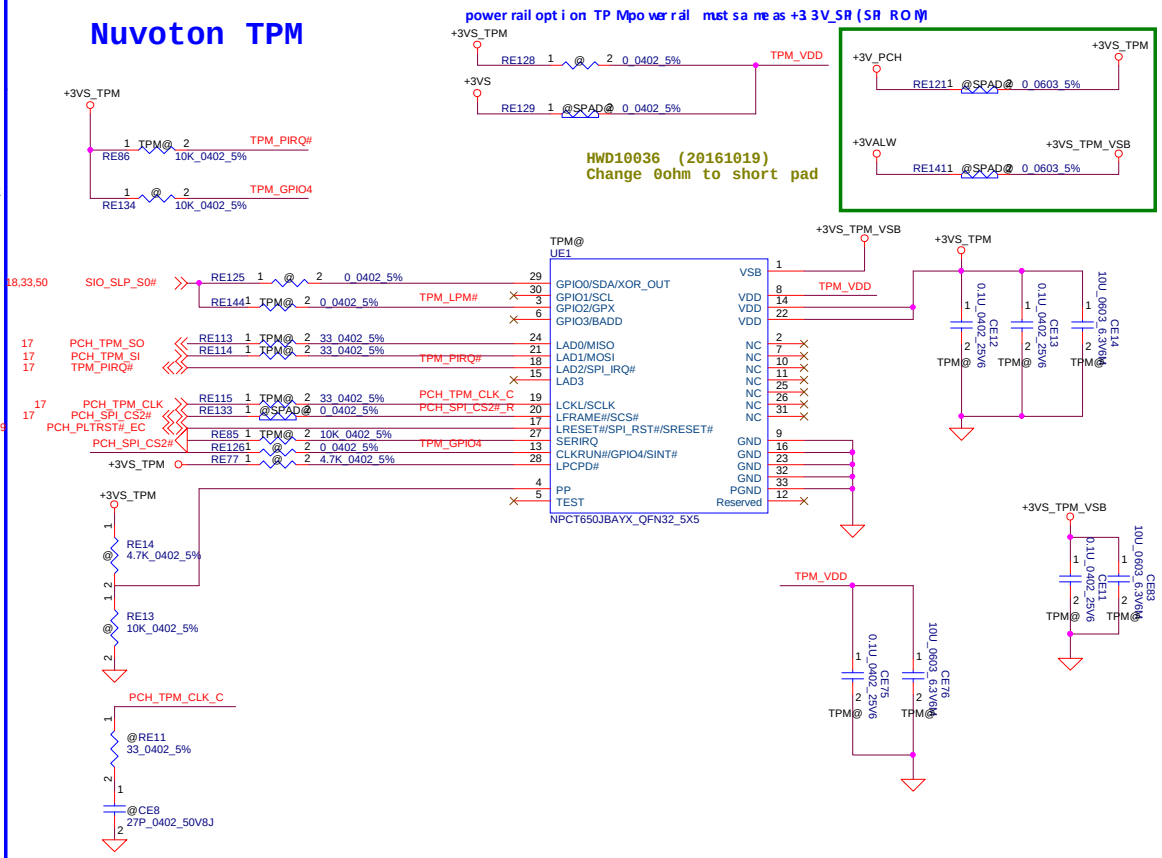
PWM FAN



Touch pad



Nuvoton TPM



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

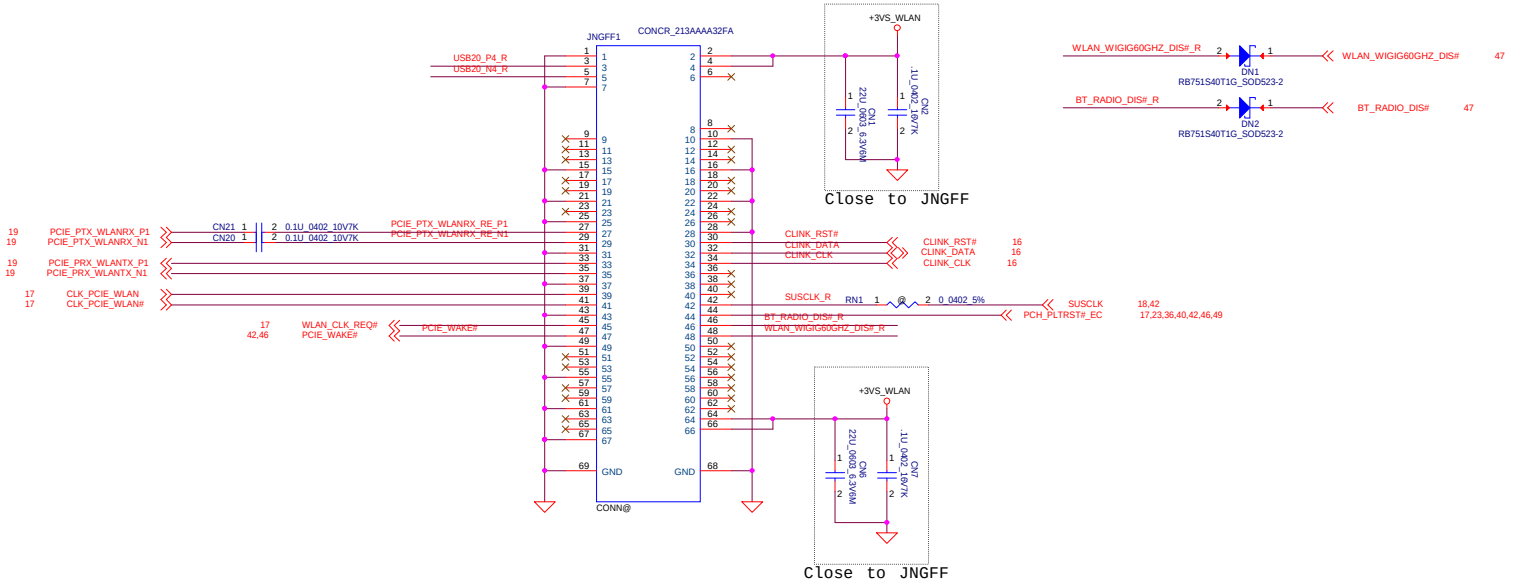
Compal Electronics, Inc.

Title: **FAN/TP/KB/PWR SW**

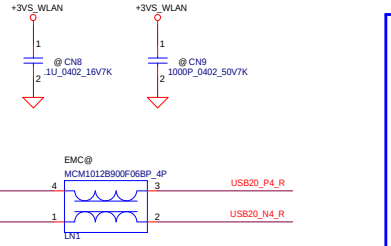
Size	Document Number	Rev
Custom	LA-E331P	0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 40 of 75

M.2 Slot-A Key-A (WLAN + BT)

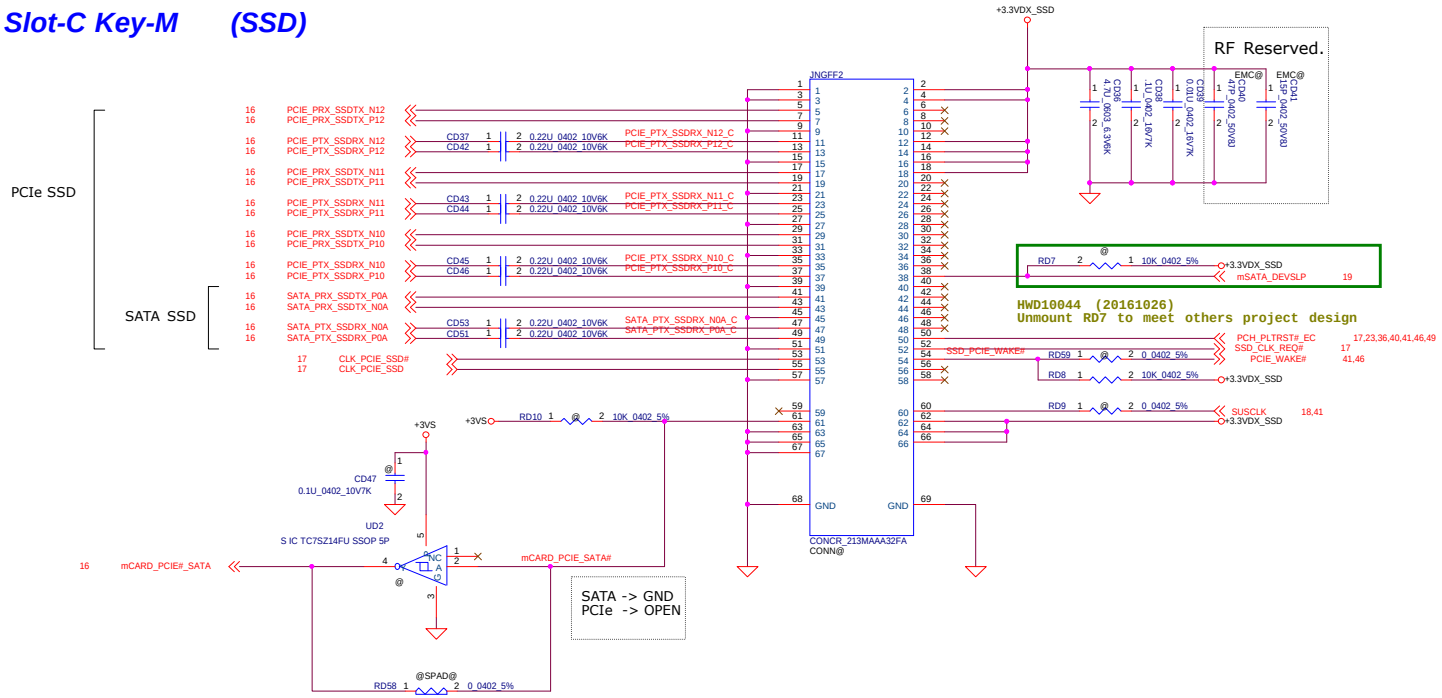


Reserve for EMI



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	NGFF		
Size C	Document Number LA-E331P		Rev 0.1(000)
Date: Wednesday, October 26, 2016	Sheet 41 of 75		

M.2 Slot-C Key-M (SSD)



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

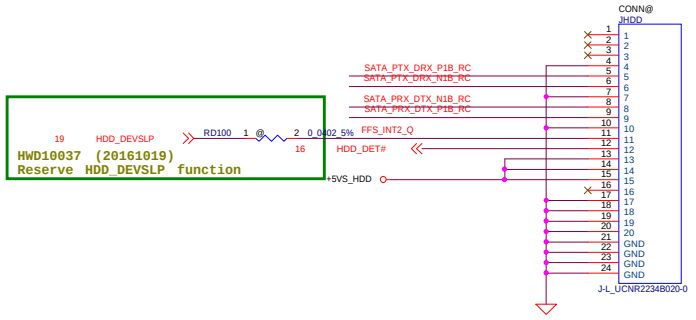
Compal Electronics, Inc.

Title: SSD

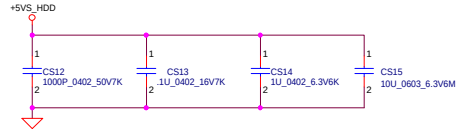
Size	Document Number	Rev
C	LA-E331P	0.1(000)

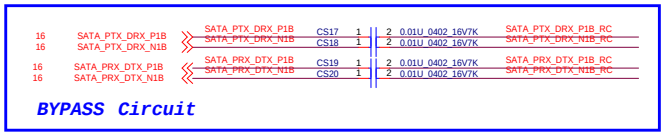
Date: Wednesday, October 26, 2016 | Sheet 42 of 75

HDD CONN

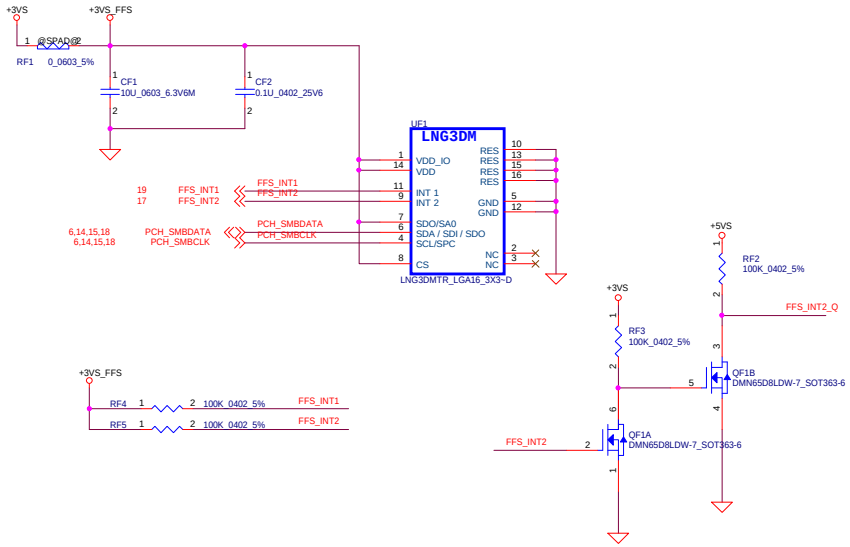


Place near HDD CONN (JHDD1)





Free Fall Sensor



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DC/DC INTERFACE**

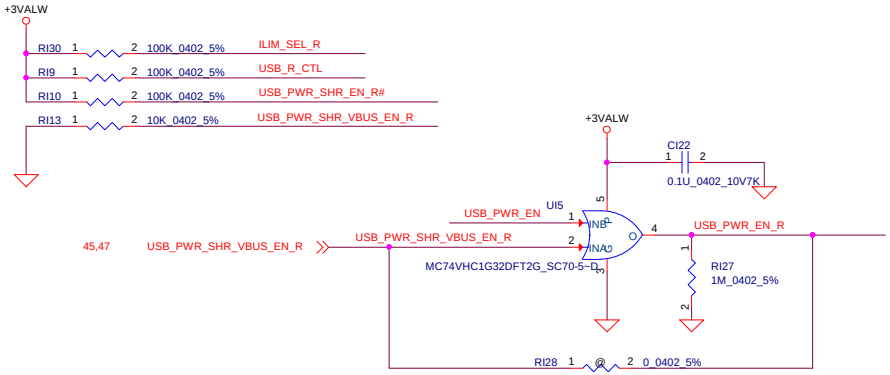
Size	Document Number	Rev
C	LA-E331P	0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 43 of 75

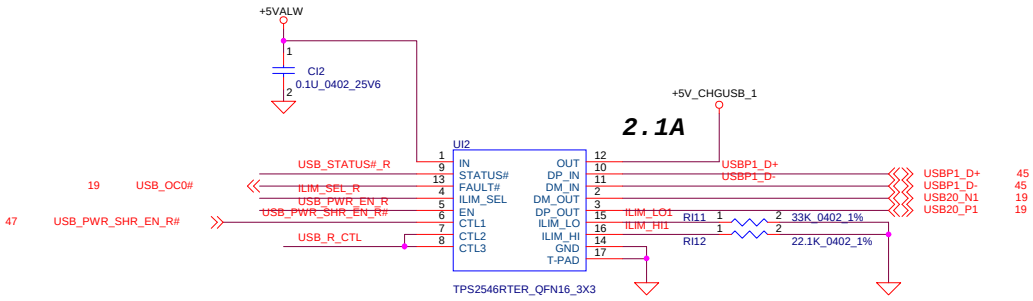
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

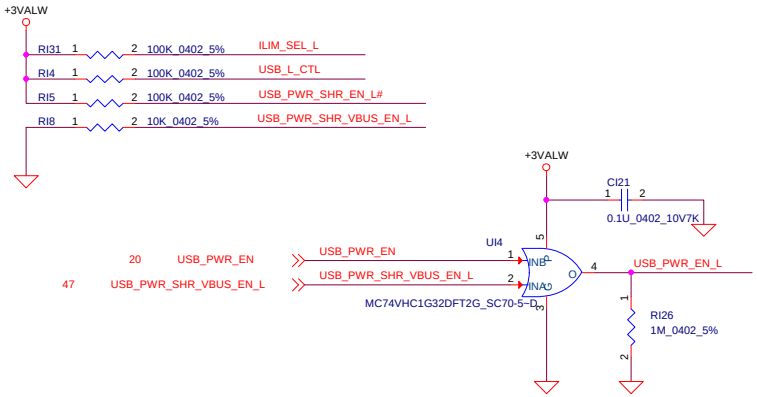
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

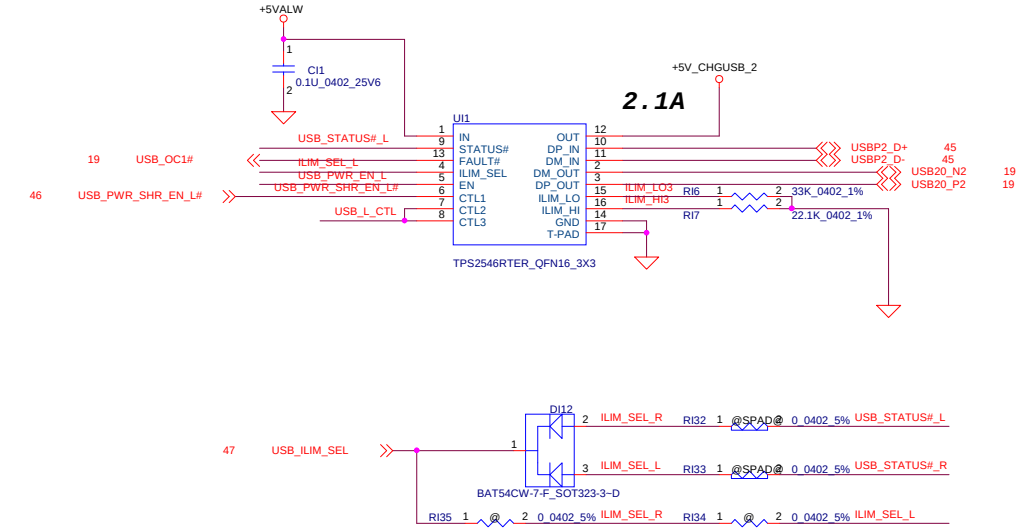


USB3.0 / USB2.0 Port1 (Right Side)



USB3.0 / USB2.0 Port2 (Left Side)





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: USB Powershare

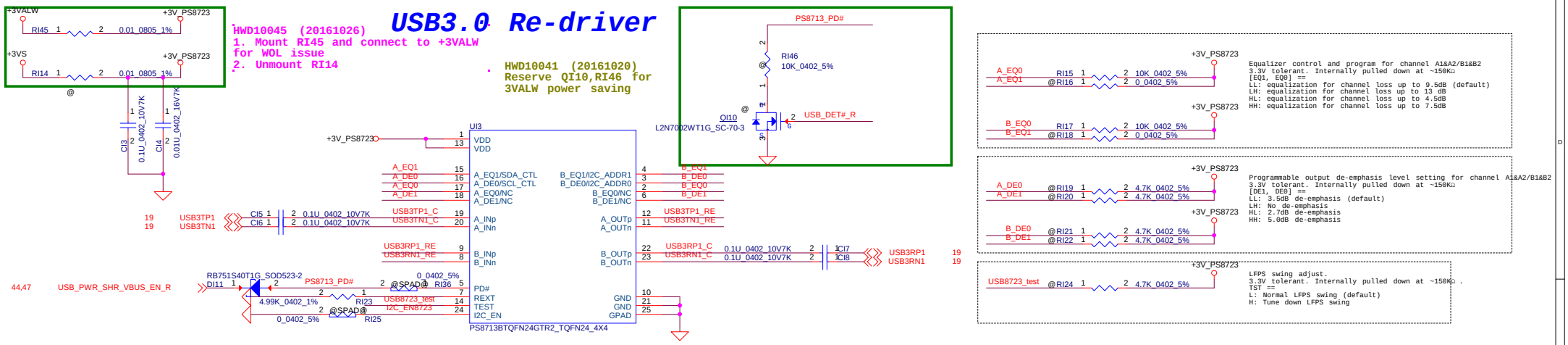
Size | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 44 of 75

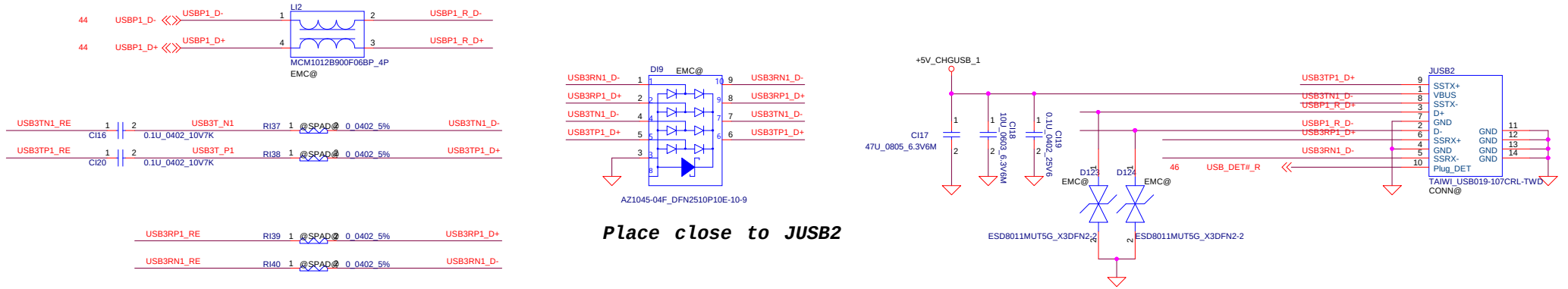
USB3.0 Re-driver

HWD10045 (20161026)
1. Mount RI45 and connect to +3VALW for WOL issue
2. Unmount RI14

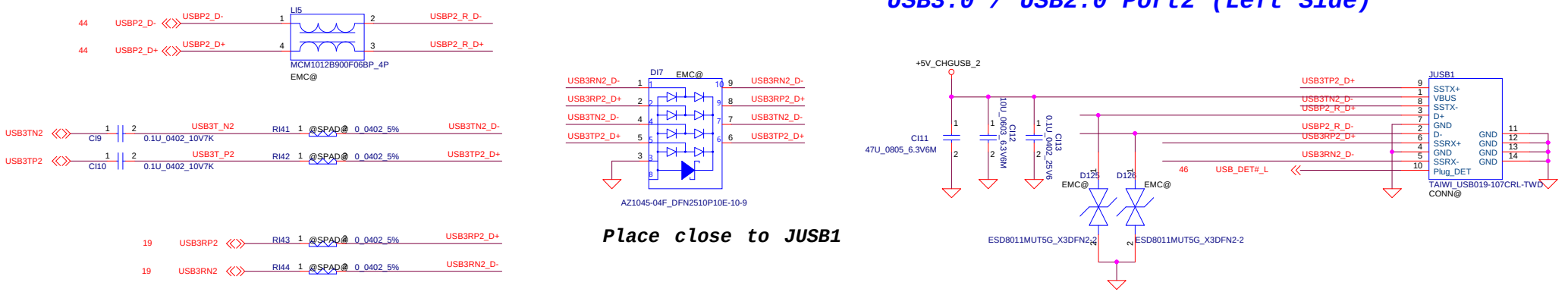
HWD10041 (20161020)
Reserve QI10,RI46 for 3VALW power saving



USB3.0 / USB2.0 Port1 (Right Side)



USB3.0 / USB2.0 Port2 (Left Side)



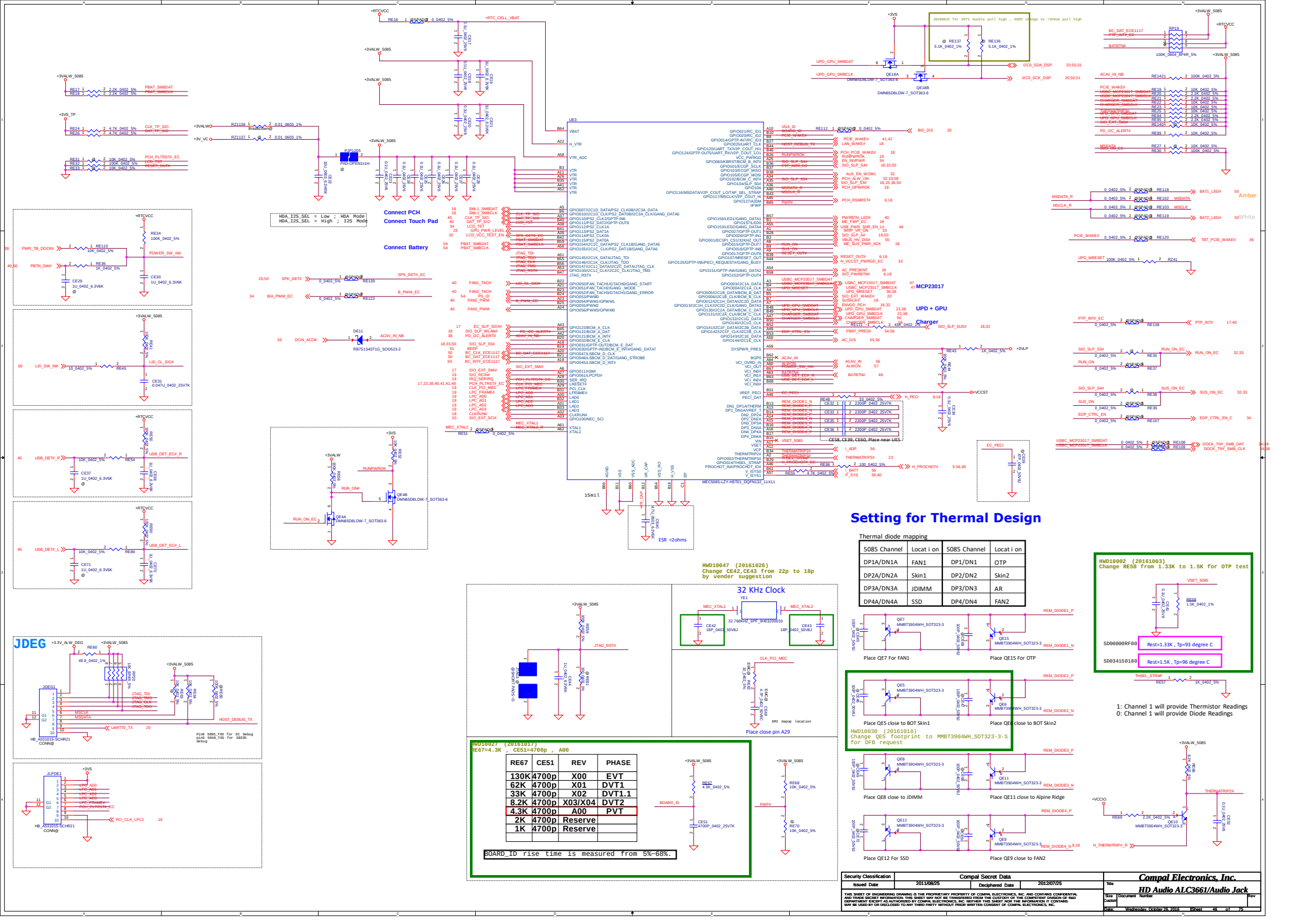
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

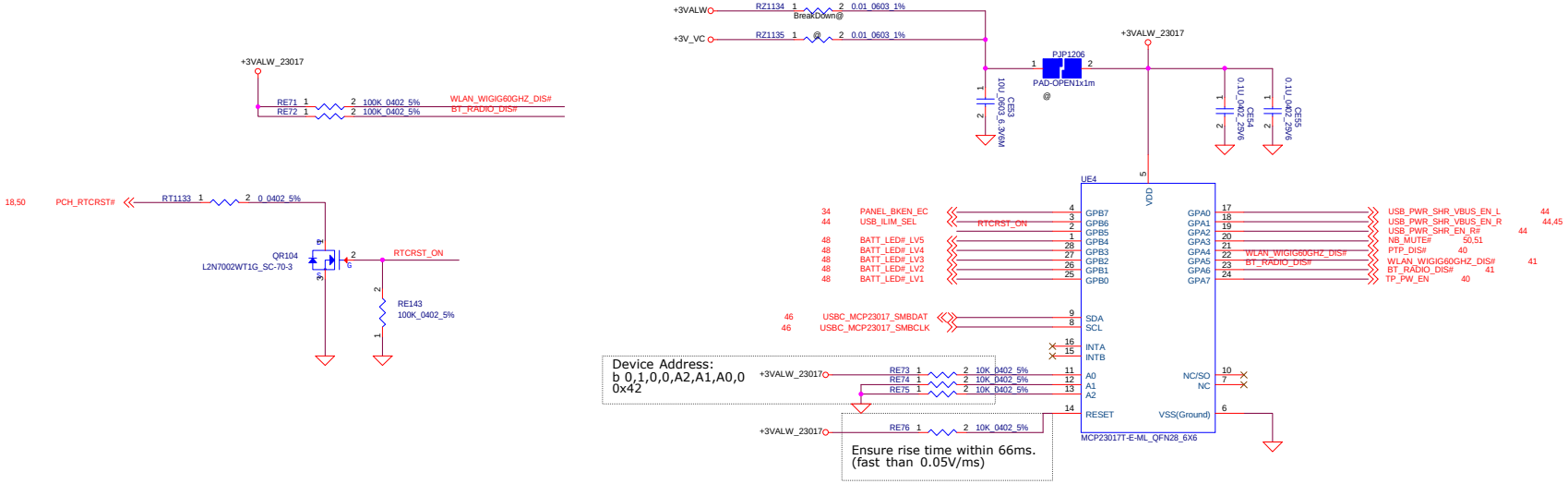
Compal Electronics, Inc.

Title: USB conn.

Size | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 45 of 75


Connect PCH
Connect Touch Pad
Connect Battery
HDA_I2S_SEL = Low ; HDA Mode
HDA_I2S_SEL = High ; I2S Mode
MCP23017
UPD + GPU
Charger
ESR <2ohms
Setting for Thermal Design
Thermal diode mapping
5085 Channel | Locat i on | 5085 Channel | Locat i on
DP1A/DN1A | FAN1 | DP1/DN1 | OTP
DP2A/DN2A | Skin1 | DP2/DN2 | Skin2
DP3A/DN3A | JDIMM | DP3/DN3 | AR
DP4A/DN4A | SSD | DP4/DN4 | FAN2
Place QE7 For FAN1
Place QE15 For OTP
Place QE5 close to BOT Skin1
Place QE6 close to BOT Skin2
Place QE8 close to JDIMM
Place QE11 close to Alpine Ridge
Place QE12 For SSD
Place QE9 close to FAN2
HWD10047 (20161026)
Change CE42,CE43 from 22p to 18p
by vender suggestion
32 KHz Clock
Place close pin A29
HWD10027 (20161017)
RE67=4.3K , CE51=4700p , A00
RE67 | CE51 | REV | PHASE
130K | 4700p | X00 | EVT
62K | 4700p | X01 | DVT1
33K | 4700p | X02 | DVT1.1
8.2K | 4700p | X03/X04 | DVT2
4.3K | 4700p | A00 | PVT
2K | 4700p | Reserve |
1K | 4700p | Reserve |
BOARD_ID rise time is measured from 5%~68%.
HWD10002 (20161003)
Change RE58 from 1.33K to 1.5K for OTP test
SD00000RF00 Rest=1.33K , Tp=93 degree C
SD034150180 Rest=1.5K , Tp=96 degree C
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings
HWD10030 (20161018)
Change QE5 footprint to MMBT3904WH_SOT323-3-S
for DFB request
JDEG
Compal Electronics, Inc.
HD Audio ALC3661/Audio Jack
Compal Secret Data
2011/08/25
2012/07/25
Wednesday, October 26, 2016



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/21

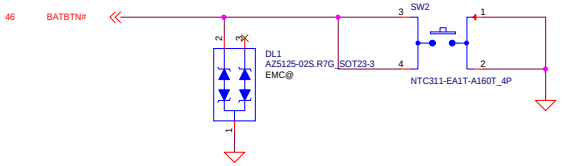
Compal Electronics, Inc.

Title: AMP TPA3113/SPK conn.

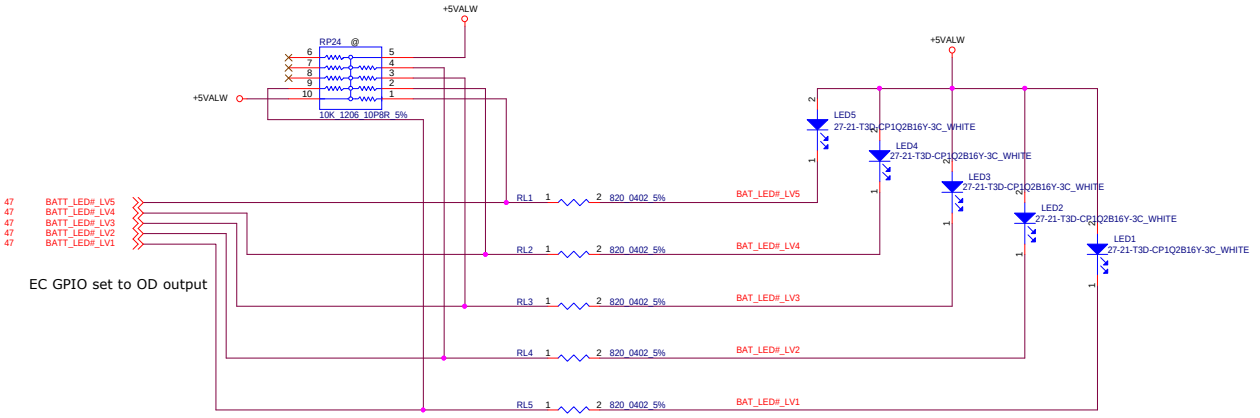
Size	Document Number	Rev
C	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 Sheet 47 of 75

BATT LED Power Button

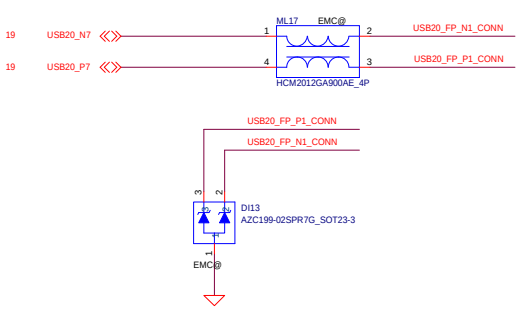


Battery Gauge LED

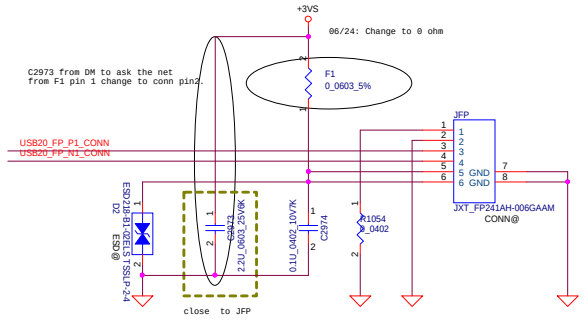


Finger Print circuit

Fingerprint Reader CONN



(Fingerprint Reader)
Current capability: 3.3V 150mA

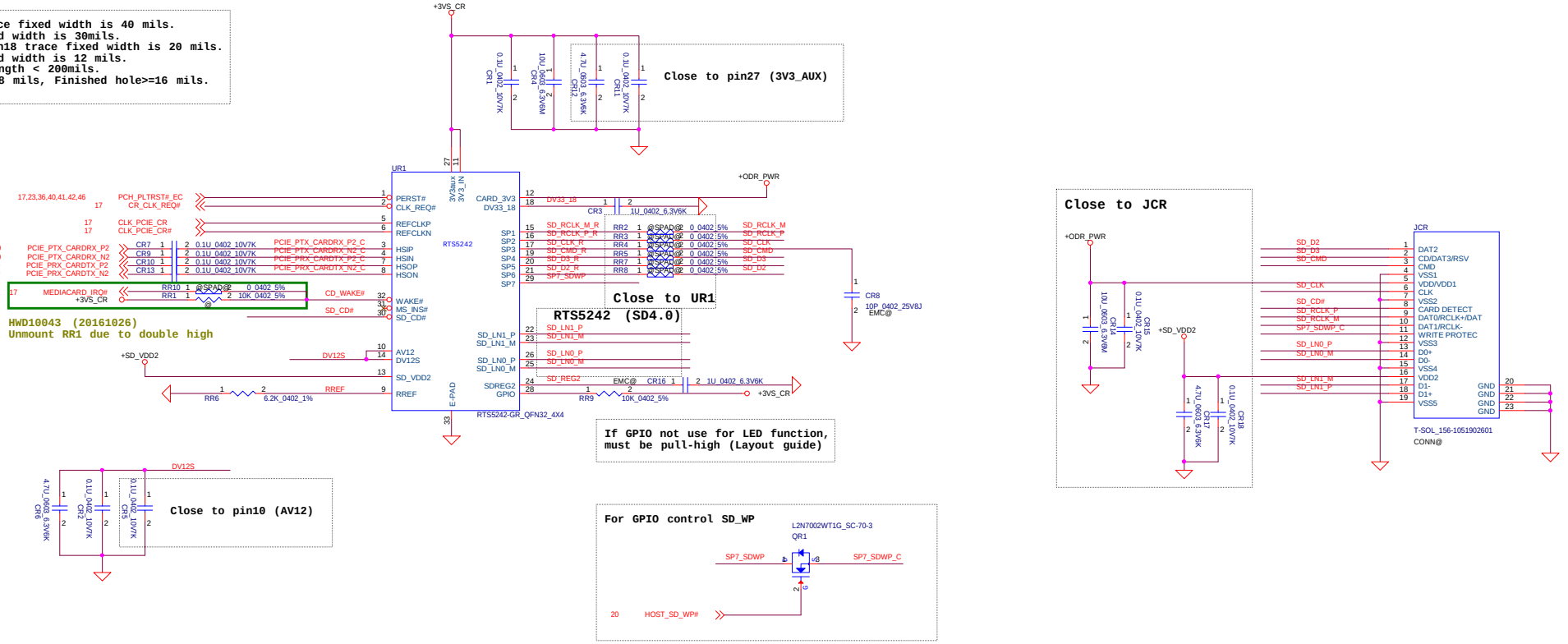


12/10 : JFPR1 Follow ME P/N and CIS SP01001Y900
12/28 : FPR connect pin define mirror vertically for BOT side

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/15
Title	LED indicator		
Size C	Document Number LA-E331P		Rev 0.1(000)
Date: Wednesday, October 26, 2016	Sheet 48 of 75		

Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

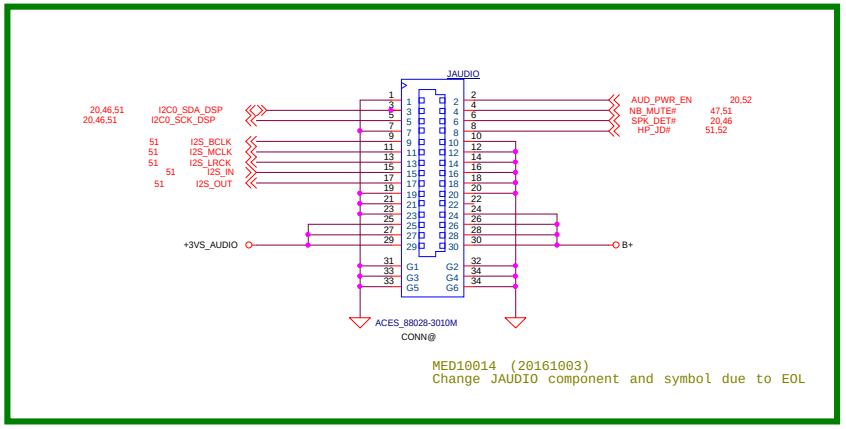
Title: **Card Reader**

Size	Document Number	Rev
		0.1(000)

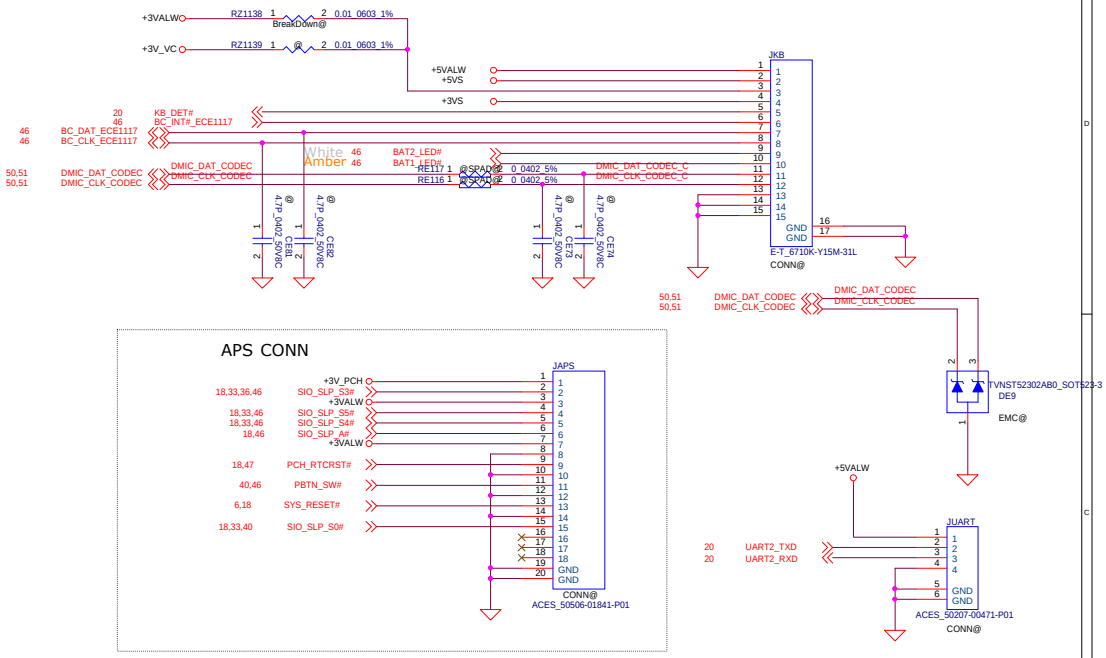
Date: Wednesday, October 26, 2016 | Sheet 49 of 75

AUDIO Board Conn.

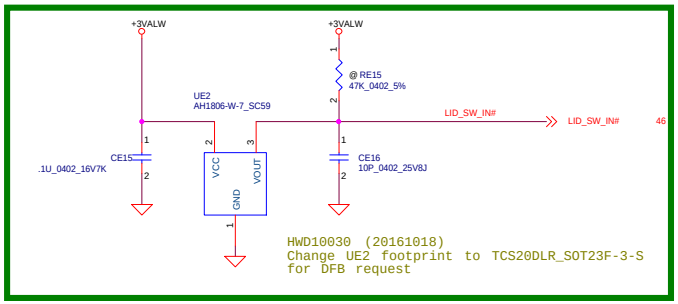
20160415 follow berlinetta broad to broad CONN



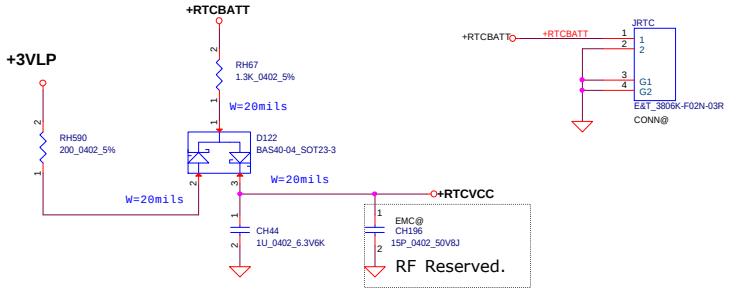
Keyboard Controller board + DMIC



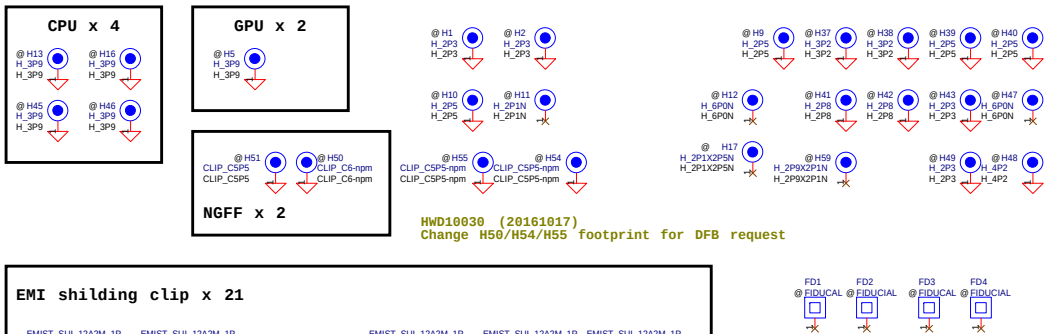
Lid Switch

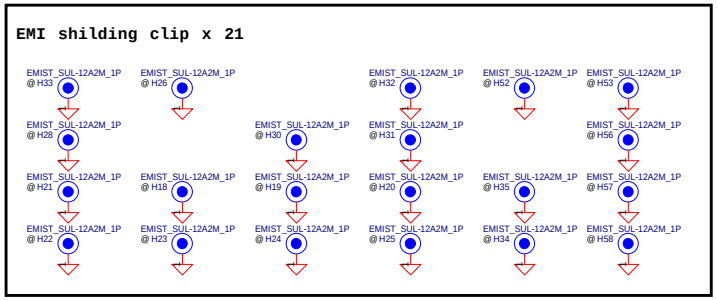


RTC Battery With Charge Function



Screw Hole





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

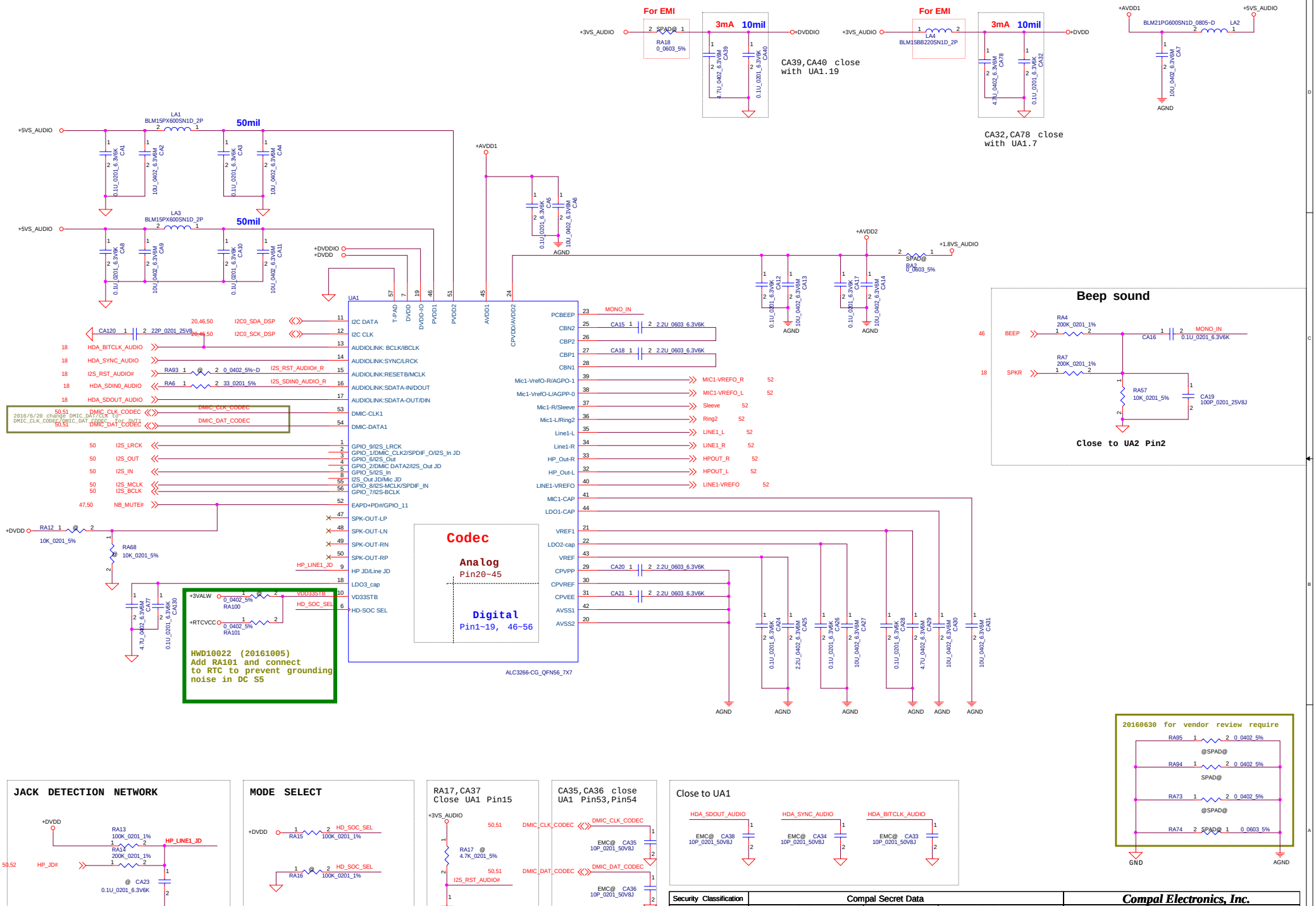
Compal Electronics, Inc.

Title: **TPM/BTB conn.**

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 50 of 75

HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

Compal Electronics, Inc.

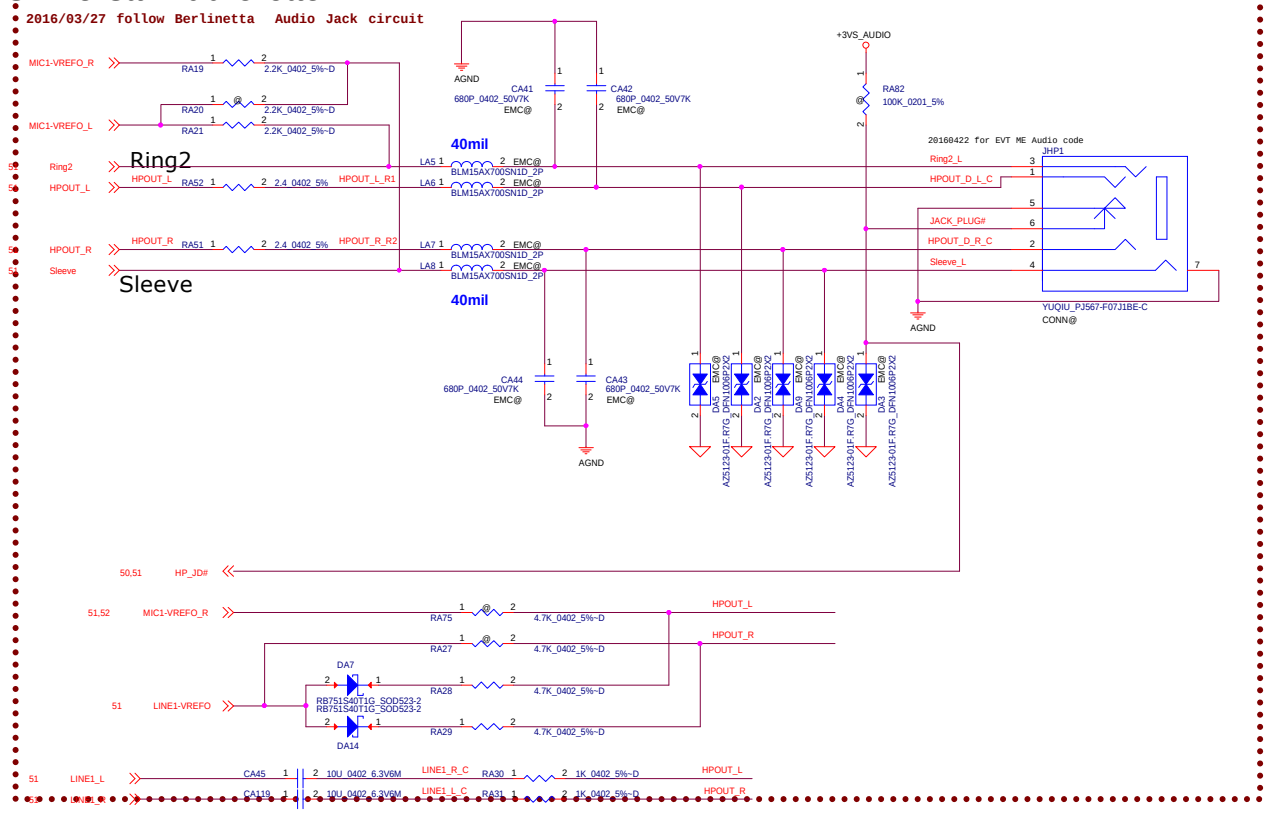
Title: **P21-Audio Codec**

Size | Document Number: **LA-E331P** | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 51 of 75

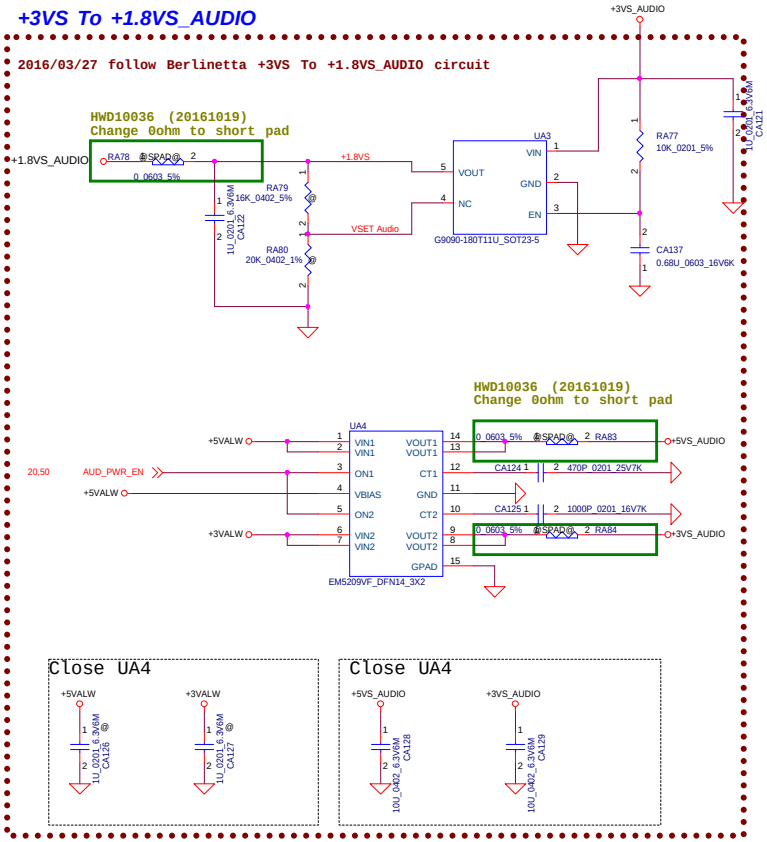
Universal Audio Jack

2016/03/27 follow Berlinetta Audio Jack circuit



+3VS To +1.8VS_AUDIO

2016/03/27 follow Berlinetta +3VS To +1.8VS_AUDIO circuit



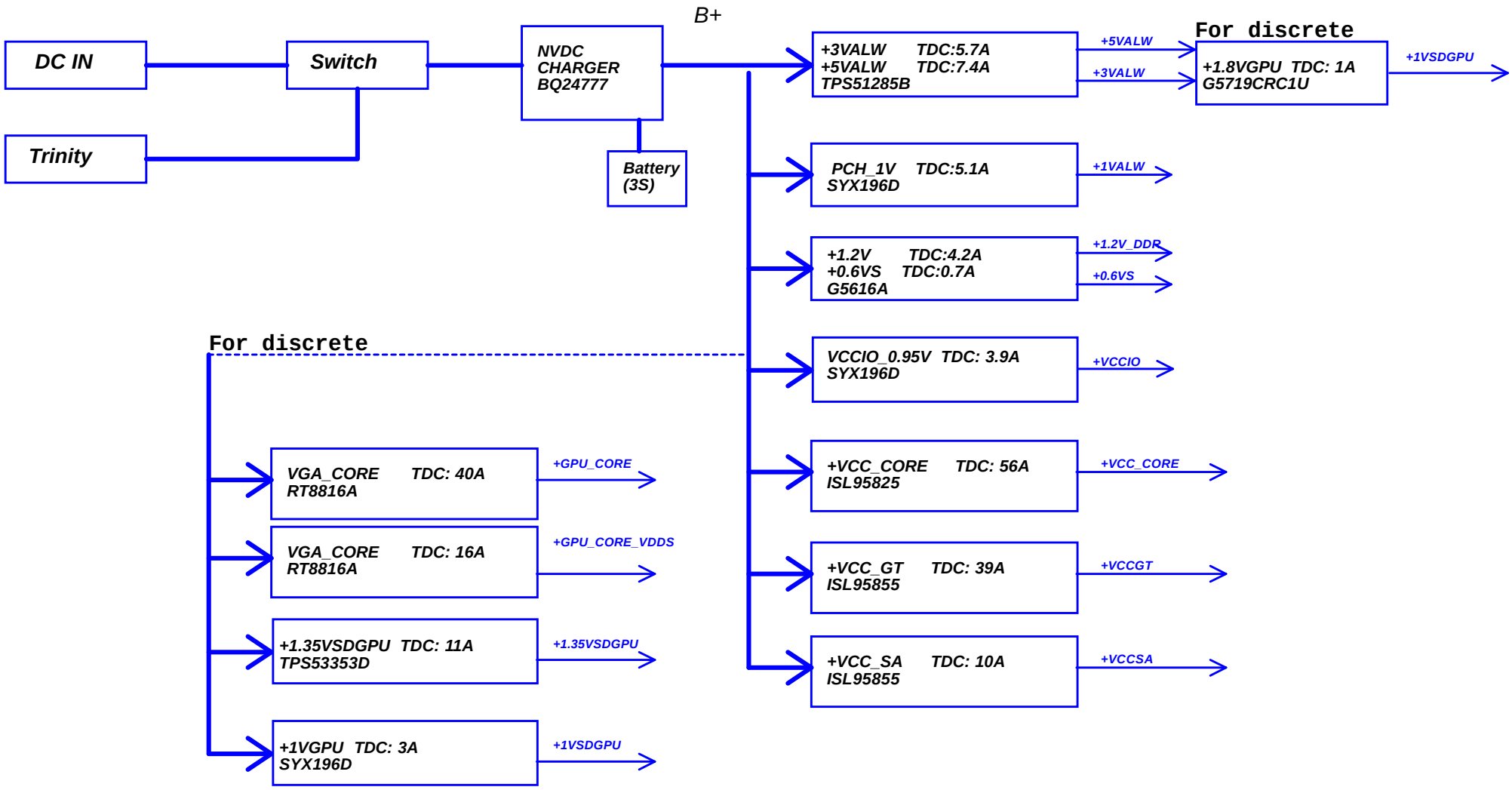
Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P22-Audio Conn

Size	Document Number	Rev
	LA-E331P	0.1(000)

Date: Wednesday, October 26, 2016 Sheet 52 of 75



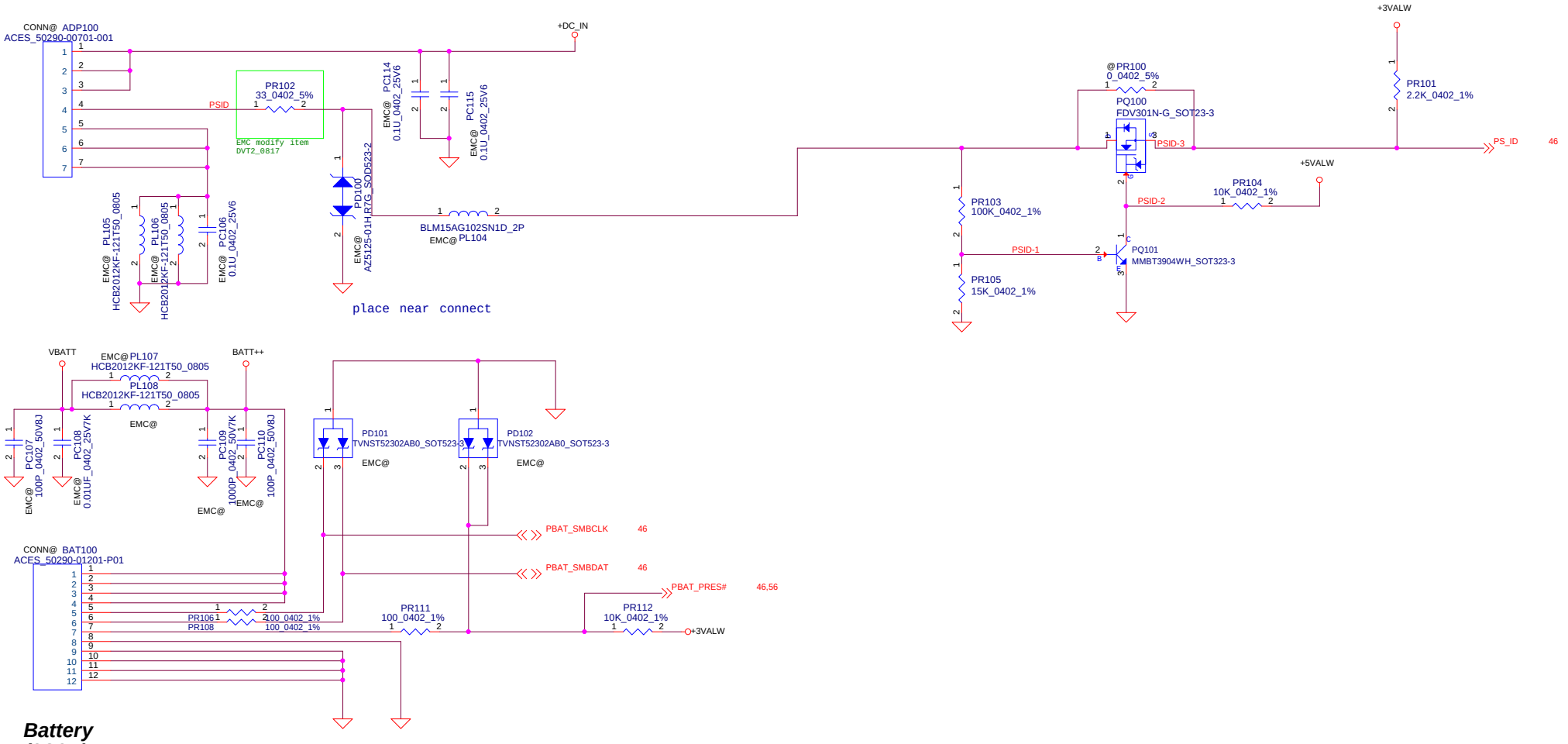
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Power Sequence diagram**

Size	Document Number	Rev
		0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 53 of 75



Battery (3S3P)

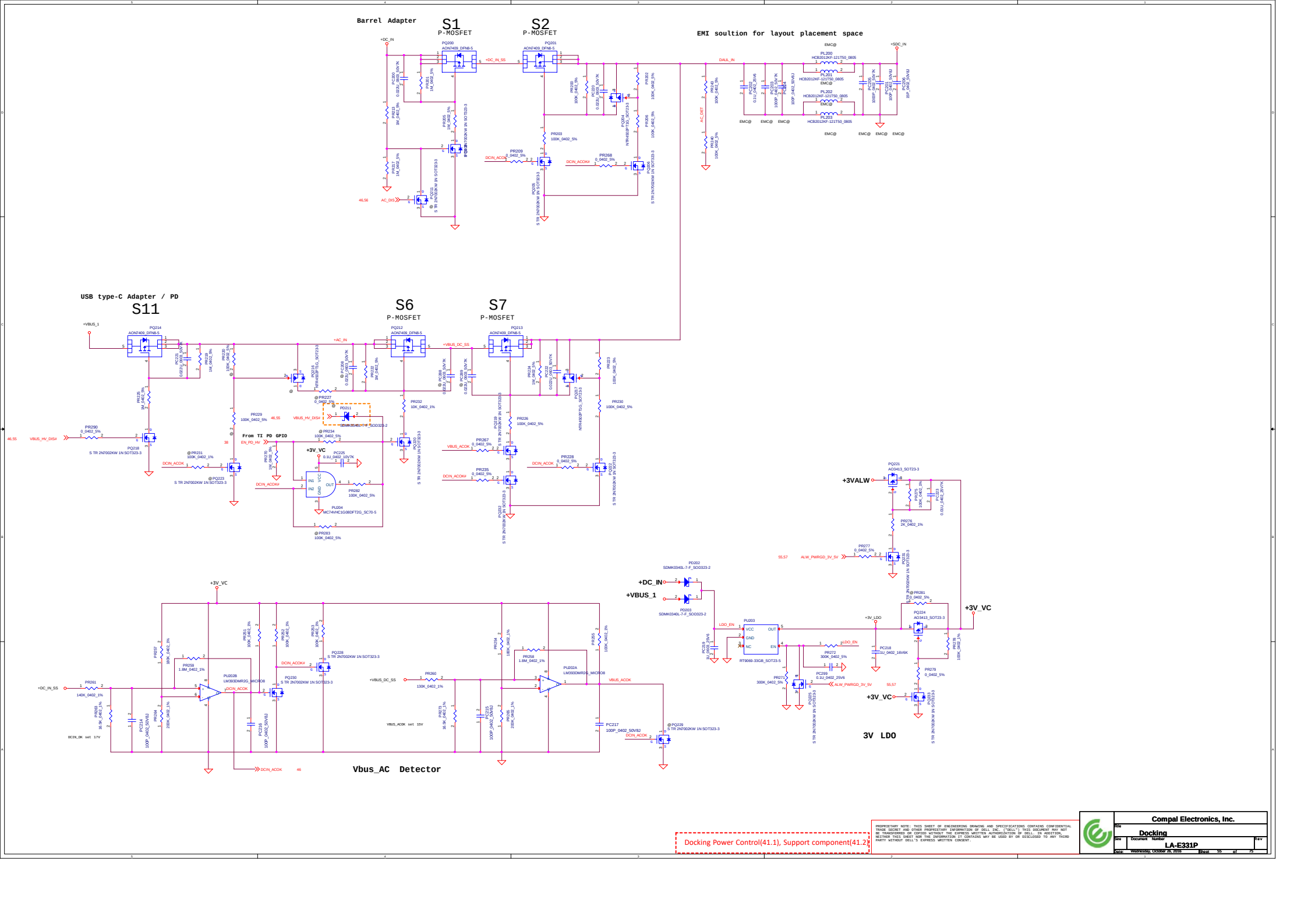
JIMBTY battery connector

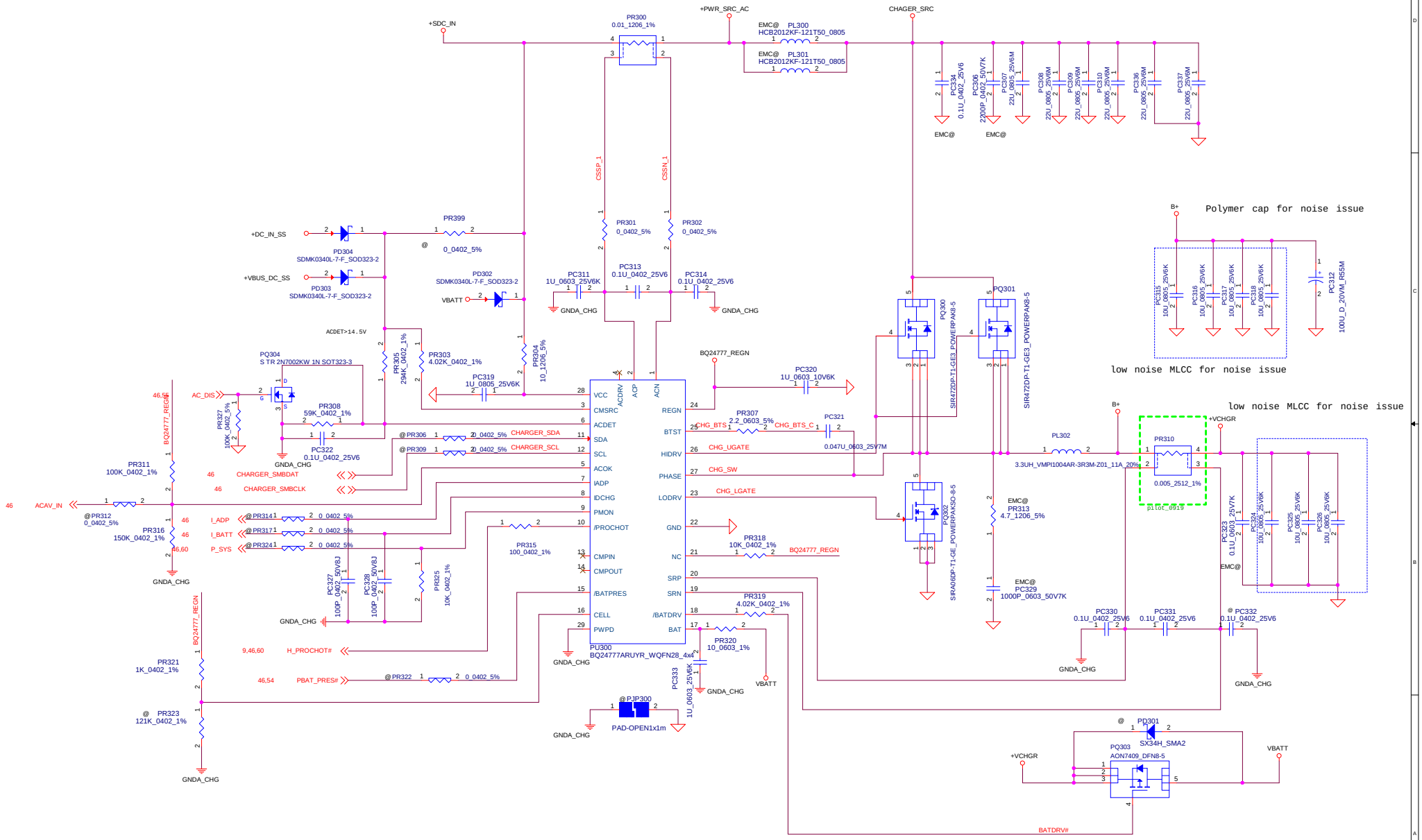
SMART Battery:

01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

Smart Adapter circuit (39.1)

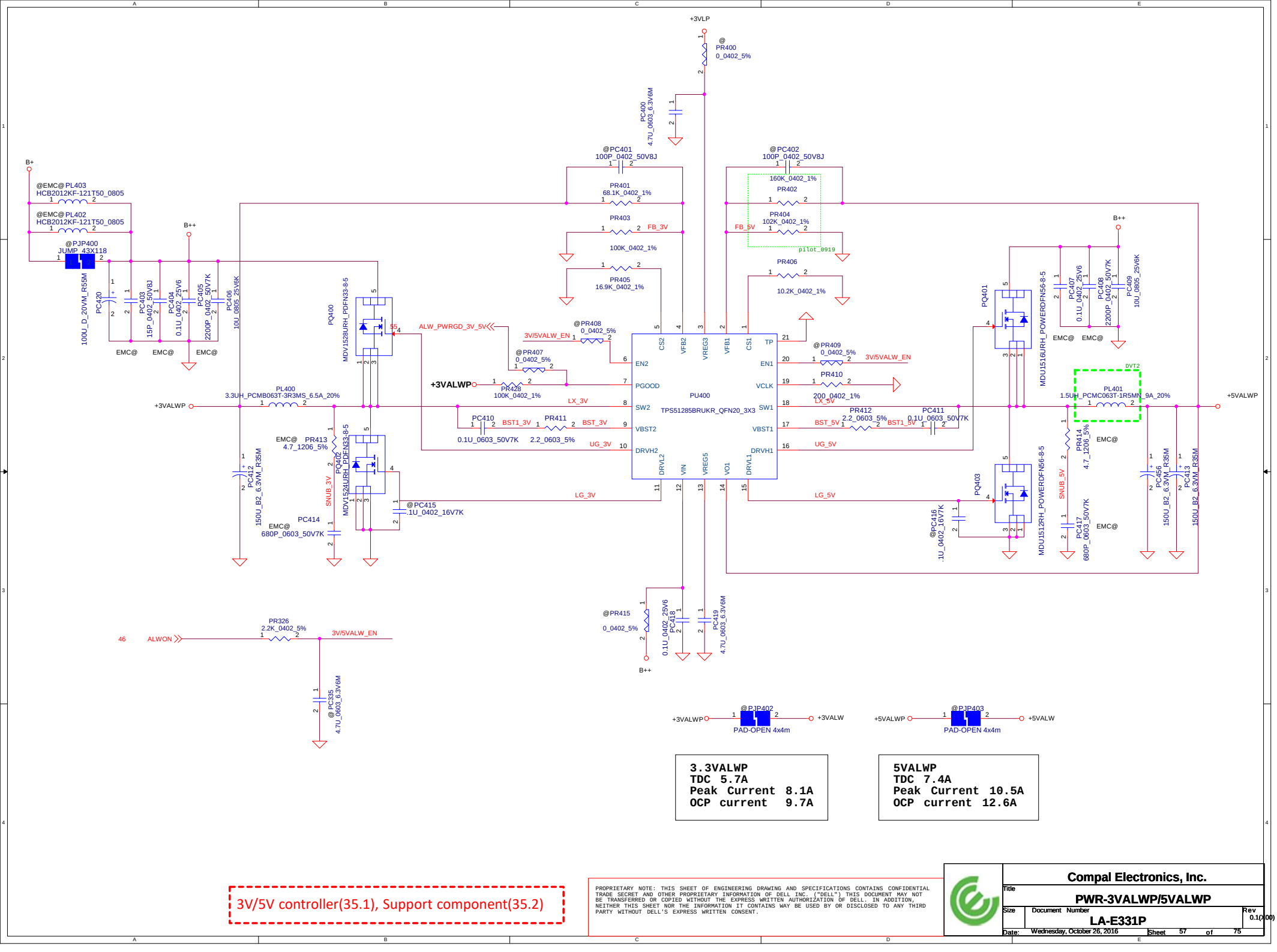
Compal Electronics, Inc.
Title: PWR-DCIN / BATT CONN / OTP
Size: Document Number: LA-E331P
Rev: 0.1(X00)
Date: Wednesday, October 26, 2016
Sheet 54 of 75


Barrel Adapter
S1
P-MOSFET
S2
P-MOSFET
EMI soultion for layout placement space
USB type-C Adapter / PD
S11
S6
P-MOSFET
S7
P-MOSFET
From TI PD GPIO
+3VALW
+3V_VC
+DC_IN
+VBUS_1
3V LDO
Vbus_AC Detector
Docking Power Control(41.1), Support component(41.2)
Compal Electronics, Inc.
Docking
LA-E331P
Wednesday, October 28, 2015



Charger controller(40.1), Support component(40.2)

Compal Electronics, Inc.	
Title	Charger
Size	Document Number: LA-E331P
Rev	0.1(X00)
Date:	Wednesday, October 26, 2016
Sheet	56 of 75

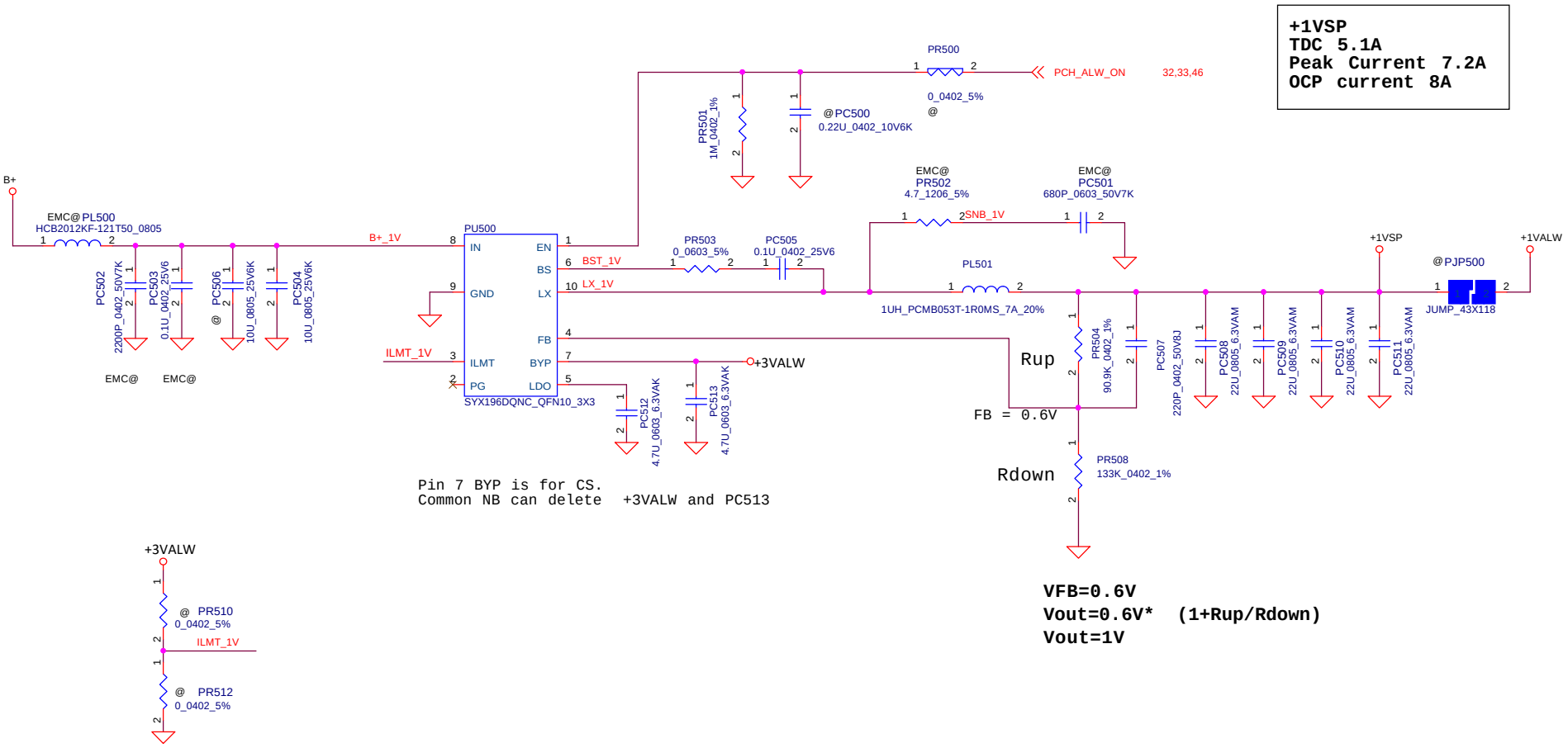


Compal Electronics, Inc.

Title: PWR-3VALWP/5VALWP

Size: | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 57 of 75



PWR.Plane.Regulator(35.25), Support component(35.26)

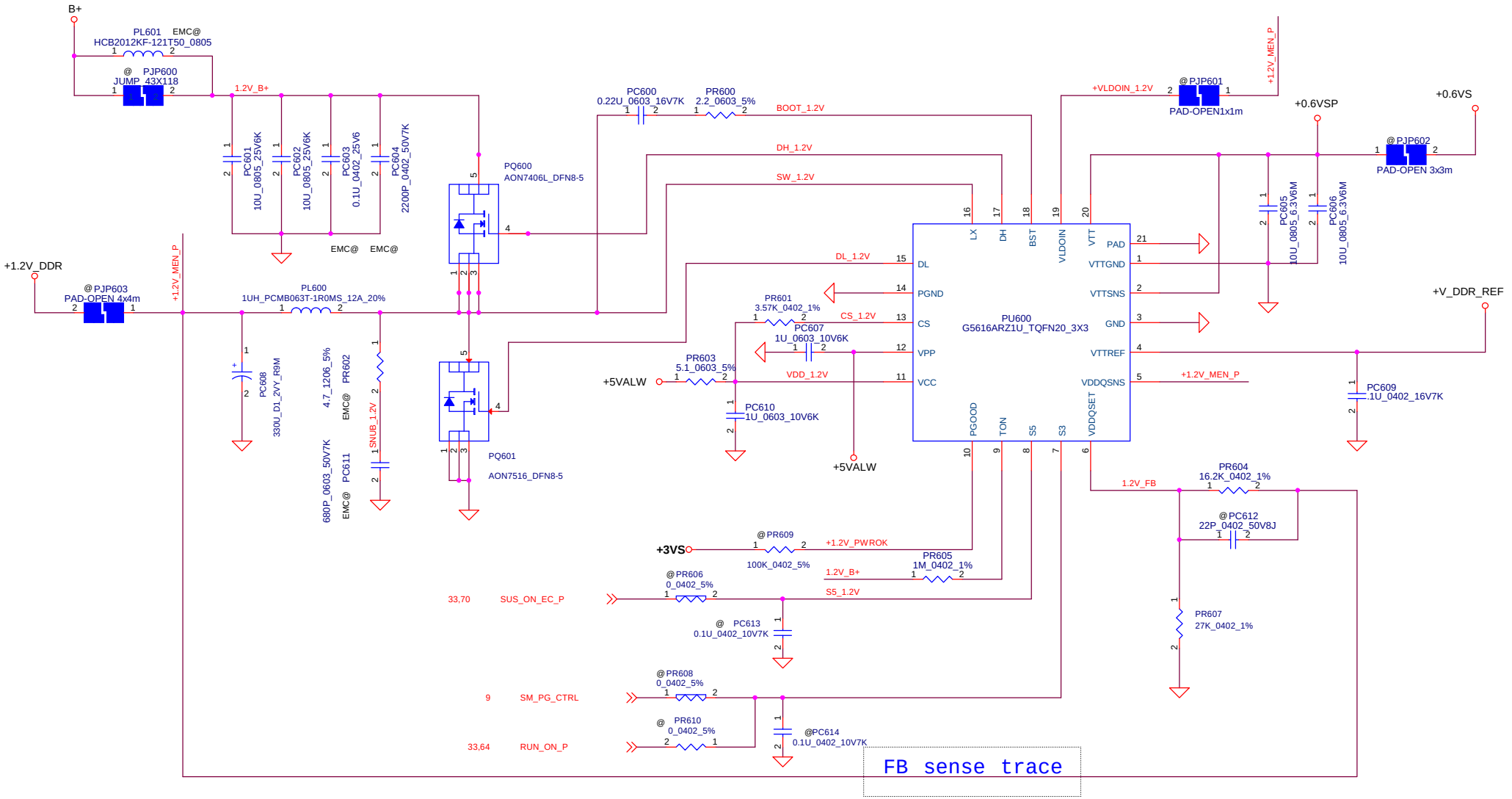
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: PWR_+1VALW

Size | Document Number: LA-E331P | Rev: 0.1(X00

Date: Wednesday, October 26, 2016 | Sheet 58 of 75



1.2Volt +/- 5%
TDC 4.2A
Peak Current 6A
OCP current 7.2A

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

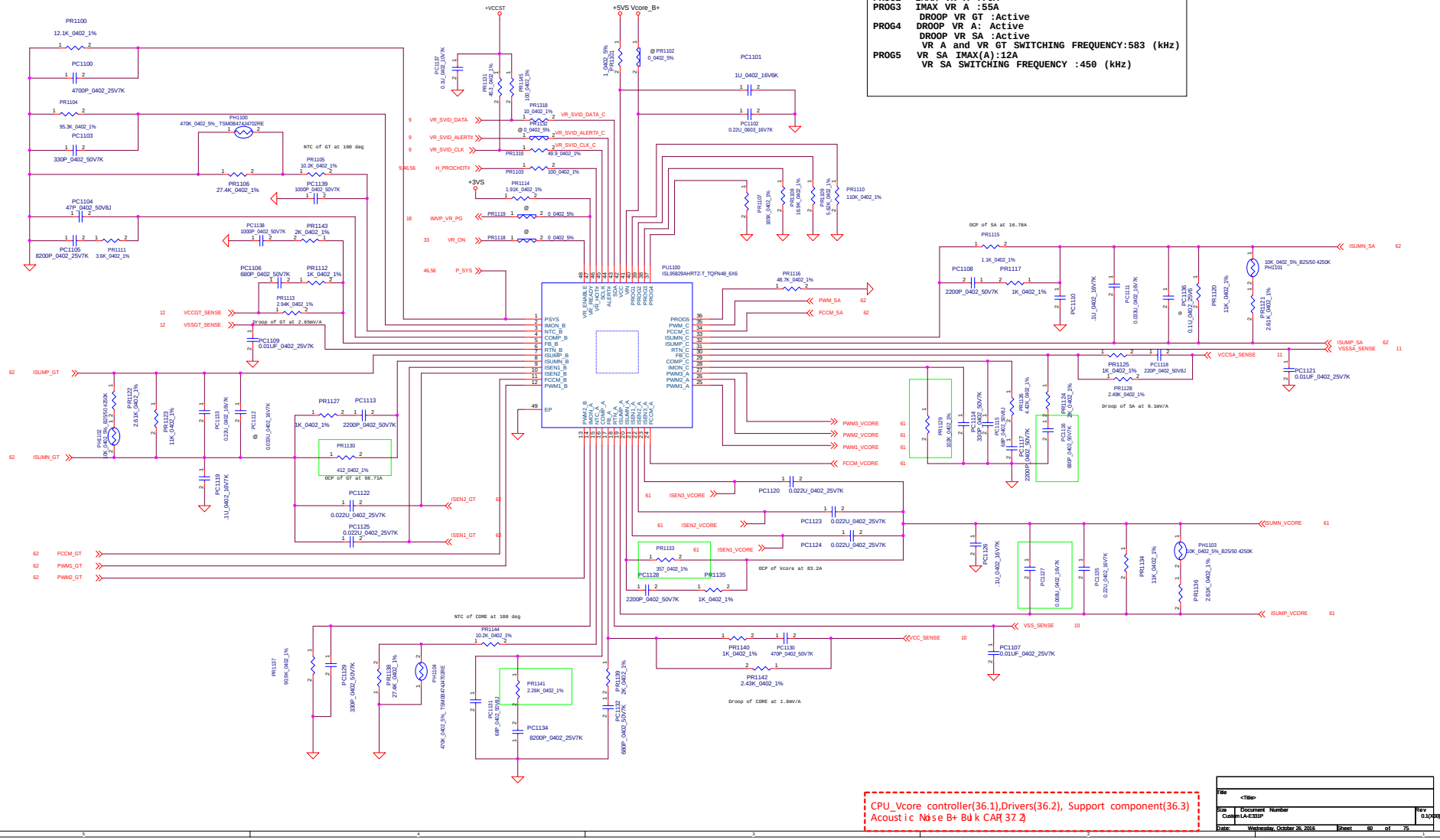
DDR controller(35.3), Support component(35.4)

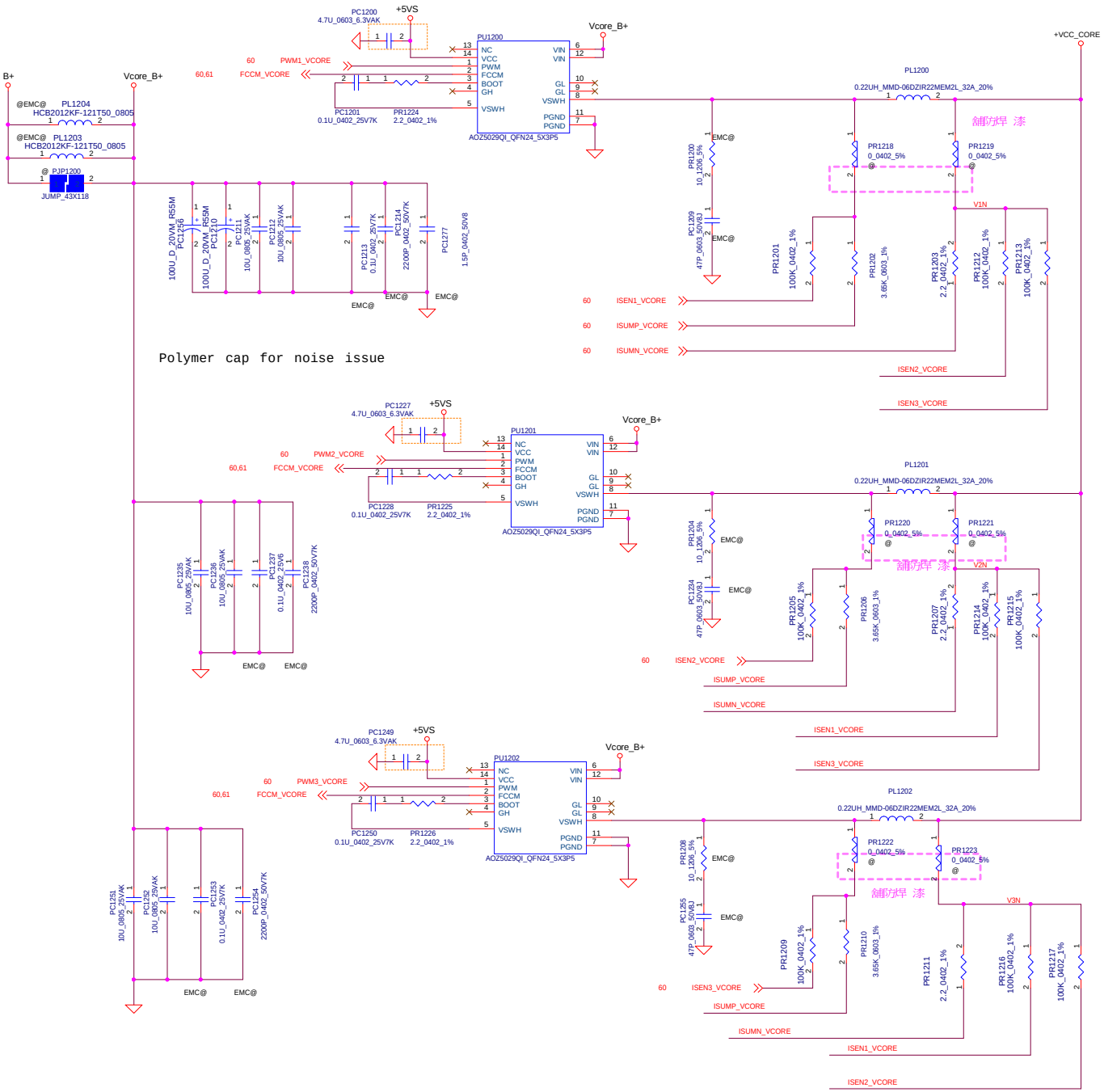
Compal Electronics, Inc.

Title: +1.35V_MEN/+0.675V_DDR_VTT

Size | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 59 of 75


PROG sets
PROG1 Vboot :0V
slew rate :30 mV/uS
PROG2 IMAX VR A :70A
PROG3 IMAX VR A :55A
DROOP VR GT :Active
PROG4 DROOP VR A: Active
DROOP VR SA :Active
VR A and VR GT SWITCHING FREQUENCY:583 (kHz)
PROG5 VR SA IMAX(A):12A
VR SA SWITCHING FREQUENCY :450 (kHz)
+VCCST
+5VS Vcore_B+
+3VS
PU1100
ISL95829AHRTZ-T_TQFN48_6X6
NTC of GT at 100 deg
NTC of CORE at 100 deg
Droop of GT at 2.65mV/A
Droop of SA at 9.1mV/A
Droop of CORE at 1.8mV/A
OCP of GT at 68.71A
OCP of Vcore at 83.2A
OCP of SA at 16.78A
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)
Title
<Title>
Size
Custom
Document Number
LA-E331P
Rev
0.1(X03)
Date: Wednesday, October 26, 2016
Sheet 60 of 75

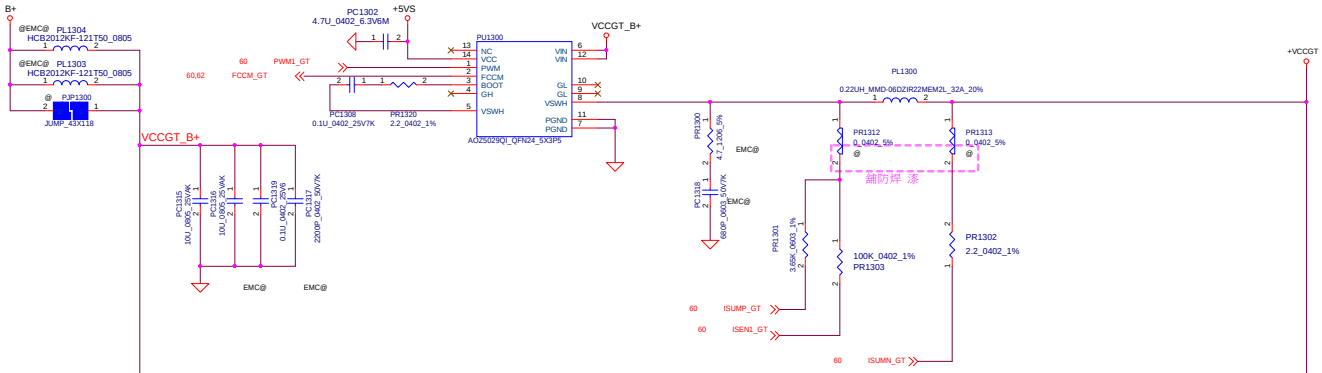


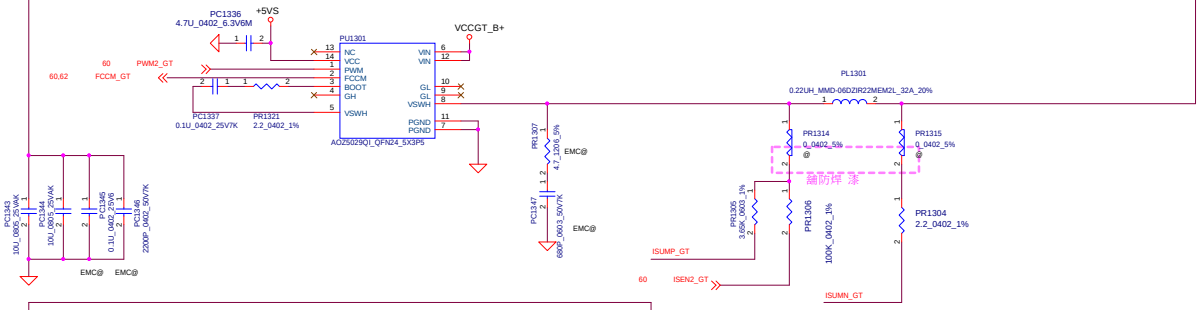
VCC_core
PL2 TDC__default):50A
PL2 TDC_max (40Sec):56A
Peak Current 68A
DC Load line -1.8mV/A
AC Load line -1.8mV/A
OCP Current 83.2A
DCR 0.97mohm +/-5%

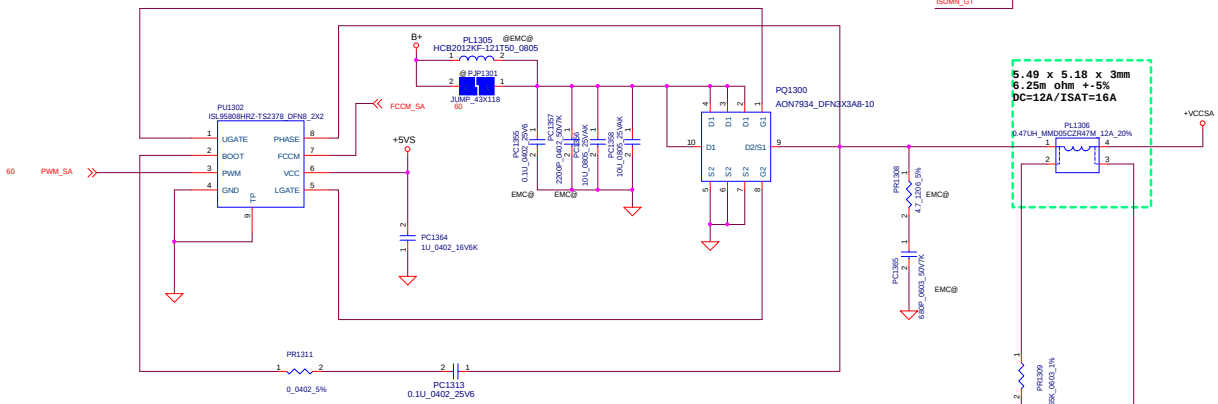
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3),
CPU_Core output CAP(36.4),Acoustic Nose B+ Bulk CAP(37.2)

Title	<Title>		
Size C	Document Number LA-E331P		Rev 0.1(X00)
Date: Wednesday, October 26, 2016	Sheet 61 of 75		

VCCGT (Base on PDDG rev 0.7)
PL2 TDC__default):25
PL2 TDC_max (40Sec):39A
Max Current 55A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 66.7A
DCR 0.98mohm +/-5%



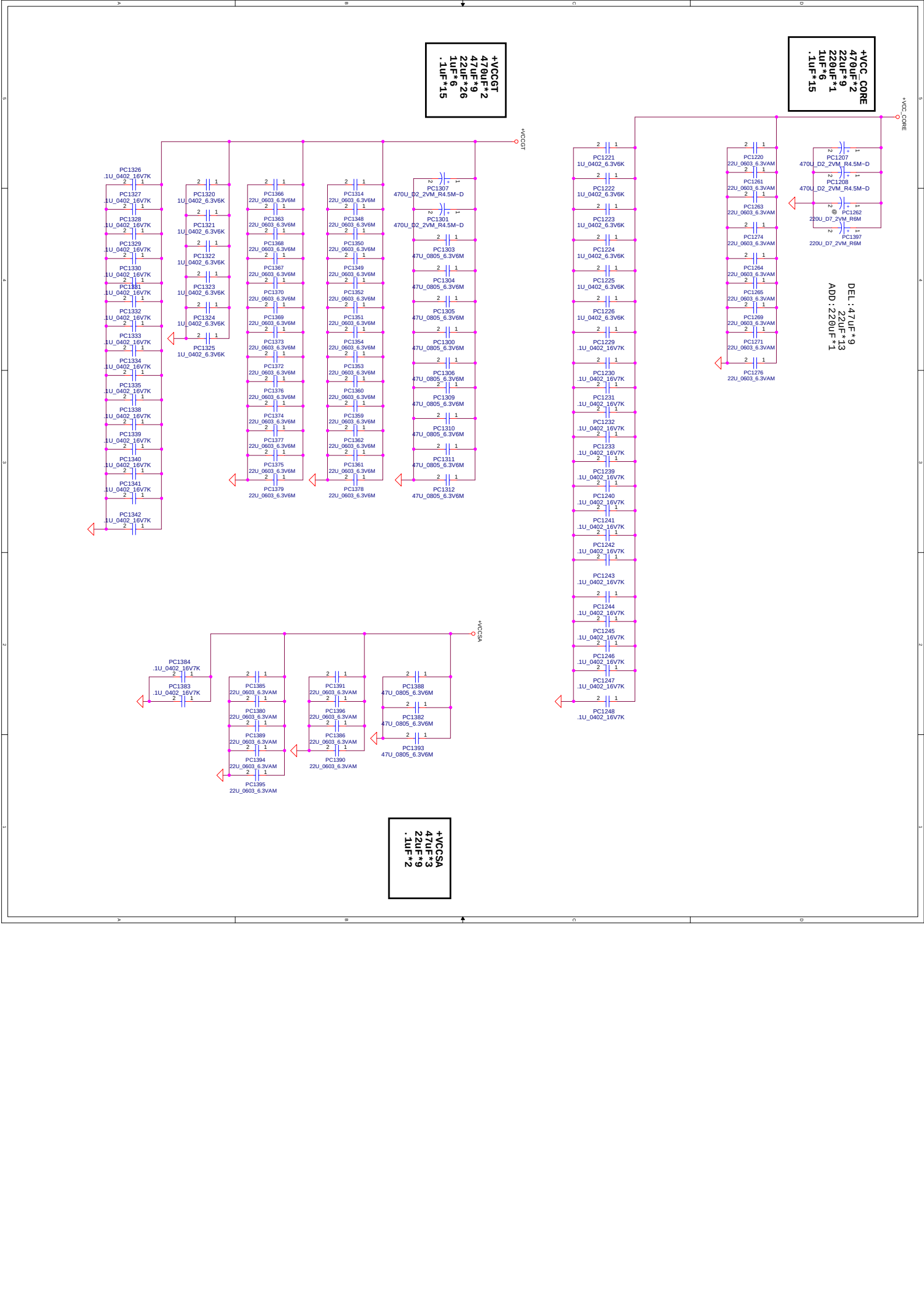


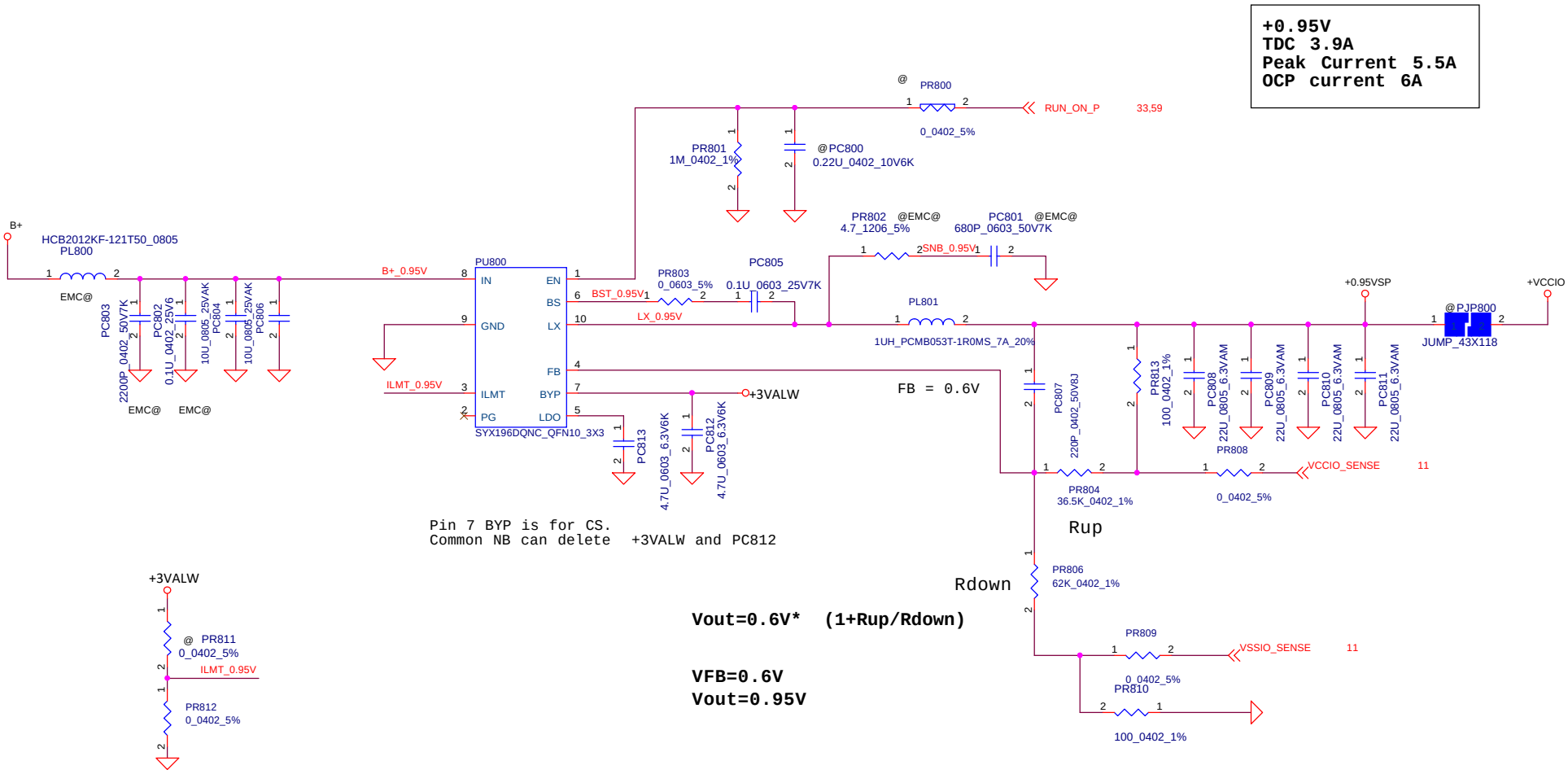


VCCSA (Base on PDDG rev 0.7)
PL2 TDC__default):10A
PL2 TDC_max (40Sec):10A
Max Current 11A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
DCR 6.2 ± 5%

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), GFX output CAP(36.5)

Title	<Title>		
Size	Document Number		Rev
Custom	LA-E331P		0.1(X00)
Date:	Wednesday, October 26, 2016	Sheet 62 of 75	


+VCCGT
470uF*2
47uF*9
22uF*26
1uF*6
.1uF*15
+VCC_CORE
470uF*2
22uF*9
220uF*1
1uF*6
.1uF*15
+VCCSA
47uF*3
22uF*9
.1uF*2
DEL : 47uF*9
22uF*13
ADD : 220uF*1
+VCCGT
+VCC_CORE
+VCCSA
PC1326 .1U_0402_16V7K
PC1327 .1U_0402_16V7K
PC1328 .1U_0402_16V7K
PC1329 .1U_0402_16V7K
PC1330 .1U_0402_16V7K
PC1331 .1U_0402_16V7K
PC1332 .1U_0402_16V7K
PC1333 .1U_0402_16V7K
PC1334 .1U_0402_16V7K
PC1335 .1U_0402_16V7K
PC1338 .1U_0402_16V7K
PC1339 .1U_0402_16V7K
PC1340 .1U_0402_16V7K
PC1341 .1U_0402_16V7K
PC1342 .1U_0402_16V7K
PC1320 1U_0402_6.3V6K
PC1321 1U_0402_6.3V6K
PC1322 1U_0402_6.3V6K
PC1323 1U_0402_6.3V6K
PC1324 1U_0402_6.3V6K
PC1325 1U_0402_6.3V6K
PC1366 22U_0603_6.3V6M
PC1363 22U_0603_6.3V6M
PC1368 22U_0603_6.3V6M
PC1367 22U_0603_6.3V6M
PC1370 22U_0603_6.3V6M
PC1369 22U_0603_6.3V6M
PC1373 22U_0603_6.3V6M
PC1372 22U_0603_6.3V6M
PC1376 22U_0603_6.3V6M
PC1374 22U_0603_6.3V6M
PC1377 22U_0603_6.3V6M
PC1375 22U_0603_6.3V6M
PC1379 22U_0603_6.3V6M
PC1314 22U_0603_6.3V6M
PC1348 22U_0603_6.3V6M
PC1350 22U_0603_6.3V6M
PC1349 22U_0603_6.3V6M
PC1352 22U_0603_6.3V6M
PC1351 22U_0603_6.3V6M
PC1354 22U_0603_6.3V6M
PC1353 22U_0603_6.3V6M
PC1360 22U_0603_6.3V6M
PC1359 22U_0603_6.3V6M
PC1362 22U_0603_6.3V6M
PC1361 22U_0603_6.3V6M
PC1378 22U_0603_6.3V6M
PC1307 470U_D2_2VM_R4.5M~D
PC1301 470U_D2_2VM_R4.5M~D
PC1303 47U_0805_6.3V6M
PC1304 47U_0805_6.3V6M
PC1305 47U_0805_6.3V6M
PC1300 47U_0805_6.3V6M
PC1306 47U_0805_6.3V6M
PC1309 47U_0805_6.3V6M
PC1310 47U_0805_6.3V6M
PC1311 47U_0805_6.3V6M
PC1312 47U_0805_6.3V6M
PC1221 1U_0402_6.3V6K
PC1222 1U_0402_6.3V6K
PC1223 1U_0402_6.3V6K
PC1224 1U_0402_6.3V6K
PC1225 1U_0402_6.3V6K
PC1226 1U_0402_6.3V6K
PC1229 .1U_0402_16V7K
PC1230 .1U_0402_16V7K
PC1231 .1U_0402_16V7K
PC1232 .1U_0402_16V7K
PC1233 .1U_0402_16V7K
PC1239 .1U_0402_16V7K
PC1240 .1U_0402_16V7K
PC1241 .1U_0402_16V7K
PC1242 .1U_0402_16V7K
PC1243 .1U_0402_16V7K
PC1244 .1U_0402_16V7K
PC1245 .1U_0402_16V7K
PC1246 .1U_0402_16V7K
PC1247 .1U_0402_16V7K
PC1248 .1U_0402_16V7K
PC1220 22U_0603_6.3VAM
PC1261 22U_0603_6.3VAM
PC1263 22U_0603_6.3VAM
PC1274 22U_0603_6.3VAM
PC1264 22U_0603_6.3VAM
PC1265 22U_0603_6.3VAM
PC1269 22U_0603_6.3VAM
PC1271 22U_0603_6.3VAM
PC1276 22U_0603_6.3VAM
PC1207 470U_D2_2VM_R4.5M~D
PC1208 470U_D2_2VM_R4.5M~D
PC1262 220U_D7_2VM_R6M
PC1397 220U_D7_2VM_R6M
PC1384 .1U_0402_16V7K
PC1383 .1U_0402_16V7K
PC1385 22U_0603_6.3VAM
PC1380 22U_0603_6.3VAM
PC1389 22U_0603_6.3VAM
PC1394 22U_0603_6.3VAM
PC1395 22U_0603_6.3VAM
PC1391 22U_0603_6.3VAM
PC1396 22U_0603_6.3VAM
PC1386 22U_0603_6.3VAM
PC1390 22U_0603_6.3VAM
PC1388 47U_0805_6.3V6M
PC1382 47U_0805_6.3V6M
PC1393 47U_0805_6.3V6M



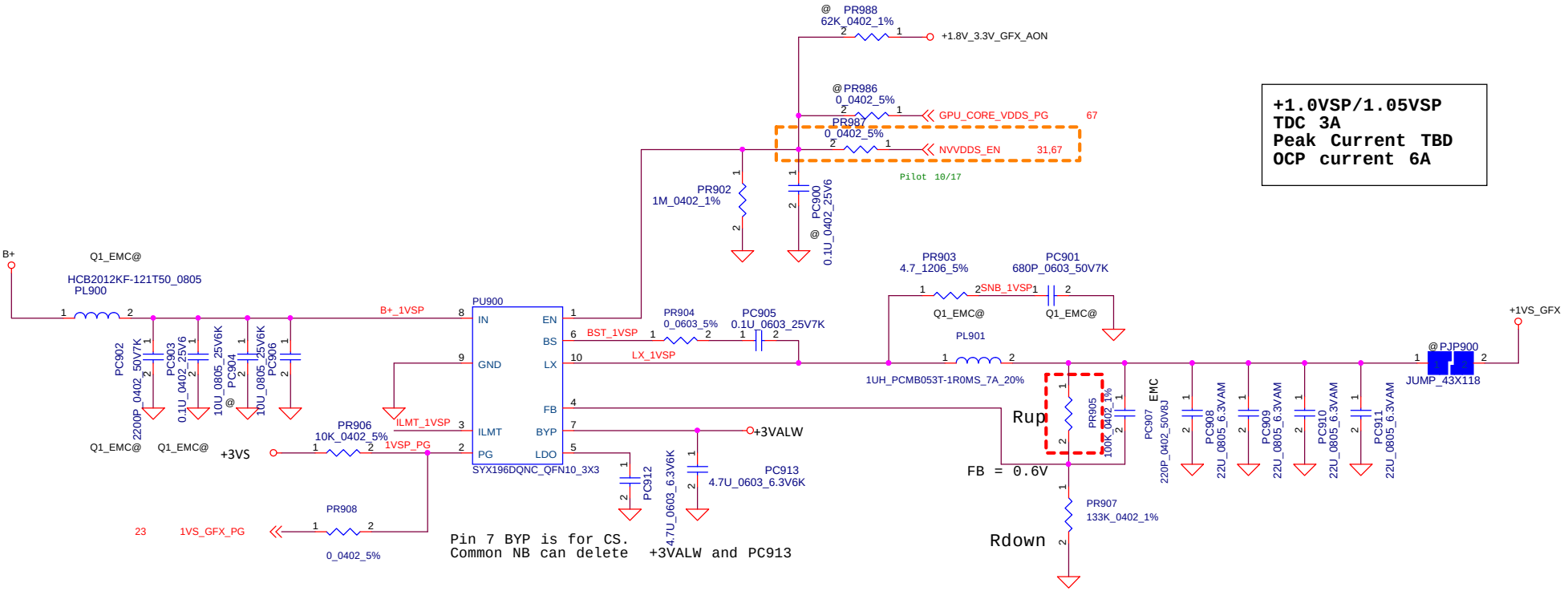
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P67-PWR_+0.95VA

Size | Document Number: LA-E331P | Rev: 0.1(X00

Date: Wednesday, October 26, 2016 | Sheet 64 of 75



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P64-PWR_+1VS_GFX*

Size | Document Number: *LA-E331P* | Rev: 0.1(X00

Date: Wednesday, October 26, 2016 | Sheet 65 of 75

2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

	2Phase DEM	2Phase CCM
PSI	1.2V	1.8V
Rb	22.6Kohm	0ohm
Rc	169Kohm	NC

Rb
G0=22.6K SD034226280
Q1=5.62K SD034562180

Ra

Rc

Vmax=1.3V
Vmin=0.3V
Vboot=0.8V

Enable 1.2V
Disable 0.55V

Fsw=370KHz

GPU_CORE (0.95V)
TDC 48A
Peak Current 92A
OCP current 100A
DCR 0.98mohm +/- 5%

	MIN	MAX
H/S Rds(on)	3.7mohm	4.5mohm
L/S Rds(on)	1.5mohm	1.9mohm

+GPU_CORE (place under GPU)

+GPU_CORE (place near GPU)

7 x 7 x 4mm

Under:
4.7U_0603_6.3VAK *16
1U_0402_6.3VAK *10

Near:
10U_0805_6.3V6M*7
22U_0805_6.3V6M *7
4.7U_0805_6.3V6K *6
330u*3

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Compal Electronics, Inc.

Title: VGA_CORE

Size: Document Number: LA-E331P Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 Sheet 66 of 75

For G0

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V

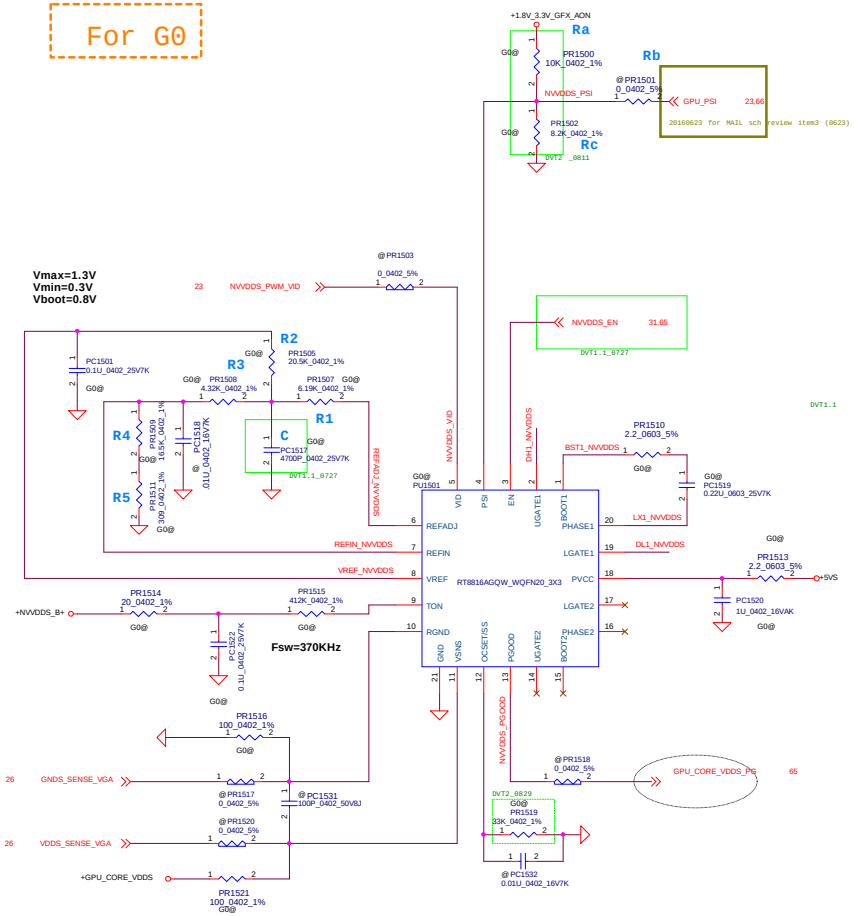
	1Phase DEM	1Phase CCM
PSI	0V	
Ra	NC	10Kohm
Rb	NC	0ohm
Rc	0ohm	8.06Kohm

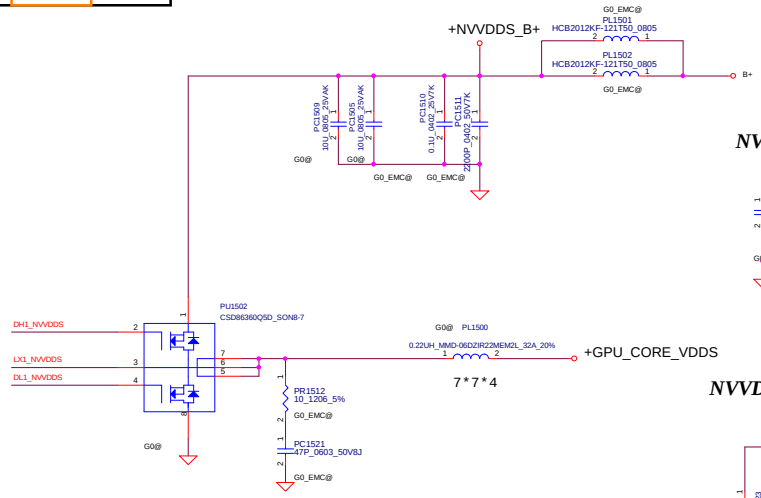
+GPU_CORE_VDDS
TDC 12A
Peak Current 16A
OCP current 21A
DCR 0.98mohm +/- 5%

	MIN	MAX
H/S Rds(on)	3.7mohm	4.5mohm
L/S Rds(on)	1.5mohm	1.9mohm

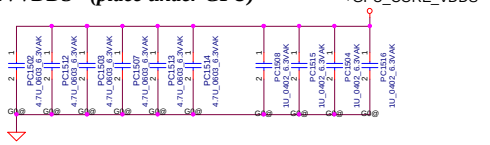
Vmax=1.3V
Vmin=0.3V
Vboot=0.8V

Fsw=370KHz

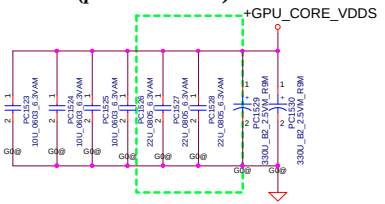




NVVDDS (place under GPU)



NVVDDS (place near GPU)



Under:
4.7U_0603_6.3VAK *6
1U_0402_6.3VAK *4

Near:
10U_0603_6.3V6M *3
22U_0805_6.3V6M *3
330u*2

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

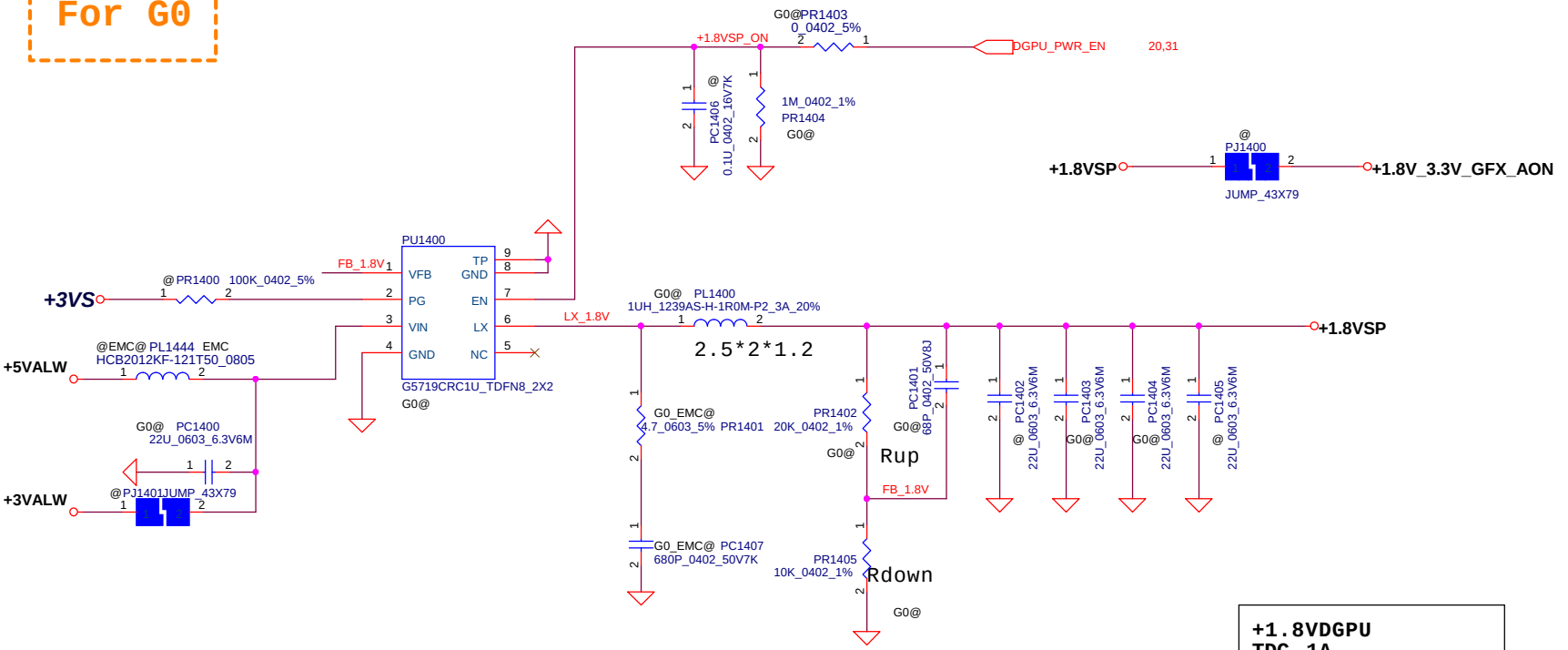
Compal Electronics, Inc.

Title: +GPU_CORE_VDDS

Size: | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 67 of 75

For G0



Vout=0.6V* (1+Rup/Rdown)

+1.8VDGPU
TDC 1A
Peak Current TBD
OCP current 3A(FIX)

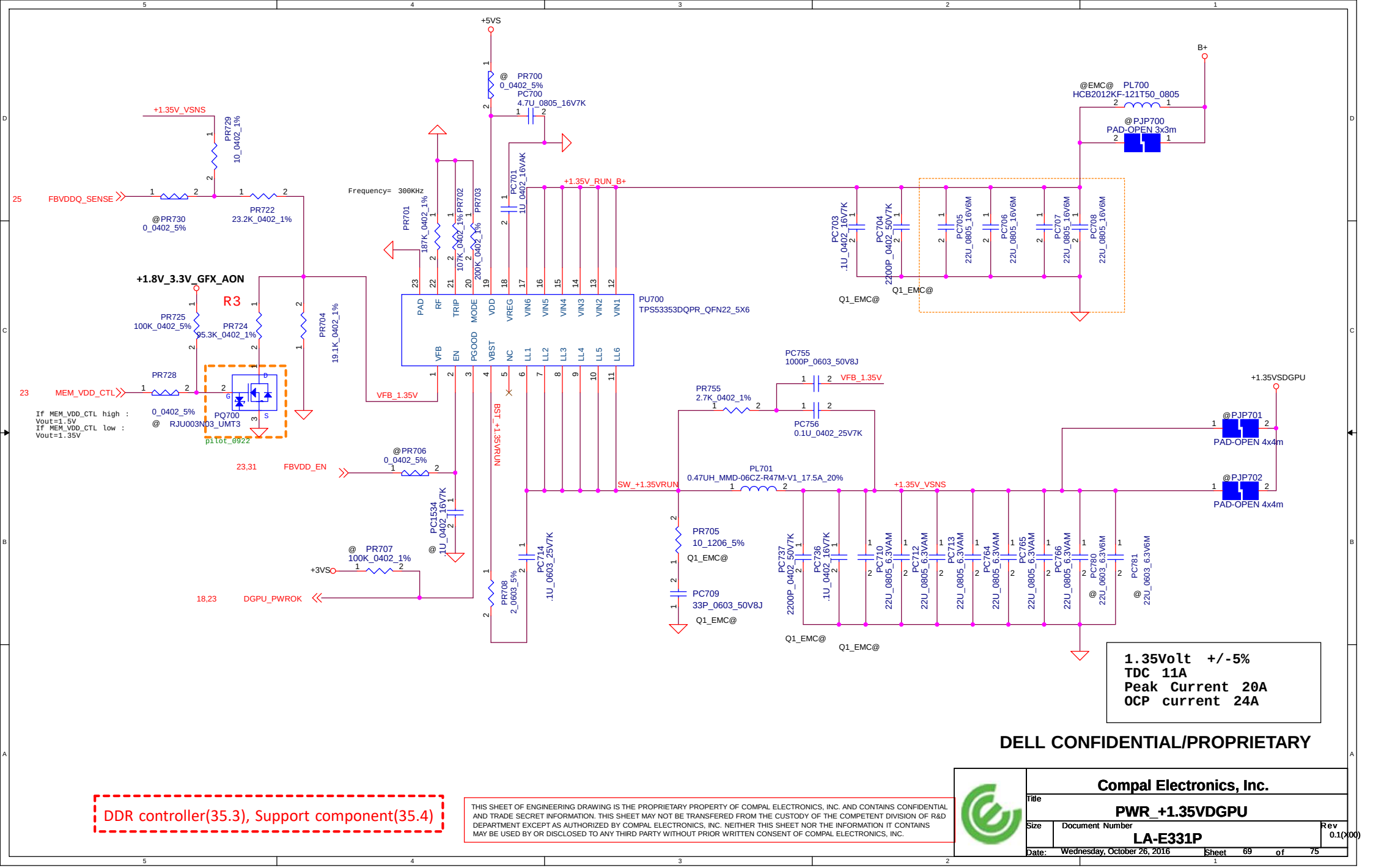
Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: +1.8VSP

Size: B | Document Number | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 68 of 75



DDR controller(35.3), Support component(35.4)

Compal Electronics, Inc.

Title: PWR_+1.35VDGPU

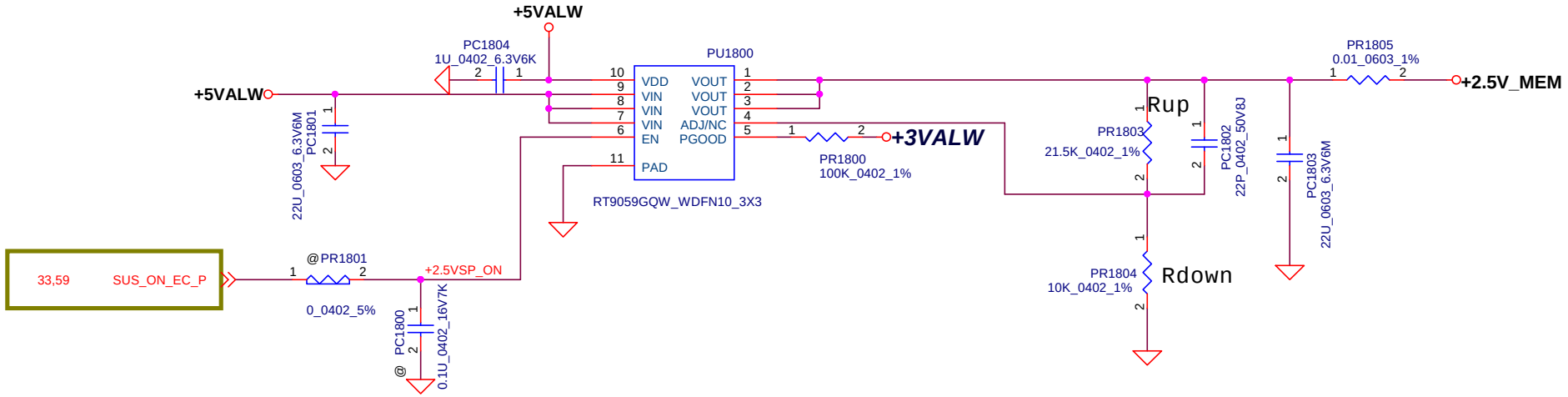
Size: | Document Number: LA-E331P | Rev: 0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 69 of 75

2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

EE no need 2.5V_PWROK
Delete 2.5V_PWROK



Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: **PWR_+2.5V_MEM**

Size	Document Number	Rev
	LA-D993P	0.1(X00)

Date: Wednesday, October 26, 2016 | Sheet 70 of 70

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
16				EE			X01
17				EE			X01
18				EE			X01
19				EE			X01
20				EE			X01
21				EE			X01
22				EE			X01
23				EE			X01
24				EE			X01
25				EE			X01
26				EE			
27				EE			
28				EE			
29				EE			
30				EE			
31				EE			
32				EE			
33				EE			
34				EE			
35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

Compal Electronics, Inc.

Title		
	NOTE	
Size	Document Number	Rev
	LA-E331P	0.1(000)
Date: Wednesday, October 26, 2016	Sheet 71 of 75	

Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
16				EE			X01
17				EE			X01
18				EE			X01
19				EE			X01
20				EE			X01
21				EE			X01
22				EE			X01
23				EE			X01
24				EE			X01
25				EE			X01
26				EE			
27				EE			
28				EE			
29				EE			
30				EE			
31				EE			
32				EE			
33				EE			
34				EE			
35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

Compal Electronics, Inc.

Title: NOTE

Size | Document Number: LA-E331P | Rev: 0.1(000)

Date: Wednesday, October 26, 2016 | Sheet 72 of 75