ZZZ PCB@

PCB 1G7 LA-D051P REV1 M/B

DA80013U010

Compal Confidential

BAV00 / BAV10
MB Schematic Document

LA-D051P

Rev: 1.0
2015.07.15

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

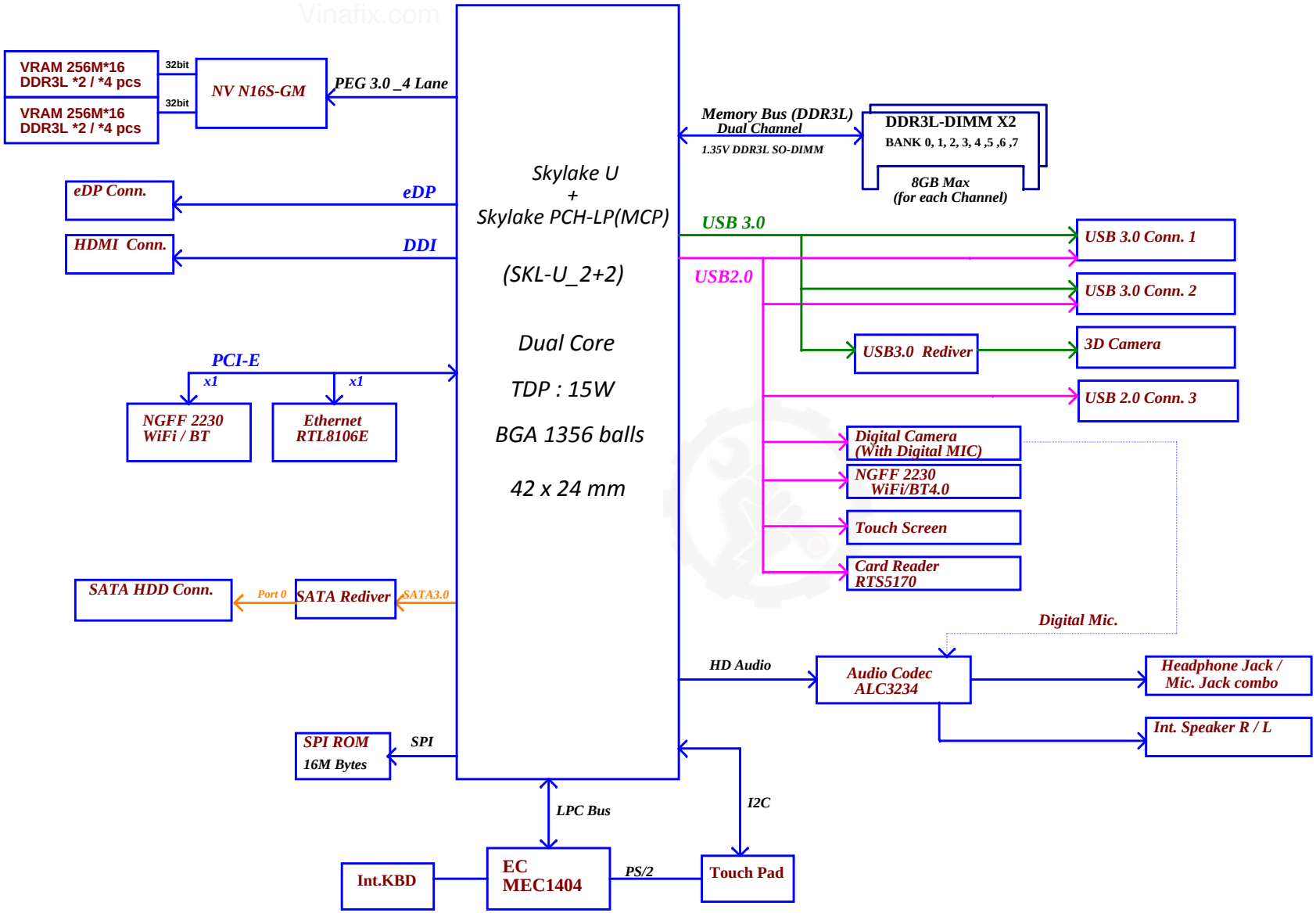
Compal Electronics, Inc.

Title: Cover Sheet

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 1 of 55

Skylake U_2+2 Block Diagram



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/05/19	Deciphered Date	2015/12/31
Title	SKL-U 2+2 Block Diagrams		
Size: Custom	Document Number: LA-C071P		Rev: 0.2
Date: Tuesday, July 28, 2015	Sheet 2 of 55		

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Title: Notes List

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Date: Tuesday, July 28, 2015 | Sheet 3 of 55

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Issued Date	2013/11/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.		
Title: ***Power MAP***		
Size:	Document Number	Rev: 0.2
Date: Tuesday, July 28, 2015	Sheet 4 of 55	

(Blanking)

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

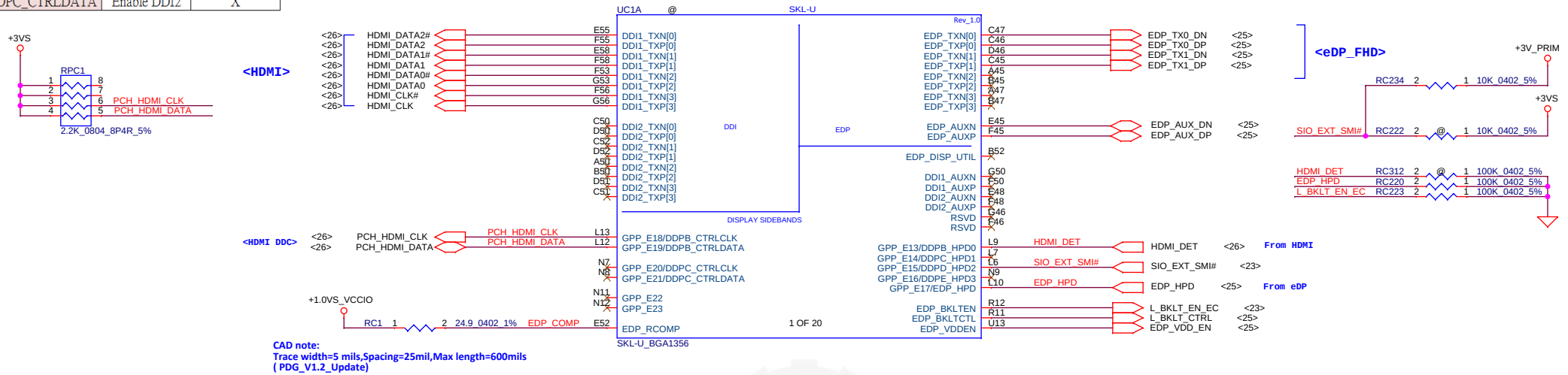
Title: **Power Sequence**

Size: | Document Number | Rev 0.2

Date: Tuesday, July 28, 2015 | Sheet 5 of 55

Main Func : CPU

	Ext. PU_2.2K	N.C
DDPB_CTRLDATA	Enable DDI1	X
DDPC_CTRLDATA	Enable DDI2	X



CAD note:
Trace width=5 mils,Spacing=25mil,Max length=600mils
(PDG_V1.2_Update)

UC1 ES_2.3G@
S IC A31 FJ8066201924925 QHMF C0 2.3G
SA00008M40L

UC1 ES_1.6G@
S IC A31 FJ8066201924932 QHMG C0 1.6G
SA00008M30L

UC1 QS_i5@
S IC A31 FJ8066201930409 QJ8N D0 2.3G
SA000092O0L

UC1 SQS_i5@
S IC A31 FJ8066201930409 QJKP D1 2.3G
SA000092O1L

UC1 QS_i7@
S IC A31 FJ8066201930408 QJ8L D0 2.5G
SA000092P0L

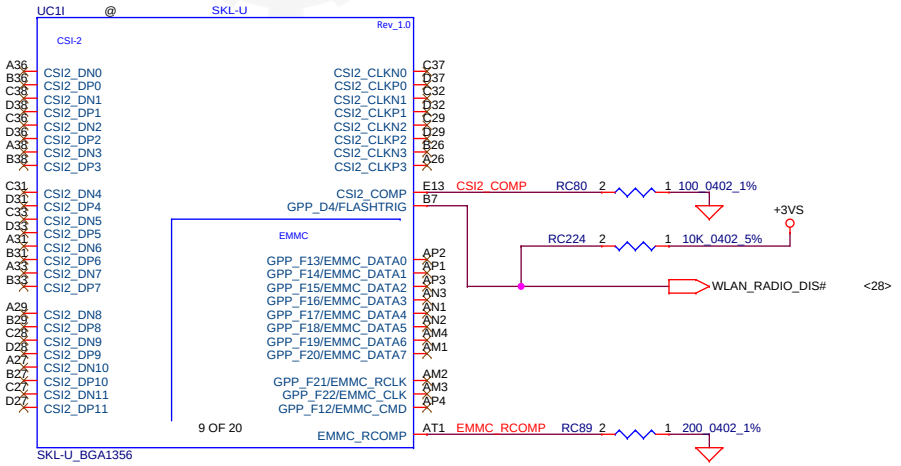
UC1 SQS_i7@
S IC A31 FJ8066201930408 QJKK D1 2.5G
SA000092P1L

UC1 MP_i5@
S IC FJ8066201930409 SR2EY D1 2.3G A31!
SA000092O3L

UC1 MP_i7@
S IC FJ8066201930408 SR2EZ D1 2.5G A31!
SA000092P3L

UC1 SQS_2.1G@
S IC A31 FJ8066201930905 QJKT D1 2.1G
SA00009420L

UC1 MP_2.1G@
S IC A31 FJ8066201930905 SR2EX D1 2.1G BGA 1356 A31 !
SA00009422L



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

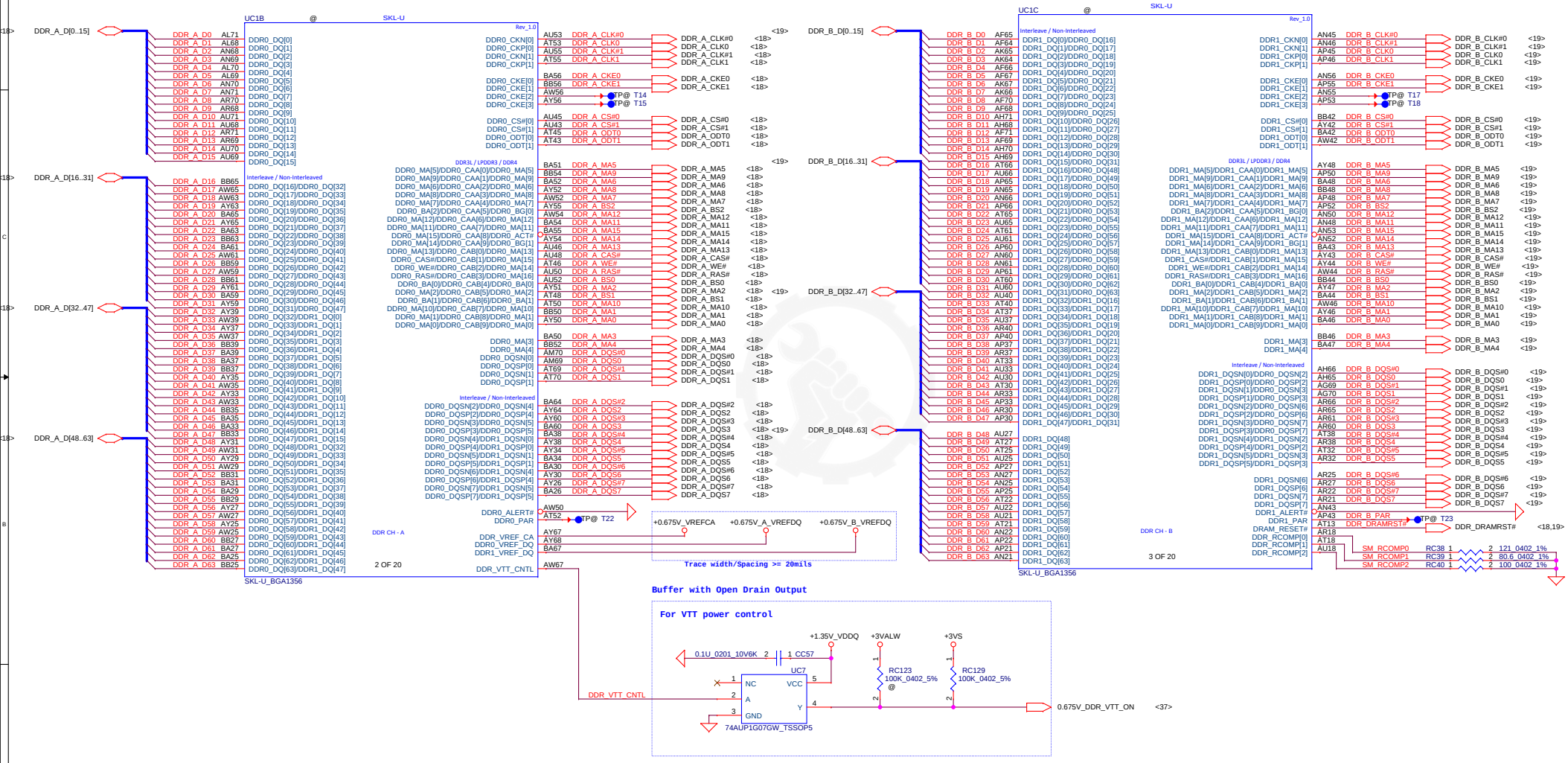
Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 6 of 55

Main Func : CPU

Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

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Compal Electronics, Inc.

Title: SKL-U(2/12)DDRIII

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 7 of 55

Main Func : CPU

From WW48 MOW for PCH SPI0_MOSI Pin

<14> XDP_SPI_SI — RC44 2 CMC@ 1 1K_0402_5% — PCH_SPI_D0

<14> XDP_SPI_IO2 — RC21 2 CMC@ 1 1K_0402_5% — PCH_SPI_D2

RC21/44 place to within 1100 mil of SPIO_MOSI/SPI0_IO2 pin for CMC

SMB_ALERT#

TLS Confidentiality	
1	Enable (for iAMT)
0	Disable (Default)

SML0_ALERT#

EC interface	
1	ESPI mode
0	LPC mode (Default)

SML1_ALERT#

EXI BOOT STALL BYPASS	
1	Enable
0	Disable (Default)

+3VS

PCH_SMBCLK RC390 2 1 1K_0402_5%

PCH_SMBDAT RC391 2 1 1K_0402_5%

+3V_PRIM

SML0_SMBCLK RC49 1 2 499_0402_1%

SML0_SMBDATA RC50 1 2 499_0402_1%

SML1CLK — 1 8 — SML1DATA — 2 7 — 3 6 — DSX@ 4 5 — 1K_0804_8P4R_5% — RPC7

SMBCLK — 1 8 — SMBDATA — 2 7 — 3 6 — 4 5 — 1K_0804_8P4R_5% — RPC18

SUS_STAT# — RC110 1 @ 2 8.2K_0402_5%

SMB -> XDP, DDR

Strap Pin

Strap Pin

SML1 -> EC,DGPU

Strap Pin

+3V_SPI

1K_0402_1% 2 1 RC47 PCH_SPI_D2

1K_0402_1% 2 @ 1 RC48 PCH_SPI_D3

4.7K_0402_5% 2 1 RC53 PCH_SPI_CS#0

1K_0402_1% 2 ES@ 1 RC51 PCH_SPI_D3

*****ONLY*****

From WW36 MOW for SKL-U ES sample

+3VS

SMBCLK — 6 1 — QC2B DMN66D0LDW-7_SOT363-6 — PCH_SMBCLK <18,19>

SMBDATA — 3 4 — QC2A DMN66D0LDW-7_SOT363-6 — PCH_SMBDAT <18,19>

UC1E @ SKL-U

SPI - FLASH

PCH_SPI_CLK AV2 — SPI0_CLK

PCH_SPI_D1 AW3 — SPI0_MISO

PCH_SPI_D0 AV3 — SPI0_MOSI

PCH_SPI_D2 AW2 — SPI0_IO2

PCH_SPI_D3 AU4 — SPI0_IO3

PCH_SPI_CS#0 AU3 — SPI0_CS0#

AU2 — SPI0_CS1#

AU1 — SPI0_CS2#

SPI - TOUCH

GPP_D1/SPI1_CLK M2

GPP_D2/SPI1_MISO M3

GPP_D3/SPI1_MOSI J4

GPP_D21/SPI1_IO2 V1

GPP_D22/SPI1_IO3 V2

GPP_D0/SPI1_CS# M1

C LINK

CL_CLK G3

CL_DATA G2

CL_RST# G1

LPC

GPP_A0/RCIN# AW13

GPP_A6/SERIRQ AY11

5 OF 20

SKL-U_BGA1356

Rev_1.0

SMBUS, SMLINK

GPP_C0/SMBCLK R7 SMBCLK

GPP_C1/SMBDATA R8 SMBDATA

GPP_C2/SMBALERT# R10 SMB_ALERT#

GPP_C3/SML0CLK R9 SML0_SMBCLK

GPP_C4/SML0DATA W2 SML0_SMBDATA

GPP_C5/SML0ALERT# W1 SML0_ALERT#

GPP_C6/SML1CLK W3 SML1CLK — SML1CLK <8>

GPP_C7/SML1DATA V3 SML1DATA — SML1DATA <8>

GPP_B23/SML1ALERT#/PCHHOT# AM7 SML1_ALERT#

GPP_A1/LAD0/ESPI_IO0 AY13 — LPC_LAD0 <23>

GPP_A2/LAD1/ESPI_IO1 BA13 — LPC_LAD1 <23>

GPP_A3/LAD2/ESPI_IO2 BB13 — LPC_LAD2 <23>

GPP_A4/LAD3/ESPI_IO3 AY12 — LPC_LAD3 <23>

GPP_A5/LFRAME#/ESPI_CS# BA12 — LPC_LFRAME# <23>

GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT#

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9

GPP_A10/CLKOUT_LPC1 AY9 PCI_CLK_LPC1

GPP_A8/CLKRUN# AW11 CLKRUN#

RC45 1 EMI@ 2 22_0402_5% — CLK_PCI_LPC_MEC <23> To EC

RC54 1 EMI@ 2 22_0402_5% — CLK_PCI_LPDEBUG <23> To Debug

CLKRUN# — RC107 1 2 8.2K_0402_5% — +1.8VS_3VS_PGPPA

+3V_PRIM

SML0_ALERT# 4.7K_0402_5% 2 @ 1 RC202

SMB_ALERT# 10K_0402_5% 2 @ 1 RC229

SML1_ALERT# 4.7K_0402_5% 2 @ 1 RC221

+3VS

*** Not Strap Pin ***

High --> 1 DIMM

Low --> 2 DIMM

10K_0402_5% 2 @ 1 RC231 — ONE_DIMM#

10K_0402_5% 2 1 RC232

+1.8VS_3VS_PGPPA

10K_0402_5% 2 1 RC225

10K_0402_5% 2 1 RC122

Follow 543016_SKL_U_Y_PDG_0_9

<23> SIO_RCIN# — SIO_RCIN#

<23> SERIRQ — SERIRQ

Single SPI ROM_CS0#

To SPI ROM

PCH_SPI_CS#0

PCH_SPI_D2 RC52 1 2 33_0402_5%

PCH_SPI_D1 RC57 1 2 33_0402_5%

PCH_SPI_D0 RC58 1 2 33_0402_5%

PCH_SPI_CLK RC59 1 2 33_0402_5%

PCH_SPI_D3 RC60 1 2 33_0402_5%

L1 Routing

L2 Routing

L3 Routing

Layout need meet L1 = L2 = L3

From EC (For share ROM)

<23> EC_MISO_R — EC_MISO_R

<23> EC_MOSI_R — EC_MOSI_R

<23> EC_SPICLK_R — EC_SPICLK_R

<23> EC_SPICS#_R — EC_SPICS#_R

16M SPI ROM (Confirmed by BIOS RD)

UC2 W25Q128FVSIQ_SO8

/CS — PCH_SPI_D1_R

IO1 — PCH_SPI_D2_R

IO2

GND

VCC — +3V_SPI

IO3

CLK — PCH_SPI_CLK_R

IO0 — PCH_SPI_D0_R

RC61 1 2 15_0402_1%

RPC5 8 7 6 5 1 2 3 4 15_0804_8P4R_5%

CC8 1 2 0.1U_0201_10V6K

CC9 1 2 10P_0402_50V8J @EMI@

<< JC1 colay UC2 >>

ROM Socket

JC1 ACES_91960-0084N_MX25L3206EM2I CONN@

PCH_SPI_CS#0 — CS#

PCH_SPI_D2_R — WP#

PCH_SPI_D3_R — HOLD#

GND

VCC — +3V_SPI

SCLK — PCH_SPI_CLK_R

SI/SIO0 — PCH_SPI_D0_R

SO/SIO1 — PCH_SPI_D1_R

+3V_PRIM

<8> SML1CLK — QC3A DMN66D0LDW-7_SOT363-6 DSX@ — GPU_THM_SMBCLK <23,30,48>

<8> SML1DATA — QC3B DMN66D0LDW-7_SOT363-6 DSX@ — GPU_THM_SMBDAT <23,30,48>

RC397 1 NDSX@ 2 0_0402_5%

RC399 1 NDSX@ 2 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 8 of 55

Main Func : CPU

NRB_BIT

NO REBOOT	
1	Reboot Disable
0	Reboot Enable (Default)

Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (AN5)

BOOT BIOS STRAP (BBS)	
1	LPC mode
0	SPI mode (Default)

3D Camera

Win7 Debug

TO DGPU

UC1F @ SKL-U — LPSS / ISH — Rev_1.0

SKL-U_BGA1356

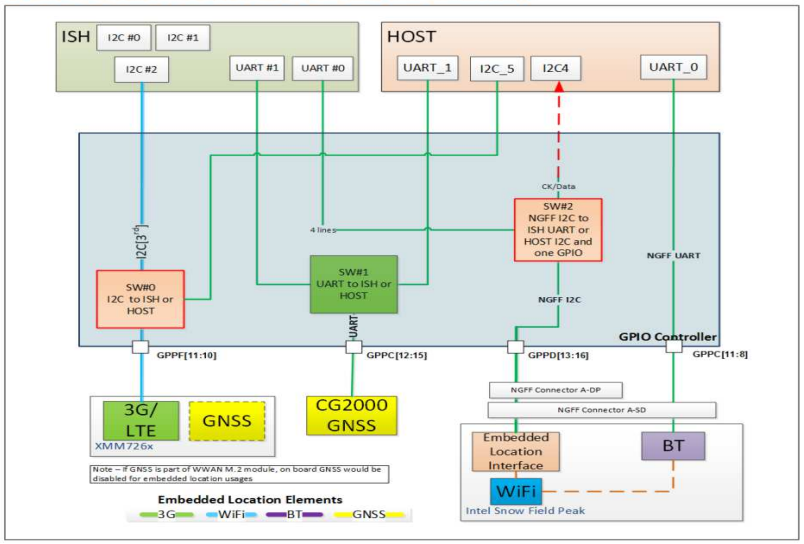
6 OF 20

PROJECT ID	PROJECT_ID2	PROJECT_ID1
*BAV00	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

BOARD ID	BOARD_ID3	BOARD_ID2
*BAV00	0	0
Reserved	0	1
Reserved	1	1

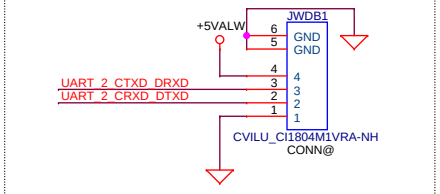
VRAM ID (PCBA VRAM Size Config.)	VRAM_ID2	VRAM_ID1
UMA	0	0
2G	0	1
4G	1	0
Reserved	1	1

Figure 64-1. Embedded Location - Host and ISH Connectivity



*** Pin defintion was defined by Customer ***

Win7 Debug solution



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

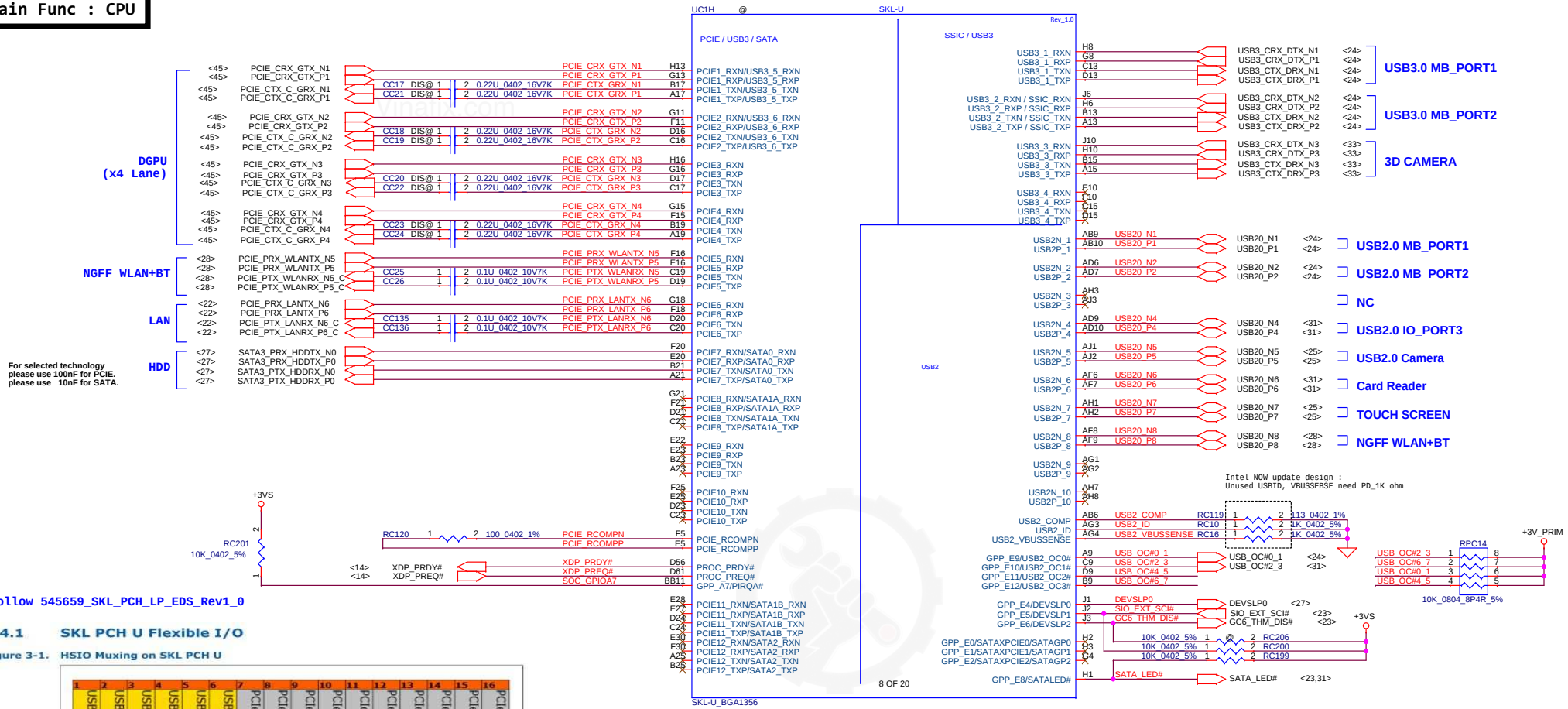
Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 9 of 55

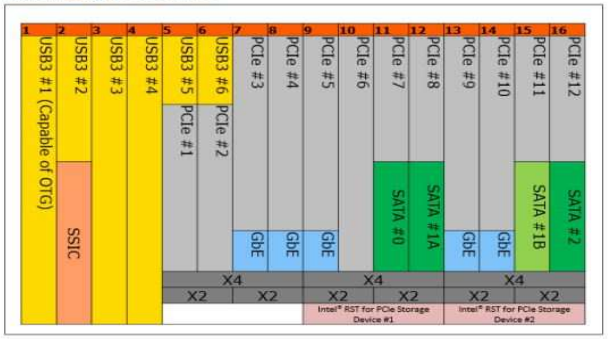
Main Func : CPU



Follow 545659_SKL_PCH_LP_EDS_Rev1_0

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:

1. Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
   - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
   - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as 4x1, 2x2, 1x2 + 2x1, or 1x4.
2. Up to 3 SATA ports (multiplexed with PCIe*)
   - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
3. Up to 6 USB 3.0 ports (multiplexed with PCIe*)
   - USB Dual Role (OTG) capability is available on USB 3.0 Port 1
   - One SSIC x1 port is multiplexed with USB 3.0 Port 2
4. One GbE lane
   - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10
   - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
5. Up to 2 Intel RST for PCIe* storage devices supported
   - Devices can be x2 or x4
   - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12

Follow 545659_SKL_PCH_LP_EDS_Rev1_0

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

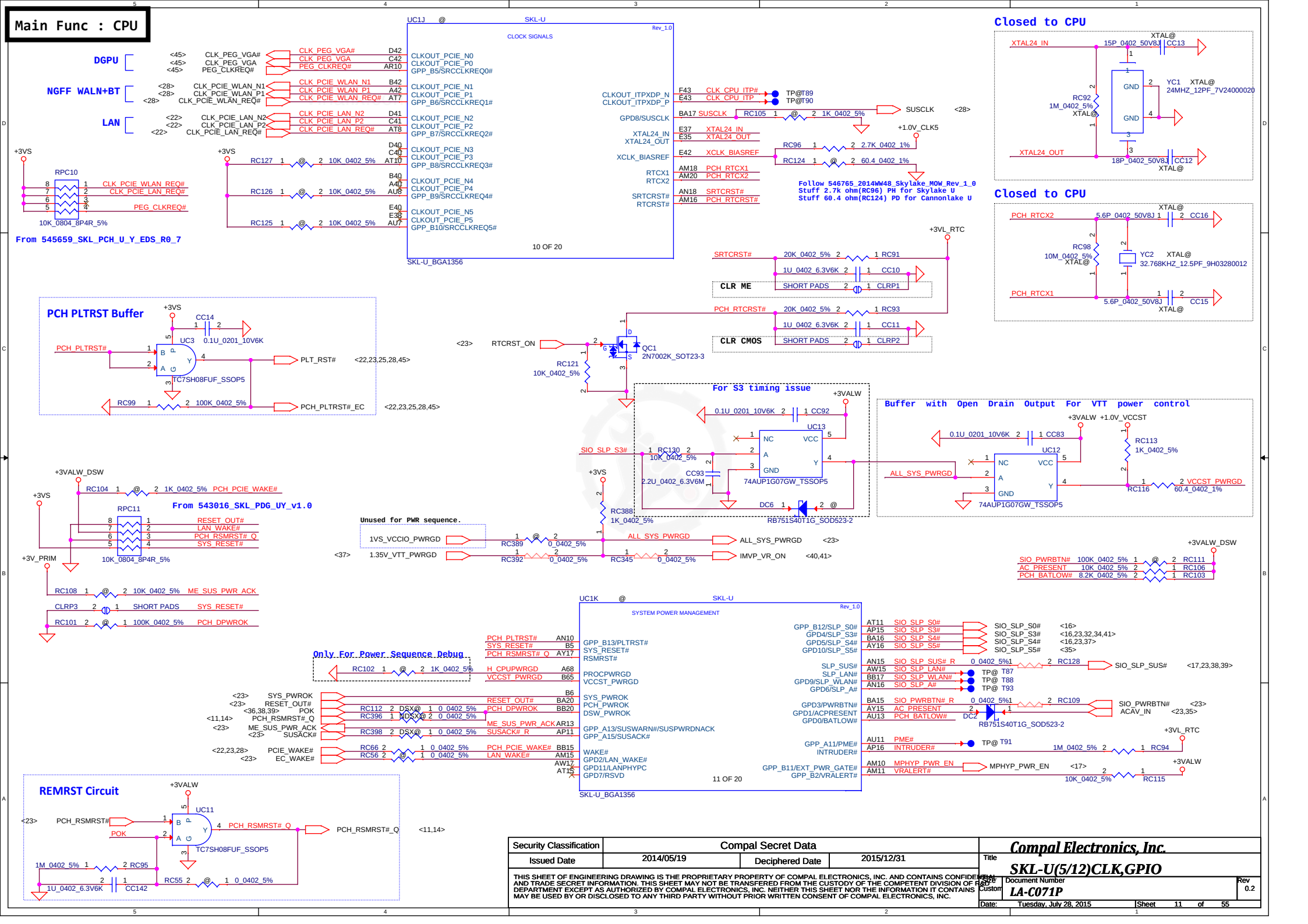
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 10 of 55

Main Func : CPU



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

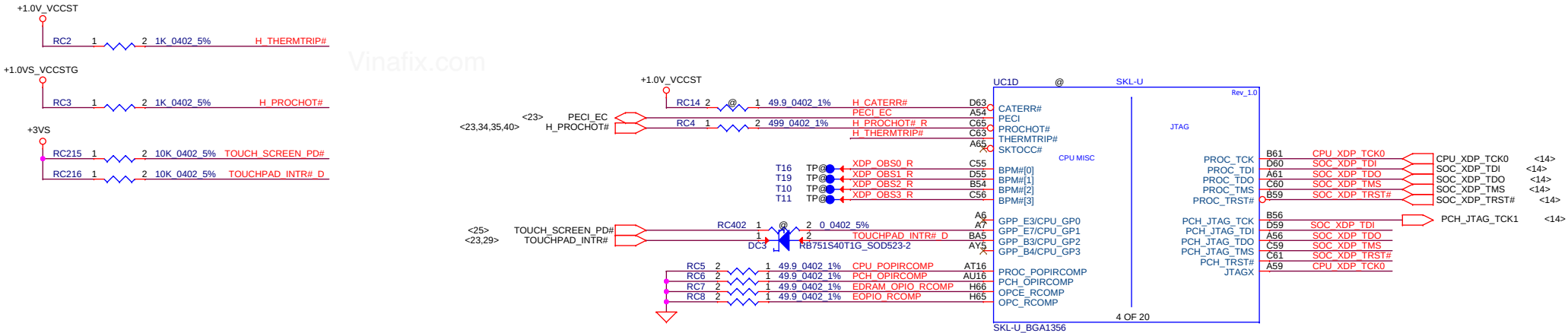
Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 11 of 55

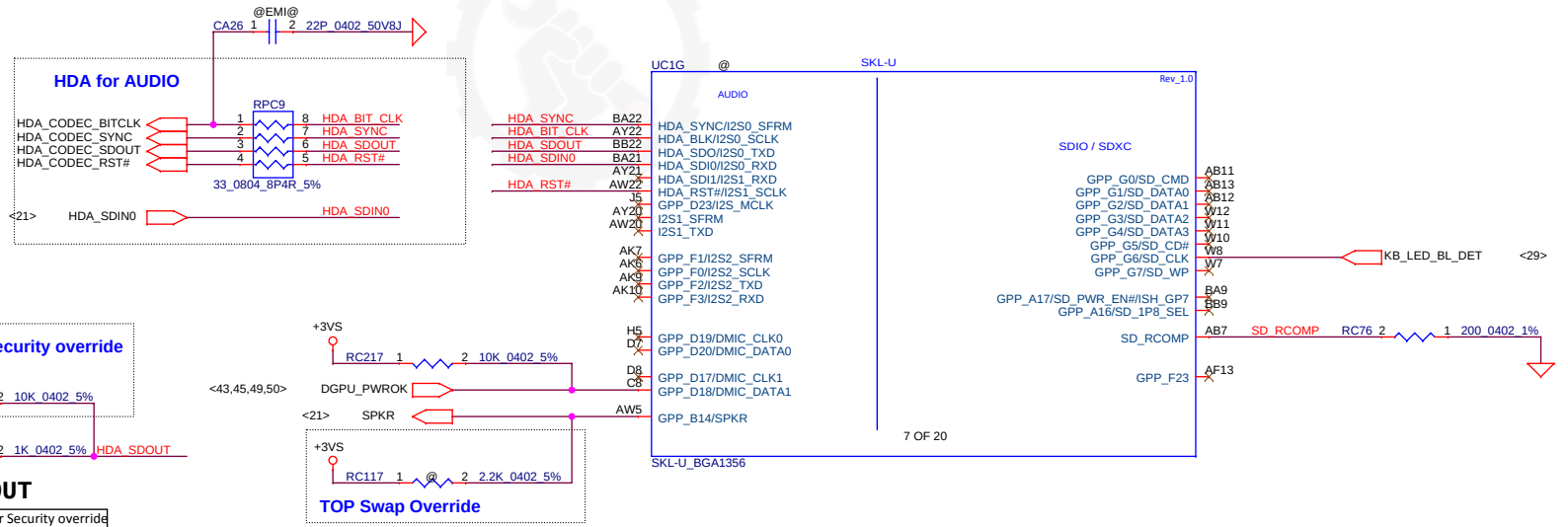
Main Func : CPU

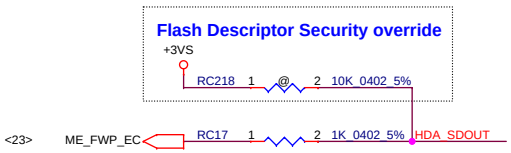


#545659 SKL_PCH_EDS_R0.7 P.84

11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
  - SDO double pumped up to 48 Mb/s
  - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.





HDA_SDOUT

Flash Descriptor Security override	
1	Disable
0	Enable (Default)

SPKR

TOP Swap Override	
1	Enable
0	Disable (Default)

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

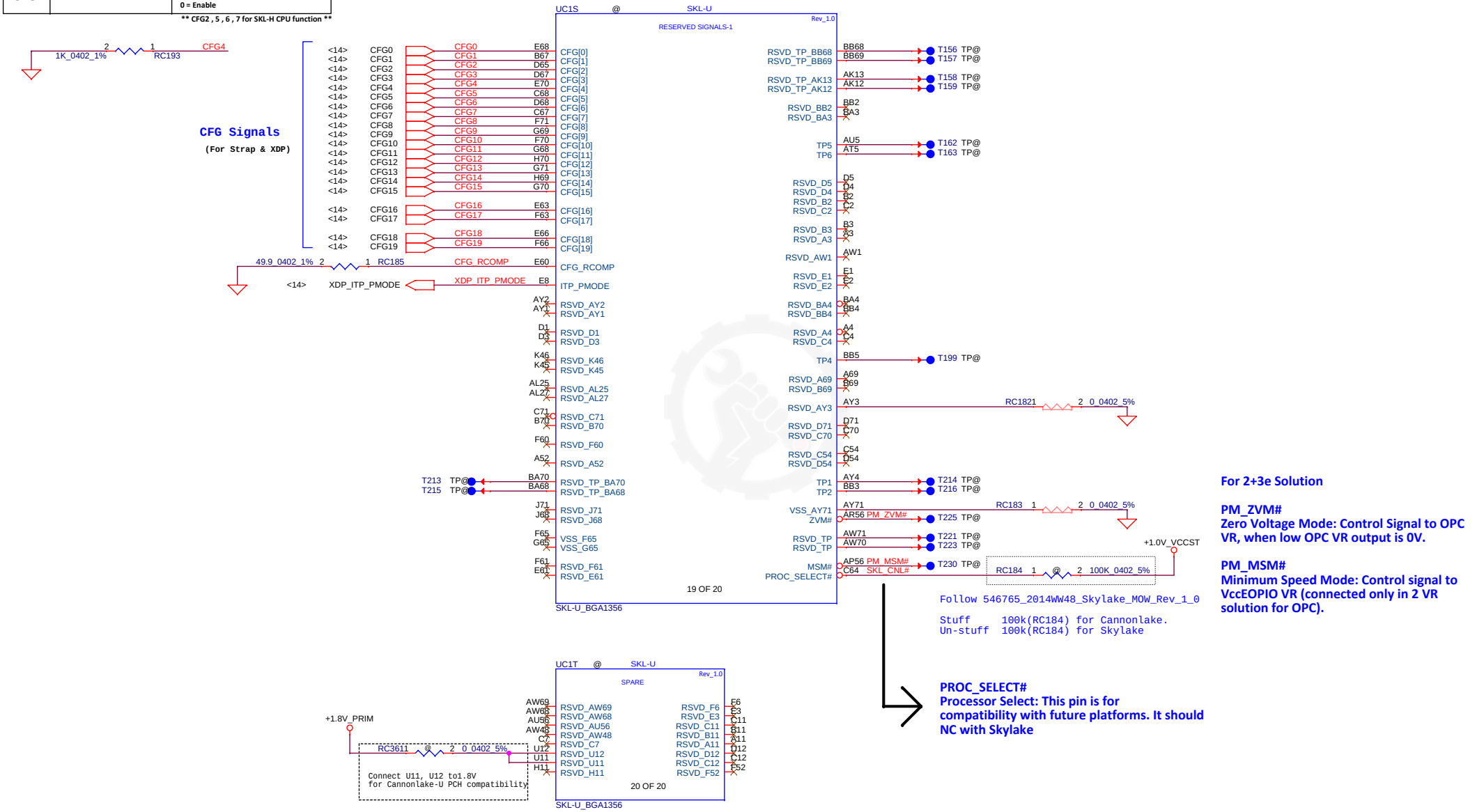
Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 12 of 55

Main Func : CPU

CFG Configuration Signals		
CFG0	Stall reset sequence after PCU PLL lock until de-asserted	1 = Normal Operation ; No Stall (Default)
		0 = Stall
CFG4	eDP enable	1 = Disable (Default)
		0 = Enable

** CFG2 , 5 , 6 , 7 for SKL-H CPU function **



Follow 546765_2014WW48_Skylake_MOW_Rev_1_0

Stuff 100k(RC184) for Cannonlake.
Un-stuff 100k(RC184) for Skylake

For 2+3e Solution

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).

PROC_SELECT#
Processor Select: This pin is for compatibility with future platforms. It should NC with Skylake

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

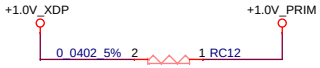
Title: SKL-U(12/12)RSVD

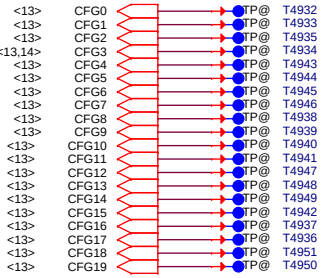
Size: Custom | Document Number: LA-C071P | Rev: 0.2

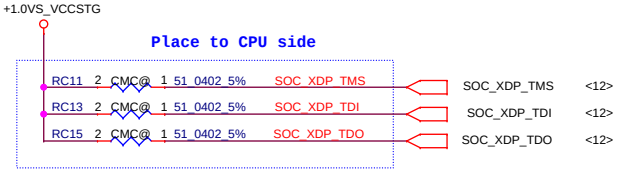
Date: Tuesday, July 28, 2015 | Sheet 13 of 55

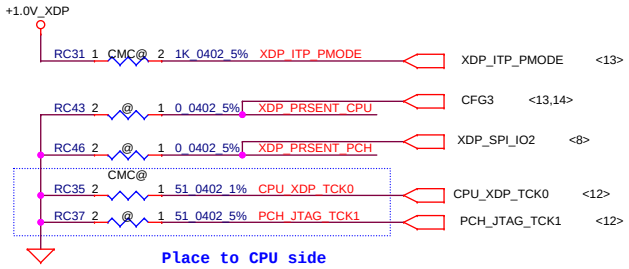
Main Func : CPU

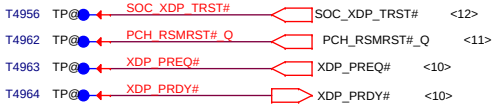
PRIMARY CMC CONN

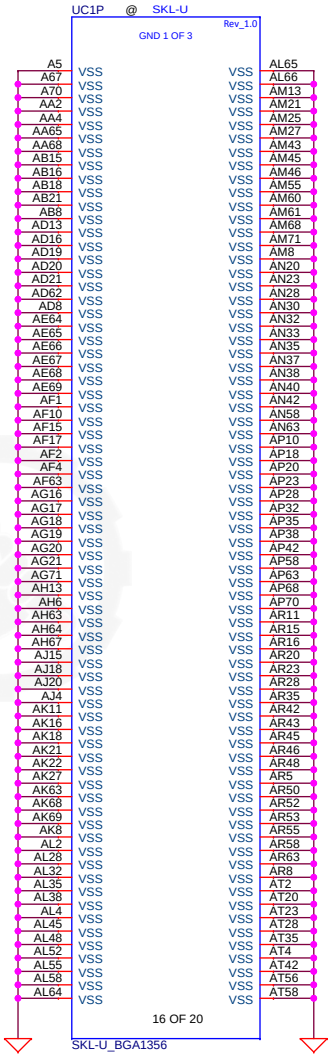


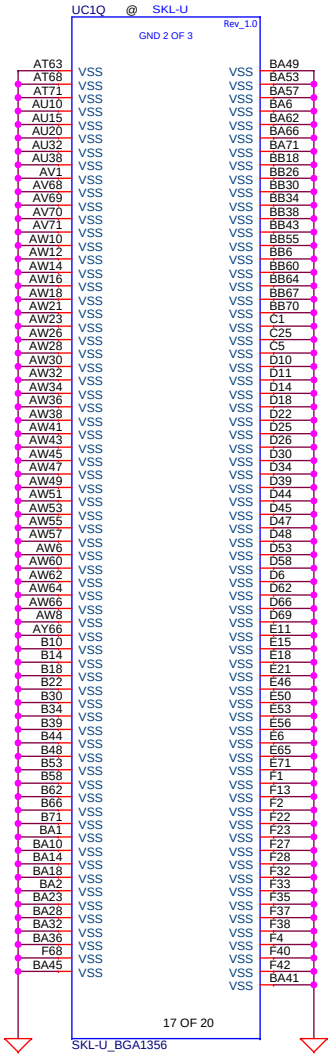


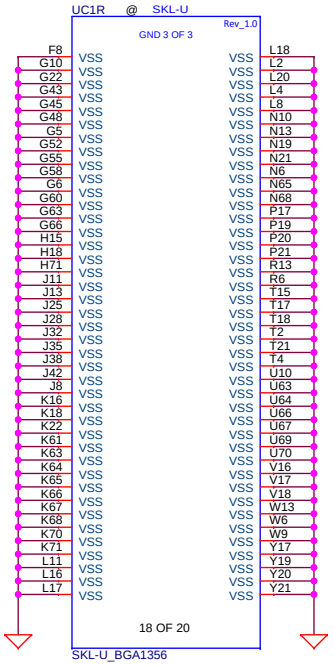












Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

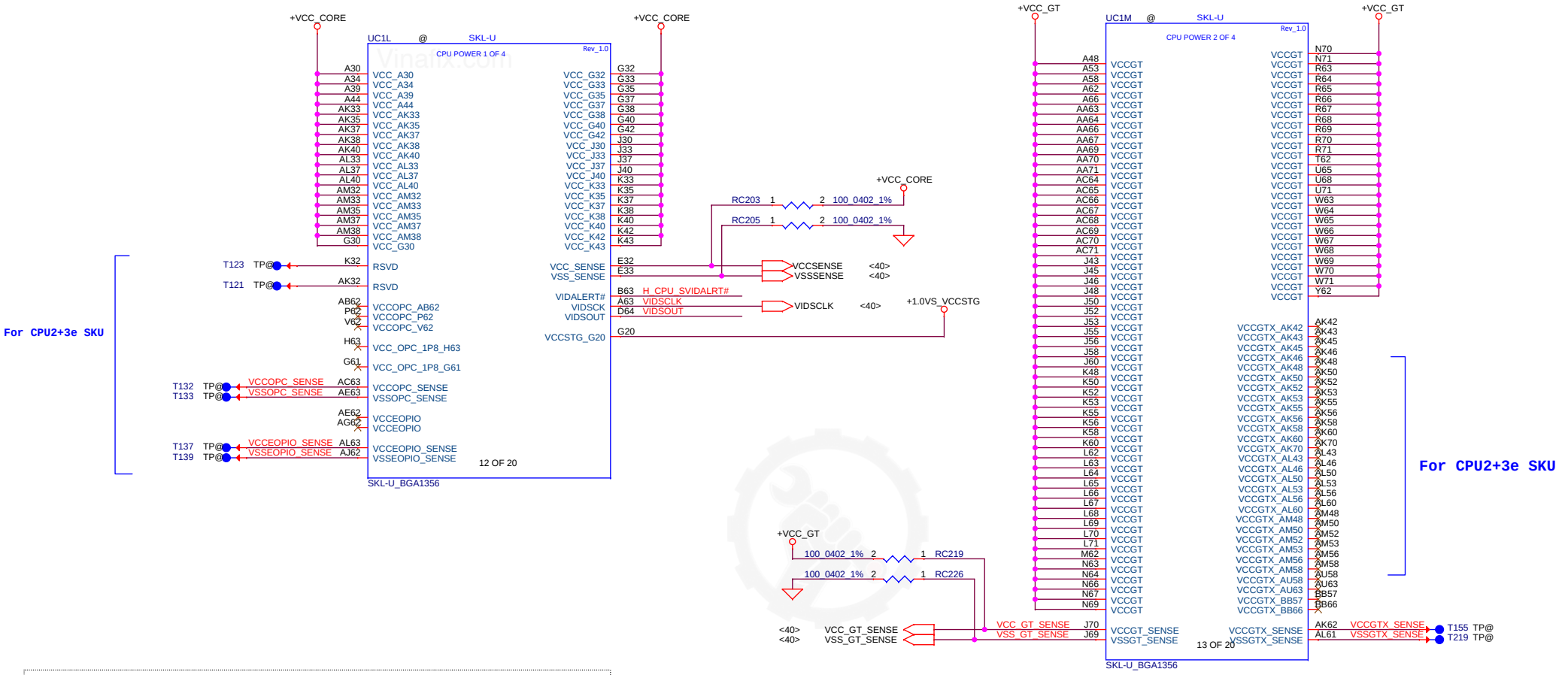
Compal Electronics, Inc.

Title: SKL-U(11/12)GND

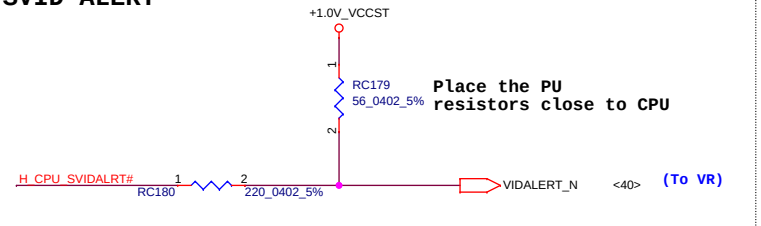
Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 14 of 55

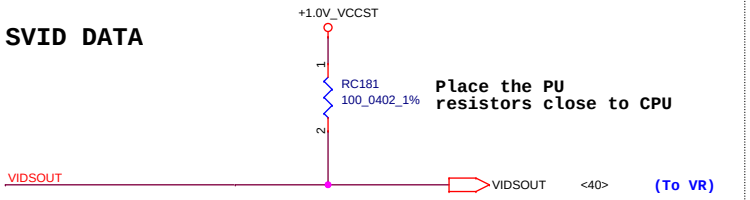
Main Func : CPU



SVID ALERT



SVID DATA



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 15 of 55

Main Func : CPU

+1.35V_VDDQ

PSC Side: CC37 CC38 CC39 CC40 — BSC Side: CC41 CC42 CC43 CC44 CC45 CC46 — 10U_0603_6.3V6M / 1U_0402_6.3V6K

+1.35V_VDDQ : 10UF/6.3V/0603 *6 + 1UF/6.3V/0402 * 4

+1.35V_VDDQC

RC208 1 @ 2 0_0603_5%

BSC Side: CC47 1U_0402_6.3V6K

PSC Side: CC1411 10U_0402_6.3V6M

+1.0V_VCCSTU

RC140 1 2 0_0402_5%

+1.0V_VCCST

PSC Side: CC48 1U_0402_6.3V6K

+1.0VS_VCCSTG

BSC Side: CC56 1U_0201_6.3V6K

+1.35V_VCCSFR_OC

RC141 1 2 0_0402_5%

BSC Side: CC49 0.1U_0201_10V6K

+1.0V_VCCSFR

RC143 1 2 0_0402_5%

PSC Side: CC55 1U_0402_6.3V6K

UC1N @ SKL-U — CPU POWER 3 OF 4 — Rev_1.0

AU23 AU28 AU35 AU42 BB23 BB32 BB41 BB47 BB51	VDDQ_AU23 VDDQ_AU28 VDDQ_AU35 VDDQ_AU42 VDDQ_BB23 VDDQ_BB32 VDDQ_BB41 VDDQ_BB47 VDDQ_BB51	VCCIO ×8	AK28 AK30 AL30 AL42 AM28 AM30 AM42
AM40	VDDQC	VCCSA ×20	AK23 AK25 G23 G25 G27 G28 J22 J23 J27 K23 K25 K27 K28 K30
A18	VCCST		
A22	VCCSTG_A22		
AL23	VCCPLL_OC		
K20	VCCPLL_K20		
K21	VCCPLL_K21		
		VCCIO_SENSE	AM23 VCCIO_SENSE
		VSSIO_SENSE	AM22 VSSIO_SENSE
		VSSSA_SENSE	H21 VSA_SEN-
		VCCSA_SENSE	H20 VSA_SEN+

14 OF 20 — SKL-U_BGA1356

T124 TP@ T125 TP@

+1.0VS_VCCIO

PSC Side: CC36 CC35 CC34 — BSC Side: CC33 CC32 CC31 CC30 CC29 CC28 CC27 — 1U_0402_6.3V6K / 1U_0201_6.3V6K / 10U_0402_6.3V6M

+VCC_SA

RC227 1 2 100_0402_1%

RC228 1 2 100_0402_1%

VSA_SEN- <40>

VSA_SEN+ <40>

+1.0V_PRIM TO +1.0V_VCCSTU

I (Max) : 0.04 A(+1.0V_VCCSTU)
RON(Max) : 25 mohm
V drop : 0.001 V

to +1.0VS_VCCSTG/ +1.0VS_VCCIO <--------

+1.0V_PRIM_JP — @JP14 JUMP_43X79 — +1.0V_PRIM — Imax : 2.77 A

+5VALW

CC98 1U_0402_6.3V6K

CC97 1U_0402_6.3V6K @

+1.0V_VCCSTU

CC96 0.1U_0402_25V6

UC5 EM5209VF_DFN14_2X3

1 2	VIN1 VIN1	VOUT1 VOUT1	14 13
3	ON1	CT1	12 — CC95 1 2 10P_0402_50V8J
4	VBIAS	GND	11
5	ON2	CT2	10 — CC94 1 2 1000P_0402_50V7K
6 7	VIN2 VIN2	VOUT2 VOUT2	9 8
		GPAD	15

Follow 543977_SKL_PDDG_Rev0_91
CC95 10PF ->22us(Spec:<= 65us)

<11,23,37> SIO_SLP_S4# — RC144 1 2 0_0402_5% — EN_1.0V_VCCSTU — @ CC104 1U_0402_6.3V6K

<11,16,23,32,34,41> SIO_SLP_S3# — RC194 1 2 0_0402_5% — EN_1.8VS

+1.8V_PRIM — RC3931 @ 2 0_0603_5% — +1.8V_PRIM_VS — CC99 1U_0402_6.3V6K @

+1.8VS — CC100 0.1U_0402_25V6

For Power consumption Measurement

I (Max) : 0.536 A(+1.8VS)
RON(Max) : 25 mohm
V drop : 0.013 V

+1.8V_PRIM TO +1.8VS

<11,16,23,32,34,41> SIO_SLP_S3#
<11> SIO_SLP_S0#

UC15 TC7SH08FU_SSOP5~D

RZ75 1 @ 2 0_0402_5% — +3VALW

RB751S40T1G_SOD523-2 — DC7

VCCSTG_EN — RC67 49.9K_0402_1% — CC101 0.1U_0402_25V6

VCCSTG_EN_R

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

I (Max) : 3 A(+1.0VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V

+5VALW — CC88 0.1U_0402_25V6 @

+1.0V_PRIM_JP — CC117 1U_0402_6.3V6K

UC6 TPS22961DNYR_WSON8

1 2	VIN1 VIN2	VOUT	6 — +1.0VS_VCCSTG_IO
7	VIN thermal		
3	VBIAS		
4	ON	GND	5

Imax : 0.04 A — RC188 1 2 0_0402_5% — +1.0VS_VCCSTG — CC89 0.1U_0402_25V6 @

Imax : 3 A — @JP15 JUMP_43X79 — +1.0VS_VCCIO — CC90 0.1U_0402_25V6 @

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

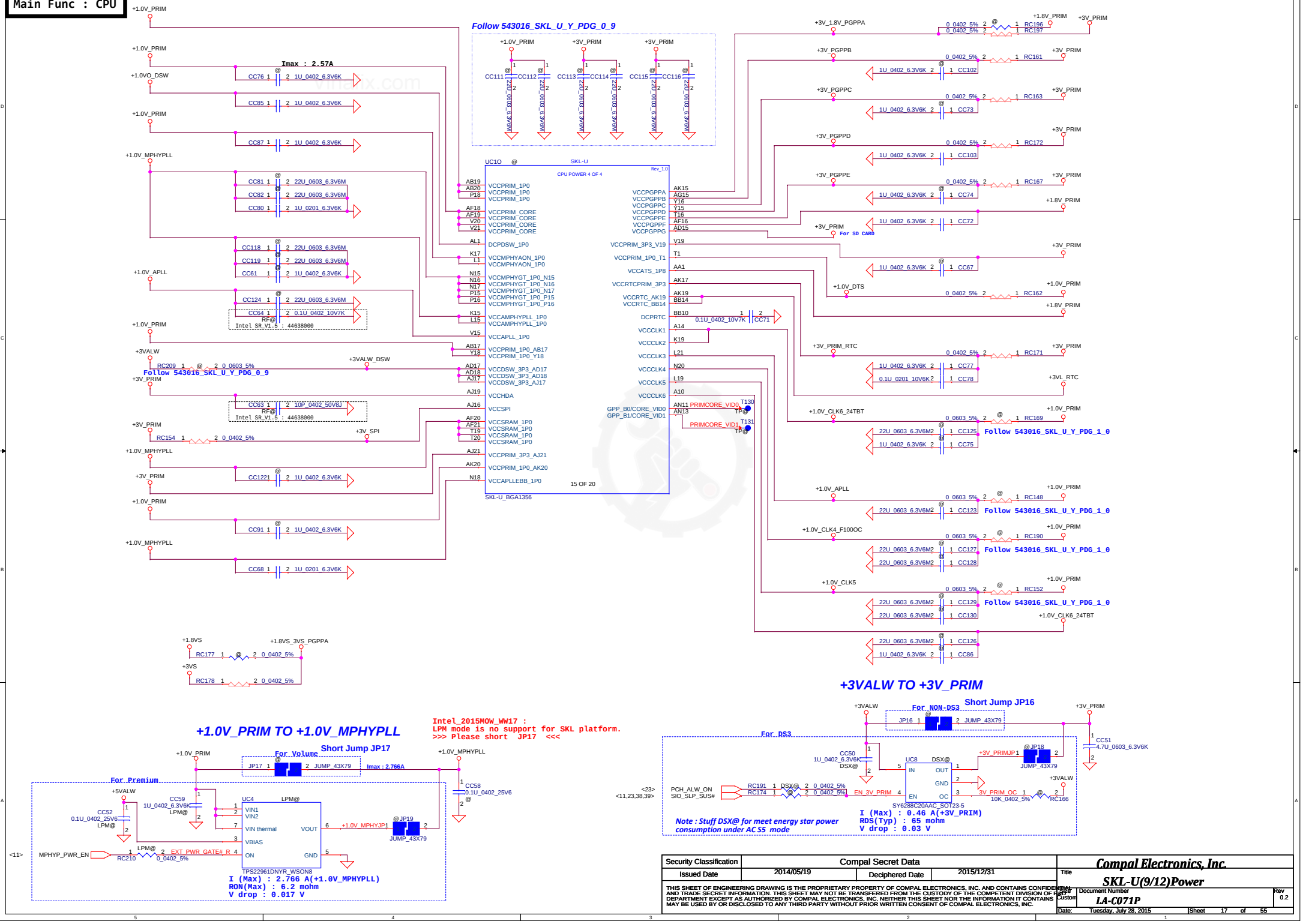
Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: LA-C071P | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 16 of 55

Main Func : CPU



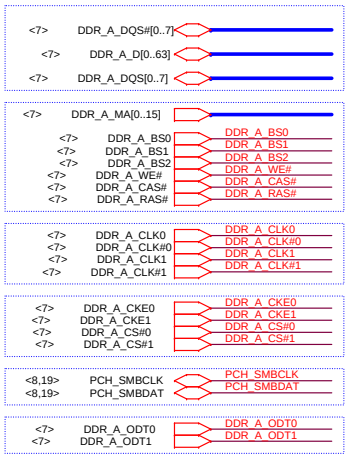
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: LA-C071P		Rev: 0.2
Date: Tuesday, July 28, 2015	Sheet 17 of 55		

Main Func : SO-DIMM A

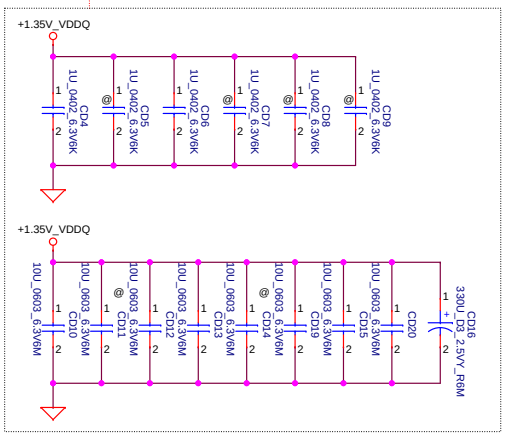
Reverse Type

2-3A to 1 DIMMs/channel

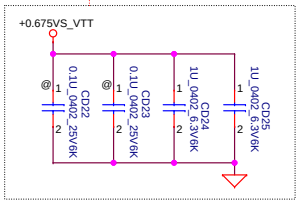


Layout Note:
Place near JDIMM1

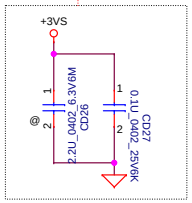
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



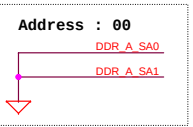
Layout Note:
Place near JDIMM1.203,204

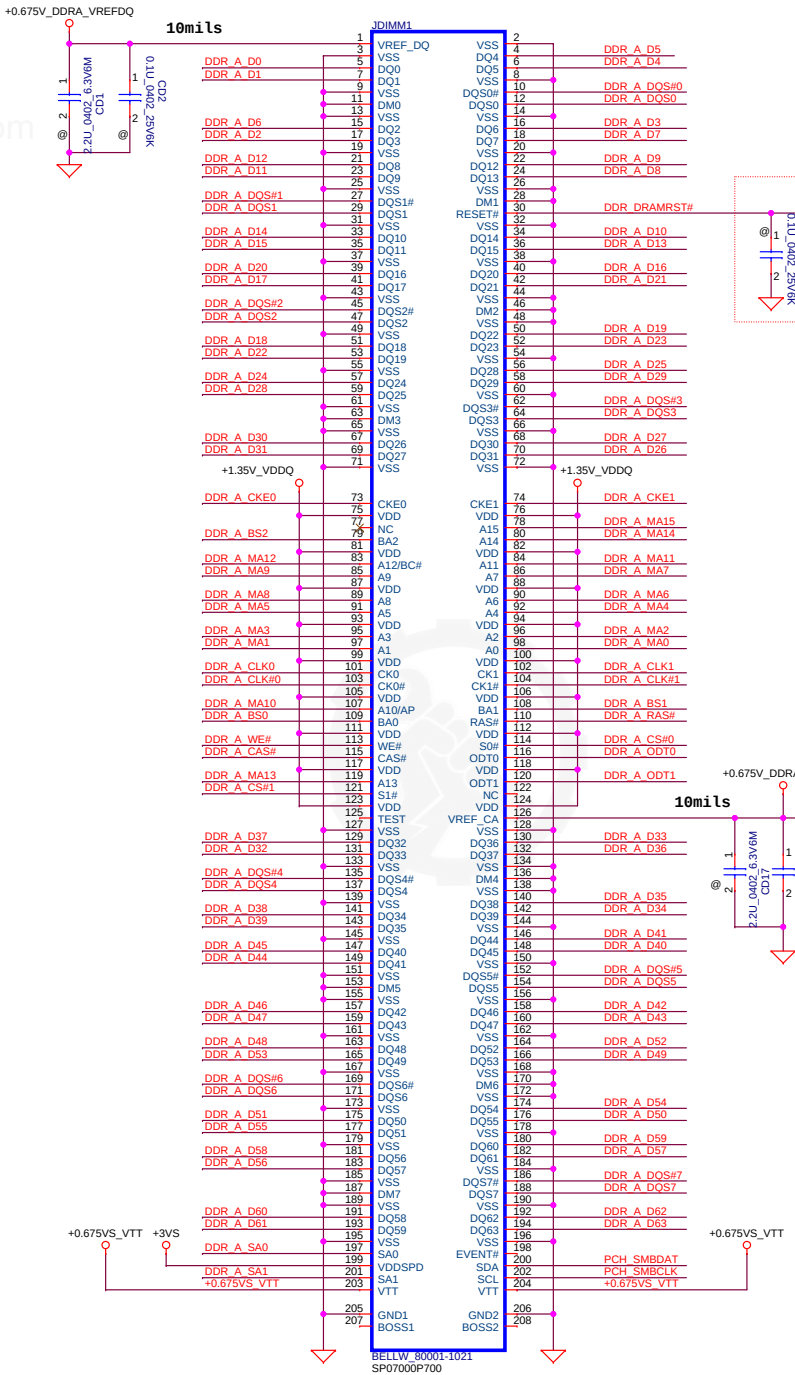


Layout Note:
Place near JDIMM1.199



Address : 00





Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **DDR3L DIMMA**

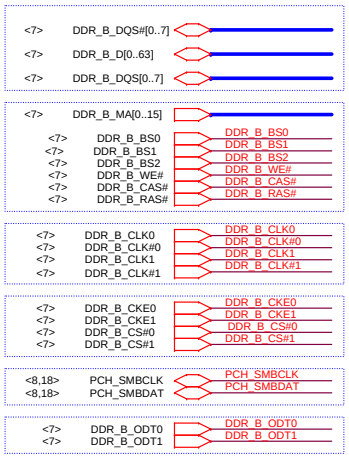
Size: Custom | Document Number: **LA-C071P** | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 18 of 55

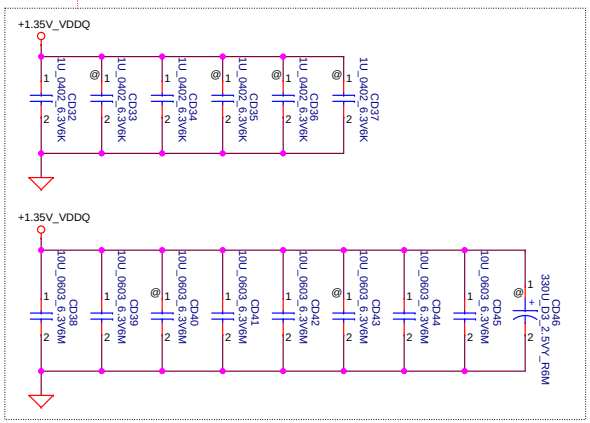
Main Func : SO-DIMM B

Reverse Type

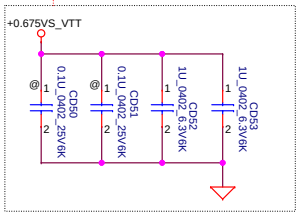
2-3A to 1 DIMMs/channel



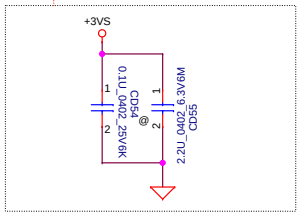
Layout Note:
Place near JDIMM2



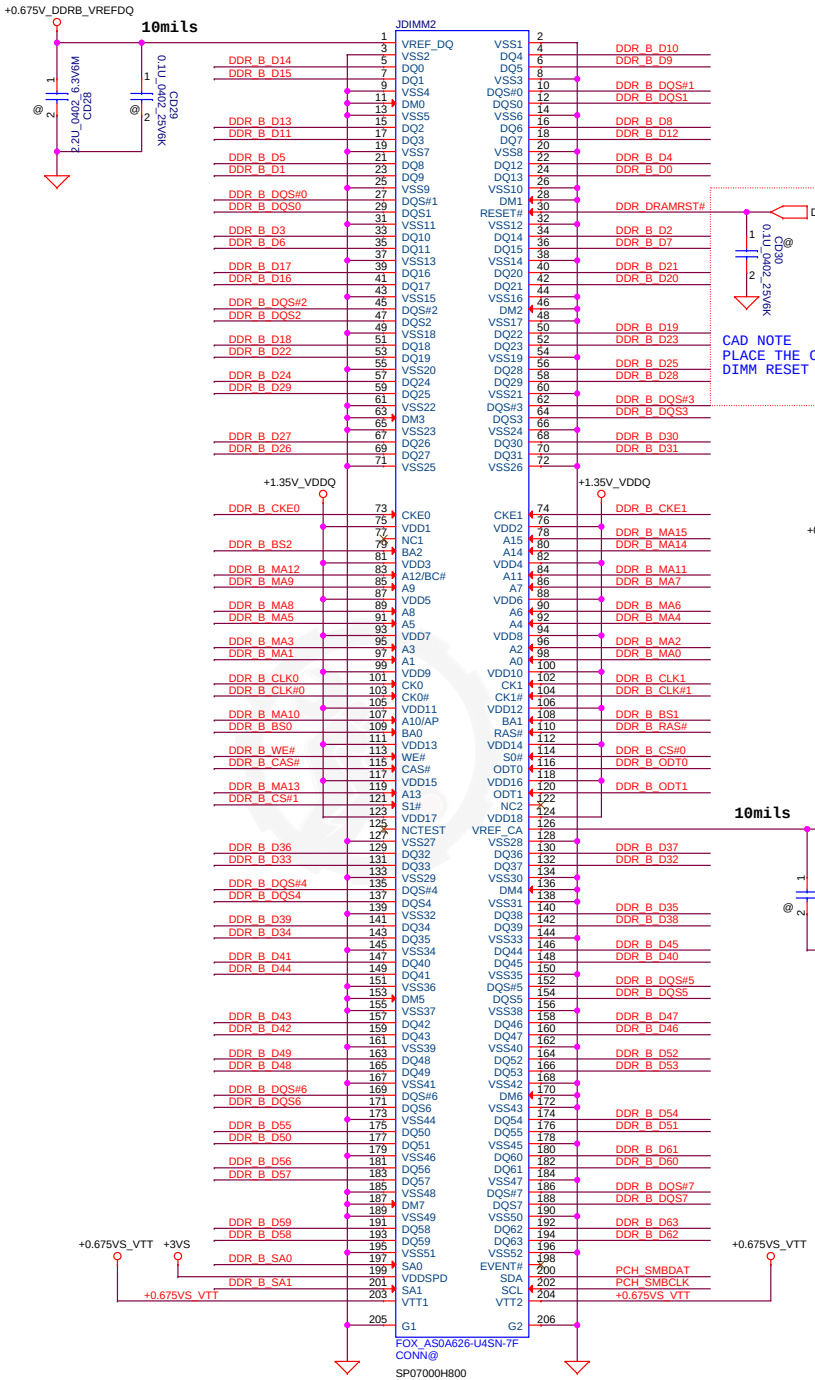
Layout Note:
Place near JDIMM2.203,204

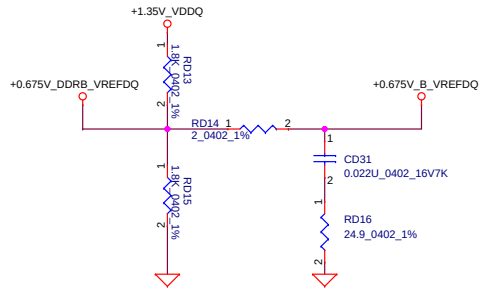


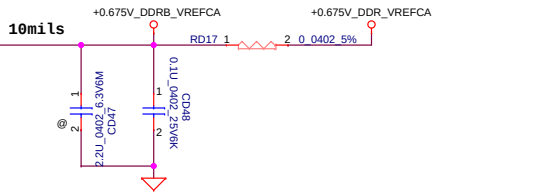
Layout Note:
Place near JDIMM2.199

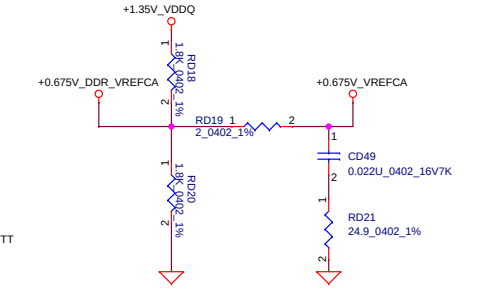


Address : 01









Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **DDR3L DIMMB**

Size: Custom | Document Number: **LA-C071P** | Rev: 0.2

Date: Tuesday, July 28, 2015 | Sheet 19 of 55

Main Func : Screw

Screw Hole

H1 H_2P8N @
H20 H_2P8N @
H21 H_2P8N @
H22 H_2P8X3P3N @
H23 H_2P8X4P8N @

H2 H_2P8 @
H3 H_2P8 @
H4 H_2P8 @
H5 H_2P8 @
H6 H_2P8 @
H7 H_2P8 @
H8 H_2P8-G @
H9 H_2P8 @

H10 Delete.
Layout informed PCB vendor to do PTH solution.
(Function is same as beofre.)

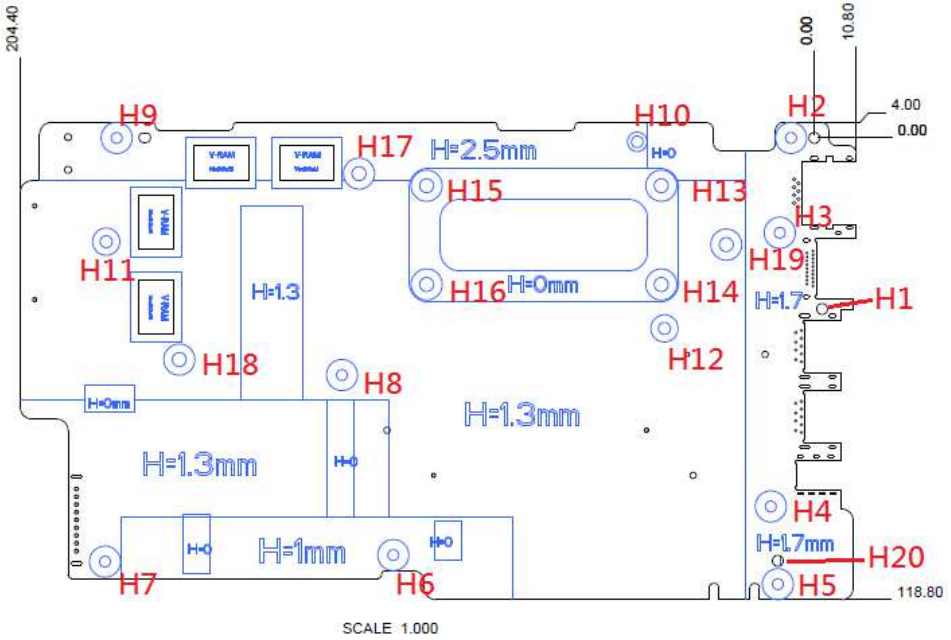
H11 H_2P8 @
H12 H_2P8 @

H13 H_3P6-G @
H14 H_3P6-G @
H15 H_3P6-G @
H16 H_3P6-G @
CPU bracket

H17 H_3P3-G @
H18 H_3P3-G @
VGA stand-off

H19 H_3P3 @
NGFF stand-off

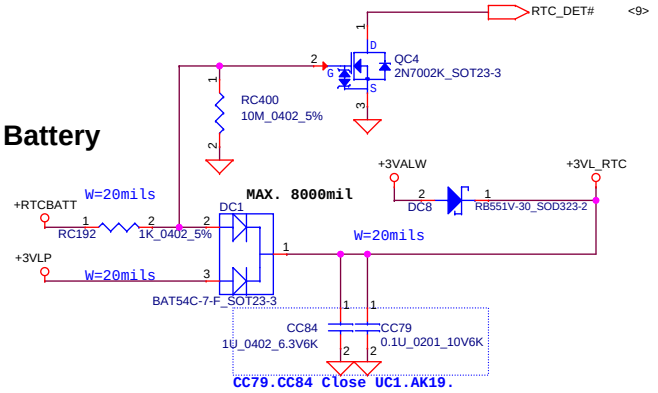
FD1 @FIDUCAL
FD2 @FIDUCIAL
FD3 @FIDUCAL
FD4 @FIDUCIAL



SCALE 1.000

Main Func : RTC

RTC Battery



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: Screw Hole

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Tuesday, July 28, 2015 | Sheet 20 of 55

Main Func : Audio

Reserve for HDA issue

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

Close to UA1
Pin11,13,14,16

AGND was requested by Realtek

EC Beep

MCU Beep

Place on the moat between GND & GNDA.

iPhone and Nokia type Combo Jack

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

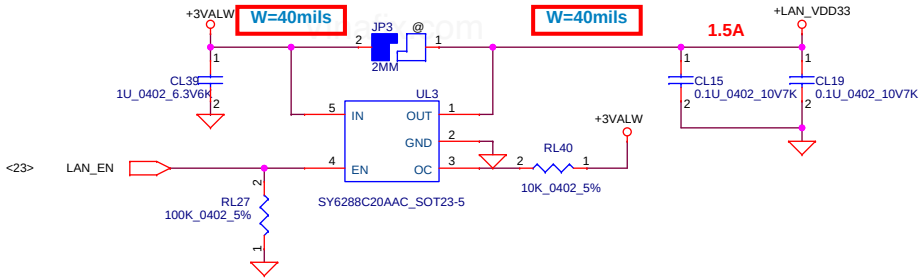
Title: **Audio Codec ALC3234**

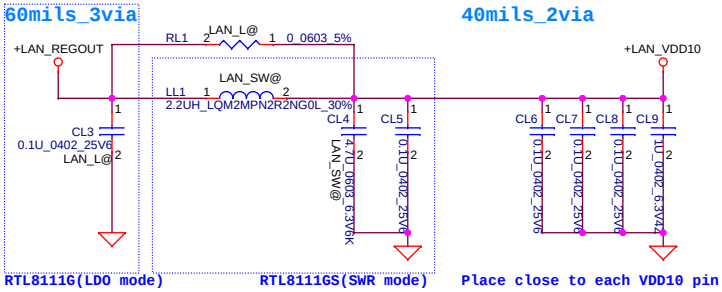
Size | Document Number: **LA-B015P** | Rev: 0.1

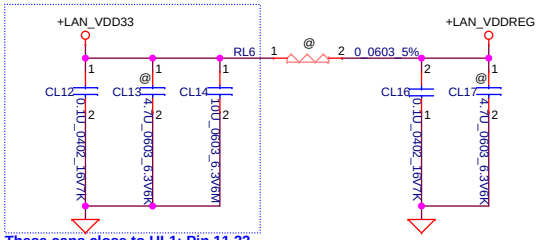
Date: Tuesday, July 28, 2015 | Sheet 21 of 55

Main Func : 10/100 LAN

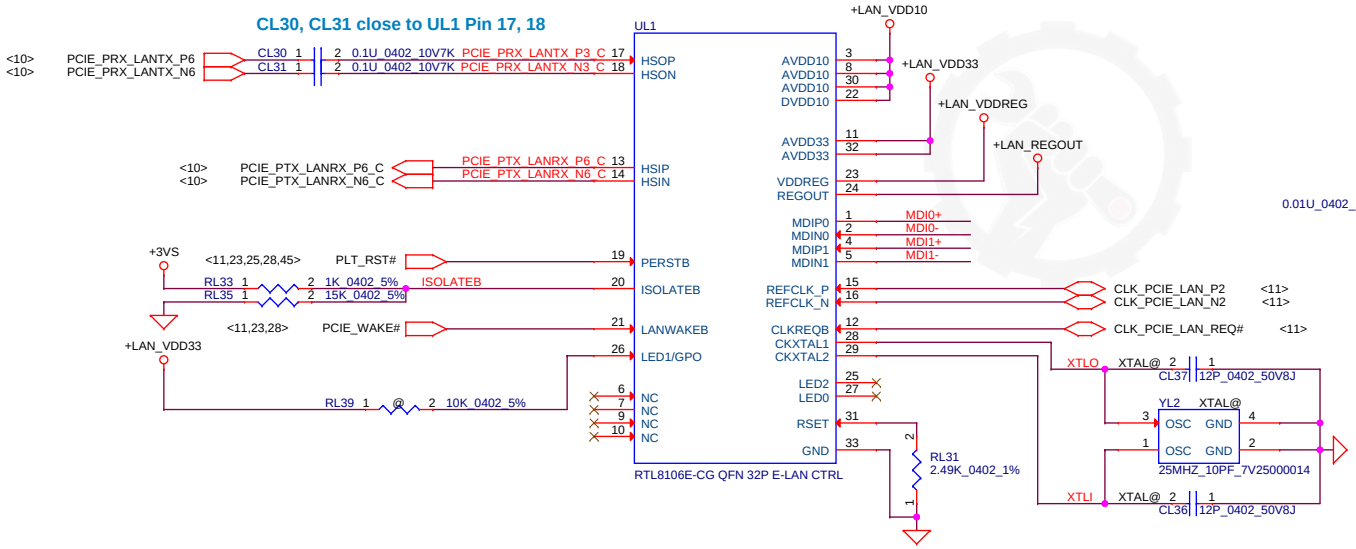
+LAN_VDD33 rising time : >1ms and <100ms

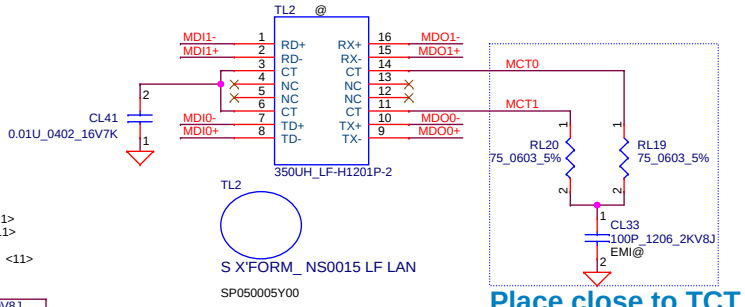




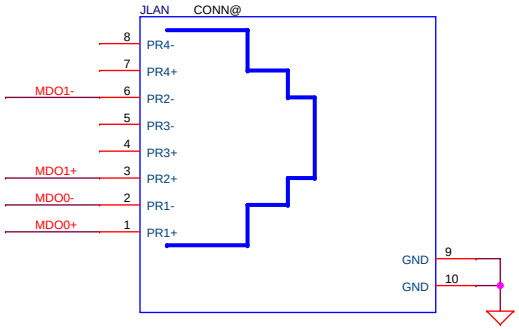


CL30, CL31 close to UL1 Pin 17, 18





Place close to TCT pin



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

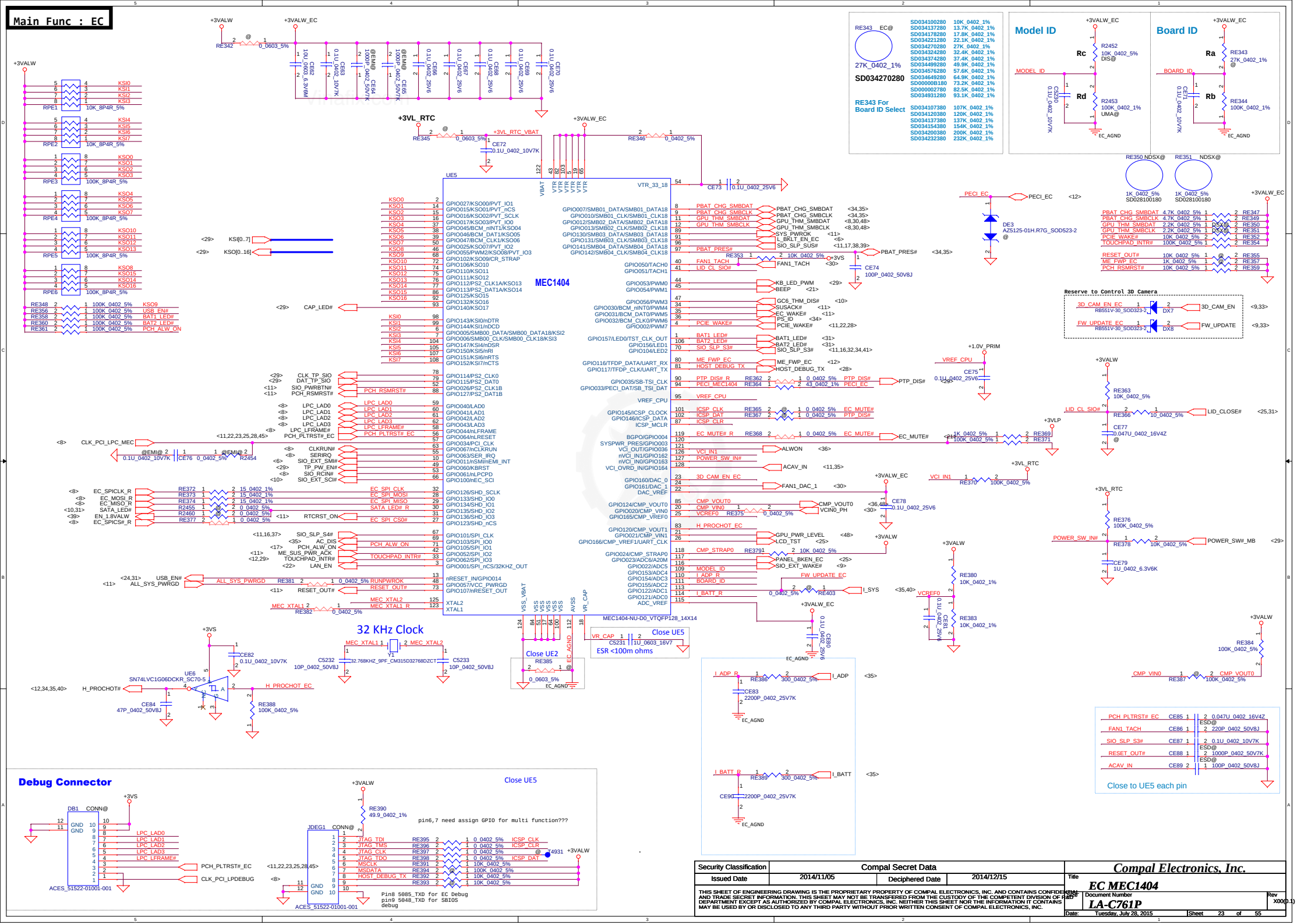
Compal Electronics, Inc.

Title: 10/100 LAN

Size: Custom | Document Number: LA-B015P | Rev: 0.1

Date: Tuesday, July 28, 2015 | Sheet 22 of 55

Main Func : EC



Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

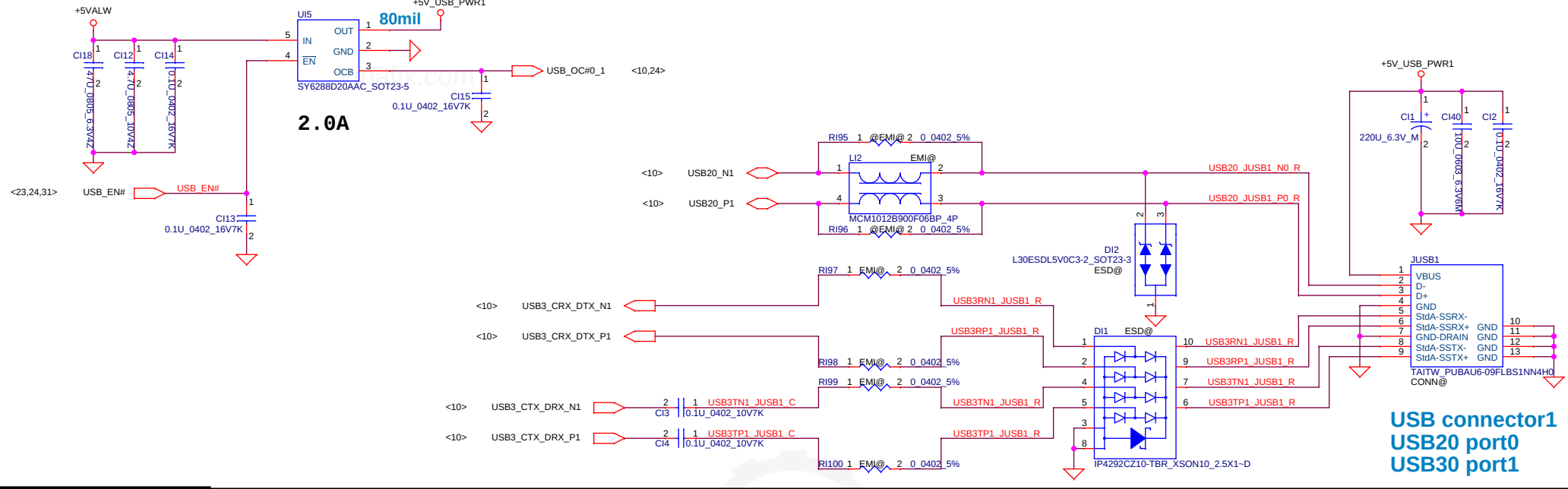
Title: EC MEC1404

Document Number: LA-C761P

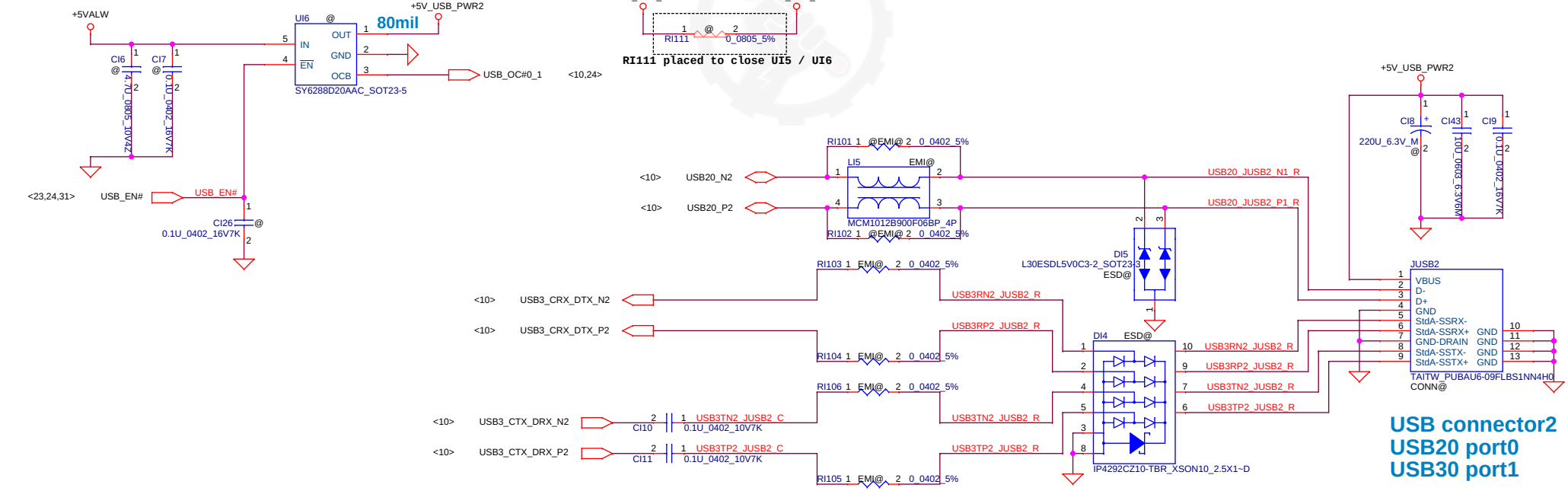
Rev: X00(0.1)

Date: Tuesday, July 28, 2015 Sheet 23 of 55

Main Func : USB 3.0 Port



Main Func : USB 3.0 Port



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

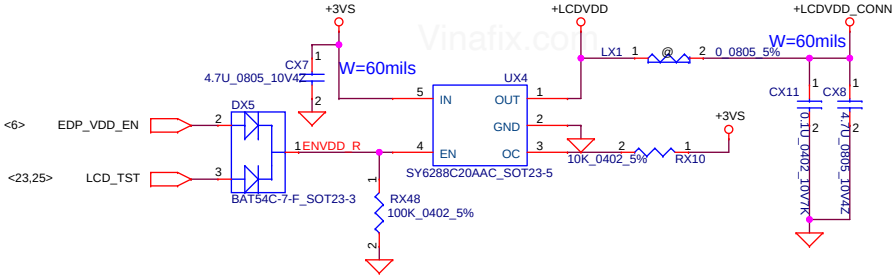
Title: **USB3.0**

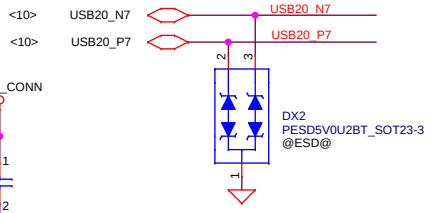
Size: B | Document Number: **LA-B015P** | Rev: 0.1

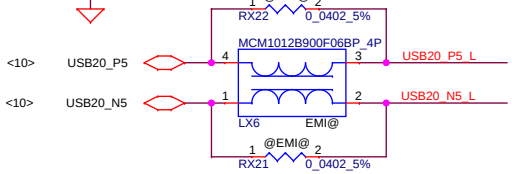
Date: Tuesday, July 28, 2015 | Sheet 24 of 55

Main Func : LCD

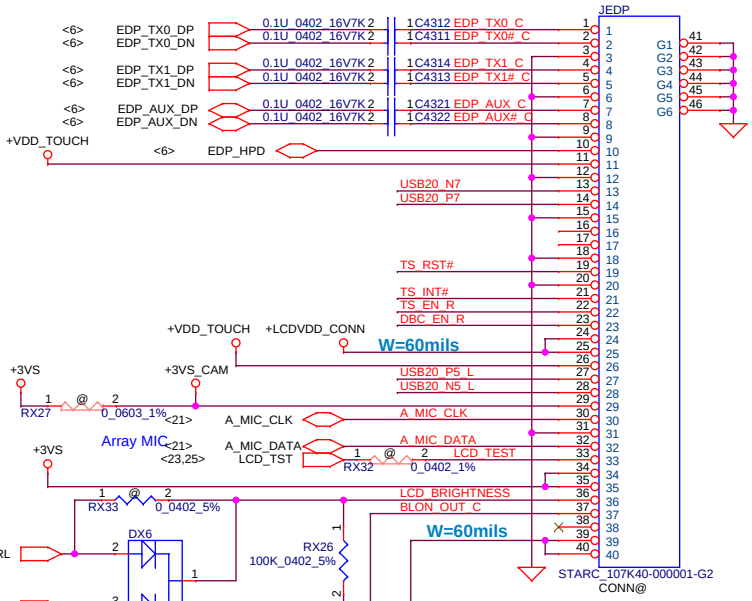
LCD PWR CTRL





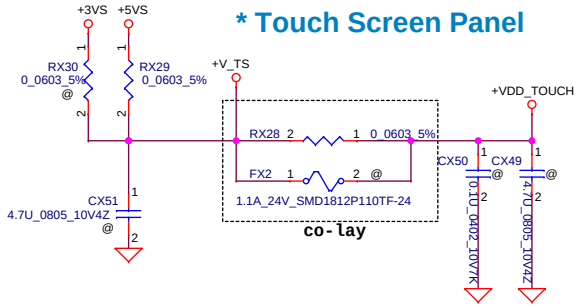


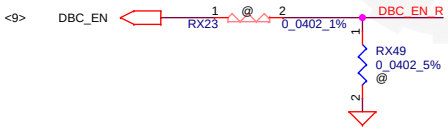
eDP Connector

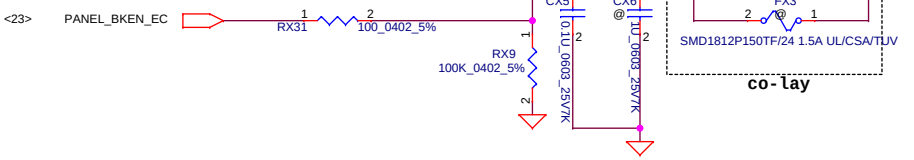


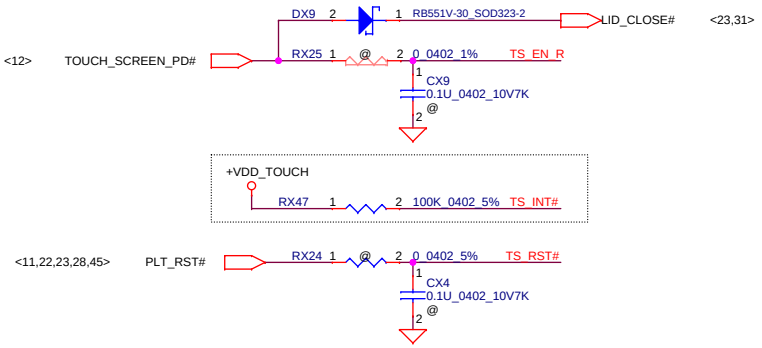
Web Cam PWR

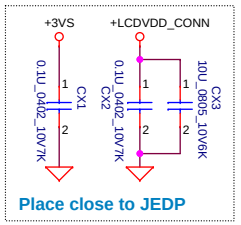
* Touch Screen Panel









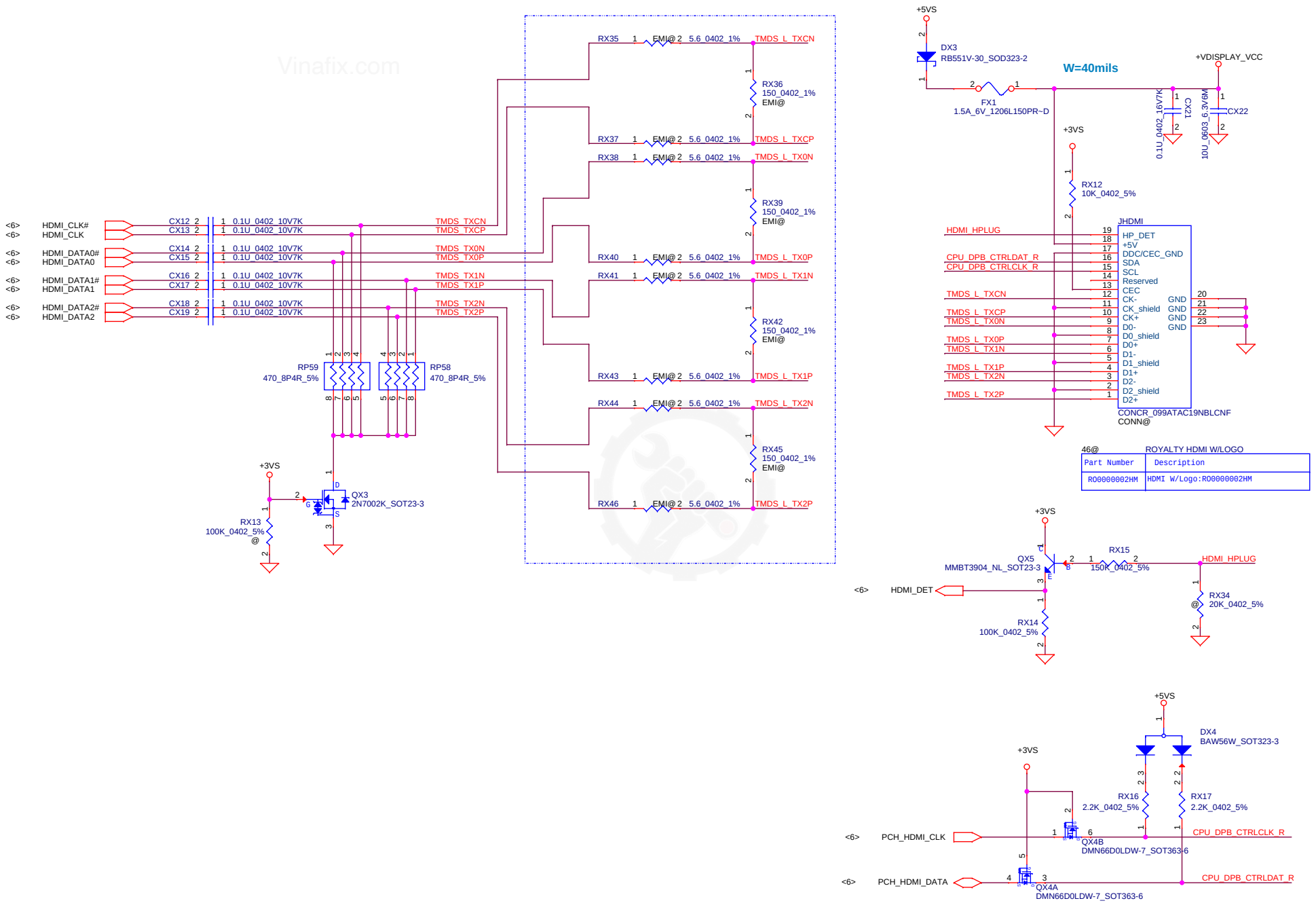


Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.			
Title: eDP / webcam / TouchScreen			
Size: C	Document Number: LA-B015P		Rev: 0.1
Date: Tuesday, July 28, 2015	Sheet 25 of 55		

Main Func : HDMI

Place close to JHDMI



46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

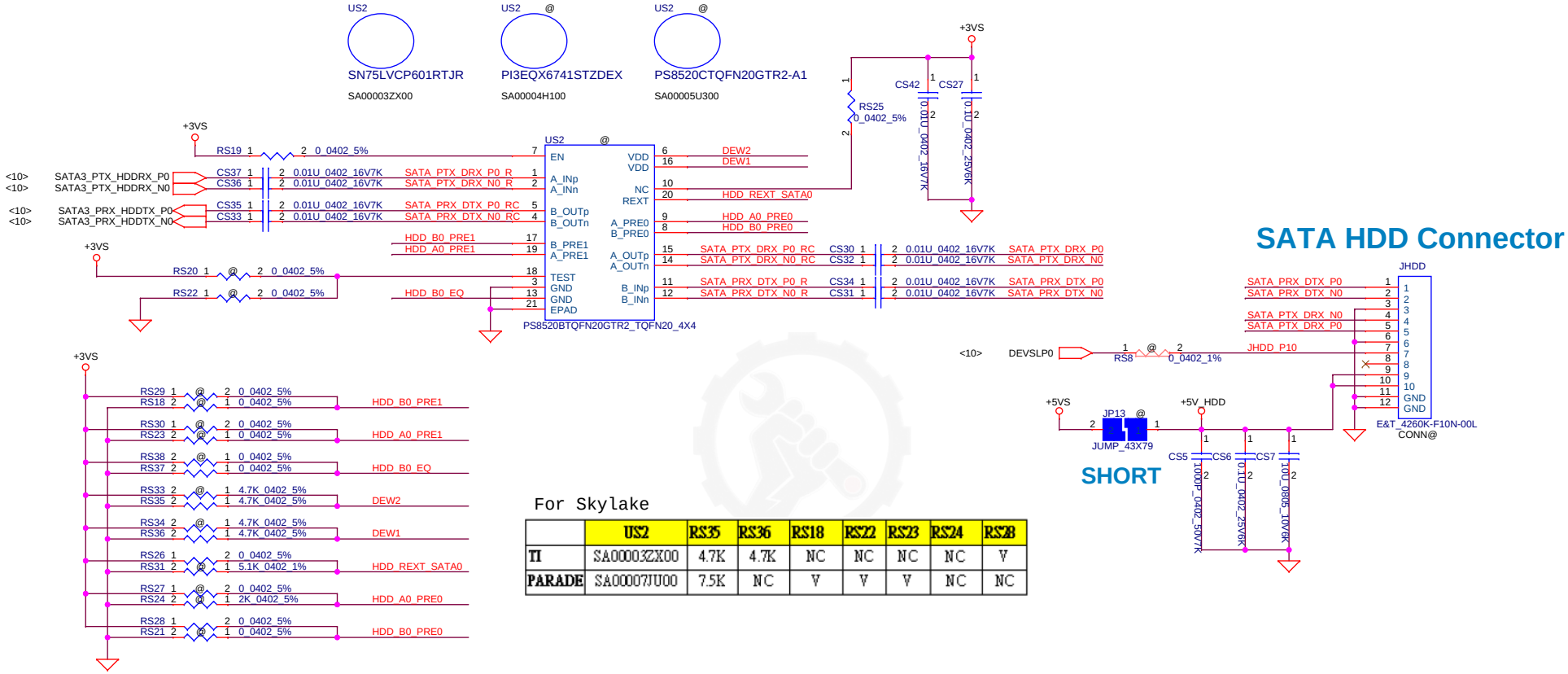
Compal Electronics, Inc.

Title: **HDMI**

Size: B | Document Number: **LA-B015P** | Rev: 0.1

Date: Tuesday, July 28, 2015 | Sheet 26 of 55

Main Func : HDD



For Skylake

	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	NC	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

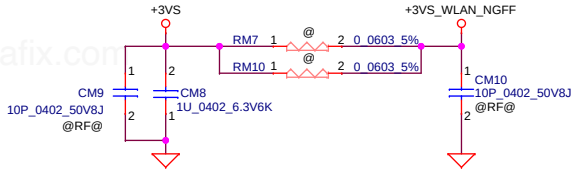
Title: HDD / Free Fall Sensor

Size: Document Number: LA-B015P Rev: 0.1

Date: Tuesday, July 28, 2015 Sheet 27 of 55

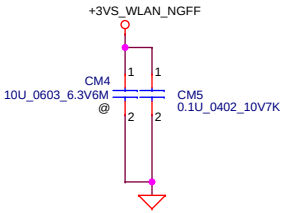
Main Func : WiFi/BT

+3S TO +3VS_WLAN_NGFF

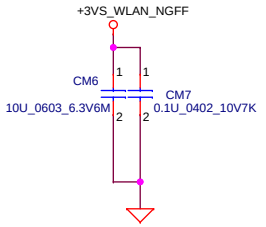


NGFF WL Con (E Key)

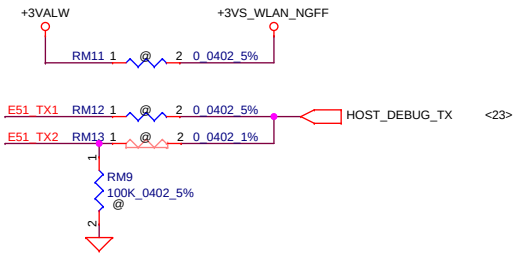
closed to pin 2, 4



closed to pin 64, 66



Reserved for NGFF Debug Card



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: NGFF WLAN

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Tuesday, July 28, 2015 | Sheet 28 of 55

Main Func : PWR SW

Power ON Circuit

ON/OFF switch

TOP Side

SW1
SMT1-05-A_4P

POWER_SW#_MB <23>

CE20
0.1U_0402_16V7K

DE2
L03ESDL5V0CC3-2_SOT23-3
@ESD@

Main Func : Keyboard

INT_KBD Connector

JKB

<9> KB_DET#

KSI[0..7]
KSO[0..16]

<23> KSI[0..7]
<23> KSO[0..16]

CAP_LED

HB_A823020-SBHR21
CONN@

+3VS

RE330
100K_0402_5%

<23> CAP_LED#

QE11
LN2306LT1G_SOT23-3

CAP_LED_R

QE10
DDTA144VCA-7-F-GP

+5VS

CAP_LED_Q

RE401
1K_0402_5%

CAP_LED

Main Func : KBBL

Key Board Back Light

Tulip 設計，要看CPU 電壓耐壓SPEC
建議改 56K_5% (SD028560200)

<12> KB_LED_BL_DET

+5VS
20mil
FE12 KBBL@
0.5A_13.2V_NANOSMDC050F-13.2-2

+5VS_KBL
20mil

CE56
1U_0603_10V6K
KBBL@

CE57
10U_0603_6.3V6M
@

RE61 KBBL@ 51K_0402_5%

RE58
100K_0402_5%
KBBL@

JKBBL
ACES_50524-00401-P01
CONN@

KB_BL_PWM

20mil

QE5
AP2606AGY-HF 1N SOT26-6

<23> KB_LED_PWM

KBBL@

Main Func : TouchPAD

Touch PAD

+3VS
+3VS_TOUCH

RE399 @ 0_0402_5%

+3VALW

QE9 @
NTK3139PT1G_SOT723-3

RE4001 0_0402_5%

CE61
1U_0402_6.3V6K
@

RE402
100_0402_1%

<23> TP_PW_EN#

QE8
2N7002KW 1N SOT323-3

QE9
S TR PJV1701 1P SOT723-3

SB000017J00

+3VS
+3VS_TOUCH

RE335
4.7K_0402_5%
PTP@

RE334
4.7K_0402_5%
PTP@

<9> I2C_SDA_TP
<9> I2C_SCL_TP

QE6B
DMN66D0LDW-7_SOT363-6
PTP@

QE6A
DMN66D0LDW-7_SOT363-6
PTP@

I2C_SDA_TP_R
I2C_SCL_TP_R

RE336 @ 0_0402_5%
RE337 @ 0_0402_5%

TP/PTP

+3VS_TOUCH

RE329
10K_0402_5%

RC78
100K_0402_5%
PTP@

CE58
1U_0402_6.3V6K~D

JTP
ACES_51524-0080N-001
CONN@

I2C_SDA_TP_R
I2C_SCL_TP_R

INT_TP#

DE4
RB551V-30_SOD323-2

TP_LOCK#

<23> PTP_DIS#
<23> DAT_TP_SIO
<23> CLK_TP_SIO

<12,23> TOUCHPAD_INTR#

QE7
2N7002KW 1N SOT323-3

RE339
4.7K_0402_5%

RE338
4.7K_0402_5%

@EMI@

CE91 680P_0402_50V7K
CE92 680P_0402_50V7K

DAT_TP_SIO
CLK_TP_SIO

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size: Document Number: LA-B015P

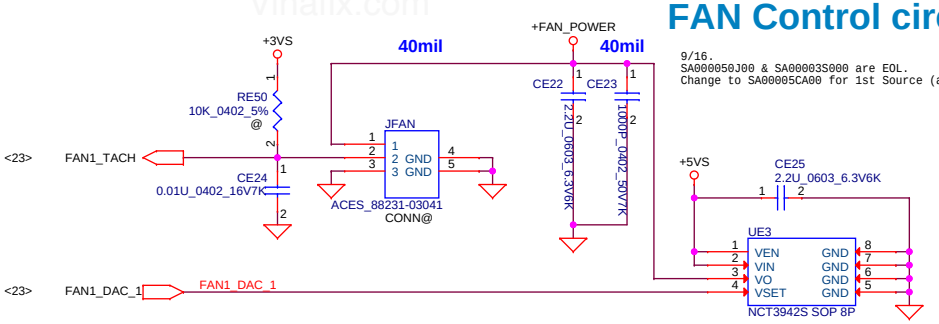
Rev: 0.1

Date: Tuesday, July 28, 2015

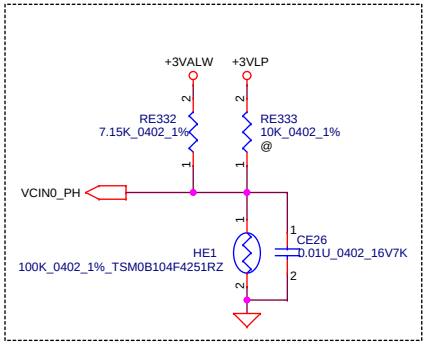
Sheet 29 of 55

Main Func : Fan/Thermal

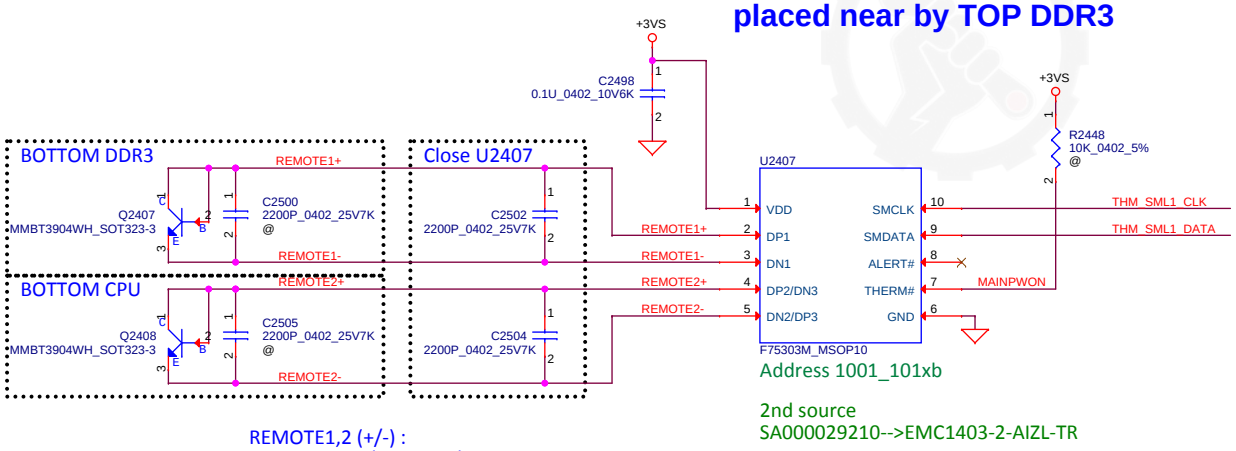
FAN Control circuit



CPU Bottom side



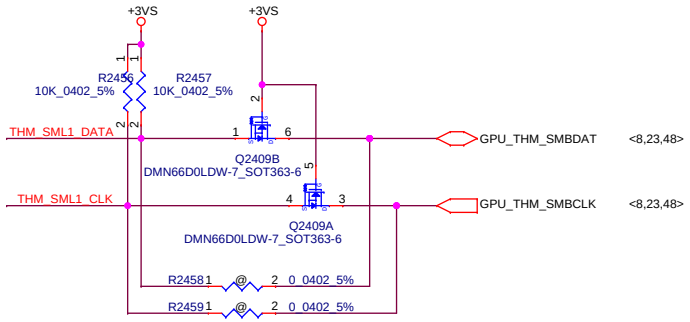
Fintek thermal sensor placed near by TOP DDR3



Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

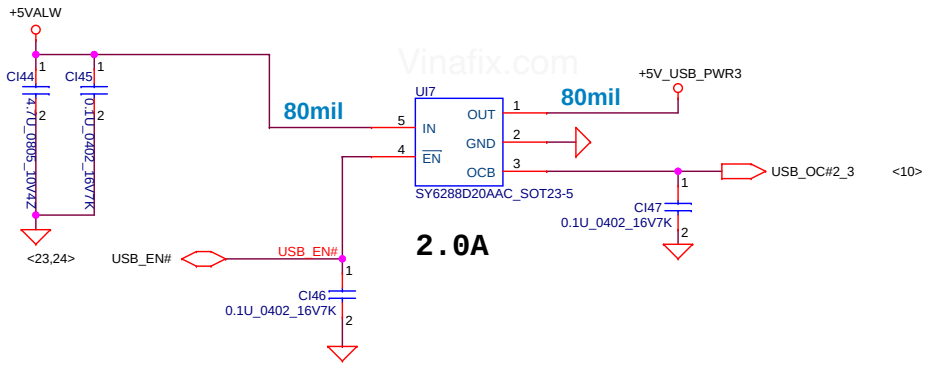
Compal Electronics, Inc.

Title: **Thermal Sensor**

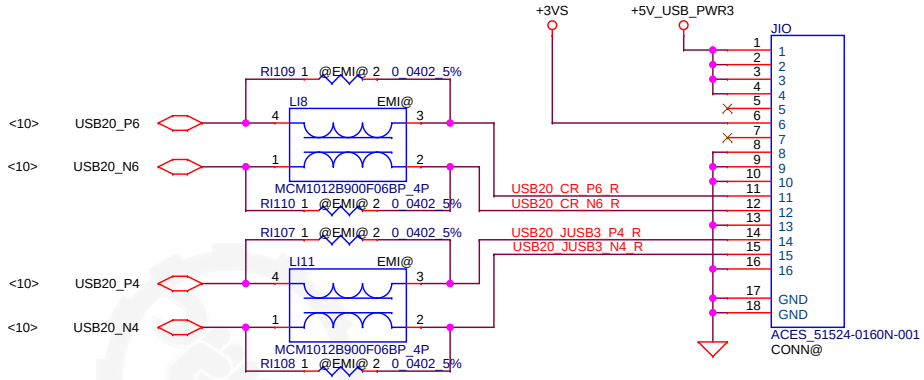
Size: Document Number: **LA-B015P** Rev: 0.1

Date: Tuesday, July 28, 2015 Sheet 30 of 55

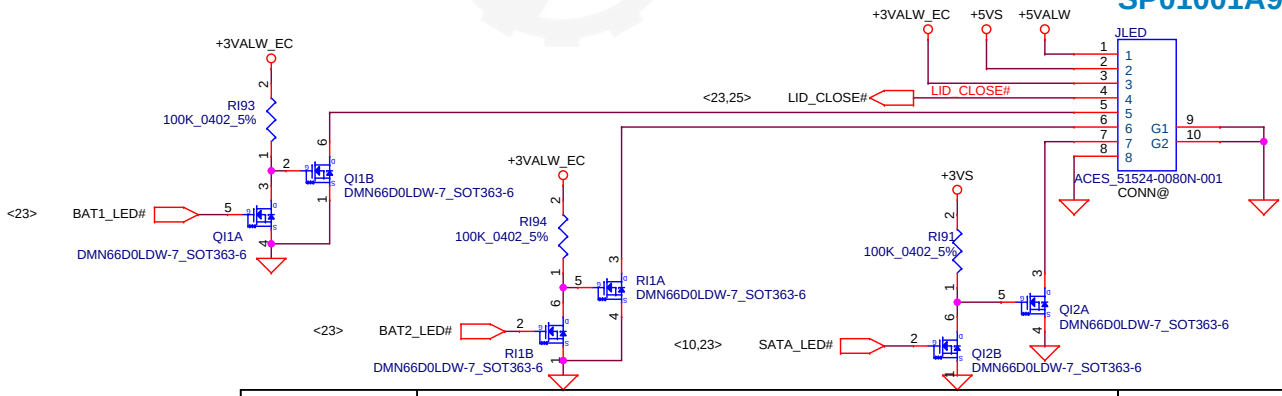
Main Func : DB CONN



IO to MB CONN
Substitute:SP01001FS00



LED/B TO M/B
SP01001A900

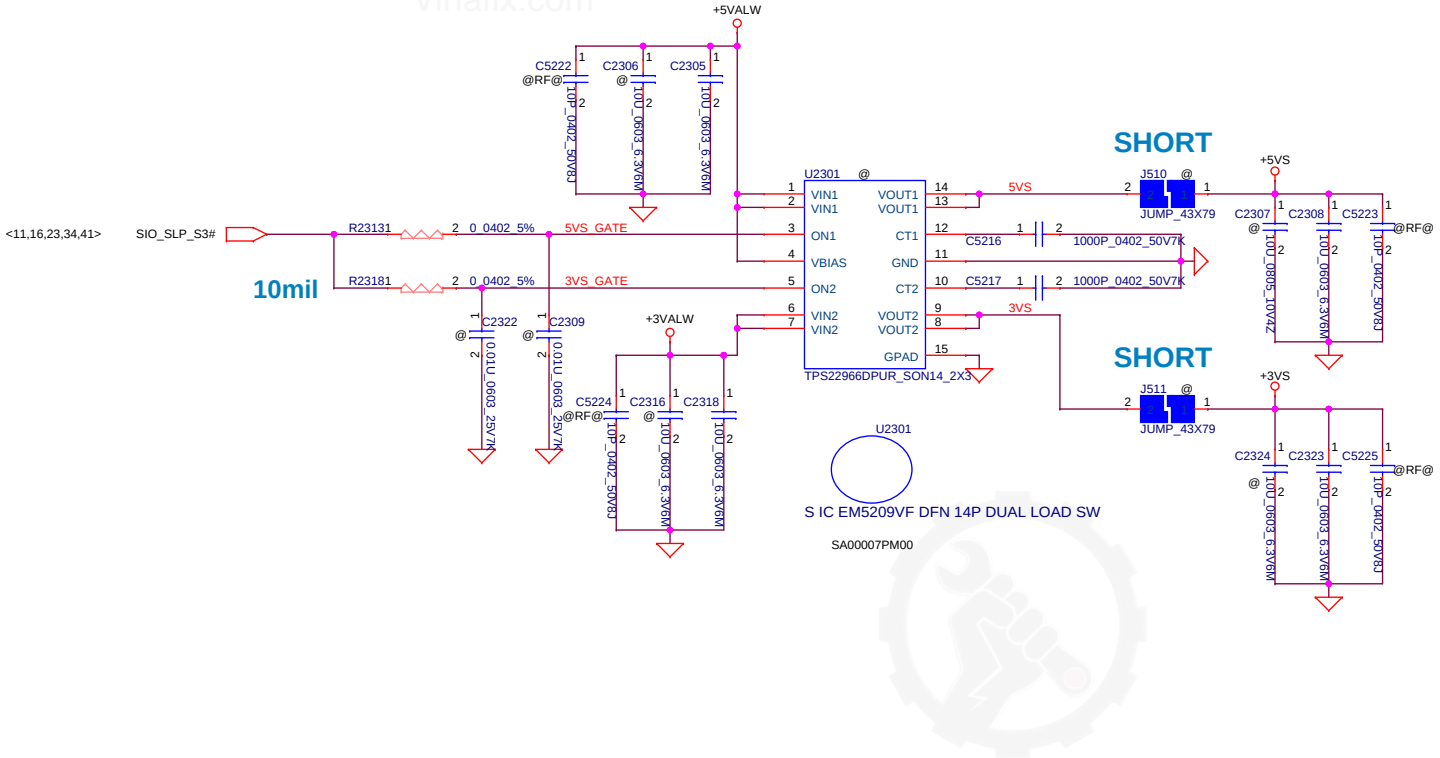


Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Title	IO/B, LED/B		
Size: B	Document Number: LA-B015P		Rev: 0.1
Date: Tuesday, July 28, 2015	Sheet 31 of 55		

Main Func : DC/DC

+5VS and +3VS switch



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: DC/DC Interface

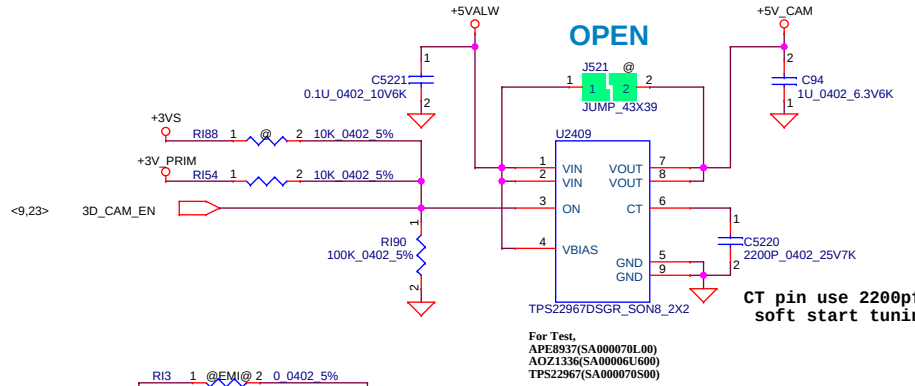
Size: D | Document Number: LA-B015P | Rev: 0.1

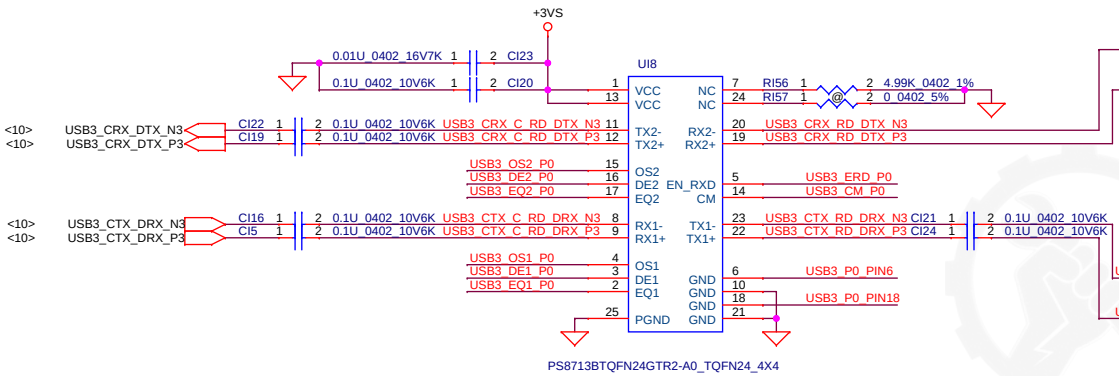
Date: Tuesday, July 28, 2015 | Sheet 32 of 55

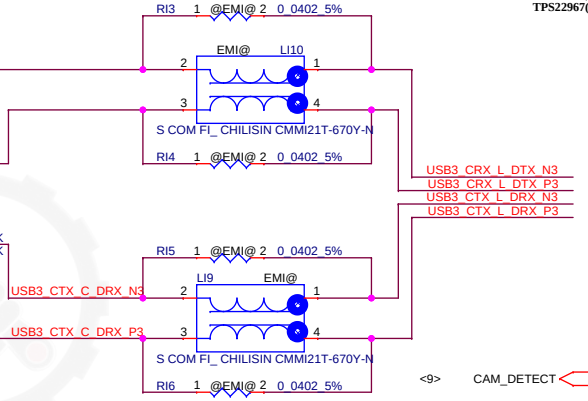
Main Func : 3D Camera

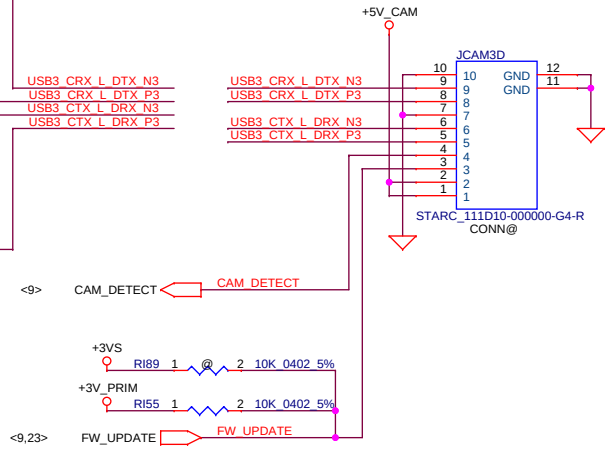
	Vendor	PS8713B	TI	Spec			schematic netname	3Vs		GND	
1		VDD	VCC	Same							
2		B_EQ0	EQ1	**LL:** 9.5dB (default)	**LH:** 13dB	**HL:** 4.5dB **HH:** 7.7 dB	USB3_EQ1_P0	RI23	@	RI32	@
3		DE0	DE1	LL: 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB **HH:** 5 dB	USB3_DE1_P0	RI26	@	RI35	@
4		EQ1	OS1	**LL:** 9.5dB	**LH:** 13dB	**HL:** 4.5dB **HH:** 7.7 dB	USB3_OS1_P0	RI22	@	RI40	@
5		PD#	EN_RXD	it can be left open			USB3_ERD_P0	RI44	@	RI48	@
6		B_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB **HH:** 5 dB	USB3_P0_PIN6	RI53	@	RI49	@
7		REXT	NC	4.99K						RI56	4.99K
8		B_Inn	RX1-	Same							
9		B_Inp	RX1+	Same							
10		GND	GND	Same							
11		A_OUTn	TX2-	Same							
12		A_OUTp	TX2+	Same							
13		VDD	VCC	Same							
14		TST/NC	CM	4.7K ohm resistor for perfomance adjustment			USB3_CM_P0	RI42	@	RI46	@
15		A_EQ1	OS2	LL: 9.5 dB (default)	**LH:** 13 dB		USB3_OS2_P0	RI19	@	RI87	@
16		A_DE0	DE2	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB **HH:** 5 dB	USB3_DE2_P0	RI20	@	RI31	@
17		A_EQ0	EQ2	LL: 9.5 dB (default)	**LH:** 13 dB		USB3_EQ2_P0	RI21	@	RI36	@
18		A_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB **HH:** 5 dB	USB3_P0_PIN18	RI52	@	RI50	@
19		A_Inp	RX2+	Same							
20		A_Inn	RX2-	Same							
21		GND	GND	Same							
22		B_OUTp	TX1+	Same							
23		B_OUTn	TX1-	Same							
24		I2C_EN	NC	this pin canbe NC or connected to GND			NC			RI57	@

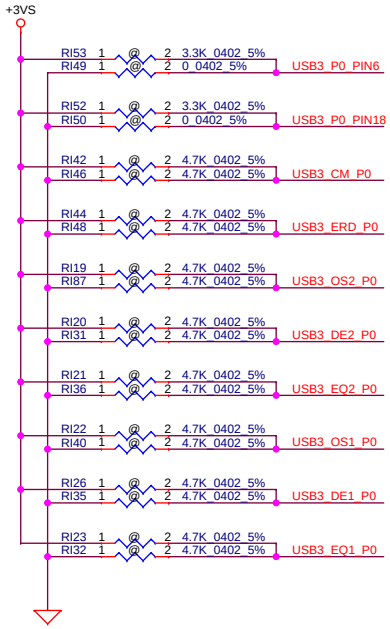
+5VALW TO +5V_3DCAM



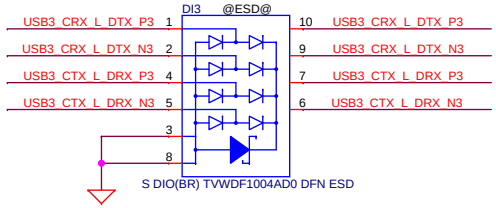








Layout request to swap pin !



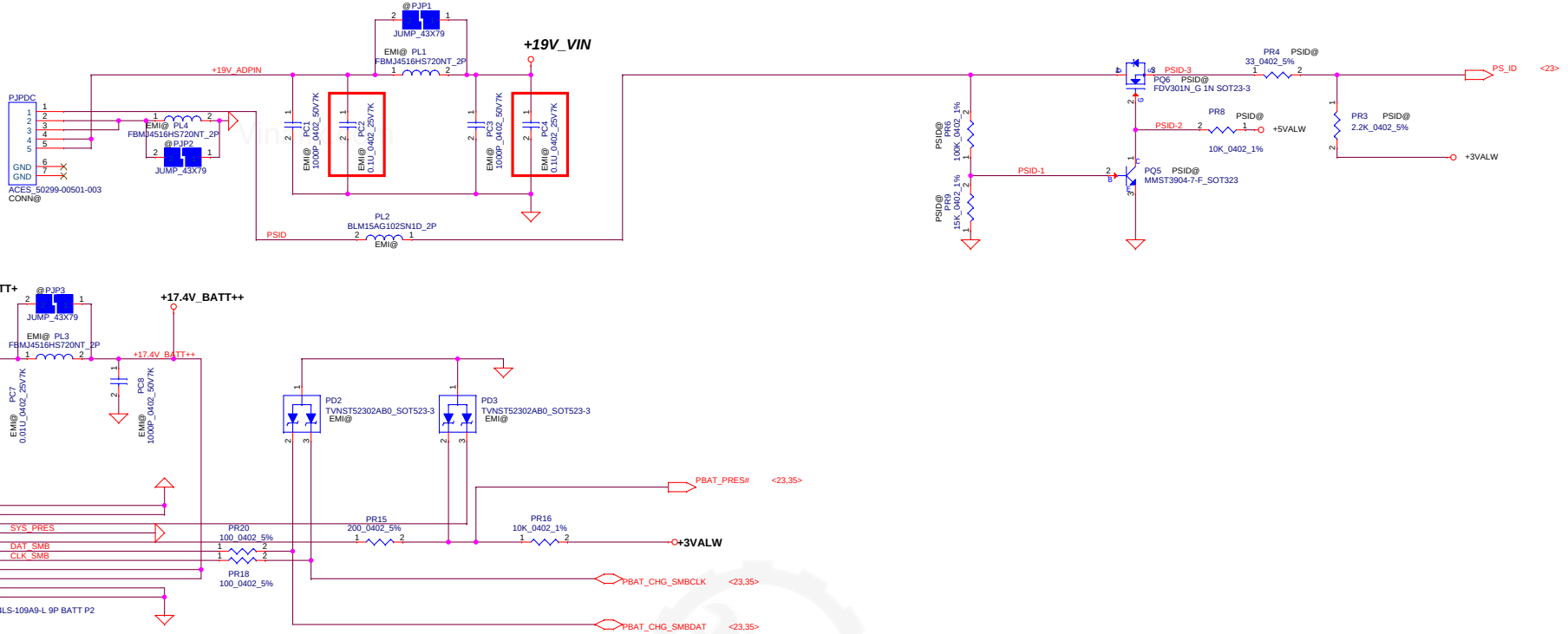
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **3D CAMERA**

Size: B | Document Number: **LA-B015P** | Rev: 0.1

Date: Tuesday, July 28, 2015 | Sheet 33 of 55

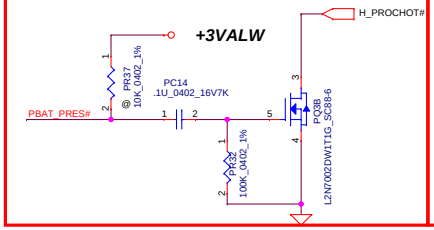


SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)

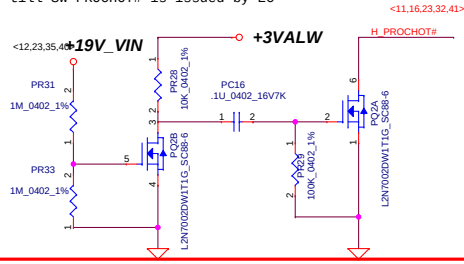
Adapter protection:

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

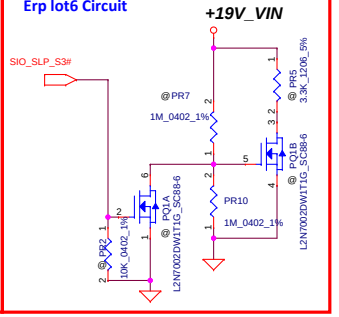


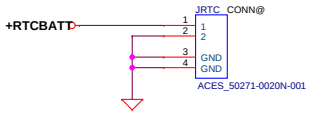
Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit





DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

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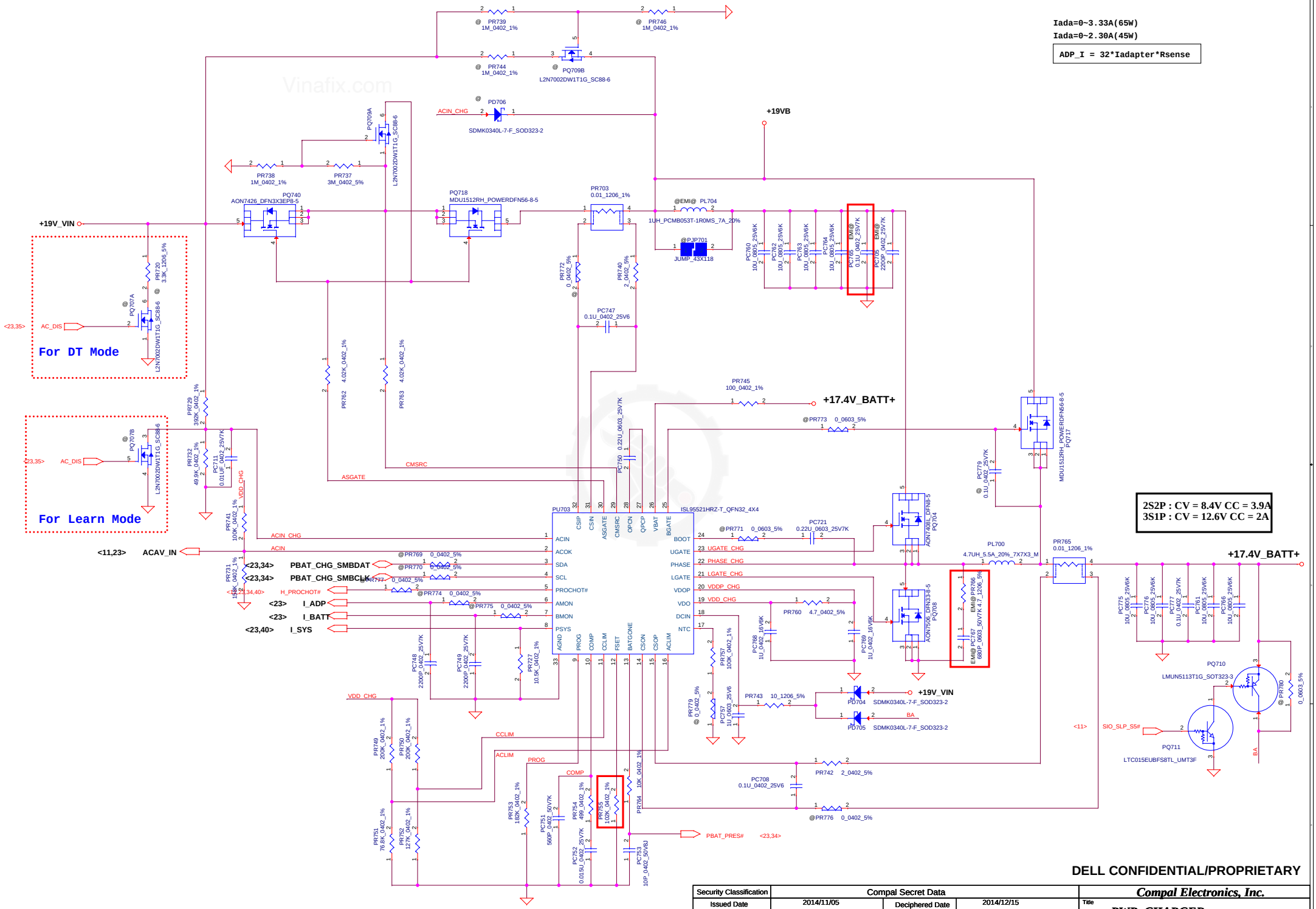
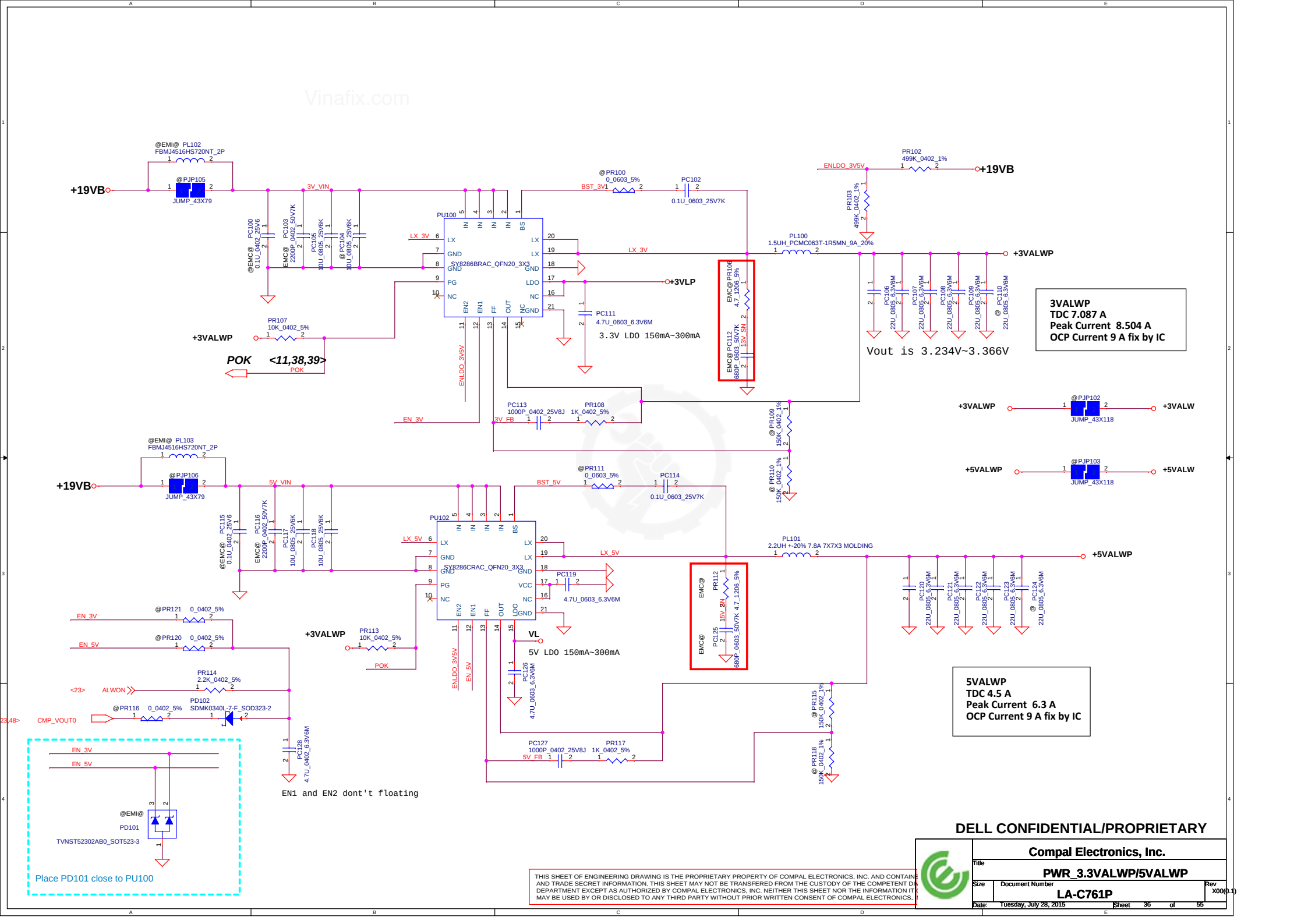
Compal Electronics, Inc.

Title: **PWR_DCIN/BATT CONN/OTP**

Size | Document Number | Rev X00(0.1)

Date: Tuesday, July 28, 2015 | Sheet 34 of 55


Iada=0~3.33A(65W)
Iada=0~2.30A(45W)
ADP_I = 32*Iadapter*Rsense
+19VB
+19V_VIN
+17.4V_BATT+
For DT Mode
For Learn Mode
2S2P : CV = 8.4V CC = 3.9A
3S1P : CV = 12.6V CC = 2A
ACAV_IN
PBAT_CHG_SMBDAT
PBAT_CHG_SMBCLK
H_PROCHOT#
I_ADP
I_BATT
I_SYS
PBAT_PRES#
ISL95521HRZ-T_QFN32_4X4
L2N7002DW1T1G_SC88-6
AON7426_DFN3X3EP8-5
MDU1512RH_POWERDFN56-8-5
AON7506_DFN33-8-5
AON7408L_DFN8-5
LMUN5113T1G_SOT323-3
LTC015EUBFS8TL_UMT3F
SDMK0340L-7-F_SOD323-2
1UH_PCMB053T-1R0MS_7A_20%
4.7UH_5.5A_20%_7X7X3_M
JUMP_43X118
DELL CONFIDENTIAL/PROPRIETARY
Compal Secret Data
2014/11/05
2014/12/15
Compal Electronics, Inc.
PWR_CHARGER
Tuesday, July 28, 2015
Sheet 35 of 55



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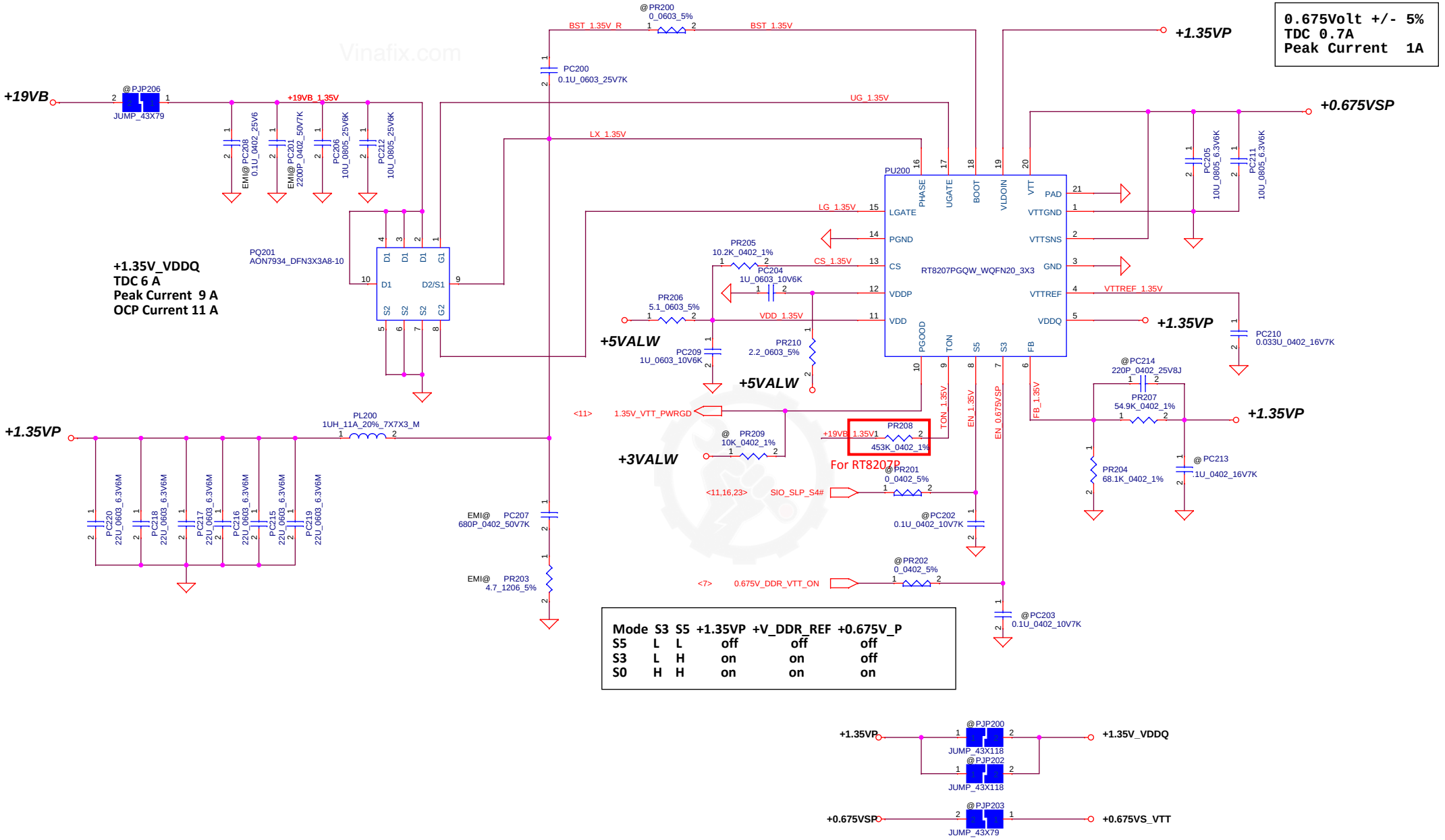
Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-C761P | Rev: X00(0.1)

Date: Tuesday, July 28, 2015 | Sheet 36 of 55


0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A
+19VB
+1.35VP
+0.675VSP
+1.35V_VDDQ
TDC 6 A
Peak Current 9 A
OCP Current 11 A
+5VALW
+3VALW
PU200
RT8207PGQW_WQFN20_3X3
For RT8207P
PQ201
AON7934_DFN3X3A8-10
PL200
1UH_11A_20%_7X7X3_M
Mode S3 S5 +1.35VP +V_DDR_REF +0.675V_P
S5 L L off off off
S3 L H on on off
S0 H H on on on
+1.35VP
+1.35V_VDDQ
+0.675VSP
+0.675VS_VTT
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Security Classification
Compal Secret Data
Issued Date
2014/11/05
Deciphered Date
2014/12/15
PWR_+1.35V_VDDQ/+0.675VS_VTT
Document Number
Rev X00(0.1)
Tuesday, July 28, 2015
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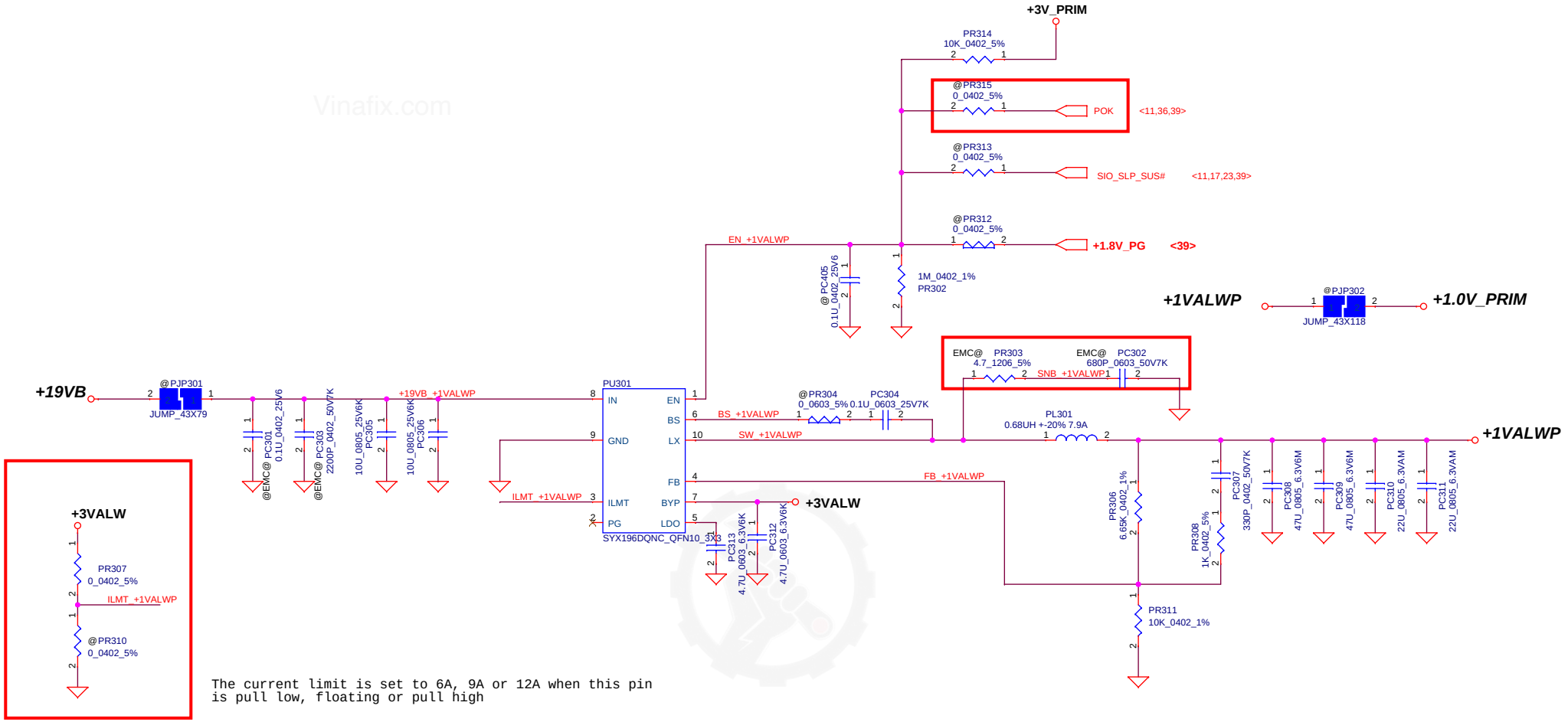

+1.0V_PRIM
TDC 6.5 A
Peak Current 9.3 A
OCP Current 12 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm , 12.0mohm	

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Title	***PWR_+1VALWP***		
Size: Custom	Document Number		Rev X00(0.1)
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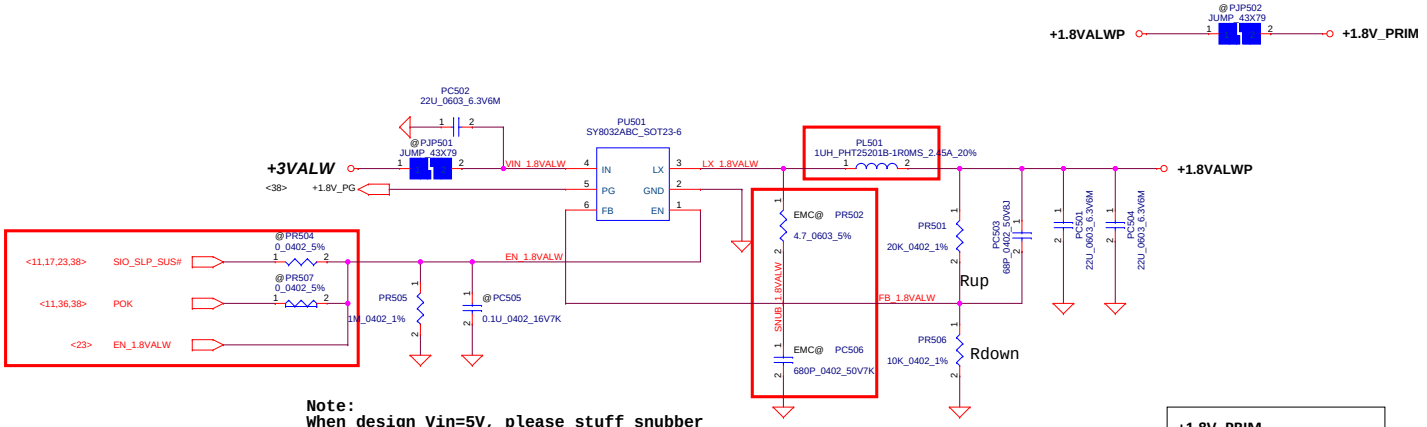
TDC = 0.76A
Prak current : 1.096A
OCP : 3A
FB=0.6V



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

+1.8V_PRIM
TDC 0.66 A
Peak Current 0.95 A
OCP Current 3.5A fix by IC

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1.8V_PRIM

Size: C | Document Number | Rev: X00(0.1)

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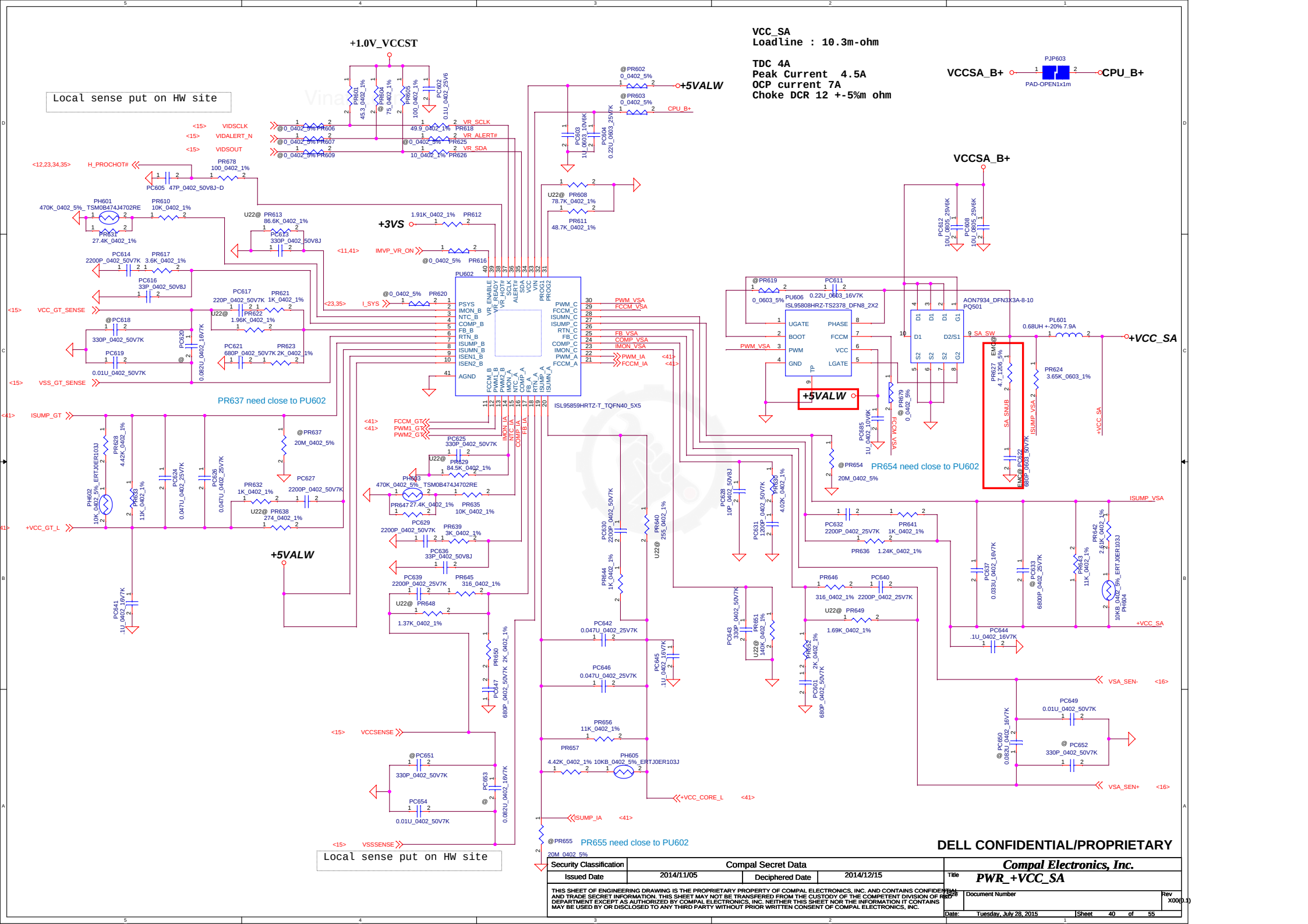
VCC_SA
Loadline : 10.3m-ohm
TDC 4A
Peak Current 4.5A
OCP current 7A
Choke DCR 12 +-5%m ohm
VCCSA_B+
PJP603
PAD-OPEN1x1m
CPU_B+
+1.0V_VCCST
Local sense put on HW site
+5VALW
+3VS
VCCSA_B+
PU602
ISL95859HRTZ-T_TQFN40_5X5
PU606
ISL95808HRZ-TS2378_DFN8_2X2
PU501
AON7934_DFN3X3A-8-10
PQ501
PL601
0.68UH +-20% 7.9A
+VCC_SA
PR637 need close to PU602
PR654 need close to PU602
PR655 need close to PU602
Local sense put on HW site
VCCSENSE
VSSSENSE
VSA_SEN-
VSA_SEN+
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Compal Secret Data
Issued Date
2014/11/05
Deciphered Date
2014/12/15
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PWR_+VCC_SA
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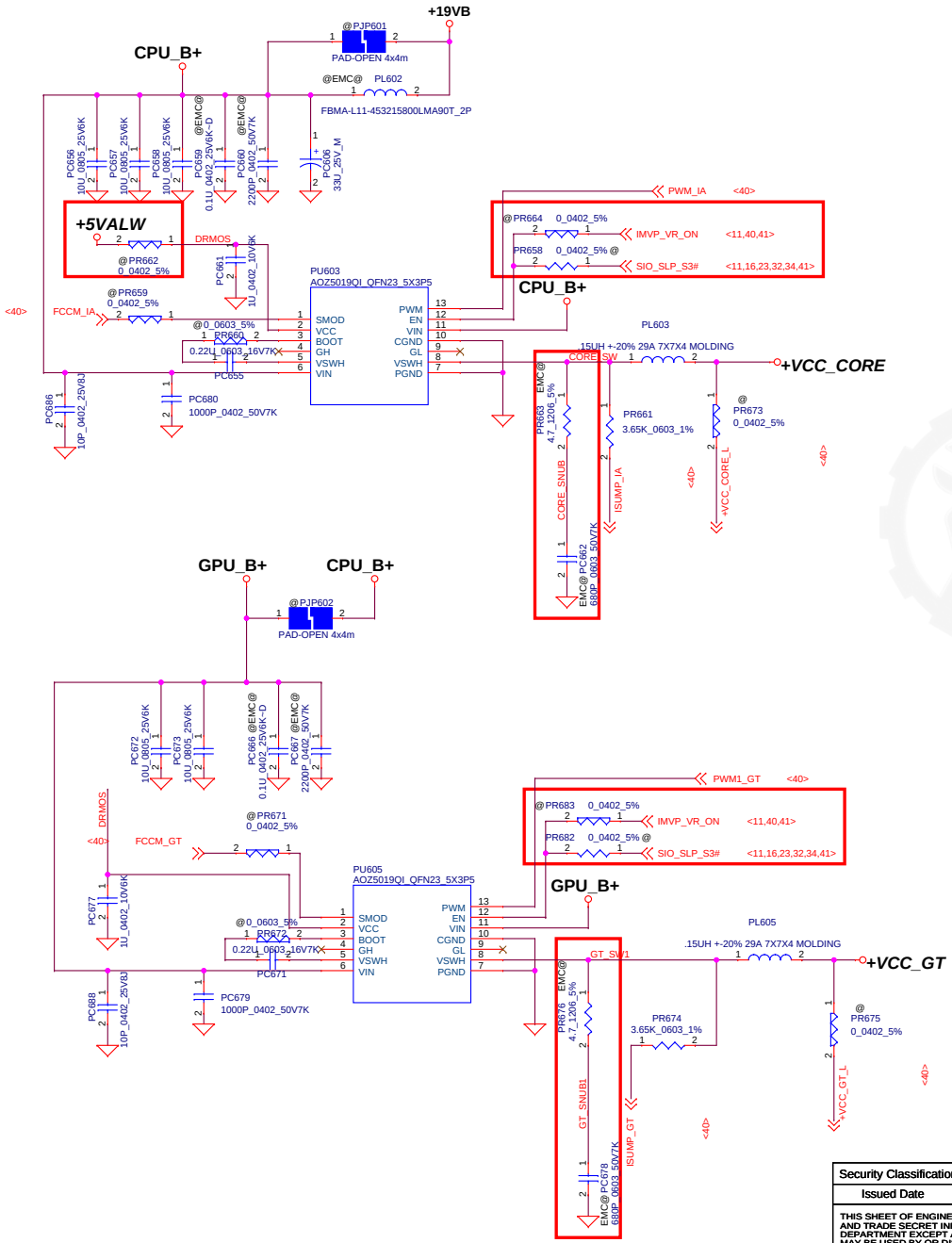
VCC_core
Loadline : 2.4m-ohm
TDC 21A
Peak Current 29A
OCP current 35A
Choke DCR 0.66 +-7%m ohm

VCC_GT
Loadline : 3.1m-ohm
TDC 18A
Peak Current 31A
OCP current 40A
Choke DCR 0.66 +-7%m ohm



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Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

Title: PWR_+VCC_core and +VCC_GT

Size: D | Document Number | Rev: X00(0.1)

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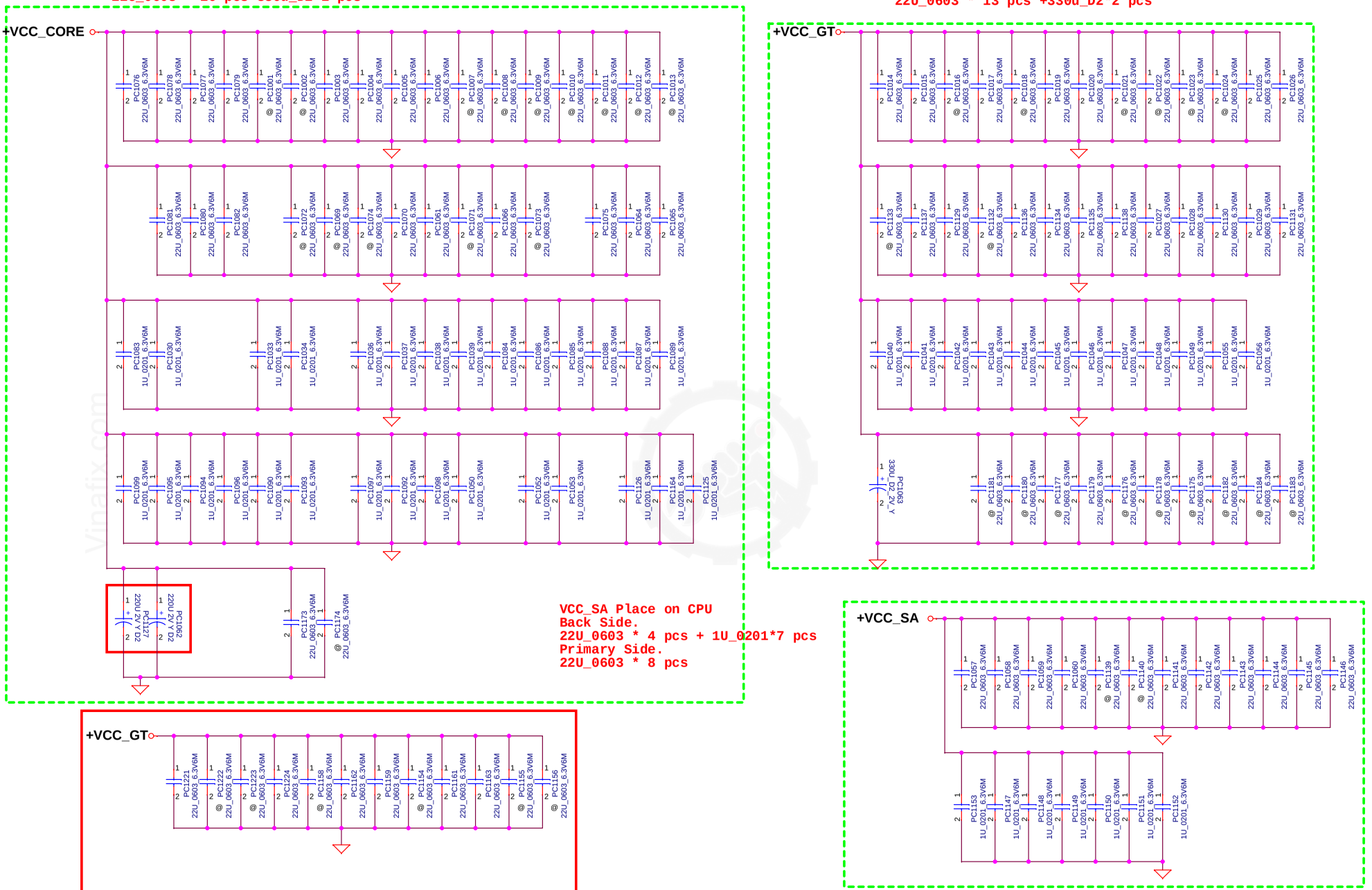
VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+330u_D2*2 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +330u_D2*2 pcs

VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs



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Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_CPU&VGA bulk and MLCC

Size: | Document Number: | Rev: X00(0.1)

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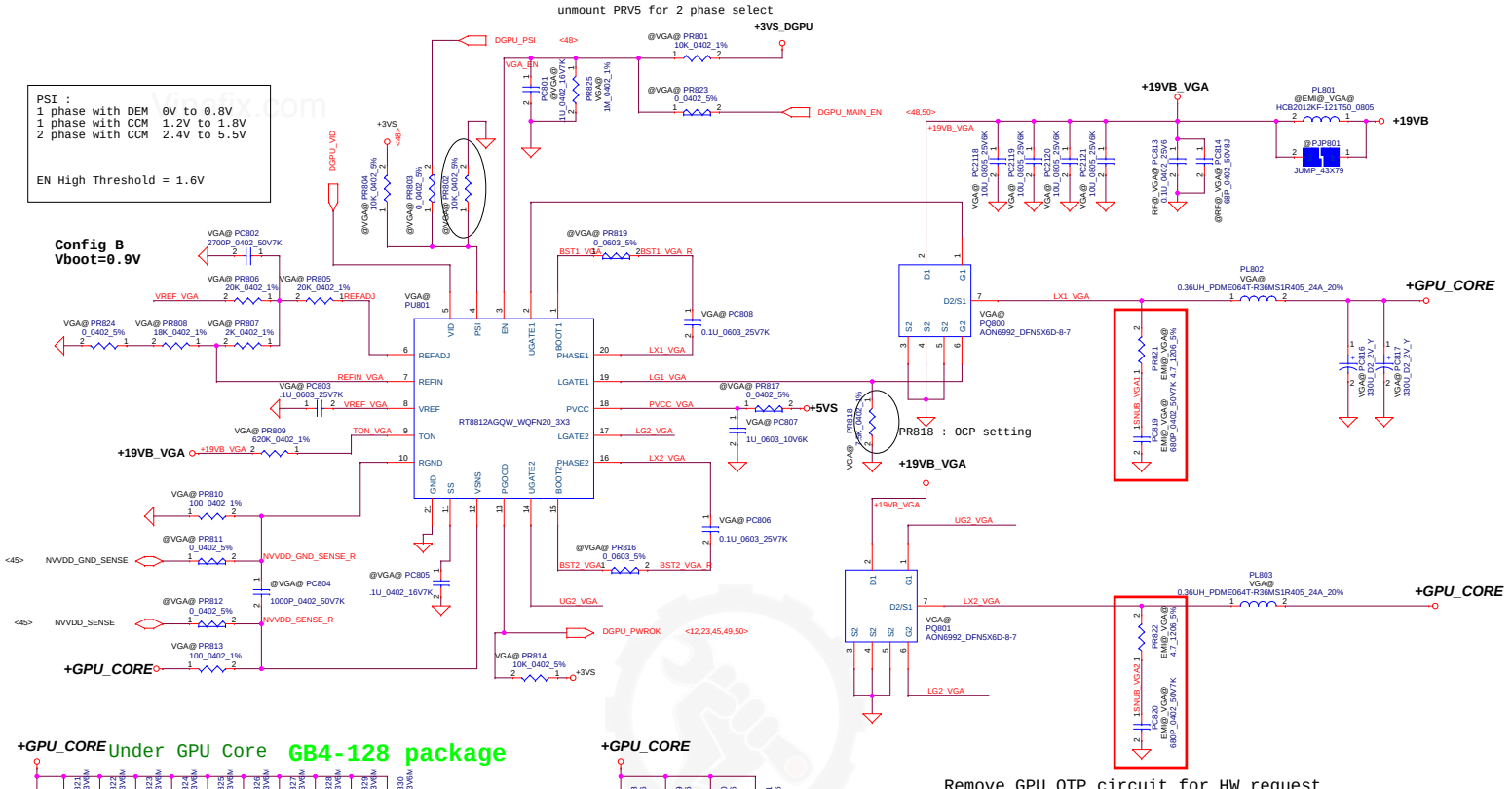

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Issued Date	2014/11/05	Deciphered Date	2014/12/15
Title	PWR_VGA_CORE		
Size: Custom	Document Number		Rev: X00(0.1)
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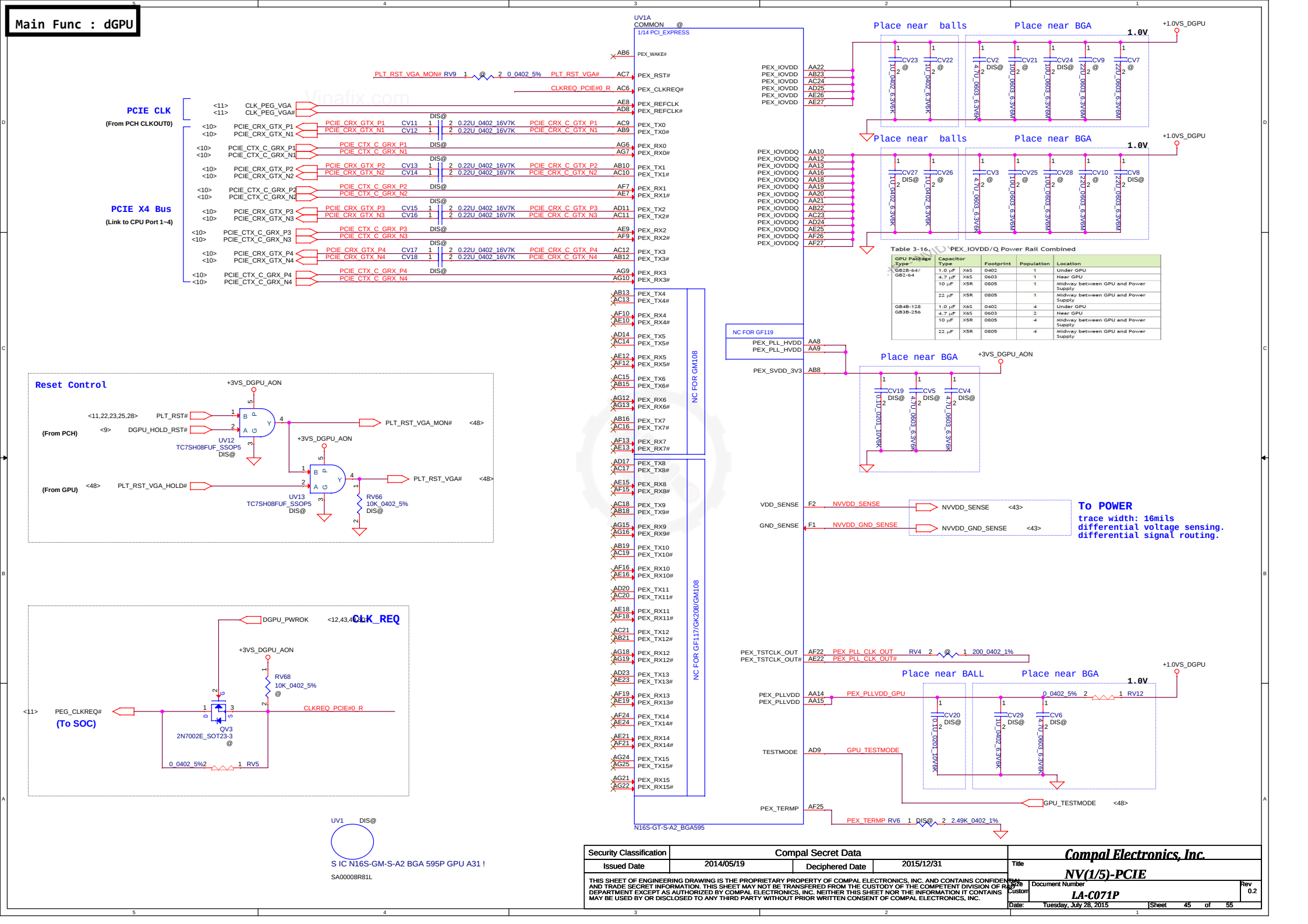
Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	38	PWR	2015/04/27	COMPAL	reserve from EE request	add PR315 and net to POK	0.2
2	39	PWR	2015/04/27	COMPAL	reserve from EE request	add PR507 and net to POK	0.2
3	40	PWR	2015/04/27	COMPAL	add from RF request	pop PR627 and PC622	0.2
4	40	PWR	2015/04/27	COMPAL	abnormal shutdown when enter S3	change PU606.12 from +5VS to +5VALW	0.2
5	41	PWR	2015/04/27	COMPAL	abnormal shutdown when enter S3	change PU603.2 and PU605.2 net from +5VS to +5VALW change PU603.12 and PU605.12 net from +5VS to IMVP_VR_ON	0.2
6	39	PWR	2015/06/09	COMPAL	change from EE request	swap resister from PR504 to PR507	0.3
7	35	PWR	2015/06/09	COMPAL	change from EMI request	change PC2,PC4 from 100p to 0.1u	0.3
8	36	PWR	2015/06/09	COMPAL	change from EMI request	add PC765	0.3
9	34	PWR	2015/07/14	COMPAL	revise S5 power consumption issue	delete PQ1,PR2,PR5,PR7,PR10	
10				COMPAL			

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/11/05	Deciphered Date 2014/12/15	Title: PWR_Change list
			Size / Document Number / Rev: X00(0.1)
			Date: Tuesday, July 28, 2015 Sheet 44 of 55

Main Func : dGPU



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: NV(1/5)-PCIE

Size: Custom | Document Number: LA-C071P | Rev: 0.2

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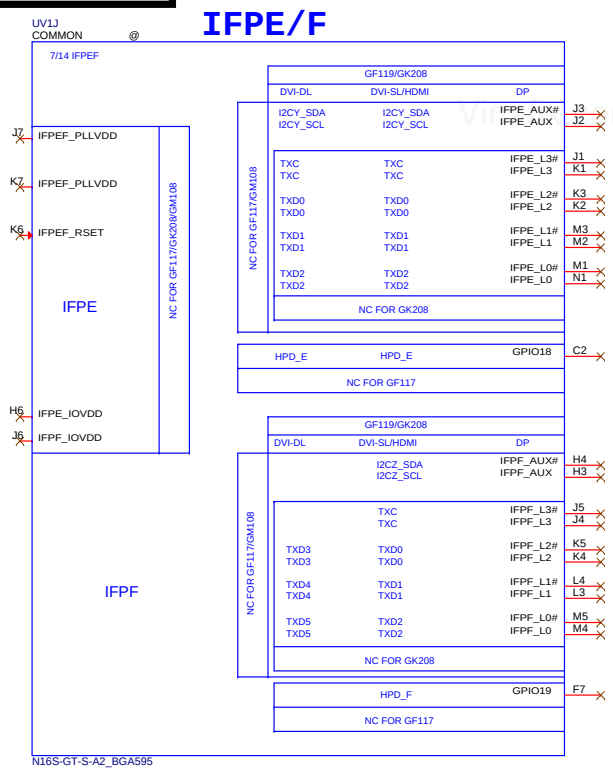
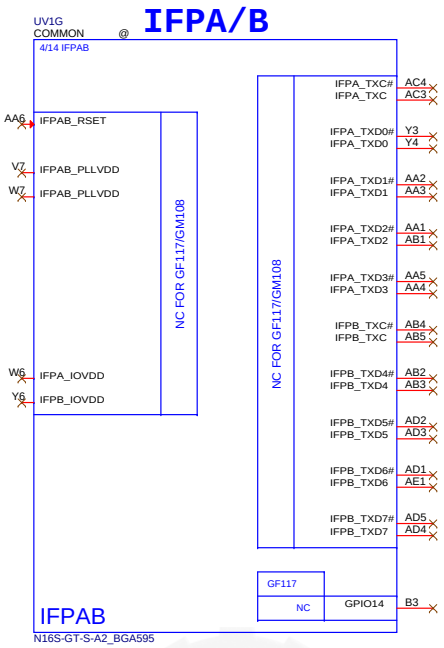
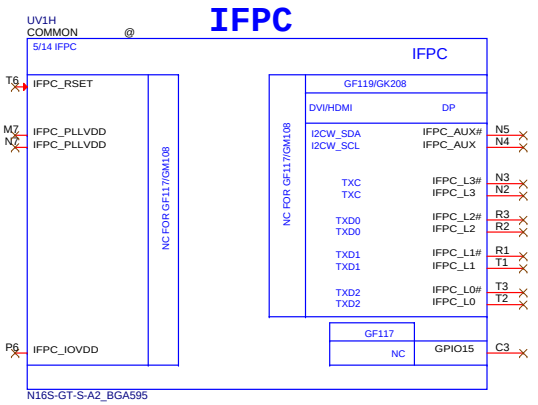
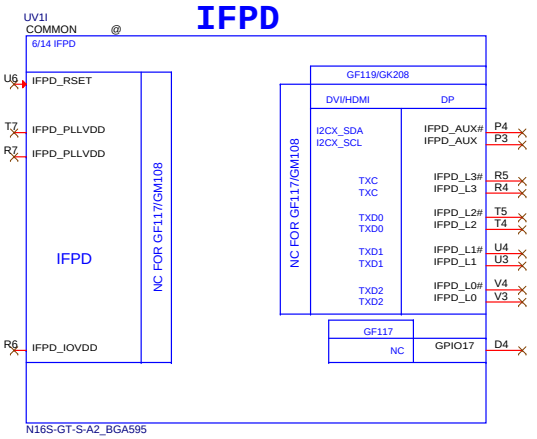
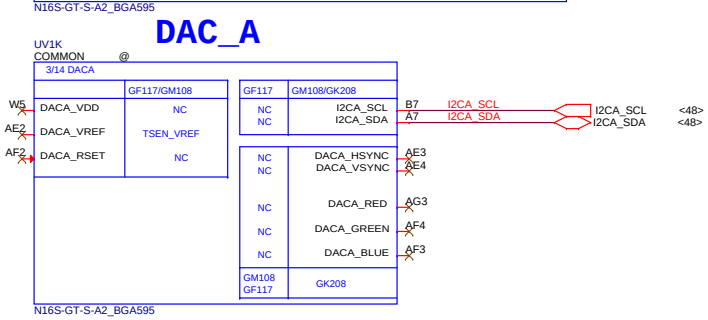
Main Func : dGPU

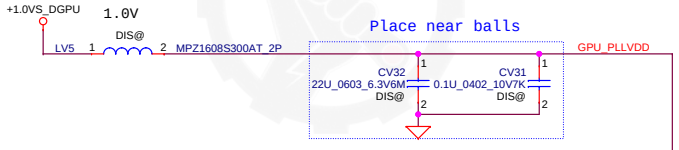


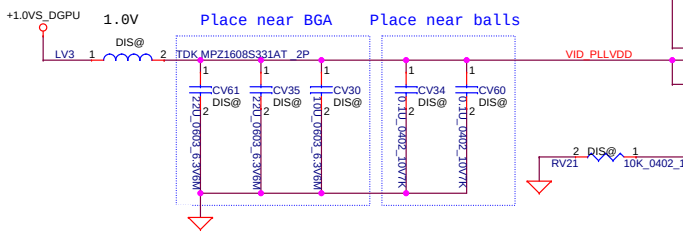












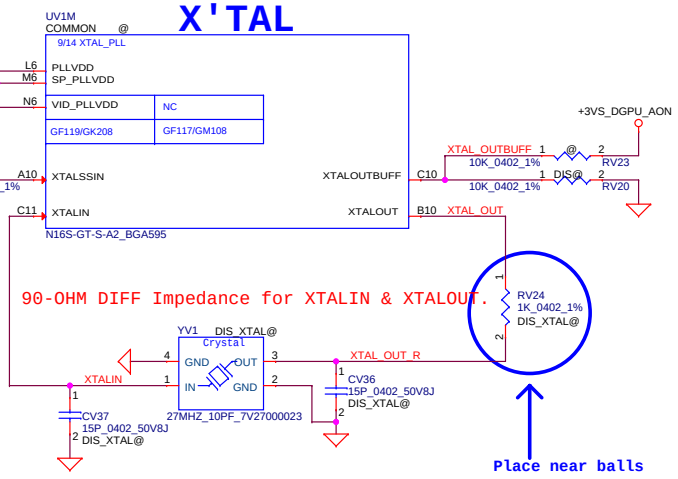


Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:

1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

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Title	NV(2/5)-IFP ABCDEF DAC XTAL
Size: Custom	Document Number: LA-C071P
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Date: Tuesday, July 28, 2015	Sheet 46 of 55

Main Func : dGPU

GPU_Decoupling CAPs @ Power Page

+1.35VS_VRAM

Place under GPU

CV40 DIS@ 4.7U_0603_6.3V6K
CV38 DIS@ 4.7U_0603_6.3V6K
CV41 DIS@ 10U_0402_6.3V6K
CV42 DIS@ 0.1U_0201_10V6K
CV39 DIS@ 0.1U_0201_10V6K
CV43 DIS@ 0.1U_0201_10V6K

Place near GPU

CV45 DIS@ 22U_0603_6.3V6M
CV44 DIS@ 100U_0603_6.3V6M

UV1D
COMMON @
12/14 FBVDDQ

B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 L22 L24 L26 M21 N21 R21 T21 V21 W21 — FBVDDQ

H24 H26 J21 K21 — FBVDDQ_AON

GF117 GF119 GK208: FBVDDQ_AON → FBVDDQ

N16S-GT-S-A2_BGA595

+1.35VS_VRAM

Near Ball

FB_CAL_PD_VDDQ — D22 40.2_0402_1% 1 DIS@ 2 RV41
FB_CAL_PU_GND — C24 42.2_0402_1% 2 DIS@ 1 RV42
FB_CALTERM_GND — B25 51.1_0402_1% 2 DIS@ 1 RV43

+GPU_CORE

Voltage by GPU SKU

UV1E
COMMON @
11/14 NVVDD

K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18 — VDD

N16S-GT-S-A2_BGA595

UV1F
COMMON @
13/14 GND

A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E9 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11 — GND

GND M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 — GND

GND AA7 GND AB7 — GND

N16S-GT-S-A2_BGA595

UV1C
COMMON @
14/14 XVDD/VDD33

AD10 NC
AD7 NC
GM108: 3V3_AON 3V3_AON
F11 3V3AUX_NC
V5 FERMI_RSVD1_NC
V6 FERMI_RSVD2_NC

G8 G9 G10 G12 — VDD33

CONFIGURABLE POWER CHANNELS
* nc on substrate

G1 XPWR_G1
G2 XPWR_G2
G3 XPWR_G3
G4 XPWR_G4
G5 XPWR_G5
G6 XPWR_G6
G7 XPWR_G7
V1 XPWR_V1
V2 XPWR_V2
W1 XPWR_W1
W2 XPWR_W2
W3 XPWR_W3
W4 XPWR_W4

N16S-GT-S-A2_BGA595

Under GPU / Near GPU

CV69 DIS@ 0.1U_0201_10V6K
CV50 DIS@ 0.1U_0201_10V6K
CV49 DIS@ 10U_0402_6.3V6K
CV48 DIS@ 4.7U_0603_6.3V6K

0_0402_5% 2 1 RV40 — +3VS_DGPU

Under GPU / Near GPU

CV46 DIS@ 0.1U_0201_10V6K
CV47 DIS@ 10U_0402_6.3V6K
CV54 DIS@ 4.7U_0603_6.3V6K

0_0402_5% 2 1 RV58 — +3VS_DGPU_AON

** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: NV(3/5)-POWER

Size: Custom | Document Number: LA-C071P | Rev: 0.2

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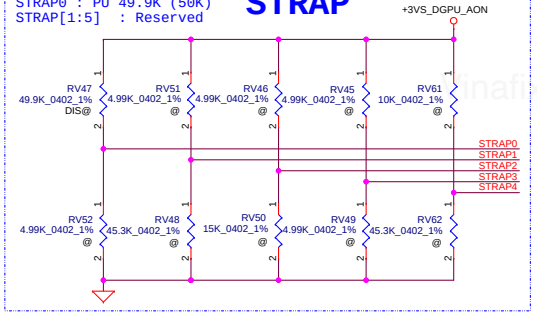
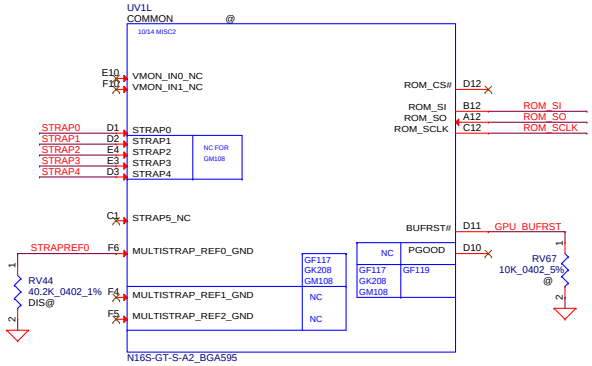
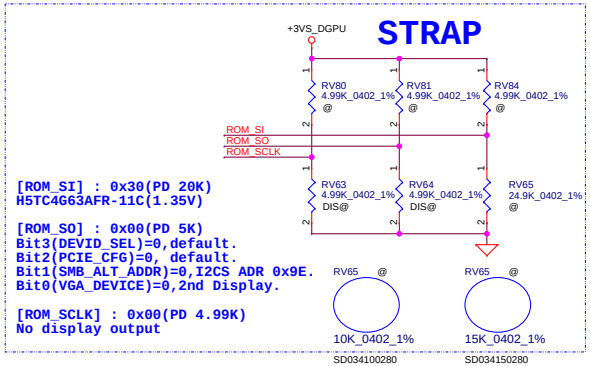
Main Func : dGPU

STRAP

STRAP0 : PU 49.9K (50K)
STRAP[1:5] : Reserved







same Maple_BDW	Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
	Samsung	K4W4G1646E-BC1A	E-die	0x1	900	N/A	Production ready
same Tulip_SKL	Hynix	H5TC4G63CFR-H0C	C-die	0x2	900	N/A	Post production ready

Single Rank or Single Rank Stuffing for Dual Rank

1.35V
1.35V

256Mx16

RAM_CFG[3:0] (ROM_SI)	BAV00
0x4(PD 24.9K)	V (SSI)
0x1(PD 10K)	
0x2(PD 15K)	

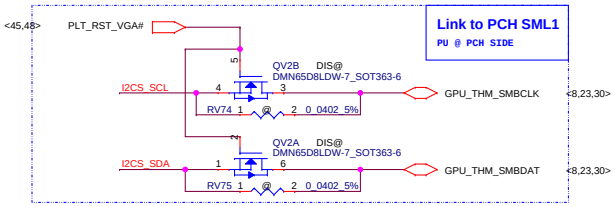
Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

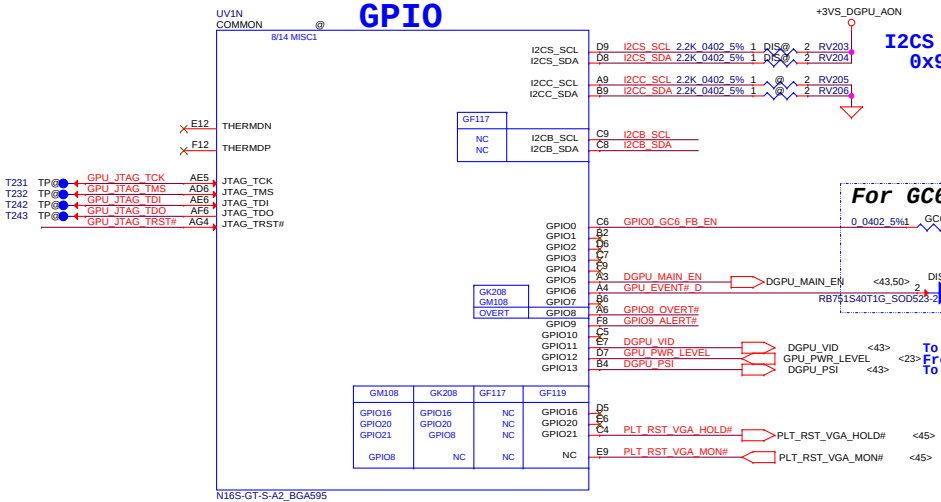
10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful I²CS Slave addresses can be used with SMB_ALT_ADDR strapping.

Internal Thermal Sensor

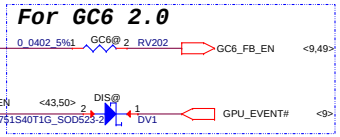


GPIO



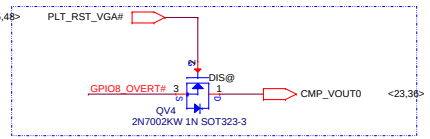
I2CS SMBUS:
0x96 and 0x9E(Default)

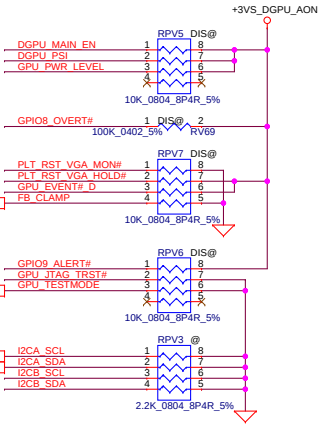
For GC6 2.0



To DGPU VR
From EC
To DGPU VR

Shutdown System when GPU over Temp.





VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

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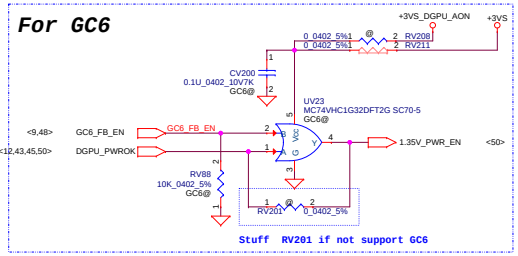
Main Func : dGPU



From DG-07158-001_v03_secured(NVDIA Spec)

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2-64 GB2B-64 GB4B-128	D	Mode D is optimized for N16x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2-64 GB2B-64	E	Mode E is optimized for DDR3 dual rank designs.
Note: 1. Not including two additional layers for power planes.		

Table 6-4. Mode E Command Mapping

	Rank 0		Rank 1	
N16x DDR3 Mode E	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				
FBx_CMD34	DBG0[2]			
FBx_CMD35	DBG1[2]			

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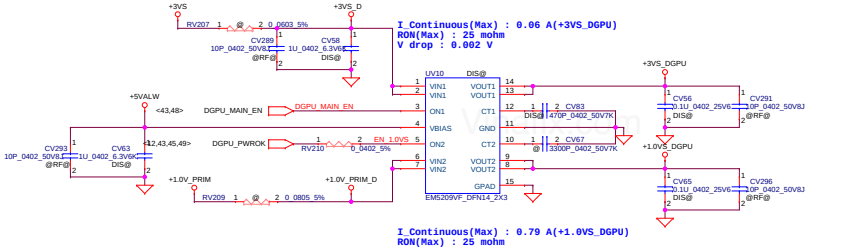
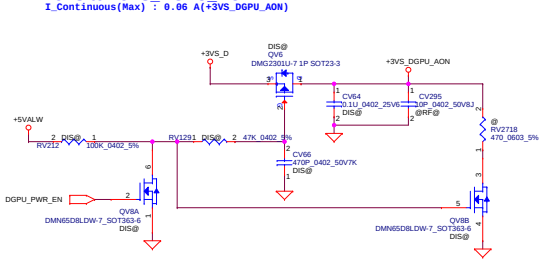




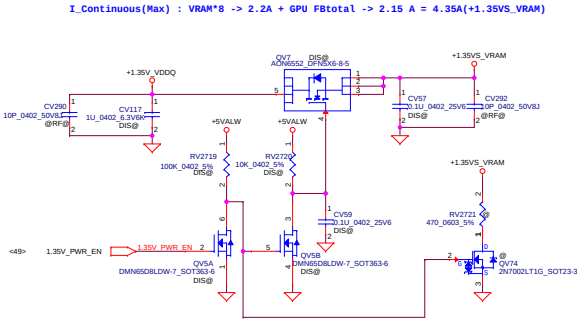


Table 5. EDP-Continuous [3]

Products	VRM Type	GPU Core	GPU FBIO		FB Total [1, 5]		1.05V Total [2]	3.3V Total
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GT	DDR3/L	26	1.37	1.33	2.32	2.12	0.79	0.06
N16S-GM	DDR3/L	20	1.37	1.31	2.32	2.05	0.79	0.06
N16S-LP	DDR3L	16	N/A	1.29	N/A	2.05	0.79	0.06

Table 3-15. PCI Express Power Rails Specification

GPU Package	Power Rails	Voltage	Transient Noise
GB2-64/ GB2B-64	PEX_IOVDD/Q and	1.05 V ± 30 mV or	100 mV pk-pk within 20 MHz (1.05V) or
	PEX_PLLVDD	1.0 V ± 15mV	70 mV pk-pk within 20 MHz (1.0V)

Table 3-7. Power Rail Specification for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V (DDR3) or 1.35V (DDR3L)
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW
	High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW

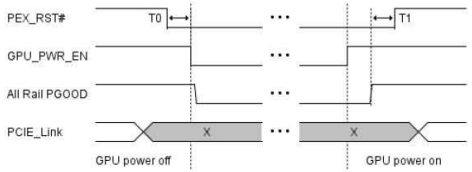


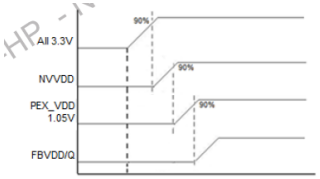
Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Chapter 3

- Added 1.0V support to PEX_VDD and all 1.05V Power Rails



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.

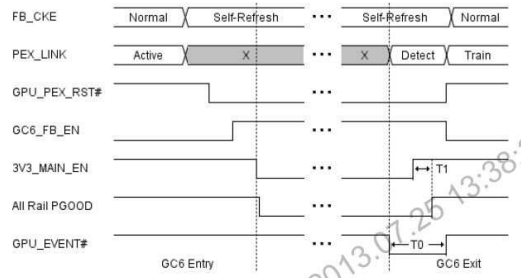
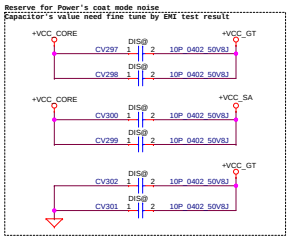


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

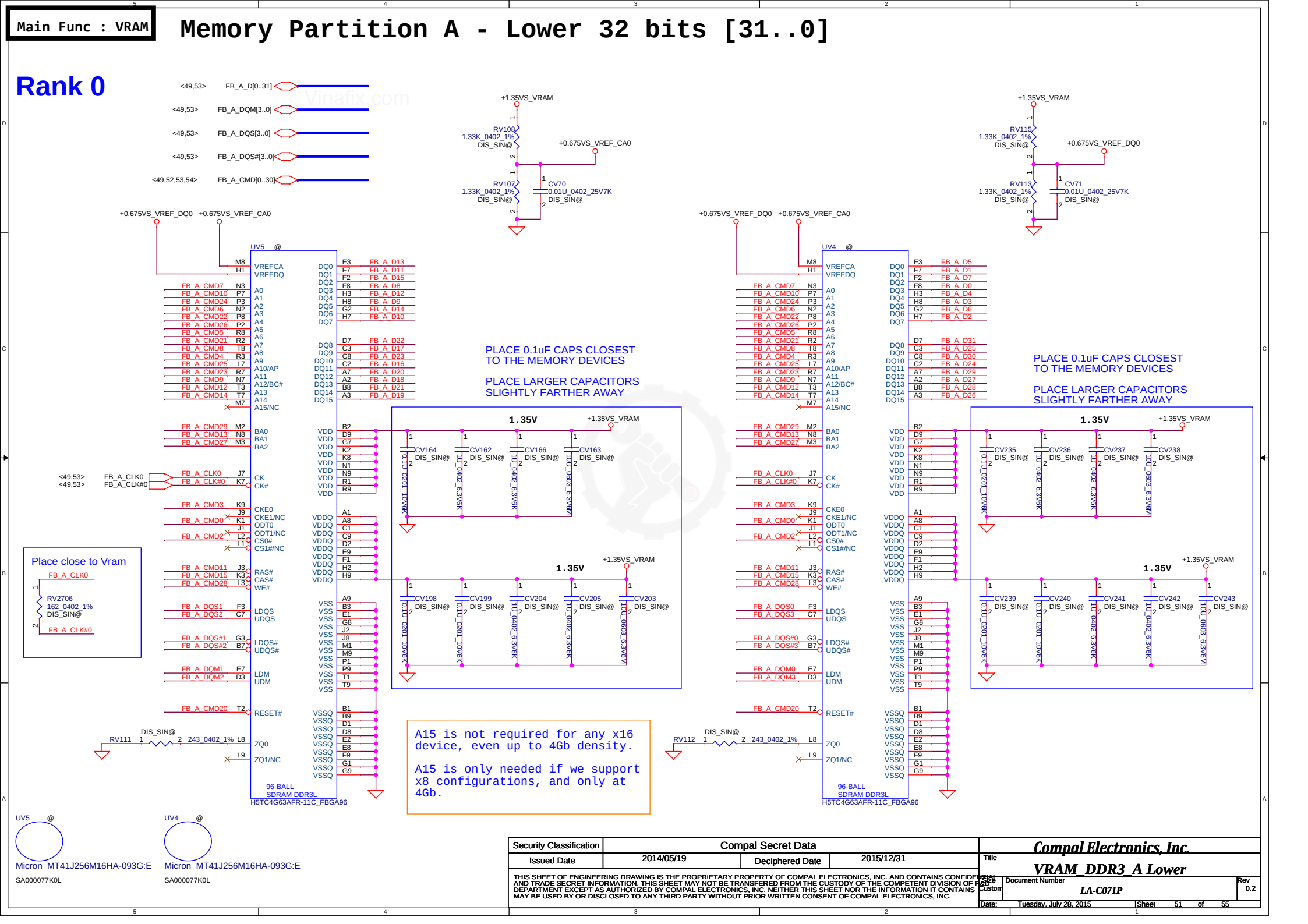
Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms



Main Func : VRAM

Memory Partition A - Lower 32 bits [31..0]

Rank 0



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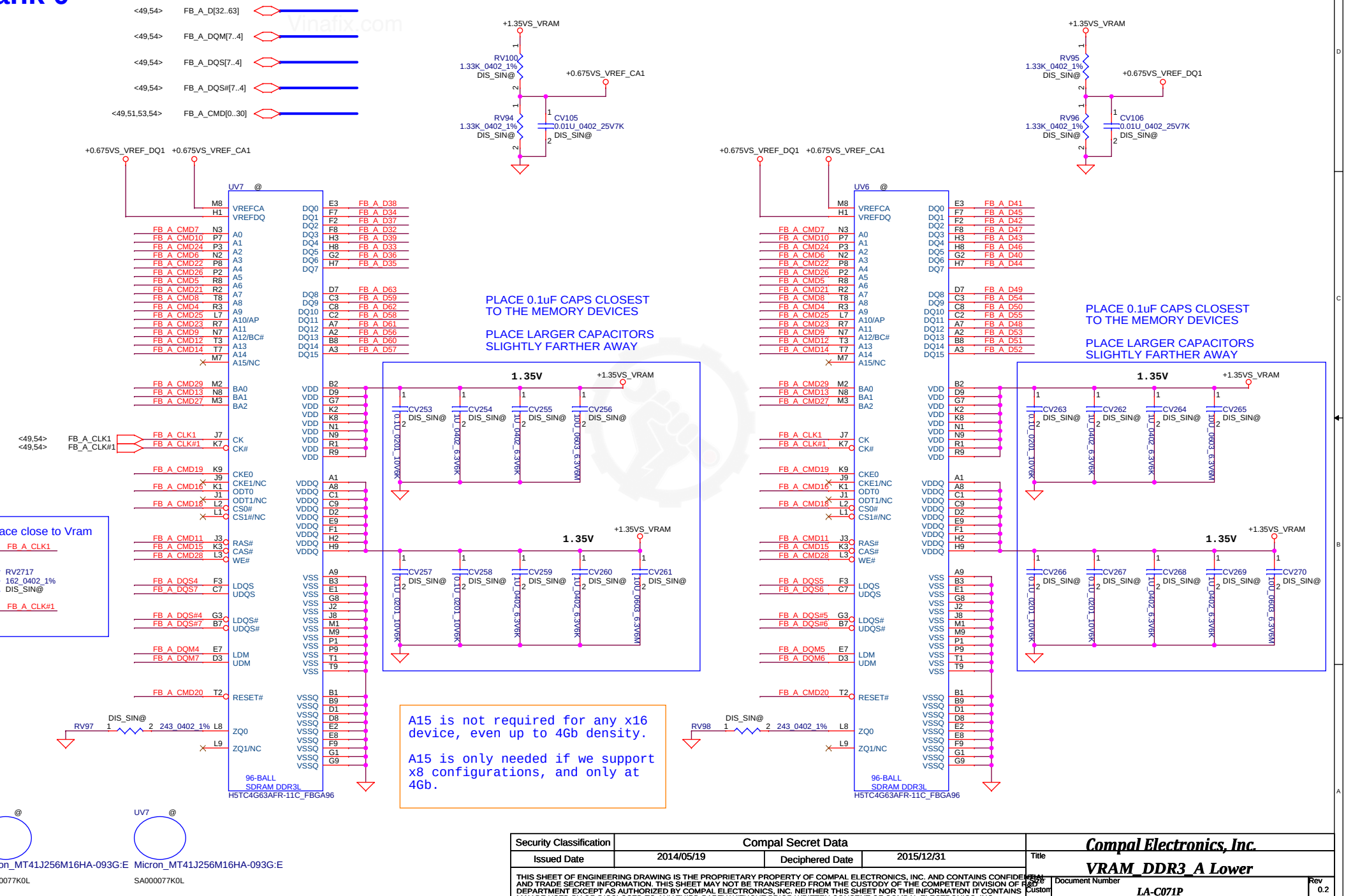
Main Func : VRAM

Memory Partition A - Upper 32 bits [63..32]

Rank 0



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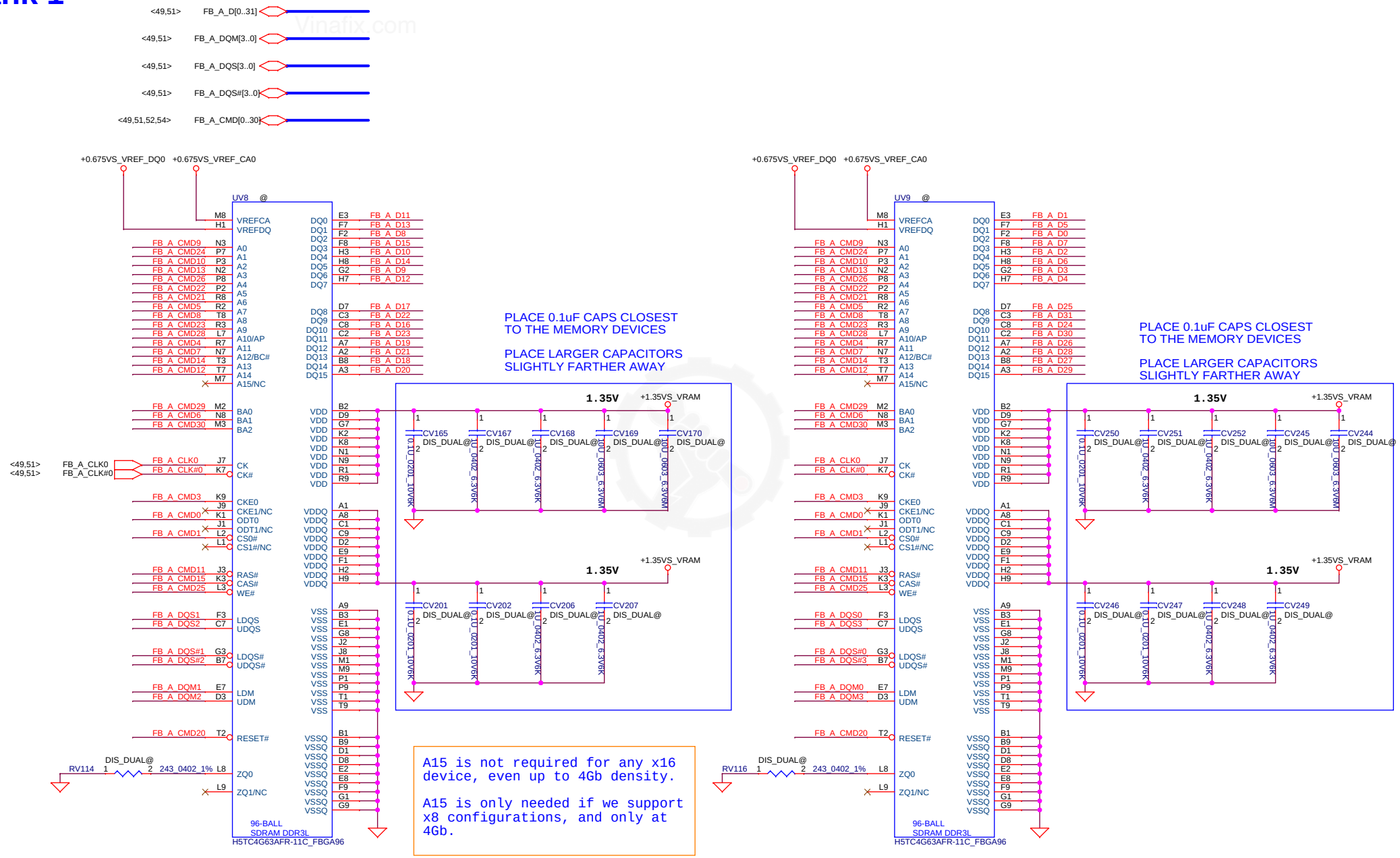
Main Func : VRAM

Memory Partition A - Lower 32 bits [31..0]

Rank 1



UV8 @ Micron_MT41J256M16HA-093G:E SA000077K0L

UV9 @ Micron_MT41J256M16HA-093G:E SA000077K0L

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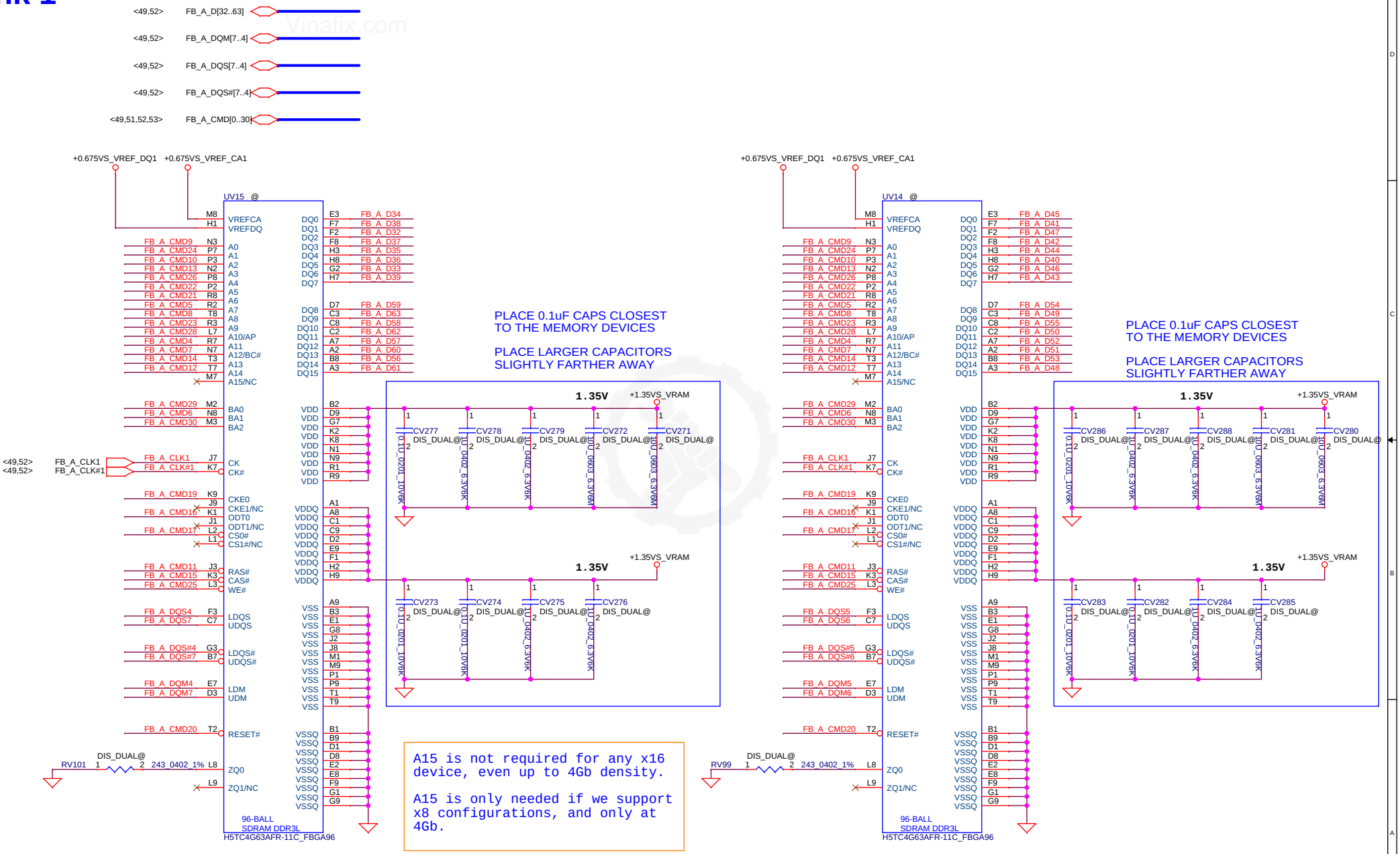
Main Func : VRAM

Memory Partition A - Upper 32 bits [63..32]

Rank 1



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