MODEL NAME : ZAP00
PROJECT CODE : ANRZAP0000
PCB NO : DA8000WL000 LA-A301P M/B
DA4001XN000 LS-A301P LOGO/B
DA4001XO000 LS-A302P IND/B
DA4001XP000 LS-A303P BTN/B
DA4001XQ000 LS-A304P NGFF/B
FPC NO : LF-A301P HEAD/B
LF-A302P SLIT_R/B
LF-A303P SLIT_L/B
LF-A304P KB/B

Compal Confidential
Schematic Document

Crescent Bay Platform
Intel Broadwell ULT
2014-09-23 Rev: 1.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
@ESD@ : Reserve ESD parts
RF@ : RF parts
BDWI5@ : CPU BDW I5
H@:Haswell
B@:Broadwell

DAX
PCB
DAZ16C00100
R1@

DAX
PCB
DAZ16C00101
R3@

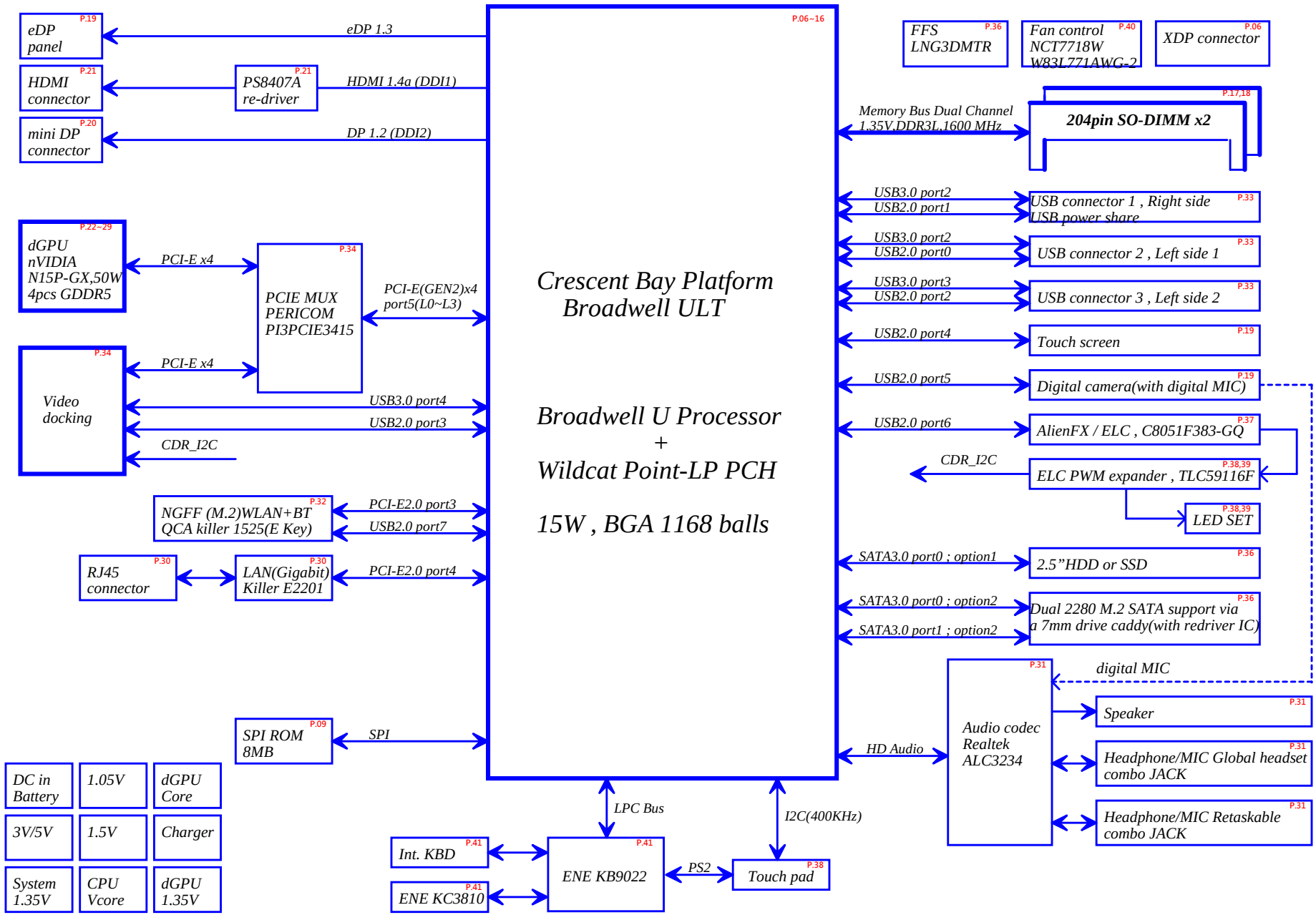
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: Cover page

Size: Custom | Document Number: LA-A301P | Rev: 1.0

Date: Thursday, September 25, 2014 | Sheet 1 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **Block diagram**

Size	Document Number	Rev
	LA-A301P	1.0

Date: Friday, September 19, 2014 Sheet 2 of 56

Board ID Table for AD channel

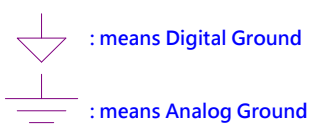
Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	NVIDIA Graphic
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	AMD Graphic
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF	

Board ID table and PCB version

ID	Rb	HSW(Haswell)	BDW(Broadwell)
0	0	EVT-1(R0.1) , EVT-2(R0.1)	EVT-1(R0.1)
1	12K	EVT-3(R0.2)	EVT-2(R0.2)
2	15K	DVT-1(R0.3) , DVT1.1(R0.4)	DVT-1(R0.5)
3	20K	DVT-2(R0.5)	Not use
4	27K	Not use	DVT-1.1(N16P,R0.6)
5	33K	Not use	DVT-2(R1.0)
6	43K	Pilot(R1.0)	Pilot(R1.0)

Symbol Note :



CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	M.2 Card WLAN
CLKOUT_PCIE3	10/100/1000 LAN
CLKOUT_PCIE4	N15P-GX , Video docking
CLKOUT_PCIE5	

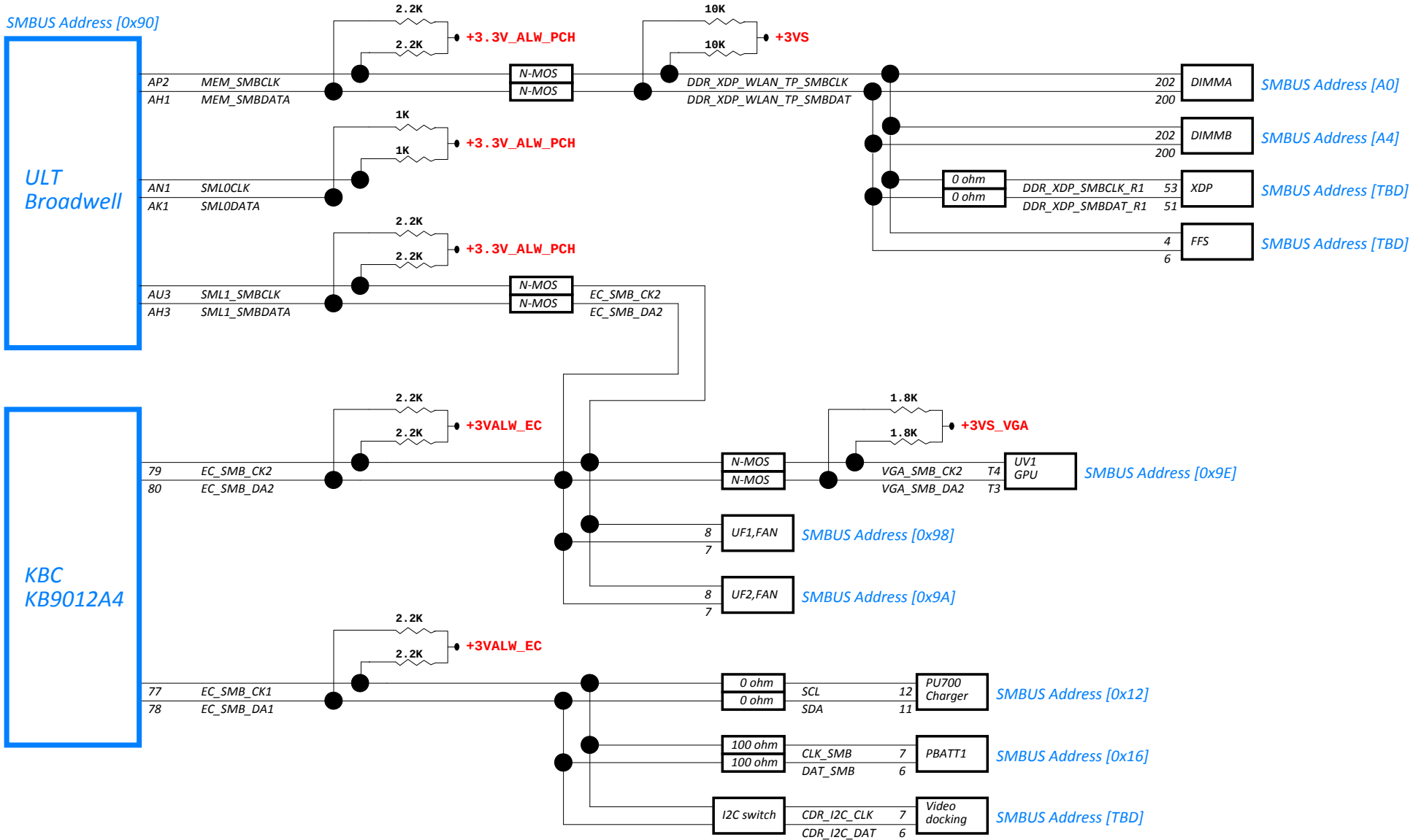
ULT		
	USB3.0	
	Port1	Left side 1
	Port2	Right side (power share)
	Port3	Left side 2
	Port4	Caldera
	USB2.0	
	Port0	Left side 1
	Port1	Right side (power share)
	Port2	Left side 2
	Port3	Caldera
	Port4	Touch screen
	Port5	Camera
	Port6	ELC
	Port7	BT
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	WLAN(M.2 Card)
	Lane 4	10/100/1000 LAN
	Lane 5	PCIE 4x MUX
	Lane 6	
	SATA	
	SATA0	HDD or NGFF SSD1
	SATA1	NGFF SSD2
	SATA2	
	SATA3	

Compal Electronics, Inc.

Title: Notes list

Size | Document Number: LA-A301P | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 4 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **SMBus block diagram**

Size: B | Document Number: **LA-A301P** | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 5 of 56

UC1

S IC CL8064701477802 SR1EF D0 1.7G A31
SA00007LO2L
R1HSW15@

UC1

IS IC A31 FH8065801620203 QH17 E0 2G
SA00008991L
R1BDW15@

UC1

S IC A31 FH8065801620004 QH3E F0 2.4G
SA000089A1L
R1BDW17@

UC1

S IC CL8064701477802 SR1EF D0 1.7G A31
SA00007LO1L
R3HSW15@

UC1

IS IC A31 FH8065801620203 QH17 E0 2G
SA00008992L
R3BDW15@

UC1

S IC A31 FH8065801620004 QH3E F0 2.4G
SA000089A2L
R3BDW17@

HDMI

mini DP

UC1A — HASWELL_MCP_E — DDI — EDP — 1 OF 19 — Rev1p2

<21> DDI1_LANE_N0	DDI1_LANE_N0	C54	DDI1_TXN0		
<21> DDI1_LANE_P0	DDI1_LANE_P0	C55	DDI1_TXP0		
<21> DDI1_LANE_N1	DDI1_LANE_N1	B58	DDI1_TXN1		
<21> DDI1_LANE_P1	DDI1_LANE_P1	C58	DDI1_TXP1		
<21> DDI1_LANE_N2	DDI1_LANE_N2	B55	DDI1_TXN2		
<21> DDI1_LANE_P2	DDI1_LANE_P2	A55	DDI1_TXP2		
<21> DDI1_LANE_N3	DDI1_LANE_N3	A57	DDI1_TXN3		
<21> DDI1_LANE_P3	DDI1_LANE_P3	B57	DDI1_TXP3		
<20> DDI2_LANE_N0	DDI2_LANE_N0	C51	DDI2_TXN0		
<20> DDI2_LANE_P0	DDI2_LANE_P0	C50	DDI2_TXP0		
<20> DDI2_LANE_N1	DDI2_LANE_N1	C53	DDI2_TXN1		
<20> DDI2_LANE_P1	DDI2_LANE_P1	B54	DDI2_TXP1		
<20> DDI2_LANE_N2	DDI2_LANE_N2	C49	DDI2_TXN2		
<20> DDI2_LANE_P2	DDI2_LANE_P2	B50	DDI2_TXP2		
<20> DDI2_LANE_N3	DDI2_LANE_N3	A53	DDI2_TXN3		
<20> DDI2_LANE_P3	DDI2_LANE_P3	B53	DDI2_TXP3		

EDP_TXN0	C45	EDP_TX0#	<19>
EDP_TXP0	B46	EDP_TX0	<19>
EDP_TXN1	A47	EDP_TX1#	<19>
EDP_TXP1	B47	EDP_TX1	<19>
EDP_TXN2	C47	EDP_TX2#	<19>
EDP_TXP2	C46	EDP_TX2	<19>
EDP_TXN3	A49	EDP_TX3#	<19>
EDP_TXP3	B49	EDP_TX3	<19>
EDP_AUXN	A45	EDP_AUX#	<19>
EDP_AUXP	B45	EDP_AUX	<19>
EDP_RCOMP	D20	EDP_COMP	
EDP_DISP_UTIL	A43	EDP_DISP_UTIL	

EDP_BIA_PWM <10,19> — RC1 0_0402_5%

+VCCIOA_OUT — RC2 24.9_0402_1%~D

COMPENSATION PU FOR eDP
CAD Note:
Trace width=20mils
Spacing=25mils
Max length=100mils

+3VS — CC1 0.1U_0402_10V7K

UC3 — 74CBTLV3126BQ_DHVQFN14_2P5X3

<8> PCH_JTAG_TDO	PCH_JTAG_TDO	RC3 0_0402_1%	TDO_XDP
<8> PCH_JTAG_TDI	TDI_XDP	RC4 0_0402_1%	TDI_XDP_R
<8> PCH_JTAG_TMS	TMS_XDP	RC5 0_0402_1%	
	TRST#_XDP	RC6 0_0402_1%	
<41> RUNPWROK	RUNPWROK		

VCC	14		
1A	2	1B	3 XDP_TDO
1OE	1		
2A	5	2B	6 XDP_TDI
2OE	4		
3A	9	3B	8 XDP_TMS
3OE	10		
4A	12	4B	11 XDP_TRST#
4OE	13	GND	7
		GND PAD	15

RUNPWROK — @ESD@ CC5 0.1U_0402_10V7K

Place CC5 close to UC4

+1.05VS — XDP_DBRESET# — RC22 0_0402_1% — SYS_RESET# <10>

+3VALW_PCH — RC21 1K_0402_5% — SYS_PWROK_XDP — @ESD@ CC7 0.1U_0402_10V7K

Place near JXDP pin47

+1.05VS — RC16 49.9_0402_1% H_CATERR# — RC18 62_0402_5% H_PROCHOT#

PCH_JTAG_RST#	RC17 0_0402_1%	XDP_TRST#	
<8> PCH_JTAG_JTAGX	RC19 0_0402_1%	XDP_TCLK	
	RC20 0_0402_5% XDP@	TDO_XDP	
PCH_JTAG_TDO	RC23 0_0402_5% XDP@	TDI_XDP_R	
<8> PCH_JTAG_TCK	PCH_JTAG_TCK RC24 0_0402_5% XDP@	XDP_TCLK	

+1.05VS — JXDP

XDP_PREQ#	3	GND0	1
XDP_PRDY#	5	OBSFN_A0	4
	7	OBSFN_A1	6
	9	GND2	8
<16> CFG0	11	OBSDATA_A0	10
<16> CFG1	13	OBSDATA_A1	12
	15	GND4	14
<16> CFG2	17	OBSDATA_A2	16
<16> CFG3	19	OBSDATA_A3	18
	21	GND6	20
XDP_OBS0_R	23	OBSFN_B0	22
XDP_OBS1_R	25	OBSFN_B1	24
	27	GND8	26
<16> CFG4	29	OBSDATA_B0	28
<16> CFG5	31	OBSDATA_B1	30
	33	GND10	32
<16> CFG6	35	OBSDATA_B2	34
<16> CFG7	37	OBSDATA_B3	36
	39	GND12	38
	41	PWRGOOD/HOOK0	40
	43	HOOK1	42
	45	VCC_OBS_AB	44
	47	HOOK2	46
	49	HOOK3	48
	51	GND14	50
	53	SDA	52
	55	SCL	54
	57	TCK1	56
	59	TCK0	58
		GND16	60

SAMTE_BSH-030-01-L-D-A — CONN@

		GND1	2
		OBSFN_C0	4
		OBSFN_C1	6
		GND3	8
		OBSDATA_C0	10
		OBSDATA_C1	12
		GND5	14
		OBSDATA_C2	16
		OBSDATA_C3	18
		GND7	20
		OBSFN_D0	22
		OBSFN_D1	24
		GND9	26
		OBSDATA_D0	28
		OBSDATA_D1	30
		GND11	32
		OBSDATA_D2	34
		OBSDATA_D3	36
		GND13	38
		ITPCLK/HOOK4	40
		ITPCLK#/HOOK5	42
		VCC_OBS_CD	44
		RESET#/HOOK6	46
		DBR#/HOOK7	48
		GND15	50
		TDO	52
		TRST#	54
		TDI	56
		TMS	58
		GND17	60

CFG17	4	CFG17	<16>
CFG16	6	CFG16	<16>
CFG8	10	CFG8	<16>
CFG9	12	CFG9	<16>
CFG10	16	CFG10	<16>
CFG11	18	CFG11	<16>
CFG19	22	CFG19	<16>
CFG18	24	CFG18	<16>
CFG12	28	CFG12	<16>
CFG13	30	CFG13	<16>
CFG14	34	CFG14	<16>
CFG15	36	CFG15	<16>
CLK_XDP	40	CLK_CPU_ITP	<9>
CLK_XDP#	42	CLK_CPU_ITP#	<9>
XDP_RST# R	46	PLT_RST#	<10,30,32,41>
XDP_DBRESET#	48	+3VS	
TDO_XDP	52		
TRST#_XDP	54		
TDI_XDP	56		
TMS_XDP	58		
CFG3_R	60	CFG3	

RC8 XDP@ 0_0402_5% — RC10 XDP@ 0_0402_5% — RC13 1K_0402_5% XDP@ — RC14 1K_0402_1% — RC15 1K_0402_5% XDP@ — CC6 0.1U_0402_10V7K

PLT_RST# — ESD@ CC4 0.047U_0402_16V4Z

Place CC4 close to RC13.1

Place near JXDP

H_CPUPWRGD	RC7 1K_0402_5% XDP@	H_VCCST_PWRGD_XDP	
<10,41> PBTN_OUT#	RC9 0_0402_5% XDP@	CFG_PWRBTN#_XDP	
<13> CPU_PWR_DEBUG#	RC11 1K_0402_5% XDP@	CPU_PWR_DEBUG# R	
SYS_PWROK	RC12 0_0402_5% XDP@	SYS_PWROK_XDP	
<9,17,18,36> DDR_XDP_WLAN_TP_SMBDAT	RPC1 8	DDR_XDP_SMBDAT_R1	
<9,17,18,36> DDR_XDP_WLAN_TP_SMBCLK	7	DDR_XDP_SMBCLK_R1	
PCH_JTAG_TCK	6	XDP_TCLK	
	5 0_8P4R_5% XDP@		

H_CPUPWRGD — RC25 10K_0402_5% — CC8 100P_0402_50V8J ESD@

UC1B — HASWELL_MCP_E — MISC — JTAG — THERMAL — PWR — DDR3 — 2 OF 19 — Rev1p2

<41> PECI_EC	H_CATERR#	D61	
	PECI_EC	K61	
		N62	
<41,47,48> H_PROCHOT#	RC26 56_0402_5% H_PROCHOT# R	K63	
H_CPUPWRGD		C61	
		AU60	
	SM_RCOMP0	AV60	
	SM_RCOMP1	AU61	
	SM_RCOMP2	AV15	
<17,18> DDR3_DRAMRST#_CPU	SM_DRAMRST	AV61	
<17> DDR_PG_CTRL	SM_PG_CNTL1		

PRDY	J62	XDP_PRDY#	
PREQ	K62	XDP_PREQ#	
PROC_TCK	E60	XDP_TCK	
PROC_TMS	E61	XDP_TMS	
PROC_TRST	E59	XDP_TRST#	
PROC_TDI	K59	XDP_TDI	
PROC_TDO	F63	XDP_TDO	
	F62		
	J60	XDP_OBS0_R	
	H60	XDP_OBS1_R	
BPM#0	H61		
BPM#1	H62		
BPM#2	H63		
BPM#3	K60		
BPM#4	J61		
BPM#5			
BPM#6			
BPM#7			

RC28 1 2 0_0402_1% — RC27 @ 0_0402_5% — PCH_JTAG_RST# — PCH_JTAG_RST# <8>

T1 T2 T3 T4 T5 T6

PU/PD for JTAG signals

+1.05VS — XDP_TMS XDP_TDI XDP_PREQ# TDO_XDP — RPC2 51_8P4R_5% — XDP_TDO XDP_TCK XDP_TRST# — RPC3 51_8P4R_5%

200_0402_1%	RC29	SM_RCOMP0	
120_0402_1%	RC30	SM_RCOMP1	
100_0402_1%	RC31	SM_RCOMP2	

DDR3 COMPENSATION SIGNALS
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

DDR3_DRAMRST#_CPU — @ESD@ CC9 0.047U_0402_16V4Z

Place CC9 on BOT

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

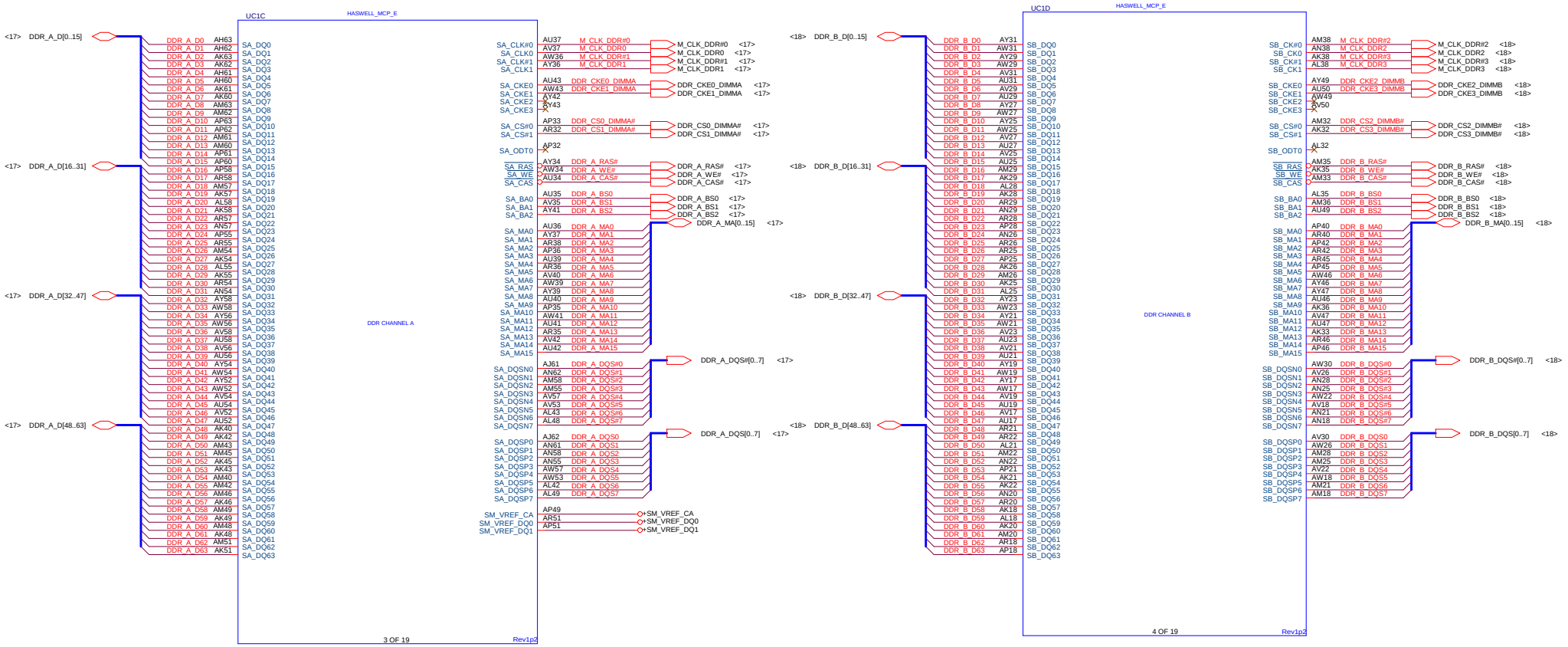
Compal Electronics, Inc.

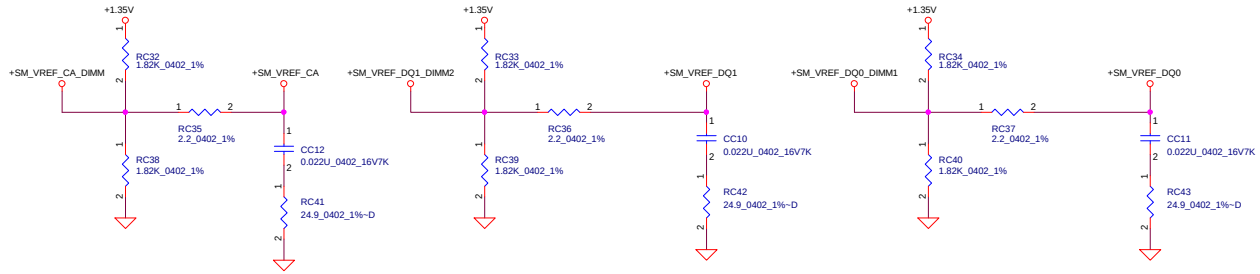
Title: **MCP(1,2/19) eDP,XDP,MISC**

Size: | Document Number: **LA-A301P** | Rev: 1.0

Date: Wednesday, September 24, 2014 | Sheet 6 of 56

Non-Interleaved memory





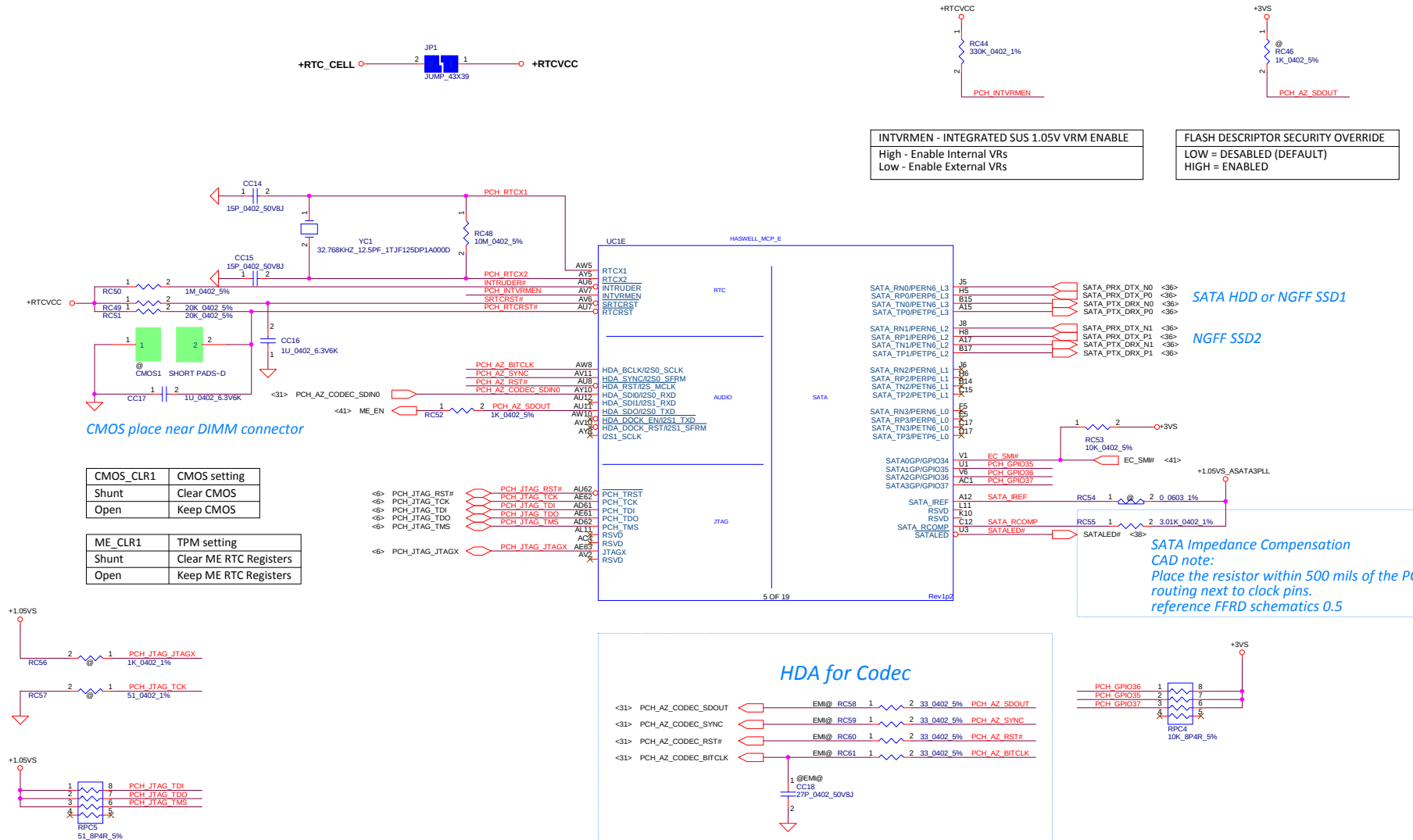
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(3,4/19) DDR3L**

Size: | Document Number: **LA-A301P** | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 7 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

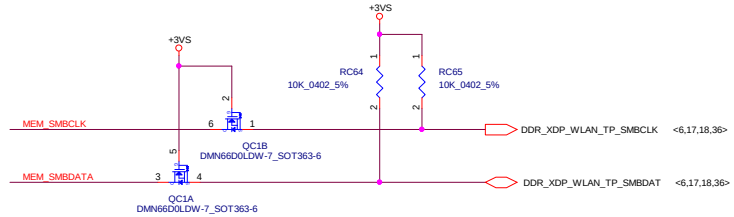
Compal Electronics, Inc.

Title: MCP(5/19) RTC,SATA,HDA,JTAG

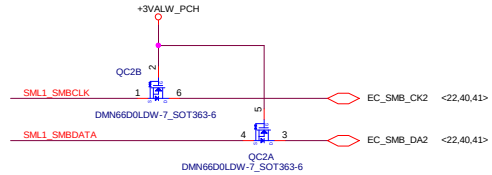
Size	Document Number	Rev
	LA-A301P	1.0

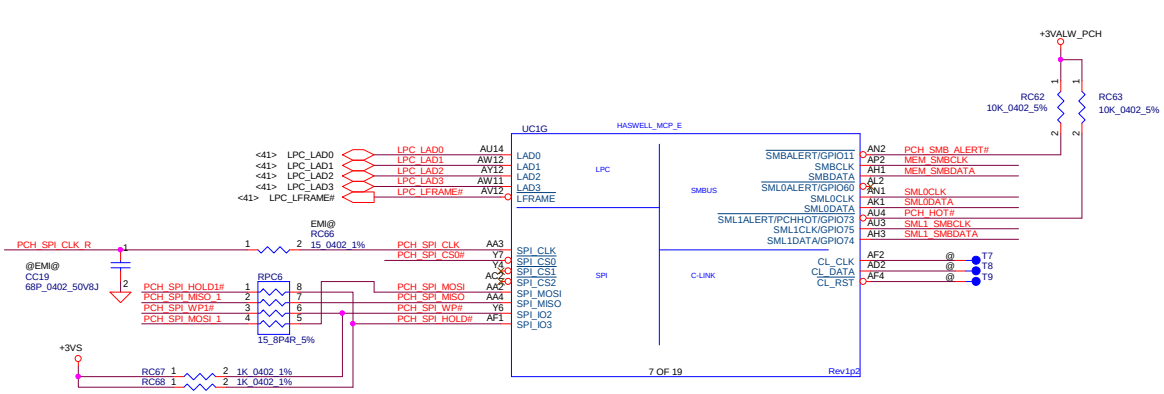
Date: Friday, September 19, 2014 Sheet 8 of 56

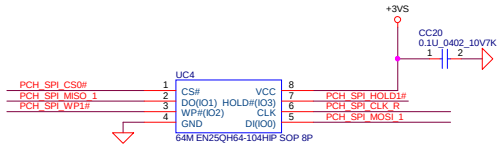
MEM Bus : DDR/XDP/WLAN/TP

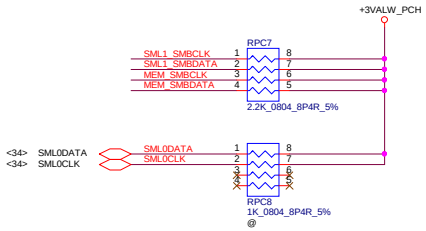


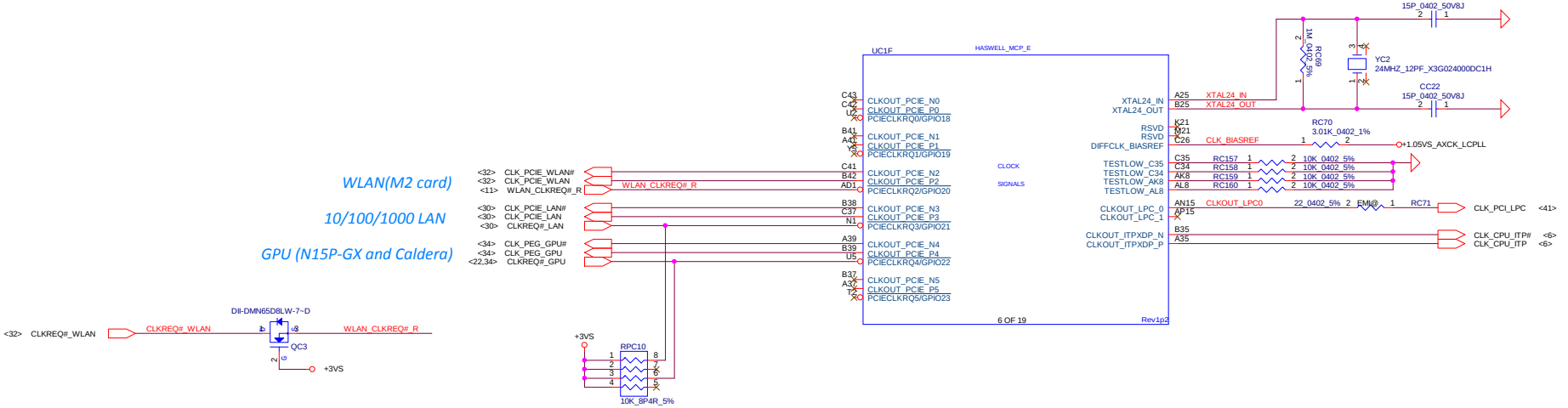
SML1 Bus : EC/Sensors











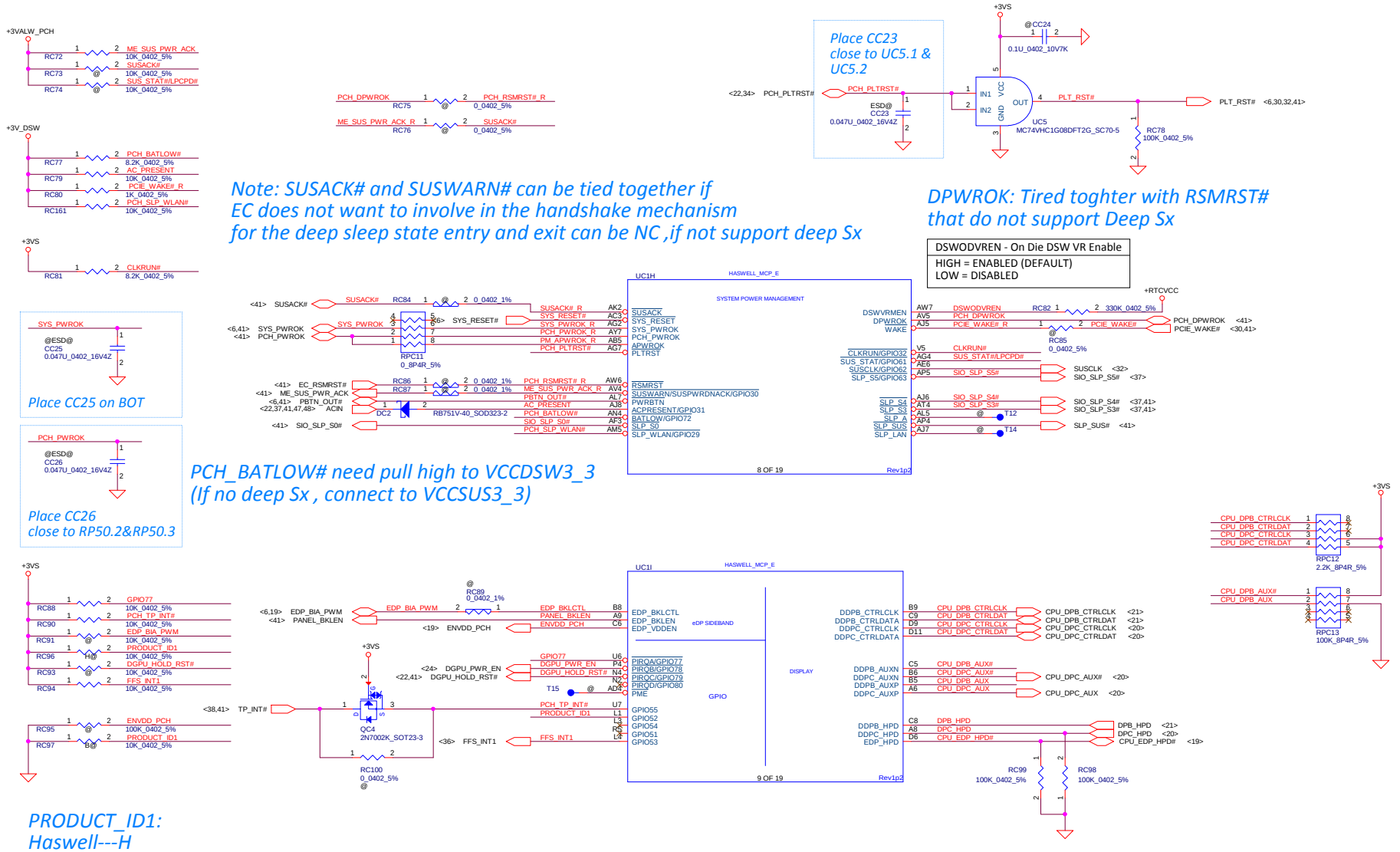
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(6,7/19) CLK,SMB,SPI,LPC**

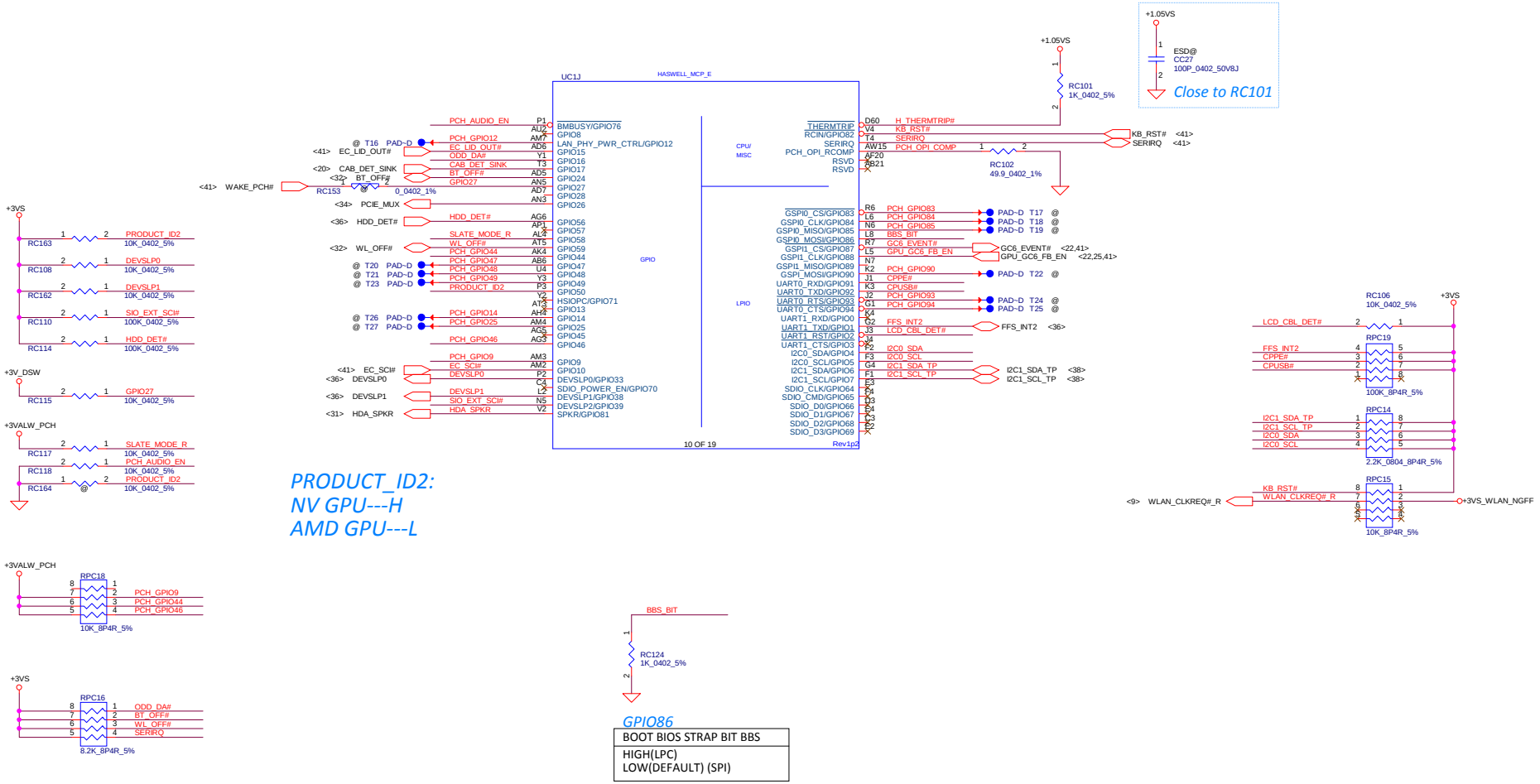
Size: | Document Number: **LA-A301P** | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 9 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.	
Title	MCP(8,9/19) DDI,EDP,GPIO
Size	Document Number: LA-A301P
Rev	1.0
Date: Friday, September 19, 2014	Sheet 10 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(10/19) GPIO,LPIO,MISC**

Size	Document Number	Rev
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Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(11/19) PCIE,USB**

Size: | Document Number: **LA-A301P** | Rev: 1.0

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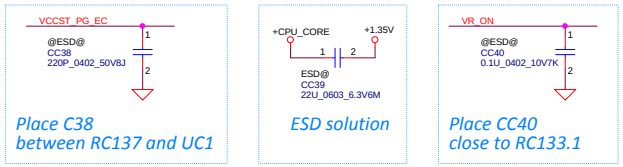
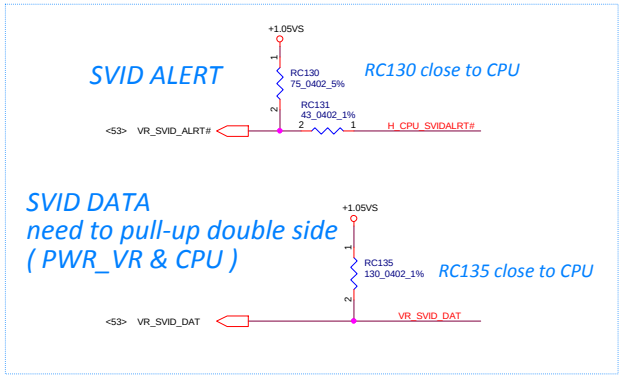
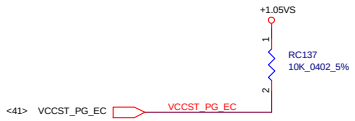
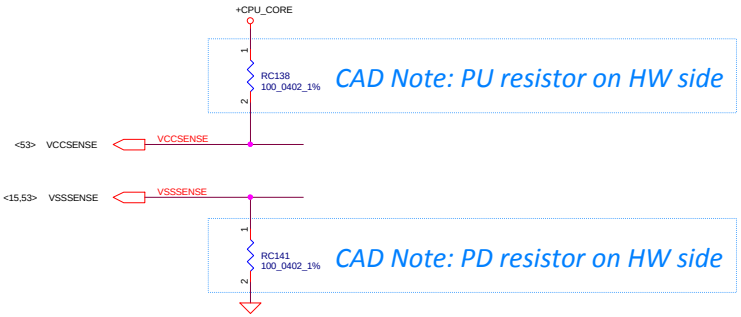
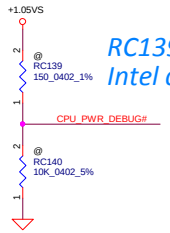




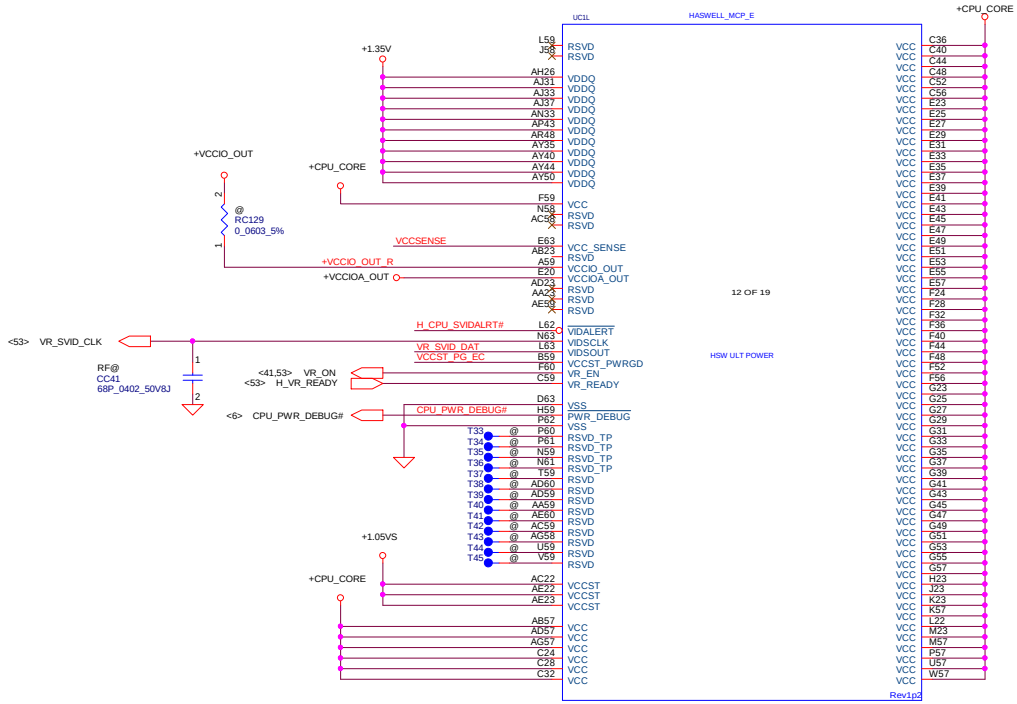


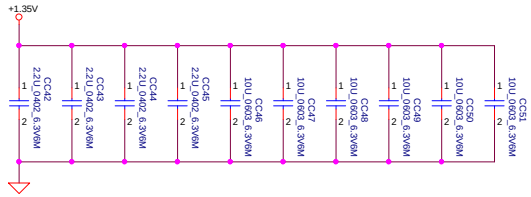
Define EC OD pin
need double confirm.





RC139
Intel check list , XDP use only





VDDQ DECOUPLING
*+1.35V : 470UF/2V/7343 *2 (PWR)*
*10UF/6.3V/0603 * 6*
*2.2UF/6.3V/0402 * 4*

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(12/19) Power**

Size | Document Number: **LA-A301P** | Rev: 1.0

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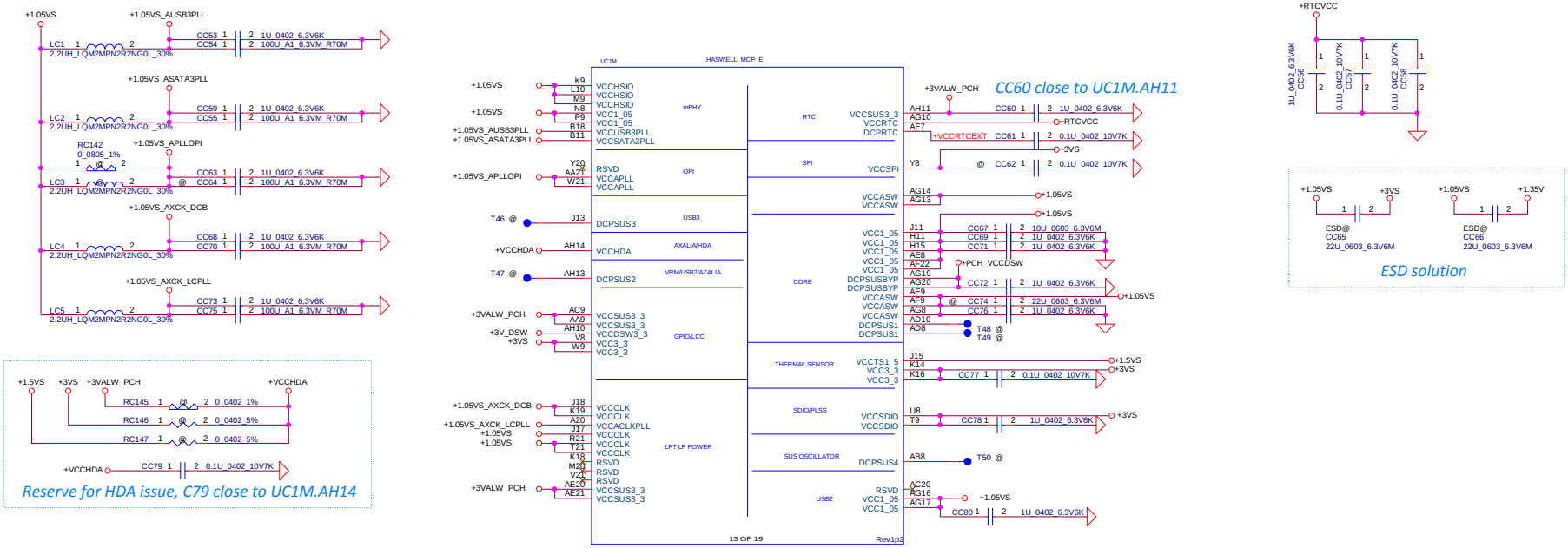

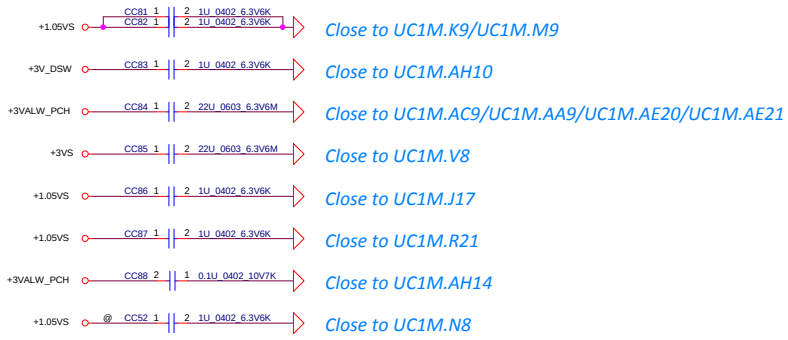

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(13/19) Power**

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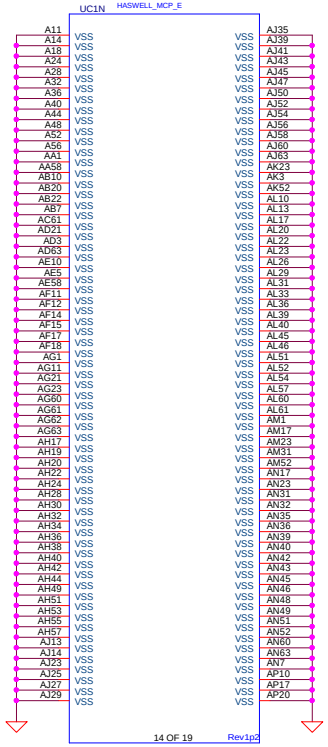

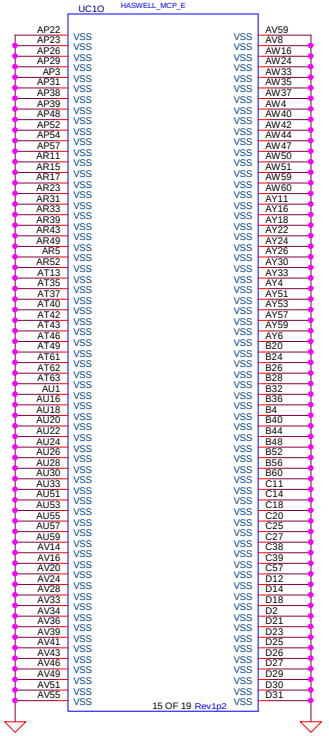

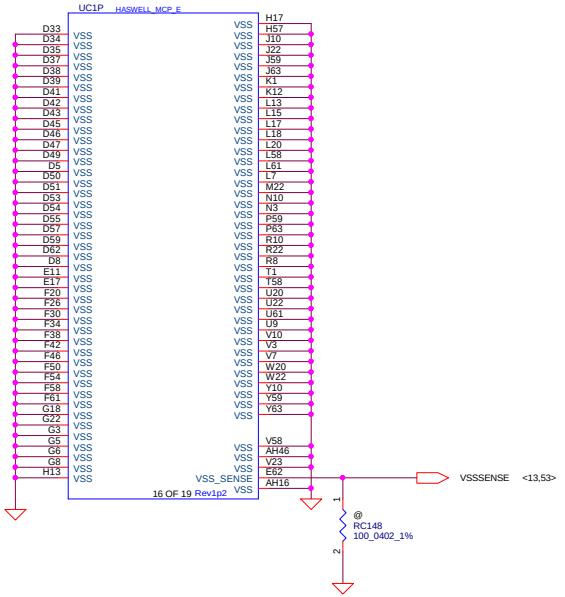

RC148 SHOULD BE PLACED CLOSE TO CPU

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **MCP(14,15,16/19) VSS**

Size | Document Number: **LA-A301P** | Rev: 1.0

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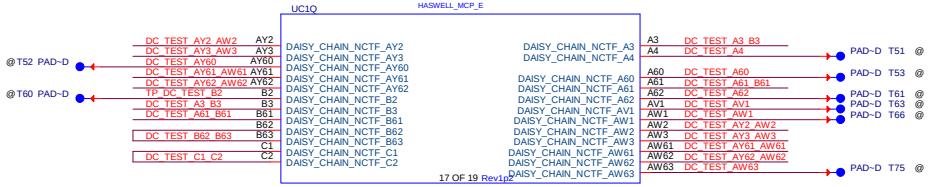
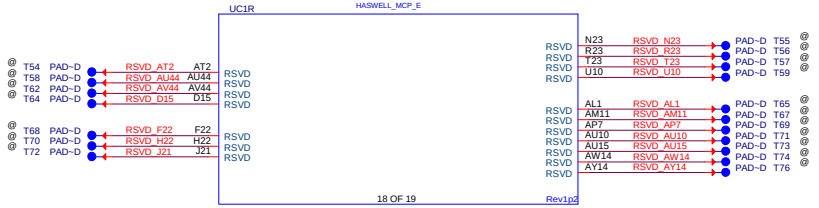
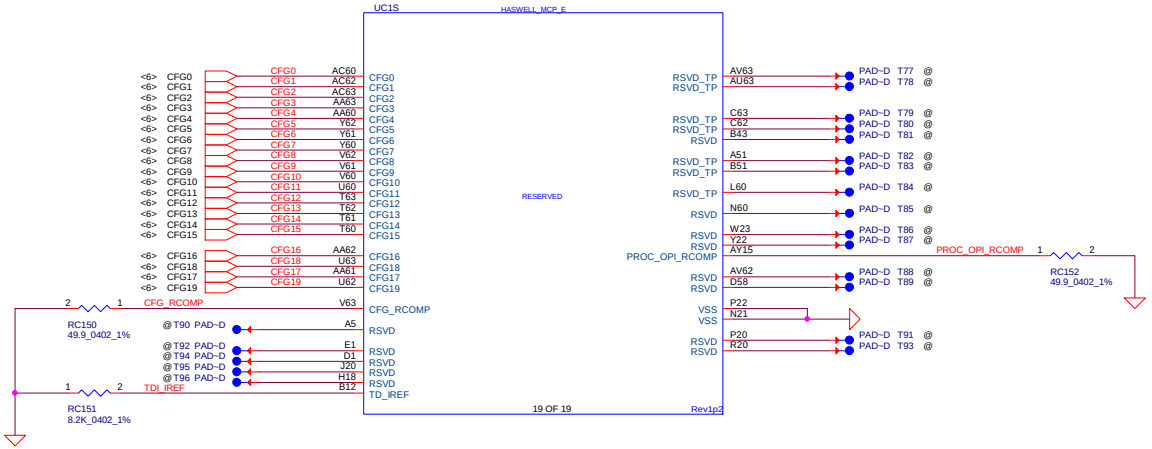
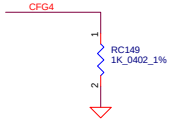






CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

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2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_A_DQS#[0..7]
<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

+SM_VREF_DQ0_DIMM1
+1.35V
JDIMM1
FOX_AS0A621-J4RB-7H
CONN@

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

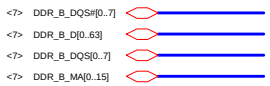
ESD solution

DDR3L SODIMM ODT GENERATION

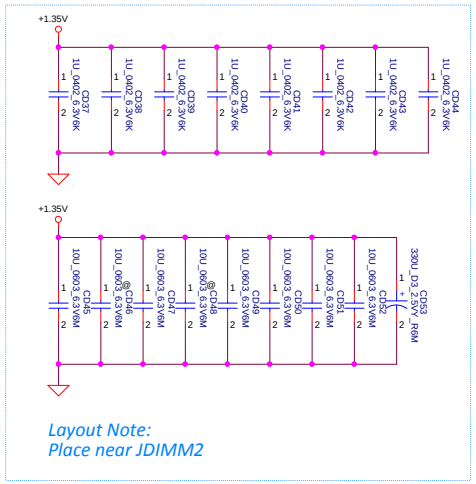
Place CD21 between QD1 and RD6

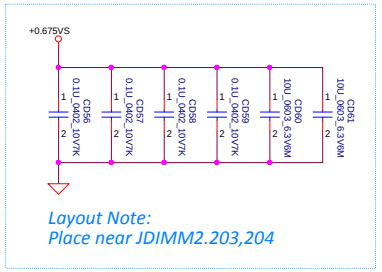
2-3A to 1 DIMMs/channel

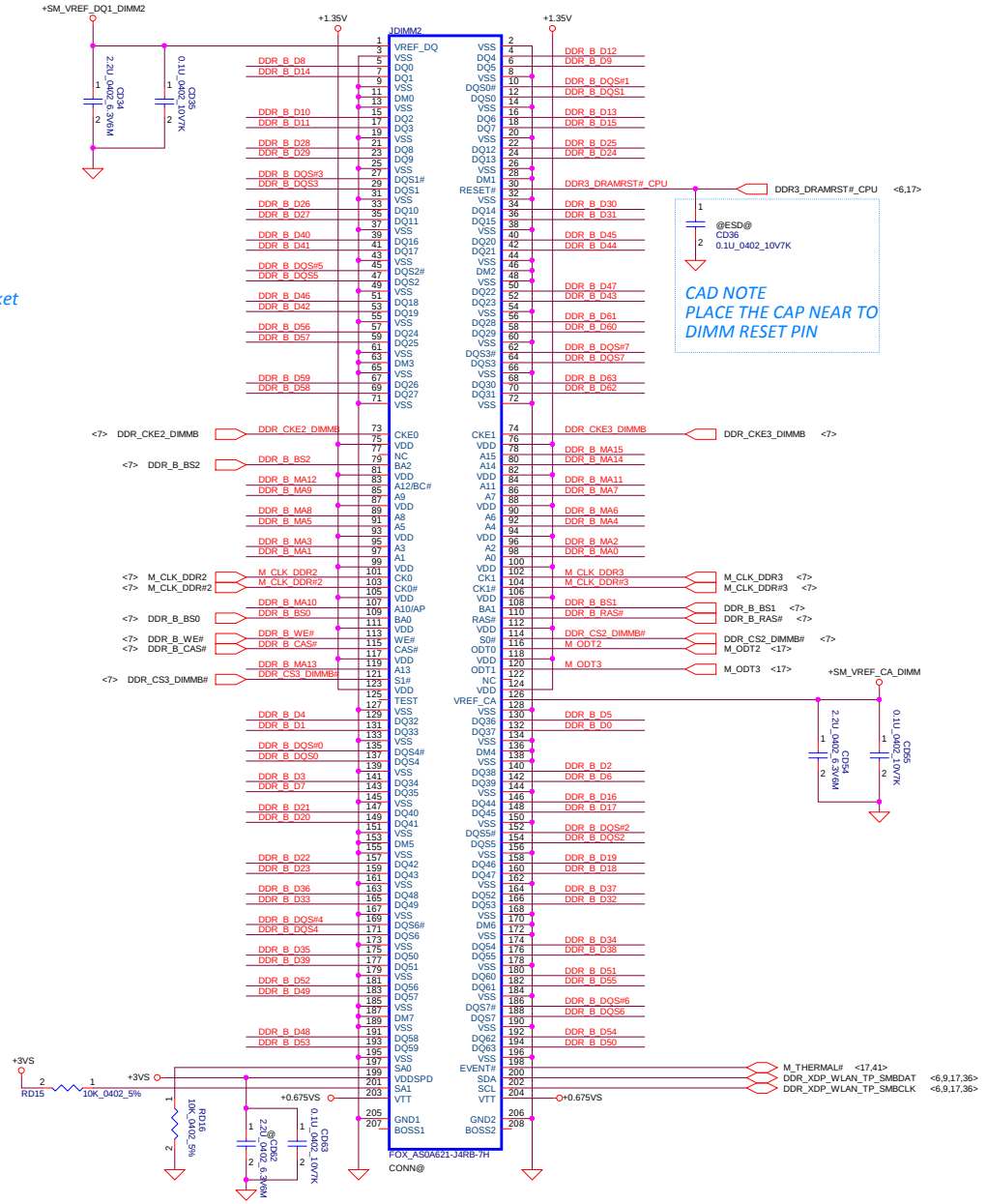
Populate RD13, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD13 for Intel DDR3
VREFDQ multiple methods M3



All VREF traces should
have 10 mil trace width
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

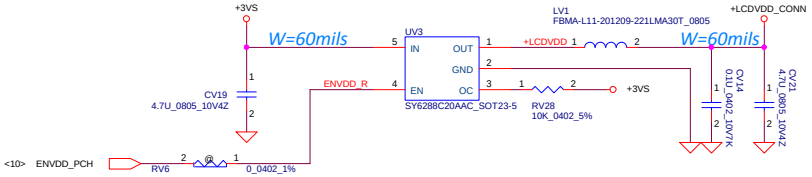


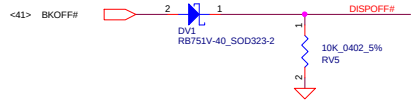


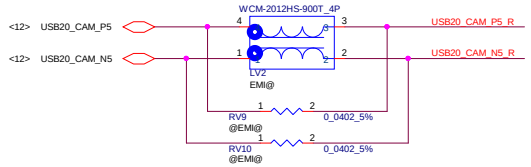


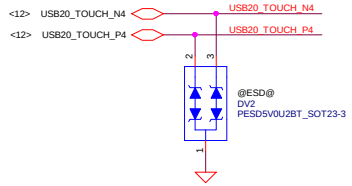
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2014/09/09	Title: DDRIII DIMMB
				Size: Document Number: LA-A301P Rev: 1.0
				Date: Friday, September 19, 2014 Sheet 18 of 56

LCD power control

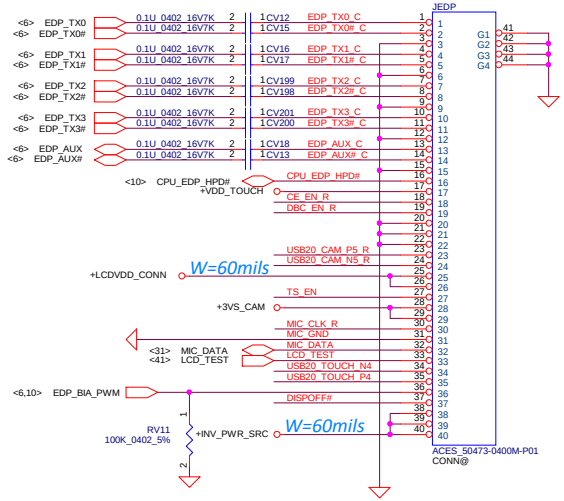




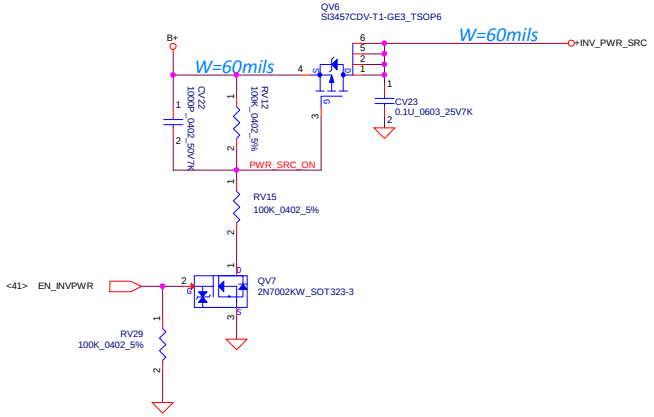


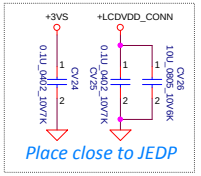


eDP connector

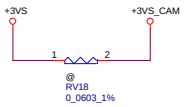


LCD backlight power control

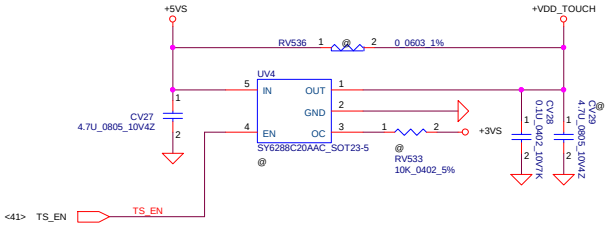


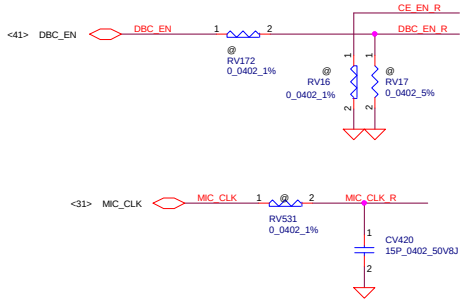


Webcam power control



Touch screen panel power control





Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: eDP/webcam/touch

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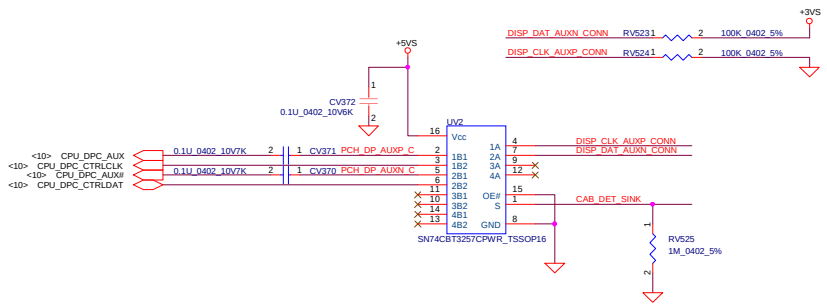
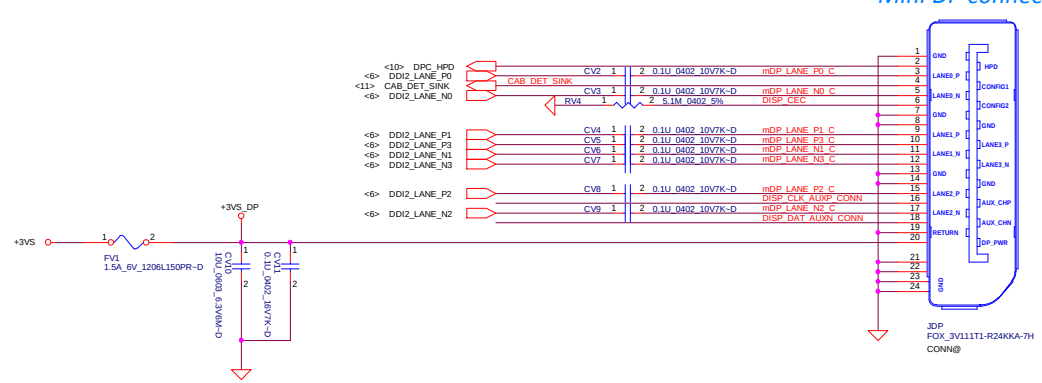


S = L, A port = B1 port (DP Port)
S = H, A port = B2 port (HDMI/DVI/VGA Dongle)

Mini DP connector



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: Mini DP

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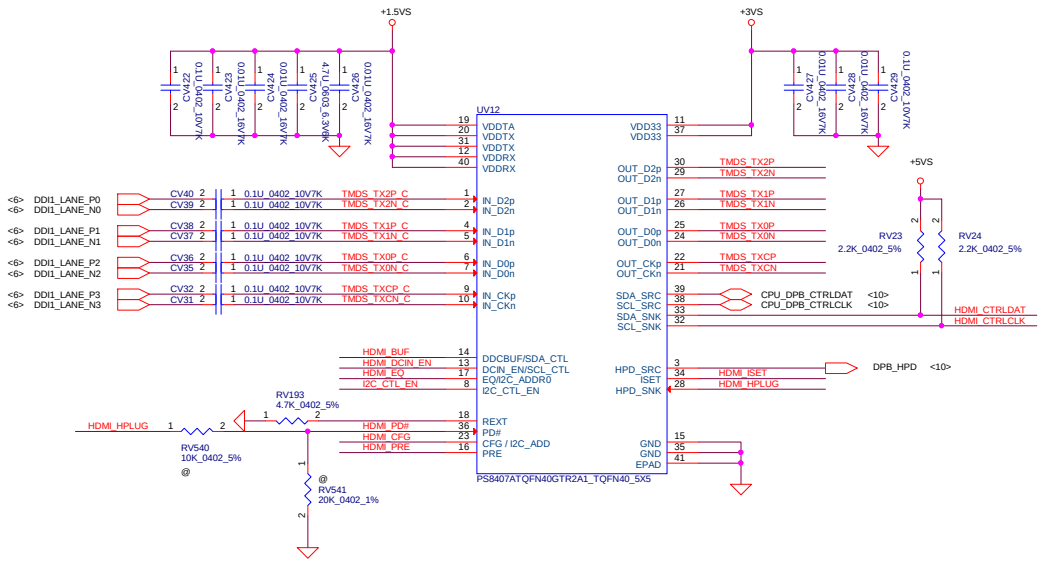
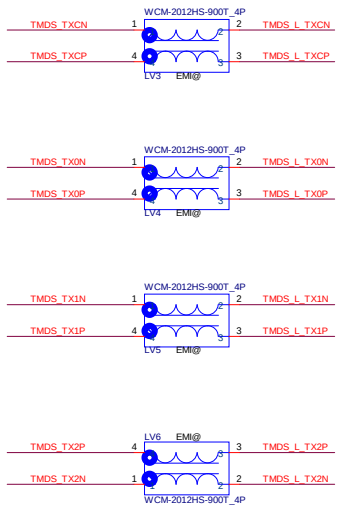
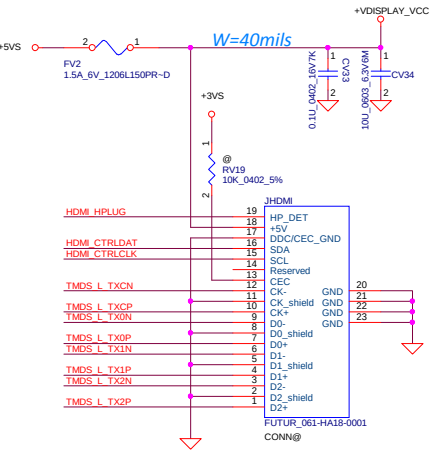
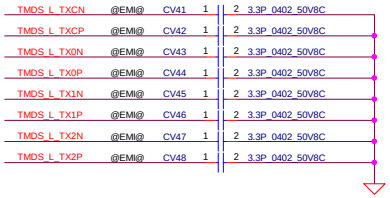


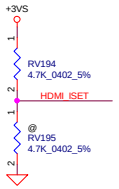
Place close to JHDMI



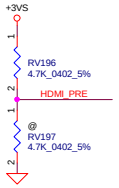


ROYALTY HDMI W/LOGO
CPN:RO0000002HM

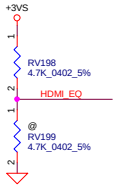




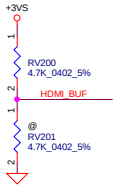
TMDS output swing adjustment; Internal 150K PD)
( ) L: default
(*) H: increase +13%
( ) M: reduce -13%



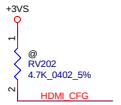
Output pre-emphasis setting(Internal 150K PD)
( ) L: no pre-emphasis
(*) H: 1.6dB pre-emphasis
( ) M: 3.0dB pre-emphasis



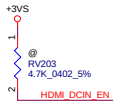
Receiver equalization setting(Internal 150K PD)
( ) L: programmable EQ for channel loss up to 5.3dB
(*) H: programmable EQ for channel loss up to 10dB
( ) M: programmable EQ for channel loss up to 14dB



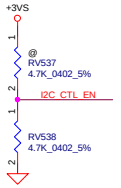
Enable active DDC buffer(Internal 150K PD)
( ) L: default, passive DDC pass-through
(*) H: active DDC buffer W/ internal PU 2.36K resistor
( ) M: active DDC buffer W/O internal PU resistor



CFG(Internal 150K PD)
(*) L: HDMI ID disable(default)
( ) H: HDMI ID enable



DC en(Internal 150K PD)
(*) L: AC coupling input(default)
( ) H: DC coupling input



I2C control en(Internal 150K PD)
(*) L: auto jitter cleaning(default)
( ) H: I2C address
( ) M: full jitter cleaning

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: HDMI/PS8407A

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UV1
S IC CL8064701477802 SR1EF D0 1.7G A31!
SA00007CM0L
R1N15P@

UV1
S IC CL8064701477802 SR1EF D0 1.7G A31!
SA00007CM1L
R3N15P@

UV1
S IC CL8064701477802 SR1EF D0 1.7G A31!
SA00084Q0L
R1N16P@

UV1
S IC CL8064701477802 SR1EF D0 1.7G A31!
SA00084Q1L
R3N16P@

UV1A
Part 1 of 7
N15P-GT_BGA908
@

PCI EXPRESS
GPIO
DACs
I2C
CLK

<34> PEG_CTX_GRX_P0_GPU
<34> PEG_CTX_GRX_N0_GPU
<34> PEG_CTX_GRX_P1_GPU
<34> PEG_CTX_GRX_N1_GPU
<34> PEG_CTX_GRX_P2_GPU
<34> PEG_CTX_GRX_N2_GPU
<34> PEG_CTX_GRX_P3_GPU
<34> PEG_CTX_GRX_N3_GPU

PEX_RX0 AN12
PEX_RX0_N AN13
PEX_RX1 AN14
PEX_RX1_N AP14
PEX_RX2 AP15
PEX_RX2_N AN15
PEX_RX3 AM15
PEX_RX3_N AN17
PEX_RX4 AM17
PEX_RX4_N AP17
PEX_RX5 AP18
PEX_RX5_N AN18
PEX_RX6 AM18
PEX_RX6_N AN20
PEX_RX7 AM20
PEX_RX7_N AP20
PEX_RX8 AP21
PEX_RX8_N AN21
PEX_RX9 AM21
PEX_RX9_N AN23
PEX_RX10 AM23
PEX_RX10_N AP23
PEX_RX11 AP24
PEX_RX11_N AN24
PEX_RX12 AM24
PEX_RX12_N AN26
PEX_RX13 AM26
PEX_RX13_N AP26
PEX_RX14 AP27
PEX_RX14_N AN27
PEX_RX15 AM27
PEX_RX15_N AK14

<34> PEG_CRX_GTX_P0_GPU
<34> PEG_CRX_GTX_N0_GPU
<34> PEG_CRX_GTX_P1_GPU
<34> PEG_CRX_GTX_N1_GPU
<34> PEG_CRX_GTX_P2_GPU
<34> PEG_CRX_GTX_N2_GPU
<34> PEG_CRX_GTX_P3_GPU
<34> PEG_CRX_GTX_N3_GPU

CV54 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_P0
CV55 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_N0
CV56 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_P1
CV57 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_N1
CV58 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_P2
CV59 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_N2
CV60 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_P3
CV61 1 2 0.22U_0402_10V6K PEG_CRX_GTX_C_N3

PEX_TX0 AJ14
PEX_TX0_N AH14
PEX_TX1 AG14
PEX_TX1_N AK15
PEX_TX2 AJ15
PEX_TX2_N AL16
PEX_TX3 AK16
PEX_TX3_N AK17
PEX_TX4 AJ17
PEX_TX4_N AH17
PEX_TX5 AG17
PEX_TX5_N AK18
PEX_TX6 AJ18
PEX_TX6_N AL19
PEX_TX7 AK19
PEX_TX7_N AK20
PEX_TX8 AJ20
PEX_TX8_N AH20
PEX_TX9 AG20
PEX_TX9_N AK21
PEX_TX10 AJ21
PEX_TX10_N AL22
PEX_TX11 AK22
PEX_TX11_N AK23
PEX_TX12 AJ23
PEX_TX12_N AH23
PEX_TX13 AG23
PEX_TX13_N AK24
PEX_TX14 AJ24
PEX_TX14_N AL25
PEX_TX15 AK25
PEX_TX15_N AJ11
NC AL13
PEX_REFCLK AK13
PEX_REFCLK_N AK12
PEX_CLKREQ_N AJ26
PEX_TSTCLK_OUT AK26
PEX_TSTCLK_OUT_N AJ12
PEX_RST_N AP25
PEX_TERMP

<34> CLK_PEG_N15P
<34> CLK_PEG_N15P#
CLK_REQ
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
DGPU_PEX_RST#
PEX_TSTCLK_OUT
DGPU_PEX_RST# R
PEX_TERMP
RV47 200_0402_1%
RV40 0_0402_1%
RV50 2.49K_0402_1%

GPIO0 P6 GPU_GC6_FB_EN
GPIO1 M3
GPIO2 L6
GPIO3 P5
GPIO4 P7
GPIO5 L7 3V3_MAIN_EN
GPIO6 M7 GC6_EVENT#_D
GPIO7 N8
GPIO8 L3 SYS_PEX_RST_MON#
GPIO9 M2 THERMAL_ALERT#
GPIO10 L1 MEM_VREF
GPIO11 M5 NVVDD PWM_VID
GPIO12 N3 GPU_LEVEL
GPIO13 M4 NVVDD PSI
GPIO14 N4
GPIO15 P2
GPIO16 R8
GPIO17 M6
GPIO18 R1
GPIO19 P3
GPIO20 P4
GPIO21 P1 GPU_PEX_RST_HOLD#

GPU_GC6_FB_EN <11,25,41>
3V3_MAIN_EN <25,52>
NVVDD PWM_VID <52>
NVVDD PSI <52>
MEM_VREF <27,28>
RV27 100K_0402_5%~D

GC6_EVENT#_D 2 1 GC6_EVENT#
DV9 RB751S40T1G_SOD523-2
GC6_EVENT# <11,41>

+3.3V_GFX_AON
THERMAL_ALERT# RV526 10K_0402_5%
SYS_PEX_RST_MON# RV532 10K_0402_5%
GPU_PEX_RST_HOLD# RV41 10K_0402_5%
3V3_MAIN_EN RV55 10K_0402_1%
GC6_EVENT#_D RV42 10K_0402_5%
GPU_LEVEL RV60 100K_0402_5%~D
NVVDD PSI RV35 10K_0402_1%

+3.3V_GFX_AON
VGA_SMB_CK2 RV191 1.8K_0402_5%
VGA_SMB_DA2 RV192 1.8K_0402_5%
GPU_GC6_FB_EN RV37 10K_0402_5%
MEM_VREF RV38 100K_0402_5%~D

DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
DACA_VDD AG10
DACA_VREF AP9
DACA_RSET AP8

SYS_PEX_RST_MON#
THERMAL_ALERT# 4 3 GPU_ALERT# <41>
2N7002DW-T/R7_SOT363-6
QV2B

SYS_PEX_RST_MON#
<23> OVERT# OVERT# 1 6 GPU_OVERT# <41>
2N7002DW-T/R7_SOT363-6
QV2A

I2CA_SCL R4 VGA_CRT_CLK
I2CA_SDA R5 VGA_CRT_DATA RV510 RV511 1.8K_0402_5%
I2CB_SCL R7 I2CB_SCL
I2CB_SDA R6 I2CB_SDA RV512 RV513 1.8K_0402_5%
I2C2C_SCL R2 VGA_EDID_CLK
I2C2C_SDA R3 VGA_EDID_DATA RV514 RV515 1.8K_0402_5%
I2C5_SCL T4 VGA_SMB_CK2
I2C5_SDA T3 VGA_SMB_DA2

+3.3V_GFX_AON
CV422 0.1U_0402_10V7K
GPU_LEVEL 4
GPU_PWR_LEVEL <41>
ACIN <10,37,41,47,48>
UV15 MC74VHC1G09DFT2G_SC70-5

GPU_PWR_LEVEL	
Low	Low Performace
High	High Performace

PLLVDD AD8
SP_PLLVDD AE8
VID_PLLVDD AD7
XTAL_IN H3 XTALIN
XTAL_OUT H2 XTAL_OUT
XTAL_OUTBUFF J4 XTALOUT
XTAL_SSIN H1 XTALSSIN
RV49 10K_0402_5%
RV51 10K_0402_5%

W=78mils
W=71mils
W=41mils
+PLLVDD
RV45 0_0402_5%
+SP_PLLVDD

+1.05VS_VGA
LV7 BLM18PG181SN1D_2P
180 ohm (ESR=0.2) Bead
150mA
+SP_PLLVDD
CV50 22U_0805_6.3V6M
CV51 4.7U_0402_6.3V6M
CV52 0.1U_0402_10V7K
CV53 0.1U_0402_10V7K
Under GPU (below 150mils)

+3VALW
RV58 10K_0402_5%
CV212 0.1U_0402_10V7K
<10,41> DGPU_HOLD_RST#
DGPU_HOLD_RST#
<10,34> PCH_PLTRST#
PCH_PLTRST#
UV14 TC7SH08FU_SSOP5~D
SYS_PEX_RST_MON#
RV187 10K_0402_5%
+3.3V_GFX_AON
RV39 10K_0402_5%
RV208 0_0402_5%
SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD#
DV8
DGPU_PEX_RST#
BAT54A-7-F_SOT23-3
GC6 2.0 function

Internal Thermal Sensor

+PLLVDD
RV52 10M_0402_5%
YV1 27MHZ_10PF_7V27000050
XTALIN
XTAL_OUT
GND GND
CV70 10P_0402_50VBJ
CV71 10P_0402_50VBJ

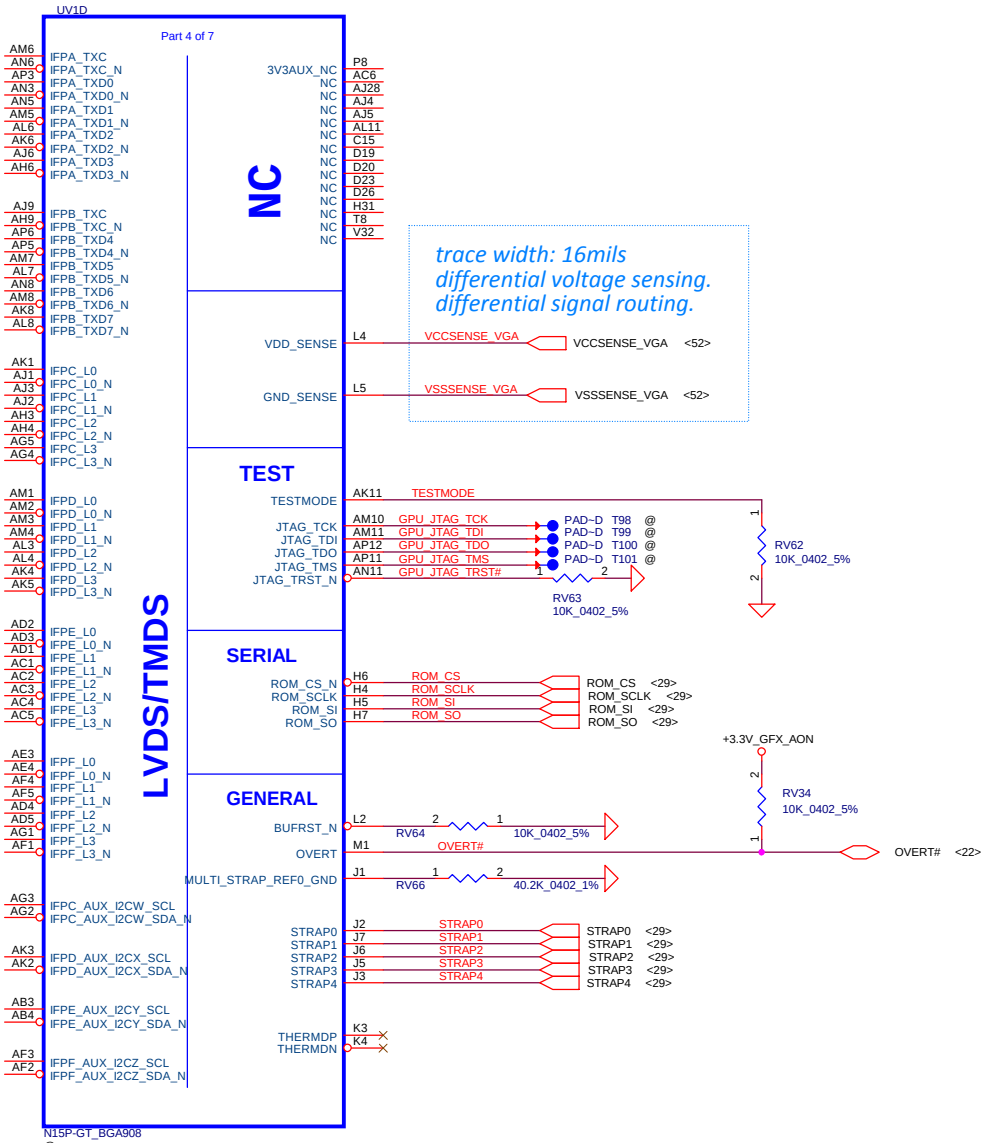
+PLLVDD
CV72 0.1U_0402_10V7K
CV73 22U_0805_6.3V6M
LV8 BLM18PG181SN1D_2P
+1.05VS_VGA
30 ohm@100MHz (ESR=0.05)
CV72 under GPU
CV73 near GPU

<25,52> NVVDD_PWR_GD
+3.3V_GFX_AON
RV56 10K_0402_5%
RV57 10K_0402_5%
QV12
<9,34> CLKREQ#_GPU
CLK_REQ
2N7002H 1N_SOT23-3

SYS_PEX_RST_MON#
VGA_SMB_CK2
EC_SMB_CK2 <9,40,41>
2N7002DW-T/R7_SOT363-6
QV1B
VGA_SMB_DA2
EC_SMB_DA2 <9,40,41>
2N7002DW-T/R7_SOT363-6
QV1A

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.
Title: N15P PCIE/DAC/GPIO
Size: B
Document Number: LA-A301P
Rev: 1.0
Date: Tuesday, September 23, 2014
Sheet 22 of 56



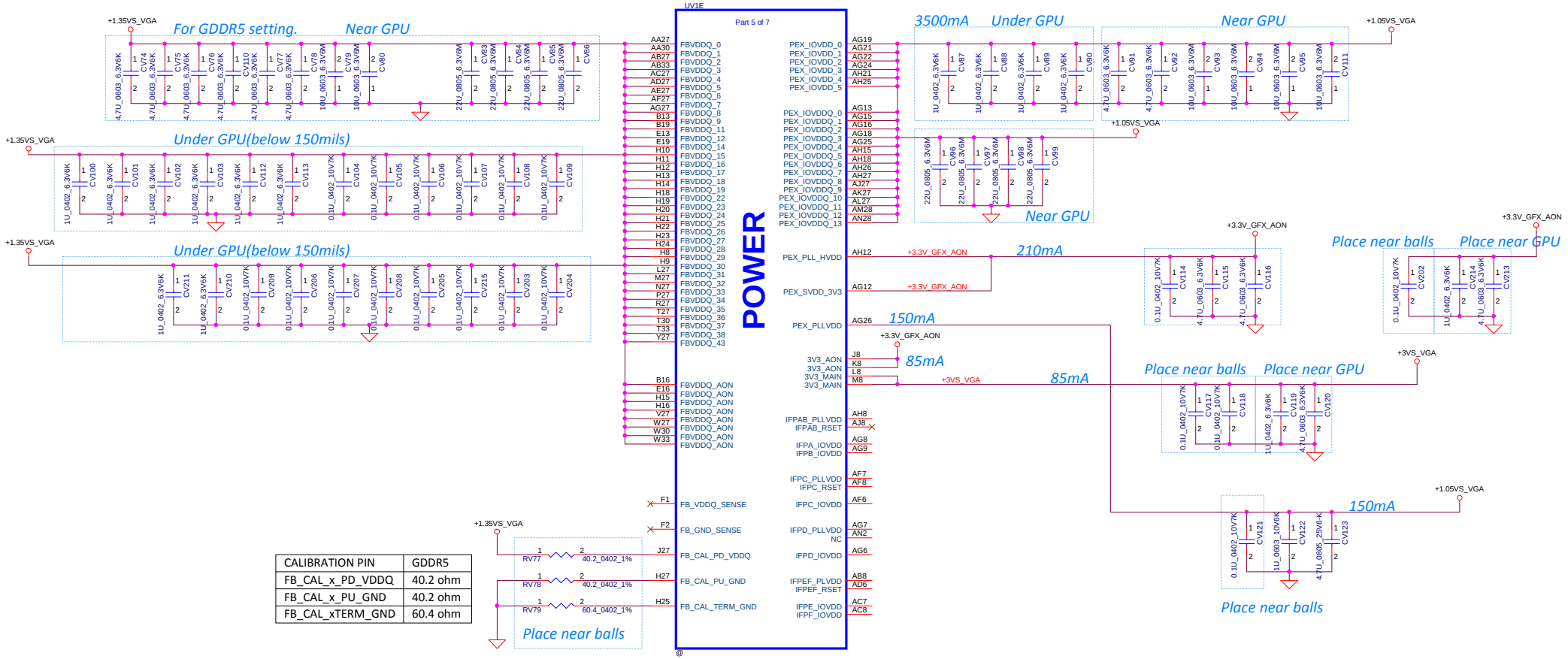
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **N15P_eDP/HDMI/mDP**

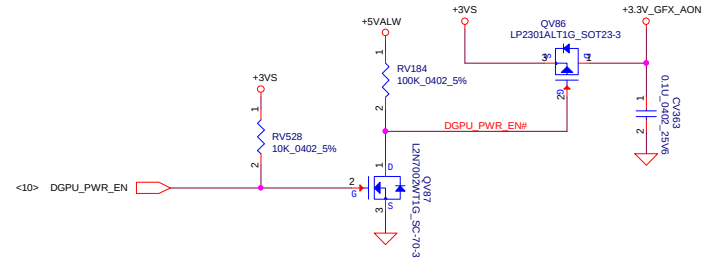
Size | Document Number: **LA-A301P** | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 23 of 56



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

+3.3V_GFX_AON



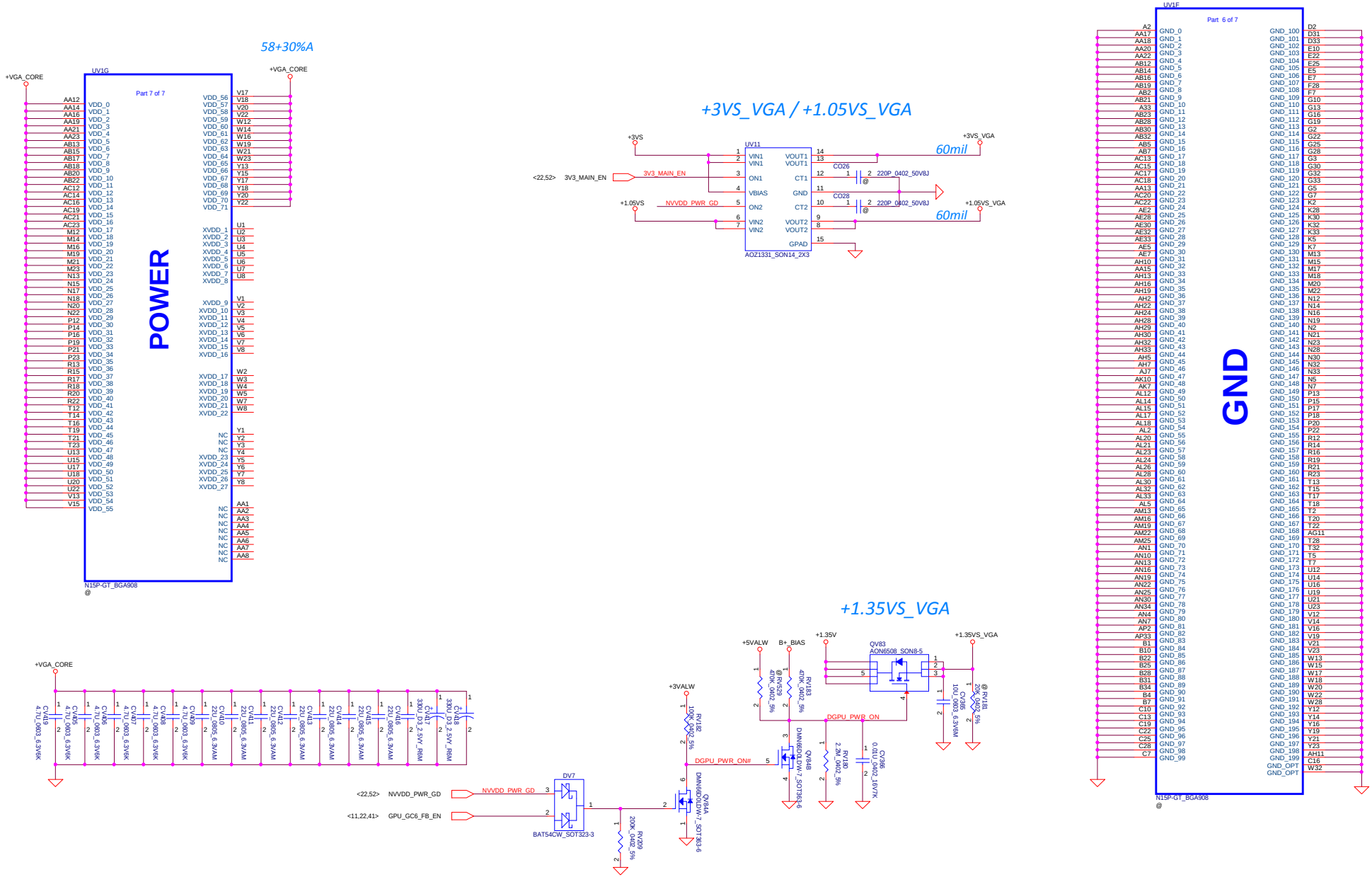
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **N15P_Power**

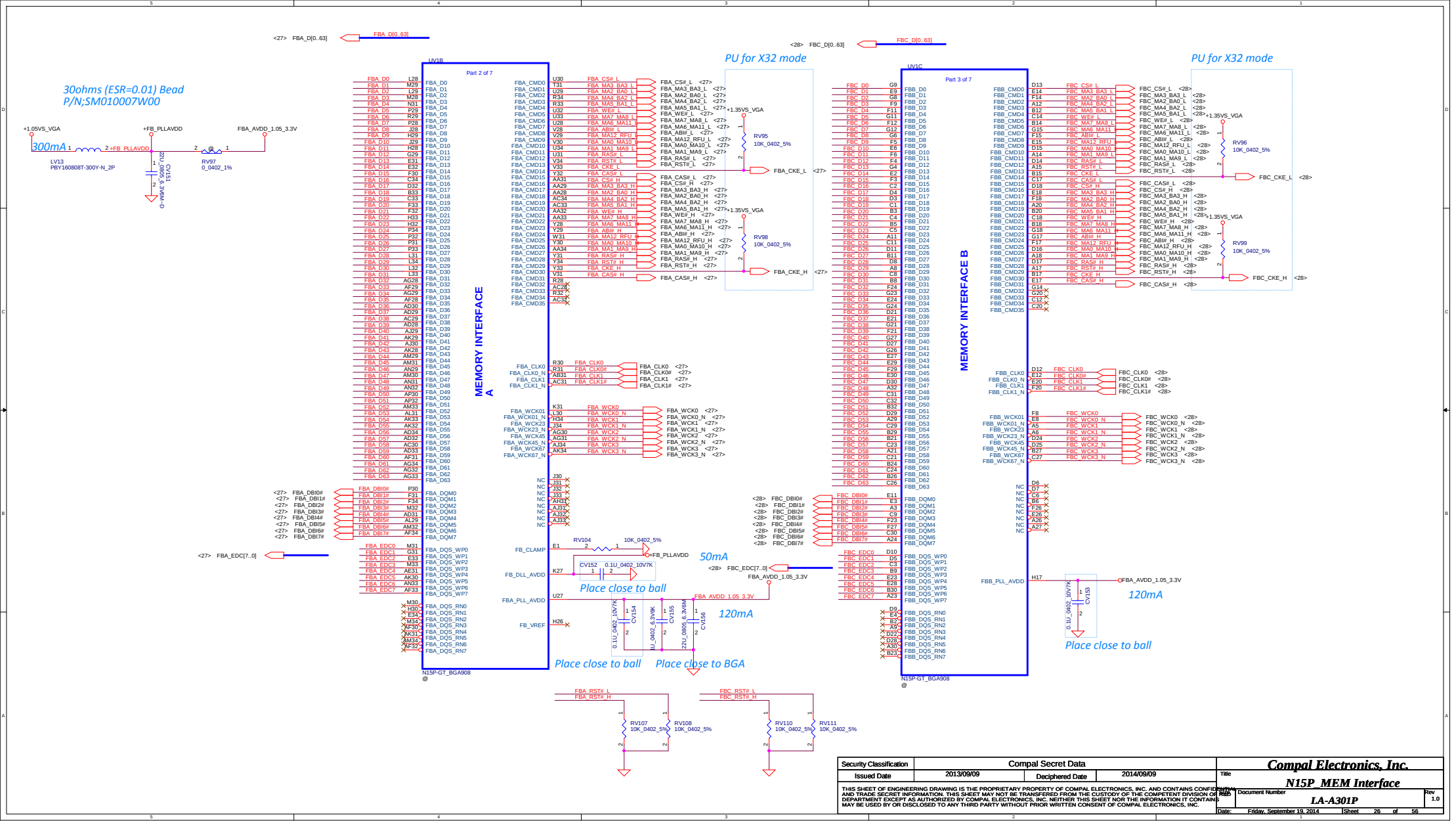
Size: | Document Number: **LA-A301P** | Rev: 1.0

Date: Friday, October 17, 2014 | Sheet 24 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.			
Title	N15P_VGA CORE/GND		
Size	Document Number		Rev
	LA-A301P		1.0
Date:	Friday, September 19, 2014	Sheet	25 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: *N15P_MEM Interface*

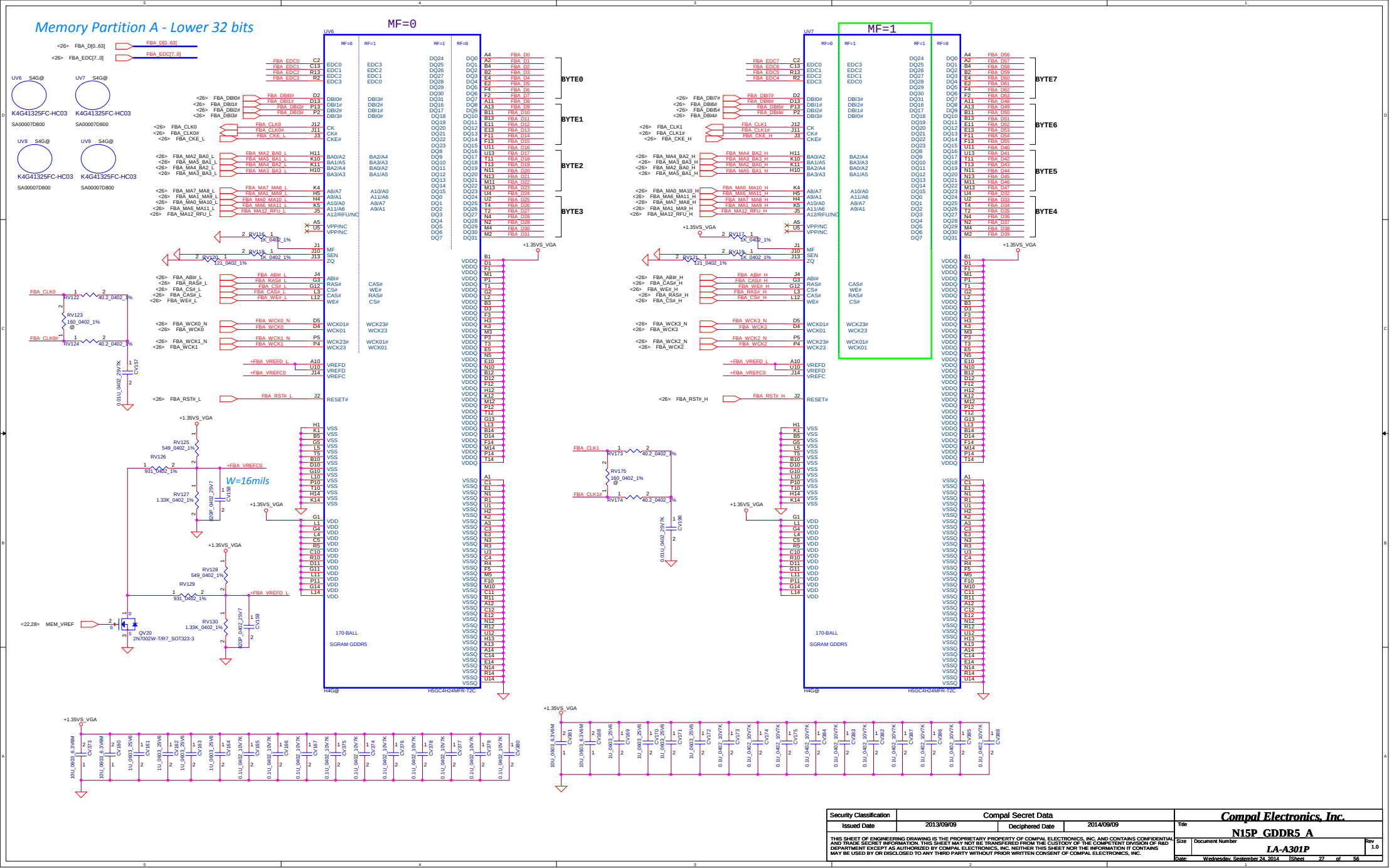
Size: A3 | Document Number: *LA-A301P* | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 26 of 56

Memory Partition A - Lower 32 bits

MF=0

MF=1



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

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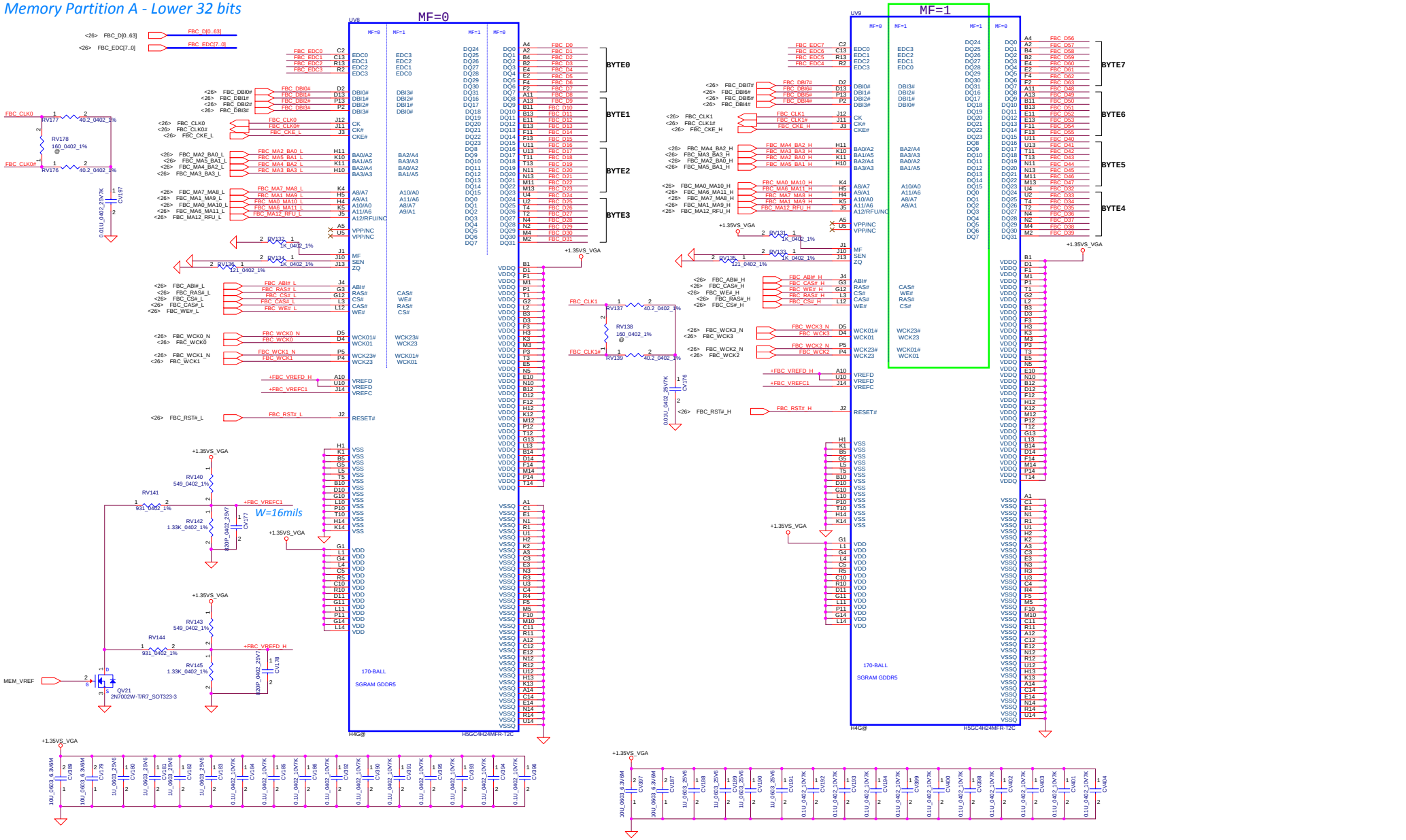
Compal Electronics, Inc.

Title: N15P GDDR5 A

Size: | Document Number: LA-A301P | Rev: 1.0

Date: Wednesday, September 24, 2014 | Sheet 27 of 56

Memory Partition A - Lower 32 bits



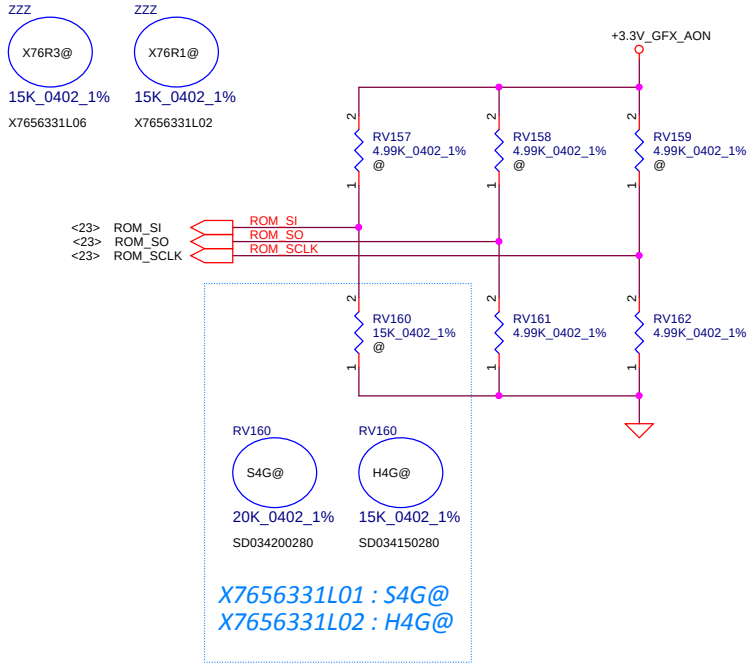
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

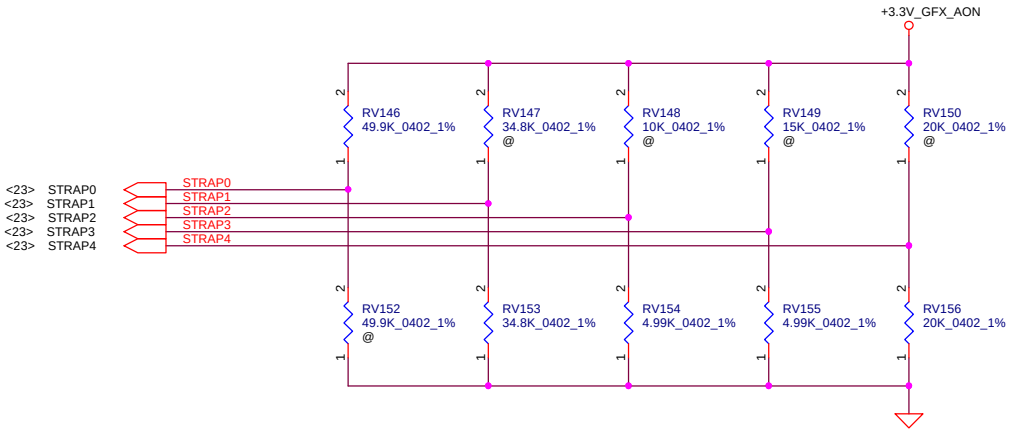
Compal Electronics, Inc.

Title: N15P_GDDR5_B

Size: | Document Number: LA-A301P | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 28 of 56

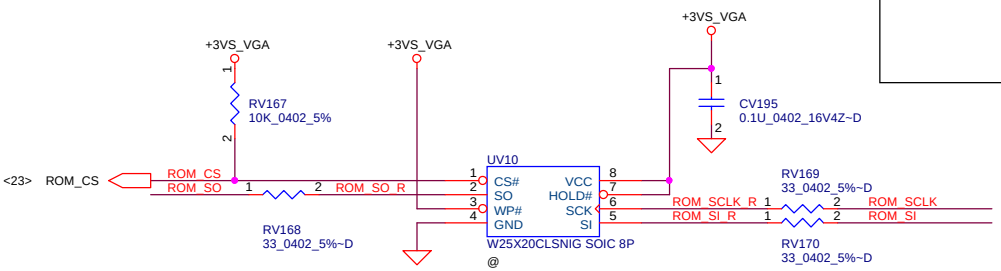




SA00007D800 S IC D5 128M32 K4G41325FC-HC03 FBGA 170P

SA00006O40L S IC D5 128M32/2.5G H5GC4H24MFR-T2C FBGA
SA00006O41L S IC D5 128M32/2.5G H5GC4H24MFR-T2C A31!

GPU	FB Memory GDDR5		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15P-GX	Samsung 2500MHz	K4G41325FC-HC03 256Mx16	PD 4.99K	PD 4.99K	PD 20K	PU 49.9K	PD 34.8K	PD 4.99K	PD 4.99K	PD 20K
	Hynix 2500MHz	H5GC4H24MFR-T2C 256Mx16	PD 4.99K	PD 4.99K	PD 15K	PU 49.9K	PD 34.8K	PD 4.99K	PD 4.99K	PD 20K



W25X20CL 2M-Bit/256K-byte

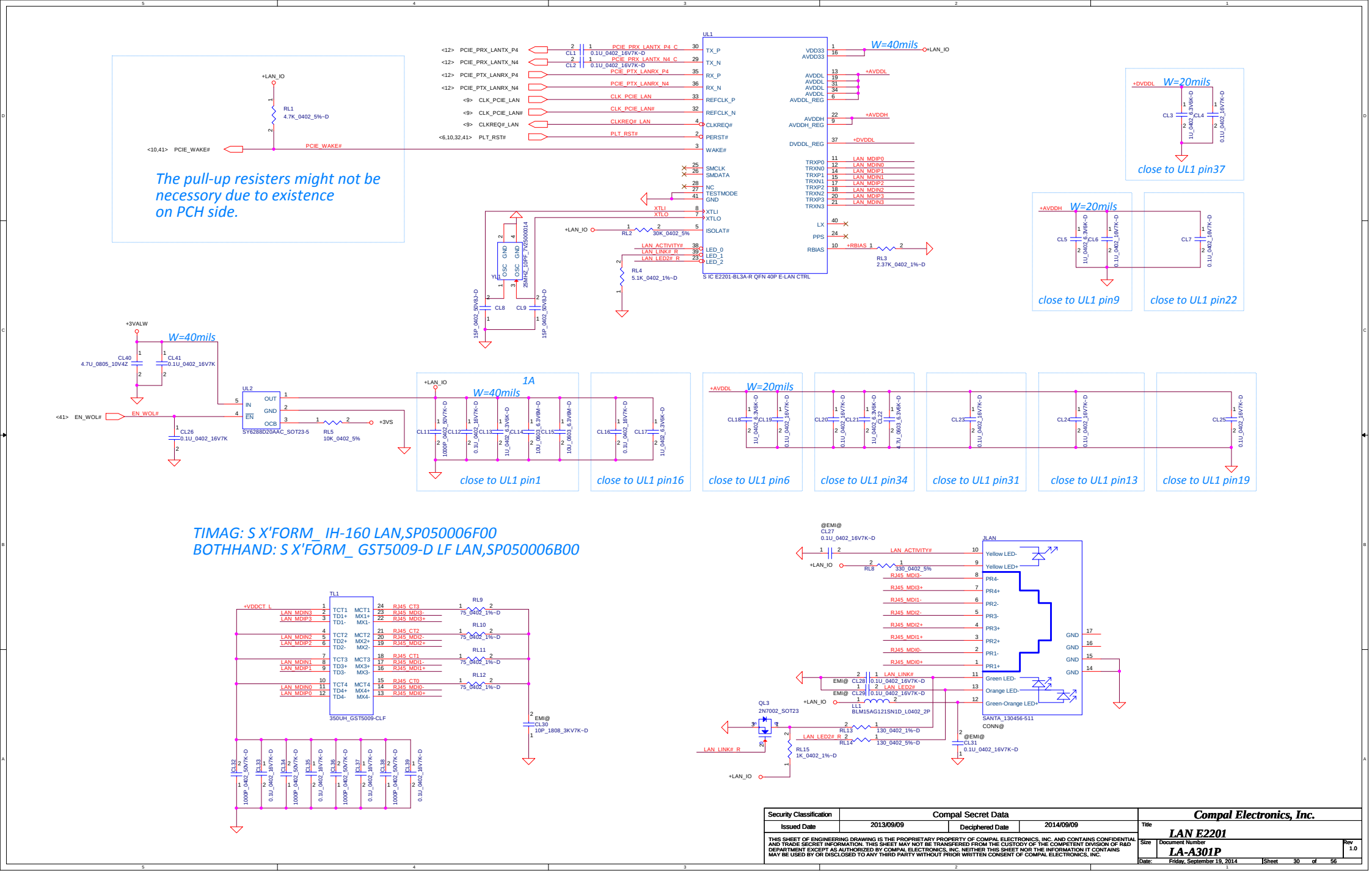
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **N15P_MISC**

Size	Document Number	Rev
Custom	LA-A301P	1.0

Date: Wednesday, September 24, 2014 | Sheet 29 of 56


The pull-up resisters might not be necessory due to existence on PCH side.
W=40mils
W=20mils
close to UL1 pin37
close to UL1 pin9
close to UL1 pin22
close to UL1 pin1
close to UL1 pin16
close to UL1 pin6
close to UL1 pin34
close to UL1 pin31
close to UL1 pin13
close to UL1 pin19
TIMAG: S X'FORM_ IH-160 LAN,SP050006F00
BOTHHAND: S X'FORM_ GST5009-D LF LAN,SP050006B00
S IC E2201-BL3A-R QFN 40P E-LAN CTRL
SY6288D20AAC_SOT23-5
350UH_GST5009-CLF
SANTA_130456-511
Security Classification
Compal Secret Data
Issued Date
2013/09/09
Deciphered Date
2014/09/09
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LAN E2201
Size
Document Number
LA-A301P
Rev
1.0
Date:
Friday, September 19, 2014
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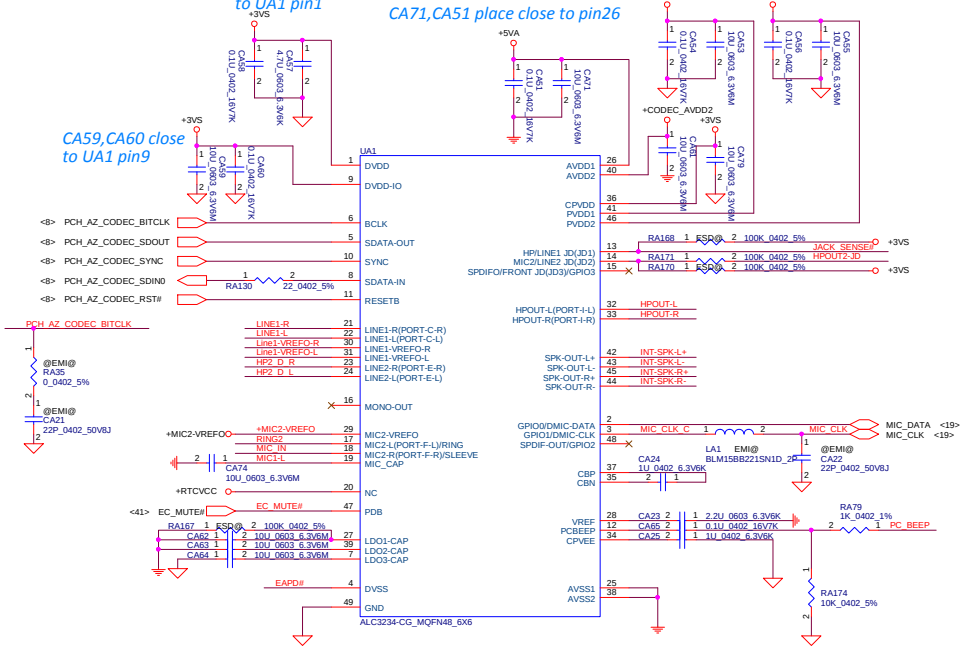
30
of
56

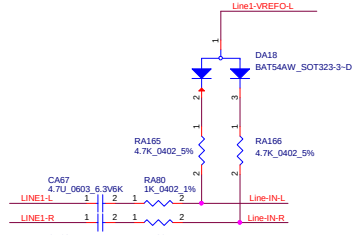
CA57,CA58 close to UA1 pin1

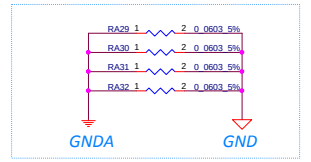
CA71,CA51 place close to pin26

CA53,CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

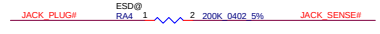
CA59,CA60 close to UA1 pin9



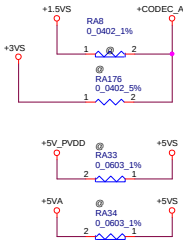




Place on the moat between GND & GNDA.

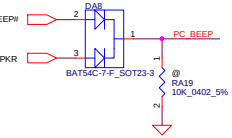


Reserve for cancel Delay circutis

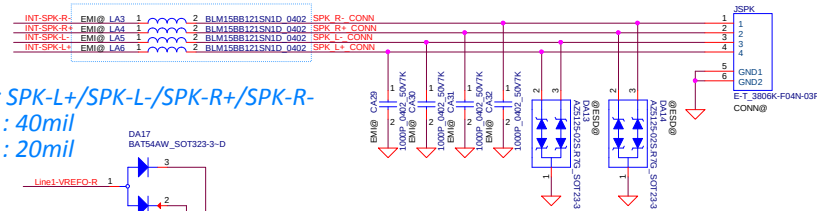


EC Beep

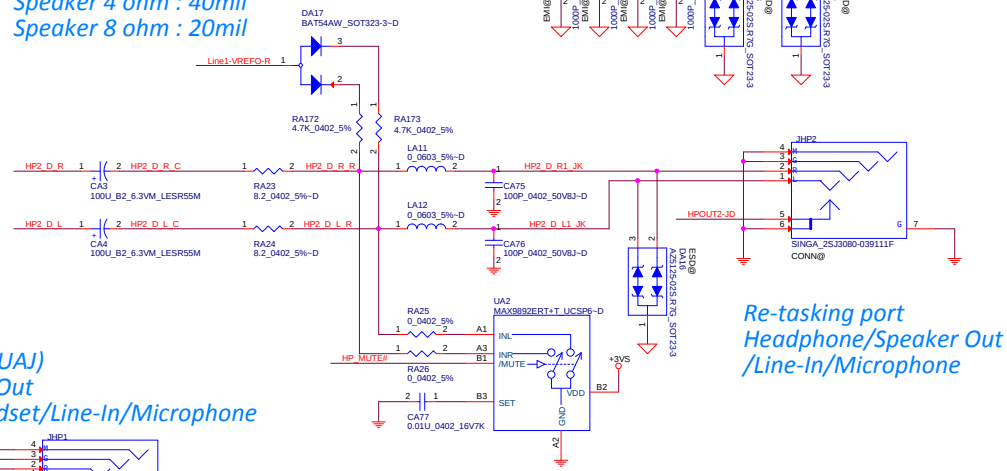
MCU Beep



Close to UA1 Pin42,43,44,45



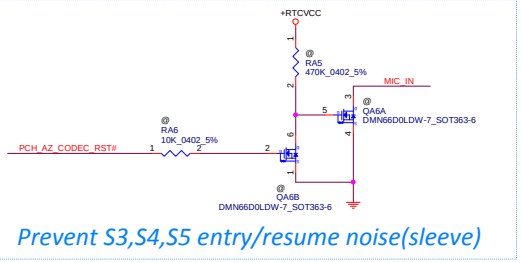
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

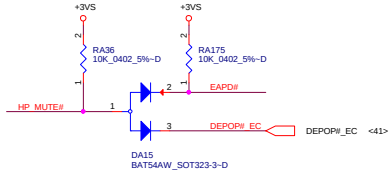


Re-tasking port
Headphone/Speaker Out
/Line-In/Microphone

Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)

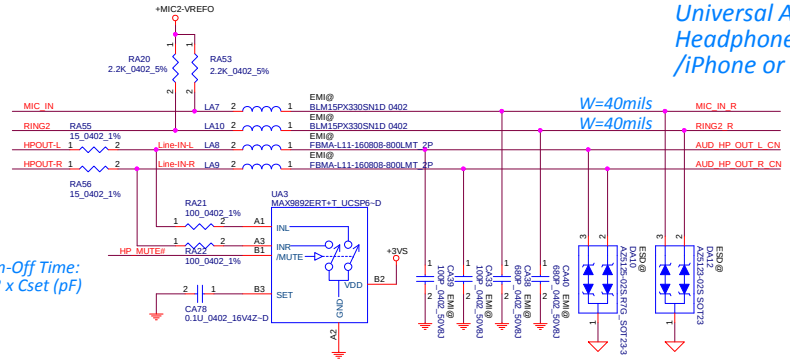
Prevent S3,S4,S5 entry/resume noise(sleeve)





Universal Audio Jack(UAJ)
Headphone/Speaker Out
/iPhone or Nokia headset/Line-In/Microphone

W=40mils
W=40mils



Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/09/30

Compal Electronics, Inc.

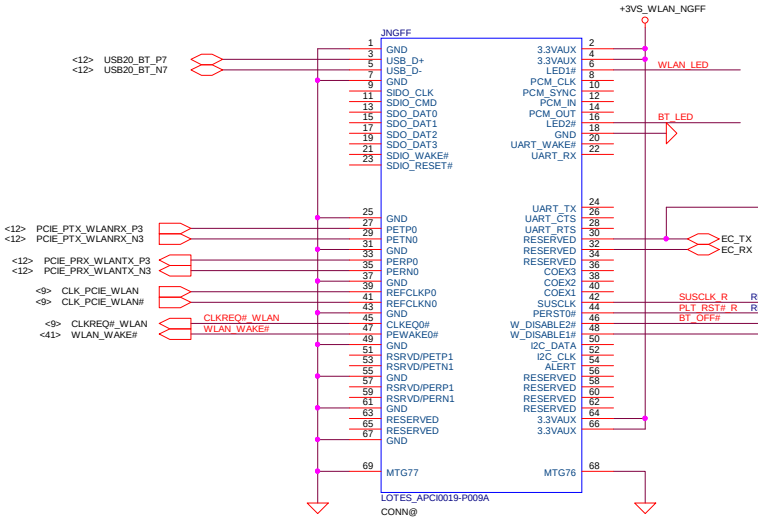
Title: Audio Codec ALC3234

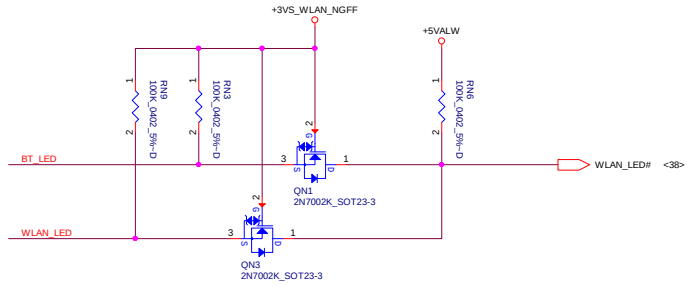
Document Number: LA-A301P

Rev: 1.0

Date: Friday, September 19, 2014 Sheet 31 of 56

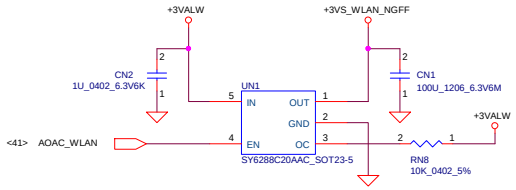
NGFF(M.2)2230 slot(E Key)



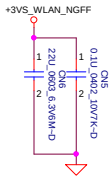


For EC to detect debug card insert.

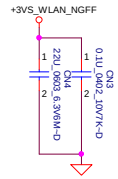
Prevent backdriver from +3VS_WLAN_NGFF to +3VS



closed to pin 2, 4



closed to pin 72,74



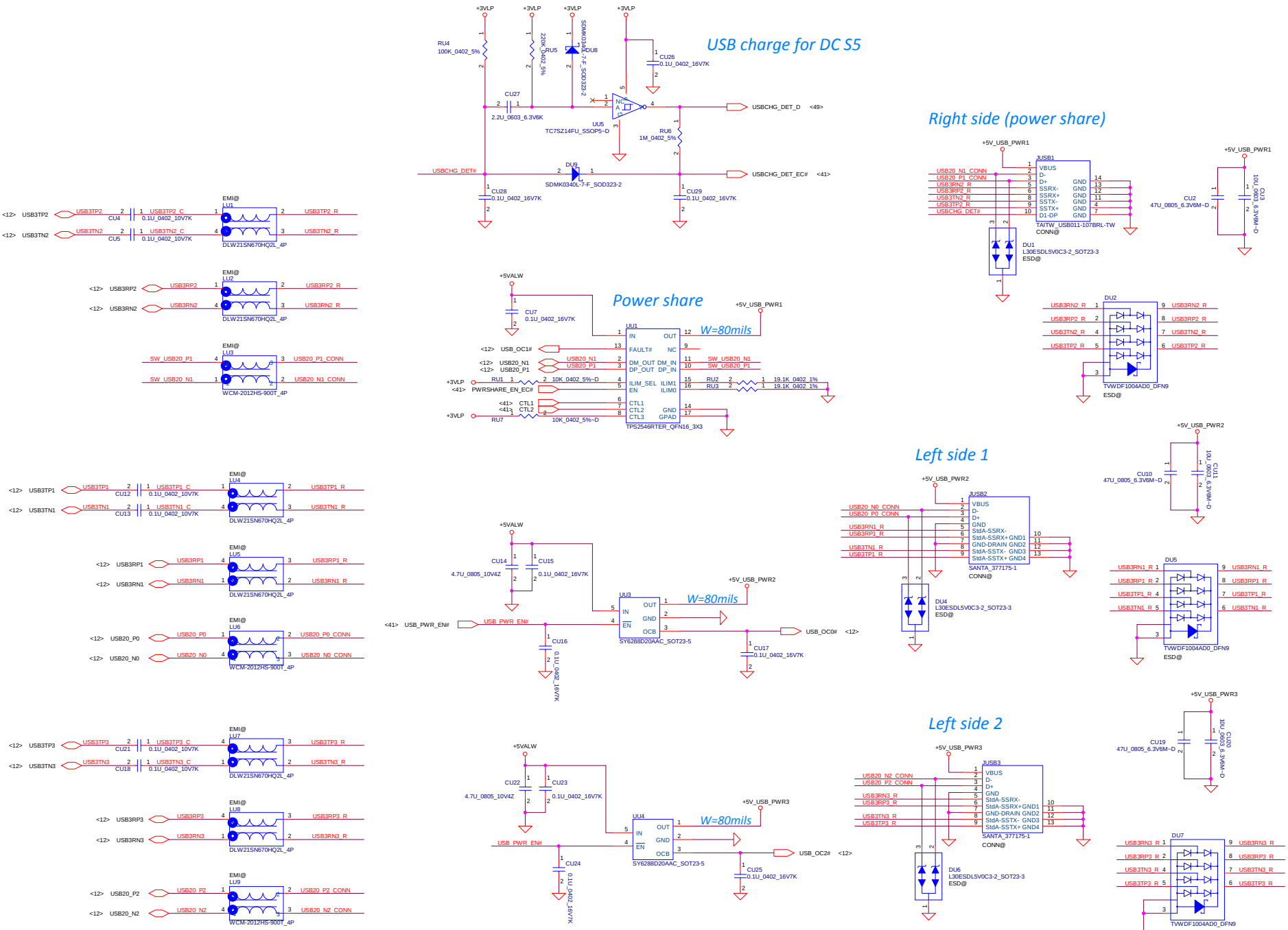
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: NGFF WLAN/BT

Size | Document Number: LA-A301P | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 32 of 56


USB charge for DC S5
Right side (power share)
Power share
Left side 1
Left side 2
W=80mils
+3VLP
+3VALW
+5V_USB_PWR1
+5V_USB_PWR2
+5V_USB_PWR3
USBCHG_DET_D
USBCHG_DET_EC#
USBCHG_DET#
USB_OC0#
USB_OC1#
USB_OC2#
USB_PWR_EN#
PWRSHARE_EN_EC#
TPS2546RTER_QFN16_3X3
SY6288D20AAC_SOT23-5
TAITW_USB011-107BRL-TW
SANTA_377175-1
TVWDF1004AD0_DFN9
DLW21SN670HQ2L_4P
WCM-2012HS-900T_4P
L30ESDL5V0C3-2_SOT23-3
SDMK0340L-7-F_SOD323-2
TC7SZ14FU_SSOP5~D
Compal Secret Data
2013/09/09
2014/09/09
Compal Electronics, Inc.
USB 3.0/2.0 x3
LA-A301P
1.0
Friday, September 19, 2014
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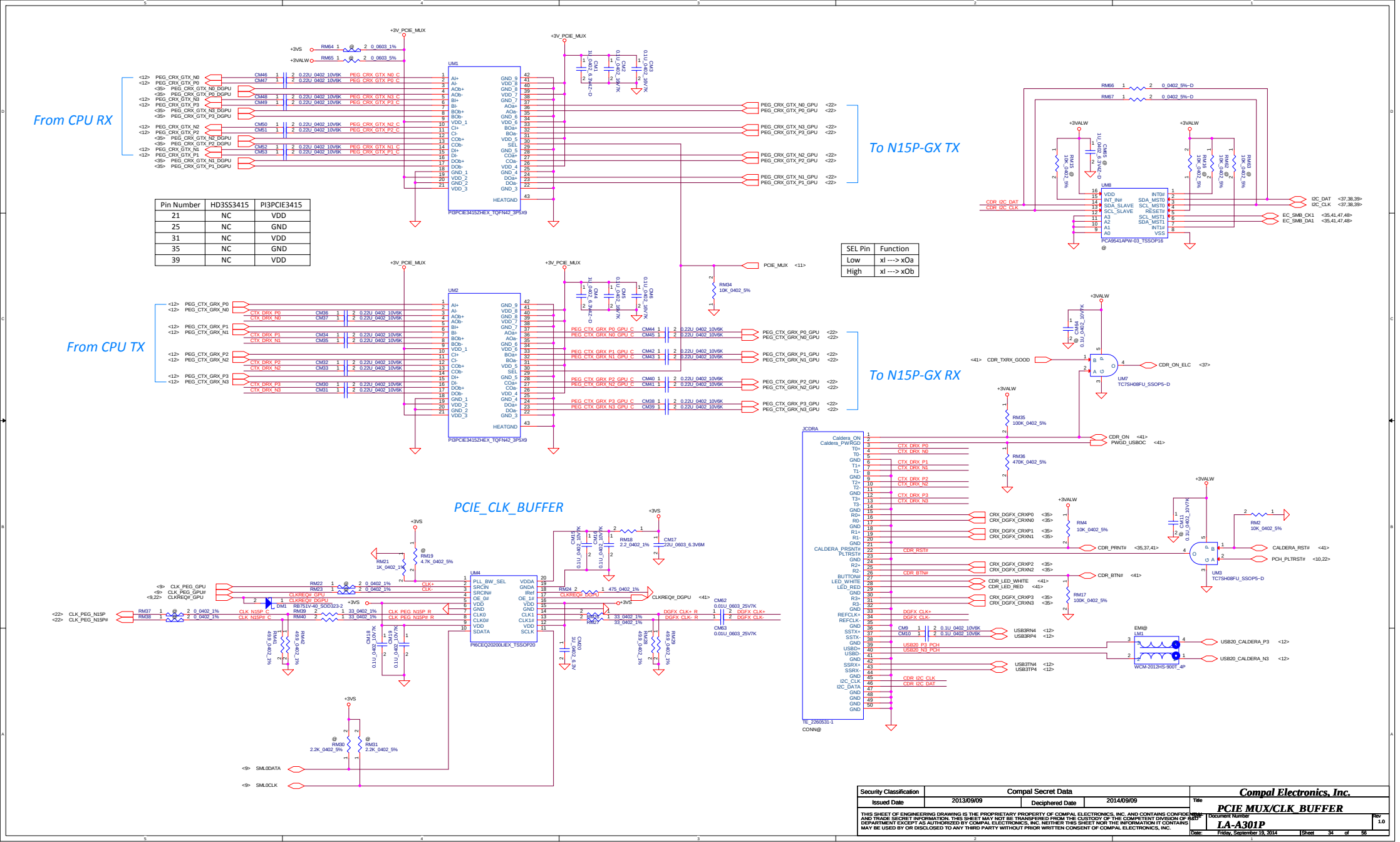

Pin Number	HD3SS3415	PI3PCIE3415
21	NC	VDD
25	NC	GND
31	NC	VDD
35	NC	GND
39	NC	VDD

SEL Pin	Function
Low	xI ---> xOa
High	xI ---> xOb

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Issued Date	2013/09/09	Deciphered Date	2014/09/09

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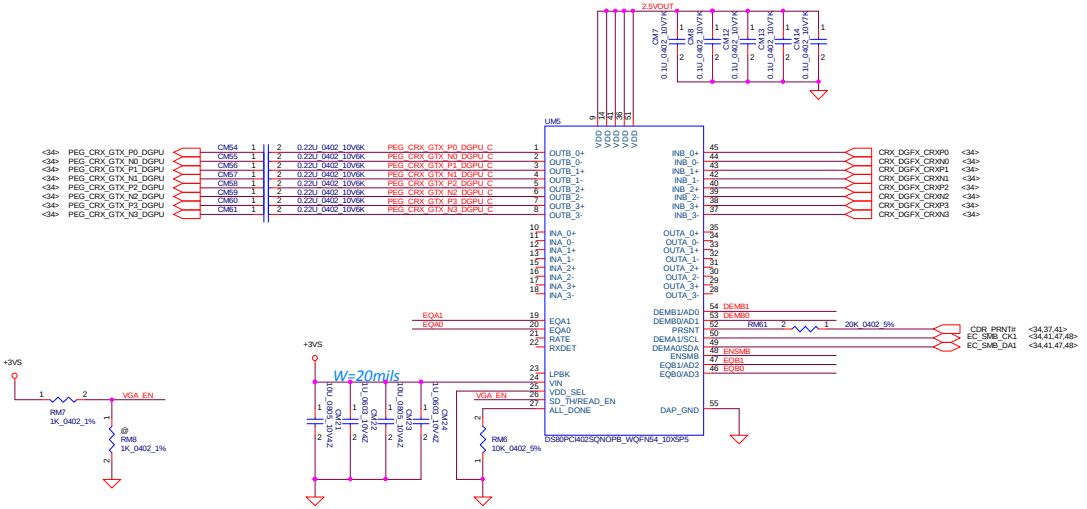
Compal Electronics, Inc.

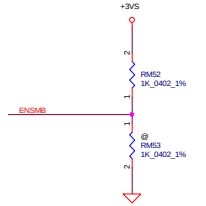
Title: PCIE MUX/CLK_BUFFER

Size: A3 | Document Number: LA-A301P | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 34 of 56



Tie 1KΩ to VDD = Register Access SMBus Slave mode
FLOAT = Read External EEPROM (Master SMBUS Mode)
Tie 1KΩ to GND = Pin Mode



EQ Settings

Level	EQA1 EQB1	EQA0 EQB0	dB at 2.5G	dB at 4G	Suggested Use
1	0	0	3.7	4.9	< 5 inch trace
2	0	R	5.8	7.9	5 inch 5–mil trace
3	0	F	7.7	9.9	5 inch 4–mil trace
4	R	1	8.9	11	10 inch 5–mil trace
5	R	0	11.2	14.3	10 inch 4–mil trace
6	R	R	11.4	14.6	15 inch 4–mil trace
7	R	F	13.5	17	20 inch 4–mil trace
8	R	1	15	18.5	25 to 30 inch 4–mil trace
9	F	0	12.8	18	30 inch 4–mil trace
10	F	R	17.4	22	35 inch 4–mil trace
11	F	F	19.7	24.4	10m, 30awg cable
12	F	1	21.1	25.8	
13	1	0	21.7	27.4	
14	1	R	23.5	29.0	10m – 12m cable
15	1	F	25.8	31.4	
16	1	1	27.3	32.7	

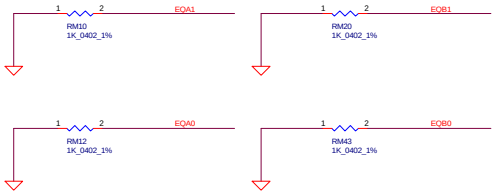
DEMA Settings

Level	DEMA1 DEMB1	DEMA0 DEMB0	DEM dB	Suggested Use
1	0	0	0	<5 inch 4–mil trace
2	0	R	0	<5 inch 4–mil trace
3	0	F	-3.5	10 inch 4–mil trace
4	0	1	0	<5 inch 4–mil trace
5	R	0	-3.5	10 inch 4–mil trace
6	R	R	-6	15 inch 4–mil trace
7	R	F	0	<5 inch 4–mil trace
8	R	1	-3.5	10 inch 4–mil trace
9	F	0	-6	15 inch 4–mil trace
10	F	R	0	<5 inch 4–mil trace
11	F	F	-3.5	10 inch 4–mil trace
12	F	1	-6	15 inch 4–mil trace
13	1	0	0	<5 inch 4–mil trace
14	1	R	-3.5	10 inch 4–mil trace
15	1	F	-6	15 inch 4–mil trace
16	1	1	-9	20 inch 4–mil trace

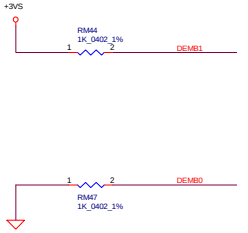
Level control Settings

Level	Pin Setting	Description	Suggested Use
1	0	1kΩ to GND	<5 inch 4–mil trace
2	R	20kΩ to GND	<5 inch 4–mil trace
3	F	Float	10 inch 4–mil trace
4	1	1kΩ to VDD	<5 inch 4–mil trace

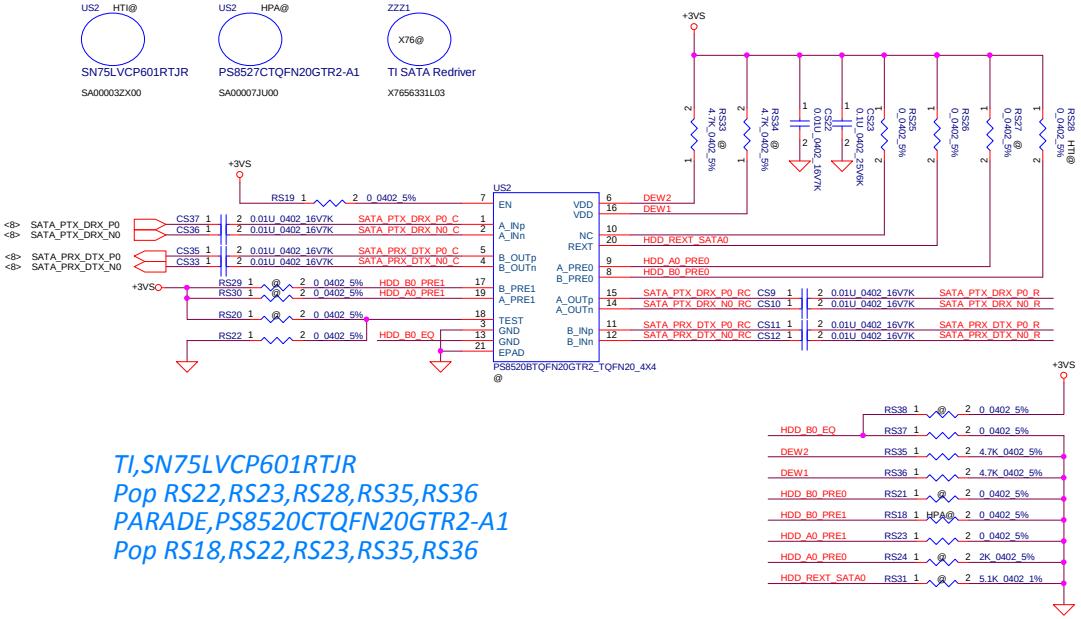
EQ*MB



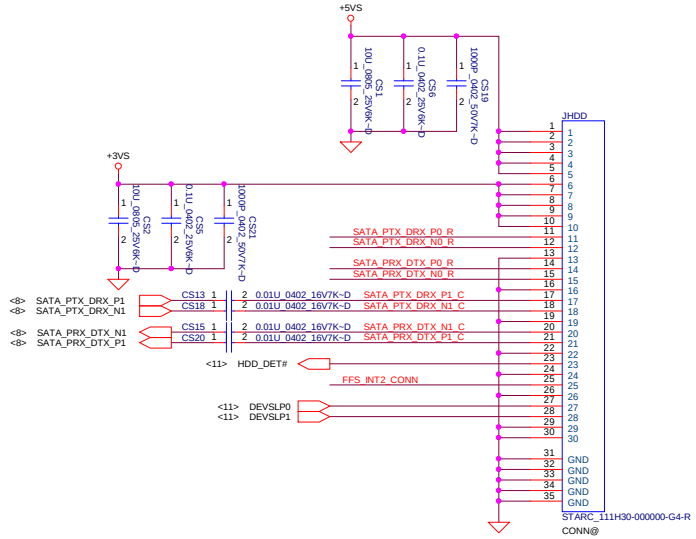
DEM*EGPU

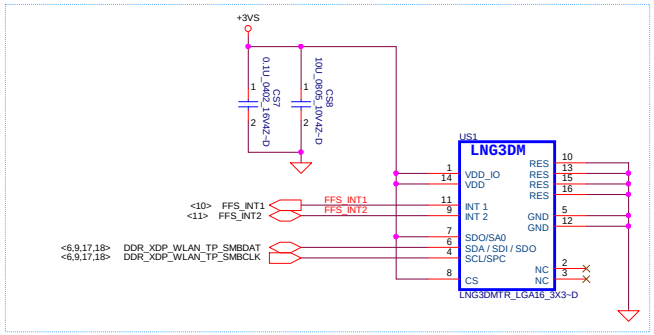


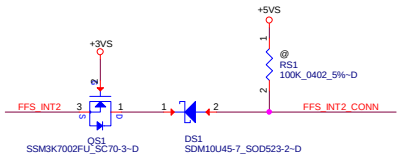
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date 2014/09/09	Title: PCIE re-driver
			Size: Document Number: LA-A301P Rev: 1.0
			Date: Friday, September 19, 2014 Sheet 35 of 56



TI,SN75LVCP601RTJR
Pop RS22,RS23,RS28,RS35,RS36
PARADE,PS8520CTQFN20GTR2-A1
Pop RS18,RS22,RS23,RS35,RS36







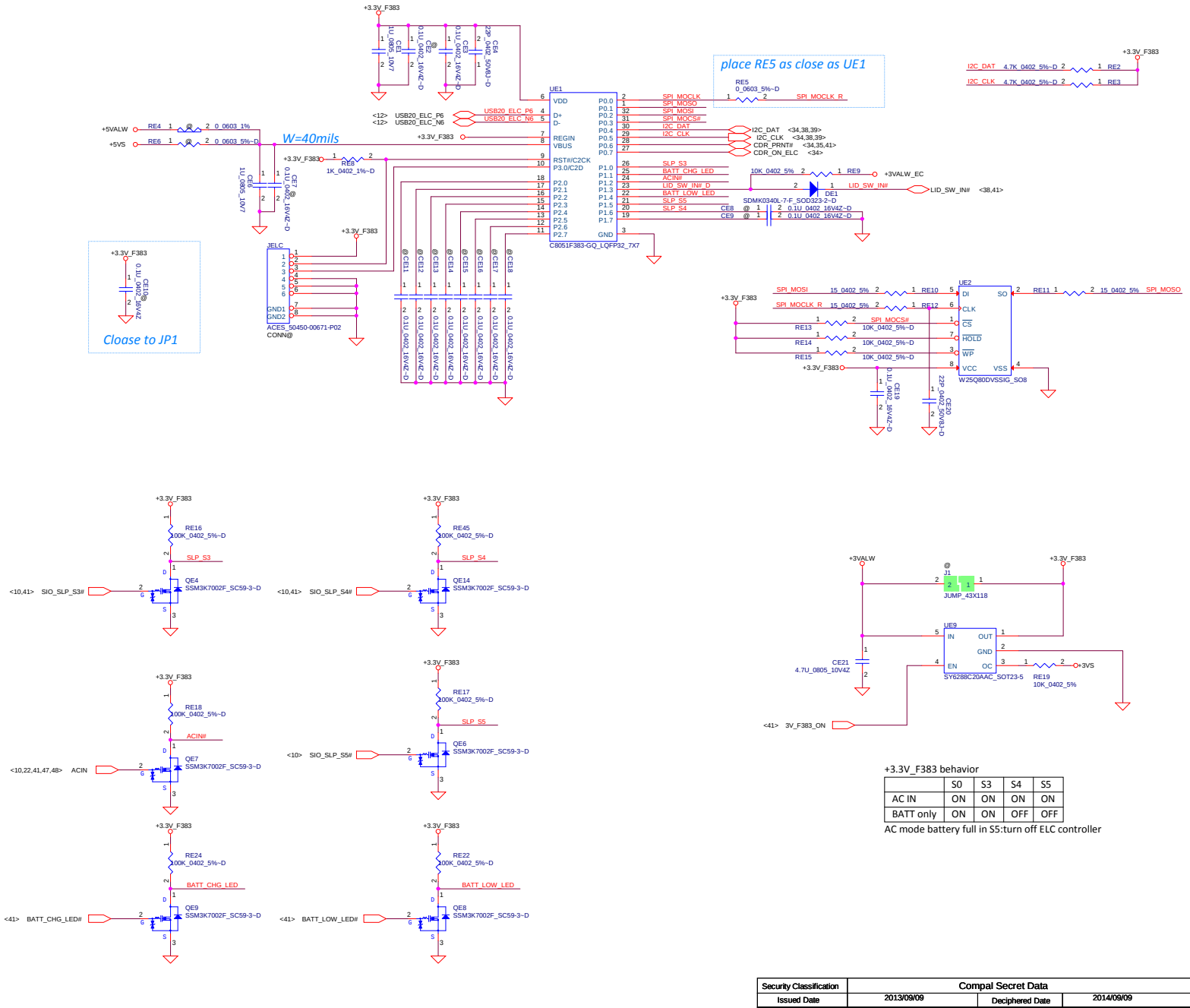
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: *SATA HDD/M2 cards*

Size | Document Number: *LA-A301P* | Rev: 1.0

Date: Wednesday, September 24, 2014 | Sheet 36 of 56



	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BATT only	ON	ON	OFF	OFF

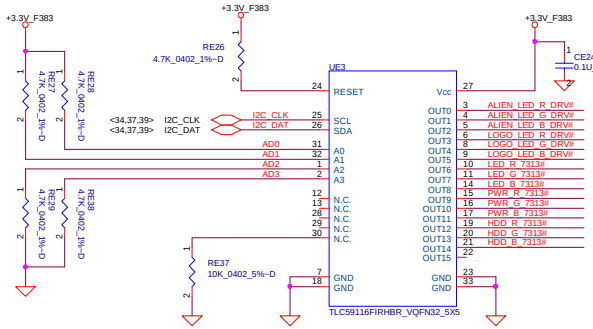
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

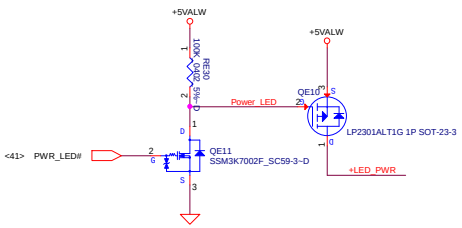
Title: ELC (1)C8051F383

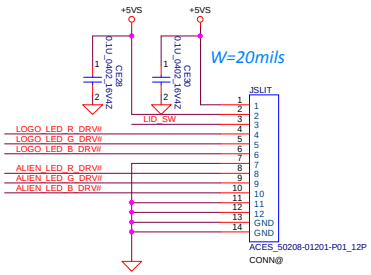
Size: Custom | Document Number: LA-A301P | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 37 of 56

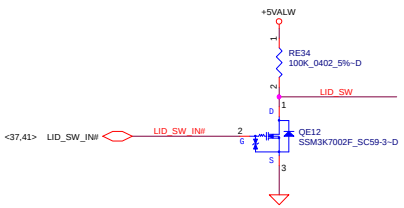


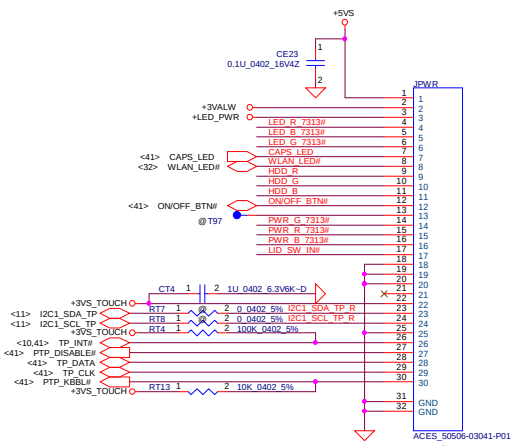
Power LED





Logic up LED board

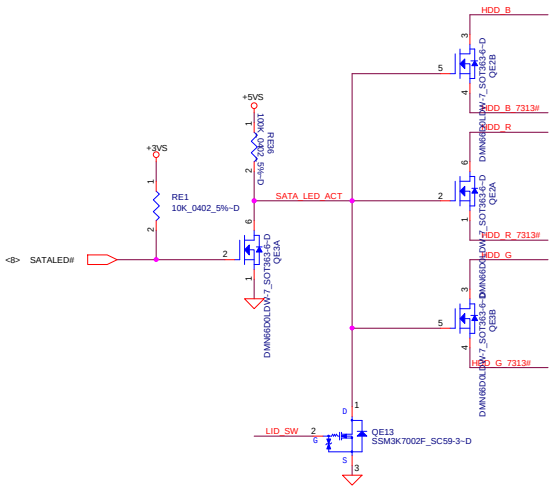


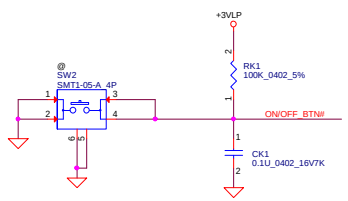


PTP pin define

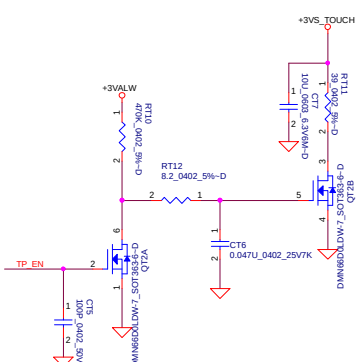
VDD
I2C_DATA
I2C_CLK
GND
ATTN
PTP_DISABLE#(CLOSE LID)
PS2_DATA
PS2_CLK
PTP_KBBL#(KB BL)
NC

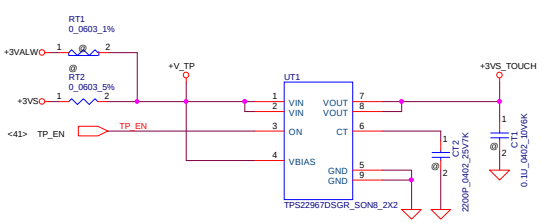
Logic low LED board



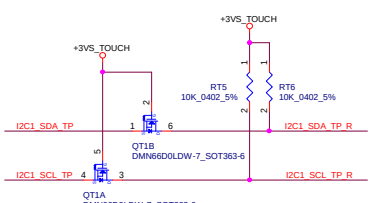


ON/OFF switch power button
Bottom Side pop only before MP





APE8937(SA000070L00)
TPS22967(SA000070S00)



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.	
Title	ELC (2)PTP/PWR SW
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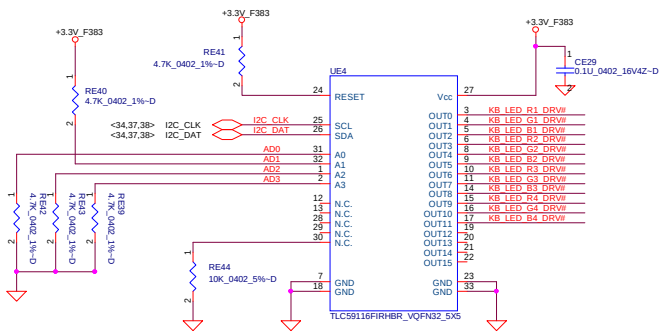
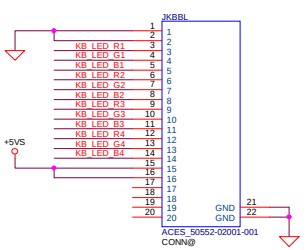
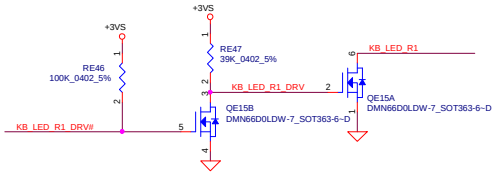
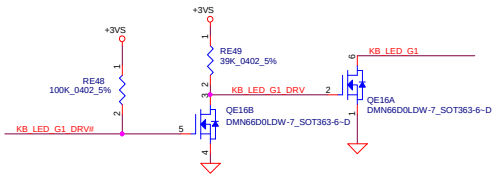
I2C address

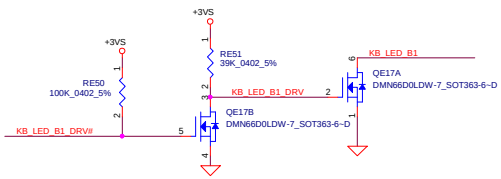
	A3	A2	A1	A0
UE1 (sheet 10 in Caldera board)	0	0	0	1
UE4 (sheet 39)	0	0	1	0
UE3 (sheet 38)	0	0	1	1
3rd LED drive (reserve)	0	1	0	0

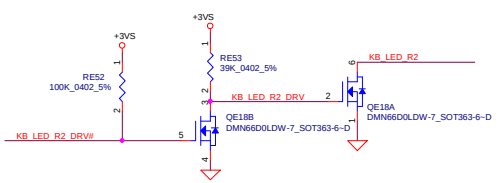


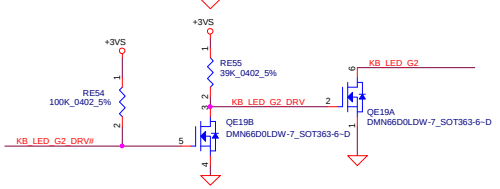


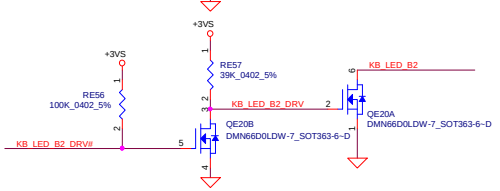


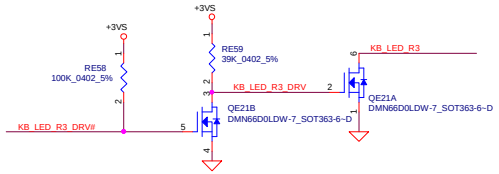


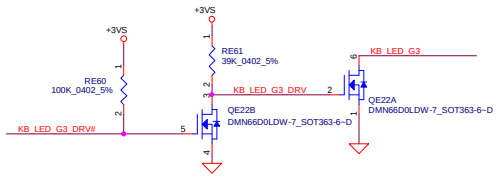


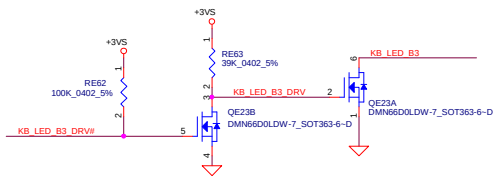


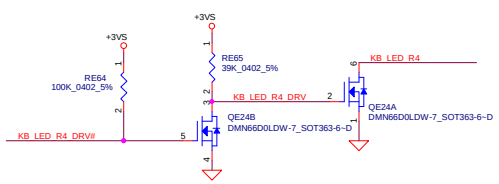


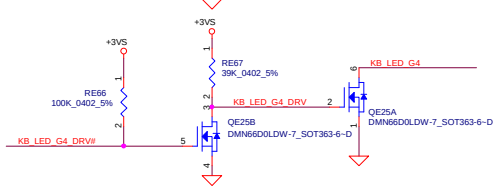


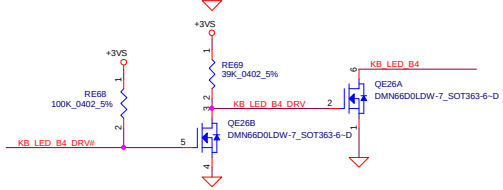












Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

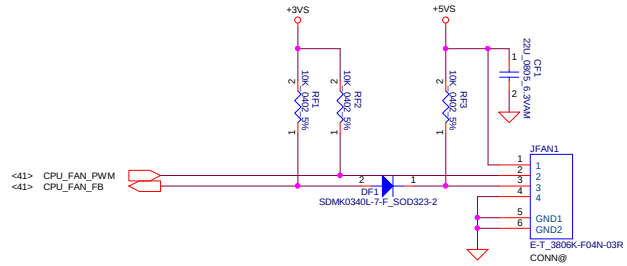
Compal Electronics, Inc.

Title: ELC (3)KBBL

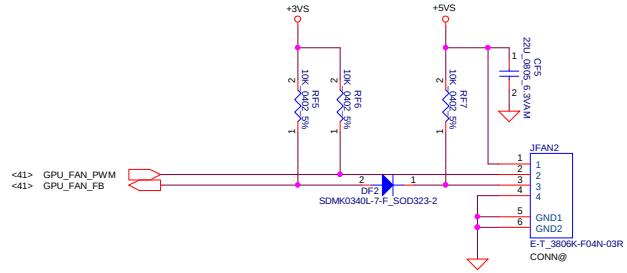
Size: Custom | Document Number: LA-A301P | Rev: 1.0

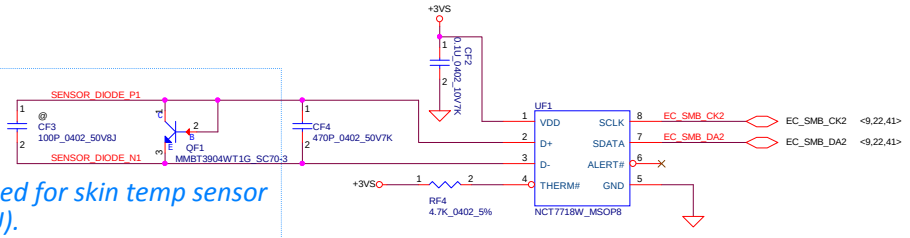
Date: Friday, September 19, 2014 | Sheet 39 of 56

CPU FAN control circuit

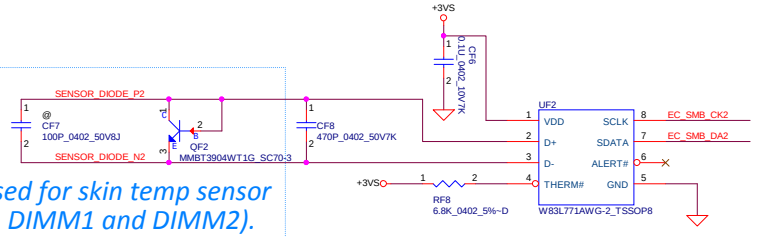


GPU FAN control circuit





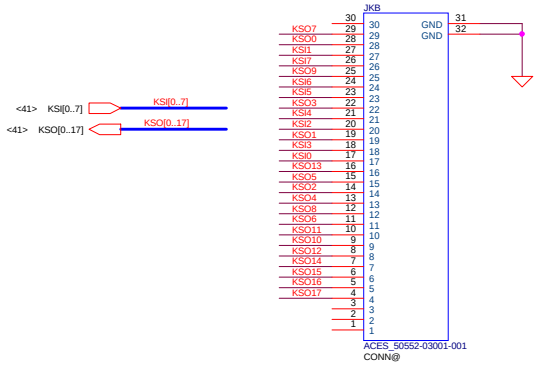
Diode circuit s used for skin temp sensor (placed near CPU).
Place CF3 close to QF1 as possible.



Diode circuit s used for skin temp sensor (placed between DIMM1 and DIMM2).
Place CF7 close to QF2 as possible.

UF1
NCT7718W(SA000067P00)Address:1001_100xb(0x98h)
ADM1032ARMZ-REEL(SA010320110)Address:100_1100(0x4C)
UF2
W83L771AWG-2(SA00003PU00)Address:1001_101xb(0x9Ah)
ADM1032ARMZ-2R(SA010320120)Address:100_1101(0x4D)

INT_KBD Connector



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2014/09/09	Title: FAN/KB/Thermal sensor
				Size: Document Number: LA-A301P Rev: 1.0
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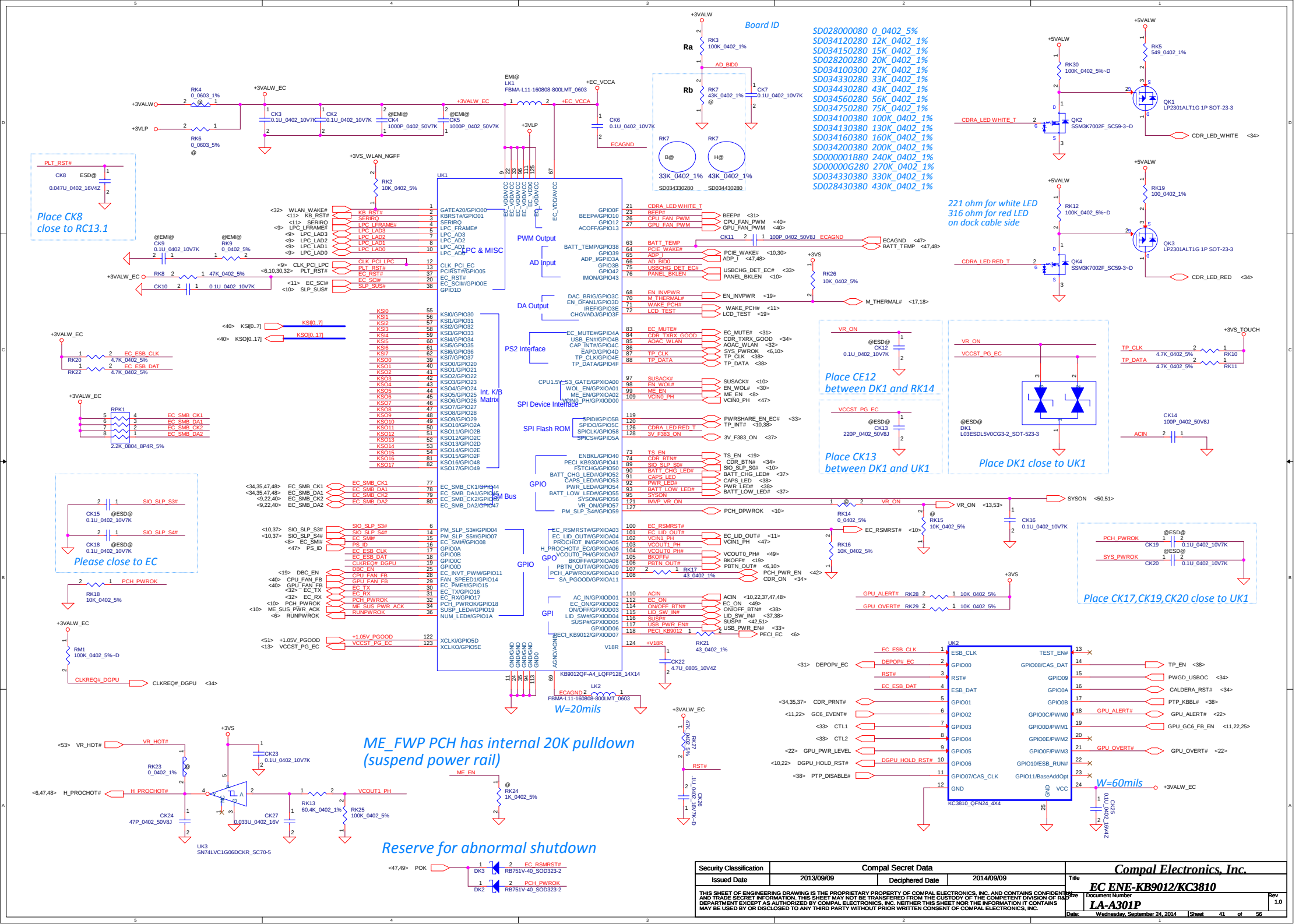

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Issued Date	2013/09/09	Deciphered Date	2014/09/09

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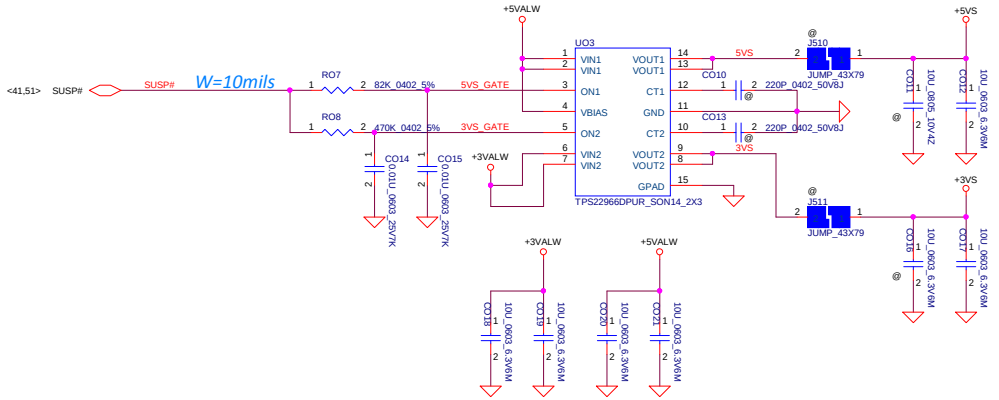
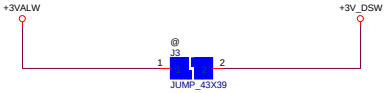
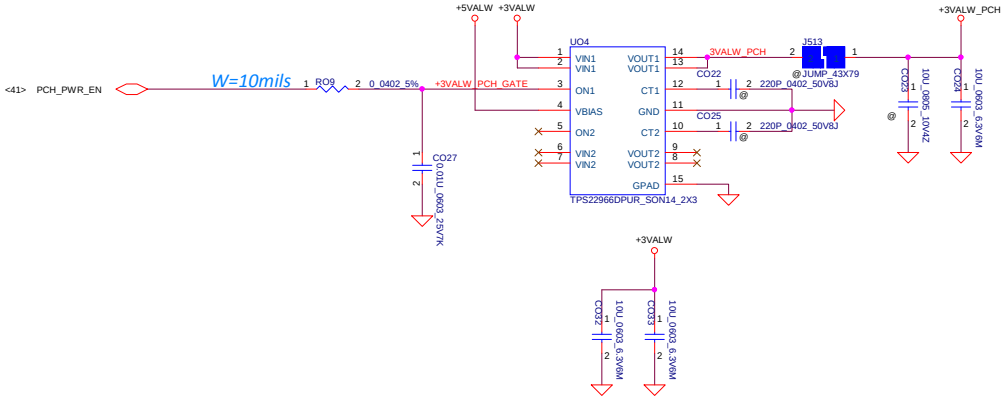
+5VS and +3VS switch

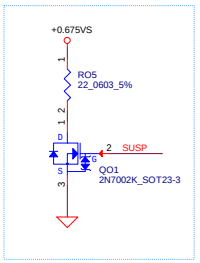


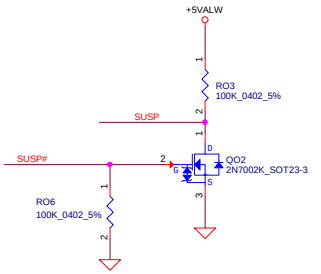
+3VALW TO +3V_DSW



+3VALW_PCH switch







For Intel S3 power reduction

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

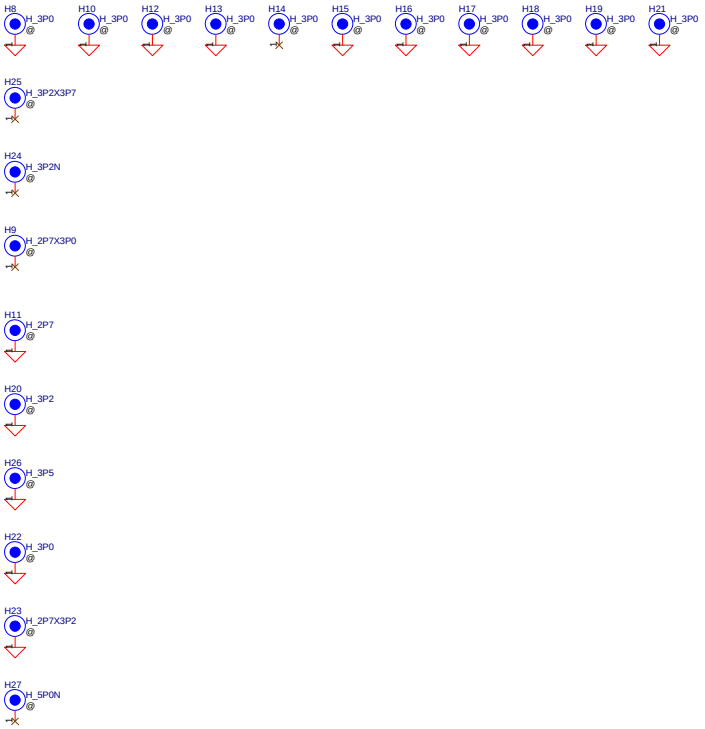
Compal Electronics, Inc.

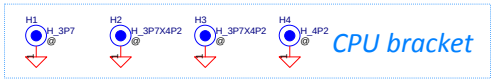
Title: **DC/DC Interface**

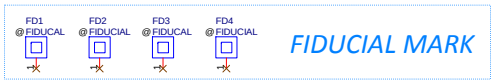
Size | Document Number: **LA-A301P** | Rev: 1.0

Date: Monday, September 22, 2014 | Sheet 42 of 56

Screw Hole







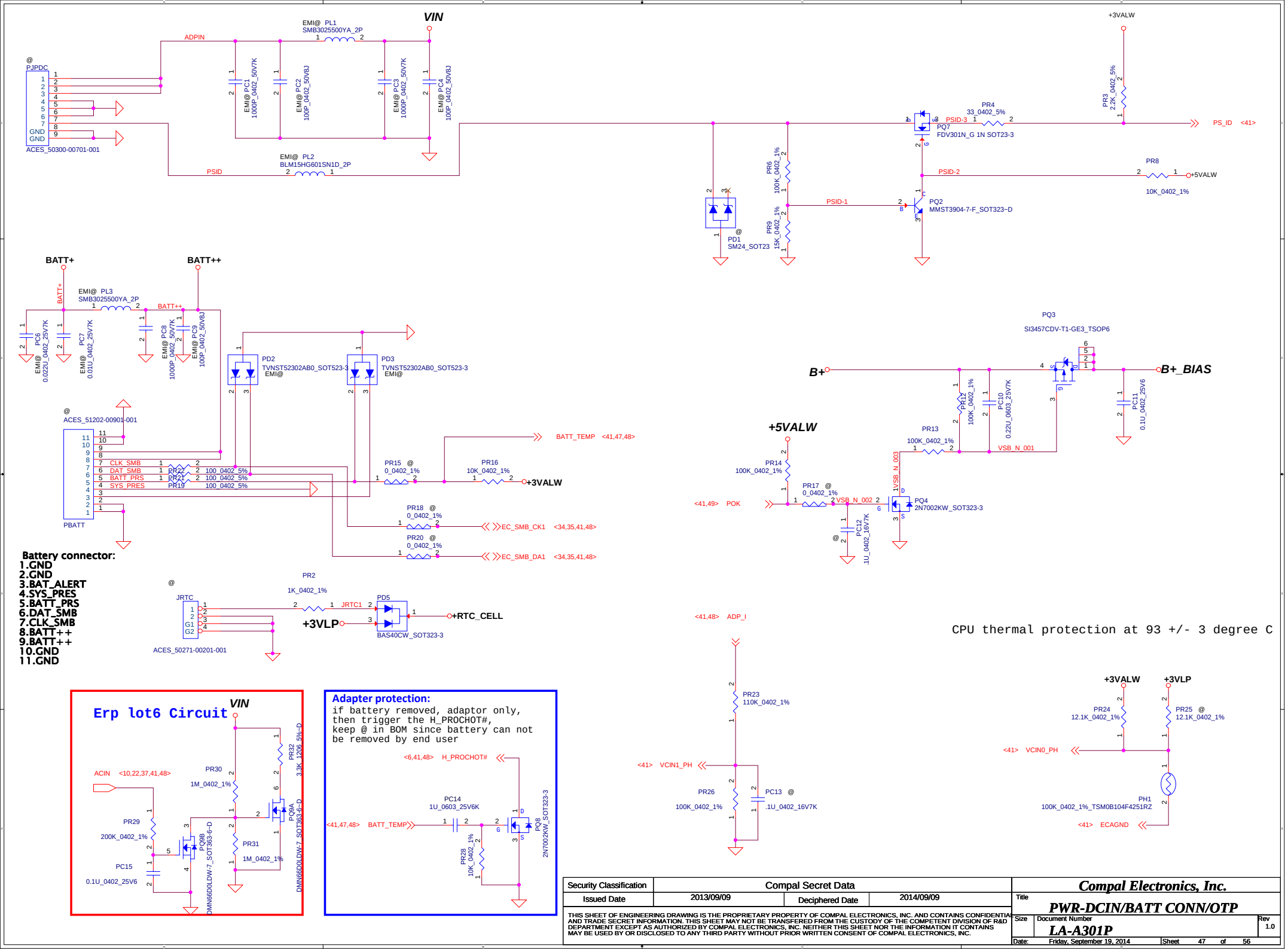
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **Screw Hole**

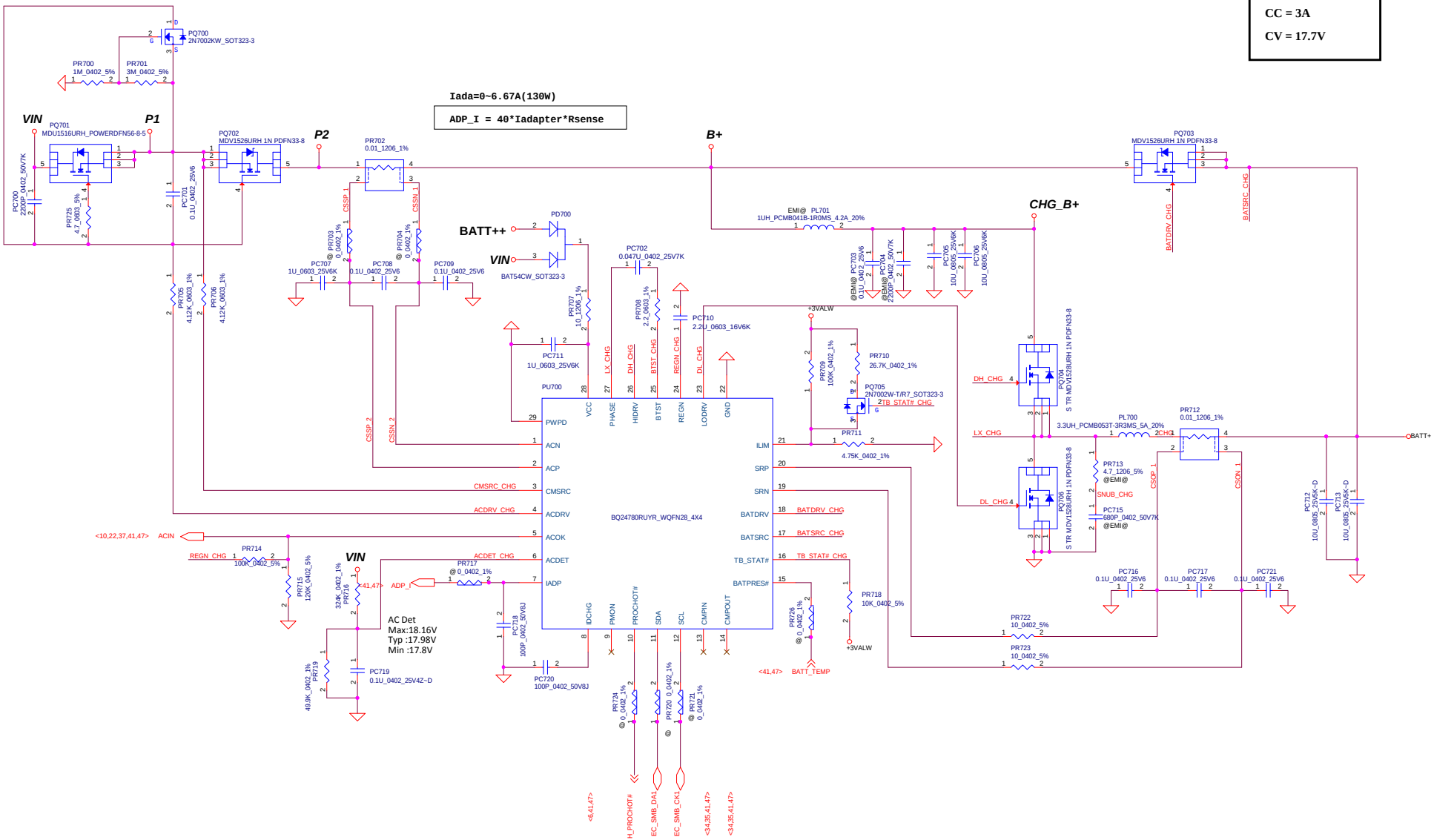
Size | Document Number: **LA-A301P** | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 43 of 56



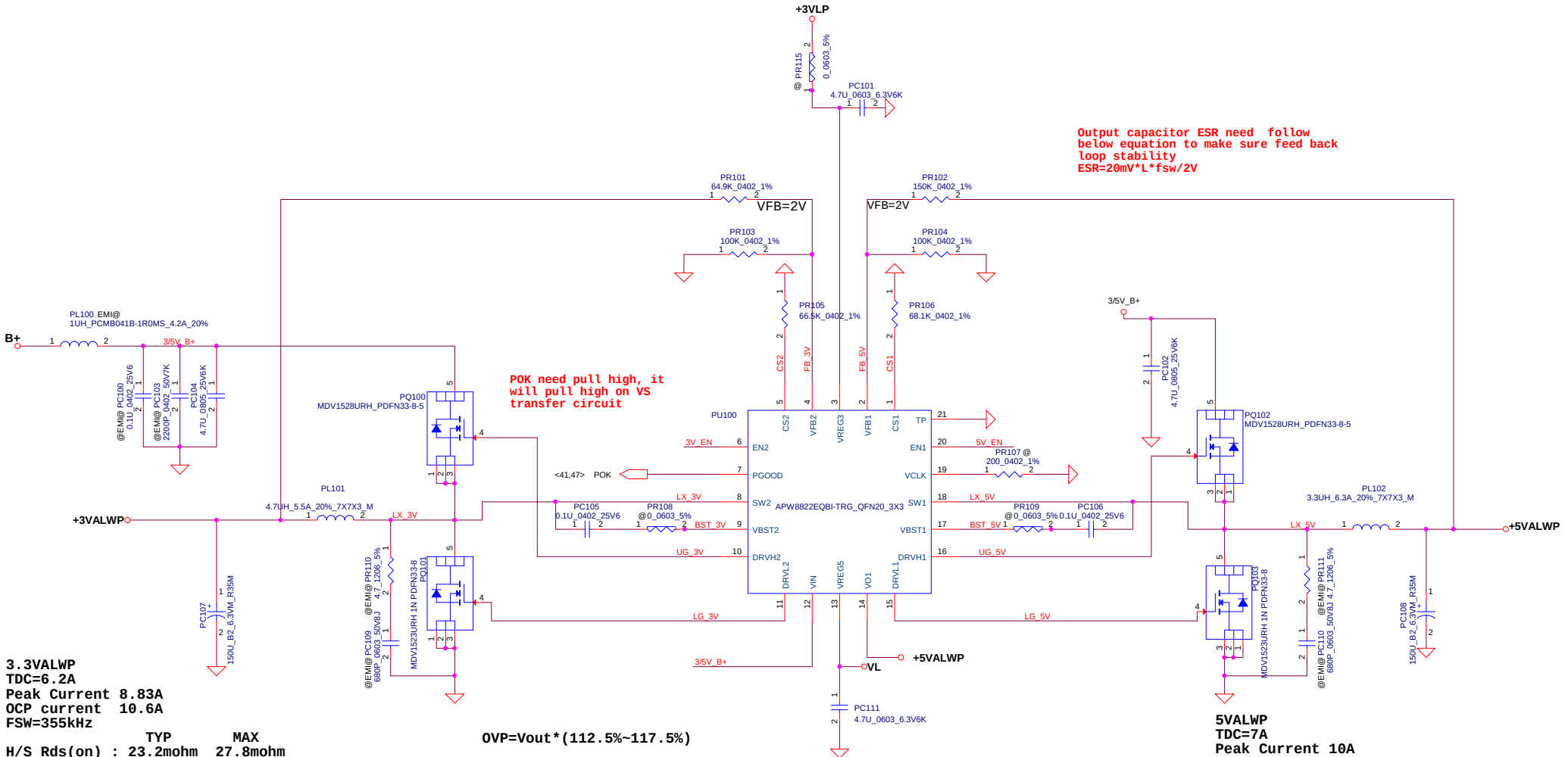
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.			
Title	PWR-DCIN/BATT CONN/OTP		
Size	Document Number LA-A301P		Rev 1.0
Date: Friday, September 19, 2014	Sheet 47 of 56		



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.			
Title: PWR-Charger			
Size	Document Number: LA-A301P		Rev: 1.0
Date: Friday, September 19, 2014	Sheet 48 of 56		



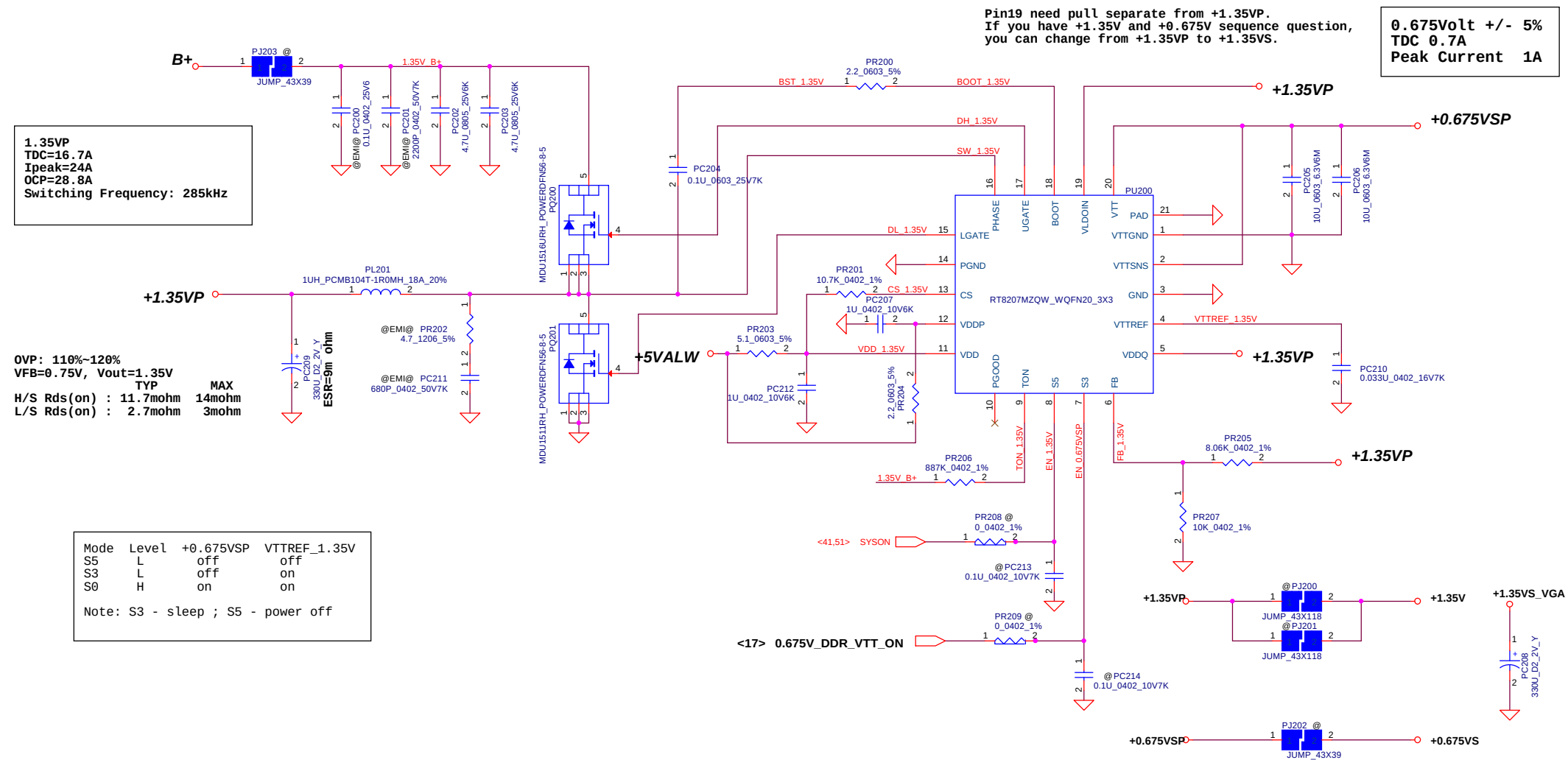
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: B | Document Number: LA-A301P | Rev: 1.0

Date: Friday, September 19, 2014 | Sheet 49 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **PWR-1.35VP/0.675VSP**

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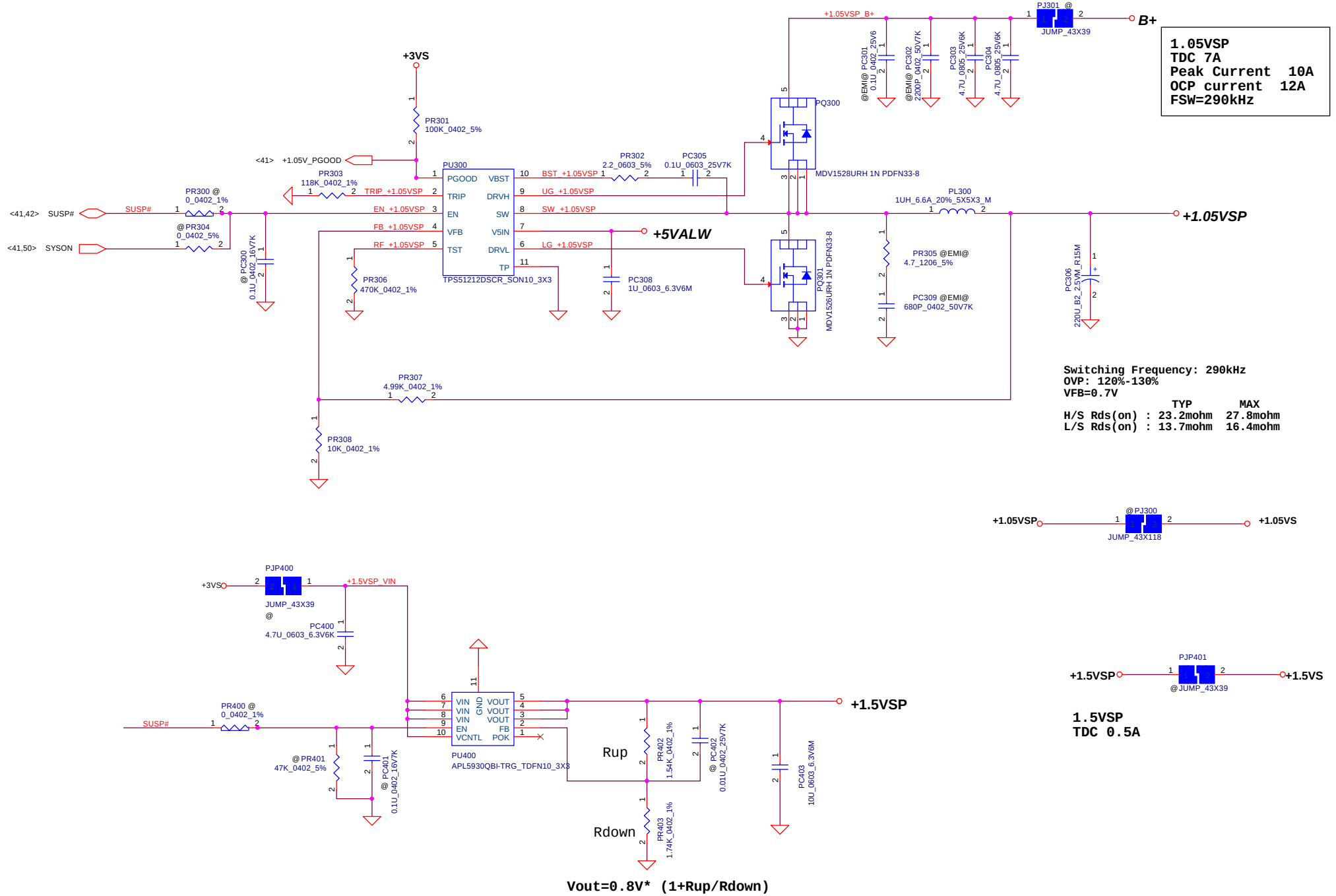
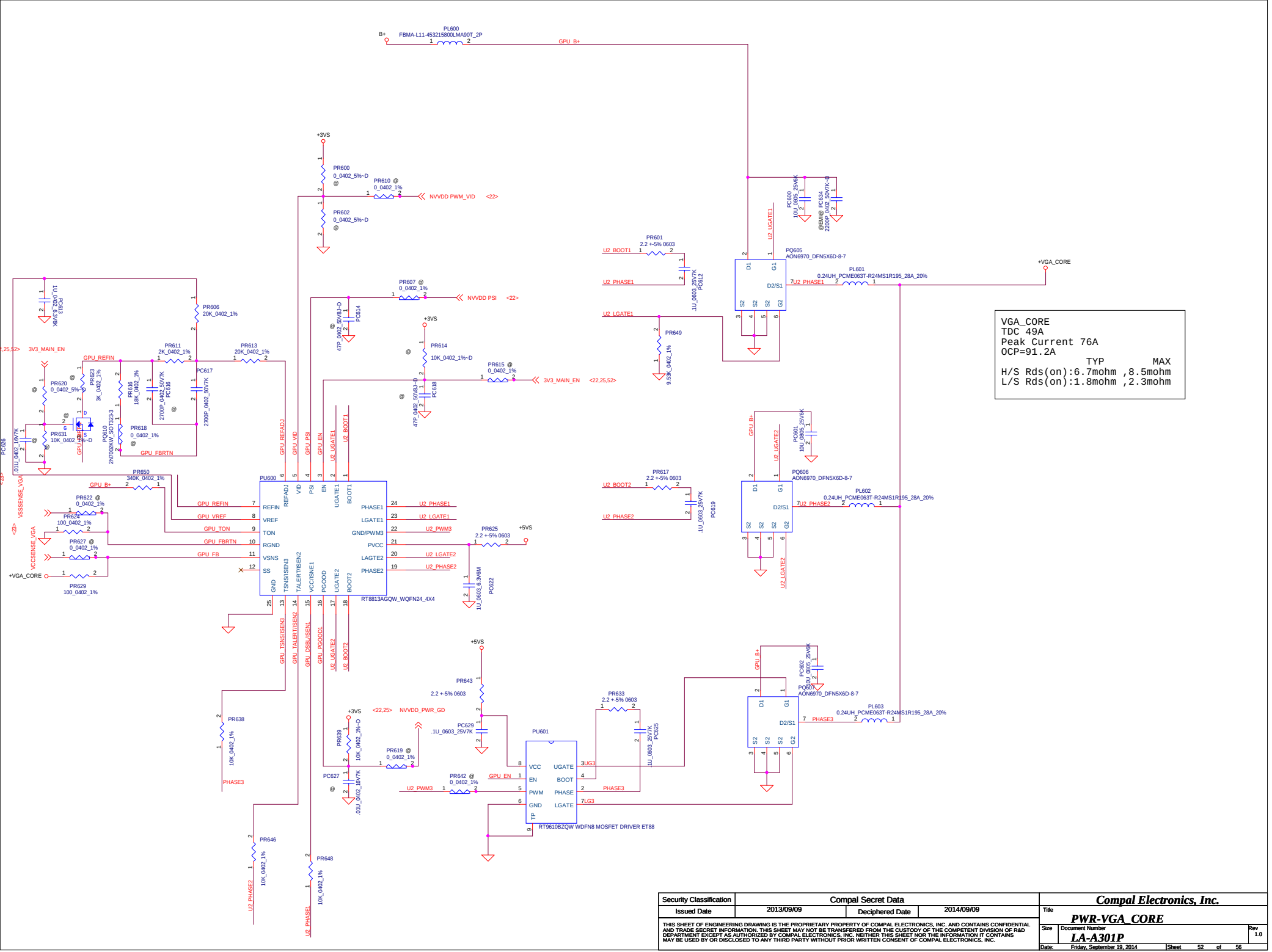
Date: Friday, September 19, 2014 Sheet 50 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.			
Title: PWR-1.05VSP/1.5VSP			
Size	Document Number: LA-A301P		Rev: 1.0
Date: Friday, September 19, 2014	Sheet 51 of 56		



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Issued Date	2013/09/09	Deciphered Date	2014/09/09

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Title: **PWR-VGA_CORE**

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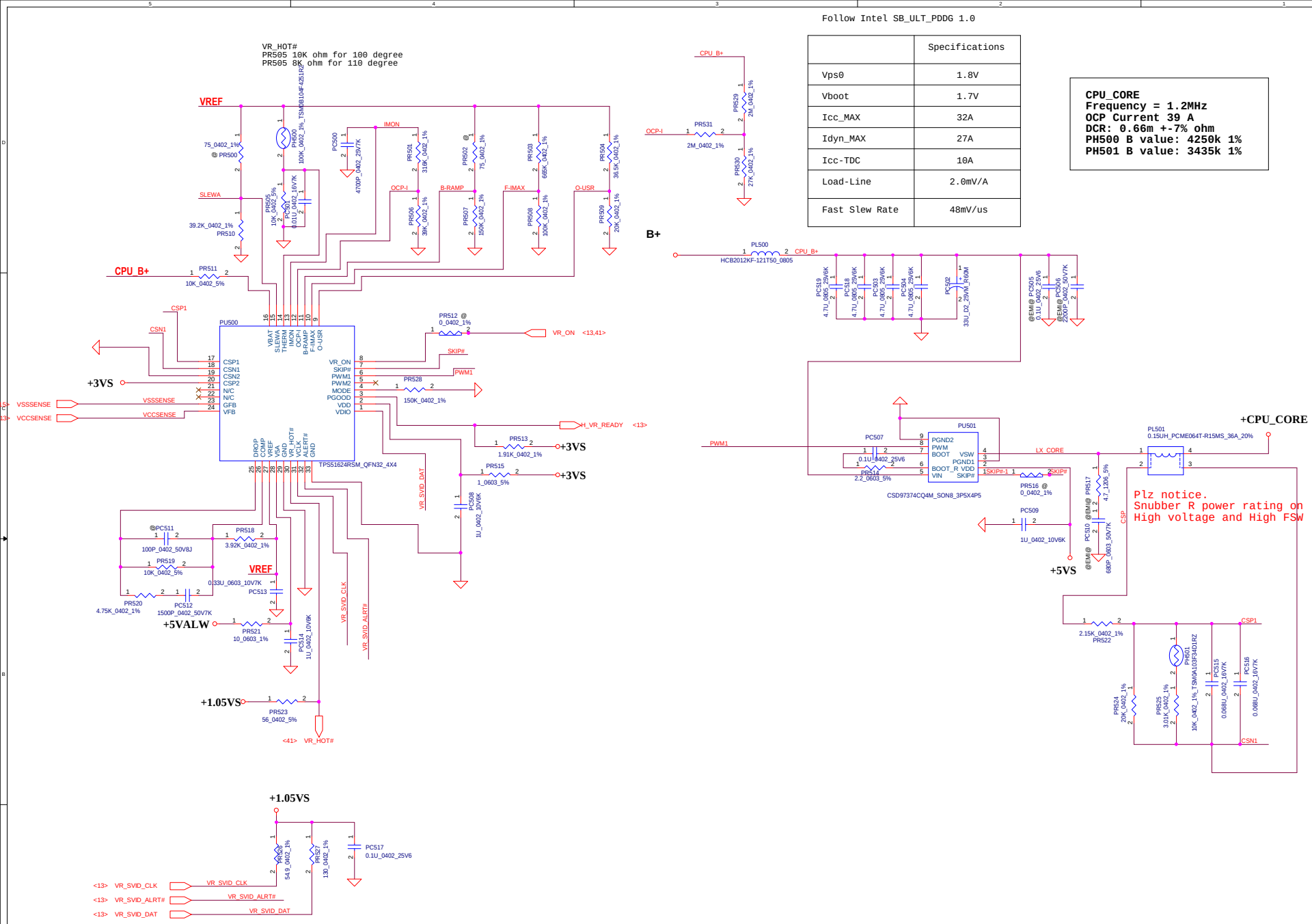
Follow Intel SB_ULT_PDDG 1.0

	Specifications
Vps0	1.8V
Vboot	1.7V
Icc_MAX	32A
Idyn_MAX	27A
Icc-TDC	10A
Load-Line	2.0mV/A
Fast Slew Rate	48mV/us

CPU_CORE
Frequency = 1.2MHz
OCP Current 39 A
DCR: 0.66m +-7% ohm
PH500 B value: 4250k 1%
PH501 B value: 3435k 1%

VR_HOT#
PR505 10K ohm for 100 degree
PR505 8K ohm for 110 degree



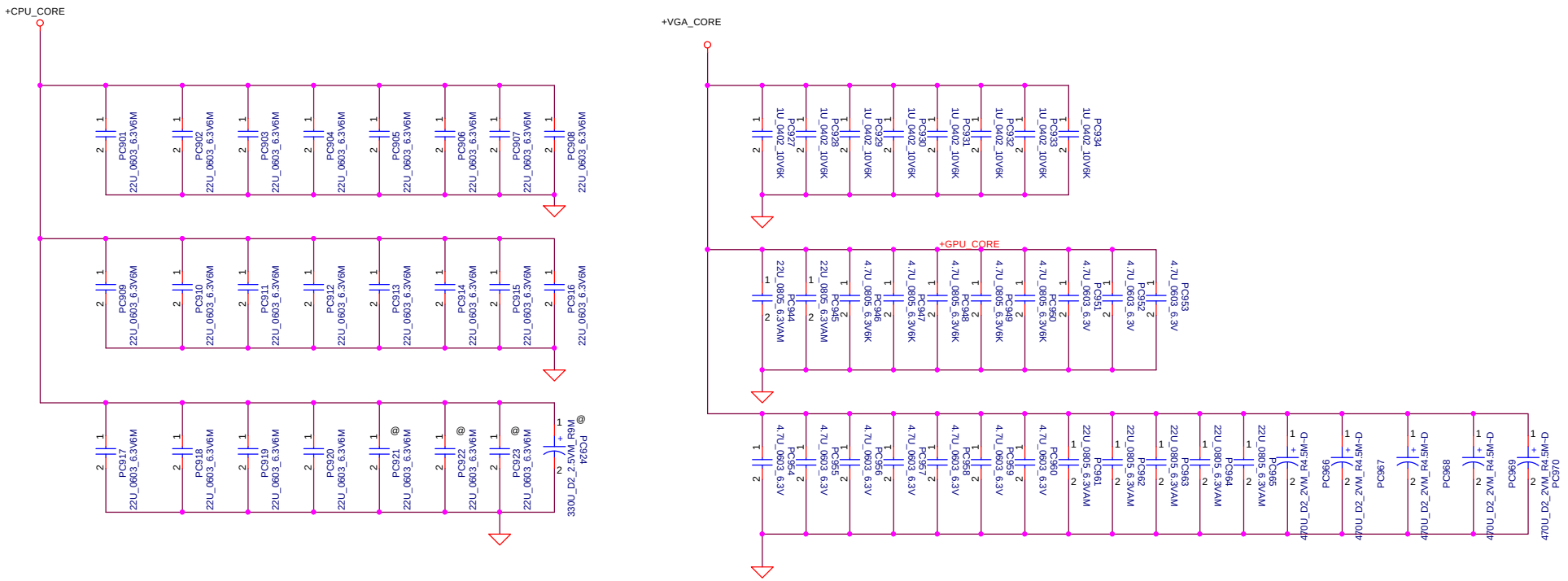
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

Size	Document Number	Rev
	LA-A301P	1.0

Date: Friday, September 19, 2014 Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2014/09/09

Compal Electronics, Inc.

Title: **PWR-PROCESSOR DECOUPLING**

Size	Document Number	Rev
	LA-A301P	1.0

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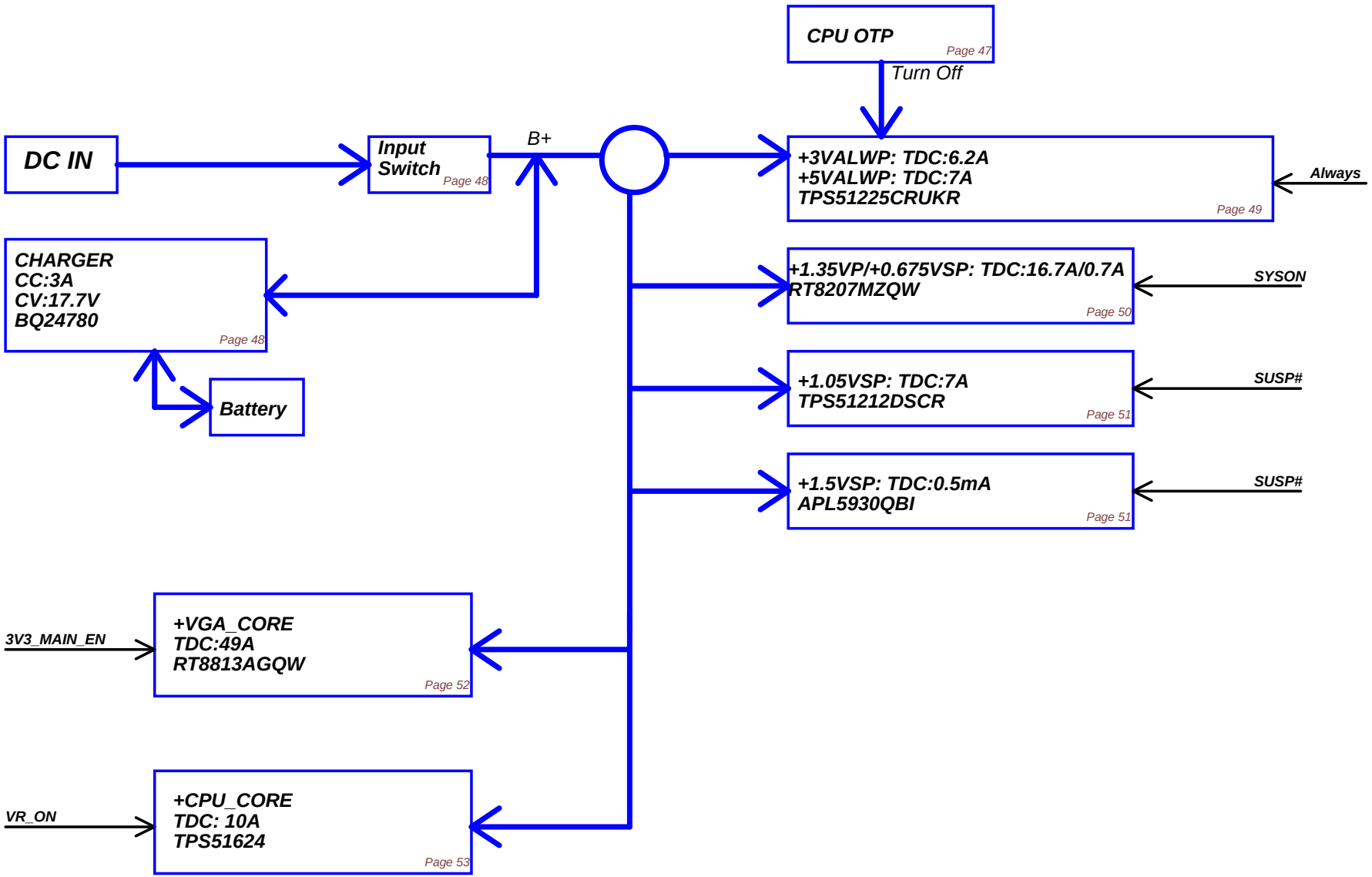
Power block



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date 2014/09/09	Title: PWR_POWER BLOCK DIAGRAM
Document Number: LA-A301P			Rev: 1.0
Date: Friday, September 19, 2014		Sheet 55 of 56	