Foxconn Precision Co. Inc.

MCP73M03 Schematic

Fab.B
Data: 2007/08/23

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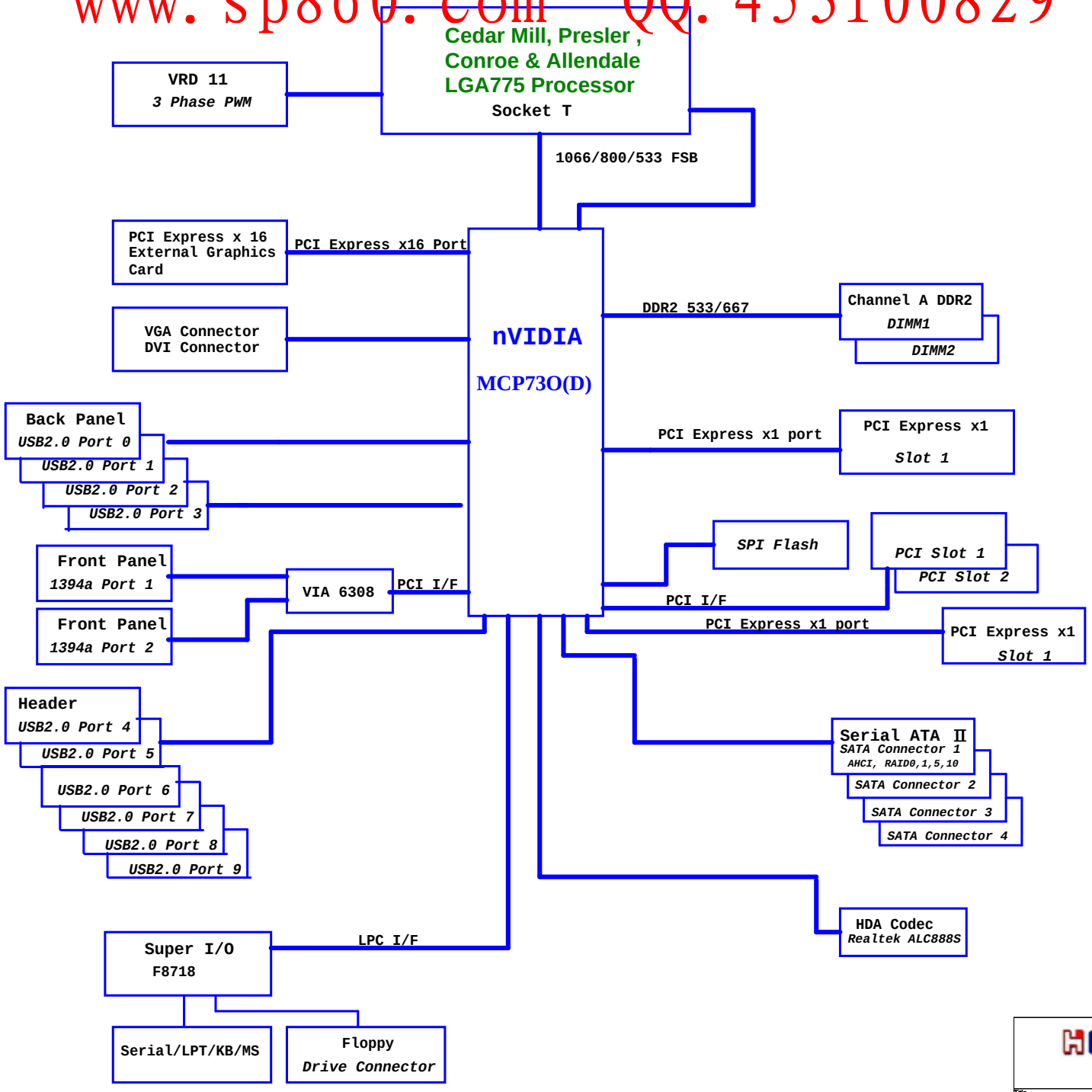

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Title: Topology

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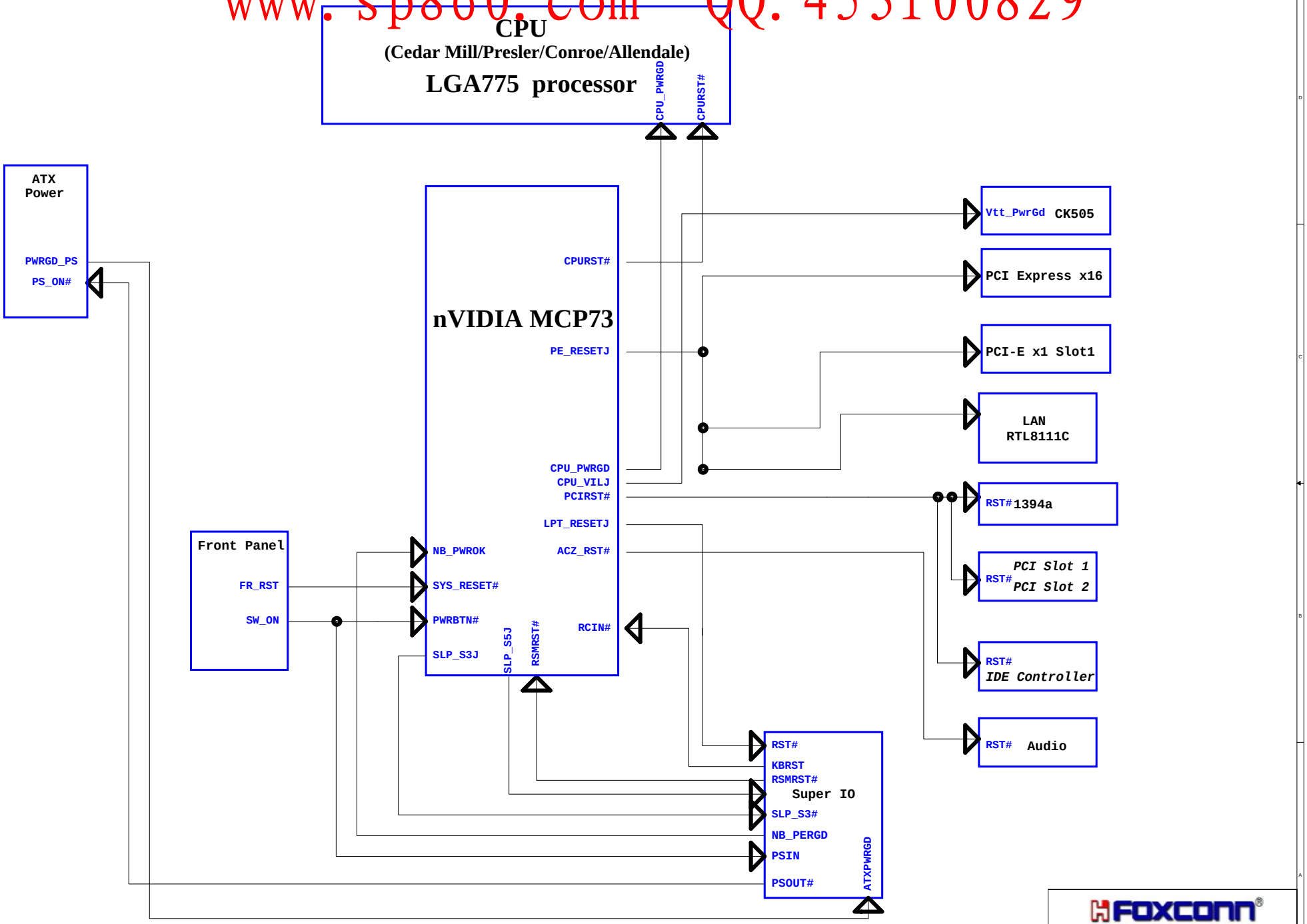

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Title: Reset Map

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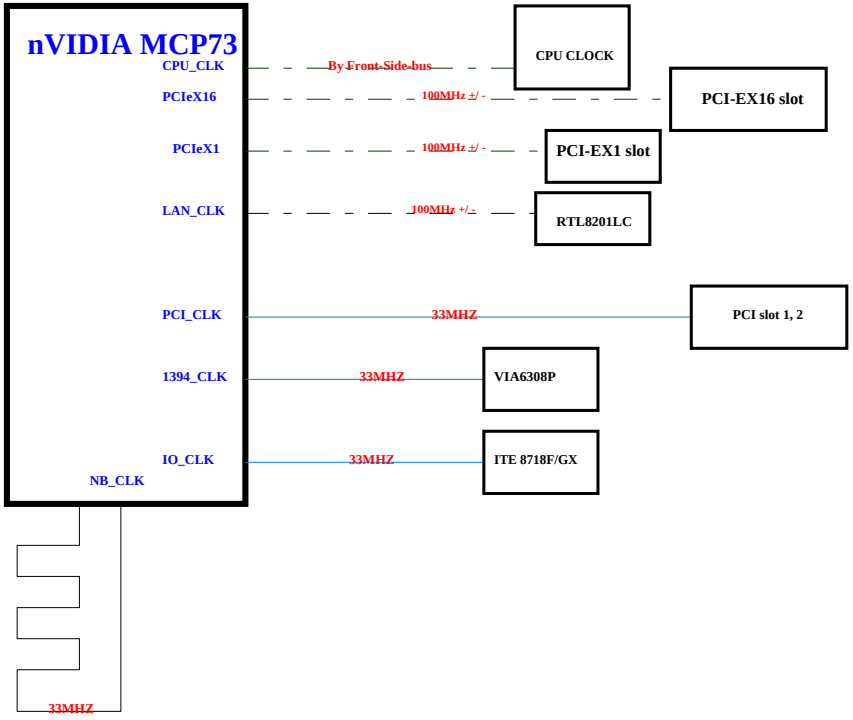

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Title: CLOCK Distribution

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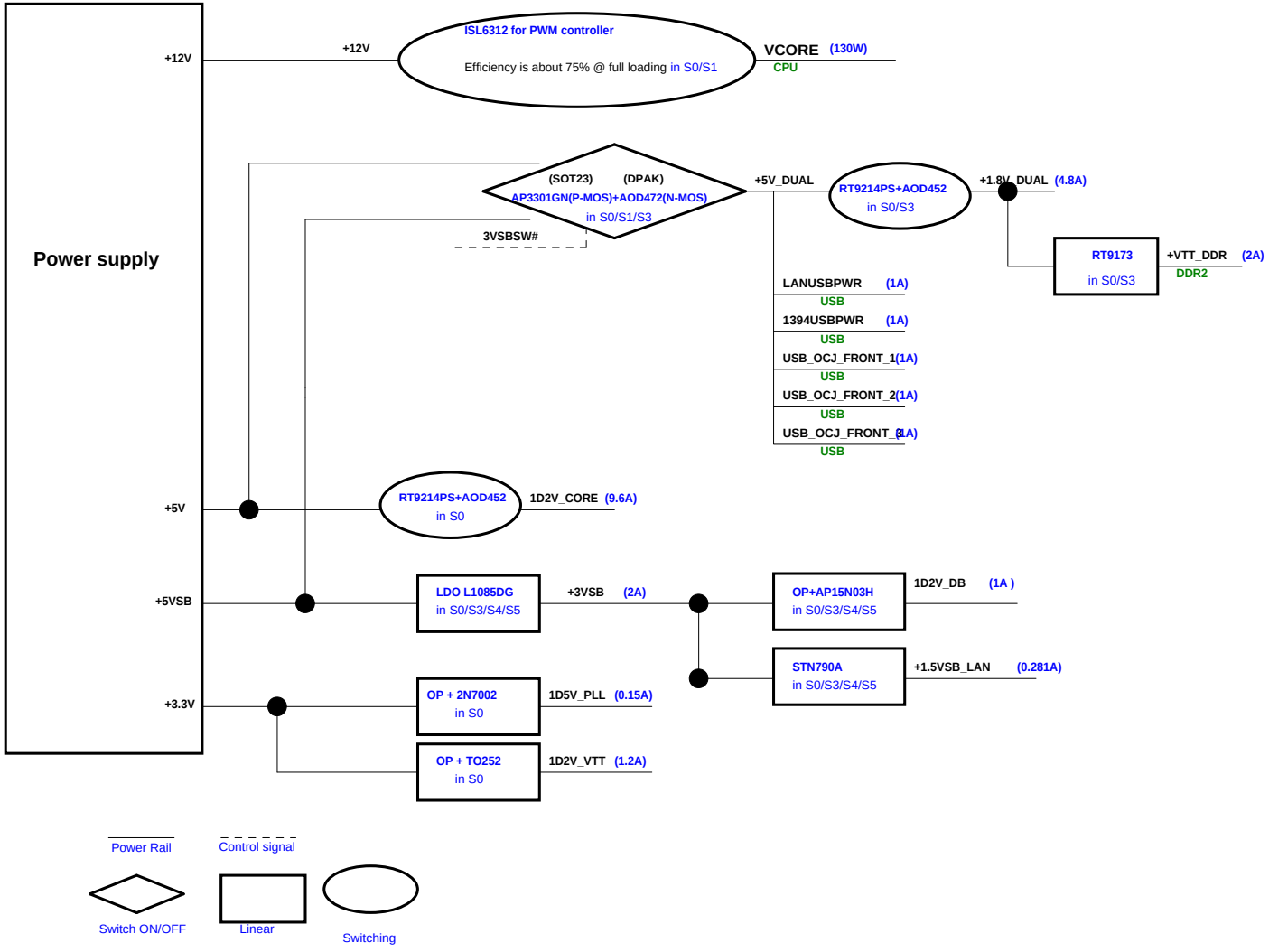

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Title: Power Delivery Map

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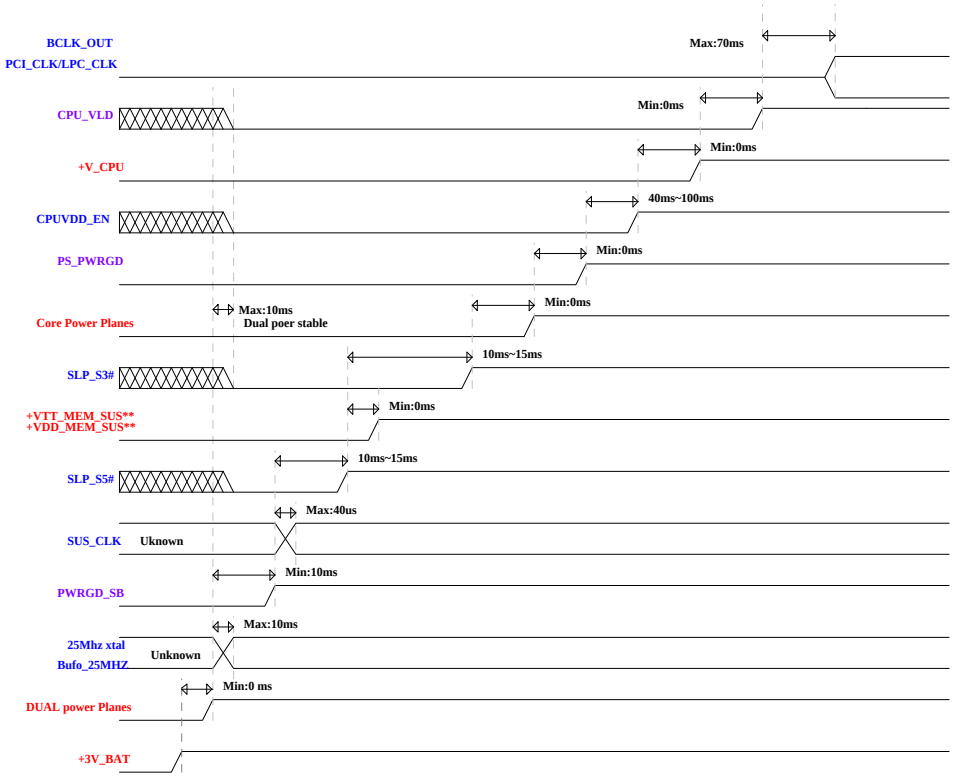
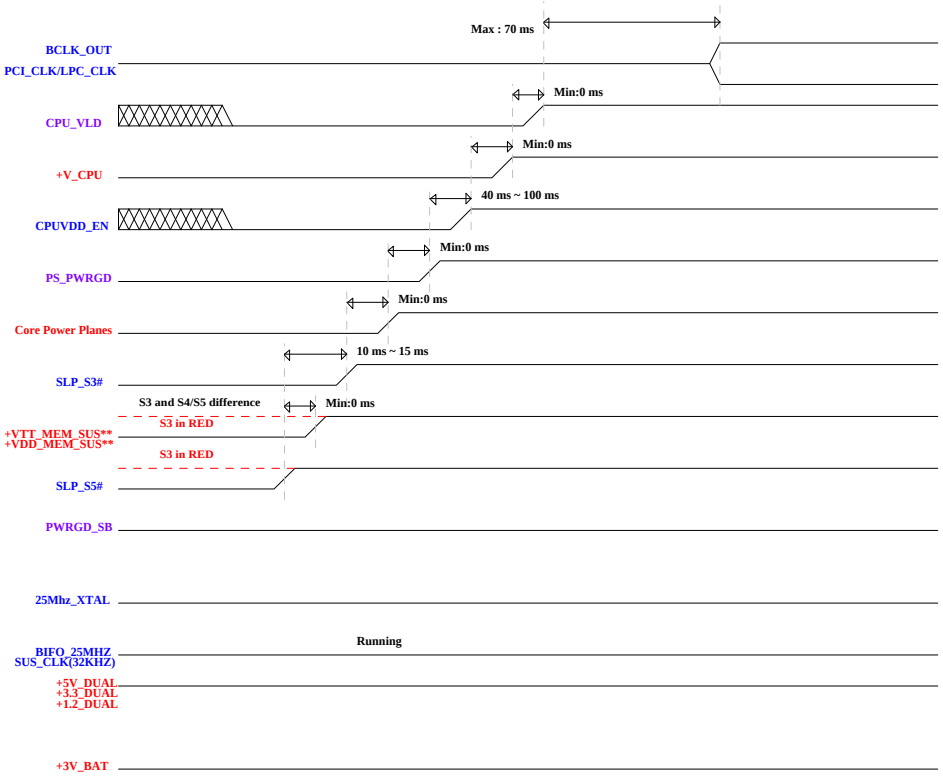
G3-tO-S0 Power Sequence



Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

S3/S4/S5 to S0 Resume Sequence



Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

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Title: Power Sequence

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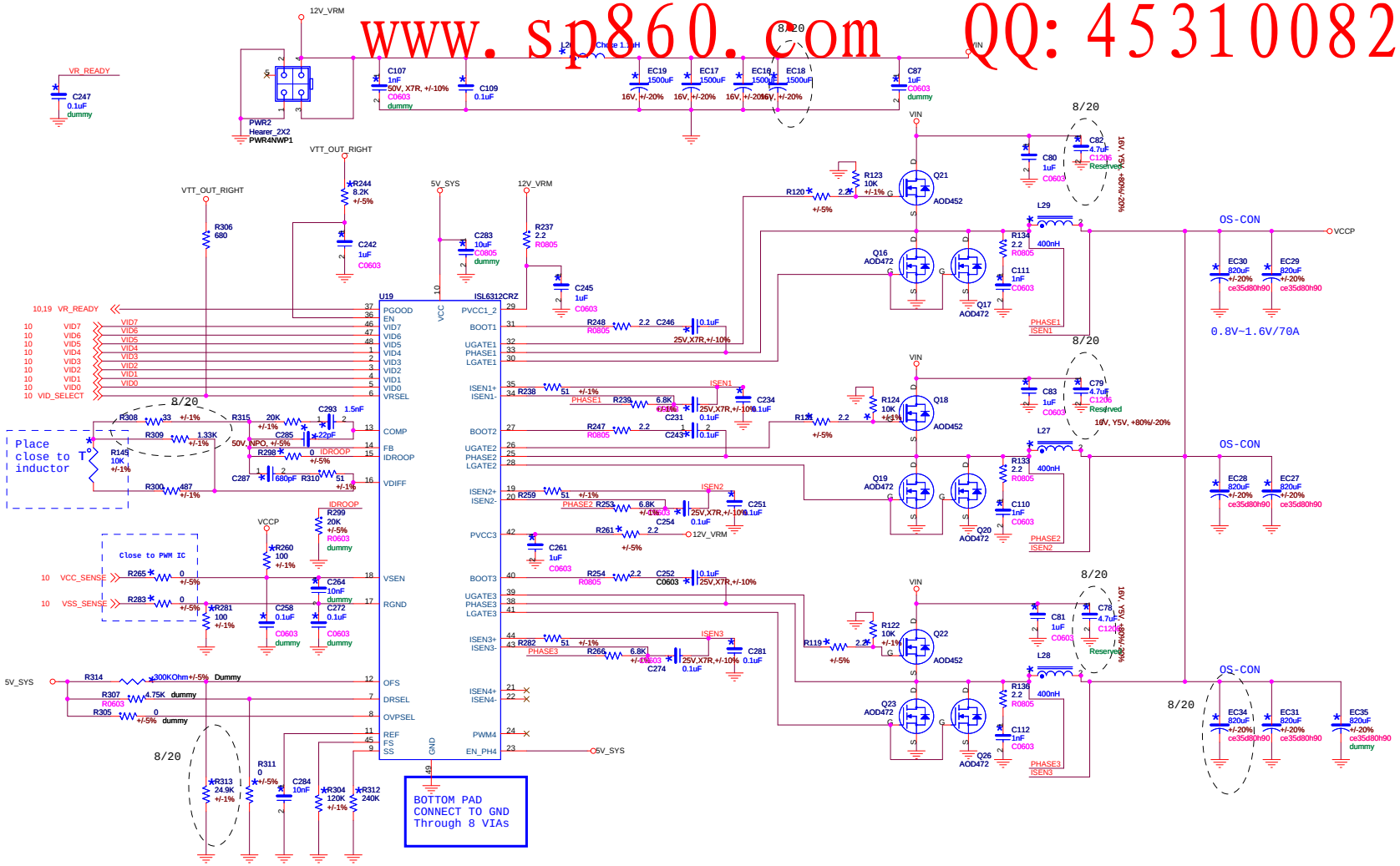

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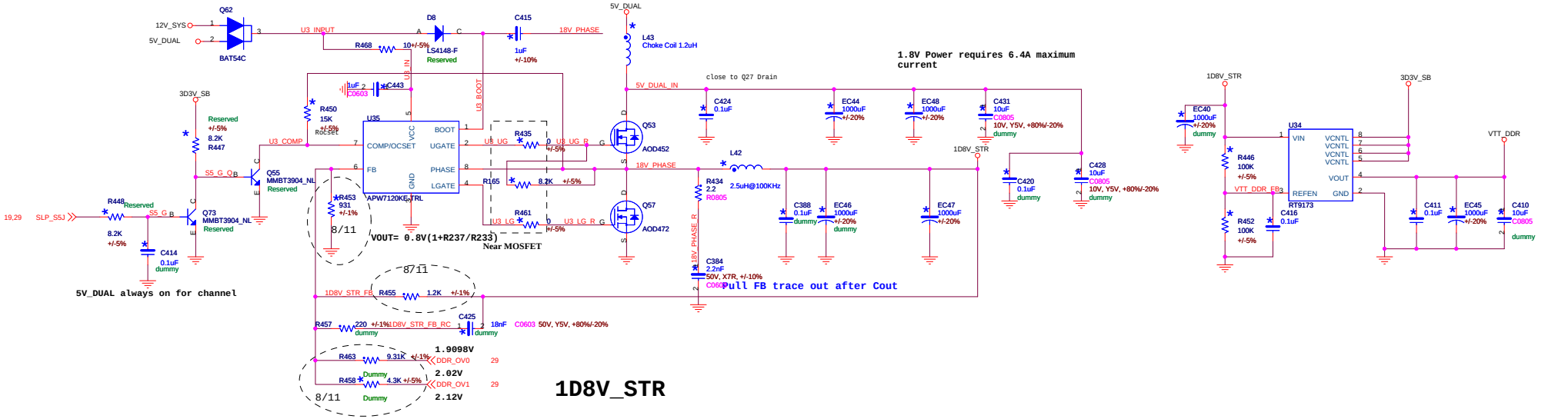
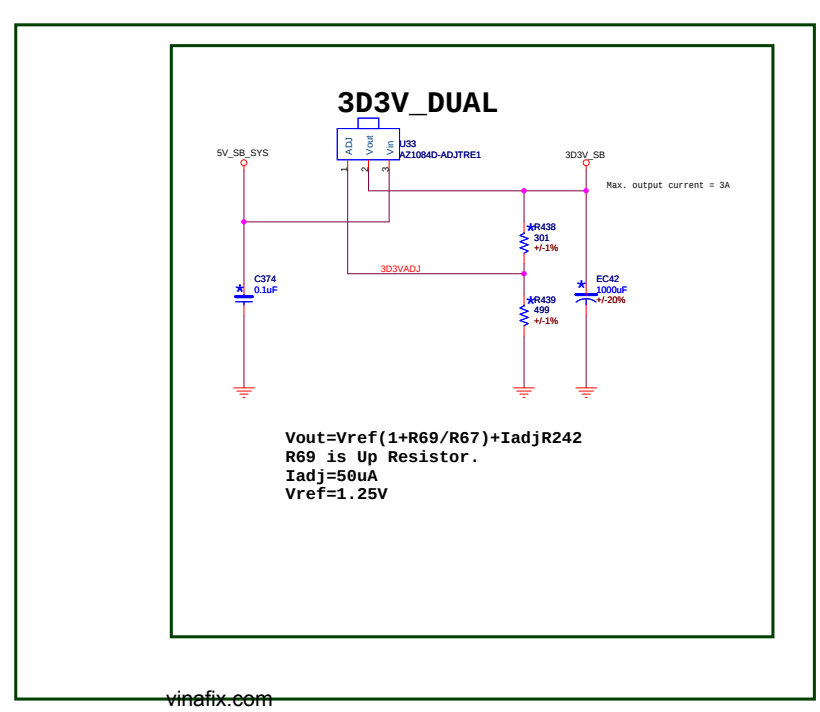
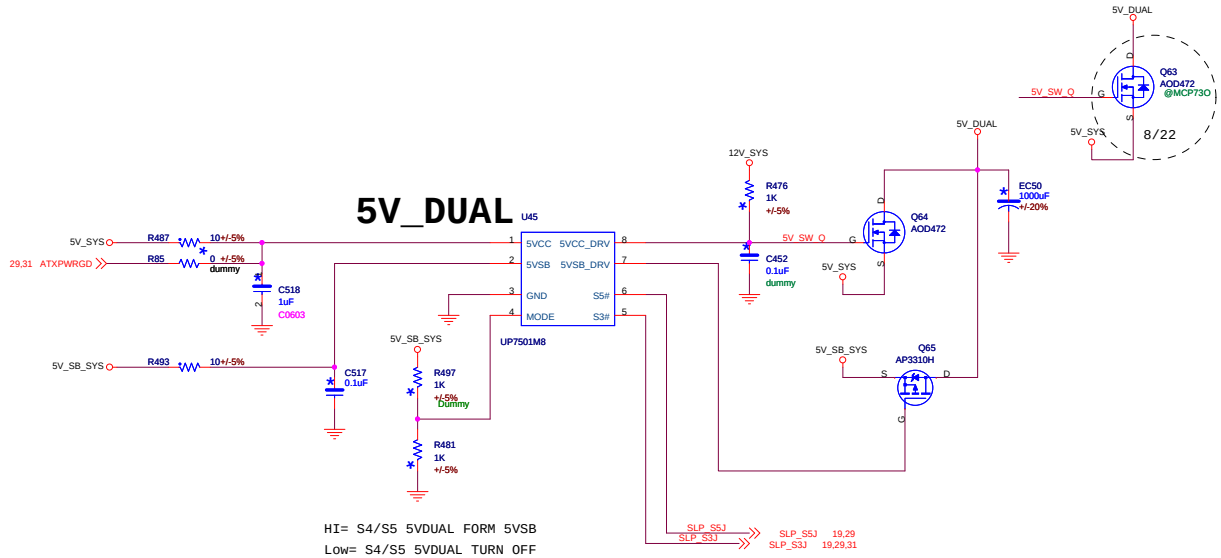
1.8V Voltage

DDR_VTT







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Title: ACPI-1

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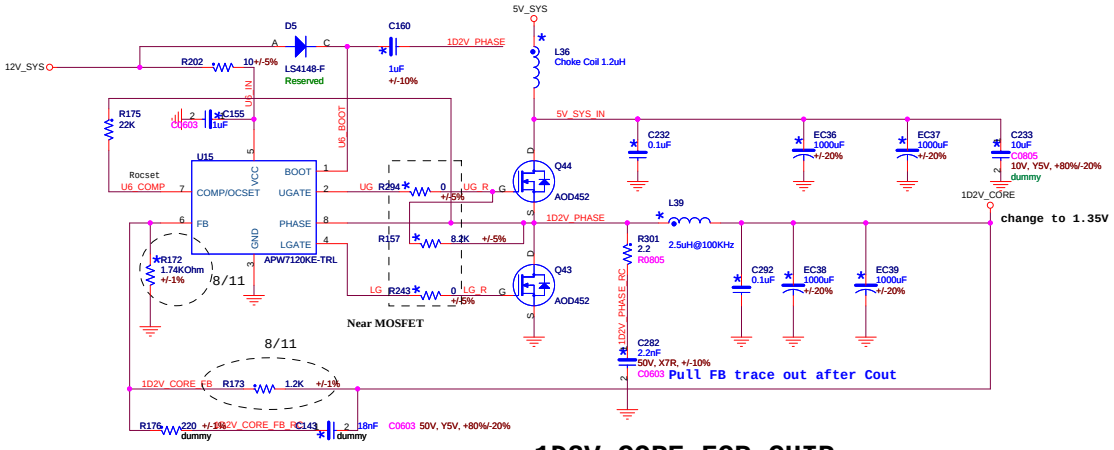
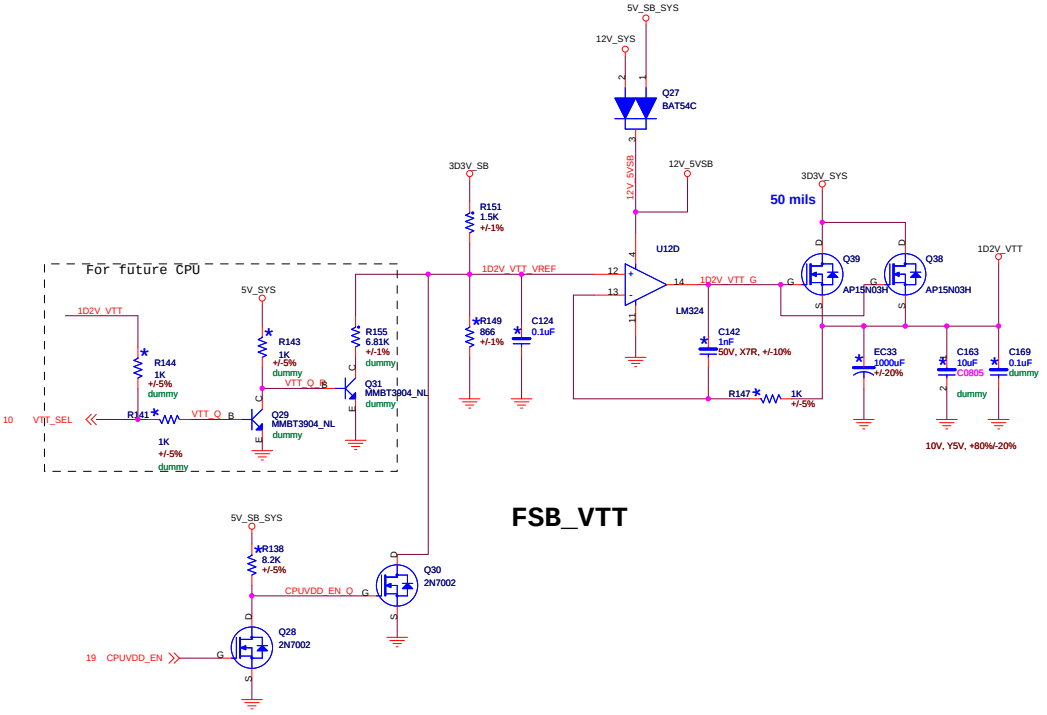
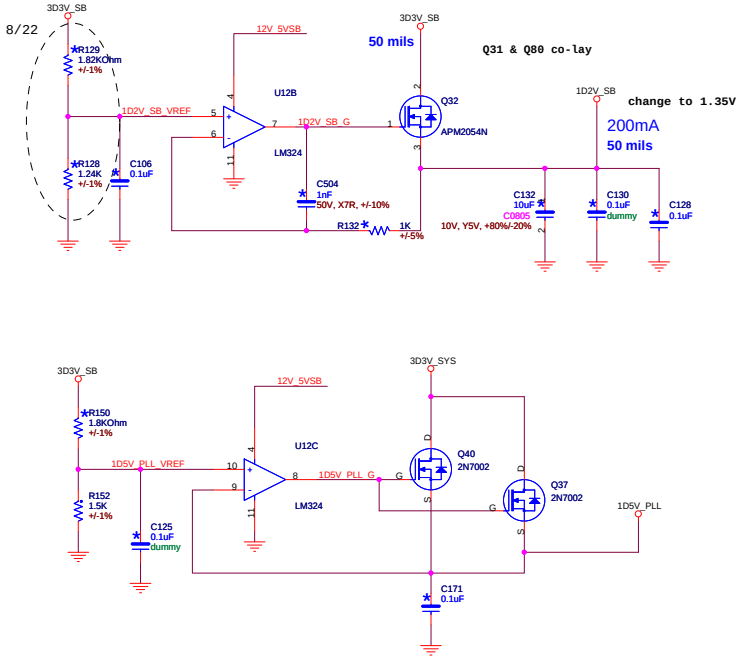


1D2V_CORE FOR CHIP



FSB_VTT



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Title: ACPI-2			
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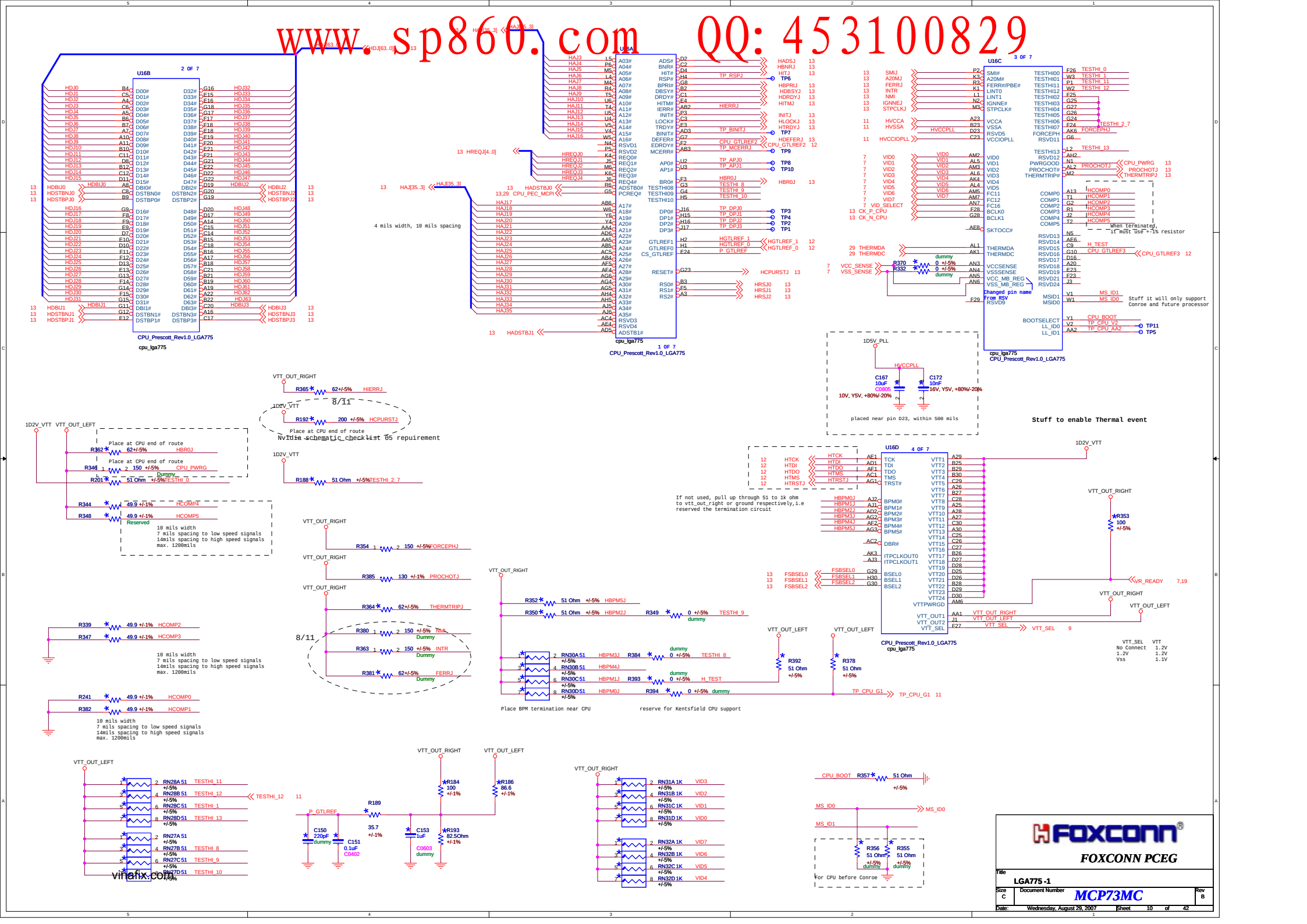

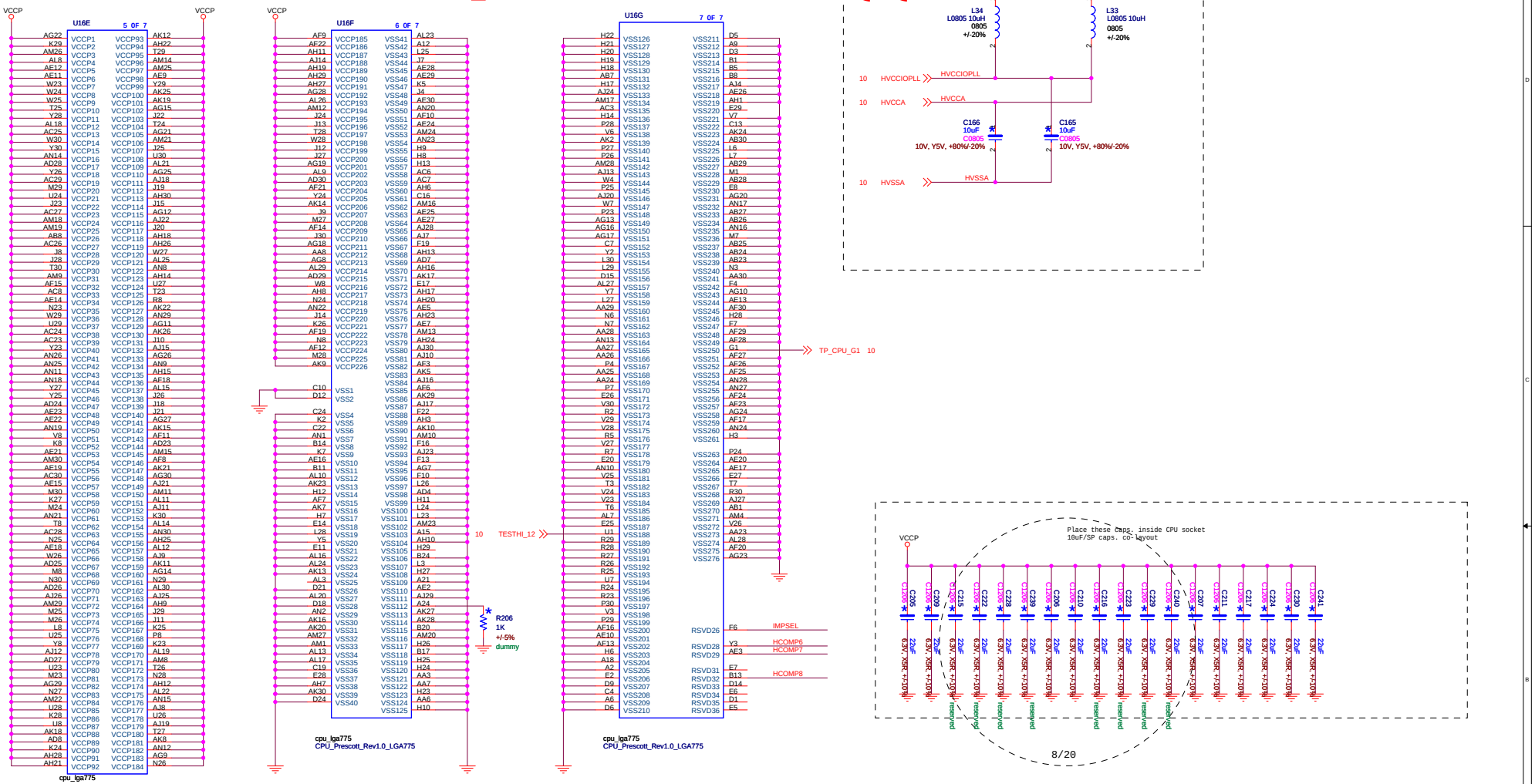

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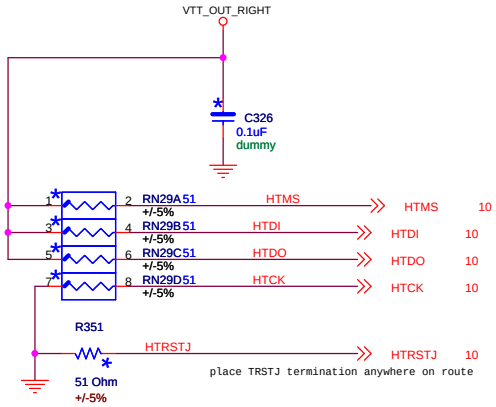
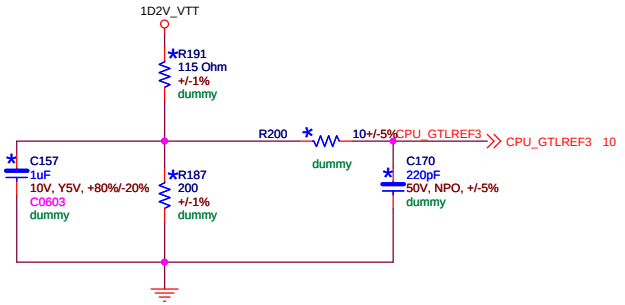
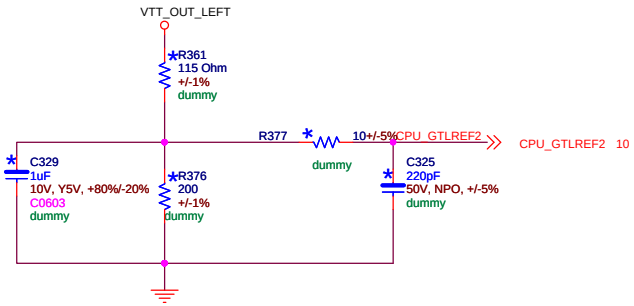
	VRD10.1	VRD11
H_VID_SELECT	GND	HIGH
H_CPUBOOT	FLOATING	GND
H_MSID0	GND	FLOATING

NEW CPU SWITCH (Conroe/Wolfdale)







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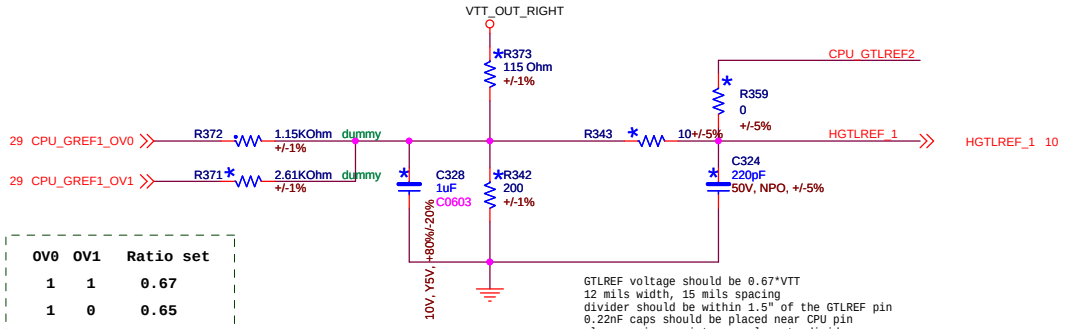
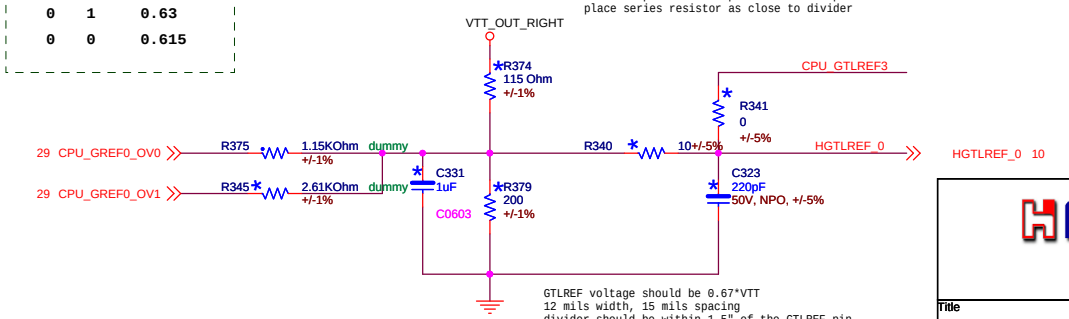


OV0	OV1	Ratio set
1	1	0.67
1	0	0.65
0	1	0.63
0	0	0.615



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Title: LGA775 -2		
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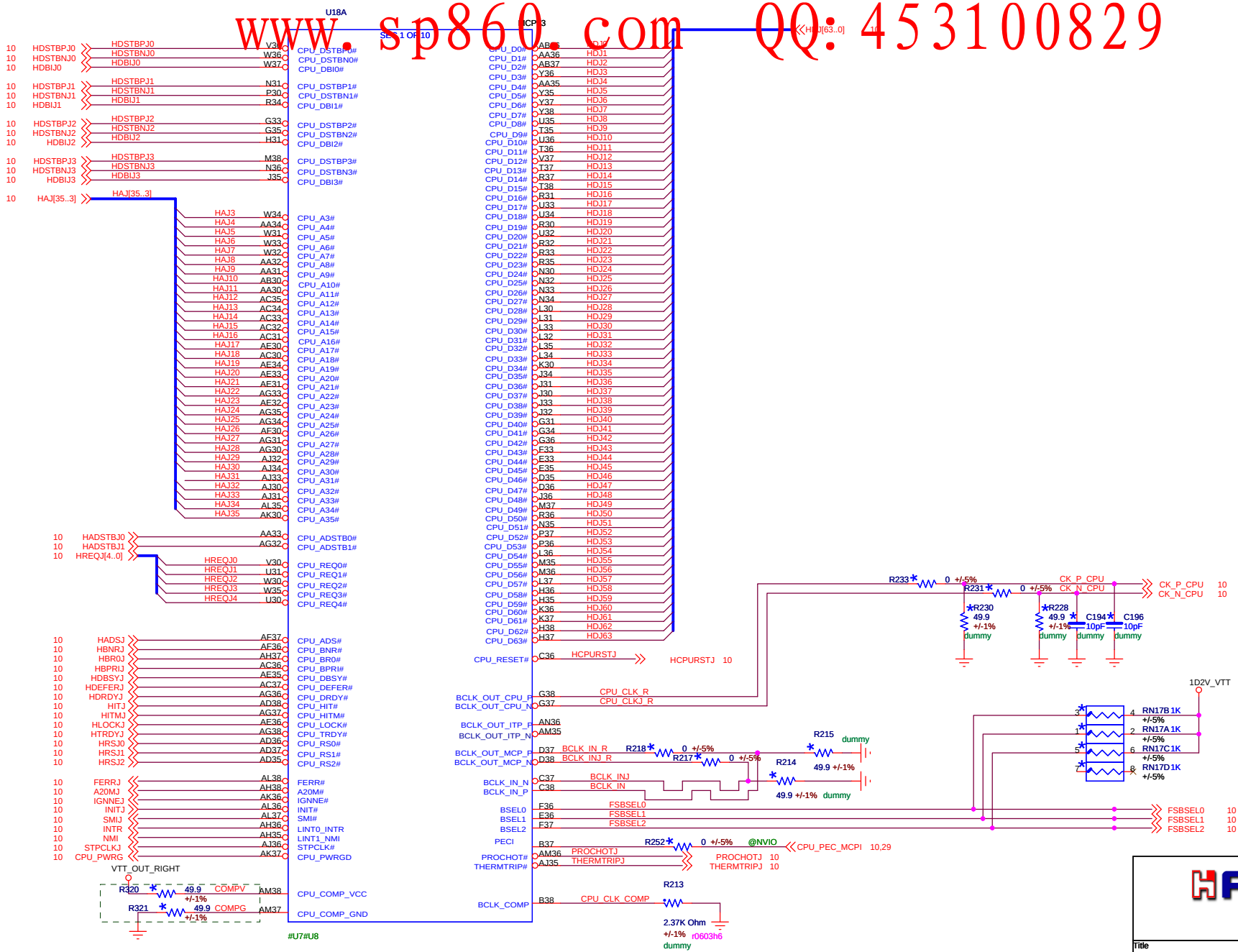

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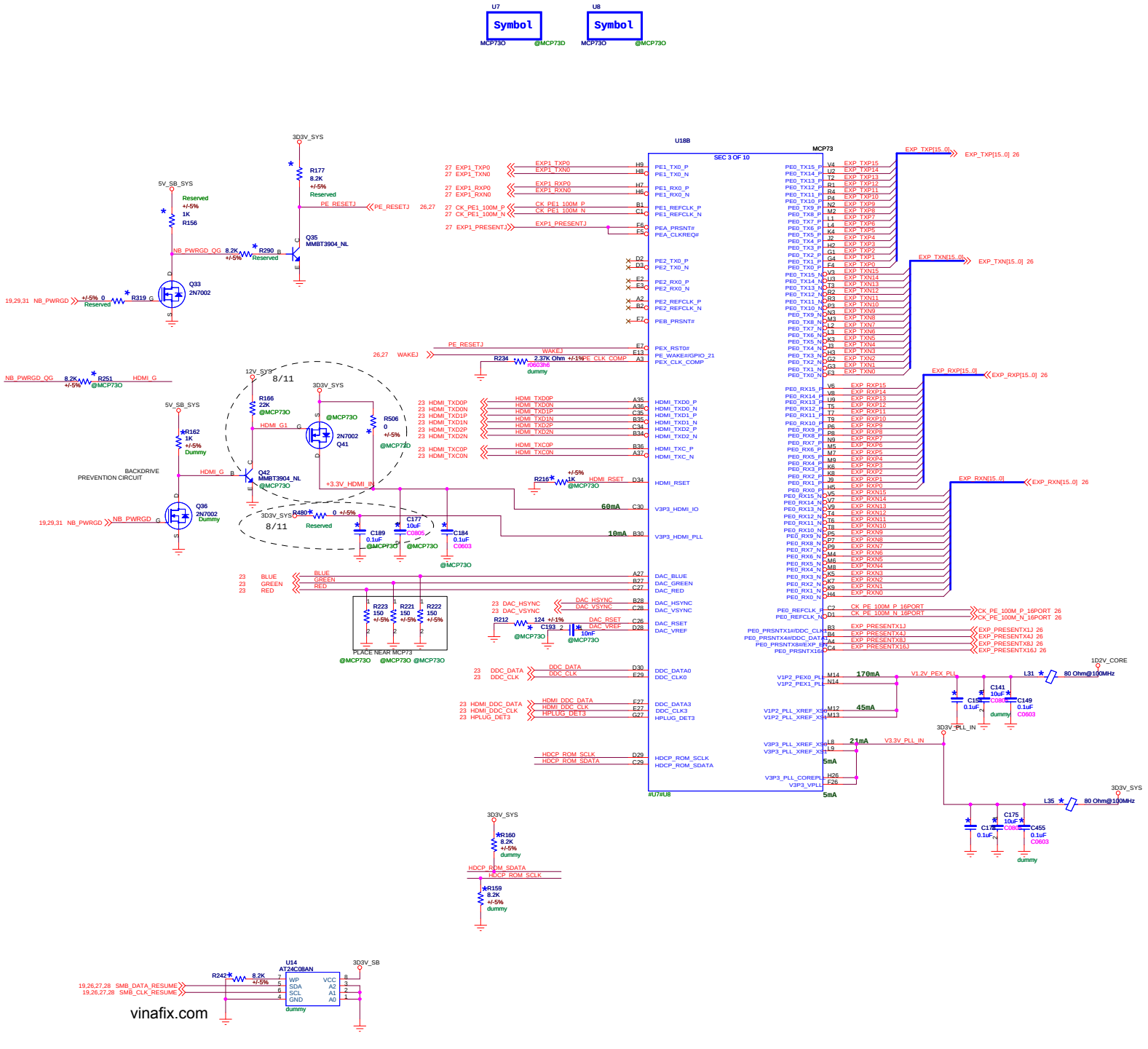

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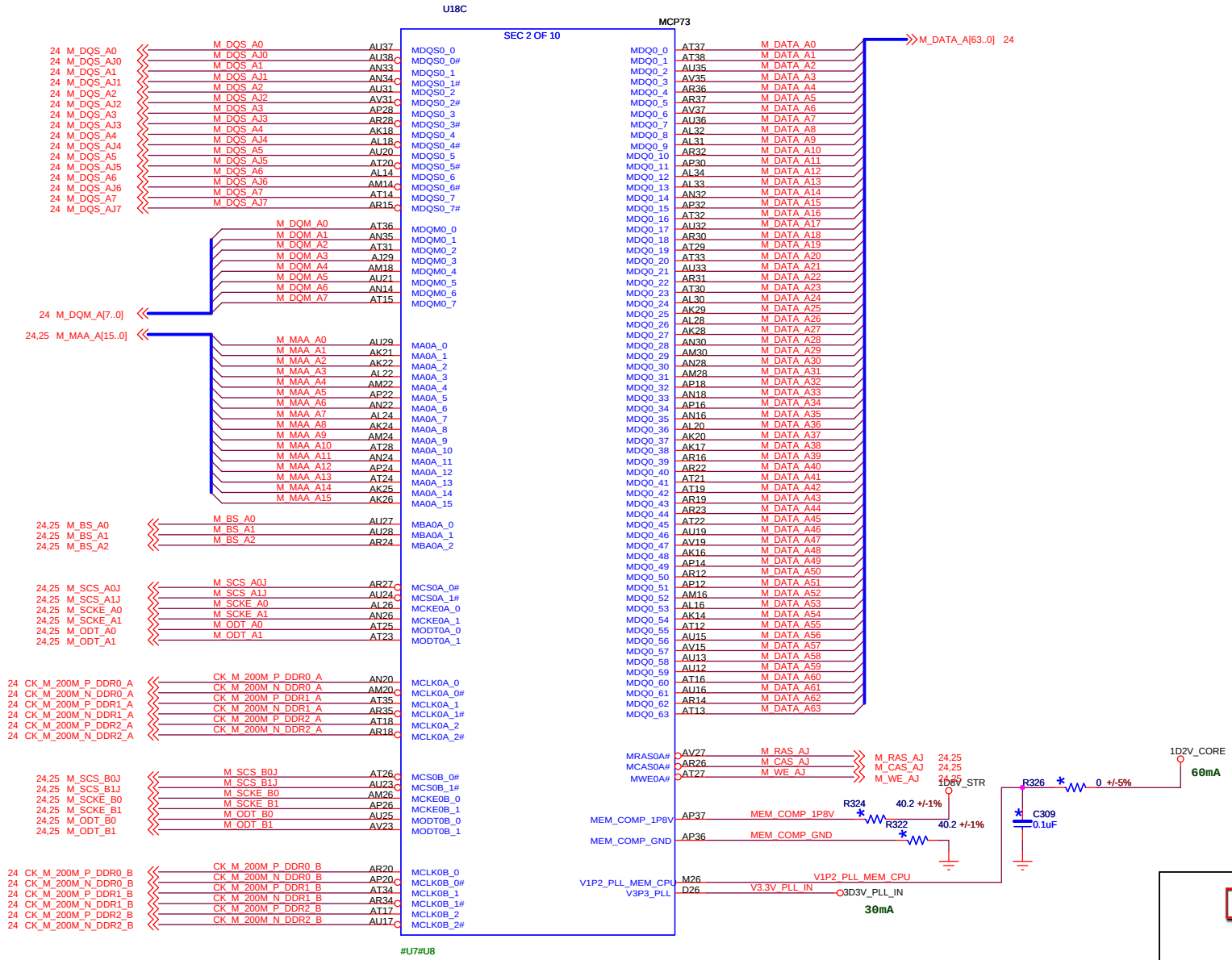

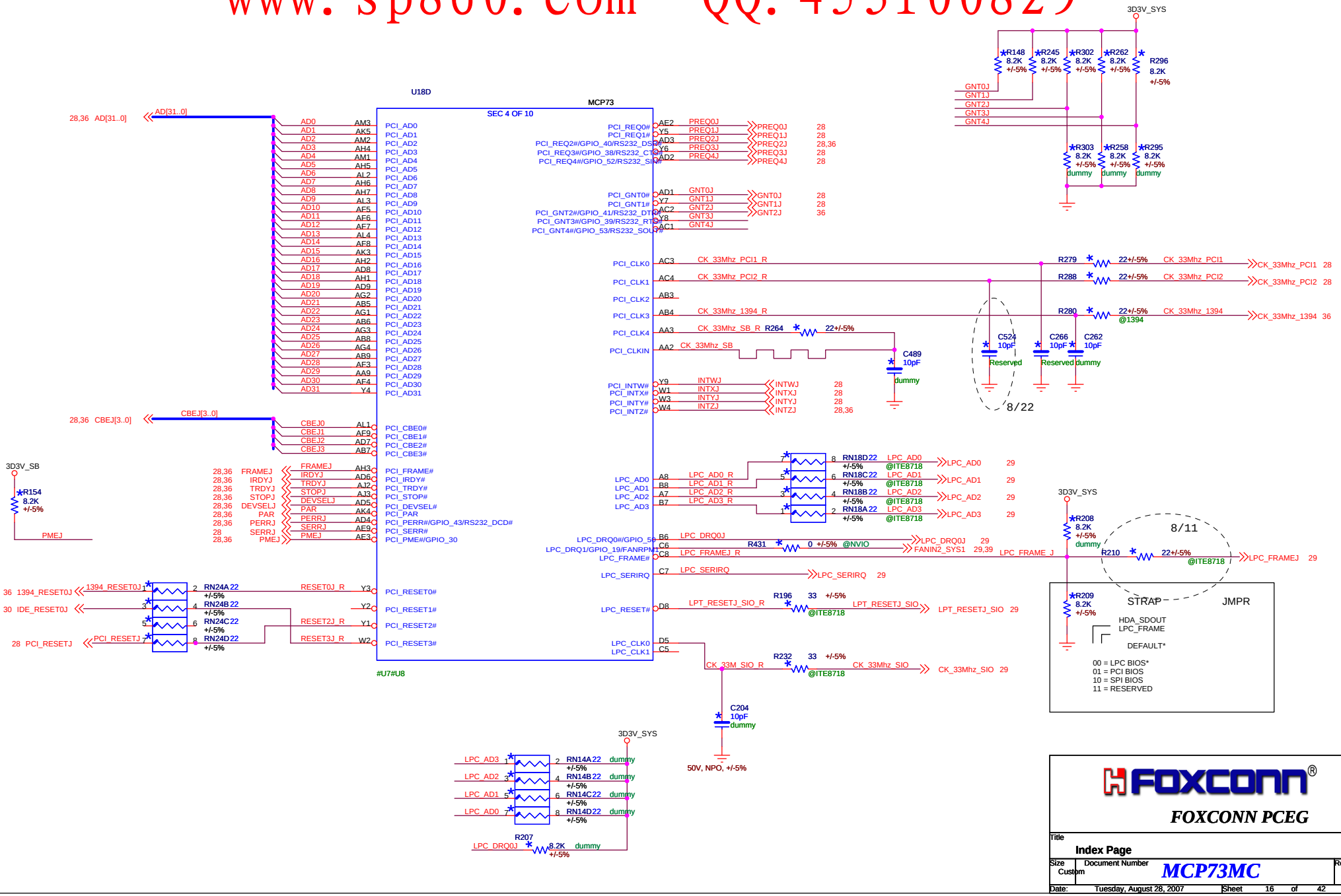

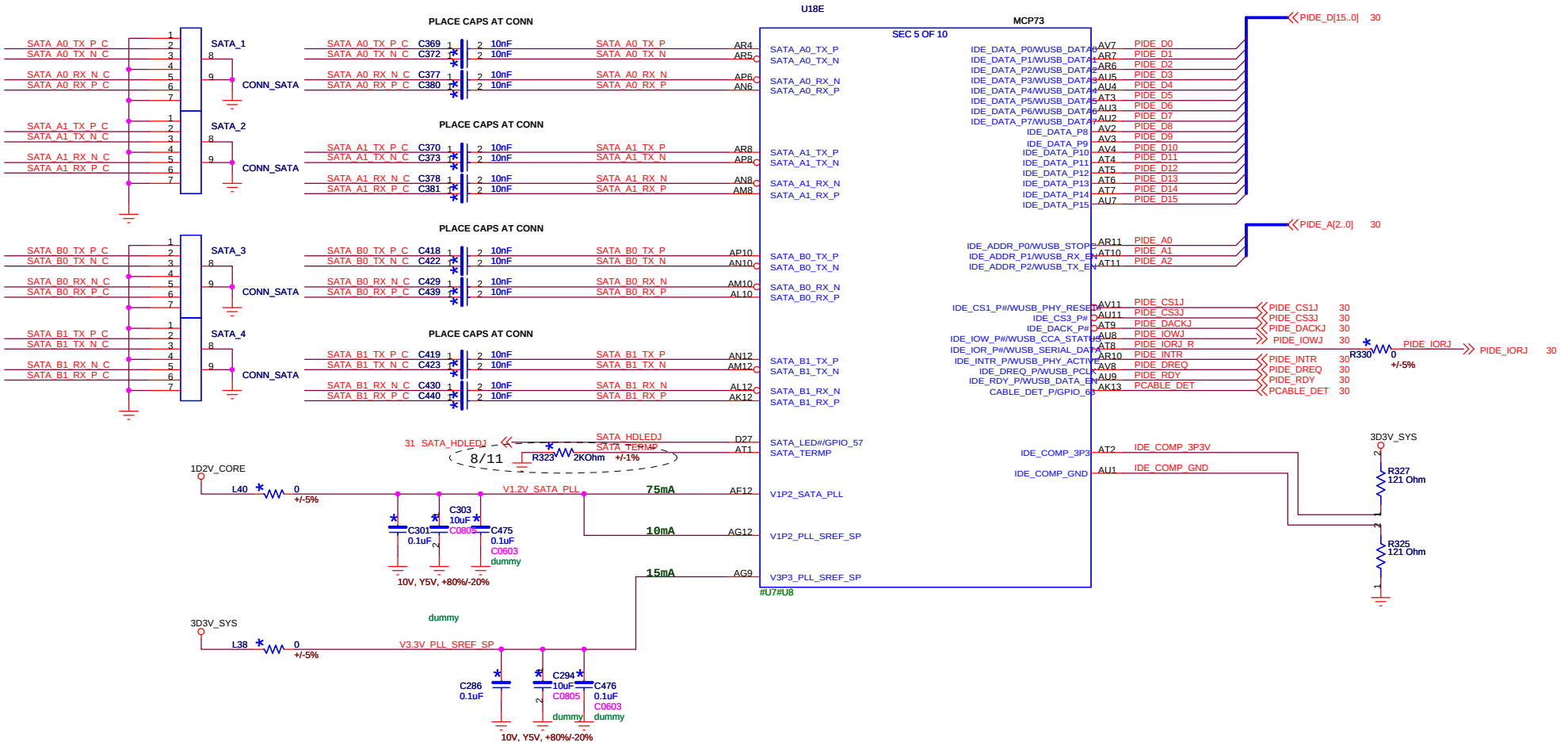

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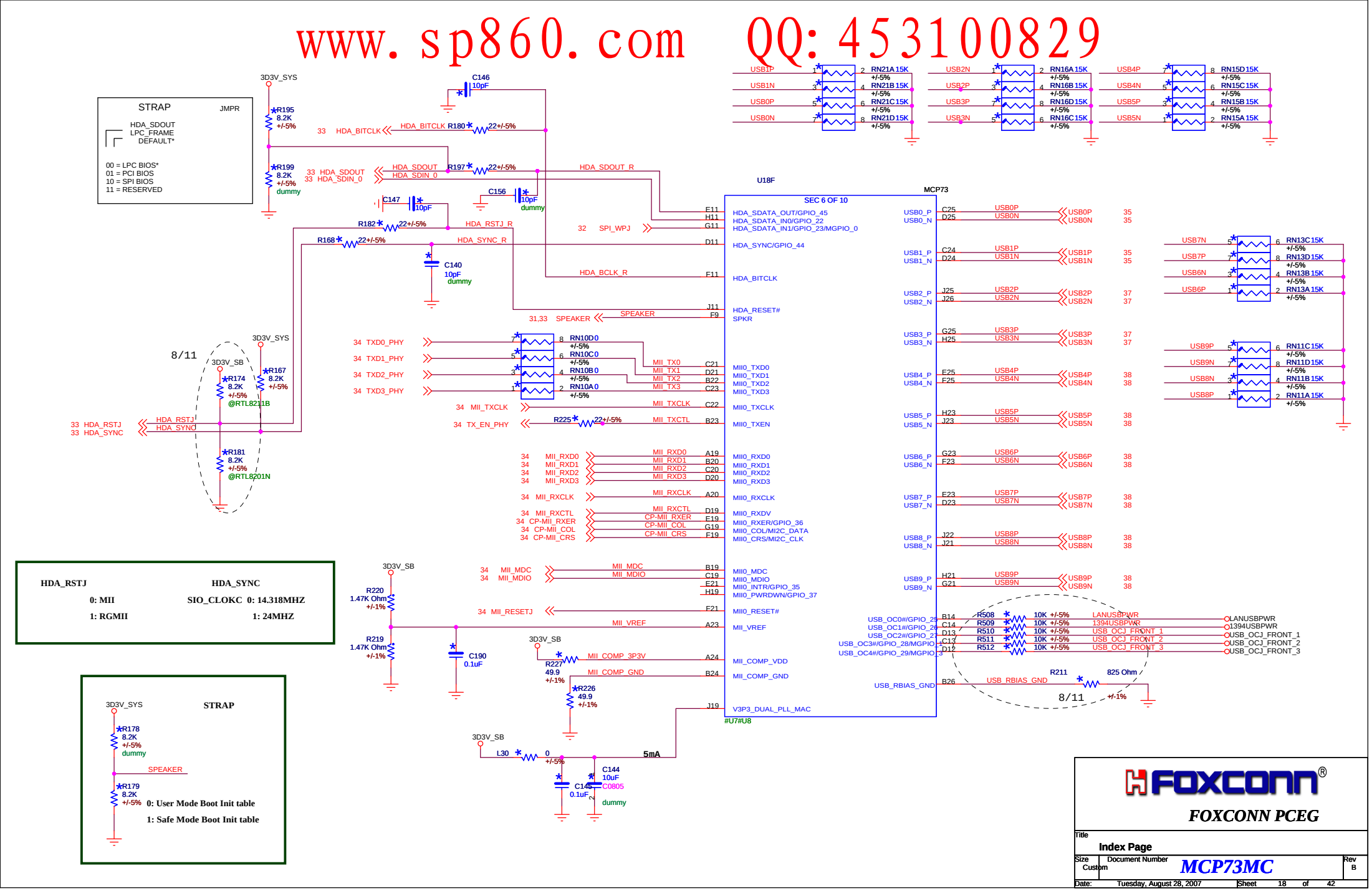

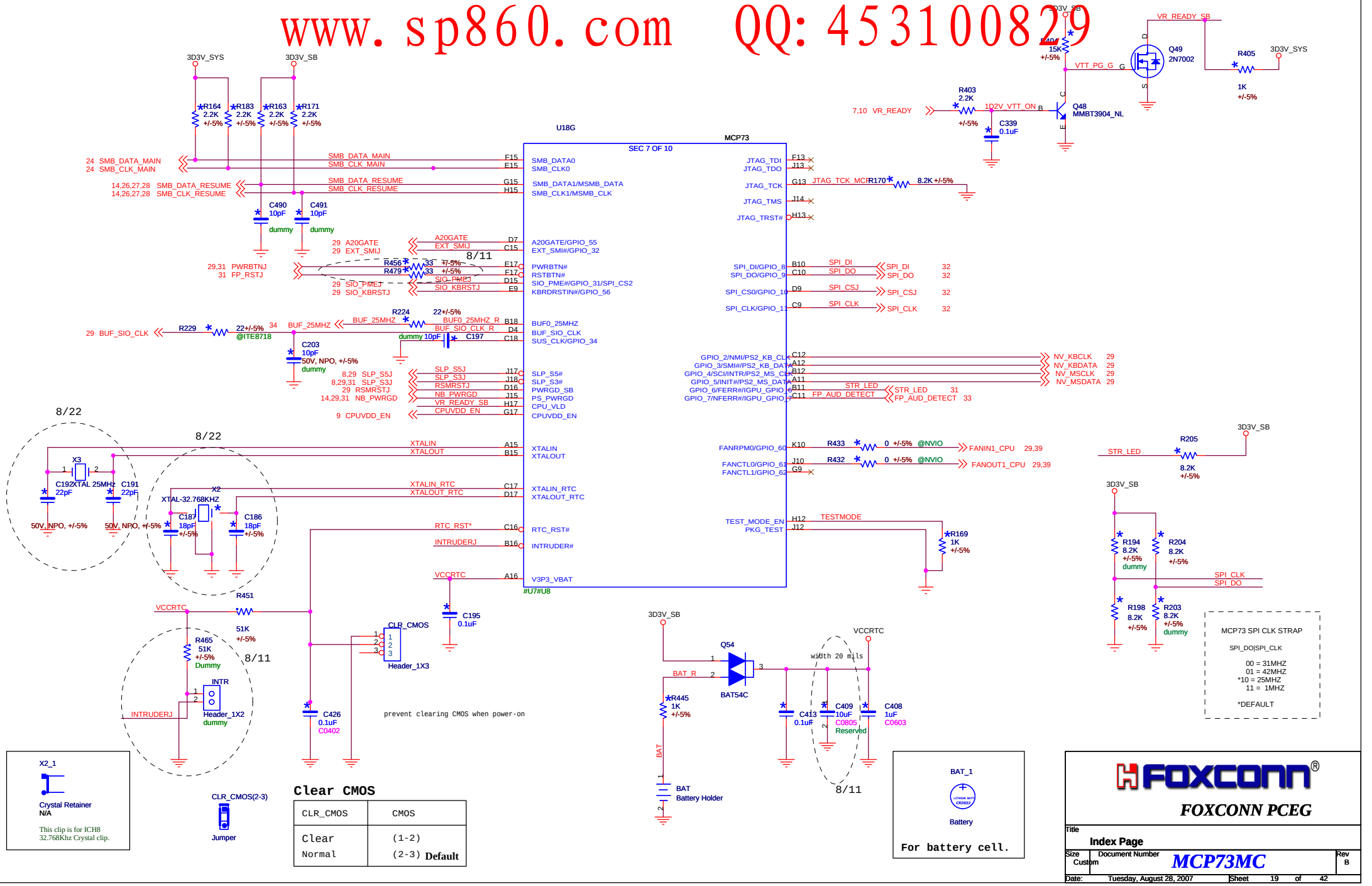

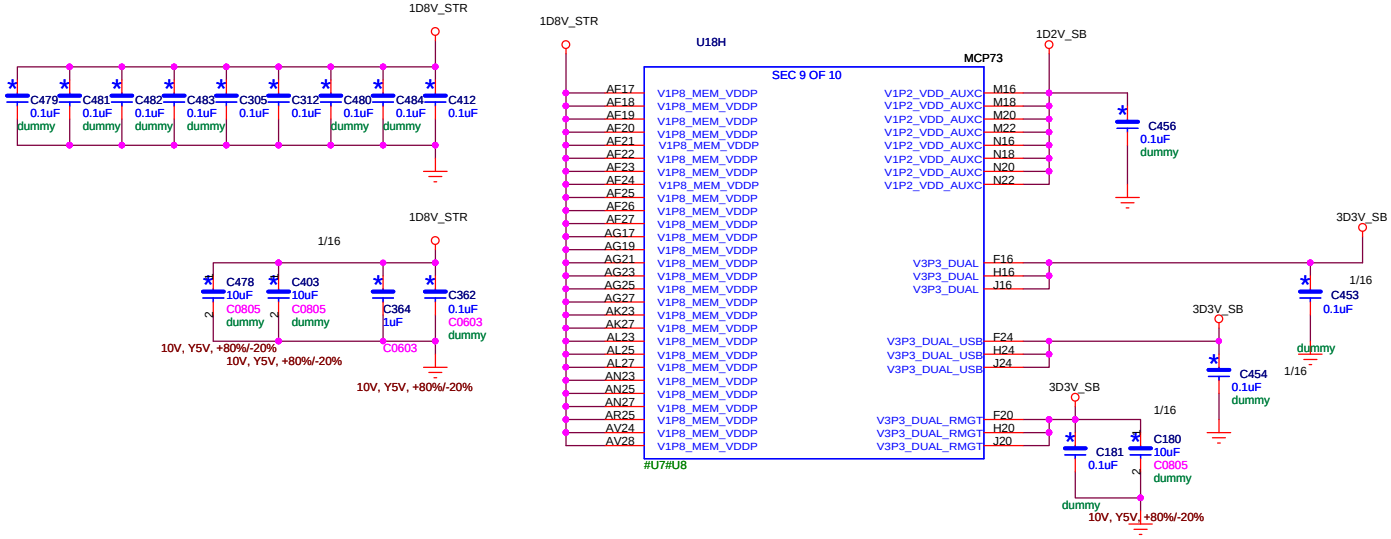

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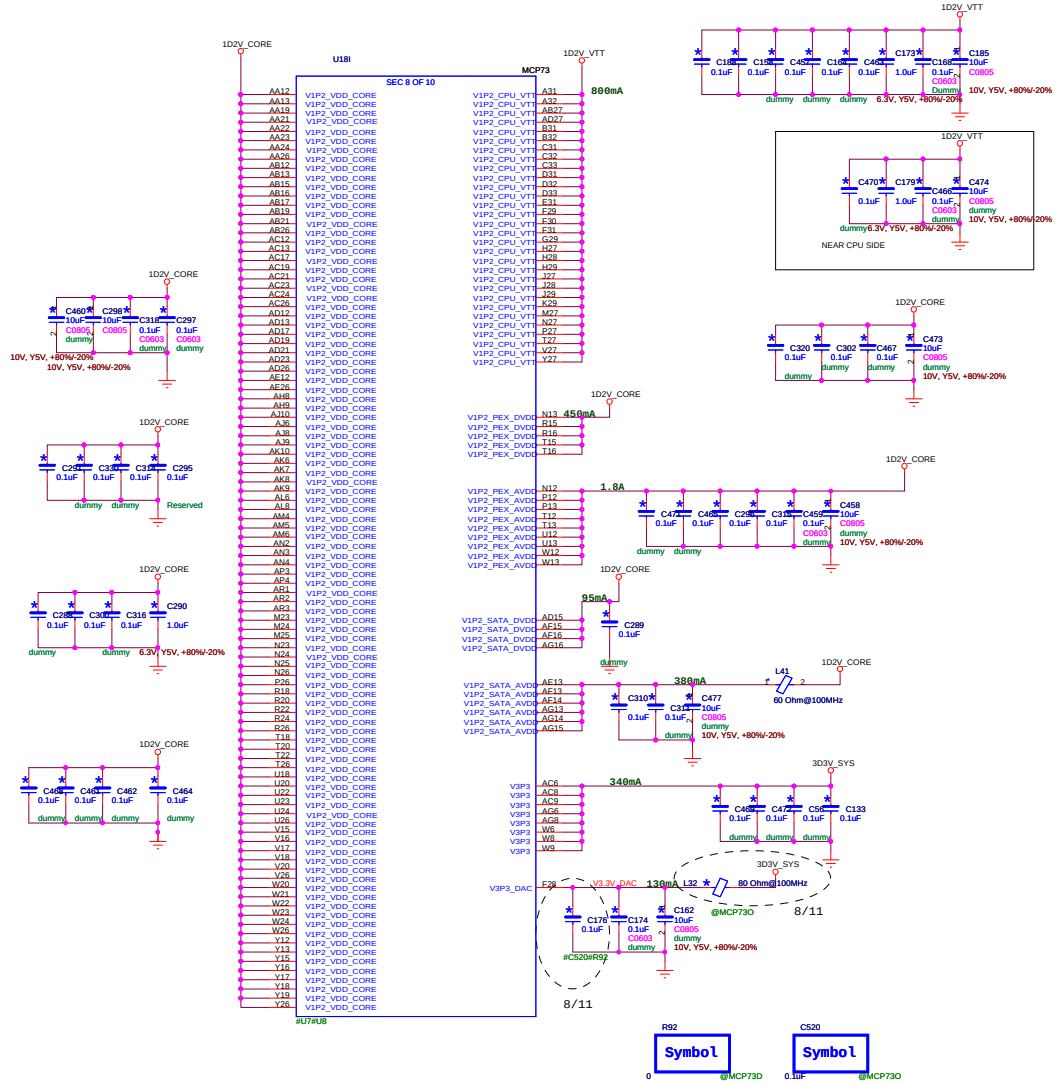

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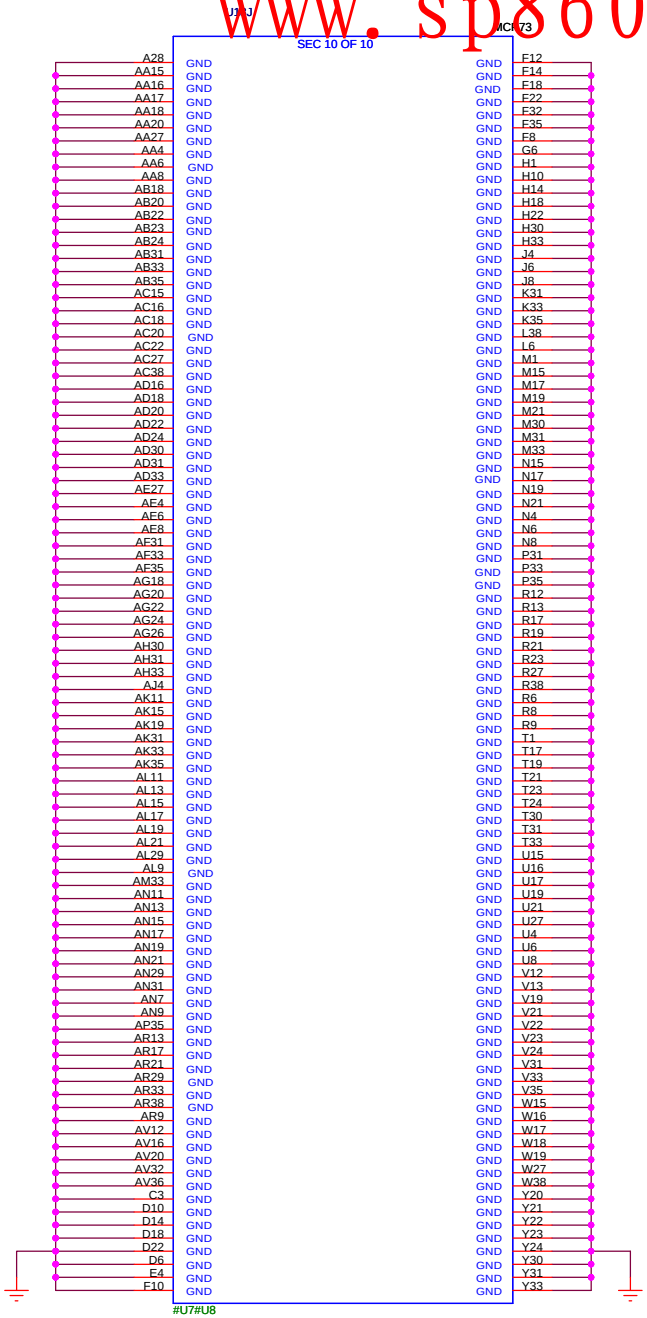

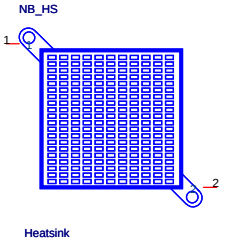

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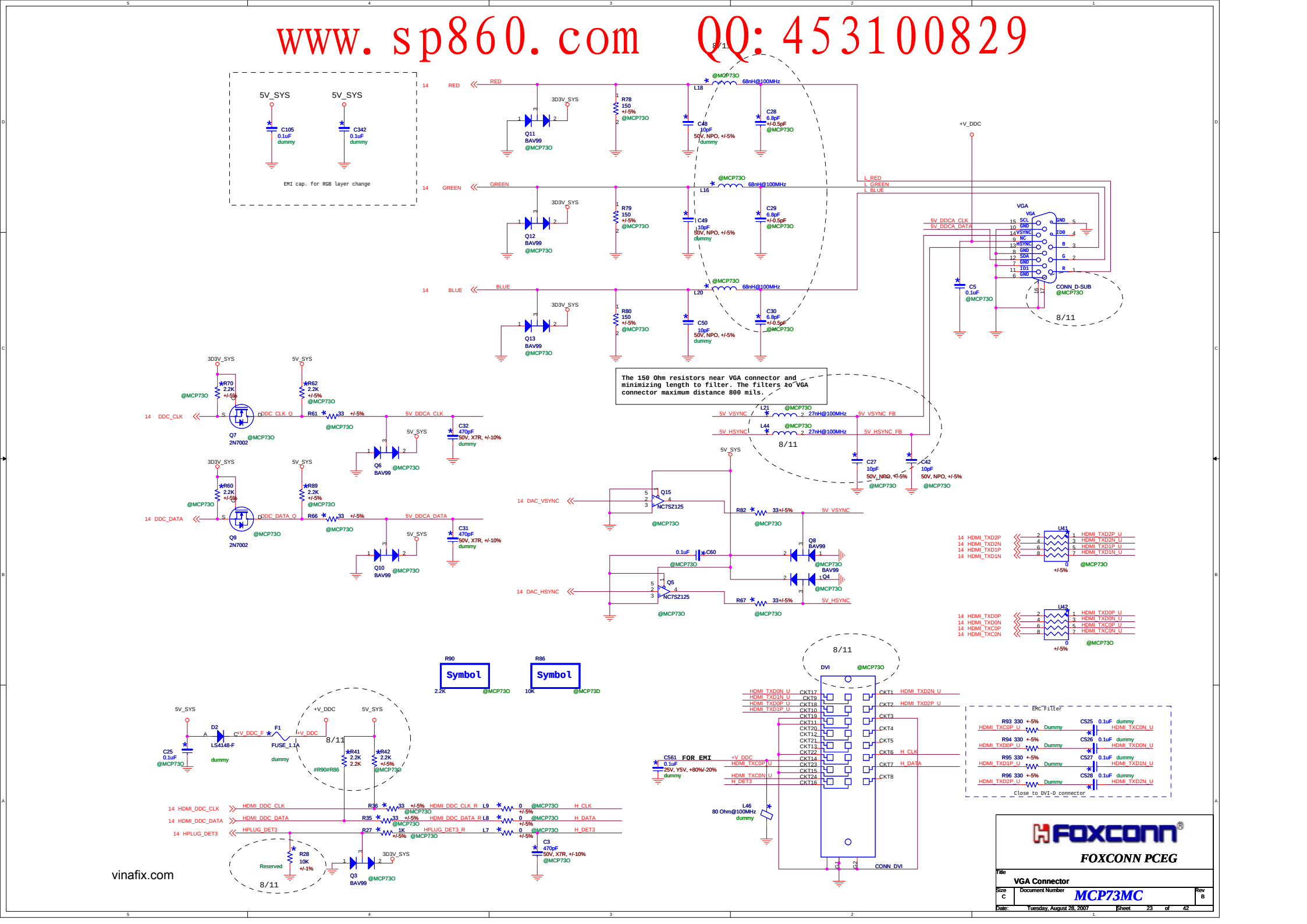

DIMM1

DIMM2

1D8V_STR

EC41 1000uF +/-20%

Channel A DIMM 1 1.8V high-frequency decoupling caps. place as close to DIMM power pins as possible

C396 0.1uF dummy

C394 0.1uF

C395 0.1uF Reserved

C393 0.1uF

SMB_CLK_MAIN SMB_DATA_MAIN

C375 22pF 50V, NPO, +/-5% dummy

C382 22pF 50V, NPO, +/-5% dummy

For ESD or EOS

3D3V_SB

BAV99 1Q52

BAV99 1Q51

3D3V_SYS

SMVREF_A

R413 121 Ohm

R412 121 Ohm

C356 0.1uF

C357 0.1uF

close to DIMM pin dummy

Width 10 mils minimum, Spacing 10 mils minimum.

C396 0.1uF dummy

C397 1.0uF

C398 0.1uF

C399 0.1uF

6.3V, Y5V, +80%-20%

Channel A DIMM II 1.8V high-frequency decoupling caps. place as close to DIMM power pins as possible

DDR II

DDR II

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Title: DDR2 Channel A DIMM 1, 2

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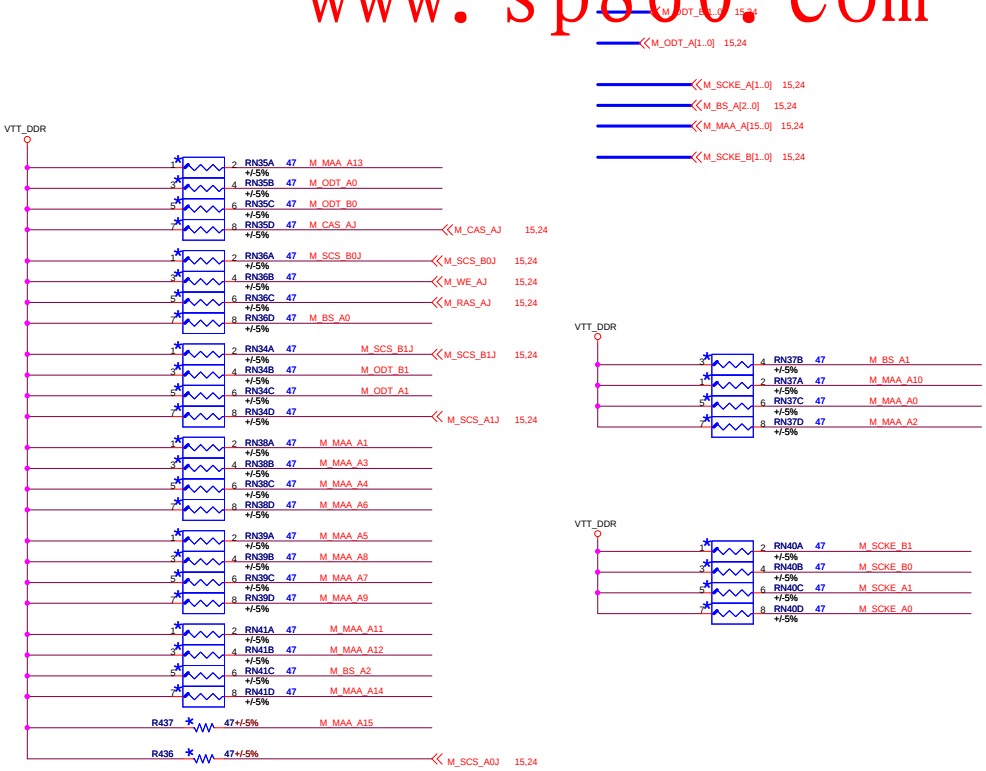
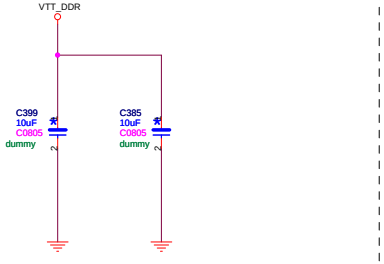
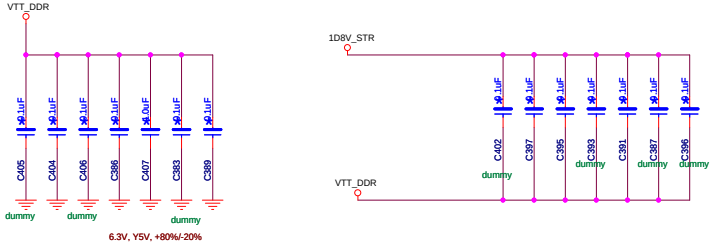




Channel A VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

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Title: DDR2 Channel A Termination

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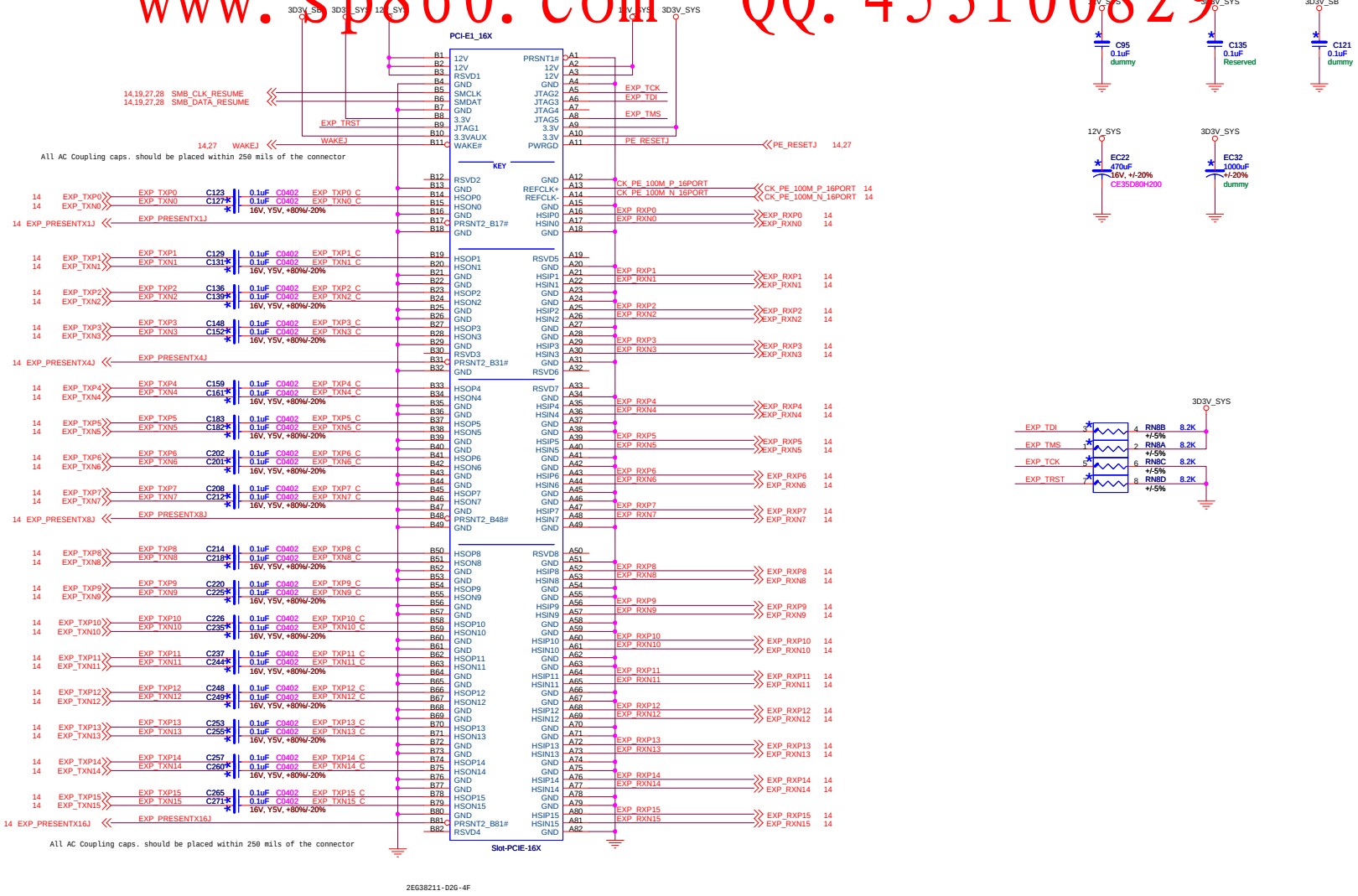

2EG38211-D2G-4F

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Title: PCI Express x16 Gfx Slot

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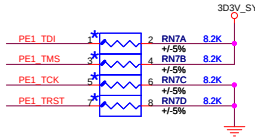
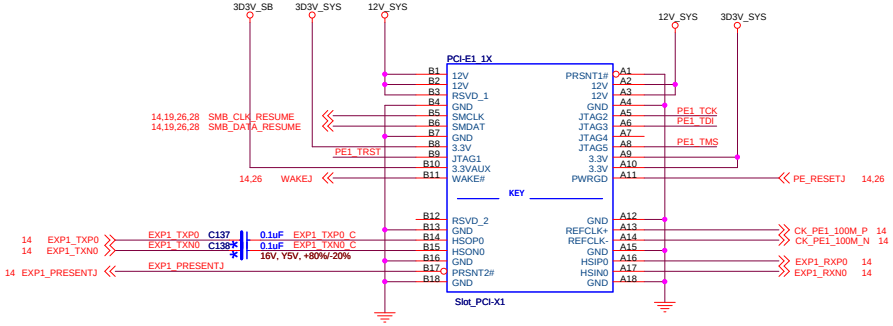
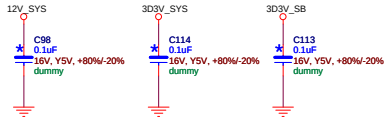
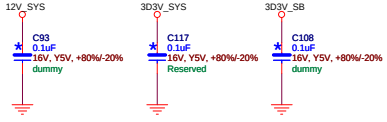




PCI-E x1 Slot 1





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Title: PCI Express x1 Slot

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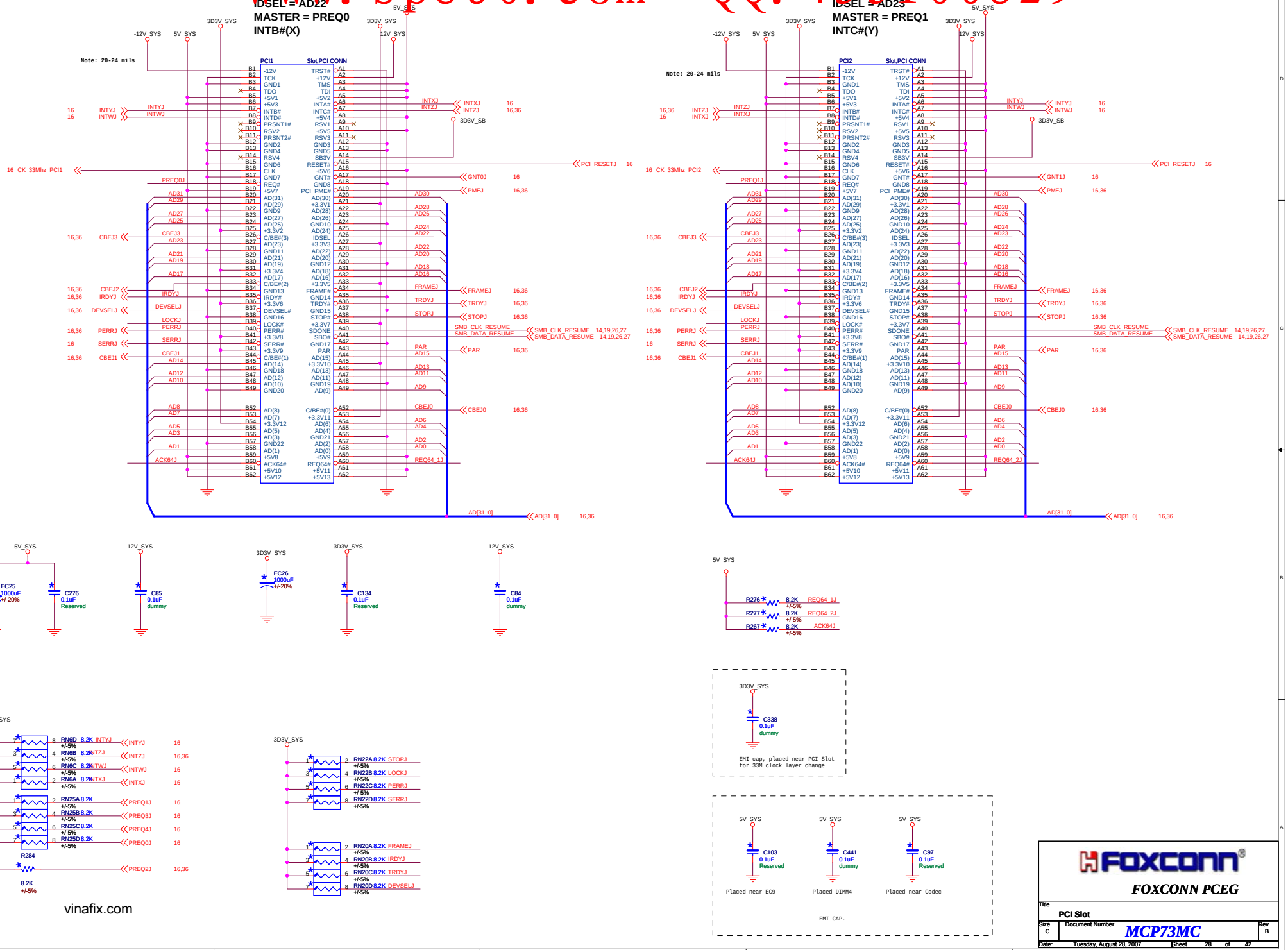

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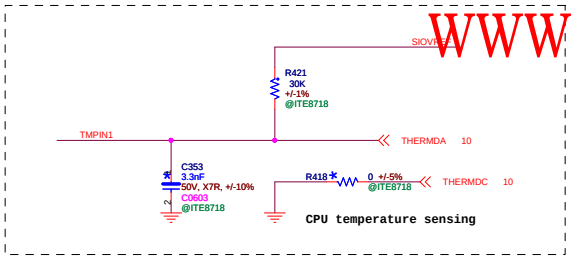

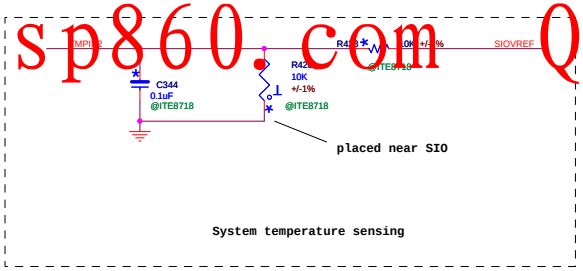

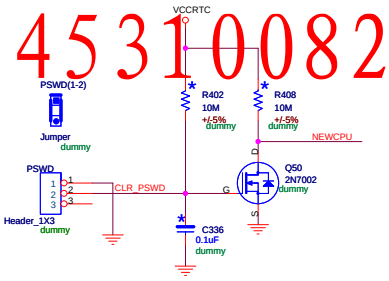

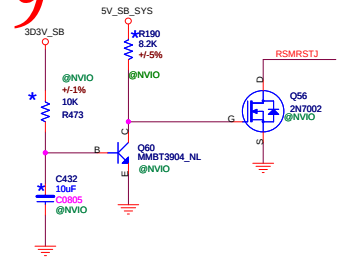

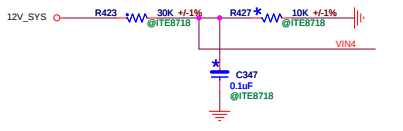

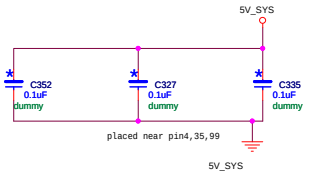

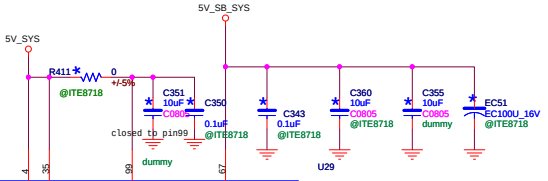

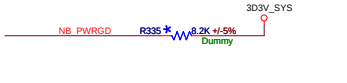

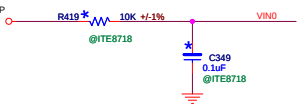

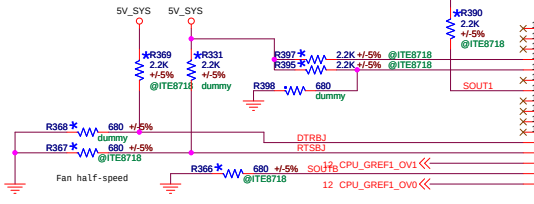

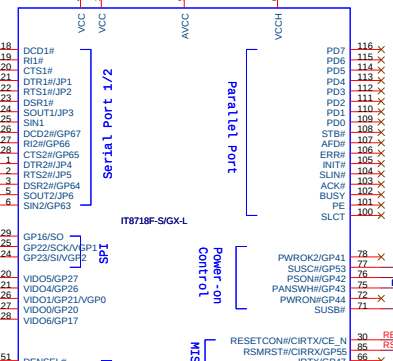

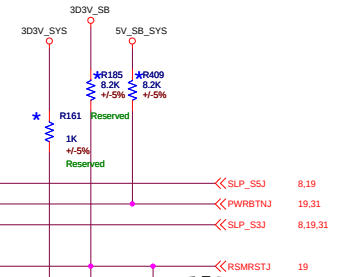

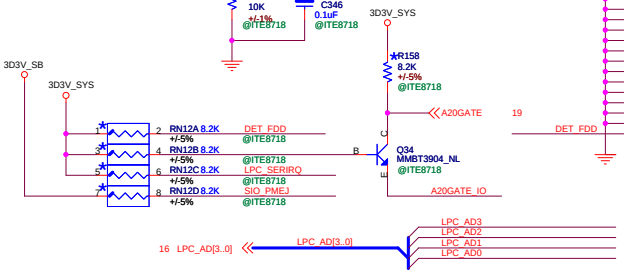

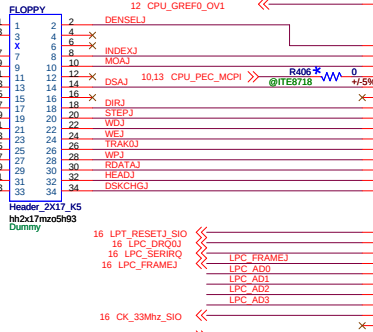

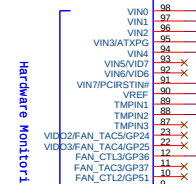

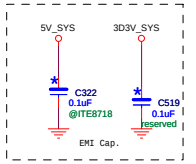

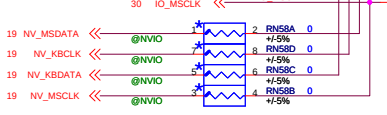

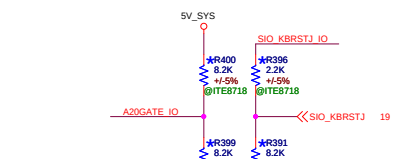

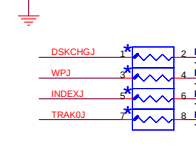

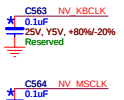

Power On Strapping Options

	Symbol	value	Description
DTR1#/JP1 (pin 121)	Flashseg1_EN	1	Disable
		0	Flash I/F Address Segment1 is enable
RTS1#/JP2 (pin 122)	VID_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
		0	Enable VIDOUT pins
SOUT1/JP3 (pin 124)	CHIP_SEL	--	Chip selection in configuration.
DTR2#/JP4 (pin 1)	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, and PCIRST4# are enhanced open-drain. It will drive high about 10~20ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
RTS2#/JP5 (pin 2)	FAN_CTL_SEL	1	The default of EC index 15h/16h/17h is 00h 100%
		0	The default of EC index 15h/16h/17h is 40h 50%
SOUT2/JP6 (pin 5)	VID_ISEL	1	The threshold voltage of VID is 2.0/0.8V
		0	The threshold voltage of VID is 0.4/0.8V

FOXCONN PCEG

Title: Super I/O IT8718F

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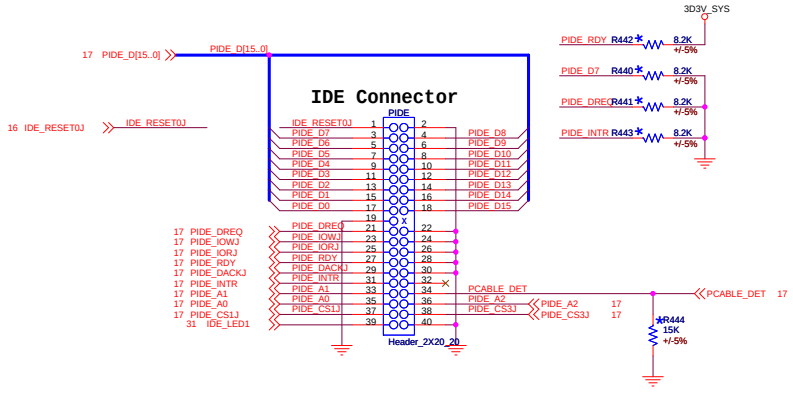

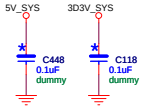

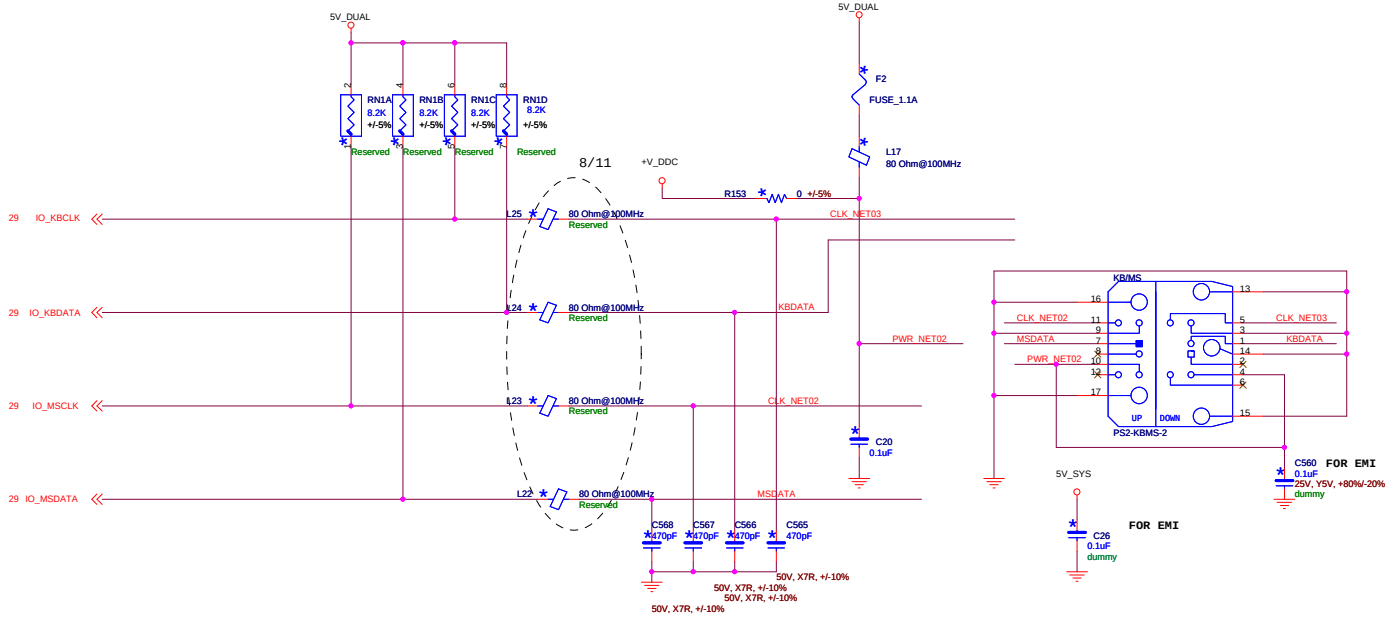

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Title: Serial Port

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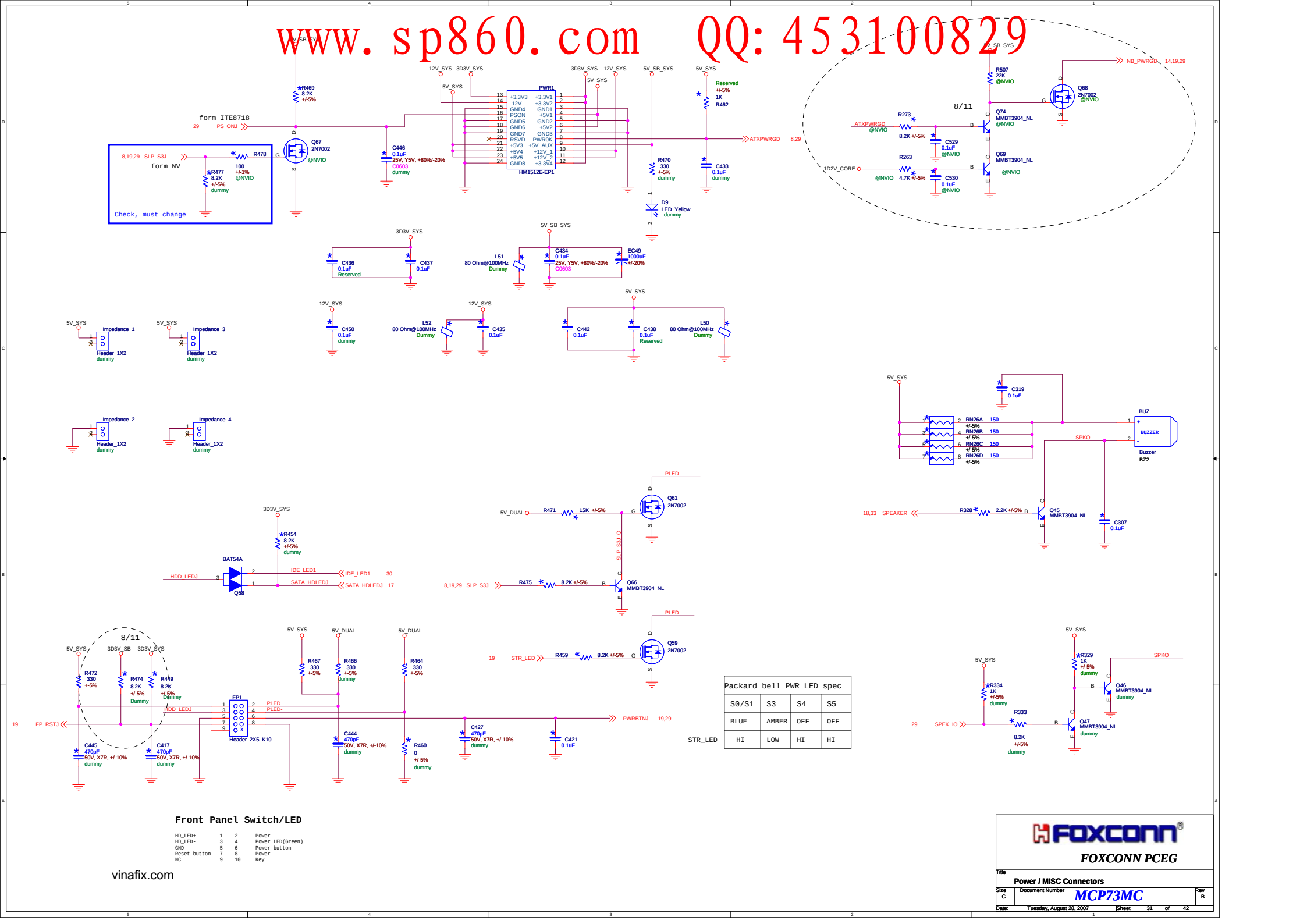

Packard bell PWR LED spec			
S0/S1	S3	S4	S5
BLUE	AMBER	OFF	OFF
HI	LOW	HI	HI

STR_LED

Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Power
NC	9	10	Key

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Title: Power / MISC Connectors

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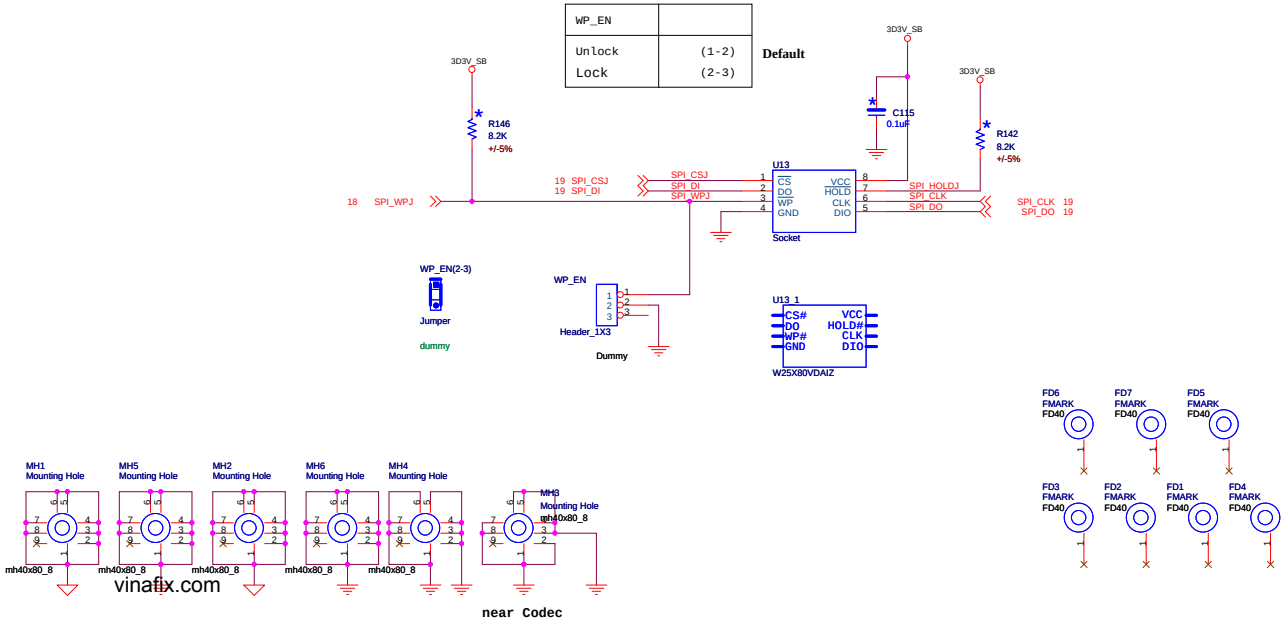
Primary Serial FLASH



near Codec

FOXCONN PCEG

Title: Serial FLASH

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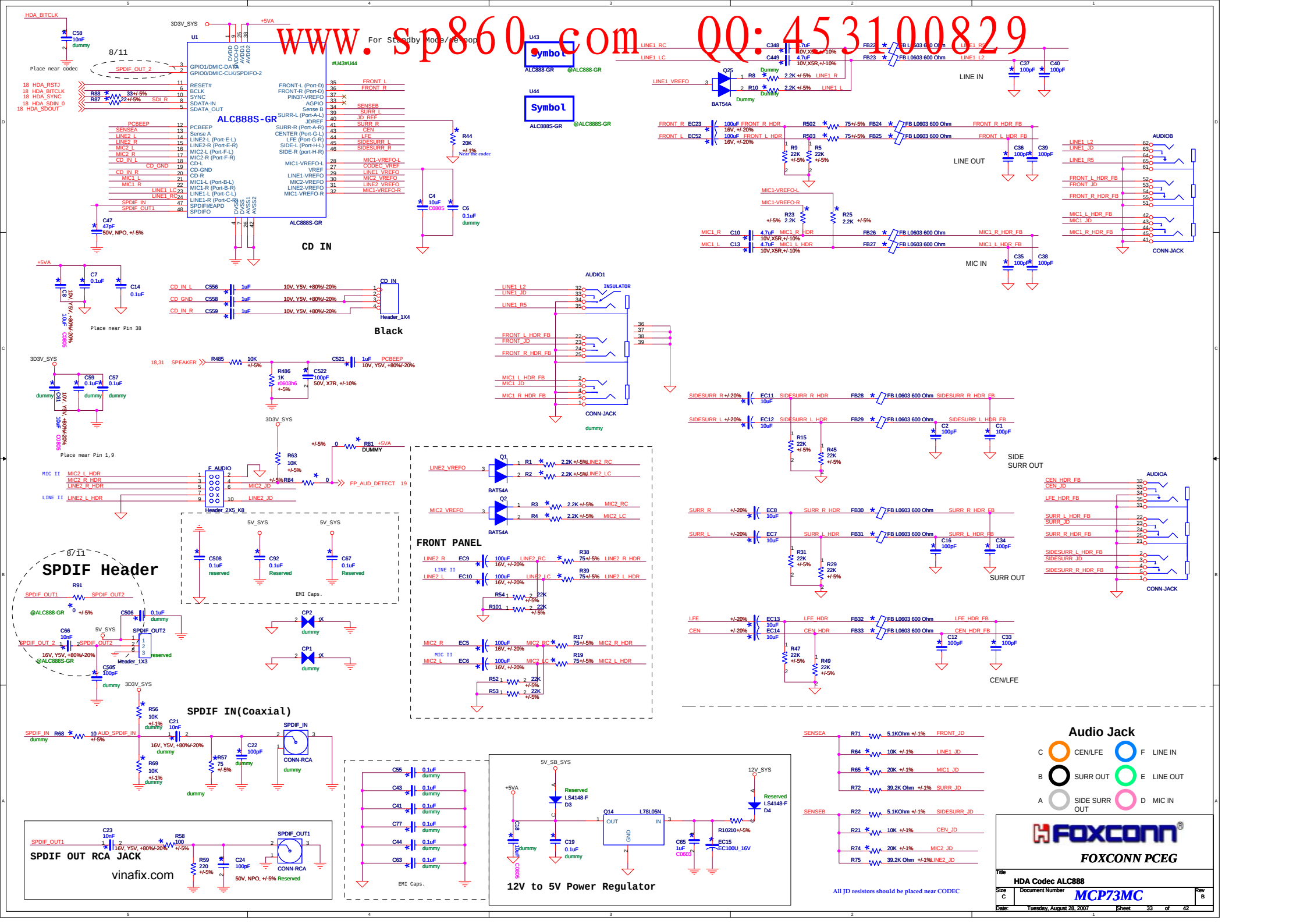
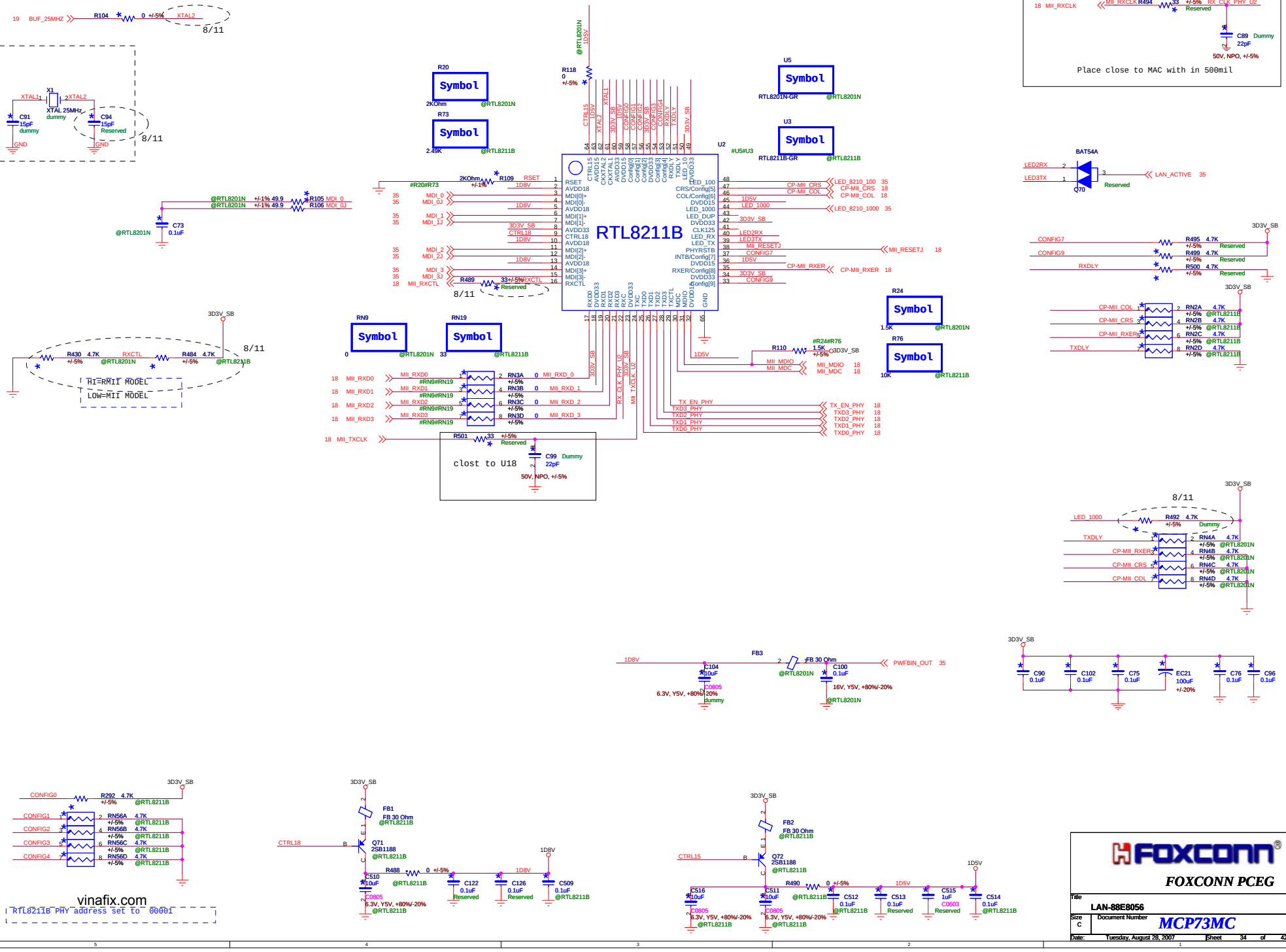
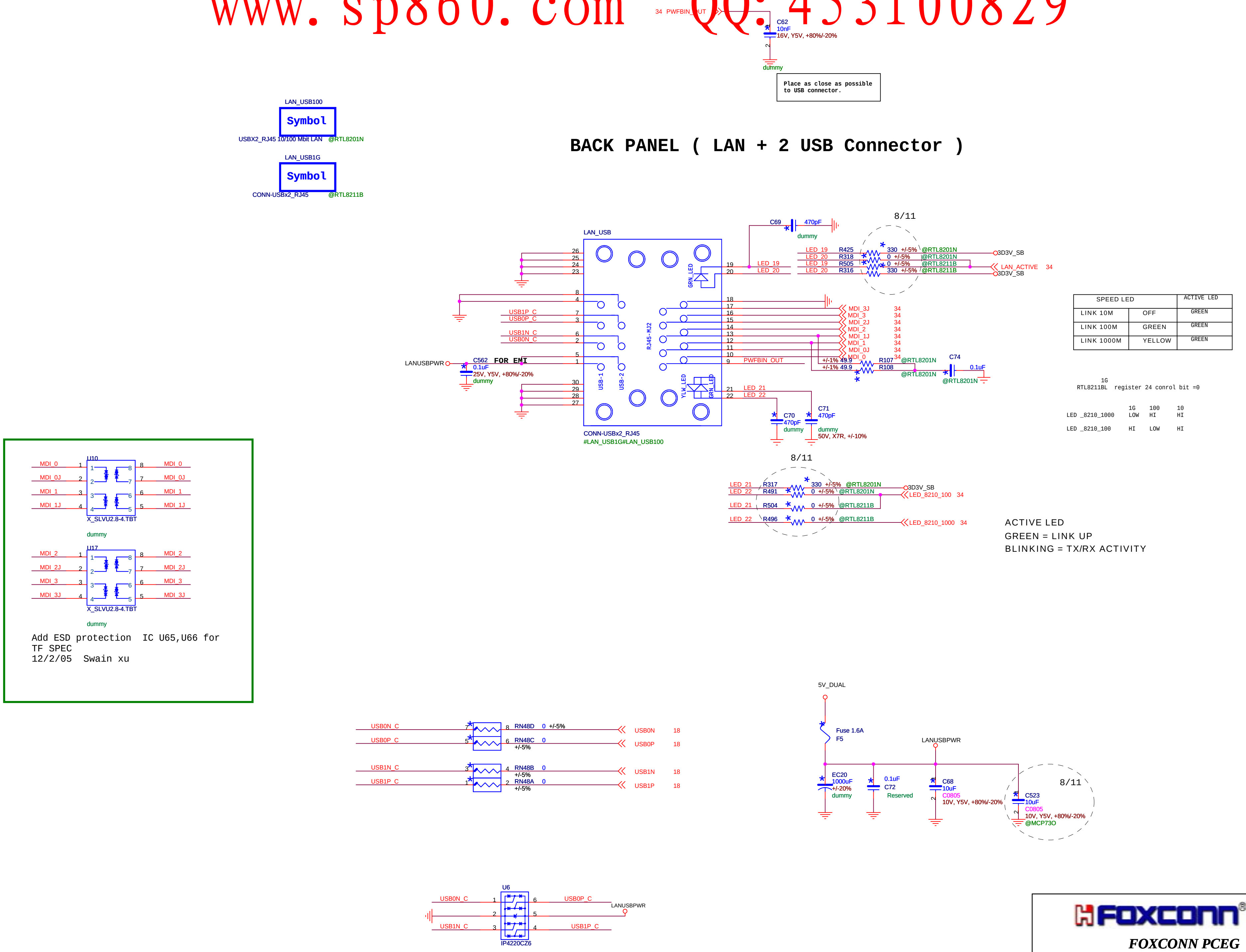




BACK PANEL (LAN + 2 USB Connector)



34 PWFBIN_OUT
C62
10nF
16V, Y5V, +80%/-20%
dummy
Place as close as possible to USB connector.
LAN_USB100
Symbol
USBX2_RJ45 10/100 Mbit LAN @RTL8201N
LAN_USB1G
Symbol
CONN-USBx2_RJ45 @RTL8211B
8/11
C69 470pF dummy
LAN_USB
LED_19
LED_20
R425 330 +/-5% @RTL8201N
R318 0 +/-5% @RTL8201N
R505 0 +/-5% @RTL8211B
R316 330 +/-5% @RTL8211B
3D3V_SB
LAN_ACTIVE 34
USB1P_C
USB0P_C
USB1N_C
USB0N_C
MDI_3J
MDI_3
MDI_2J
MDI_2
MDI_1J
MDI_1
MDI_0J
MDI_0
PWFBIN_OUT
R107 49.9 +/-1% @RTL8201N
R108 49.9 +/-1% @RTL8201N
C74 0.1uF @RTL8201N
LANUSBPWR
C562 0.1uF 25V, Y5V, +80%/-20% dummy
FOR EMI
GRN_LED
YLW_LED
RJ45-MJ2
USB-1
USB-2
LED_21
LED_22
C70 470pF dummy
C71 470pF dummy 50V, X7R, +/-10%
CONN-USBx2_RJ45
#LAN_USB1G#LAN_USB100
8/11
R317 330 +/-5% @RTL8201N
R491 0 +/-5% @RTL8201N
R504 0 +/-5% @RTL8211B
R496 0 +/-5% @RTL8211B
3D3V_SB
LED_8210_100 34
LED_8210_1000 34
U10
X_SLVU2.8-4.TBT
dummy
U17
X_SLVU2.8-4.TBT
dummy
MDI_0
MDI_0J
MDI_1
MDI_1J
MDI_2
MDI_2J
MDI_3
MDI_3J
Add ESD protection IC U65,U66 for TF SPEC
12/2/05 Swain xu
SPEED LED | ACTIVE LED
LINK 10M | OFF | GREEN
LINK 100M | GREEN | GREEN
LINK 1000M | YELLOW | GREEN
1G
RTL8211BL register 24 conrol bit =0
1G 100 10
LED_8210_1000 LOW HI HI
LED_8210_100 HI LOW HI
ACTIVE LED
GREEN = LINK UP
BLINKING = TX/RX ACTIVITY
5V_DUAL
Fuse 1.6A
F5
LANUSBPWR
EC20 1000uF +/-20% dummy
C72 0.1uF Reserved
C68 10uF C0805 10V, Y5V, +80%/-20%
8/11
C523 10uF C0805 10V, Y5V, +80%/-20% @MCP73O
USB0N_C
USB0P_C
USB1N_C
USB1P_C
RN48D 0 +/-5%
RN48C 0 +/-5%
RN48B 0 +/-5%
RN48A 0 +/-5%
USB0N 18
USB0P 18
USB1N 18
USB1P 18
U6
IP4220CZ6
LANUSBPWR

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Title	LAN / USB Connectors	
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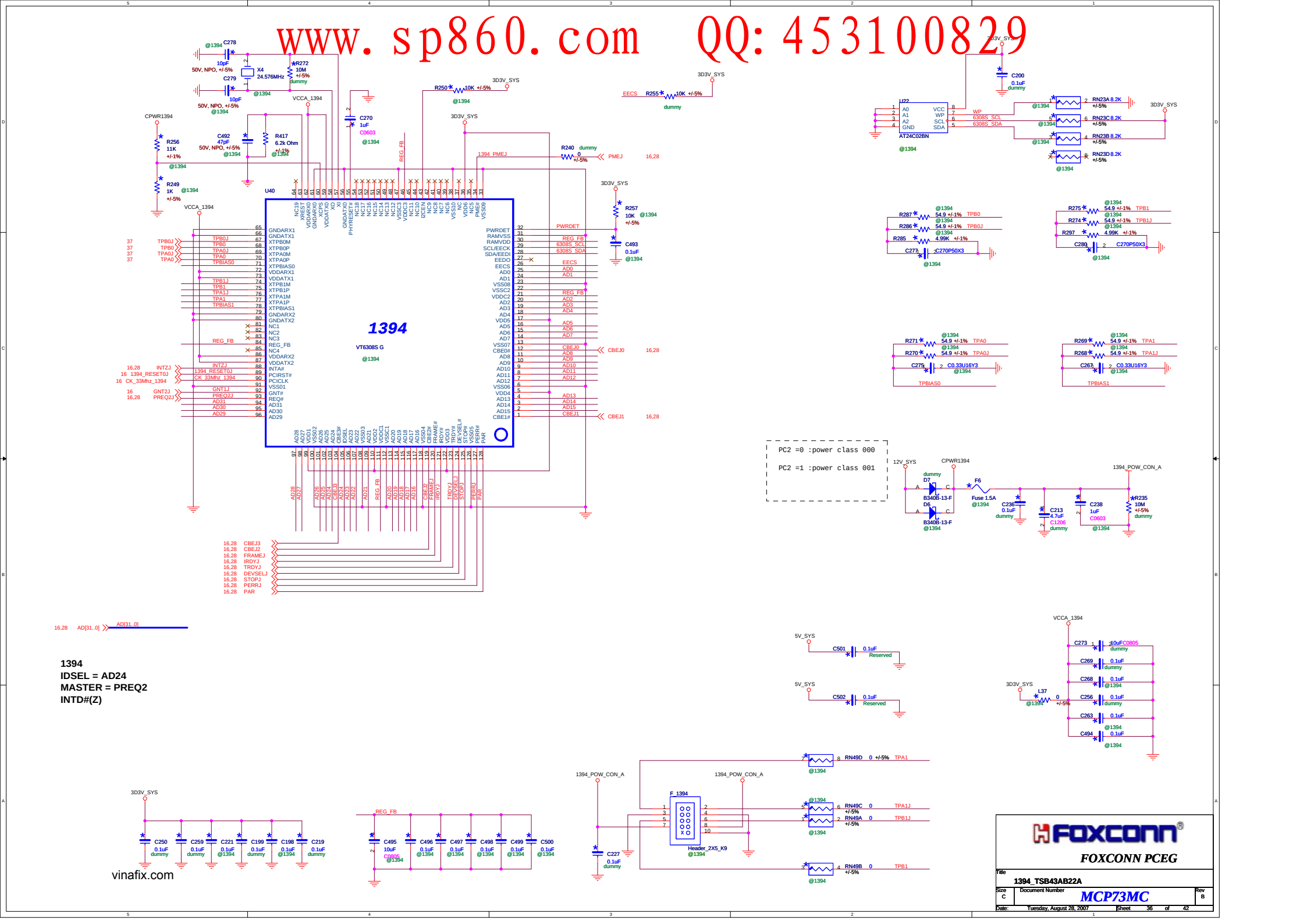

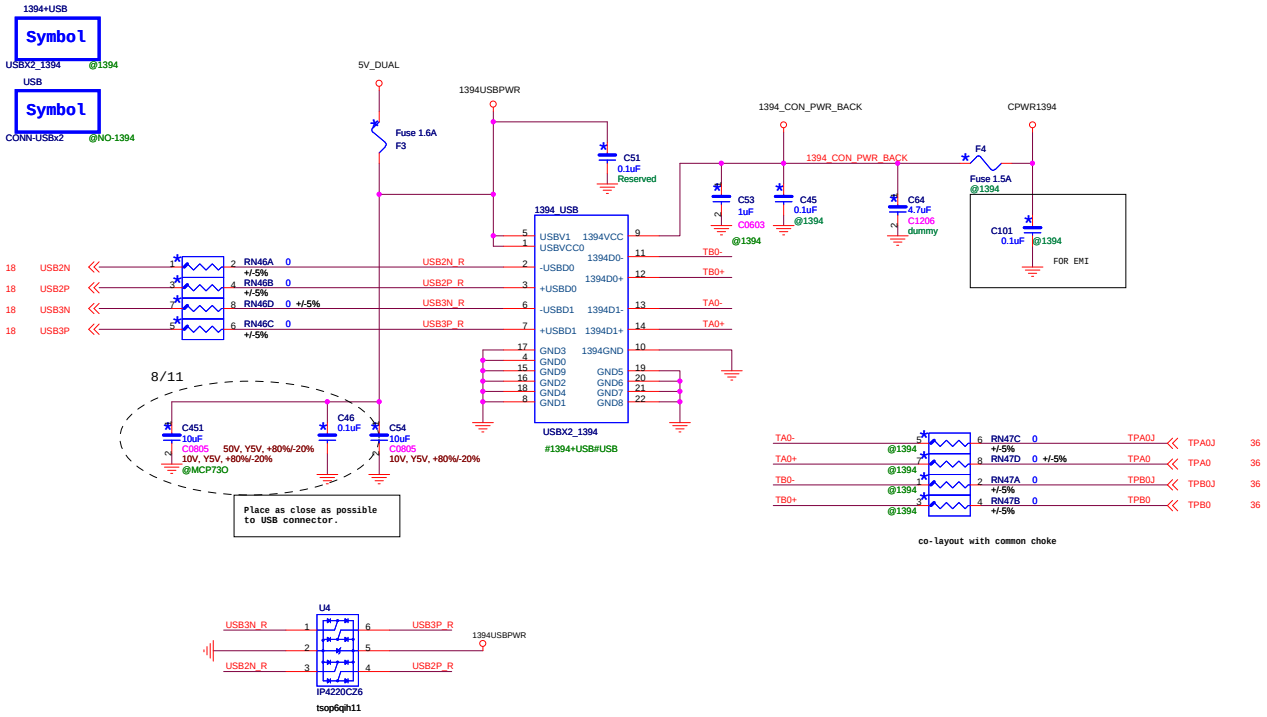

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FOXCONN PCEG

Title: 1394/USB Connectors

Size	Document Number	Rev
C	MCP73MC	B

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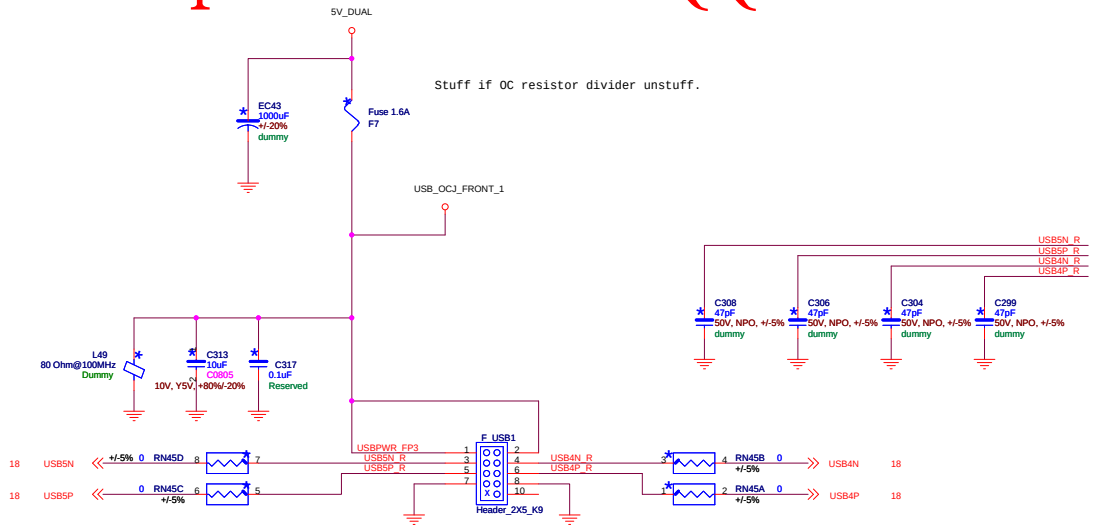
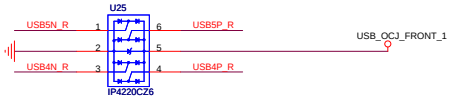
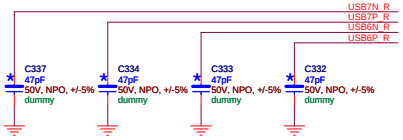
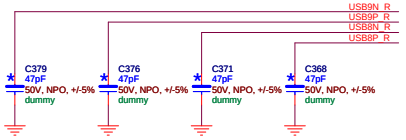
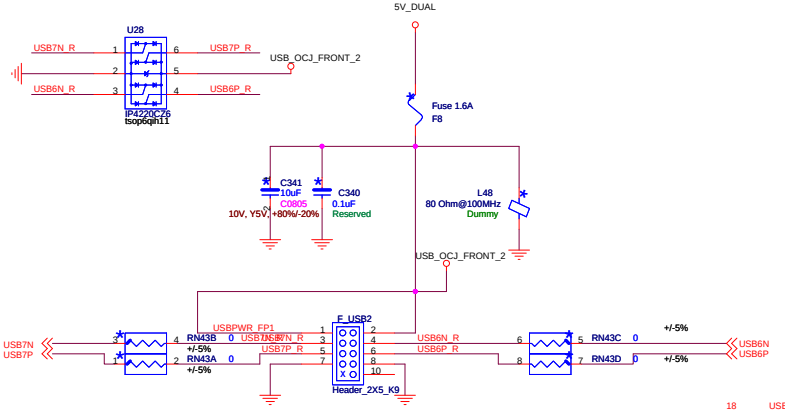


USB Front Header 1

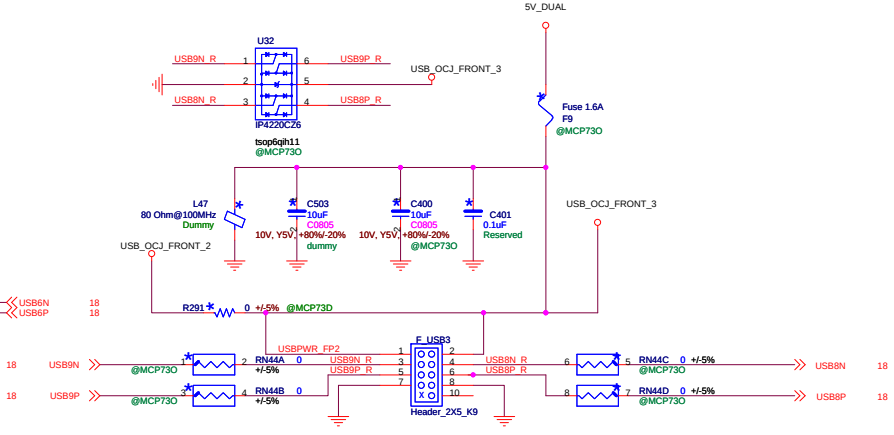




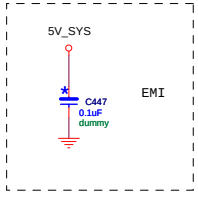




USB Front Header 2



USB Front Header 3



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Title: Front USB Connector			
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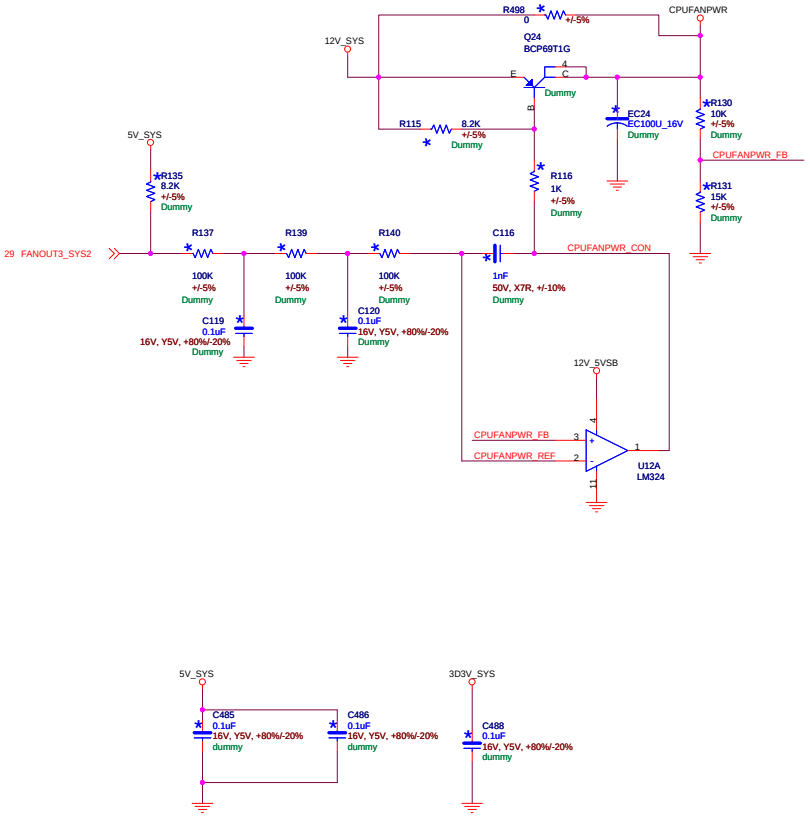
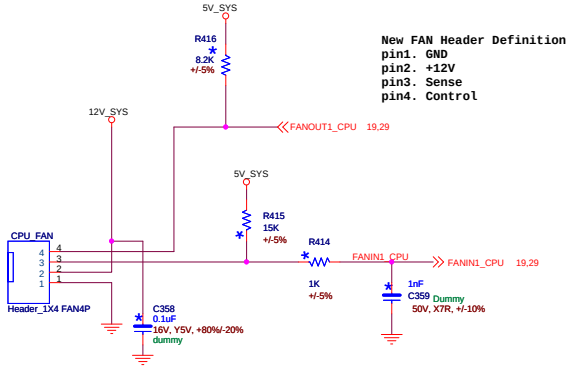
CPU FAN

4-pin FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

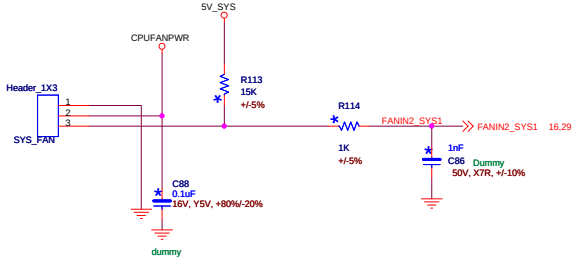
Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%





New FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

New FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense



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Title: CPU / System Fan
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MCP73 GPIO Summary

Offset	Pin Name	Alternate Func	Default	MODE	Drive Tol.
C0h	GPIO1	GPIO1	Normal	8h	+3.3V_DUAL
C1h	GPIO2	GPIO2	GPIO Input	0h	+3.3V_DUAL**
C2h	GPIO3	GPIO3	GPIO Input	0h	+3.3V_DUAL**
C3h	GPIO4	GPIO4	GPIO Input	0h	+3.3V_DUAL
C4h	GPIO5	GPIO5	GPIO Input	0h	+3.3V_DUAL**
C5h	GPIO6	GPIO6	GPIO Input	0h	+3.3V_DUAL
C6h	GPIO7	GPIO7	GPIO Input	0h	+3.3V_DUAL
C7h	GPIO8	GPIO8	Normal	8h	+3.3V_DUAL
C8h	GPIO9	GPIO9	Normal	8h	+3.3V_DUAL
C9h	GPIO10	GPIO10	Normal	8h	+3.3V_DUAL
CAh	GPIO11	GPIO11	Normal	8h	+3.3V_DUAL
CBh	GPIO12	GPIO12	GPIO Input	0h	+3.3V
CCh	GPIO13	GPIO13	Normal	8h	+3.3V
CDh	GPIO14	GPIO14	Normal	8h	+3.3V
CEh	GPIO15	GPIO15	Normal	8h	+3.3V
CFh	PEX4_CLKREQ	GPIO16	Normal	8h	+3.3V
D0h	PEX5_CLKREQ	GPIO17	Normal	8h	+3.3V
D1h	PEX6_CLKREQ	GPIO18	Normal	8h	+3.3V
D2h	LPC_DRQ1	GPIO19	GPIO Input	0h	+3.3V
D3h	PROCHOT	GPIO20	Normal	8h	+3.3V_DUAL**
D4h	PE_WAKE	GPIO21	Normal	8h	+3.3V_DUAL
D5h	AC_SDATA0		Normal	8h	+3.3V_DUAL
D6h	AC_SDATA1		Normal	8h	+3.3V_DUAL
D7h	AC_SDATA2	GPIO24	Normal	8h	+3.3V_DUAL
D8h	USB_OC0	GPIO25	Normal	8h	+3.3V_DUAL
D9h	USB_OC1	GPIO26	Normal	8h	+3.3V_DUAL
DAh	USB_OC2	GPIO27	Normal	8h	+3.3V_DUAL
DBh	USB_OC3	GPIO28	Normal	8h	+3.3V_DUAL
DCh	USB_OC4	GPIO29	Normal	8h	+3.3V_DUAL
DDh	PCI_PME	GPIO30	Normal	8h	+3.3V_DUAL
DEh	SIO_PME	GPIO31	Normal	8h	+3.3V_DUAL
DFh	EXTSMI	GPIO32	Normal	8h	+3.3V_DUAL**
E0h	RI	GPIO33	Normal	8h	+3.3V_DUAL
E1h	SUS_CLK	GPIO34	Normal	8h	+3.3V_DUAL
E2h	MII0_INTR	GPIO35	Normal	8h	+3.3V_DUAL
E3h	MII0_RXER	GPIO36	Normal	8h	+3.3V_DUAL
E4h	MII0_PHY_PWRDN	GPIO37	Normal	8h	+3.3V_DUAL
E5h	PCI_REQ3	GPIO38	GPIO Input	0h	+5.0V
E6h	PCI_GNT3	GPIO39	GPIO Output	0h	+5.0V
E7h	PCI_REQ2	GPIO40	GPIO Input	0h	+5.0V
E8h	PCI_GNT2	GPIO41	GPIO Output	0h	+5.0V
E9h	PCI_CLKRUN	GPIO42	Normal	8h	+5.0V
EAh	PCI_PERR	GPIO43	GPIO Input	0h	+5.0V
EBh	AC_SYNC	GPIO44	Normal	8h	+3.3V
ECh	AC_SDATA_OUT	GPIO45	Normal	8h	+3.3V
EDh	AC_DOCK_RST_L	GPIO46	Normal	8h	+3.3V_DUAL
EEh	THERM_SID1	GPIO47	Normal	8h	+3.3V_DUAL**
EFh	THERM_SIC	GPIO48	Normal	8h	+3.3V_DUAL**
F0h	THERM_SID	GPIO49	Normal	8h	+3.3V_DUAL**
F1h	LPC_DRQ0	GPIO50	Normal	8h	+3.3V
F2h	AC_DOCK_EN_L	GPIO51	Normal	8h	+3.3V_DUAL
F3h	PCI_REQ4	GPIO52	GPIO Input	0h	+5.0V
F4h	PCI_GNT4	GPIO53	GPIO Output	0h	+5.0V
F5h	LPC_PD	GPIO54	Normal	8h	+3.3V
F6h	A20GATE	GPIO55	Normal	8h	+3.3V
F7h	KBDRSTIN	GPIO56	Normal	8h	+3.3V
F8h	SATA_LED	GPIO57	Normal	8h	+3.3V
F9h	THERMTRIP	GPIO58	Normal	8h	+3.3V_DUAL**
FAh	THERM	GPIO59	Normal	8h	+3.3V
FBh	FANRPM	GPIO60	Normal	8h	+3.3V
FCh	FANCTL0	GPIO61	Normal	8h	+3.3V
FDh	FANCTL1	GPIO62	Normal	8h	+3.3V
FEh	CABLE_DET_P	GPIO63	Normal	8h	+5.0V
FFh	SMB_ALERT	GPIO64	Normal	8h	+3.3V_DUAL

Note.

** - These pins are powered by the 3.3V_DUAL rail, but they will not operate correctly when the system is in low power system states when PWRGD is not asserted (S3-S5). Use other 3.3V_DUAL powered pins without ** for low power state operation. These pins will work as expected during states where PWRGD is asserted (S0, S1).

MCP73 GPIO Use

Pin Name	Function
GPIO6	STR_LED
GPIO7	FP_AUD_DETECT
GPIO23	WP_EN

I/O ITE8718F/G GPIO Use

Pin Name	Function
GP16	CPU_GREF0_OV0
GP17	CPU_GREF0_OV1
GP63	CPU_GREF1_OV0
GP64	CPU_GREF1_OV1
GP20	DDR_OV0
GP21	DDR_OV1
GP22	FDD_Detect
GP26	Ext_SMI
GP40	3VSBSWJ

PCI Routing Summary

	PCI1	1394
INTWJ	Y	Z
INTXJ	Z	
INTYJ	W	
INTZJ	X	
REG#/GNT#	0	1
IDSEL	22	23

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Title: GPIO / IRQ / IDSEL Map

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Jumper Setting Summary

CLR_CMOS	**Clear CMOS** 1-2 : Clear CMOS 2-3 : Normal (Default)
PSWD	**Clear Password** 1-2 : Clear PSWD 2-3 : Normal (Default)

Strapping Pins

Signal Name	Strapped Value	Description
SPKR	0 = User Mode Boot Init table (default) 1 = Safe Mode Boot Init table	Selects between a USER and SAFE table for boot initialization parameters. 10 k to GND : USER mode boot 10 k to +3.3V: SAFE mode boot
HDA_SYNC / GPIO_44	0 = 14.31818 MHz 1 = 24 MHz (default)	Selects the SIO clock to be either 14.31818 MHz or 24 MHz 10 k to GND : 14.31818 MHz 10 k to +3.3V : 24 MHz
HDA_RESET#	0 = MII (default) 1 = RGMII	Selects between the MII and RGMII interface for MCP67 MAC 10 k to GND : MII 10 k to +3.3V_DUAL : RGMII
HDA_SDATA_OUT0 (MSB) LPC_FRAME# (LSB)	00 = LPC BIOS 01 = PCI BIOS 10 = SPI BIOS (default) 11 = Reserved (SPI BIOS)	Select which bus the BIOS will be executed from 8.2 k to GND or 8.2 k to +3.3V
SPI_DO / GPIO_9 (MSB) SPI_CLK / GPIO_11 (LSB)	00 = 31 MHz 01 = 42 MHz 10 = 25 MHz (default) 11 = 1 MHz	Selects the clock frequency for the SPI EEPROM 8.2 k to GND or 8.2 k to +3.3V_DUAL

FOXCONN PCEG

Title: Jumper Setting / Option Table

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Title: Modify List

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