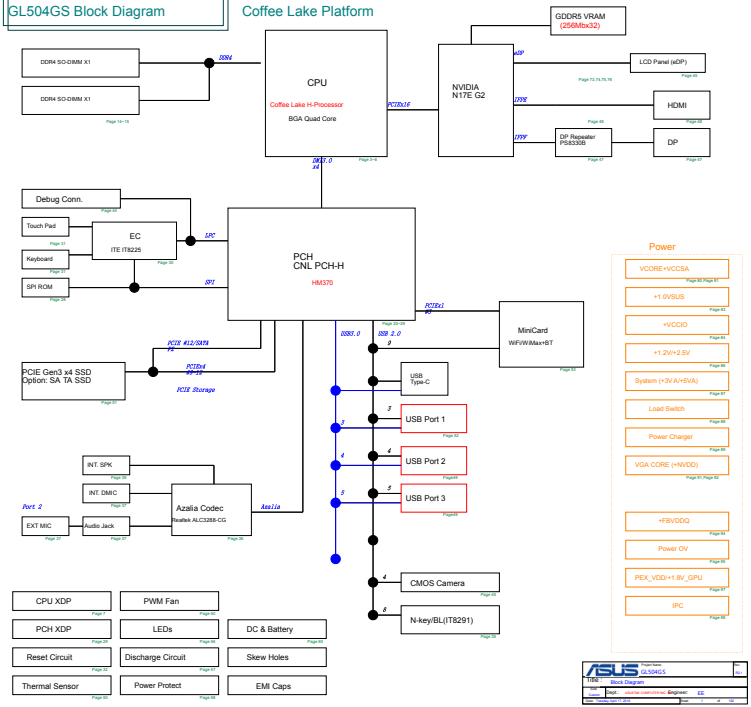
GL504GS Block Diagram

Coffee Lake Platform



ASUS	Project Name: GL504GS		Rev:
Title: Block Diagram			
Size:	Document Number:		Rev:
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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQ0#_X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_GLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/NV_GPU_EVENT#		PU 10K(@)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/NV_GC6_FB_EN		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2			
GPP_C3	SML0CLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(@)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 1K	
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT		PU 10K	+VCC3V3_SX
GPP_D1	GPI	GPO	GPIO_3_FORCE_PWR		PD 10K	
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#			
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID			
GPP_D12	GPI	Strap	TOUCH_PANEL_ID			
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(@)	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET2		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)			
GPP_E4	GPI	Native	NGFF0_DEVSLP			
GPP_E5	GPI	Native	(N.C)			
GPP_E6	GPI	Native	NGFF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(@)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1			
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1			
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_USB31#_X1		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 100K	
GPP_I1	GPI	Native	(N.C)		PD 100K	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	Native	(N.C)			
GPP_I4	GPI	Native	GPP_I4		PD 100K	
GPP_I5	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)		PU 2.2K(@)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	NKey_WRST	PD 10k	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4/INTR#	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN#_wCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K(@)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH		
GPG4	GPI		EC_SI/EC_SI_PCH		
GPG5	GPI		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VBUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K(@)	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	KB_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
SO-DIMM A(0)	A0h	
SO-DIMM B(0)	A2h	
EC Master (SMB1)	SM-Bus Address	
SM-Bus Device		
VGA Thermal Sensor	9Eh	
CPU Thermal Sensor	90h	
Power Thermal Sensor	7Eh	

Device Identification

CPU Thermal Sensor		
1st	06G023123010	NCT7717U
2nd		

N501VW PCIE & USB Function define

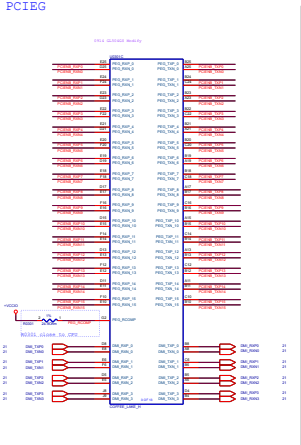
Skylake HM170

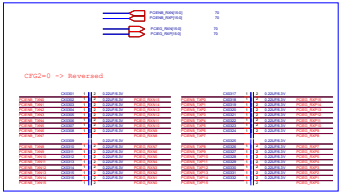
HSIO	HSIO Capabilies	Funcon	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 Port1	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3.0 Port3	
06	USB3#06	USB3.0 Port4	
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	LAN	SRC4
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA#1 SSD	SRC6
16	PCIE#10 / SATA#1	PCIE*4 SSD	
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	SATA#3 HDD	
23			
24			
25			
26			

USB 2.0	Funcon
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	XBOX
USB2_04	Camera
USB2_05	USB3.0 MB Port3
USB2_06	USB3.0 MB Port4
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

ASUS	Project Name: GL504GS	Rev: R2.1
Title : System Setting		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 2 of 102	

PCIEG





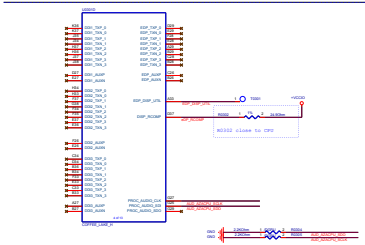


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CFG-0 PDG P.243 (Doc.571991)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

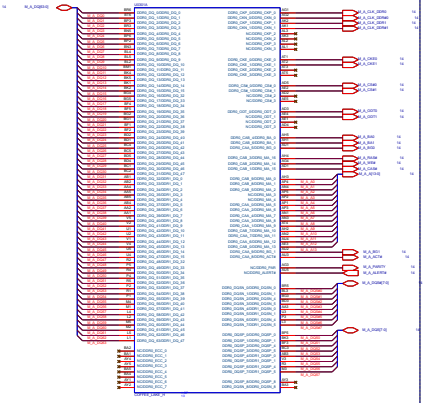
When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

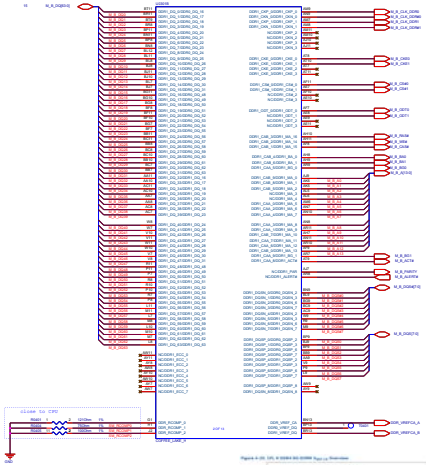
ASUS	Project Name: GL504GS	Rev: 0.1	
Title: CPU_DMI,PEG,FDI,eDP			
Size:	Dept.: Mobile/NB COMPUTER INC.	Engineer:	NB1 RD2 EE1
A			
Date: Tuesday, April 17, 2018		Sheet 1 of 102	

Memory Channel A

Memory Channel B

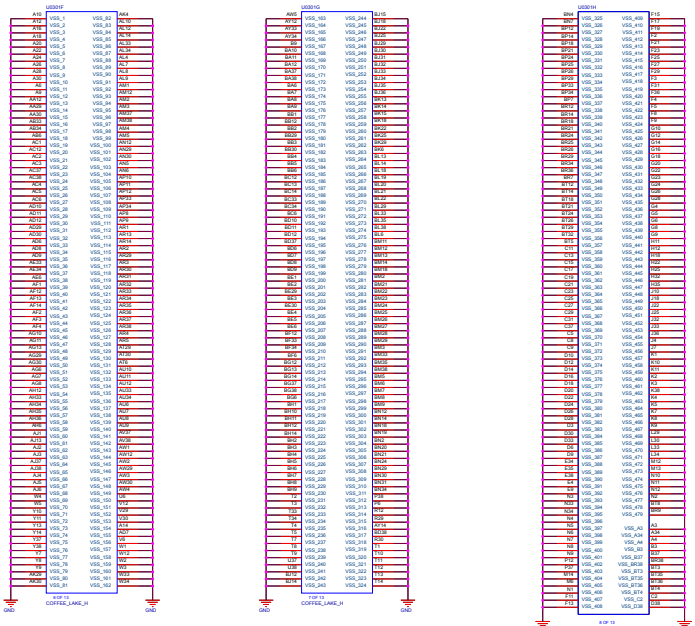
Main Board





ASUS	Project Name: GL504GS		Rev: REV
Title: CPU_DDR4			
Size: A	Dept: All of the COMPUTER Inc	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018		Sheet: 6	of: 100

Main Board



www.teknisi-indonesia.com

Project Name: GL504GS			Rev: 82.1
Title: CPU_GND			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018	Sheet: 5	of: 102	

Main Board

CFG

Boundary Scan

CFG Straps

CFG Straps for Processor

CFG[0] : Stall reset sequence after PCU PLL lock until de-asser ted
- 1 : (default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : (default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable
- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation
- 00 : 1 x8, 2 x4 PCI Express*
- 01 : 2 x8 PCI Express*
- 10 : 2 x4 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training
- 1 : (Default) PEG Train immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training.

CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

Refer : Intel 570605_CFL_S0S_Vol1_Rev1.3, Table 6-7, P.116

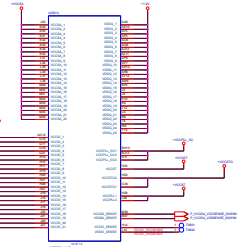
DDR_VTT_CNTL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator in C8 and deeper and S3.

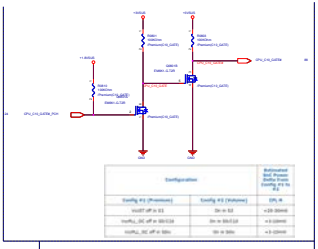
VTT Enable

CPU SIDEBAND SIGNALS

ASUSTeK COMPUTER INC.
Project Name: GL504GS
Rev: 0.1
Title: CPU_CFG,RSVD
Size: C
Document Number: Engineer: NB1 RD2 EE1
Date: Tuesday, April 17, 2018
Sheet 6 of 100

Main Board

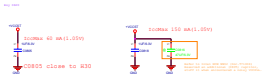




Configuration		Estimated Platform Battery Life Config #1 Vs #2
Config #1 (Premium)	Config #2 (Volume)	Diff, H
VccST off in S3	3h in S3	+2h 30min
VccPLL_OC off in S0ix24	3m in S0ix12	+10 (min)
VccPLL_OC off in S0ix	0h in S0ix	+3 (min)

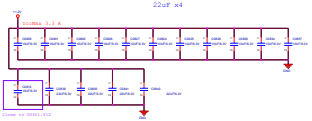
Main Source	1st PWR	2nd PWR	3rd PWR
AC_BAT_SYS	1.8VSPUS	+VCCIO	+1.05V_VCCIO
		+VCCSFR	+1.05V_VCCPLL
	1.1_LP	+VDDQ_LPDDR	
		+VCCSRAM_LPDDR	
	+VCCSA		
	+VCCSTG		

+VCCST/+VCCPLL
DECAPS Place Back Side (TOP)

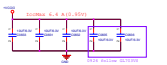


+VDDQ DECAPS Place Back Side (TOP)

10UF x 11
22uF x4

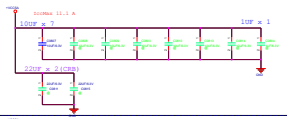


+VCCIO DECAPS Place Back Side (TOP)



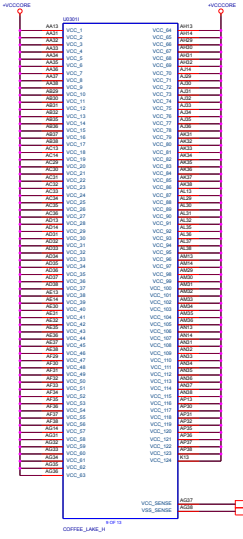
+VCCPLL_OC DECAPS Place Back Side (TOP)

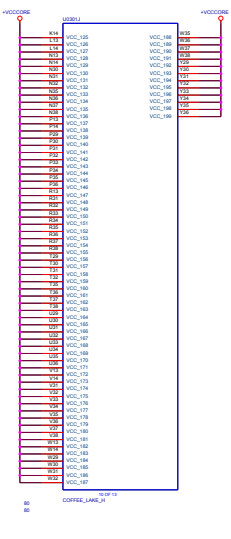
+VCCSA DECAPS Place Back Side (TOP)



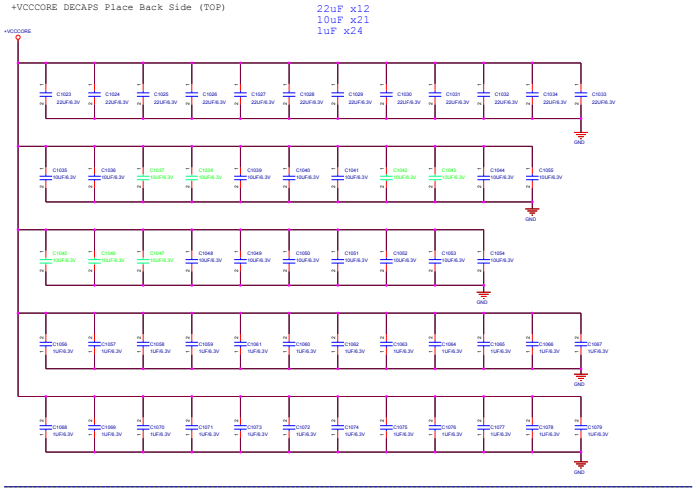
+VCCSA cap near CPU

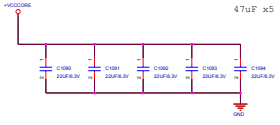
+VCCSTG DECAPS Place Back Side (TOP)





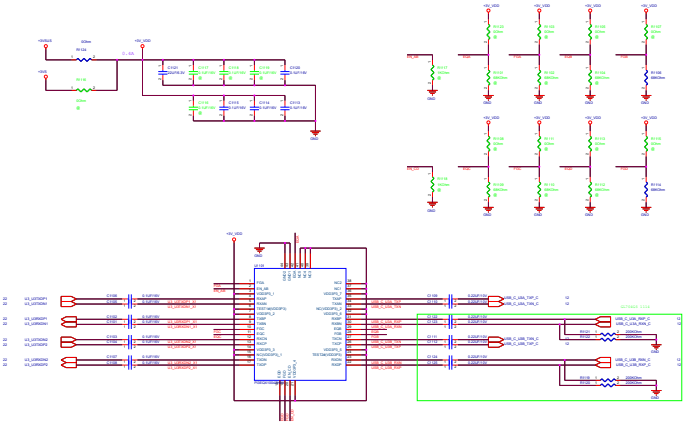
ASUS	Project Name	GL504GS		Rev	
				RD 1	
Title :	CPU_PWR				
Size	Dept. :	ASUSTeK COMPUTER INC	Engineer:	NB1 RD2 EE1	
B					
Date:	Tuesday, April 17, 2018		Sheet	8 of 102	





ASUS	Project Name: GL504GS	Rev: R2.1
Title : CPU_POWER_CAP		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Tuesday, April 17, 2018	Sheet 10 of 102	

Main Board



	Equalizer setting(dB)
HZ R/W/C/D	0500a
0(k to Gnd)	10.9
N(Heat to Gnd)	6.7
F(Floating)	8.9
1(S to VDD)	13.1

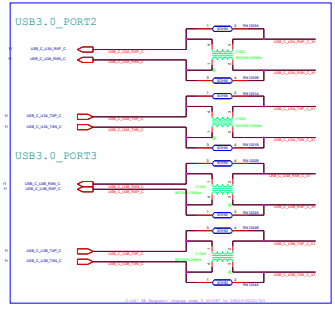
	Flat Gain setting
FS R/W/C/D	x8
0(k to Gnd)	-3
N(Heat to Gnd)	-1.5
F(Floating)	0
1(S to VDD)	+2

	Channel Enable setting
ES	With internal 200kohm pull-up Resister
0	Disable
1	Enable

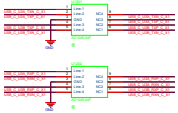
ASUS	Compal Electronics, Inc.	GL504GS	Rev 1.0
Title :	TBT_Alpine-Ridge		
Size	Document Number		
Date: Tuesday, April 17, 2018	Sheet	of	
Dept:	ASUSTeK COMPUTER INC.	Engineer:	NB1 RD2 EE1

Main Board

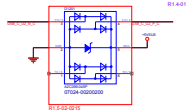
PCH USB3.0 / USB2.0



USB3.0 ESD-Protection



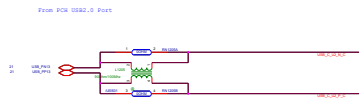
USB2.0 ESD-Protection



U4702 & U4703 ESD PROTECTION 1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F 2nd Source: P/N:07G028153010 ESD PROTECTION SP4024MC210-TB	D4701 ESD Diode 1st Source: P/N:07024-00200200 AMAZING/AZC099-04S1F RTG 2nd Source: P/N:07024-00710000 NXP/PLUSE2K40

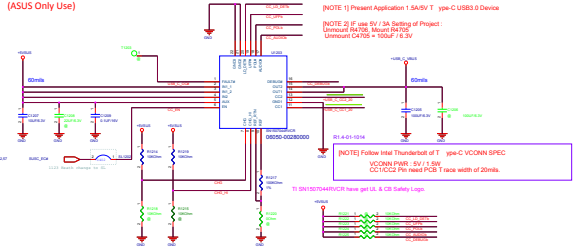
TYPE-C Connector

USB2.0 EMI-Protection With ECMF(PCB 1.2mm_/Layer)



TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A

(ASUS Only Use)



[NOTE 1] Present Application 1.5A/5V T ype-C USB3.0 Device

[NOTE 2] IF use 5V / 3A Setting of Project :
Unmount R4705, Mount R4705
Unmount C4705 = 100uF / 6.3V

[NOTE] Follow Intel Thunderbolt of T ype-C VCONN SPEC
VCONN PWR : 5V / 1.5W
CC1/CC2 Pin need PCB T race width of 20mils.

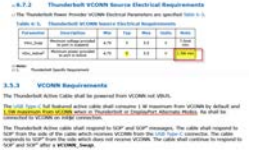
TI SN1507044RVCR have get UL & CB Safety Logo.

[NOTE] Vendor TI got New Name for ASUS Only , so TI SN1507044RVCR=TPS25810RVCR.
Please Follow Design IP : TYPE-C CC Logic IC need use P/N:06050-00280000 TI/SN1507044R VCR

Set CC
I limit = 1.7A

Table 1. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A



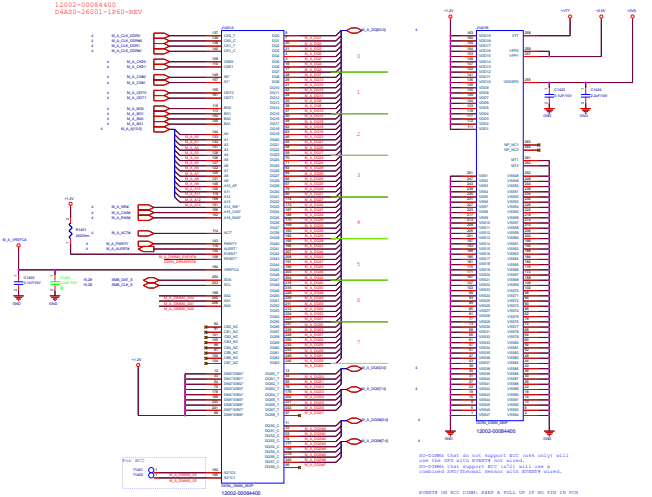
[NOTE] PCH USB3.0 & Asmedia USB3.1 Co-layout of Design Rule :

1. Co-layout 元件擺置，盡量離TYPE-C Connector 越近越好。
2. Co-layout Y -型走線要越短越好。

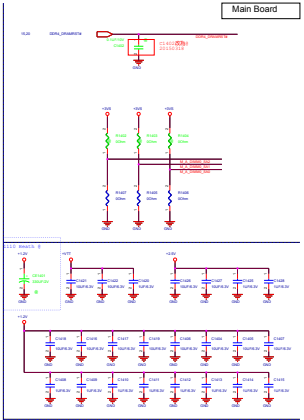
ASUS	Compal Electronics, Inc.		Rev:
	GL40405		0.1
Title :	T87_TPS65983 C		
Size: D	Dept: ASUSTeK COMPUTER INC.	Engineer:	N81 R02 EE1
Date: Tuesday, April 17, 2018		Sheet 10 of 102	

SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

12002-00084400
D4AS0-26001-1P60-REV



Main Board



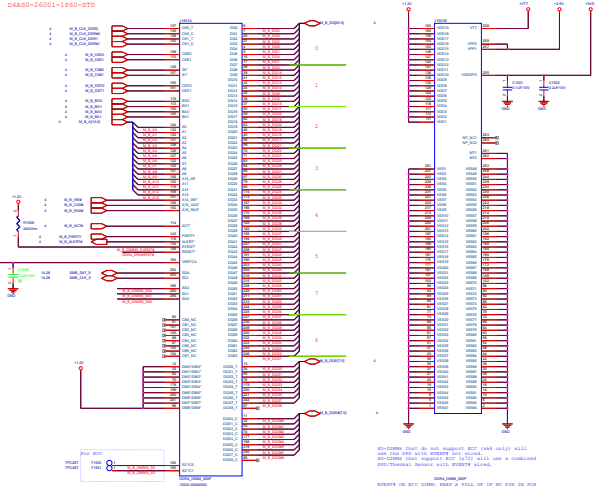
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From RT8450)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

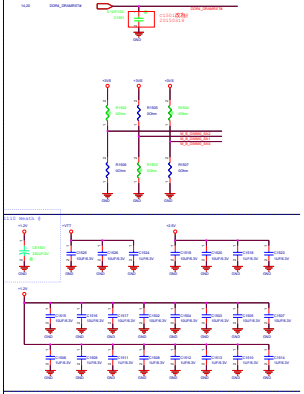
ASUS	Project Name: G1.SIM2S	Rev: REV:
Title :	DIM_DDR4 SO-DIMM A1	
Size: D	Dept: ASUSTeK COMPUTER INC	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 1 of 1	

Main Board

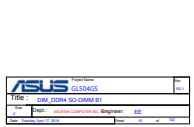
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1501)

12002-00084500
D4AS0-26001-1P60-STD



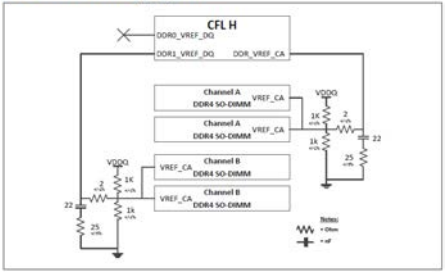


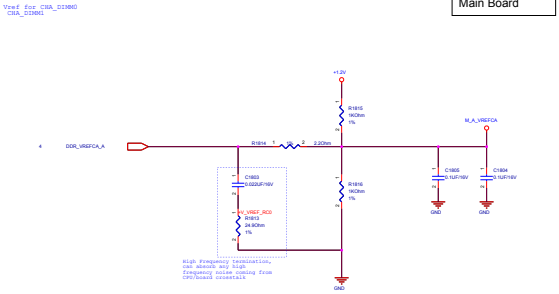
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From RT8603)
		M_A_VREFCA (0.6V From rt.2V)
	+3VA_DDR	+3VS
		+2.5V



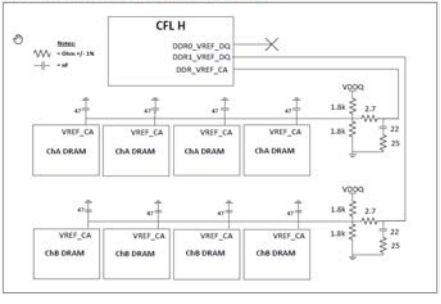
Main Board

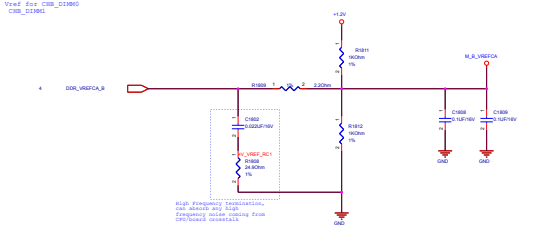
CFL H DDR4 SO-DIMM V_{REF-CA} Overview



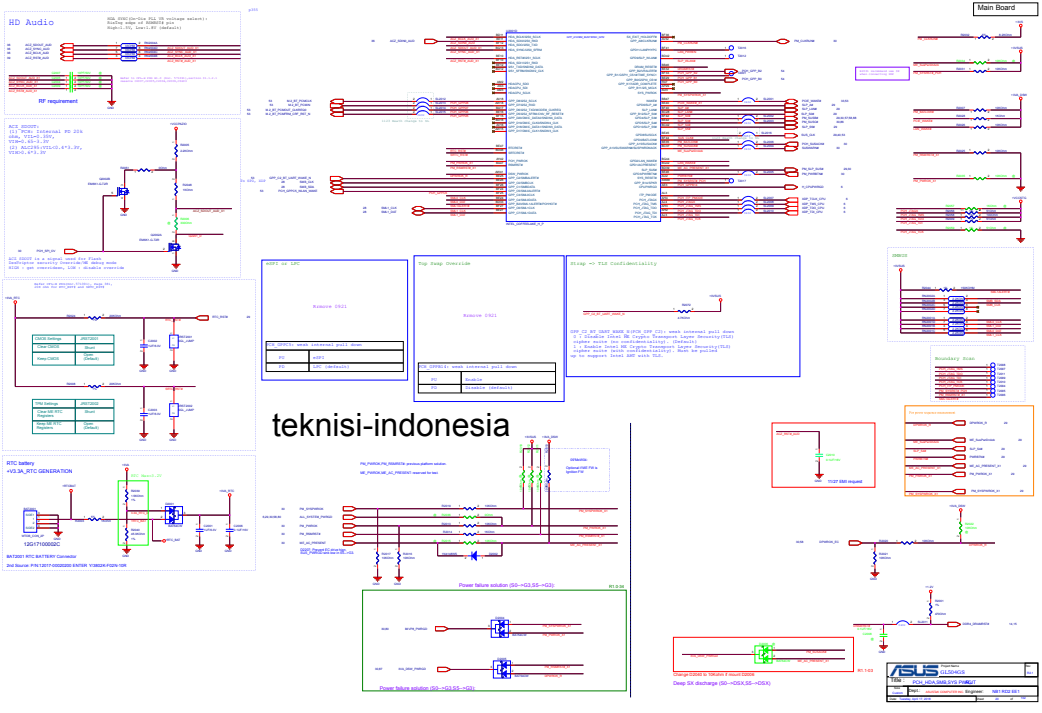


CFL H DDR4 x16 Memory Down V_{REF-CA} Overview





ASUS	Project Name: GL504GS		Rev: R2.1
Title :	DIM_CA/DQ Image		
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018		Sheet 18 of 102	


Main Board
HD Audio
RF requirement
RTC battery
+V3.3A_RTC GENERATION
SATA001 RTC BATTERY Connector
2nd Source: P/N:12017-000020200 ENTER: Y1386241-F0276-10R
12017Y0000021
Power failure solution (S0->G2,S5->G3)
Power failure solution (S0->G3,S5->G3)
Deep SX discharge (S0->DSX,S5->DSX)
teknisi-indonesia

Main Board

USB Setting

USB 2.0	
USB2_01	
USB2_02	
USB2_03	USB3.1 type A
USB2_04	USB3.1 type A
USB2_05	USB3.1 type A
USB2_06	
USB2_07	
USB2_08	
USB2_09	Camera
USB2_10	N-Key + KB BL control
USB2_11	BT
USB2_12	
USB2_13	USB3.1 type C
USB2_14	

USB 3.0	
USB3_01	USB3.1 type C
USB3_02	
USB3_03	USB3.1 type A
USB3_04	USB3.1 type A
USB3_05	USB3.1 type A
USB3_06	
USB3_07	Card Reader
USB3_08	

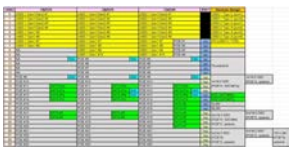
USB3 Card Reader

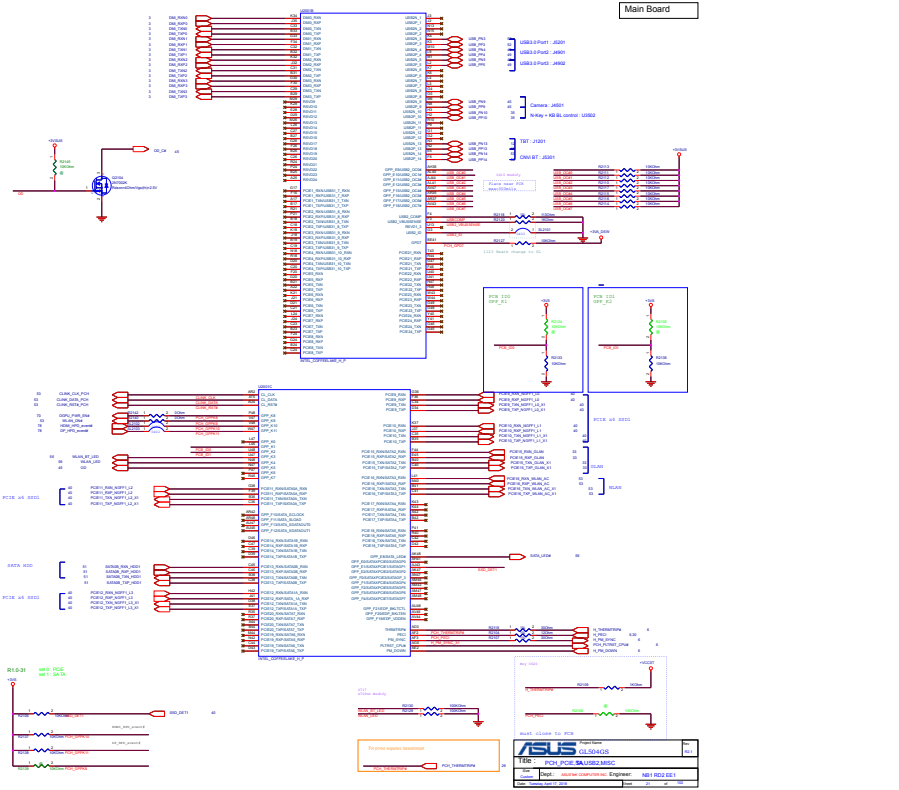
GL504GS PCIE/SATA Function define

	Funcon
PCIE-01 (USB3-7)	
PCIE-02	
PCIE-03	
PCIE-04	
PCIE-05	
PCIE-06	
PCIE-07	
PCIE-08	
PCIE-09	PCIE /SATA SSD
PCIE-10	PCIE SSD
PCIE-11 (SATA-0A)	PCIE SSD
PCIE-12 (SATA-1A)	PCIE SSD

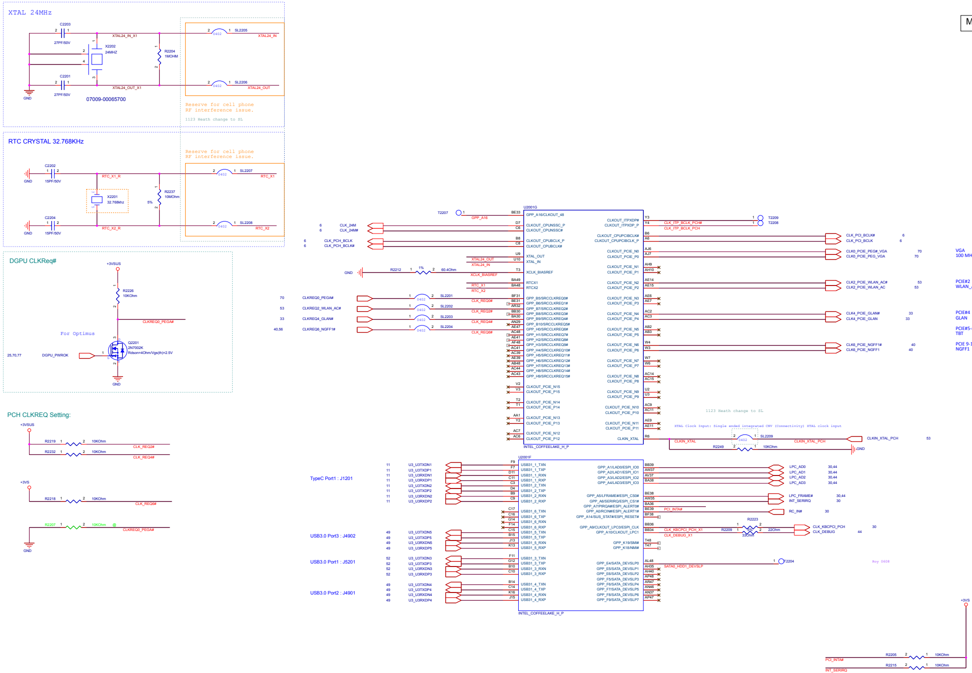
	Funcon
PCIE-13 (SATA-0B)	SATA HDD
PCIE-14 (SATA-1B)	SATA SSD
PCIE-15 (SATA-2)	
PCIE-16 (SATA-3)	WLAN-AC
PCIE-17 (SATA-4)	PCIE /SATA SSD
PCIE-18 (SATA-5)	PCIE SSD
PCIE-19 (SATA-6)	PCIE SSD
PCIE-20 (SATA-7)	PCIE SSD
PCIE-21	GLAN
PCIE-22	GLAN
PCIE-23	
PCIE-24	

	Funcon
CLKREQ-0	DGPU
CLKREQ-1	
CLKREQ-2	WLAN-AC
CLKREQ-3	
CLKREQ-4	GLAN
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	PCIE SSD
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	



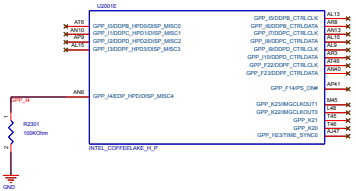


Main Board



ASUS	Project Name: GL504GS	Rev: R2.1
Title : PCH_CLK,LPC,USB3		
Size: C	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1
Date: Tuesday, April 17, 2018	Sheet 22 of 102	

G703GI display output from dGPU only,
so these strap are NC.
(Refer to PDG ch5.6, how to disable DDI)
If there is a MS-hybrid project, please notice the below strap



Strap => Display Port B Detected

```
PCH_GPP_I6: weak internal pull down
 0 : Port B is not detected. (Default)
 1 : Port B is detected.
```

Strap => Display Port C Detected

```
PCH_GPP_I8: weak internal pull down
 0 : Port C is not detected. (Default)
 1 : Port C is detected.
```

Strap => Display Port D Detected

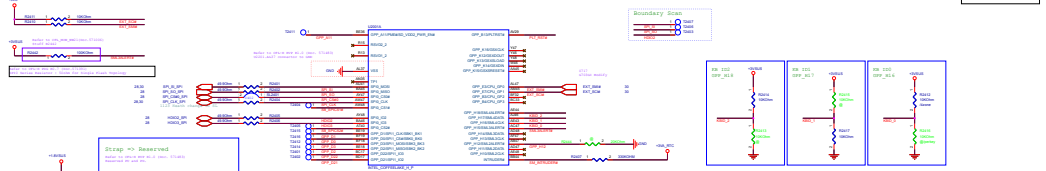
```
PCH_GPP_I10: weak internal pull down
 0 : Port D is not detected. (Default)
 1 : Port D is detected.
```

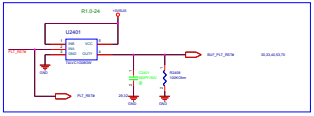
Strap => Display Port F Detected

```
PCH_GPP_F23: weak internal pull down
 0 : Port F is not detected. (Default)
 1 : Port F is detected.
```

Project Name: GL504GS		Rev: R2.1
Title : PCH_VDS,eDBP		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Tuesday, April 17, 2018	Sheet 23 of 102	

Main Board



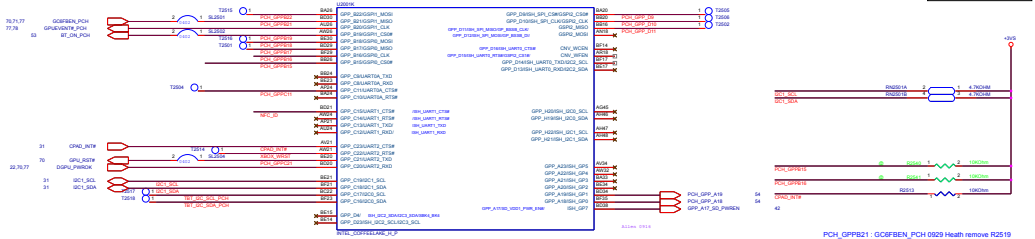


PCH Side (SPI 請依照此表格做設計判斷)			
	KBID 2	KBID 1	KBID 0
Code	ROG RGB KB Type	(GPP_H18)	(GPP_H17)	(GPP_H16)
0x00	Non-RGB	H	H	H
0x01	RGB per Region via CM/FE/NKRO modes	H	H	L
0x02	RGB per Region via 4 zones	H	L	H
0x03	RGB per key	H	L	L

5. 需請 BIOS RD 在KB ID 讀取的部分，額外加入 **Reverse** code, 以符合第1點 table

Project Name	GL5046GS
Rev	A0.1
Title	PCH_SPI
Engineer	NB1 RD2 EE1
Date	Tuesday, April 17, 2018
Sheet	24 of 74

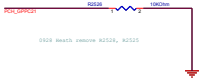
Main Board



PCH_GPP21 : GC6FBEN_PCH 0929 Heath remove R2519

PCH_GPP8, C9 : follow IP remove

PCH_GPPC21 : GPU_RST#
PCH_GPPC20 : DGPU_PWROK



0928 Weath remove R2528, R2525

PCH_GPP20 : GPUEVENT#_PCH

Boot BIOS Strap Bit BBS

Remove 0921

PCH_GPP822: weal internal pull down	
PU	LPC
PD	SPI (Default)

No Reboot

Remove 0921

NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

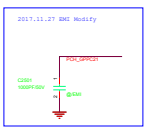
PCH_GPP818: weak internal pull down	
PU	Enable
PD	Disable (Default)

Onboard Memory PCB-ID:
GPP_C12 => DIMM_SEL0
GPP_C13 => DIMM_SEL1
GPP_C14 => DIMM_SEL2

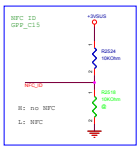
Remove 0921

	Hynix (2Gb)	XXX (2Gb)	Micron (2Gb)
DIMM_SEL0			
DIMM_SEL1			
DIMM_SEL2			

2017.11.27 EMI Modify



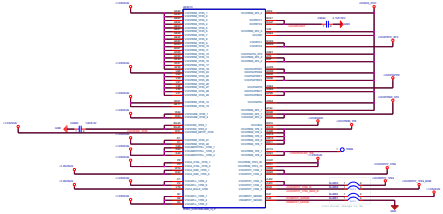
NFC ID
GPP_C15



H: no NFC
L: NFC

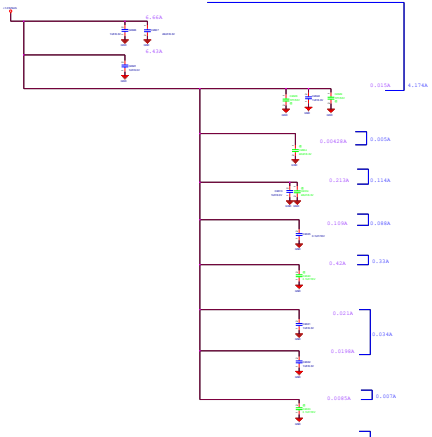
Project Name	GL504GS	Rev
Title :	PCH_GPIO	
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018	Sheet 26 of 152	

PCH_GPPC21

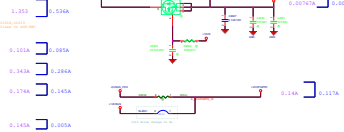


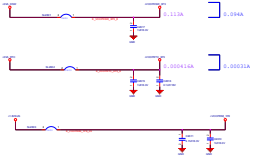
GPIO Voltage Level

Group	Power pin	Power option	Power phase
GPP_A	VCCPRIM_	3.3V	+3VDUS
GPP_B	VCCPRIM_	3.3V	+3VDUS
GPP_C	VCCPRIM_	3.3V	+3VDUS
GPP_D	VCCPRIM_	1.8V or 3.3V	+1.8VDUS
GPP_E	VCCPRIM_	3.3V	+3VDUS
GPP_F	VCCPRIM_	3.3V	+3VDUS
GPP_G	VCCSPI_	Level voltage supported(1.8Vor3.3V)	+3VDUS
GPP_H	VCCPRIM_	3.3V	+3VDUS
GPP_I	VCCPRIM_3P3	3.3V Only	+3VDUS
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8VDUS
GPP_K	VCCPRIM_	1.8V	+3VDUS
GPD	VCCSUS_3P3	3.3V Only	+3VA_SUS



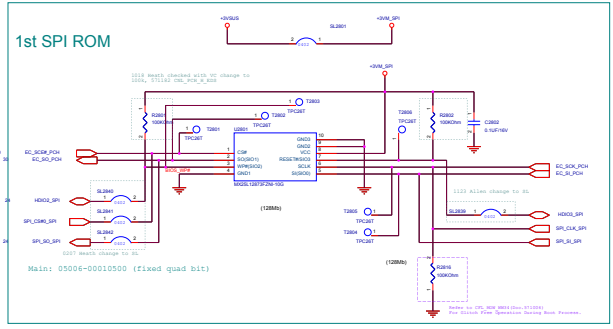
Purple reference CRM
Blue reference EDS

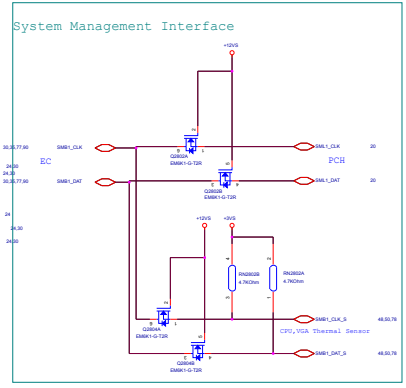


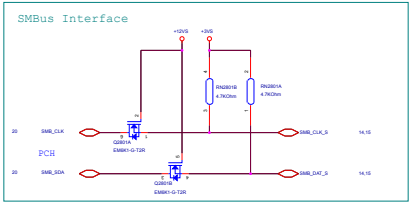


Main Board

Project Name: GL504GS			Rev: R2.1
Title : PCH_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Tuesday, April 17, 2018	Sheet: 27	of: 102	







ASUS	Project Name: GL504GS		Rev: XG1
Title :	PCH_SPI ROM,OTH		
Size: B	Dept : ASUSTeK COMPUTER INC.	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018		Sheet: 28	of: 102

Main Board

For power sequence measurement, place on CPU & GPU side of PCB

+1.0V_VCCPLL ----------> R2809

M_VCCST_PWRGD ----------> R2420

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ASUS	Project Name: GL504GS		Rev: 82.1
Title : <Title>			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018		Sheet: 28 of 102	

EC 8995

Only 3V Torlence
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

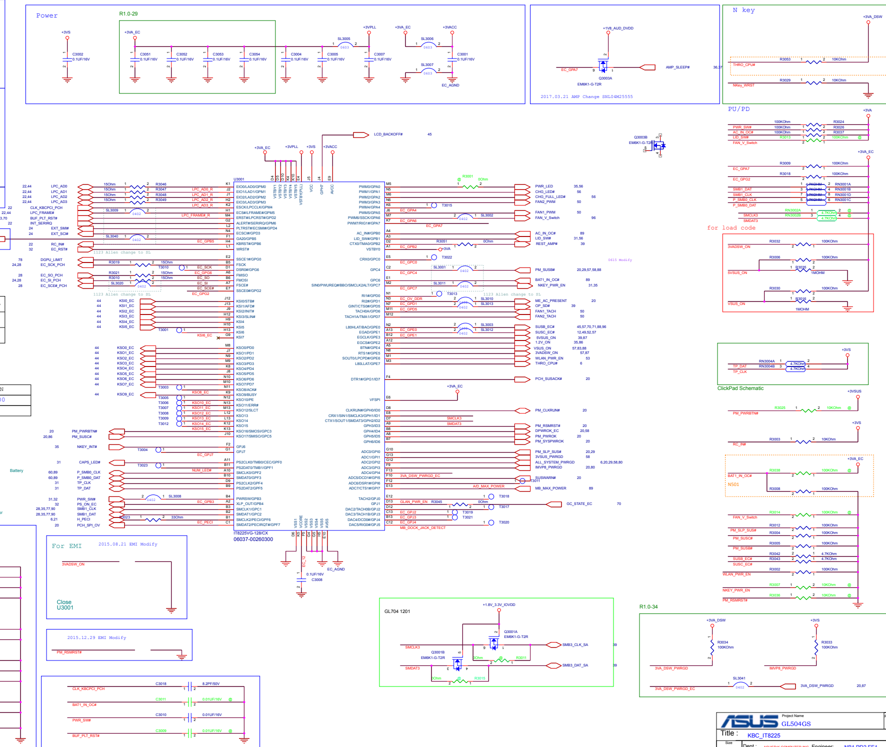
Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

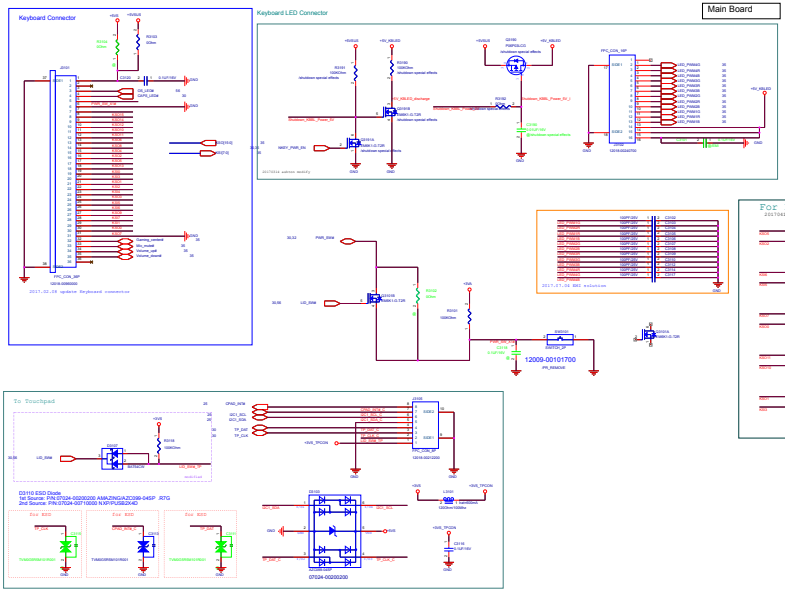
EC Require

	US	UK	JP
KB_LANG_ID0 (KB pin33)	1	0	0
KB_LANG_ID1 (KB pin34)	0	0	1

ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000



Project Name: GL504GS
Rev: R2.1
Title : KBC_IT8225
Dept.: ASUSTeK COMPUTER INC. Engineer: NB1 RD2 EE1
Date: Tuesday, April 17, 2018 Sheet 30 of 102

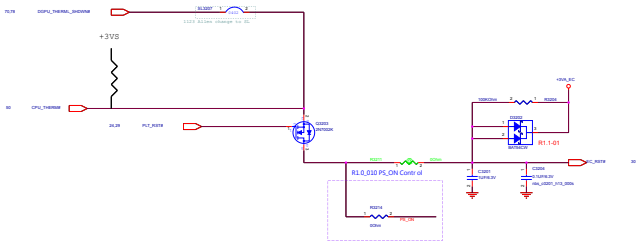


ASUS	Project Name: GL504GS	Rev: REV 2
Title :	KBC, KB & TP	
Size: D	Dept: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 31 of 153	

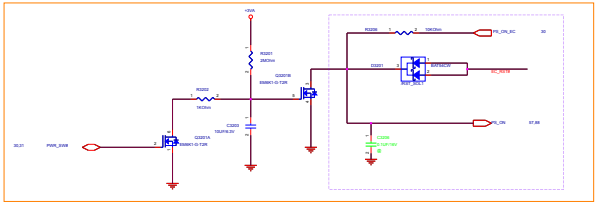
Main Board

Reset Circuit

Pull up +3VSG through R7507(10kOhm+100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



Battery embedded (press pwr_sw 10sec, then reset ec)

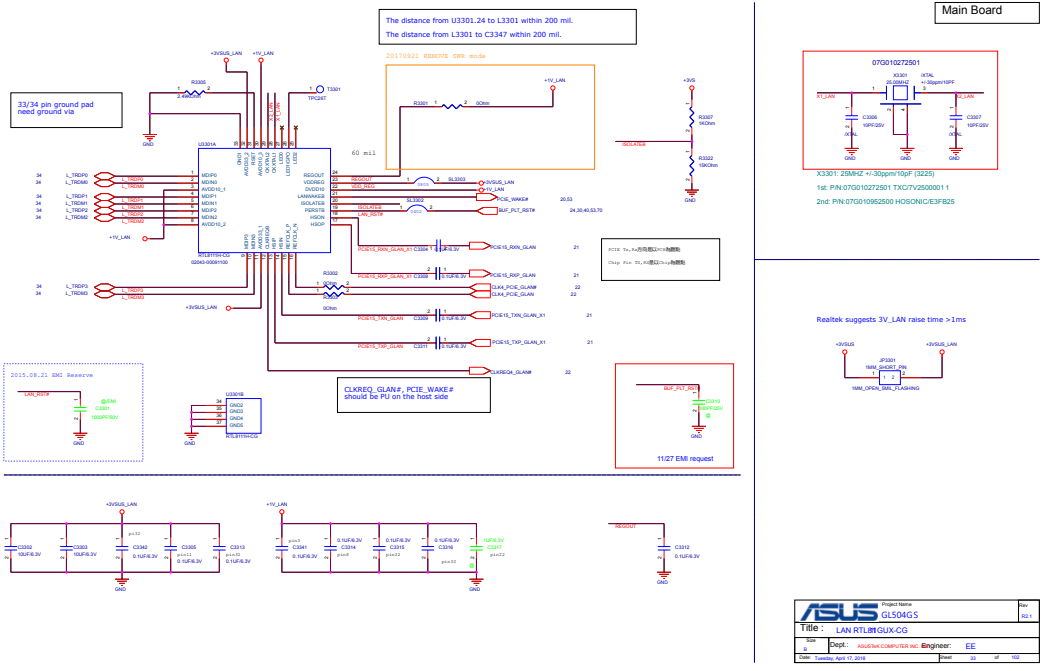


EC power off solution:
Solution1 Mount R3208, D3201/ Unmount R3216
Solution2 Mount R3208/R3216/ Unmount D3201- for reserved 0402 footprint

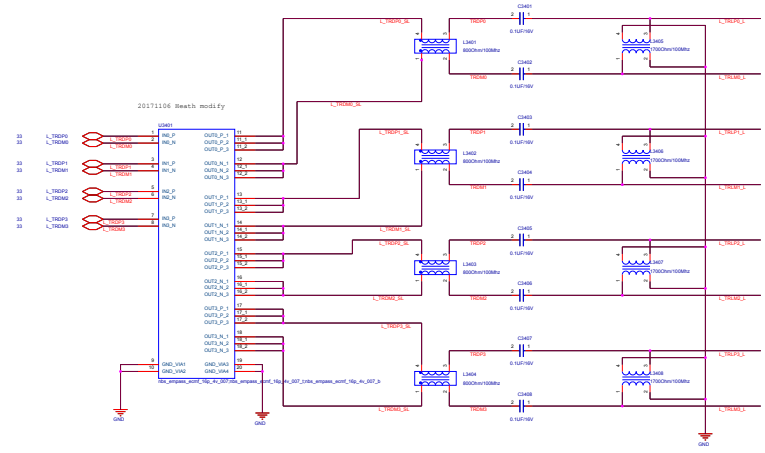
R1.2-65

<Variant Name>

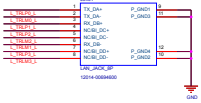
ASUS	Project Name: GL504GS		Rev: REX
Title : RST_Reset Circuit			
Size: A	Dept: ADJUSTME COMPUTER	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet 34 of 102		

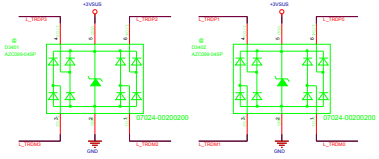

The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.
20170921 REMOVE SWR mode
33/34 pin ground pad need ground via
60 mil
U3301A
RTL8111HH-CG
02040-00004100
CLKREQ_GLAN#, PCIE_WAKE# should be PU on the host side
2015.08.21 EMI Reserve
11/27 EMI request
U3301B
Realtek suggests 3V_LAN raise time >1ms
Main Board
07G010272501
X3301 25.00MHZ 20PF
X3301 25MHZ +/-30ppm/10PF (3225)
1st: P/N:07G010272501 TXC/7V25000011
2nd: P/N:07G010962500 HOSONIC/E3FB25
JP3301 1MM_SHORT_PIN
1MM_OPEN_EMI_FLASHING
Project Name GL504GS
Rev R2.1
Title : LAN RTL8111GUX-CG
Size B
Dept.: ASUSTeK COMPUTER INC.
Engineer: EE
Date: Tuesday, April 17, 2018
Sheet 33 of 102

Main Board



LAN Connector



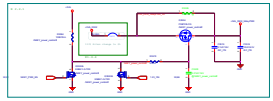


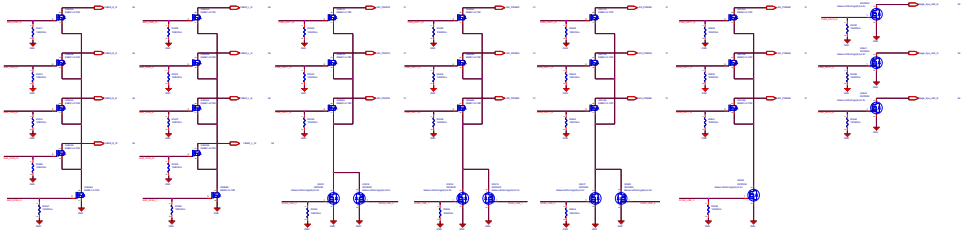
D3401,D3402 ESD Diode

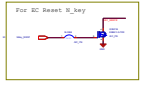
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP .R7G

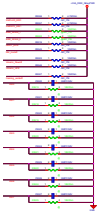
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

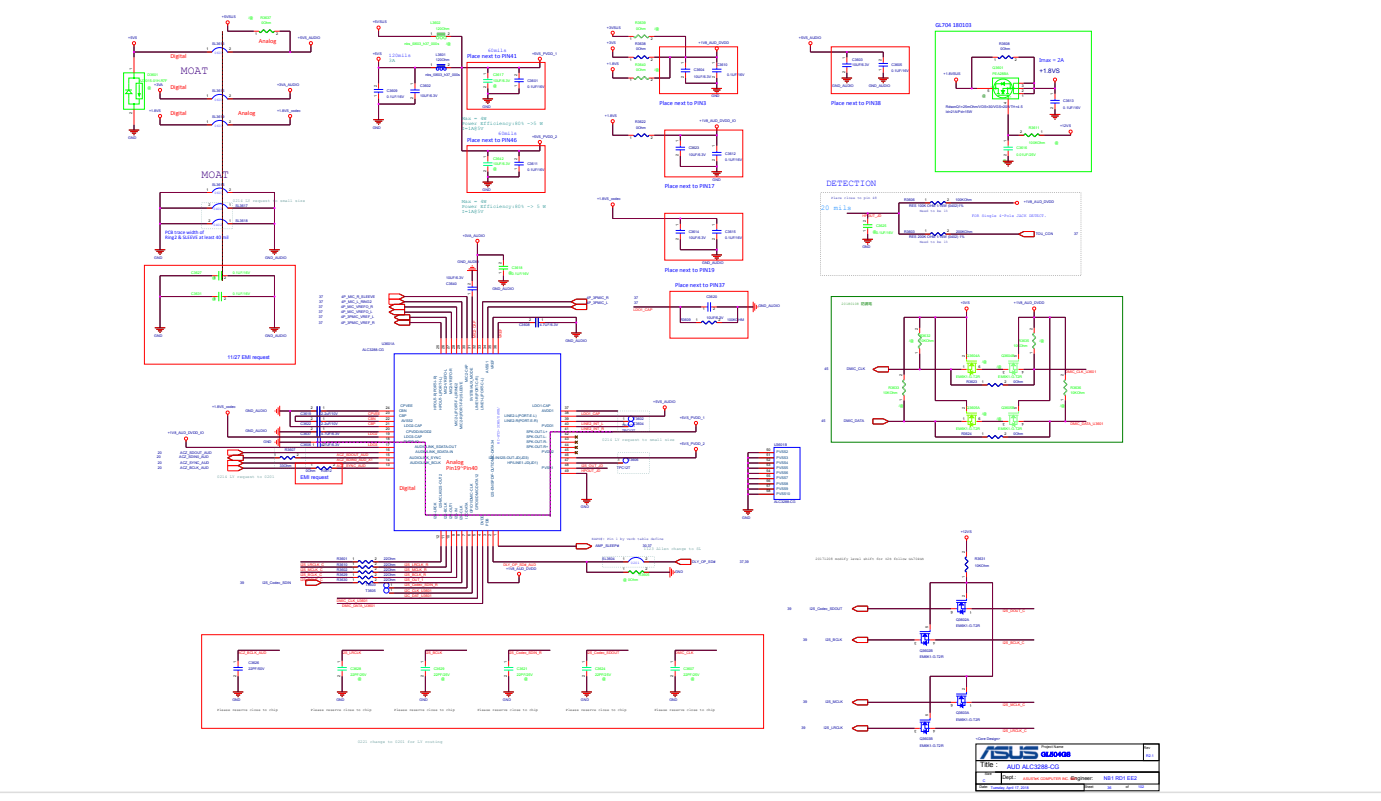
ASUS	Project Name: GL504GS		Rev: 62.1
Title :	LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet: 34	of: 102	



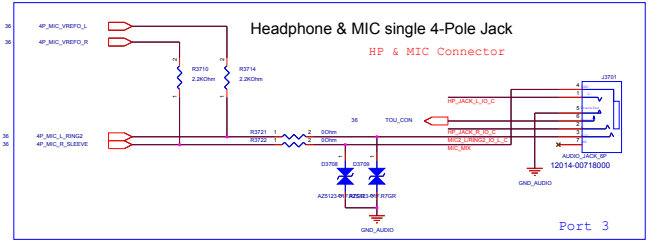


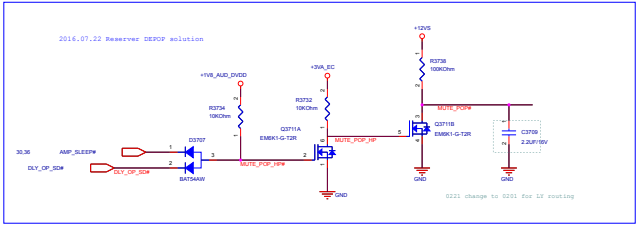


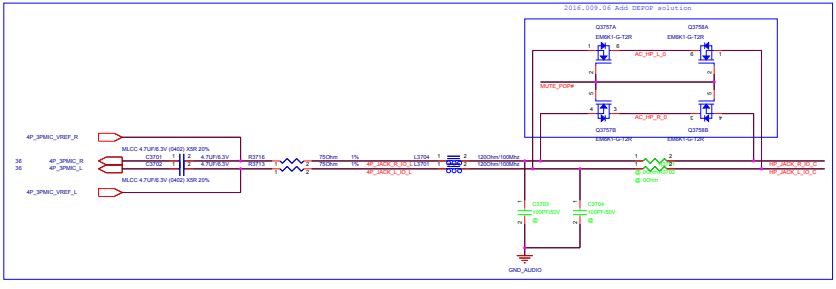




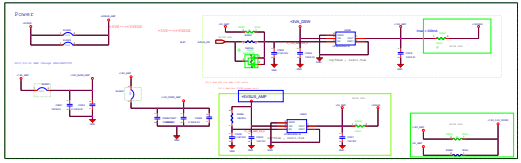
Title :	AUD ALC3288-CG
Size: A3	Dept: AAEntek-Shanhuan AE
Engineer:	NB1-RD1 EE2
Date:	Tuesday, April 17, 2018
Sheet	66 of 102



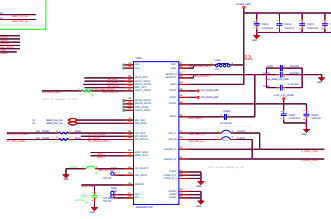


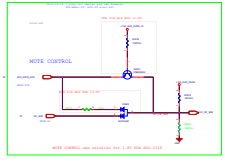


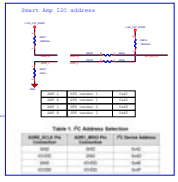
ASUS	Project Name: GL504GS		Rev: R2.1
Title : AUD ESS HP&MIC			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD1EE2	
Date: Tuesday, April 17, 2018		Sheet 37 of 102	

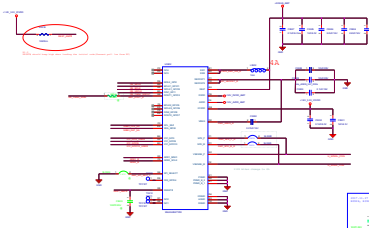

Power
+3VA_DSW
Smart_AMP

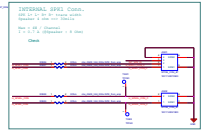

1116 pull high to +3VA_DSW

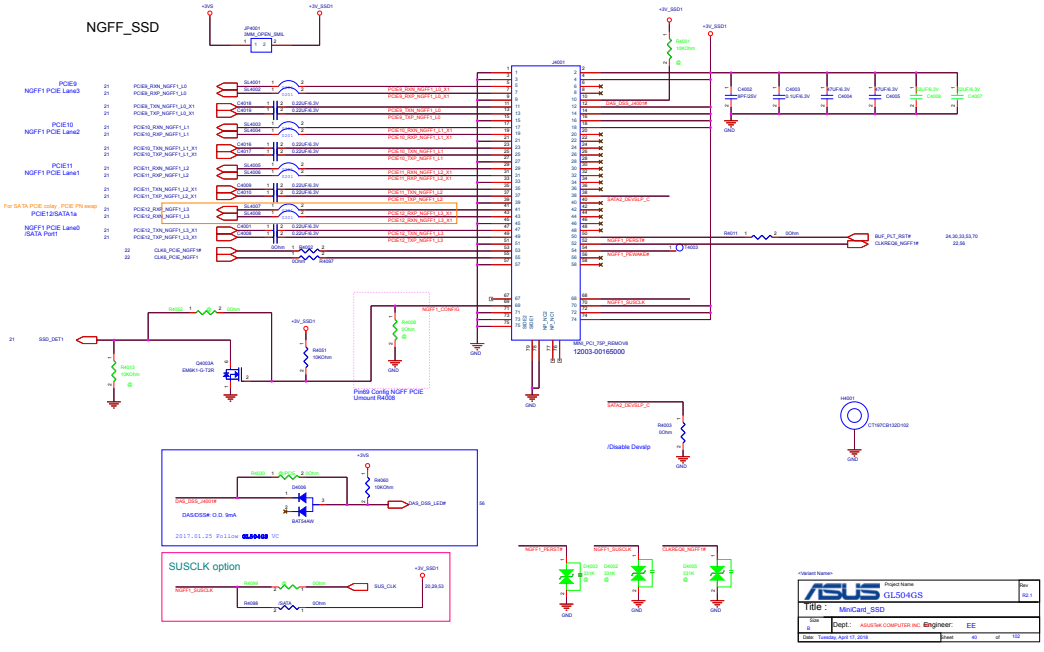


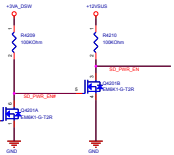

MUTE CONTROL


Smart Amp I2C address
ADR 1
ADR 0
Table 1. I²C Address Selection



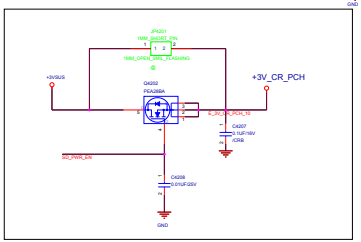

INTERNAL SPK1 Conn.
Check

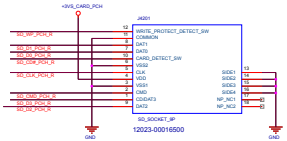

NGFF_SSD
PCIE9
NGFF1 PCIE Lane3
PCIE10
NGFF1 PCIE Lane2
PCIE11
NGFF1 PCIE Lane1
For SA TA PCIE oday , PCIE PN swap
PCIE12/SATA1a
NGFF1 PCIE Lane0
/SATA Port1
PCIE9_RXN_NGFF1_L0
PCIE9_RXP_NGFF1_L0
PCIE9_TXN_NGFF1_L0_X1
PCIE9_TXP_NGFF1_L0_X1
PCIE10_RXN_NGFF1_L1
PCIE10_RXP_NGFF1_L1
PCIE10_TXN_NGFF1_L1_X1
PCIE10_TXP_NGFF1_L1_X1
PCIE11_RXN_NGFF1_L2
PCIE11_RXP_NGFF1_L2
PCIE11_TXN_NGFF1_L2_X1
PCIE11_TXP_NGFF1_L2_X1
PCIE12_RXP_NGFF1_L3
PCIE12_RXN_NGFF1_L3
PCIE12_TXN_NGFF1_L3_X1
PCIE12_TXP_NGFF1_L3_X1
CLKE_PCIE_NGFF1#
CLKE_PCIE_NGFF1
+3VS
+3V_SSD1
JP4001
3MM_OPEN_SML
J4001
SATA2_DEVSLP_C
NGFF1_PERST#
NGFF1_PEWAKE#
NGFF1_SUSCLK
MINI_PCI_75P_RDMOV8
12003-00165000
Pin62 Config NGFF PCIE
Umount R4008
SSD_DET1
Q4003A
EMMK1-G-T3R
Q4003B
EMMK1-G-T3R
DAS/DSS# O.D. 5mA
DAS_DSS_LED#
2017.01.25 Follow GL504GS VC
SUSCLK option
SUS_CLK
CLKREQ0_NGFF1#
CT1167CB1322D102
/Disable Devslp
<Variant Name>
Project Name
GL504GS
Rev
R2.1
Title : MiniCard_SSD
Size
B
Dept.: ASUSTeK COMPUTER INC.
Engineer: EE
Date: Tuesday, April 17, 2018
Sheet 40 of 102

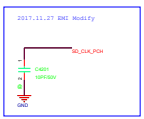


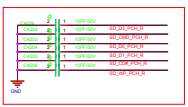
CR Socket

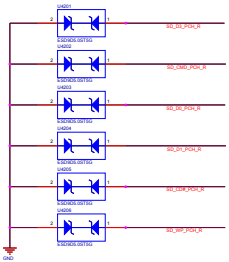
Reserved fuse for safety

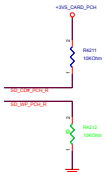








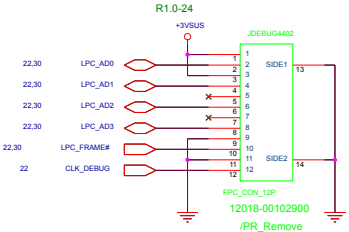




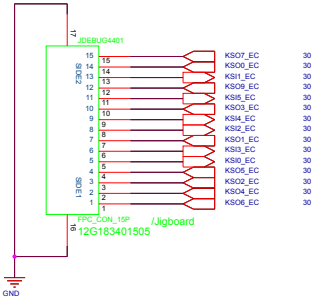
11/28 Mario suggested

ASUS	Project Name: GL504GS		Rev: 0.2
Title: CB_GL3213L_R0.2			
Size: A	Dept.: MB-NB2-EE1	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet: 42	of: 102	

LPC Debug Port

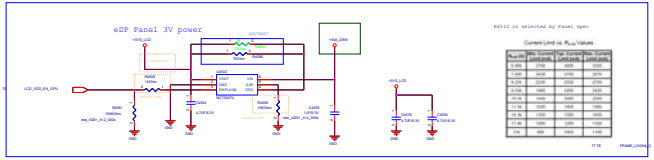


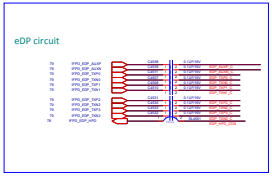
2016/03/21

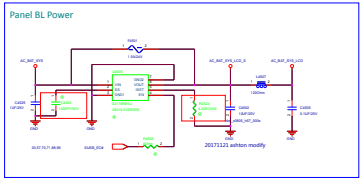


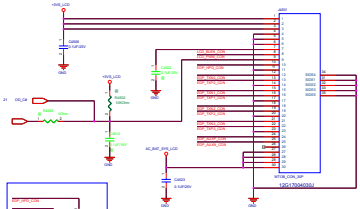
<Variant Name>

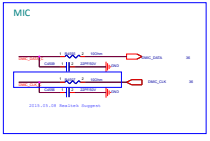
ASUS	Project Name: GL504GS	Rev: R2.1
Title : DEBUG_LPC		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 44 of 102	

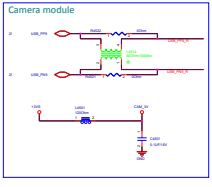

eDP Panel 3V power
+3VS_LCD
+3VS_DISP
LCD_VDD_EN_IOPU
R4454
100Ohm
R4455
100Ohm
R4456
100Ohm
R4457
100Ohm
C4454
4.7UF/6.3V
C4455
4.7UF/6.3V
C4456
4.7UF/6.3V
C4457
4.7UF/6.3V
R4460
100K/1%
R4461
100K/1%
R4462
100K/1%
R4463
100K/1%
C4458
0.1UF/50V
C4459
0.1UF/50V
C4460
0.1UF/50V
C4461
0.1UF/50V
+3VS_LCD
C4476
4.7UF/6.3V
C4462
4.7UF/6.3V
R4510 is selected by Panel spec
Current Limit =5 , R_set Values
Rset (KΩ)
Min. Current Limit (mA)
Typ. Current Limit (mA)
Max. Current Limit (mA)
77.76
FRAME_LOCKED

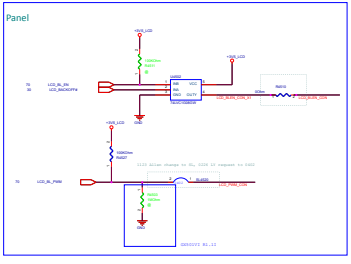

eDP circuit
C4538
C4537
C4536
C4535
C4534
C4533
C4531
C4530
C4529
C4528
0.1UF/16V
EDP_TXP0
EDP_TXN0
EDP_TXP1
EDP_TXN1
EDP_TXP2
EDP_TXN2
EDP_TXP3
EDP_TXN3
EDP_AUXP
EDP_AUXN
EDP_HPD


Panel BL Power
AC_BAT_SYS
AC_BAT_SYS_LCD_S
AC_BAT_SYS_LCD
C4548
1UF/25V
C4549
0.1UF/50V
R4534
100K/1%
C4552
1UF/25V
C4556
0.1UF/50V
R4535
100K/1%
20171121 wilson modify


eDP Panel Conn.
+5VS_LCD
C4558
1UF/25V
+3VS_LCD
R4552
100Ohm
C4553
1UF/25V
C4554
1UF/25V
C4555
1UF/25V
AC_BAT_SYS_LCD
C4553
1UF/25V
EDP_AUXP
EDP_AUXN
EDP_HPD
EDP_TXP0
EDP_TXN0
EDP_TXP1
EDP_TXN1
EDP_TXP2
EDP_TXN2
EDP_TXP3
EDP_TXN3
LCD_BLEN_CON
LCD_BLPWM_CON
LCD_VDD_EN
EDP_AUXP
EDP_AUXN
EDP_HPD
EDP_TXP0
EDP_TXN0
EDP_TXP1
EDP_TXN1
EDP_TXP2
EDP_TXN2
EDP_TXP3
EDP_TXN3
LCD_BLEN_CON
LCD_BLPWM_CON
LCD_VDD_EN
20180226 EMI modify
CAM_3V
CAM_DATA_P
CAM_DATA_N
CAM_CLK_P
CAM_CLK_N
1201710410083


MIC
MIC_IN
C4568
2.2UF/50V
C4569
2.2UF/50V
MIC_CLK
MIC_DATA
2015.05.08 Realtek Suggest

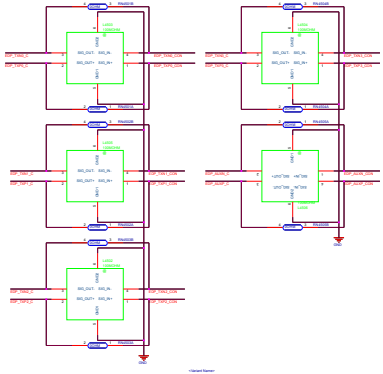

Camera module
USB_P6N
USB_P6P
R4523
22Ohm
R4524
22Ohm
U4514
USB_P6N_R
USB_P6P_R
+3VS
L4501
120Ohm
C4502
0.1UF/16V
CAM_3V


Panel
+3VS_LCD
C4504
1UF/25V
LCD_VCC
R4530
100Ohm
C4505
0.1UF/50V
LCD_BLEN_CON_R
LCD_BLEN_CON
LCD_BL_EN_IOPU
LCD_BKCHOPFB
+3VS_LCD
R4537
100Ohm
C4506
0.1UF/50V
R4538
0Ohm
LCD_BLPWM_CON_R
LCD_BLPWM_CON
LCD_BL_PWM
1123 &Use change to BL_220K ST request to 0402
0255YY0 R1.1I

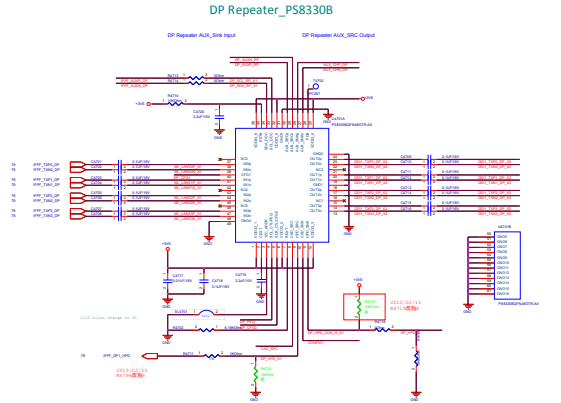

EDP_HPD_CON
D4550
3V/4
CAM_DATA_N
D4551
3V/4
CAM_DATA_P
D4552
3V/4
CAM_CLK_N
D4553
3V/4
CAM_CLK_P
D4554
3V/4

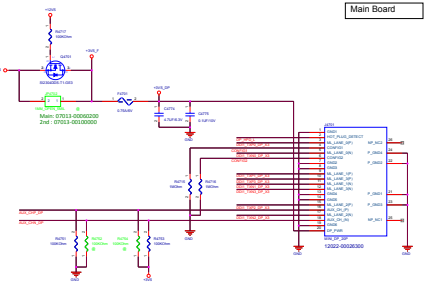

EDP_HPD_CON
C4572
0.1UF/16V
20180226 EMI modify

For EMI


EDP_TXN0_C
EDP_TXP0_C
EDP_TXN1_C
EDP_TXP1_C
EDP_TXN2_C
EDP_TXP2_C
EDP_TXN3_C
EDP_TXP3_C
EDP_TXN0_CON
EDP_TXP0_CON
EDP_TXN1_CON
EDP_TXP1_CON
EDP_TXN2_CON
EDP_TXP2_CON
EDP_TXN3_CON
EDP_TXP3_CON
RN4555B
RN4555A
RN4556B
RN4556A
RN4557B
RN4557A
RN4558B
RN4558A
L4550
120OHM/2A
L4551
120OHM/2A
L4552
120OHM/2A
L4553
120OHM/2A
L4554
120OHM/2A
L4555
120OHM/2A
L4556
120OHM/2A
L4557
120OHM/2A

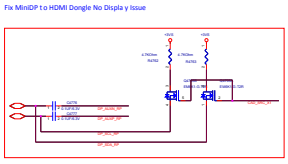

ASUS
Project Name
GXL50/40S
Title :
CRT_eDP
Size
Document Number
Rev
Date:
Sheet
of
Tuesday, April 17, 2018

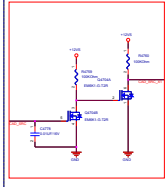


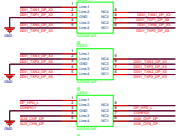


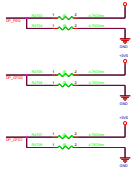
Main Board

20171121 ashton modify



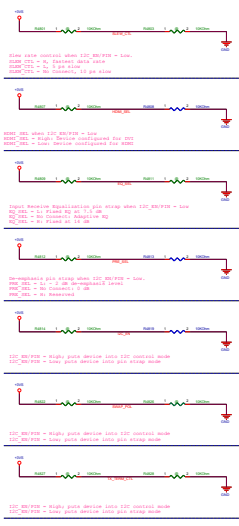




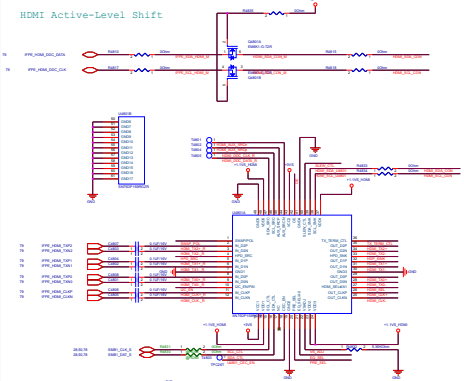


ASUS	Project Name: GL504GS		Rev: REV 1
Title : Display Port Conn.			
Size:	Project:	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet 17 of 108		

Main Board

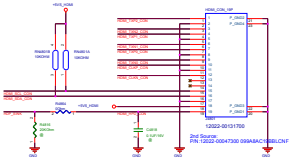


HDMI Active-Level Shift

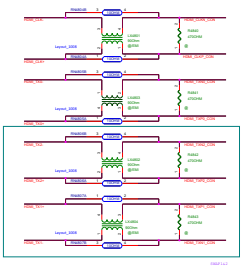


HDMI PWR_+5VS_HDMI

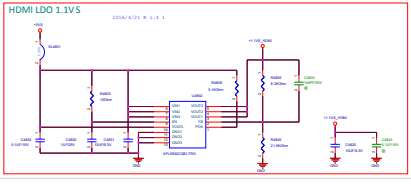
HDMI Conn.

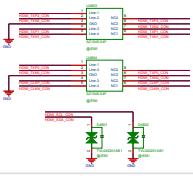


HDMI EMI



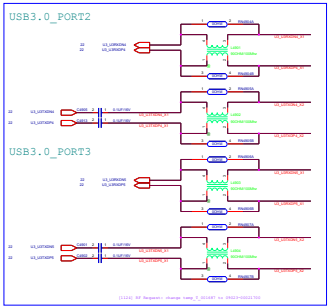
HDMI LDO 1.1VS

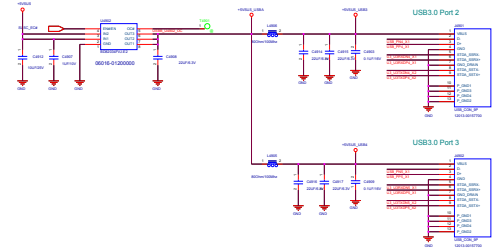


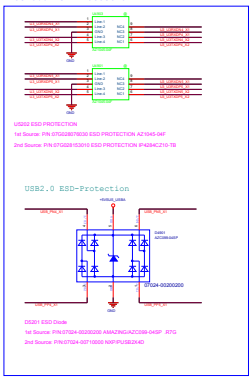


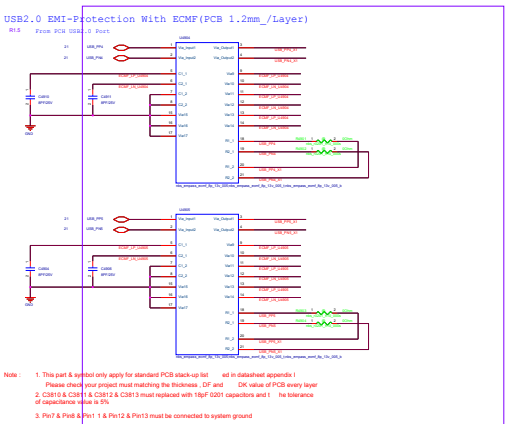
Title :	HDMI		
Size	Dwg.:	Engineer:	NB1 RD2 EE1
Date: Tuesday, April 17, 2018	Sheet 15 of 50		

Main Board

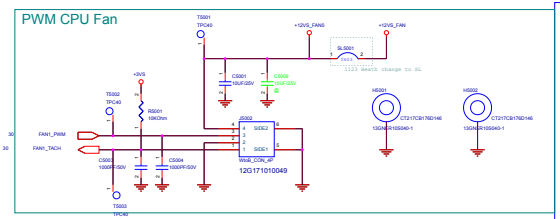


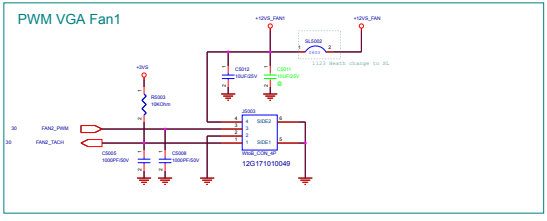


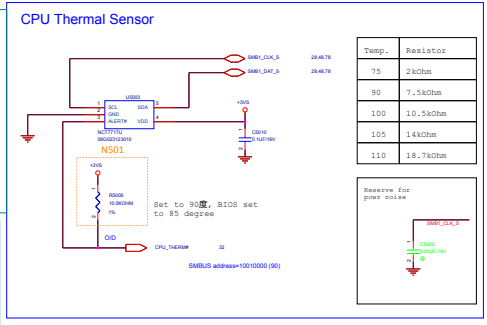




Project Name: GL504GS			Rev: 1.0
Title: USB 3.1 MB-C			
Size: C	Dwg.:	Engineer: EE	
Date: Tuesday, April 17, 2018		Sheet 22 of 102	

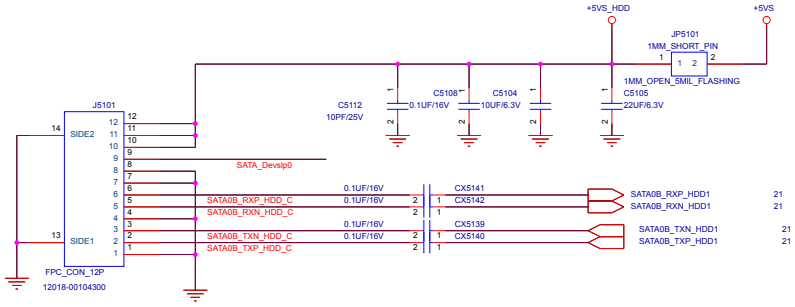


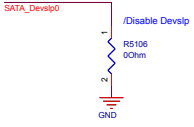


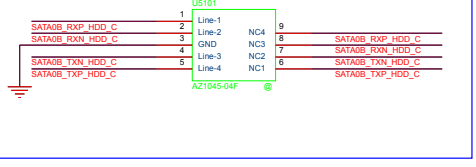


Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

ASUS	Project Name: GL504GS		Rev: 82.1
Title : FAN_Thermal Sensor & Fan			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 17, 2018		Sheet 50 of 102	





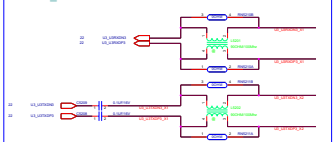


<Variant Name>

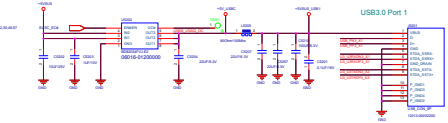
ASUS	Project Name: GL504GS	Rev: R2.1
Title : XDD_HDD & ODD CON		
Size: A	Dept.: ASUSTeK COMPUTER INC. (E	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 51 of 102	

Main Board

USB3.0_EMI-Protection



USB3.0 Port 1



USB3.0 ESD-Protection

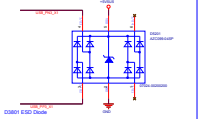
1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

USB2.0 EMI-Protection With ECMF(PCB 1.2mm_/Layer)

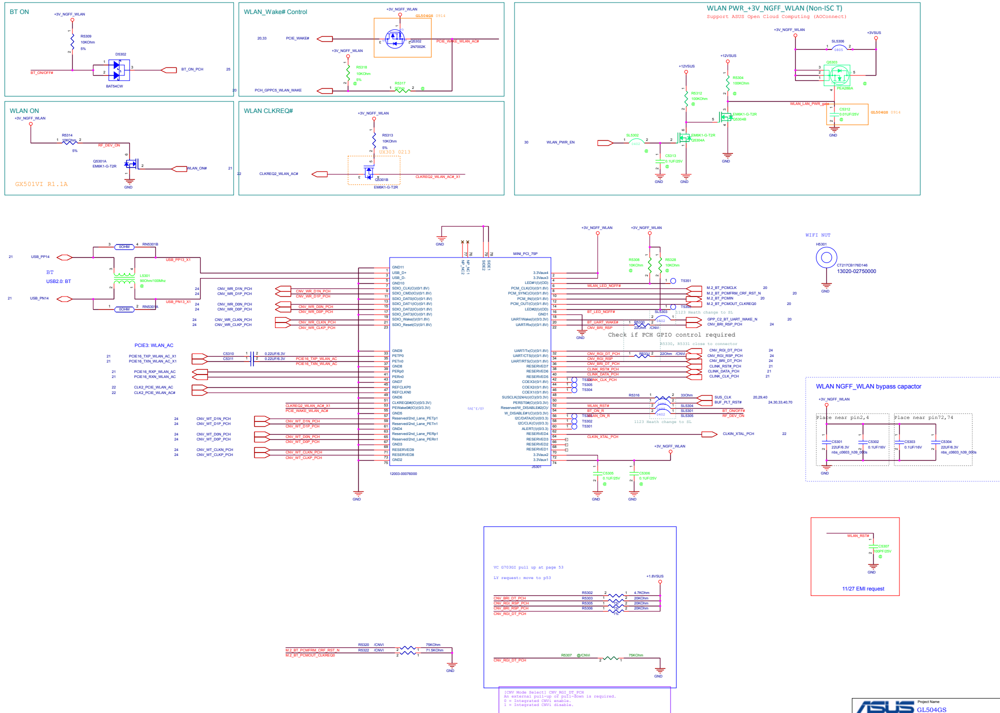
Note : 1. This part & symbol only apply for standard PCB stack-up list ed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. CS210 & CS211& CS212 & CS213 must replaced with 18pF 0201 capacitors and th e tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin1 1& Pin12 & Pin13 must be connected to system ground
4. Pin14 to Pin17 are floated in regular scheme

USB2.0 ESD-Protection

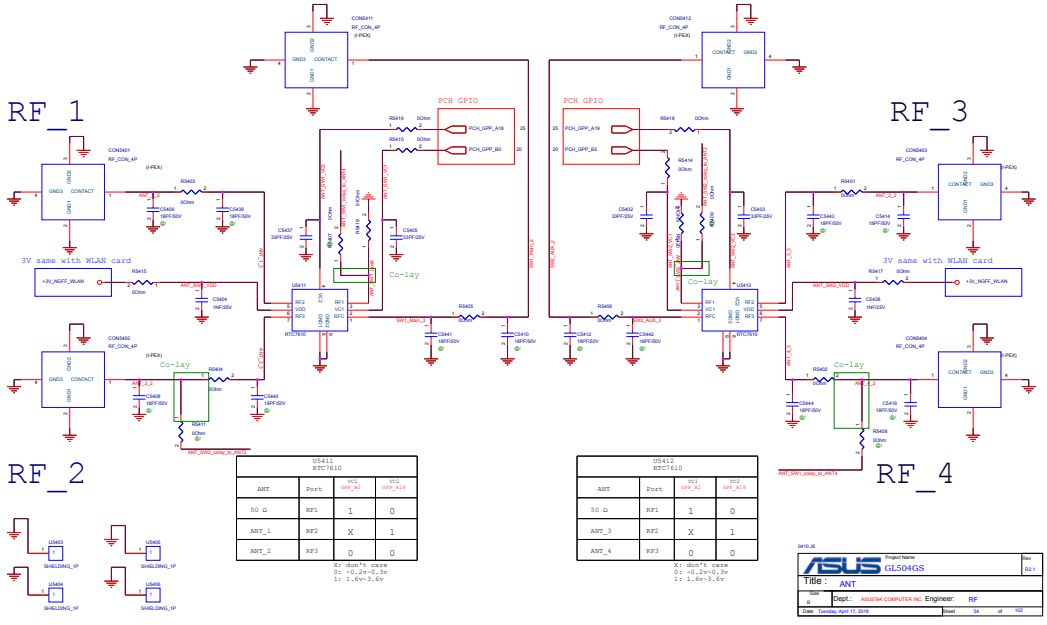


D3801 ESD Diode
1st Source: P/N 07024-00203200 AMAZING/AZC099-04SP RTG
2nd Source: P/N 07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: G1,5GHG2S		Rev: 0.1
Title : USB Charger			
Size:	Dept.: ABOVE COMPUTER INC	Engineer: EE	
Date: Tuesday, April 27, 2010	Sheet: 10	of: 100	

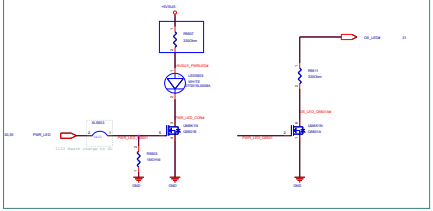


Project Name	GL504GS
Rev	R2.1
Title :	WiFi/WMax
Size	C
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Tuesday, April 17, 2018
Sheet	53 of 102

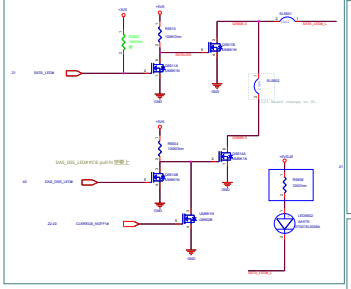

Module_Main
Module_AUX
RF_1
RF_2
RF_3
RF_4
PCH GPIO
PCH_GPP_A18
PCH_GPP_B0
PCH_GPP_A19
PCH_GPP_B2
3V same with WLAN card
+3V_NGFF_WLAN
Co-lay
U5411
RTC7610
U5412
RTC7610
ANT | Port | VCC1 GPP_B2 | VCC2 GPP_A18
50 Ω | RF1 | 1 | 0
ANT_1 | RF2 | X | 1
ANT_2 | RF3 | 0 | 0
ANT | Port | VCC1 GPP_B2 | VCC2 GPP_A18
50 Ω | RF1 | 1 | 0
ANT_3 | RF2 | X | 1
ANT_4 | RF3 | 0 | 0
X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v
Module_Main
Module_AUX
ASUSTeK COMPUTER INC.
Project Name: GL504GS
Rev: A01
Title: ANT
Dept.: RF
Engineer:
Date: Tuesday, April 17, 2018
Sheet 54 of 102

Main Board

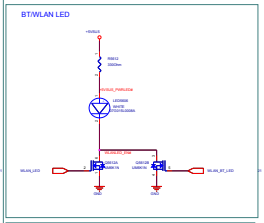
PWR LED



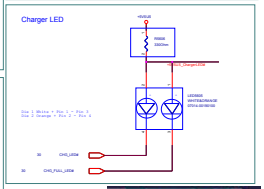
HDD LED & PCIE SSD LED



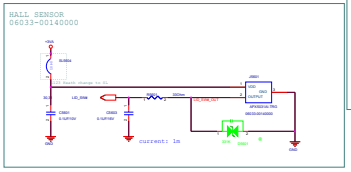
BT/WLAN LED



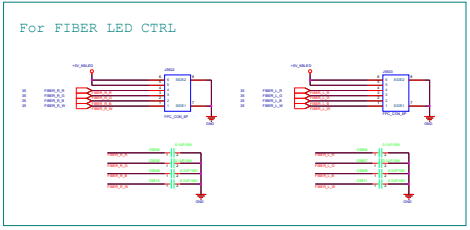
Charger LED



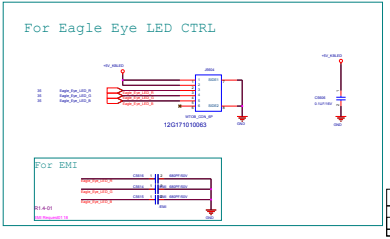
HALL SENSOR 06033-00140000



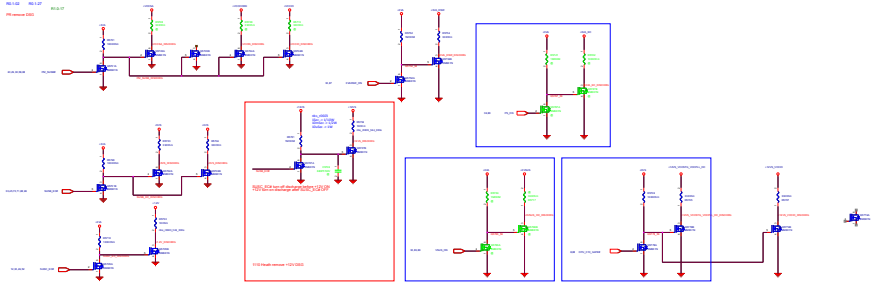
For FIBER LED CTRL

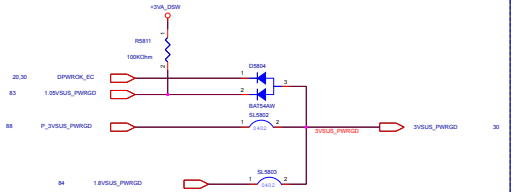


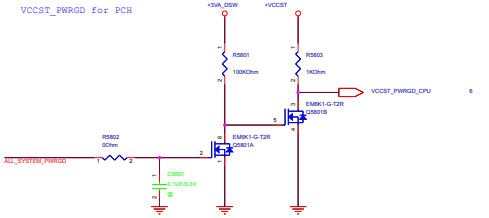
For Eagle Eye LED CTRL

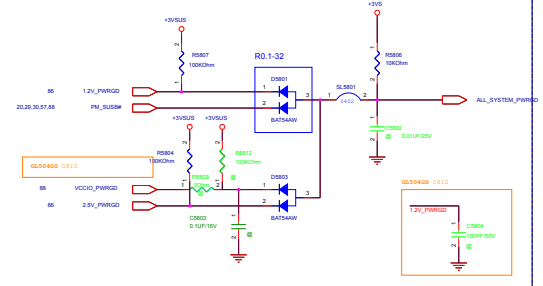


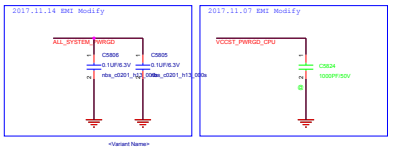
ASUS	Project Name: GL504GS		Rev: Rev 1
Title : LED Indicator			
Size:	Dept: xGSeries COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet: 56	of: 100	


R0.1-12
R0.1-27
R1.0-17
PR reserve C923
PR reserve C922
R1.0-12 reserve +12V GND



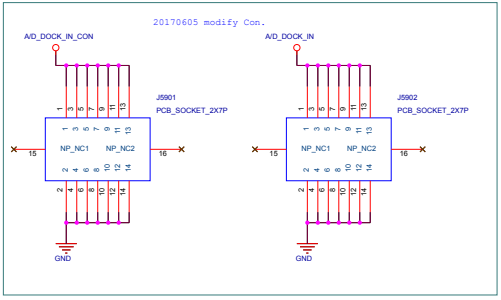






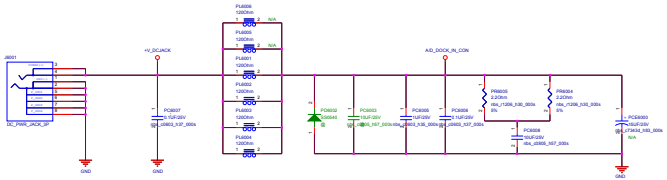
<Variant Name>

ASUS	Project Name: GL504GS		Rev: R2.1
Title : Power Protect			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet 58	of 102	



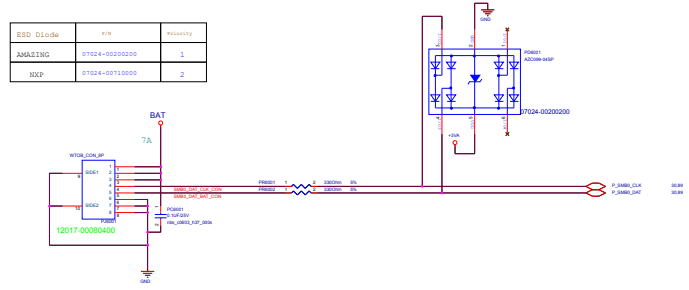
ASUS	Project Name: GL504GS		Rev: R2.1
Title : I/O_Main board Conn.			
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 17, 2018	Sheet 59 of 102		

DC-IN Connector



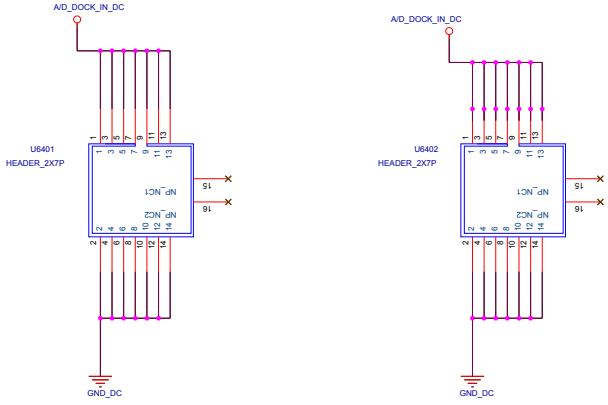
Battery Connector

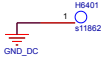
ESD Diode	P/N	Priority
AMAZING	07024-00200200	1
NXP	07024-00710000	2

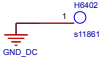


Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GL504GS		Rev: 1G1
Title: DC & BAT IN			
Size: A3	Dept: NB_Power team	Engineer: Hon	
Date: Tuesday, April 17, 2018	Sheet: 83	of: 102	

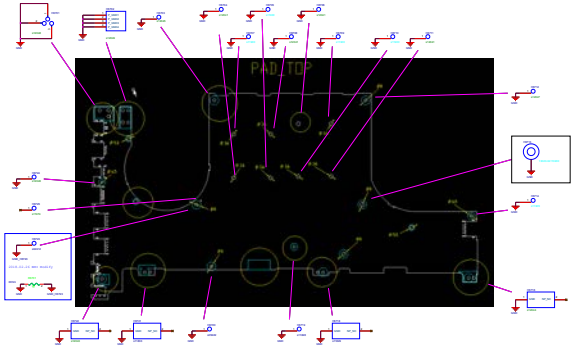




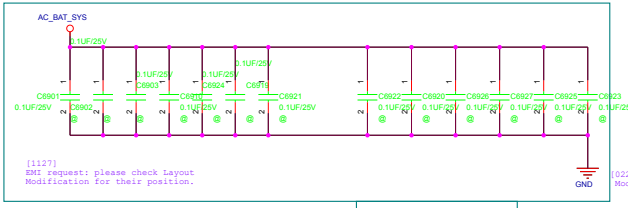


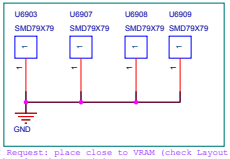
<Variant Name>

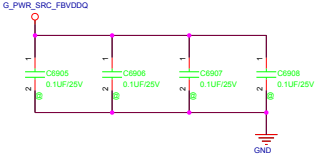
ASUS	Project Name: GL504GS	Rev: R2.1
Title : I/O board(1-3)_USB		
Size: A	Dept.: ASUSTeK COMPUTER INC. (I	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 64 of 102	

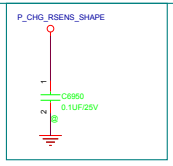

PAD_TOP


PAD_BOT

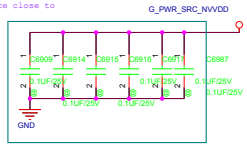


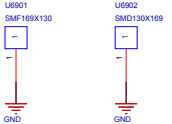


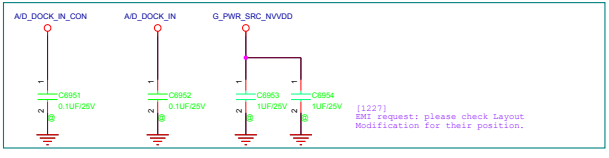


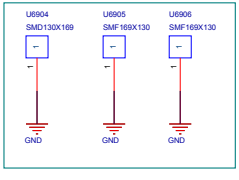


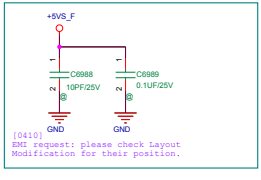
[1127] EMI Request: place close to PQR9201, PQR9208







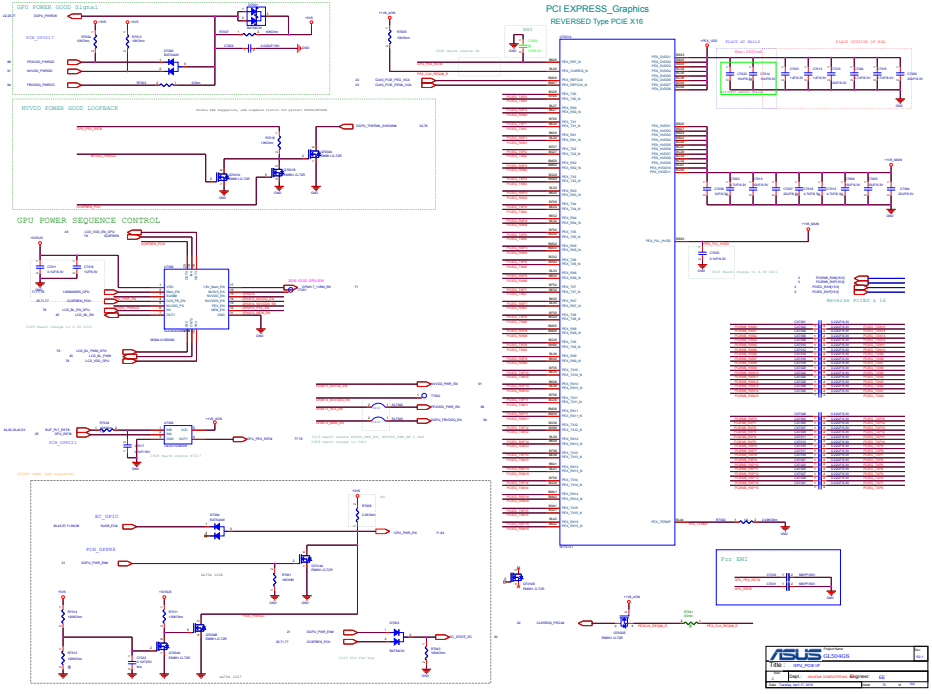


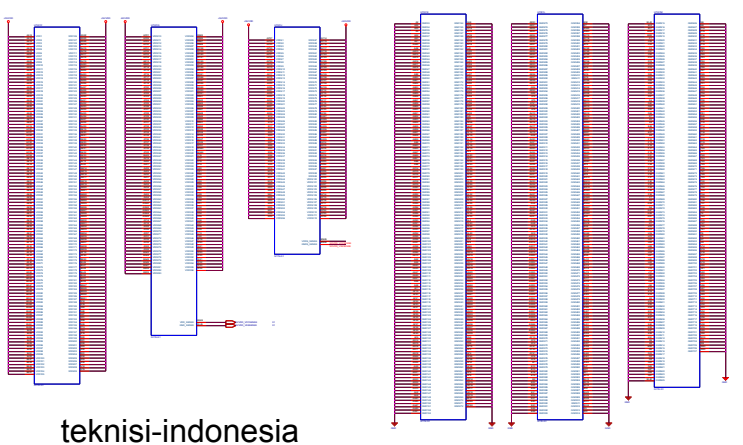


<Variant Name>

ASUS	Project Name: GL504GS	Rev: R2.1
Title : OTH_EMI		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, April 17, 2018	Sheet 69 of 102	

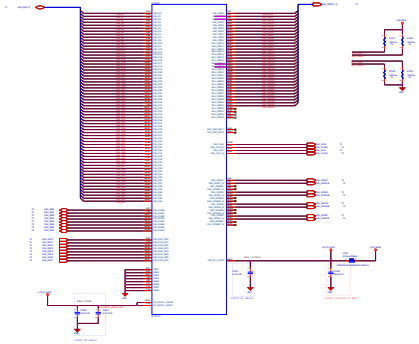
Main Board


GPU POWER GOOD Signal
NVVDD POWER GOOD LOOPBACK
GPU POWER SEQUENCE CONTROL
PCI EXPRESS_Graphics
REVERSED Type PCIE X16
PLACE AT BACK
PLACE OPPSIDE OF VGA
Reverse PCIE x 16
For EMI
EC_GPIO
PCH_GPIO65
ASUSTeK
Project Name
VILSON-MGS
Title
GPU_PCIE-I/F
Engineer

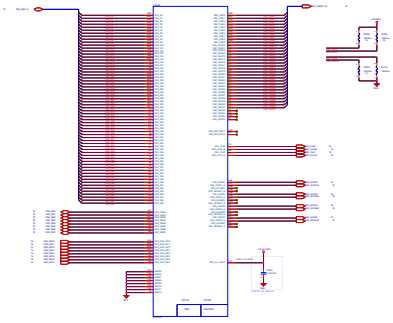


teknisi-indonesia

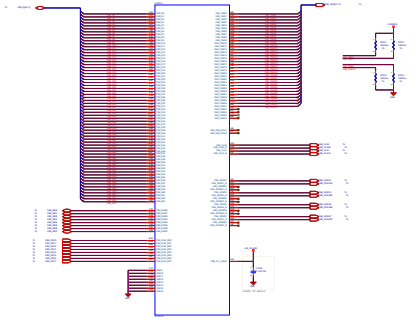
MEMORY: GPU FB Partition A



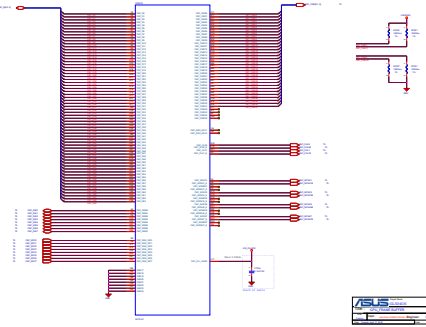
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



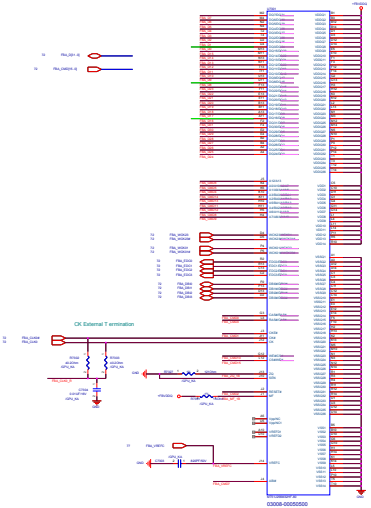
MEMORY: GPU FB Partition C



Main Board

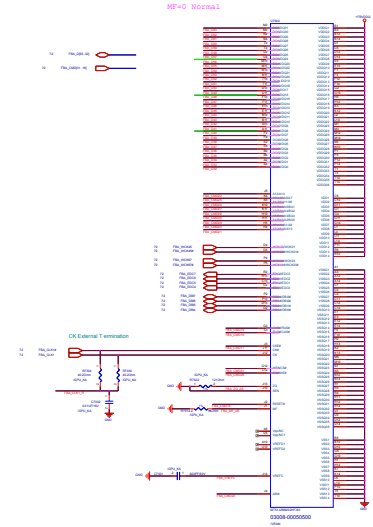
FBA Partition Memory (1 of 2)

MF=1 Mirror



FBA Partition Memory (2 of 2)

MF=0 Normal



PCB-0.6D - 2/1-2-2/6

GDS: GDDR5 VRAM 128Bit x 32 (512MB)

1st: P/N:03008-00020100 HYNIX/H5GC4H24MFR-T2C (fbga: 3 x2

2nd: P/N:03008-00020200 SAMSUNG/K4G41325FC-HC03 (fbga: 0x3

3rd: P/N:03008-00020400 Micron/EDW8032BABG-80-F (fbga: 0x4

GDD5 MODE SELECTION

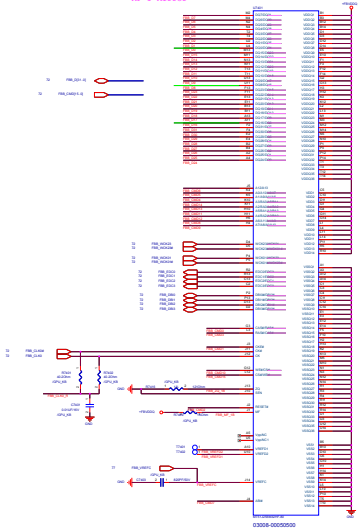
MODE	MF	GDC1	GDC2
+OE	0	VDDQ	VDDQ
+OE	1	VDDQ	VDDQ
+OE removed	VDDQ	VDDQ	VDDQ
+OE removed	VDDQ	VDDQ	VDDQ

ASUS	Project Name: G1,5044GS		Rev: 1.1
Title:	VRAM-CHANNEL A		
Date:	2015/Feb/13 09:51:20	Engineer:	KE
Size:	Custom	Sheet: 15	of: 100

Main Board

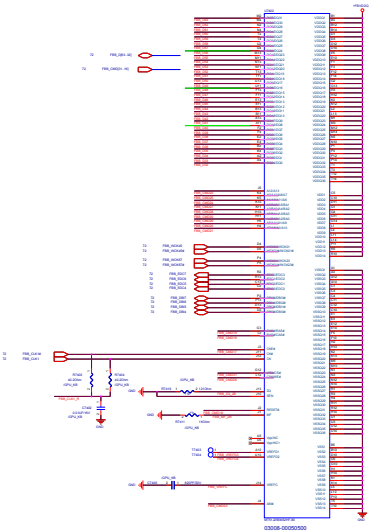
FBB Partition Memory (1 of 2)

MF=1 Mirror



FBB Partition Memory (2 of 2)

MF=0 Normal



R1 x-69 R1 2-26

DIE: GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 H7N0X45GCAH0HMFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

2nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EMC1	EMC3
x16	0	VSS	VSS
x16 Mirrored	VDD	VSS	0
x32	0	VDD	VDD
x32 Mirrored	VDD	VDD	VDD

ASUS Project Name: G1.Sniper M5 G1.SNIPER M5 Rev: 1.01

Title: VRAM-CHANNEL B

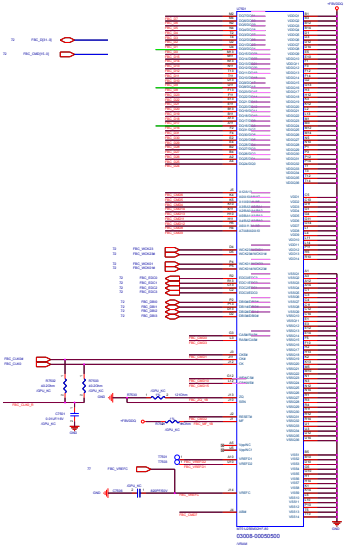
Size: Document Number: Rev: 1.01

Date: Tuesday, April 17, 2018 Sheet 13 of 100

Main Board

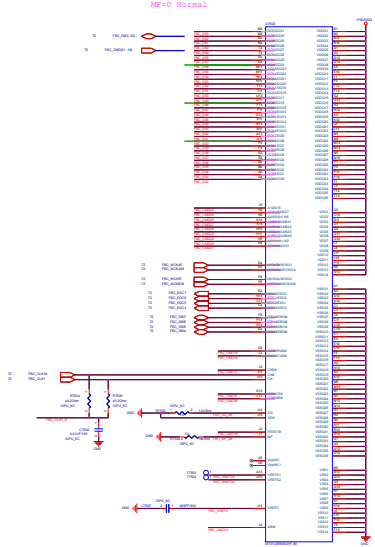
FBC Partition Memory (1 of 2)

MF=1 Mirror



FBC Partition Memory (2 of 2)

MF=0 Normal



R1.3-02 _ R1.2-25

DDR GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3rd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

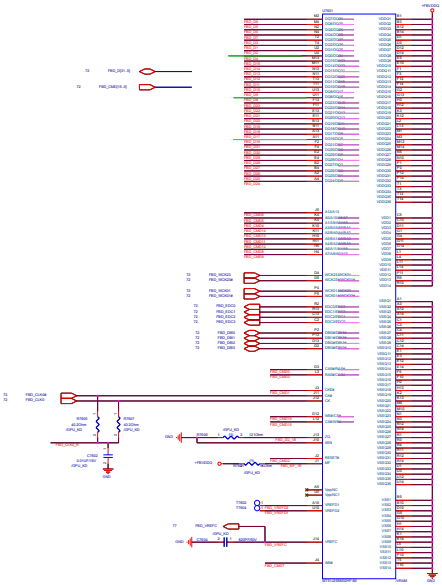
GDD5 MODE SELECTION

MODE	MF	EDC 1	EDC 0
x4	0	VSSQ	VSSQ
x32	0	VSSQ	VSSQ
x16 mirrored	1	VSSQ	VDDQ
x32 mirrored	VDDQ	VSSQ	VDDQ

ASUS	Project Name: GL504GS		Rev:
Title:	VRAM-CHANNEL C		
Size: B	Dept:	Author:	Engineer: EE
Date: Tuesday, April 17, 2018		Sheet: 7/8	of: 100

FBD Partition Memory (1 of 2)

MF=1 Mirror

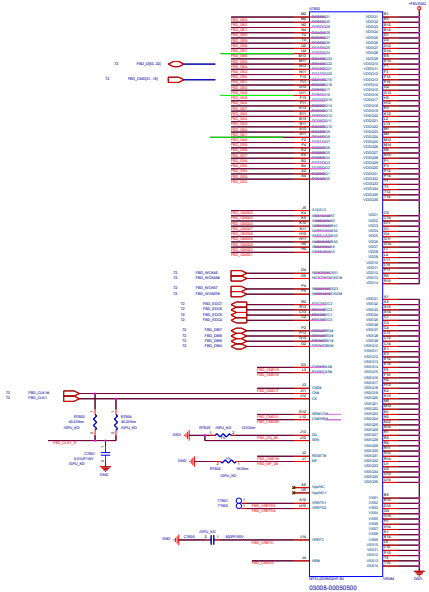


03008-00050500

FBD Partition Memory (2 of 2)

Main Board

MF=0 Normal



03008-00050500

R1.3-S2 R1.2-25

USE GDDR3 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIXH5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MA[9]	MF	BA[1]	BA[0]
x16	0	0	VSSQ
x32	0	VSSQ	VSSQ
x16 mirrored	VSSQ	VSSQ	0
x32 mirrored	VSSQ	VSSQ	VSSQ

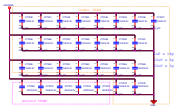
ASUS	Project Name: GL504GS		Rev: R2.1
Title:	VRAM-CHANNEL D		
Size: A3	Dwg No:		
Date: Tuesday, April 17, 2018	Sheet: 19	of: 150	

Channel A

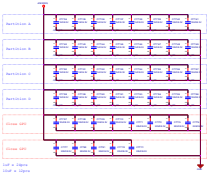
Channel B

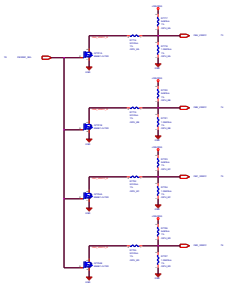
Channel C

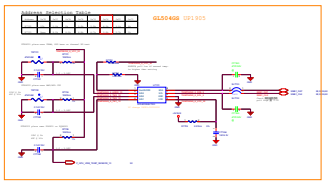
Channel D

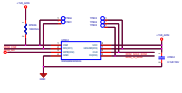


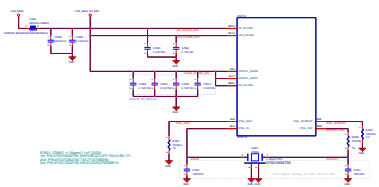
VRAM PWR_FBVDDQ

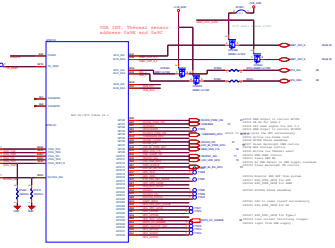


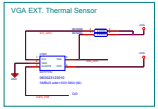


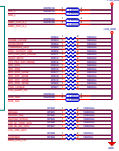




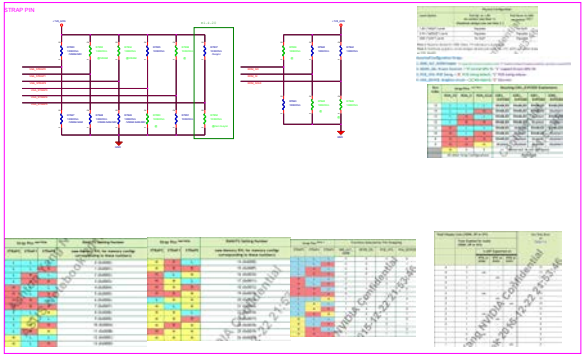


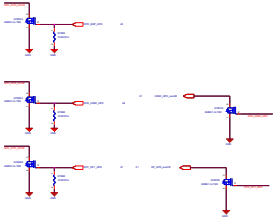

VGA INT. Thermal sensor address 0x98 and 0x90


VGA EXT. Thermal Sensor

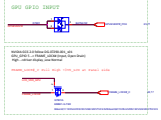



Thermal Protection

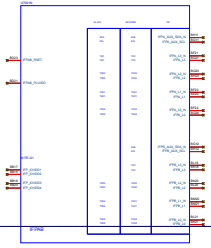

STRAP PIN

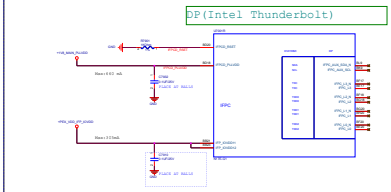

HPD Invert

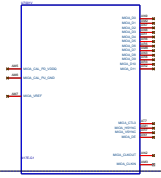
Level shift

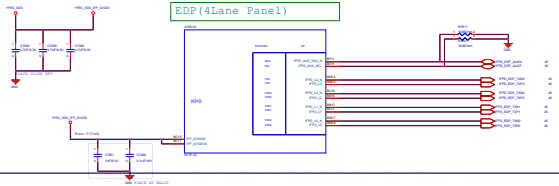

GPU GPIO INPUT

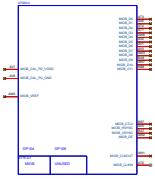
Main Board

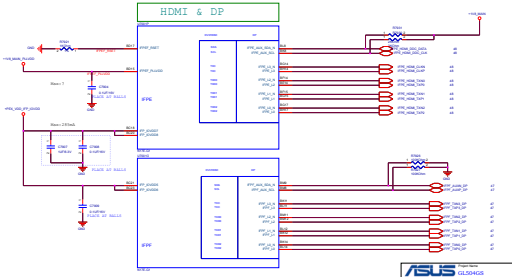








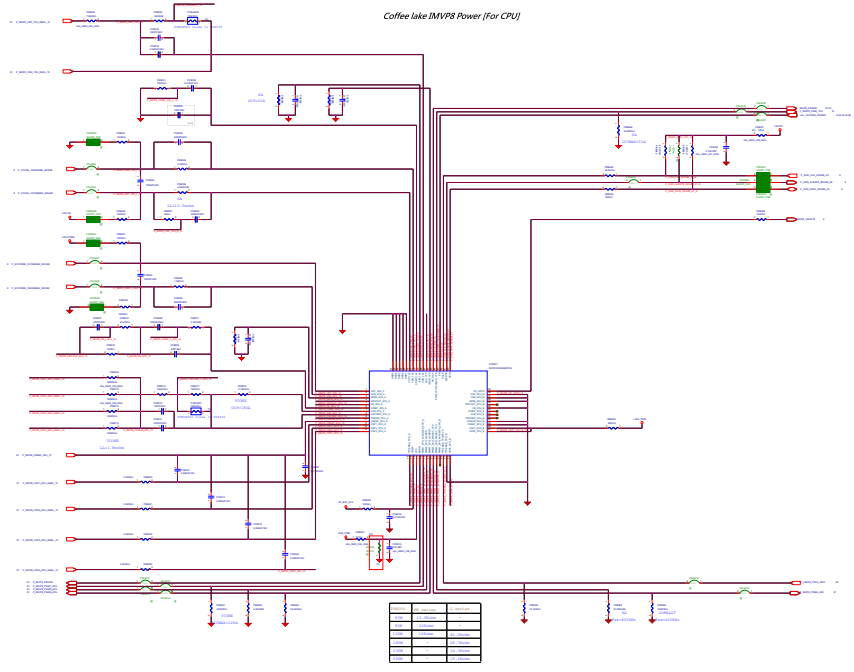


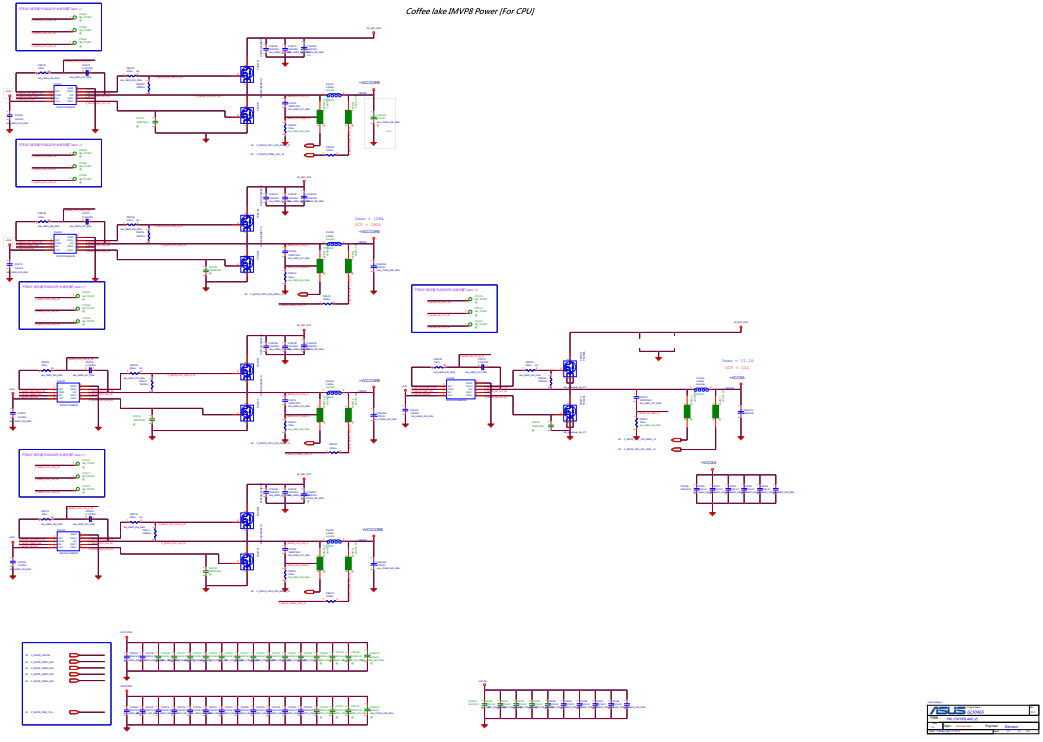


15.2.3 Unconnected Signals (NC)

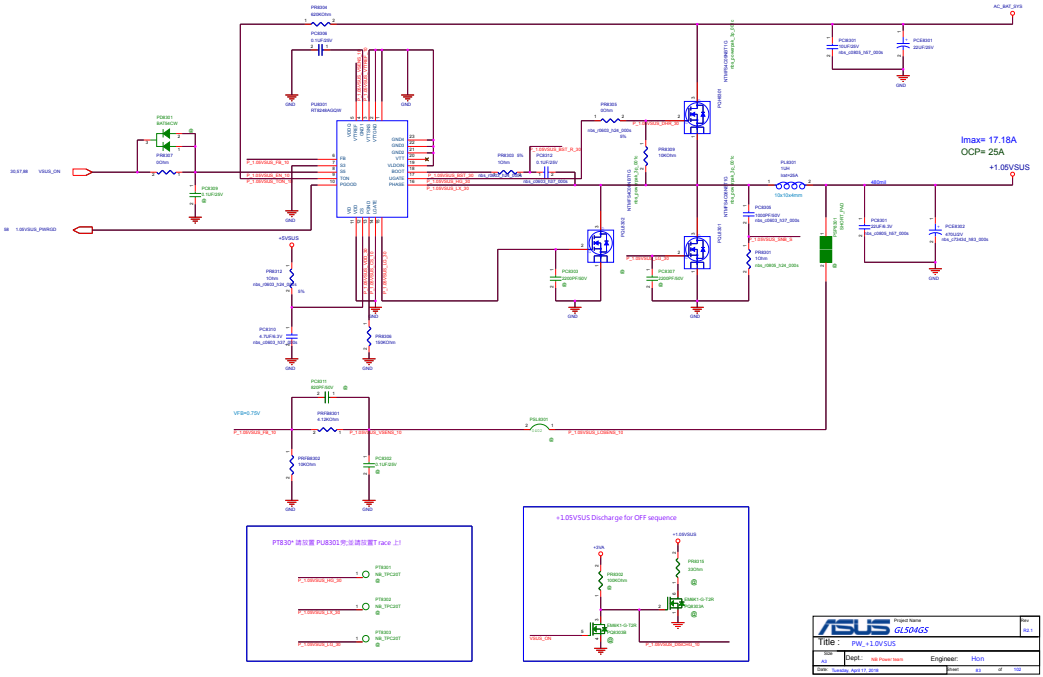
The following guidelines apply to unused MIPI interfaces:

- Power up all VDD18 pins.
- Leave MIO data pins and clock pins floating.

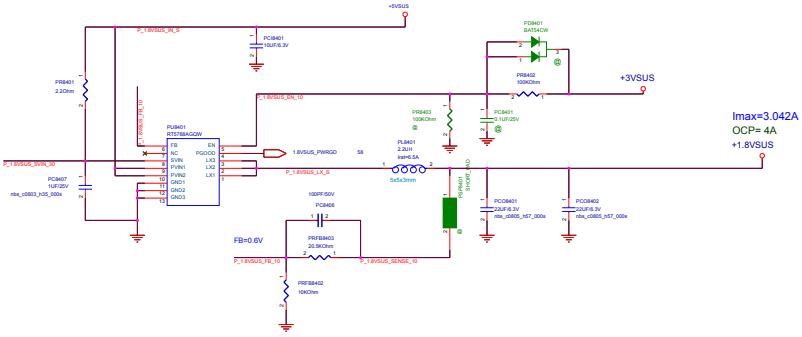

Coffee lake IMVP8 Power [For CPU]



+1.05VSUS [For PCH]



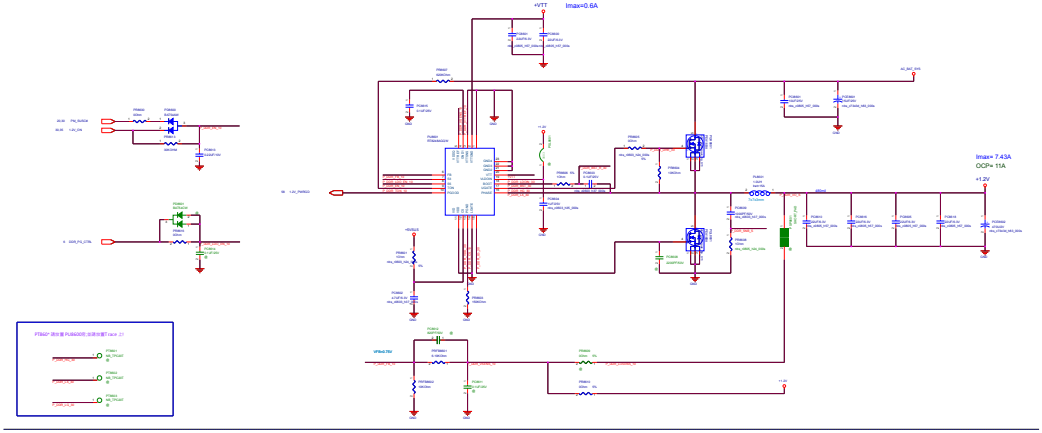
+1.8VSUS [For GPU]



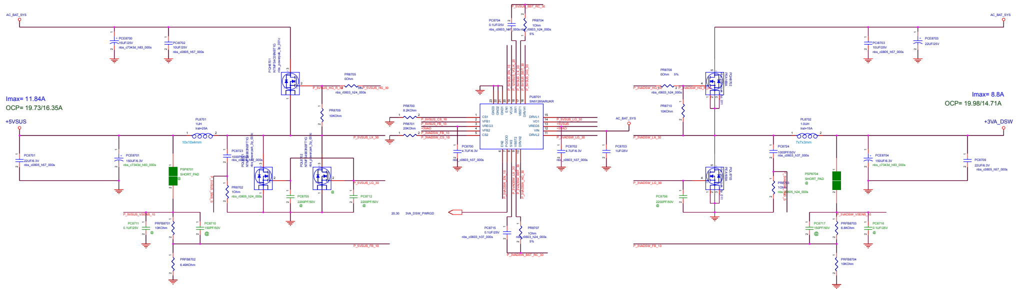
<Variant Name>

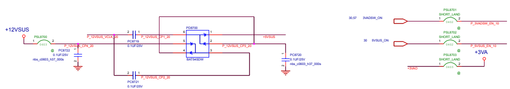
ASUS	Project Name: GL504GS		Rev: R2.1
Title : PW_+1.8VSUS			
Size: A3	Dept.: NB Power Team	Engineer: Hon	
Date: Tuesday, April 17, 2018	Sheet: 84	of: 102	

+1.2V / +VTT / +2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]





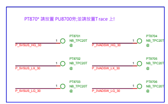
請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

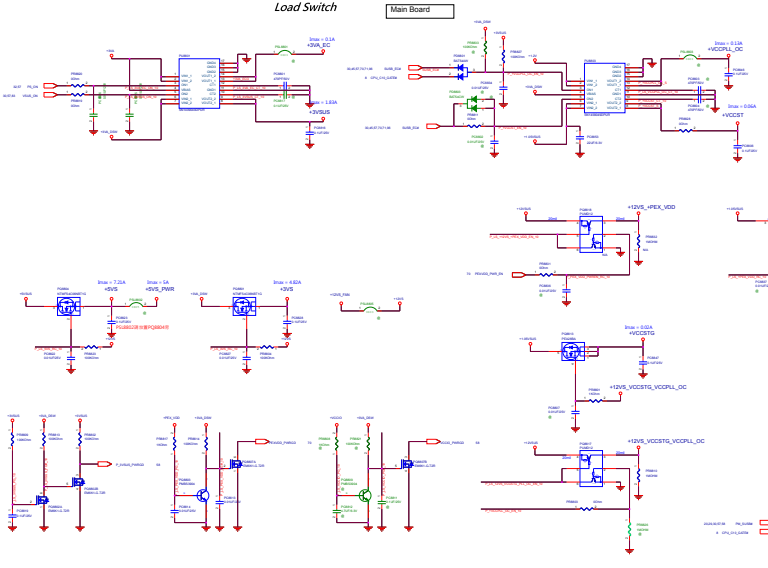


<Variant Name>

ASUS	Project Name GL504GS	Rev R2.1
Title : PW_+3VA_DSW/+5VSUS		
Size A2	Dept.: NB Power team	Engineer: Hon
Date: Tuesday, April 17, 2018	Sheet 87 of 102	

Load Switch

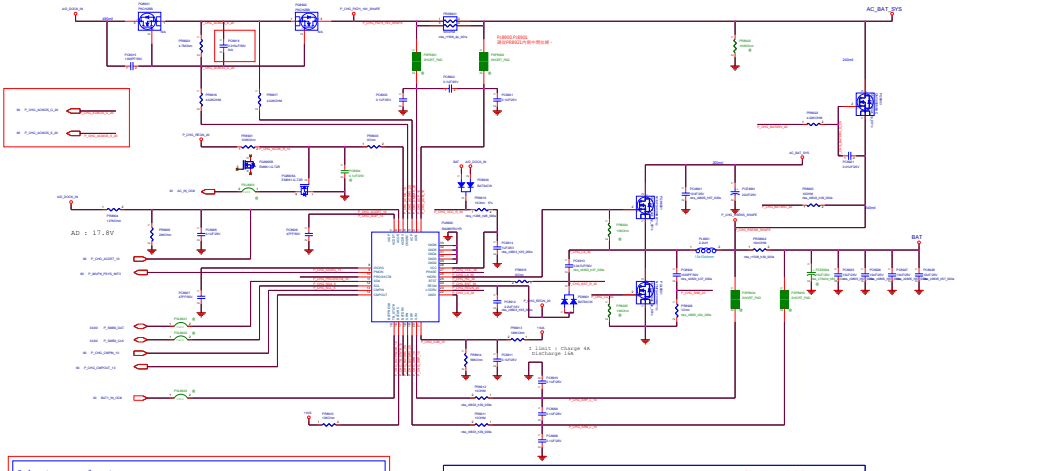
Main Board



ASUS	Project Name: GL504GS				Rev:
Title:	PW_LOAD SWITCH				
Size: A3	Project:	Design Event	Engineer:	Hsin	
Date: Thursday, April 27, 2017		Sheet: 1	of: 1		

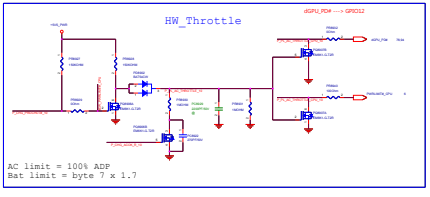
Main Board

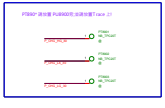
PR89801	<=150W	<=230W	>230W	>330W
	10K	5K	3K	2K



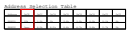
Adaptor select
total power = 90% ADP

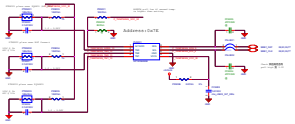
Adaptor select			
PR89334	10n	5n	
14K	0.4V	30W	120W
31.6K	0.8V	60W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	260W
270K	2.4V	90W	310W
560K	2.8V	120W	400W

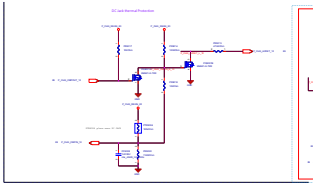


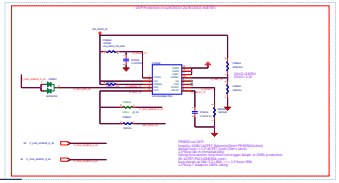


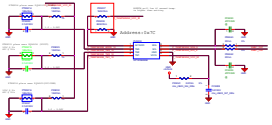
ASUS	Project name: GL504GS	Rev: 0.1
Title: PW_CHARGER		
Size:	Project:	Drawn by: Engineer: Mark
Date: Wednesday, April 11, 2018	Sheet 46 of 48	

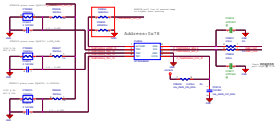


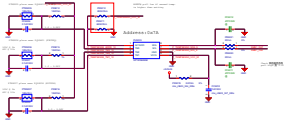


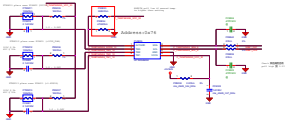












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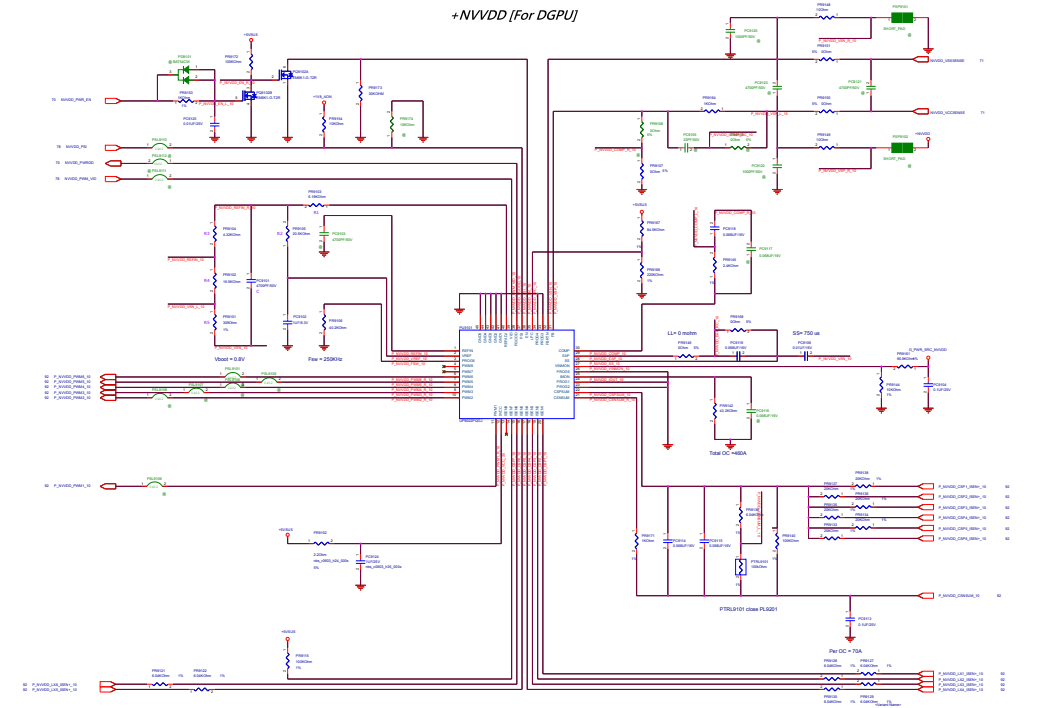
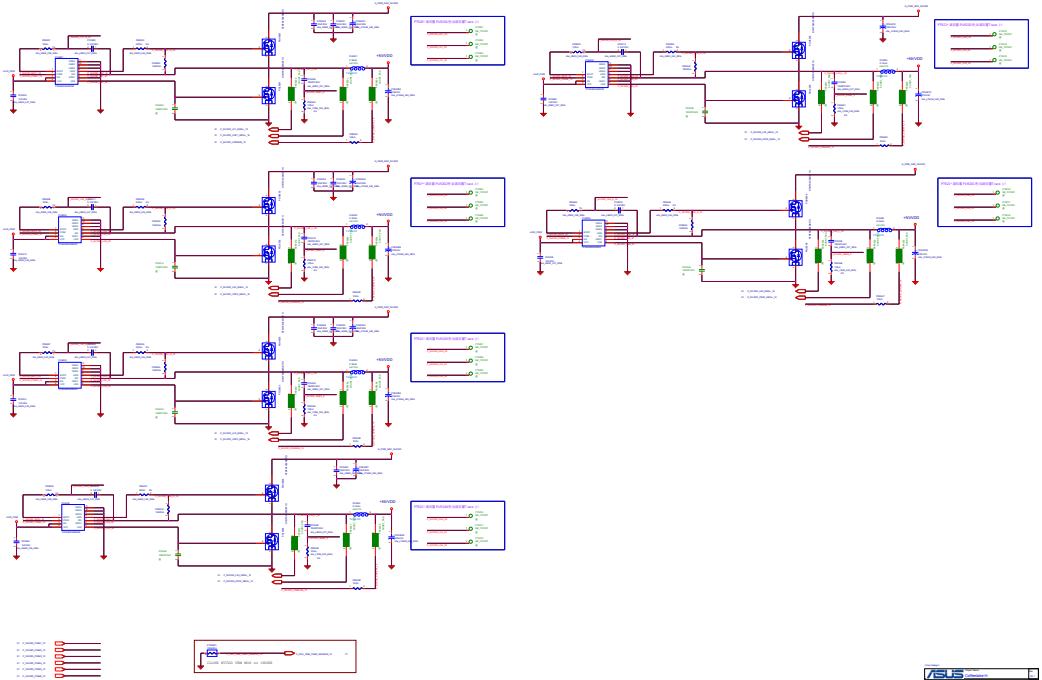
+NVVDD [For DGPU]



+NVVDD [For DGPU]

Imax=203+53.7+268.7A

Ilyn63+24.5+1.1= 53.6A



Title			
Size	Number	Revision	
Date	Sheet of		
File	Drawn By		

+FBVDDQ [For VRAM]

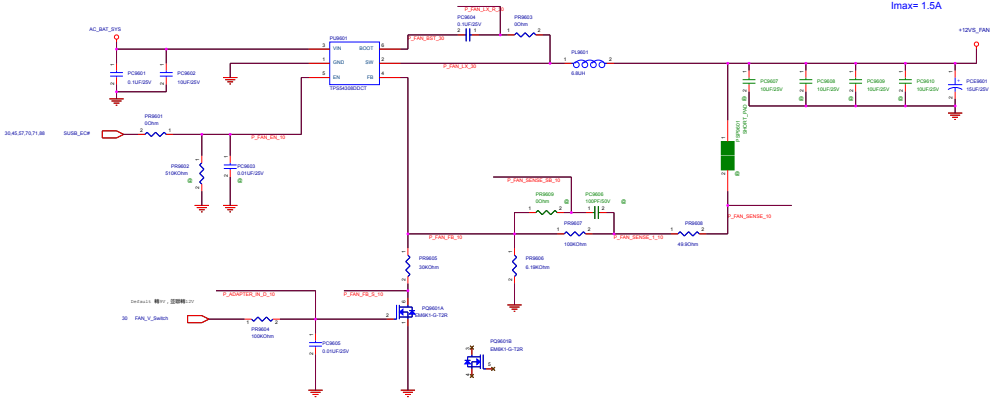
Imax=30.6A
Ityp=25A

	DVID Setting		
Clock range	0.300/1.500	1.350/2.00	1.350
PR9404	1.00Kohm	133Kohm	133Kohm
PR9405	76.7-Kohm	51.1Kohm	42.2Kohm
PR9423	44.2Kohm	64.9Kohm	

Thermal Throttle = 95℃
PT94401 close to PQN9402

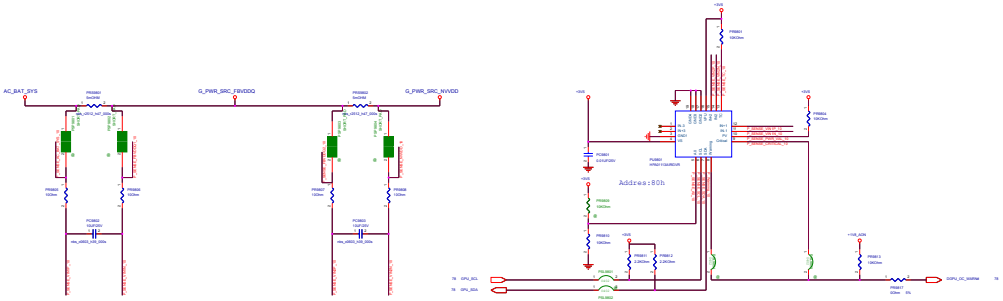
PT9402 請短置 PU94011 和 並聯短置Trace 計

ASUS Project Name: Coffeelake-H
Title: PWR_+FBVDDQ
Size: Dept.: NB Power Team
Engineer: Benson
Date: Tuesday, April 17, 2018
Sheet 52 of 102

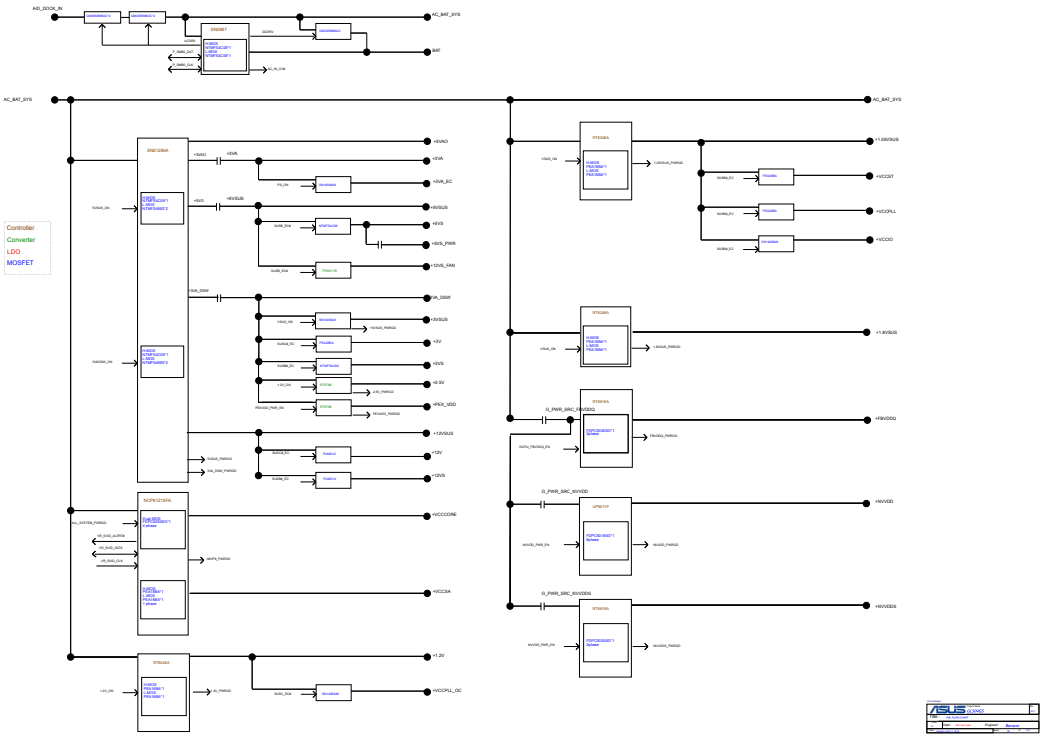


<Variant Name>

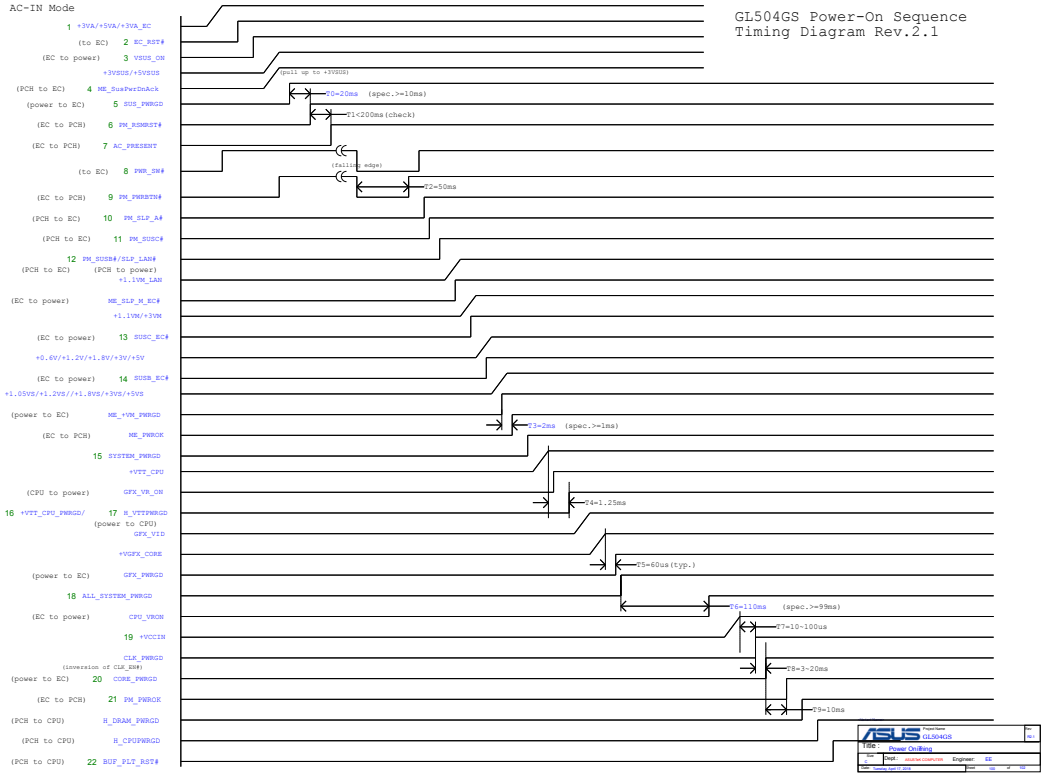
ASUS	Project Name: GL503GS	Rev: 62.1
Title : PW_+12VS_FAN		
Size: A	Dept.: NB Power team	Engineer: Edison
Date: Tuesday, April 17, 2018	Sheet 98 of 102	



Variant Name			
ASUS	Project Name: GL504GS		Rev: 0.1
Title : PWR_SRC			
Size: Custom	Dept.: Power Team	Engineer: Hsin	
Date: Tuesday, April 17, 2018	Sheet 50 of 100		


AIO_DCIN_IN
NC_BAT_SYS
BAT
AC_BAT_SYS
Controller
Converter
LDO
MOSFET
+5VNO
+3VA
+3VA_EC
+5VSUS
+5VS
+5VS_PWR
+12VS_FAN
SW_DSW
+3VSUS
+2V
+3VS
+2.5V
+PEX_VDD
+12VSUS
+12V
+12VS
+VCCCORE
+VCCSA
+1.2V
+VCCPLL_OC
+1.05VSUS
+VCCST
+VCCPLL
+VCCIO
+1.8VSUS
+1.8VSDQ
G_PWR_SRC_1V05SDQ
+1.05VDD
G_PWR_SRC_NVVDD
+NVVDD
G_PWR_SRC_NVVDDS
+NVVDDS

GL504GS Power-On Sequence Timing Diagram Rev.2.1



GL504GS Power-On Sequence Timing Diagram Rev.2.1