PROJECT NAME : BAL22 15" , BAL32 17"
PCB NO : LA-D803P(Bristol)

Dell / Compal Confidential

Schematic Document

AMD Bristol
AMD R16M-M70 (23 X 23mm)+GDDR5 x4

2016-06.21 Rev: 1.0 (A00)

@ : Un-pop Component
FX_R3@/A12_R3@/A10_R3@:APU R3 PN
FX_R1@/A12_R1@/A10_R1@:APU R1 PN
45@/ HDMI LOGO
PCB@/ MB part number
PCB_R3G@/PCB_R3T@PCB_R3H@:PCB R3 PN
ST@ / stoney only
BR@ /Bristol only
4G_S@/4G_M@/4G_H@/2G_H@/2G_M@/2G_S:VRAM Strap Pin:
S4G_R1@:samsung R1/ H4G_R1@:Hynix R1 /M4G_R1@ :Micron R1
S4G_R3@:samsung R3/ H4G_R3@:Hynix R3 /M4G_R3@ :Micron R3
DIS@/ GPU only
M30@/ R16M1-M30
M70@ /R16M1-M70
M30_R3@/M70_R3@:GPU R3 PN
M30_R1@/M70_R1@:GPU R1 PN
UMA@/ UMA only
TI@/PARADE@/NRDSA@ : SATA
3234@/3246@ :Audio
EMI@/ESD@/RF@ : EMI, ESD ,RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD,RF unpop
KBBL@:for KB backlight use
PTP@/NPTP@/TP_WAKE@:Touch pad
HDT@ /Debug use

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Title	Cover Page		
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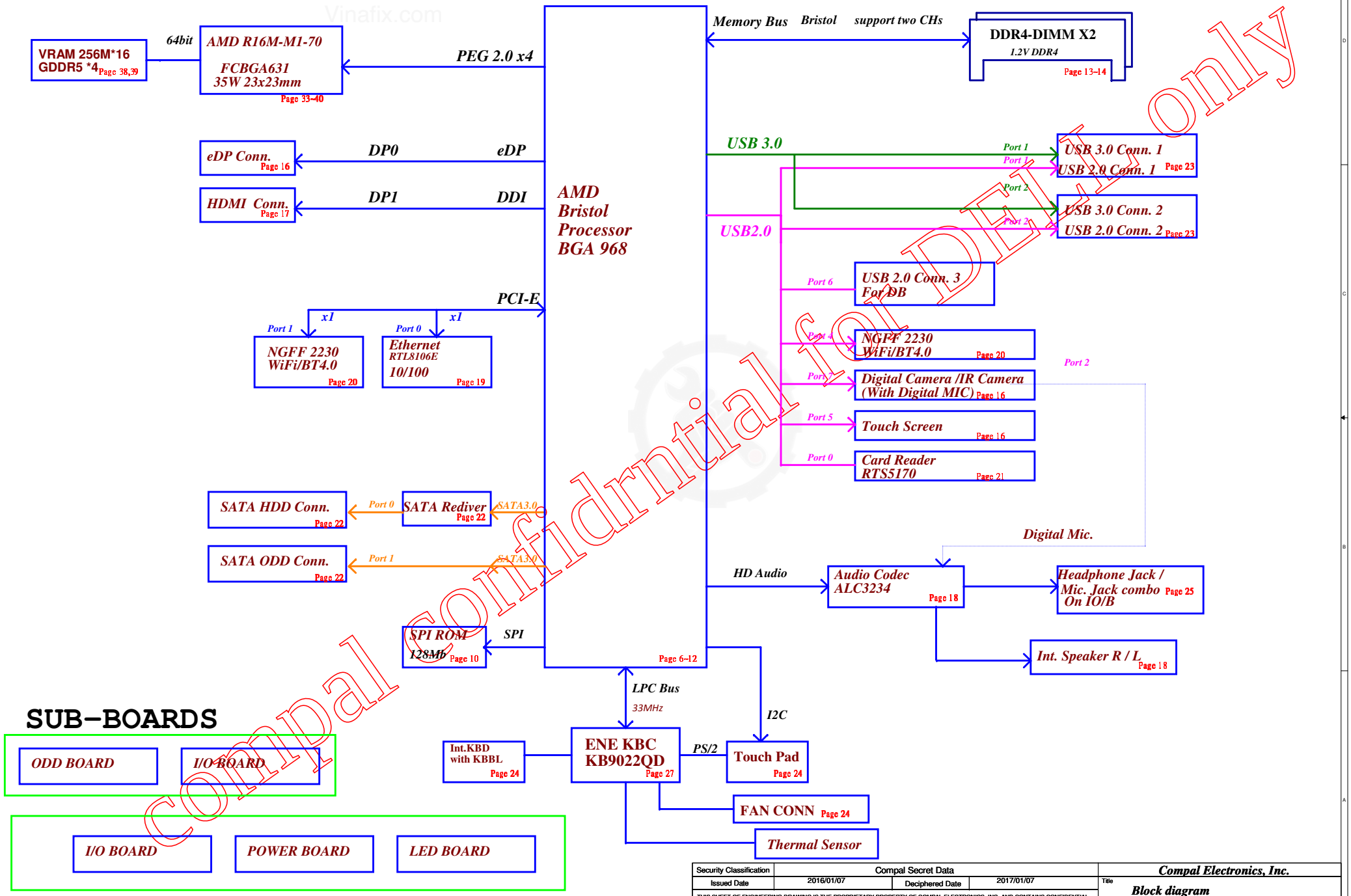

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: BAL22 LA-D803P		Rev: A00
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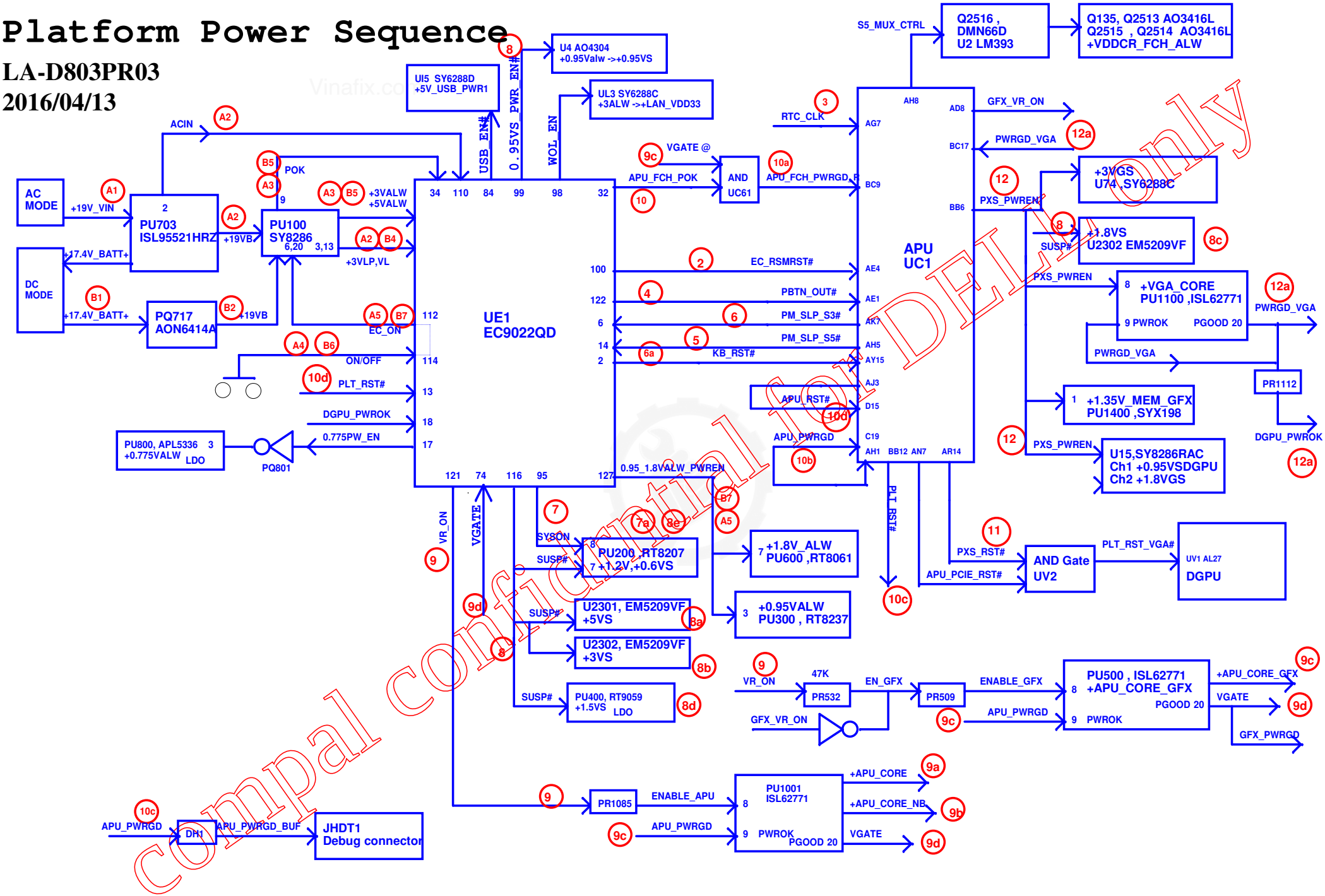
Platform Power Sequence

LA-D803PR03
2016/04/13



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Compal Electronics, Inc.

Title: *Power Sequence diagram*

Size: Document Number: *BAL22 LA-D803P* Rev: A00

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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	bristol EVT
1	bristol DVT1
2	bristol DVT2
3	bristol XB
4	
5	
6	
7	
8	
9	
10	Stoney
11	Stoney
12	Stoney
13	Stoney
14	Stoney
15	Stoney
16	Stoney
17	Stoney
18	Stoney
19	Stoney

SMBUS Control Table

	SOURCE	BATT	Charger		DIMM		Thermal Sensor		
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9022Q						V		
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q								
APU_SCLK0 APU_SDATA0	APU				V				
APU_SCLK1 APU_SDATA1	APU								
APU_SIC APU_SID	APU						V		

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	10/100 LAN
CLKOUT_PCIE1	NGFF Card (WLAN)
CLKOUT_PCIE2	
CLKOUT_PCIE3	
GFX CLK	dGPU

ULT	USB3.0	
	Port1	NA
	Port2	USB3 connector 1
	Port3	USB3 connector 2
	Port4	NA
	USB2.0	
	Port0	Card Reader
	Port1	Touch Screen Panel
	Port2	Camera
	Port3	USB connector 1(D/B)
	Port4	NGFF Card (WLAN)
	Port5	USB connector 1
	Port6	USB connector 2
	Port7	NA
	PCI EXPRESS	
	Lane 1	10/100 LAN
	Lane 2	NGFF Card (WLAN)
	Lane 3	
	Lane 4	
	Lane 5	PEG (AMD)M70
	Lane 6	PEG (AMD)M70
	Lane 7	PEG (AMD)M70
	Lane 8	PEG (AMD)M70
	SATA	
	SATA0	HDD
	SATA1	ODD

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Compal Electronics, Inc.

Title: Notes List

Size: B

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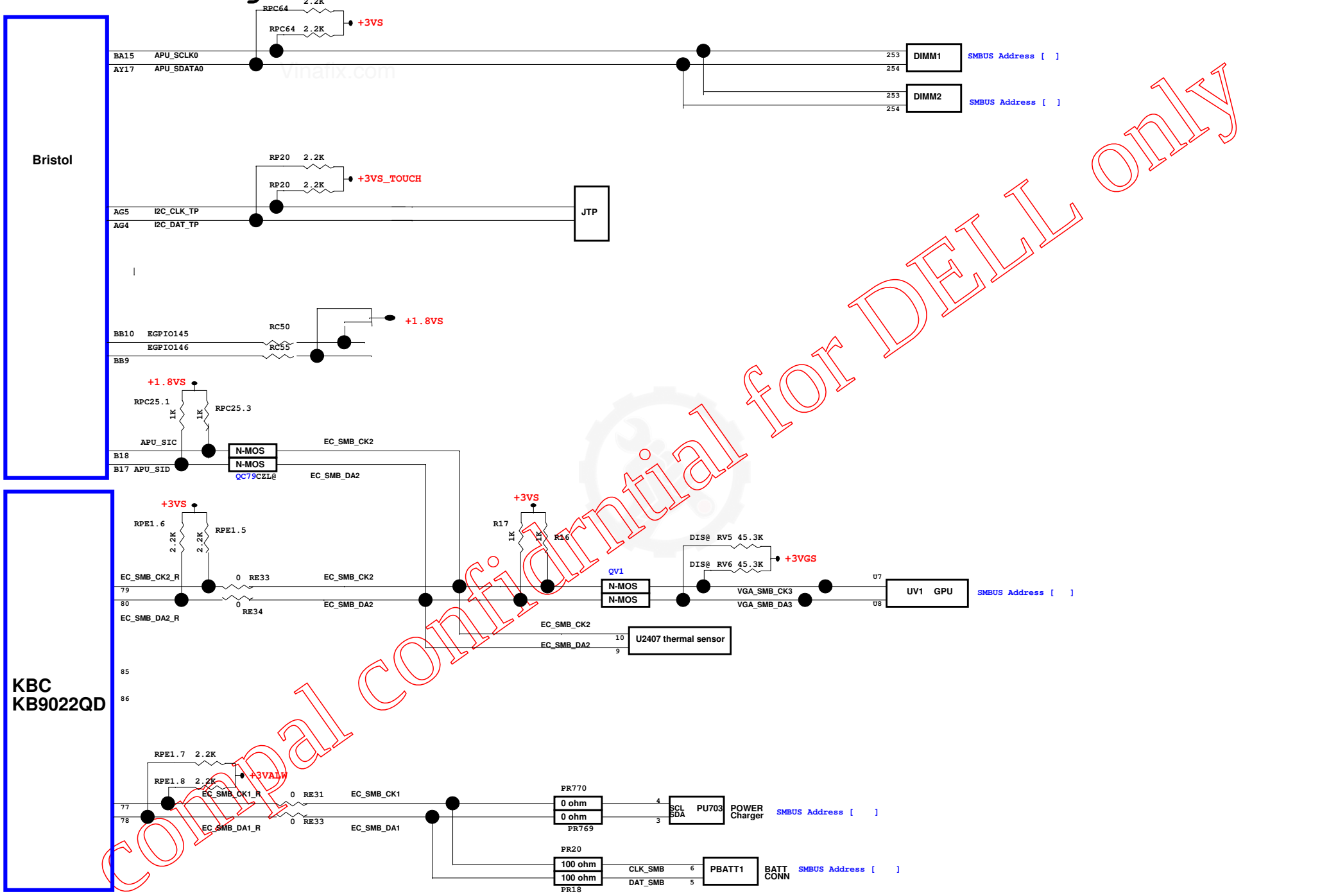
SMBus Block Diagram



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: SMBus block diagram		
Size	Document Number: BAL22 LA-D803P	Rev: A00
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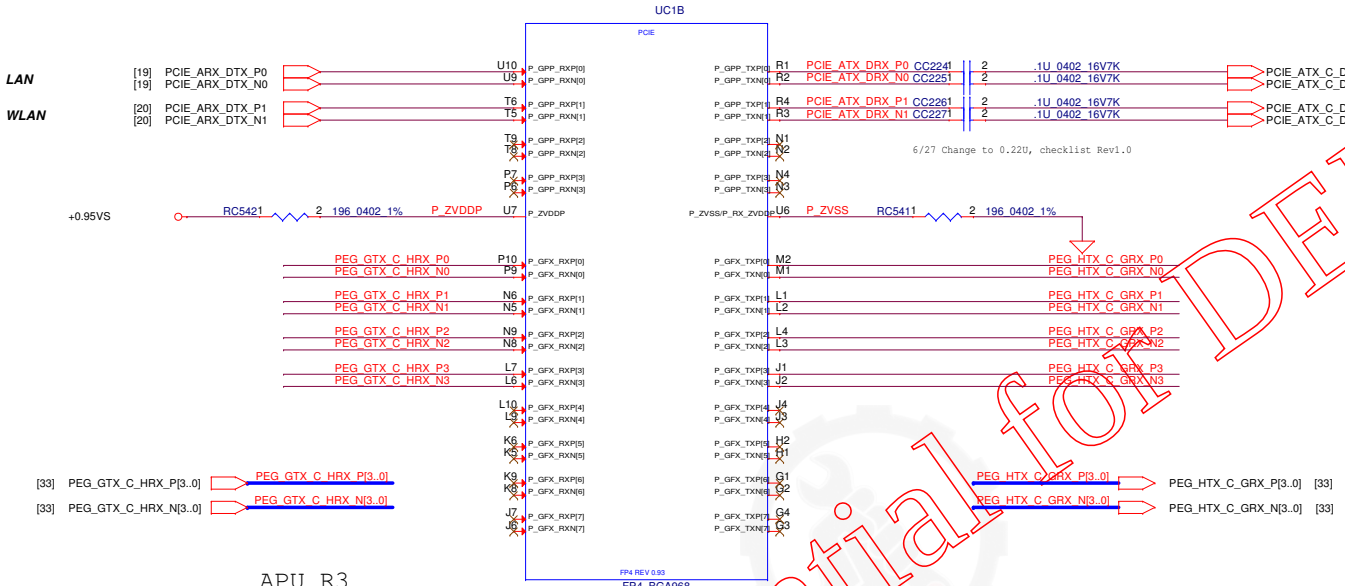
Main Func = CPU



APU R1

UC1 SA00009LB0L FX_R1@
S IC FX-9800P FM980PADY44AB 2.7G BGA 968P

UC1 SA00009LC0L A12_R1@
S IC A12-9700P AM970PADY44AB 2.5G BGA 968P

UC1 SA00009LD0L A10_R1@
S IC A10-9600P AM960PADY44AB 2.4G BGA 968P

APU R3

UC1 SA00009LB1L FX_R3@
S IC FX-9800P FM980PADY44AB 2.7G A31!

UC1 SA00009LC1L A12_R3@
S IC A12-9700P AM970PADY44AB 2.5G A31!

UC1 SA00009LD1L A10_R3@
S IC A10-9600P AM960PADY44AB 2.4G A31!

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: FP4 PCIE/UMI

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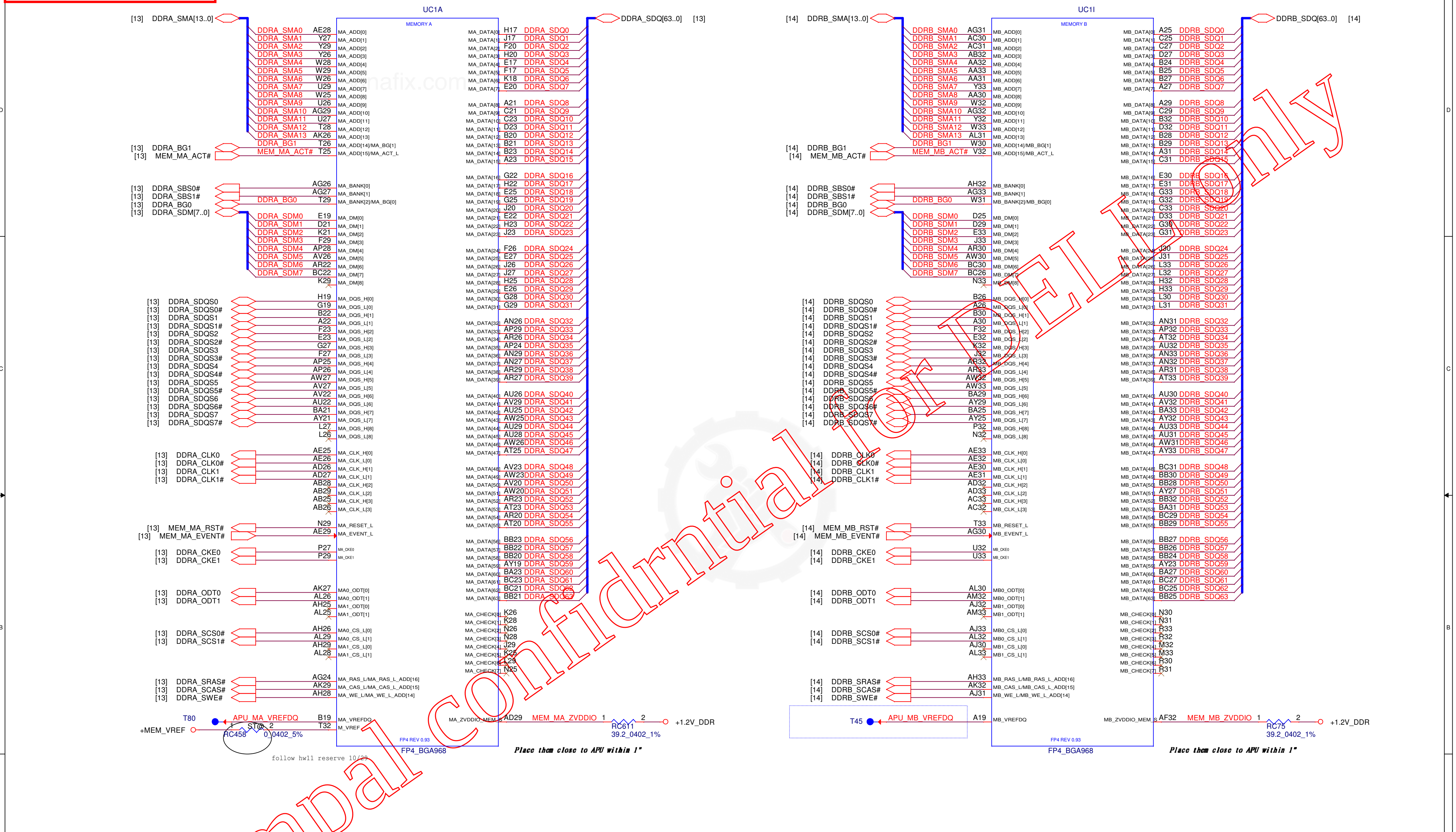
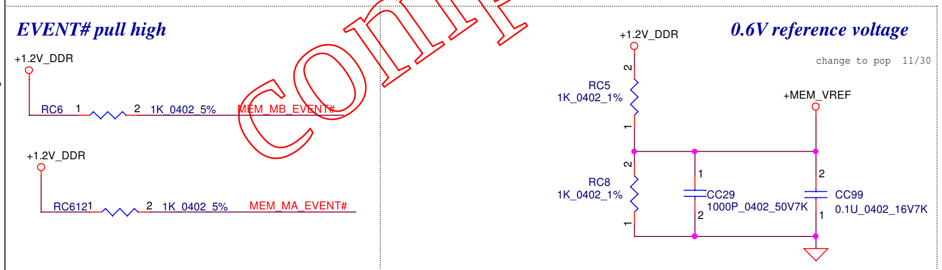
Main Func = CPU





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Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: FP4 DDR4 MEMORY I/F

Size: Custom | Document Number: BAL22 LA-D803P | Rev: A00

Main Func = CPU

DP1: HDMI
DP0: eDP

UC1C
DISPLAY/SVID/JTAG/TEST
FP4_BGA968

HDMI
eDP

2014/08/12 Modify

Place near APU

del colay crt circuit 10/16

remove cap for emi 10/16

del cz@ 10/15

PU at EC side

follow esd require 11/27

reserve 0 ohm 11/24

del edp hpd buffer 10/18

add test point 10/16

change to pu up11/19

change to 0.01u 10/19

HDT+

HDT debug + HDT@

JHDT1 CONN@
SAMTE_ASP-136446-07-B

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Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: FP4 DISP/MISC/HDT

Size: Custom | Document Number: BAL22 LA-D803P | Rev: A00

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Main Func = CPU

VBIOS (PCBA VRAM Size Config.)	VBIOS_ID3 (AGPIO102)	VBIOS_ID2 (AGPIO64)	VBIOS_ID1 (AGPIO66)
2G GDDR5	0	0	0
4G GDDR5	0	0	1
2G DDR3	0	1	0
Reserved	0	1	1

UMA: LOW
DIS: HIGH

	LPC_CLK0_EC	LPC_CLK1	LPC_FRAME#	MEM_VOLT_SEL	RTC_CLK <INT PU>	BLINK/GPIO11 <INT PU>	SYS_RST# <INT PU>
H	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	SPI ROM (DEFAULT)	Enhanced Reset logic (default)	COIN BATT ON BOARD (DEFAULT)	LDT_RST#/PG OUTPUT TO APU (DEFAULT)	NORMAL RESET MODE (DEFAULT)
L	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	LPC ROM	Traditional Reset logic:	COIN BATT NOT ON BOARD	OUTPUT TO PADS	SHORT RST MODE

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Issued Date	2016/01/07	Deciphered Date	2017/01/07
Title	FP4 GPIO/AZ/MISC/STRAPS		
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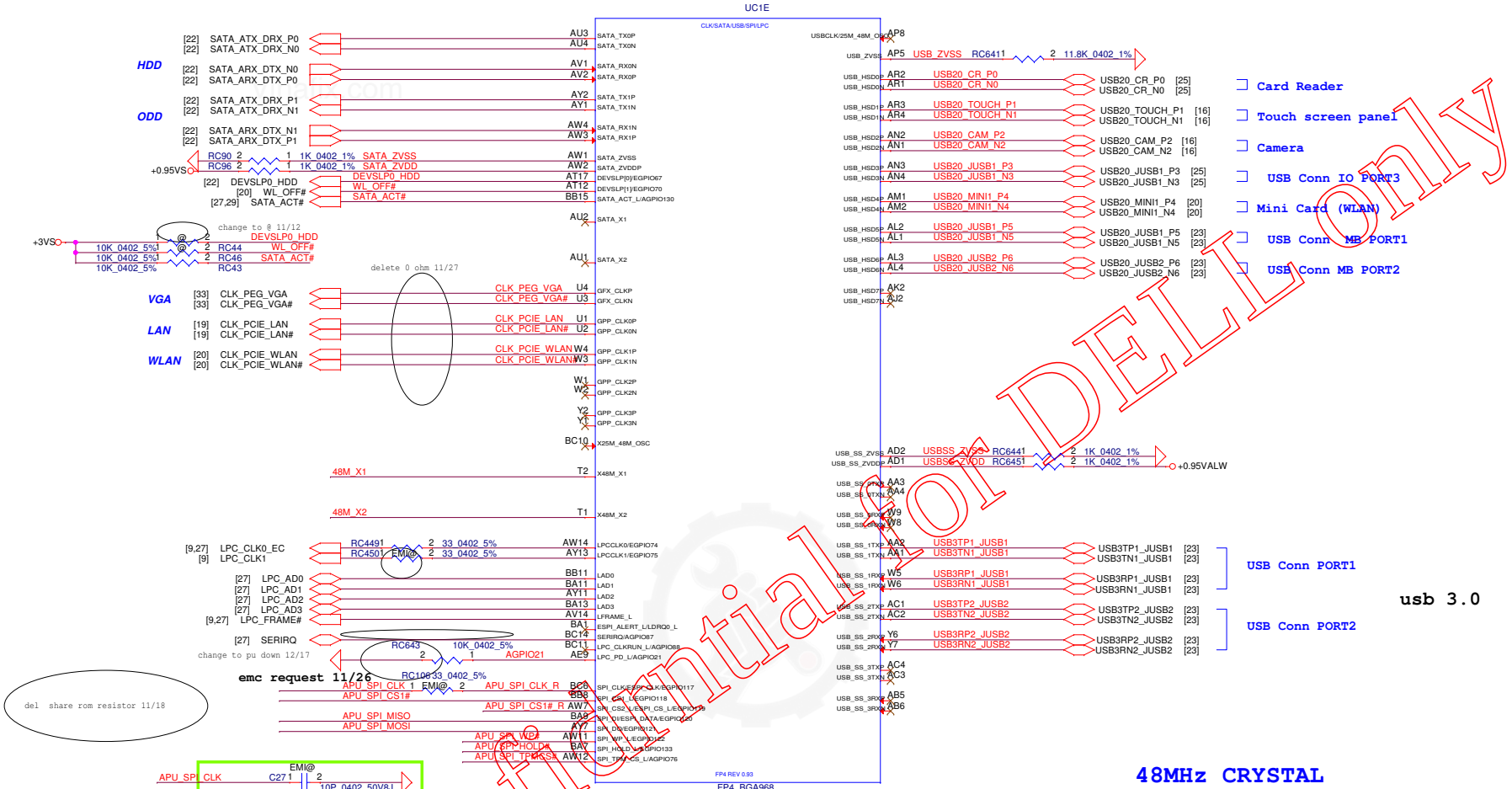
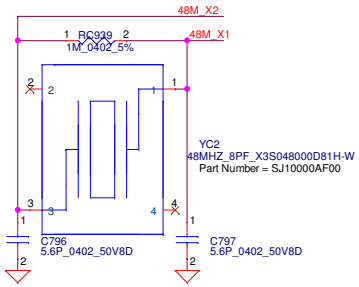
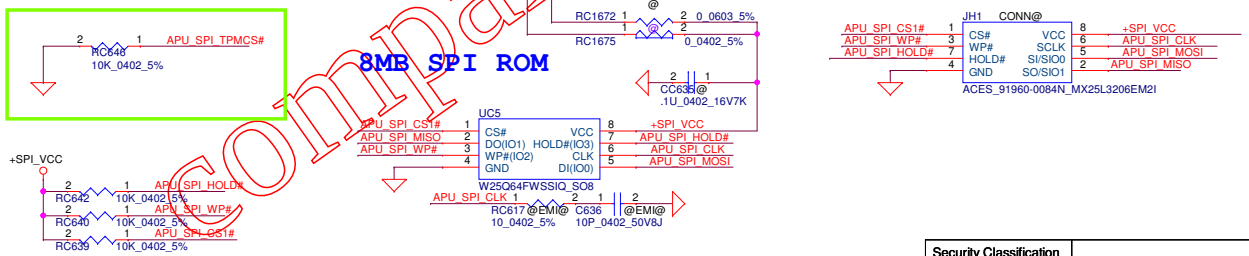
Main Func = CPU



48MHz CRYSTAL



8MB SPI ROM



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Compal Electronics, Inc.	
Title	FP4 SATA/CLK/USB/SPI
Size: Custom	Document Number: BAL22 LA-D803P
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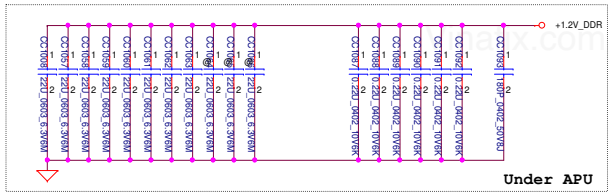
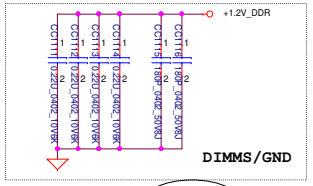
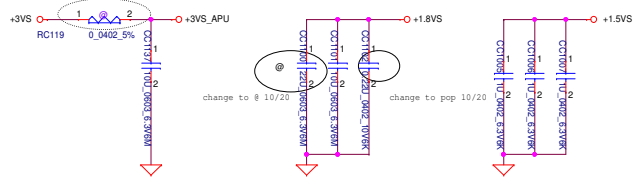
Date: Tuesday, June 21, 2016	Sheet 10 of 56

Main Func = CPU





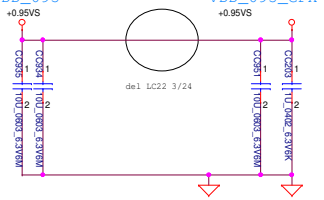
change to shortpad 03/10
FOR DEBUG ONLY



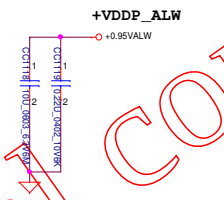
+0.95VALW/+0.95VS OF APU

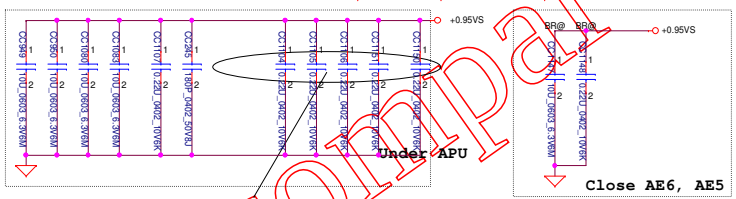
+VDDP_VS

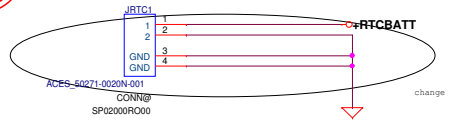
VDD_095 VDD_095_GFX

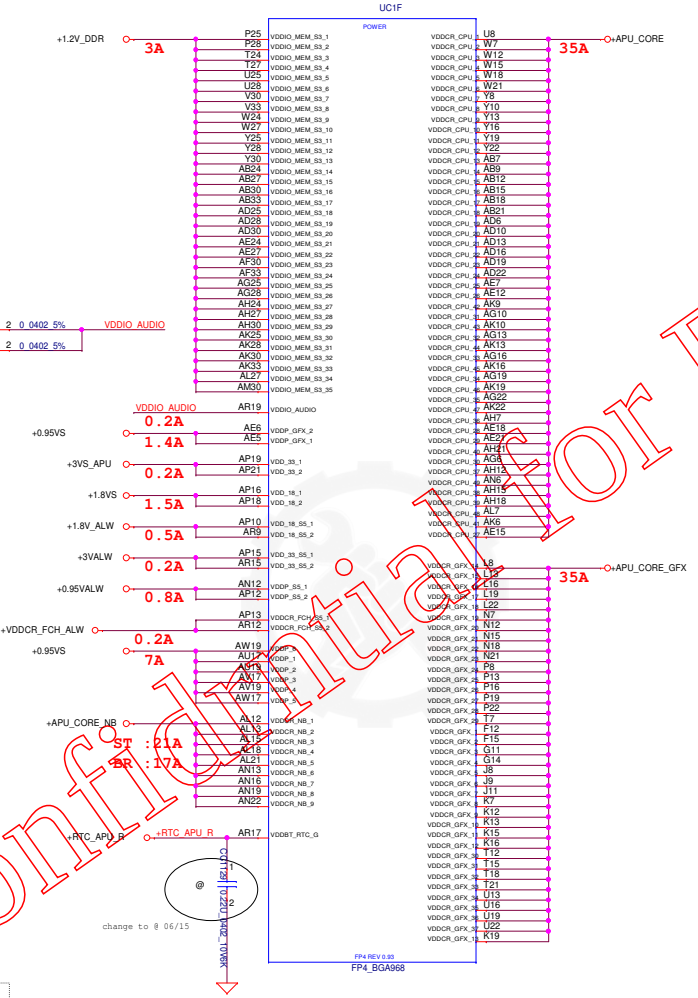


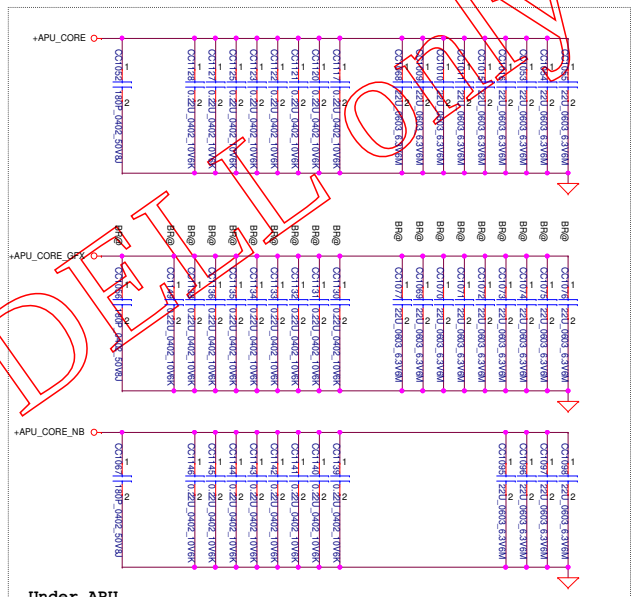
+VDDP_ALW

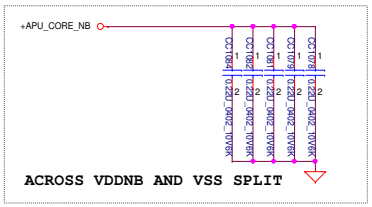








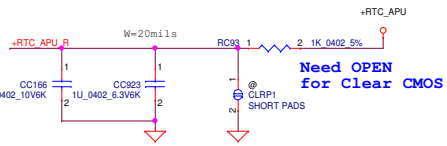




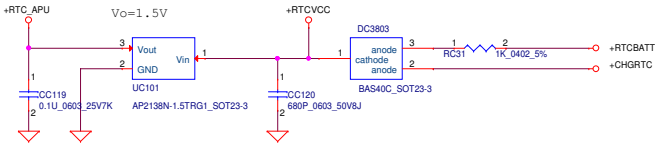
OPEN

SHORT

RTC OF APU



Need OPEN for Clear CMOS



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Compal Electronics, Inc.

Title: FP4 PWR

Size	Document Number	Rev
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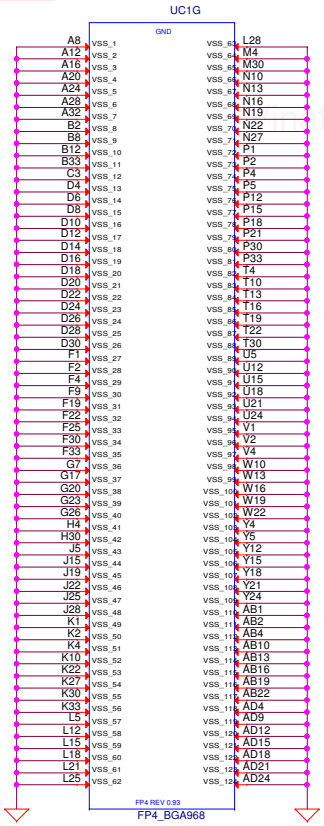
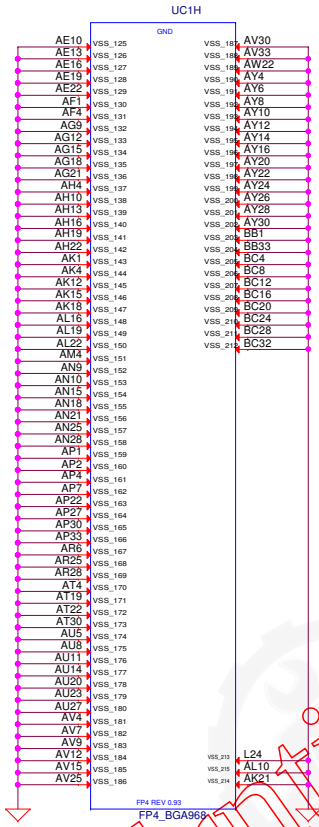
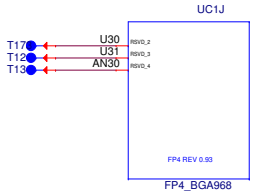
Main Func = CPU







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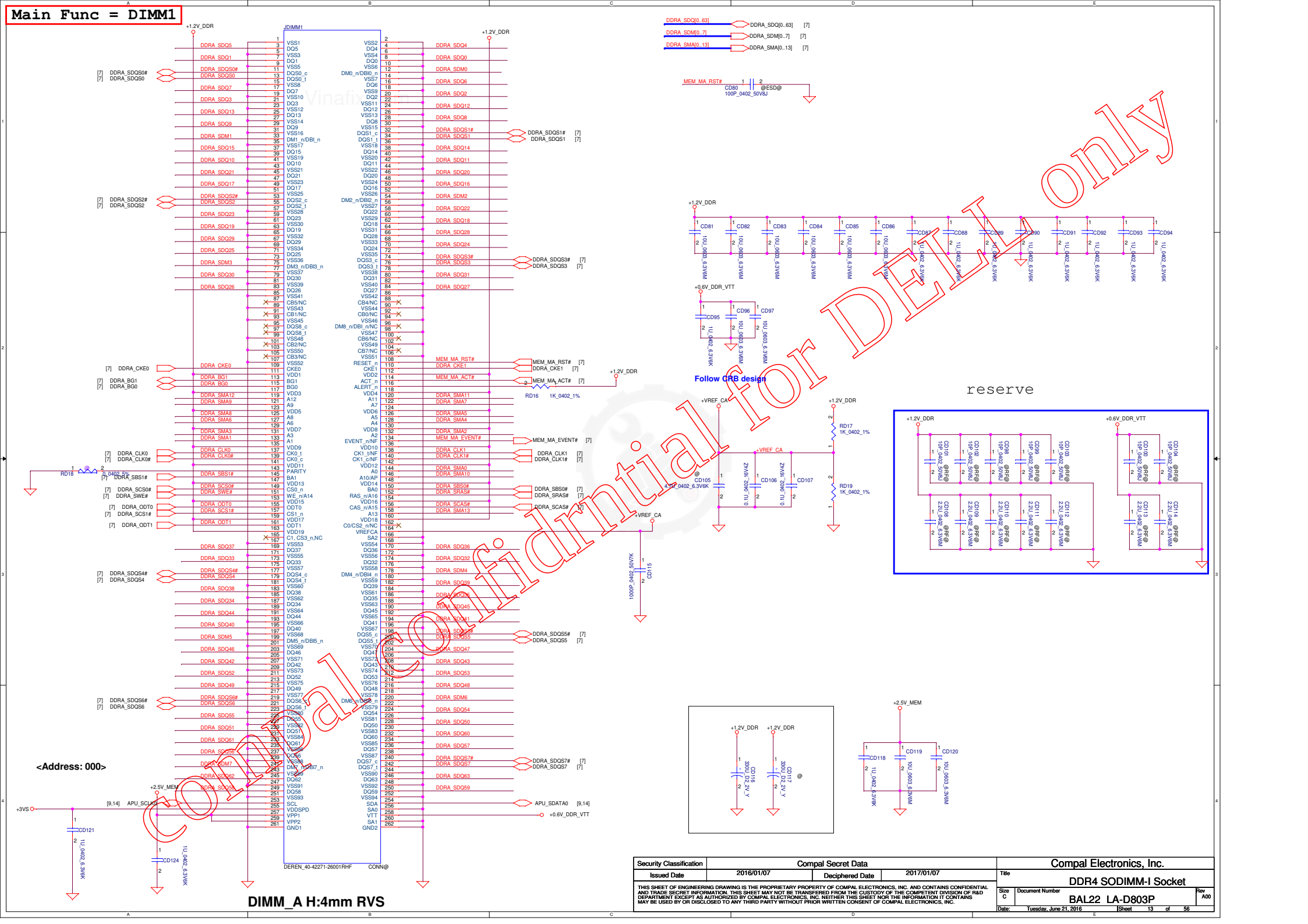
Issued Date	2016/01/07	Deciphered Date 2017/01/07	Title: FP4 GND
			Size: Custom; Document Number: BAL22 LA-D803P; Rev: A00
			Date: Tuesday, June 21, 2016; Sheet 12 of 56

Main Func = DIMM1



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: DDR4 SODIMM-I Socket

Size	Document Number	Rev
C	BAL22 LA-D803P	A00

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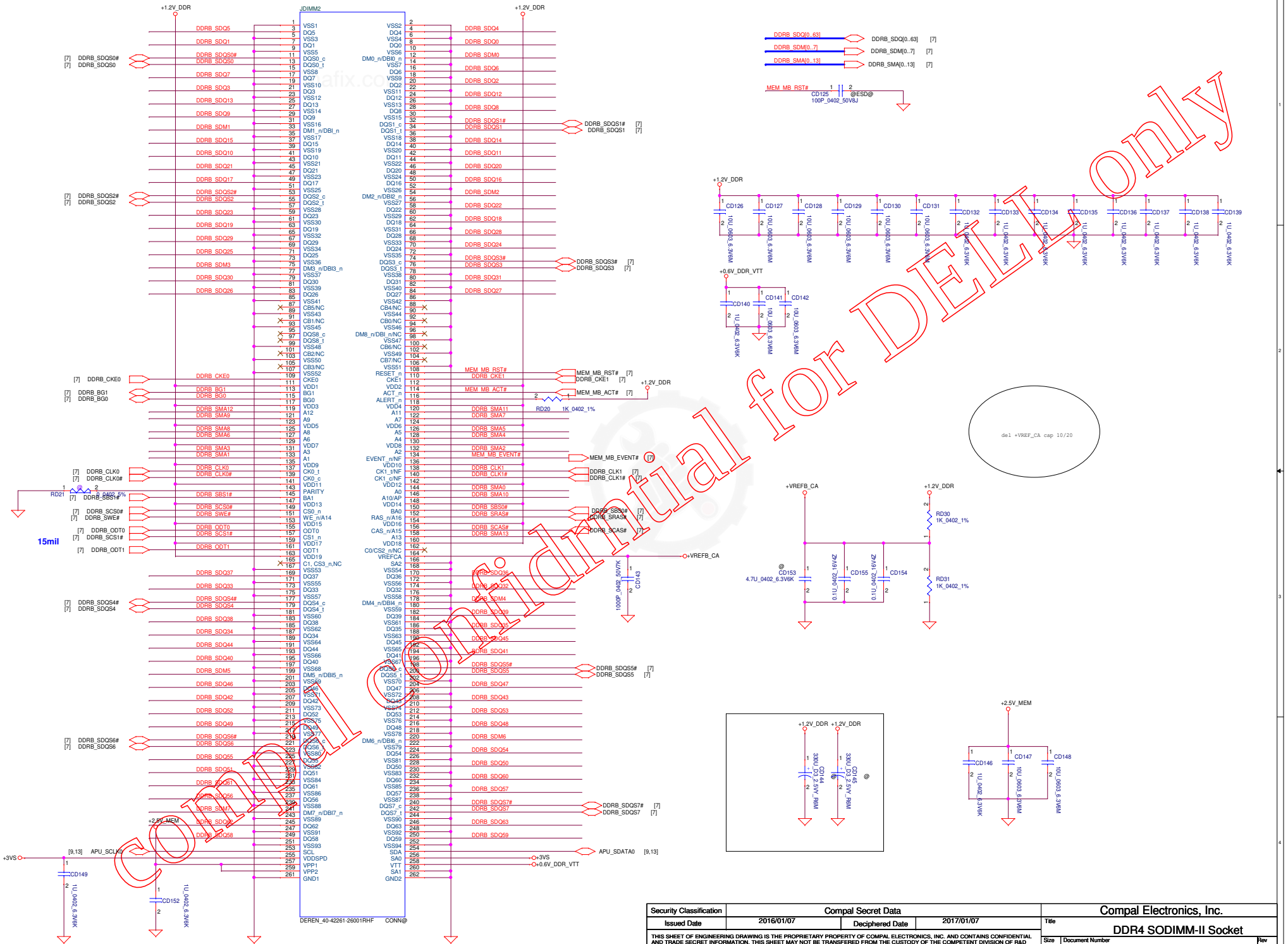
Main Func = DIMM2



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: DDR4 SODIMM-II Socket

Size	Document Number	Rev
C	BAL22 LA-D803P	A00

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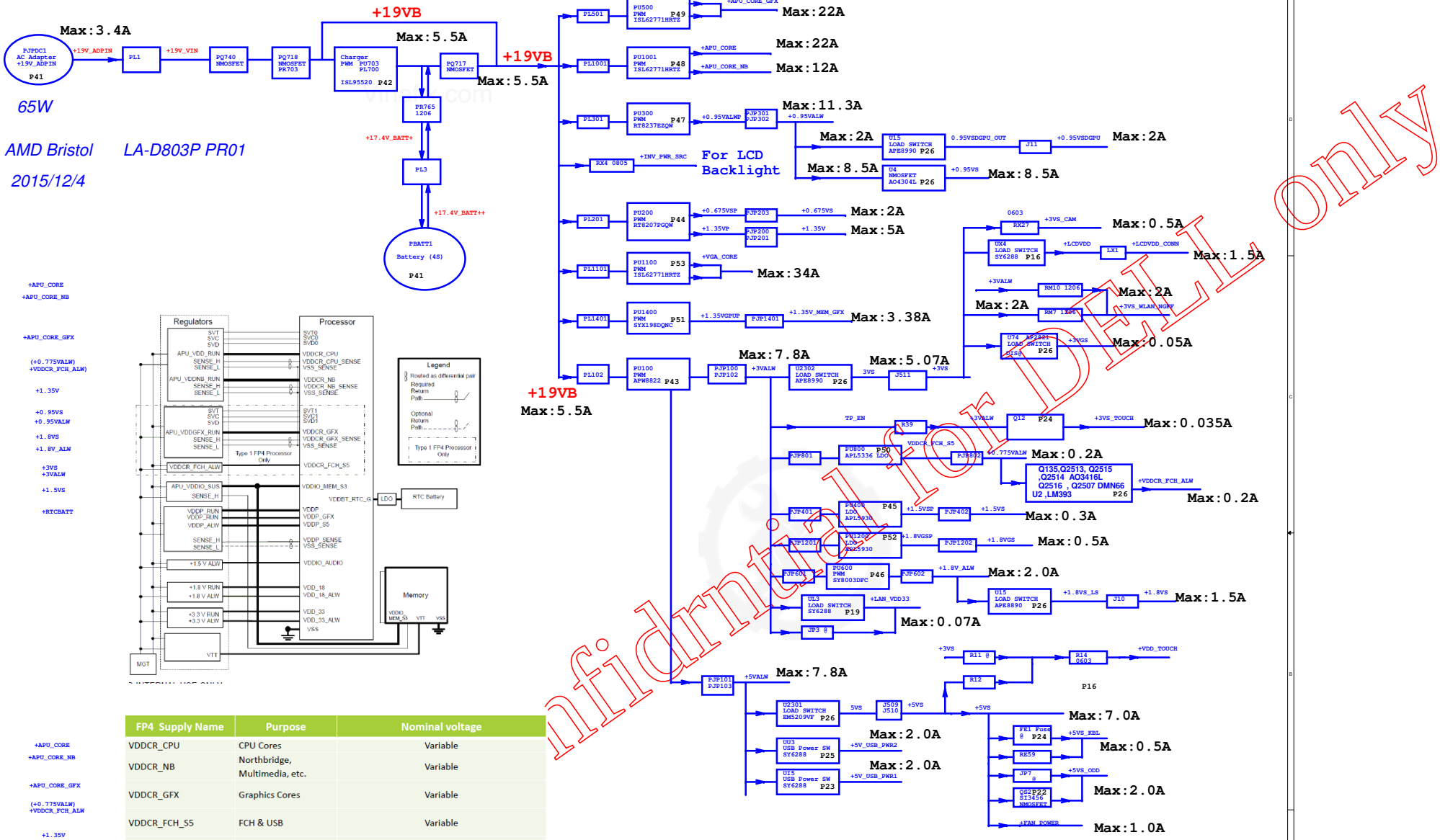
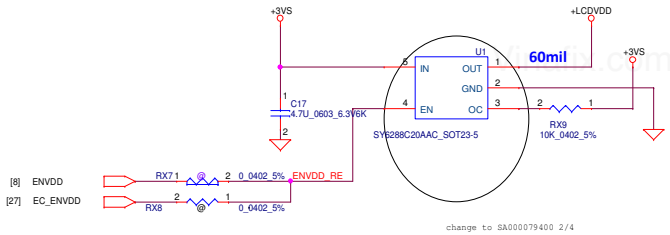
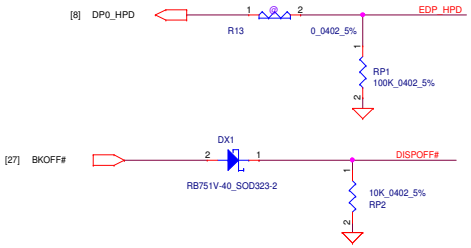


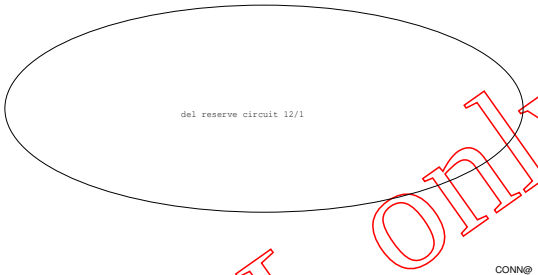
FP4 Supply Name	Purpose	Nominal voltage
VDDCR_CPU	CPU Cores	Variable
VDDCR_NB	Northbridge, Multimedia, etc.	Variable
VDDCR_GFX	Graphics Cores	Variable
VDDCR_FCH_S5	FCH & USB	Variable
VDDIO_MEM_S3	MEM PHY	DDR3 = 1.5V, 1.35V, DDR4 = 1.20V
VDDP	PCIE & DISPLAY PHYs	1.05V
VDDP_GFX	x8 dGPU PCIE PHY	
VDDP_S5	USB PHYs	
VDD_18	PLLs	1.8V
VDD18_S5	RTC, USB2, USB3	1.8V
VDD_33	GPIO (S0), SDIO, I2C, LPC, etc.	3.3V
VDD_33_S5	GPIO (S5), USB2	3.3V
VDDIO_AUDIO	AZ, I2S	1.5V (AZ)/1.8V (I2S)
VDDBT_RTC_G	RTC	1.5V

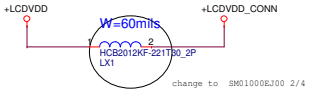
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date 2017/01/07	Title: Green CLK
			Size: Document Number: BAL22 LA-D803P Rev: A00
			Date: Tuesday, June 21, 2016 Sheet 15 of 56

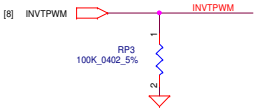
Main Func = LCD

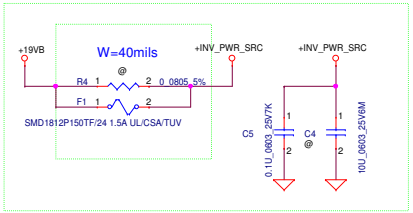


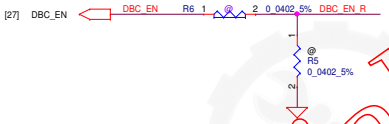


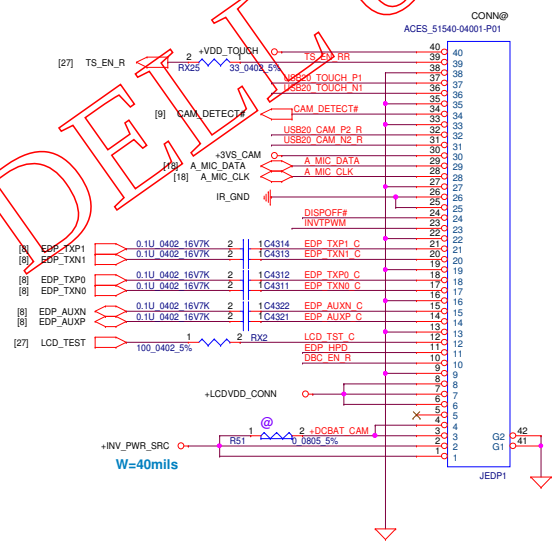




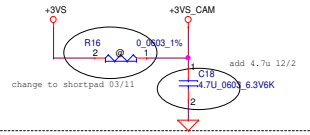


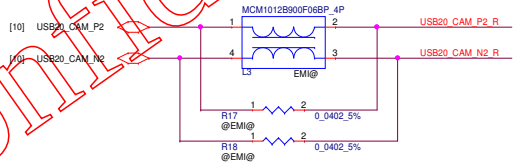


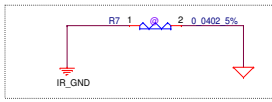




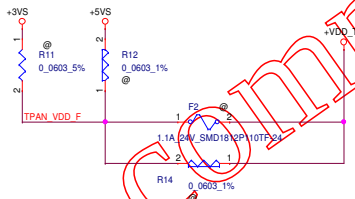
Webcam PWR CTRL

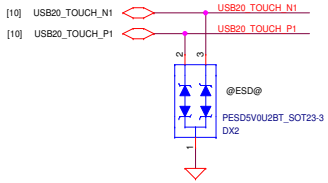


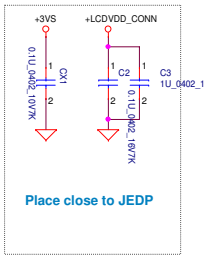




* Touch Screen Panel

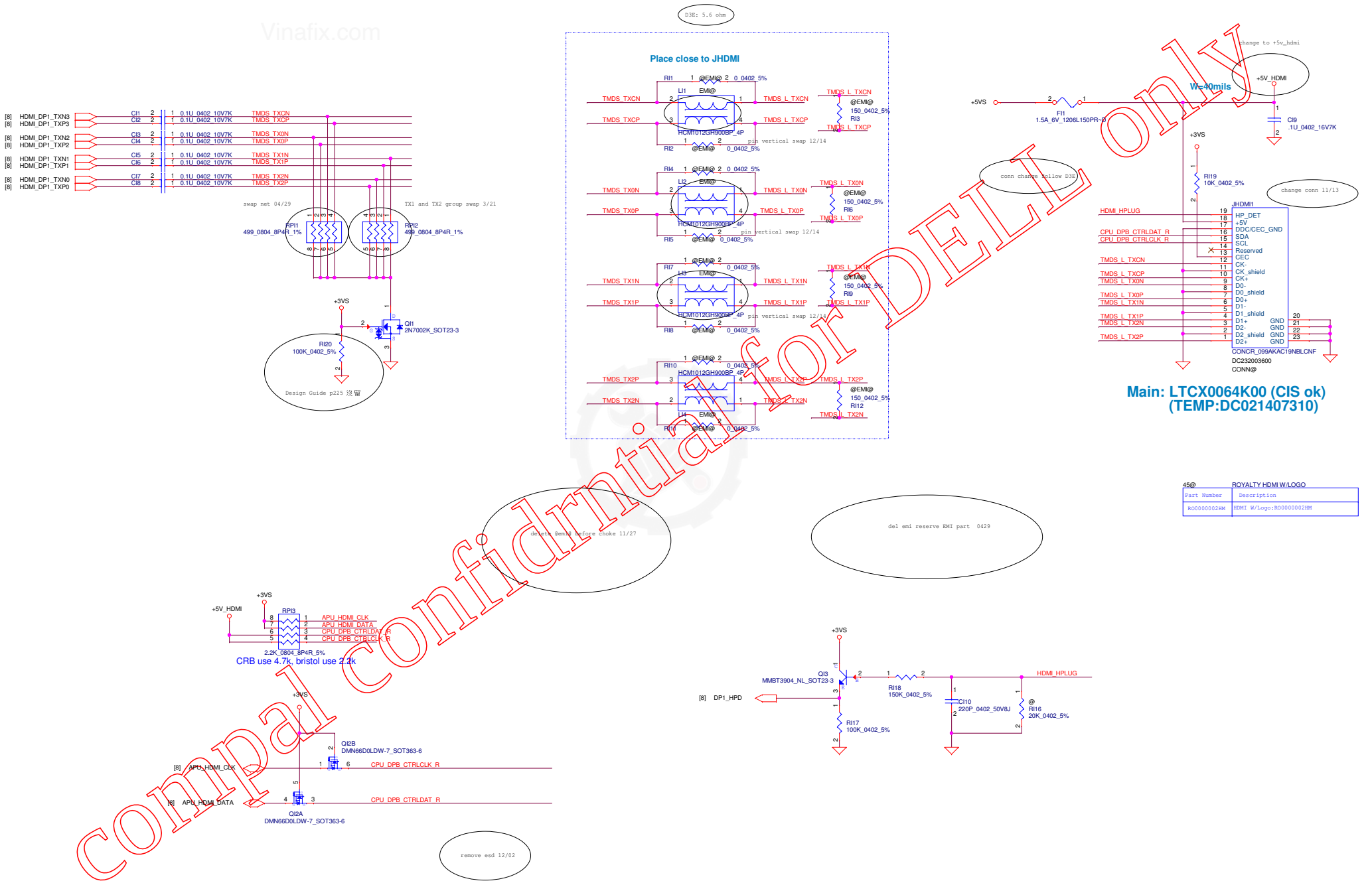






Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date	2017/01/07
Title	eDP / webcam / TouchScreen		
Size	Document Number		Rev
	BAL22 LA-D803P		A00
Date:	Tuesday, June 21, 2016	Sheet	16 of 56

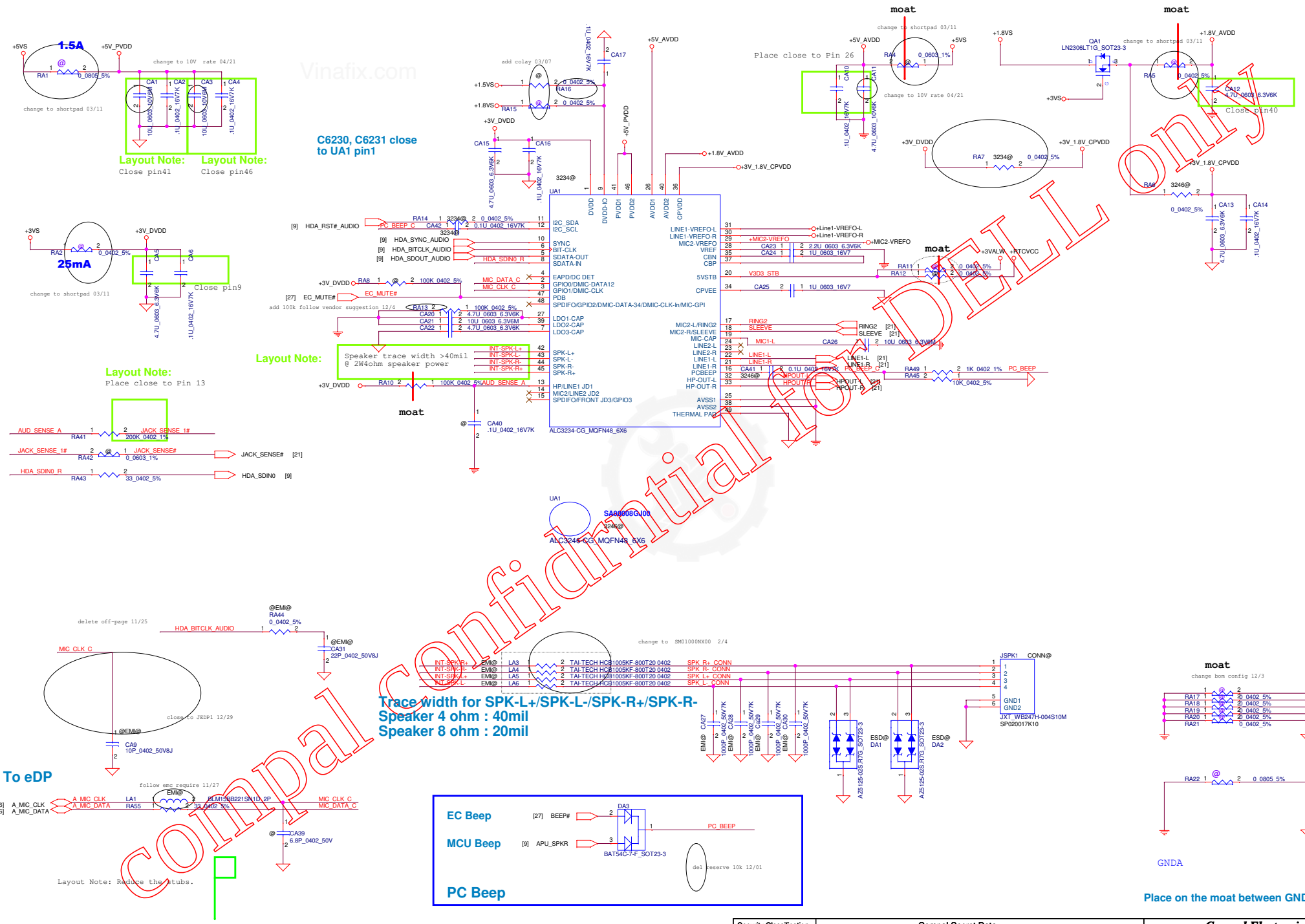
Main Func = HDMI



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.	
Title	HDMI
Size	Document Number: BAL22 LA-D803P
Rev	A00
Date: Tuesday, June 21, 2016	Sheet 17 of 56

Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: Audio Codec ALC3234			
Size	Document Number: BAL22 LA-D803P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 18 of 56		

Main Func = LAN

followe nuvision Patrick suggestion

+LAN_VDD33 rising time : >0.5ms and <100ms

OPEN

+3VALW — JP3 2MM — +LAN_VDD33

W=60mils — W=60mils

+3VALW +LAN_VDD33

CL9 1U_0402_6.3V6K

UL3 SY6288C20AAC_SOT23-5 (IN, OUT, GND, EN, OC)

[27] WOL_EN — WOL_EN

RL7 10K_0402_5%

RL6 100K_0402_5%

change to SA000079400 12/22

+LAN_VDD10

CL3 0.1U_0402_25V6 — CL4 0.1U_0402_25V6

W=60mils

followe nuvision Patrick suggestion

+LAN_VDD33 — 1.5A — CL7 47U_0603_6.3V6K — CL8 0.1U_0402_10V7K

RL5 0_0603_1% — +LAN_VDDREG — CL14 0.1U_0402_25V6

change to shortpad 03/11

Place close to UL1: Pin 32

follow nuvision Patrick suggestion

UL1 RTL8106E-CG_QFN32_4X4

CL1, CL2 close to UL1 Pin 17, 18

MDI0+ MDI0- MDI1+ MDI1- — MDIP0 MDIN0 MDIP1 MDIN1

HSOP HSON — PCIE_ARX_DTX_P0_C 0.1U_0402_10V7K — CL1 — PCIE_ARX_DTX_P0 [6]

PCIE_ARX_DTX_N0_C 0.1U_0402_10V7K — CL2 — PCIE_ARX_DTX_N0 [6]

HSIP HSIN — PCIE_ATX_C_DRX_P0 — PCIE_ATX_C_DRX_P0 [6]

PCIE_ATX_C_DRX_N0 — PCIE_ATX_C_DRX_N0 [6]

+LAN_VDD10 — +LAN_VDD33 — +LAN_VDDREG — AVDD10 AVDD10 AVDD33 DVDD33

PERSTB — PLT_RST#_R — 0_0402_5% — RL8 — PLT_RST# — PLT_RST# [9,20,27]

ISOLATEB — RL9 0_0402_5% — APU_PCIE_RST# — APU_PCIE_RST# [9,20,33]

[10] CLK_PCIE_LAN — REFCLK_P

[10] CLK_PCIE_LAN# — REFCLK_N

LANWAKEB — APU_PCIE_WAKE# — APU_PCIE_WAKE# [9,27]

[9] LAN_CLKREQ# — CLKREQB

XTLI — CKXTAL1

XTLO — CKXTAL2

GPO — 10K_0402_5% — RL1 — +LAN_VDD33

T94 T95 — LED0 LED1

2.49K_0402_1%~D — RL2 — RSET

GND

NC NC NC NC NC NC NC NC

follow nuvision Patrick suggestion

change pin 12/15

TL1 350UH_NS14-1-LF

MDI1- MDI1+ +V_DAC +V_DAC MDI0- MDI0+

RX+ RX- RCT TCT TD+ TD-

MDO1- MDO1+ MCT0 MCT1 MDO0- MDO0+

+V_DAC — CL12 0.01U_0402_16V7K

Place close to TCT pin

MCT0 — RL14 75_0603_5%

MCT1 — RL15 75_0603_5%

T-GND_L — EMI@ CL13 100P_1206_2KV8J — T-GND

follow esd require reserve 12/2

EU3501 @ESD@

MDI1- MDI1+ MDI0- MDI0+

p/n swap 12/14

JLAN1 SANTA_130460-N CONN@

PR4- PR4+ PR2- PR3- PR3+ PR2+ PR1- PR1+

MDO1- MDO1+ MDO0- MDO0+

GND GND GND GND — T-GND

+LAN_VDD33 — RL10 10K_0402_5% — APU_PCIE_WAKE#

+3VS — RL3 1K_0402_5% — ISOLATEB

RL4 15K_0402_1%

LAN_CLKREQ# — RL11 10K_0402_5%

WOL_EN — RL12 10K_0402_5%

Reserve 10K pull LAN_IO

CL10 10P_0402_50V8J — XTLI

YL1 XTAL0 GND0 XTAL1 GND1 25MHZ_10PF_7V25000014

CL11 10P_0402_50V8J — XTLO

XTAL

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

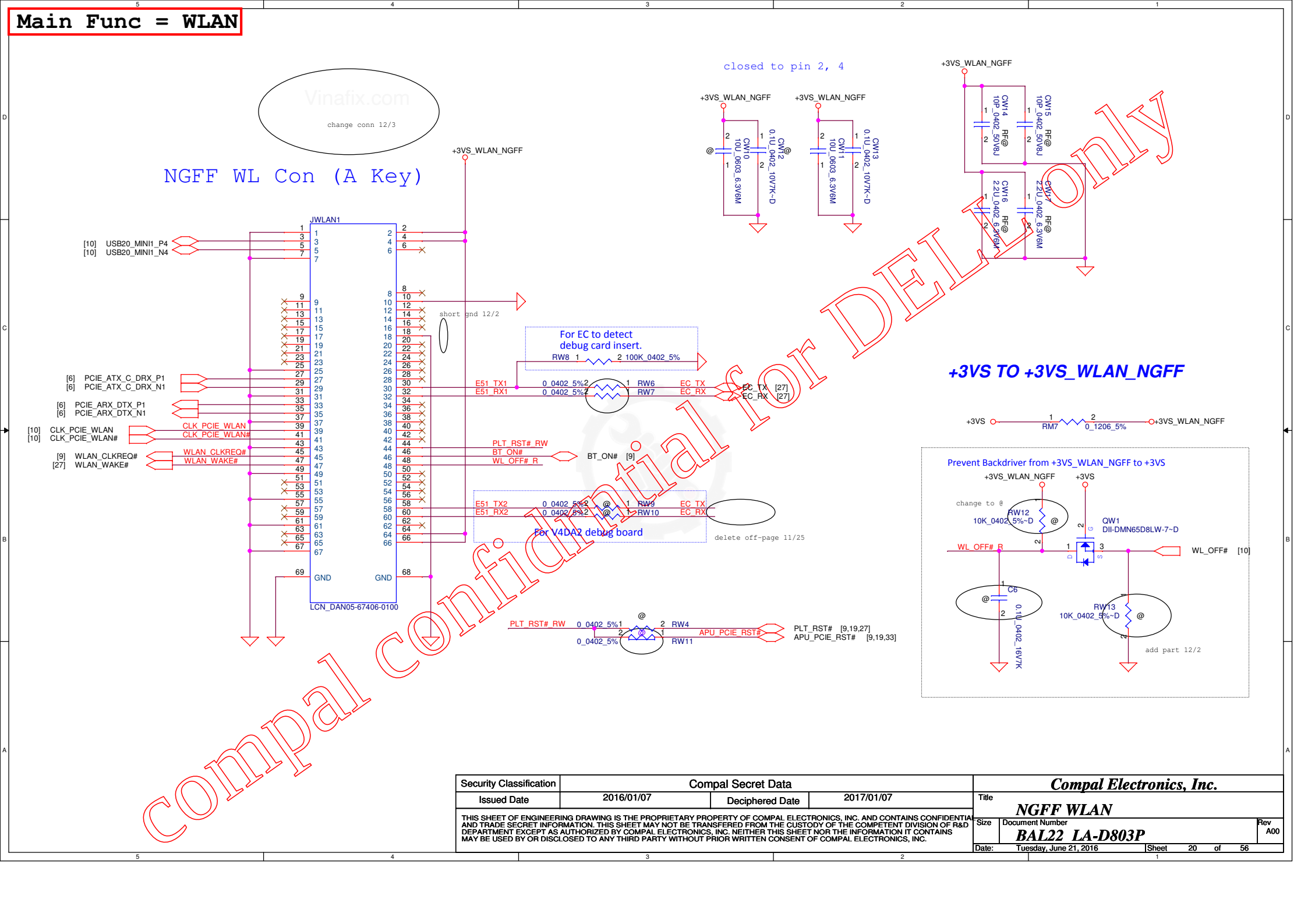
Compal Electronics, Inc.

Title: LAN RTL8106EUS

Size: Custom — Document Number: BAL22_LA-D803P — Rev: A00

Date: Tuesday, June 21, 2016 — Sheet 19 of 56

Main Func = WLAN



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

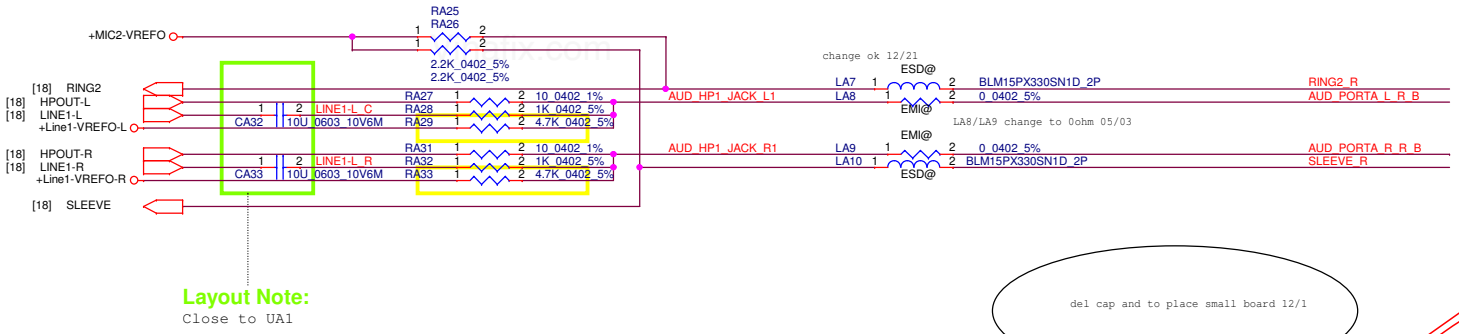
Compal Electronics, Inc.

Title: **NGFF WLAN**

Size	Document Number	Rev
	BAL22 LA-D803P	A00

Date: Tuesday, June 21, 2016 Sheet 20 of 56

Main Func = Audio Jack

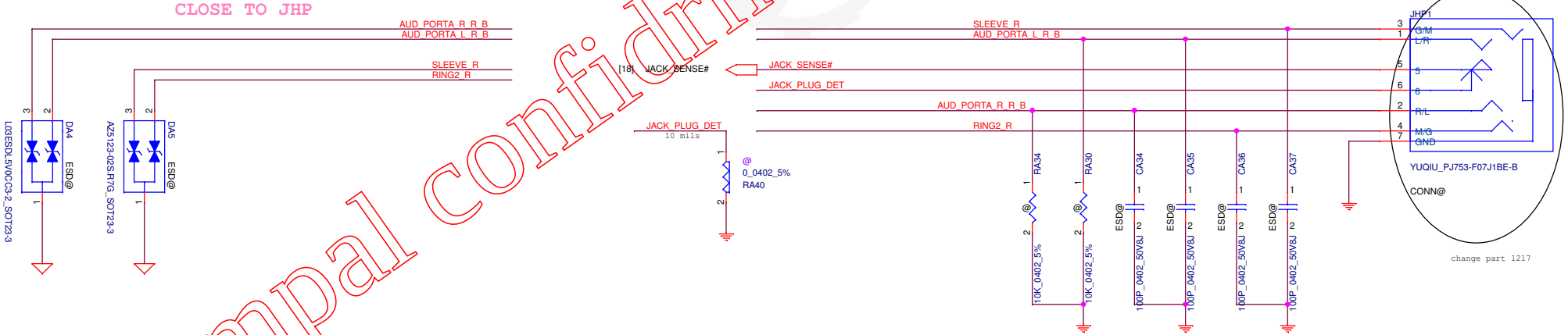


Layout Note:
Close to UA1

del cap and to place small board 12/1

Universal Jack
(Global Headset Jack + mic phone in + line in support)

CLOSE TO JHP



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

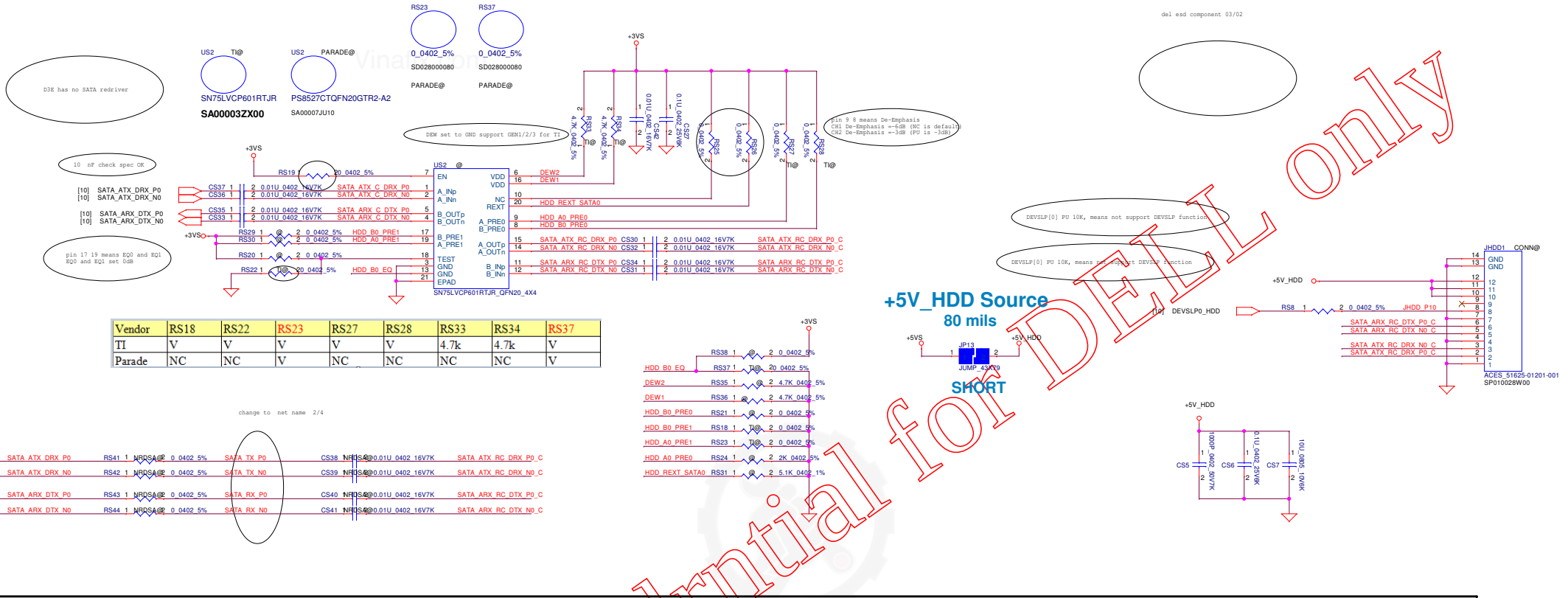
Compal Electronics, Inc.

Title: **JACK**

Size | Document Number | Rev A00

Date: Tuesday, June 21, 2016 | Sheet 21 of 56

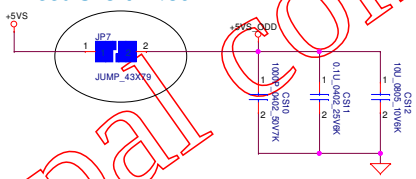
Main Func = HDD



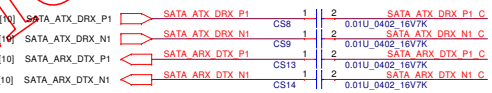
Vendor	RS18	RS22	RS23	RS27	RS28	RS33	RS34	RS37
TI	V	V	V	V	V	4.7k	4.7k	V
Parade	NC	NC	V	NC	NC	NC	NC	V

ODD Power Control

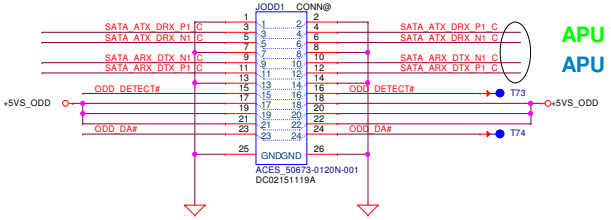
60 mils
need short 11/30



SOC TX
SOC RX



SATA ODD Connector (FFC Type)



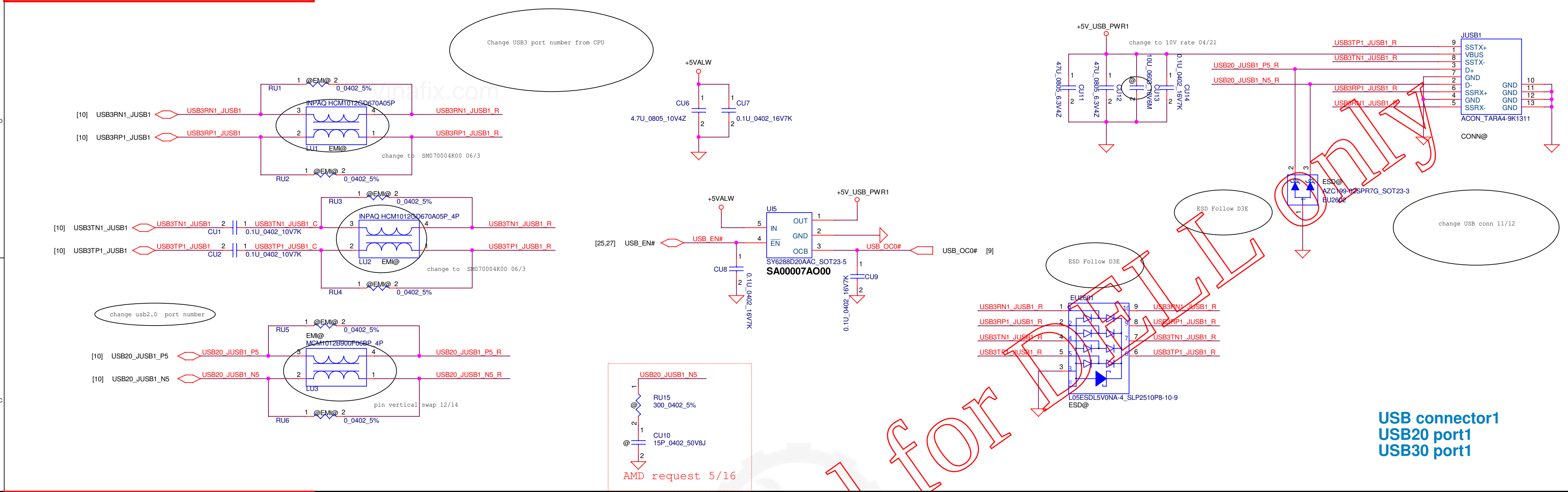
APU TX
APU RX

change conn 11/30

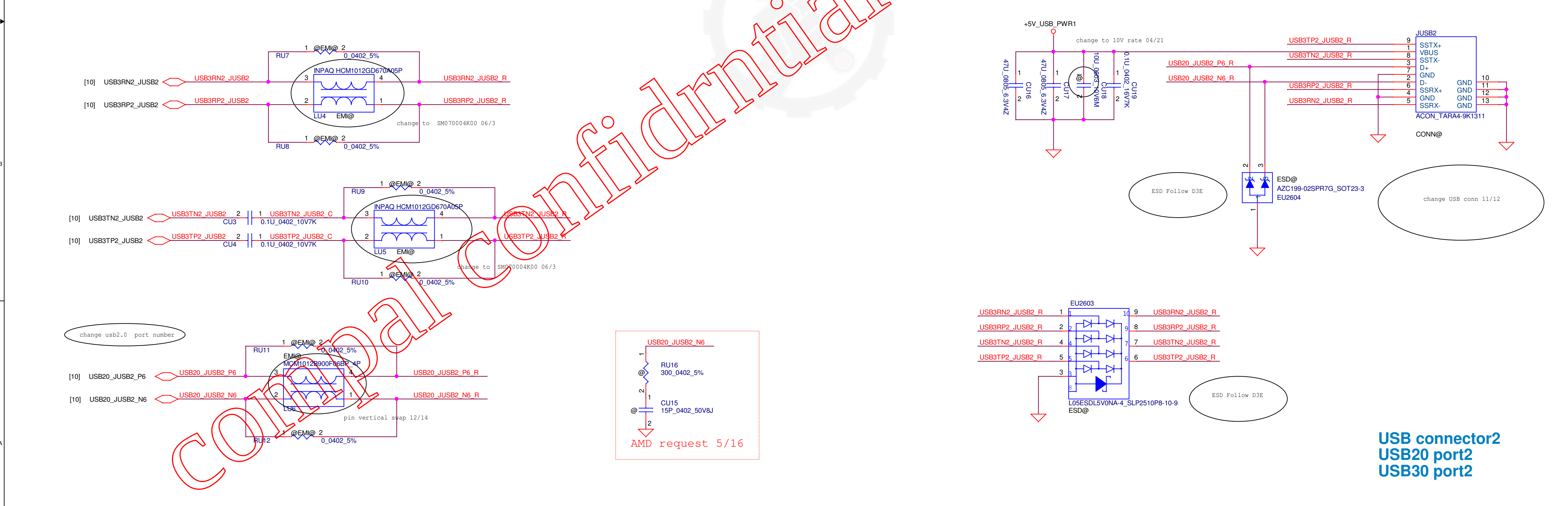
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: HDD			
Size	Document Number: BAL22 LA-D803P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 22 of 56		

Main Func = USB3.0 Port1



Main Func = USB3.0 Port2



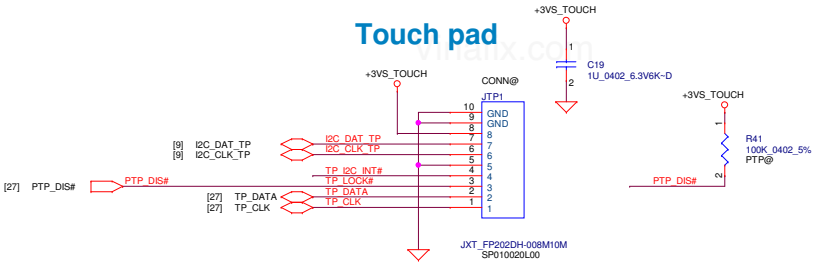
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date 2017/01/07	Title: USB3.0

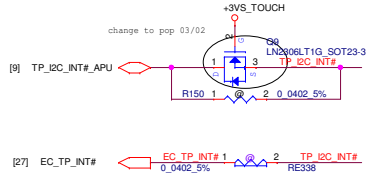
Size | Document Number: BAL22 LA-D803P | Rev A00

Date: Tuesday, June 21, 2016 | Sheet 23 of 56

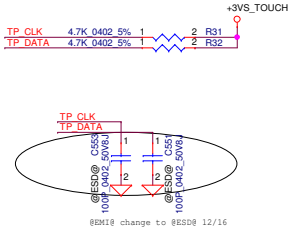
Main Func = Touch Pad

Touch pad

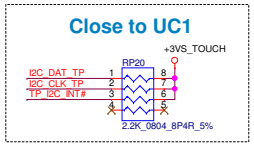


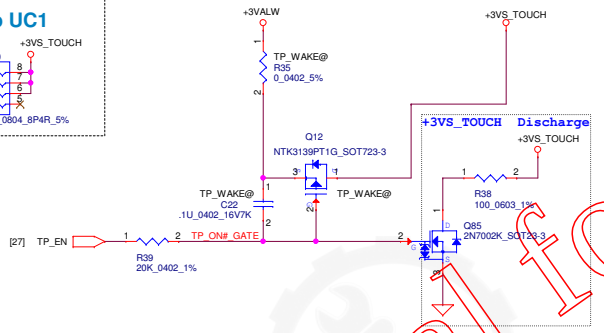


Close to UE1

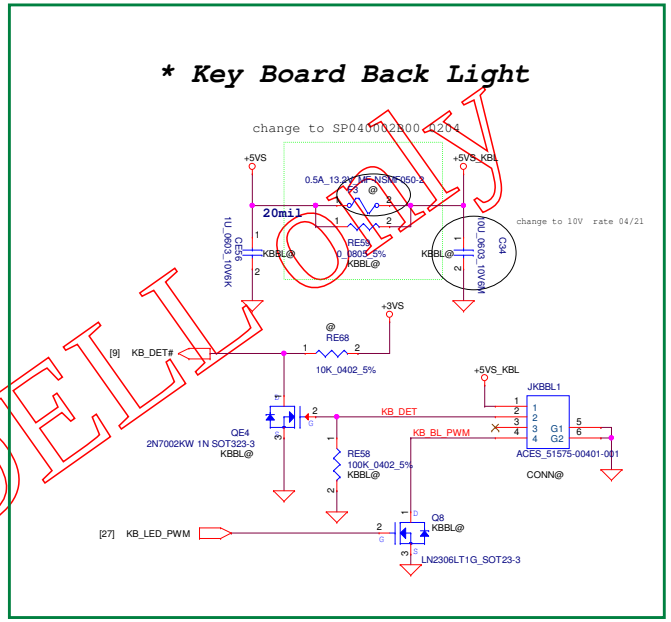


Close to UC1

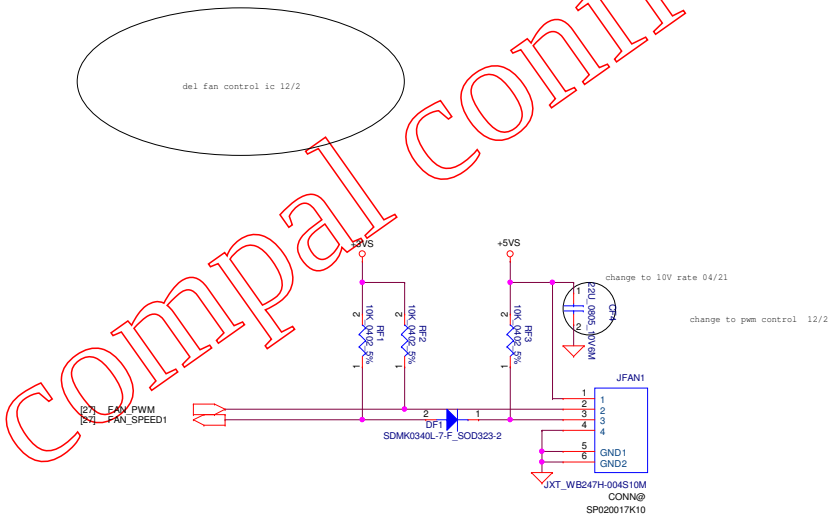


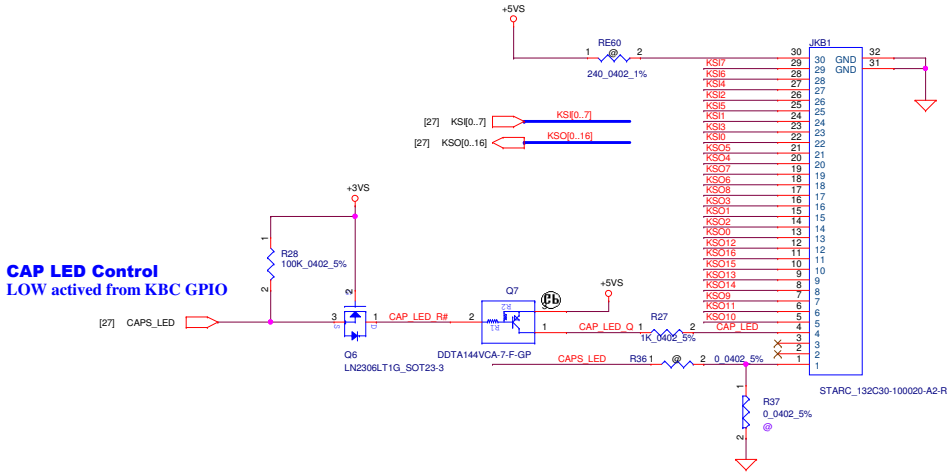


* Key Board Back Light



Main Func = FAN Control





Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

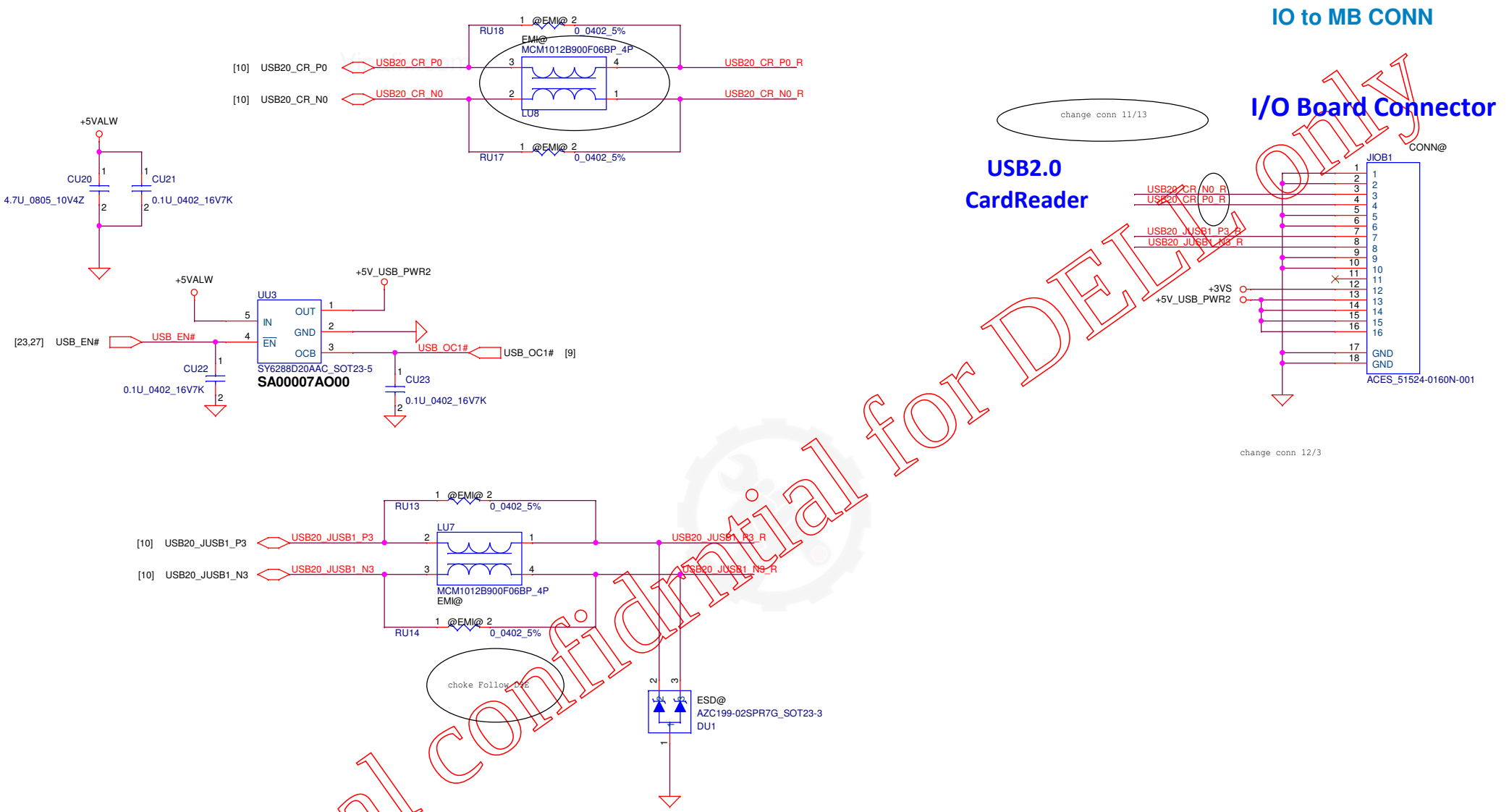
Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size | Document Number: BAL22 LA-D803P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 24 of 56

Main Func = IO Connector



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Title	IO-DB		
Size B	Document Number BAL22 LA-D803P		Rev A00
Date: Tuesday, June 21, 2016	Sheet 25 of 56		

Main Func = DC Interface

+5VS and +3VS switch

SHORT

Max:7.0A

10mil

U2301 EM5209VF DFN 14P DUAL LOAD SW

SA00007PM00

+3VS to +3VGS
+1.8V_ALW to +1.8VS

2000mA

20mil(0.5A)

U15 EM5209VF DFN 14P DUAL LOAD SW

SA00007PM00

Max:5.07A

10mil

U2302 EM5209VF DFN 14P DUAL LOAD SW

SA00007PM00

SHORT

1500mA

U74 SY6288C20AAC_SOT23-5

U4 AO4354_SO8

Q84 2N7002K_SOT23-3

Q83 @ 2N7002K_SOT23-3

U2A LM393DR_SO8

U2B LM393DR_SO8

Q2516B DMN66D0LDW-7_SOT363-6

Q2516A DMN66D0LDW-7_SOT363-6

Q135 AO3416L_SOT23-3

Q2513 AO3416L_SOT23-3

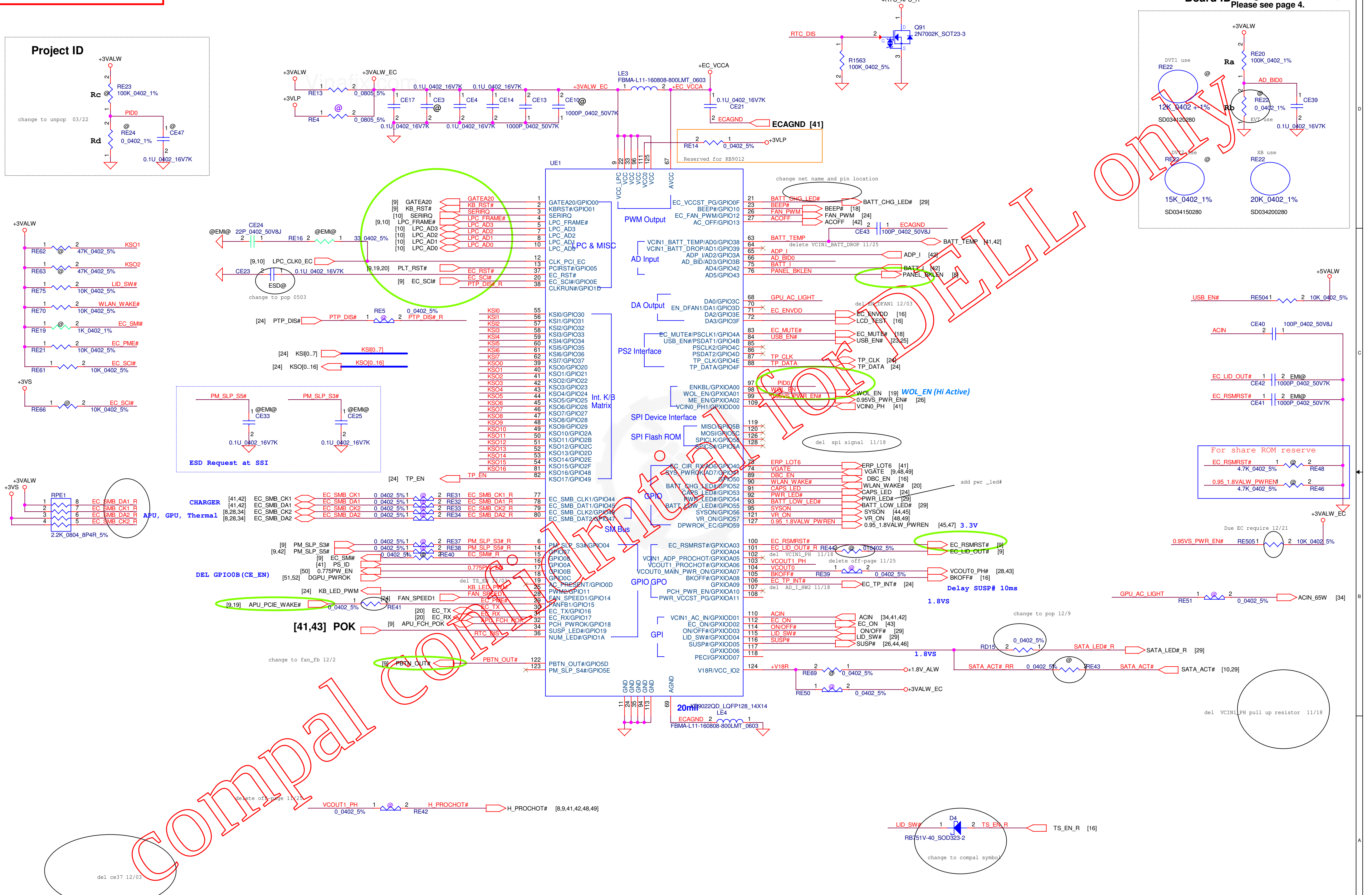
Q2515 AO3416L_SOT23-3

Q2514 AO3416L_SOT23-3

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: BAL22 LA-D803P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 26 of 56		

Main Func = KBC



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

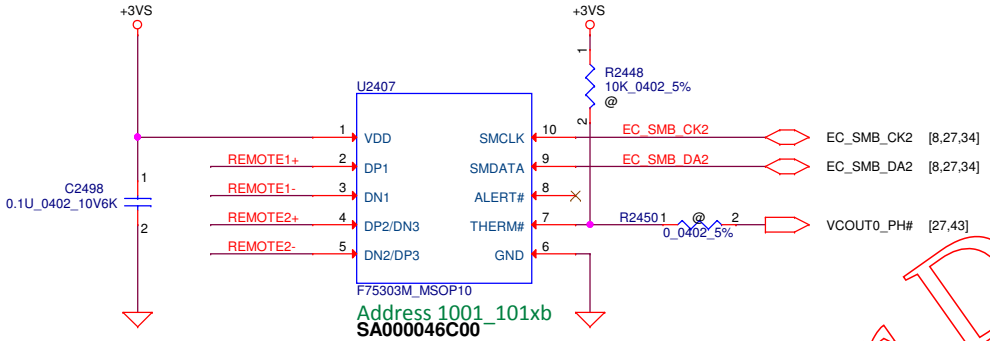
Title: **EC ENE-KB9012A4/KB9022QC**

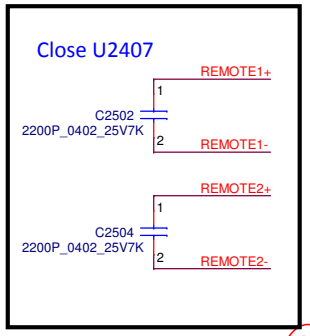
Size | Document Number: **BAL22 LA-D803P** | Rev A00

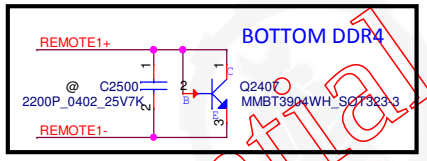
Date: Tuesday, June 21, 2016 | Sheet 27 of 56

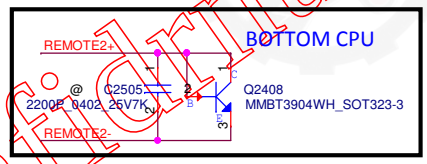
Main Func = Thermal Sensor

Fintek thermal sensor placed near by TOP DDR4







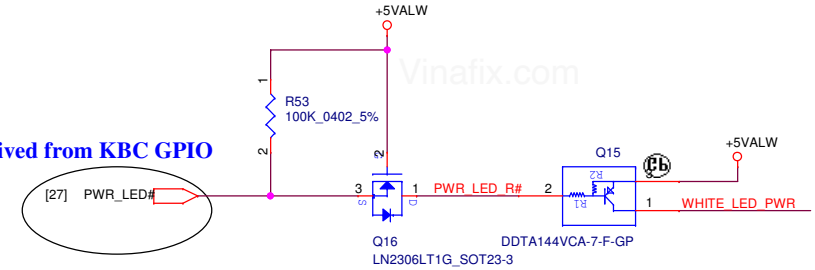


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

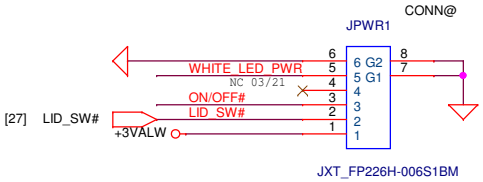
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

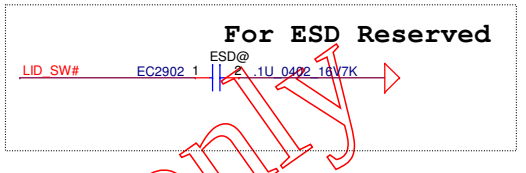
Compal Electronics, Inc.			
Title: Thermal Sensor			
Size	Document Number: BAL22 LA-D803P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 28 of 56		

Main Func = POWER BTN



Power button

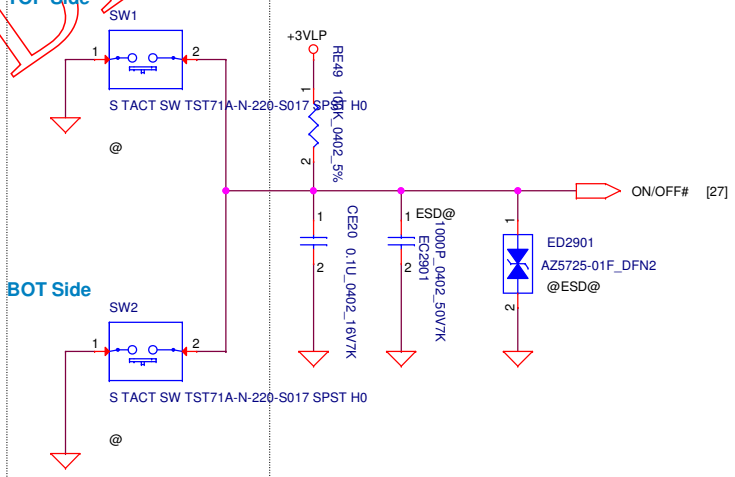




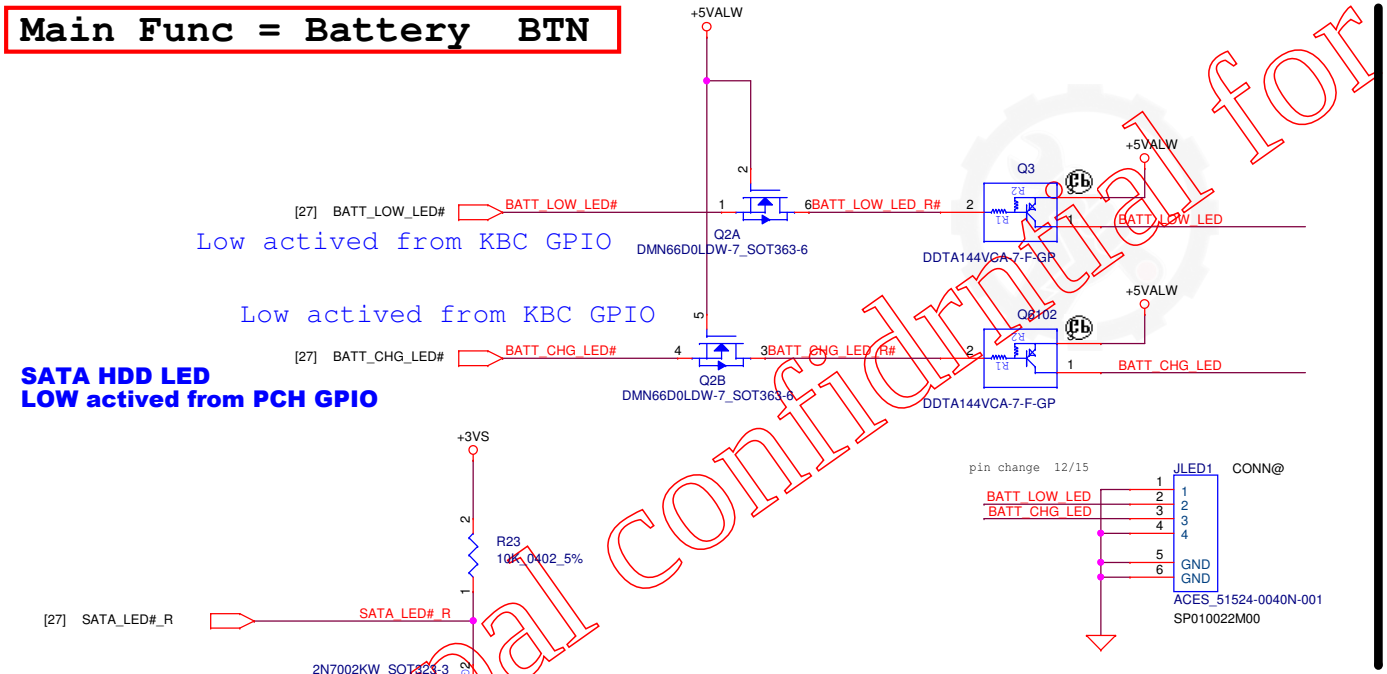
Pop only before MP

ON/OFF switch

TOP Side



Main Func = Battery BTN



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: LED/PWR-DB			
Size	Document Number: BAL22 LA-D803P		Rev: A00
Date: Tuesday, June 21, 2016	Sheet 29 of 56		

Main Func = Screw Hole

ZZZ

Part Number	Description
DAZ1PK00100	PCB BAL22 LA-D803P LS-D802P/D803P/D806P/D807P/D809P

PCB_R1@

GCE

ZZZ1

Part Number	Description
DAZ1PK00101	PCB BAL22 LA-D803P LS-D802P-3P/D806P/D807P/D809P GOLD A31 !

PCB_R3G@

TRiPOD

ZZZ2

Part Number	Description
DAZ1PK00102	PCB BAL22 LA-D803P LS-D802P-3P/D806P-7P/D809P TRIPOD A31 !

PCB_R3T@

HANNSTAR

ZZZ3

Part Number	Description
DAZ1PK00103	PCB BAL22 LA-D803P LS-D802P-3P/D806P-7P/9P HANNSTARB A31 !

PCB_R3H@

enlarge hole 04/23

H1 HOLEA H_3P0
H2 HOLEA H_3P0
H3 HOLEA H_3P0
H4 HOLEA H_3P0
H5 HOLEA H_3P0
H6 HOLEA H_5P6N
H7 HOLEA H_3P0N
H8 HOLEA H_3P5
H9 HOLEA H_3P5
H10 HOLEA H_3P5
H11 HOLEA H_3P2
H12 HOLEA H_3P2X2P6
H13 HOLEA H_6P0

HCPU1 HOLEA H_3P7X4P3
HCPU2 HOLEA H_3P9
HCPU3 HOLEA H_3P7
HCPU4 HOLEA H_3P7X4P3

follow EMI require 12/15

@ CLIP1 1 1 EMIST_SQ-55G_1P
@ CLIP2 1 1 EMIST_SQ-55G_1P

Follow EMC require add cap around +19VB 11/25

need to place separately

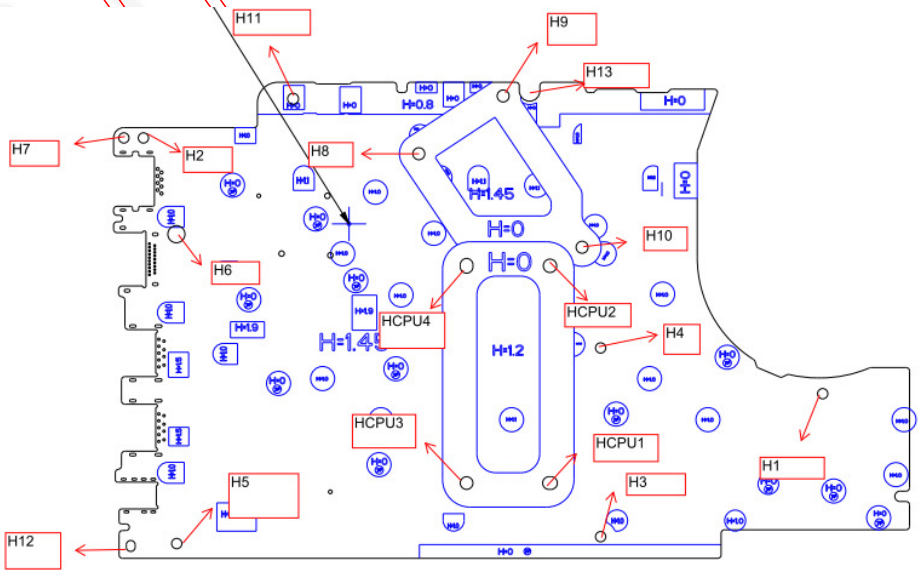
change to 25V rate 04/21

+19VB

@EMI@ C35 0.1U_0402_25V6
@EMI@ C36 0.1U_0402_25V6
@EMI@ C37 0.1U_0402_25V6
@EMI@ C38 0.1U_0402_25V6
@EMI@ C39 0.1U_0402_25V6
@EMI@ C40 0.1U_0402_25V6
@EMI@ C41 1000P_0402_50V7K
@EMI@ C42 1000P_0402_50V7K
@EMI@ C43 1000P_0402_50V7K
@EMI@ C44 1000P_0402_50V7K
@EMI@ C45 1000P_0402_50V7K
@EMI@ C47 1000P_0402_50V7K
@EMI@ C48 1000P_0402_50V7K
@EMI@ C49 1000P_0402_50V7K

FD1 @FIDUCIAL
FD2 @FIDUCIAL
FD3 @FIDUCIAL
FD4 @FIDUCIAL

del FD5 FD6 12/1



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date 2017/01/07	Title: Screw Hole
			Size: Document Number: BAL22 LA-D803P Rev: A00
			Date: Tuesday, June 21, 2016 Sheet 30 of 56

SSID1 = TPM2.0

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2017/01/07

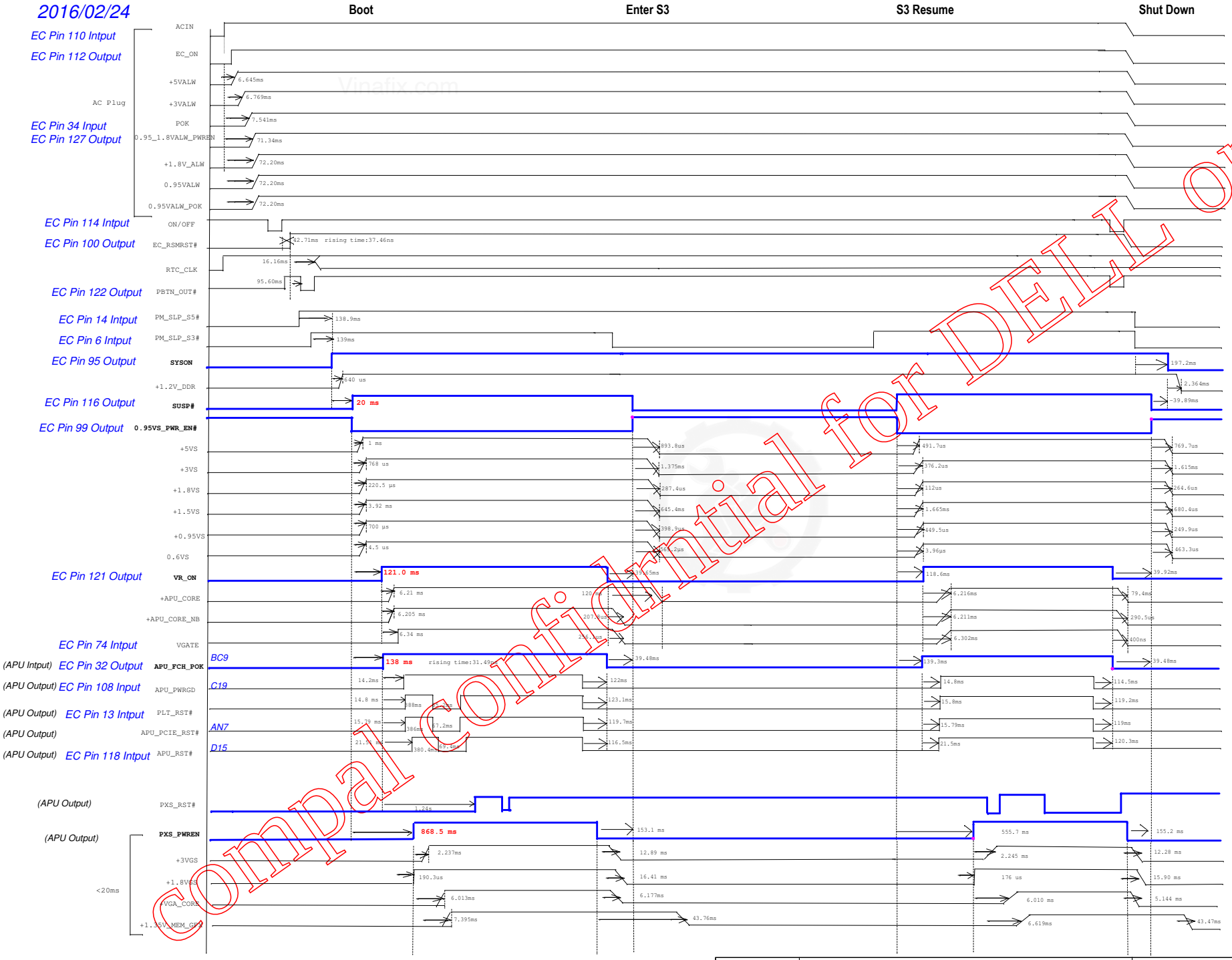
Compal Electronics, Inc.

Title: ***TPM***

Size: Custom | Document Number: ***BAL22 LA-D803P*** | Rev: A00

Date: | Sheet 31 of 56

2016/02/24



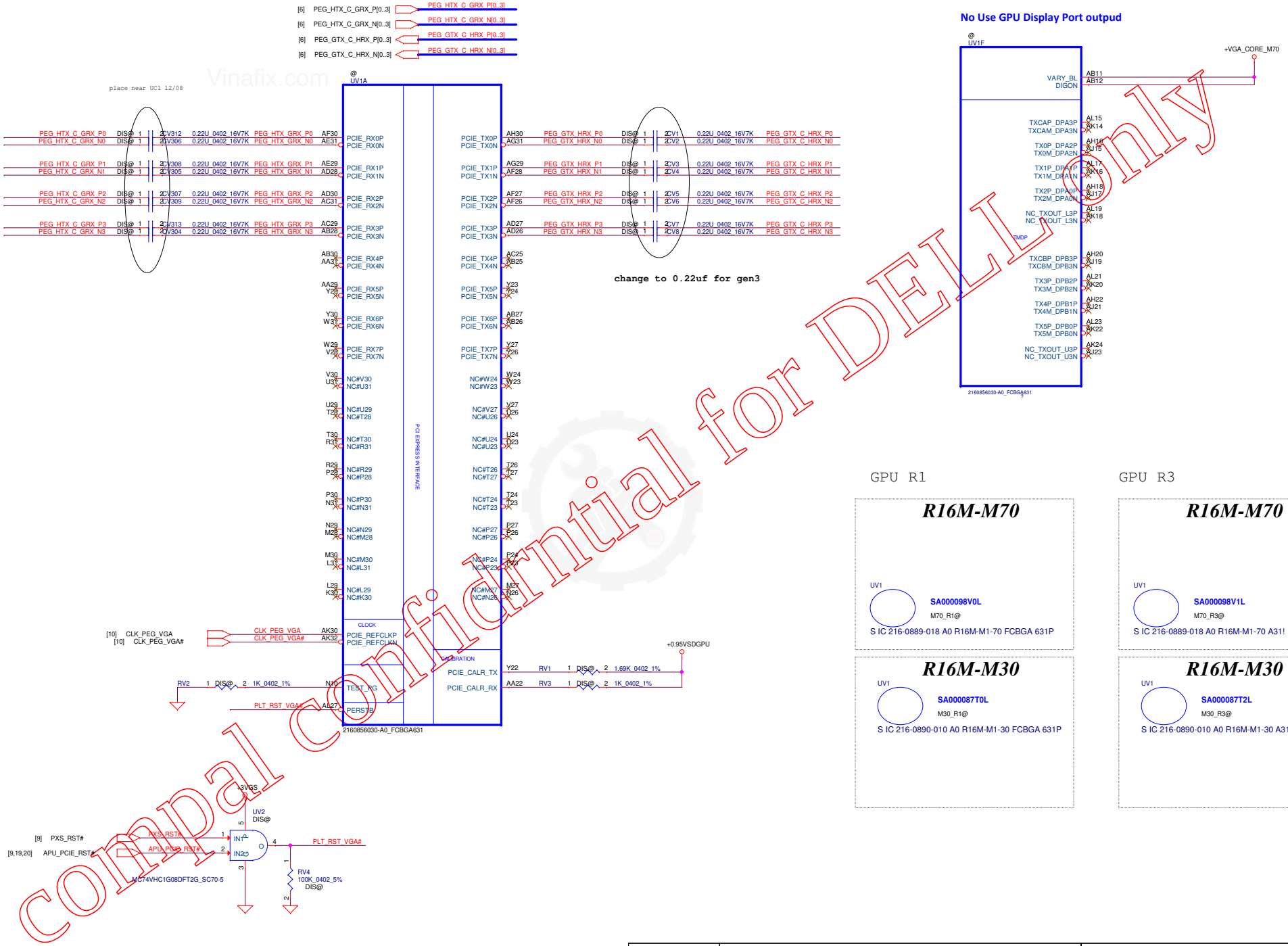
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: S5_MUX_CTRL

Size: | Document Number: BAL22 LA-D803P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 32 of 56



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: **M30/M70_PCIE/DP**

Size: Custom | Document Number: **BAL22_LA-D803P** | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 33 of 56

del thermal sensor 11/19

change to 4.7K 11/23

Reduce 3.3V TO 1.8V level shift for EXO.
BOM contorl in POWER sheet

reserve level shift colay resistor 11/20

3.3V TO 1.8V LEVEL SHIF
For JET/SUN to support SVI2 reaulator
DNI for TOPAZ

ADD GPU POWER SAVING MODE 11/26

REMOVE THERMAL SENSOR SIGNAL 11/24

13mA

Enable MLPS

TOPAZ Thermal Address—>0x82

Enable --> Low
Disable --> High

Peak Current Control (PCC) CKT
Reversed

change bom structure to dis@ 11/24

change to support gen3 11/24

VRAM Type
Need reference
X76 Schematic

Resistor Divider Lookup Lable

0402 1% resistors are equired

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

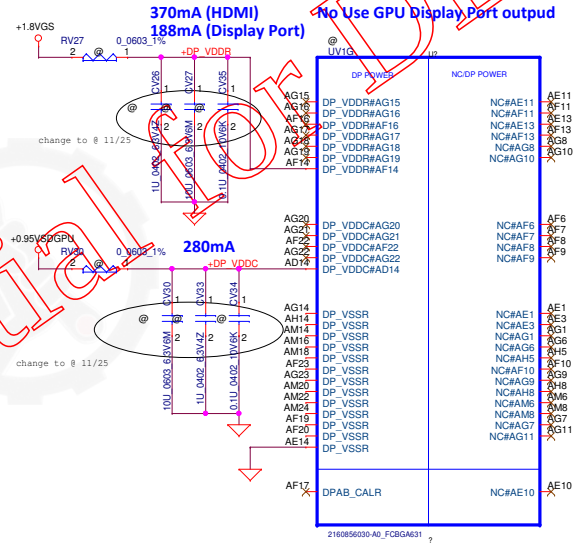
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: M30/M70_MSIC

Size: Custom | Document Number: BAL22_LA-D803P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 34 of 56



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: **M30/M70_Power/GND**

Size: Custom | Document Number: **BAL22_LA-D803P** | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 35 of 56

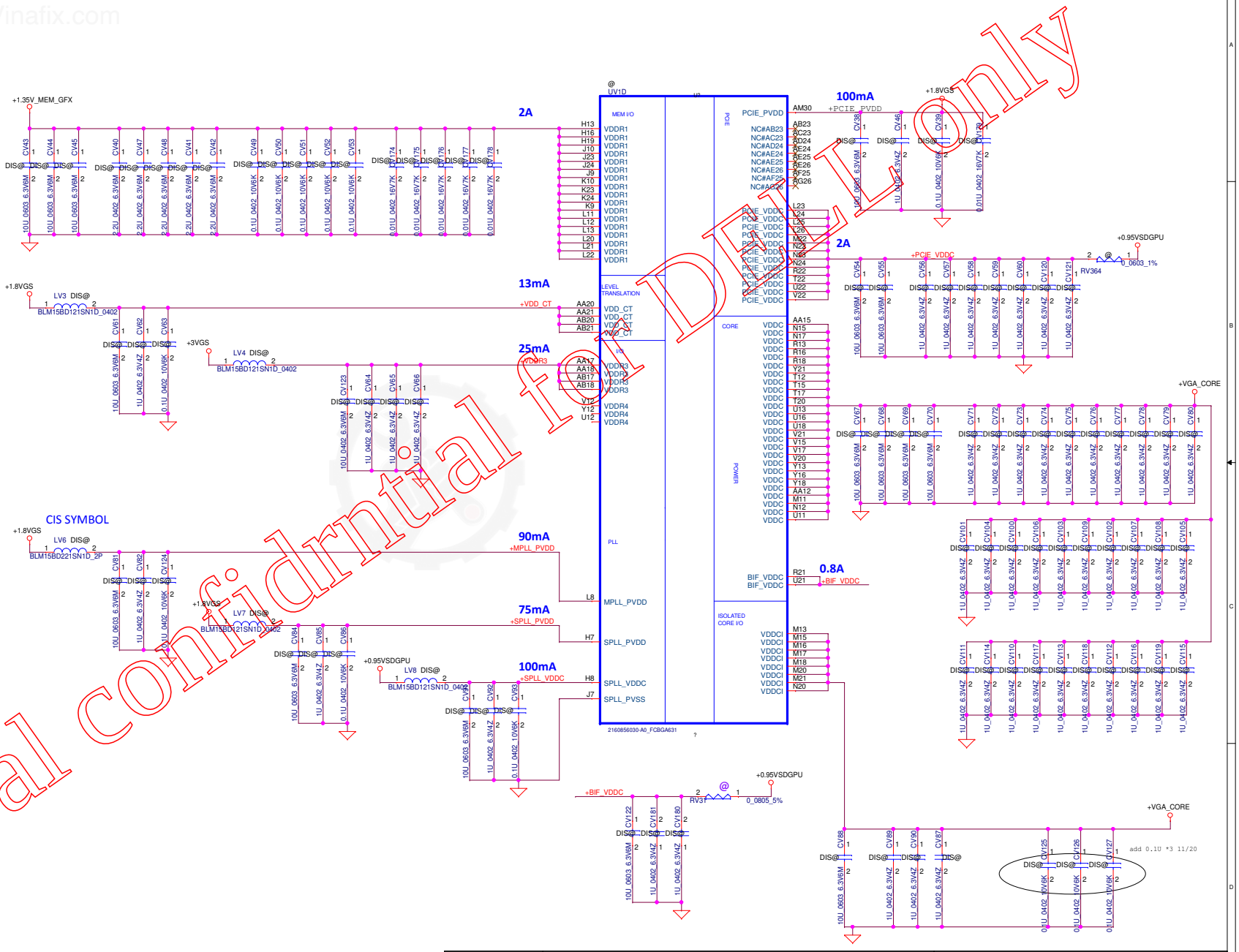
+VGA_CORE		10uF	1uF	0.1uF
VDDC		4	30	0
VDDC and VDDCI TDC 28A				
VDDCI		1	3	3

+0.95VSDGPU		10uF	1uF	0.1uF
PCIE_VDDC	2A	2	7	0
BIF_VDDC	0.8A	1	2	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	2A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF	0.01uF
PCIE_PVDD	100mA	1	1	1	1
MPLL_PVDD	90mA	1	1	1	0
SPLL_PVDD	75mA	1	1	1	0
VDD_CT	13mA	1	1	1	0
+DP_VDDR	40mA	1(@)	1(@)	1(@)	0
+DP_VDDC		1(@)	1(@)	1(@)	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	1	3	0



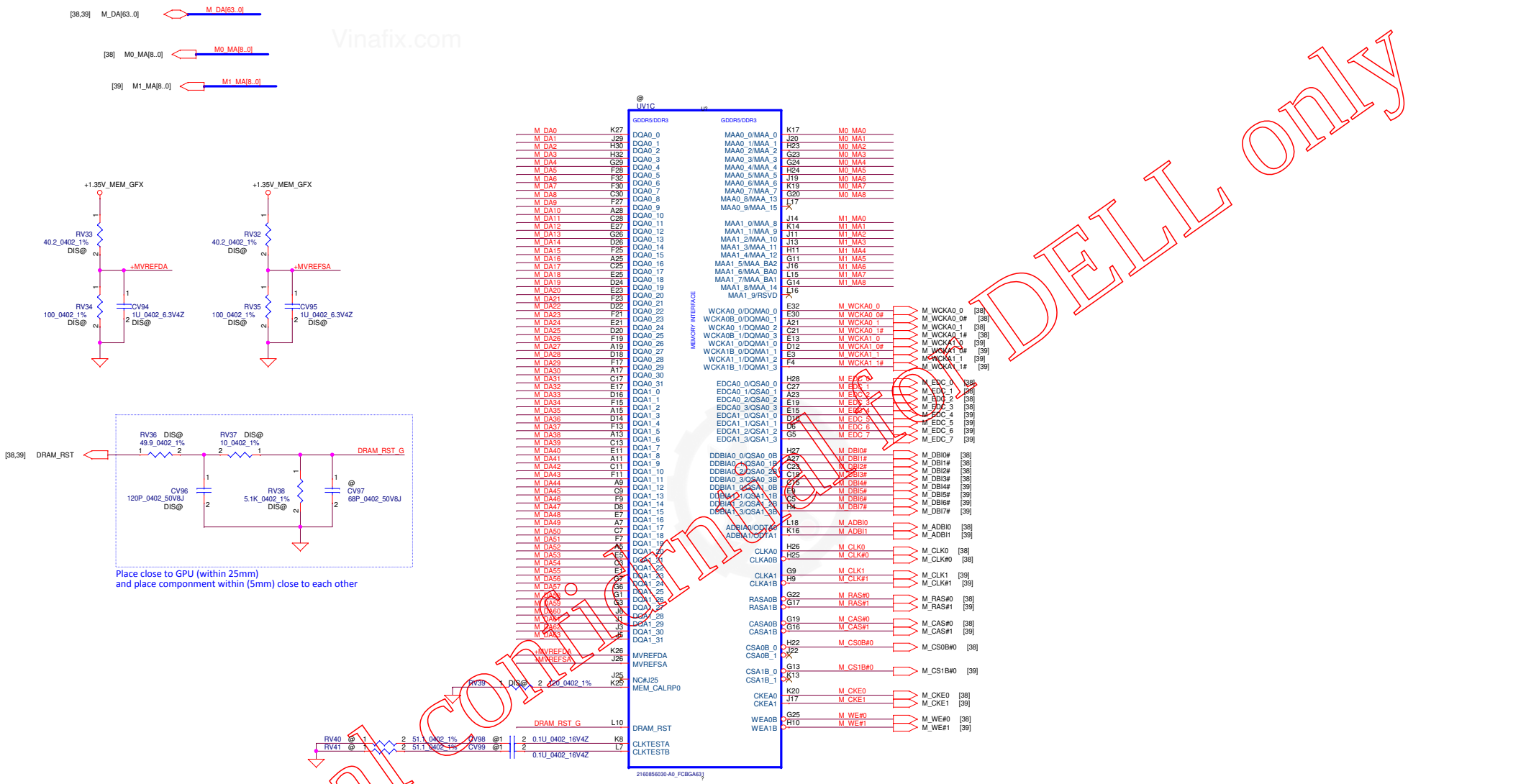
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: M30/M70_Power

Size: Custom | Document Number: BAL22_LA-D803P | Rev: A00

Date: Tuesday, June 21, 2016 | Sheet 36 of 56



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	M30/M70_MEM		
Size: Custom	Document Number: BAL22_LA-D803P		Rev: A00
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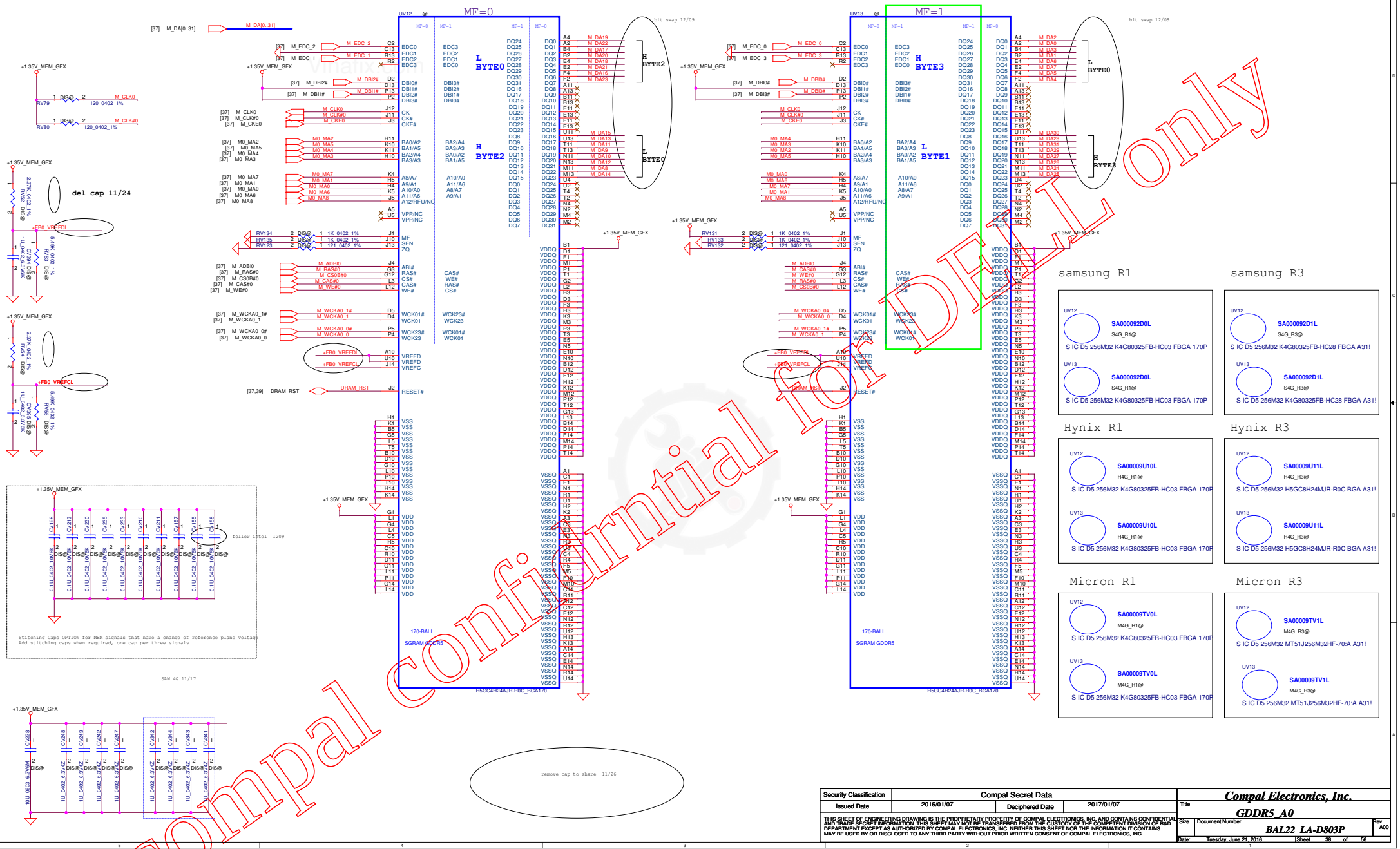
clamshell configuration 11/26



samsung R1

UV12 SA000092D0L S4G_R1@
S IC D5 256M32 K4G80325FB-HC03 FBGA 170P

UV13 SA000092D0L S4G_R1@
S IC D5 256M32 K4G80325FB-HC03 FBGA 170P

samsung R3

UV12 SA000092D1L S4G_R3@
S IC D5 256M32 K4G80325FB-HC28 FBGA A31!

UV13 SA000092D1L S4G_R3@
S IC D5 256M32 K4G80325FB-HC28 FBGA A31!

Hynix R1

UV12 SA00009U10L H4G_R1@
S IC D5 256M32 K4G80325FB-HC03 FBGA 170P

UV13 SA00009U10L H4G_R1@
S IC D5 256M32 K4G80325FB-HC03 FBGA 170P

Hynix R3

UV12 SA00009U11L H4G_R3@
S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!

UV13 SA00009U11L H4G_R3@
S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!

Micron R1

UV12 SA00009TV0L M4G_R1@
S IC D5 256M32 K4G80325FB-HC03 FBGA 170P

UV13 SA00009TV0L M4G_R1@
S IC D5 256M32 K4G80325FB-HC03 FBGA 170P

Micron R3

UV12 SA00009TV1L M4G_R3@
S IC D5 256M32 MT51J256M32HF-70:A A31!

UV13 SA00009TV1L M4G_R3@
S IC D5 256M32 MT51J256M32HF-70:A A31!

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	GDDR5_A0		
Size	Document Number	BAL22_LA-D803P	Rev A00
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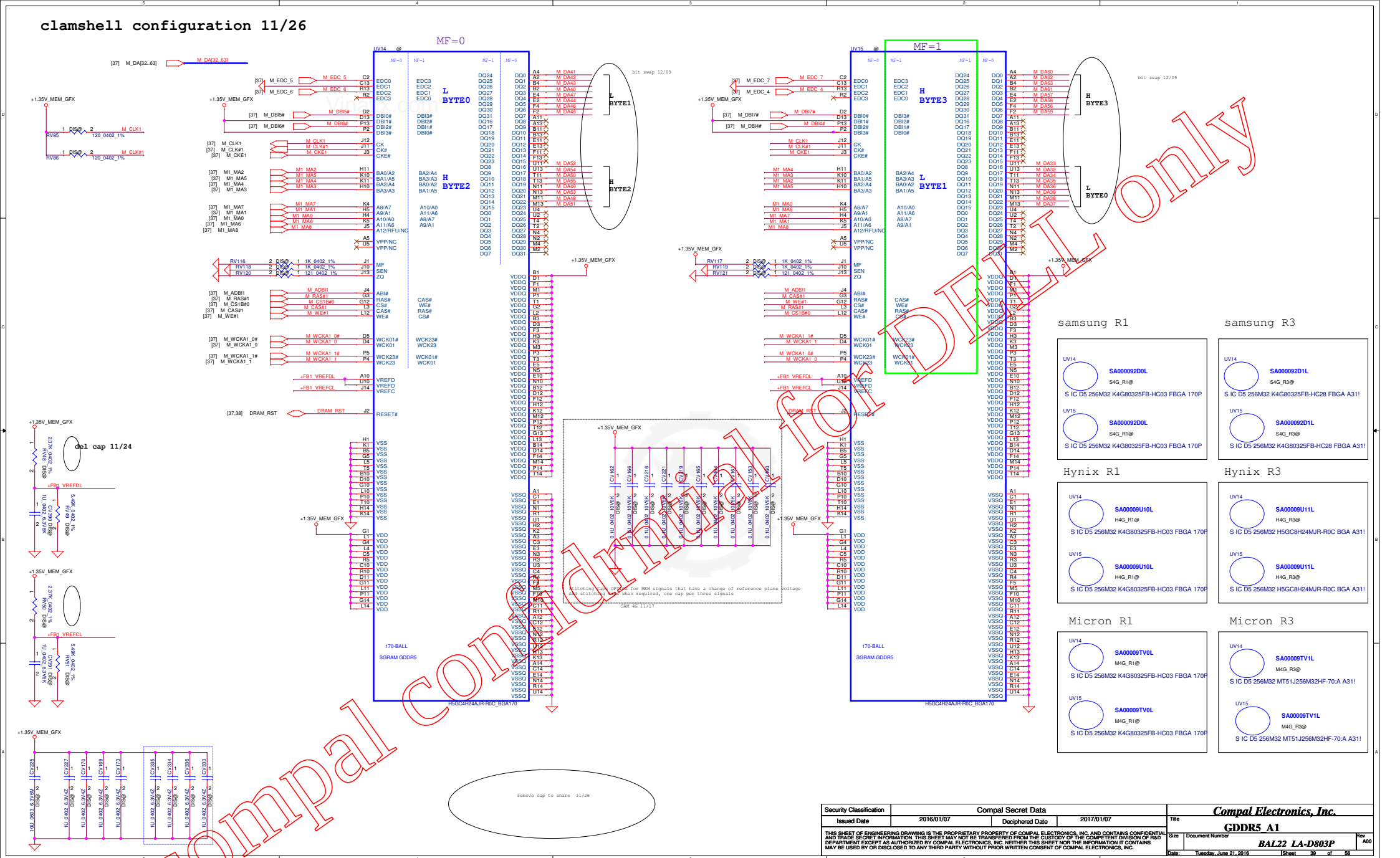
clamshell configuration 11/26



samsung R1

samsung R3

Hynix R1

Hynix R3

Micron R1

Micron R3

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	GDDR5_A1		
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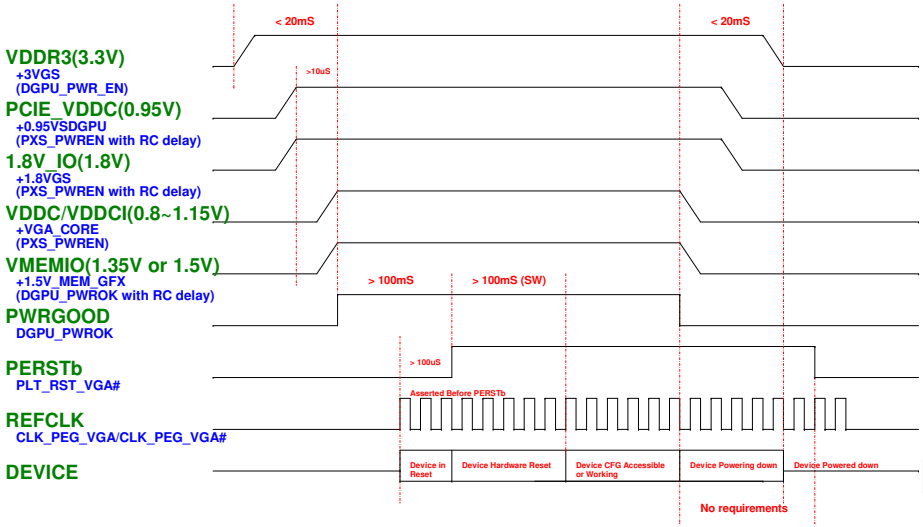
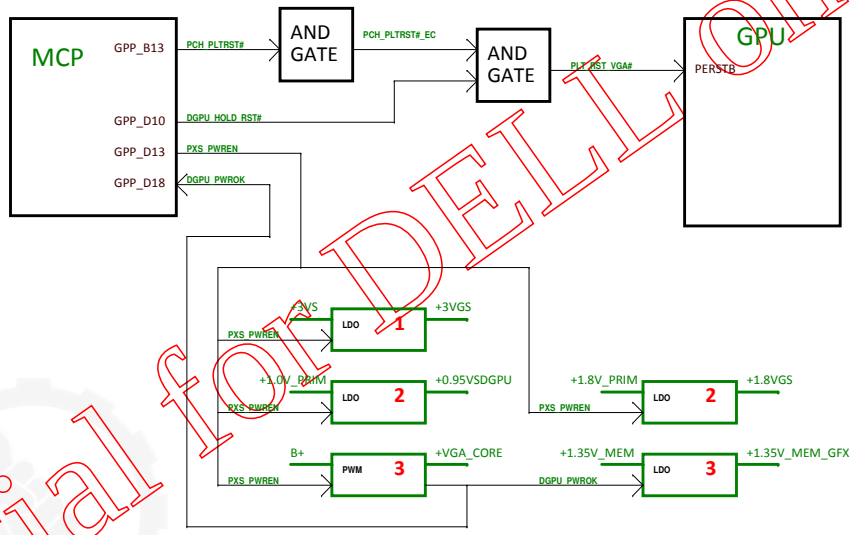
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µs).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.





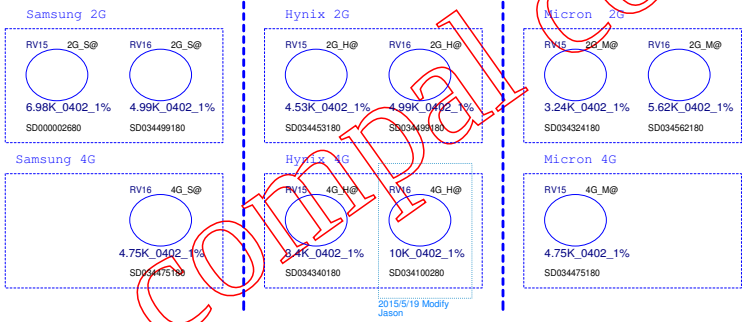


Table 3–21 Resistor Divider Lookup T

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R16M-M30/M70 VRAM Only

Memory ID	R3 P/N	Vendor	Configuration	Size
100	SA00009U10L	Hynix	H5GC8H24MJR-R0C	2GB
011	SA000092D0L	SAMSUNG	K4G80325FB-HC28	2GB
101	SA00009TV0L	Micron	MT51J256M32HF-70:A	2GB

Memory ID	R3 P/N	Vendor	Configuration	Size
110	SA00009U10L	Hynix	H5GC8H24MJR-R0C	4GB
000	SA000092D0L	SAMSUNG	K4G80325FB-HC28	4GB
111	SA00009TV0L	Micron	MT51J256M32HF-70:A	4GB

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: M30/M70_NOTE

Size | Document Number: BAL22 LA-D803P | Rev: A00

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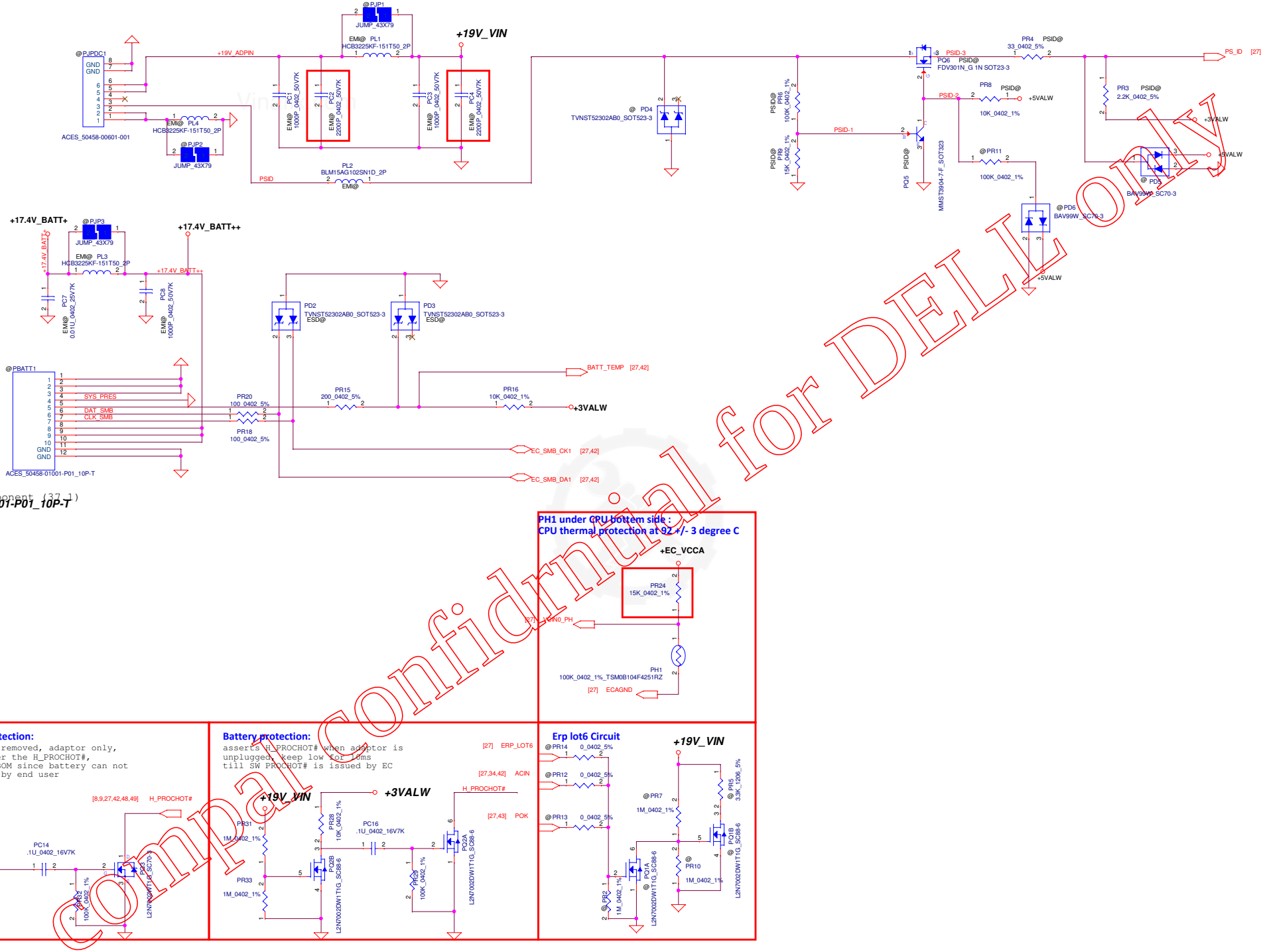

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Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev A00
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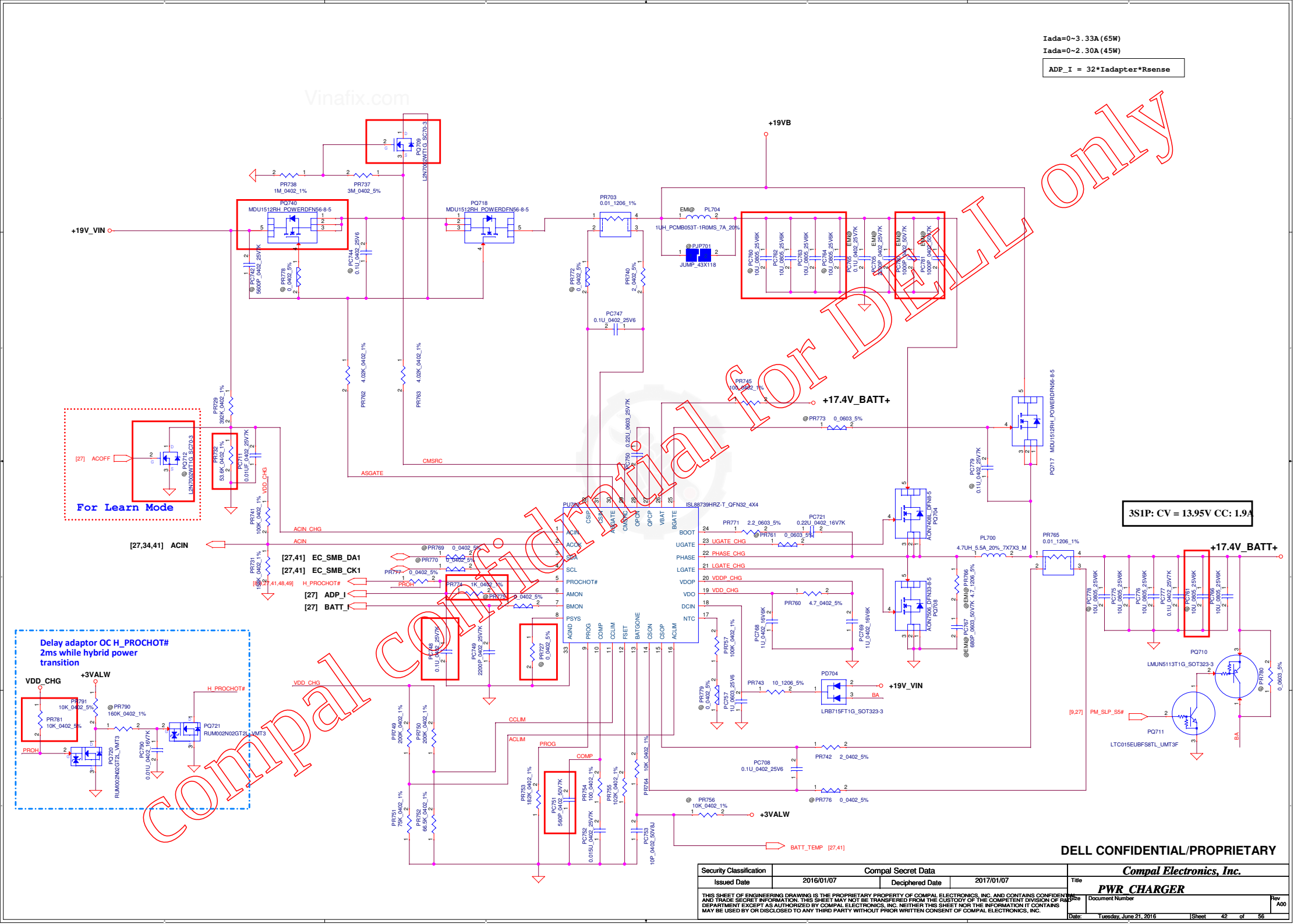
Iada=0~3.33A(65W)
Iada=0~2.30A(45W)
ADP_I = 32*Iadapter*Rsense
+19VB
+19V_VIN
+17.4V_BATT+
+3VALW
ISL88739HRZ-T_QFN32_4X4
For Learn Mode
Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition
3S1P: CV = 13.95V CC: 1.9A
[27,34,41] ACIN
[27,41] EC_SMB_DA1
[27,41] EC_SMB_CK1
[27] ADP_I
[27] BATT_I
[27] ACOFF
[9,27] PM_SLP_S5#
BATT_TEMP [27,41]
Vinafix.com
Compal confidential for DELL only
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_CHARGER
Security Classification: Compal Secret Data
Issued Date: 2016/01/07
Deciphered Date: 2017/01/07
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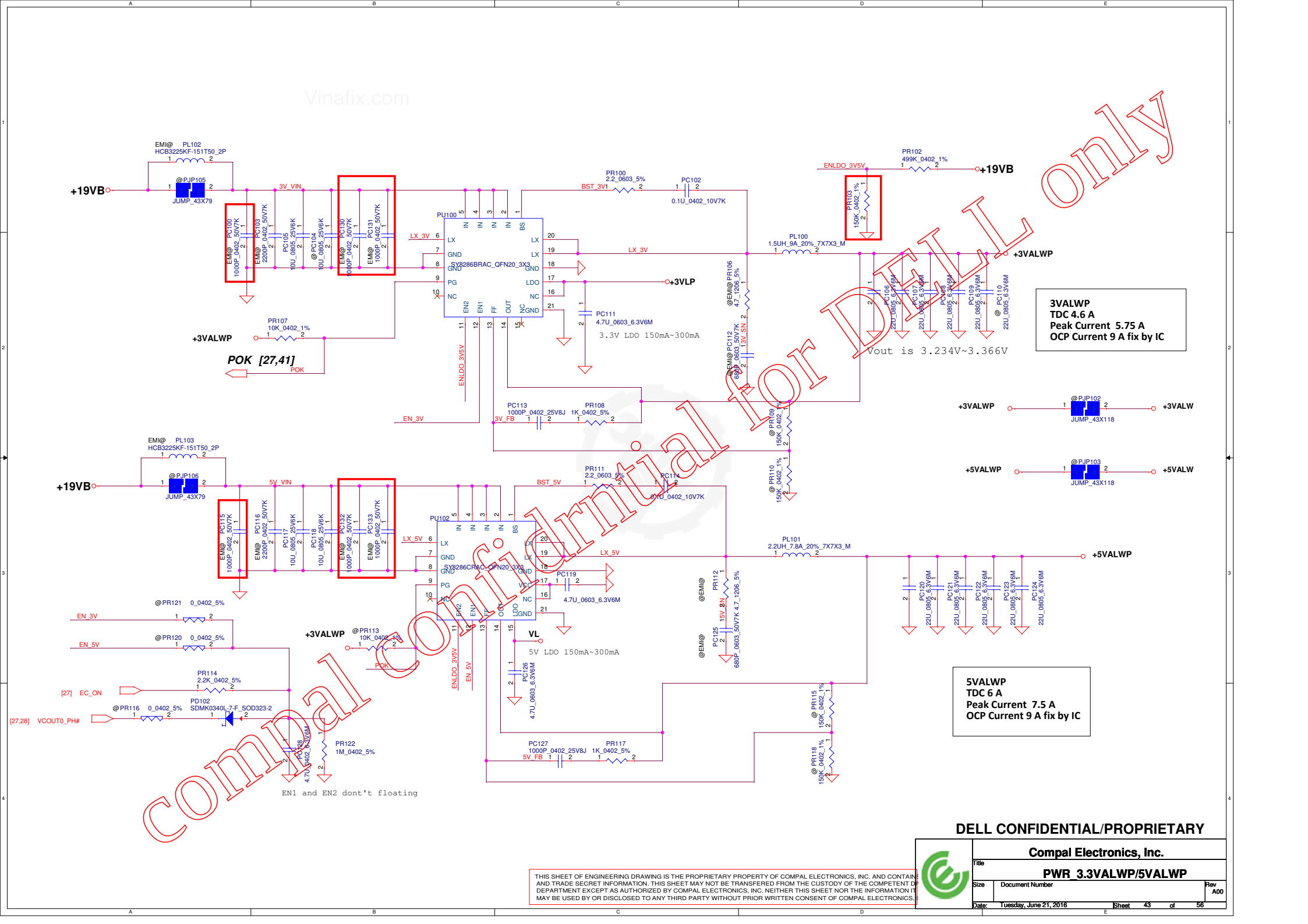
+19VB
EMI@ PL102 HCB3225KF-151T50_2P
@PJP105 JUMP_43X79
3V_VIN
PU100 SY8286BRAC_QFN20_3X3
LX_3V
BST_3V1
PR100 2.2_0603_5%
PC102 0.1U_0402_10V7K
PL100 1.5UH_9A_20%_7X7X3_M
+3VALWP
+3VLP
PC111 4.7U_0603_6.3V6M
3.3V LDO 150mA~300mA
Vout is 3.234V~3.366V
ENLDO_3V5V
PR102 499K_0402_1%
PR103 150K_0402_1%
PR107 10K_0402_1%
POK [27,41]
EN_3V
PC113 1000P_0402_25V8J
PR108 1K_0402_5%
3V_FB
PR109 150K_0402_1%
PR110 150K_0402_1%
3VALWP
TDC 4.6 A
Peak Current 5.75 A
OCP Current 9 A fix by IC
+3VALW
+5VALW
JUMP_43X118
+19VB
EMI@ PL103 HCB3225KF-151T50_2P
@PJP106 JUMP_43X79
5V_VIN
PU102 SY8286CRAC_QFN20_3X3
LX_5V
BST_5V
PR111 2.2_0603_5%
PC114 0.1U_0402_10V7K
PL101 2.2UH_7.8A_20%_7X7X3_M
+5VALWP
PC119 4.7U_0603_6.3V6M
VL
5V LDO 150mA~300mA
PR112 15V_8N
PC125 680P_0603_50V7K
4.7_1206_5%
@PR121 0_0402_5%
@PR120 0_0402_5%
EN_5V
@PR113 10K_0402_1%
PR114 2.2K_0402_5%
[27] EC_ON
PD102 SDMK0340L-7-F_SOD323-2
@PR116 0_0402_5%
[27,28] VCOUT0_PH#
PC126 4.7U_0603_6.3V6M
PC128 4.7U_0603_6.3V6M
PR122 1M_0402_5%
PC127 1000P_0402_25V8J
PR117 1K_0402_5%
5V_FB
PR115 150K_0402_1%
PR118 150K_0402_1%
5VALWP
TDC 6 A
Peak Current 7.5 A
OCP Current 9 A fix by IC
EN1 and EN2 dont't floating
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Compal Electronics, Inc.
PWR_3.3VALWP/5VALWP
Size Document Number Rev A00
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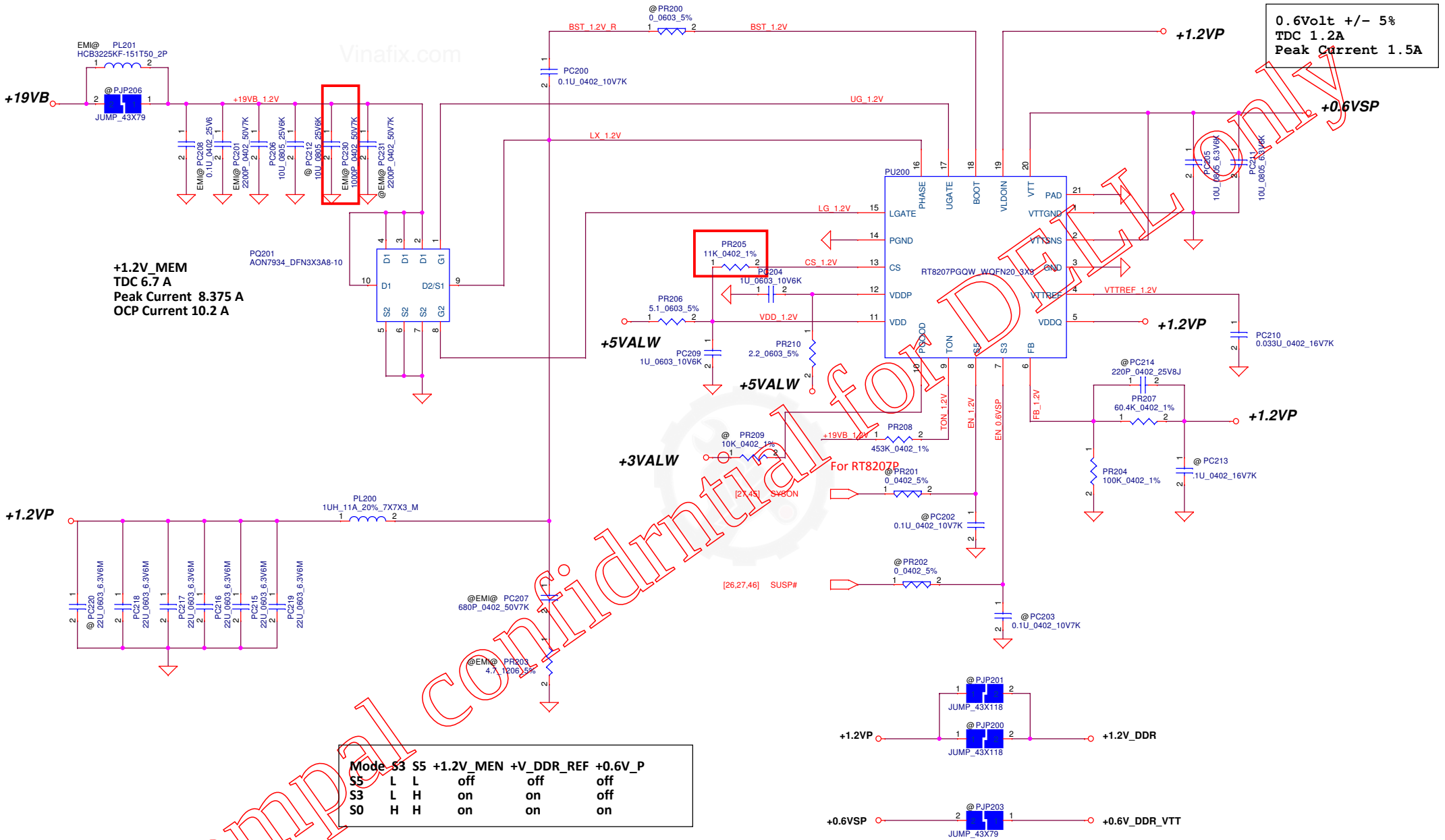
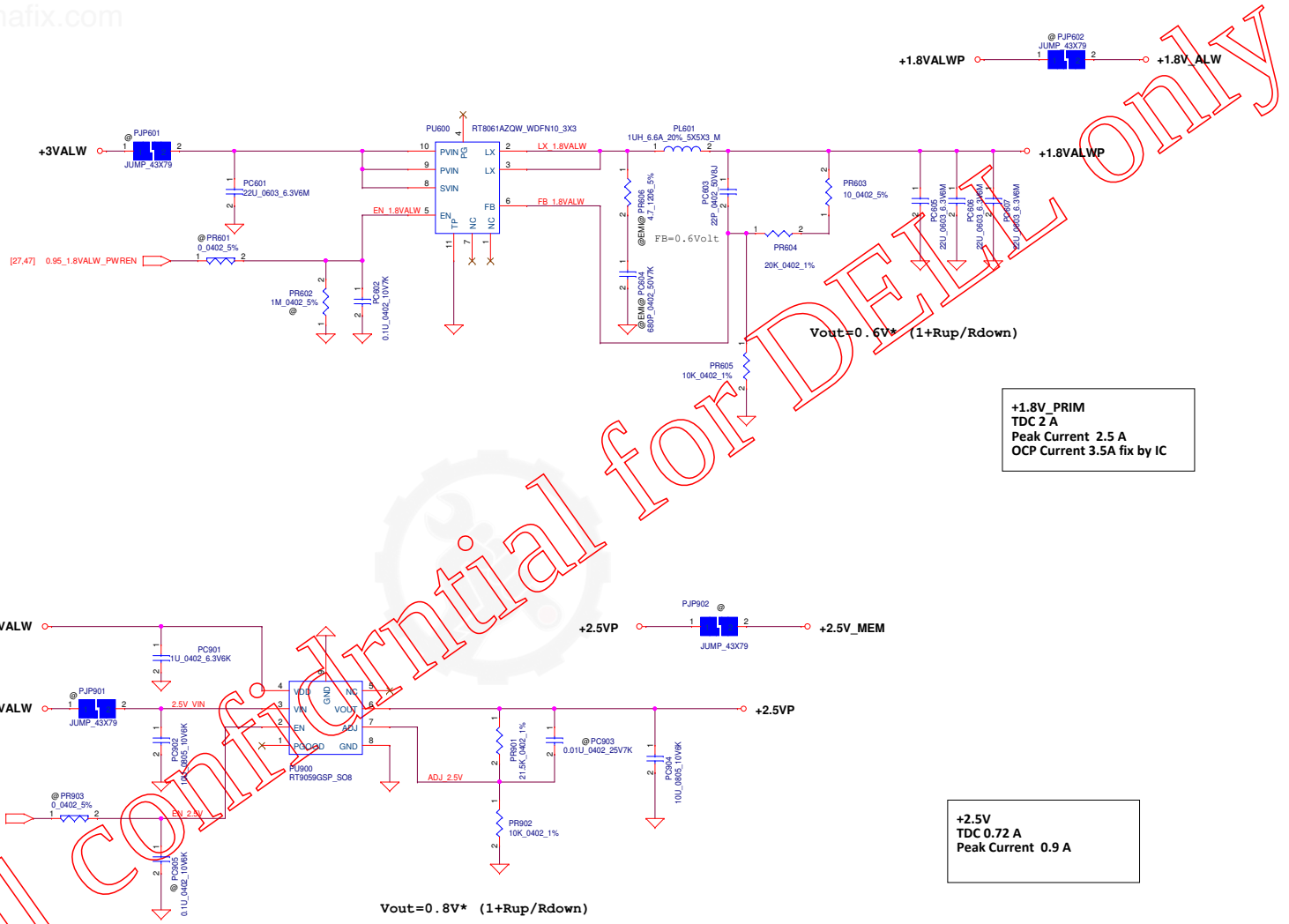


Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT

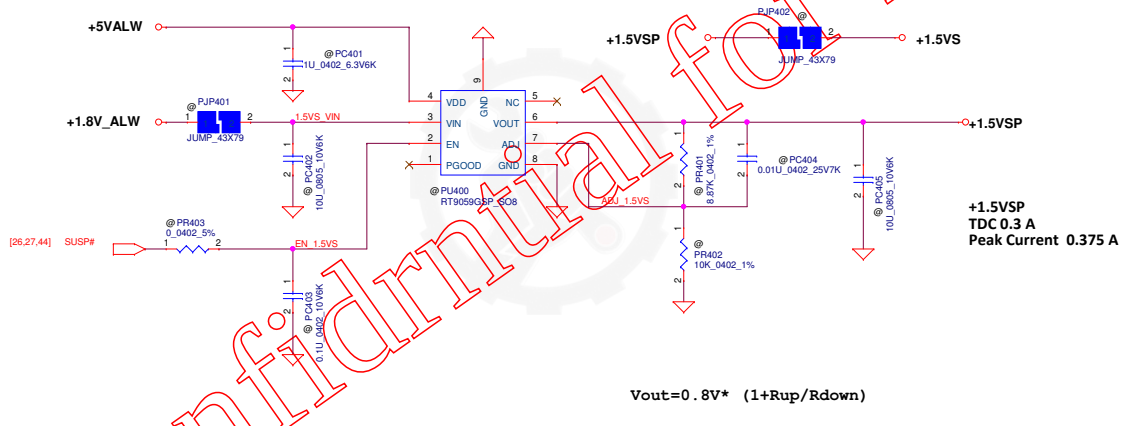
Size	Document Number	Rev
Custom		A00

Date: Tuesday, June 21, 2016 Sheet 44 of 56



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	PWR_+1.8V_PRIM and +2.5V		
Size C	Document Number		Rev A00
Date: Tuesday, June 21, 2016	Sheet 45 of 56		

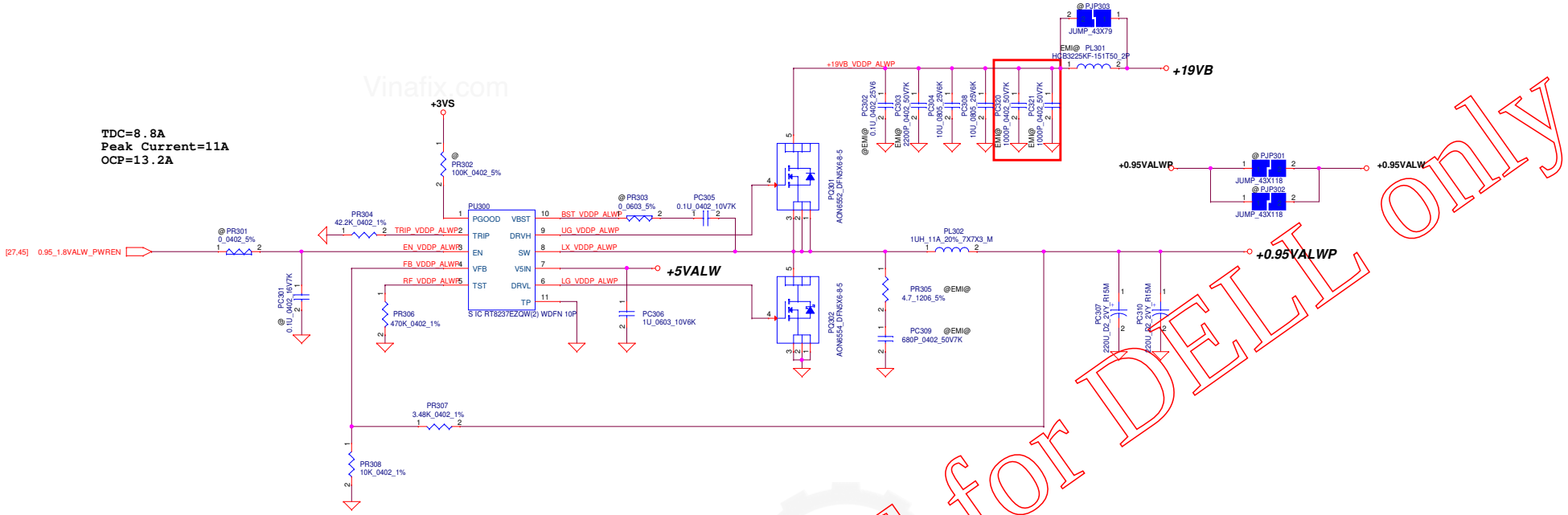


Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

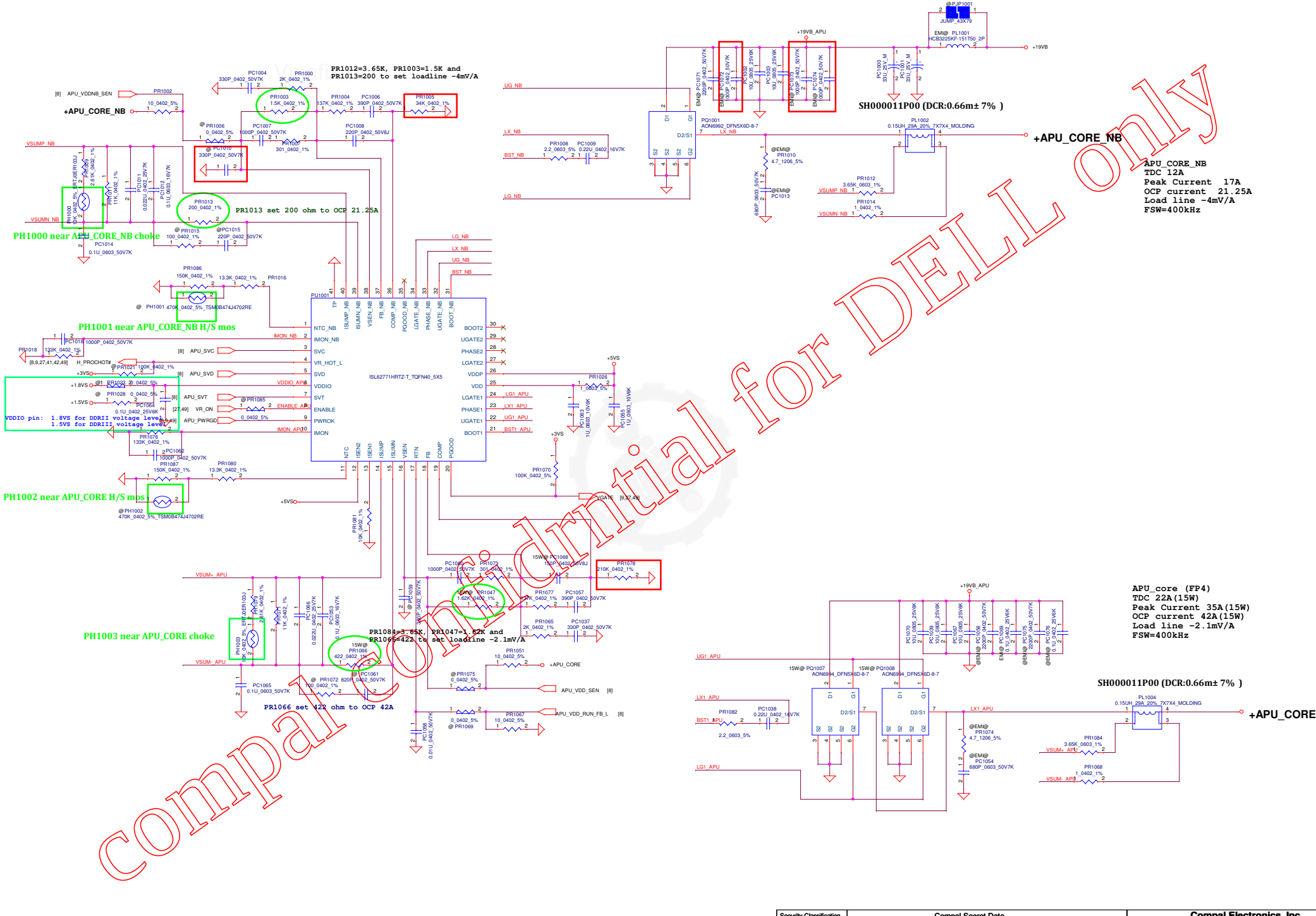
Title: **PWR_1.5VSP**

Size	Document Number	Rev A00
Date: Tuesday, June 21, 2016	Sheet 46 of 56	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Title	P45-PWR_VDDP_ALWP(+0.95V)		
Size C	Document Number		Rev A00
Date: Tuesday, June 21, 2016	Sheet 47 of 56		



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.	
Title	PWR_APU_CORE/APU_CORE_NB
Size: Custom	Document Number:
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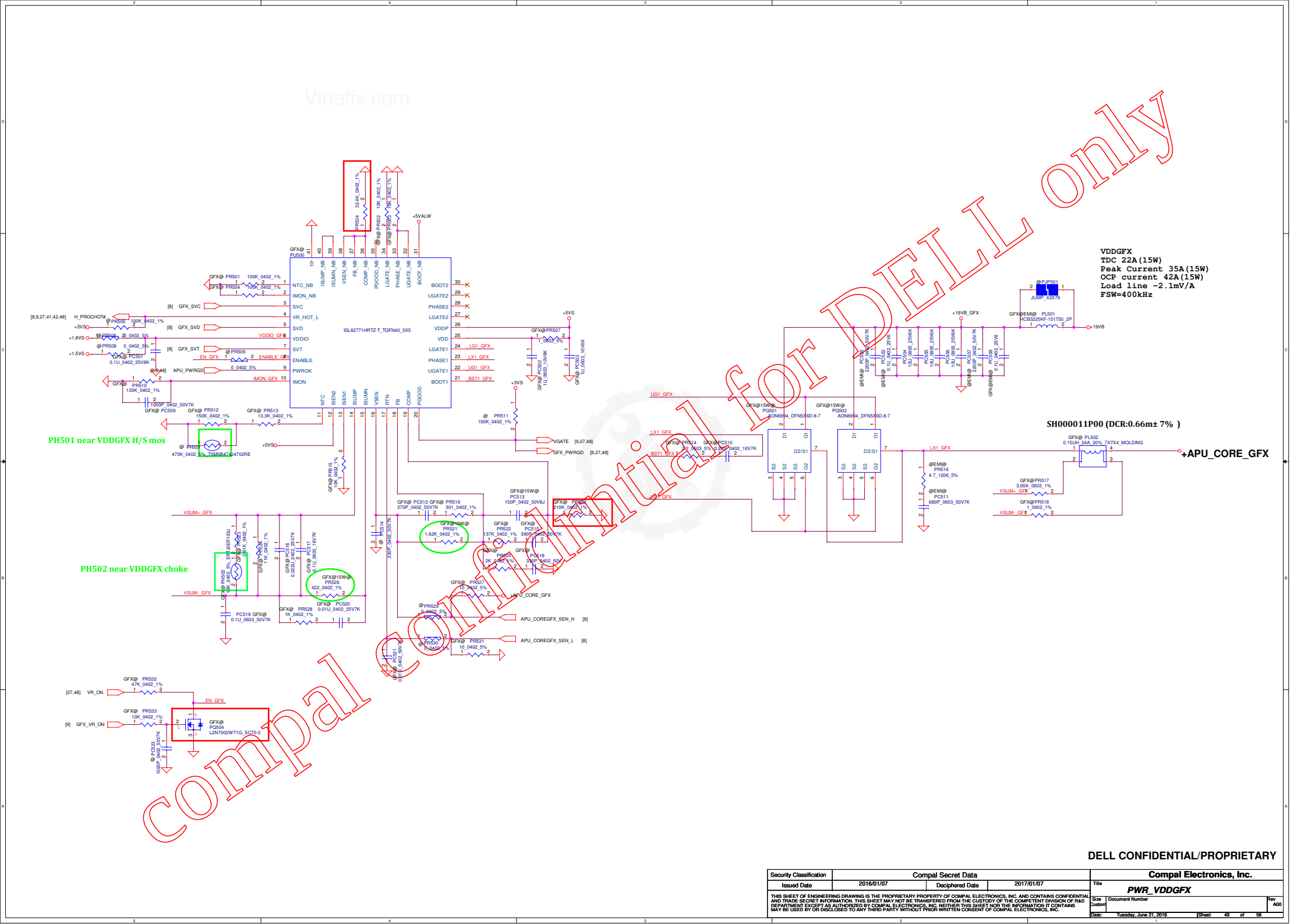

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date 2017/01/07	Title: PWR_VDDGFX
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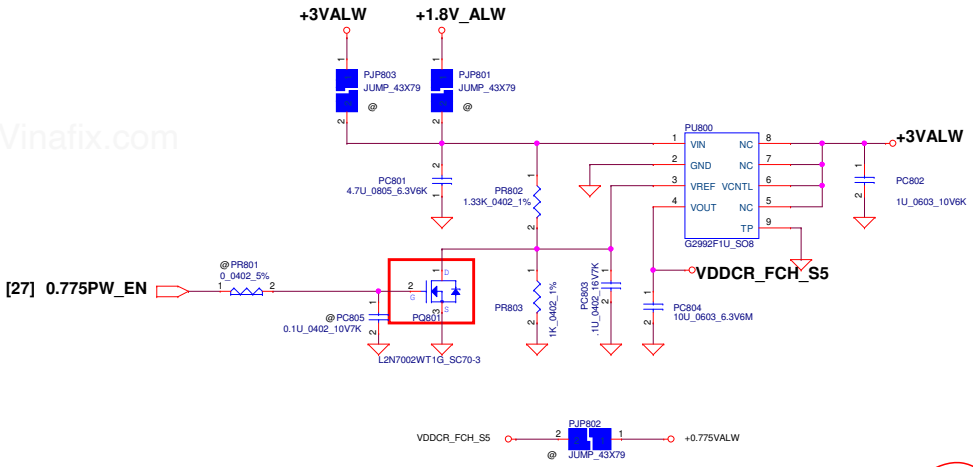
			Date: Tuesday, June 21, 2016; Sheet 49 of 56



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.		
Title	PWR_1.5V/VDDCR_FCH_S5	
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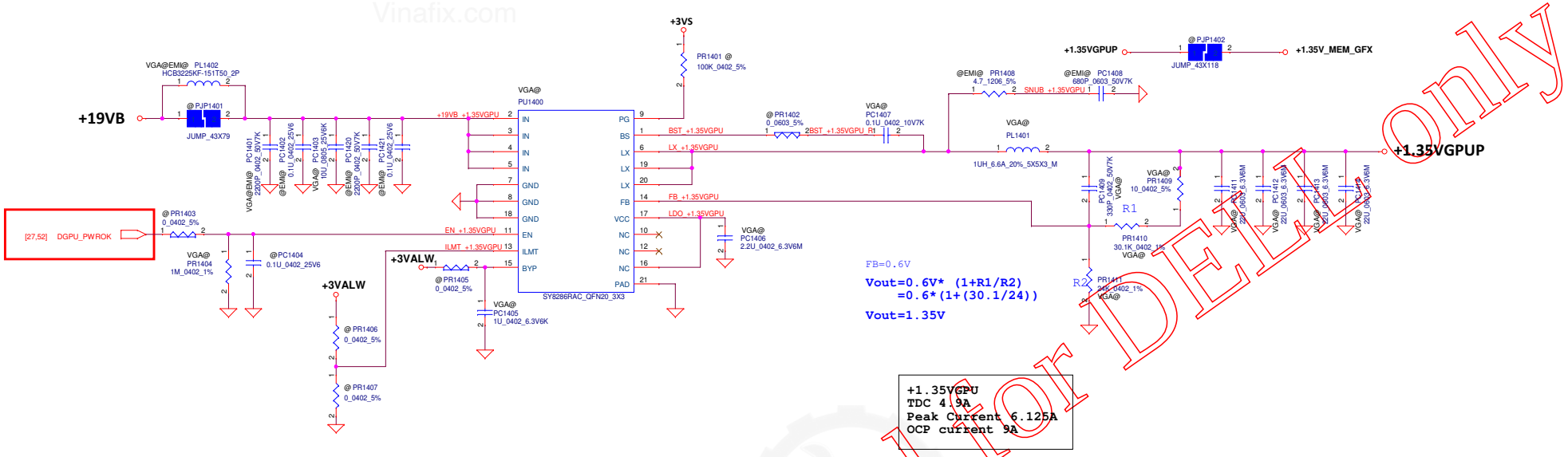

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin13)
6A	Pull low
9A	Floating
12A	Pull high

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.	
Title	PWR_+1.35VGPU
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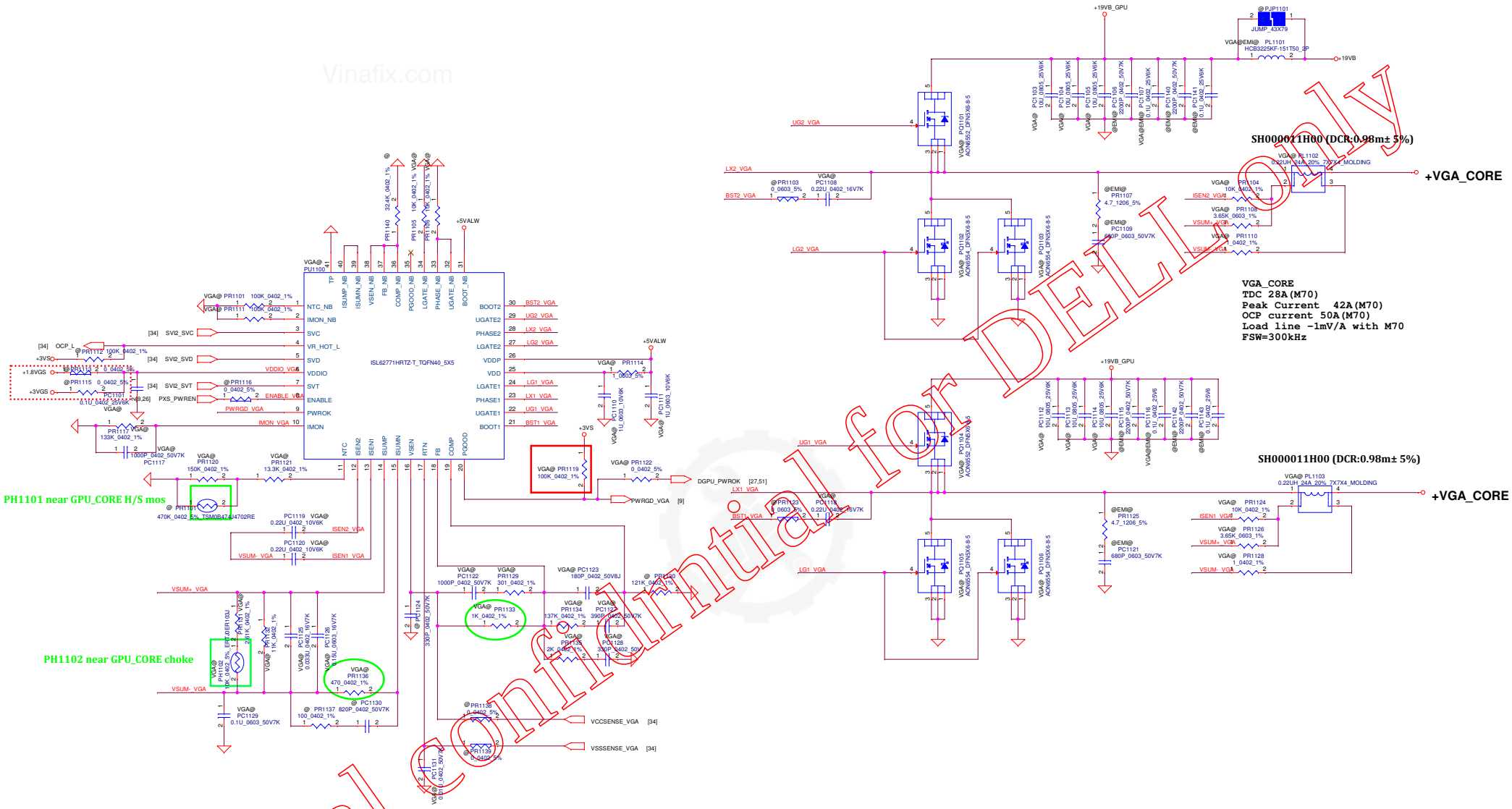

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date 2017/01/07	Title: PWR_VGA_CORE
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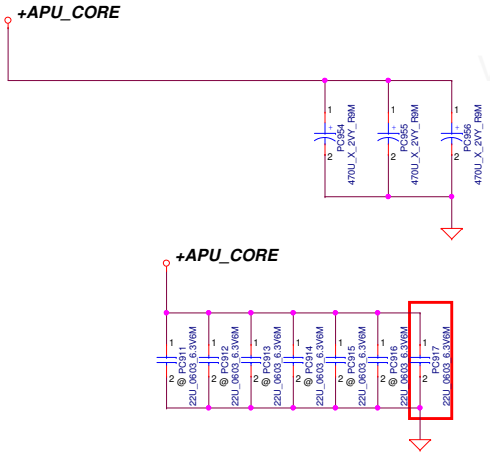
			Date: Tuesday, June 21, 2016; Sheet 52 of 56

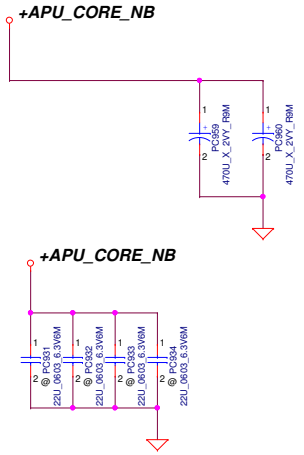
+APU_CORE

APU_CORE
470uF*3



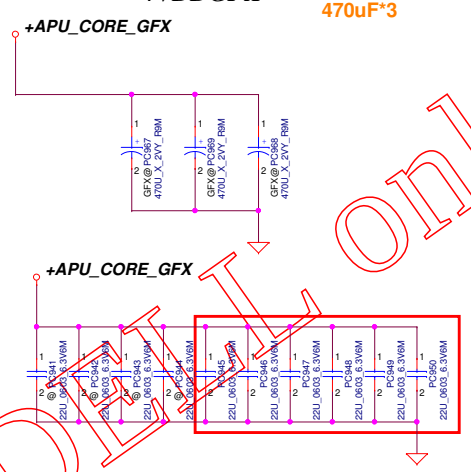
+APU_CORE_NB

APU_CORE_NB
470uF*2

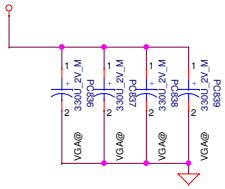


+VDDGFX

+VDDGFX
470uF*3



+VGA_CORE



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title: PWR_PROCESSOR DECOUPLING
				Size: Document Number: Rev: A00
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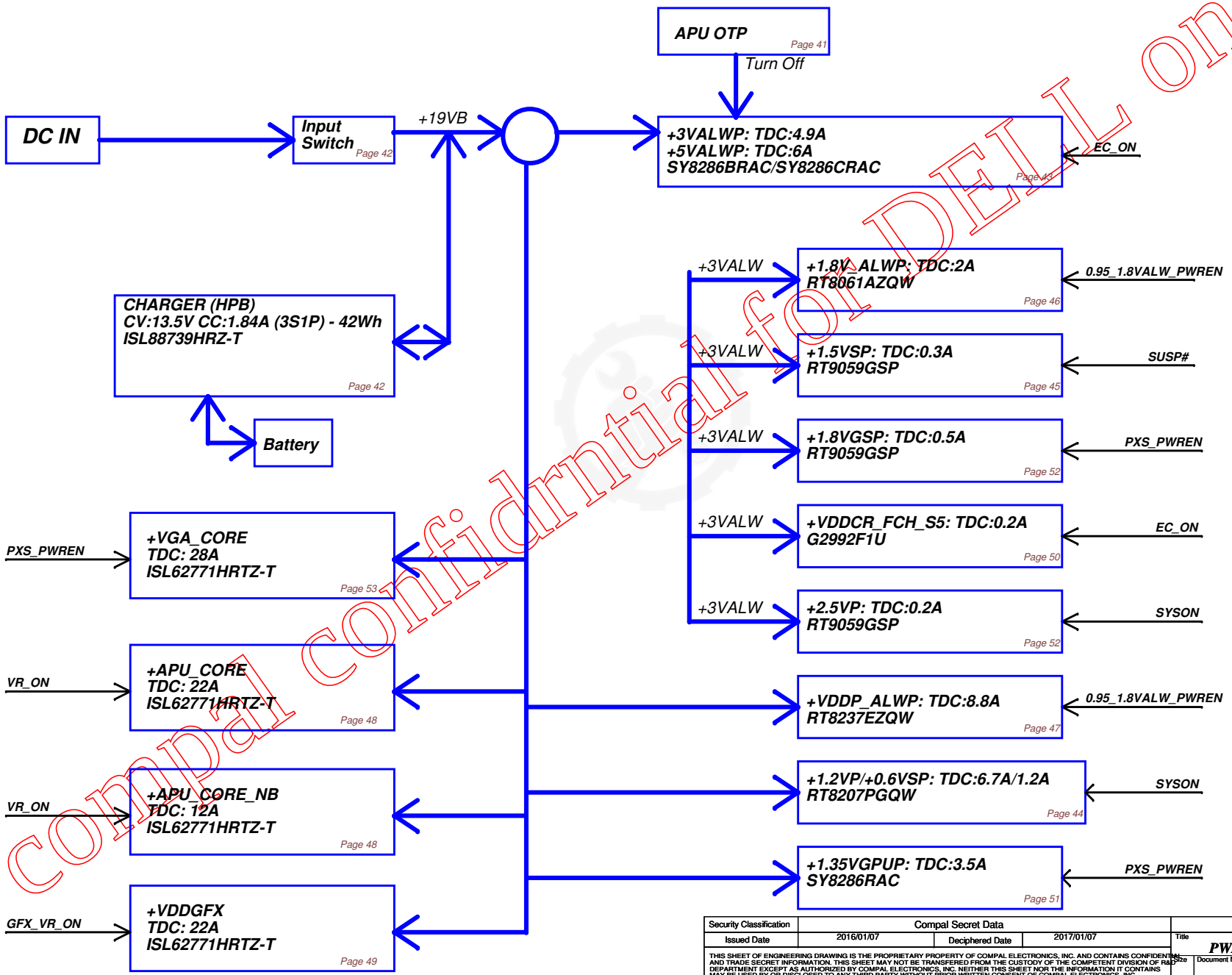
Power block



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: PWR_POWER BLOCK DIAGRAM			
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	CHARGER	2016/3/24	COMPAL	customer recommend	change PU703 from SA00009RO00 to SA00009Q50L	0.2
2	42	CHARGER	2016/3/24	COMPAL	adjust T/V setting	change PR732 from 49.9K to 53.6K	0.2
3	42	CHARGER	2016/3/24	COMPAL	design change	add PC751 560P change PR774 from 0 to 1K change PC748 from 2200P to 0.1U delete PC760 PC761 PC764	0.2
4	46	+1.5VSP	2016/3/24	COMPAL	change power rail from 1.5V to 1.8V by EE side	delete all 1.5VS component	0.2
5	48	APU_CORE	2016/3/24	COMPAL	design change to adjust APU_CORE setting	delete PC1010 change PR1005 from 11.5K to 34K change PR1078 from 95.3K to 210K	0.2
6	49	VDD_GFX	2016/3/24	COMPAL	design change to adjust GFX_CORE setting	add PR534 32.4K change PR520 from 95.3K to 210K	0.2
7	52	VGA_CORE	2016/3/24	COMPAL	design change from EE recommend	add PR1119 100K	0.2
8	41	DCIN/BATT CONN/OTP	2016/5/06	COMPAL	adjust OTP setting from thermal recommend	change PR24 from 14K to 16.9K	0.3
9	41	DCIN/BATT CONN/OTP	2016/5/06	COMPAL	design change to remove Erp lot6 circuit	delete PR2,PR5,PR7,PR10,PQ1	0.3
10	44	+1.2V_MEN/+0.6V_DDR	2016/5/06	COMPAL	adjust OCP setting	change PR205 from 8.25K to 11K	0.3
11	42	CHARGER	2016/5/06	COMPAL	design change	change PQ740 from SB000014900 to SB00000SY00	0.3
12	53	PROCESSOR DECOUPLING	2016/5/06	COMPAL	design change to meet stardust test result	add PC917,PC945,PC946,PC947,PC948,PC949,PC950	0.3
13	41	DCIN/BATT CONN/OTP	2016/6/16	COMPAL	design change from EMI recommend	change PC2,PC4 from 0.1U to 2200P	1.0
14	43	3.3VALWP/5VALWP	2016/6/16	COMPAL	design change	change PR103 from 499K to 150K	1.0
15	41	DCIN/BATT CONN/OTP	2016/6/16	COMPAL	adjust OCP setting	change PR24 from 16.9K to 15K	1.0

DVT1 change list

Item	Page	Date	Rev.	Reason for change	Modify Item
1	26	2016/1/28	0.2	modify the capacitor value	C621 change 1u_0603 capacitor to 4.7u_0603
2	26	2016/1/28	0.2	modify the capacitor value	C620 change 4.7u_0603 capacitor to 1u_0603
3	26	2016/1/28	0.2	Part count	C344 pop change to " DIS@ "
4	13	2016/1/29	0.2	Change Capacitor to H1.9	CD229 Change to SGA20331E10
5	26	2016/3/13	0.2	modify RC Delay for +1.8VGS	1.8VGS_0.95VSDGPU_ON connect to U15.3 & U15.5 (R440 pop 47K, C624 pop 0.1uF)
6	24	2016/3/13	0.2	pop Q9 for touch-pad (PTP)	Q9 Change to pop
7	16	2016/3/15	0.2	Follow Intel KBL BOM to cost reduce	+LCDVDD power switch U1 change to SA000079400
8	11,18	2016/3/15	0.2	Audio codec +1.5VS change to +1.8VS cost down +1.5VS LDO	Add RC18/RA15/RA16 ,reserve +1.5VS
9	24	2016/315	0.2	JKB1.30 remove KB_DET# (follow Tulip)	Add RE60 reserve to +5VS
10		2016/3/16	0.2	part count reduce	change to R-short RC119, RA1,RA2,RA4,RA5,RL5,R16,RC53,RC52
11	10,25	2016/3/16	0.2	change USB Port (AMD request)	USB20 Port7 change to Port2 (camera device)
12	22	2016/3/16	0.2	SATA net name modify	modify to SATA_TX_P0/N0 SATA_RX_P0/N0
13	22	2016/3/18	0.2	remove SATA ESD, confirm with ESD team	Delete EU3101
14	17	2016/3/18	0.2	for layout request swap RPI2 pin	Swap RPI2 pin
15	9	2016/3/18	0.2	BOM name error	R7C03 ---> RC703
16	9	2016/3/18	0.2	modify VRAM config.	net name vram size/APU_ID/Panel size_ID change to VBIOS_ID1/ID2/ID3
17	6	2016/3/21	0.2	add AMD FX-9800P CPU	Add FX-9800P CPU
18	26	2016/3/21	0.2	modify to meet the GPU power sequence	modfiy R438 1K ohm to 47K ohm
19	30	2016/3/21	0.2	ME drawing add a screw hole	add H13 H_6P0 screw hole
20	24	2016/3/21	0.2	Follow Intel KBL BOM to cost reduce	F3 SP040002400 change to SP040002B00
21	30	2016/3/21	0.2	DFx review stand off pad can't place via	H11 H_3P2-G modify to H_3P2
22	18	2016/3/21	0.2	vendor feedback have extra pull-up Resistor	remove RA46, RA47
23	29	2016/3/21	0.2	remove PWR/Board unused pin	remove JPWR1.4 +5VALW net name
24		2016/3/21	0.2	fix Hi-Pot	LANGND Change to GND
25	19	2016.01.14	0.2	modify UL3 BOM config	remove UL3 BOM config
26	26	2016.01.14	0.2	modify R439 BOM config	add DIS@ BOM config to R439
27	34	2016.01.14	0.2	modify RV164 BOM config	add DIS@ BOM config to RV164
28	18	2016.01.14	0.2	modify CA42 BOM config	add 3234@ BOM config to CA42
29	26	2016.01.14	0.2	modify GPU power sequence	C622, C623 change 4.7U 0603 to 0.1U 0402 and unpop
30	9	2016.03.21	0.2	unify name with stoney	AGPIO65 change to SKU_ID
31	14	2016.01.14	0.2	For cost reduce	unpop CD144
32	13	2016.01.14	0.2	For cost reduce	change CD116 SGA00006A00 to SGA20331E10
33	16	2016.02.04	0.2	Colay F1	unpop R4 and pop F1
34	27	2016.01.14	0.2	DVT1 board ID	RE22 0 ohm change to 12K ohm
35	26	2016.02.04	0.2	follow spec suggestion	C621 change 4.7U 0603 to 1U 0402
36	26	2016.02.04	0.2	modify GPU power sequence	pop C344
37	18	2016.02.04	0.2	Follow EMC suggestion	LA3, LA4, LA5, LA6 change SM01000EI00 to SM01000NX00 (change part size 0603 to 0402)
38	26	2016.02.04	0.2	modify GPU power sequence	R438 change 1K ohm to 47K
39	26	2016.02.04	0.2	modify GPU power sequence	add C983 0.1uF
40	27	2016.03.22	0.2	EC require due to no use	unpop RE44,RE40,RE23,RE24,CE47
41	20	2016.03.22	0.2	confirm EC use RW6,RW7 to debug	unpop RW9.RW10
42	26	2016.03.22	0.2	Follow Intel KBL	add C625 0.1uF
43	29	2016.03.22	0.2	ME DFX require	JPWR1 change part
44	22	2016.03.17	0.2	meet DFX require	modity JHDD1 footprint
45	13	2016.03.17	0.2	For cost reduce	change CD117 SGA00006A00 to SGA20331E10
46	22	2016.03.17	0.2	for fine tune sata redriver setting	unpop RS37,RS27,RS28,RS22
47	40	2016.03.17	0.2	meet dell require	UV12,UV13,UV14,UV14 VRAM part change
48	11	2016.03.24	0.2	add+0.95 GFX power shape	delete LC22
49	8.27	2016.03.24	0.2	add +APU_CORE power shape	delete APU_RST#_EC/APU_PWRGD_EC reserve compoent

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Title: **HW-PIR-1**

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DVT2 change list

Item	Page	Date	Rev.	Reason for change	Modify Item
1		2016.04.12	0.3	reduce part count	change to R-short: RC20,RC1675,R12,R14,R7,R51,RA22,RA11,RA42,RE338,RE5,RE31,RE32,RE33,RE34,RE37,RE38,RE39,RE50, RE51,RE42
2	27	2016.04.13	0.3	EC Board id change	RE22 12K 1% change to 15K 1% (SD034150280)
3	16	2016.04.14	0.3	reduce part count	change to R-short:R6,R13,RX7
4	30	2016.04.21	0.3	correct part	C35~C40 16V change to 25V rating (SE00000G880)
5		2016.04.21	0.3	increase voltage rate	C4 10U 6.3V change to 10U 25V (SE00000X210)
6		2016.04.21	0.3	increase voltage rate	C34,C2305,C2306,C2308,CA1,CA3,CU13,CU18 :10U 6.3V change to 10U 10V(SE00000SU00)
7		2016.04.21	0.3	increase voltage rate	CA11 4.7U 6.3V change to 4.7U 10V (SE00000MA00)
8		2016.04.21	0.3	increase voltage rate	CF4 22U 6.3V change to 22U 10V (SE00000VJ80)
9	29	2016.04.22	0.3	follow ME require	change PWR CONN("E-T_6915K-Q06N-00L_6P")
10	30	2016.04.23	0.3	factory JQE require	modify H6 from 5 to 5.6 mm
11	17	2016.04.29	0.3	for layout modify	RPI1 net swap
12	17	2016.04.29	0.3	for layout spacing	del CI11~CI18 emi part
13	27	2016.05.03	0.3	follow ESD require	CE23 change to pop
14	21	2016.05.03	0.3	follow EMI require	LA8,LA9(SD028000080) from bead change to 0 ohm 0402
15	30	2016.05.03	0.3	follow EMI require	C35~C49 change to unpop
16		2016.05.03	0.3	reduce part count	RC22,RC664,RA15,RC18,RD18,RD21,RA40,R37,RL9,RW11,RV164,RV27,RV30,RV364,RV31
17	29	2016.05.03	0.3	follow ME require	Update JPWR1 footprint to "JXT_FP226H-006S1BM_6P"

XB change list

Item	Page	Date	Rev.	Reason for change	Modify Item
1	9	2016.05.21	1.0	fixed PCIE wake on DC mode	reserve for RC667(0 ohm 0402)
2	26	2016.05.31	1.0	modify +0.95VGS/+1.8VGS sequence	C343,C344 From 330P to 1000P (SE074102K80)
3	6	2016.06.03	1.0	APU R3 PN	add APU R3 PN
4	33	2016.06.03	1.0	GPU M70 R3 PN	add GPU M70 R3 PN
5	38,39	2016.06.06	1.0	VRAM R3 PN	add VRAM R3 PN
6	30	2016.06.06	1.0	PCB R3 PN	add PCB R3 PN
7	23	2016.06.06	1.0	fixed factory usb 3.0 fail issue	change LU1,LU2,LU4,LU5 from SM070003V00 90 ohm to SM070004K00 67ohm
8	9	2016.06.06	1.0	fixed RTC idle 24hrs over +-2S	change CC682 from 22P to 18P
9		2016.06.06	1.0	follow DFB suggestion	R17,R18,RU5,RU6,RU11,RU12,RU13,RU14,RU18,RU17,RU9,RU10, RI1,RI2,RI4,RI5,RI7,RI8,RI10,RI11,RU3,RU4,RU7,RU8,RU1,RU2 cover the solder mask ,so change footprint
10	18	2016.06.06	1.0	reduce part count	RA17,RA18,RA19,RA20,RA21 change to R_short
11	27	2016.06.06	1.0	EC board ID	RE22 from 15K(SD034150280) to 20K (SD034200280)
12	24	2016.06.13	1.0	follow DFB suggestion	JKB1 from SP01001LM00(S H-CONN ACES 50699-03041 30P) to SP01001LN00(S H-CONN STARCONN 132C30-100020 30P)
13	29	2016.06.13	1.0	reduce part count	reserve for SW1 SW2(For debug) on pilot run