MODEL NAME :DAZ10
PCB NO :LA-F211P

Dell/Compal Confidential

Schematic Document

La Ferrari (KABY LAKE-G)

2018-02-26 Rev: 1.0 (A00)

@ : Nopop Component
@SPAD@ : Nopop Component 0 Ohm Short-PAD
CMC@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, PCH, PCB
TPM@ : TPM funct i on
EMC@ : Pop of EMI parts
BreakDown@ : for measure power consumpt i on
SDP@ : for DDR4 8G
DDP@ : for DDR4 16G
DIS@ : for I5,I7 CPU
RF@ : RF Solut i on Co mponent

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

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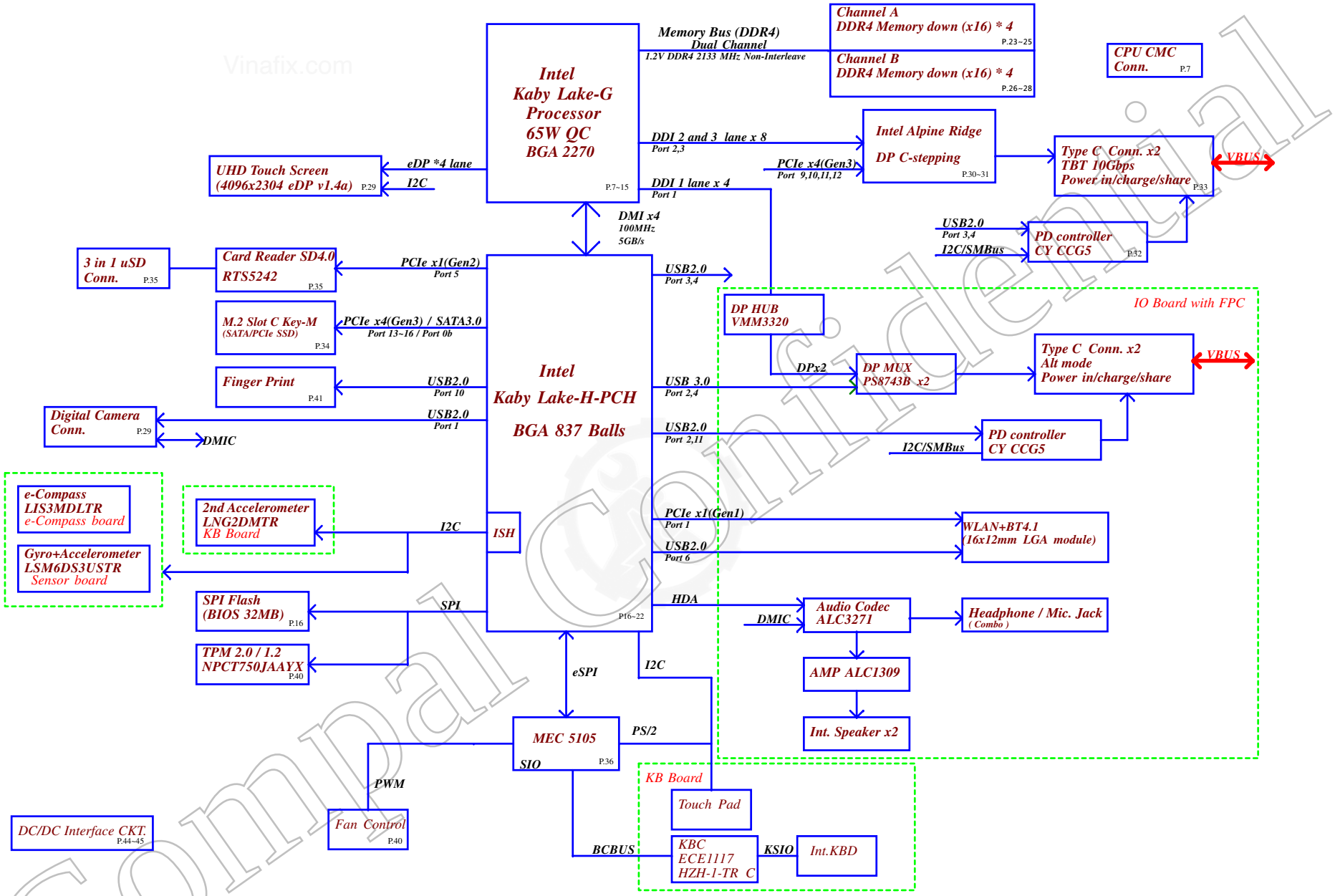
Title: Cover Page		
Size	Document Number: LA-F211P	Rev: 1.0(A00)
Date: Monday, February 26, 2018	Sheet 1 of 71	



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Issued Date	2017/04/07	Deciphered Date 2018/12/31	Title: Block diagram
			Size: Document Number: LA-F211P Rev: 1.0(A00)
			Date: Thursday, January 11, 2018 Sheet 2 of 71

Board ID	Resistor
X00	240K
X01	130K
X02	62K
A00	4.3K

USB3	DESTINATION
1	DP MUX-1
2	DP MUX-2
3	None
4	Debug
5	None
6	None

USB 2.0	DESTINATION
1	CAMERA
2	TYPEC Port4(DB)
3	TYPEC Port1(MB)
4	TYPEC Port2(MB)
5	None
6	BT
7	None
8	Debug
9	None
10	Finger Print
11	TYPEC Port3(DB)
12	None

DDI	DESTINATION
1	DP HUB
2	Alpine Ridge
3	Alpine Ridge

PCI EXPRESS	DESTINATION
Lane 1	WLAN
Lane 2	None
Lane 3	None
Lane 4	None
Lane 5	CARD READER
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	Alpine Ridge
Lane 10	Alpine Ridge
Lane 11	Alpine Ridge
Lane 12	Alpine Ridge
Lane 13	SSD
Lane 14	SSD
Lane 15	SSD
Lane 16	SSD

USB3	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0A	N/A
1A	N/A
N/A	N/A
N/A	N/A
0B	SSD
1B	None
2	None
3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	NGFF-2 SSD	10	None
1	None	11	None
2	None	12	None
3	WLAN	13	None
4	None	14	None
5	None	15	None
6	Thunderbolt		
7	DGPU		
8	CARD READER		
9	None		

Symbol Note :

: means Digital Ground

: means Analog Ground

Voltage Rails

Power Plane	Descript i on	S0	S0ix	S3	S4/S5	DS3
+RTCVCC	RTC power	ON	ON	ON	ON	ON
+CHG_VIN_20V	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+3V_LDOP	+CHG_VIN_20V to +3V_LDOP power rail for suspend power	ON	ON	ON	ON	ON
+VBATT	BATT power supply	N/A	N/A	N/A	N/A	N/A
B+	AC or BATT power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+3VALW/+3VD	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+5VALW/+5VD	System +5VALW power rail	ON	ON	ON	ON*	ON
+1VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+1V_MPHY_MPHYPLL	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+3V_PCH_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3V_PCH	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	ON	OFF	ON
+0.6VS	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+VCCIO	+0.95VS IO power rail	ON	OFF	OFF	OFF	OFF
+VCCSA	System Agent power rail	ON	OFF	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCCGT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+VDD_33	I/O power for 3.3V pins, such as GPIOs and AUX	ON	OFF	OFF	OFF	OFF
+VDD_18	1.8V supply for TMDP, PLL, PCIE, HBM2PHY, XTAL, ON etc.	ON	OFF	OFF	OFF	OFF
+VDD08	Digital power supply for PLL, PCIe and Display PHYs	ON	OFF	OFF	OFF	OFF
+VPP_25	Charge pump voltage for HBM2	ON	OFF	OFF	OFF	OFF
+VDDCI	Supply voltage for I/O logic	ON	OFF	OFF	OFF	OFF
+VGA_CORE	dGPU supply voltage for Graphics Core	ON	OFF	OFF	OFF	OFF
+VDD12	dGPU supply voltage for HBM2 interface	ON	OFF	OFF	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF						

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Title: Notes List

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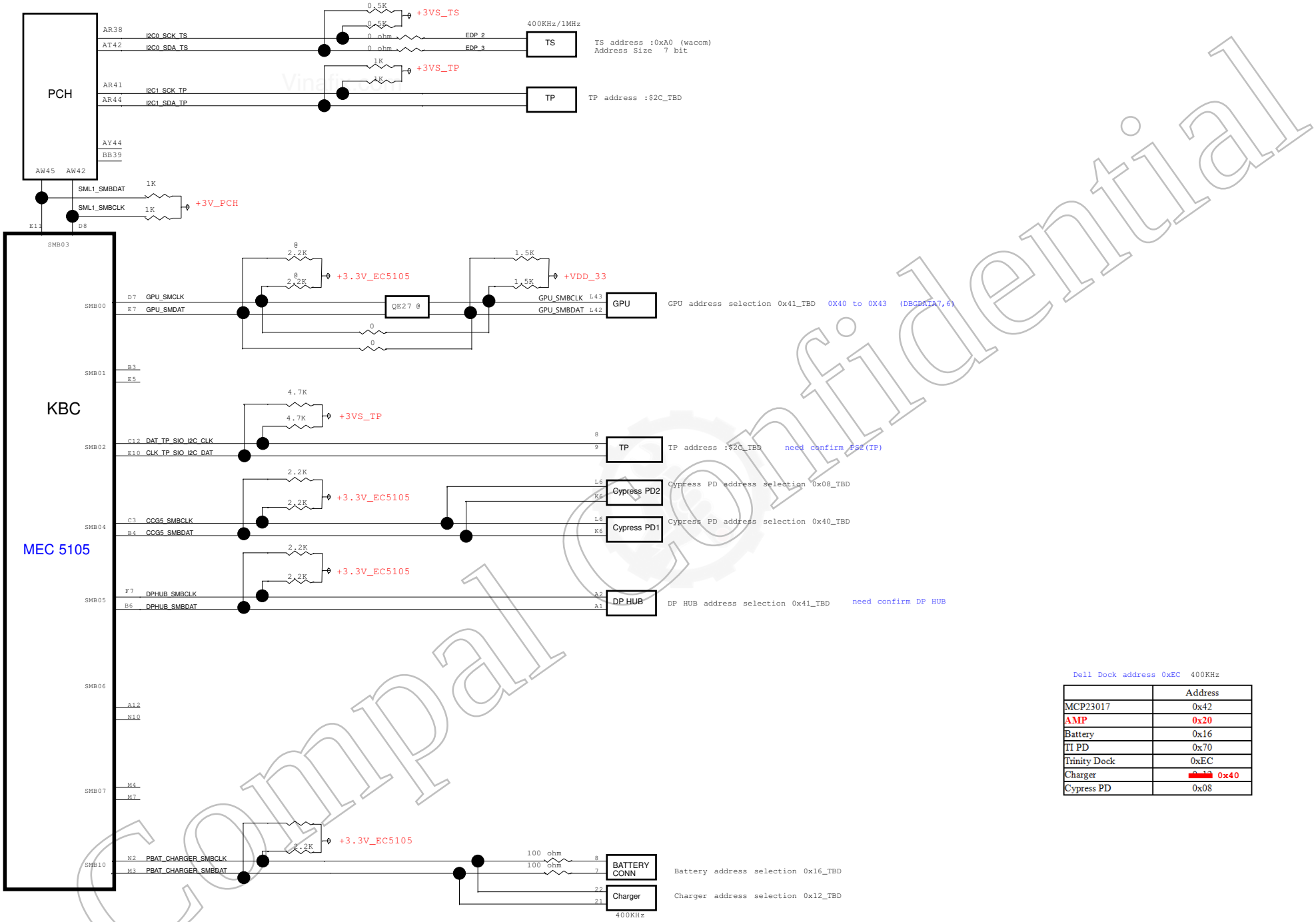

Dell Dock address 0xEC 400KHz

	Address
MCP23017	0x42
AMP	0x20
Battery	0x16
TI PD	0x70
Trinity Dock	0xEC
Charger	0x40
Cypress PD	0x08

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Title: SMBus Block Diagram

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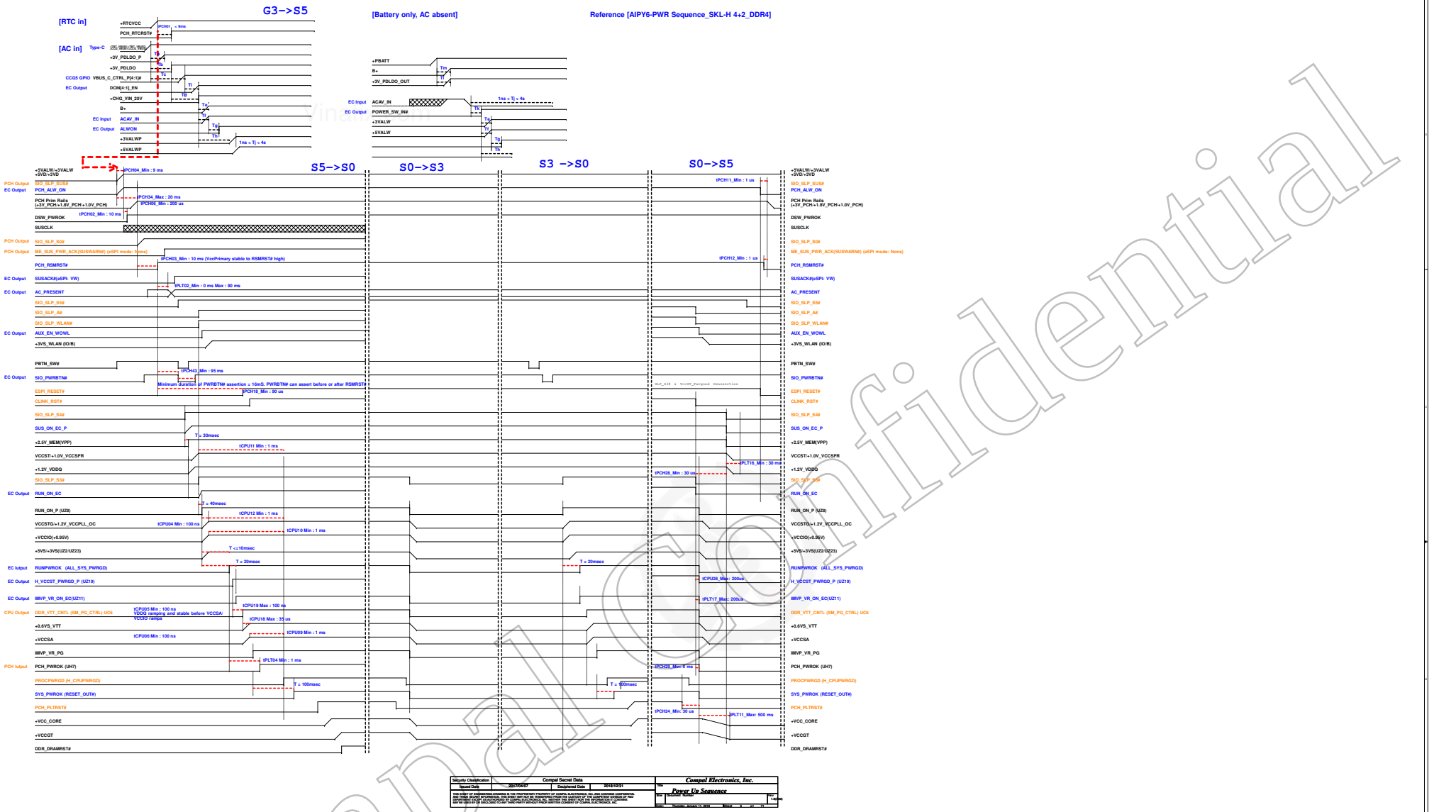

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Title: Power Up Sequence

Size	Document Number	Rev
		1A(P/S)

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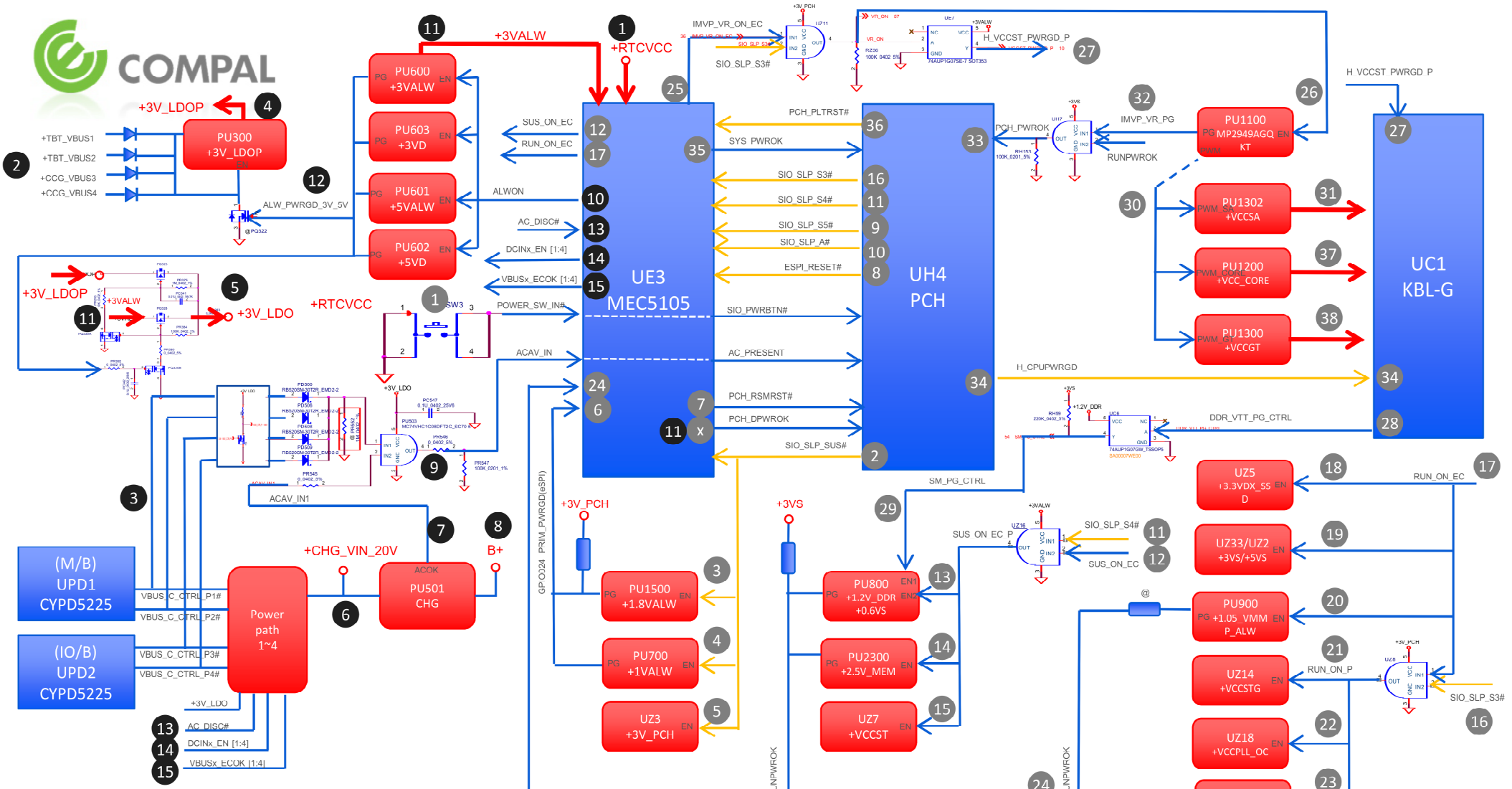

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Title	P07-Power Sequence-2		
Size	Document Number		Rev
Custom			0.0(NOI)
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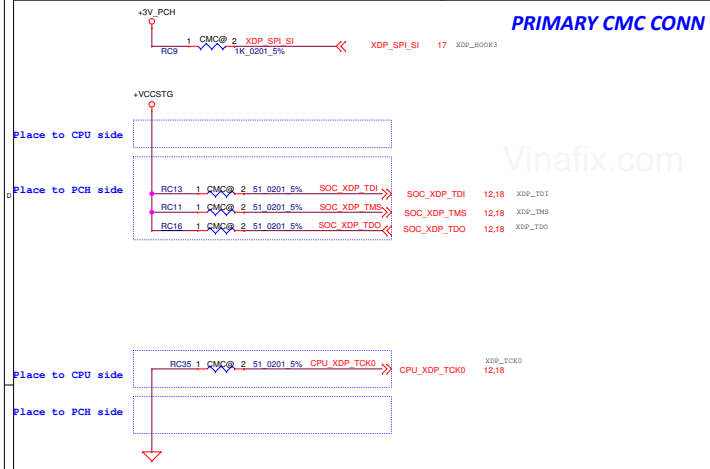
PRIMARY CMC CONN

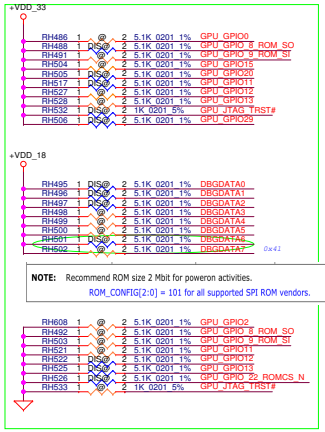


dGPU Pin Straps

Table 1-57. dGPU Pin Straps

Signal Name	Description	dGPU Default	Recommended settings[1]
1 GPIO[29]	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).	0 (Internal pull-down)	Provide a pull-up resistor option to V_{DD_33} only for designs where dGPU does not drive any displays (headless)
1 GPIO[20]	PCI Express transmitter de-emphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.	0 (Internal pull-down)	Install pull-up resistor to V_{DD_33} when full swing is used. DNI for half swing usage. Pull down resistor to GND is optional and should DNI for headless designs
0 GPIO[0]	Controls the transmitter full/half swing mode. 0: The transmitter full-swing is enabled. 1: The transmitter half-swing is enabled.	0 (Internal pull-down)	Install pull-up resistor to V_{DD_33} only if design requires PCIe half swing. Pull down resistor to GND is optional and should DNI for half swing
X01 001 GPIO[13] GPIO[12] GPIO[11]	• If BIOS_ROM_EN = 1, then ROM_CONFIG[2:0] defines the ROM type. See **ROM Configurations TBD** for details. • If BIOS_ROM_EN = 0,then ROM_CONFIG[2:0] defines the primary memory aperture size	101 (Internal pull-up/pull-down)	Design dependent. Provide a pull-down resistor option to GND on the PCB for GPIO_13. Provide a pull-up resistor option to V_{DD_33} on the PCB for GPIO_12. Provide a pull-down resistor option to GND on the PCB for GPIO_11.
0 (X01) GPIO[22]_ROMCS#[2]	0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device. **Note:** When an external BIOS ROM device is used, GPIO[22]_ROMCS# also connects to the ROM device's chip select (active low).	1 (Internal pull-up)	Connect to Chip Select of the external ROM through a series 33Ω resistor. Provide a pull-down resistor option to GND on the PCB.
HSYNC VSYNC	Special usage 1: Pull up resistor to V_{DD_33} 0: Pull down resistor to GND	0 (Internal pull-down)	Design dependent Provide a pull-up resistor option to V_{DD_33} on the PCB for each pin

dGPU Pin Straps



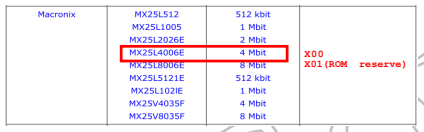
DESIGN THAT HAS ROM FOR VIDEO BIOS:
GPIO[13:11] =101, SPI ROM for all supported SPI ROM vendors follow 571726 MOW22

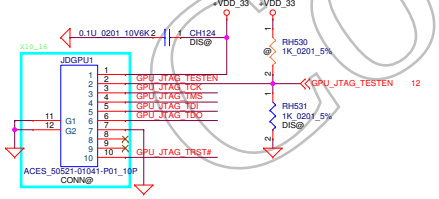
DESIGN THAT DOES NOT HAVE ROM FOR VIDEO BIOS (ROMLESS):
GPIO[13:11] =001

GPIO_22(GPU_GPIO_22_ROMCS_N):
PULL-UP: FOR DESIGN THAT HAS ROM FOR VIDEO BIOS
PULL-DOWN: FOR DESIGN THAT DOES NOT HAVE ROM FOR VIDEO BIOS (ROMLESS)

ROMLess
GPIO_[22], 0: Disable external BIOS ROM device.
GPIO_[13:12:11], 001: 256MB AP Size for ROMless

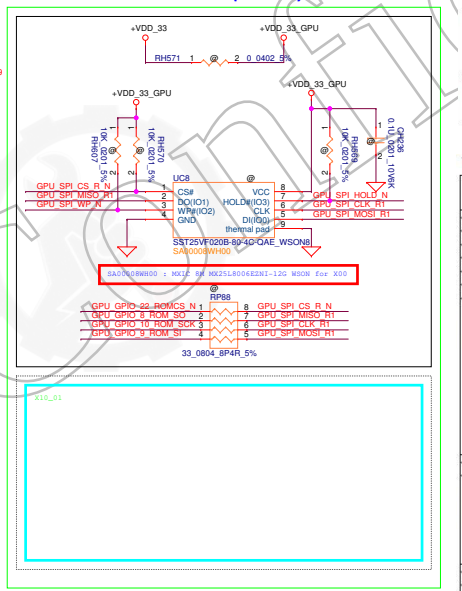
External VGA ROM
GPIO_[22], 1: Enable external BIOS ROM device.
GPIO_[13:12:11], 101: External ROM

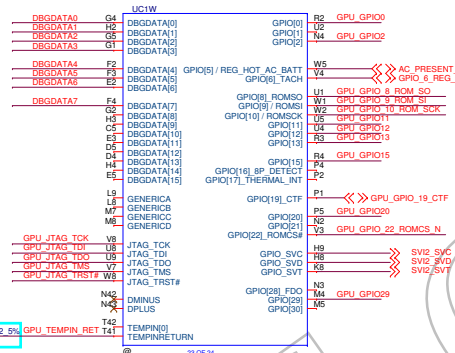




Reserve SPI ROM only for Pre EVT,EVT. DVT1 remove DGPU ROM.

SPI ROM FOR GPU (2MBit)





dGPU Pin Straps

Table 1-57. dGPU Pin Straps

Signal Name	Description	dGPU Default	Recommended settings[1]
111 DBGDATA[2] DBGDATA[1] DBGDATA[0]	Determine the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the GPU itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. 111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable	0 (Internal pull-down)	1: Pull up 5.1kΩ resistor to V_{DDIO_18}/V_{DDAN_18}. 0: Pull down 5.1kΩ resistor to GND. both for each pin
000 DBGDATA[5] DBGDATA[4] DBGDATA[3]	Provides an option to specify certain board-level specifics to the VBIOS or driver. If a board needs certain customized parameters to pass over to vBIOS/driver during boot up, they can use these three balls to generate a data pattern for AMD to react. Have footprints of pull-ups to V_{DD_18}/V_{DDAN_18} on the balls if this usage is required. Footprints of pull-downs to GND are optional since GPU defaults these balls to GND if without pull-ups. Can be left NC if the feature is not needed.	0 (Internal pull-down)	1: Pull up resistor to VDDIO_18/VDDAN_18. 0: Pull down resistor to GND. both for each pin
01 DBGDATA[7] DBGDATA[6]	Provide a strap option to change the SMBUS slave address of the GPU. 00: 0×40 01: 0×41 10: 0×42 11: 0×43	00 (Internal pull-down)	Design dependent Provide a pull-up resistor option to V_{DD_18}. on the PCB for each pin. Strap on the PCB the address **to 0×41** if it does not cause address conflict on the platform.
1 GPIO[2]	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported	1 (Internal pull-up)	Pull-up resistor to V_{DD_33} is optional and should DNI for designs that do not support PCIe Gen3 speed. Provide a pull-down resistor to GND for designs that do not support Gen3 speed.
0 GPIO[15]	Reserved	0 (Internal pull-down)	Must default to 0 for production. Provide a pull-up resistor option to V_{DD_33}. on the PCB for each pin

Note: 1) To change the straps from the default values, use pull-up or pull-down resistors of 5.1K Ω (5%) on the PCB.

Table 1-45. dGPU Serial Flash Interface

Signal Name	Description	Dir.	Buffer Type	Link Type	
1 GPIO[8]_ROMSO	PD-reset. Serial-ROM input to ROM, or GPIO if ROM is not used. Also pin strap at power up. 1: The CLKREQ# power management capability is enabled. Install a pull-up 5.1 kΩ resistor to V_{DD_33} only for designs that support CLKREQ#. 0: The CLKREQ# power management capability is disabled. dGPU default. Pull-down 5.1 kΩ resistor to GND is optional and should DNI for designs that support CLKREQ#.	I	TBD	SE	1, Ext. PU
GPIO[9]_ROMSI	PD-reset. Serial-ROM input to ROM, or GPIO if ROM is not used. Also pin strap at power up. 1: Pull up 5.1 kΩ resistor to V_{DD_33}. Have a footprint of pull up resistor to V_{DD_33}. DNI for normal operation 0: Pull down 5.1 kΩ resistor to GND. GPU default. Pull-down resistor to GND is optional	O	TBD	SE	Serial-input to ROM
GPIO[10]_ROMSCK	PD-reset. Serial-ROM clock to ROM, or GPIO if ROM is not used.	O	TBD	SE	Seria
1 GPIO[22]_ROMCS#[2]	BIOS-ROM chip select for an external serial-ROM device. Used to enable the ROM for ROM read and program operations. Or GPIO if ROM is not used. Also used as pin strap at power up.	O	TBD	SE	1, Ext. PU

— For designs that have a dedicated ROM device for the GPU video BIOS use the GPU default strap on GPIO_22_ROMCS# (i.e '1').
— Connect to Data input of the external ROM through a series 33 Ω resistor

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Title: CPU(1/8) CMC,JTAG,Straps			
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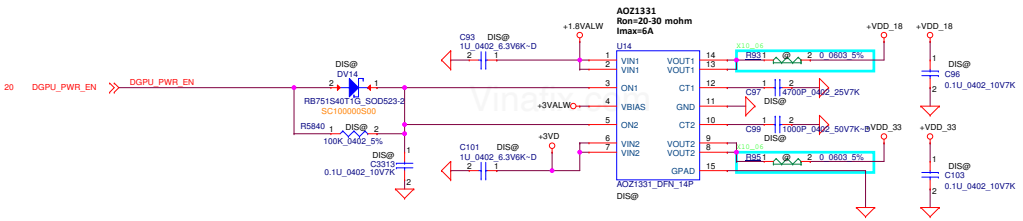
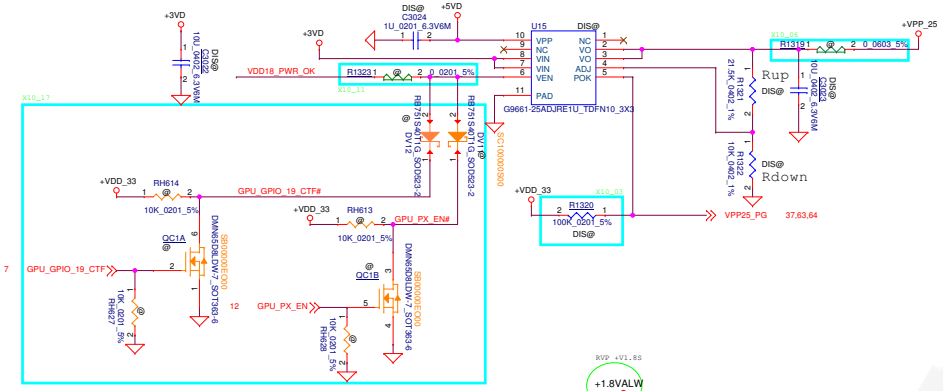
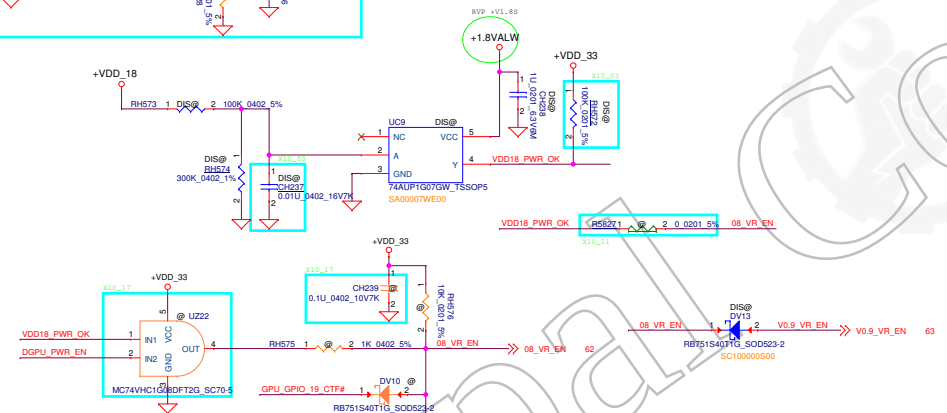
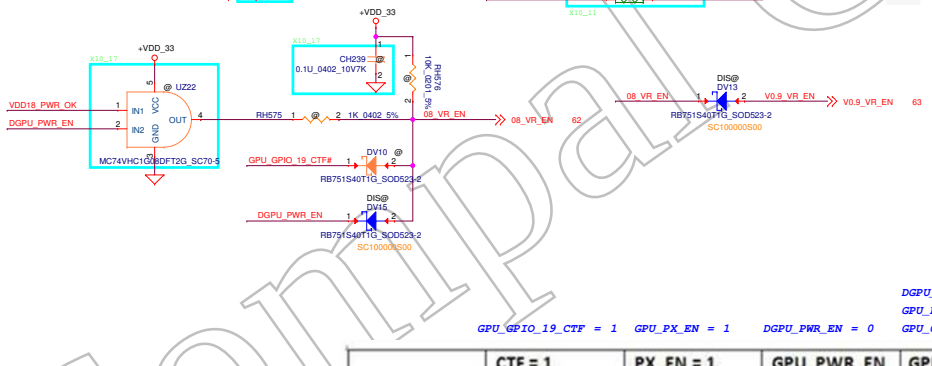
1.8V_ DGPU /3.3V__DGPU Load Switch



dGPU_VPP 2.5V Load Switch



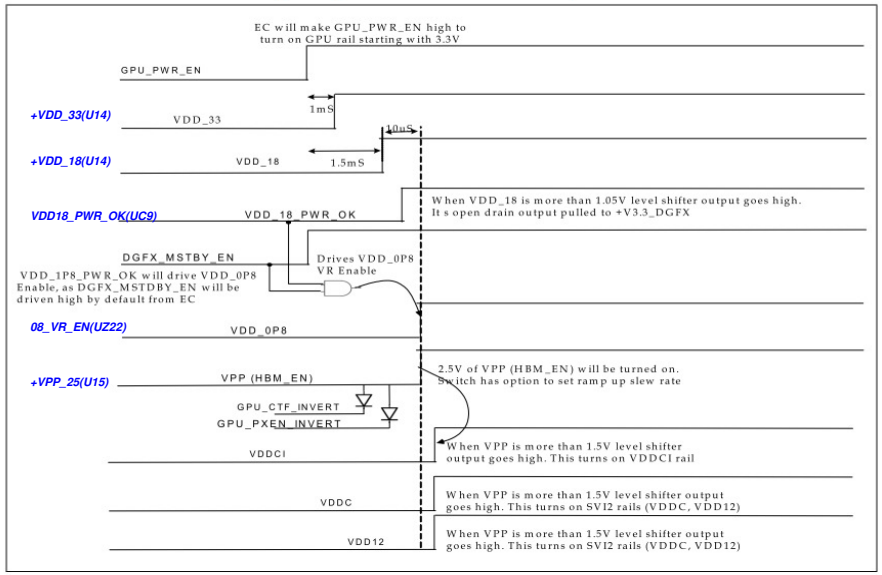




GPU_GPIO_19_CTF = 1 *GPU_PX_EN = 1* *DGPU_PWR_EN = 0* *GPU_GPIO_19_CTF = 0*

	CTF = 1	PX_EN = 1 (BACO)	GPU_PWR_EN = 0 (HG)	GPU_PWR_EN = 1, PX_EN = 0, CTF = 0 (GPU ON)
VDDC	OFF	OFF	OFF	ON
VDDCI	OFF	OFF	OFF	ON
VDD12	OFF	OFF	OFF	ON
VPP	OFF	OFF	OFF	ON
0.8V	OFF	ON	OFF	ON
1.8V	ON	ON	OFF	ON

Figure 42-17.KBL G dGFX Module Timing Diagram for Power ON Sequence



Reference 571726_KBL_G_MOW_WW12_2017.pdf

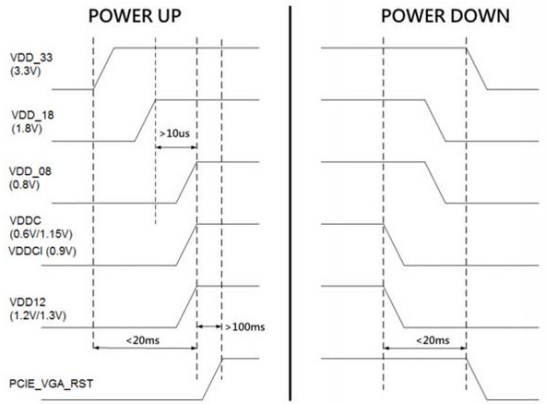
GPU

- KBL G GPU Module Timing Diagram Update:

The following requirements should be met with regards to power-supply sequencing to avoid damaging the GPU:

1. All GPU supplies except for VDD_33, must fully reach to their nominal values within 20ms from start of ramp up sequence. The maximum slew rate on all rails is 50 mV/µs.
2. It is recommended VDD_33 ramps up first.
3. VDD_18 must reach its steady state at least 10us before other rails VDD_0P8, VDD_0P9, VDD12, VDDC, VDDCI, VPP start to ramp up.

POWER UP / POWER DOWN SEQUENCE



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Title	PROCESSOR(7/7) VSS		
Size	Document Number		Rev
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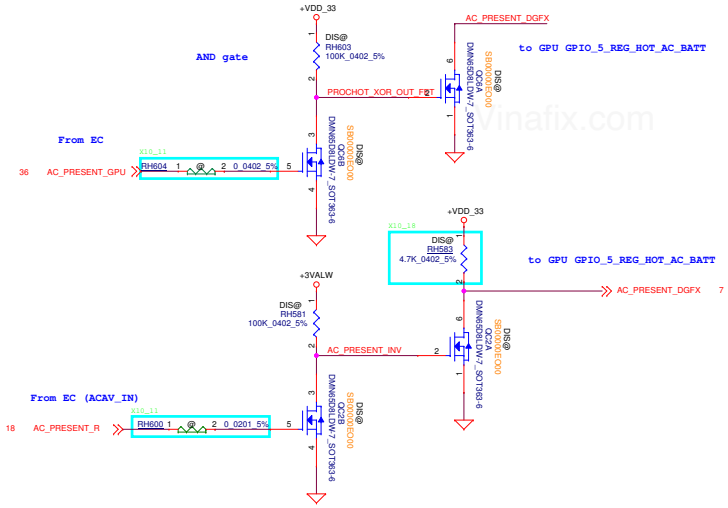
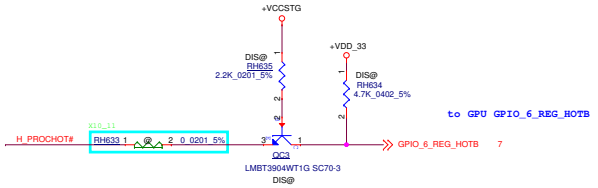
Reference RVP:571538_KBL_G_RVP_DDR4_Sch_Rev0p71.pdf



An input which allows the system to request a fast power reduction by setting GPIO_5_REG_HOT_AC_BATT to low (0V).
The resulting state transition may disturb the display momentarily.
This pin can be used for:
1-Battery protection on notebooks when AC power supply is suddenly removed. In this usage,
the GPU will first be forced to the lowest DPM level of AC state then moved to battery state Or
2-Other critical graphics/platform event that requires immediate power reduction on GPU.

For example, voltage regulator overheating and over power/current on the platform.
In this usage, the GPU will be forced to the lowest DPM level of AC state until the event disappears after
which normal DPM switching will be re-enabled.

If both protection methods are required on the same platform, use GPIO_5 for battery protection and GPIO_6 for the other protection event.



Used as alternate input for VR_HOT if GPIO[5] is used for AC/DC switch protection
Implement footprint for pull up 10KΩ resistor to VDD_33

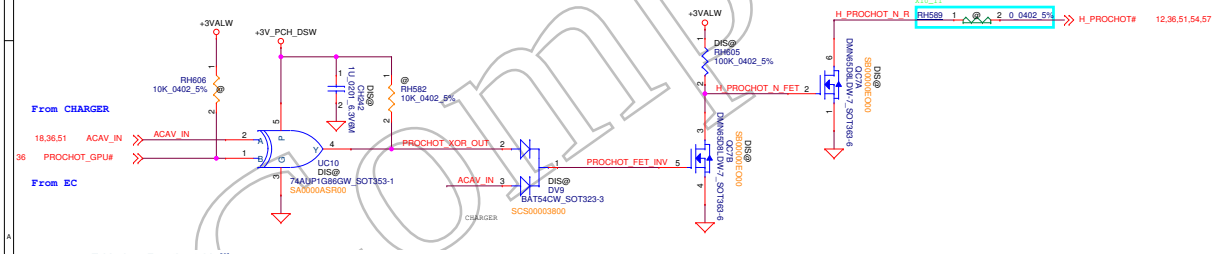
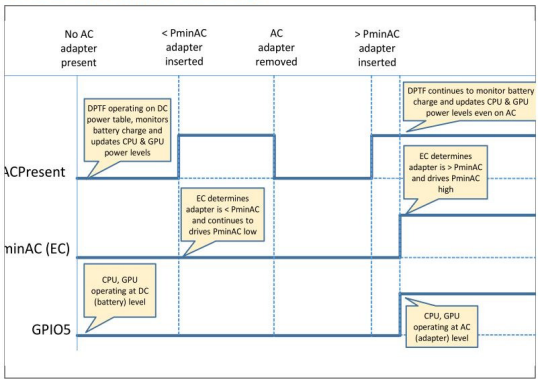


Table 4: Function table [1]

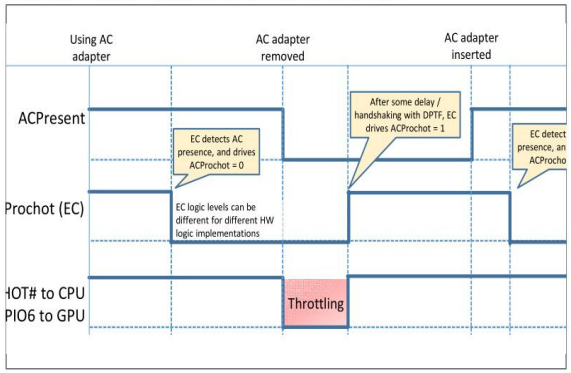
Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

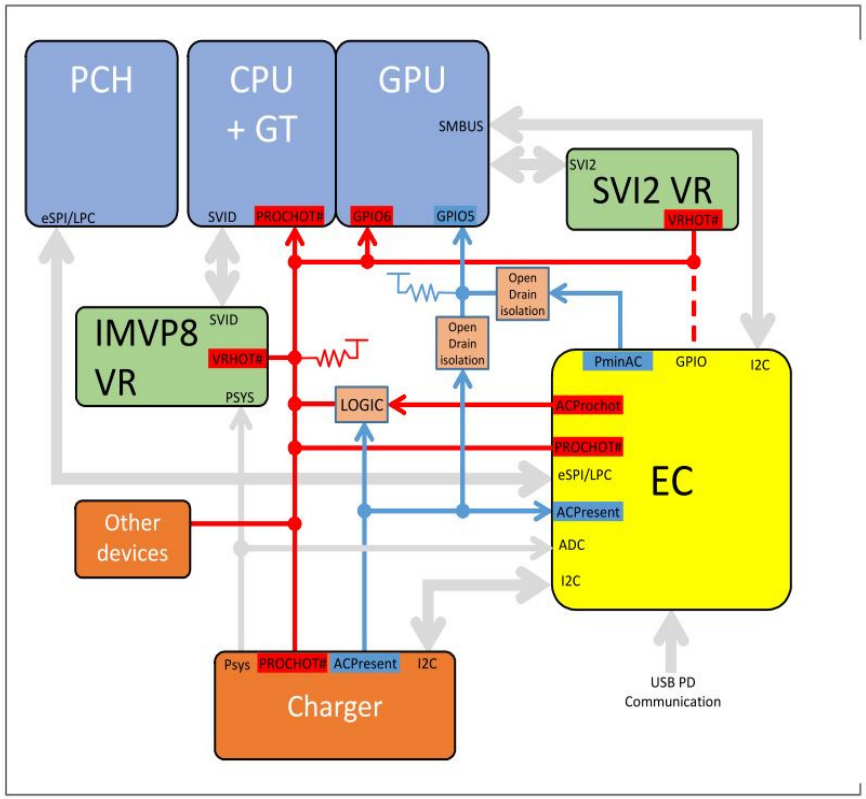
GPIO5 Behavior with AC State Change



PROCHOT# and GPIO6 Behavior with AC State Change



Hardware Power Source Protection Diagram



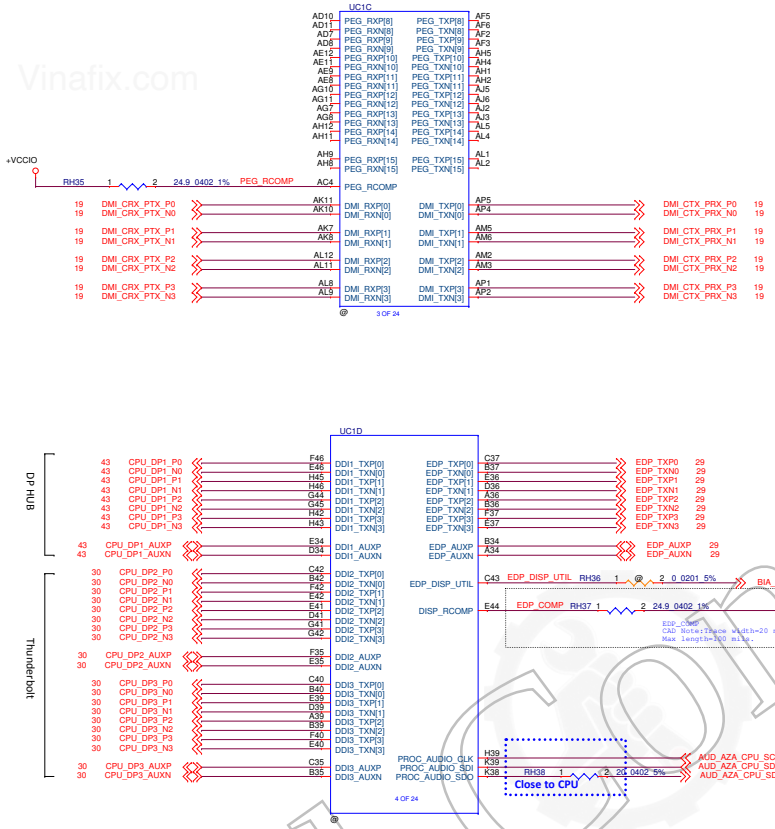
Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: DGPU PWR Management

Size | Document Number: LA-F211P | Rev: 1.0(A00)

Date: Thursday, January 11, 2018 | Sheet 9 of 71



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Title: CPU(2/8) DMI,DDI,EDP

Size	Document Number	Rev
Custom	LA-F211P	1.0(A00)

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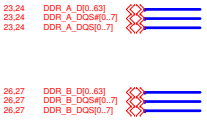
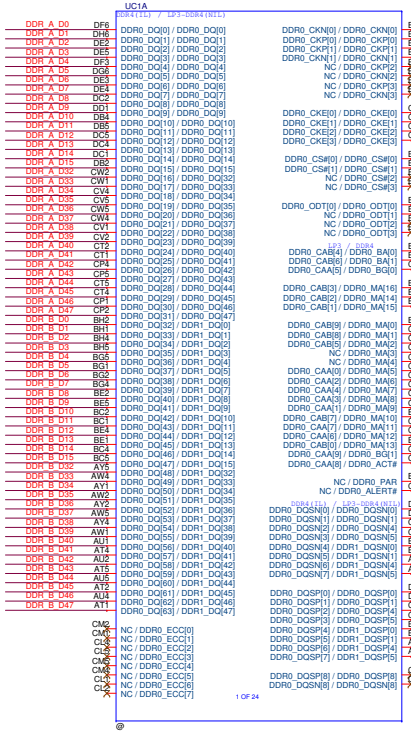
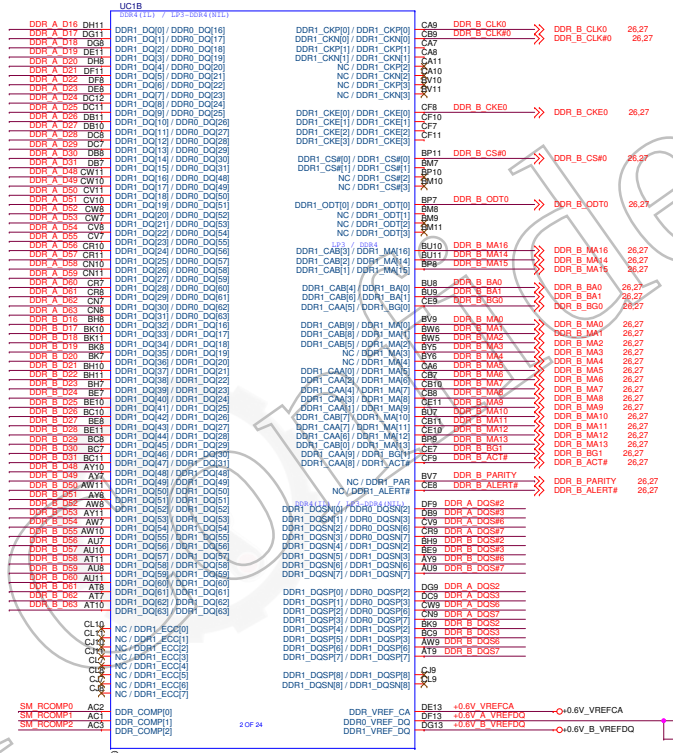
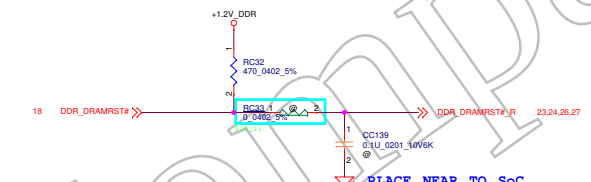
Non-Interleave for DDR4









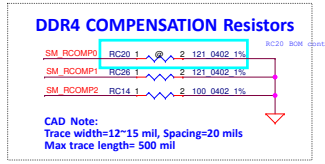


Table 4-9. KBL-G DDR4 1Rx16 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)			Max (mils) Length			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group[1&2] Byte [1&2]	Region	Breakout	Total		

Notes:

1. Avoid any parallel routing between two adjacent layers. When parallel routing can not be avoided in the CPU Break Out, it is recommended to offset the signals from two adjacent layers so no direct overlap occurs. If needed, the total parallel routing length in the CPU Break Out, which includes both overlapped and offset parallel routing, must be 300 mils or less.
2. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
3. Use individual termination resistors (R1) for each signal. Don't use Rpacks
4. For Option #1 (Single Rank) configuration there are only 8 DRAM Devices connected to each CMD Group Signal and only 1 DRAM Device connected to each Strobe/Data Group Signal. For these designs DRAM Devices [15:8] and their corresponding BI1 routing segments need to be removed for each CMD Group Signal and the second DRAM Device and corresponding BI routing segment needs to be removed for each Strobe/Data Group Signal.
5. The Strobe and Data Group Signals within the same byte must always route together on the same layers for their entire route
6. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
7. Clock (CLK and CLK≠) and Strobe (DQS and DQS≠) differential signal swapping within a pair is not allowed
8. Capacitor C1 is a defensive design and should be NO STUFF by default
9. DQ and DQS signals must route at the same layer and have same width
10. Route 2 adjacent bytes to same DRAM device - like DRAM0(BYTE0,1) DRAM1 (BYTE 2,3),,, for better VREF training per DRAM device.
11. Impedance numbers are for reference only, it is calculating according to the stackup layers thickness, the material conductivity, traces spacing and width. The recommendation is to follow stackup and traces geometries.
12. RCOMP[0] value for SDP is 200+/-1% ohm, and for DDP is 121+/- 1% ohm.

Security Classification	Compal Secret Data	
Issued Date	2017/04/07	Deciphered Date 2018/12/31

Title: CPU(3/8) DDRIV

Size	Document Number	Rev
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CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted

CFG0	★ 1 = (Default) Normal Operation; No stall. 0 = Stall.

Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps

CFG[6]	0 : 2x4 PCI Express* ★ 1 : 1x8 PCI Express*

PEG DEFER TRAINING

CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG[5]: Should be set to 0

CFG[2]: Should be set to 1

Follow 570766_KBL_G_EDS_Vol_1_Rev0_7.pdf

CAD NOTE: PLACE ALL RESISTORS ON THIS PAGE NEAR CPU

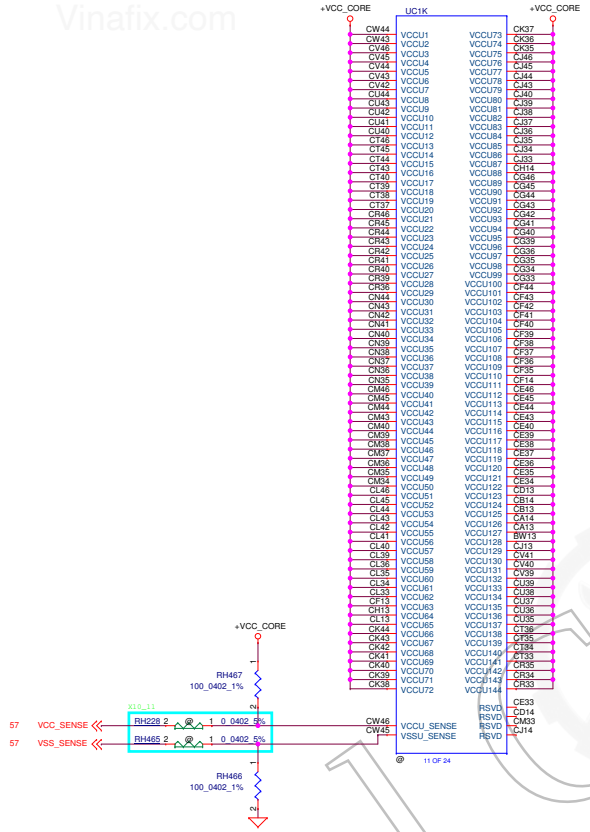
To power regulator RVP PU to +V3.3_DGPX Currently double PU to +3VS, need confirm!

Level shift

SMBUS CONNECTION TO EC FOR THERMAL MONITORING OF GPU PU PRESENT ON I2C_GPU_SCL/DAT

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Title	CPU(4/8) RSVD,CFG,DGPU	
Size: D	Document Number: LA-F211P	Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 12 of 71	



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Title: CPU(5/8) PWR

Size	Document Number	Rev
Custom	LA-F211P	1.0(A00)

Date: Thursday, January 11, 2018 Sheet 13 of 71

12/25
Change 22uF X6S 0603 (SE00001CA00) to 22uF X5R 0603 (SE00000M000)* 2.

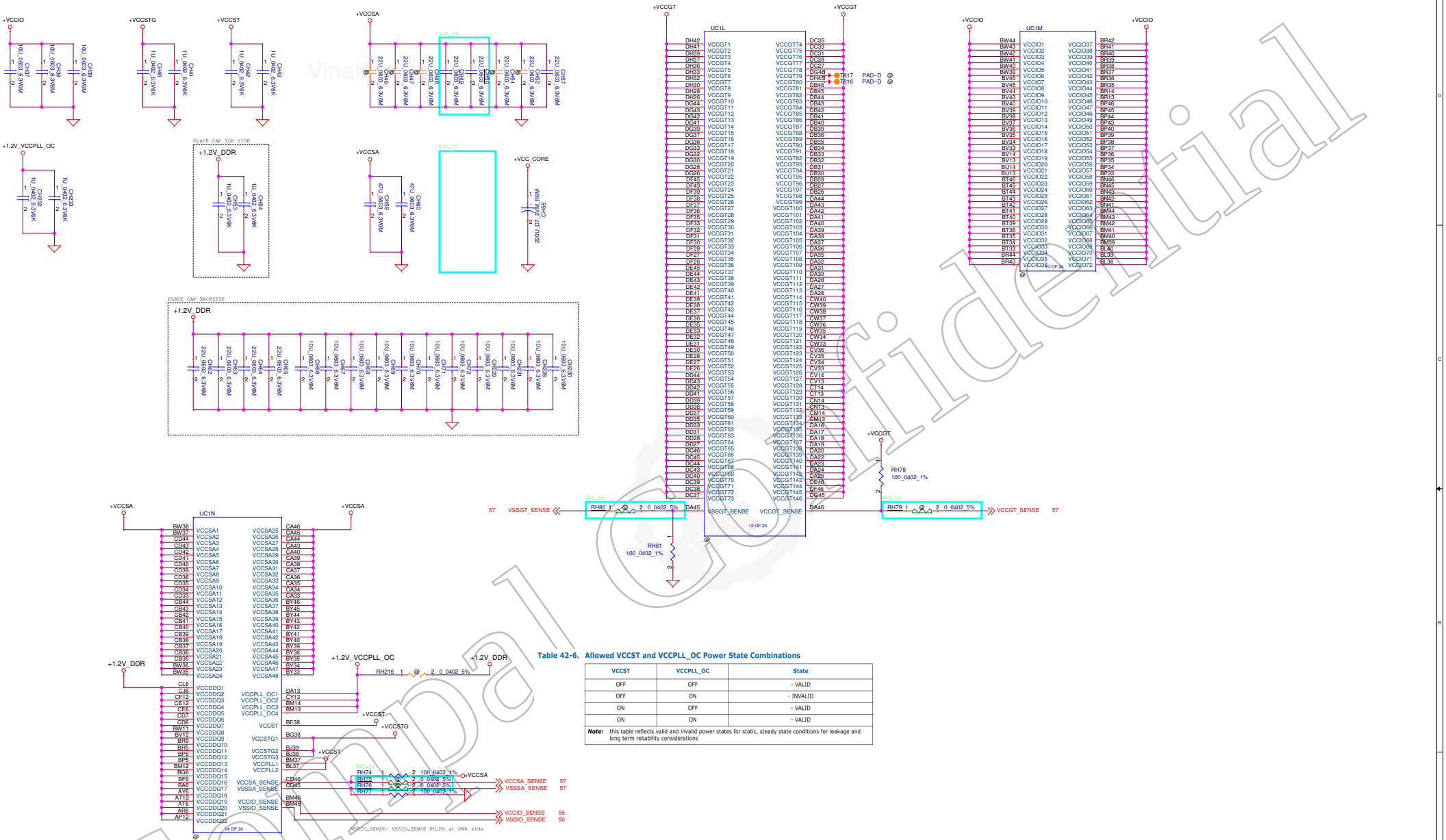


Table 42-6. Allowed VCCST and VCCPLL_OC Power State Combinations

VCCST	VCCPLL_OC	State
OFF	OFF	- VALID
OFF	ON	- INVALID
ON	OFF	- VALID
ON	ON	- VALID

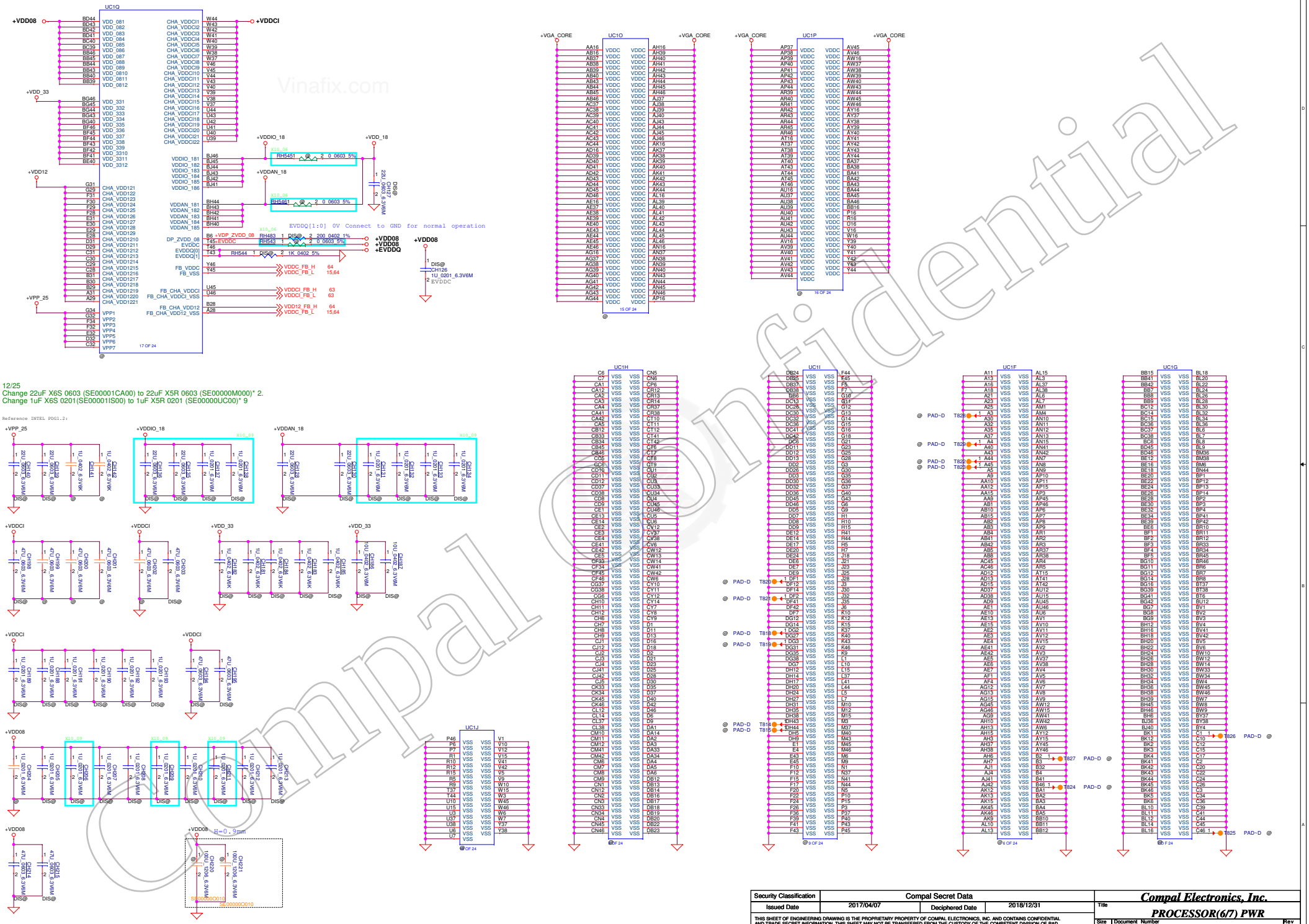
Note: this table reflects valid and invalid power states for static, steady state conditions for leakage and long term reliability considerations

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Title: CPU(6/8) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-F211P	1.0(A00)

Date: Thursday, January 11, 2018 Sheet 14 of 71



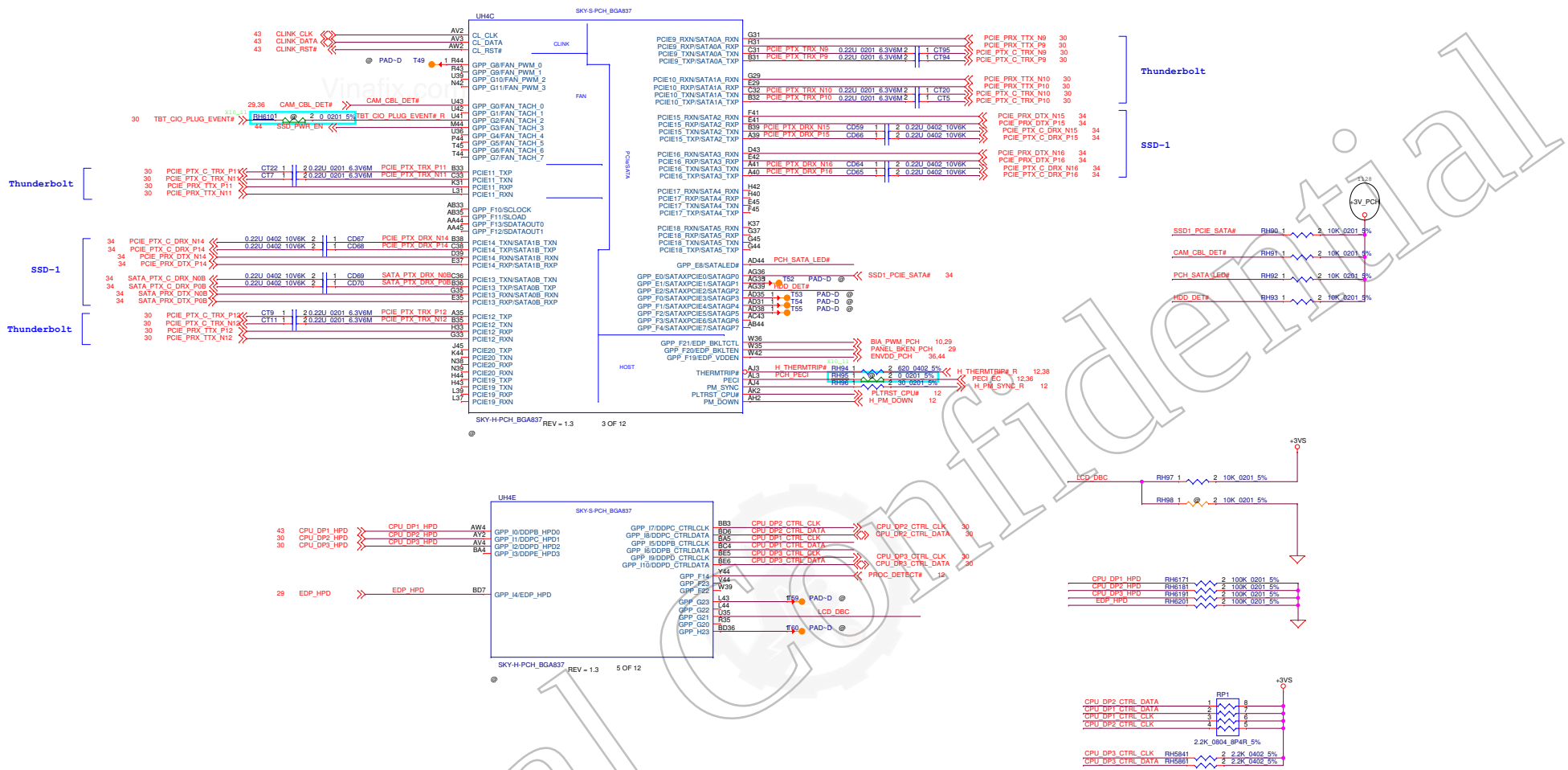
Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
	LA-F211P	1.0(A00)

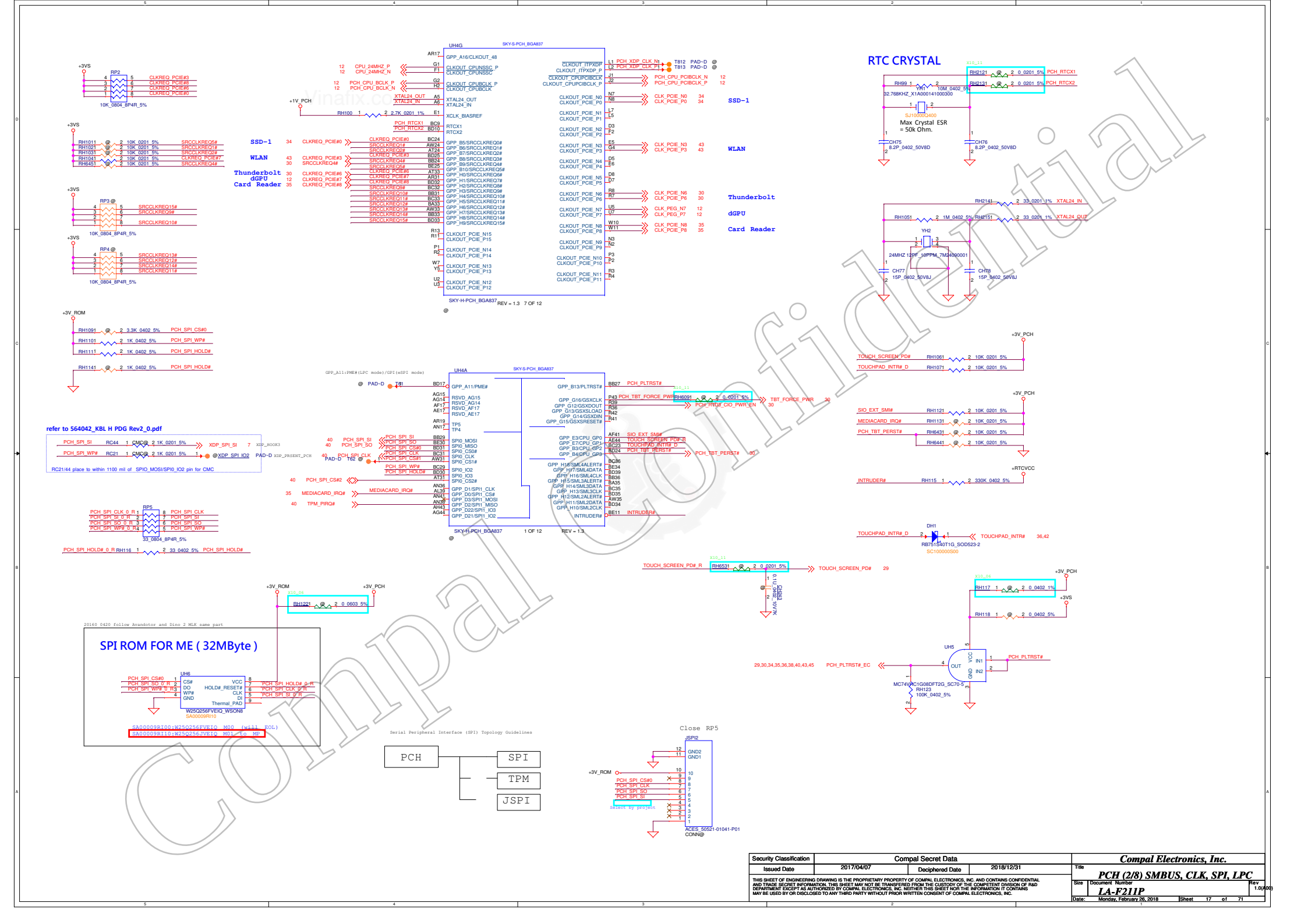
Date: Thursday, January 11, 2018 | Sheet 15 of 71



Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: PCH (1/8) SATA,HDA			
Size	Document Number: LA-F211P		Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 16 of 71		



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Issued Date	2017/04/07	Deciphered Date	2018/12/31

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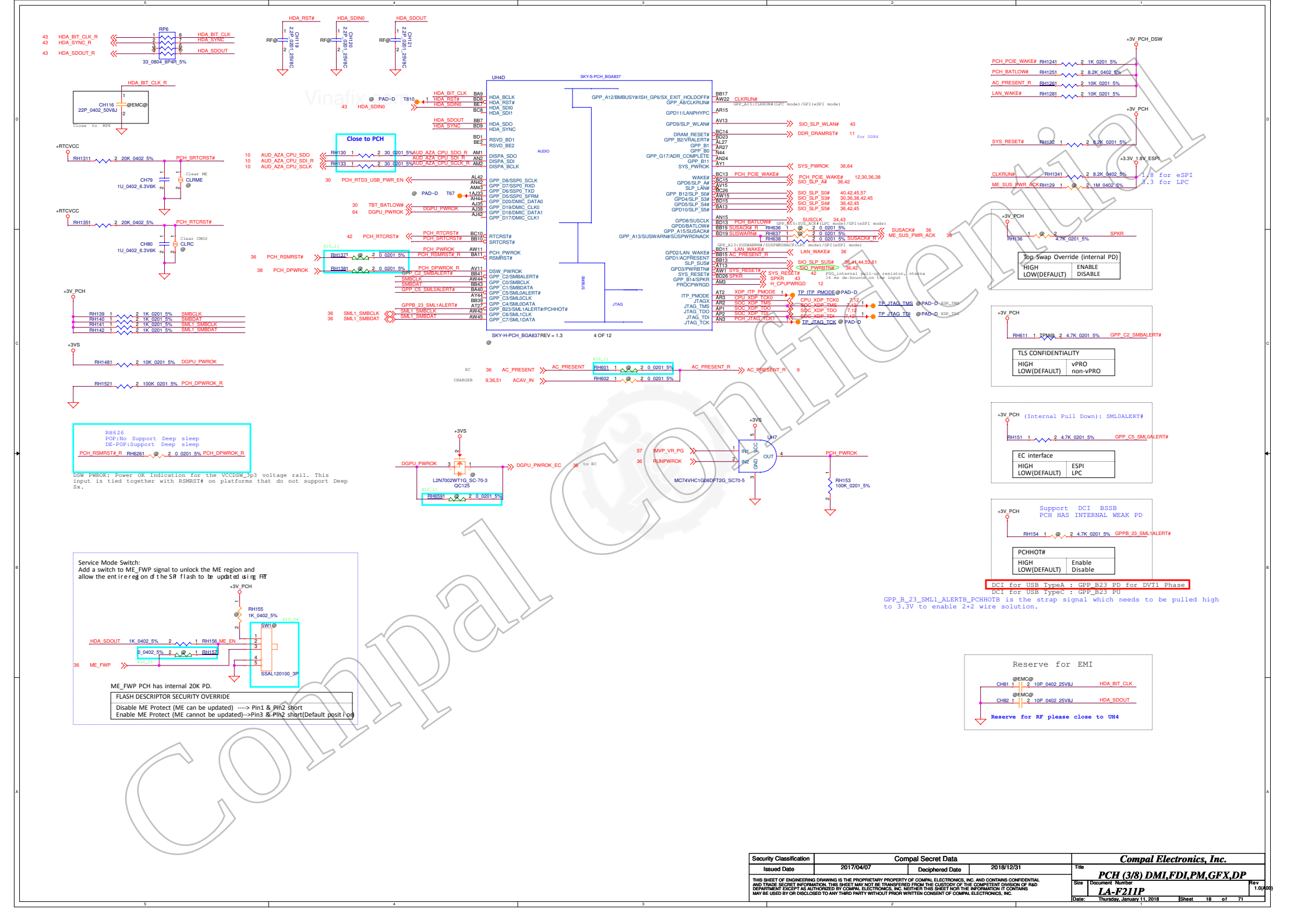
Compal Electronics, Inc.

Title: PCH (2/8) SMBUS, CLK, SPI, LPC

Size: | Document Number: LA-F211P | Rev: 1.0(A00)

Date: Monday, February 26, 2018 | Sheet 17 of 71



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Issued Date	2017/04/07	Deciphered Date	2018/12/31

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Compal Electronics, Inc.	
Title	PCH (3/8) DMI,FDI,PM,GFX,DP
Size	Document Number: LA-F211P
Rev	1.0(A00)
Date:	Thursday, January 11, 2018
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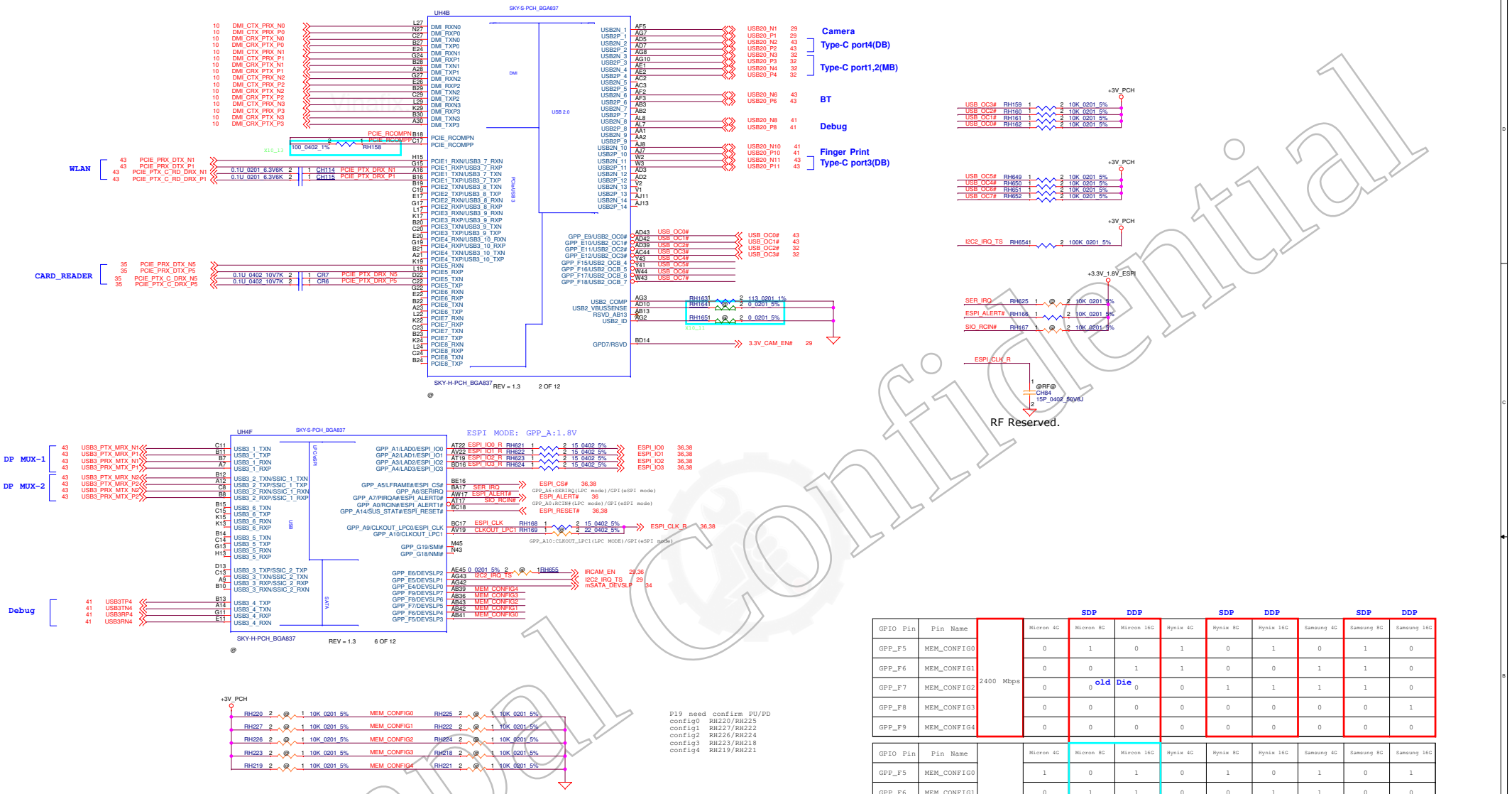

GPIO Pin	Pin Name		SDP Micron 4G	SDP Micron 8G	DDP Micron 16G	SDP Hynix 4G	SDP Hynix 8G	DDP Hynix 16G	SDP Samsung 4G	SDP Samsung 8G	DDP Samsung 16G
GPP_F5	MEM_CONFIG0	2400 Mbps	0	1	0	1	0	1	0	1	0
GPP_F6	MEM_CONFIG1		0	0	1	1	0	0	1	1	0
GPP_F7	MEM_CONFIG2		0	0	old Die 0	0	1	1	1	1	0
GPP_F8	MEM_CONFIG3		0	0	0	0	0	0	0	0	1
GPP_F9	MEM_CONFIG4		0	0	0	0	0	0	0	0	0

GPIO Pin	Pin Name		Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_F5	MEM_CONFIG0		1	0	1	0	1	0	1	0	1
GPP_F6	MEM_CONFIG1		0	1	1	0	0	1	1	0	0
GPP_F7	MEM_CONFIG2		0	0	new Die 0	1	1	1	1	0	0
GPP_F8	MEM_CONFIG3		1	1	1	1	1	1	1	0	0
GPP_F9	MEM_CONFIG4		0	0	0	0	0	0	0	1	1

GPIO Pin	Pin Name		Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_F5	MEM_CONFIG0		0	1	0	1	0	1	0	1	0
GPP_F6	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_F7	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_F8	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_F9	MEM_CONFIG4		1	1	1	1	1	1	1	1	1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date 2018/12/31	Title: PCH (4/8) PCI, USB
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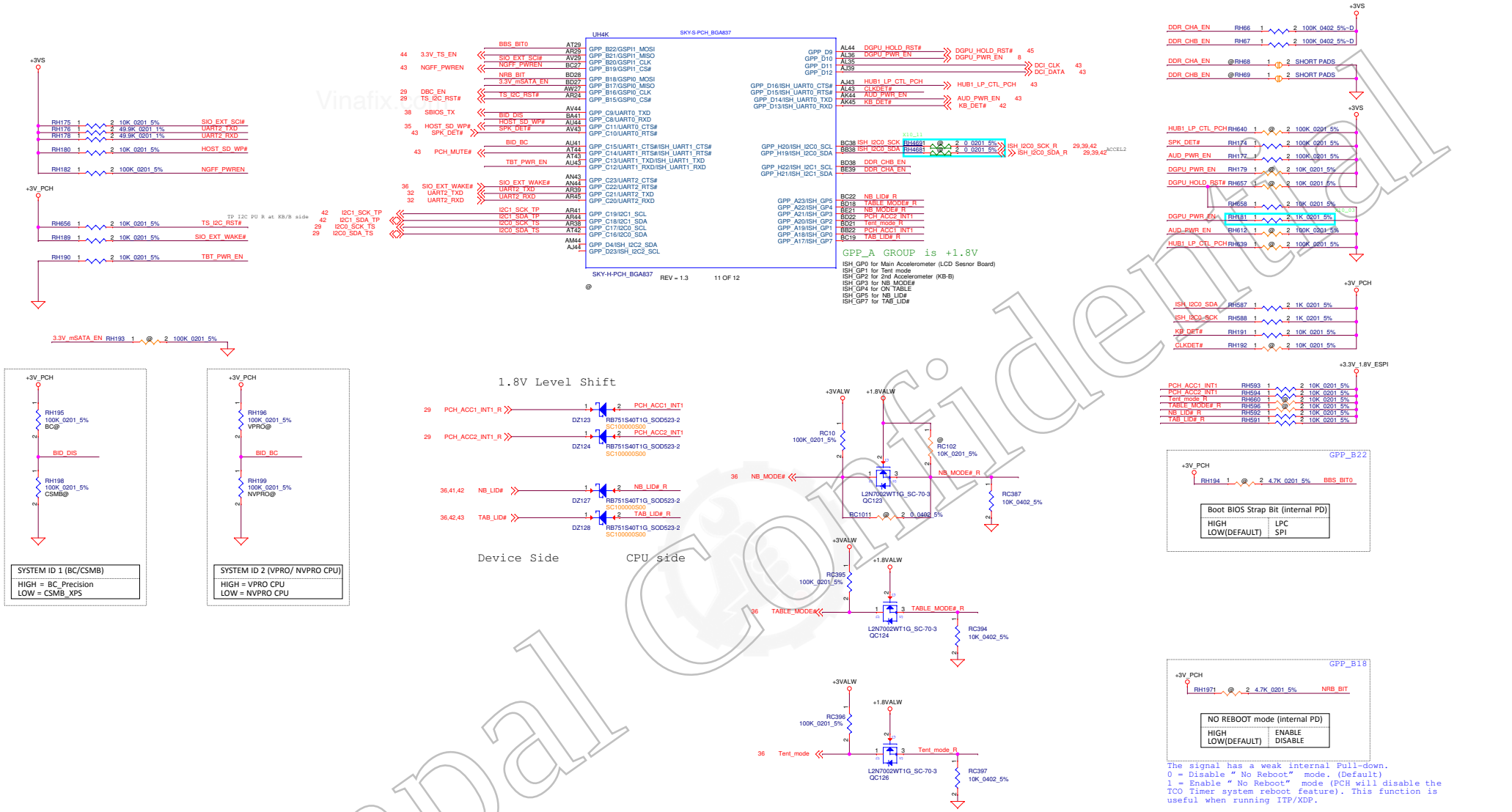
			Date: Thursday, January 11, 2018 Sheet 19 of 71



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title	PCH (5/8) GPIO, CPU, MISC		
Size	Document Number		Rev
	LA-F211P		1.0(A00)
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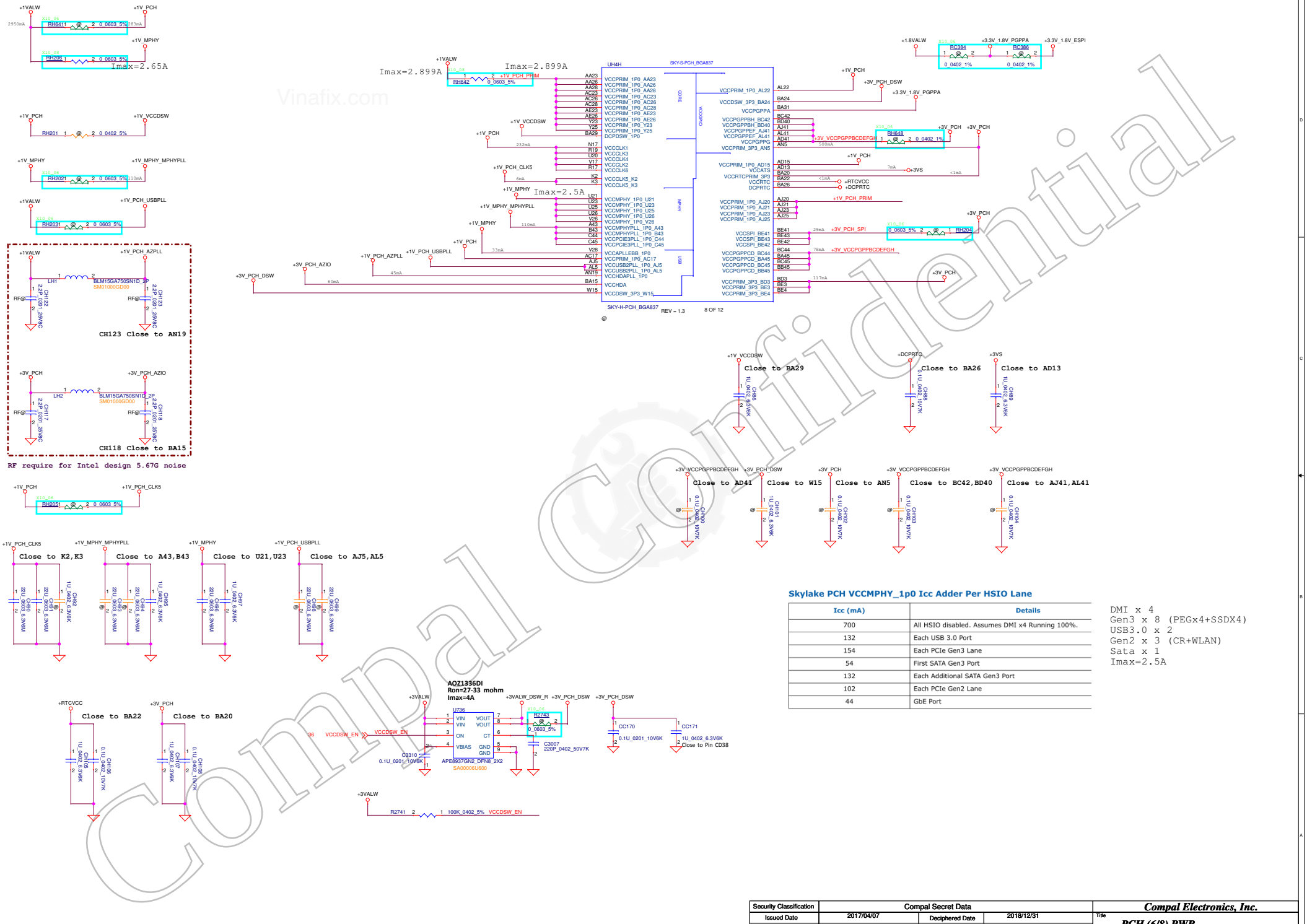

Skylake PCH VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (mA)	Details
700	All HSIO disabled. Assumes DMI x4 Running 100%.
132	Each USB 3.0 Port
154	Each PCIe Gen3 Lane
54	First SATA Gen3 Port
132	Each Additional SATA Gen3 Port
102	Each PCIe Gen2 Lane
44	GbE Port

DMI x 4
Gen3 x 8 (PEGx4+SSDX4)
USB3.0 x 2
Gen2 x 3 (CR+WLAN)
Sata x 1
Imax=2.5A

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.	
Title	PCH (6/8) PWR
Size	Document Number: LA-F211P
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Date:	Thursday, January 11, 2018
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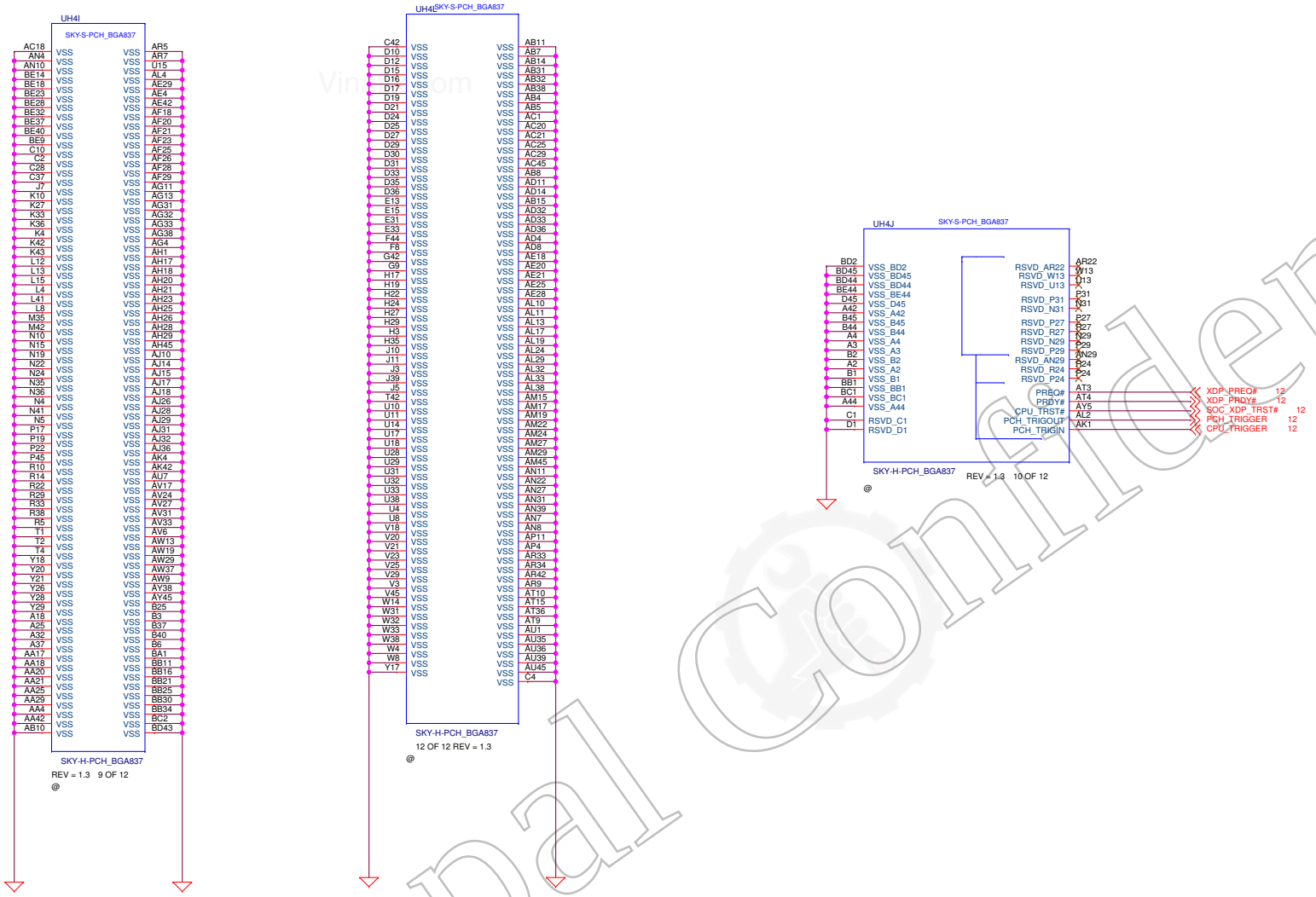

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.		
Title: PCH (8/8) VSS		
Size	Document Number: LA-F211P	Rev: 1.0(A00)
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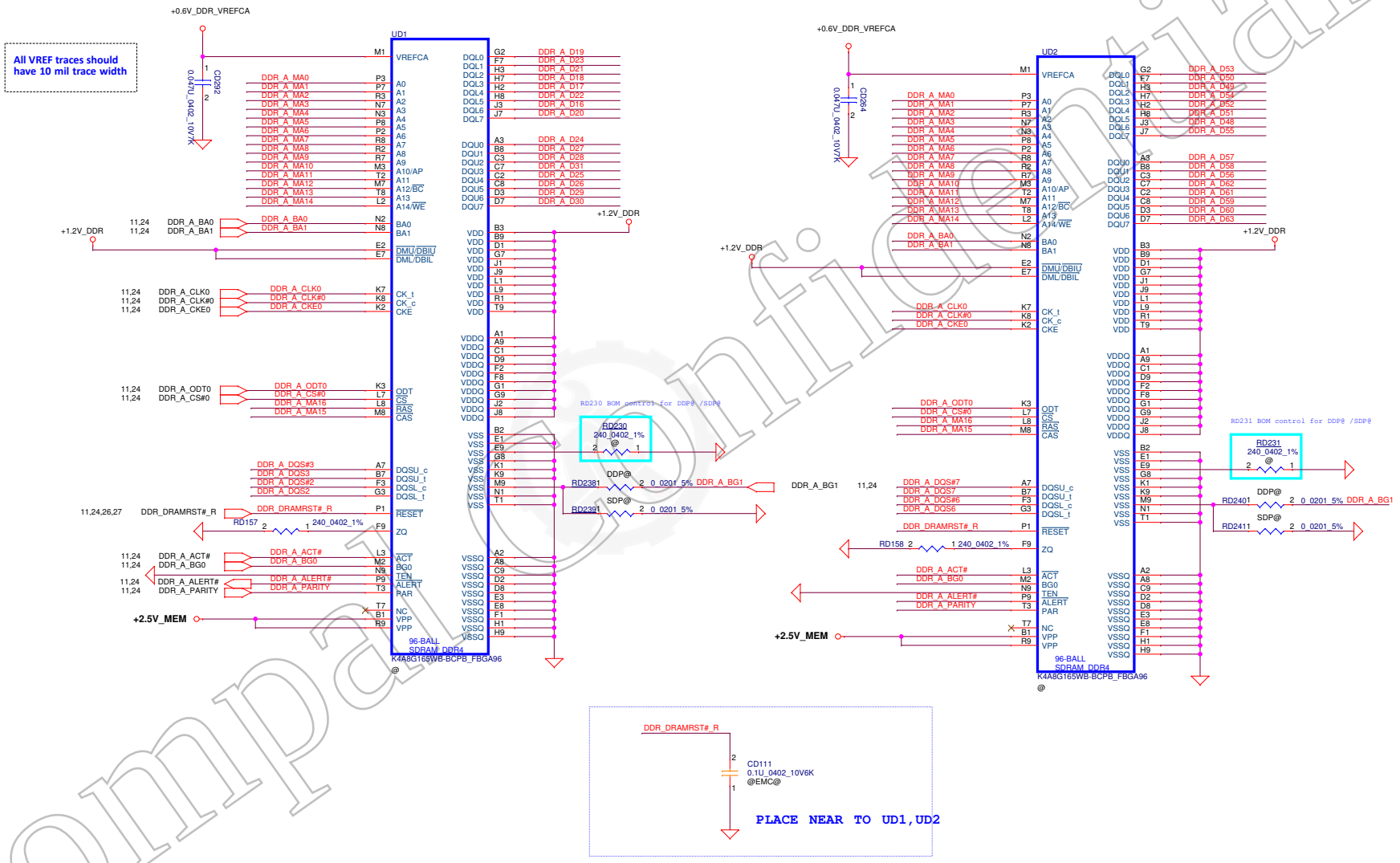
DDR4 Memory Down_CHA

Non-Interleave Memory



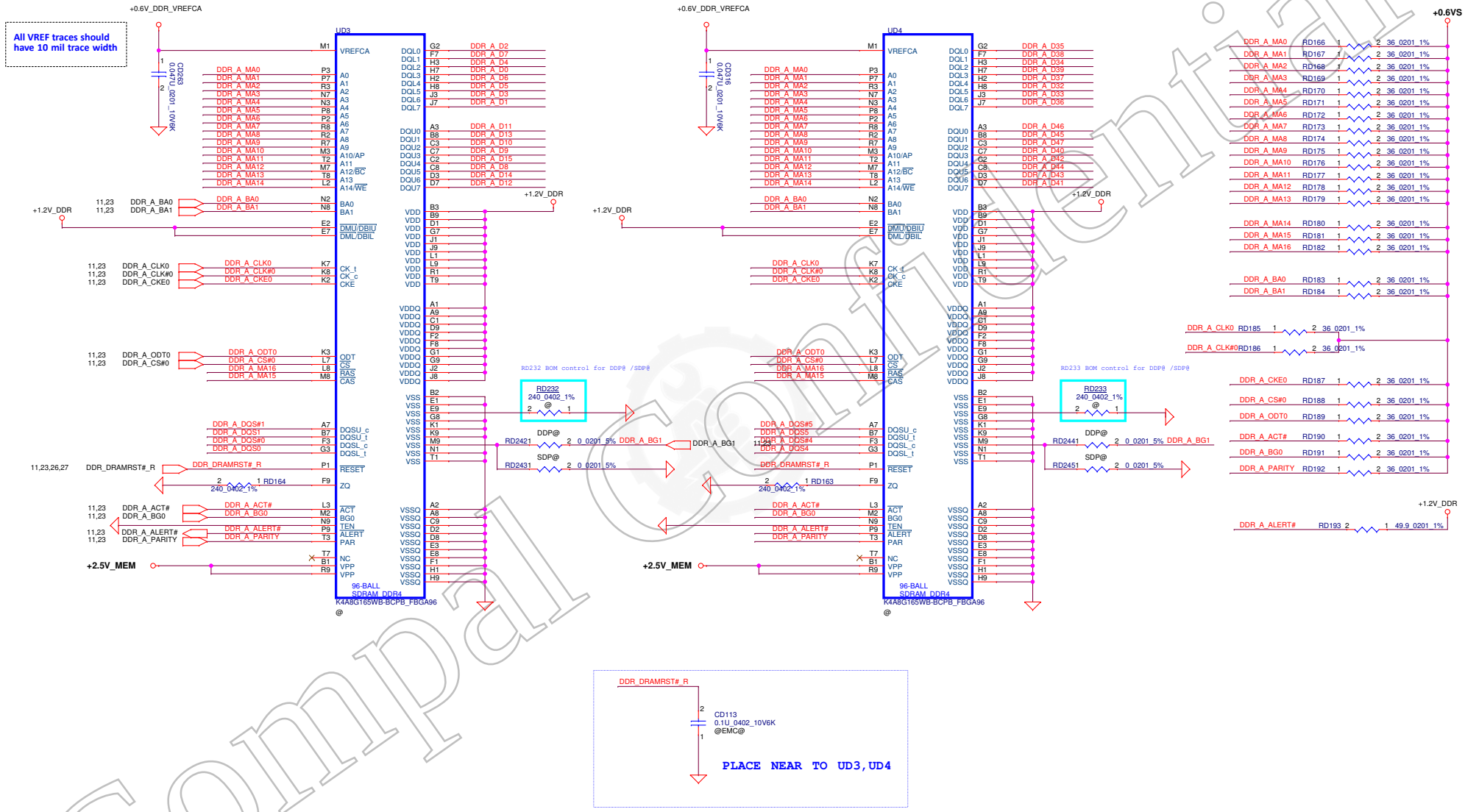
Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: DDR4 Memory Down_CHA			
Size: Custom	Document Number: LA-F211P		Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 23 of 71		

DDR4 Memory Down_CHA

Non-Interleave Memory

11,23 DDR_A_MA[0..16]
11,23 DDR_A_DQS[0..7]
11,23 DDR_A_DQS#[0..7]
11,23 DDR_A_D[0..63]

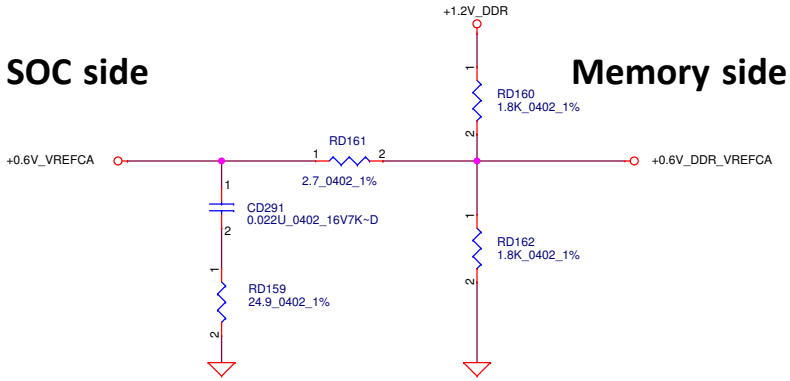


Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

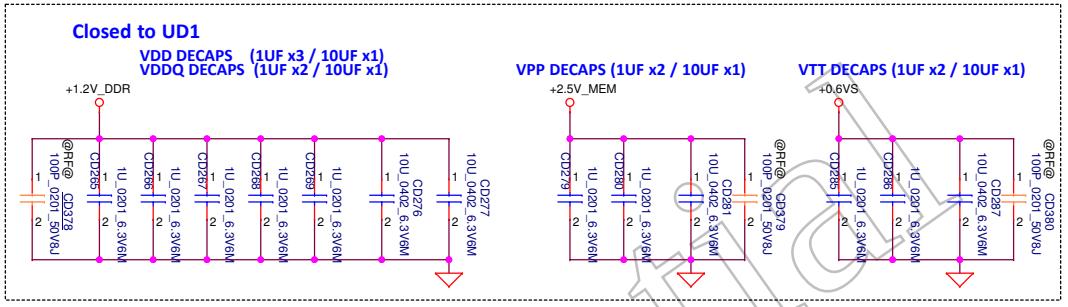
Compal Electronics, Inc.			
Title: DDR4 Memory Down_CHA			
Size: Custom	Document Number: LA-F211P		Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 24 of 71		

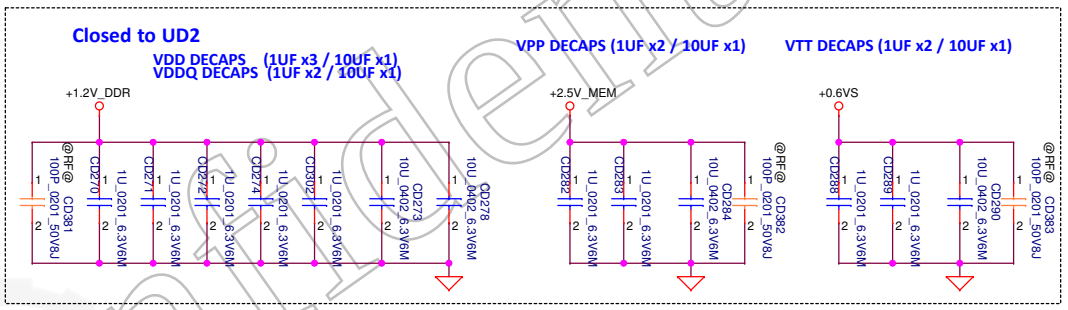
DDR4 Memory Down_CHA

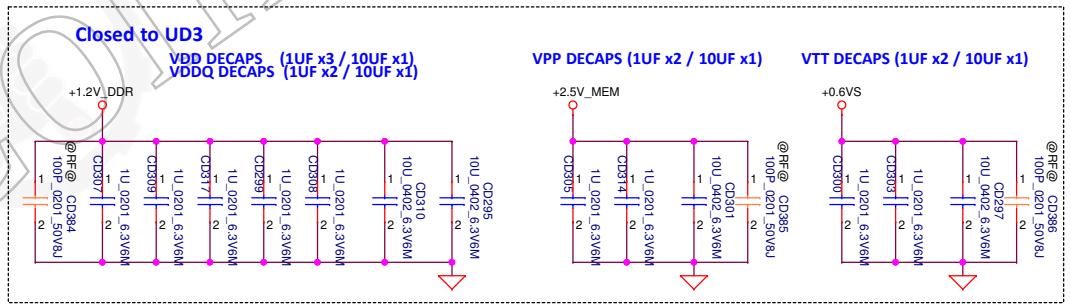
Non-Interleave Memory

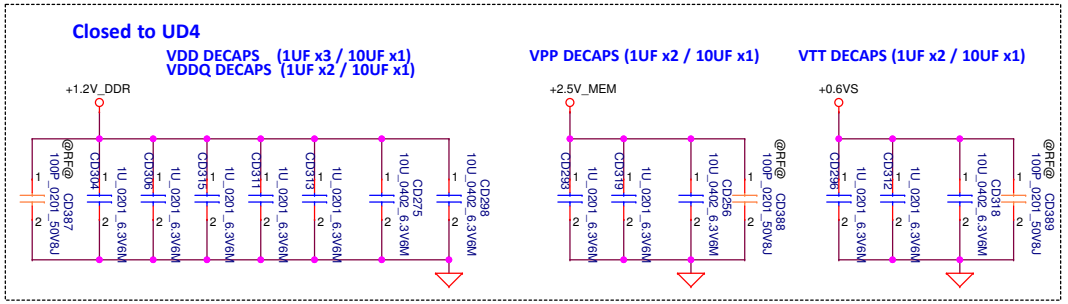


VREF traces should be at least 20 mils wide
with 20 mils spacing to other signals/planes.









Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: DDR4 VREF/DECAPS CHA

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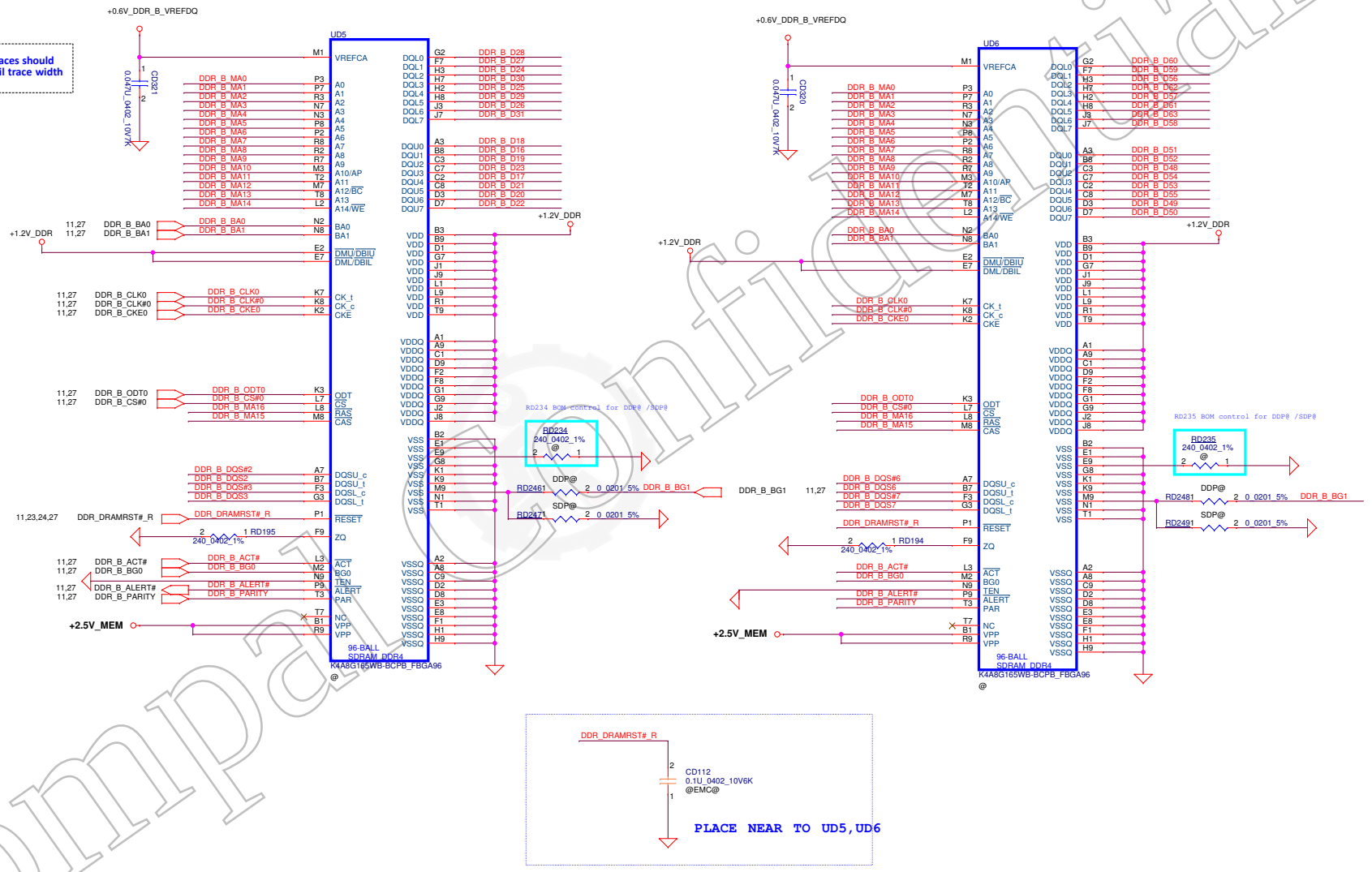
DDR4 Memory Down_CHB

Non-Interleave Memory

11,27 DDR_B_MA[0..16]
11,27 DDR_B_DQS[0..7]
11,27 DDR_B_DQS#[0..7]
11,27 DDR_B_D[0..63]

All VREF traces should have 10 mil trace width



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: DDR4 Memory Down_CHB			
Size: Custom	Document Number: LA-F211P		Rev: 1.0(A00)
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DDR4 Memory Down_CHB

Non-Interleave Memory

11,26 DDR_B_MA[0..16]
11,26 DDR_B_DQS[0..7]
11,26 DDR_B_DQS#[0..7]
11,26 DDR_B_D[0..63]

All VREF traces should have 10 mil trace width

+0.6V_DDR_B_VREFDQ

CD323 0.047U_0201_10V6K

UD7

M1 VREFCA

DDR_B_MA0 P3 A0
DDR_B_MA1 P7 A1
DDR_B_MA2 R3 A2
DDR_B_MA3 N7 A3
DDR_B_MA4 N3 A4
DDR_B_MA5 P8 A5
DDR_B_MA6 P2 A6
DDR_B_MA7 R8 A7
DDR_B_MA8 R2 A8
DDR_B_MA9 R7 A9
DDR_B_MA10 M3 A10/AP
DDR_B_MA11 T2 A11
DDR_B_MA12 M7 A12/BC
DDR_B_MA13 T8 A13
DDR_B_MA14 L2 A14/WE

11,26 DDR_B_BA0 N2 BA0
11,26 DDR_B_BA1 N8 BA1

E2 DMU/DBIU
E7 DMU/DBIL

11,26 DDR_B_CLK0 K7 CK_t
11,26 DDR_B_CLK#0 K8 CK_c
11,26 DDR_B_CKE0 K2 CKE

11,26 DDR_B_ODT0 K3 ODT
11,26 DDR_B_CS#0 L7 CS
DDR_B_MA16 L8 RAS
DDR_B_MA15 M8 CAS

DDR_B_DQS#0 A7 DQSU_c
DDR_B_DQS0 B7 DQSU_t
DDR_B_DQS#1 F3 DQSL_c
DDR_B_DQS1 G3 DQSL_t

11,23,24,26 DDR_DRAMRST#_R P1 RESET

DDR_DRAMRST#_R — 2 — RD196 240_0402_1% — 1 F9 ZQ

11,26 DDR_B_ACT# L3 ACT
11,26 DDR_B_BG0 M2 BG0
N9 TEN
11,26 DDR_B_ALERT# P9 ALERT
11,26 DDR_B_PARITY T3 PAR

T7 NC
B1 VPP
R9 VPP

+2.5V_MEM

DQL0 G2 DDR_B_D11
DQL1 F7 DDR_B_D13
DQL2 H3 DDR_B_D14
DQL3 H7 DDR_B_D8
DQL4 H2 DDR_B_D12
DQL5 H8 DDR_B_D9
DQL6 J3 DDR_B_D15
DQL7 J7 DDR_B_D10

DQU0 A3 DDR_B_D5
DQU1 B8 DDR_B_D1
DQU2 C3 DDR_B_D7
DQU3 C7 DDR_B_D6
DQU4 C2 DDR_B_D4
DQU5 C8 DDR_B_D3
DQU6 D3 DDR_B_D2
DQU7 D7 DDR_B_D0

+1.2V_DDR

VDD B3, B9, D1, G7, J1, J9, L1, L9, R1, T9
VDDQ A1, A9, C1, D9, F2, F8, G1, G9, J2, J8
VSS B2, E1, E9, G8, K1, K9, M9, N1, T1
VSSQ A2, A8, C9, D2, D8, E3, E8, F1, H1, H9

RD236 BOM control for DDP@ /SDP@

RD236 240_0402_1% @ — 2 — 1

DDP@ RD2501 2 0_0201_5% DDR_B_BG1
SDP@ RD2511 2 0_0201_5%

96-BALL SDRAM_DDR4
K4A8G165WB-BCPB_FBGA96
@

+0.6V_DDR_B_VREFDQ

CD322 0.047U_0201_10V6K

UD8

M1 VREFCA

DDR_B_MA0 P3 A0
DDR_B_MA1 P7 A1
DDR_B_MA2 R3 A2
DDR_B_MA3 N7 A3
DDR_B_MA4 N3 A4
DDR_B_MA5 P8 A5
DDR_B_MA6 P2 A6
DDR_B_MA7 R8 A7
DDR_B_MA8 R2 A8
DDR_B_MA9 R7 A9
DDR_B_MA10 M3 A10/AP
DDR_B_MA11 T2 A11
DDR_B_MA12 M7 A12/BC
DDR_B_MA13 T8 A13
DDR_B_MA14 L2 A14/WE

DDR_B_BA0 N2 BA0
DDR_B_BA1 N8 BA1

E2 DMU/DBIU
E7 DMU/DBIL

DDR_B_CLK0 K7 CK_t
DDR_B_CLK#0 K8 CK_c
DDR_B_CKE0 K2 CKE

DDR_B_ODT0 K3 ODT
DDR_B_CS#0 L7 CS
DDR_B_MA16 L8 RAS
DDR_B_MA15 M8 CAS

DDR_B_DQS#4 A7 DQSU_c
DDR_B_DQS4 B7 DQSU_t
DDR_B_DQS#5 F3 DQSL_c
DDR_B_DQS5 G3 DQSL_t

DDR_DRAMRST#_R P1 RESET

DDR_DRAMRST#_R — 2 — RD197 240_0402_1% — 1 F9 ZQ

DDR_B_ACT# L3 ACT
DDR_B_BG0 M2 BG0
N9 TEN
DDR_B_ALERT# P9 ALERT
DDR_B_PARITY T3 PAR

T7 NC
B1 VPP
R9 VPP

+2.5V_MEM

DQL0 G2 DDR_B_D47
DQL1 F7 DDR_B_D40
DQL2 H3 DDR_B_D41
DQL3 H7 DDR_B_D42
DQL4 H2 DDR_B_D46
DQL5 H8 DDR_B_D44
DQL6 J3 DDR_B_D43
DQL7 J7 DDR_B_D45

DQU0 A3 DDR_B_D38
DQU1 B8 DDR_B_D34
DQU2 C3 DDR_B_D33
DQU3 C7 DDR_B_D35
DQU4 C2 DDR_B_D37
DQU5 C8 DDR_B_D32
DQU6 D3 DDR_B_D39
DQU7 D7 DDR_B_D36

+1.2V_DDR

VDD B3, B9, D1, G7, J1, J9, L1, L9, R1, T9
VDDQ A1, A9, C1, D9, F2, F8, G1, G9, J2, J8
VSS B2, E1, E9, G8, K1, K9, M9, N1, T1
VSSQ A2, A8, C9, D2, D8, E3, E8, F1, H1, H9

RD237 BOM control for DDP@ /SDP@

RD237 240_0402_1% @ — 2 — 1

RD252 1 DDP@ 2 0_0201_5% DDR_B_BG1
SDP@ RD2531 2 0_0201_5%

96-BALL SDRAM_DDR4
K4A8G165WB-BCPB_FBGA96
@

+0.6VS

DDR_B_MA0 RD206 1 — 2 36_0201_1%
DDR_B_MA1 RD198 1 — 2 36_0201_1%
DDR_B_MA2 RD217 1 — 2 36_0201_1%
DDR_B_MA3 RD213 1 — 2 36_0201_1%
DDR_B_MA4 RD205 1 — 2 36_0201_1%
DDR_B_MA5 RD204 1 — 2 36_0201_1%
DDR_B_MA6 RD211 1 — 2 36_0201_1%
DDR_B_MA7 RD216 1 — 2 36_0201_1%
DDR_B_MA8 RD214 1 — 2 36_0201_1%
DDR_B_MA9 RD224 1 — 2 36_0201_1%
DDR_B_MA10 RD209 1 — 2 36_0201_1%
DDR_B_MA11 RD215 1 — 2 36_0201_1%
DDR_B_MA12 RD219 1 — 2 36_0201_1%
DDR_B_MA13 RD221 1 — 2 36_0201_1%
DDR_B_MA14 RD203 1 — 2 36_0201_1%
DDR_B_MA15 RD223 1 — 2 36_0201_1%
DDR_B_MA16 RD222 1 — 2 36_0201_1%
DDR_B_BA0 RD218 1 — 2 36_0201_1%
DDR_B_BA1 RD212 1 — 2 36_0201_1%
DDR_B_CLK0 RD201 1 — 2 36_0201_1%
DDR_B_CLK#0 RD225 1 — 2 36_0201_1%
DDR_B_CKE0 RD220 1 — 2 36_0201_1%
DDR_B_CS#0 RD207 1 — 2 36_0201_1%
DDR_B_ODT0 RD199 1 — 2 36_0201_1%
DDR_B_ACT# RD200 1 — 2 36_0201_1%
DDR_B_BG0 RD210 1 — 2 36_0201_1%
DDR_B_PARITY RD208 1 — 2 36_0201_1%

+1.2V_DDR

DDR_B_ALERT# RD202 2 — 1 49.9_0201_1%

DDR_DRAMRST#_R — CD114 0.1U_0201_10V6K — @EMC@

PLACE NEAR TO UD7,UD8

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.

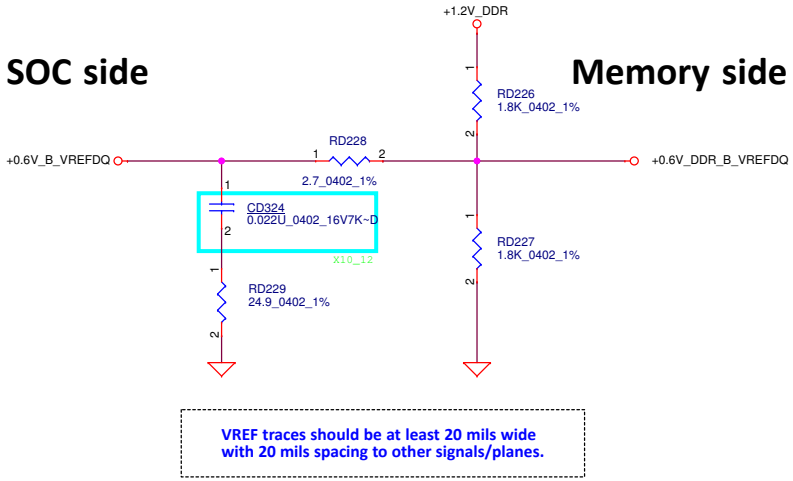
Title: DDR4 Memory Down_CHB

Size: Custom | Document Number: LA-F211P | Rev: 1.0(A00)

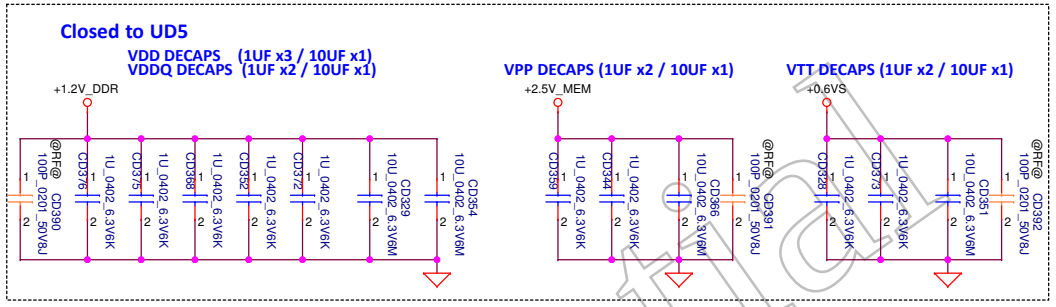
Date: Thursday, January 11, 2018 | Sheet 27 of 71

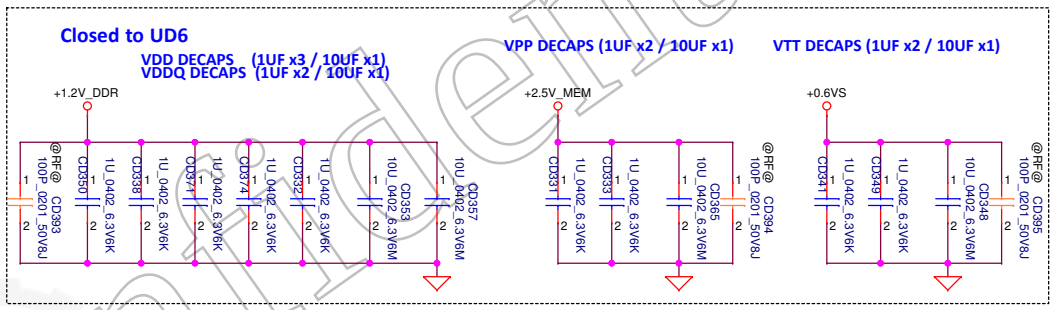
DDR4 Memory Down_CHB

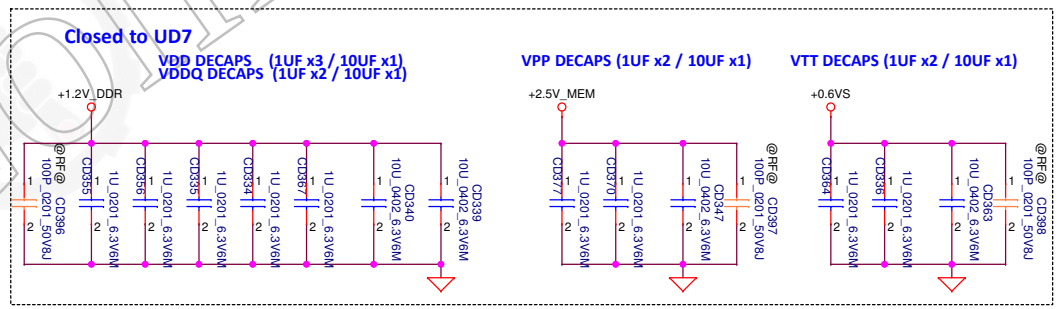
Non-Interleave Memory

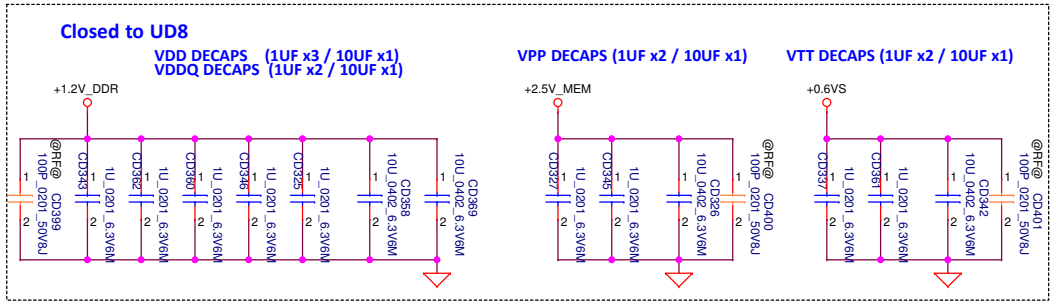


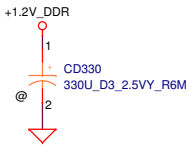
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.











Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

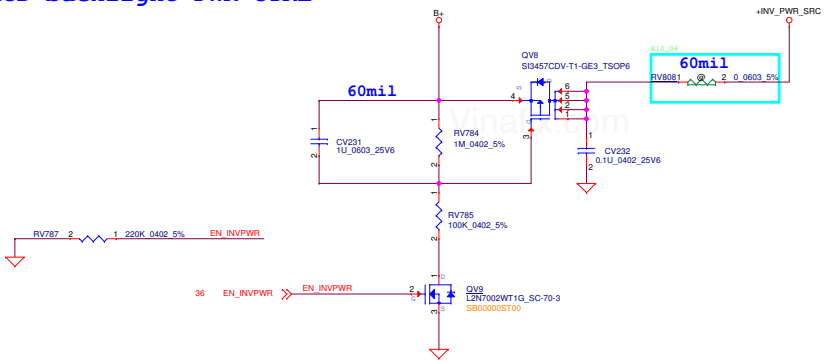
Compal Electronics, Inc.

Title: DDR4 VREF/DECAPS CHB

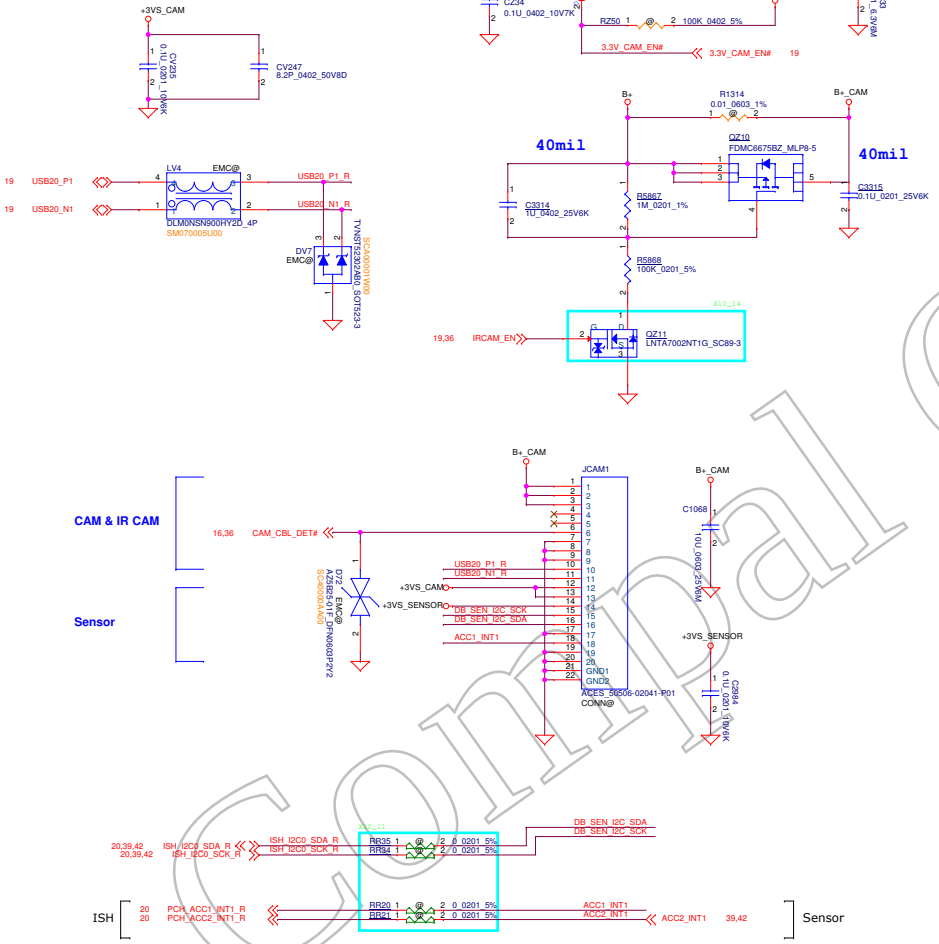
Size: Custom | Document Number: LA-F211P | Rev: 1.0(A00)

Date: Thursday, January 11, 2018 | Sheet 28 of 71

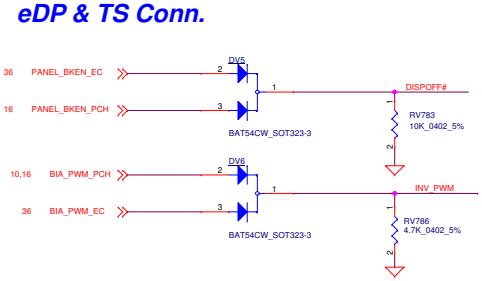
LCD backlight PWR CTRL

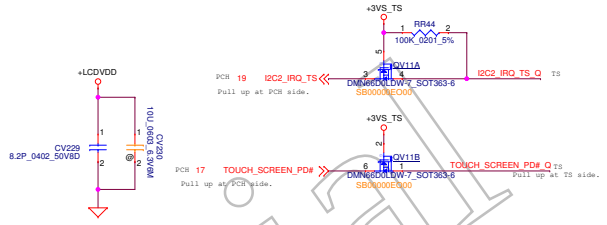


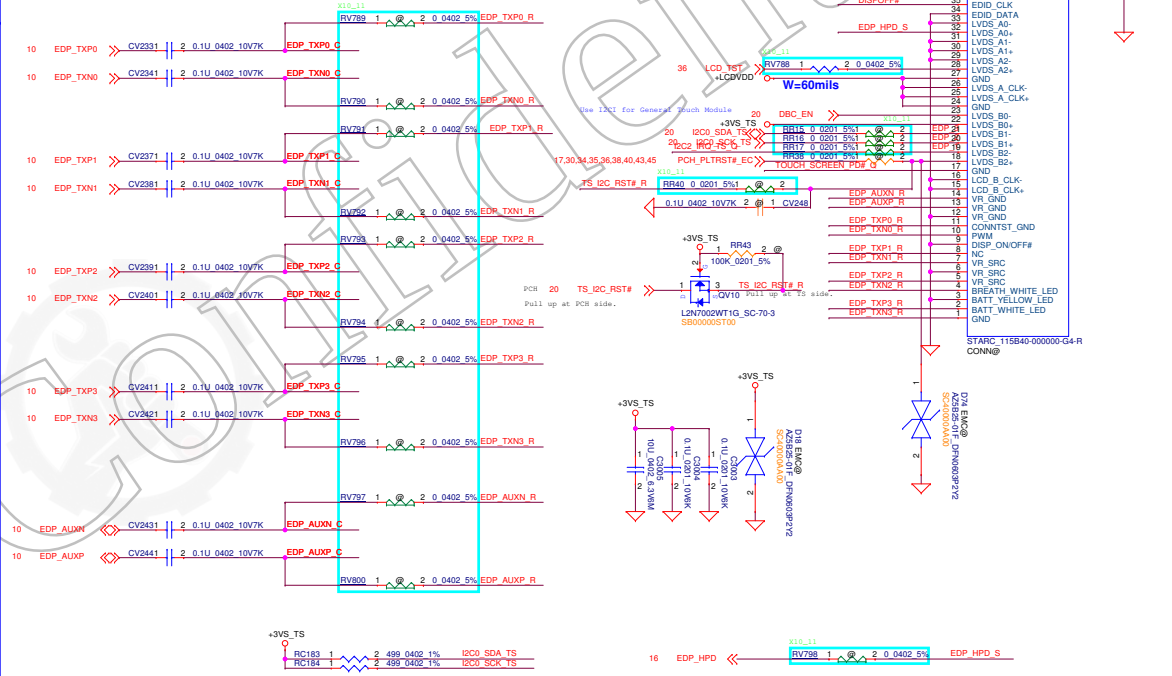
IR Digital Camera+Sensor



eDP & TS Conn.







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date 2018/12/31	Title: eDP/CCD/TS
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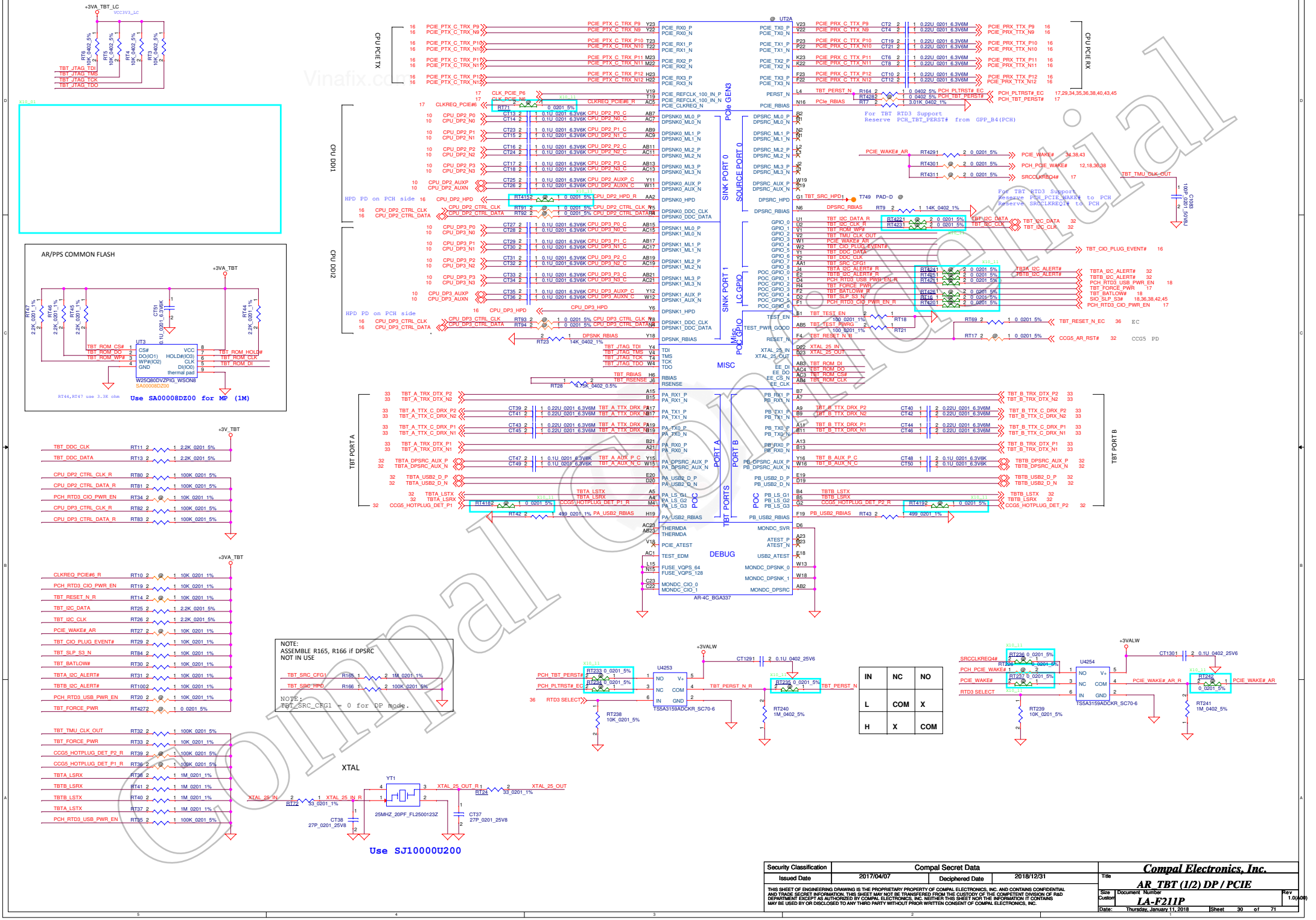
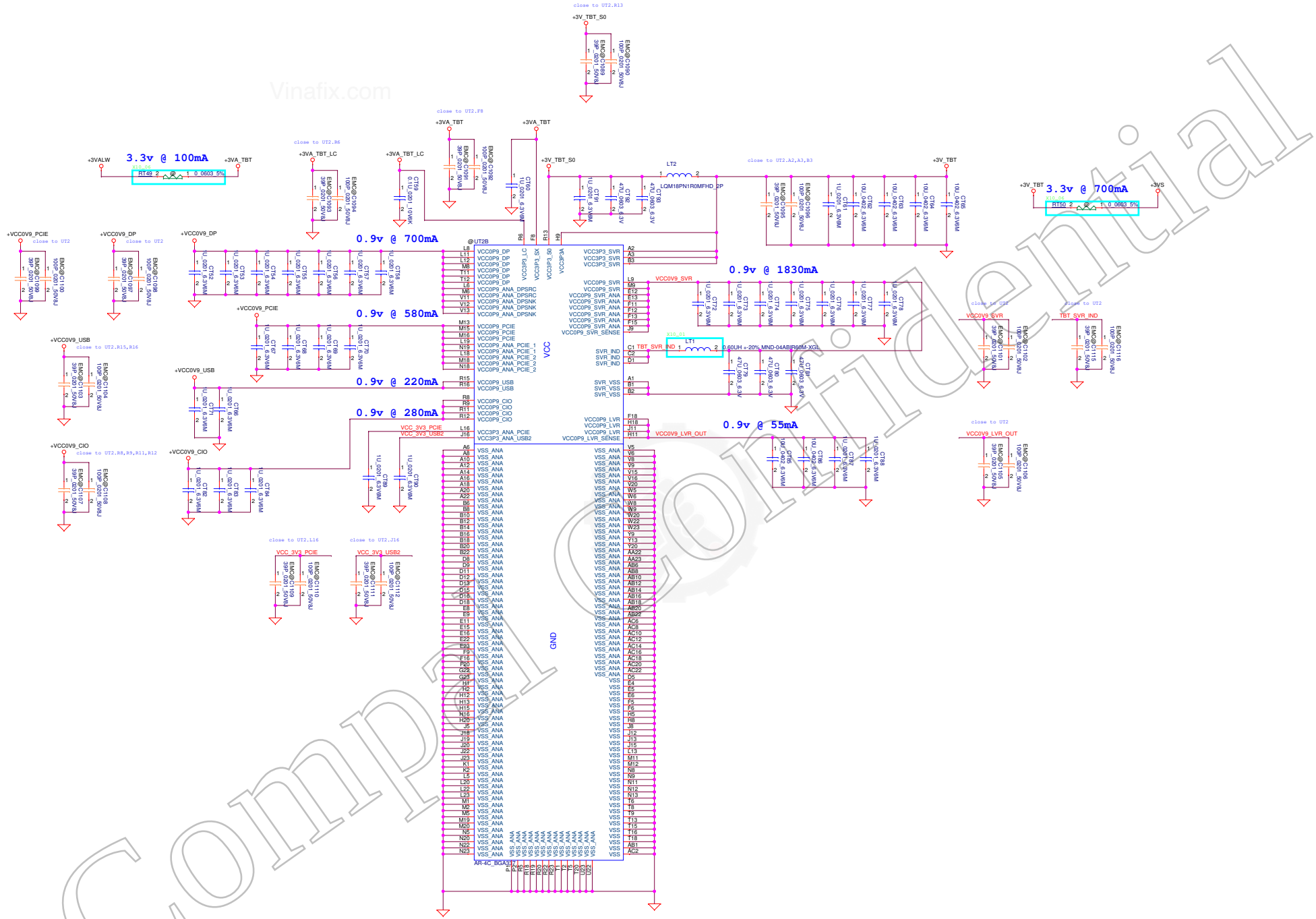
			Date: Thursday, January 11, 2018; Sheet 29 of 71



Security Classification	Compal Secret Data	
Issued Date	2017/04/07	Deciphered Date 2018/12/31

Title	Compal Electronics, Inc.
	AR_TBT (1/2) DP / PCIE
Size: Custom	Document Number: LA-F211P
Rev	1.0(0.0)
Date: Thursday, January 11, 2018	Sheet 30 of 71



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

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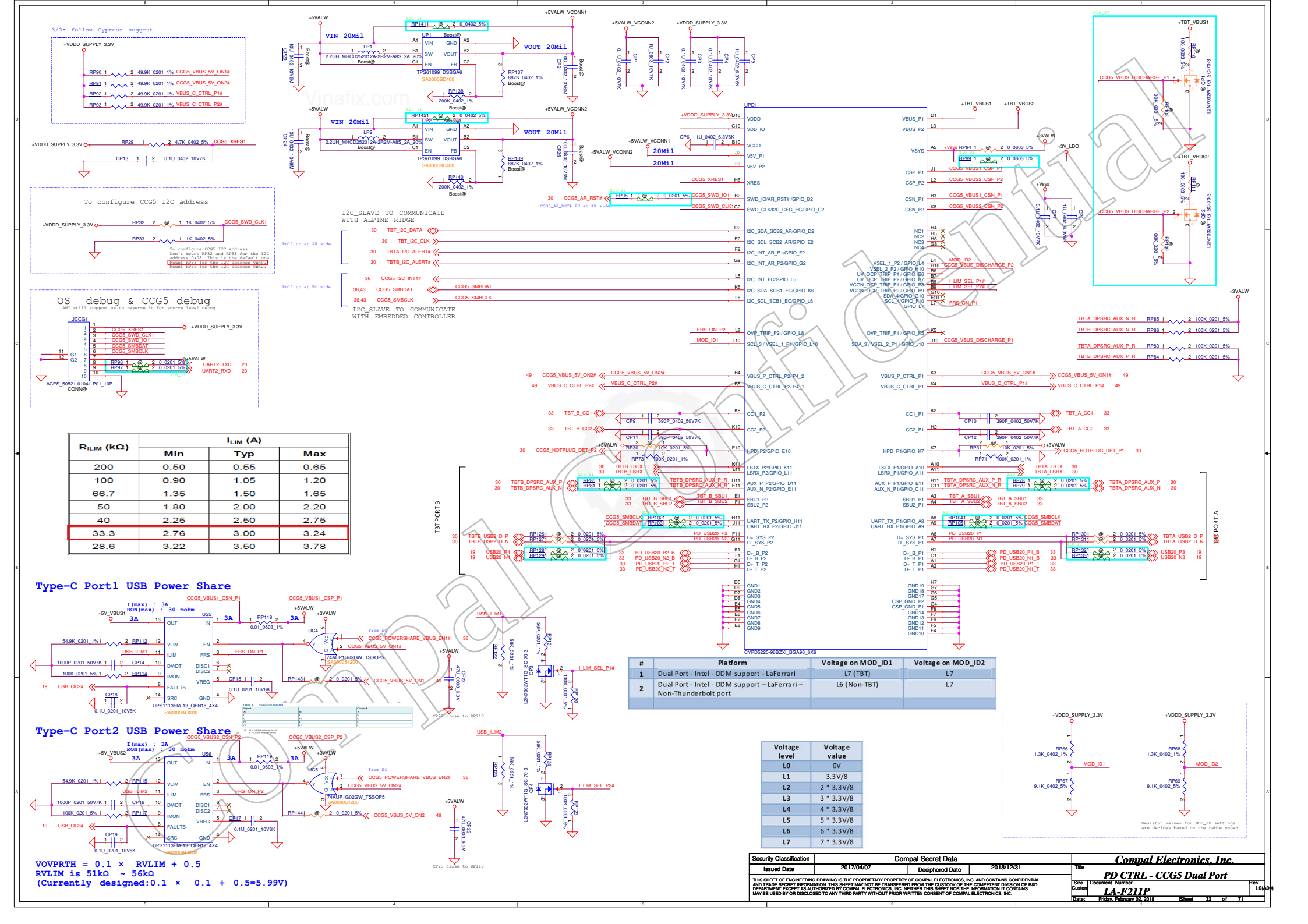
Compal Electronics, Inc.

Title: AR_TBT (2/2) PWR / VSS

Size	Document Number	Rev
Custom	LA-F211P	1.0(A00)

Date: Thursday, January 11, 2018 | Sheet 31 of 71



R_{ILIM} (kΩ)	I_{LIM} (A)		
	Min	Typ	Max
200	0.50	0.55	0.65
100	0.90	1.05	1.20
66.7	1.35	1.50	1.65
50	1.80	2.00	2.20
40	2.25	2.50	2.75
33.3	2.76	3.00	3.24
28.6	3.22	3.50	3.78

#	Platform	Voltage on MOD_ID1	Voltage on MOD_ID2
1	Dual Port - Intel - DDM support - LaFerrari	L7 (TBT)	L7
2	Dual Port - Intel - DDM support – LaFerrari – Non-Thunderbolt port	L6 (Non-TBT)	L7

Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

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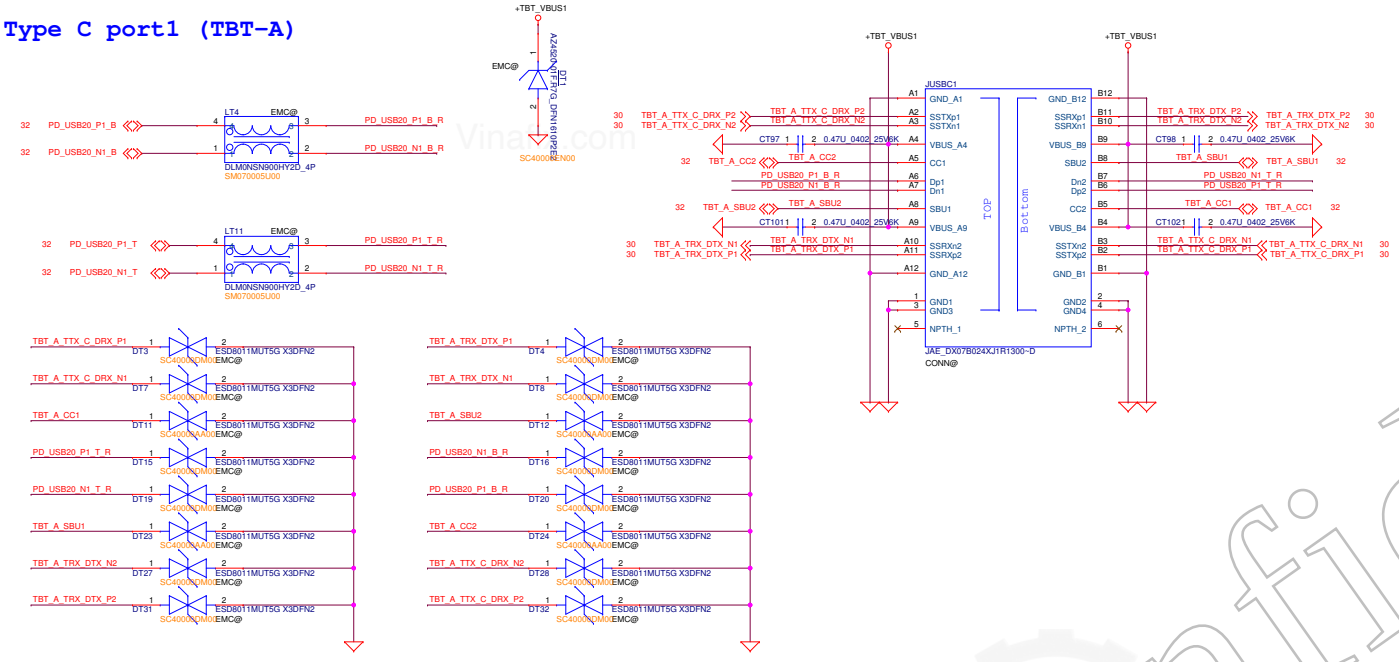
Compal Electronics, Inc.

Title: PD CTRL - CCG5 Dual Port

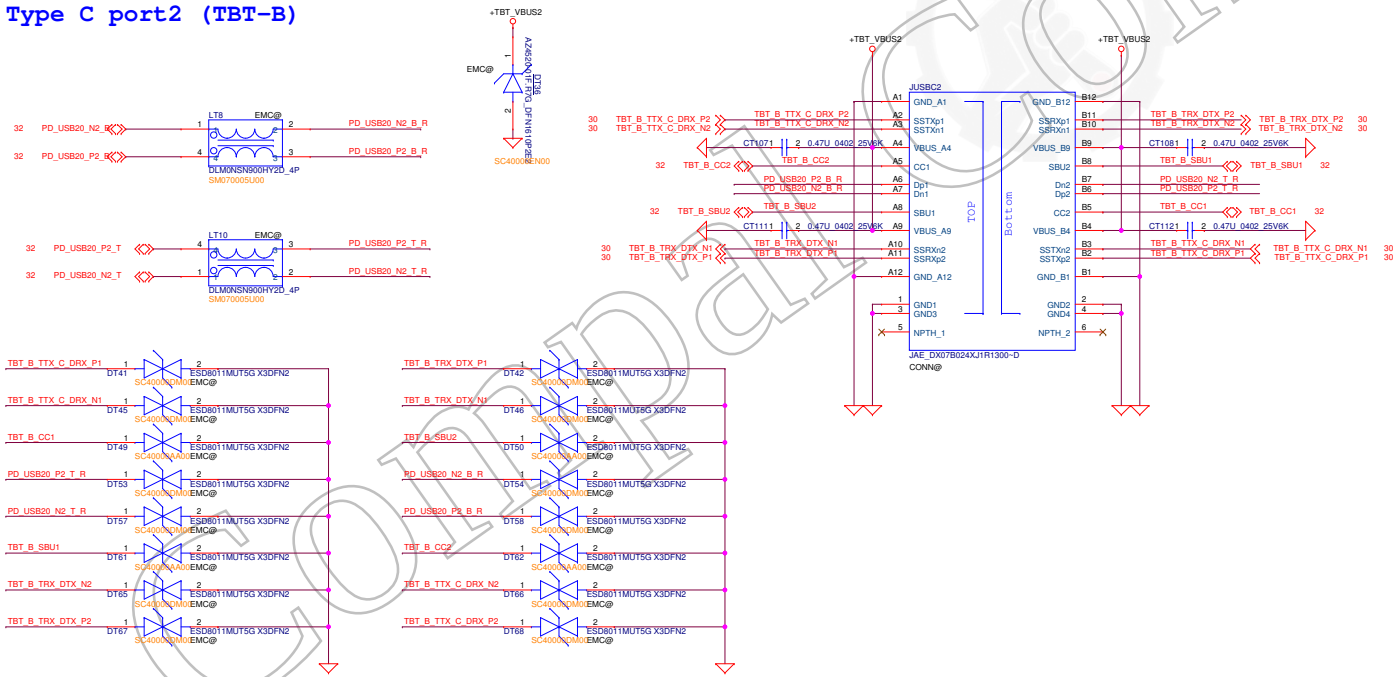
Size: Custom | Document Number: LA-F211P | Rev: 1.0(0.0)

Date: Friday, February 02, 2018 | Sheet 32 of 71

Type C port1 (TBT-A)



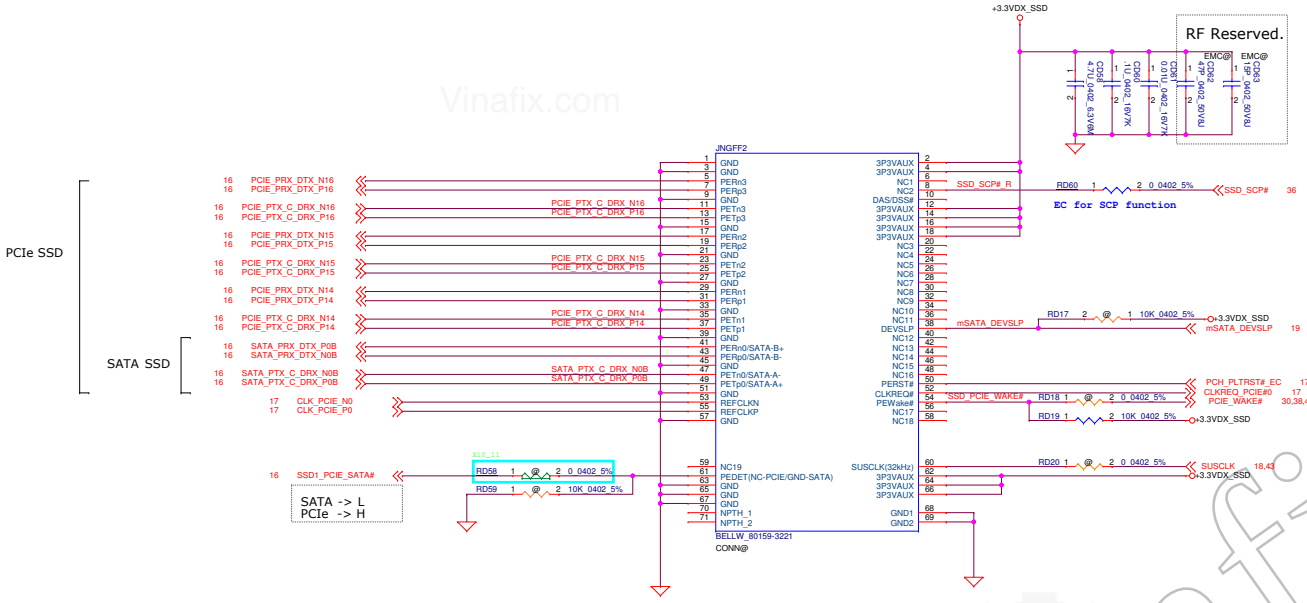
Type C port2 (TBT-B)



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: USB TYPE-C CONN			
Size: Custom	Document Number: LA-F211P	Rev: 1.0(A00)	
Date: Monday, February 26, 2018	Sheet 33 of 71		

M.2 Slot-C Key-M (SSD-1)

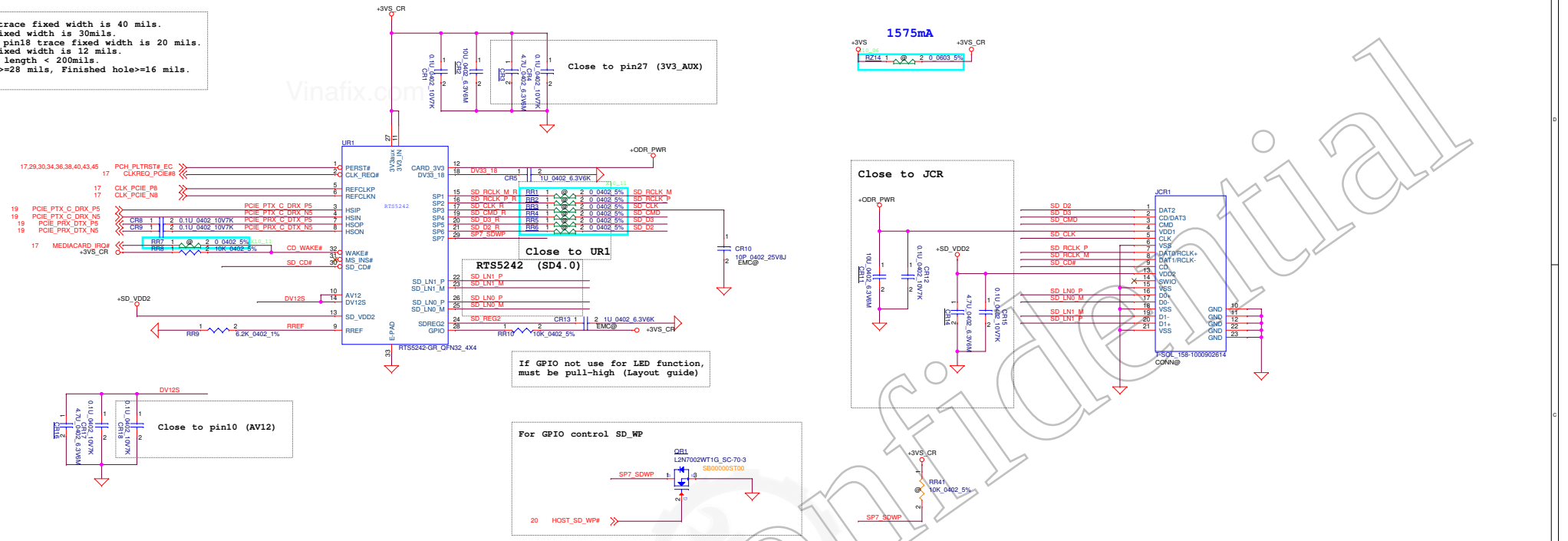


Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: NGFF-SSD			
Size: Custom	Document Number: LA-F211P		Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 34 of 71		

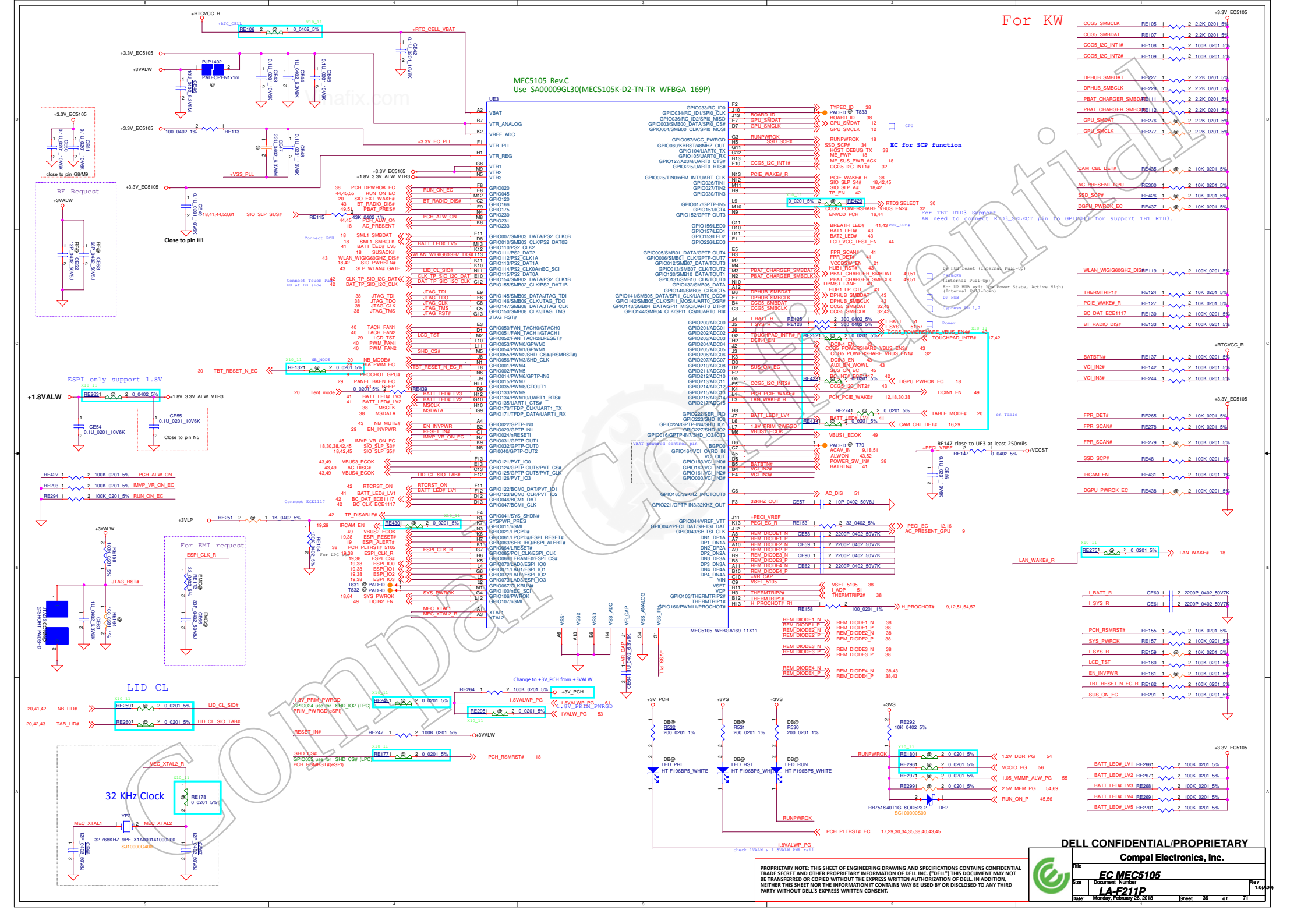
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: Card Reader_RTS5242			
Size	Document Number: LA-F211P		Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 35 of 71		


For KW
MEC5105 Rev.C
Use SA00009GL30(MEC5105K-D2-TN-TR WFBGA 169P)
EC for SCP function
For TBT RTD3 Support
AR need to connect RTD3_SELECT pin to GPIO017 for support TBT RTD3.
ESPI only support 1.8V
RF Request
LID CL
32 KHz Clock
For EMI request
Close to pin H1
Close to pin N5
close to pin G8/M9
Change to +3V_PCH from +3VALW
RE147 close to UE3 at least 250mils
MEC5105_WFBGA169_11X11
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
EC MEC5105
LA-F211P
Monday, February 26, 2018
Sheet 36 of 71
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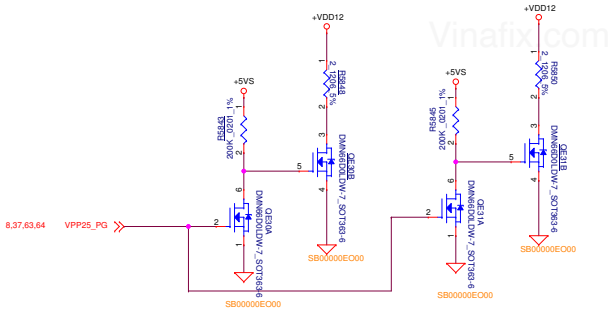
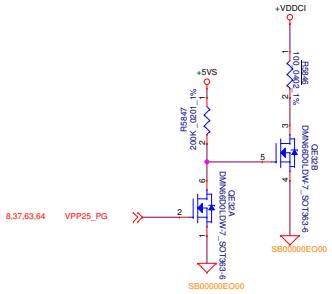
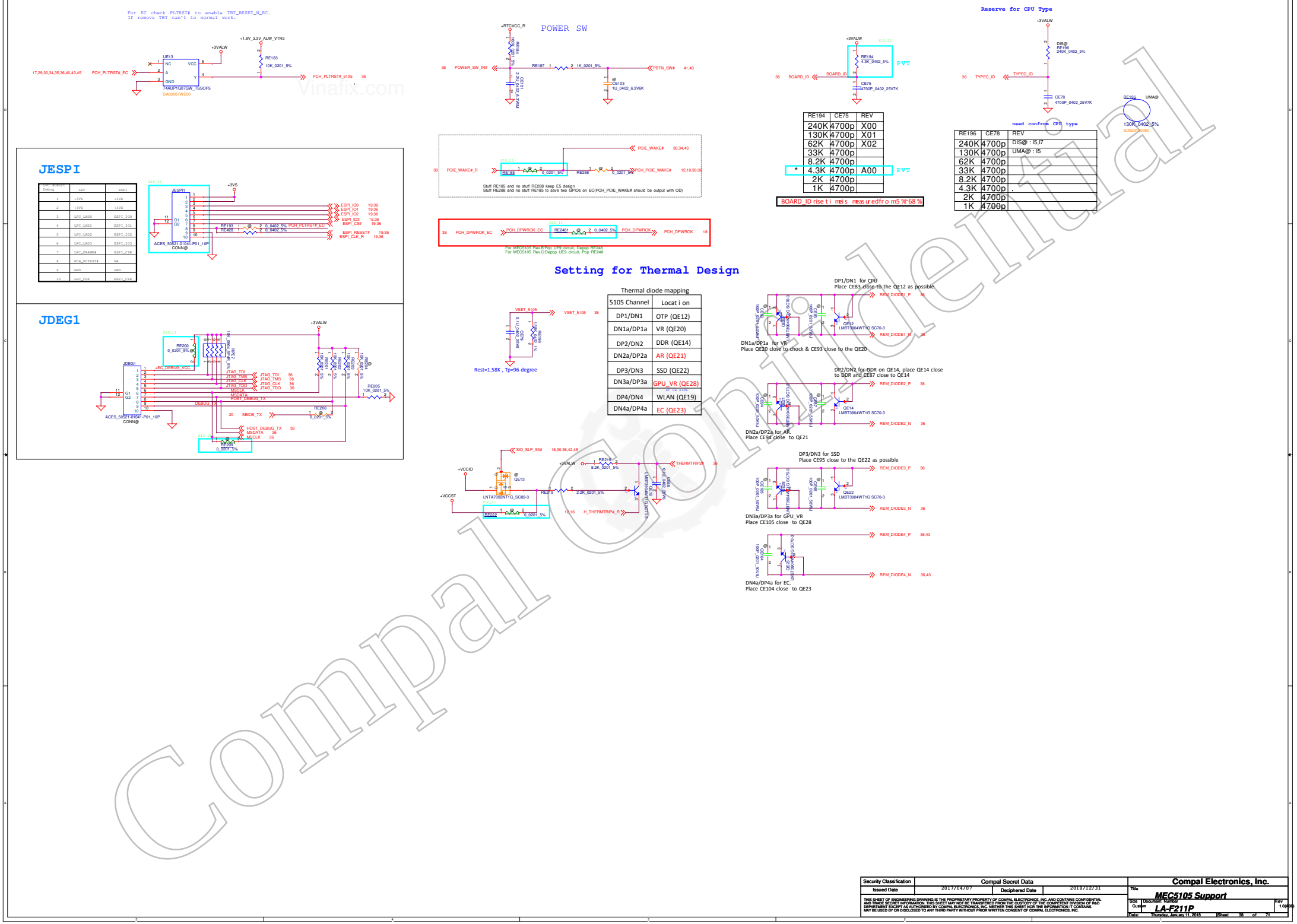
+VDD12 Discharge



+VDDCI Discharge



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date 2018/12/31	Title: MCP 23017
			Size: Custom; Document Number: LA-F211P; Rev: 1.0(A00)
			Date: Thursday, January 11, 2018; Sheet 37 of 71



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

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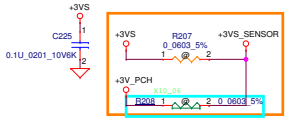
Compal Electronics, Inc.

Title: MEC5105 Support

Size: Custom | Document Number: LA-F211P | Rev: 1.0(00)

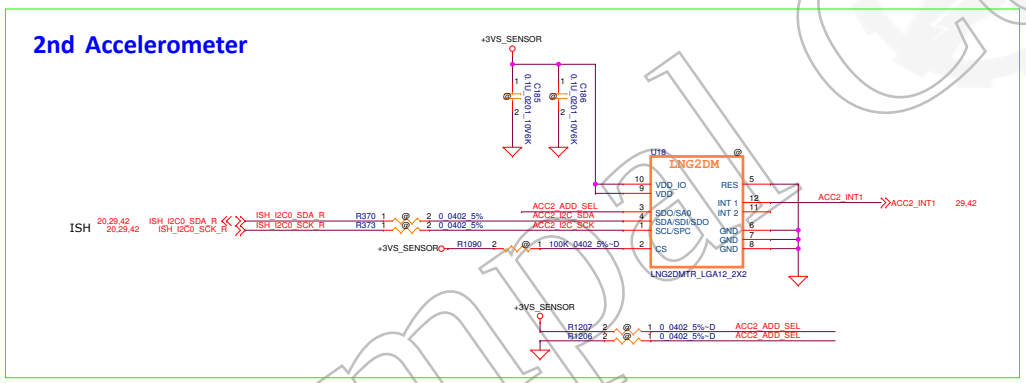
Date: Thursday, January 11, 2018 | Sheet 38 of 71

Sensor Hub



DVT1 move to KB-B, reserve MB

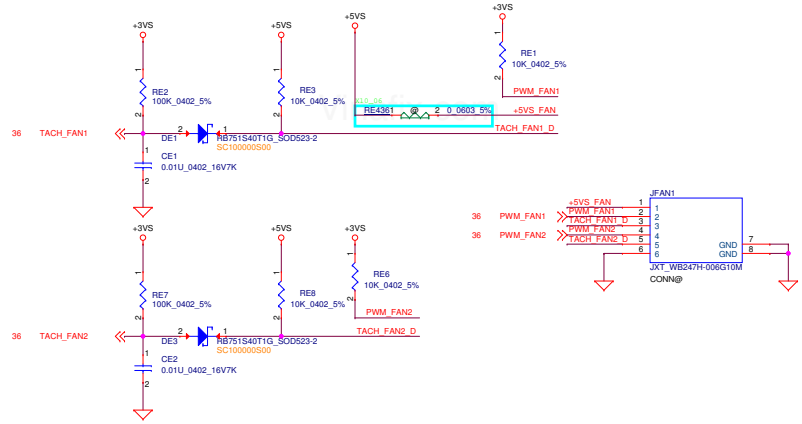
2nd Accelerometer



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date	2018/12/31

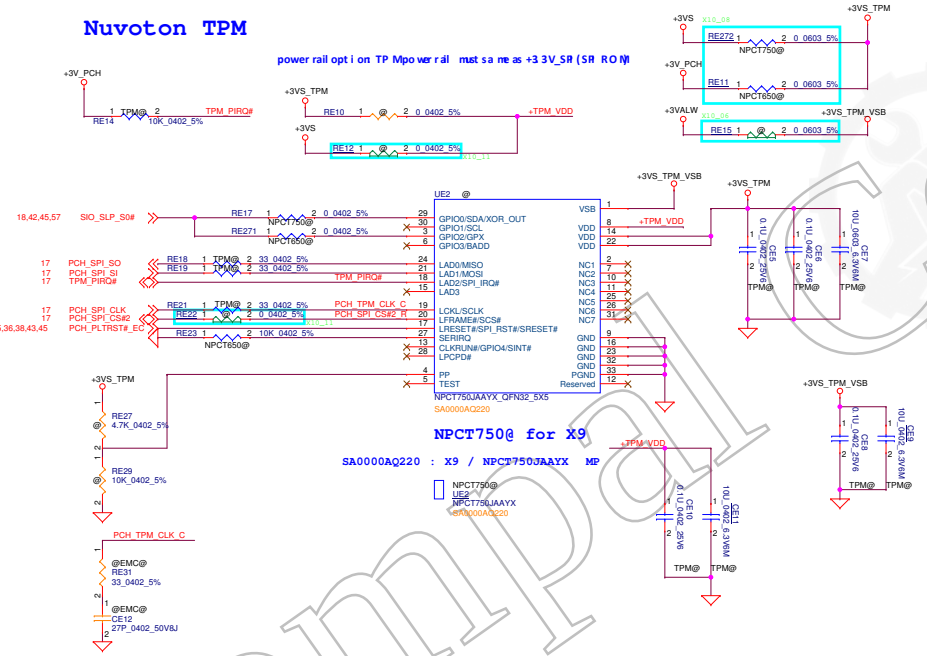
Title	Sensor		
Size	Document Number LA-F211P		Rev 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 39 of 71		

PWM FAN



Nuvoton TPM

power rail option TPM power rail must same as +3.3V_SPI (SPI ROM)



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Compal Electronics, Inc.

Title: FAN/TPM

Size: Custom | Document Number: LA-F211P | Rev: 1.0(A00)

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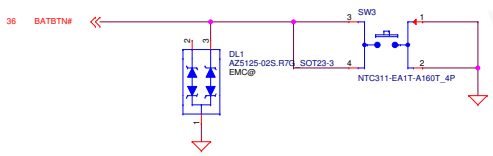
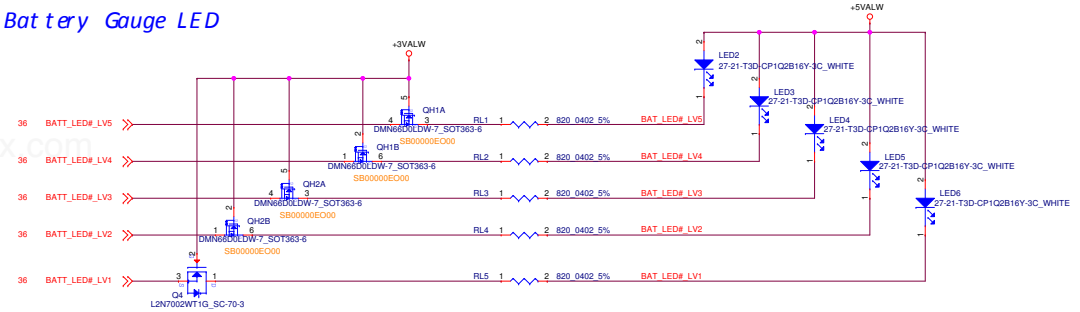
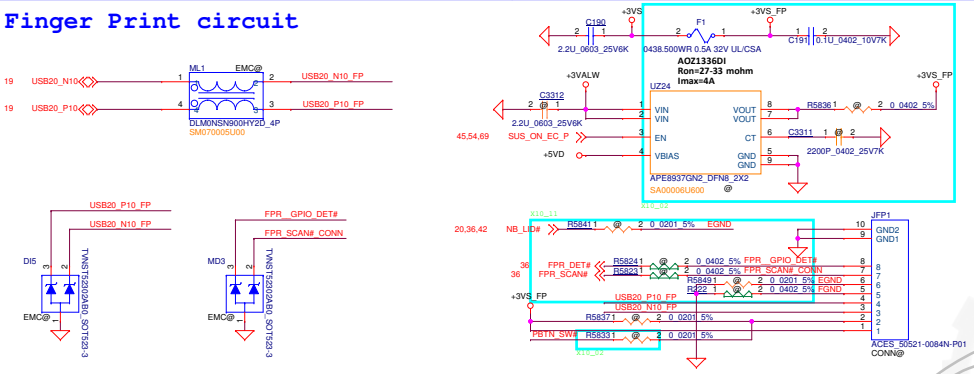
BATT LED Power Button



Battery Gauge LED

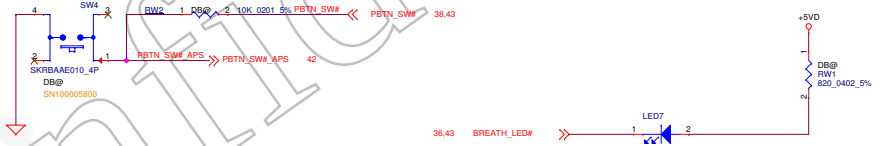


Finger Print circuit

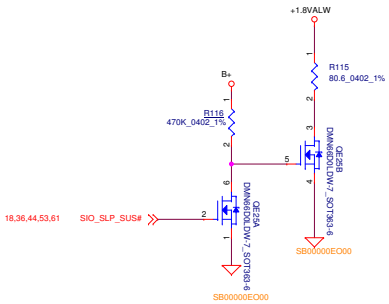


Power Button and LED for DEBUG only (MP remove)

+5VD - Trace width : 20mil

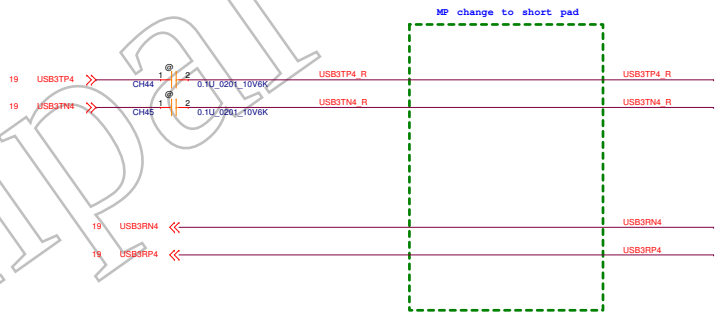


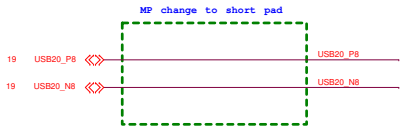
+1.8VALW Discharge

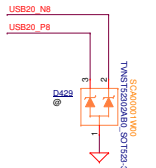


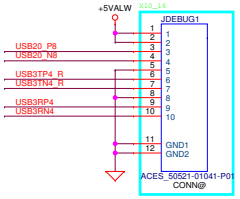
Reference Aspen

WIN debug









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Issued Date	2017/04/07	Deciphered Date 2018/12/31	Title: BAT LED/FP/PWRM
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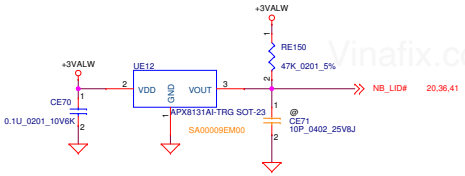
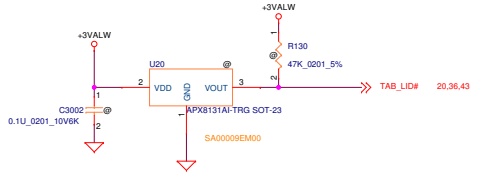
Lid Switch

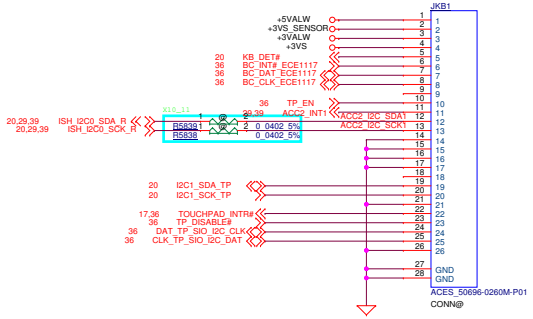
NB LID SW

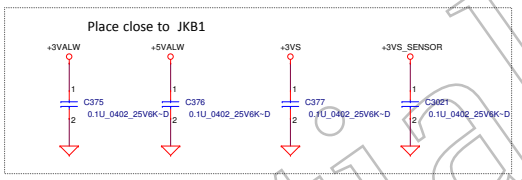


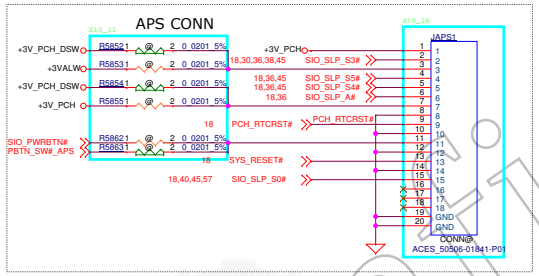
Tablet LID SW



Keyboard Controller board + DMIC + TP + ACC2

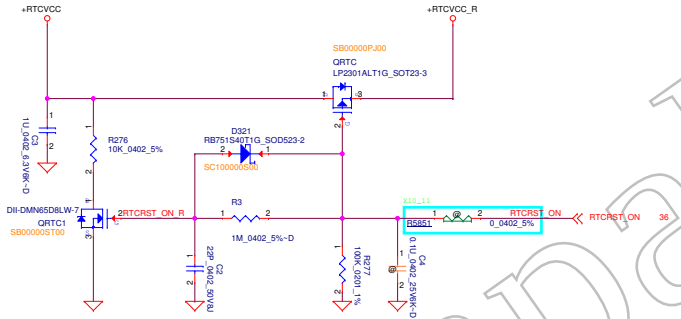




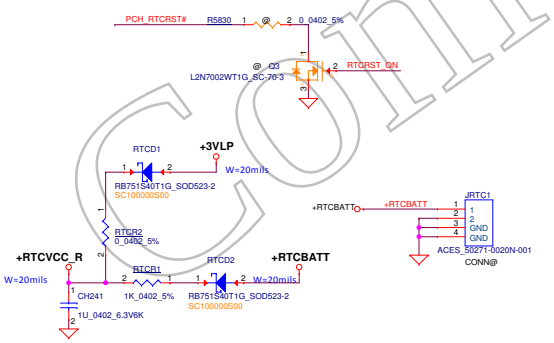


RTC Battery non- Charge Function

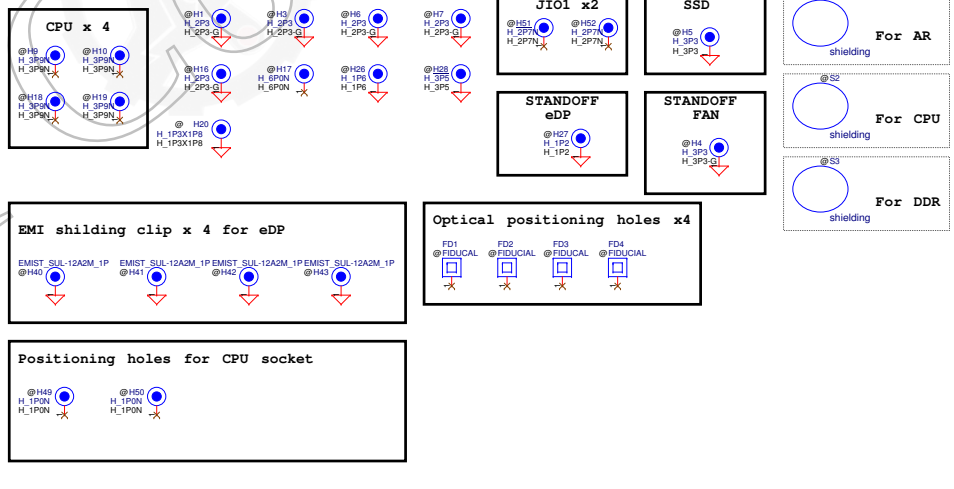
Default: OD EC drives GPIOs to LOW to turn off power to VCCRTC.



X00: add X9&X8 RTC diccgarge schematic



Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: CONN/Lid/RTC/Screws			
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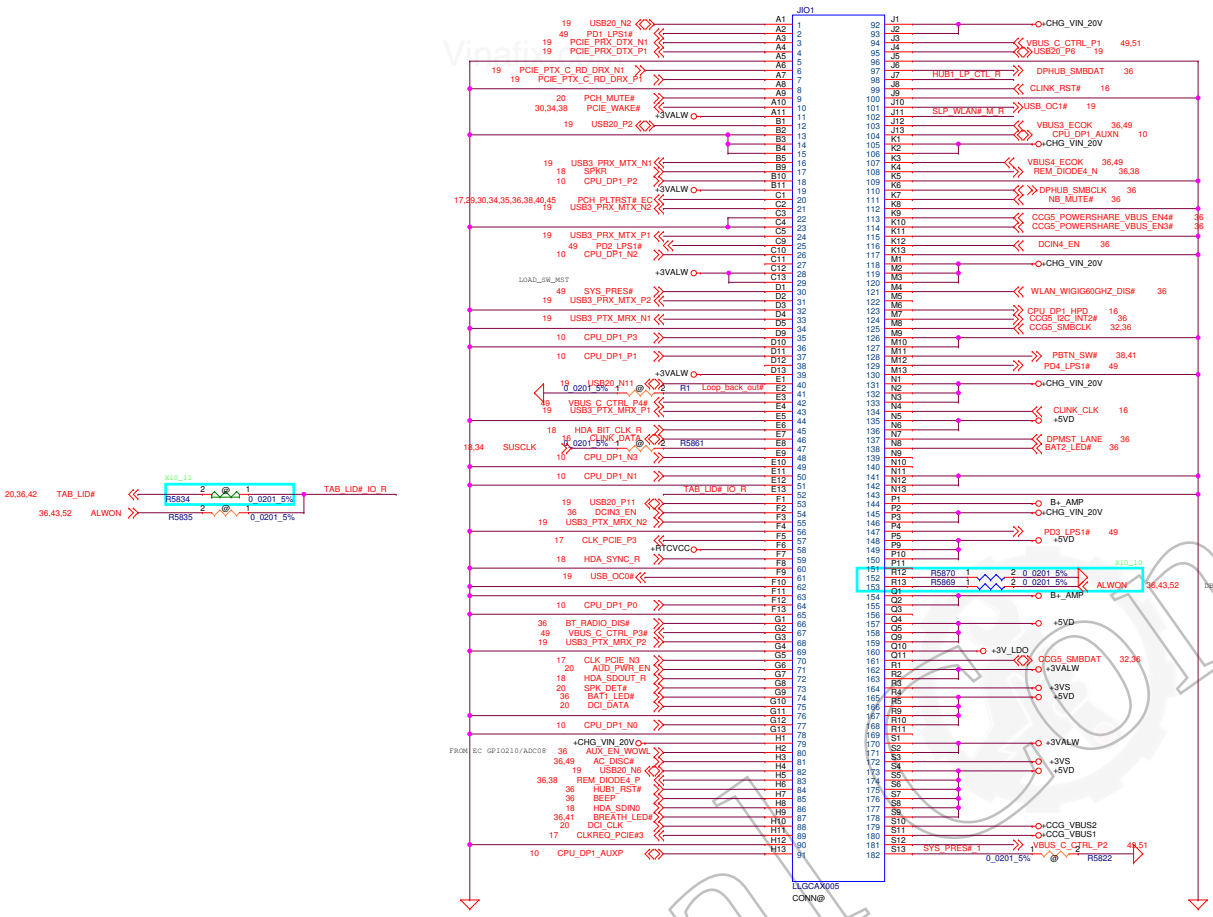
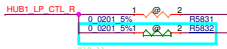
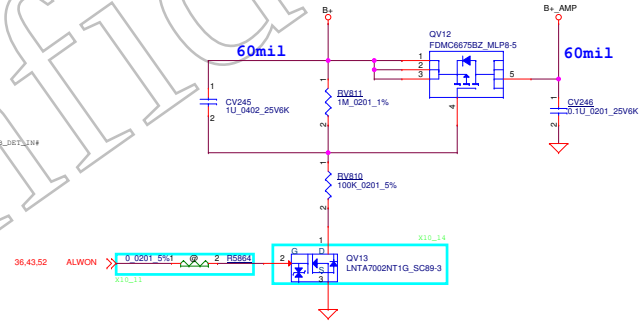
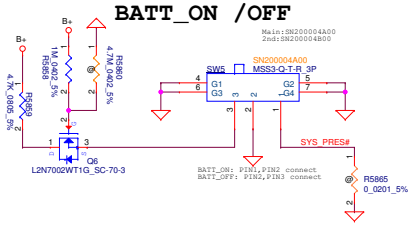
+CHG_VIN_20V : 13 PIN
+5VD: 14PIN -> change to 18 PIN
B+ : 3 PIN
+3VS : 2 PIN
+3VALW : 3 PIN -> change to 8 PIN
+1.05V_VMM_ALW : 3 PIN -> move to IO/B
+3V_LDO : 1 PIN
+RTCVCC : 1 PIN

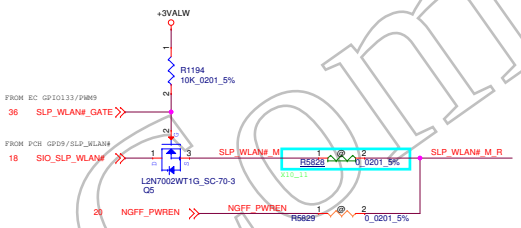








Gen 9 WLAN power for WiAMT



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Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: IO/B CONN

Size: | Document Number: LA-F211P | Rev: 1.0(A00)

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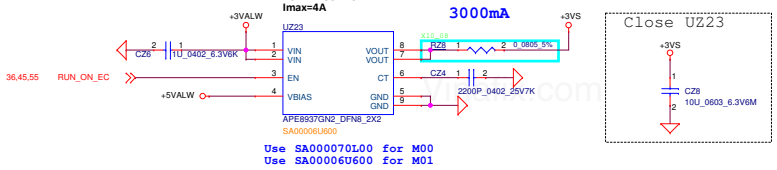
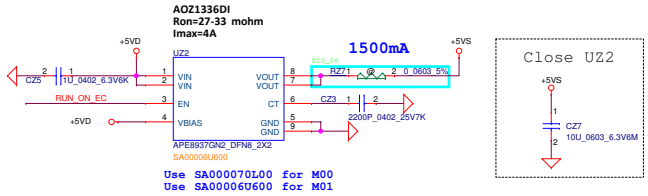
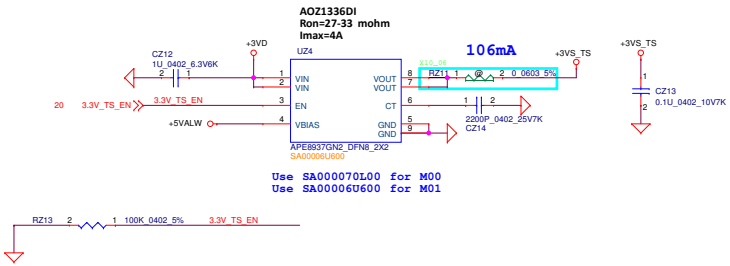
+3VALW to +3VS



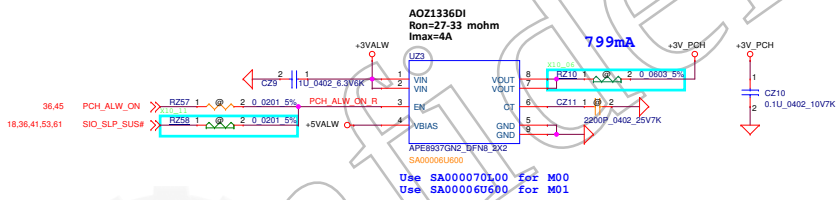
+5VD to +5VS



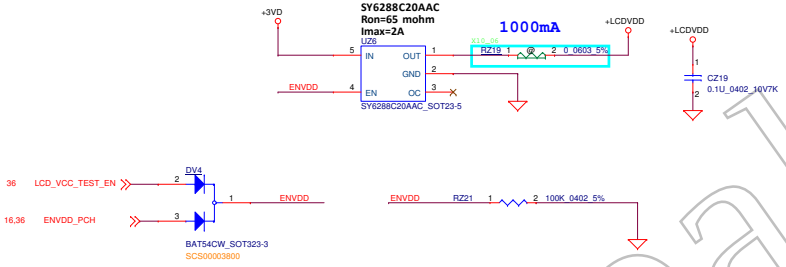
Touch Screen Load Switch



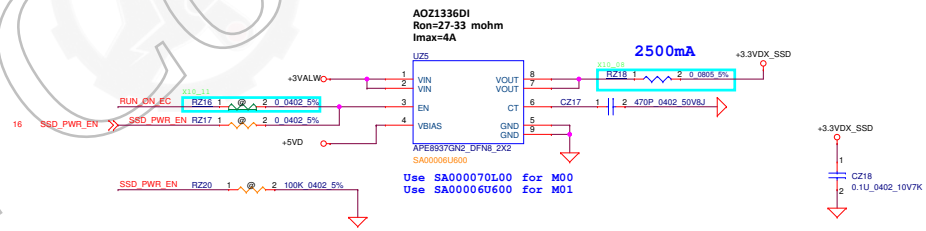
+3VALW to +3V_PCH



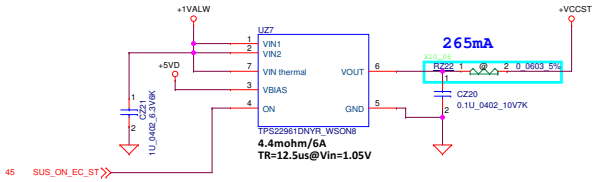
eDP Load Switch



SSD Load Switch



+VCCST Load Switch



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.	
Title	SYS DC/DC Interface
Size	Document Number: LA-F211P
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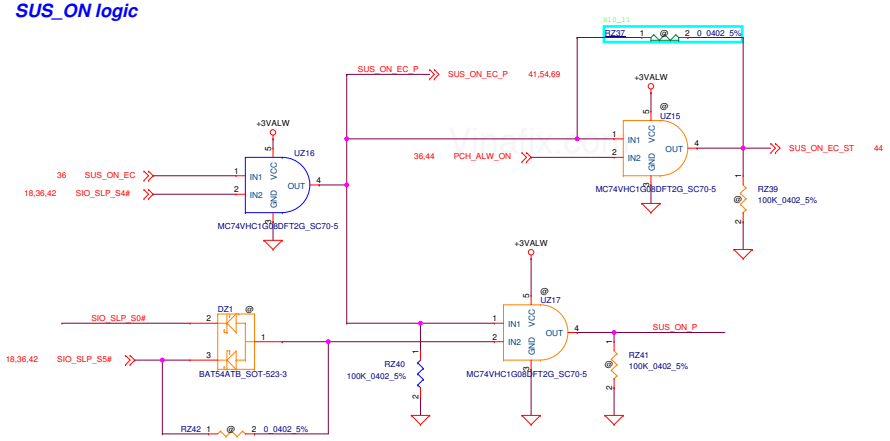
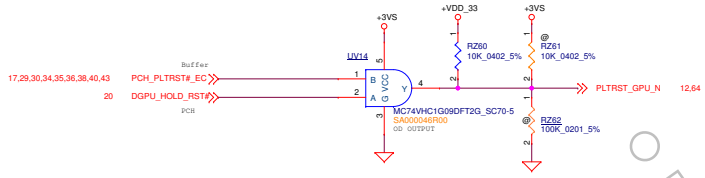
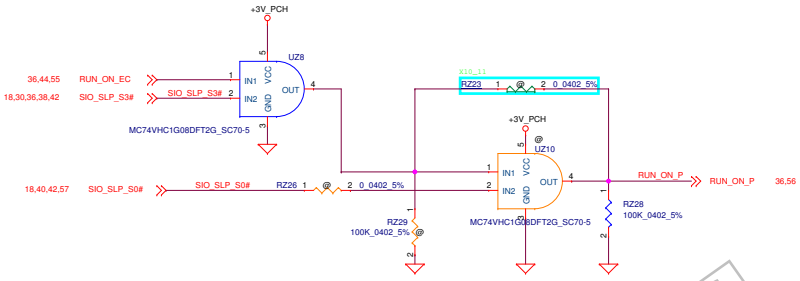
SUS_ON logic



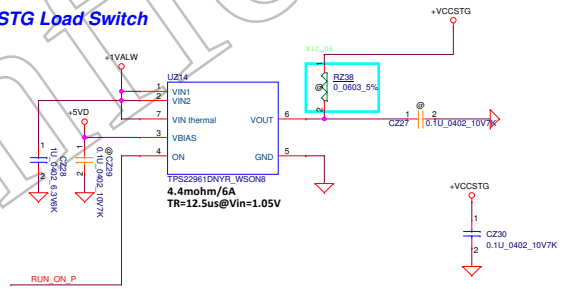
dGPU reset



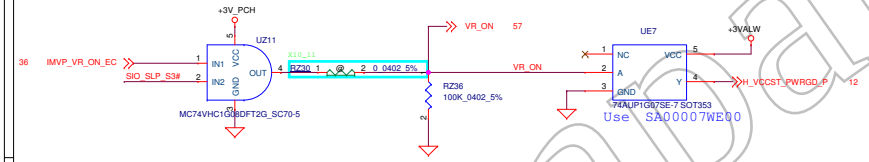
RUN_ON logic



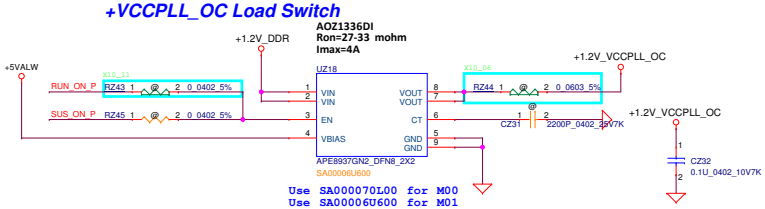
+VCCSTG Load Switch



H_VCCST_PWRGD logic



+VCCPLL_OC Load Switch



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Issued Date	2017/04/07	Deciphered Date	2018/12/31
Title	DC/DC/S0iX/CS		
Size	Document Number		Rev
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Compal Confidential

Project Code :
File Name :

PCB

ZZZ CPU@ — R1

PCB DAZ10 LA-F211P LS-F211P
SA20470020

R3
DA224700201:GOLD
DA224700202:TRIPOD
DA224700203:FOUNDER

CPU

UC1 ISQNTR@ — i5_DIS R1	UC1 I7QNTN@ — i7_DIS R1	UC1 I7QNV0@ — i7_DIS vPRO R1
FH80677034177 14 QNTR B0 SA00008J1YA	FH80677034175 15 QNTN B0 SA00008J1WA	FH80677034174 18 QNV0 B0 SA00008J1WG
UC1 I5SR3RM@ — i5_DIS R3	UC1 I7SR3RK@ — i7_DIS R3	UC1 I7SR3RJ@ — i7_DIS vPRO R3
FH80677034177 14 SR3RM B0 SA00008J1YL	FH80677034175 15 SR3RK B0 SA00008J1YJ	FH80677034174 18 SR3RJ B0 SA00008J1YH

PCH

UH4 SR30VR1@	UH4 SR30VR3@
GL82QM175 SR30V D1 SA00004AE0L	GL82QM175 SR30V D1 SA00004AE2L

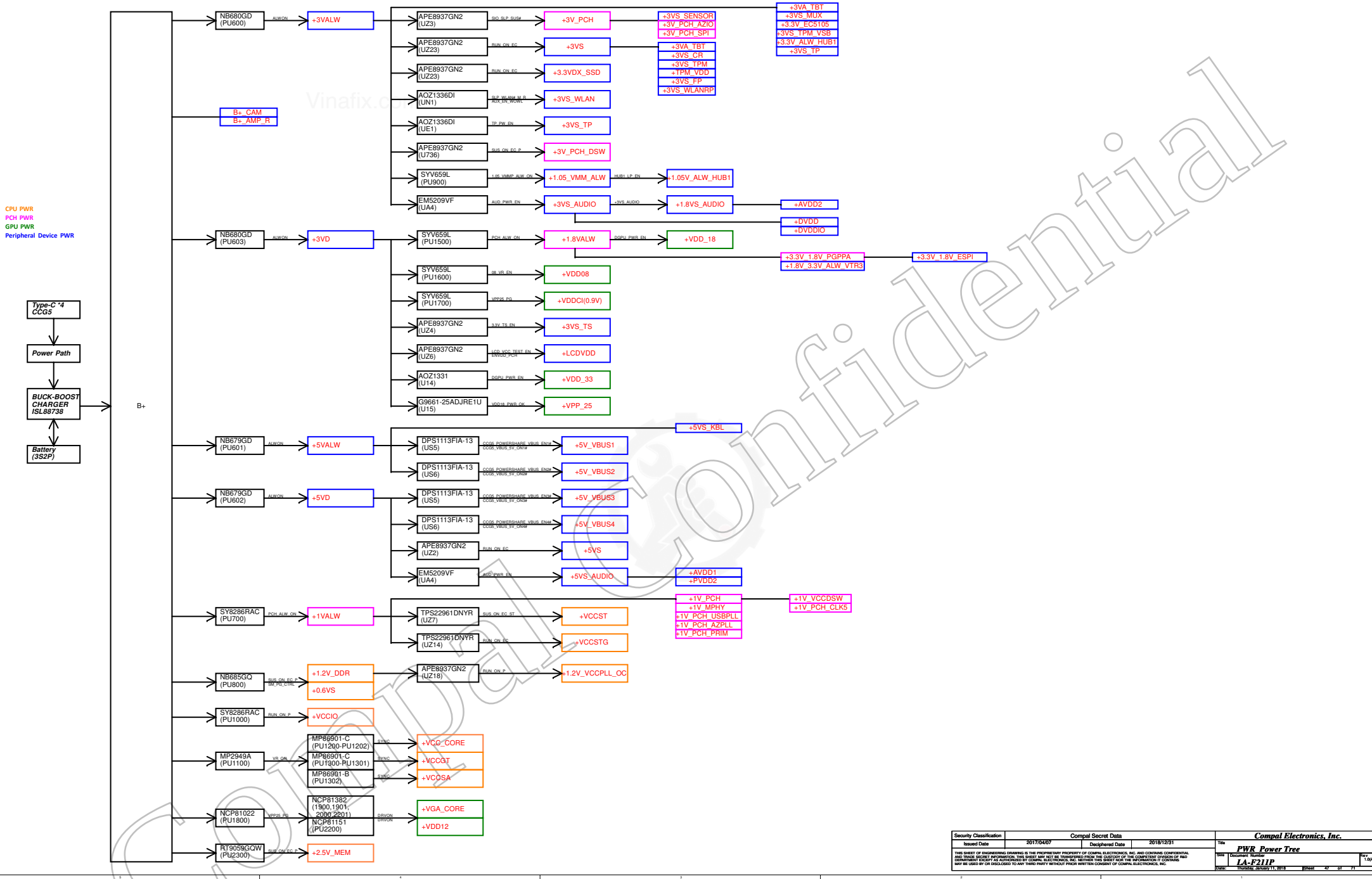
AR

UT2 SLLSMR1@	UT2 SLLSMR3@
JHL6540 SLLSM C1 FC-CSP SA00002EY2L	JHL6540 SLLSM C1 FC-CSP SA00002EY3L

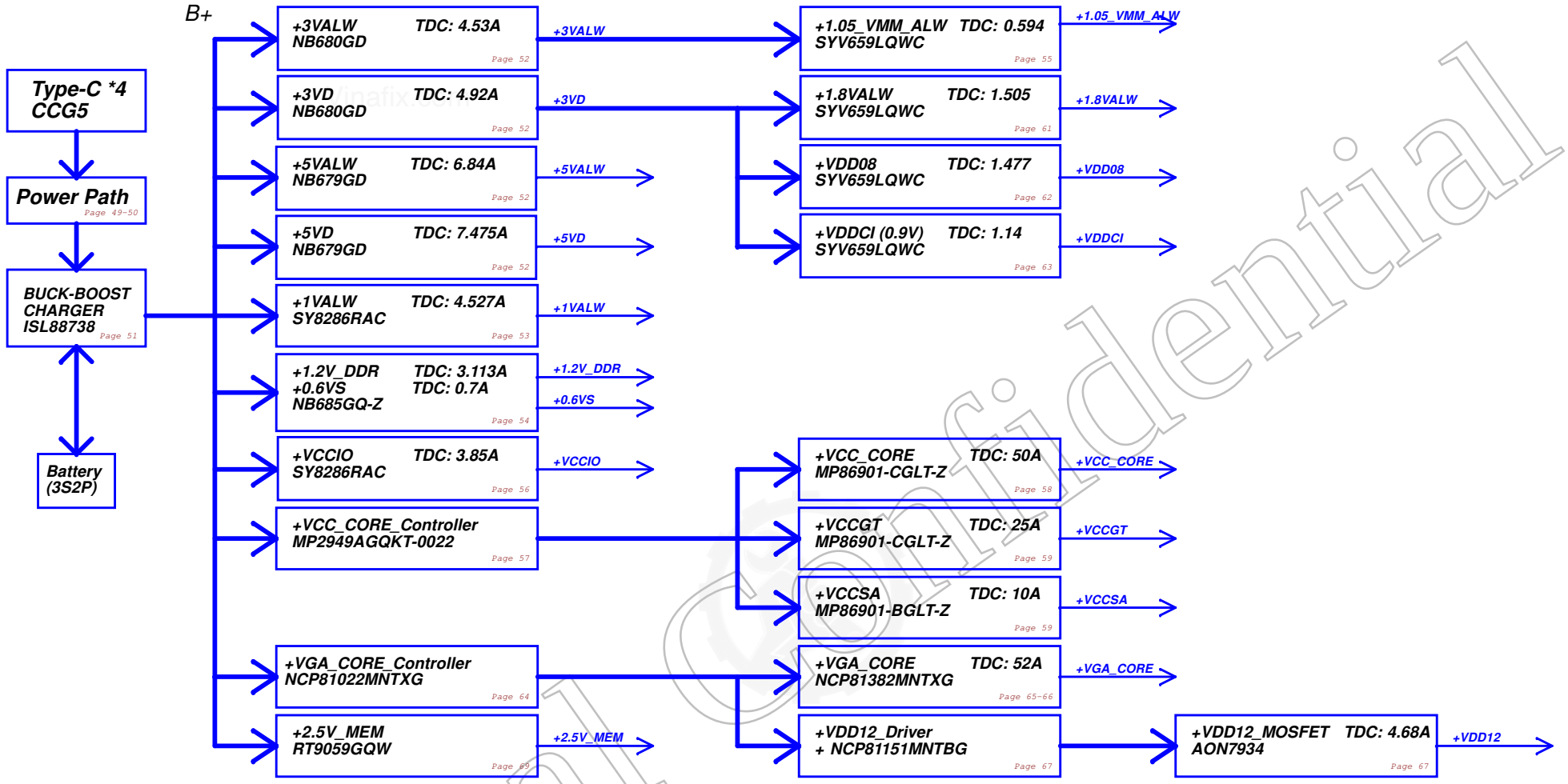
P1 need confirm P1/P2
config0 RH220/RH225
config1 RH227/RH222
config2 RH226/RH224
config3 RH223/RH218
config4 RH219/RH221

DRAM Option	DRAM Config Option MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4	DRAM SDP / DDP Option	R_COMP	X76
SDP MICRON 8G/2400	M8G_2400@ RH225 10K_0201_5% SDA03100280	M8G_2400@ RH224 10K_0201_5% SDA03100280	M8G_2400@ RH218 10K_0201_5% SDA03100280	M8G_2400@ RH221 10K_0201_5% SDA03100280	M8G_2400@ RH221 10K_0201_5% SDA03100280			R1:X7674531L07 R3:X7674531L19
SDP MICRON 8G/2666	M8G_2666@ RH225 10K_0201_5% SDA03100280	M8G_2666@ RH224 10K_0201_5% SDA03100280	M8G_2666@ RH218 10K_0201_5% SDA03100280	M8G_2666@ RH221 10K_0201_5% SDA03100280	M8G_2666@ RH221 10K_0201_5% SDA03100280	SDP@ RD230 0_0402_5% SDA03600080 … SDP@ RD237 0_0402_5% SDA03600080	SDP@ RC26 200_0402_1% SDA24200280	R1:X7674531L16 R3:X7674531L18
SDP HYNIX 8G/2400	H8G_2400@ RH225 10K_0201_5% SDA03100280	H8G_2400@ RH224 10K_0201_5% SDA03100280	H8G_2400@ RH218 10K_0201_5% SDA03100280	H8G_2400@ RH221 10K_0201_5% SDA03100280	H8G_2400@ RH221 10K_0201_5% SDA03100280			R1:X7674531L09 R3:X7674531L21
SDP SAMSUNG 8G/2400	S8G_2400@ RH225 10K_0201_5% SDA03100280	S8G_2400@ RH227 10K_0201_5% SDA03100280	S8G_2400@ RH226 10K_0201_5% SDA03100280	S8G_2400@ RH218 10K_0201_5% SDA03100280	S8G_2400@ RH221 10K_0201_5% SDA03100280			R1:X7674531L08 R3:X7674531L20
DDP MICRON 16G/2400	M16G_2400@ RH225 10K_0201_5% SDA03100280	M16G_2400@ RH224 10K_0201_5% SDA03100280	M16G_2400@ RH218 10K_0201_5% SDA03100280	M16G_2400@ RH221 10K_0201_5% SDA03100280	M16G_2400@ RH221 10K_0201_5% SDA03100280			R1:X7674531L10 R3:X7674531L23
DDP MICRON 16G/2666	M16G_2666@ RH225 10K_0201_5% SDA03100280	M16G_2666@ RH227 10K_0201_5% SDA03100280	M16G_2666@ RH224 10K_0201_5% SDA03100280	M16G_2666@ RH223 10K_0201_5% SDA03100280	M16G_2666@ RH221 10K_0201_5% SDA03100280	DDP@ RD230 240_0402_1% SDA05000780 … DDP@ RD237 240_0402_1% SDA05000780	DDP@ RC26 162_0402_1% SDA24178200	R1:X7674531L17 R3:X7674531L22
DDP HYNIX 16G/2400	H16G_2400@ RH225 10K_0201_5% SDA03100280	H16G_2400@ RH224 10K_0201_5% SDA03100280	H16G_2400@ RH218 10K_0201_5% SDA03100280	H16G_2400@ RH221 10K_0201_5% SDA03100280	H16G_2400@ RH221 10K_0201_5% SDA03100280			R1:X7674531L15 R3:X7674531L25
DDP SAMSUNG 16G/2400	S16G_2400@ RH225 10K_0201_5% SDA03100280	S16G_2400@ RH224 10K_0201_5% SDA03100280	S16G_2400@ RH218 10K_0201_5% SDA03100280	S16G_2400@ RH221 10K_0201_5% SDA03100280	S16G_2400@ RH221 10K_0201_5% SDA03100280			R1:X7674531L11 R3:X7674531L24

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date	2018/12/31
Title: BOM Option			
Size	Document Number: LA-F211P		Rev: 1.0
Date: Thursday, January 31, 2019	Sheet 46 of 71		

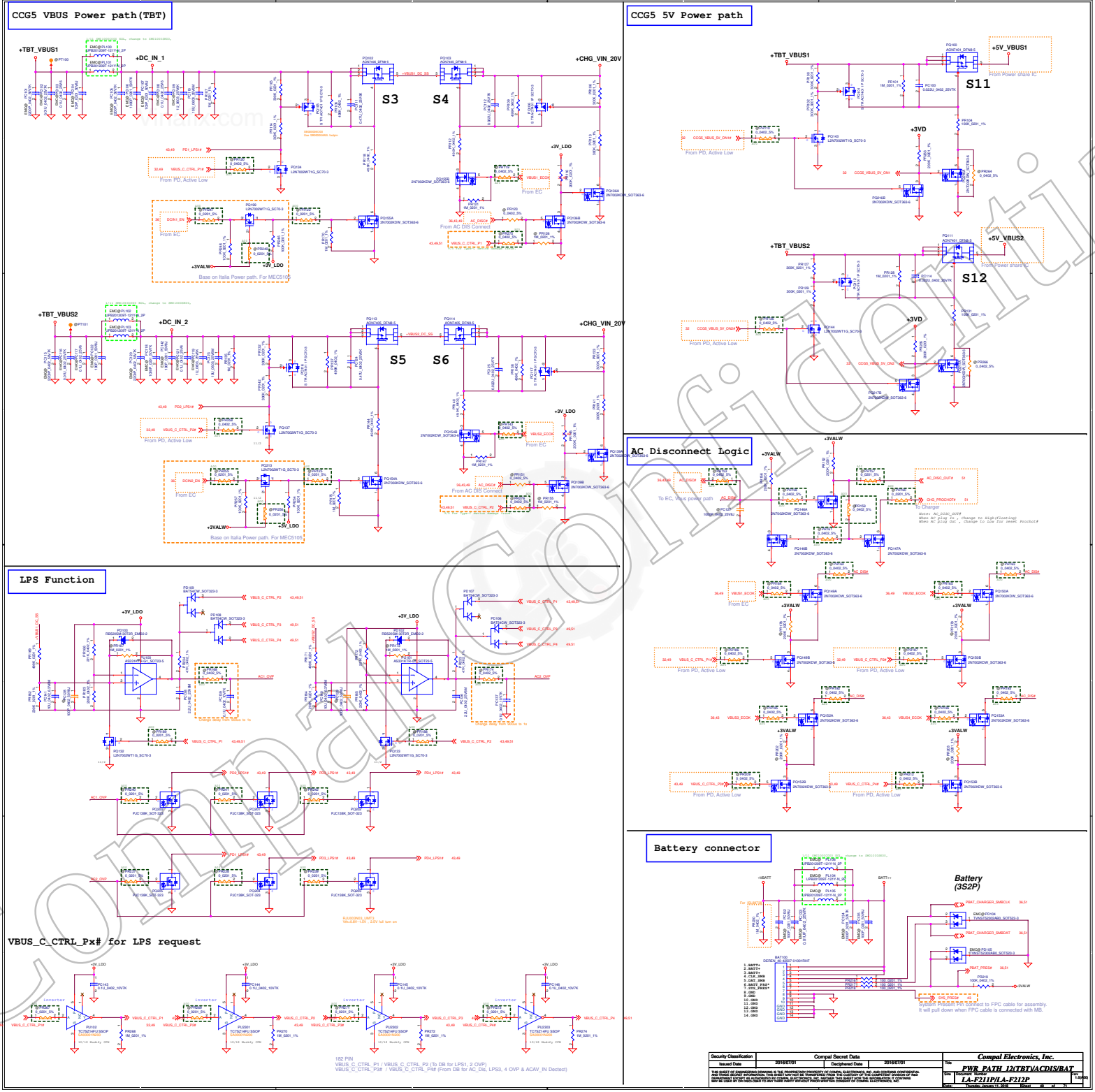


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date	2018/12/31
Title	PWR_Power Tree		
Size	Document Number		Rev
	LA-P211P		1.0(M0)
Date: Thursday, January 11, 2018	Sheet 47 of 71		

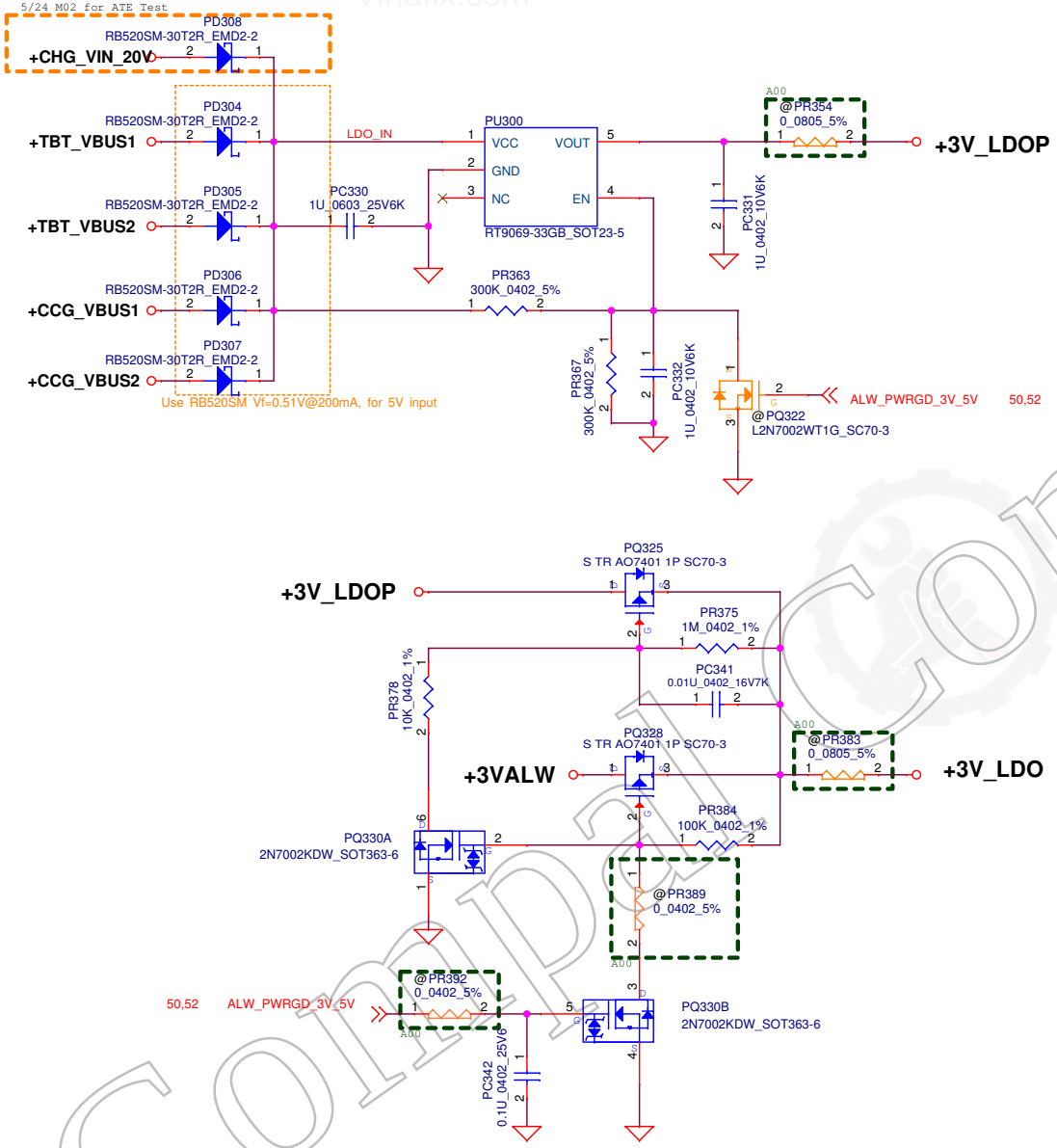


Security Classification	Compal Secret Data		
Issued Date	2016/07/01	Deciphered Date	2016/07/01

Compal Electronics, Inc.	
Title	Power_Block_diagram
Size	Document Number
Rev	1.0(A00)
Date: Thursday, January 11, 2018	Sheet 48 of 71


CCG5 VBUS Power path(TBT)
+TBT_VBUS1
+DC_IN_1
+CHG_VIN_20V
S3
S4
+3V_LDO
+3VALW
Base on Italia Power path. For MEC5105
+TBT_VBUS2
+DC_IN_2
S5
S6
CCG5 5V Power path
+TBT_VBUS1
+5V_VBUS1
S11
+3VD
+TBT_VBUS2
+5V_VBUS2
S12
AC Disconnect Logic
+3VALW
LPS Function
+3V_LDO
VBUS_C_CTRL_Px# for LPS request
Battery connector
Battery
(3S2P)
Compal Confidential

3V LDO



Compal Electronics, Inc.		
Title: PWR_+3V_LDO		
Size: B	Document Number: LA-F211P/LA-F212P	Rev: 1.0(A00)
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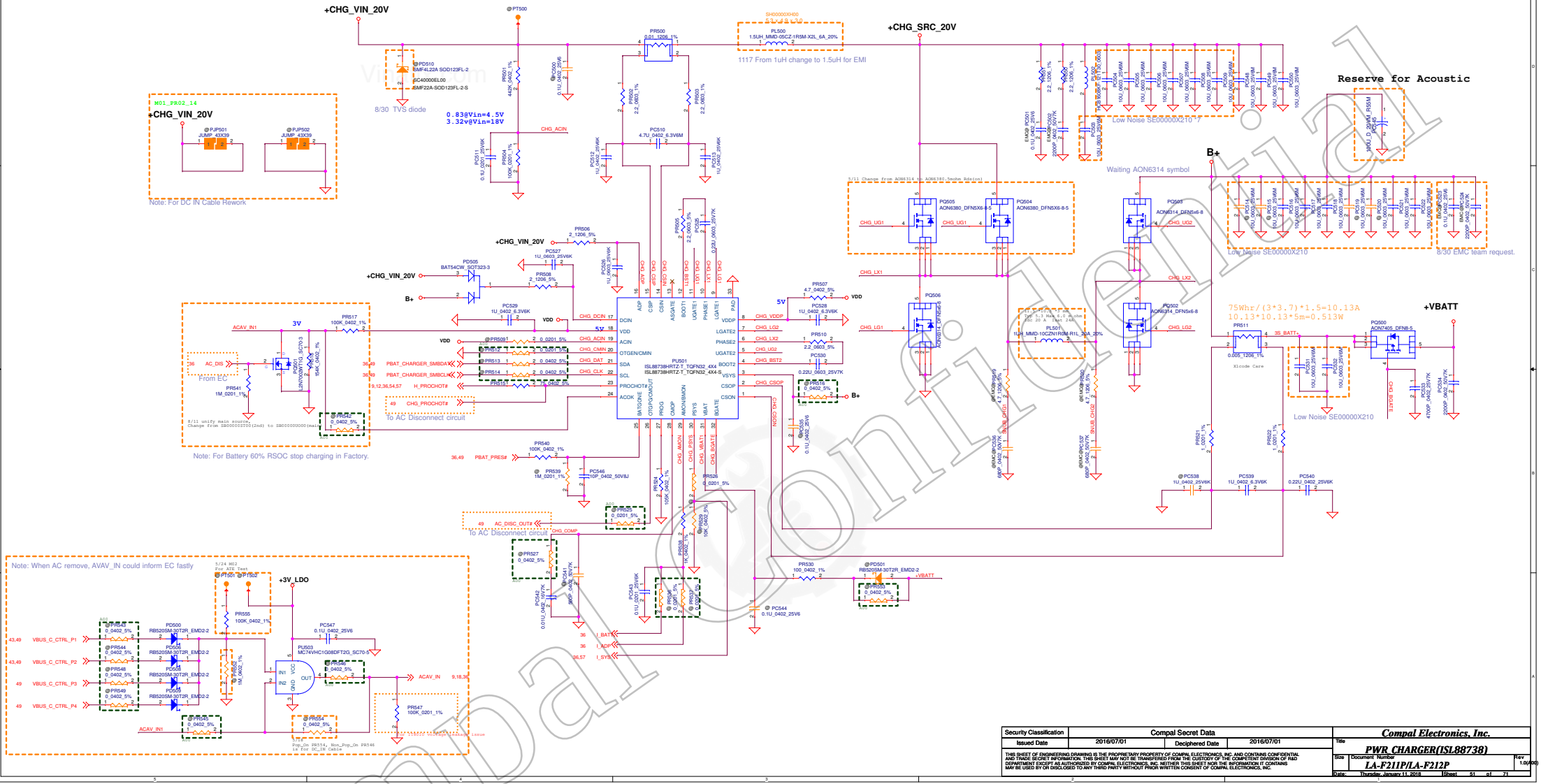
Charger controller(40.1), Support component(40.2)



Security Classification	Compal Secret Data		
Issued Date	2016/07/01	Deciphered Date	2016/07/01

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Compal Electronics, Inc.			
Title: PWR_CHARGER(ISL88738)			
Size:	Document Number: LA-F211P/LA-F212P		Rev: 1.0(A00)
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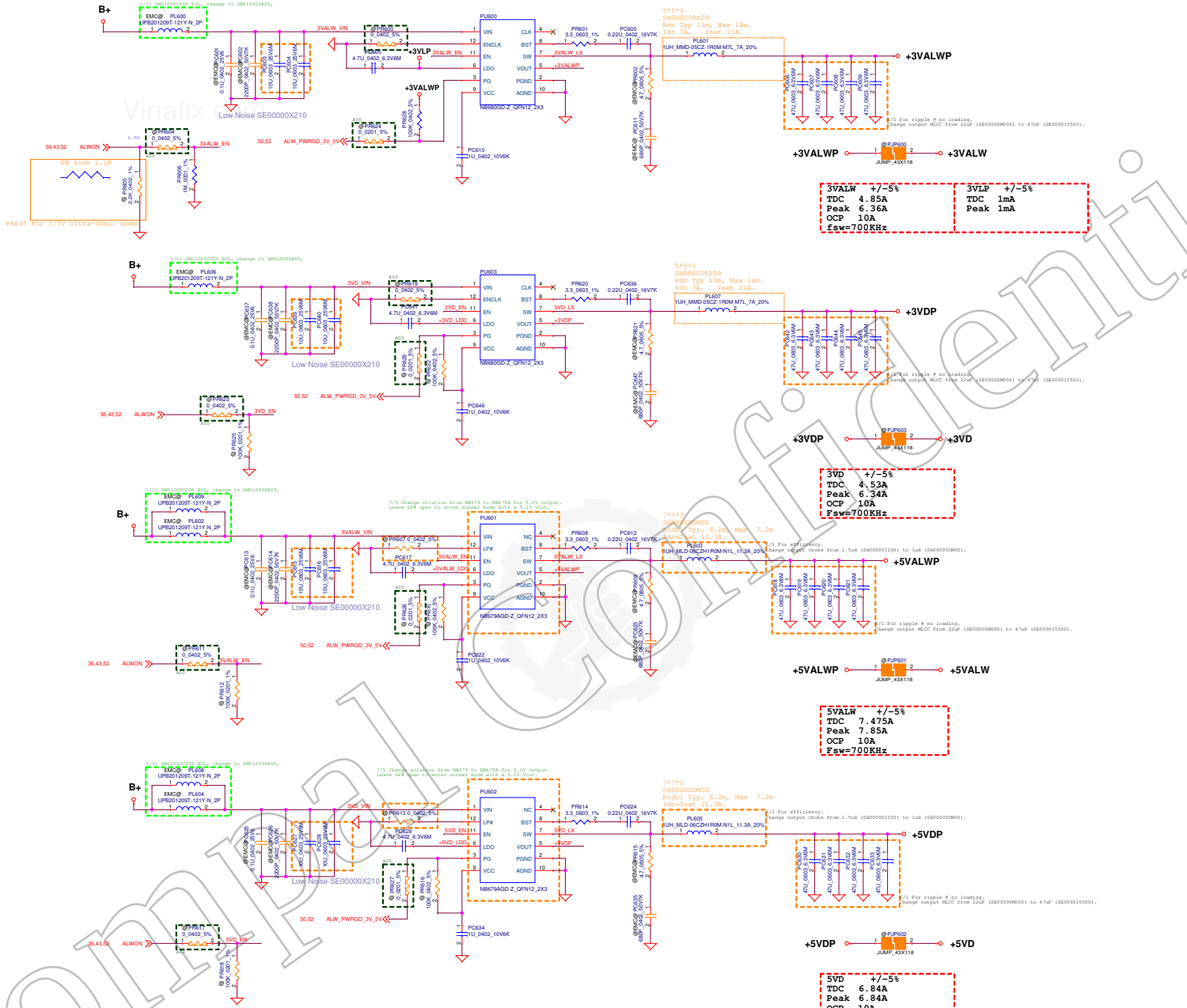


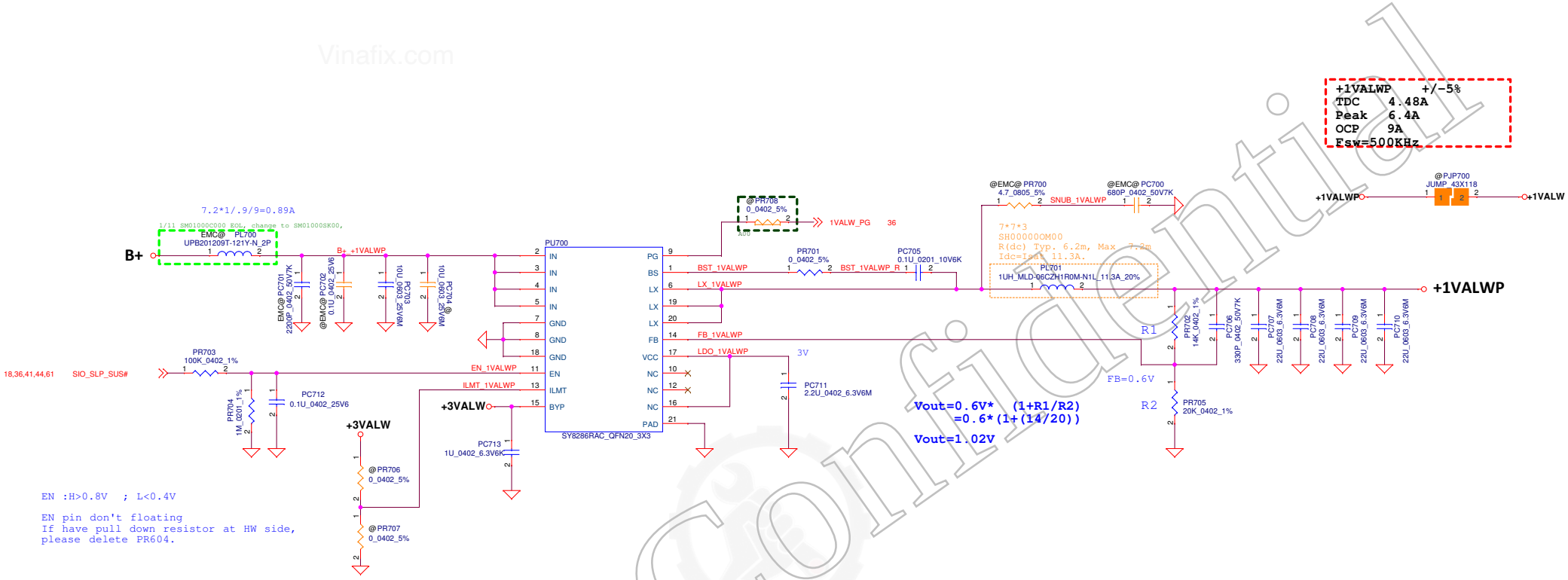
3V/5V controller(35.1), Support component(35.2)

Compal Electronics, Inc.

Title: PWR_+3VALWP/+3VDP/+5VALWP/+5VDP

Size: | Document Number: LA-F211P/LA-F212P | Rev: 1.0(000)

Date: Thursday, January 11, 2018 | Sheet 52 of 71



PWR.Plane.Regulator(35.25), Support component(35.26)

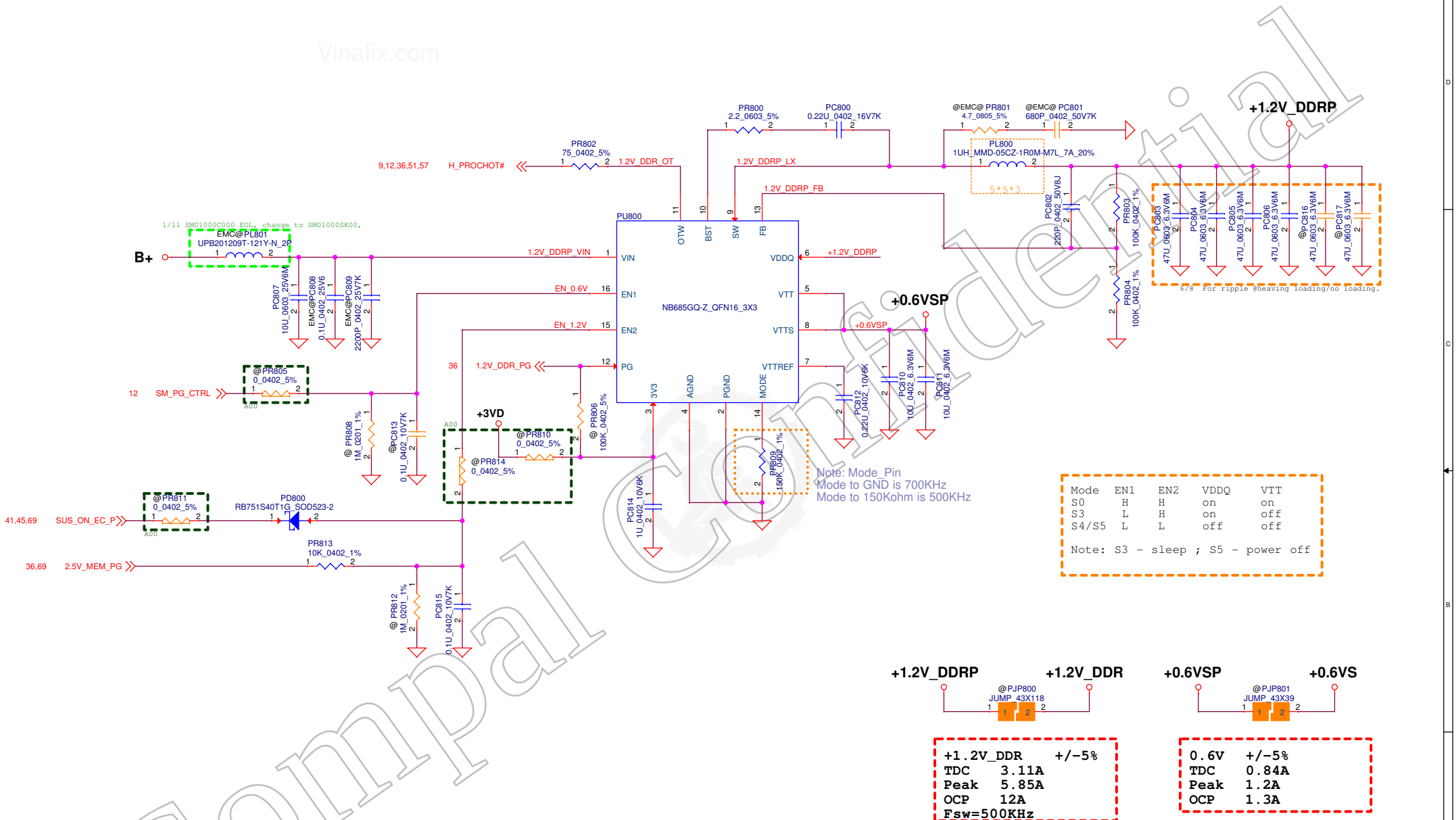
Security Classification	Compal Secret Data		
Issued Date	2016/07/01	Deciphered Date	2016/07/01

Compal Electronics, Inc.

Title: PWR_+1VALWP

Size | Document Number: LA-F211P/LA-F212P | Rev: 1.0(A00)

Date: Thursday, January 11, 2018 | Sheet 53 of 71

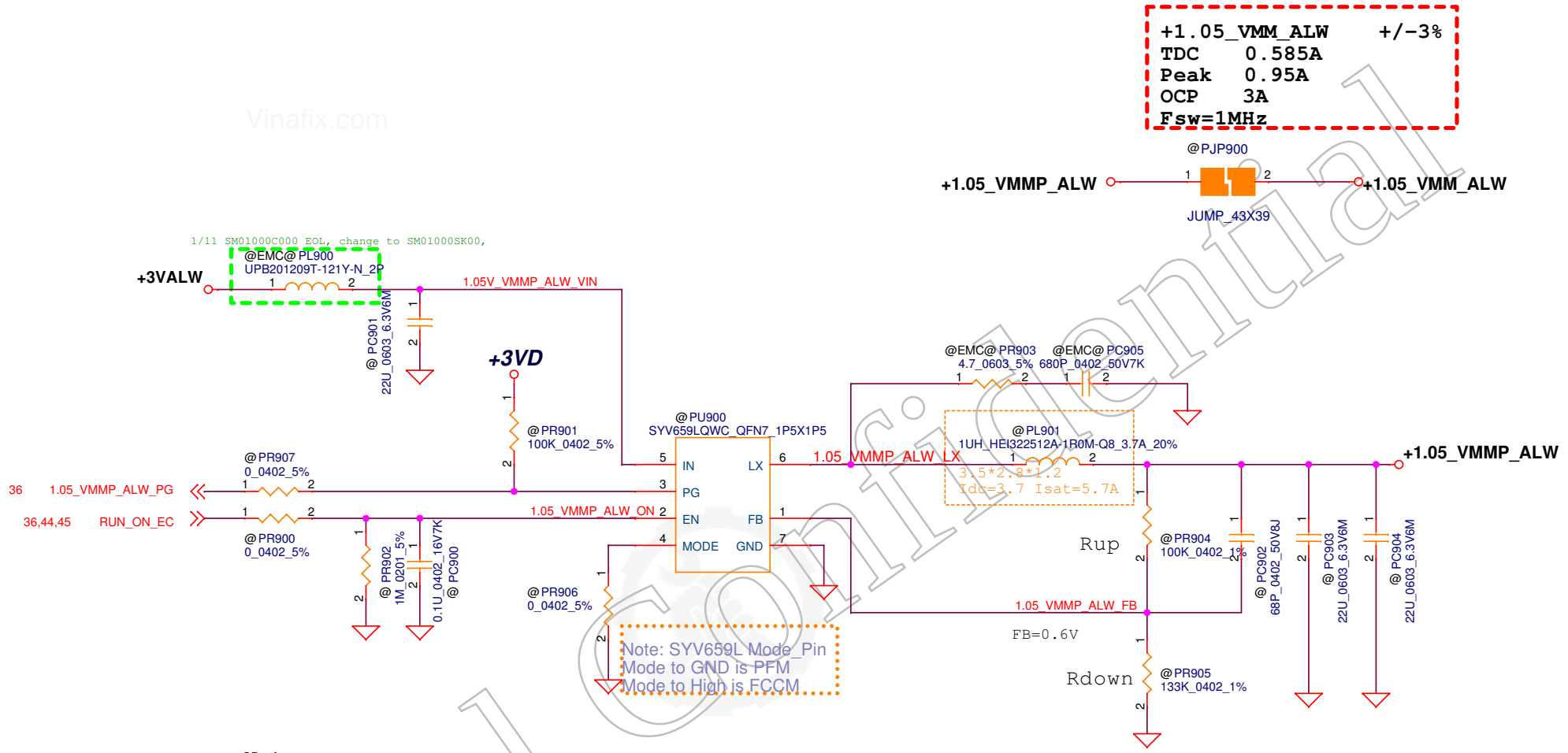


Compal Electronics, Inc.

Title: PWR_+1.2V_DDR/+0.6V

Size | Document Number: LA-F211P/LA-F212P | Rev: 1.0(A00)

Date: Thursday, January 11, 2018 | Sheet 54 of 71



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

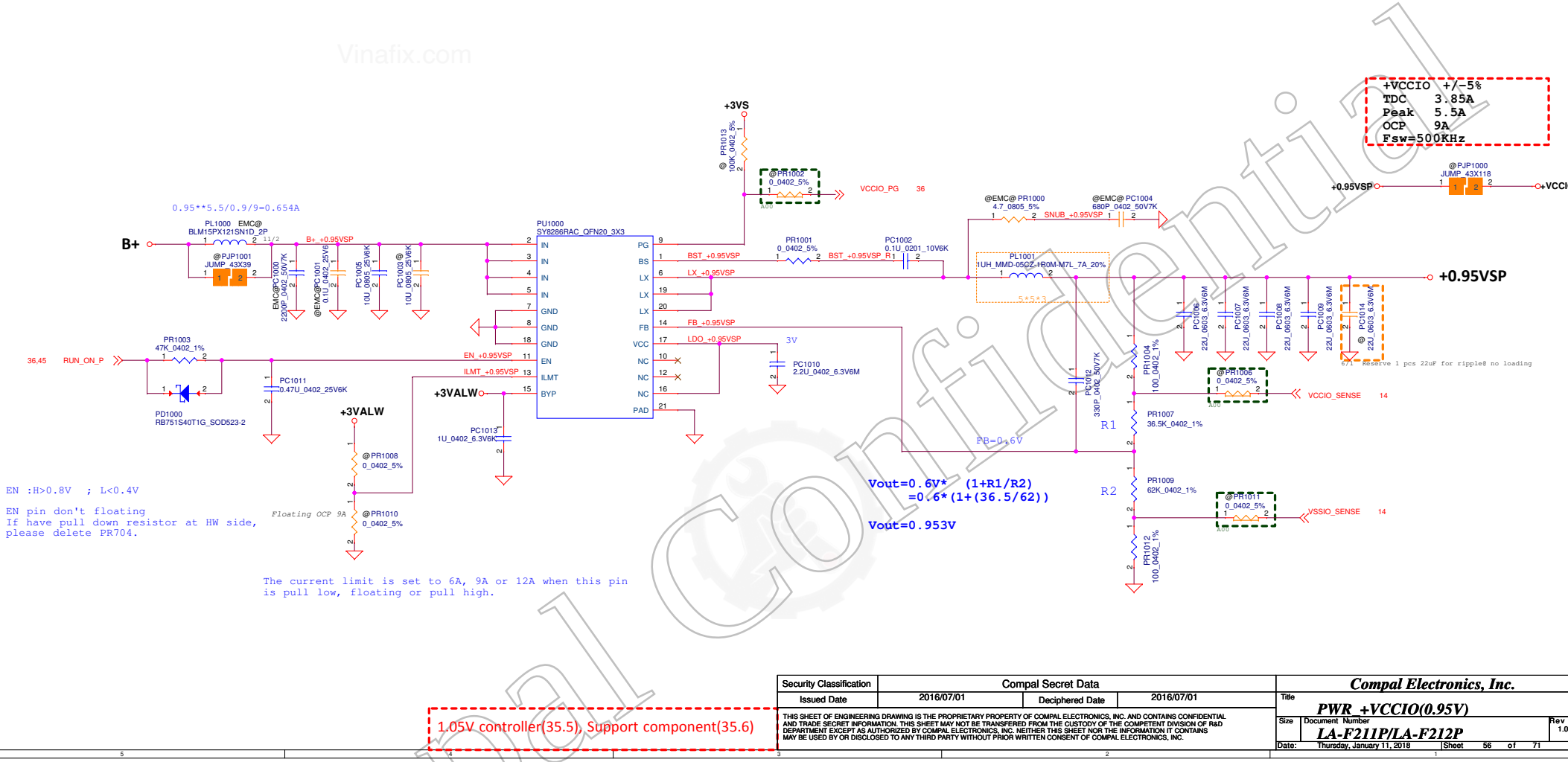
Security Classification	Compal Secret Data		
Issued Date	2016/07/01	Deciphered Date	2016/07/01

Compal Electronics, Inc.

Title: **PWR_+1.05V_VMM**

Size | Document Number: **LA-F211P/LA-F212P** | Rev: 1.0(A00)

Date: Thursday, January 11, 2018 | Sheet 55 of 71



Security Classification	Compal Secret Data		
Issued Date	2016/07/01	Deciphered Date	2016/07/01

Compal Electronics, Inc.			
Title	PWR +VCCIO(0.95V)		
Size	Document Number		Rev
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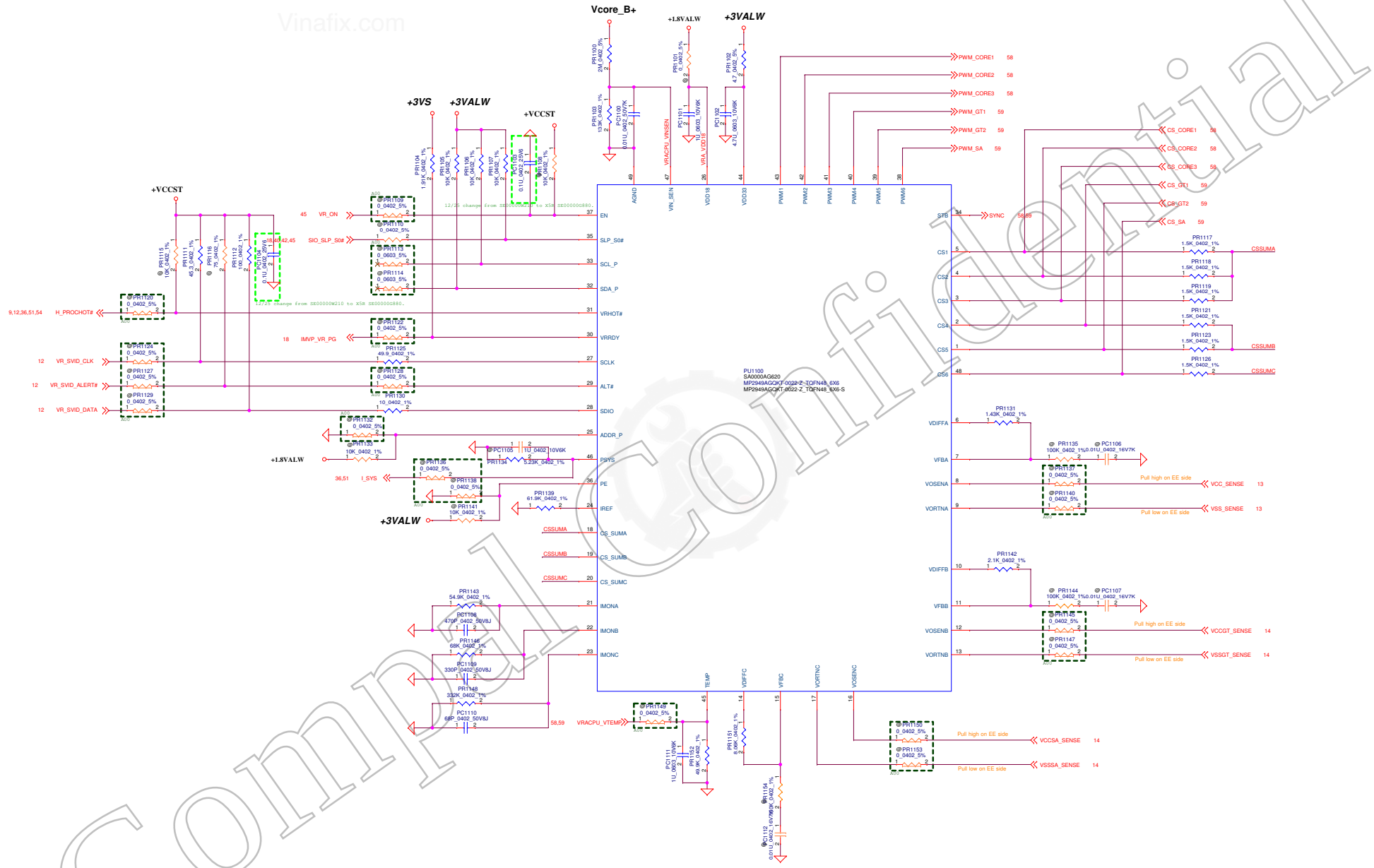
VCC_CORE controller(36.1), Drivers (36.2), Support component(36.3)



Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2014/12/05

Compal Electronics, Inc.	
Title	PWR_VCORE_MPS2949A
Size	Document Number: LA-F211P/LA-F212P
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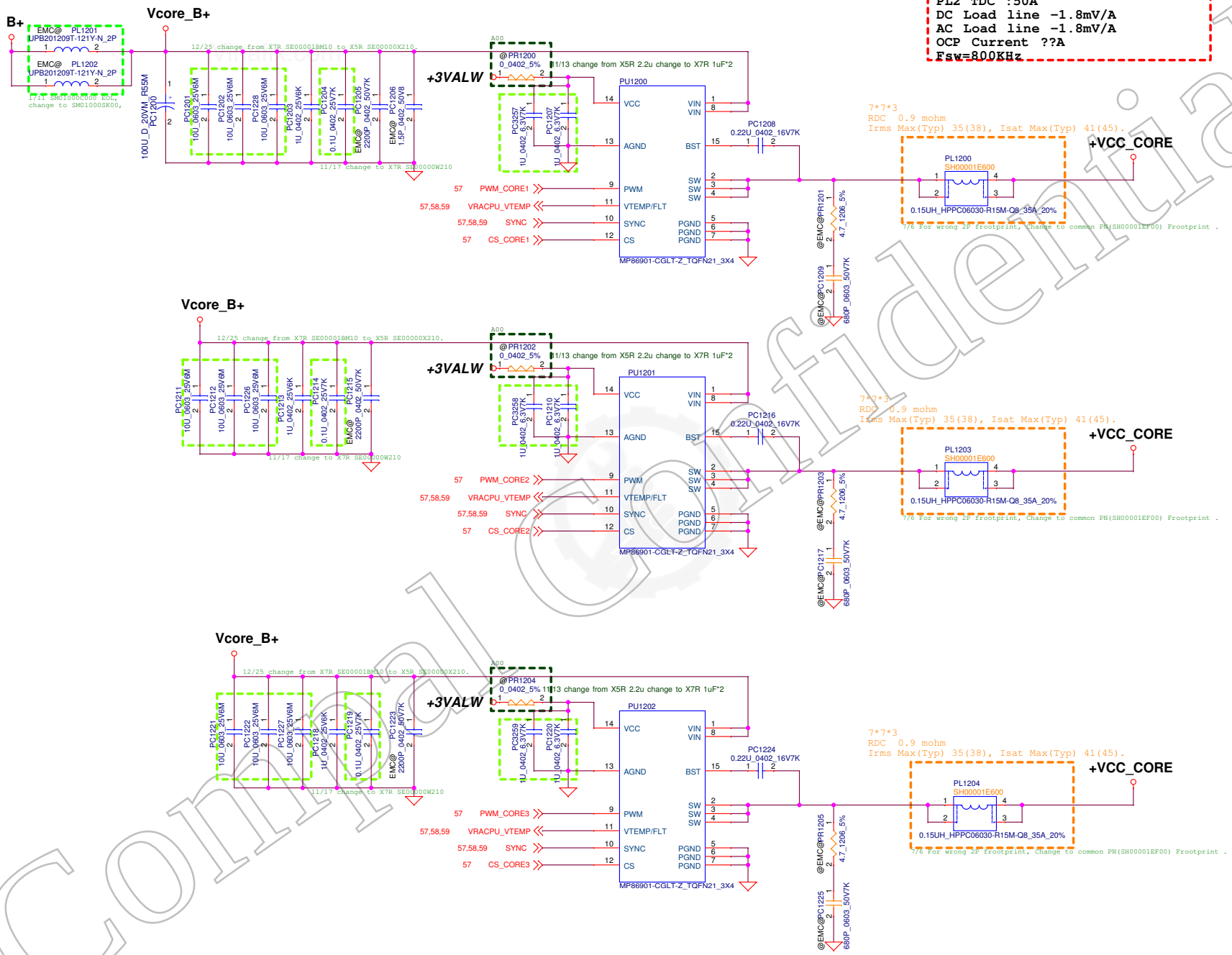
Date: Thursday, January 11, 2018	Sheet 57 of 71

VCC_CORE Dr. MOS (36.2), Support component(36.3)

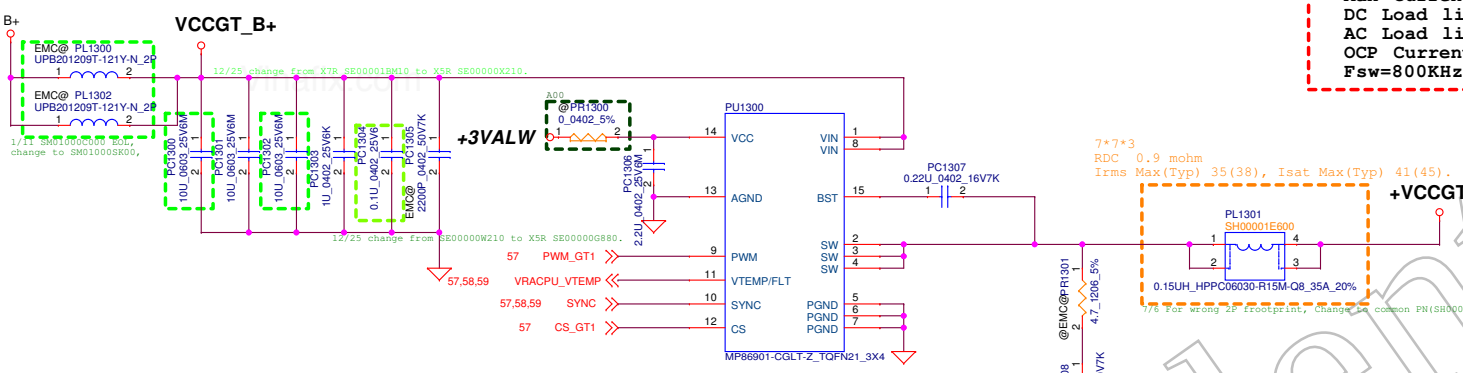
```
VCC_core (Base on PAG rev 0.5)
Peak Current 68A
PL2 TDC :50A
DC Load line -1.8mV/A
AC Load line -1.8mV/A
OCP Current ??A
Fsw=800KHz
```

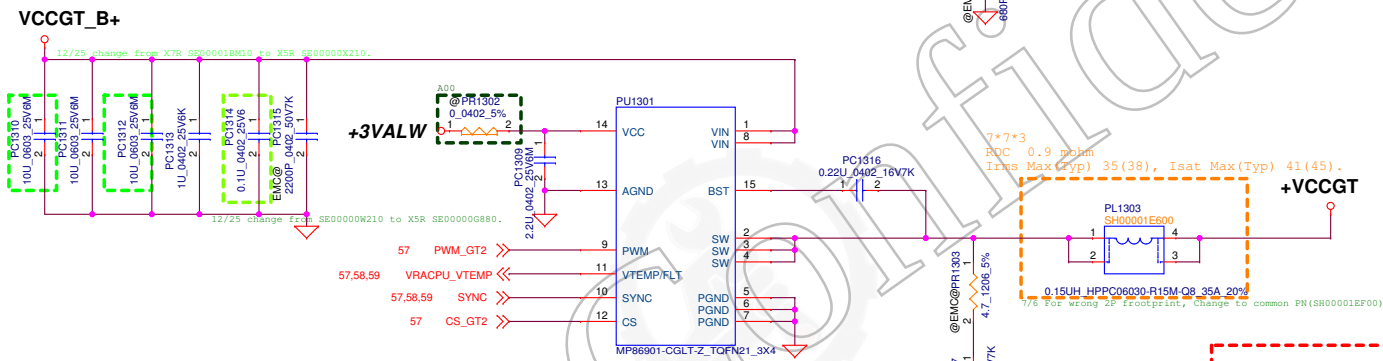


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date 2013/10/28	Title: PWR_+VCORE
			Size / Document Number: LA-F211P/LA-F212P — Rev: 1.0(400)
			Date: Thursday, January 11, 2018 — Sheet 58 of 71

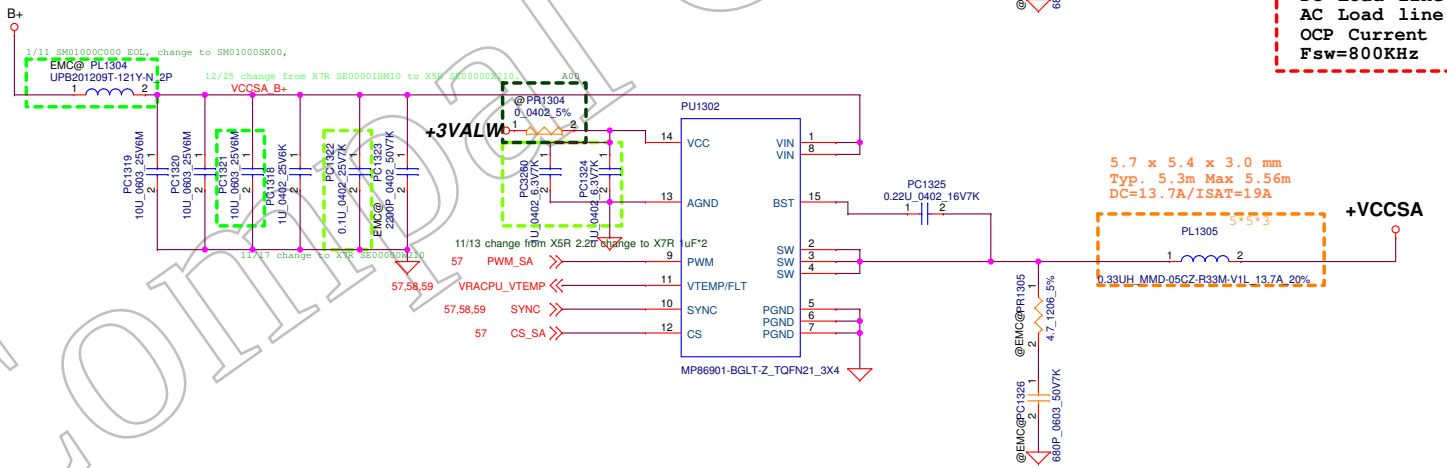
VCC_GT/SA Dr. MOS (36.2), Support component(36.3)

VCCGT (Base on PAG rev 0.5)
PL2 TDC_max :25A
Max Current 55A
DC Load line -2.7mV/A
AC Load line -2.7mV/A
OCP Current ??A
Fsw=800KHz





VCCSA (Base on PAG rev 0.5)
PL2 TDC_max :10A
Max Current 11.1A
DC Load line -10mV/A
AC Load line -10mV/A
OCP Current ??A
Fsw=800KHz



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	PWR_VCCGT/+VCCSA
Size	Document Number: LA-F211P/LA-F212P
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VCC_CORE

560uF 4.5mOhm*1
220uF 6 mOhm *2
22uF X6S_0603 ZRB *(5)
22uF X5R_0603 ZRB *(5@)
22uF X5R_0603 * (7+3@)
10uF X6S_0402 *(8+7@)
1uF X6S_0201 *20
0.1uF 0402 *2
100pF 0402 *2

VCCGT

330uF 9mohm *2
220uF *1
22uF X5R_0603 *(5+13@)
10uF X6S_0402 *12
1uF X6S_0201 *14
0.1uF 0402 *2
100pF 0402 *2

VCCSA

47uF X6S_0603*(4+2@)
22uF X6S_0603*8

+VCC_CORE

12/28
22uF X6S (SE00001CA10) * 5 (Blue)
1/8
22uF X5R (SE00000M020) * (5@) (Green)

12/25
10uF X5R (SE00000UD00) * (8+7@).

10/18
1uF X5R (SE00000UC00) * 20.

Intel Recommend
Close to SOC

+VCCGT

12/25
22uF X5R (SE00000M000) * (5+13@).

10/18
10uF X5R (SE00000UD00) * 12.

10/18
1uF X5R (SE00000UC00) * 14.

Intel Recommend
Close to SOC

+VCCSA

12/25
22u X6S (SE00001CA00) * (2+1@).
22u X5R (SE00000M000) * (10+1@).

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_CPU_VR_DECOUPLING

Size	Document Number	Rev
	LA-F211P/LA-F212P	1.0(A00)

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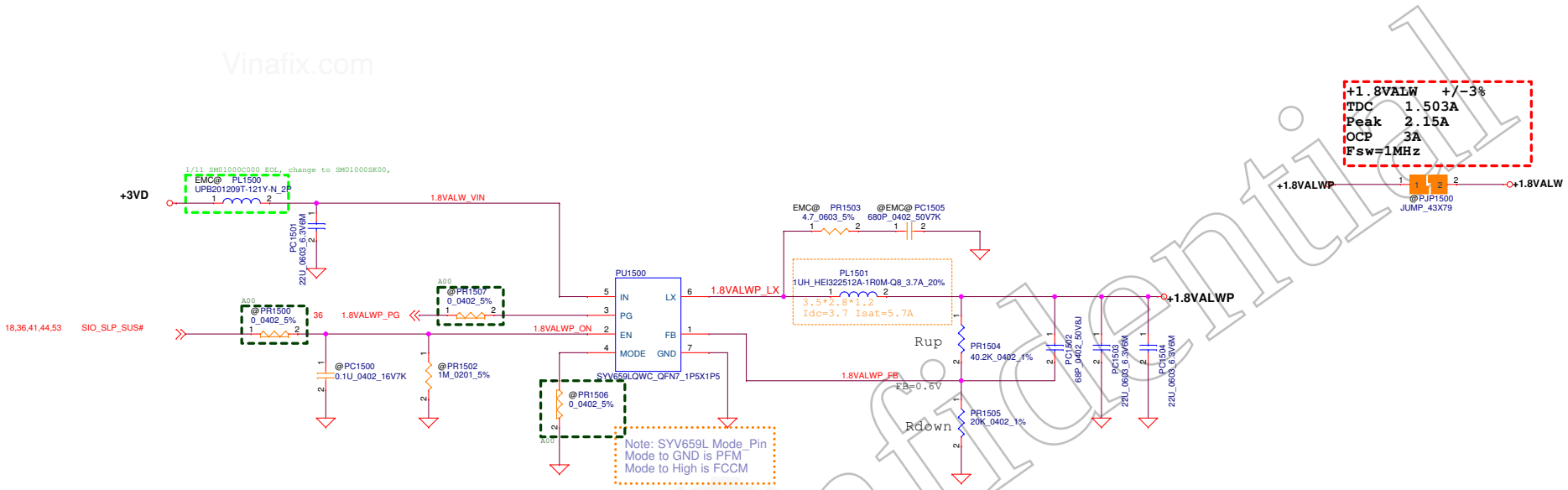

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

GPU other power_Regulatorr(43.7), Support component(43.8)

Security Classification	Compal Secret Data		
Issued Date	2016/07/01	Deciphered Date	2016/07/01

Compal Electronics, Inc.

Title: **PWR +1.8VALWP**

Size | Document Number: **LA-F211P/LA-F212P** | Rev: 1.0(A00)

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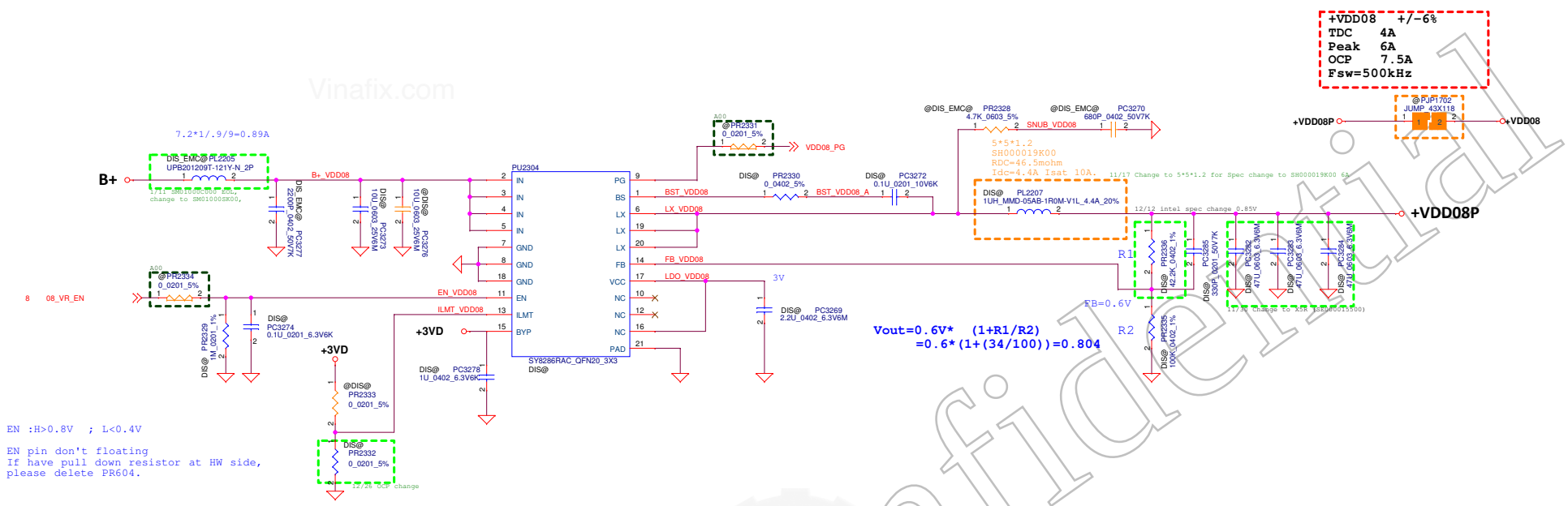
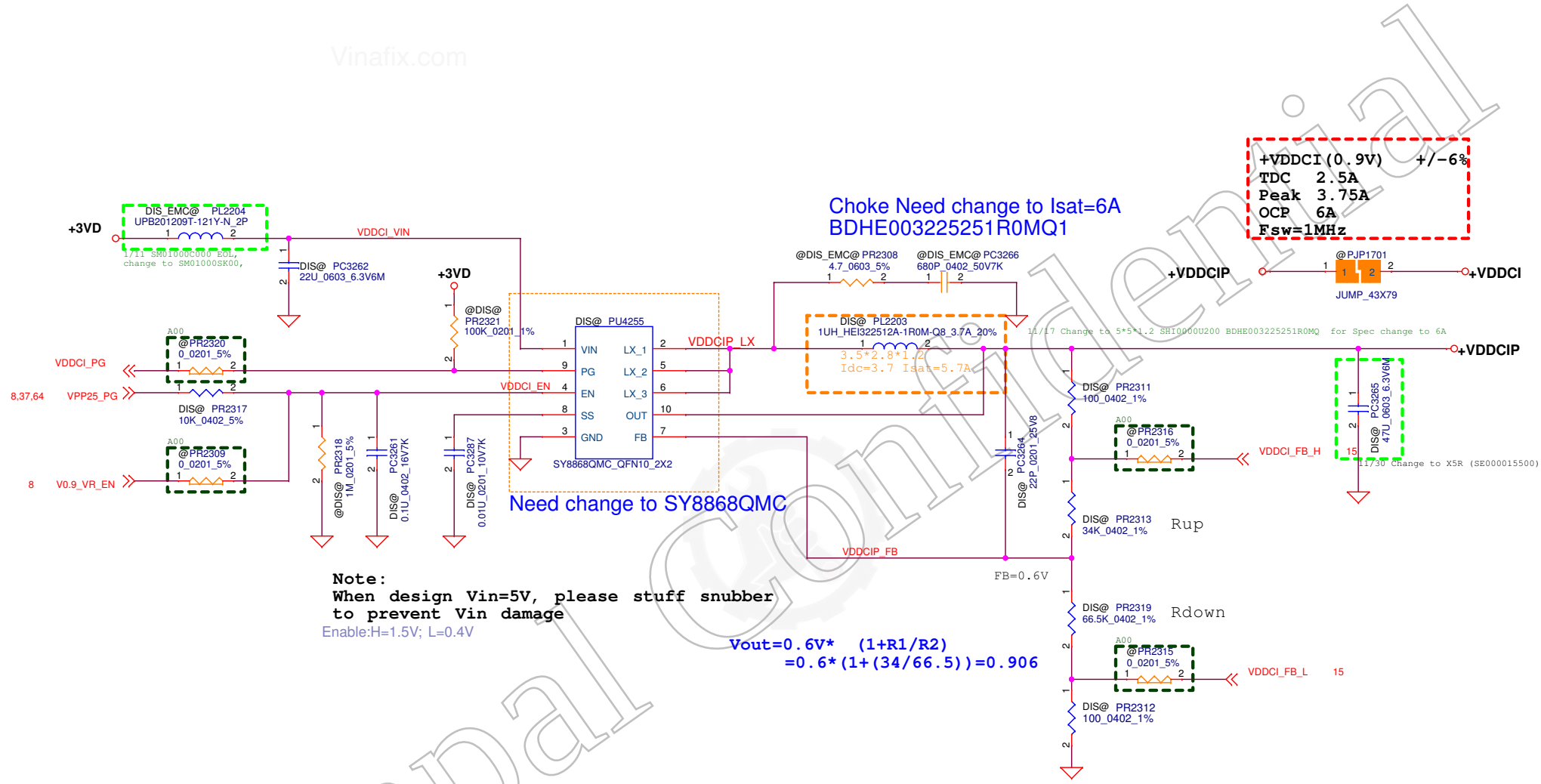


Title	<Title>	
Size C	Document Number <Doc>	Rev 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 62 of 71	



Title	<Title>		
Size B	Document Number <Doc>		Rev 1.0(A00)
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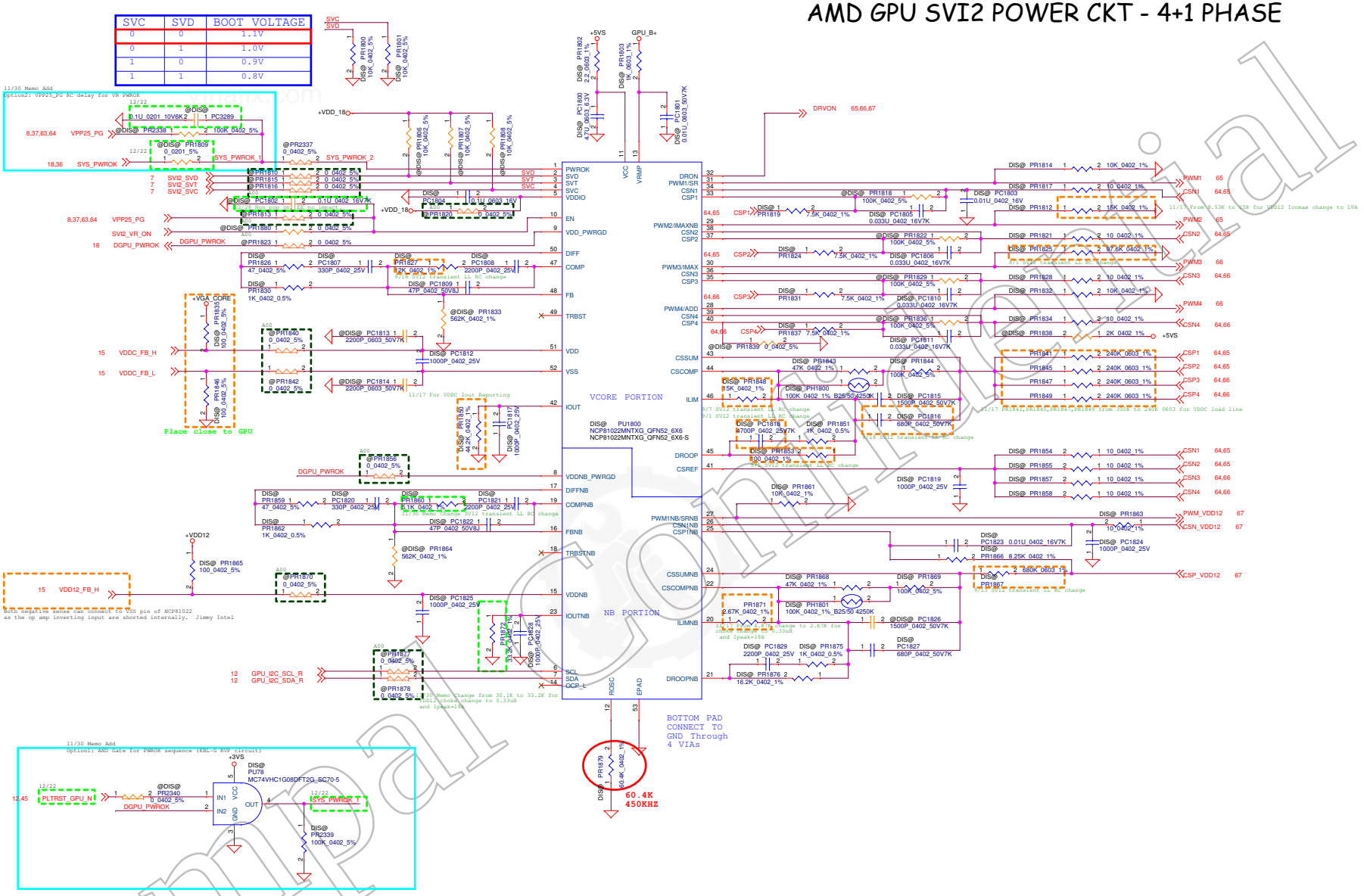
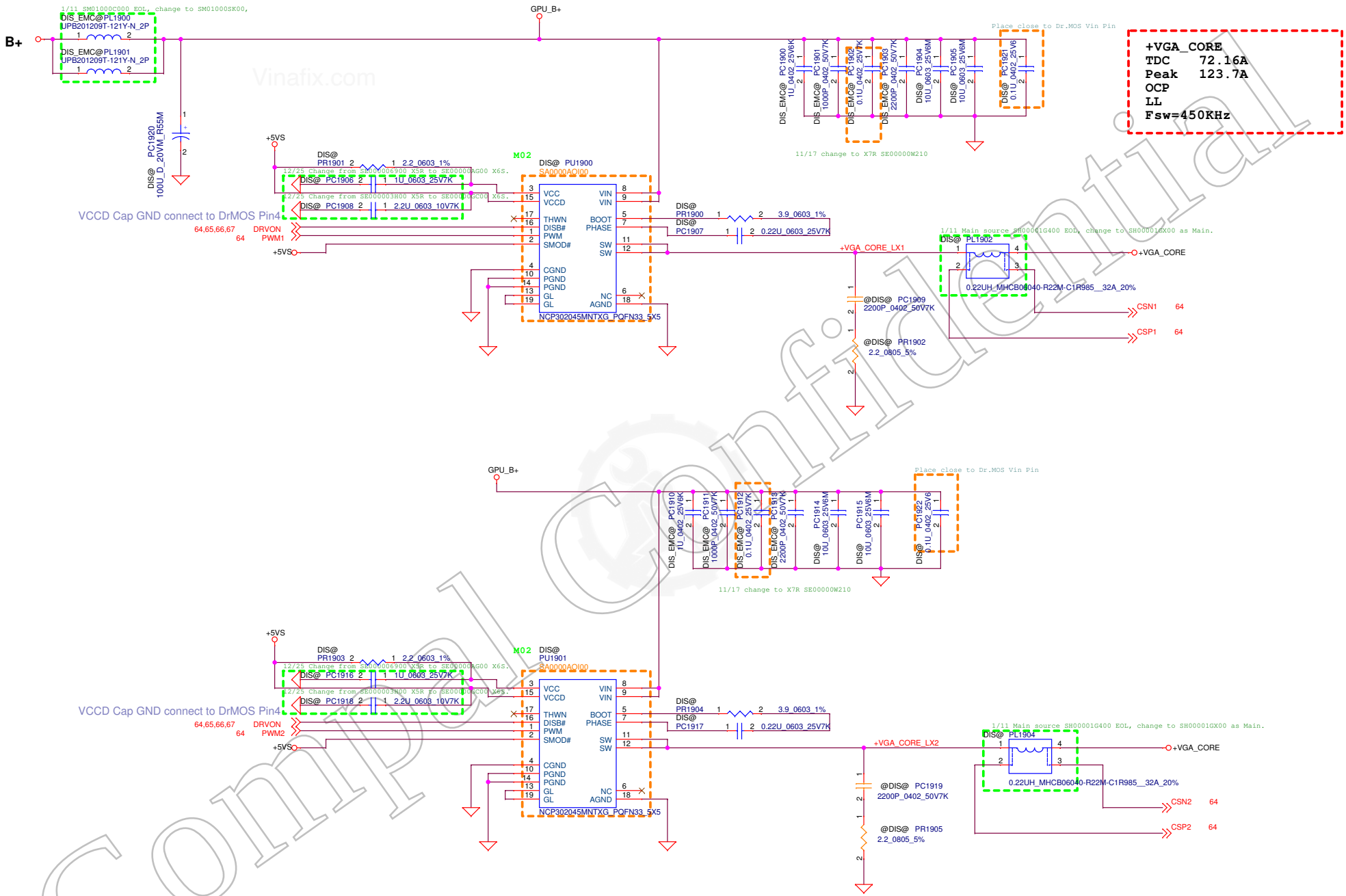
AMD GPU SVI2 POWER CKT - 4+1 PHASE

SVC	SVD	BOOT VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



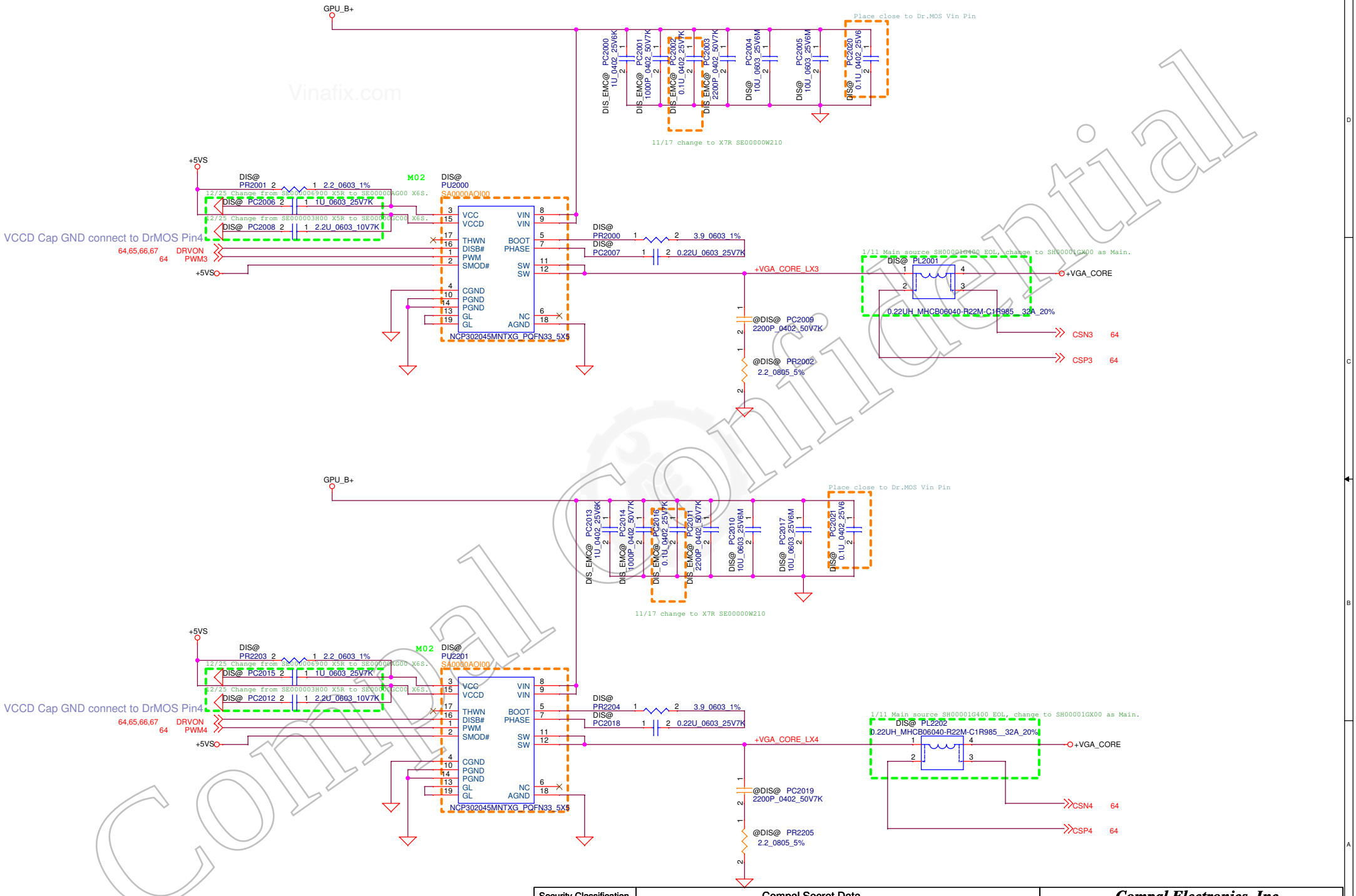
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR +VDDC NCP81022		
Size	Document Number		Rev
	LA-F211P/LA-F212P		1.0(A00)
Date: Thursday, January 11, 2018	Sheet 64 of 71		



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: PWR_+VDDC-Phase1&2			
Size	Document Number: LA-F211P/LA-F212P		Rev: 1.0(A00)
Date: Thursday, January 11, 2018	Sheet 65 of 71		



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+VDDC-Phase3&4**

Size | Document Number: **LA-F211P/LA-F212P** | Rev: 1.0(A00)

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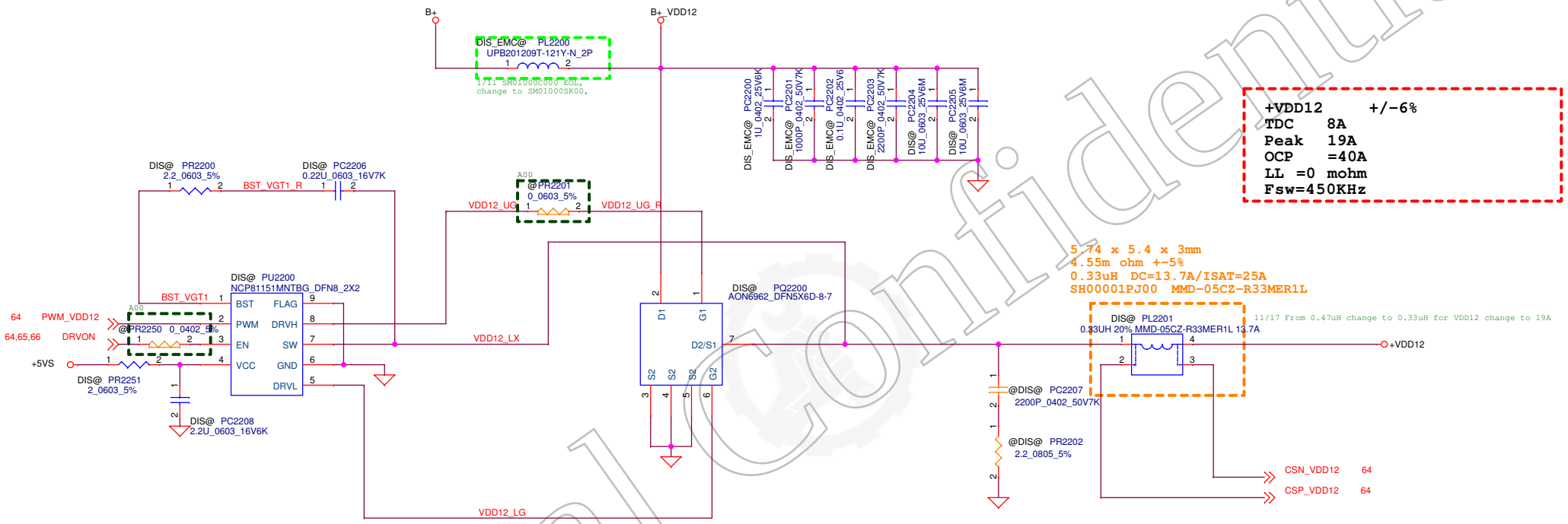

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+VDD12**

Size | Document Number: **LA-F211P/LA-F212P** | Rev: 1.0(A00)

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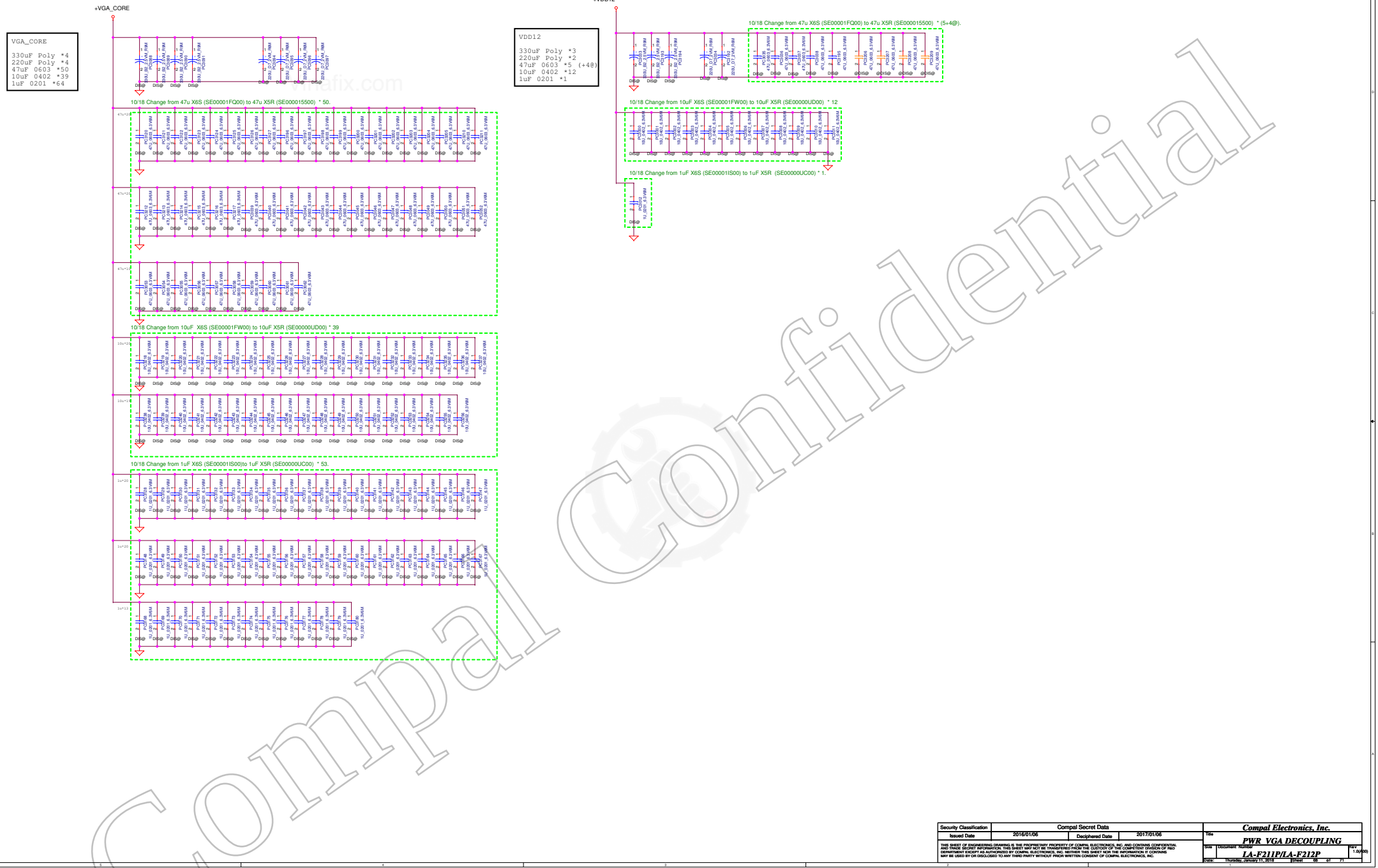
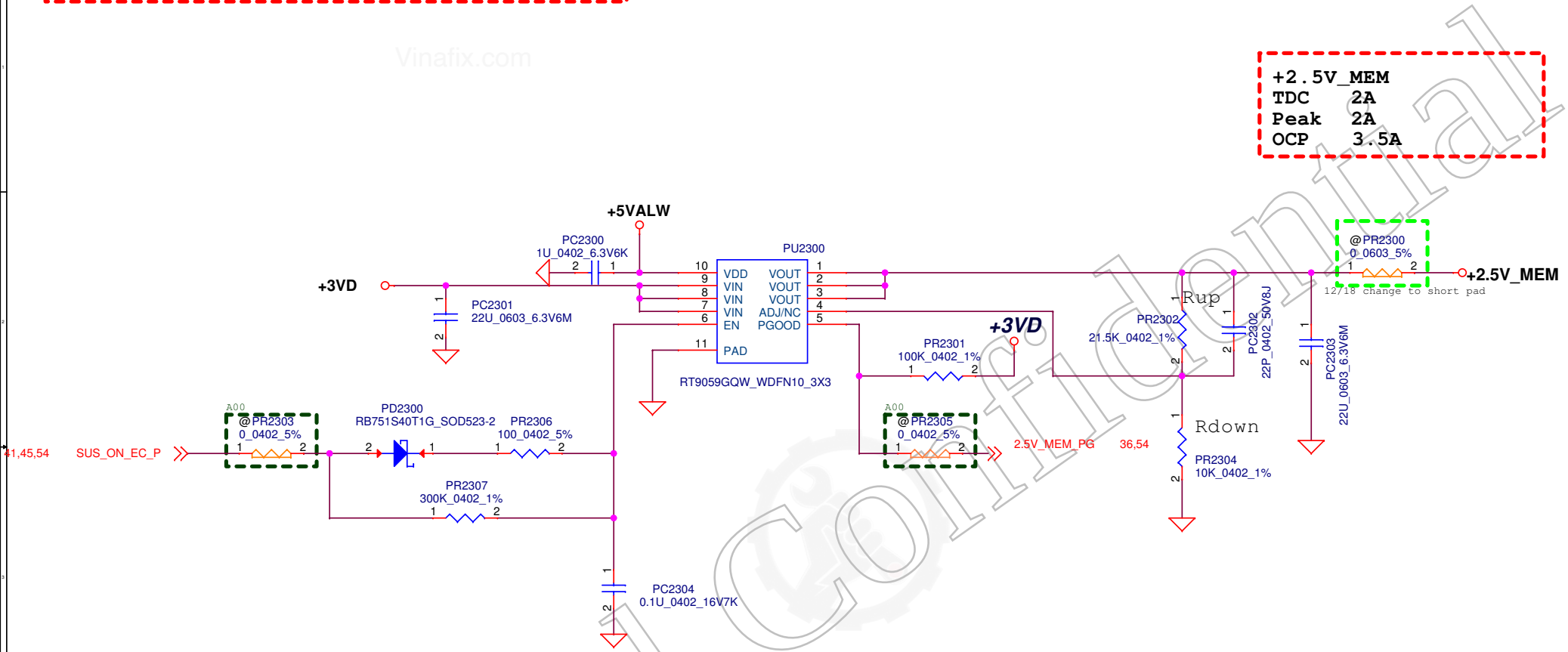


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date 2017/01/06	Title: PWR VGA DECOUPLING
			Size: Document Number: LA-F211P/LA-F212P Rev: 1.0(0G)
			Date: Thursday, January 11, 2018 Sheet 65 of 71

2.5V_MEM controller(35.13), Support component(35.14)



Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: **PWR_+2.5V_MEM_DDR4**

Size	Document Number	Rev
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