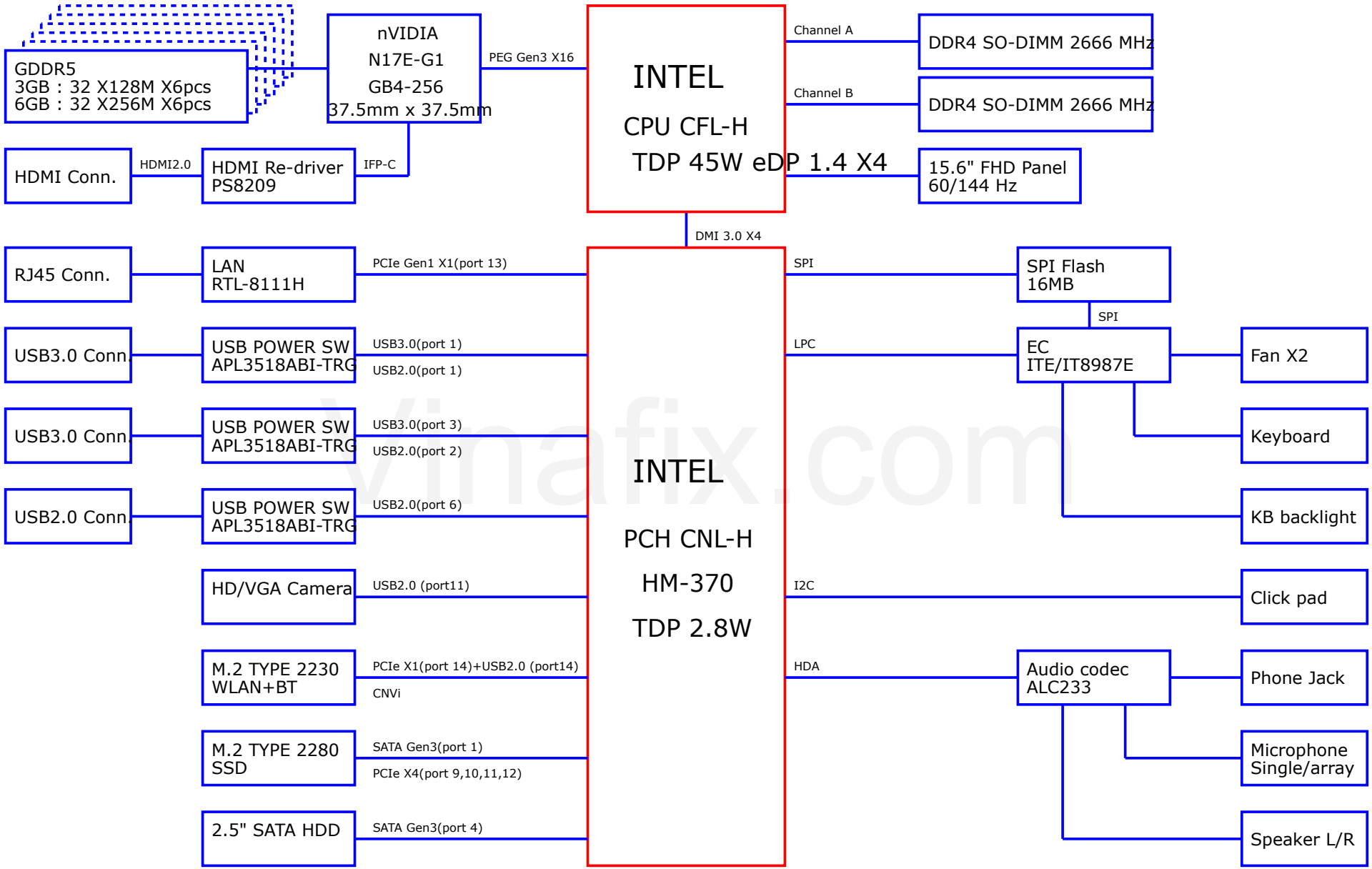
FX505GM Block Diagram



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Title BLOCK DIAGRAM

BG1-HW RD Div.2-HW RD Dept.1 Engineer:

Size	Project Name	Rev
Custom	FX505	1.0

Date: Monday, July 23, 2018 Sheet 1 of 99

I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		
I2C_1			
SMBUS	DDR Channel A(CON1601)		
	DDR Channel B(CON1701)		
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24780SRUYR	0X09
SMBUS1 (EC)	GPU		0X9E

PEGATRON Title : I2C MAP

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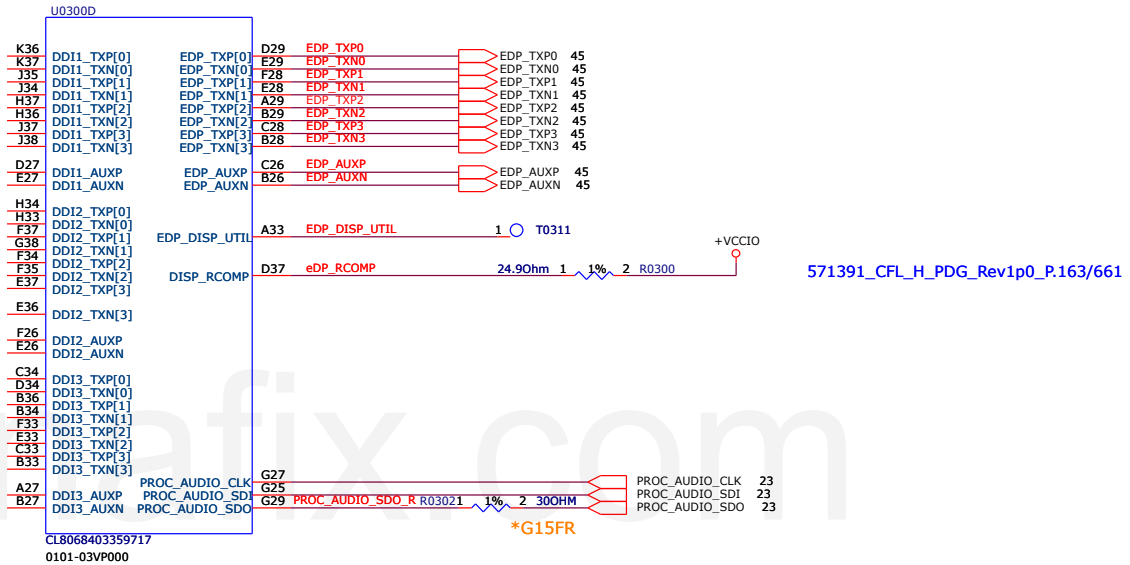
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0

Date: Monday, July 23, 2018 Sheet 2 of 99



571391_CFL_H_PDG_Rev1p0_P.163/661

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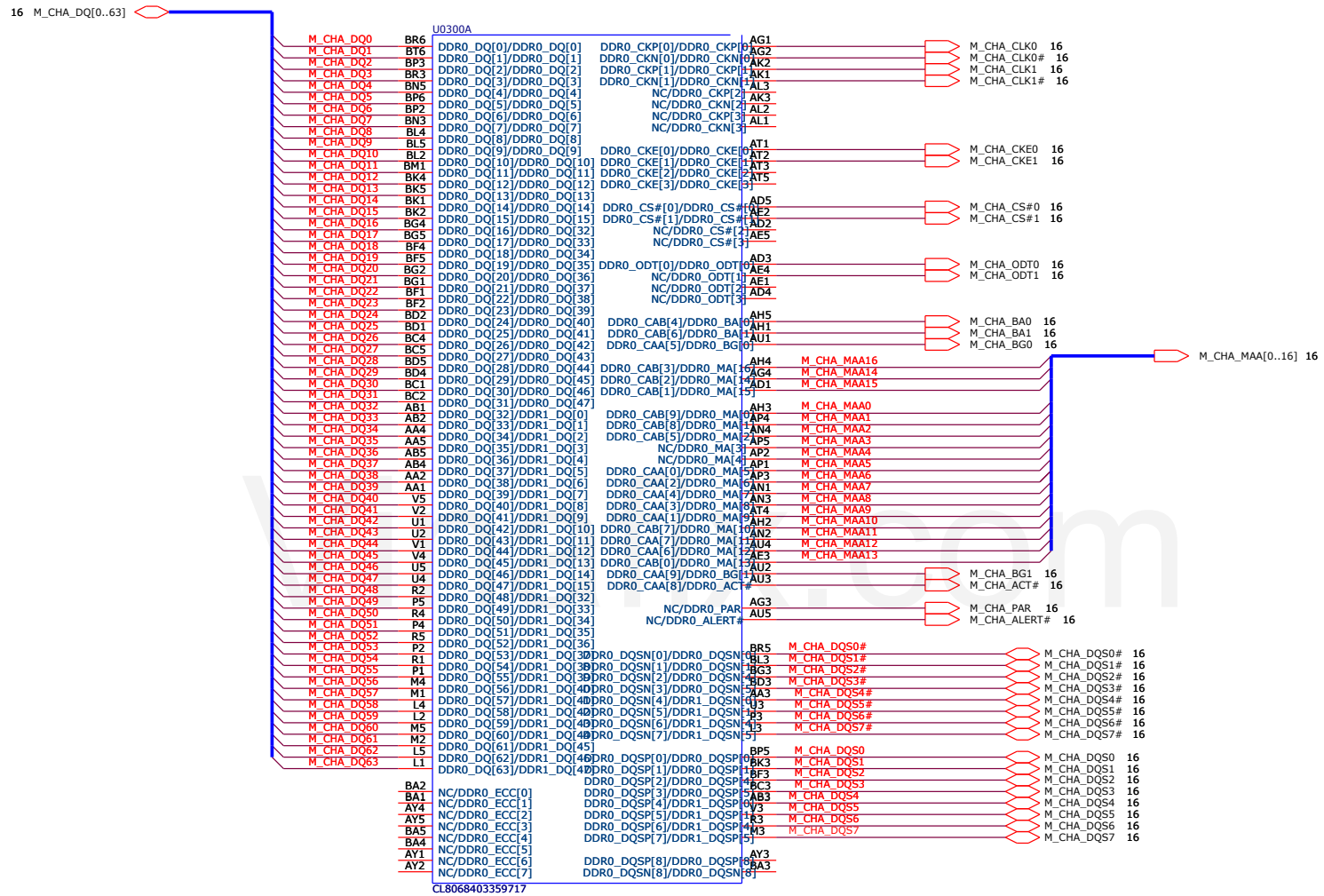
Title : DDI/EDP

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0

Date: Monday, July 23, 2018 Sheet 3 of 99



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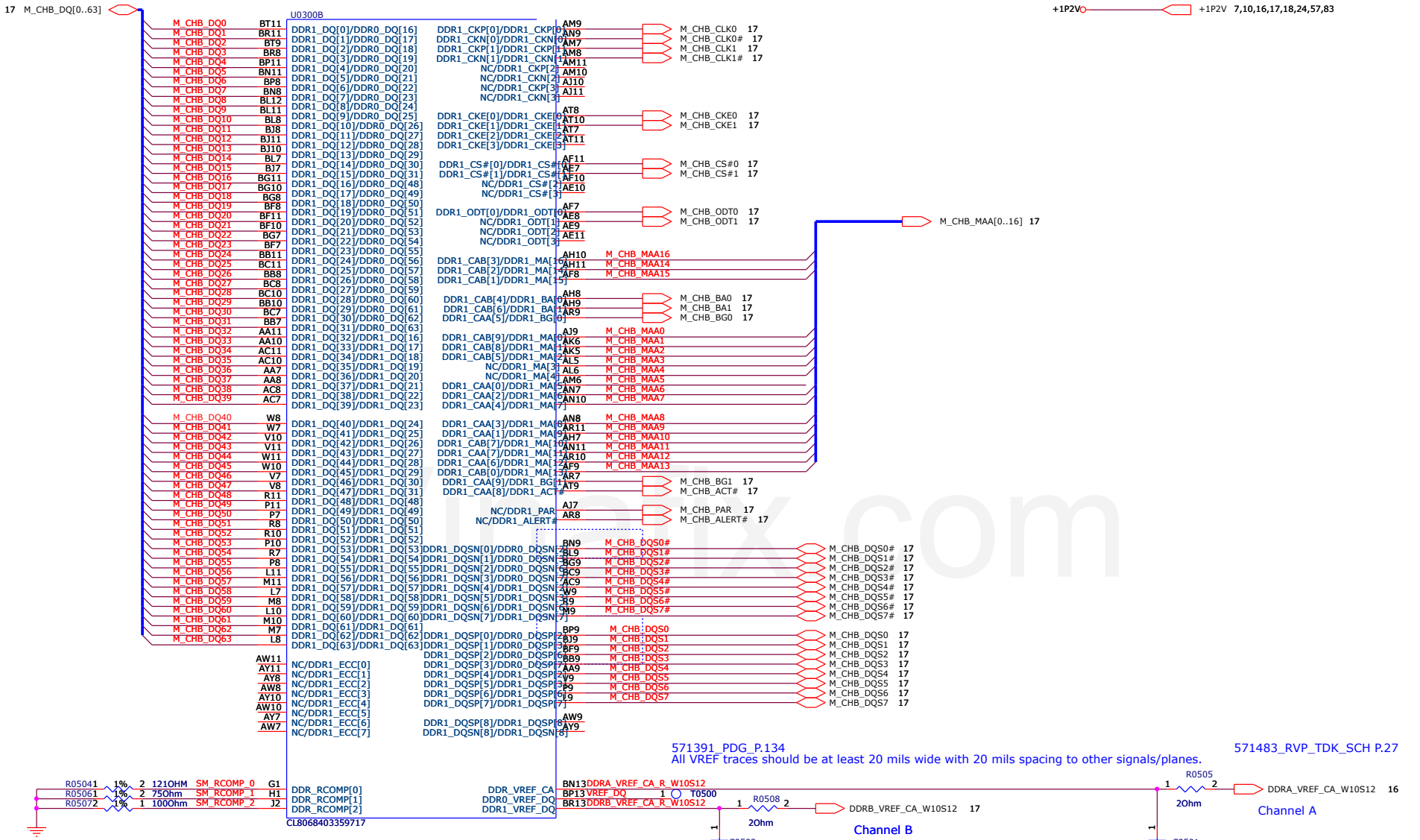
Title : DDR4 A

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

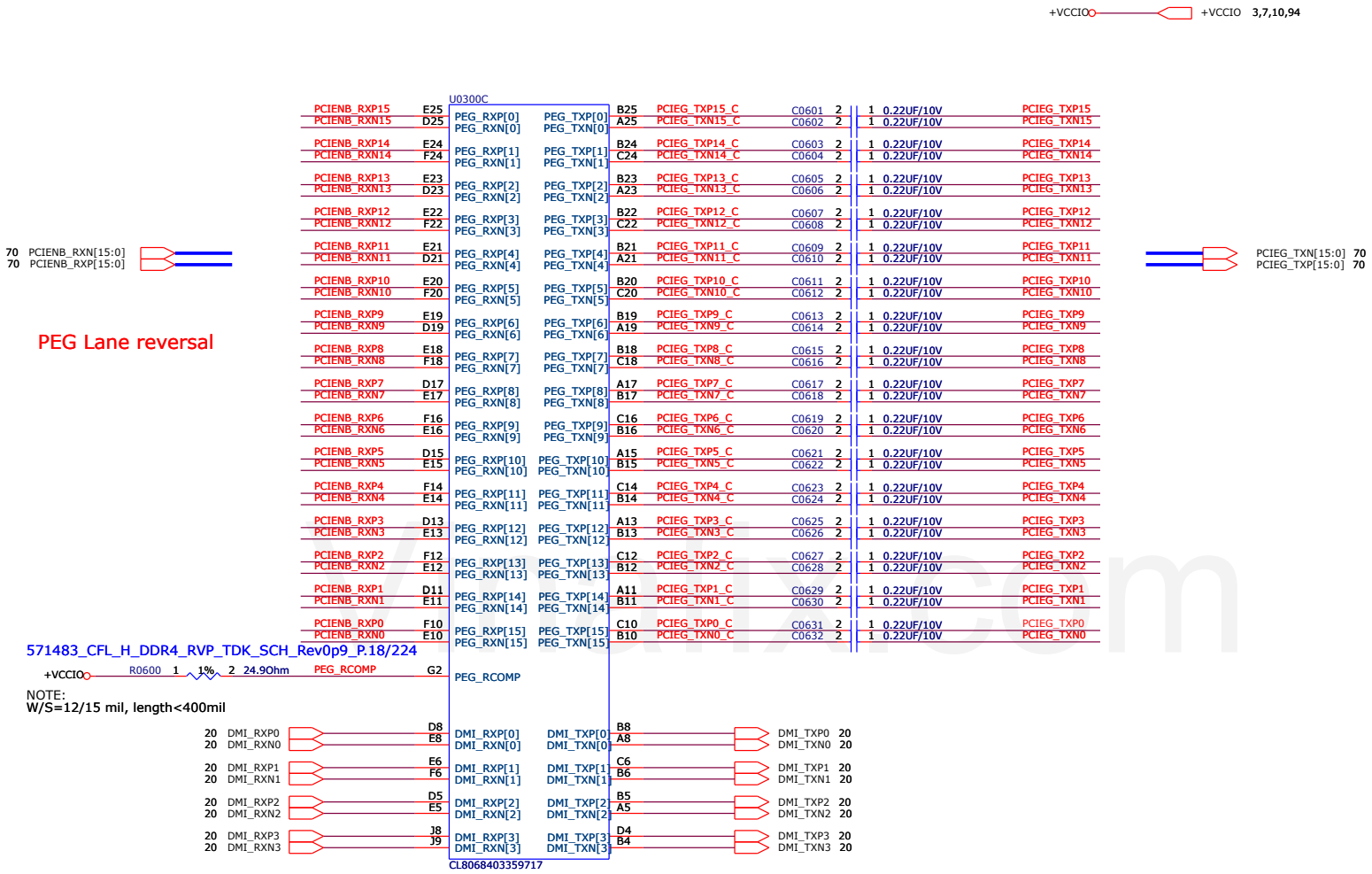
Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 4 of 99	



Title : DDR4 B

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 5 of 99	



PCIENB_RXP15	E25	PEG_RXP[0]	PEG_TXP[0]	B25	PCIEG_TXP15_C	C0601	2	1	0.22UF/10V	PCIEG_TXP15
PCIENB_RXN15	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PCIEG_TXN15_C	C0602	2	1	0.22UF/10V	PCIEG_TXN15
PCIENB_RXP14	E24	PEG_RXP[1]	PEG_TXP[1]	B24	PCIEG_TXP14_C	C0603	2	1	0.22UF/10V	PCIEG_TXP14
PCIENB_RXN14	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PCIEG_TXN14_C	C0604	2	1	0.22UF/10V	PCIEG_TXN14
PCIENB_RXP13	E23	PEG_RXP[2]	PEG_TXP[2]	B23	PCIEG_TXP13_C	C0605	2	1	0.22UF/10V	PCIEG_TXP13
PCIENB_RXN13	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PCIEG_TXN13_C	C0606	2	1	0.22UF/10V	PCIEG_TXN13
PCIENB_RXP12	E22	PEG_RXP[3]	PEG_TXP[3]	B22	PCIEG_TXP12_C	C0607	2	1	0.22UF/10V	PCIEG_TXP12
PCIENB_RXN12	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PCIEG_TXN12_C	C0608	2	1	0.22UF/10V	PCIEG_TXN12
PCIENB_RXP11	E21	PEG_RXP[4]	PEG_TXP[4]	B21	PCIEG_TXP11_C	C0609	2	1	0.22UF/10V	PCIEG_TXP11
PCIENB_RXN11	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PCIEG_TXN11_C	C0610	2	1	0.22UF/10V	PCIEG_TXN11
PCIENB_RXP10	E20	PEG_RXP[5]	PEG_TXP[5]	B20	PCIEG_TXP10_C	C0611	2	1	0.22UF/10V	PCIEG_TXP10
PCIENB_RXN10	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PCIEG_TXN10_C	C0612	2	1	0.22UF/10V	PCIEG_TXN10
PCIENB_RXP9	E19	PEG_RXP[6]	PEG_TXP[6]	B19	PCIEG_TXP9_C	C0613	2	1	0.22UF/10V	PCIEG_TXP9
PCIENB_RXN9	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PCIEG_TXN9_C	C0614	2	1	0.22UF/10V	PCIEG_TXN9
PCIENB_RXP8	E18	PEG_RXP[7]	PEG_TXP[7]	B18	PCIEG_TXP8_C	C0615	2	1	0.22UF/10V	PCIEG_TXP8
PCIENB_RXN8	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PCIEG_TXN8_C	C0616	2	1	0.22UF/10V	PCIEG_TXN8
PCIENB_RXP7	D17	PEG_RXP[8]	PEG_TXP[8]	A17	PCIEG_TXP7_C	C0617	2	1	0.22UF/10V	PCIEG_TXP7
PCIENB_RXN7	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PCIEG_TXN7_C	C0618	2	1	0.22UF/10V	PCIEG_TXN7
PCIENB_RXP6	F16	PEG_RXP[9]	PEG_TXP[9]	C16	PCIEG_TXP6_C	C0619	2	1	0.22UF/10V	PCIEG_TXP6
PCIENB_RXN6	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PCIEG_TXN6_C	C0620	2	1	0.22UF/10V	PCIEG_TXN6
PCIENB_RXP5	D15	PEG_RXP[10]	PEG_TXP[10]	A15	PCIEG_TXP5_C	C0621	2	1	0.22UF/10V	PCIEG_TXP5
PCIENB_RXN5	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PCIEG_TXN5_C	C0622	2	1	0.22UF/10V	PCIEG_TXN5
PCIENB_RXP4	F14	PEG_RXP[11]	PEG_TXP[11]	C14	PCIEG_TXP4_C	C0623	2	1	0.22UF/10V	PCIEG_TXP4
PCIENB_RXN4	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PCIEG_TXN4_C	C0624	2	1	0.22UF/10V	PCIEG_TXN4
PCIENB_RXP3	D13	PEG_RXP[12]	PEG_TXP[12]	A13	PCIEG_TXP3_C	C0625	2	1	0.22UF/10V	PCIEG_TXP3
PCIENB_RXN3	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PCIEG_TXN3_C	C0626	2	1	0.22UF/10V	PCIEG_TXN3
PCIENB_RXP2	F12	PEG_RXP[13]	PEG_TXP[13]	C12	PCIEG_TXP2_C	C0627	2	1	0.22UF/10V	PCIEG_TXP2
PCIENB_RXN2	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PCIEG_TXN2_C	C0628	2	1	0.22UF/10V	PCIEG_TXN2
PCIENB_RXP1	D11	PEG_RXP[14]	PEG_TXP[14]	A11	PCIEG_TXP1_C	C0629	2	1	0.22UF/10V	PCIEG_TXP1
PCIENB_RXN1	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PCIEG_TXN1_C	C0630	2	1	0.22UF/10V	PCIEG_TXN1
PCIENB_RXP0	F10	PEG_RXP[15]	PEG_TXP[15]	C10	PCIEG_TXP0_C	C0631	2	1	0.22UF/10V	PCIEG_TXP0
PCIENB_RXN0	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PCIEG_TXN0_C	C0632	2	1	0.22UF/10V	PCIEG_TXN0

D8	DMI_RXP[0]	DMI_TXP[0]	B8
E8	DMI_RXN[0]	DMI_TXN[0]	A8
E6	DMI_RXP[1]	DMI_TXP[1]	C6
F6	DMI_RXN[1]	DMI_TXN[1]	B6
D5	DMI_RXP[2]	DMI_TXP[2]	B5
E5	DMI_RXN[2]	DMI_TXN[2]	A5
J8	DMI_RXP[3]	DMI_TXP[3]	D4
J9	DMI_RXN[3]	DMI_TXN[3]	B4

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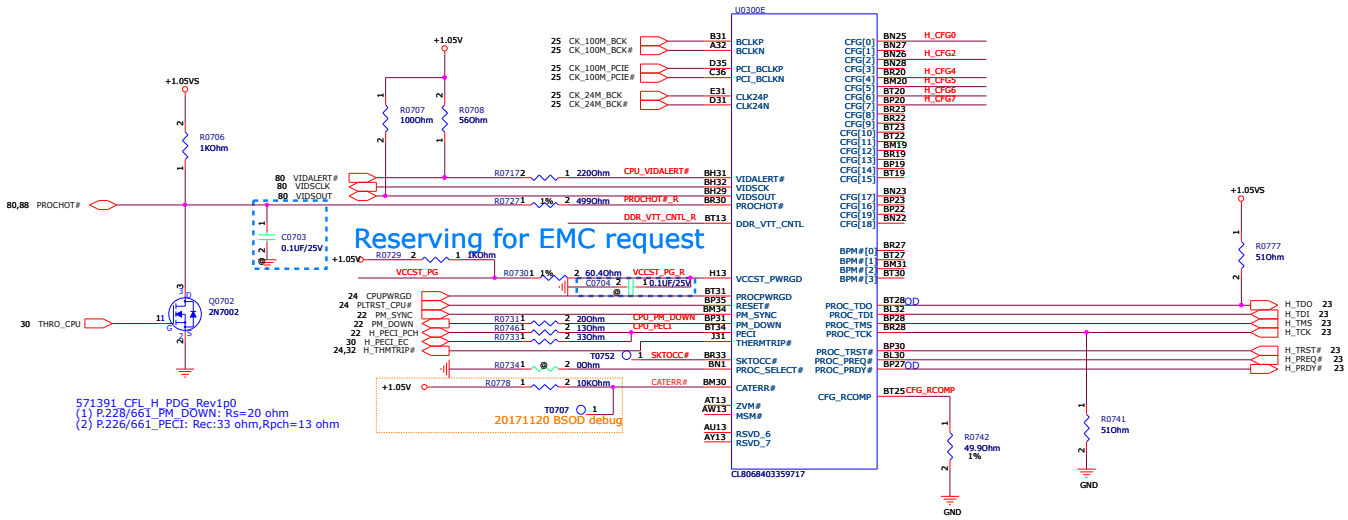
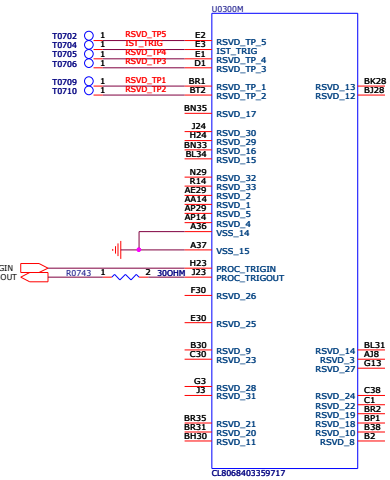
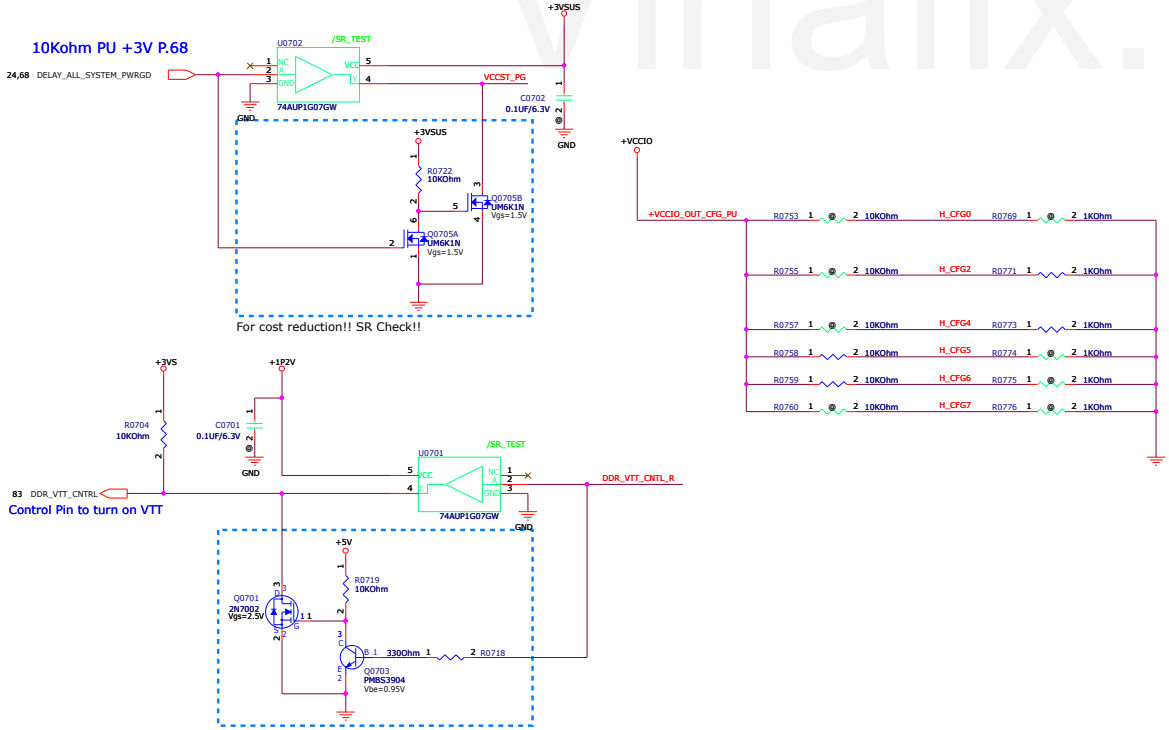
Title : DMI/PEG
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 6 of 99	





571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.17/224
571391_CFL_H_PDG_Rev1p0_P.224/661
VCCST_PWRGD



570805_CFL_Processor_EDS_Vol1_Rev_1.4_p.117/156

Table 6-7. Reset and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-Processor Line only and test point may be placed on the board for them.

PEGATRON Title : MISC
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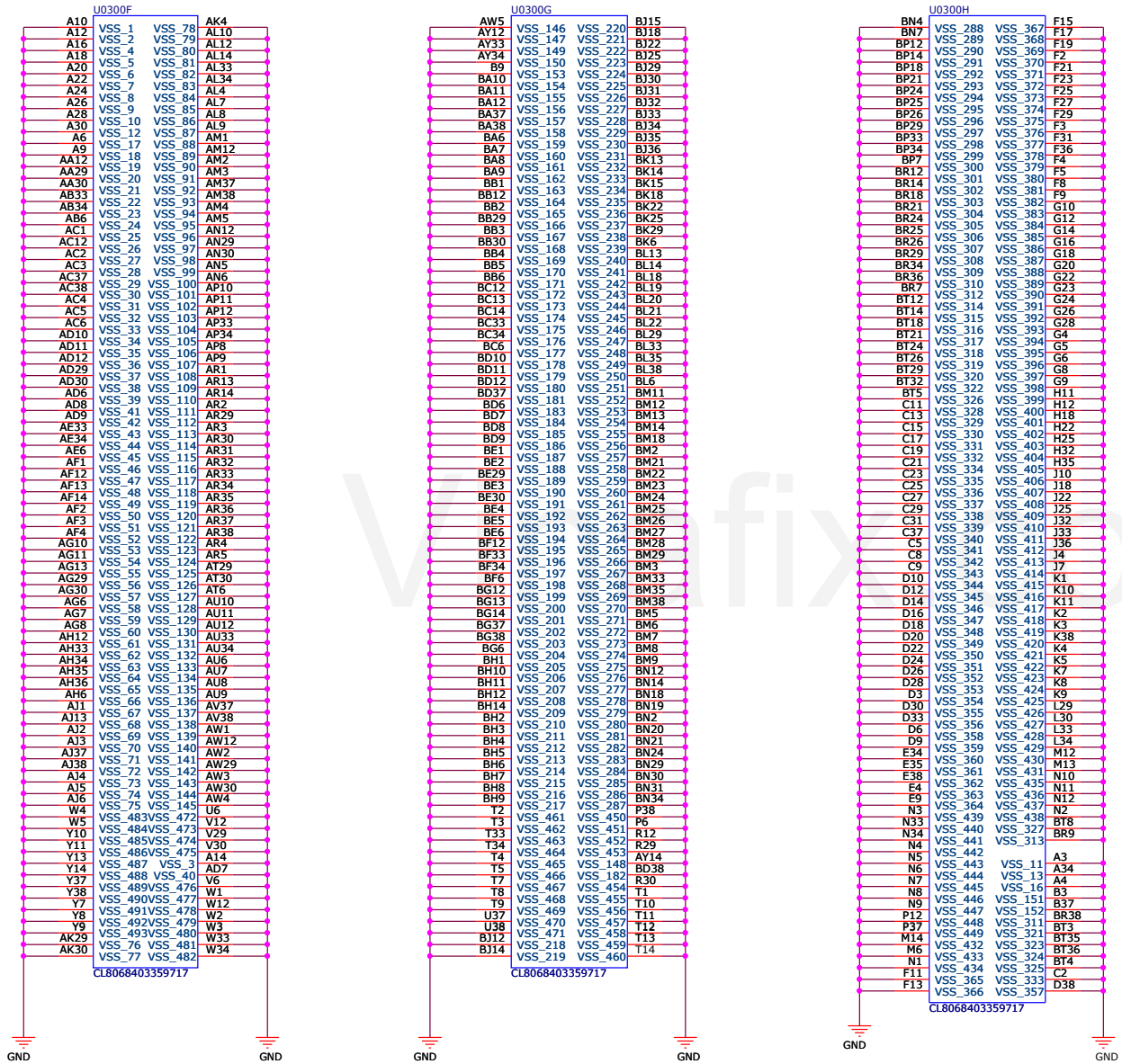
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 7 of 99



PEGATRON Title : VSS

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 8 of 99	

+VCORE
+VCCGT

+VCORE 80
+VCCGT 80

+VCORE

+VCORE

U0300I

128A

AA13	VCC_1	VCC_64	AH13
AA31	VCC_2	VCC_65	AH14
AA32	VCC_3	VCC_66	AH29
AA33	VCC_4	VCC_67	AH30
AA34	VCC_5	VCC_68	AH31
AA35	VCC_6	VCC_69	AH32
AA36	VCC_7	VCC_70	AJ14
AA37	VCC_8	VCC_71	AJ29
AA38	VCC_9	VCC_72	AJ30
AB29	VCC_10	VCC_73	AJ31
AB30	VCC_11	VCC_74	AJ32
AB31	VCC_12	VCC_75	AJ33
AB32	VCC_13	VCC_76	AJ34
AB35	VCC_14	VCC_77	AJ35
AB36	VCC_15	VCC_78	AJ36
AB37	VCC_16	VCC_79	AK31
AB38	VCC_17	VCC_80	AK32
AC13	VCC_18	VCC_81	AK33
AC14	VCC_19	VCC_82	AK34
AC29	VCC_20	VCC_83	AK35
AC30	VCC_21	VCC_84	AK36
AC31	VCC_22	VCC_85	AK37
AC32	VCC_23	VCC_86	AK38
AC33	VCC_24	VCC_87	AL13
AC34	VCC_25	VCC_88	AL29
AC35	VCC_26	VCC_89	AL30
AC36	VCC_27	VCC_90	AL31
AD13	VCC_28	VCC_91	AL32
AD14	VCC_29	VCC_92	AL35
AD31	VCC_30	VCC_93	AL36
AD32	VCC_31	VCC_94	AL37
AD33	VCC_32	VCC_95	AL38
AD34	VCC_33	VCC_96	AM13
AD35	VCC_34	VCC_97	AM14
AD36	VCC_35	VCC_98	AM29
AD37	VCC_36	VCC_99	AM30
AD38	VCC_37	VCC_100	AM31
AE13	VCC_38	VCC_101	AM32
AE14	VCC_39	VCC_102	AM33
AE30	VCC_40	VCC_103	AM34
AE31	VCC_41	VCC_104	AM35
AE32	VCC_42	VCC_105	AM36
AE35	VCC_43	VCC_106	AN13
AE36	VCC_44	VCC_107	AN14
AE37	VCC_45	VCC_108	AN31
AE38	VCC_46	VCC_109	AN32
AF29	VCC_47	VCC_110	AN33
AF30	VCC_48	VCC_111	AN34
AF31	VCC_49	VCC_112	AN35
AF32	VCC_50	VCC_113	AN36
AF33	VCC_51	VCC_114	AN37
AF34	VCC_52	VCC_115	AN38
AF35	VCC_53	VCC_116	AP13
AF36	VCC_54	VCC_117	AP30
AF37	VCC_55	VCC_118	AP31
AF38	VCC_56	VCC_119	AP32
AG14	VCC_57	VCC_120	AP35
AG31	VCC_58	VCC_121	AP36
AG32	VCC_59	VCC_122	AP37
AG33	VCC_60	VCC_123	AP38
AG34	VCC_61	VCC_124	K13
AG35	VCC_62		
AG36	VCC_63		

VCC_SENSE	AG37
VSS_SENSE	AG38

VCORE_VCCSENSE 80
VCORE_VSSSENSE 80

CL8068403359717

+VCORE

+VCORE

U0300J

K14	VCC_125	VCC_188
L13	VCC_126	VCC_189
L14	VCC_127	VCC_190
N13	VCC_128	VCC_191
N14	VCC_129	VCC_192
N30	VCC_130	VCC_193
N31	VCC_131	VCC_194
N32	VCC_132	VCC_195
N35	VCC_133	VCC_196
N36	VCC_134	VCC_197
N37	VCC_135	VCC_198
N38	VCC_136	VCC_199
P13	VCC_137	
P14	VCC_138	
P29	VCC_139	
P30	VCC_140	
P31	VCC_141	
P32	VCC_142	
P33	VCC_143	
P34	VCC_144	
P35	VCC_145	
P36	VCC_146	
R13	VCC_147	
R31	VCC_148	
R32	VCC_149	
R33	VCC_150	
R34	VCC_151	
R35	VCC_152	
R36	VCC_153	
R37	VCC_154	
R38	VCC_155	
T29	VCC_156	
T30	VCC_157	
T31	VCC_158	
T32	VCC_159	
T35	VCC_160	
T36	VCC_161	
T37	VCC_162	
T38	VCC_163	
U29	VCC_164	
U30	VCC_165	
U31	VCC_166	
U32	VCC_167	
U33	VCC_168	
U34	VCC_169	
U35	VCC_170	
U36	VCC_171	
V13	VCC_172	
V14	VCC_173	
V31	VCC_174	
V32	VCC_175	
V33	VCC_176	
V34	VCC_177	
V35	VCC_178	
V36	VCC_179	
V37	VCC_180	
V38	VCC_181	
W13	VCC_182	
W14	VCC_183	
W29	VCC_184	
W30	VCC_185	
W31	VCC_186	
W32	VCC_187	

CL8068403359717

+VCCGT

+VCCGT

U0300K

32A

AT14	VCCGT_1	VCCGT_80	BD35
AT31	VCCGT_2	VCCGT_81	BD36
AT32	VCCGT_3	VCCGT_82	BE31
AT33	VCCGT_4	VCCGT_83	BE32
AT34	VCCGT_5	VCCGT_84	BE33
AT35	VCCGT_6	VCCGT_85	BE34
AT36	VCCGT_7	VCCGT_86	BE35
AT37	VCCGT_8	VCCGT_87	BE36
AT38	VCCGT_9	VCCGT_88	BE37
AU14	VCCGT_10	VCCGT_89	BE38
AU29	VCCGT_11	VCCGT_90	BF13
AU30	VCCGT_12	VCCGT_91	BF14
AU31	VCCGT_13	VCCGT_92	BF29
AU32	VCCGT_14	VCCGT_93	BF30
AU35	VCCGT_15	VCCGT_94	BF31
AU36	VCCGT_16	VCCGT_95	BF32
AU37	VCCGT_17	VCCGT_96	BF35
AU38	VCCGT_18	VCCGT_97	BF36
AV29	VCCGT_19	VCCGT_98	BF37
AV30	VCCGT_20	VCCGT_99	BF38
AV31	VCCGT_21	VCCGT_100	BG29
AV32	VCCGT_22	VCCGT_101	BG30
AV33	VCCGT_23	VCCGT_102	BG31
AV34	VCCGT_24	VCCGT_103	BG32
AV35	VCCGT_25	VCCGT_104	BG33
AV36	VCCGT_26	VCCGT_105	BG34
AW14	VCCGT_27	VCCGT_106	BG35
AW31	VCCGT_28	VCCGT_107	BG36
AW32	VCCGT_29	VCCGT_108	BH33
AW33	VCCGT_30	VCCGT_109	BH34
AW34	VCCGT_31	VCCGT_110	BH35
AW35	VCCGT_32	VCCGT_111	BH36
AW36	VCCGT_33	VCCGT_112	BH37
AW37	VCCGT_34	VCCGT_113	BH38
AW38	VCCGT_35	VCCGT_114	BJ16
AY29	VCCGT_36	VCCGT_115	BJ17
AY30	VCCGT_37	VCCGT_116	BJ19
AY31	VCCGT_38	VCCGT_117	BJ20
AY32	VCCGT_39	VCCGT_118	BJ21
AY35	VCCGT_40	VCCGT_119	BJ23
AY36	VCCGT_41	VCCGT_120	BJ24
AY37	VCCGT_42	VCCGT_121	BJ26
AY38	VCCGT_43	VCCGT_122	BJ27
BA13	VCCGT_44	VCCGT_123	BJ37
BA14	VCCGT_45	VCCGT_124	BJ38
BA29	VCCGT_46	VCCGT_125	BK16
BA30	VCCGT_47	VCCGT_126	BK17
BA31	VCCGT_48	VCCGT_127	BK19
BA32	VCCGT_49	VCCGT_128	BK20
BA33	VCCGT_50	VCCGT_129	BK21
BA34	VCCGT_51	VCCGT_130	BK23
BA35	VCCGT_52	VCCGT_131	BK24
BA36	VCCGT_53	VCCGT_132	BK26
BB13	VCCGT_54	VCCGT_133	BK27
BB14	VCCGT_55	VCCGT_134	BL15
BB31	VCCGT_56	VCCGT_135	BL16
BB32	VCCGT_57	VCCGT_136	BL17
BB33	VCCGT_58	VCCGT_137	BL23
BB34	VCCGT_59	VCCGT_138	BL24
BB35	VCCGT_60	VCCGT_139	BL25
BB36	VCCGT_61	VCCGT_140	BL26
BB37	VCCGT_62	VCCGT_141	BL27
BB38	VCCGT_63	VCCGT_142	BL28
BC29	VCCGT_64	VCCGT_143	BL36
BC30	VCCGT_65	VCCGT_144	BL37
BC31	VCCGT_66	VCCGT_145	BM15
BC32	VCCGT_67	VCCGT_146	BM16
BC35	VCCGT_68	VCCGT_147	BM17
BC36	VCCGT_69	VCCGT_148	BM36
BC37	VCCGT_70	VCCGT_149	BM37
BC38	VCCGT_71	VCCGT_150	BN15
BD13	VCCGT_72	VCCGT_151	BN16
BD14	VCCGT_73	VCCGT_152	BN17
BD29	VCCGT_74	VCCGT_153	BN36
BD30	VCCGT_75	VCCGT_154	BN37
BD31	VCCGT_76	VCCGT_155	BN38
BD32	VCCGT_77	VCCGT_156	BP15
BD33	VCCGT_78	VCCGT_157	BP16
BD34	VCCGT_79	VCCGT_158	BP17
BP37	VCCGT_159	VCCGT_164	BR37
BP38	VCCGT_160	VCCGT_165	BT15
BR15	VCCGT_161	VCCGT_166	BT16
BR16	VCCGT_162	VCCGT_167	BT17
BR17	VCCGT_163	VCCGT_168	BT37

VSSGT_SENSE	AH37
VCCGT_SENSE	AH38

VCCGT_VSSSENSE 80
VCCGT_VCCSENSE 80

CL8068403359717

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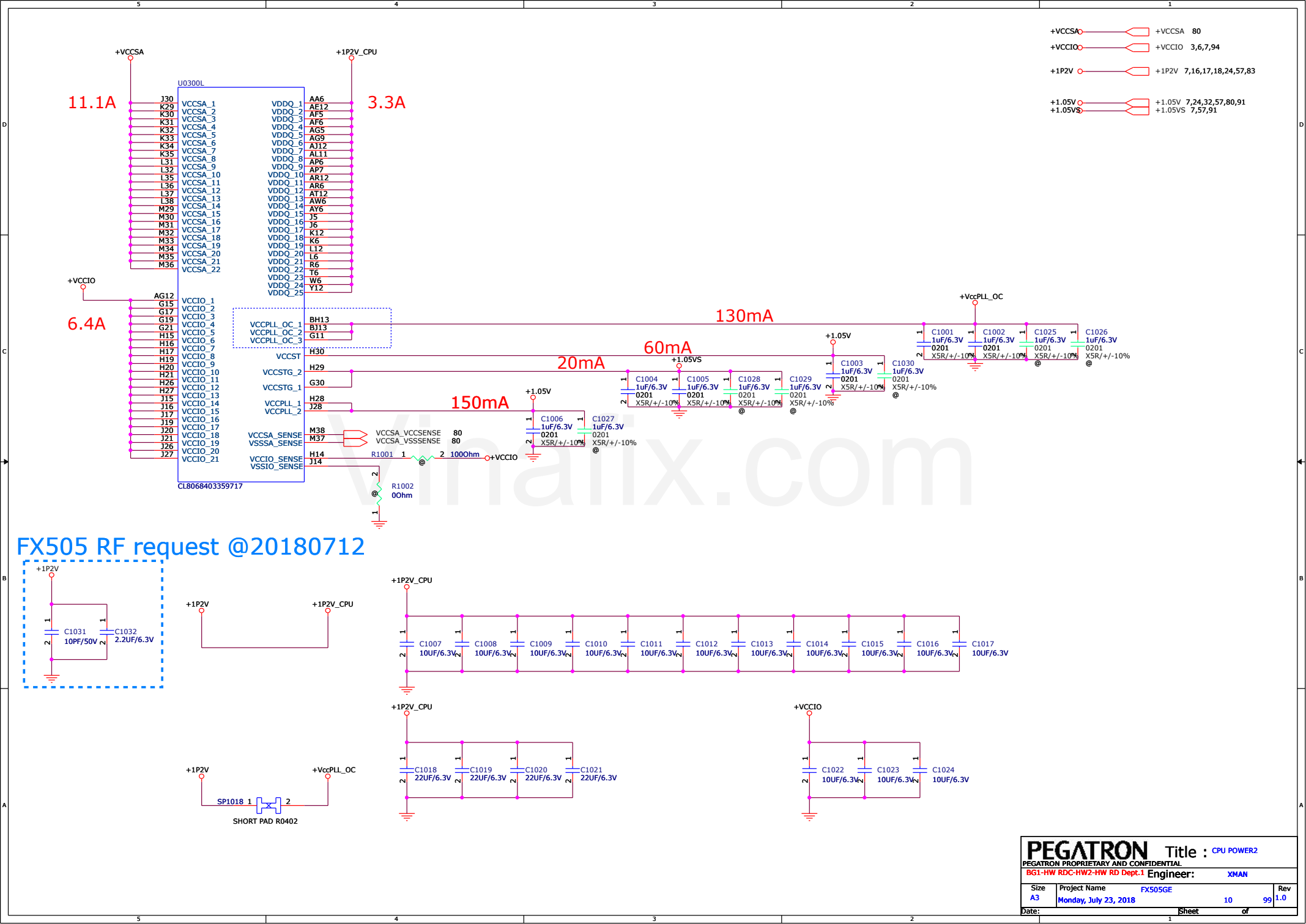
Title : CPU POWER1

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 9 of 99	



FX505 RF request @20180712

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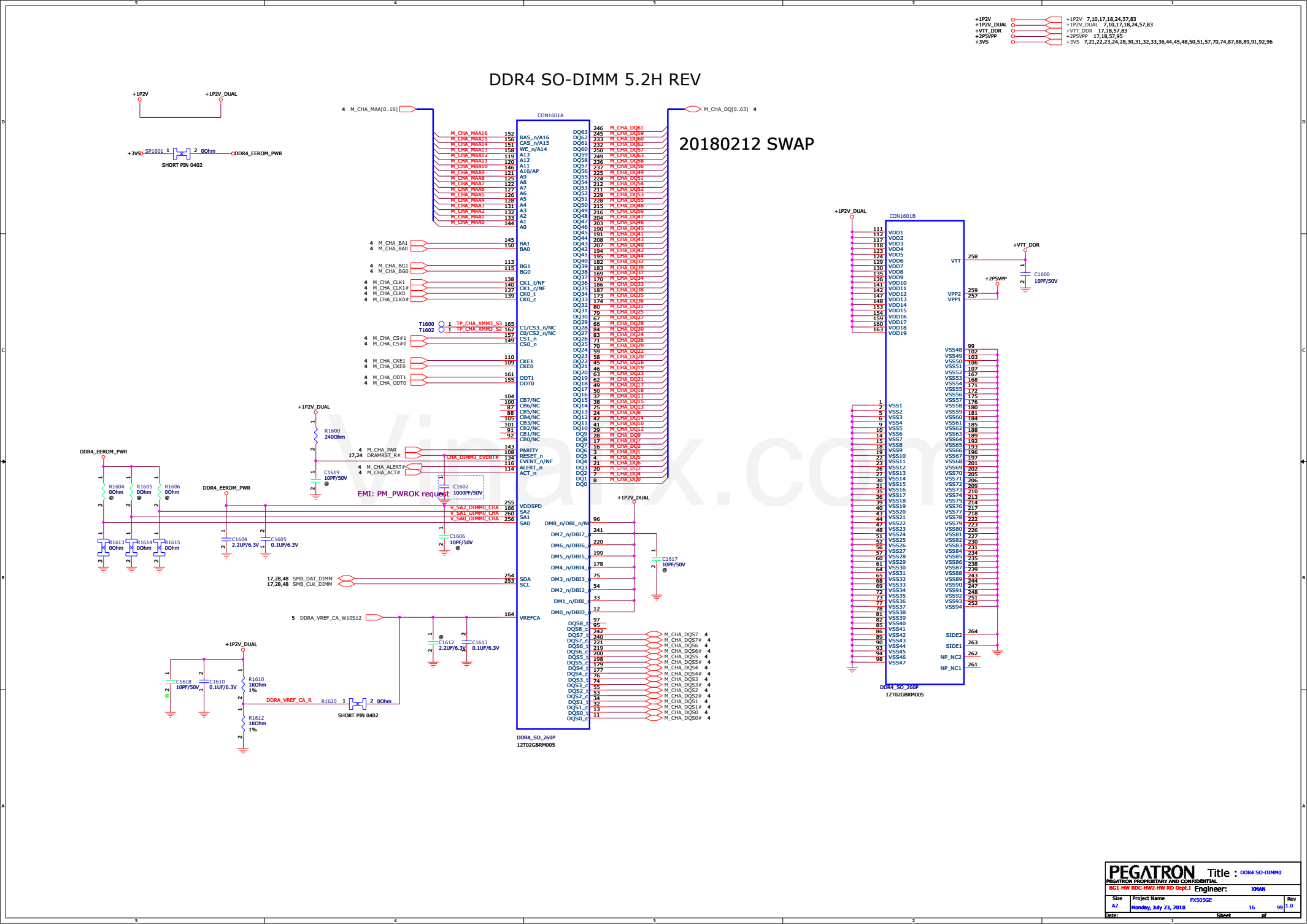
Title : CPU POWER2

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0

Date: Monday, July 23, 2018 Sheet 10 of 99

DDR4 SO-DIMM 5.2H REV



Title :	DDR4 SO-DIMM0
Engineer:	XMAN
Size	A2
Project Name	FX505GE
Rev	1.0
Date:	Monday, July 23, 2018
Sheet	16 of 99

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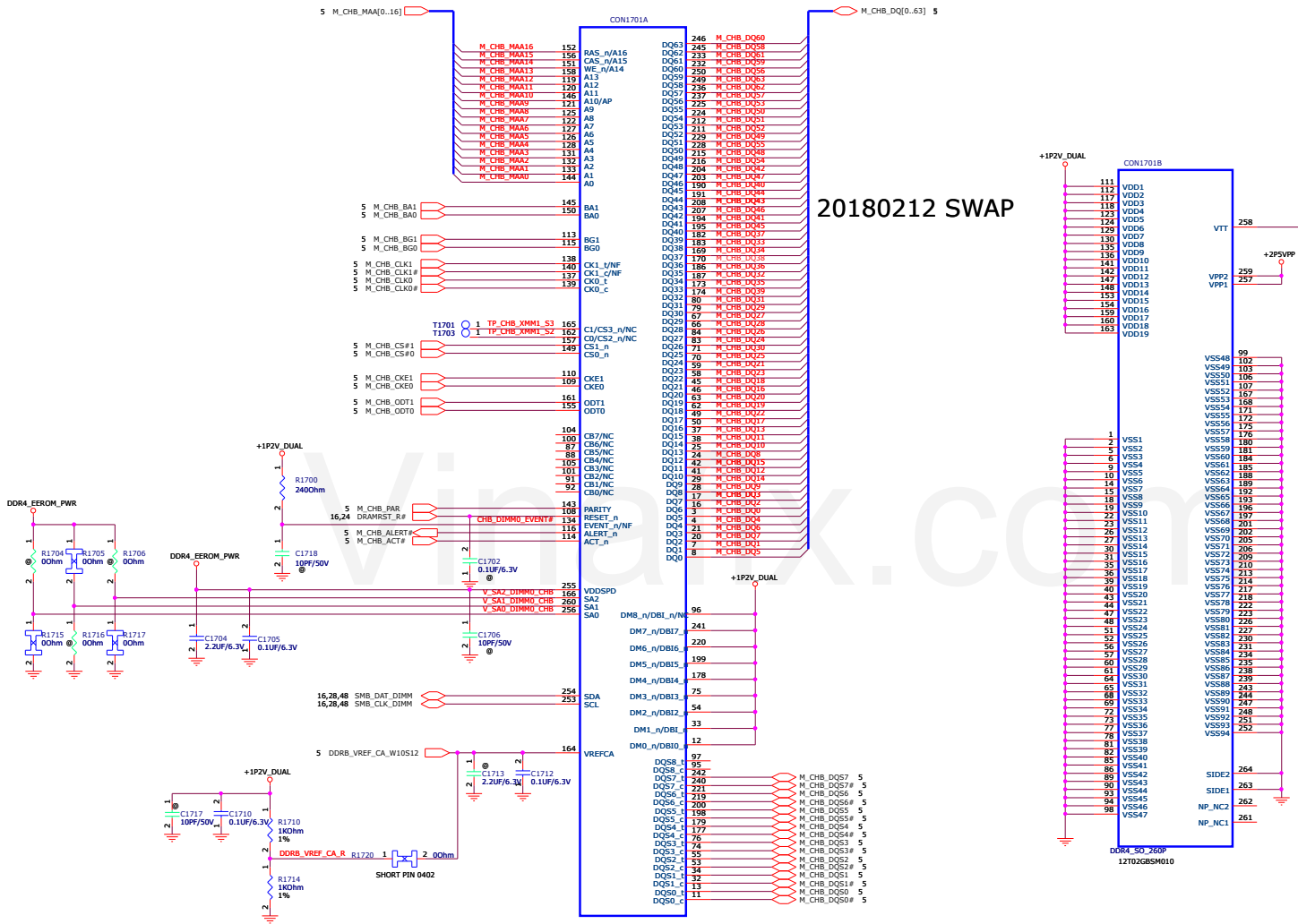
BG1-HW RDC-HW2-HW RD Dept.1

DDR4 SO-DIMM 5.2H STD

+1P2V 7,10,16,18,24,57,83
+1P2V_DUAL 7,10,16,18,24,57,83
+VTT_DDR 16,18,57,83
+2P5VPP 16,18,57,95
+3VS 7,16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,70,74,87,88,89,91,92,96

20180212 SWAP



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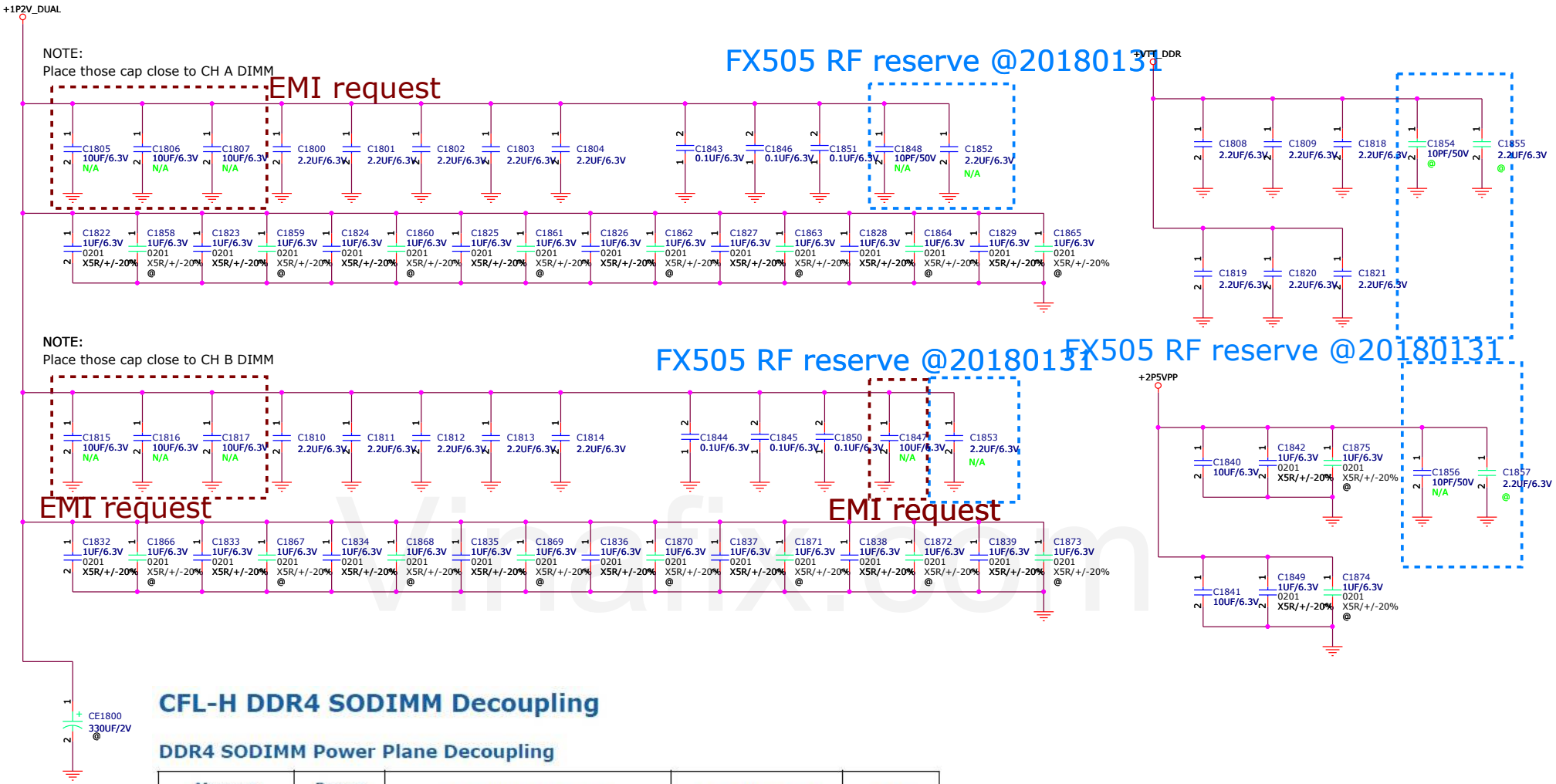
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4 SO-DIMM1
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 17 of 99

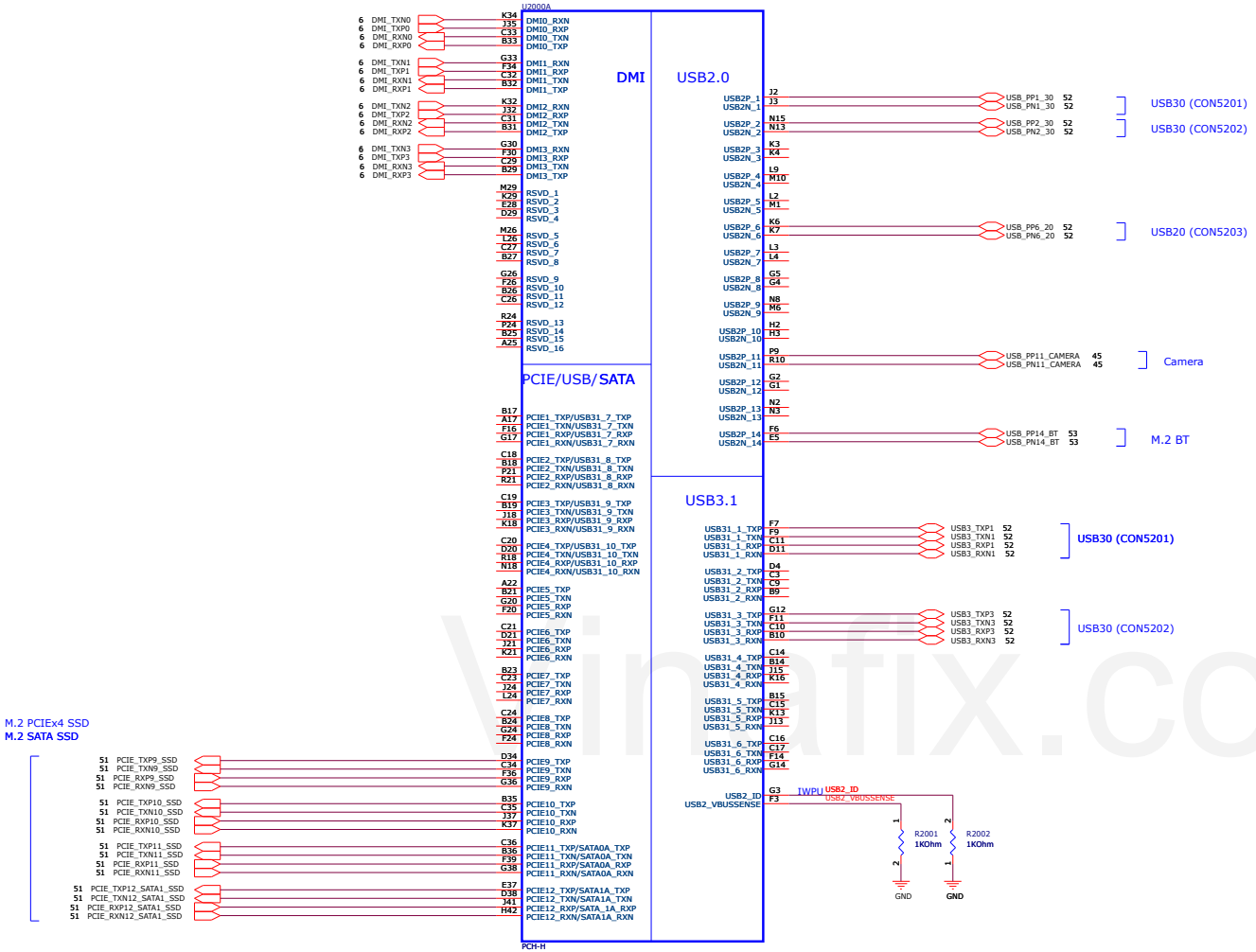


CFL-H DDR4 SODIMM Decoupling

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

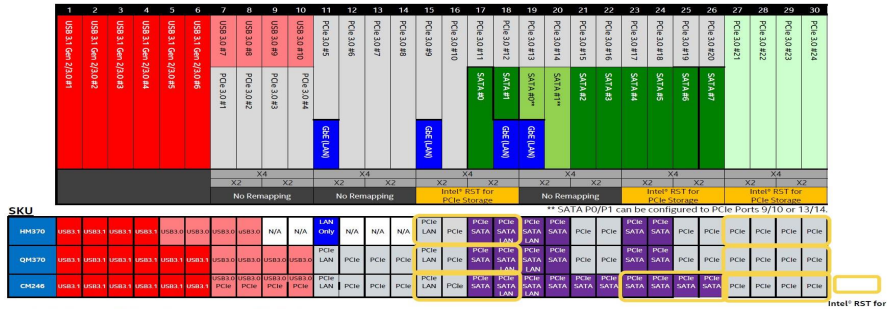
PEGATRON Title : DDR4 Caps.
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A3 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 18 of 99



USB3.1 support GEN2
HM370: 4 ports
QM370: 6 ports

Mobile PCH SKUs	SKU		
	HM370	QM370	CM246
DMI	DMI x4 Gen3	DMI x4 Gen3	DMI x4 Gen3
SATA 3.0 (6 Gbps) Ports	4	4	8
PCIe*	Up to 16 Gen3 lanes	Up to 20 Gen3 lanes	Up to 24 Gen3 lanes
Total USB Ports (Maximum USB 3.1)	14 (8)	14 (10)	14 (10)
Maximum USB 3.1 Ports: Gen 2 (10 Gbps) / Gen 1 (5 Gbps)	4 / 8	6 / 10	6 / 10
Total USB 2.0 Ports	14	14	14
Intel® Smart Sound Technology	YES	YES	YES
Intel® ME 12 Firmware	Consumer	Consumer / Corporate	Consumer / Corporate
Intel® AMT	NO	YES	YES
Intel® Optane™ Memory Support	YES	YES	YES
Intel® Rapid Storage Technology 16	YES	YES	YES
Intel® RST RAID Support	YES	YES	YES
Integrated Intel® Wireless-AC Support	YES	YES	YES
eSPI Chip Select	1	1	1
Intel® Trusted Execution Technology	NO	YES	YES

Preliminary HSIO Lane Assignments – CNL PCH-H



- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA P0/P1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

PEGATRON Title : HSIO 1
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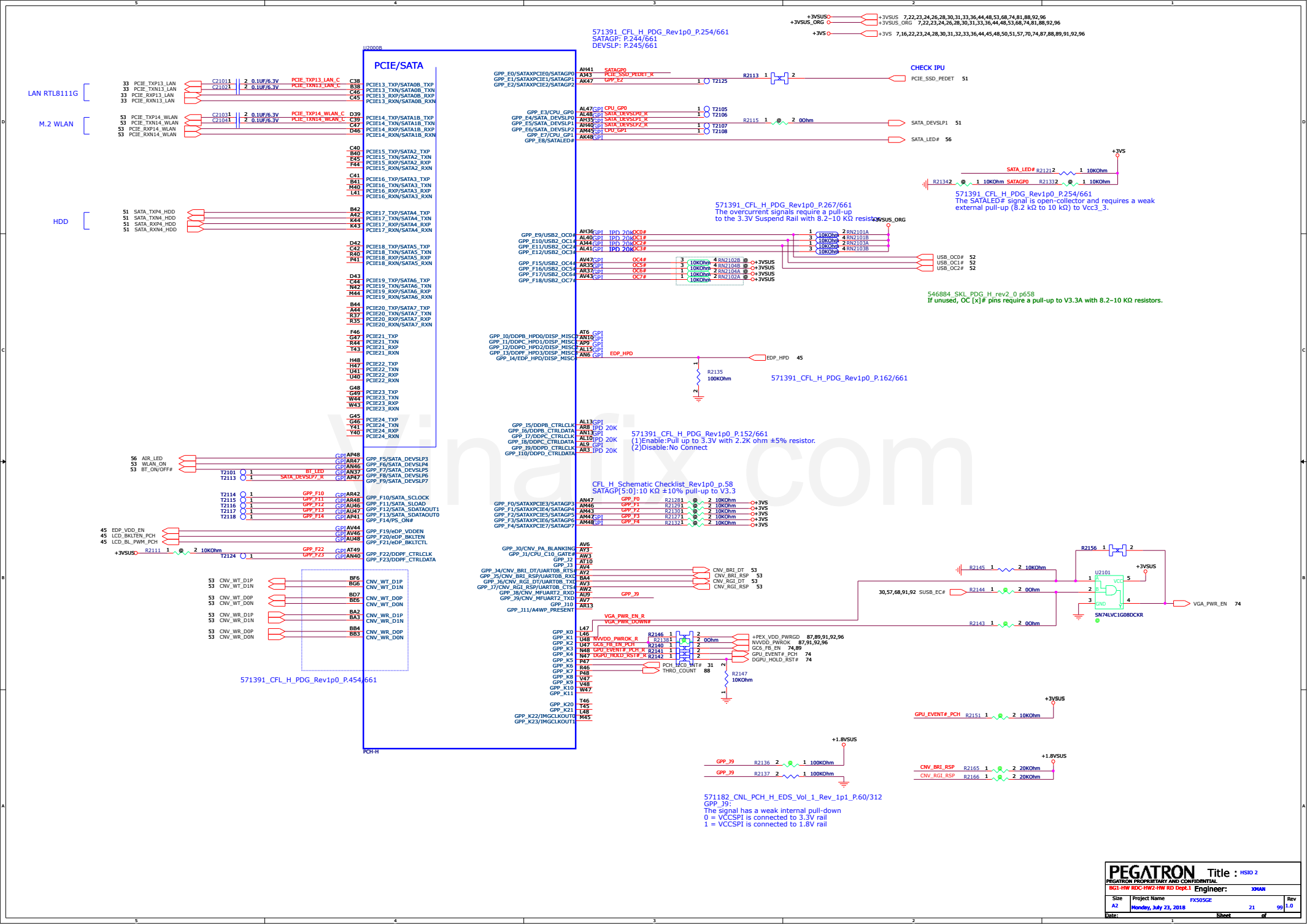
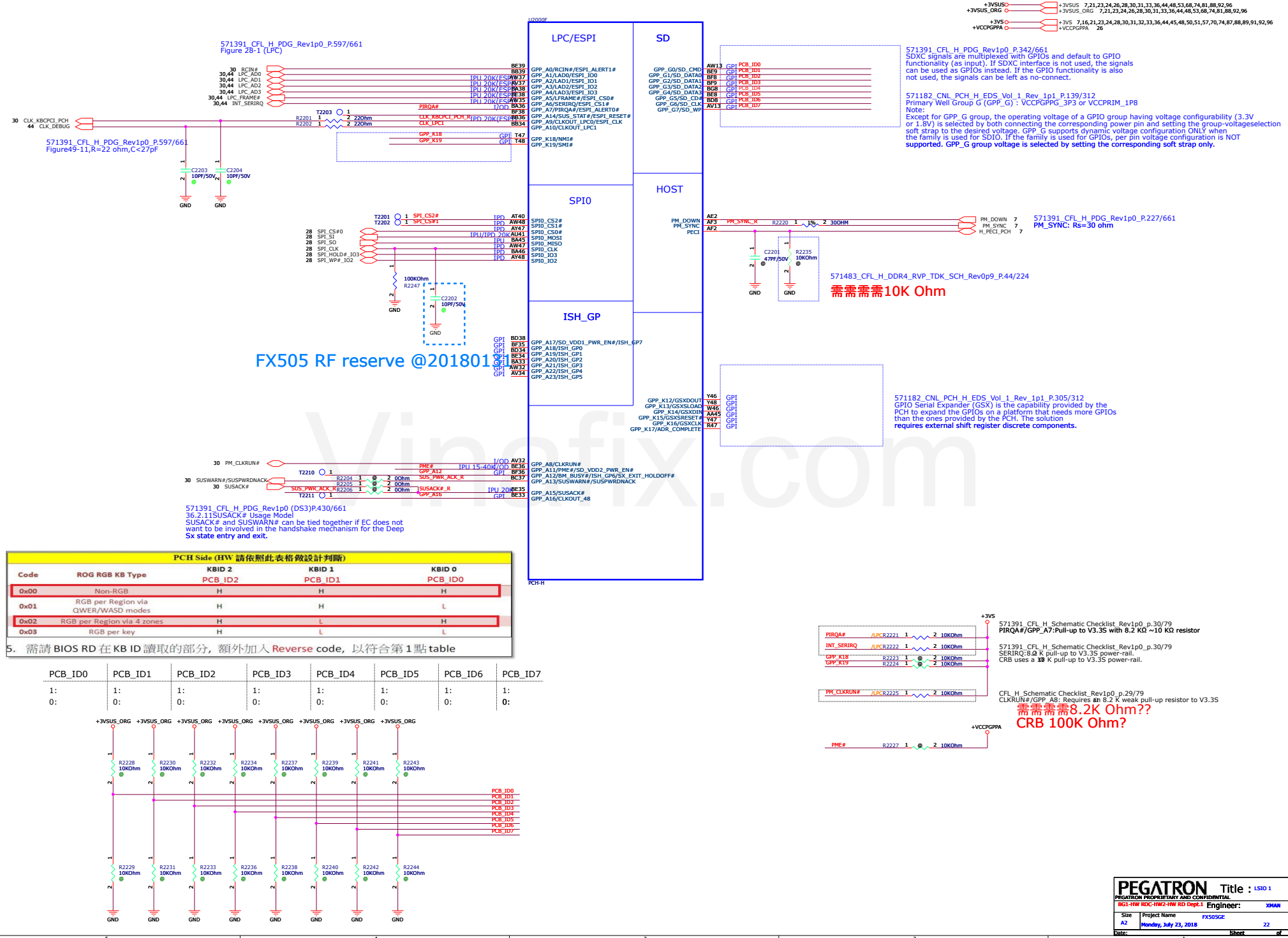
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 20 of 99


PCIE/SATA
U2000B
PCH-H
LAN RTL8111G
M.2 WLAN
HDD
571391_CFL_H_PDG_Rev1p0_P.254/661
SATAGP: P.244/661
DEVSLP: P.245/661
571391_CFL_H_PDG_Rev1p0_P.267/661
The overcurrent signals require a pull-up to the 3.3V Suspend Rail with 8.2~10 KΩ resistor.
546884_SKL_PDG_H_rev2_0 p658
If unused, OC [x]# pins require a pull-up to V3.3A with 8.2~10 KΩ resistors.
571391_CFL_H_PDG_Rev1p0_P.254/661
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.
571391_CFL_H_PDG_Rev1p0_P.162/661
571391_CFL_H_PDG_Rev1p0_P.152/661
(1)Enable:Pull up to 3.3V with 2.2K ohm ±5% resistor.
(2)Disable:No Connect
CFL_H_Schematic Checklist_Rev1p0_p.58
SATAGP[5:0]:10 KΩ ±10% pull-up to V3.3
571391_CFL_H_PDG_Rev1p0_P.454/661
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.60/312
GPP_J9:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
CHECK IPU
PEGATRON
Title : HSIO 2
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: XMAN
Size A2
Project Name FX505GE
Rev 1.0
Date: Monday, July 23, 2018
Sheet 21 of 99


+3VSUS
+3VSUS_ORG
7,21,23,24,26,28,30,31,33,36,44,48,53,68,74,81,88,92,96
+3VS
+VCCPGPPA
26
571391_CFL_H_PDG_Rev1p0_P.597/661
Figure 28-1 (LPC)
LPC/ESPI
SD
HOST
SPI0
ISH_GP
U2000F
PCH-H
571391_CFL_H_PDG_Rev1p0_P.342/661
SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.139/312
Primary Well Group G (GPP_G) : VCCPGPPG_3P3 or VCCPRIM_1P8
Note:
Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltageselection soft strap to the desired voltage. GPP_G supports dynamic voltage configuration ONLY when the family is used for SDIO. If the family is used for GPIOs, per pin voltage configuration is NOT supported. GPP_G group voltage is selected by setting the corresponding soft strap only.
571391_CFL_H_PDG_Rev1p0_P.597/661
Figure49-11,R=22 ohm,C<27pF
571391_CFL_H_PDG_Rev1p0_P.227/661
PM_SYNC: Rs=30 ohm
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.44/224
需需需需10K Ohm
FX505 RF reserve @20180122
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.305/312
GPIO Serial Expander (GSX) is the capability provided by the PCH to expand the GPIOs on a platform that needs more GPIOs than the ones provided by the PCH. The solution requires external shift register discrete components.
571391_CFL_H_PDG_Rev1p0 (DS3)P.430/661
36.2.11SUSACK# Usage Model
SUSACK# and SUSWARN# can be tied together if EC does not want to be involved in the handshake mechanism for the Deep Sx state entry and exit.
PCH Side (HW 請依照此表格做設計判斷)
Code | ROG RGB KB Type | KBID 2 PCB_ID2 | KBID 1 PCB_ID1 | KBID 0 PCB_ID0
0x00 | Non-RGB | H | H | H
0x01 | RGB per Region via QWER/WASD modes | H | H | L
0x02 | RGB per Region via 4 zones | H | L | H
0x03 | RGB per key | H | L | L
5. 需請 BIOS RD 在 KB ID 讀取的部分，額外加入 Reverse code，以符合第 1 點 table
PCB_ID0 | PCB_ID1 | PCB_ID2 | PCB_ID3 | PCB_ID4 | PCB_ID5 | PCB_ID6 | PCB_ID7
1: 0:
571391_CFL_H_Schematic Checklist_Rev1p0_p.30/79
PIRQA#/GPP_A7:Pull-up to V3.3S with 8.2 KΩ ~10 KΩ resistor
571391_CFL_H_Schematic Checklist_Rev1p0_p.30/79
SERIRQ:8.2 K pull-up to V3.3S power-rail.
CRB uses a 10 K pull-up to V3.3S power-rail.
CFL_H_Schematic Checklist_Rev1p0_p.29/79
CLKRUN#/GPP_A8: Requires an 8.2 K weak pull-up resistor to V3.3S
需需需需8.2K Ohm??
CRB 100K Ohm?
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PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : LSIO 1
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2
Project Name FX505GE
Rev 1.0
Monday, July 23, 2018
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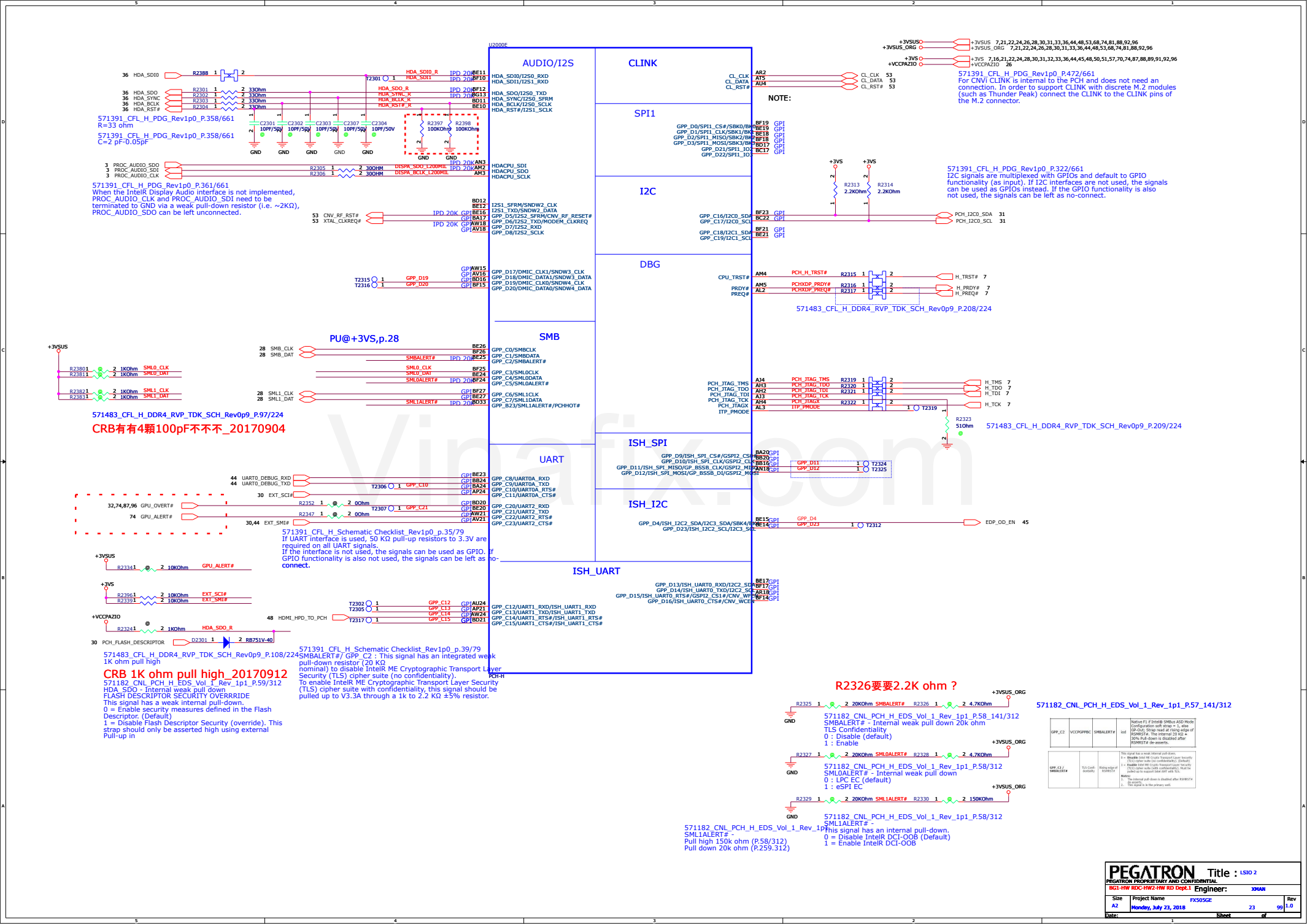

U2000E
AUDIO/I2S
CLINK
SPI1
I2C
DBG
SMB
UART
ISH_SPI
ISH_I2C
ISH_UART
HDA_SDI0
HDA_SDO
HDA_SYNC
HDA_BCLK
HDA_RST#
HDA_SDI0_R
HDA_SDO_R
HDA_SYNC_R
HDA_BCLK_R
HDA_RST#_R
R2388
R2301
R2302
R2303
R2304
330hm
C2301
C2302
C2303
C2307
C2304
10PF/50V
R2397
R2398
100KOhm
GND
571391_CFL_H_PDG_Rev1p0_P.358/661
R=33 ohm
571391_CFL_H_PDG_Rev1p0_P.358/661
C=2 pF~0.05pF
PROC_AUDIO_SDO
PROC_AUDIO_SDI
PROC_AUDIO_CLK
R2305
R2306
30OHM
DISPA_SDO_L200MIL
DISPA_BCLK_L200MIL
HDACPU_SDI
HDACPU_SDO
HDACPU_SCLK
571391_CFL_H_PDG_Rev1p0_P.361/661
When the IntelR Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.
CNV_RF_RST#
XTAL_CLKREQ#
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D7/I2S2_RXD
GPP_D8/I2S2_SCLK
T2315
T2316
GPP_D19
GPP_D20
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA
+3VSUS
R23801
R23811
SML0_CLK
SML0_DAT
R23821
R23831
SML1_CLK
SML1_DAT
1KOhm
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.97/224
CRB有有4顆100pF不不不_20170904
PU@+3VS,p.28
SMB_CLK
SMB_DAT
SMBALERT#
SML0ALERT#
SML1ALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
UART0_DEBUG_RXD
UART0_DEBUG_TXD
EXT_SCI#
GPU_OVERT#
GPU_ALERT#
EXT_SMI#
R2352
R2347
0Ohm
T2306
T2307
GPP_C10
GPP_C21
GPP_C8/UART0A_RXD
GPP_C9/UART0A_TXD
GPP_C10/UART0A_RTS#
GPP_C11/UART0A_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
571391_CFL_H_Schematic Checklist_Rev1p0_p.35/79
If UART interface is used, 50 KΩ pull-up resistors to 3.3V are required on all UART signals.
If the interface is not used, the signals can be used as GPIO. If GPIO functionality is also not used, the signals can be left as no-connect.
+3VS
+VCCPAZIO
R2334
R2396
R2339
10KOhm
R2324
1KOhm
HDA_SDO_R
D2301
RB751V-40
30 PCH_FLASH_DESCRIPTOR
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.108/224
1K ohm pull high
CRB 1K ohm pull high_20170912
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.59/312
HDA_SDO - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in
T2302
T2305
T2317
GPP_C12
GPP_C13
GPP_C14
GPP_C15
HDMI_HPD_TO_PCH
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
571391_CFL_H_Schematic Checklist_Rev1p0_p.39/79
SMBALERT#/ GPP_C2 : This signal has an integrated weak pull-down resistor (20 KΩ nominal) to disable IntelR ME Cryptographic Transport Layer Security (TLS) cipher suite (no confidentiality).
To enable IntelR ME Cryptographic Transport Layer Security (TLS) cipher suite with confidentiality, this signal should be pulled up to V3.3A through a 1k to 2.2 KΩ ±5% resistor.
GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
PCH-H
CL_CLK
CL_DATA
CL_RST#
NOTE:
571391_CFL_H_PDG_Rev1p0_P.472/661
For CNVi CLINK is internal to the PCH and does not need an connection. In order to support CLINK with discrete M.2 modules (such as Thunder Peak) connect the CLINK to the CLINK pins of the M.2 connector.
GPP_D0/SPI1_CS#/SBK0/BK0
GPP_D1/SPI1_CLK/SBK1/BK1
GPP_D2/SPI1_MISO/SBK2/BK2
GPP_D3/SPI1_MOSI/SBK3/BK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
R2313
R2314
2.2KOhm
571391_CFL_H_PDG_Rev1p0_P.322/661
I2C signals are multiplexed with GPIOs and default to GPIO functionality (as input). If I2C interfaces are not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
PCH_I2C0_SDA
PCH_I2C0_SCL
CPU_TRST#
PRDY#
PREQ#
PCH_H_TRST#
PCHXDP_PRDY#
PCHXDP_PREQ#
H_TRST#
H_PRDY#
H_PREQ#
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.208/224
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
PCH_JTAGX
ITP_PMODE
H_TMS
H_TDO
H_TDI
H_TCK
T2319
R2323
51Ohm
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.209/224
GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D11
GPP_D12
T2324
T2325
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL
GPP_D4
GPP_D23
T2312
EDP_OD_EN
R2325
R2326
R2327
R2328
R2329
R2330
20KOhm
4.7KOhm
150KOhm
SMBALERT#
SML0ALERT#
SML1ALERT#
GND
R2326要要2.2K ohm ?
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.58_141/312
SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.58/312
SML0ALERT# - Internal weak pull down
0 : LPC EC (default)
1 : eSPI EC
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.58/312
SML1ALERT# -
This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.58/312
SML1ALERT# -
Pull high 150k ohm (P.58/312)
Pull down 20k ohm (P.259.312)
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.57_141/312
PEGATRON
Title : LSIO 2
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: XMAN
Size A2
Project Name FX505GE
Rev 1.0
Monday, July 23, 2018
Sheet 23 of 99

571391_CFL_H_PDG_Rev1p0_P.329/661
Generic Serial Peripheral Interface (GSPI):
GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

571391_CFL_H_PDG_Rev1p0_P.213-214/661
(1)Any un-used SRCCLKRQ# signal must be left as no connects.
(2) Figure 12-7,pull high 10K ohm

571391_CFL_H_PDG_Rev1p0_P.429-430/661
(1)SLP_S5# is a PCH signal which indicates the system is in the ACPI S5 State.If S5 state indication is not required this pin may be left as no connect or configured as GPIO.
(2)SLP_SUS# is a PCH signal which indicates that the system is in Deep Sx state.If Deep Sx is not implemented on the platform, this signal may be left as no connect.

571391_CFL_H_PDG_Rev1p0_P.430/661
SLP_LAN# can also be configured by Intel ME FW or host BIOS to indicate when the Wireless LAN should be powered in S3-S5 to support Wake on Wireless LAN (Host or Intel ME).

571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.42/224

ALL_SYS_PWRGD delay 99 ms from EC

571391_CFL_H_PDG_Rev1p0_P.429/661
Designers can connect the System Reset signal (SYS_RESET#) on PCH directly to the reset button on the system, provided that there is a weak 8.2 K -10 K pull-up resistor to Primary 3.3 V (VCCPRIM_3p3) or pull-up to any 3.3V rails that is controlled by SLP_S3# or SLP_S4# or SLP_S5#.
When SYS_RESET# is connected to a XDP header, it will require a stronger pull up to work with ITP hardware. Use 1 kΩ ohm pull-up whenever it is connected to a XDP header. Recommend to use 3 K to minimize leakage.

CRB是30.1K ohm

571391_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.93/224
R2412=30.1K ohm

571391_CFL_H_PDG_Rev1p0_P.379/661
R=20K ohm,C=1uF

546884_SKL_PDG_H_rev2_0 p662
All unused GPIOs (which default to GPIO functionality) do not need termination.

571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.93/224
R2417=330K ohm

CRB是330K ohm,的的是的1M ohm

571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.41/224
R=30 ohm

571391_CFL_H_PDG_Rev1p0_P.229/661
R=620 OHM

CRB是30 ohm,acer的的的是的620 ohm

571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.17/224
R=1K ohm

571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.571/312
571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.141/312
SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

571391_CFL_H_Schematic Checklist_Rev1p0_p.38/79
SPKR/ GPP_B14:This signal has an integrated weak pull-down resistor (20 KΩ nominal) to disable Top-Block Sway by default.
To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 KΩ ±5% resistor

Default is GPO, to reserve pull high to +3VSUS_ORG

571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.57/312
GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

571391_CFL_H_Schematic Checklist_Rev1p0_p.38/79
GSPI0_MOSI/ GPP_B18:
This signal has an integrated weak pull-down resistor (20 KΩ nominal) to disable the no reboot strap functionality by default.
To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 KΩ ±5% resistor.

Default is GPO, to reserve pull high to +3VSUS_ORG

P.141/312 有Pull dowm電電20K ohm,pull high 2.2K ohm_20170904

571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.58/312
BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination

571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.108/224
Pull down 20K ohm

571391_CFL_H_Schematic Checklist_Rev1p0_p.38/79
SRCCLKREQ#[15:0]:
1. Any used, enabled - SRCCLKREQ# signal should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up.
2. Any un-used, disabled - SRCCLKREQ# signal must be left as no connects at the PCH side on the platform

EMI: PM_PWROK request

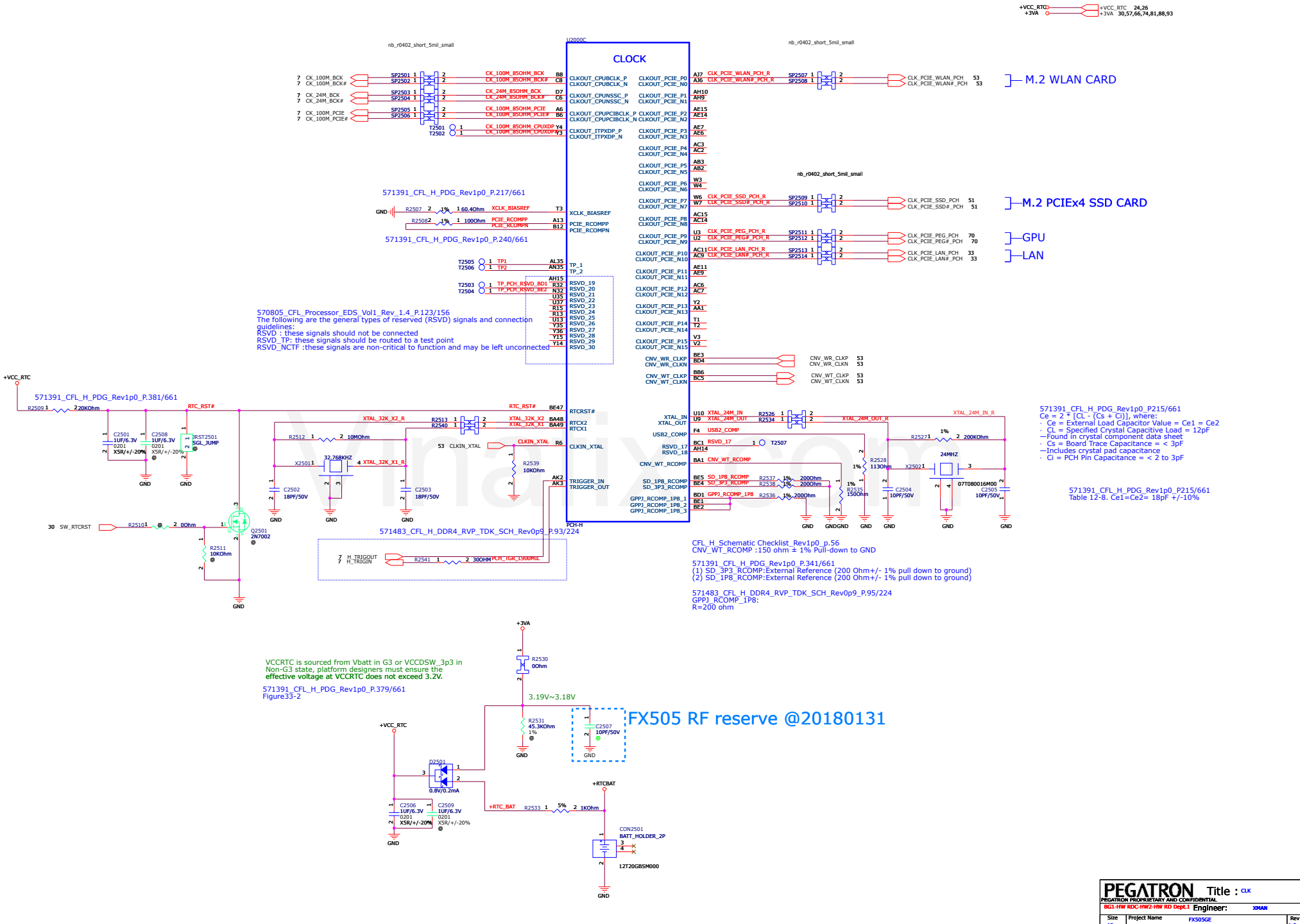
CFL_H_Schematic Checklist_Rev1p0_p.29/79
1 kΩpull-up to VCCDSW_3p3.
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_p.115/224
1k pull high

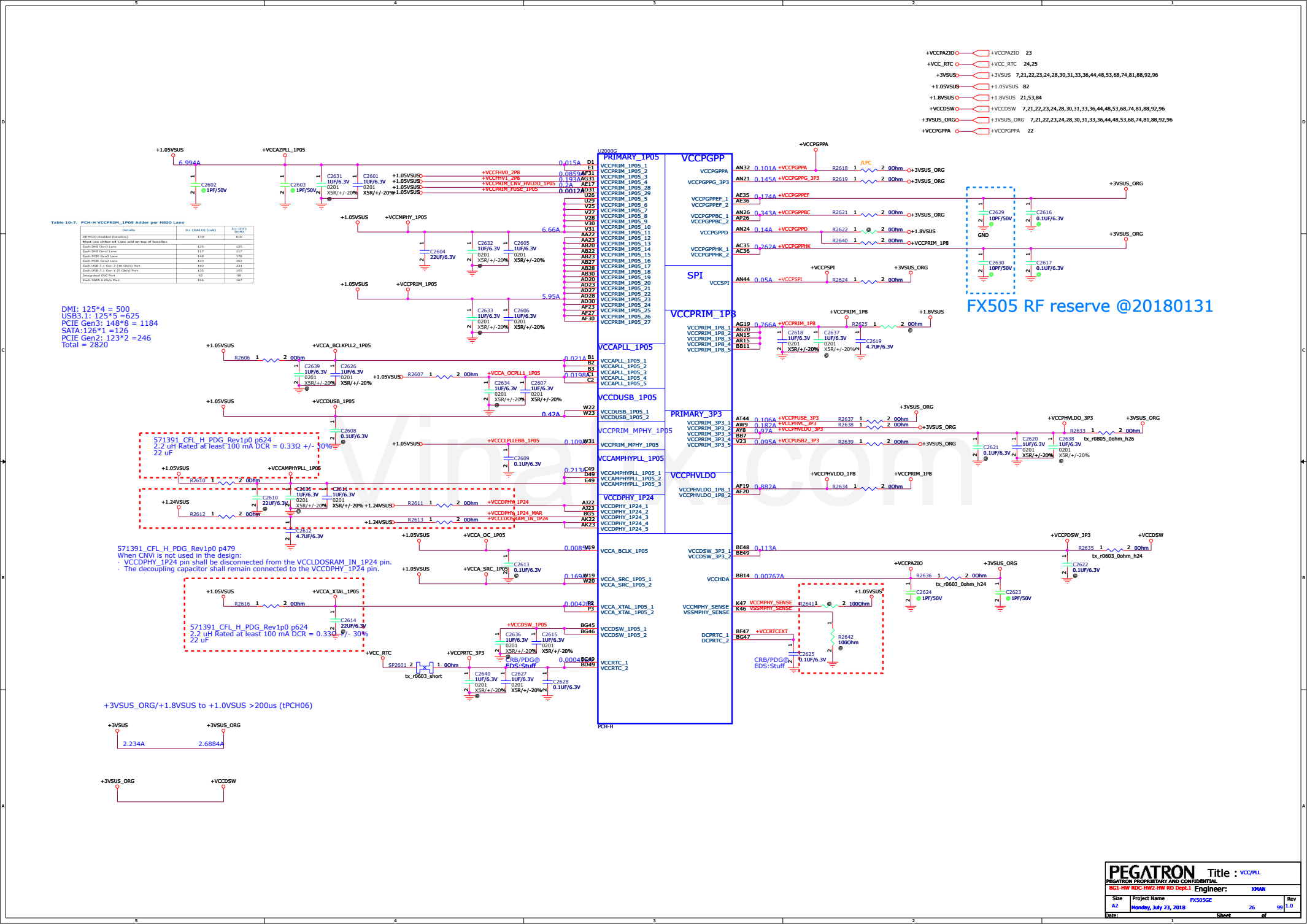
要要要1k pull high

571391_CFL_H_Schematic Checklist_Rev1p0_p.29/79
ACPRESENT/ GPD1:10 kΩ pull-down to GND.

要要要10k pull down

PEGATRON Title : LSIO 3
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 24 of 99


+VCC_RTC 24,26
+3VA 30,57,66,74,81,88,93
CLOCK
M.2 WLAN CARD
M.2 PCIEx4 SSD CARD
GPU
LAN
571391_CFL_H_PDG_Rev1p0_P.217/661
571391_CFL_H_PDG_Rev1p0_P.240/661
570805_CFL_Processor_EDS_Vol1_Rev_1.4_P.123/156
The following are the general types of reserved (RSVD) signals and connection guidelines:
RSVD : these signals should not be connected
RSVD_TP: these signals should be routed to a test point
RSVD_NCTF :these signals are non-critical to function and may be left unconnected
571391_CFL_H_PDG_Rev1p0_P.381/661
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.93/224
CFL_H_Schematic Checklist_Rev1p0_p.56
CNV_WT_RCOMP :150 ohm ± 1% Pull-down to GND
571391_CFL_H_PDG_Rev1p0_P.341/661
(1) SD_3P3_RCOMP:External Reference (200 Ohm+/- 1% pull down to ground)
(2) SD_1P8_RCOMP:External Reference (200 Ohm+/- 1% pull down to ground)
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.95/224
GPPJ_RCOMP_1P8:
R=200 ohm
571391_CFL_H_PDG_Rev1p0_P.215/661
Ce = 2 * (CL - (Cs + Ci)), where:
· Ce = External Load Capacitor Value = Ce1 = Ce2
· CL = Specified Crystal Capacitive Load = 12pF
—Found in crystal component data sheet
· Cs = Board Trace Capacitance = < 3pF
—Includes crystal pad capacitance
· Ci = PCH Pin Capacitance = < 2 to 3pF
571391_CFL_H_PDG_Rev1p0_P.215/661
Table 12-8. Ce1=Ce2= 18pF +/-10%
VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.
571391_CFL_H_PDG_Rev1p0_P.379/661
Figure33-2
FX505 RF reserve @20180131
PEGATRON
Title : CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: XMAN
Size A2
Project Name FX505GE
Rev 1.0
Date: Monday, July 23, 2018
Sheet 25 of 99


+VCCPAZIO +VCCPAZIO 23
+VCC_RTC +VCC_RTC 24,25
+3VSUS +3VSUS 7,21,22,23,24,28,30,31,33,36,44,48,53,68,74,81,88,92,96
+1.05VSUS +1.05VSUS 82
+1.8VSUS +1.8VSUS 21,53,84
+VCCDSW +VCCDSW 7,21,22,23,24,28,30,31,33,36,44,48,53,68,74,81,88,92,96
+3VSUS_ORG +3VSUS_ORG 7,21,22,23,24,28,30,31,33,36,44,48,53,68,74,81,88,92,96
+VCCPGPPA +VCCPGPPA 22
Table 10-7. PCH-H VCCPRIM_1P05 Adder per HSIO Lane
Details
Icc (HALO) (mA)
Icc (DT) (mA)
All HSIO disabled (baseline) 139 616
Must use either x4 Lane add on top of baseline
Each DMI Gen3 Lane 125 125
Each DMI Gen2 Lane 117 117
Each PCIE Gen3 Lane 148 178
Each PCIE Gen2 Lane 123 153
Each USB 3.1 Gen 2 (10 Gb/s) Port 182 221
Each USB 3.1 Gen 1 (5 Gb/s) Port 125 155
Integrated GbE Port 62 96
Each SATA 6 Gb/s Port 126 167
DMI: 125*4 = 500
USB3.1: 125*5 =625
PCIE Gen3: 148*8 = 1184
SATA:126*1 =126
PCIE Gen2: 123*2 =246
Total = 2820
571391_CFL_H_PDG_Rev1p0 p624
2.2 uH Rated at least 100 mA DCR = 0.33Ω +/- 30%
22 uF
571391_CFL_H_PDG_Rev1p0 p479
When CNVi is not used in the design:
· VCCDPHY_1P24 pin shall be disconnected from the VCCLDOSRAM_IN_1P24 pin.
· The decoupling capacitor shall remain connected to the VCCDPHY_1P24 pin.
571391_CFL_H_PDG_Rev1p0 p624
2.2 uH Rated at least 100 mA DCR = 0.33Ω +/- 30%
22 uF
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)
+3VSUS
+3VSUS_ORG
2.234A
2.6884A
+3VSUS_ORG
+VCCDSW
FX505 RF reserve @20180131
PCH-H
PEGATRON
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Title : VCC/PLL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: XMAN
Size A2
Project Name FX505GE
Rev 1.0
Monday, July 23, 2018
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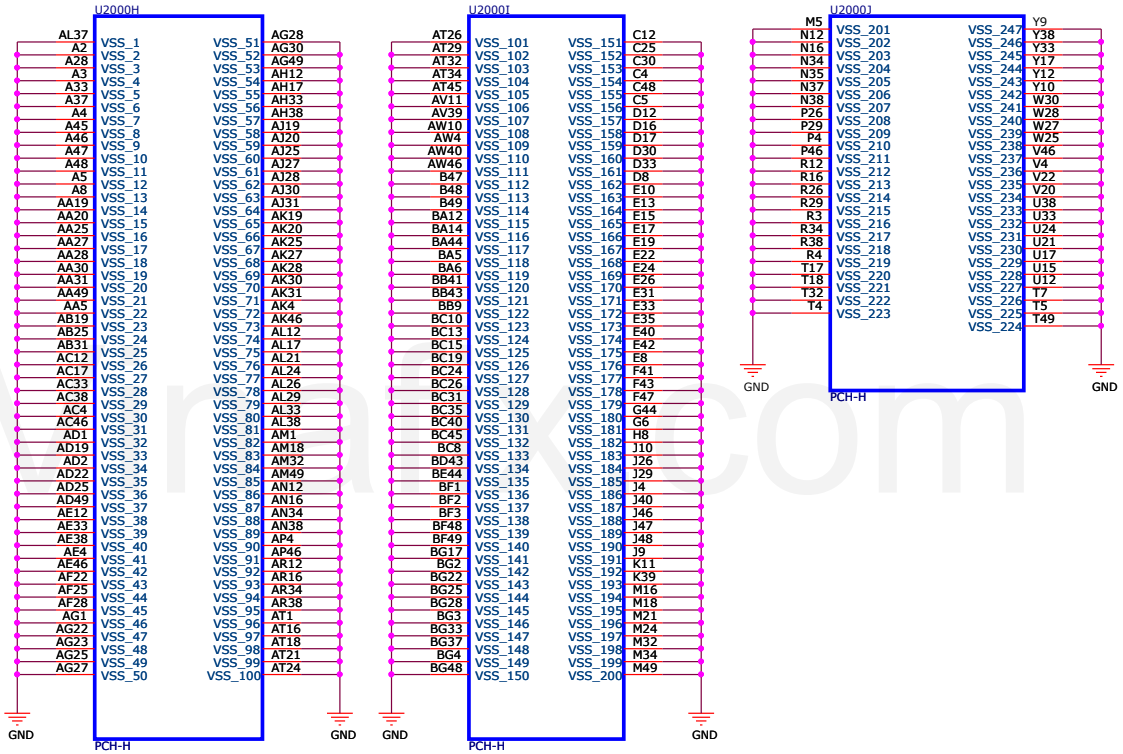

PEGATRON Title : VSS

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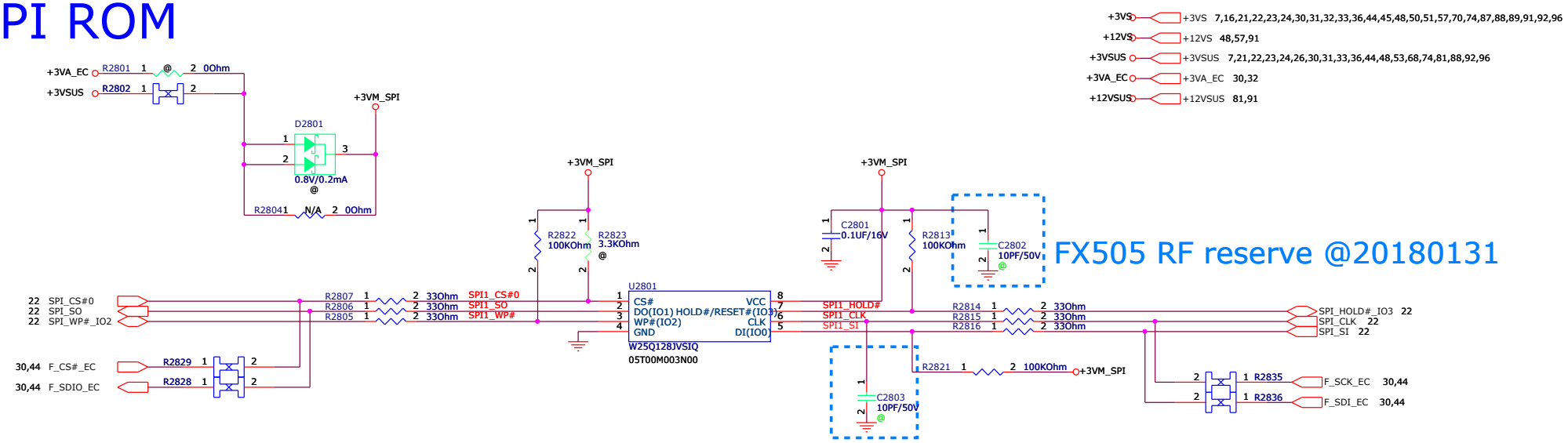
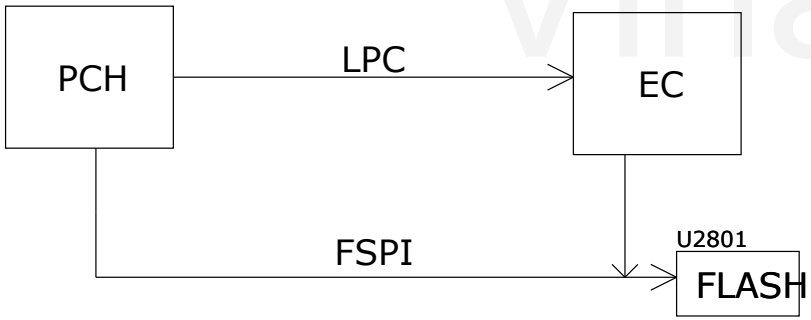
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0

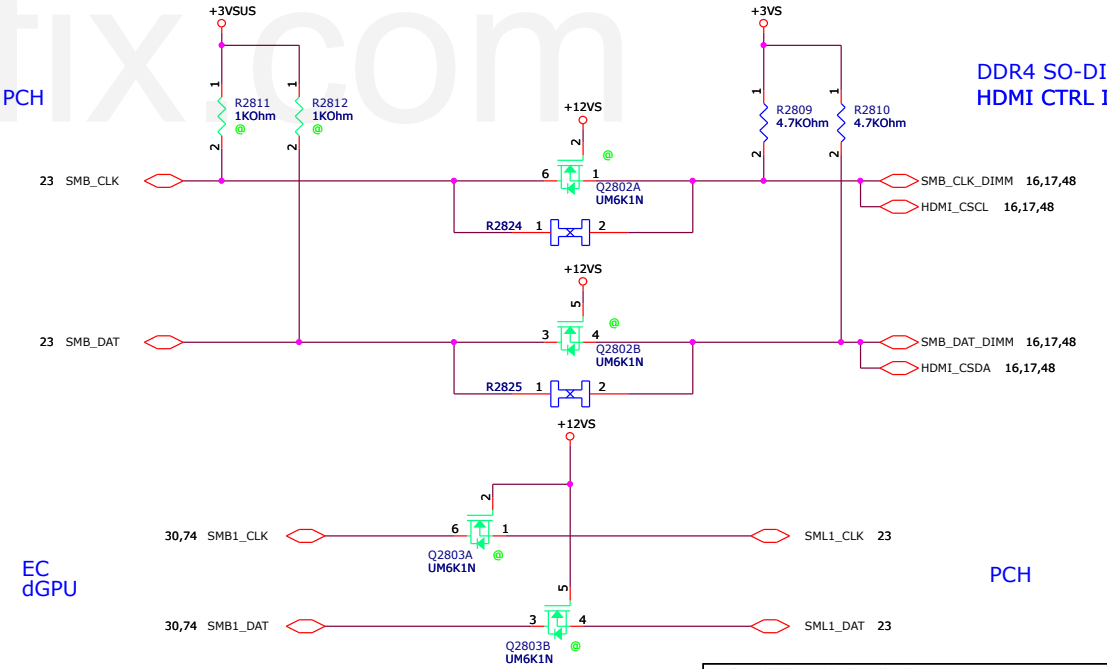
Date: Monday, July 23, 2018 Sheet 27 of 99

SPI ROM





SMBus



PEGATRON Title : SPI/SMB

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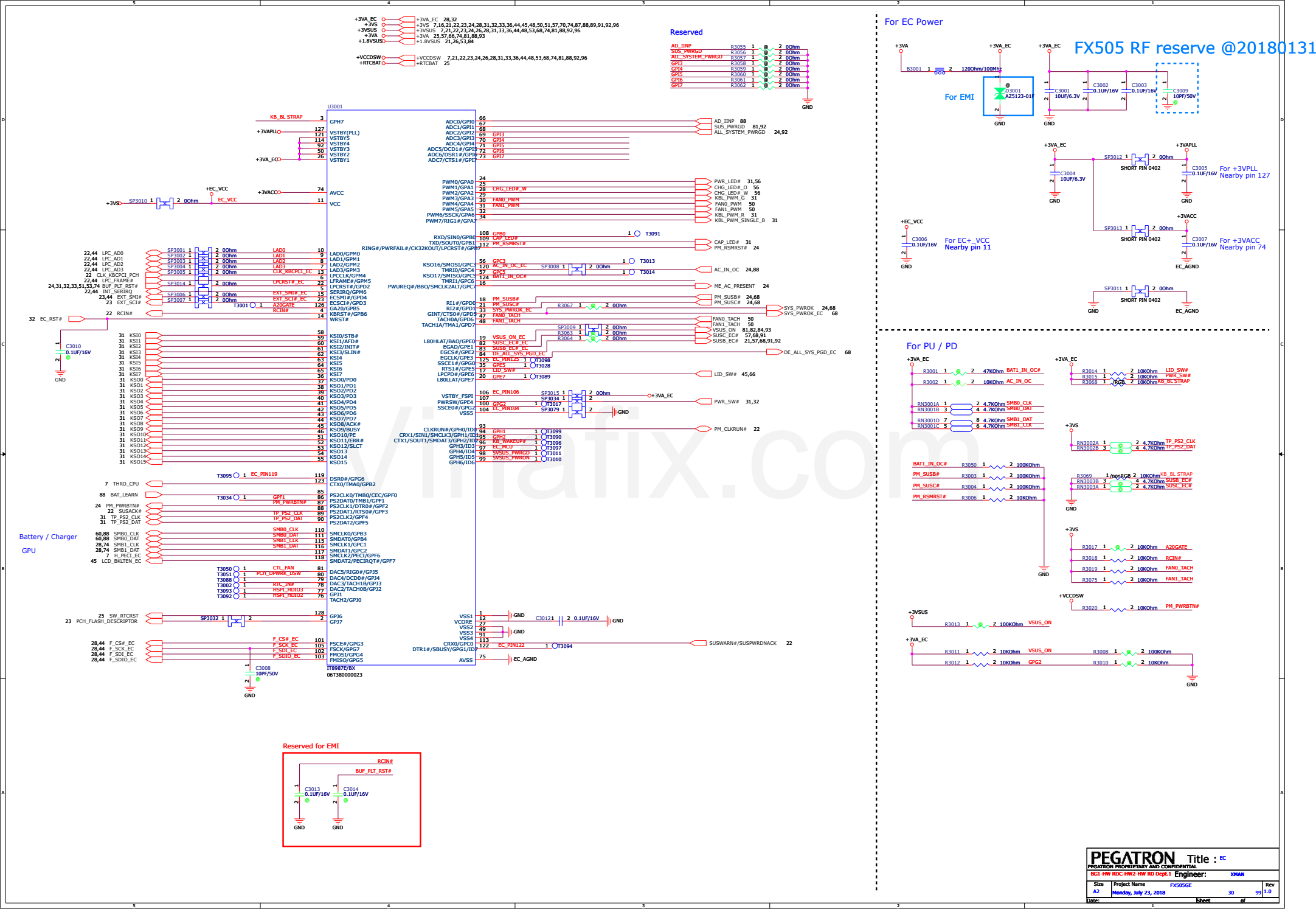
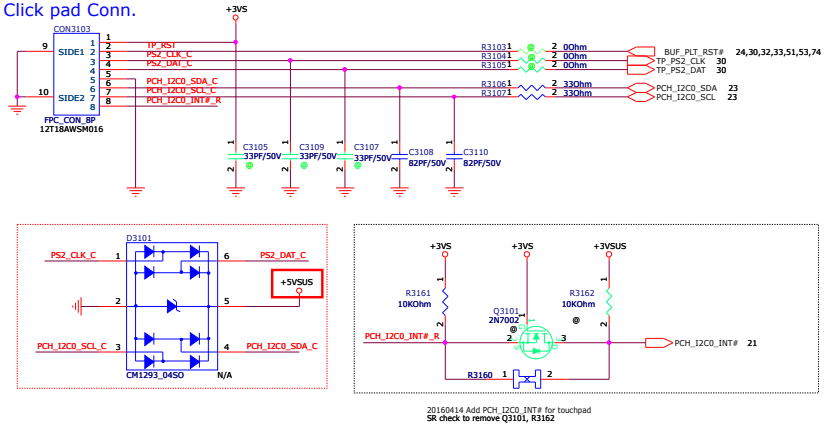
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

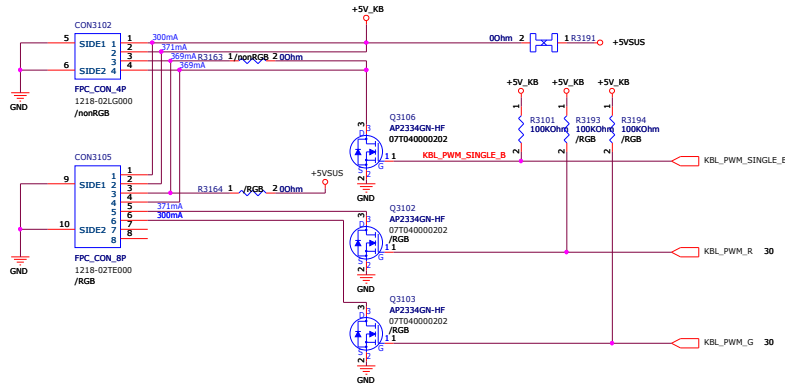
Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 28 of 99	


Reserved
For EC Power
FX505 RF reserve @20180131
For EMI
For +3VPLL
Nearby pin 127
For EC+ VCC
Nearby pin 11
For +3VACC
Nearby pin 74
For PU / PD
Battery / Charger
GPU
Reserved for EMI
U3001
IT8987E/BX
06T380000023
PEGATRON
Title : EC
FX505GE
Monday, July 23, 2018
Engineer: XMAN

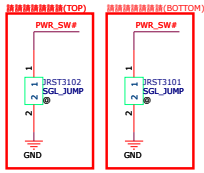
Click pad Conn.



KB Backlight Conn.

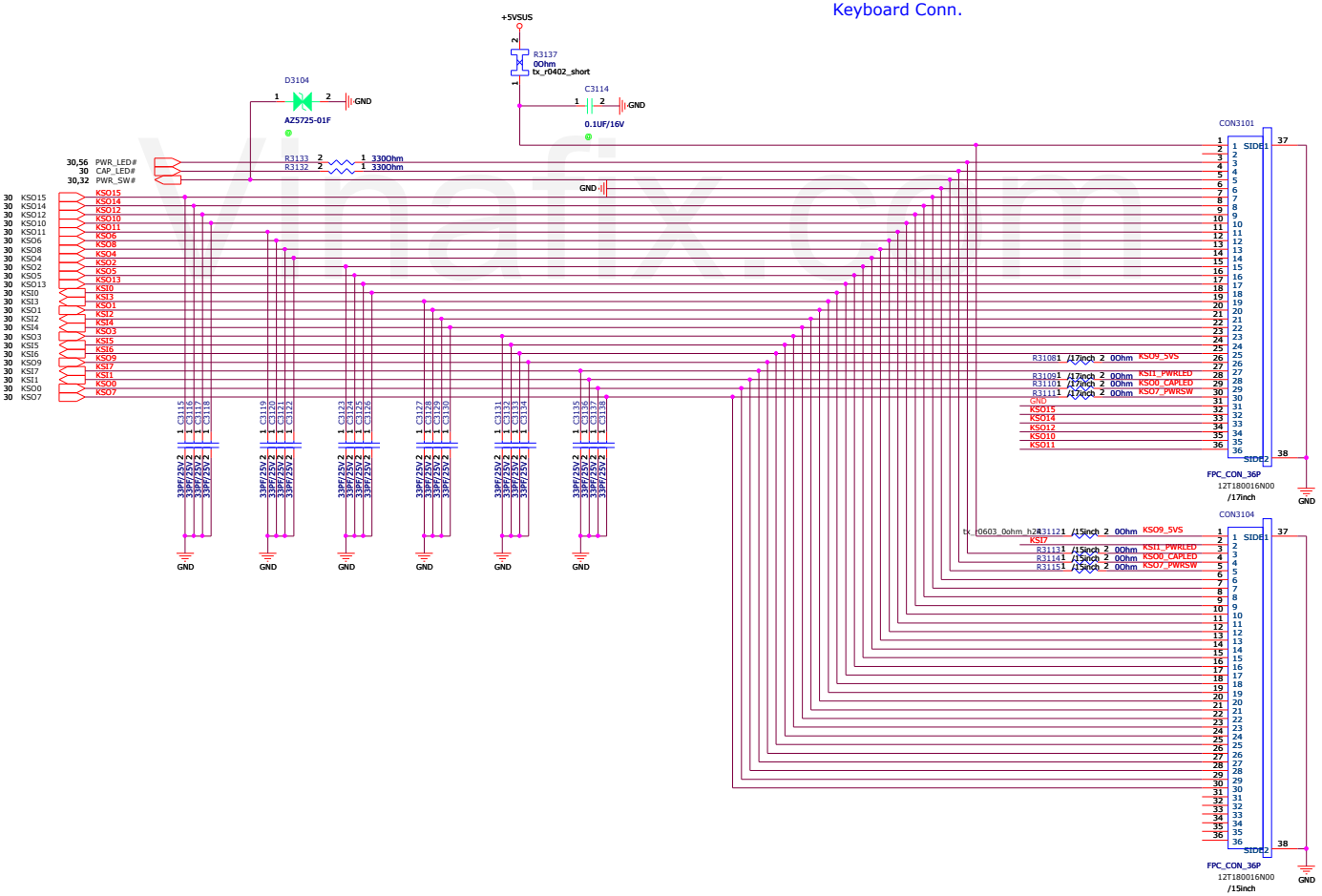


Power-on jumper



PIN 1	LED VCC
PIN 2	NC
PIN 3	Power LED
PIN 4	CapsLock LED
PIN 5	Power SW
PIN 6	Power GND
PIN 7	KSO15
PIN 8	KSO14
PIN 9	KSO12
PIN 10	KSO10
PIN 11	KSO11
PIN 12	KSO6
PIN 13	KSO8
PIN 14	KSO4
PIN 15	KSO2
PIN 16	KSO5
PIN 17	KSO13
PIN 18	KSI0
PIN 19	KSI3
PIN 20	KSO1
PIN 21	KSI2
PIN 22	KSI4
PIN 23	KSO3
PIN 24	KSI5
PIN 25	KSI6
PIN 26	KSO9
PIN 27	KSI7
PIN 28	KSI1
PIN 29	KSO0
PIN 30	KSO7
PIN 31	NC
PIN 32	NC
PIN 33	NC
PIN 34	NC
PIN 35	NC
PIN 36	NC

Keyboard Conn.



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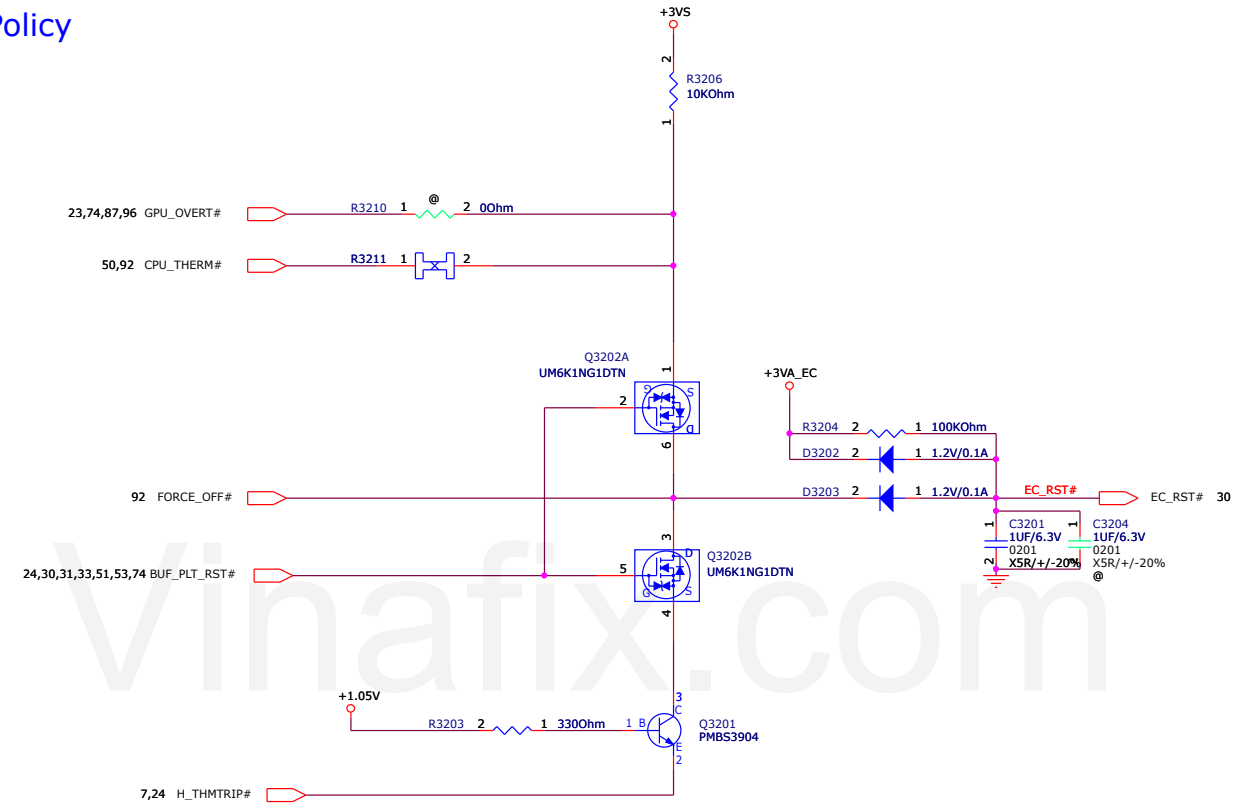
Title : KB/TP

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A2	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 31 of 99	

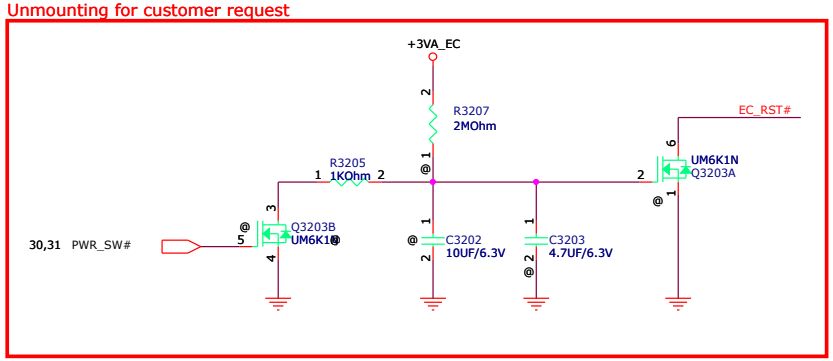
+3VA_EC +3VA_EC 28,30
+3VS +3VS 7,16,21,22,23,24,28,30,31,33,36,44,45,48,50,51,57,70,74,87,88,89,91,92,96

Thermal Policy



EC reset

Unmounting for customer request



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : RST
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
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33.Realtek RTL8111H

+3VS +3VS 7,16,21,22,23,24,28,30,31,32,36,44,45,48,50,51,57,70,74,87,88,89,91,92,96

+3VSUS +3VSUS 7,21,22,23,24,26,28,30,31,36,44,48,53,68,74,81,88,92,96

U3301A

34 L_TRLP0
34 L_TRLN0
MDIP0
MDIN0

34 L_TRLP1
34 L_TRLN1
MDIP1
MDIN1

34 L_TRLP2
34 L_TRLN2
MDIP2
MDIN2

34 L_TRLP3
34 L_TRLN3
MDIP3
MDIN3

AVDD33_1
AVDD33_2
DVDD33

VDDREG
DVDD33

REGOUT
REGOUT10

C3306 close to pins-- 24
C3307 to C3310 close to pins-- 3, 8, 22, 30
C3311 & C3397 close to pins-- 22

200 mils
0.5A
REGOUT10
R3309 1 2 0Ohm
tx_r0805_short
0.1UF/16V C3306
GND

200 mils
0.5A
VDD10
C3307 0.1UF/16V
C3308 0.1UF/16V
C3309 0.1UF/16V
C3310 0.1UF/16V
C3318 1UF/6.3V 0201 X5R/+/-20% @
C3311 1UF/6.3V 0201 X5R/+/-20%
C3397 0.1UF/16V
GND
C3307 to C3311
Close To U3301

AVDD10_0
AVDD10_1
AVDD10_2
VDD10

DVDD10
VDD10

C3316 to C3317 close to pins-- 11, 32
C3398 to C3399 close to pins-- 11, 32(Opt.

WOL of Ethernet LAN
1.2A
+3VSUS
R3311 1 2 0Ohm
tx_r0805_short
1.2A
200 mils
DVDD33
C3316 0.1UF/16V
C3317 0.1UF/16V
C3399 4.7UF/6.3V @
C3398 4.7UF/6.3V @
reserve for surge imprvement
FAE recommand
GND

PCH
(PU@+3VS,10Kohm

24 CLK_REQ10_LAN#
SP3301
CLKREQB
nb_r0402_short_5mil_small
CLKREQB

24,53 PCIE_WAKE#
SP3302
PCIE_WAKE#_LAN
nb_r0402_short_5mil_small
LANWAKEB

ISOLATE
ISOLATEB

HSIP
HSIN
PCIE_TXP13_LAN 21
PCIE_TXN13_LAN 21

HSOP
HSON
PCIE_RXP13_LAN_C
PCIE_RXN13_LAN_C
C33021 2 0.1UF/16V
C33011 2 0.1UF/16V
PCIE_RXP13_LAN 21
PCIE_RXN13_LAN 21

C3301and C3302 Close to
U3301 pin17, pin18

+3VS
R3306 1KOhm
ISOLATE
R3307 15KOhm
GND

REFCLK_P
REFCLK_N
CLK_PCIE_LAN_PCH 25
CLK_PCIE_LAN#_PCH 25

LED0
LED1/GPO
LED2

24,30,31,32,51,53,74 BUF_PLT_RST#
PERSTB

U3302
AZ5725-01F
VC
GND1
GND

RSET
R3302 2.49KOhm 1%
R3302 close to pin31
GND
GND

CKXTAL1
CKXTAL2
XTAL1_LAN
XTAL2_LAN

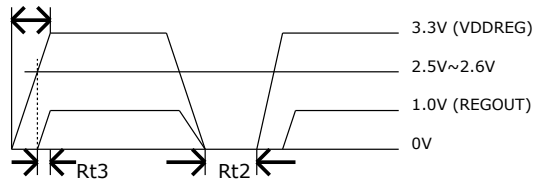
XTAL1_LAN
XTAL2_LAN
X3302 25MHZ
C3304 10PF/50V
C3303 10PF/50V
GND
GND
GND

RTL8111H-CG
02T0J0000071

U3301B
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
RTL8111H-CG
02T0J0000071
GND

Power sequence

3.3V rising time must be
more than 0.5ms and less than 100ms.



	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

PEGATRON Title : LAN 1
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
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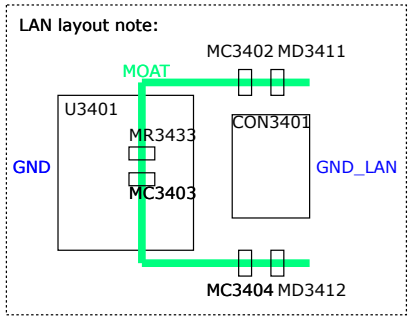
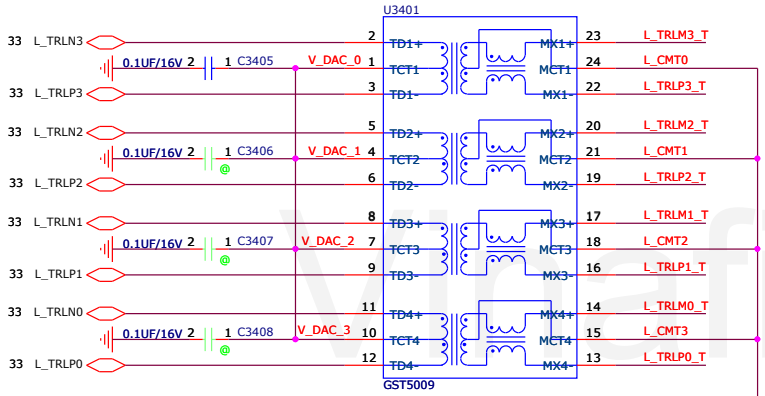
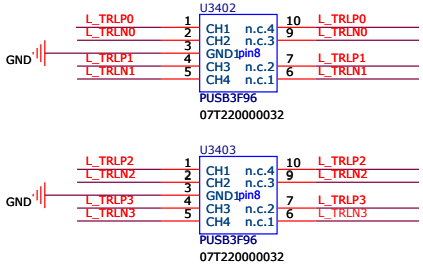
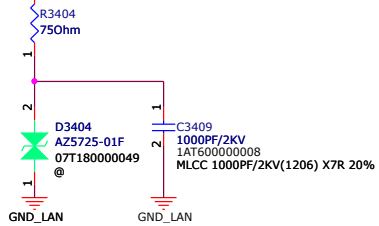
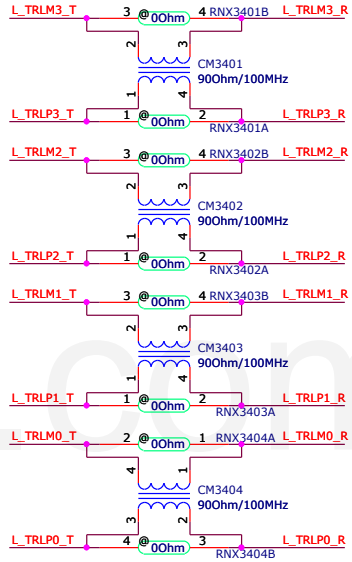
34.Transformer/RJ45

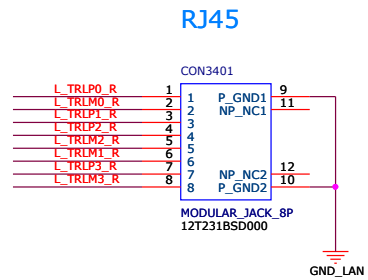


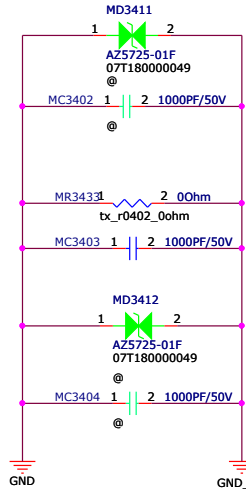












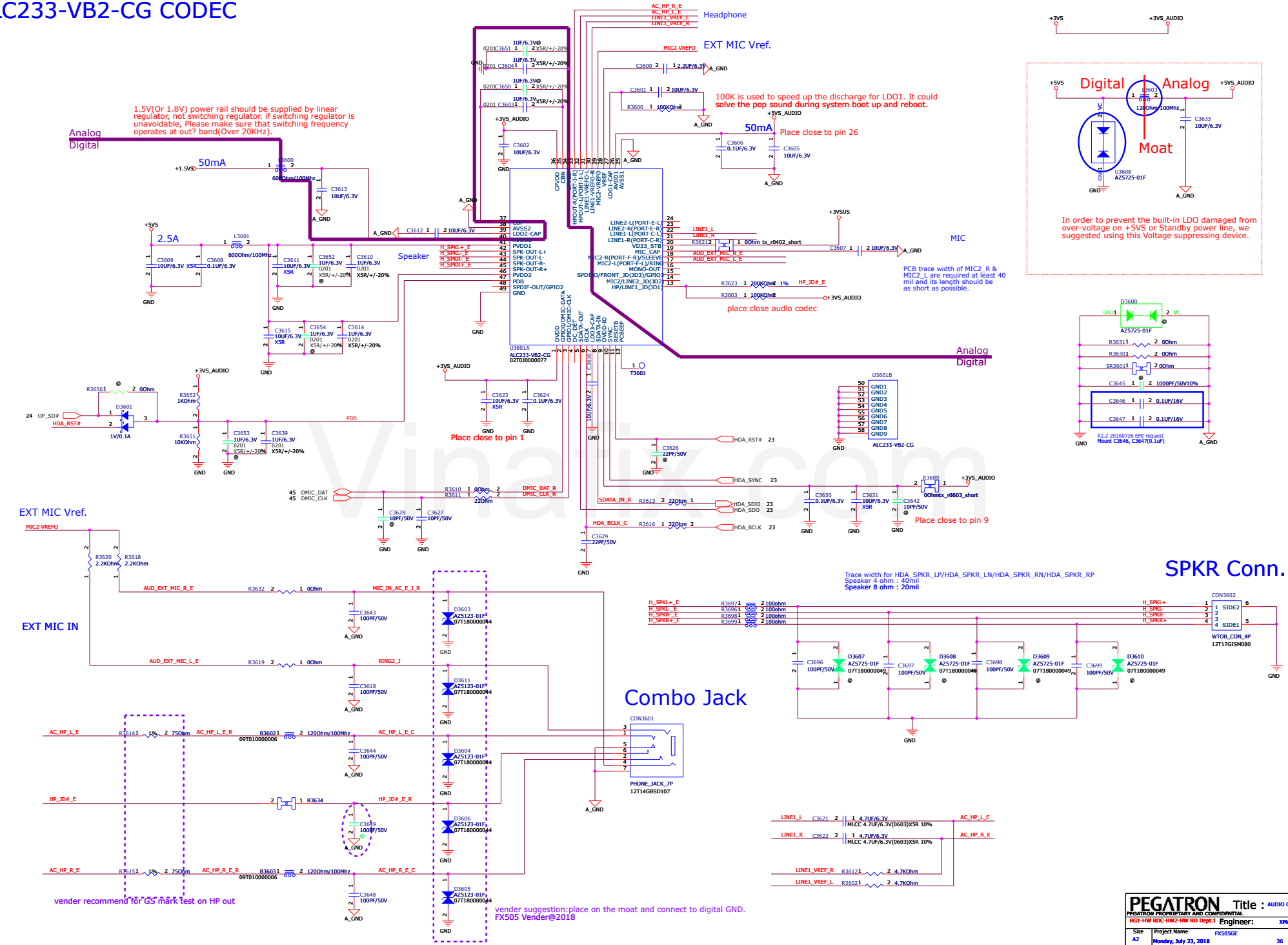
PEGATRON Title : LAN 2

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 34 of 99	

ALC233-VB2-CG CODEC

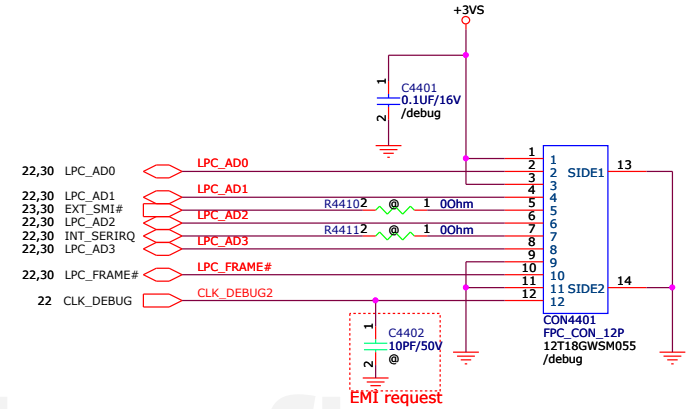


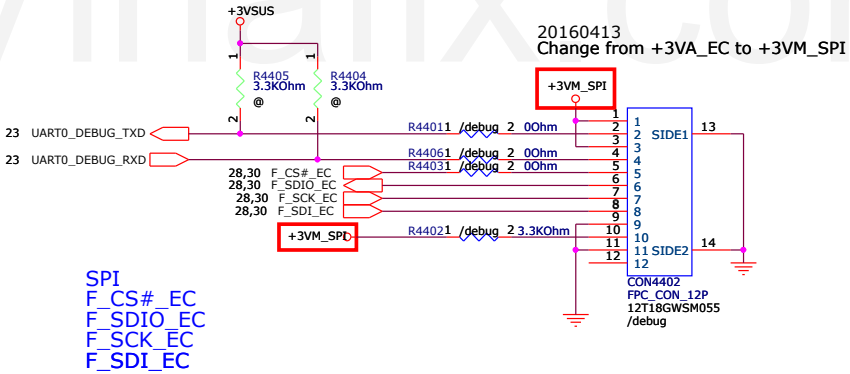
PEGATRON	Title : AUDIO CODEC		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: XMAN		
Size A2	Project Name FX505GE		Rev 1.0
Date: Monday, July 23, 2018	Sheet 36 of 99		

+3VS +3VS 7,16,21,22,23,24,28,30,31,32,33,36,45,48,50,51,57,70,74,87,88,89,91,92,96

+3VSUS +3VSUS 7,21,22,23,24,26,28,30,31,33,36,48,53,68,74,81,88,92,96

+3VM_SPI +3VM_SPI 28





SPI
F_CS#_EC
F_SDIO_EC
F_SCK_EC
F_SDI_EC

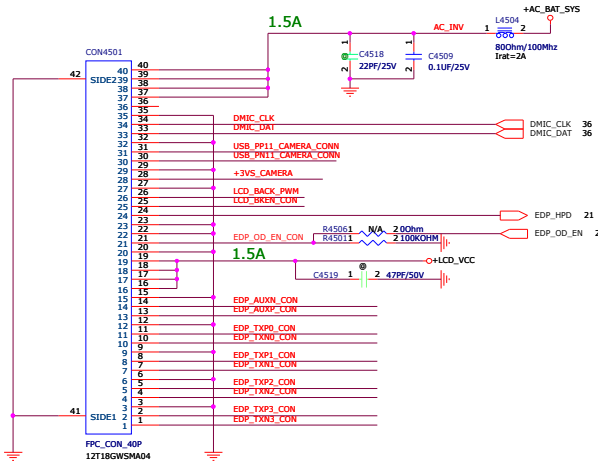
PEGATRON Title : DEBUG

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

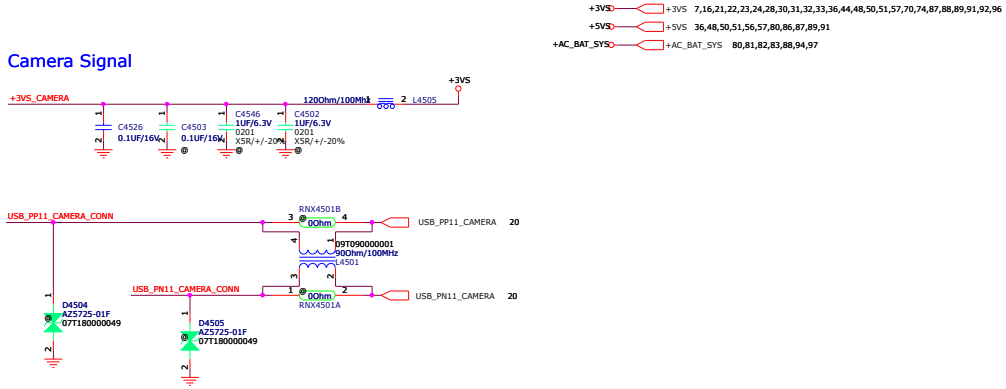
Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 44 of 99	

eDP Conn.

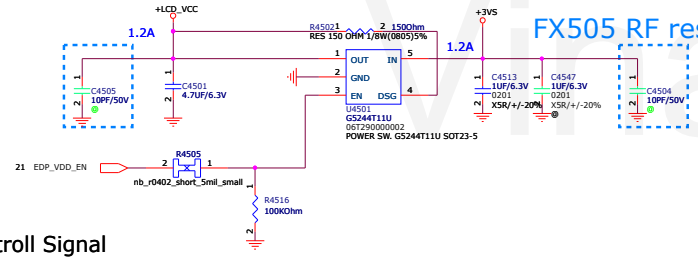


Reserving for OD function

Camera Signal

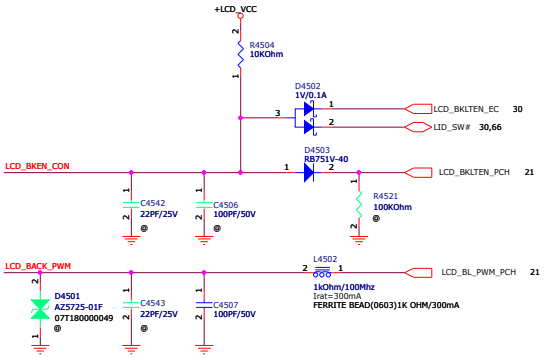


LCD VDDEN / +LED_VCC

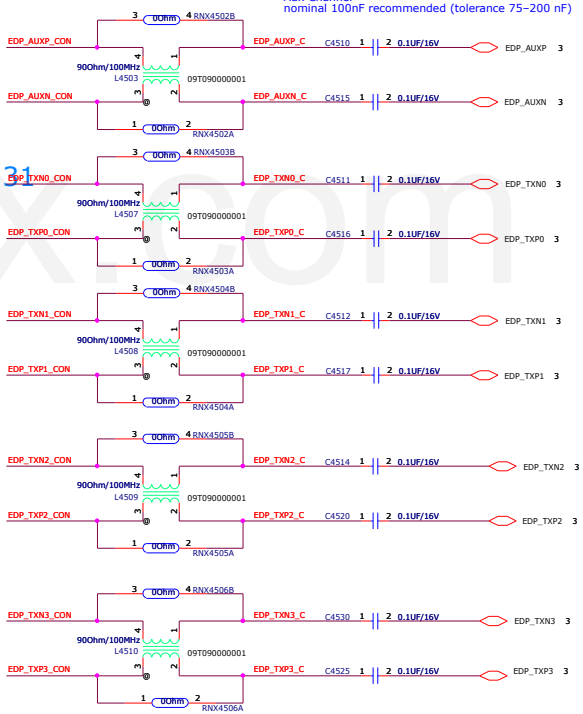


FX505 RF reserve @20180131

Controll Signal

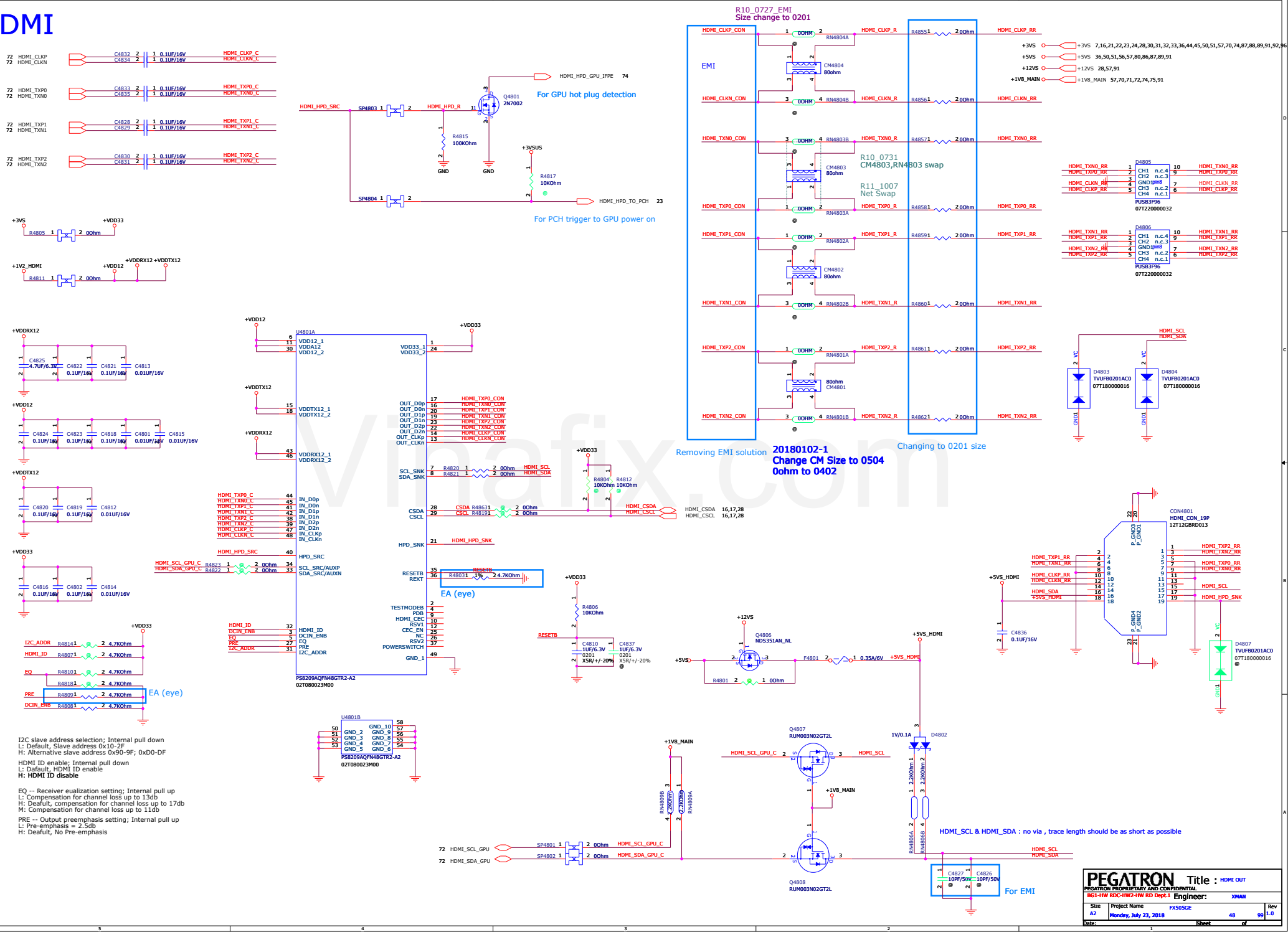


CFL PDG:
AC caps are required to be placed before the motherboard eDP* connector
Main Link
nominal 100nF recommended (tolerance 75~265 nF)
Aux Channel
nominal 100nF recommended (tolerance 75~200 nF)



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EDP/MIC
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 45 of 99

HDMI


R10_0727_EMI
Size change to 0201
EMI
Removing EMI solution
20180102-1
Change CM Size to 0504
0ohm to 0402
Changing to 0201 size
R10_0731
CM4803,RN4803 swap
R11_1007
Net Swap
For GPU hot plug detection
For PCH trigger to GPU power on
EA (eye)
EA (eye)
I2C slave address selection; Internal pull down
L: Default, Slave address 0x10-2F
H: Alternative slave address 0x90-9F; 0xD0-DF
HDMI ID enable; Internal pull down
L: Dafault, HDMI ID enable
H: HDMI ID disable
EQ -- Receiver eualization setting; Internal pull up
L: Compensation for channel loss up to 13db
H: Deafult, compensation for channel loss up to 17db
M: Compensation for channel loss up to 11db
PRE -- Output preemphasis setting; Internal pull up
L: Pre-emphasis = 2.5db
H: Deafult, No Pre-emphasis
HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible
For EMI
PEGATRON
Title : HDMI OUT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: XMAN
Size A2
Project Name FX505GE
Rev 1.0
Date: Monday, July 23, 2018
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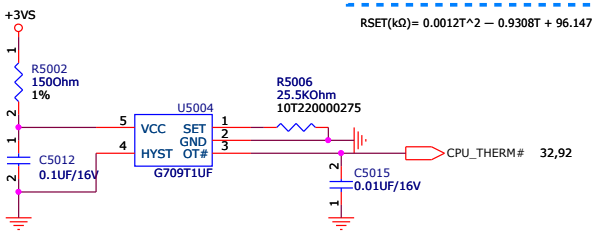
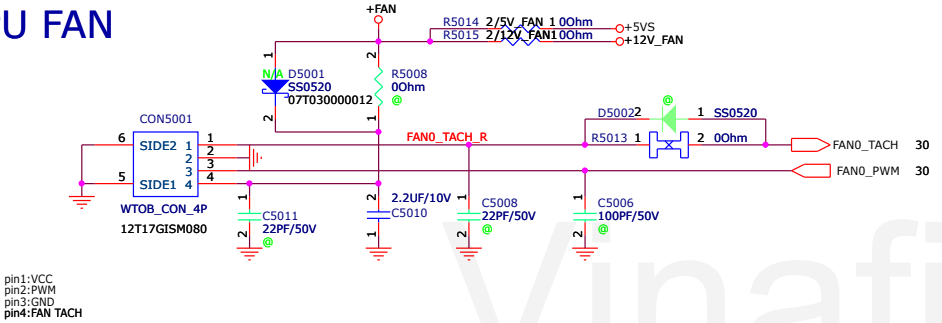
CPU Thermal Sensor

temperature set=85 C

RSET(kΩ)= 0.0012T^2 – 0.9308T + 96.147



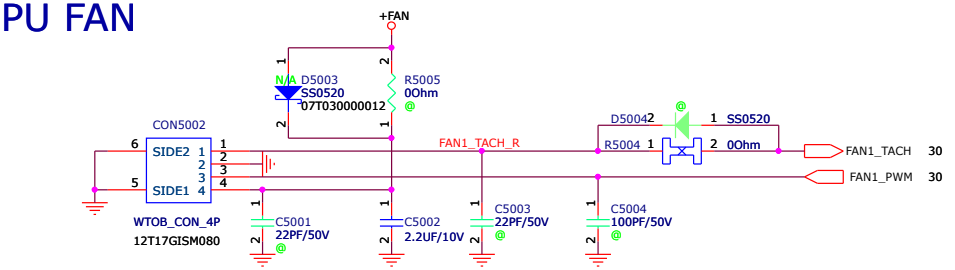
CPU FAN



EC(PU@+3VS,10Kohm

pin1:VCC
pin2:PWM
pin3:GND
pin4:FAN TACH

GPU FAN



EC(PU@+3VS,10Kohm

pin1:VCC
pin2:PWM
pin3:GND
pin4:FAN TACH

PEGATRON Title : FAN/THERMAL

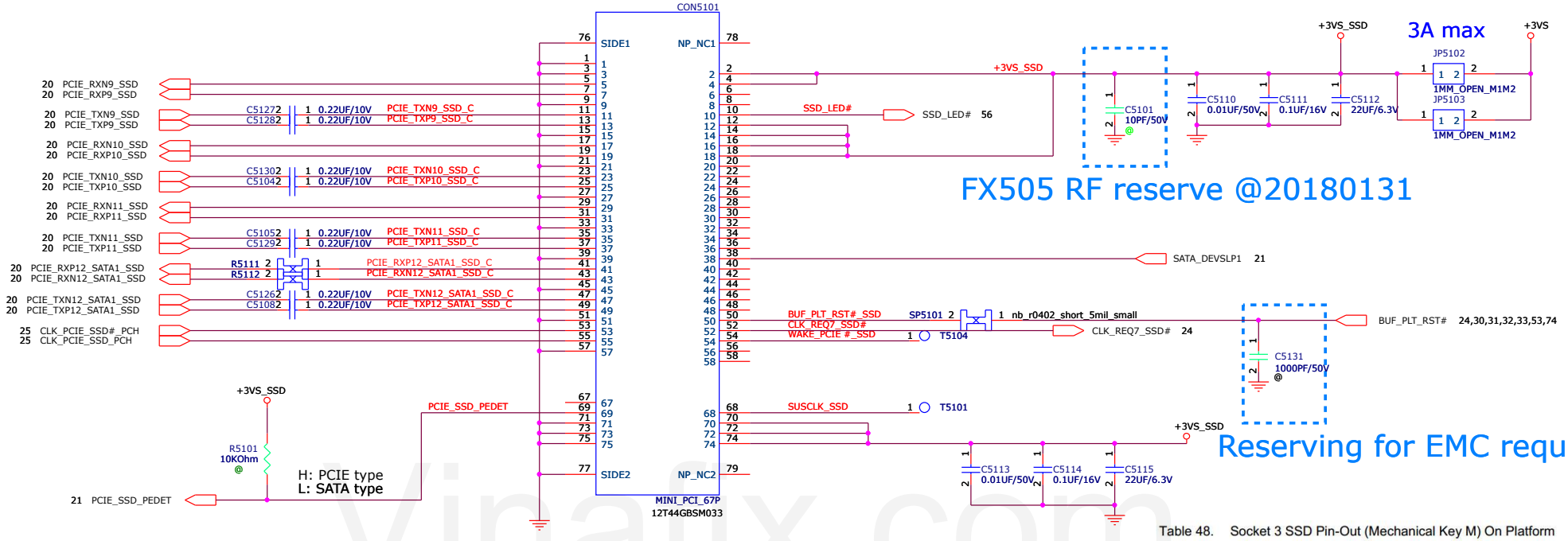
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 50 of 99	

SSD/HDD

M.2 2280 KEY-M



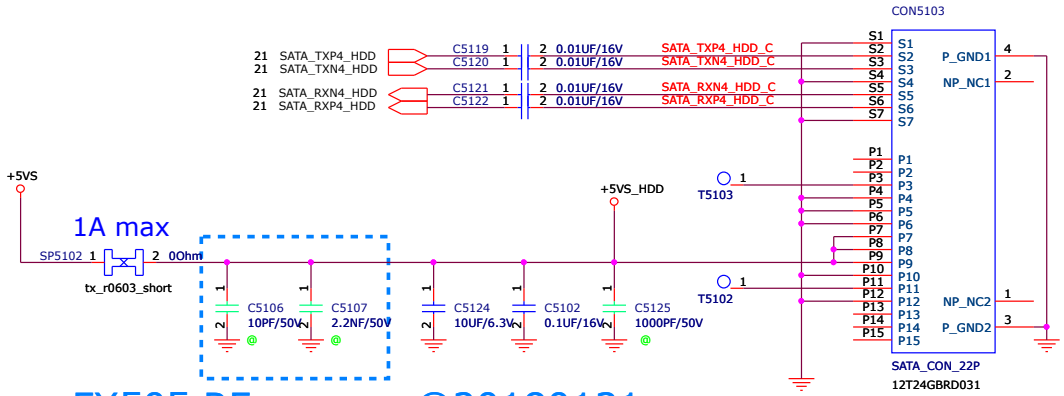
FX505 RF reserve @20180131

Reserving for EMC request

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3v	GND	75
72	3.3v	GND	73
70	3.3v	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
58	N/C		
56	N/C	GND	57
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKp	55
52	CLKREQ# (I/O)(0/3.3V) or N/C	REFCLKn	53
50	PERST# (O)(0/3.3V) or N/C	GND	51
48	N/C	PETp0/SATA-A+	49
46	N/C	PETn0/SATA-A-	47
44	N/C	GND	45
42	N/C	PERp0/SATA-B-	43
40	N/C	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	N/C	PETp1	37
34	N/C	PETn1	35
32	N/C	GND	33
30	N/C	PERp1	31
28	N/C	PERn1	29
26	N/C	GND	27
24	N/C	PETp2	25
22	N/C	PETn2	23
20	N/C	GND	21
18	3.3V	PERp2	19
16	3.3V	PERn2	17
14	3.3V	GND	15
12	3.3V	PETp3	13
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	PETn3	11
8	N/C	GND	9
6	N/C	PERp3	7
4	3.3V	PERn3	5
2	3.3V	GND	3
		GND	1

SATA Conn. 2.5"HDD



FX505 RF reserve @20180131

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

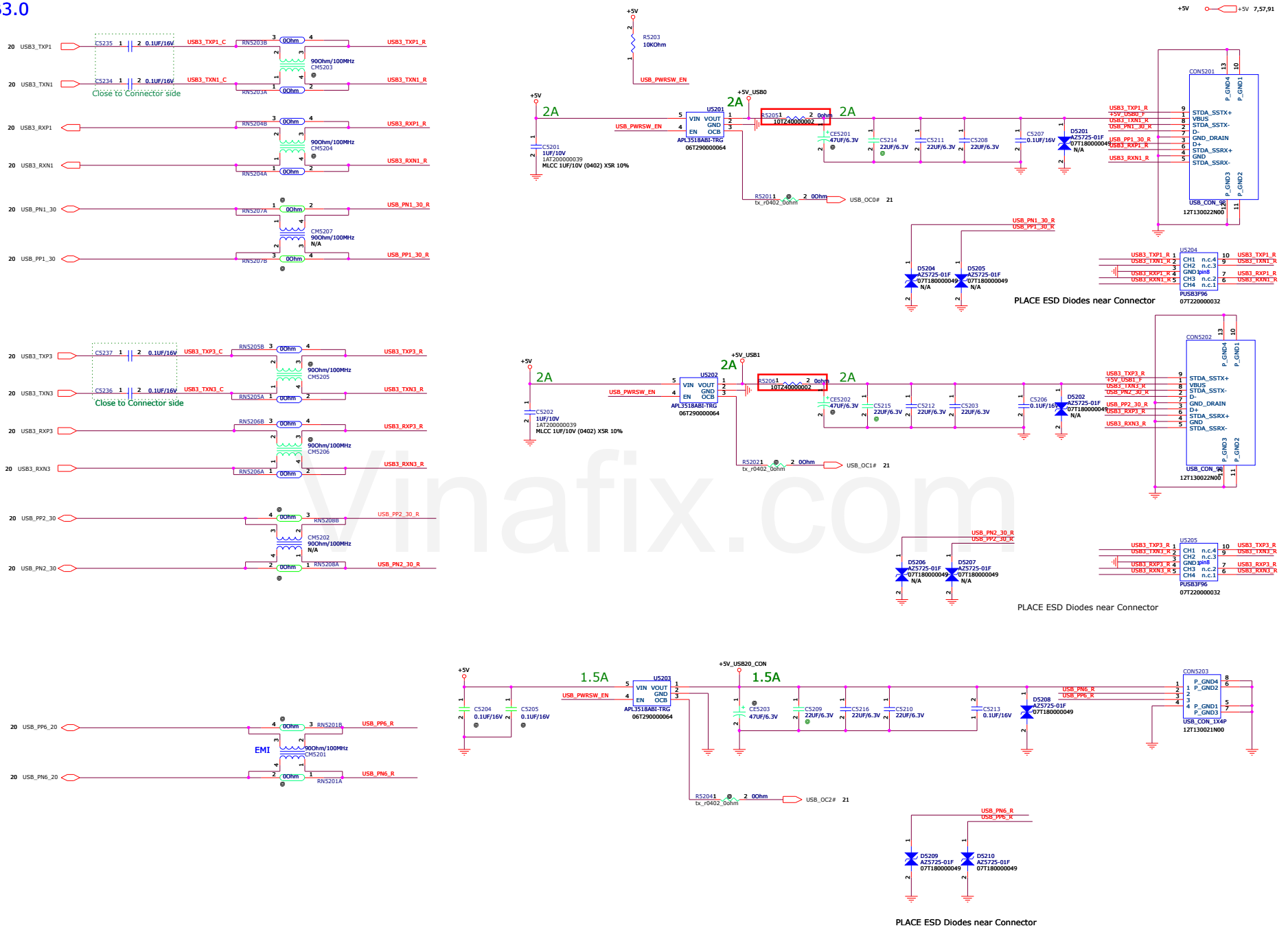
Title : SSD/HDD

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0

Date: Monday, July 23, 2018 Sheet 51 of 99

52.USB3.0



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

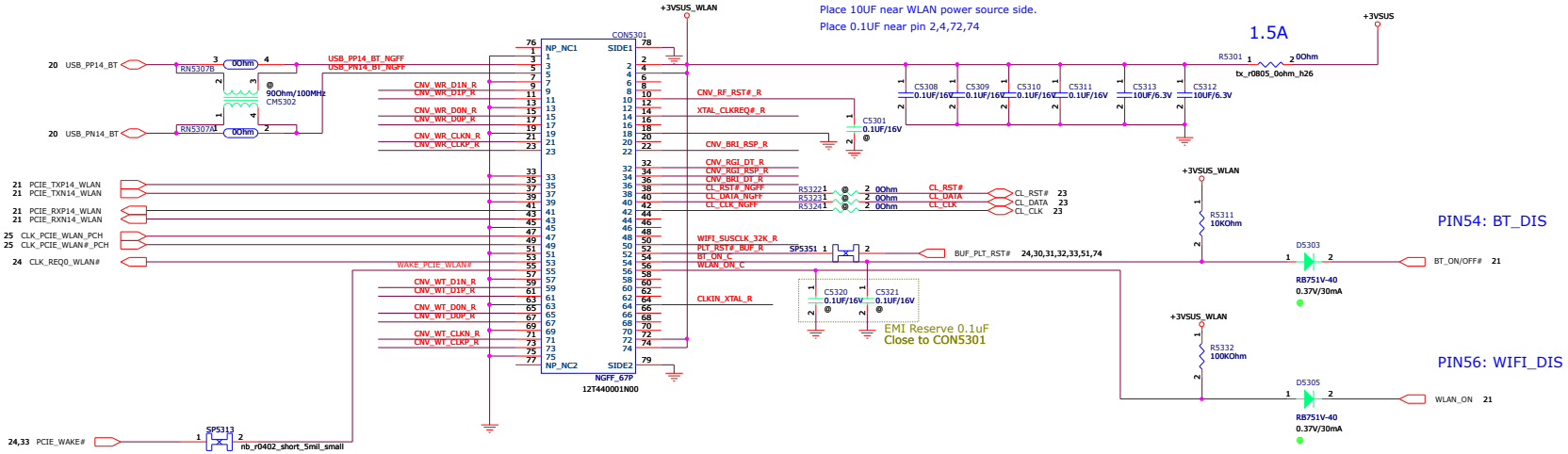
Title : USB 3CAK

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A2	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 52 of 99	

WLAN+BT

M.2 2230 KEY-E



WLAN bypass capactors:

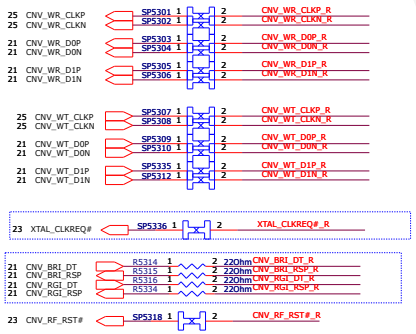
+3VSUS +3VSUS 7,21,22,23,24,26,28,30,31,33,36,44,48,68,74,81,88,92,96

+1.8VSUS +1.8VSUS 21,26,84

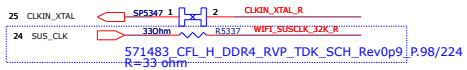
CNVi

R

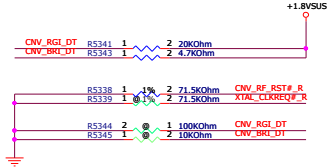
T



571391_CFL_H_PDG_Rev1p0_p.483/661



571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.98/224
R=33 ohm



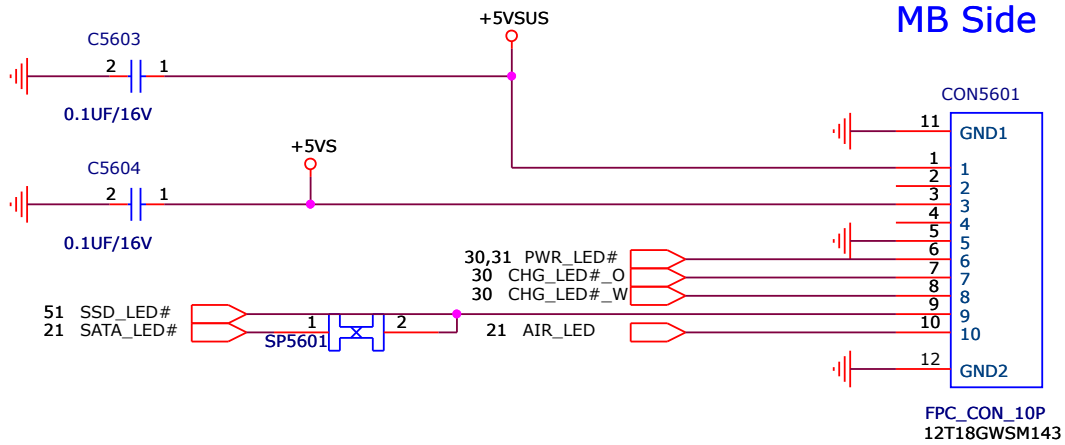
	Standard M.2 Key E	LcP Signals	LcP Signals	Standard M.2 Key E	
74	+V3P3A		GND		75
72	+V3P3A		WT_CLKP	REFCLKN1	73
70	PEWake1# (IO)(0/3.3V)		WT_CLKN	REFCLKP1	71
68	CLKREQ1# (IO)(0/3.3V)		GND		69
66	PERST1# (O)(0/3.3V)		WT_D0P	PERn1	67
64	RESERVED	REFCLKO(I)(1V@38.4MHz)	WT_D0N	PERp1	65
62	ALERT# (I)(0/1.8)	A4WP_IRQ#	GND		63
60	I2C_CLK (O)(0/1.8V)	A4WP_I2C_CLK	WT_D1P	PETn1	61
58	I2C_DATA (IO)(0/1.8)	A4WP_I2C_DATA	WT_D1N	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)		GND		57
54	W_DISABLE2# (O)(0/3.3V)		PEWake0# (IO)(0/3.3V)		55
52	PERST0# (O)(0/3.3V)		CLKREQ0# (IO)(0/3.3V)		53
50	SUSCLK(32kHz) (O)(0/3.3V)	C_P32K (3.3V Tolerant)	GND		51
48	COEX_TXD (O)(0/1.8V)		REFCLKN0		49
46	COEX_RXD (O)(0/1.8V)		REFCLKP0		47
44	COEX3 (IO)(0/1.8V)		GND		45
42	CLink CLK		PERn0		43
40	CLink DATA		PERp0		41
38	CLink RESET (O)(0/3.3V)		GND		39
36	LPSS UART RTS (O)(0/1.8V)	/ BRI_DT (MUX'd in PCH/SoC)	PETn0		37
34	LPSS UART CTS (I)(0/1.8V)	/ RGI_RSP (MUX'd in PCH/SoC)	PETp0		35
32	LPSS UART Tx (O)(0/1.8V)	/ RGI_DT (MUX'd in PCH/SoC)	GND		33
E	Connector Key		Connector Key		E
	Connector Key		Connector Key		
	Connector Key		Connector Key		
	Connector Key		Connector Key		
22	LPSS UART Rx (I)(0/1.8V)	/ BRI_RSP (MUX'd in PCH/SoC)	WGR_CLKP	SDIO Reset#(O)(0/1.8V)	23
20	UART Wake# (I)(0/3.3V)		WGR_CLKN	SDIO Wake#(I)(0/1.8V)	21
18	GND	GNO/UNA_EN (LcP Production)	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED2# (I)(OD)		WGR_D0P	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (O)(0/1.8V)	/ CLKREQ0 (MUX'd in PCH/SoC)	WGR_D0N	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (I)(0/1.8V)		GND	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (O)(0/1.8V)	/ RF_RESET_B (MUX'd in PCH/SoC)	WGR_D1P	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (O)(0/1.8V)		WGR_D1N	SDIO CLK(O)(0/1.8V)	9
6	LED1# (I)(OD)		GND		7
4	+V3P3A		USB_D-		5
2	+V3P3A		USB_D+		3
			GND		1

571391_CFL_H_PDG_Rev1p0_p.482/661
BRI,RGI:
DT:Resistor R1 Spec: 33 Ohm, to be placed close to the connector.
RSP:Resistor R1 Spec: 22 Ohm, to be placed close to the connector.
571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.97/224
R=0ohm

571182_CNL_PCH_H_EDS_Vol_1_Rev_1p1_P.60/572
GPP_J6 /CNV_RGI_DT /UART0_TXD:
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

571483_CFL_H_DDR4_RVP_TDK_SCH_Rev0p9_P.107/224
GPP_J4 /CNV_BRI_DT /UART0_RTS# :
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : WLAN
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 53 of 99



+5VSUS +5VSUS 31,81

+5VS +5VS 36,48,50,51,57,80,86,87,89,91

Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION

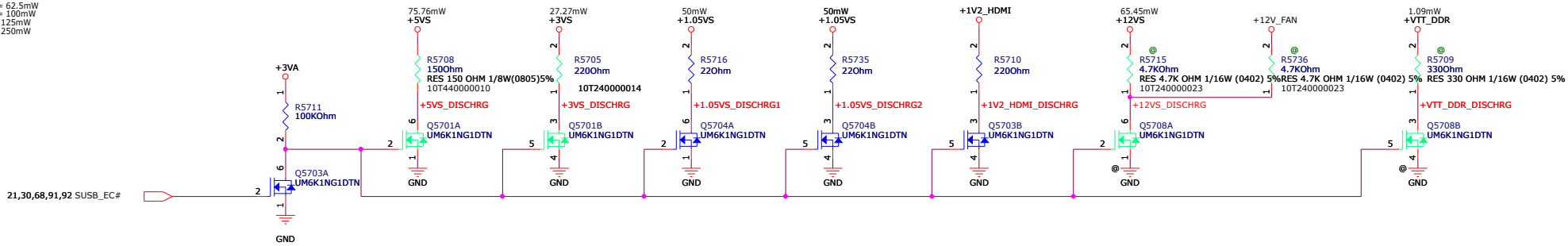
PWR LED LED5601 | Charger LED LED5606 | HDD LED LED5604 | RF LED LED5602

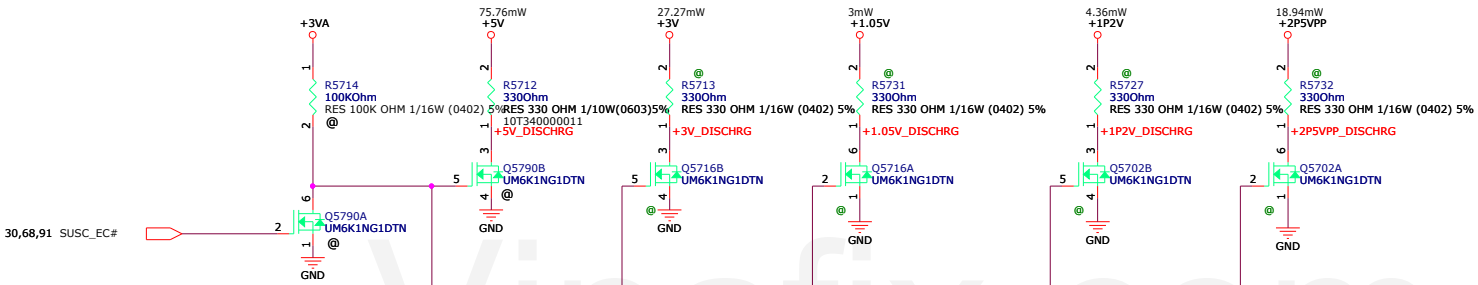
HDD LED

PEGATRON Title : LED
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept. Engineer: XMAN

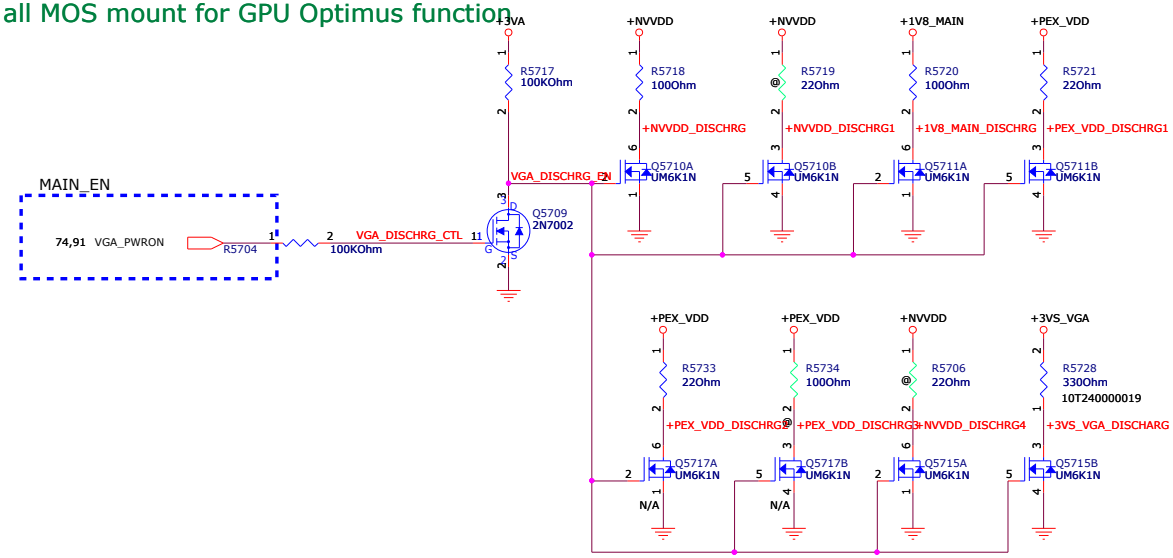
Size	Project Name	Rev
A4	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 56 of 99	

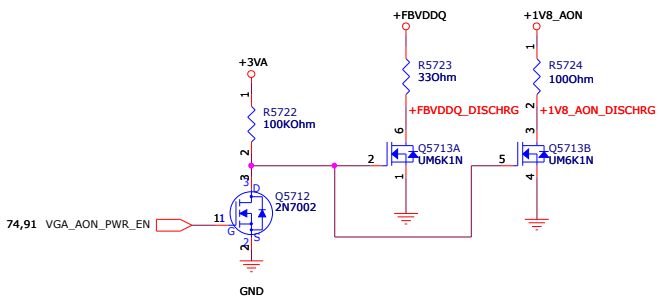
V^2/R
0402 = 1/16W = 62.5mW
0603 = 1/10W = 100mW
0805 = 1/8W = 125mW
1206 = 1/4W = 250mW





all MOS mount for GPU Optimus function





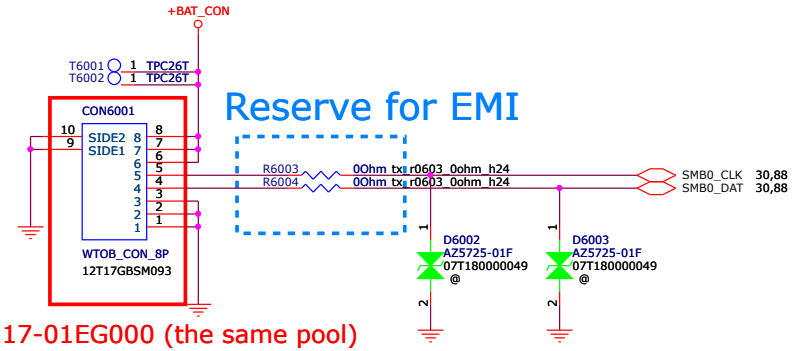
PEGATRON DT-MB RESTRICTED SECRET
<Variant Name>

PEGATRON Title : PWR discharge
BG1-HW RD Div.2-HW RD Dept.1 Engineer: Allen Kuo

Size	Project Name	Rev
Custom	FX505GE	1.0

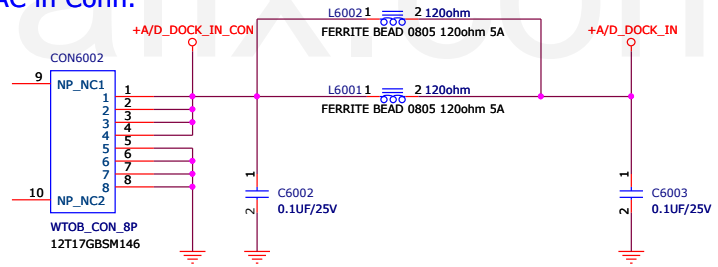
Date: Monday, July 23, 2018 Sheet 57 of 99

Battery Conn.



ABBA assign: 1217-017L000, doesn't include 1217-01EG000 (the same pool)

AC in Conn.



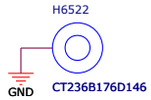
FX505GE N17P Adaptor: 120W
FX505GE N17E Adaptor: 150W

PEGATRON Title : BAT/AC IN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 60 of 99	

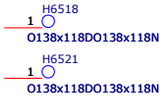
65.NUT,Screw hole,Tooling hole

M.2 SSD NUT:



Tooling hole

drill 3*3.5

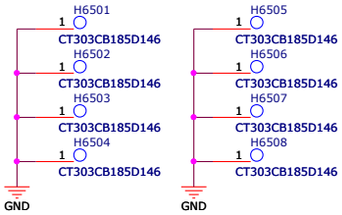


drill 1.7

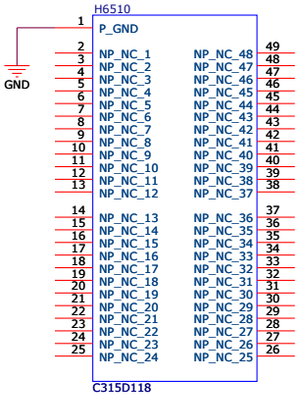
drill 2.2*1.7

Screw hole

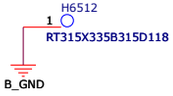
B group:
CPU GPU bracket hole

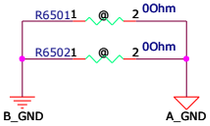


D group:

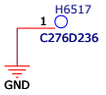


Near Audio Jack
TOP: square 8
BOT: phi 8 drill 3

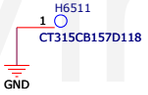




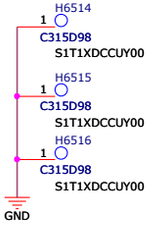
E:
TOP: phi 7 drill 6
BOT: phi 7 drill 6



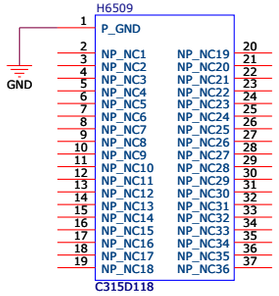
F:
TOP: phi 8 drill 3
BOT: phi 4 drill 3

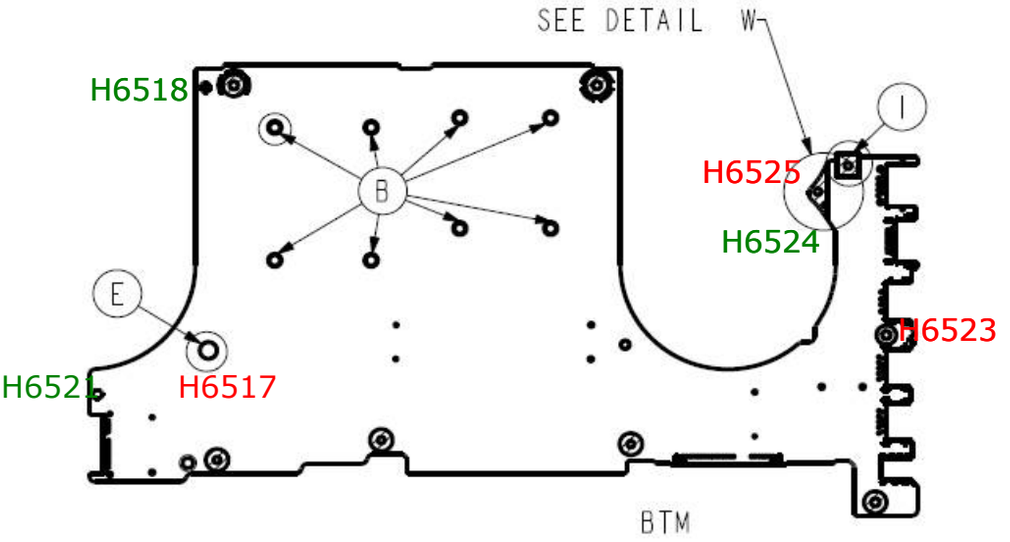


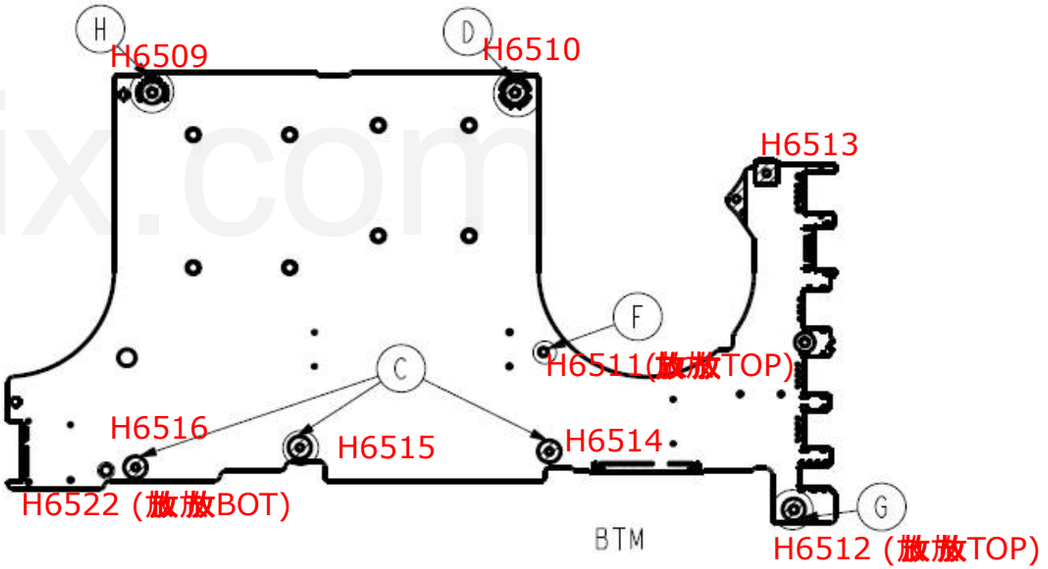
C group:
TOP: phi 8 drill 2.5
BOT: phi 8 drill 2.5



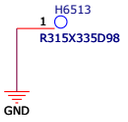
H group:



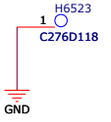




I group:
TOP: square8*8.5 drill 2.5
BOT: square8*8.5 drill 2.5



TOP: phi 7 drill 3
BOT: phi 7 drill 3

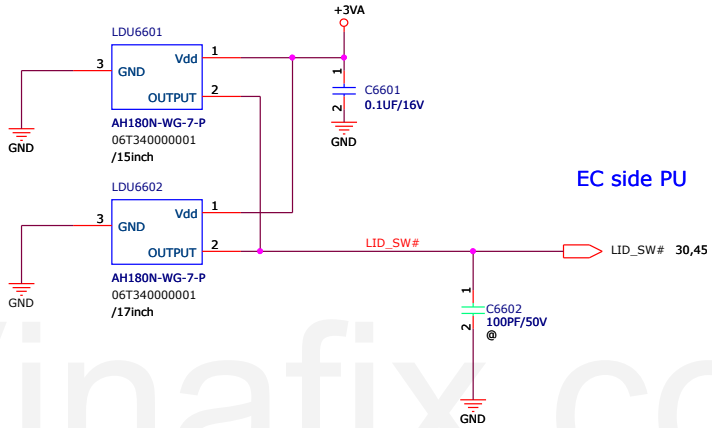


TOP: phi 3 drill 2.5
BOT: phi 3 drill 2.5

PEGATRON	Title : NUT/HOLE	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: XMAN	
Size: Custom	Project Name: FX505GE	Rev: 1.0
Date: Monday, July 23, 2018	Sheet: 65 of 99	

+3VA +3VA 25,30,57,74,81,93

Hall sensor



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : TO DB
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 66 of 99	

+3VSUS +3VSUS 7,21,22,23,24,26,28,30,31,33,36,44,48,53,74,81,88,92,96

EC processing time (3ms~33ms)

24,30 PM_SUSB# R6801 1 2 SUSB_EC# 21,30,57,91,92

24,30 PM_SUSC# R6802 1 2 SUSC_EC# 30,57,91

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms
Delay By EC(2ms)+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC R68091 2 nb_r0402_short_5mil_small

PM_SUSB# 1

U6802 A B GND VCC Y 2 3 5 4 @ Vcc=2~5.5

+3VSUS

R68111 2 nb_r0402_short_5mil_small

+3V

R6842 10KOhm

R6808 @100KOhm

C6804 0.1UF/25V @

GND GND

DE_ALL_SYS_PGD_HW

R68101 2 nb_r0402_short_5mil_small DELAY_ALL_SYSTEM_PWRGD 7,24

R68051 2 nb_r0402_short_5mil_small CPU_VRON 80

For shut down Sequence
Tplt17 < 1us

PM_SUSB# 2

D6802 1V/0.1A

EC DE_ALL_SYS_PGD_EC p.30

PM_SUSB# p.24

DELAY_ALL_SYSTEM_PWRGD p.68

15 p.68 CPU_VRON

for PM_PWROK p.24

for VCCST_PWRGD p.7

IMVP8 VR
CORE
VCCSA
VCCGT
VCCGTX

For shut down Sequence Tplt17 < 200us
Due to PDG1.2 Figure 43-5. SYS_PWROK drop after PM_SUSB# before CPU_VRON to add this solution

EC 20 SYS_PWROK_EC p.30

PM_SUSB# p.24

21 SYS_PWROK p.68 PCH

30 SYS_PWROK_EC R68431 2 nb_r0402_short_5mil_small SYS_PWROK_EC_G

PM_SUSB# 1

U6803 A B GND VCC Y 2 3 5 4 @ Vcc=2~5.5

+3VSUS

+3V

R6841 100KOhm

R6806 @100KOhm

GND

R68041 2 nb_r0402_short_5mil_small SYS_PWROK 24,30

PM_SUSB# 2

D6811 1V/0.1A

PEGATRON Title : BYPASS EC SEQ.

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size	Project Name	Rev
A3	FX505GE	1.0
Date: Monday, July 23, 2018	Sheet 68 of 99	

+1V8_AON 57,74,75,87,89,91
+3VS 7,16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,74,87,88,89,91,92,96
+PEX_VDD 57,72,96
+1V8_MAIN 48,57,71,72,74,75,91

+1V8_AON
R7003 10KOhm @
PEX_RST# 74
R7004 100KOhm
GND

+3VS +1V8_MAIN
R7005 100KOhm
SP7009
+1V8_AON
R7006 10KOhm
24 CLK_REQ9_PEG#
CLK_REQ9_PEG#_Q
Q7000 RUM003N02GT2L
Rdson=1.4Ohm/Vgs(th)=1V
PEX_RST# BK26
25 CLK_PCIE_PEG_PCH BM26
25 CLK_PCIE_PEG#_PCH BM27

Inverting polarity for route request

6 PCIENB_RXP[0..15]
6 PCIENB_RXN[0..15]

PCIEG => From CPU
PCIENB : to CPU

6 PCIEG_TXP[0..15]
6 PCIEG_TXN[0..15]

U7000A
1/23 PCI_EXPRESS

PCIENB_RXP0	C7001	0.22UF/10V	PCIENB_RXP0_C	BG26	PEX_TX0_P
PCIENB_RXN0	C7002	0.22UF/10V	PCIENB_RXN0_C	BH26	PEX_TX0_N
PCIEG_TXP0				BL27	PEX_RX0_P
PCIEG_TXN0				BK27	PEX_RX0_N
PCIENB_RXP1	C7003	0.22UF/10V	PCIENB_RXP1_C	BF26	PEX_TX1_P
PCIENB_RXN1	C7004	0.22UF/10V	PCIENB_RXN1_C	BE26	PEX_TX1_N
PCIEG_TXN1				BK29	PEX_RX1_P
PCIEG_TXP1				BL29	PEX_RX1_N
PCIENB_RXP2	C7005	0.22UF/10V	PCIENB_RXP2_C	BF27	PEX_TX2_P
PCIENB_RXN2	C7006	0.22UF/10V	PCIENB_RXN2_C	BG27	PEX_TX2_N
PCIEG_TXP2				BM29	PEX_RX2_P
PCIEG_TXN2				BM30	PEX_RX2_N
PCIENB_RXP3	C7007	0.22UF/10V	PCIENB_RXP3_C	BG29	PEX_TX3_P
PCIENB_RXN3	C7008	0.22UF/10V	PCIENB_RXN3_C	BH29	PEX_TX3_N
PCIEG_TXP3				BL30	PEX_RX3_P
PCIEG_TXN3				BK30	PEX_RX3_N
PCIENB_RXP4	C7009	0.22UF/10V	PCIENB_RXP4_C	BF29	PEX_TX4_P
PCIENB_RXN4	C7010	0.22UF/10V	PCIENB_RXN4_C	BE29	PEX_TX4_N
PCIEG_TXP4				BK32	PEX_RX4_P
PCIEG_TXN4				BL32	PEX_RX4_N
PCIENB_RXP5	C7011	0.22UF/10V	PCIENB_RXP5_C	BF30	PEX_TX5_P
PCIENB_RXN5	C7012	0.22UF/10V	PCIENB_RXN5_C	BG30	PEX_TX5_N
PCIEG_TXP5				BM32	PEX_RX5_P
PCIEG_TXN5				BM33	PEX_RX5_N
PCIENB_RXP6	C7013	0.22UF/10V	PCIENB_RXP6_C	BG32	PEX_TX6_P
PCIENB_RXN6	C7014	0.22UF/10V	PCIENB_RXN6_C	BH32	PEX_TX6_N
PCIEG_TXP6				BL33	PEX_RX6_P
PCIEG_TXN6				BK33	PEX_RX6_N
PCIENB_RXP7	C7015	0.22UF/10V	PCIENB_RXP7_C	BF32	PEX_TX7_P
PCIENB_RXN7	C7016	0.22UF/10V	PCIENB_RXN7_C	BE32	PEX_TX7_N
PCIEG_TXP7				BK35	PEX_RX7_P
PCIEG_TXN7				BL35	PEX_RX7_N
PCIENB_RXP8	C7017	0.22UF/10V	PCIENB_RXP8_C	BF33	PEX_TX8_P
PCIENB_RXN8	C7018	0.22UF/10V	PCIENB_RXN8_C	BG33	PEX_TX8_N
PCIEG_TXP8				BM35	PEX_RX8_P
PCIEG_TXN8				BM36	PEX_RX8_N
PCIENB_RXP9	C7019	0.22UF/10V	PCIENB_RXP9_C	BG35	PEX_TX9_P
PCIENB_RXN9	C7020	0.22UF/10V	PCIENB_RXN9_C	BH35	PEX_TX9_N
PCIEG_TXP9				BL36	PEX_RX9_P
PCIEG_TXN9				BK36	PEX_RX9_N
PCIENB_RXP10	C7021	0.22UF/10V	PCIENB_RXP10_C	BF35	PEX_TX10_P
PCIENB_RXN10	C7022	0.22UF/10V	PCIENB_RXN10_C	BE35	PEX_TX10_N
PCIEG_TXP10				BK38	PEX_RX10_P
PCIEG_TXN10				BL38	PEX_RX10_N
PCIENB_RXP11	C7023	0.22UF/10V	PCIENB_RXP11_C	BF36	PEX_TX11_P
PCIENB_RXN11	C7024	0.22UF/10V	PCIENB_RXN11_C	BG36	PEX_TX11_N
PCIEG_TXP11				BM38	PEX_RX11_P
PCIEG_TXN11				BM39	PEX_RX11_N
PCIENB_RXP12	C7025	0.22UF/10V	PCIENB_RXP12_C	BG38	PEX_TX12_P
PCIENB_RXN12	C7026	0.22UF/10V	PCIENB_RXN12_C	BH38	PEX_TX12_N
PCIEG_TXP12				BL39	PEX_RX12_P
PCIEG_TXN12				BK39	PEX_RX12_N
PCIENB_RXP13	C7027	0.22UF/10V	PCIENB_RXP13_C	BF38	PEX_TX13_P
PCIENB_RXN13	C7028	0.22UF/10V	PCIENB_RXN13_C	BE38	PEX_TX13_N
PCIEG_TXP13				BK41	PEX_RX13_P
PCIEG_TXN13				BL41	PEX_RX13_N
PCIENB_RXP14	C7029	0.22UF/10V	PCIENB_RXP14_C	BF39	PEX_TX14_P
PCIENB_RXN14	C7030	0.22UF/10V	PCIENB_RXN14_C	BG39	PEX_TX14_N
PCIEG_TXP14				BM41	PEX_RX14_P
PCIEG_TXN14				BM42	PEX_RX14_N
PCIENB_RXP15	C7031	0.22UF/10V	PCIENB_RXP15_C	BH41	PEX_TX15_P
PCIENB_RXN15	C7032	0.22UF/10V	PCIENB_RXN15_C	BG41	PEX_TX15_N
PCIEG_TXP15				BL42	PEX_RX15_P
PCIEG_TXN15				BK42	PEX_RX15_N

N17E-G1
020A-010R000

PEX_DVDD_1 BB33
PEX_DVDD_2 BB35
PEX_DVDD_3 BB36
PEX_DVDD_4 BC33
PEX_DVDD_5 BC35
PEX_DVDD_6 BC36
PEX_DVDD_7 BD33
PEX_DVDD_8 BD36
0.285A +PEX_DVDD

C7033 1uF/6.3V 0201 XSR/+/-10%
C7034 1uF/6.3V 0201 XSR/+/-10%
C7035 1uF/6.3V 0201 XSR/+/-10%
C7036 1uF/6.3V 0201 XSR/+/-10%
C7051 1uF/6.3V 0201 XSR/+/-10% @
C7052 1uF/6.3V 0201 XSR/+/-10% @
C7053 1uF/6.3V 0201 XSR/+/-10% @
C7054 1uF/6.3V 0201 XSR/+/-10% @

PLACE bewteen the PS and GPU PLACE NEAR GPU
+PEX_VDD
C7037 4.7UF/6.3V
C7038 4.7UF/6.3V
C7047 10UF/6.3V
C7039 10UF/6.3V
C7040 22UF/6.3V
GND

PEX_HVDD_1 BB26
PEX_HVDD_2 BB27
PEX_HVDD_3 BB29
PEX_HVDD_4 BB32
PEX_HVDD_5 BC26
PEX_HVDD_6 BC27
PEX_HVDD_7 BC29
PEX_HVDD_8 BC30
PEX_HVDD_9 BC32
PEX_HVDD_10 BD27
PEX_HVDD_11 BD30
0.75A +PEX_HVDD

PLACE NEAR GPU
C7041 1uF/6.3V 0201 XSR/+/-10%
C7042 1uF/6.3V 0201 XSR/+/-10%
C7043 1uF/6.3V 0201 XSR/+/-10%
C7044 1uF/6.3V 0201 XSR/+/-10%
C7055 1uF/6.3V 0201 XSR/+/-10% @
C7056 1uF/6.3V 0201 XSR/+/-10% @
C7057 1uF/6.3V 0201 XSR/+/-10% @
C7058 1uF/6.3V 0201 XSR/+/-10% @

PLACE bewteen the PS and GPU
+1V8_MAIN
C7045 4.7UF/6.3V
C7046 4.7UF/6.3V
C7048 10UF/6.3V
C7049 22UF/6.3V
GND

+1V8_MAIN
PEX_PLL_HVDD BB30
0.035A +PEX_PLL_HVDD
SP7007
C7050 0.1UF/16V
GND

D0-07875-001_v03-1001768-05 P.117

PEX_HVDD	7	1.8V	4 X 1uF (0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 1 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	14	1.0V	4 X 1uF (0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

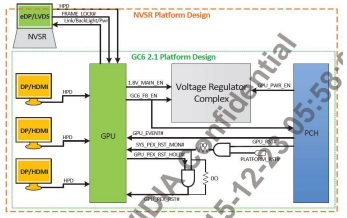


Figure 8.9 GC6 2.1 High Level Signal Connection Concept

PEX_TERMP
BL44 PEX_TERMP R7008 1 1% 2 2.49KOhm
GND

PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : NVDIA/PCIE
BG1-HW RD Div.2-HW RD Dept.3 Engineer: Hank_Zheng
Size: Custom | Project Name: FX505GE | Rev: 1.0
Date: Monday, July 23, 2018 | Sheet 70 of 105

DG-07875-001_v08 p295
IFPxy_RSET and IFPxy_PLLVDD can be left unconnected if neither of IFPx/IFPy is in use.
If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

IFPAB

U7000N 7/23 IFPAB

	DL-DVI	DVI/HDMI	DP
	SDA SCL	SDA SCL	IFPA_AUX_SDA_N BH11 / IFPA_AUX_SCL BG11
BD23 IFPAB_RSET	TXC TXC	TXC TXC	IFPA_L3_N BF21 / IFPA_L3 BG21
BD21 IFPAB_PLLVDD	TXD0 TXD0	TXD0 TXD0	IFPA_L2_N BG23 / IFPA_L2 BH23
	TXD1 TXD1	TXD1 TXD1	IFPA_L1_N BF23 / IFPA_L1 BE23
	TXD2 TXD2	TXD2 TXD2	IFPA_L0_N BF24 / IFPA_L0 BG24
	SDA SCL		IFPB_AUX_SDA_N BG12 / IFPB_AUX_SCL BH12
	TXC TXC		IFPB_L3_N BL18 / IFPB_L3 BK18
	TXD3 TXD3	TXD0 TXD0	IFPB_L2_N BK20 / IFPB_L2 BL20
	TXD4 TXD4	TXD1 TXD1	IFPB_L1_N BM20 / IFPB_L1 BM21
	TXD5 TXD5	TXD2 TXD2	IFPB_L0_N BL21 / IFPB_L0 BK21

N17E-G1

PLACE NEAR GPU / PLACE UNDER GPU

+PEX_VDD
C7227 4.7UF/6.3V 0201 X5R/+/-10% @ GND
C7229 1uF/6.3V 0201 X5R/+/-10% @ GND
C7234 1uF/6.3V 0201 X5R/+/-10% @ GND
C7228 0.1UF/6.3V GND
C7226 0.1UF/6.3V GND

BB17 IFP_IOVDD_2
BB15 IFP_IOVDD_1
BB18 IFP_IOVDD_3
BB20 IFP_IOVDD_4

eDP

U7000R 8/23 IFPC

BD20 IFPCD_RSET
BD18 IFPCD_PLLVDD

	DVI/HDMI	DP
	SDA SCL	IFPC_AUX_SDA_N BL9 / IFPC_AUX_SCL BK9
	TXC TXC	IFPC_L3_N BF17 / IFPC_L3 BE17
	TXD0 TXD0	IFPC_L2_N BF18 / IFPC_L2 BG18
	TXD1 TXD1	IFPC_L1_N BG20 / IFPC_L1 BH20
	TXD2 TXD2	IFPC_L0_N BF20 / IFPC_L0 BE20

N17E-G1

PLACE NEAR GPU / PLACE UNDER GPU

+PEX_VDD
C7218 4.7UF/6.3V 0201 X5R/+/-10% @ GND
C7232 1uF/6.3V 0201 X5R/+/-10% @ GND
C7235 1uF/6.3V 0201 X5R/+/-10% @ GND
0.087A
C7219 0.1UF/6.3V @ GND

BB21 IFP_IOVDD_5
BB23 IFP_IOVDD_6

HDMI

U7000Q 9/23 IFPD

	DVI/HDMI	DP
	SDA SCL	IFPD_AUX_SDA_N BF11 / IFPD_AUX_SCL BE11
	TXC TXC	IFPD_L3_N BM14 / IFPD_L3 BM15
	TXD0 TXD0	IFPD_L2_N BL15 / IFPD_L2 BK15
	TXD1 TXD1	IFPD_L1_N BK17 / IFPD_L1 BL17
	TXD2 TXD2	IFPD_L0_N BM17 / IFPD_L0 BM18

N17E-G1

+PEX_VDD
0.118A
C7220 0.1UF/6.3V PLACE UNDER GPU GND

BC15 IFP_IOVDD_7
BC17 IFP_IOVDD_8

U7000P 10/23 IFPE

	DVI/HDMI	DP	
	SDA SCL	IFPE_AUX_SDA_N BL8 / IFPE_AUX_SCL BK8	HDMI_SDA_GPU 48 / HDMI_SCL_GPU 48
	TXC TXC	IFPE_L3_N BG14 / IFPE_L3 BH14	HDMI_CLKN 48 / HDMI_CLKP 48
	TXD0 TXD0	IFPE_L2_N BF14 / IFPE_L2 BE14	HDMI_TXN0 48 / HDMI_TXP0 48
	TXD1 TXD1	IFPE_L1_N BF15 / IFPE_L1 BG15	HDMI_TXN1 48 / HDMI_TXP1 48
	TXD2 TXD2	IFPE_L0_N BG17 / IFPE_L0 BH17	HDMI_TXN2 48 / HDMI_TXP2 48

N17E-G1

GND R72071 1% 2 1KOhm IFPCD_RSET BD17 IFPEF_RSET
+CORE_PLLVDD 1 SP7225 2 +IFPCD_PLLVDD BD15 IFPEF_PLLVDD
0.098A
C7217 0.1UF/6.3V PLACE UNDER GPU GND

+PEX_VDD
0.118A
C7222 4.7UF/6.3V N/A GND
C7233 1uF/6.3V 0201 X5R/+/-10% @ GND
C7236 1uF/6.3V 0201 X5R/+/-10% @ GND
C7223 0.1UF/6.3V N/A GND
PLACE UNDER GPU

BC18 IFP_IOVDD_9
BC20 IFP_IOVDD_10

Type-C DP

U7000O 6/23 IFPF

	DVI/HDMI	DP
	SDA SCL	IFPF_AUX_SDA_N BM9 / IFPF_AUX_SCL BM8
	TXC TXC	IFPF_L3_N BK11 / IFPF_L3 BL11
	TXD0 TXD0	IFPF_L2_N BM11 / IFPF_L2 BM12
	TXD1 TXD1	IFPF_L1_N BL12 / IFPF_L1 BK12
	TXD2 TXD2	IFPF_L0_N BK14 / IFPF_L0 BL14

N17E-G1

+PEX_VDD
0.118A BC21 IFP_IOVDD_11
BC23 IFP_IOVDD_12
C7224 0.1UF/6.3V PLACE UNDER GPU GND

+1V8_MAIN
L7201 1 2 300Ohm/100Mhz Irat=1A
+CORE_PLLVDD
C7237 22UF/6.3V GND
C7204 22UF/6.3V GND
SP7201 1 2
C7205 4.7UF/6.3V GND
PLACE NEAR GPU / PLACE UNDER GPU
C7202 0.1UF/6.3V GND
+SP_PLLVDD

+CORE_PLLVDD SP7203 1 2
C7206 0.1UF/6.3V GND
PLACE UNDER GPU
+VID_PLLVDD 0.28A BC12 VID_PLLVDD

+CORE_PLLVDD SP7202 1 2
C7225 0.1UF/6.3V
C7207 0.1UF/6.3V
C7208 0.1UF/6.3V
C7209 0.1UF/6.3V
GND
PLACE UNDER GPU
+GPCPLL_AVDD 0.14A U42 GPCPLL_AVDD0
AF11 GPCPLL_AVDD1
BB24 XS_PLLVDD

U7000S 14/23 XTAL/PLL
0.14A BD12 SP_PLLVDD
BC12 VID_PLLVDD
BJ6 XTAL_SSIN
BL6 XTAL_IN
XTAL_OUTBUFF BK6
XTAL_OUT BM6
N17E-G1

R7203 10KOhm GND
XTAL_27M_IN
C7210 8.2PF/50V GND
X7200 27MHZ 07T080020NAS
Sourcer request
GNDGND
XTAL_27M_OUT
C7211 8.2PF/50V GND
R7204 10KOhm GND

20171229-2
10pF --> 8.2pF for Xtal test

+1V8_MAIN 48,57,70,71,74,75,91
+PEX_VDD 57,70,96

Table 10.10 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFPA_IOVDD	1.0 V ± 5%	~118 mA
IFPB_IOVDD	1.0 V ± 5%	~118 mA
IFPC_IOVDD	1.0 V ± 5%	~118 mA
IFPD_IOVDD	1.0 V ± 5%	~118 mA
IFPE_IOVDD	1.0 V ± 5%	~118 mA
IFPF_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA

Table 10.1 Standard Configurations

Link	Description
GB4-256 Standard Mode	
Link AB	DVI (Dual Link)
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link with IFPF)
Link F	DisplayPort/eDP, DVI (Dual Link with IFPE)
GB4-256 Split Mode AB	
Link A	DisplayPort, HDMI, DVI (Single Link or Dual Link)
Link B	DisplayPort/eDP, DVI (Single Link or Dual Link)
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link EF	Not Connected
GB4-256 Split Mode EF	
Link AB	Not Connected
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link)
Link F	DisplayPort/eDP, DVI (Single Link or Dual Link)

1. Only four independent display heads supported.

Table 10.5 HDMI Power Rails

Power Rails	Voltage	Maximum Current Draw
IFPA_IOVDD	1.0 V ± 5%	~87 mA
IFPB_IOVDD	1.0 V ± 5%	~87 mA
IFPC_IOVDD	1.0 V ± 5%	~87 mA
IFPD_IOVDD	1.0 V ± 5%	~87 mA
IFPE_IOVDD	1.0 V ± 5%	~87 mA
IFPF_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 5%	~98 mA
IFPCD_PLLVDD	1.8 V ± 5%	~98 mA
IFPEF_PLLVDD	1.8 V ± 5%	~98 mA

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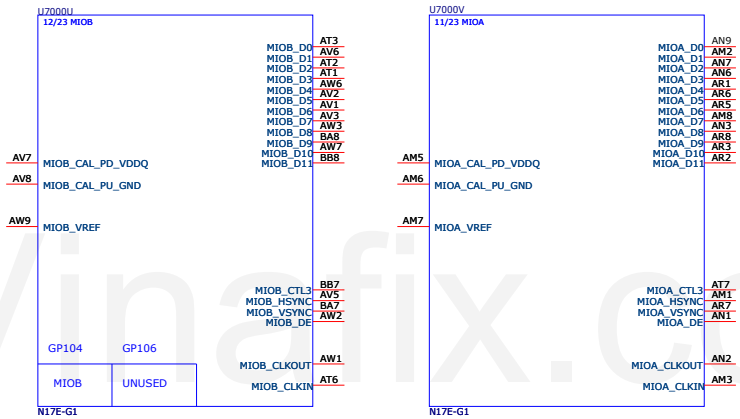
BG1-HW RD Div.2-HW RD Dept.3 Engineer: Hank_Zheng
Size C | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 Sheet 72 of 105

15.2.3 Unconnected Signals (NC)

The following guidelines apply to unused MIO interfaces:

- Power up all VDD18 pins.
- Leave MIO data pins and clock pins floating.



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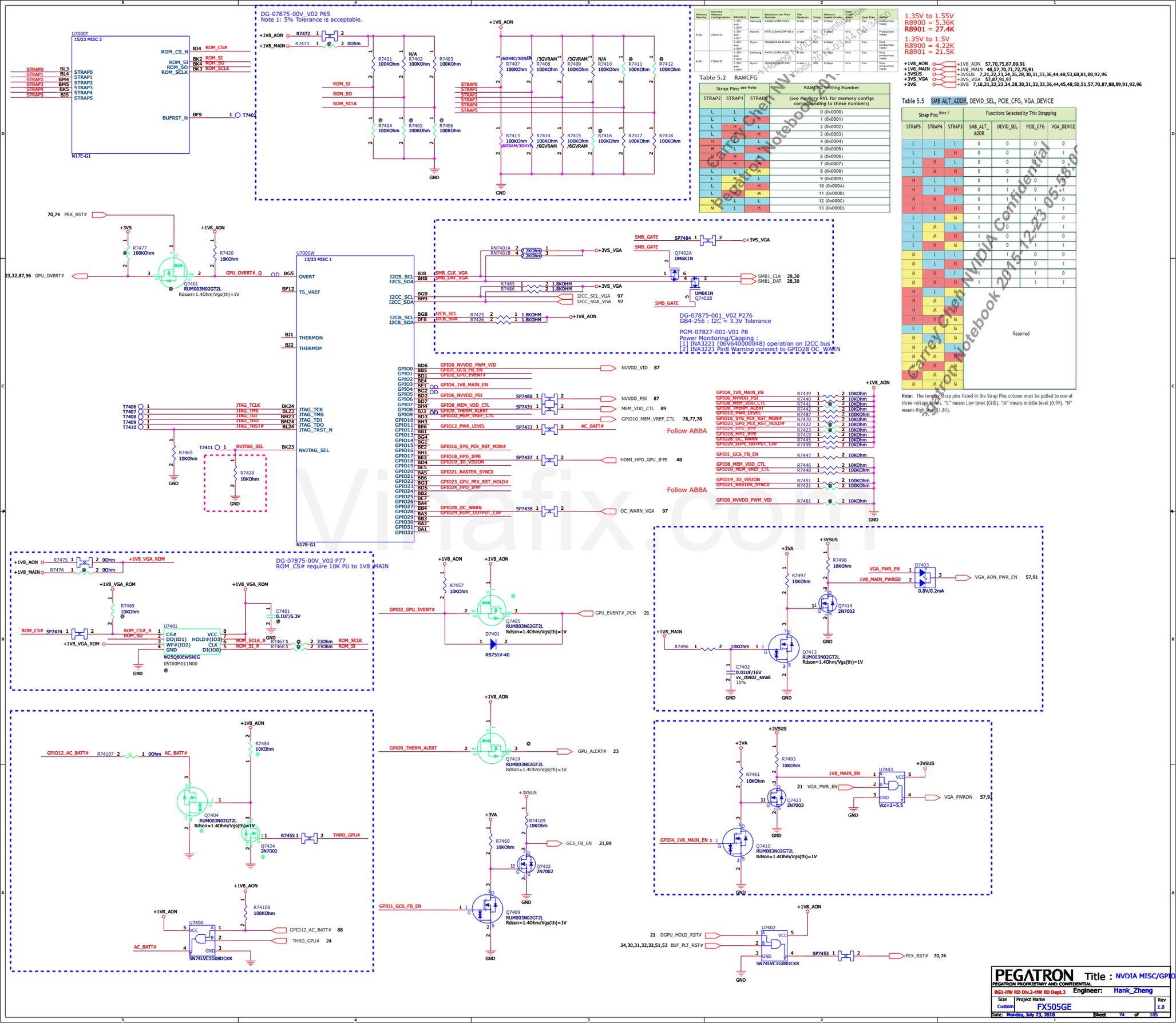
Title : NVDIA/Multi-use IO
BG1-HW RD Div.2-HW RD Dept.3
Engineer: Hank_Zheng
Size: C
Project Name: FX505GE
Rev: 1.0
Date: Monday, July 23, 2018
Sheet 73 of 105


DG-07875-00V_V02 P65
Note 1: 5% Tolerance is acceptable.
U7000T
15/23 MISC 2
N17E-G1
ROM_CS_N
ROM_SI
ROM_SO
ROM_SCLK
BUFRST_N
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5
+1V8_AON
+1V8_MAIN
R7401 100KOhm
R7402 100KOhm
R7403 100KOhm
R7404 100KOhm
R7405 100KOhm
R7406 100KOhm
R7407 100KOhm
R7408 100KOhm
R7409 100KOhm
R7410 100KOhm
R7411 100KOhm
R7412 100KOhm
R7413 100KOhm
R7414 100KOhm
R7415 100KOhm
R7416 100KOhm
R7417 100KOhm
R7418 100KOhm
GND
Table 5.2 RAMCFG
Strap Pins see Note
RAMCFG Setting Number
(see Memory RVL for memory configs corresponding to these numbers)
1.35V to 1.55V
R8900 = 5.36K
R8901 = 27.4K
1.35V to 1.5V
R8900 = 4.22K
R8901 = 21.5K
+1V8_AON 57,70,75,87,89,91
+1V8_MAIN 48,57,70,71,72,75,91
+3VSUS 7,21,22,23,24,26,28,30,31,33,36,44,48,53,68,81,88,92,96
+3VS_VGA 57,87,91,97
+3VS 7,16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,70,87,88,89,91,92,96
Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE
Strap Pins Note 1
Functions Selected by This Strapping
STRAP5
STRAP4
STRAP3
SMB_ALT_ADDR
DEVID_SEL
PCIE_CFG
VGA_DEVICE
Reserved
Note: The ternary strap pins listed in the Strap Pins column must be pulled to one of three voltage levels. "L" means Low level (GND). "H" means middle level (0.9V). "H" means High level (1.8V).
70,74 PEX_RST#
+3VS
+1V8_AON
R7477 100KOhm
R7420 10KOhm
Q7401 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
23,32,87,96 GPU_OVERT#
GPU_OVERT#_Q
U7000W
13/23 MISC 1
OVERT
TS_VREF
THERMDN
THERMDP
JTAG_TCLK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
NVJTAG_SEL
R7465 10KOhm
T7411
R7428 10KOhm
DG-07875-001_V02 P276
GB4-256 : I2C = 3.3V Tolerance
PGM-07827-001-V01 P8
Power Monitoring/Capping :
[1] INA3221 (06V640000048) operation on I2CC bus
[2] INA3221 Pin8 Warning connect to GPIO28 OC_WARN
SMB_GATE
SP7484
+3VS_VGA
Q7402A UM6K1N
Q7402B UM6K1N
SMB1_CLK 28,30
SMB1_DAT 28,30
I2CC_SCL_VGA 97
I2CC_SDA_VGA 97
I2CB_SCL
I2CB_SDA
R7485 1.8KOHM
R7486 1.8KOHM
R7425 1.8KOHM
R7426 1.8KOHM
GPIO0_NVVDD_PWM_VID
GPIO1_GC6_FB_EN
GPIO2_GPU_EVENT#
GPIO4_1V8_MAIN_EN
GPIO6_NVVDD_PSI
GPIO8_MEM_VDD_CTL
GPIO9_THERM_ALERT
GPIO10_MEM_VREF_CTL
GPIO12_PWR_LEVEL
GPIO16_SYS_PEX_RST_MON#
GPIO18_HPD_IFPE
GPIO19_3D_VISION
GPIO21_RASTER_SYNC0
GPIO23_GPU_PEX_RST_HOLD#
GPIO24_HPD_IFPF
GPIO28_OC_WARN
GPIO29_EDPC_OUTPUT_CAP
NVVDD_VID 87
NVVDD_PSI 87
MEM_VDD_CTL 89
GPIO10_MEM_VREF_CTL 76,77,78
AC_BATT# 76
HDMI_HPD_GPU_IFPE 48
OC_WARN_VGA 97
SP7488
SP7431
SP7433
SP7437
SP7438
Follow ABBA
Follow ABBA
R7439 10KOhm
R7440 10KOhm
R7441 10KOhm
R7442 10KOhm
R7487 10KOhm
R7470 10KOhm
R7422 10KOhm
R7423 10KOhm
R7419 10KOhm
R7445 10KOhm
R7499 10KOhm
R7447 10KOhm
R7446 10KOhm
R7448 10KOhm
R7451 10KOhm
R7421 10KOhm
R7481 10KOhm
DG-07875-00V_V02 P77
ROM_CS# require 10K PU to 1V8_MAIN
+1V8_VGA_ROM
R7475 0Ohm
R7476 0Ohm
R7469 10KOhm
C7401 0.1UF/6.3V
U7401
W25Q80EWSNIG
0ST00M011N00
R7471 330Ohm
R7468 330Ohm
R7457 10KOhm
Q7405 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
GPIO2_GPU_EVENT#
GPU_EVENT#_PCH 21
D7401 RB751V-40
+3VSUS
+3VA
R7498 10KOhm
R7497 10KOhm
VGA_PWR_EN
1V8_MAIN_PWRGD
D7403 0.8V/0.2mA
VGA_AON_PWR_EN 57,91
Q7414 2N7002
R7496 10KOhm
Q7413 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
C7402 0.01UF/16V vx_c0402_small 10%
R7454 10KOhm
GPIO12_AC_BATT#
R74107 0Ohm
Q7404 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
Q7424 2N7002
R7455 1
THRO_GPU#
R74108 100KOhm
U7404
SN74LVC1G08DCKR
GPIO12_AC_BATT# 88
THRO_GPU# 24
GPIO9_THERM_ALERT
Q7419 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
GPU_ALERT# 23
R74109 10KOhm
R7460 10KOhm
GC6_FB_EN 21,89
Q7422 2N7002
GPIO1_GC6_FB_EN
Q7409 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
R7493 10KOhm
R7461 10KOhm
VGA_PWR_EN 21
Q7423 2N7002
U7403
Vcc=2~5.5
VGA_PWRON 57,91
1V8_MAIN_EN
GPIO4_1V8_MAIN_EN 1
Q7410 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V
DGPU_HOLD_RST# 21
BUF_PLT_RST# 24,30,31,32,33,51,53
U7402
SN74LVC1G08DCKR
SP7453
PEX_RST# 70,74
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : NVDIA MISC/GPIO
BG1-HW RD Div.2-HW RD Dept.3
Engineer: Hank_Zheng
Size: Custom
Project Name: FX505GE
Rev: 1.0
Date: Monday, July 23, 2018
Sheet 74 of 105
Carrey Chen NVIDIA Confidential
Pegatron Notebook 2015-12-23 05:38:0
Vinafix.com

MEMORY : FBC Partition 31:0 (Mirror)
MEMORY : FBC Partition 63:32 (Normal)

+FBVDDQ 57,71,75,76,77,89

U7800A / U7800B / U7801A / U7801B — H5GC4H24MFR-T2C 03T150000077

MF =1 (PU) : Mirror
MF =0 (PD) : Normal

U7800C / U7800D / U7801C / U7801D — H5GC4H24MFR-T2C 03T150000077

PLACE NEAR DRAM

PLACE UNDER DRAM

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Title : GDDR5 256M X32bit_C

BG1-HW RD Div.2-HW RD Dept.3 Engineer: Hank_Zheng

Size: Custom | Project Name: FX505GE | Rev: 1.0

Date: Monday, July 23, 2018 | Sheet 78 of 105

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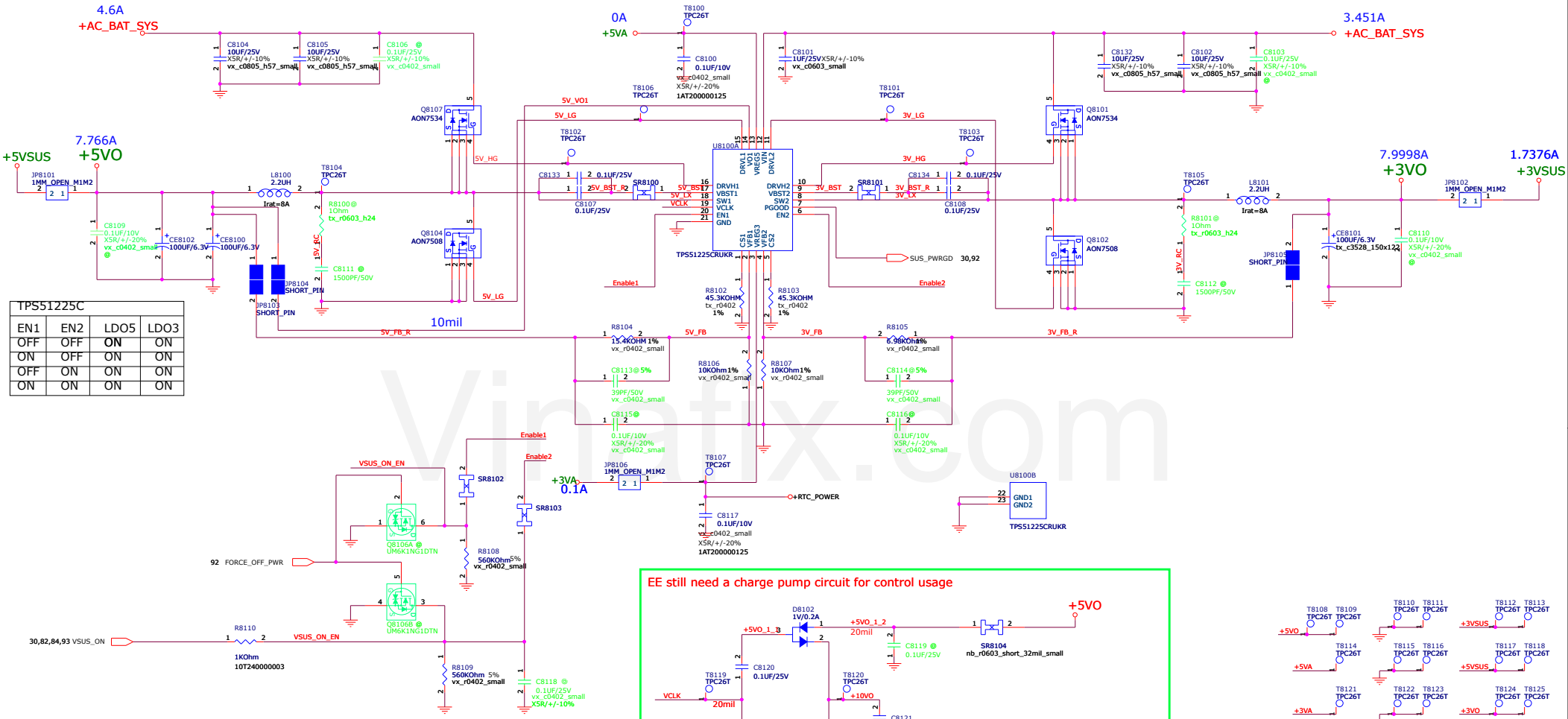
Title : SDDR5 256M X32bit_D

BG1-HW RD Div.2-HW RD Dept.3 Engineer: Hank_Zheng

Size	Project Name	Rev
C	FX505GE	1.0

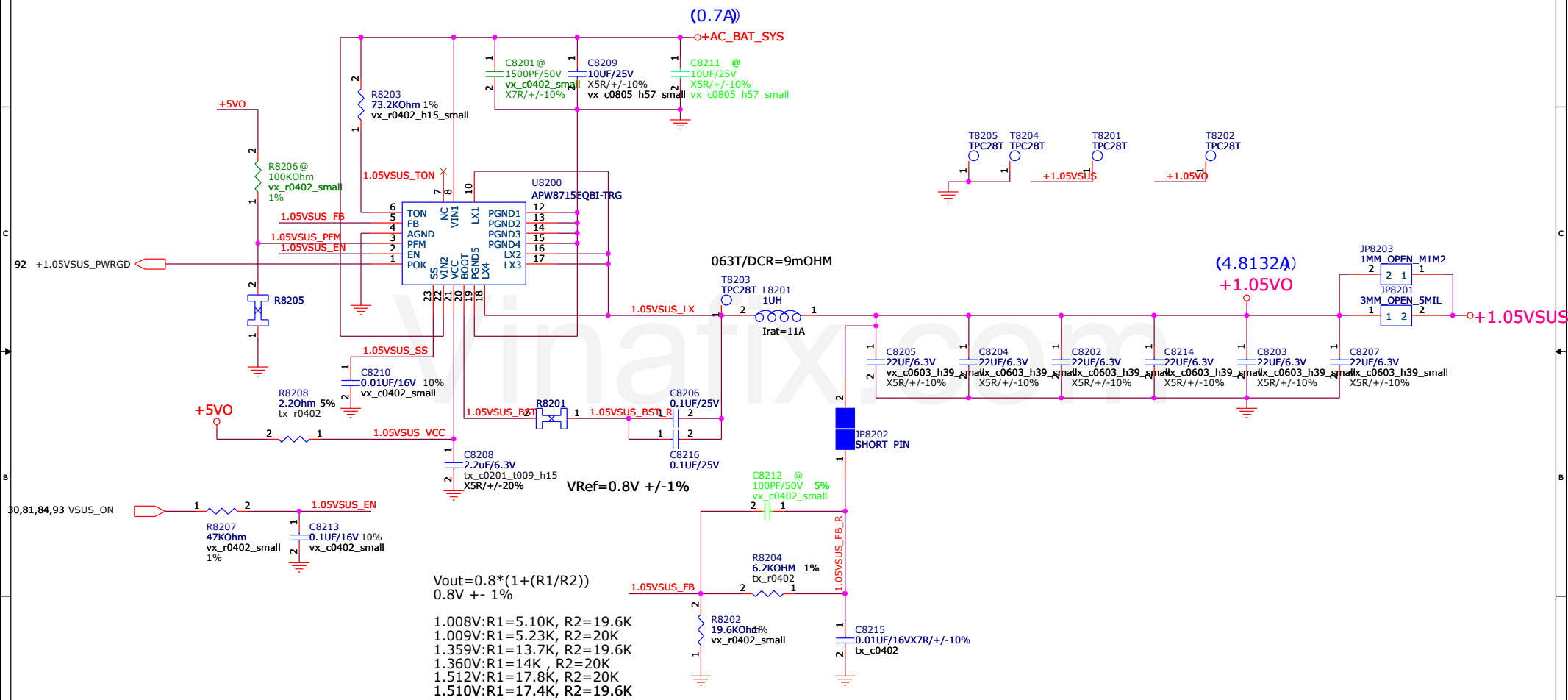
Date: Monday, July 23, 2018 Sheet 79 of 105

+5VO & +3VO POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.
Title : SYSTEM
Engineer: Steven Kuo
Size: Custom
Project Name: G15G
Rev:
Date: Monday, July 23, 2018
Sheet 81 of 108

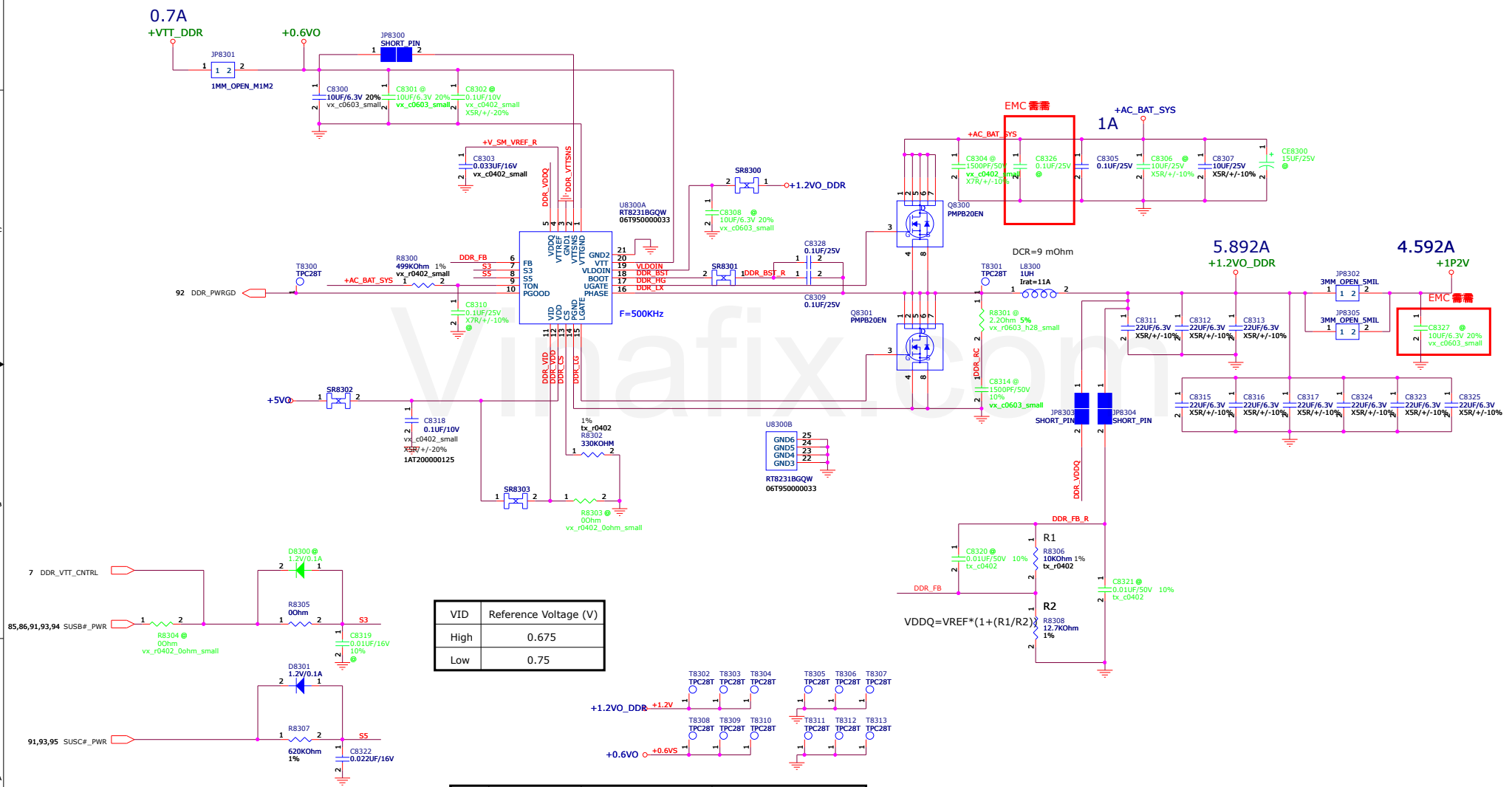
1.0VO POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +1.0VSUS
Engineer: Steven Kuo
Size: B | Project Name: G15G | Rev: A00
Date: Monday, July 23, 2018 | Sheet 82 of 108

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

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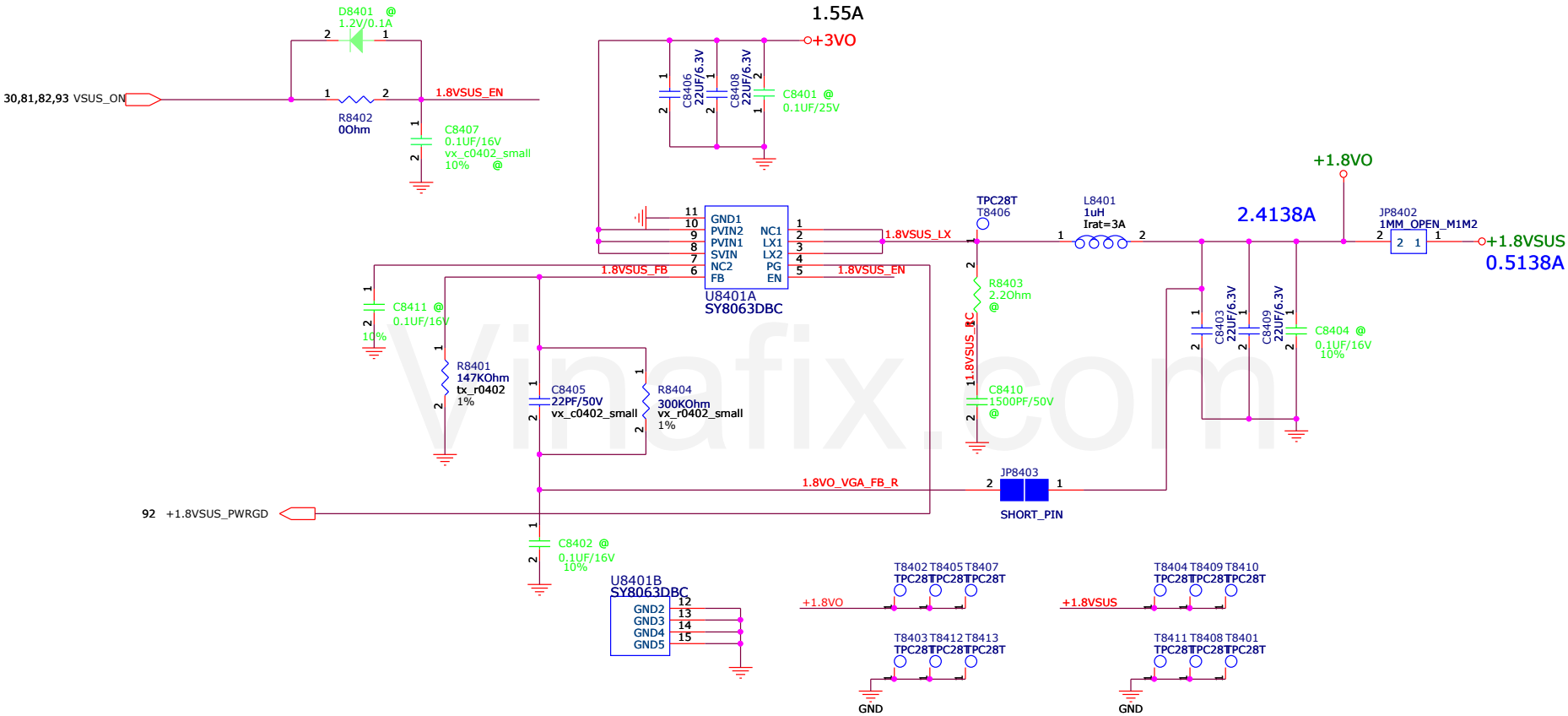
Title : +1P2V
Engineer: Steven Kuo
Size: Custom | Project Name: G15G | Rev: 1.0
Date: Monday, July 23, 2018 | Sheet 83 of 108

1.8VSUS POWER SUPPLY



PEGATRON
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Pegatron Corp.

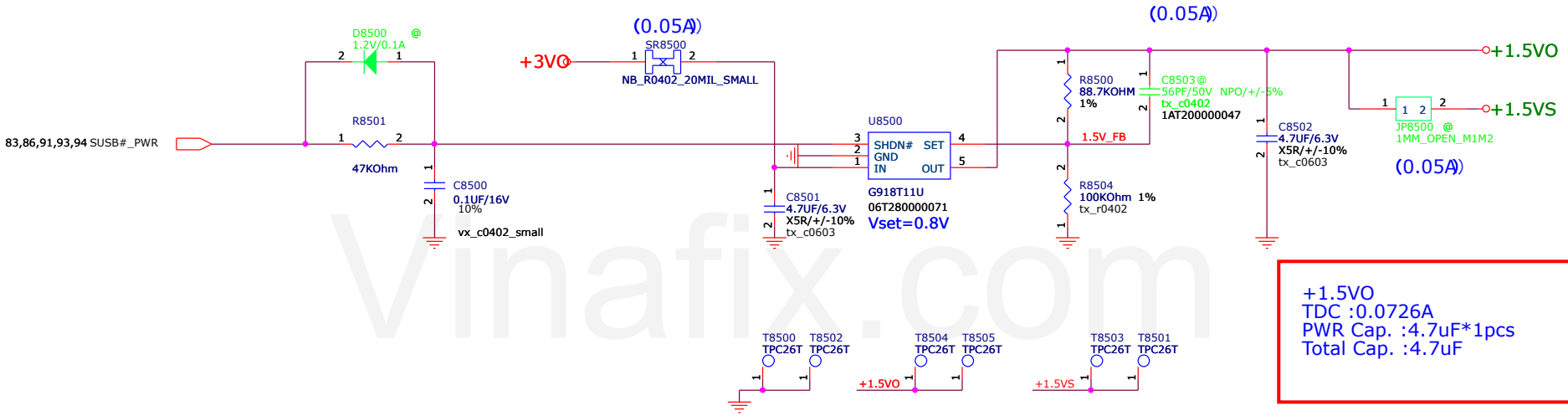
Title : +1V8SUS

Engineer: Steven Kuo

Size	Project Name	Rev
B	G15G	A00

Date: Monday, July 23, 2018 Sheet 84 of 108

1.5VS POWER SUPPLY



+1.5VO
TDC :0.0726A
PWR Cap. :4.7uF*1pcs
Total Cap. :4.7uF

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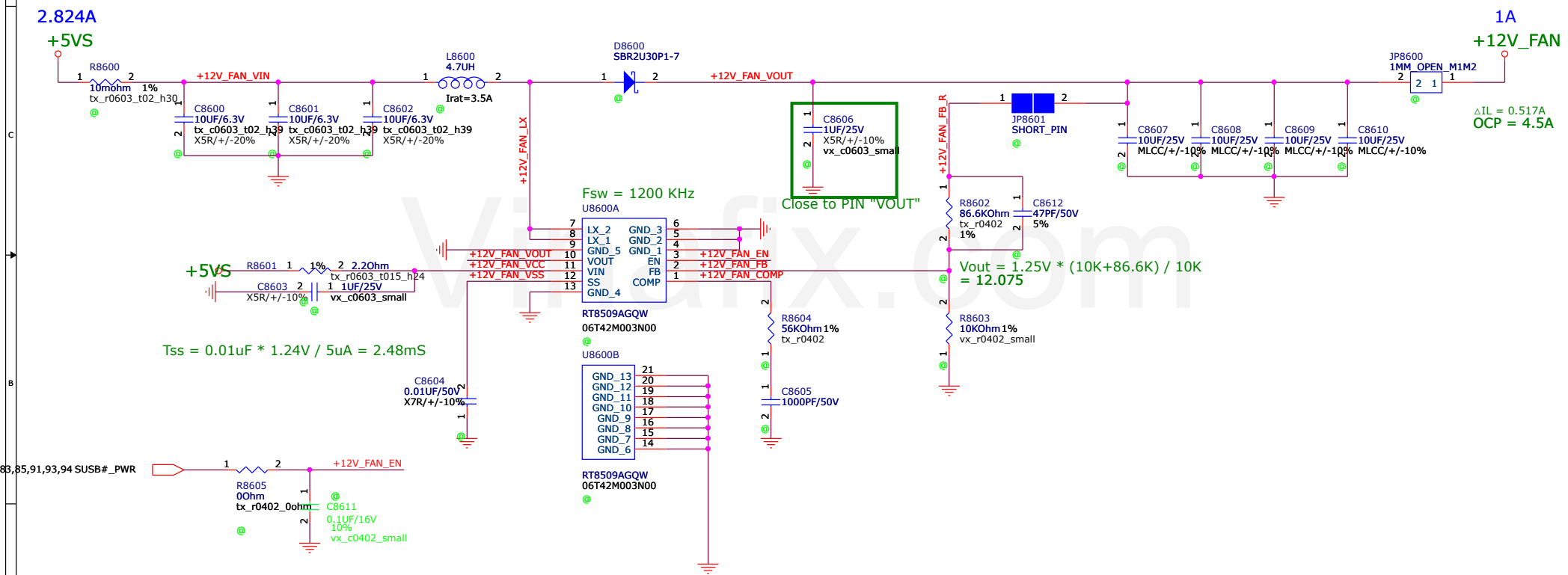
Title : *****
Engineer: Steven Kuo
Size: B | Project Name: G15G | Rev: 1.0
Date: Monday, July 23, 2018 | Sheet 85 of 108

12V_FAN POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +1V8_AON

Engineer: Steven Kuo

Size	Project Name	Rev
B	G15G	1.0

Date: Monday, July 23, 2018 Sheet 86 of 108

+NVVDD POWER SUPPLY

R8700	6.19K
R8701	20.5K
R8702	4.32K
R8704	16.5K
R8705	309
C8700	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

	PSI Voltage Setting Operation Phase Number
1phase with DEM	0V to 0.4V
1phase with CCM	0.8V to 1V
2 or 3 phase with CCM	1.4V to 5.5V

Phase 1

Phase 2

Phase 3

VGA Input current=9A

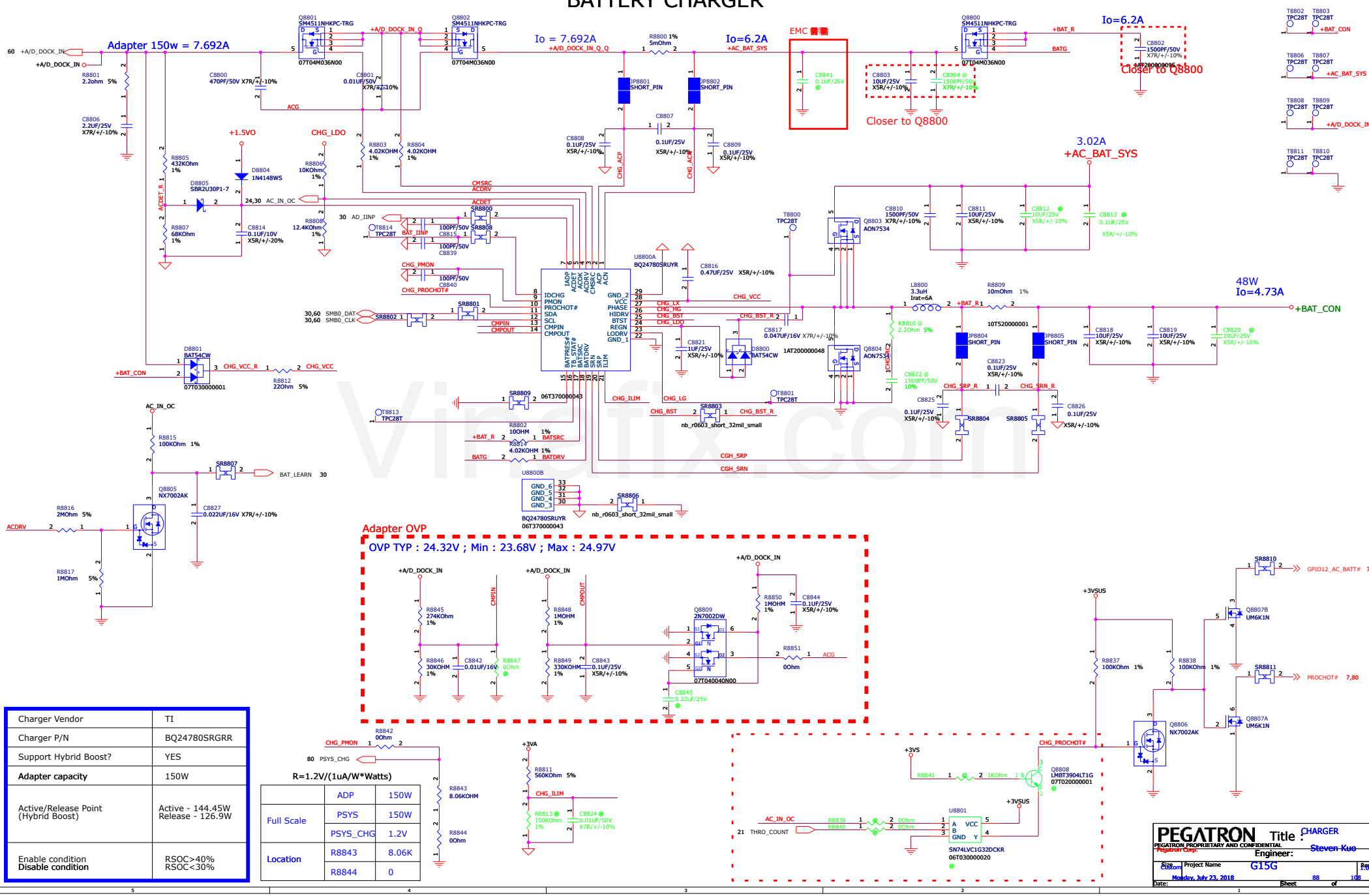
+AC_BAT_SYS_NVVDD

+NVVDD

EDP=127A
OCP:169A
TDC=78A

PEGATRON Title : +NVVDD
PEGATRON CONFIDENTIAL AND PROPRIETARY
Engineer: Steven Kuo
Size: Project Name: G15G Rev:
Date: Monday, July 23, 2018 Sheet: 87 of 100

BATTERY CHARGER



Charger Vendor	TI	
Charger P/N	BQ24780SRGRR	
Support Hybrid Boost?	YES	
Adapter capacity	150W	
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W	
Enable condition **Disable condition**	RSOC>40% RSOC<30%	

Full Scale	ADP	150W
	PSYS	150W
	PSYS_CHG	1.2V
Location	R8843	8.06K
	R8844	0

PEGATRON Title : CHARGER
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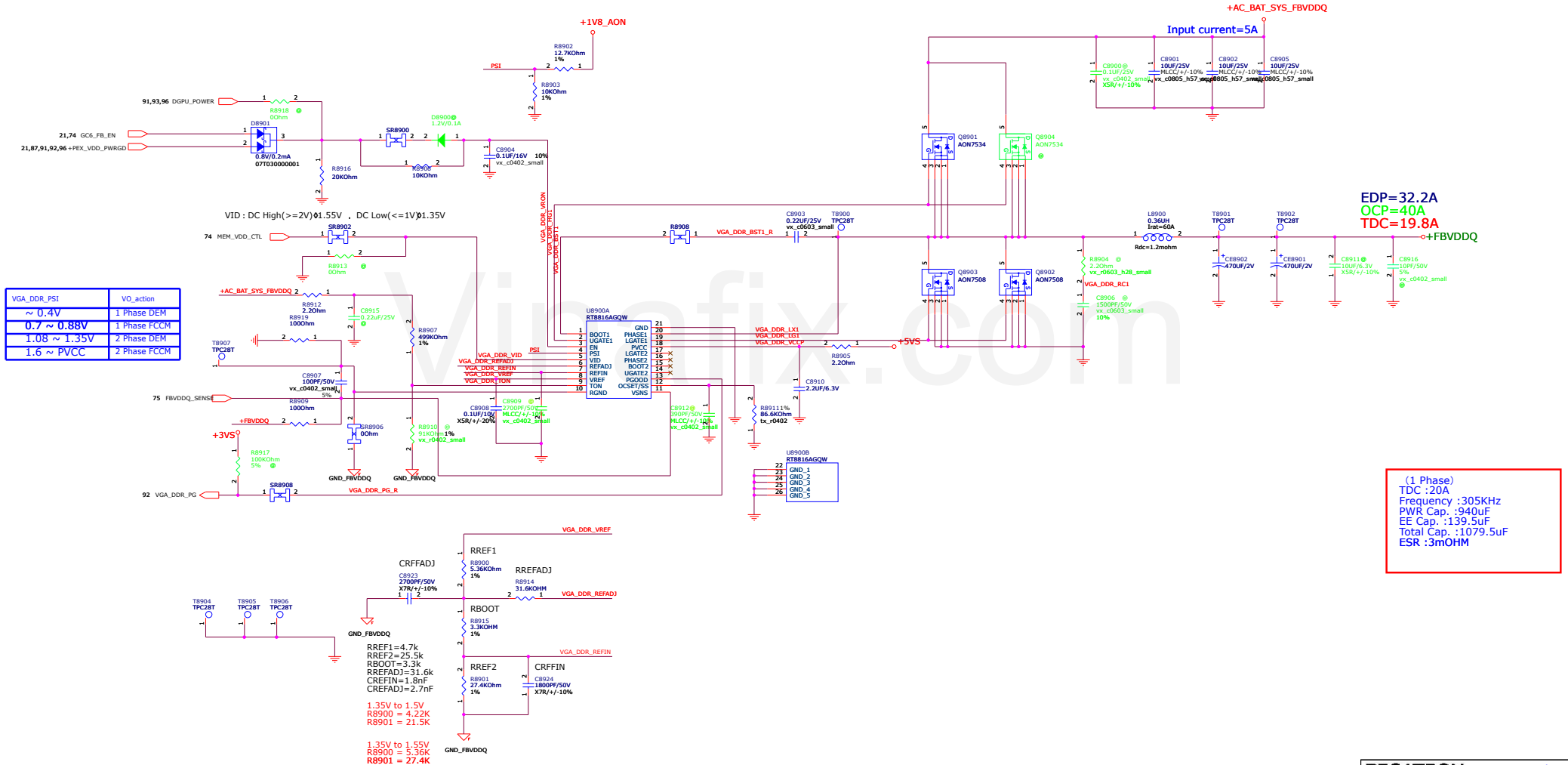
Pegatron Corp. Engineer: Steven Kuo
Size: Custom | Project Name: G15G | Rev: 1.0
Date: Monday, July 23, 2018 | Sheet: 88 of 108

+FBVDDQ POWER SUPPLY



PEGATRON Title : +FBVDDQ
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Steven Kuo
Size: Project Name: G15G Rev: 1A0
Date: Monday, July 23, 2018 Sheet 89 of 108

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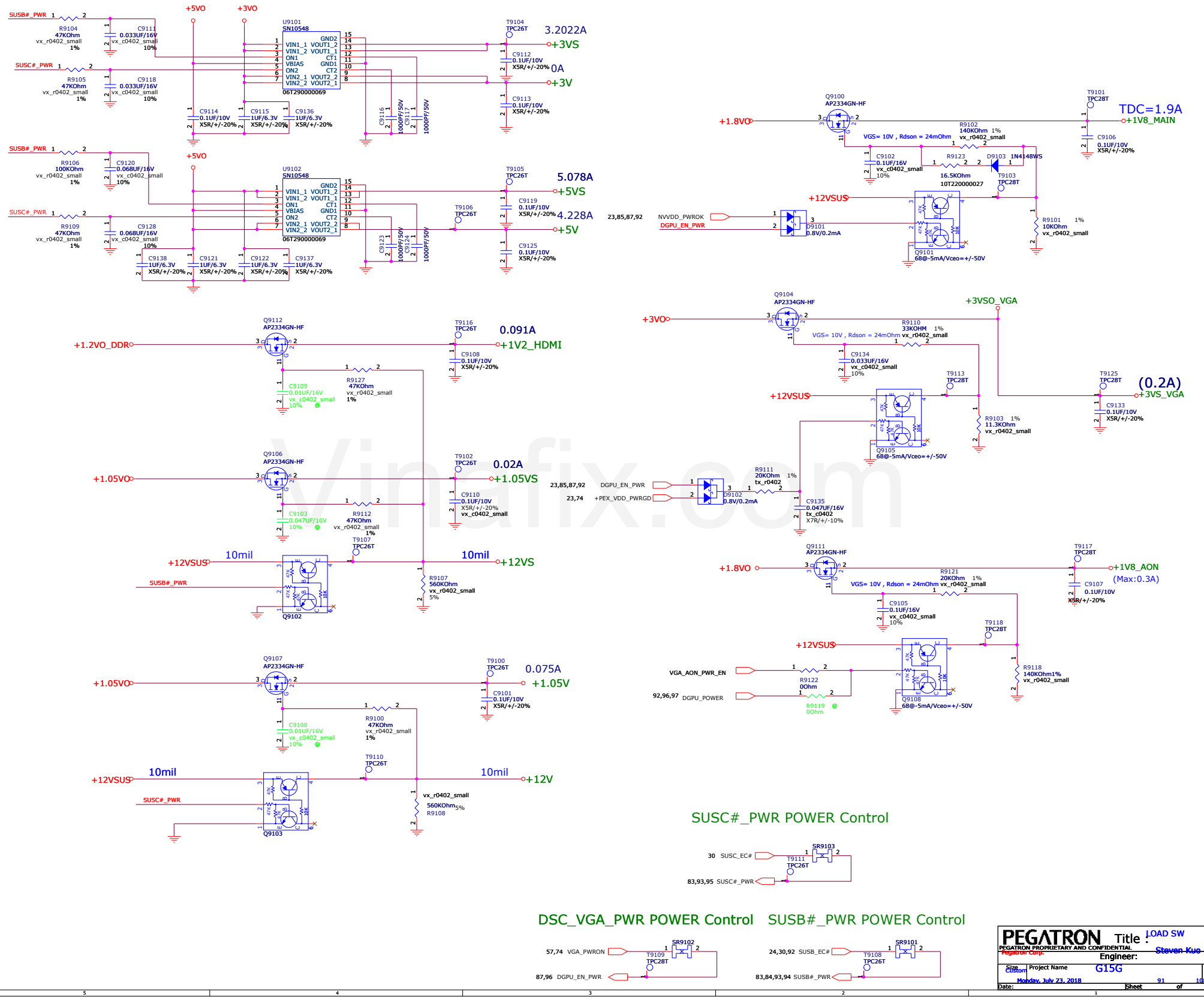
Pegatron Corp.

Title : DETECT

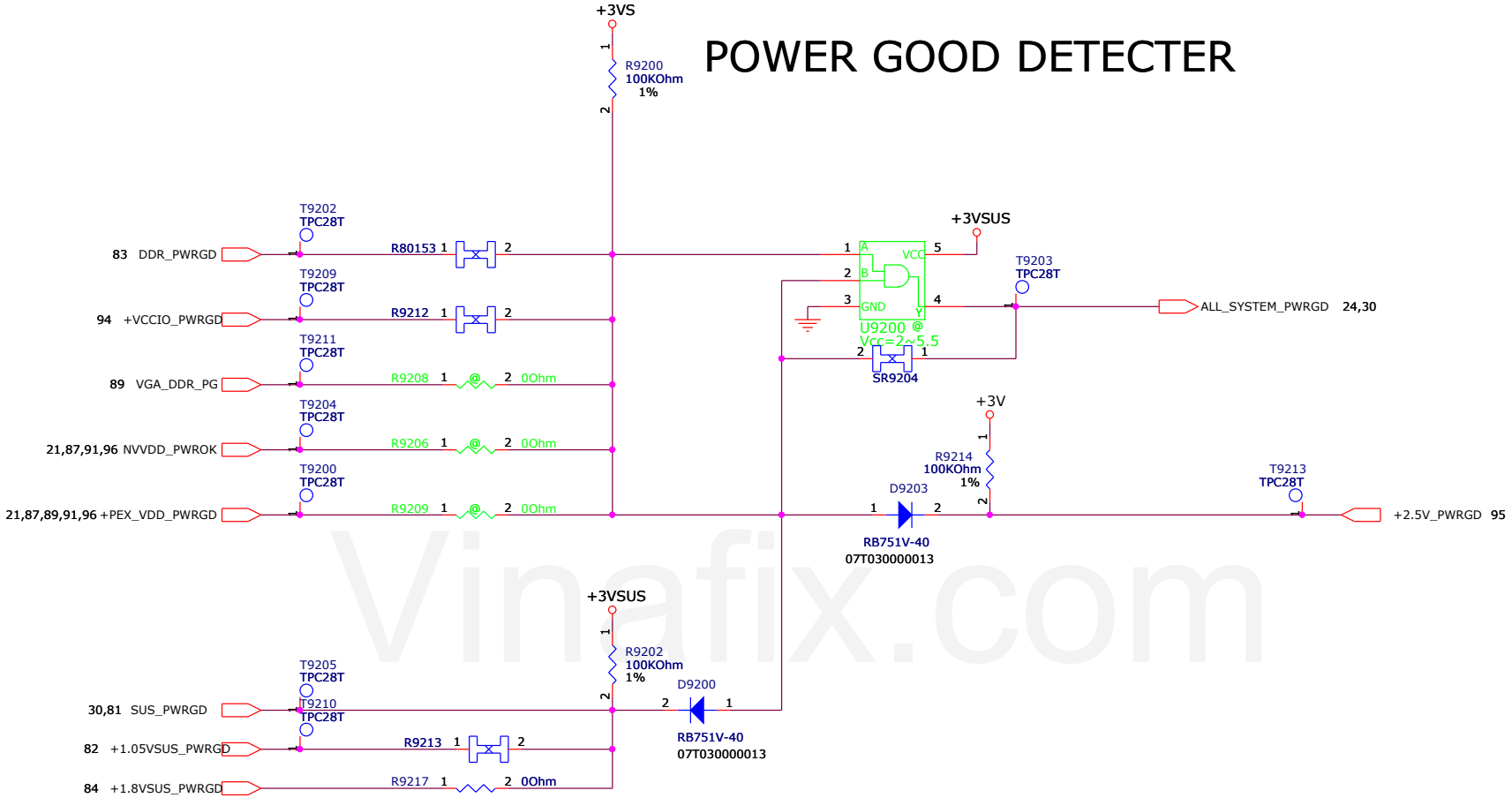
Engineer: Steven Kuo

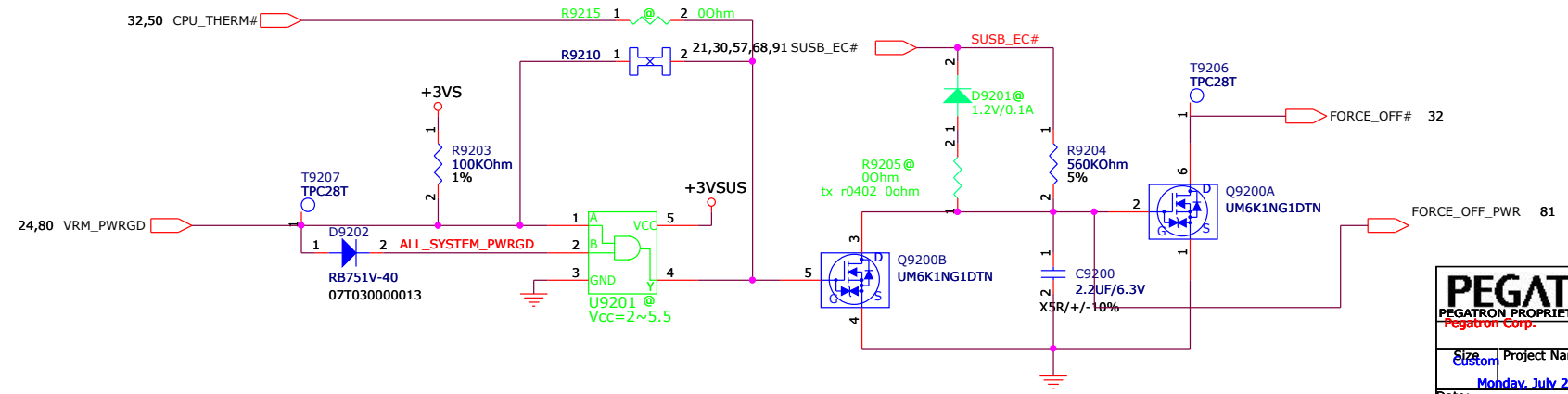
Size: Custom | Project Name: G15G | Rev: 1.0

Date: Monday, July 23, 2018 | Sheet 90 of 108


SUSB#_PWR POWER
SUSC#_PWR POWER
SUSB#_PWR
SUSC#_PWR
+5VO
+3VO
U9101
SN10548
06T290000069
T9104
TPC26T
3.2022A
+3VS
0A
+3V
U9102
T9105
5.078A
+5VS
4.228A
+5V
T9106
+1.8VO
Q9100
AP2334GN-HF
T9101
TPC28T
TDC=1.9A
+1V8_MAIN
VGS= 10V , Rdson = 24mOhm
+12VSUS
NVVDD_PWROK
DGPU_EN_PWR
D9101
0.8V/0.2mA
Q9101
68@-5mA/Vceo=+/-50V
+1.2VO_DDR
Q9112
T9116
0.091A
+1V2_HDMI
+1.05VO
Q9106
T9102
0.02A
+1.05VS
10mil
+12VS
Q9102
Q9107
T9100
0.075A
+1.05V
+12V
Q9103
+3VO
Q9104
+3VSO_VGA
T9113
T9125
(0.2A)
+3VS_VGA
Q9105
DGPU_EN_PWR
+PEX_VDD_PWRGD
D9102
+1.8VO
Q9111
T9117
+1V8_AON
(Max:0.3A)
Q9108
VGA_AON_PWR_EN
DGPU_POWER
T9118
SUSC#_PWR POWER Control
SR9103
T9111
SUSC_EC#
DSC_VGA_PWR POWER Control
VGA_PWRON
DGPU_EN_PWR
SR9102
T9109
SUSB#_PWR POWER Control
SUSB_EC#
SR9101
T9108
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.
Title : LOAD SW
Engineer: Steven Kuo
Size: Custom
Project Name: G15G
Rev: 1.0
Date: Monday, July 23, 2018
Sheet 91 of 108

POWER GOOD DETECTER





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : DETECTER
Engineer: Steven Kuo

Size	Project Name	Rev
Custom	G15G	1.0
Date: Monday, July 23, 2018	Sheet 92 of 108	

+A/D_DOCK_IN → +A/D_DOCK_IN 60,88

+BAT_CON → +BAT_CON 60,88

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,88,94,97

+12VSUS → +12VSUS 81,91

+3VO → +3VO 81,84,85,91,95

+3VSUS → +3VSUS 7,21,22,23,24,26,28,30,31,33,36,44,48,53,68,74,81,88,92,96

+3V → +3V 24,57,68,91,92

+3VS → +3VS 7,16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,70,74,87,88,89,91,92,96

+3VS_VGA → +3VS_VGA 57,74,87,91,97

+3VA → +3VA 25,30,57,66,74,81,88

+5VO → +5VO 81,82,83,91,94,95,96

+5VSUS → +5VSUS 31,56,81

+5V → +5V 7,52,57,91

+5VS → +5VS 36,48,50,51,56,57,80,86,87,89,91

+1.05VO → +1.05VO 82,91

+1.05VSUS → +1.05VSUS 26,82

+1.05V → +1.05V 7,10,24,32,57,80,91

+1.05VS → +1.05VS 7,10,57,91

+1.2VO_DDR → +1.2VO_DDR 83,91,96

+1P2V → +1P2V 7,10,16,17,18,24,57,83

+0.6VO → +0.6VO 83

+VTT_DDR → +VTT_DDR 16,17,18,57,83

+1.8VO → +1.8VO 84,91

+1.8VSUS → +1.8VSUS 21,26,53,84

+1V8_MAIN → +1V8_MAIN 48,57,70,71,72,74,75,91

+1V8_AON → +1V8_AON 57,70,74,75,87,89,91

+0.95VO → +0.95VO 94

+VCCIO → +VCCIO 3,6,7,10,94

+2.5VO → +2.5VO 95

+2P5VPP → +2P5VPP 16,17,18,57,95

+PEX_VDD → +PEX_VDD 57,70,72,96

+NVVDD → +NVVDD 57,75,87

+FBVDDQ → +FBVDDQ 57,71,75,76,77,78,89

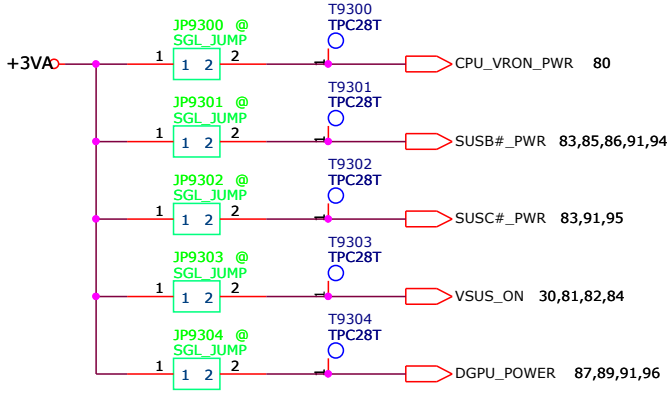
+NVVDDS → +NVVDDS

+VCORE → +VCORE 9,80

+VCCGT → +VCCGT 9,80

+VCCSA → +VCCSA 10,80

FOR POWER TEST

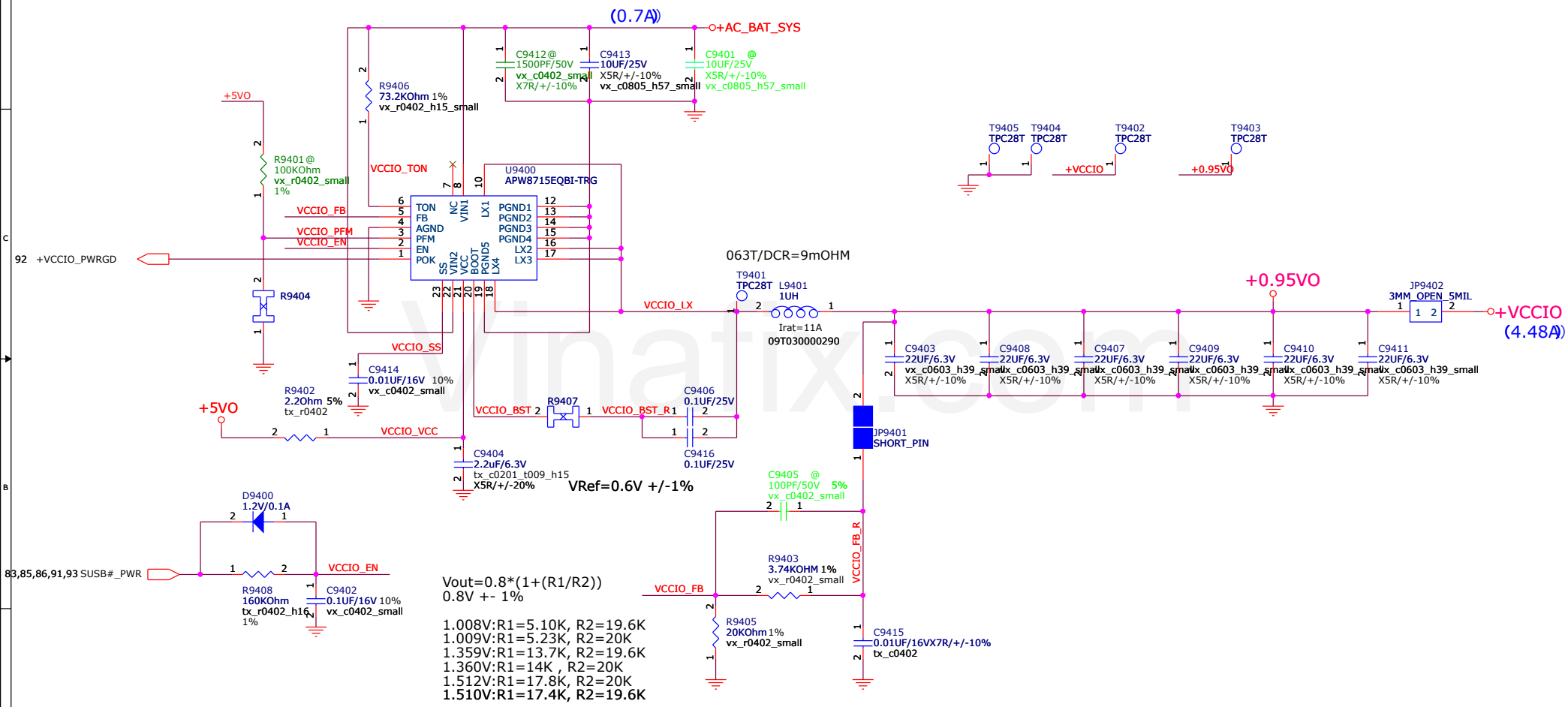


PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : Signal
Engineer: Steven Kuo

Size	Project Name	Rev
Custom	G15G	1.0
Date: Monday, July 23, 2018	Sheet 93 of 108	

+VCCIO POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

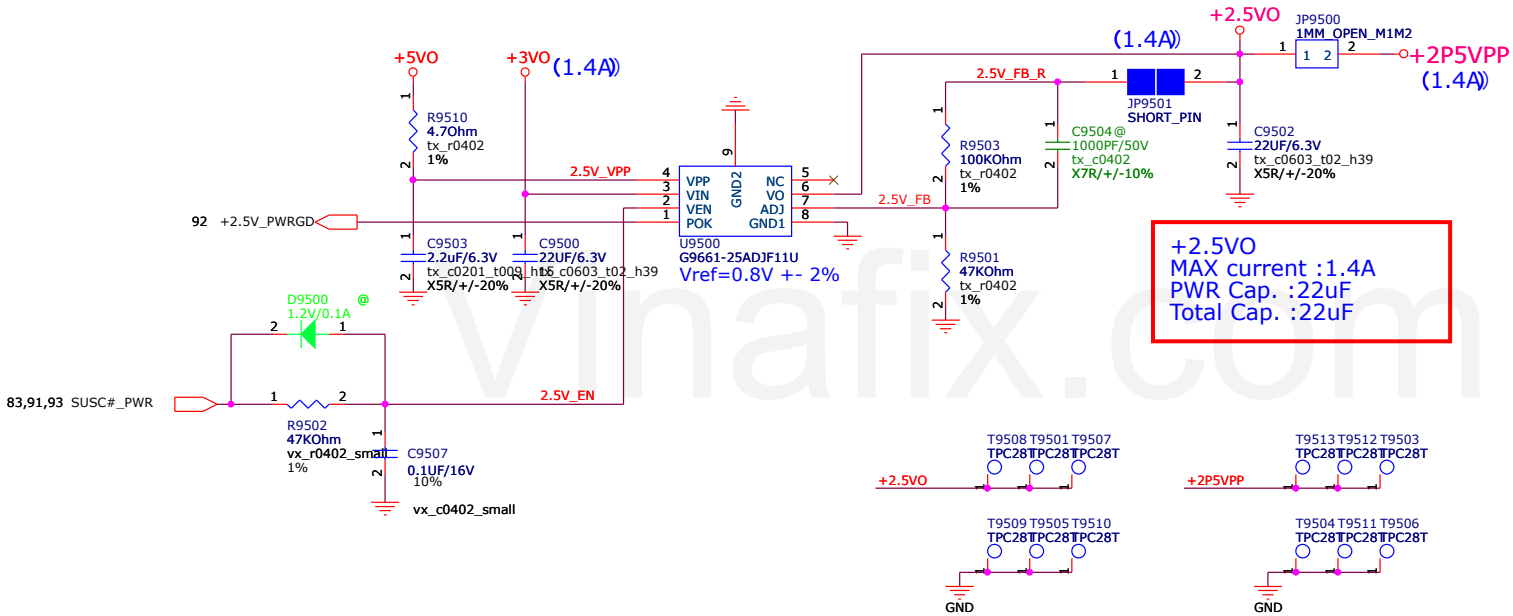
Title : +VCCIO

Engineer: Steven Kuo

Size	Project Name	Rev
B	G15G	1.0

Date: Monday, July 23, 2018 Sheet 94 of 108

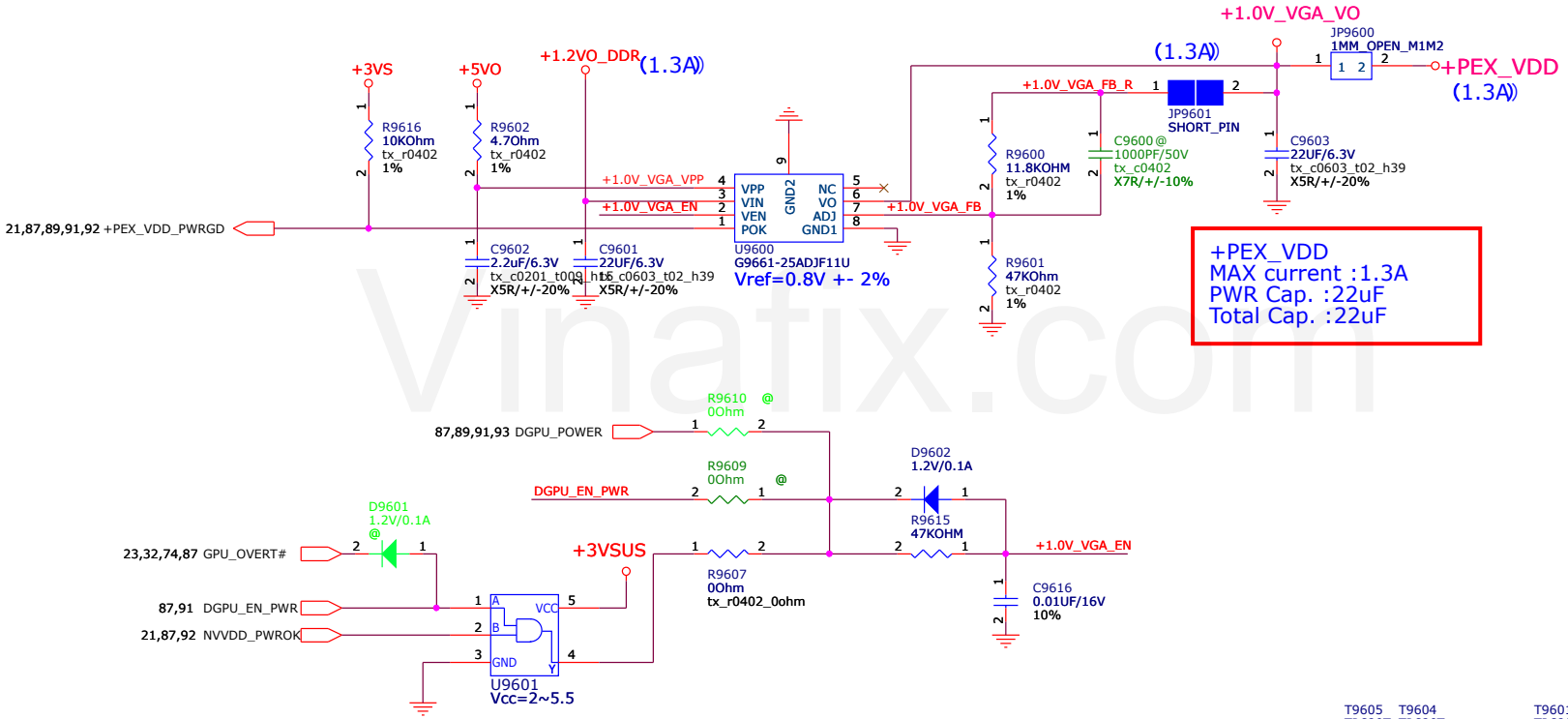
+2.5V POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +2P5VPP
Engineer: Steven Kuo
Size: B | Project Name: G15G | Rev: 1.0
Date: Monday, July 23, 2018 | Sheet 95 of 108

+PEX_VDD POWER SUPPLY



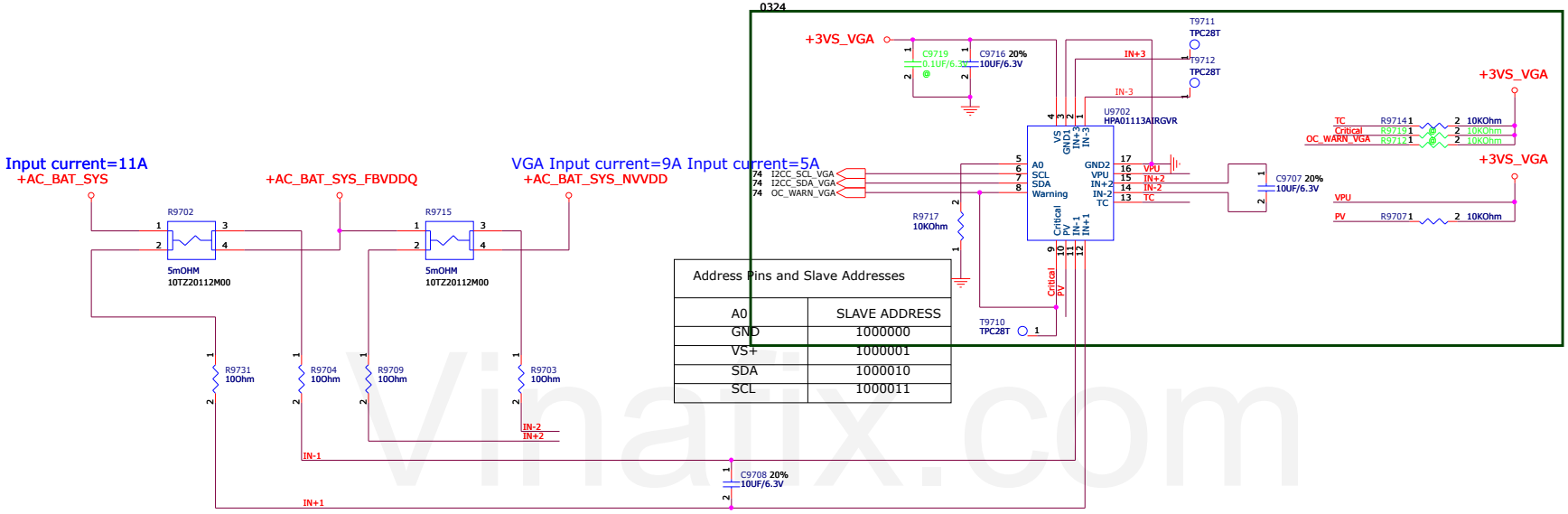
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +PEX_VDD

Engineer: Steven Kuo

Size	Project Name	Rev
B	G15G	1.0

Date: Monday, July 23, 2018 Sheet 96 of 108



Address Pins and Slave Addresses	
A0	SLAVE ADDRESS
GND	1000000
VS+	1000001
SDA	1000010
SCL	1000011

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +NVVDDS

Engineer: Steven Kuo

Size	Project Name	Rev
C	G15G	A00

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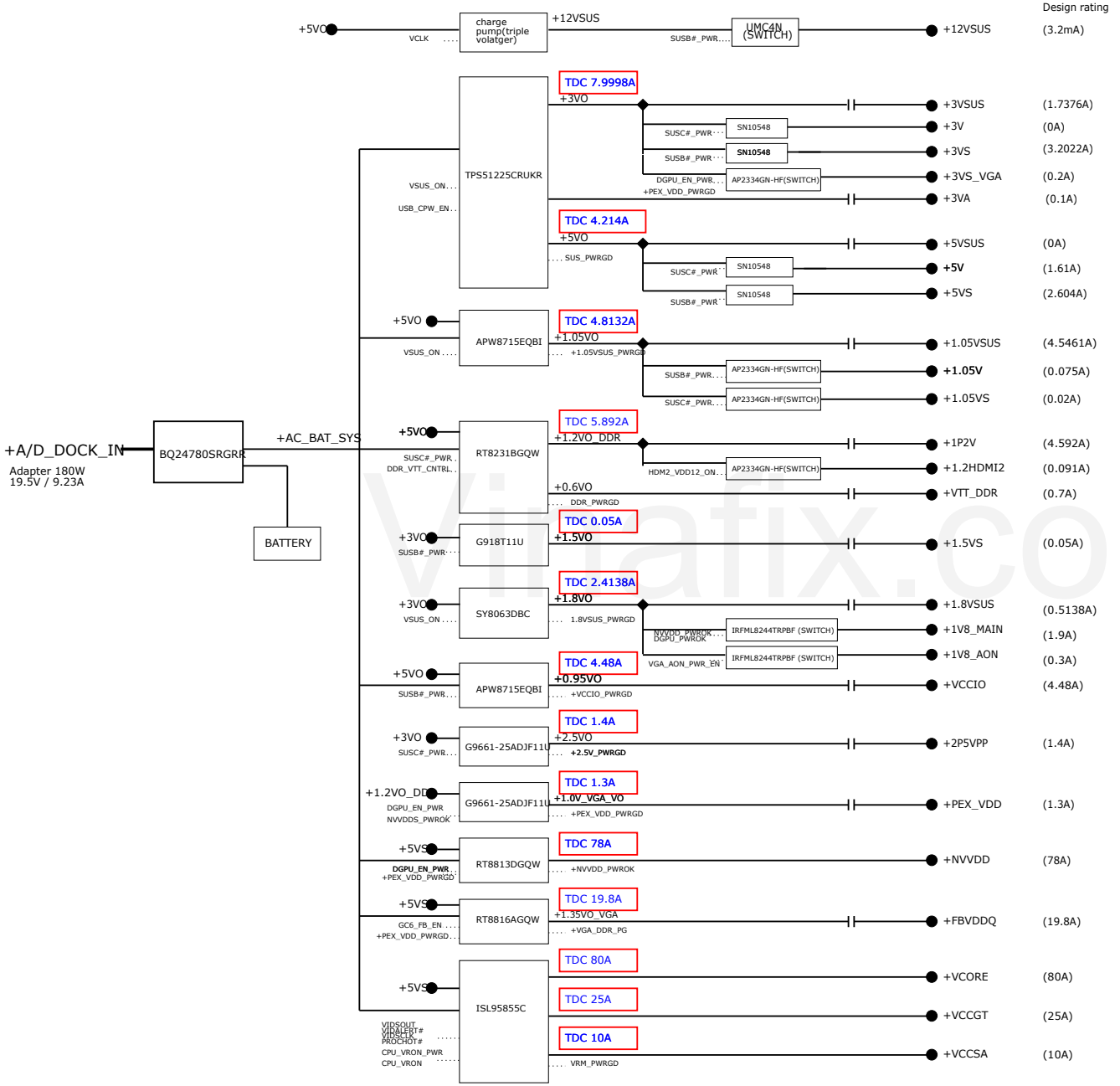
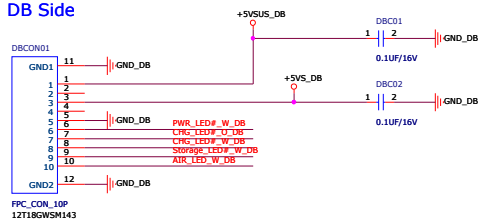


PEGATRON Title : POWER_TREE
PEGATRON CORP. Engineer: Steven Kuo
Size Project Name G15G Rev
Monday, July 23, 2018 Sheet of

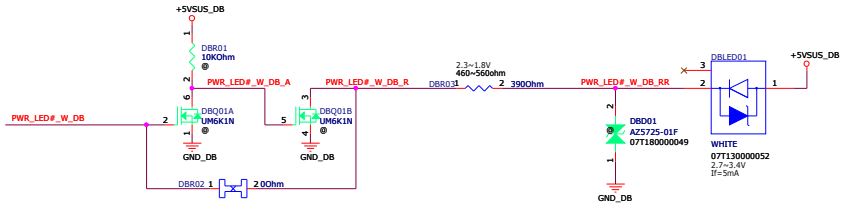
DB Side



+5VSUS +5VSUS 31,56,81

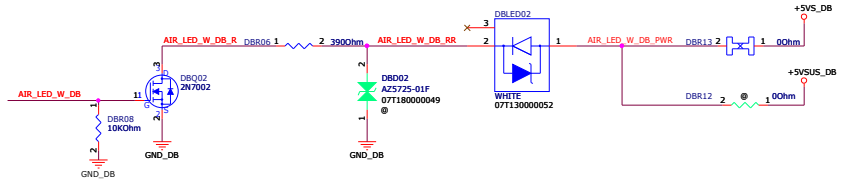
+5VS +5VS 36,48,50,51,56,57,80,86,87,89,91

Power LED

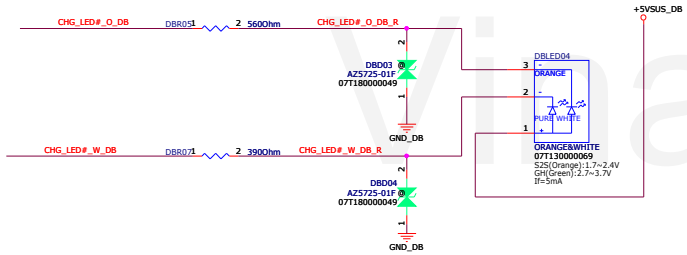


AIR PLANE LED(White)

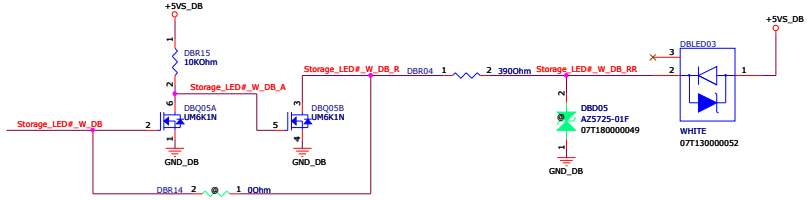
NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF



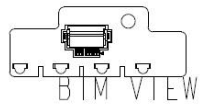
Charger LED(White/Orange)



HDD LED



PCB/ID LOCATION



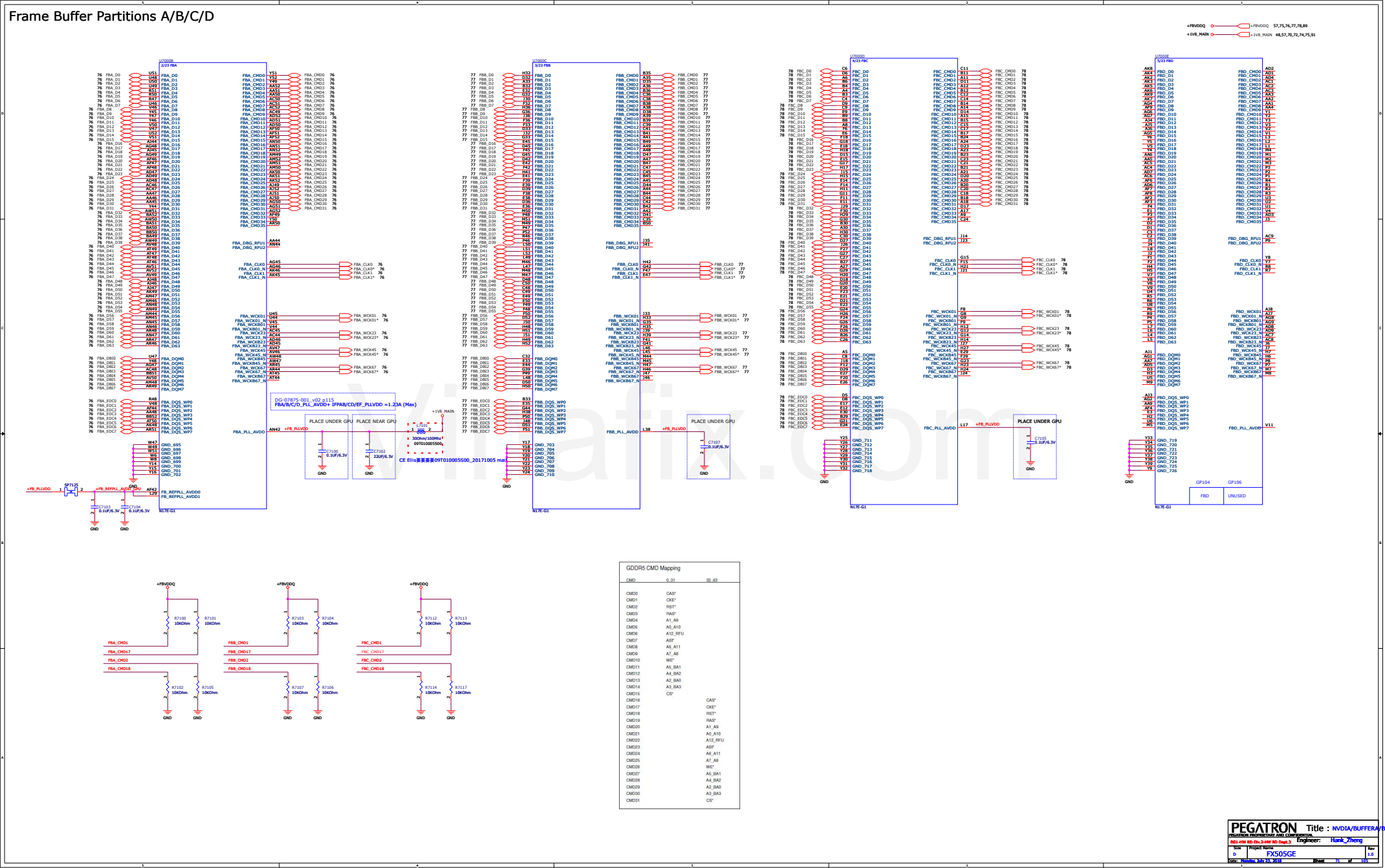
PWR LED DBLED01 | Charger LED DBLED04 | HDD LED DBLED03 | RF LED DBLED02

Tooling Hole

DBH01 HOLE_NPTH

PEGATRON Title : LED
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN
Size A2 | Project Name FX505GE | Rev 1.0
Date: Monday, July 23, 2018 | Sheet 99 of 99

Frame Buffer Partitions A/B/C/D



PEGATRON Title : NVDIA/BUFFER/A/B/C/D
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Hank_Zheng
Size: D | Project Name: FX505GE | Rev: 1.0
Date: Monday, July 23, 2018 | Sheet 71 of 105

MEMORY : FBA Partition 31:0 (Mirror)
MEMORY : FBA Partition 63:32 (Normal)

+FBVDDQ 57,71,75,77,78,89

U7600A U7600B U7601A U7601B

U7600C U7600D U7601C U7601D

H5GC4H24MFR-T2C 03T150000077

MF =1 (PU) : Mirror
MF =0 (PD) : Normal

SP7615 SP7618 R7617 0Ohm R7616 00Ohm

R7603 40.2Ohm 1% R7602 40.2Ohm 1% R7605 40.2Ohm 1% R7604 40.2Ohm 1%

C7601 0.01UF/16V C7602 0.01UF/16V

R7600 549Ohm R7601 1.33KOhm 1% R7609 931OHM 1% C7600 820PF/50V R7612 121OHM 1% C7605 820PF/50V R7613 121OHM 1%

Q7600 RUM003N02GT2L Rdson=1.4Ohm/Vgs(th)=1V

74,77,78 GPIO10_MEM_VREF_CTL

PLACE NEAR DRAM

C7657 C7658 C7659 C7660 C7661 C7662 C7663 C7628 C7629 C7630 C7631 C7632 C7633 C7634

PLACE UNDER DRAM

C7606 C7607 C7609 C7610 C7611 C7612 C7613 C7614 C7664 C7665 C7616 C7617 C7618 C7619 C7620 C7621 C7622 C7623 C7624 C7625 C7626 C7627 C7675 C7668 C7669 C7670 C7674 C7671 C7673 C7672 C7685 C7684 C7683 C7676 C7677 C7678 C7682 C7679 C7681 C7680

C7635 C7636 C7637 C7638 C7639 C7640 C7641 C7642 C7667 C7666 C7645 C7646 C7647 C7648 C7649 C7650 C7651 C7652 C7653 C7654 C7655 C7656 C7693 C7686 C7687 C7688 C7692 C7690 C7691 C7689 C76103 C76102 C76101 C7694 C7695 C7696 C76100 C7697 C7699 C7698

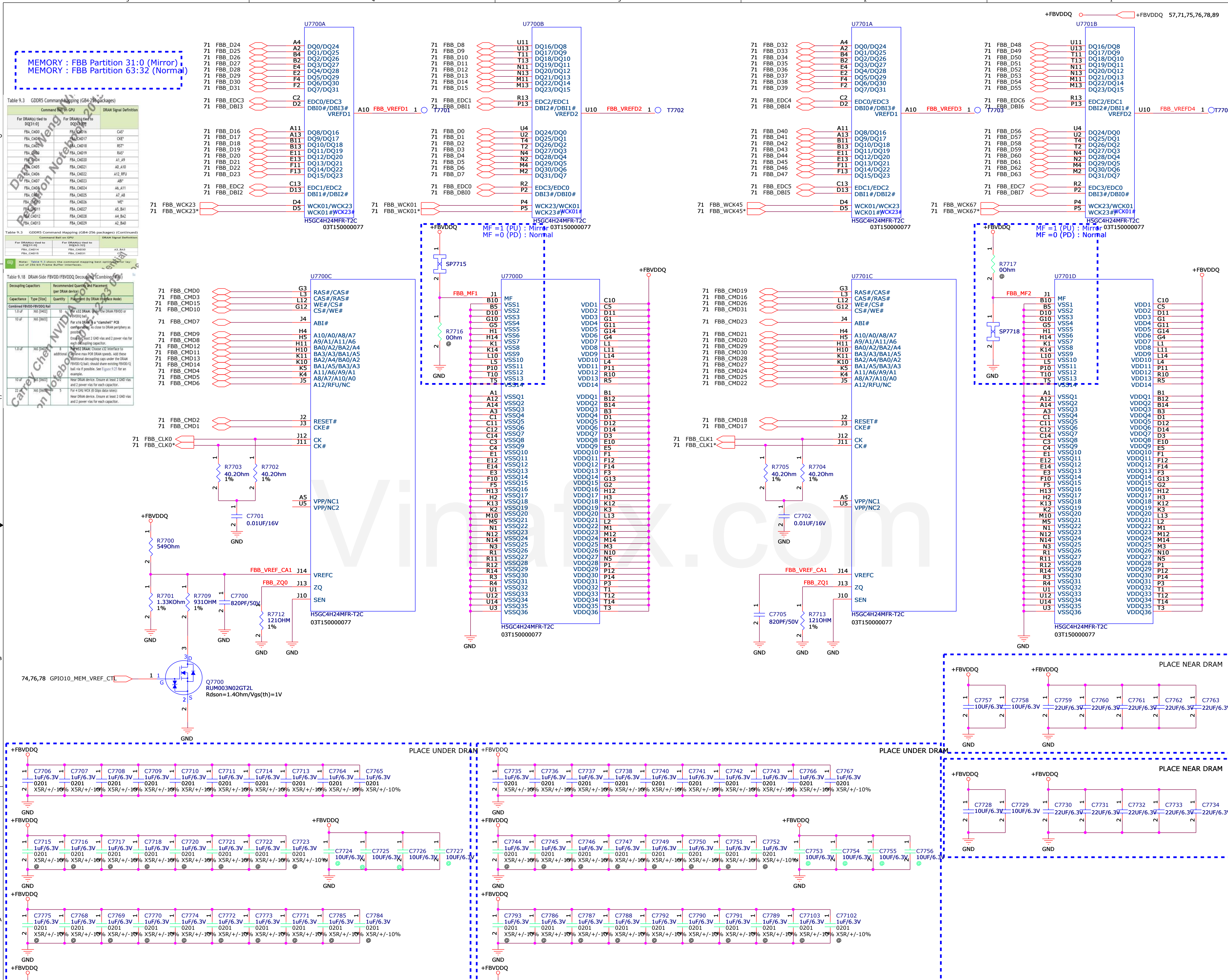
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: GDDR5 256M X32bit_A

BG1-HW RD Div.2-HW RD Dept.3 Engineer: Hank_Zheng

Size: Custom | Project Name: FX505GE | Rev: 1.0

Date: Monday, July 23, 2018 | Sheet 76 of 105



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RD Div.2-HW RD Dept.3

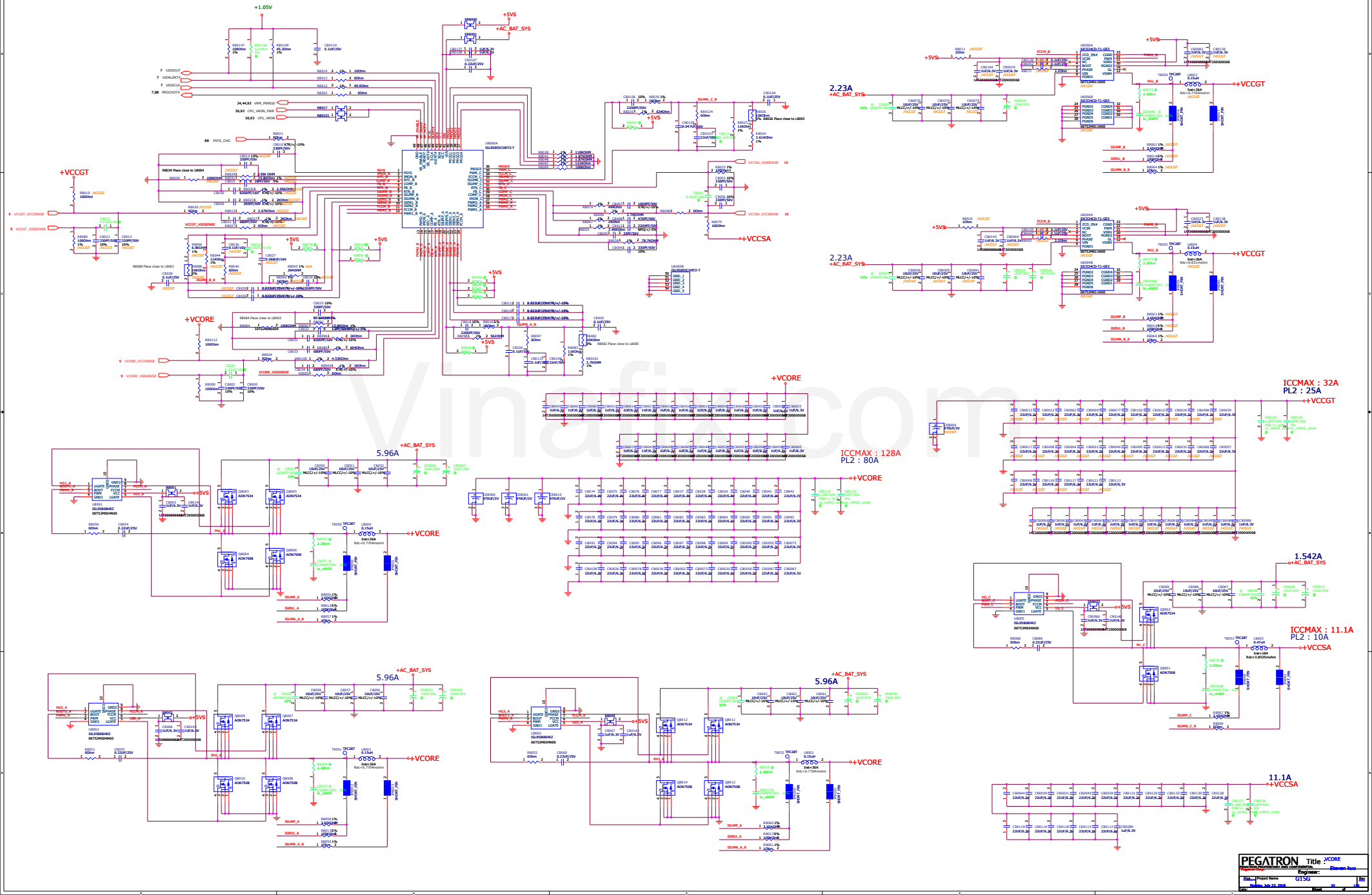
Title : GDDR5 256M X32bit_B

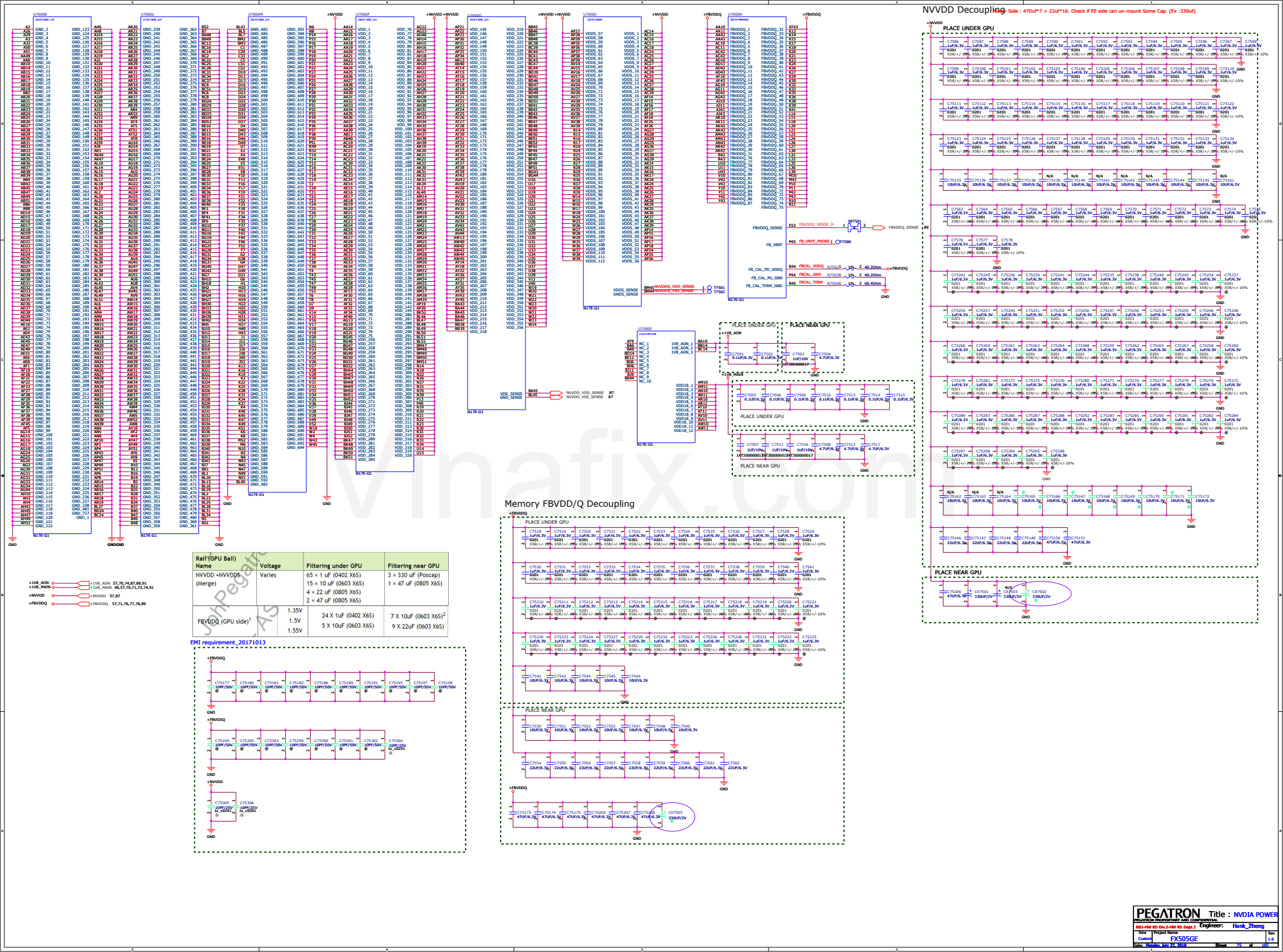
Engineer: Hank_Zheng

Size	Project Name	Rev
Custom	FX505GE	1.0

Date: Monday, July 23, 2018 Sheet 77 of 105

VCORE POWER SUPPLY





Rail (GPU Ball) Name	Voltage	Filtering under GPU	Filtering near GPU
NVVDD +NVVDD5 (Merge)	Varies	65 × 1 uF (0402 X6S) 15 × 10 uF (0603 X6S) 4 × 22 uF (0805 X6S) 2 × 47 uF (0805 X6S)	3 × 330 uF (Poscap) 1 × 47 uF (0805 X6S)
FBVDDQ (GPU side)[1]	1.35V 1.5V 1.55V	24 X 1uF (0402 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S)[2] 9 X 22uF (0603 X6S)

+1V8_AON 57,70,74,87,89,01
+1V8_MAIN 48,57,70,71,72,74,91
+NVVDD 57,87
+FBVDDQ 57,71,76,77,78,89

EMI requirement_20171013

PEGATRON	Title : NVDIA POWER	
PEGATRON CORPORATION PROPRIETARY AND CONFIDENTIAL		
DG1-HW BD Dk.3-HW BD Dapt.1	Engineer: Hank_Zheng	
Size: Custom	Project Name: FX505GE	Rev: 1.0
Date: Monday, May 28, 2018	Sheet: 75 of 105	