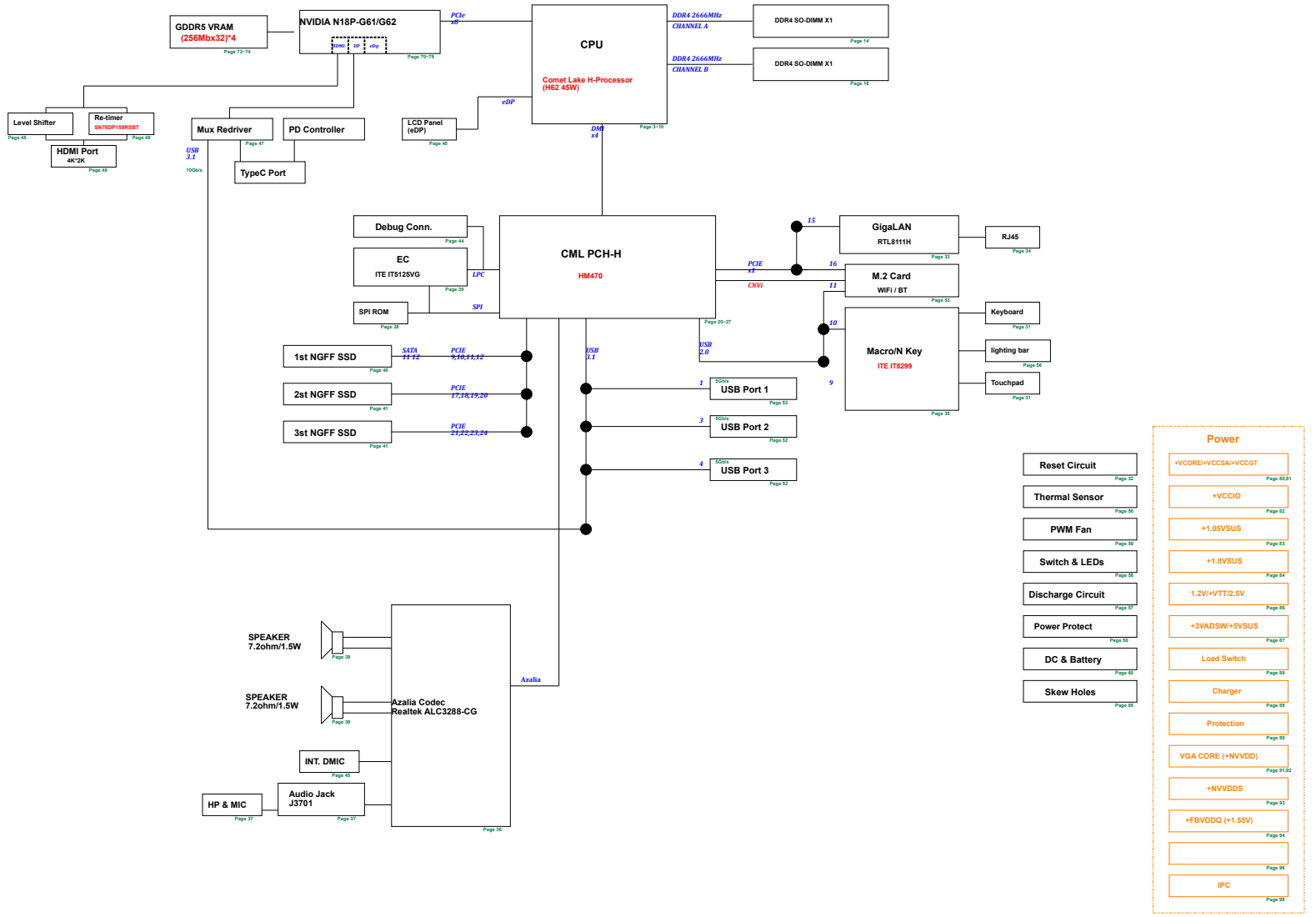
G512LI、G512LH、G712LI Block Diagram

Comet Lake H Platform



ASUS	Project Name: G512LI		Rev: 1.0
Title : Block Diagram			
Size: D	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet: 1 of 103		

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	BC1B#	Native	BC_1B#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_48CH2I_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_BusPwrDnAck		PD 10K(8)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_FREQ_REQ0# _X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN# _X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_CLKM# _X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT# _X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MSWV_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP914	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPP918	PD		
GPP_B19	GPI	GPO	PCH_GPP919/WT_ON_PCH		PD 10K(8)	
GPP_B20	GPI	GPO	PCH_GPP920/WV_GPO_EVENT#		PU 10K(8)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP921/WV_GC6_FB_EN		PU 10K(8)	+3VS
GPP_B22	GPO	Strap	PCH_GPP922	PD		
GPP_B23	GPO	GPO	SMLIALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_DATA		PU 2.2K	+3VSUS
GPP_C2	SPI	Strap	PCH_GPPC2			
GPP_C3	SMLOCLK	Native	SMLO_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLOGATA	Native	SMLO_DAT		PU 2.2K	+3VSUS
GPP_C5	SPI	Strap	PCH_GPPC5	PD		
GPP_C6	GPI	Native	SMLI_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SMLI_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SELO		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PD 10K	+3VSUS
GPP_C16	GPO	GPO	AOAC_WLANLED		PU 10K(8)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(8)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(8)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 1K	
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT		PD 10K	
GPP_D1	GPO	GPO	GPIO_3 PCH_PWM		PD 10K	+VCC3V3_EX
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#			
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCH_ID0		PD 10K	
GPP_D10	GPI	Strap	PCH_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID			
GPP_D12	GPI	Strap	TOUCH_PANEL_ID			
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(8)	+3VSUS
GPP_D14	GPO	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPO	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET2		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)			
GPP_E4	GPI	Native	MOFF2_DEVSLP			
GPP_E5	GPI	Native	(N.C)			
GPP_E6	GPI	Native	MOFF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(8)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	I_VCCEN_PCH_X1			
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	I_BKLTCTL_PCH_X1			
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)		PD 4.7K	
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_MSPI1# _X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_USB31# _X1		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CS#			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 100K	
GPP_I1	GPI	Native	(N.C)		PD 100K	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	Native	(N.C)			
GPP_I4	GPI	Native	SSP_I4		PD 100K	
GPP_I5	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)		PU 2.2K(8)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(8)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 150K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS5#		PD 150K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	GPIO	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(8)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PHYEN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PU 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (8)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (8)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	Alt	PWM	PM_LED_PWM		
GPA7	O	GPO	GS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_EC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	HDMI_WK#2	PD 10K	
GPB6	OD	GPO	BC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (8)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_THRMTRIP#	PU 10K (8)	+3VSUS
GPC4	I	GPI	EC_SATA/CHP1#	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	O	GPO	EC_SPI7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/WL_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PU 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/USB_SS#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	PCHRSTB# _WC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PU 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K (8)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VDUS_ON	PU 100K±5% 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K±5% 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0 CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0 DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	GPI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_DISACK#		
GPG2	I	GPI	EC_GPG2/PMBL1#IT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCK#/EC_SCK#_PCH		
GPG4	GPI		EC_SI/EC_SI_PCH		
GPG5	GPI		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VEN		
GPG7	GPI		EC_SCK_PCH	PD 10K (8)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB1 CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB1 DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_SUSC#T#	PU 10K (8)	
GPH4	O	GPO	DPWROK EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S0#		
GPI1	I	GPI	SYSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PU 0	+3VACC
GPI7	Alt	AD	WA_MAX_POWER	PU 100K x PU 54K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB11_5VSUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VAUSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	FL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_USB_STA7#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5	PU 2.2K	
GPJ6	I	GPI	PS_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EC0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EC01		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EC02		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EC03		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EC0CK		CLK_48CH2I_PCH		
GPM5	LFRAME#/EC0#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h

EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
VGA Thermal Sensor	90h
CPU Thermal Sensor	98h
Power Thermal Sensor	70h

Device Identification

CPU Thermal Sensor	
1st	0x0423 / 0x19
2nd	

GX501VIP/CIE & USB Function define

Kabylake HM175

GID	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 MB Port1(Charger)	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02	USB3.0 Port3	
04	USB3#04	USB3.0 Port4	
05	USB3#05		
06	USB3#06		
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE		
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA*1 SSD port0	
16	PCIE#10 / SATA#1	PCIE*4 SSD	SRC6
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4
USB2_06	
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1	x 2	x 4	NA	
8	USB3 #8	PCIE #2	x 2			
9	PCIE #3		x 2			
10	USB3 #10	PCIE #4	GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			NA	NA	NA
24	SATA #5					
25	PCIE #19			x 2		
26	PCIE #20					

SKL PCH-H H170 HSIO

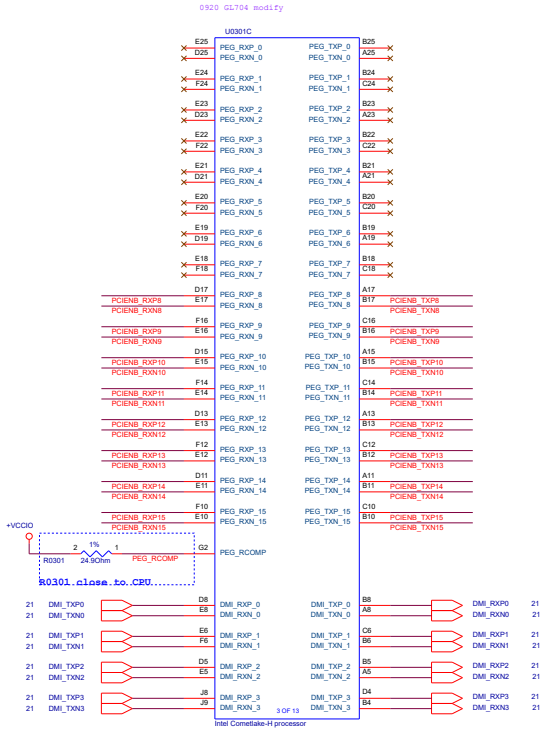
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7					
8	USB3 #8					
9	PCIE #3		x 2	NA	NA	
10	PCIE #4	GbE				
11	PCIE #5	GbE	x 2	x 4	NA	
12	PCIE #6					
13	PCIE #7		x 2			
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			NA	NA	NA
24	SATA #5					
25	PCIE #19			x 2		
26	PCIE #20					

SKL PCH-H HM170 HSIO

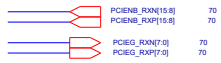
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1	x 2	x 4	NA	
8	USB3 #8	PCIE #2	x 2			
9	PCIE #3		x 2			
10	PCIE #4	GbE				
11	PCIE #5	GbE	x 2	x 4	NA	
12	PCIE #6					
13	PCIE #7		x 2			
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23				NA	NA	NA
24						
25				NA		
26						

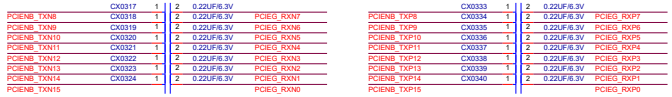
ASUS	Project Name: G512LI		
Title: System Setting		Size:	Rev: 1.0
Date: Monday, January 08, 2018	Sheet: 1 of 1	Engineer: Gaming RD	

PCIEG



CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8





Display

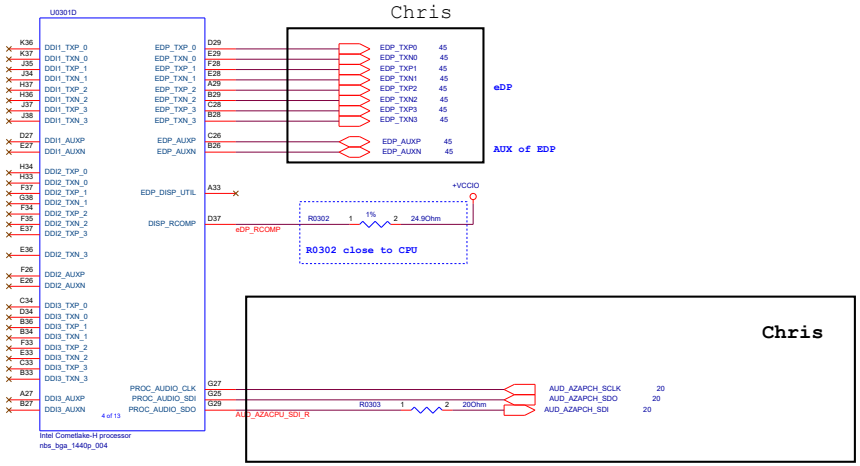


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CFL-H PDG P.363 (Doc.571391)

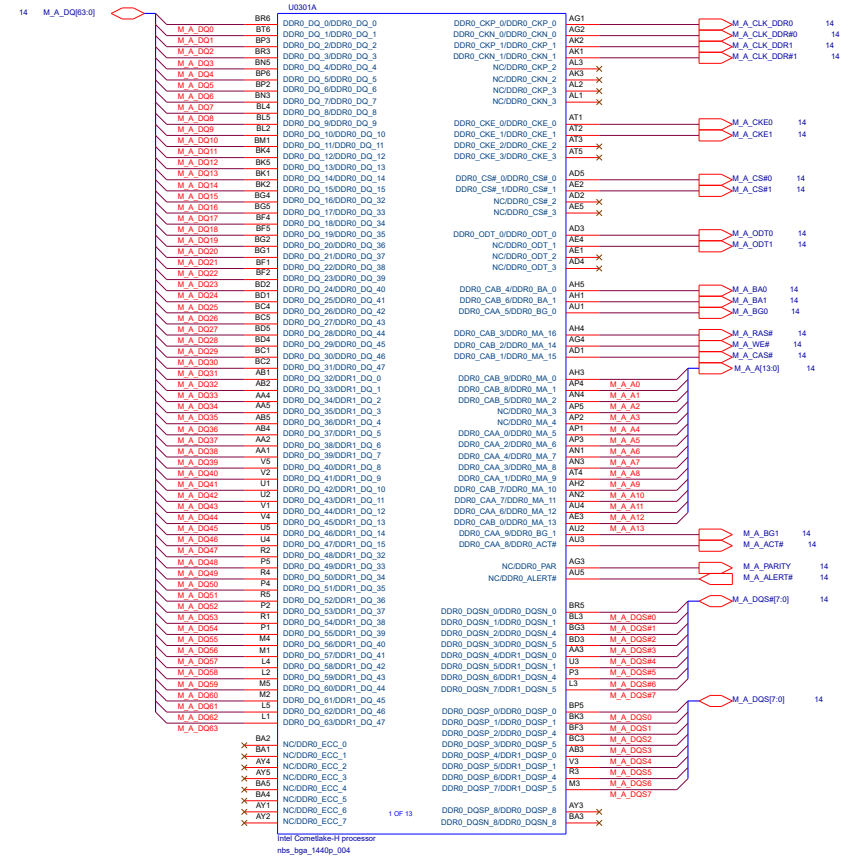
31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

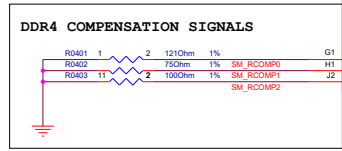
ASUS	Project Name: G512LI	Rev: R1.1
Title : CPU_DMI,PEG,FDI,eDP,DDI		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 3 of 103	

Memory Channel A



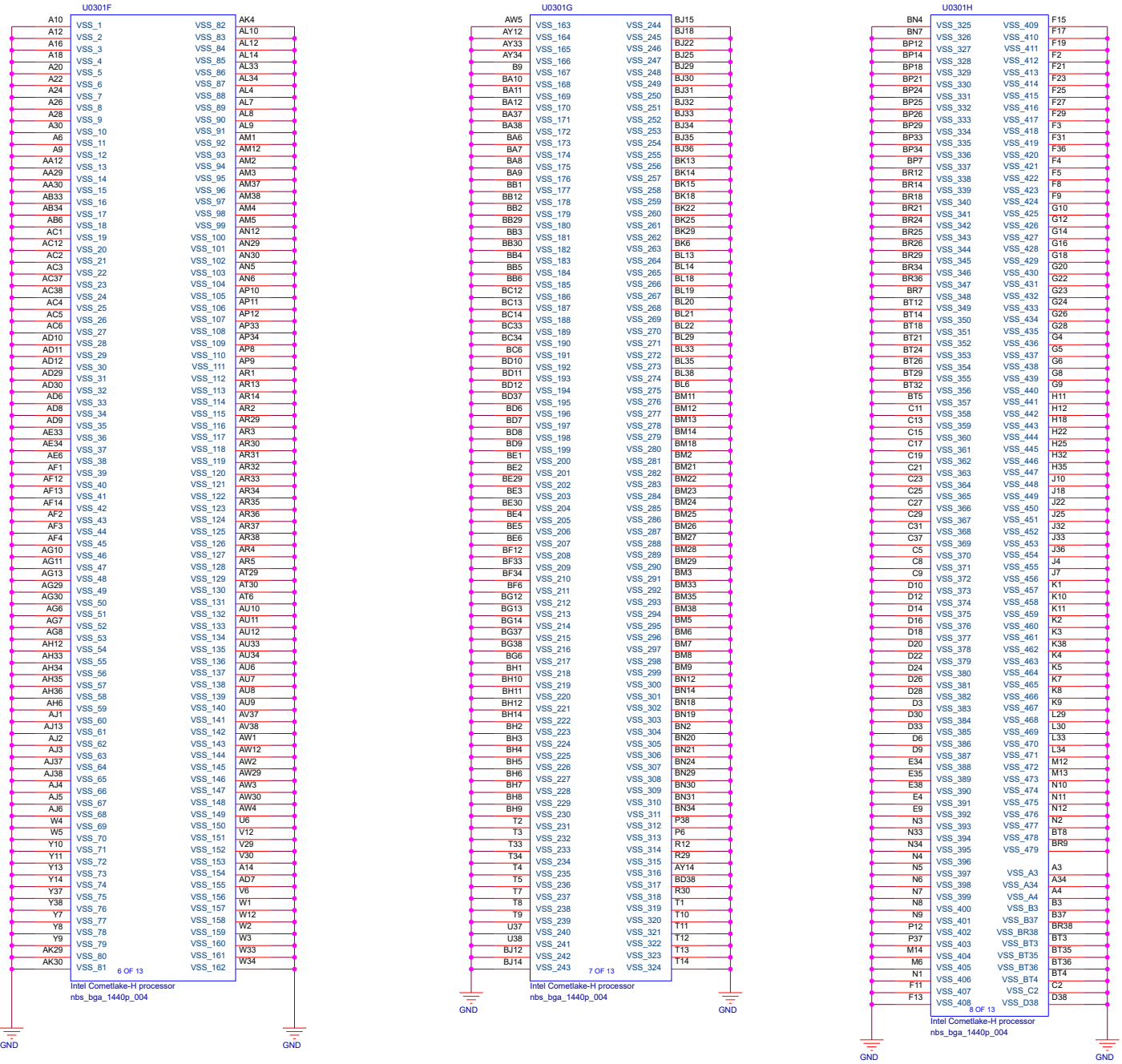
Memory Channel B

DDR4 COMPENSATION SIGNALS



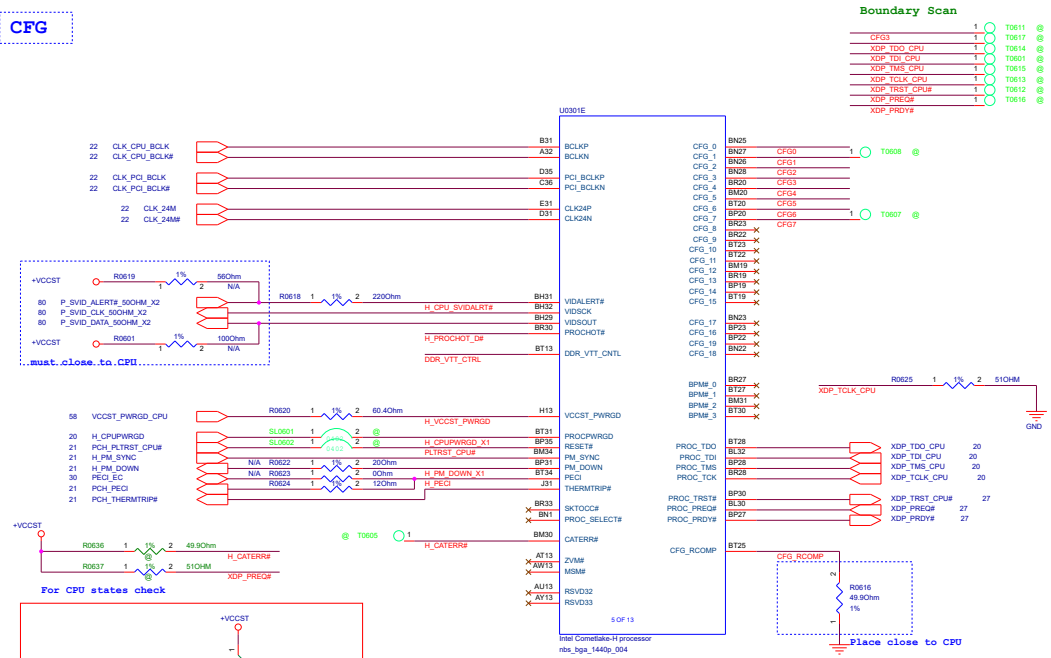
Project Name: G512LI			Rev: 1.0
Title: CPU_DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 4 of 103		

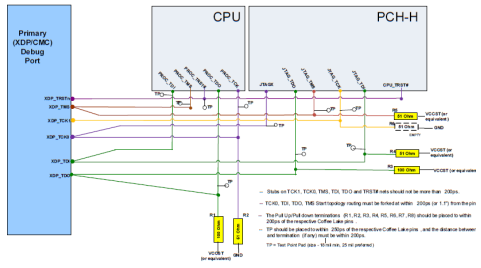
Main Board



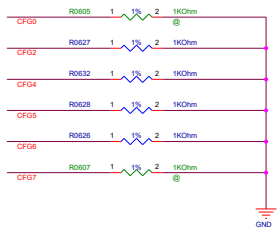
ASUS	Project Name: G512LI	Rev: 1.0
Title :	CPU_CFG,RSVD,GND	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 5 of 103	

CFG





CFG Straps



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

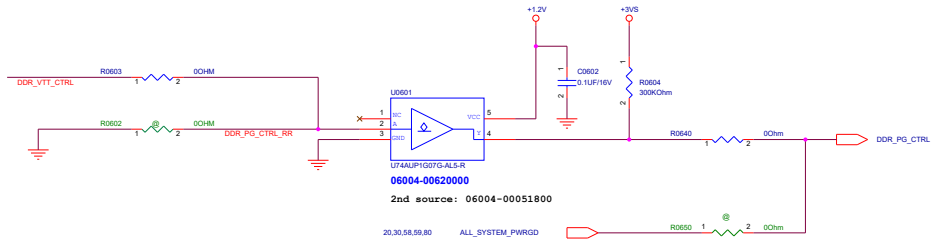
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

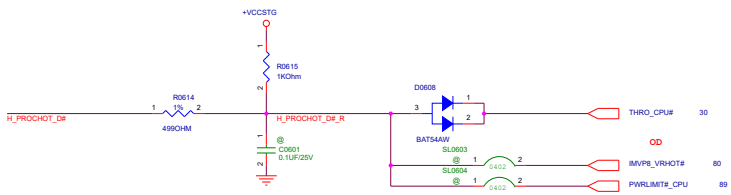
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

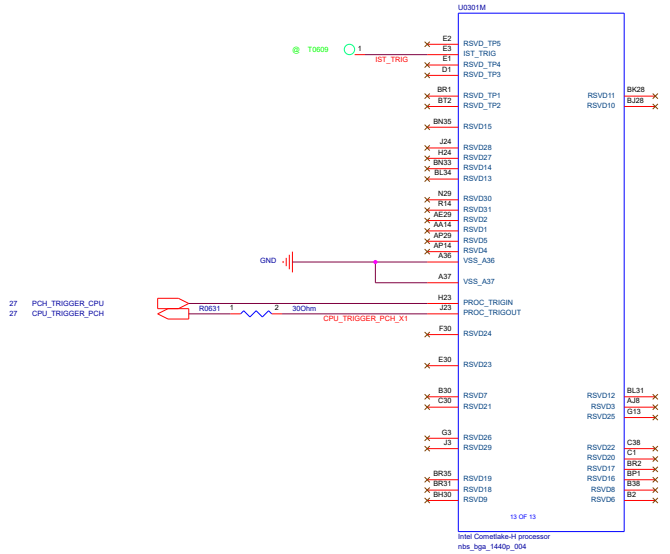
VTT Enable



CPU SIDEBAND SIGNALS

teknisi indonesia

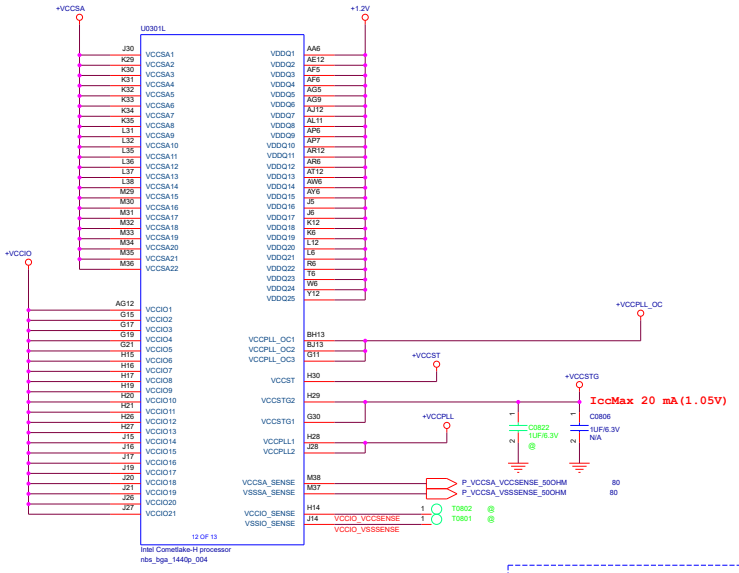


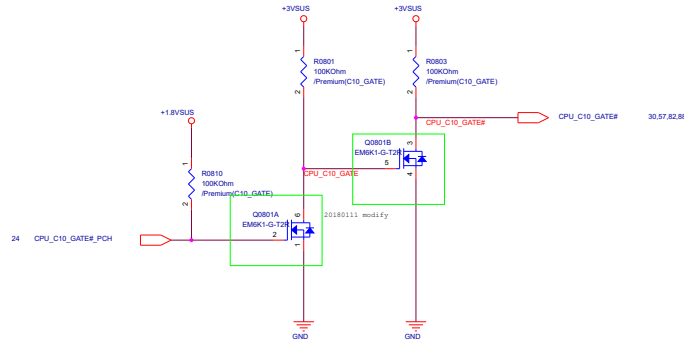


ASUS	Project Name: G512LI		Rev: 1.0
Title : CPU_CFG,RSVD			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 6 of 103		

CPU XDP(20190723 remove)

Project Name: G512LI		Rev: 1.0
Title : CPU XDP		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 7 of 103	





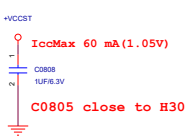
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

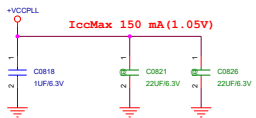
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)





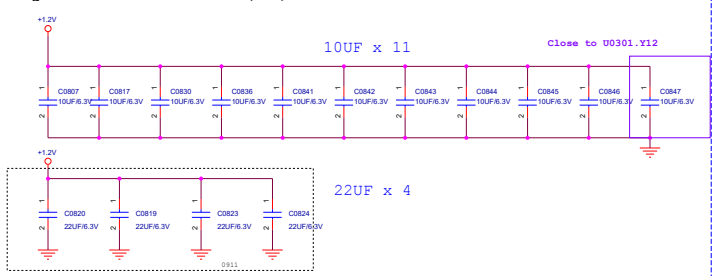
CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines

Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H IBP#571391 and CFL-U IBP#571021 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.

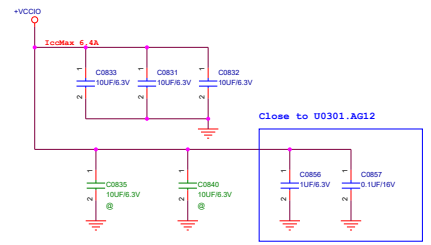
An additional capacitor 0805 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.

This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

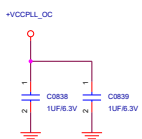
+VDDQ DECAPS Place Back Side (TOP)



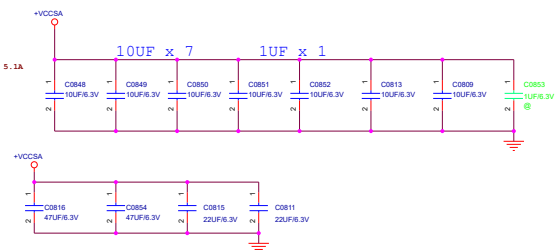
+VCCIO DECAPS Place Back Side (TOP)



+VCCPLL_OC DECAPS Place Back Side (TOP)



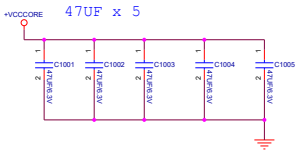
+VCCSA DECAPS Place Back Side (TOP)



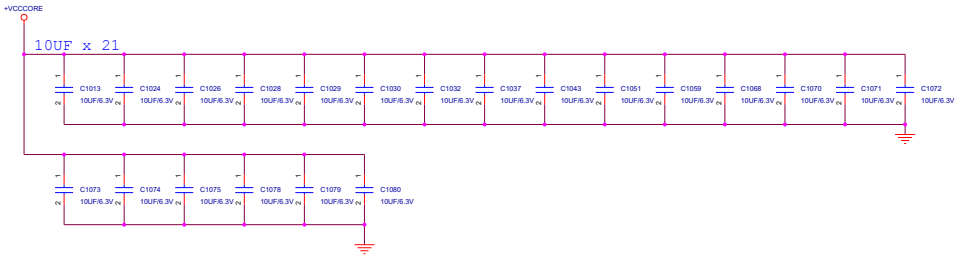
ASUS	Project Name: G512LI		Rev: 1.0
Title : CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020		Sheet 8 of 103	

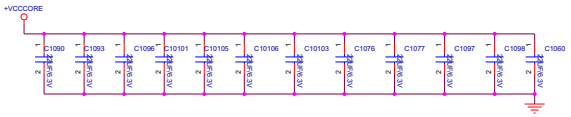
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

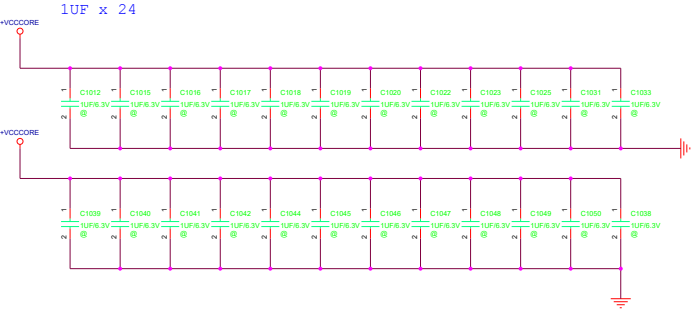
+VCCORE near CPU



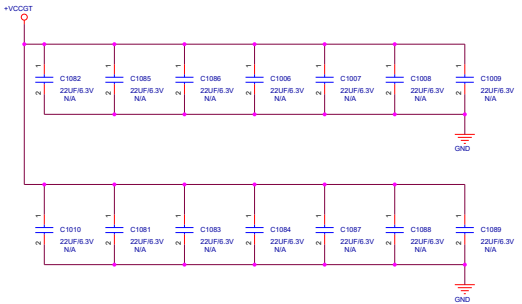
+VCCORE DECAPS Place Back Side (TOP)



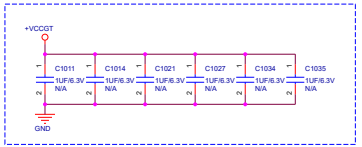




+VCCGT cap near CPU **22uF x14**



1107 add for VCCGT PI issue



ASUS	Project Name: G512LI		Rev: 1.0
Title : 010_CPU_POWER_CAP			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 10 of 103		

	Project Name G512LI	Rev R1.0

Title : TBT_Alpine-Ridge

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER	Gaming RD

Date: Monday, January 20, 2020	Sheet 11 of 103

Project Name

G512LI

Rev

R1.3

Title : CYPRESS CCG4

Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER	Gaming RD

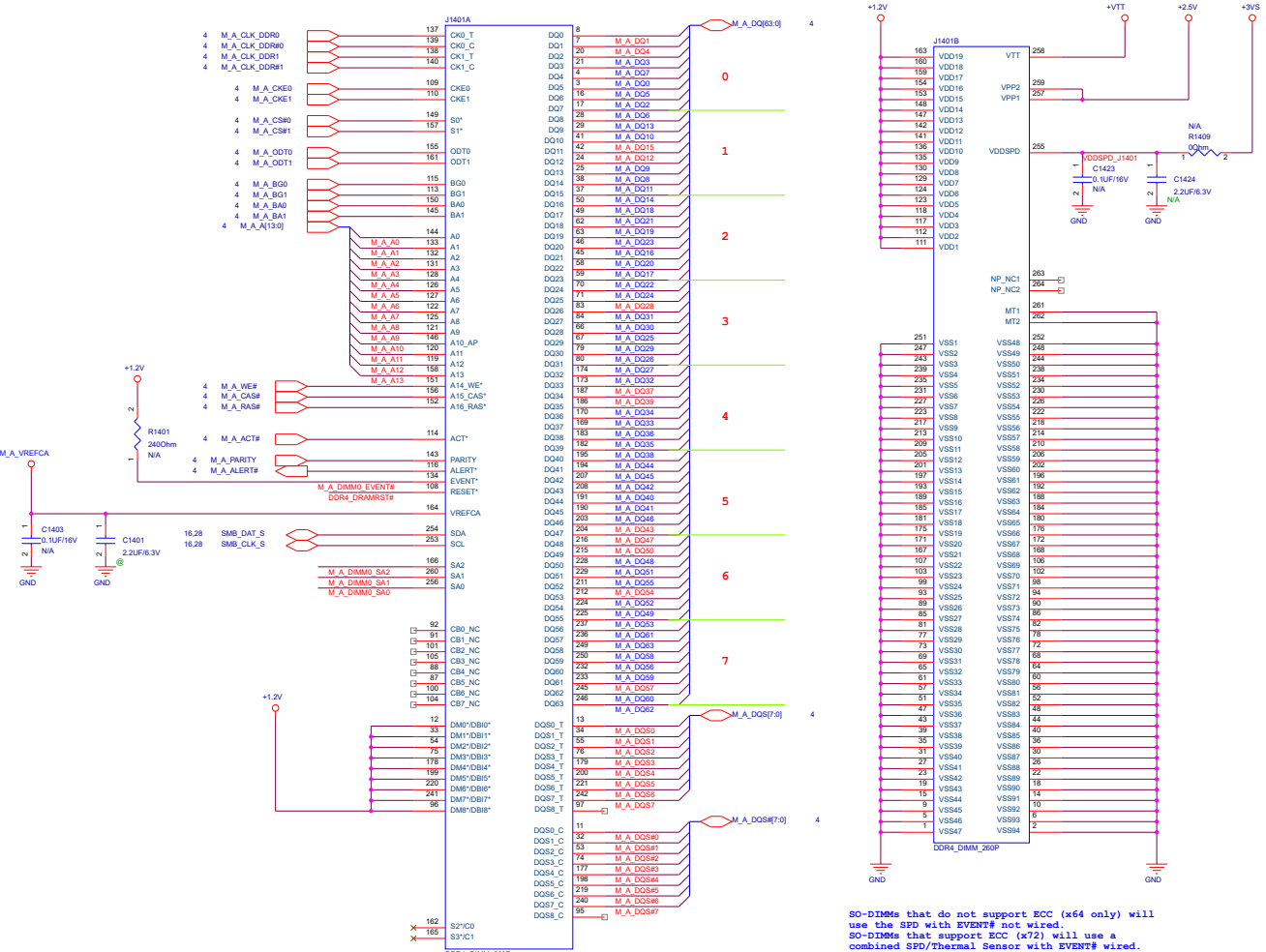
Date: Monday, January 20, 2020

<Variant Name>

ASUSTeK COMPUTER	Title : DDR4_TERMINATION	
	Engineer: Gaming RD	
Size: Custom	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 13 of 103	

Chris

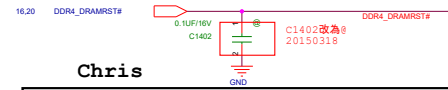
SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)



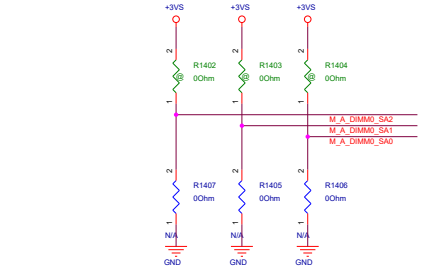
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

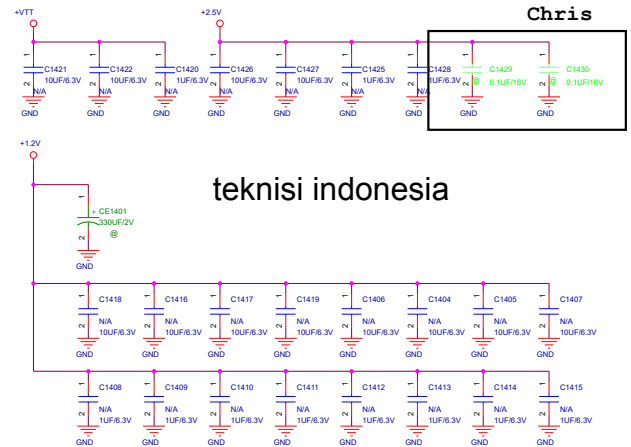
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Main Board



Chris





Chris

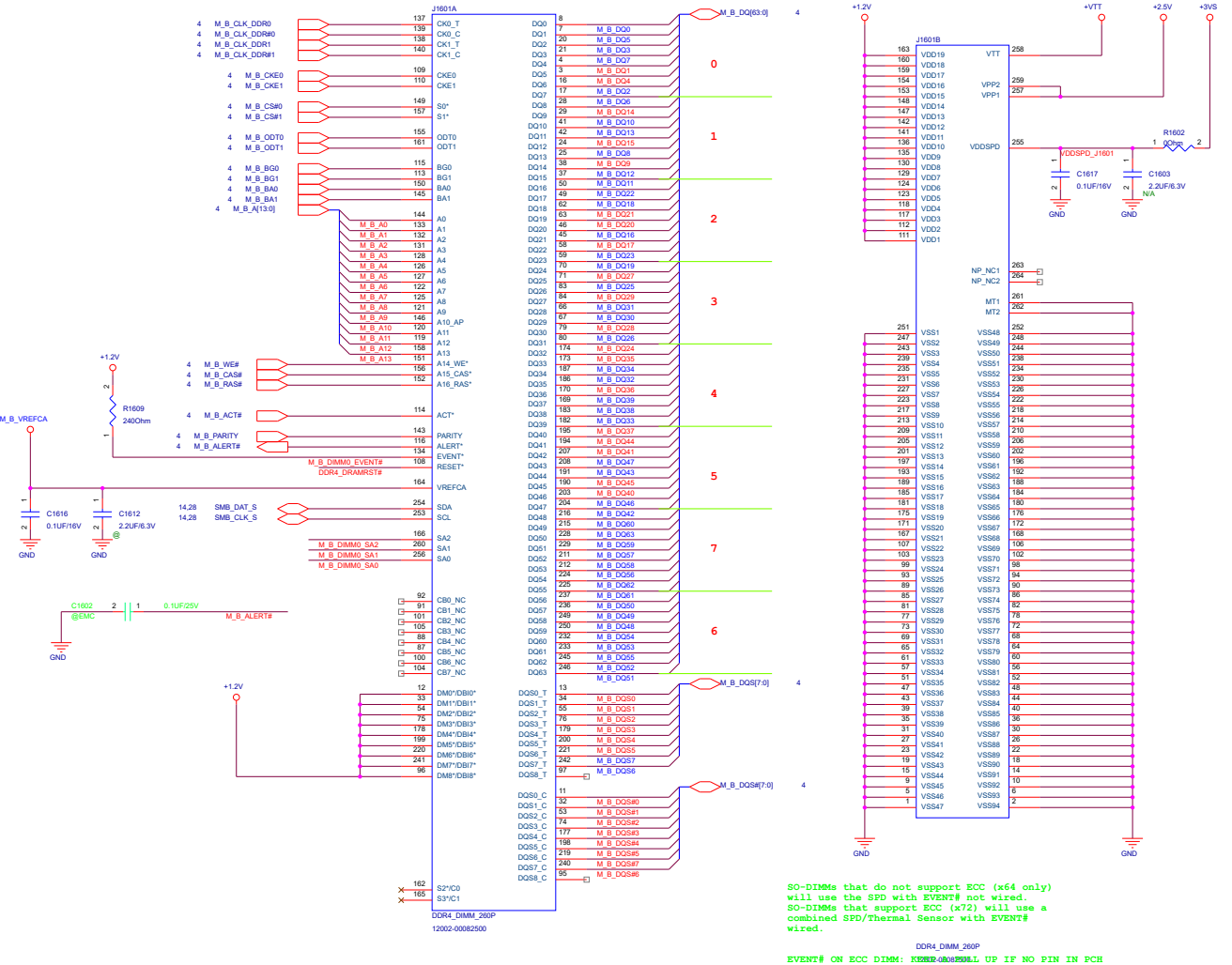
teknisi indonesia

ASUS	Project Name: G512LI		Rev: R1.0
Title :	DIM_DDR4 SO-DIMM A1		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 14 of 103		

<Variant Name>

ASUSTeK COMPUTER	Title : DDR4_ON-BOARD_A2	
	Engineer: Gaming RD	
Size: C	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 15 of 103	

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

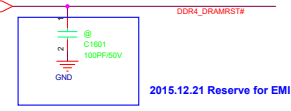


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP 10K PULL UP IF NO PIN IN PCH

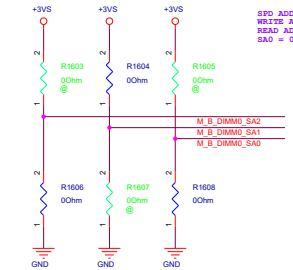
Main Board

14.20 DDR4_DRAMRST#



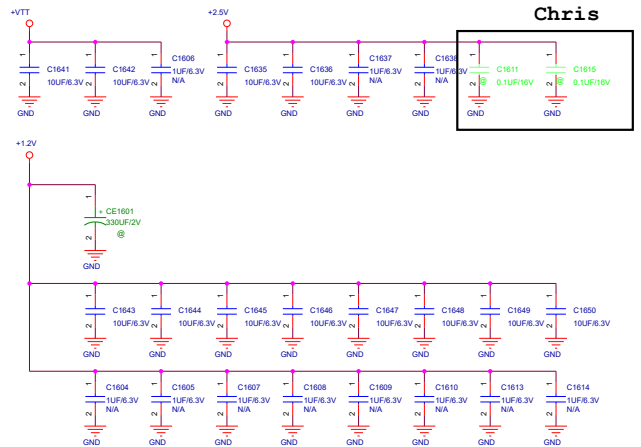
2015.12.21 Reserve for EMI

Chris



SPD ADDRESS FOR CHANNEL-B
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA5
SA0 = 0; SA1 = 1; SA2 = 0

Chris



ASUS	Project Name: G512LI	Rev: 1.0
Title :	DIM_DDR4 SO-DIMM B1	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 16 of 103	

<Variant Name>

ASUSTeK COMPUTER teknisi indonesia	Title : NB_****	
	Engineer: Gaming RD	
Size: A	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 17 of 103	

Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview

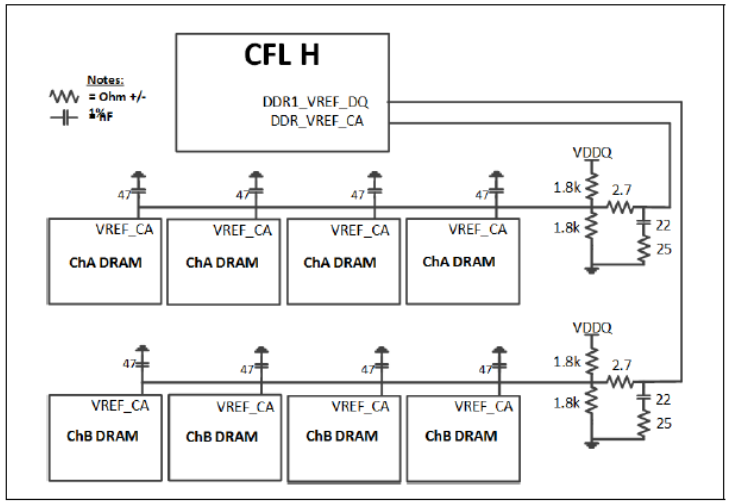
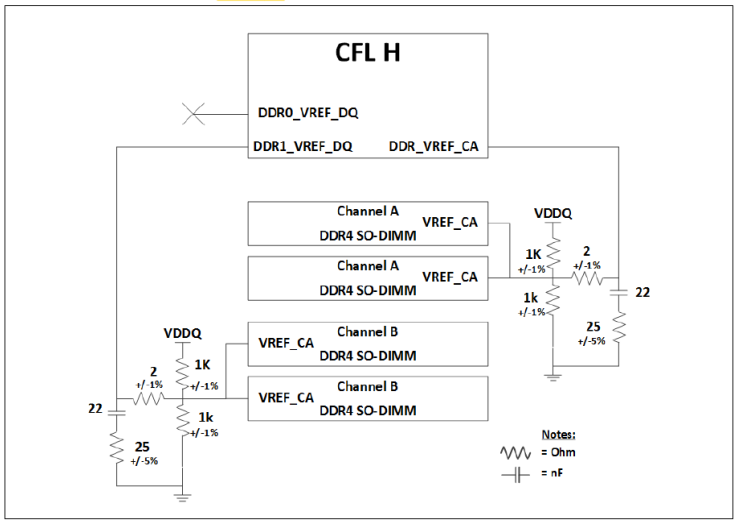
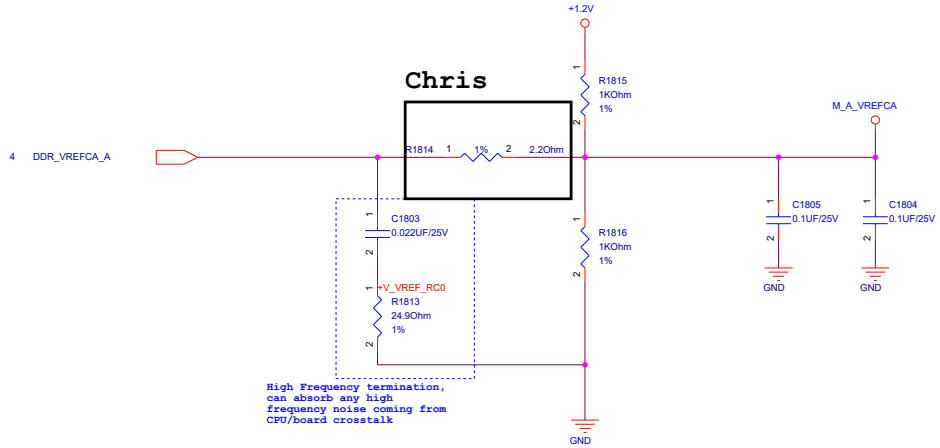


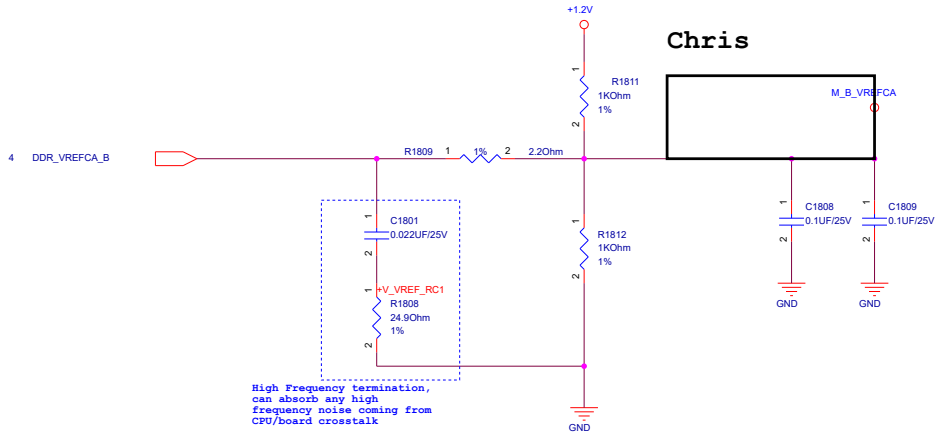
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



Vref for CHA_DIMM0



Vref for CHB_DIMM0



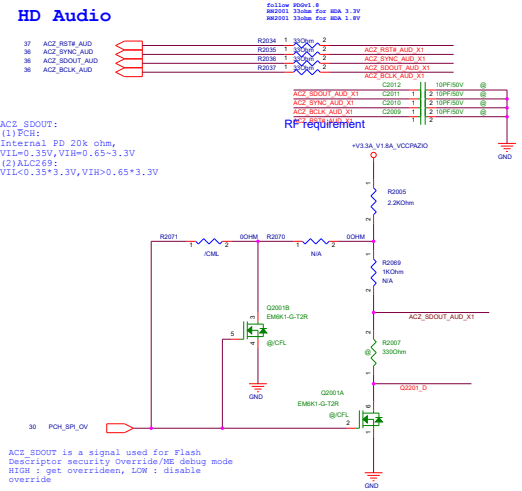
Main Board

ASUS	Project Name: G512LI	Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 18 of 103	

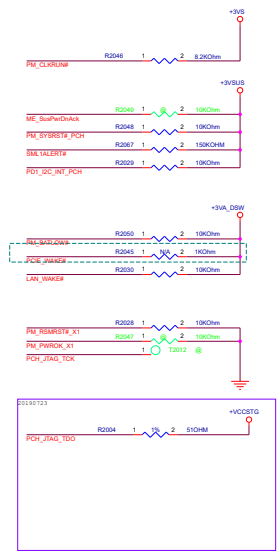
<Variant Name>

ASUSTeK COMPUTER	Title : *****	
	Engineer: Gaming RD	
Size: C	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 19 of 103	

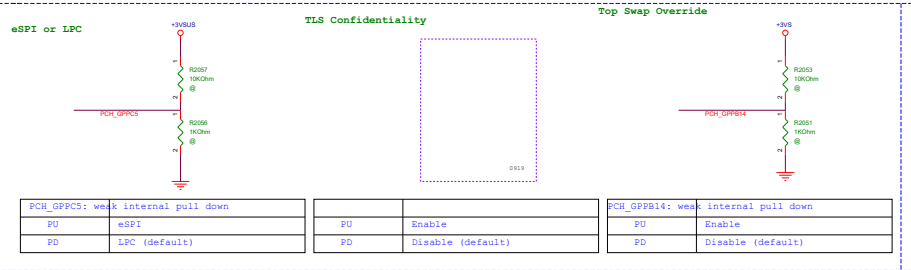
HD Audio



Main Board



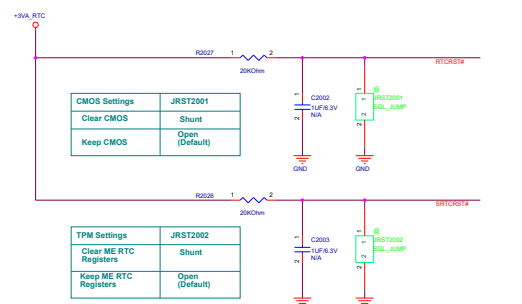
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+V3.3A_V1.8A_VCCPAZIO
		+3VS		

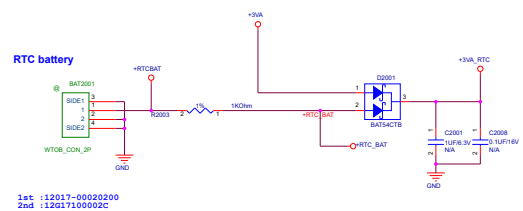


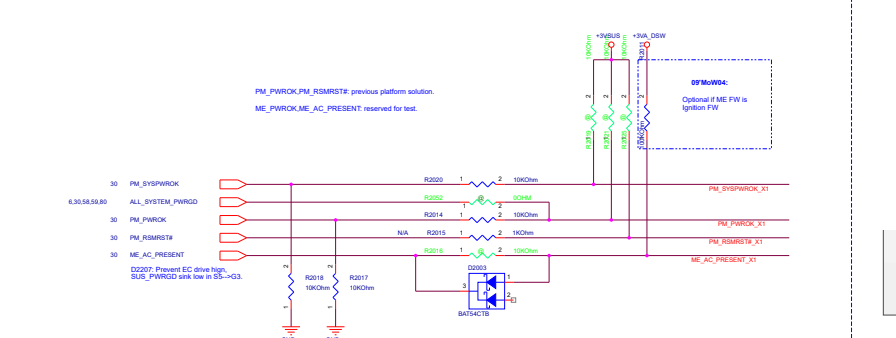
PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

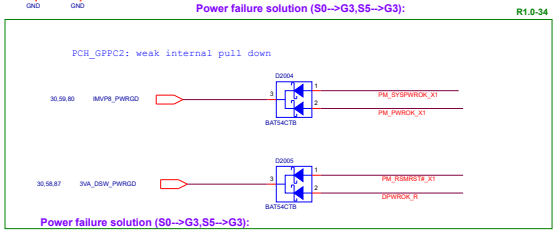
PU	Enable
PD	Disable (default)

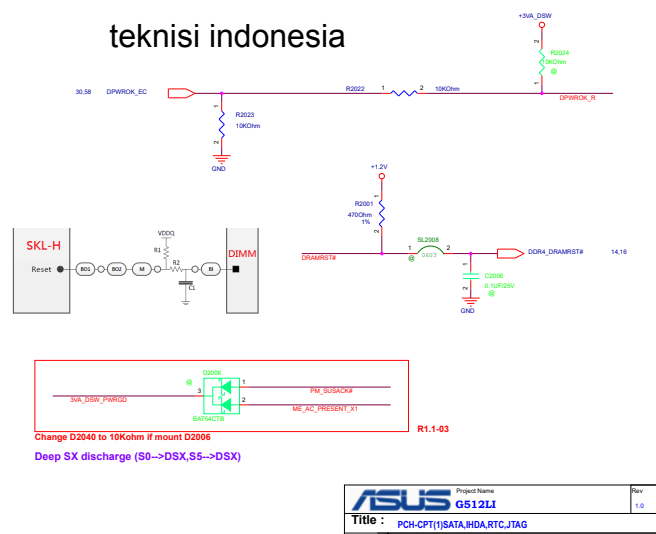
PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)











ASUS	Project Name: G512LI		Rev: 1.0
Title :	PCH-CPT(1)SATA,HDA,RTC,JTAG		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet: 20	of: 103	

PCIE Setting

GX501GI PCIE/SATA Function define

CNL HM370

HSIO Capabilities	Function
PCIEG (From GPU)	
PCIE#01 - USB3.1#07	
PCIE#02 - USB3.1#08	
PCIE#03 - USB3.1#09	
PCIE#04 - USB3.1#10	
PCIE#05	
PCIE#06	
PCIE#07	
PCIE#08	
PCIE#09	PCIE*4 SSD
PCIE#10	
PCIE#11- SATA-0a	
PCIE#12- SATA-1a	
PCIE#13- SATA-0b	
PCIE#14- SATA-1b	
PCIE#15 / SATA#2	
PCIE#16 / SATA#3	WLAN
PCIE#17 / SATA#4	
PCIE#18 / SATA#5	
PCIE#19 / SATA#6	
PCIE#20 / SATA#6	
PCIE#21	TBT (x4)
PCIE#22	
PCIE#23	
PCIE#24	

Function	
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	CR
CLKREQ-3	WLAN
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

USB Setting

GX501GI USB Function define

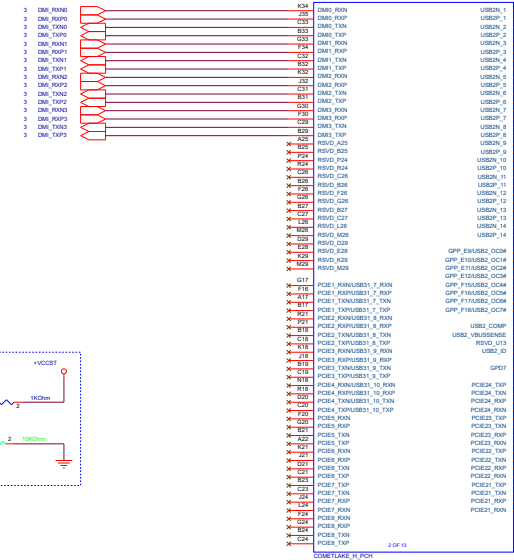
CNL HM370

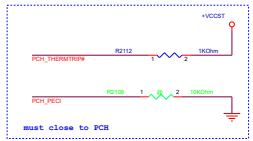
USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4(Charger)
USB2_06	TBT
USB2_07	
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

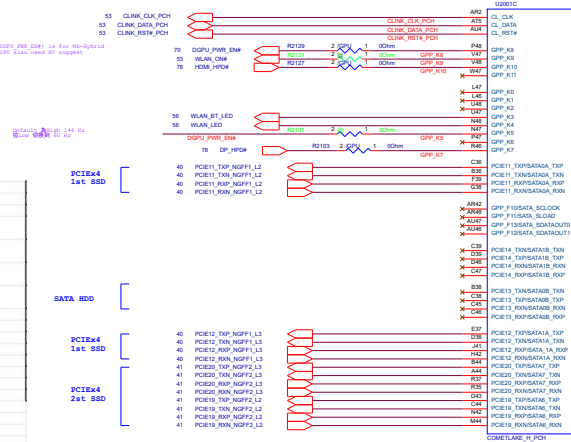
USB 3.0	Function
USB3.1#01	USB3.1MB Port1 (Support Gen2)
USB3.1#02	USB3.0 MB Port2 (Support Gen2)
USB3.1#03	USB3.0 MB Port3 (Support Gen2)
USB3.1#04	USB3.0 MB Port4 (Support Gen2)
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

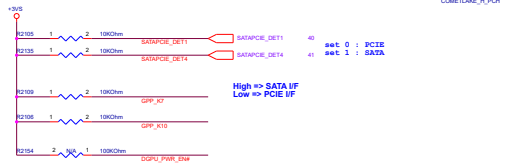
HSIO	HM370	QM370	CM246	IRST			Devices Assign
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1				(port1) USB3.1 Type C
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2				(port2) USB3.1 Type C
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3				(port1) USB3.0 Type A USB3.1 Type A
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4				(port2) USB3.0 Type A USB3.1 Type A
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5				(port3) USB3.0 Type A USB3.1 Type A
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6				(port4) USB3.0 Type A USB3.1 Type A
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7	PCIE #1			CR (USB3.0 / PCIE)
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8	PCIE #2	NO	x4	
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9	PCIE #3		x2	
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10	PCIE #4			
10	NA GbE	PCIE #5 GbE	PCIE #5 GbE		NO	x4	
11	NA	PCIE #6	PCIE #6			x2	Thunderbolt (priority 1)
12	NA	PCIE #7	PCIE #7			x2	
13	NA	PCIE #8	PCIE #8				
14	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE		Yes	x4	x2 1st M.2 SSD (PCIE*4 / SATA#1a)
15	PCIE #10	PCIE #10	PCIE #10				x2 (PCIE*4, optane)
16	PCIE #11 SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a				
17	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE				
18	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE		NO	x4	x2 HDD (SAT#0b)
19	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b				ODD (SAT#1b)
20	PCIE #15	PCIE #15	PCIE #15 SATA #2			x2	GLAN
21	PCIE #16	PCIE #16	PCIE #16 SATA #3				WLAN
22	PCIE #17 SATA #4	PCIE #17 SATA #4	PCIE #17 SATA #4		Yes	x4	x2 2nd M.2 SSD (PCIE*4 / SATA#4)
23	PCIE #18 SATA #5	PCIE #18 SATA #5	PCIE #18 SATA #5				x2 (PCIE*2, optane)
24	PCIE #19	PCIE #19	PCIE #19 SATA #6				
25	PCIE #20	PCIE #20	PCIE #20 SATA #7				
26	PCIE #21	PCIE #21	PCIE #21		Yes	x4	x2 3rd M.2 SSD (PCIE*4)
27	PCIE #22	PCIE #22	PCIE #22				x2 (PCIE*4, optane)
28	PCIE #23	PCIE #23	PCIE #23				
29	PCIE #24	PCIE #24	PCIE #24				

3rd M.2 SSD (PCIE*2, optane) | 10G LAN (PCIE*4) optional | Thunderbolt (priority 2)







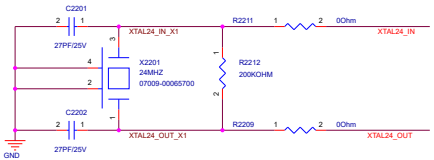


Project Name	G512LI
Rev	1.0
Title :	PCH-CPT(2)_PCIE,CLK,USB
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	Gaming RD
Date:	Monday, January 20, 2020
Sheet	21 of 103

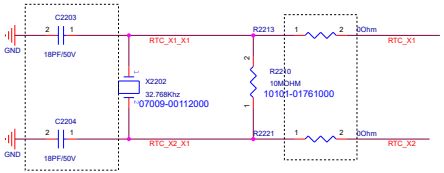
Main Board

XTAL 24MHz

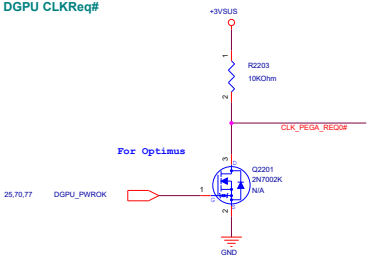
1st:07009-00065700
2nd:07009-00065800



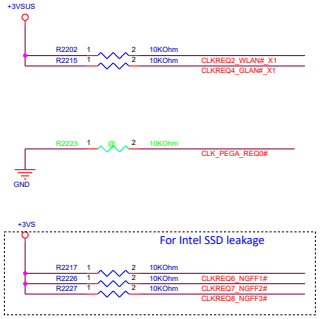
RTC CRYSTAL 32.768KHz

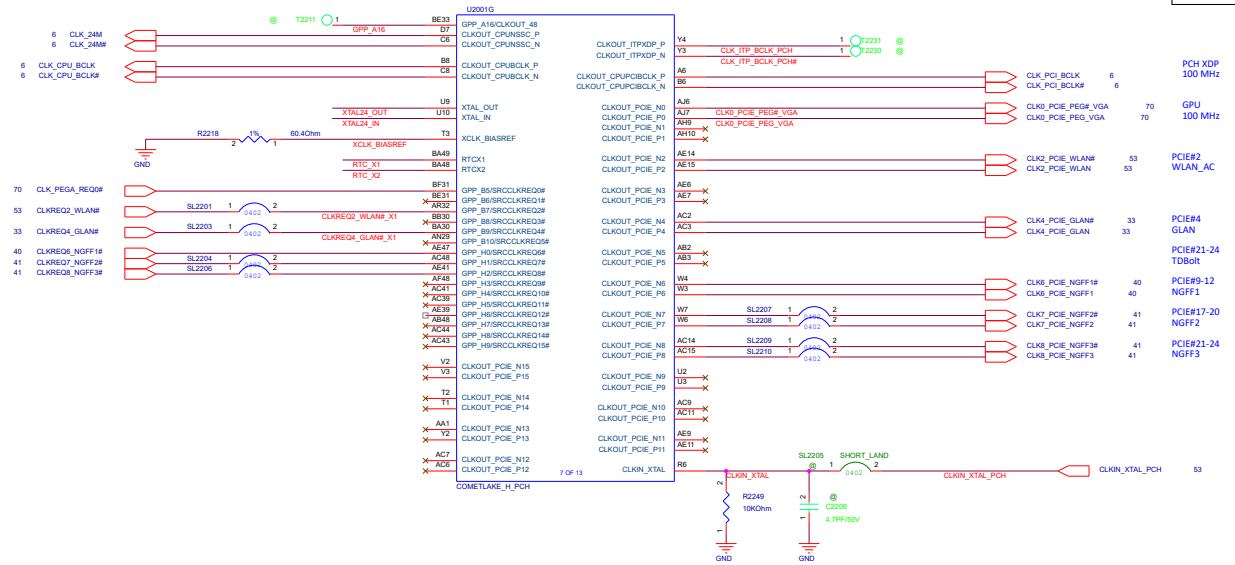


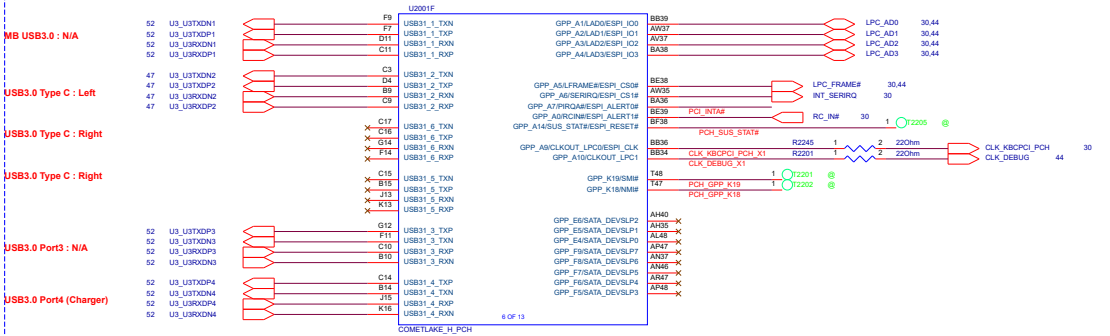
DGPU CLKReq#



PCH CLKREQ Setting:







ASUS	Project Name: G512LI		Rev: 1.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 22 of 103		

HPD0 to DP

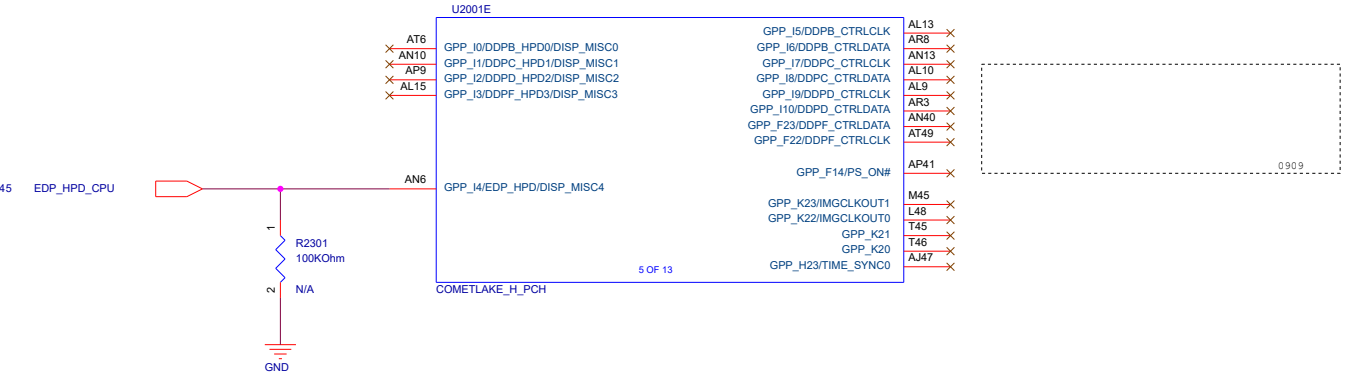
HPD1 to HDMI

HPD2 to TBT

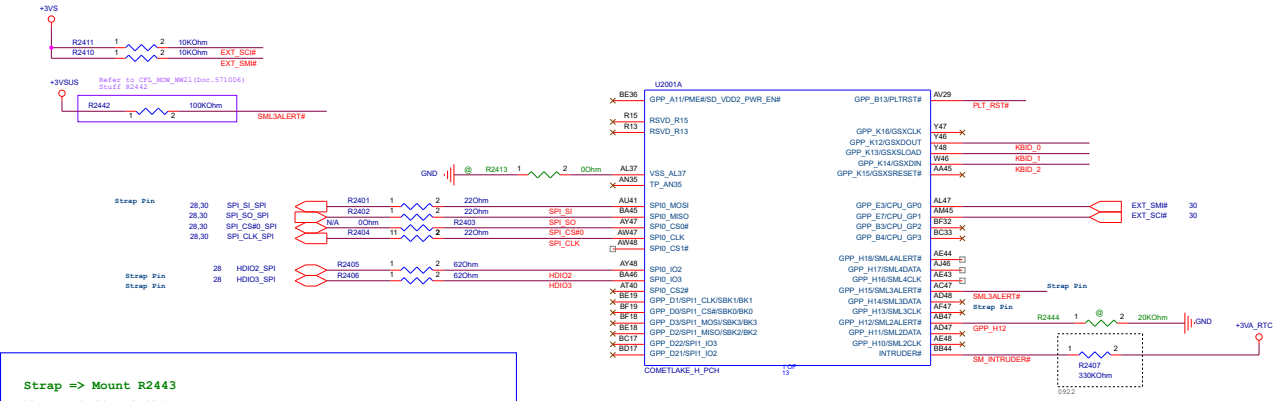
HPD3 to VGA

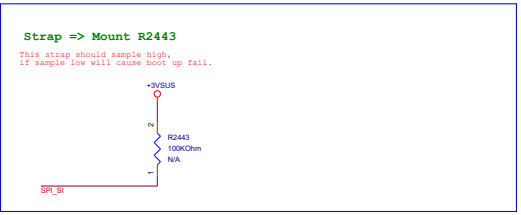
HPD4 to EDP Panel

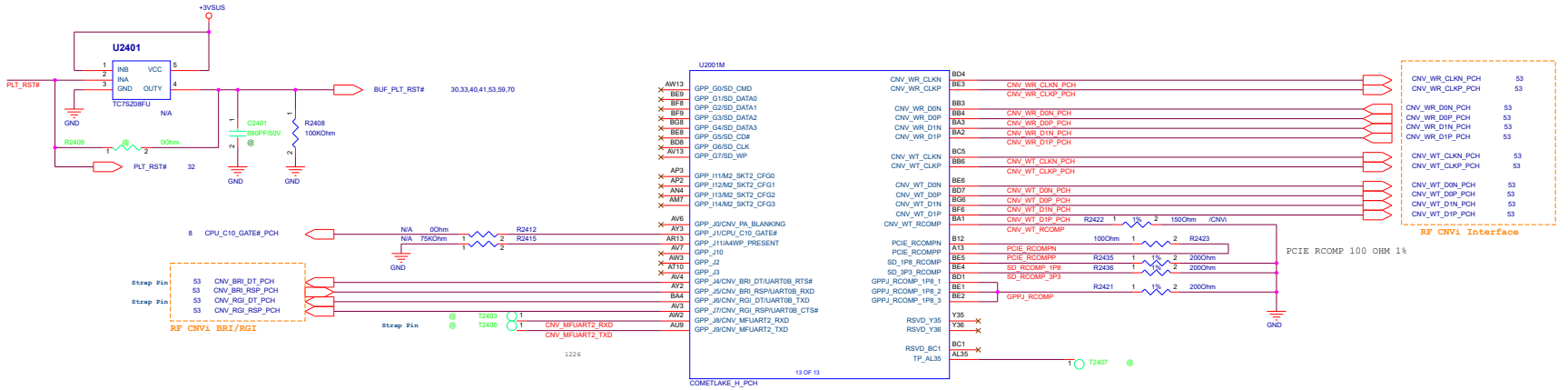
DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected

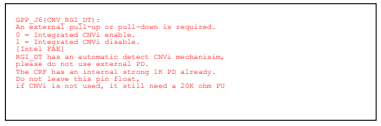


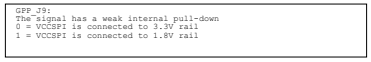
ASUS	Project Name: G512LI		Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 23 of 103		



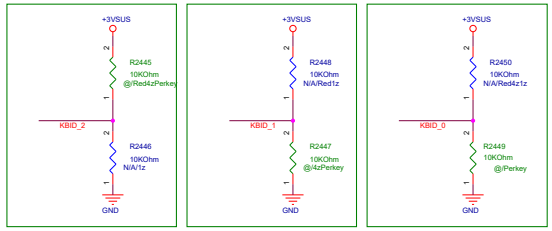






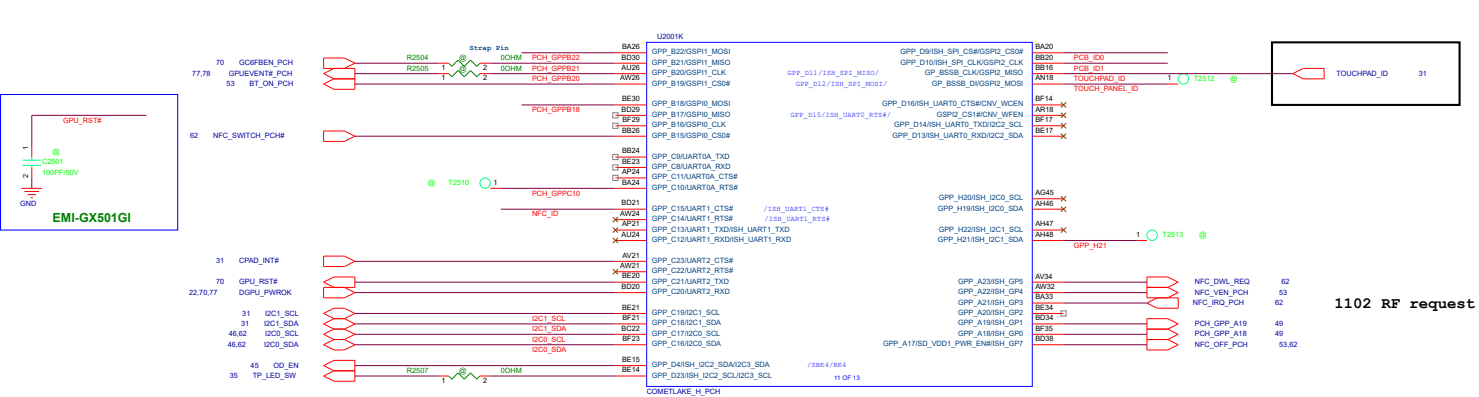


Keyboard ID

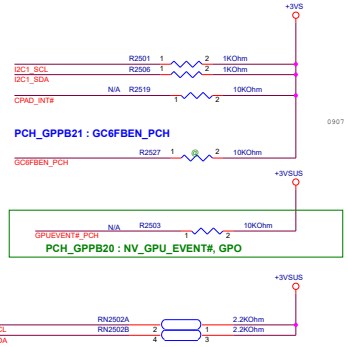


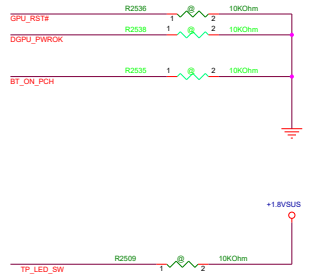
KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

ASUS	Project Name: G512LI		Rev: 1.0
Title :	PCH-CPT(5)_LPC,SPI,SMBUS		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 24 of 103		

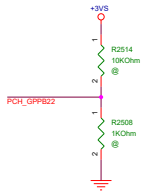


1102 RF request



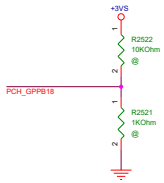


Boot BIOS Strap Bit BBS



PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

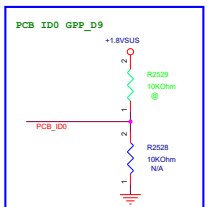
No Reboot



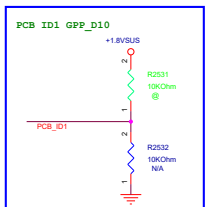
NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)

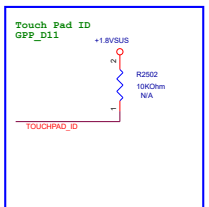
PCB ID0 GPP_D9



PCB ID1 GPP_D10

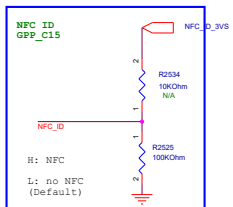


Touch Pad ID GPP_D11



Touch Panel ID GPP_D12

NFC ID GPP_C15



X-tal Frequency Select

Cannon Lake PCH-LP

- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Cannon Lake PCH-H

- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Project Name: G512LI			Rev: 1.0
Title: PCH-CPT(6)_GPIO,MISC			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 25 of 103		

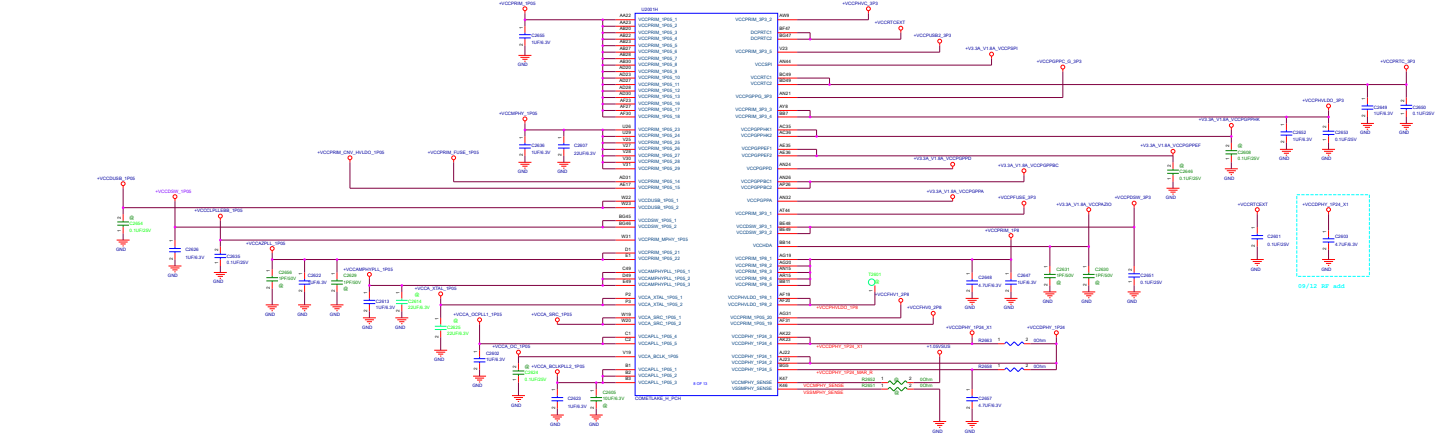
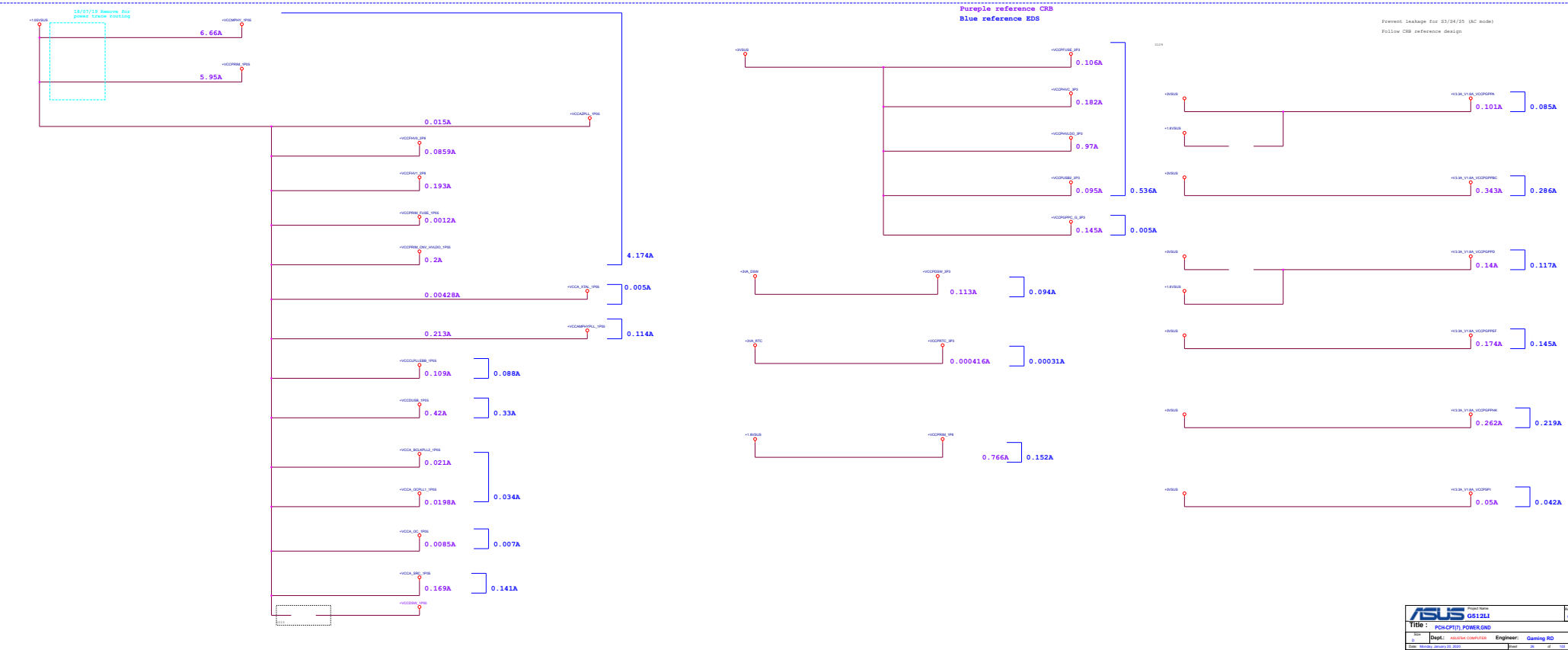


Table 8-1. Power Descriptions for PCH in CNL-H

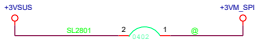
Name	Description
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	**1.8V or 3.3V for GPP_A group.**
VCCPGPPBC	**1.8V or 3.3V for GPP_B and GPP_C groups.**
VCCPGPPD	**1.8V or 3.3V for GPP_D group.**
VCCPGPPEF	**1.8V or 3.3V for GPP_E and GPP_F groups.**
VCCPGPPG_3P3	**3.3V for GPP_G group.**
VCCPGPPHK	**1.8V or 3.3V for GPP_H and GPP_K groups.**
VCCMPHY_SENSE	**1.05V Sense Line.**
VSSMPHY_SENSE	**0V (Ground) Sense Line.**
VSS	**Ground.**



ASUS	Project Name: G512LI		Rev: 1.0
Title :	PCH-CPT(7)_POWER,GND		
Size: D	Dept.: MB/BM,COMPUTER	Engineer: Gaming RD	
Date: Monday, January 06, 2020	Sheet 29 of 109		

ASUS	Project Name: G512LI	Rev: 1.0
Title :	PCH-CPT(8)_POWER,GND	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 27 of 103	

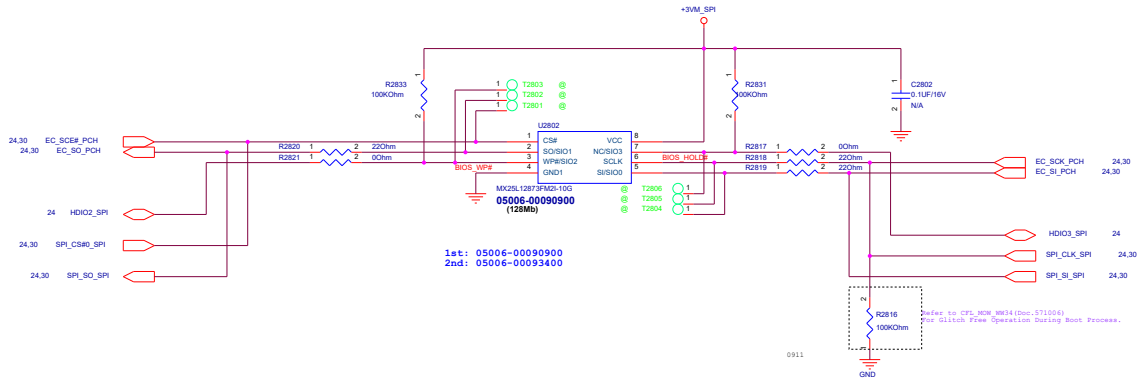
SPI Power



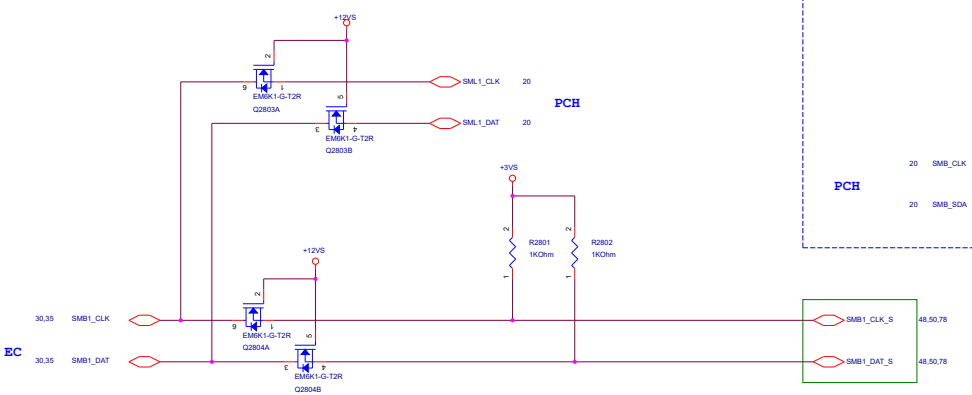
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

Main Board



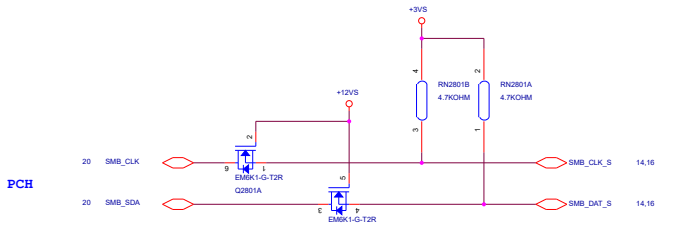
System Management Interface

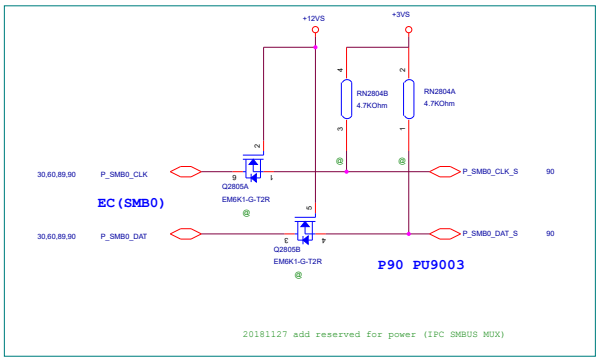


R0.1-13 R1.0-01

CPU,VGA Thermal Sensor
Power Thermal Sensor

SMBus Interface





ASUS	Project Name: G512LI		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020		Sheet 28 of 103	

ASUS	Project Name: G512LI	Rev: 1.0
Title : PCH-XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 29 of 103	

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT5125VG-128/CX	06037-00370000

Power

R1.0-29

+3VA_EC, +3VPLL, SL3005, C3051 0.1UF/16V, C3052 0.1UF/16V, C3053 0.1UF/16V, C3054 0.1UF/16V, C3004 0.1UF/16V N/A, C3005 0.1UF/16V N/A, C3007 0.1UF/16V N/A

+3VS_AUD_DVDD, EM6K1-G-T2R Q3003B, EM6K1-G-T2R Q3003A, EC_GPA7, EAPD# 36,37

2017.03.21 AMP Change SNL04M25555

+3VS, 0.1UF/16V C3002 N/A, +3VA_EC, +3VPLL, +3VACC, LCD_BACKOFF# 45

U3001

N key

ADP_INSERT_NG# R3016 0Ohm N/A, NVDD_SMB_SEL R3002 10KOhm

Battery

Thermal sensor

IT5125VG-128/CX
06037-00370000

EMI-GX501GI

C3003 100PF/50V EC_RST#
C3009 @EMI 100PF/50V BUF_PLT_RST#
C3011 @EMI 100PF/50V RC_IN#
C3012 @EMI 100PF/50V 3VA_DSW_PWRGD_EC
C3013 @EMI 100PF/50V 3VSUS_PWRGD
C3014 @EMI 100PF/50V 3VA_DSW_PWRGD
GND

C3018 8.2PF/50V CLK_KBCPCI_PCH
C3010 0.01UF/25V PWR_SW#

For EMI

C3025 100PF/50V CHG_FULL_LED#
C3026 100PF/50V PWR_LED
C3027 100PF/50V CHG_LED#
C3028 100PF/50V MEMS_PRESENT
@EMI

R1.0-34

+3VA_DSW, R3055 100KOhm, 3VA_DSW_PWRGD
+3VS, R3054 100KOhm, IMVP8_PWRGD
SL3011, 3VA_DSW_PWRGD_EC, 3VA_DSW_PWRGD 20,58,87

C3008 0.1UF/16V N/A, C3015 0.1UF/16V N/A, +3VA_EC, +3VACC, SL3006, EC_GAND 單點下地, GND

C3019 @EMC 0.1UF/25V, PM_PWROK, GND

SUSWARN#
P_IMVP8_PSYS_INFO
待確認

PU/PD

PWR_SW# R3037 100KOhm
AC_IN_OC# R3026 100KOhm
LID_SW# R3063 100KOhm
EC_GPG2 R3023 100KOhm
THRO_CPU# R3032 10KOhm
NKey_WRST R3013 N/A 10KOhm, R3050 10KOhm N/A

CHG_LED# R3043 10KOhm
CHG_FULL_LED# R3044 10KOhm
EC_GPA7 R3027 100KOhm
EC_GPG2 R3021 100KOhm
ADP_INSERT_NG# R3017 100KOhm
SMB1_DAT RN3001A 4.7KOHM
SMB1_CLK RN3003B 4.7KOHM
P_SMB0_CLK RN3003A 4.7KOHM
P_SMB0_DAT
SMB3_DAT RN3002B 4.7KOHM
SMB3_CLK RN3002A 4.7KOHM
PD_I2C_INT_EC R3007 100KOhm

3VADSW_ON R3053 100KOhm
5VSUS_ON R3006 100KOhm, R3056 1MOHM
VSUS_ON R3051 100KOhm, R3030 1MOHM

for load code

TP_DAT RN3004A 4.7KOHM
TP_CLK RN3004B 4.7KOHM

teknisi indonesia

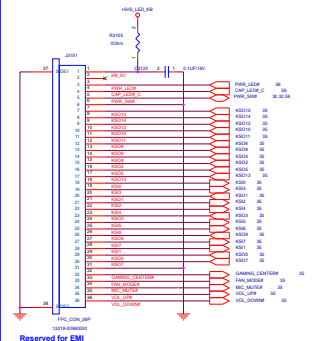
PM_PWRBTN# R3041 10KOhm
RC_IN# R3003 10KOhm N/A

N501
BAT1_IN_OC# R3065 100KOhm
R3008 100KOhm
PM_SLP_SUS# R3019 100KOhm
PM_SUSC# R3004 100KOhm
PM_SUSB# R3005 100KOhm
SUSB_EC# R3092 4.7KOhm
SUSC_EC# R3001 4.7KOhm
WLAN_PWR_EN R3015 100KOhm
PM_RSMRST# R3058 10KOhm
PM_SYSPWROK R3022 100PF/50V
DPWROK_EC C3023 100PF/50V
3VADSW_ON C3001 15PF/25V
GC_STATE_EC R3039 100KOhm

<Variant Name>

ASUSTeK COMPUTER
Title : CR_KBC_IT8521
Engineer: Gaming RD
Size C | Project Name G512LI | Rev 1.0
Date: Monday, January 20, 2020 | Sheet 30 of 103

Keyboard Connector



Reserved for EMI

Keyboard Backlight

20190813
Delete 4Zone & Red connector

4Zone

1Zone

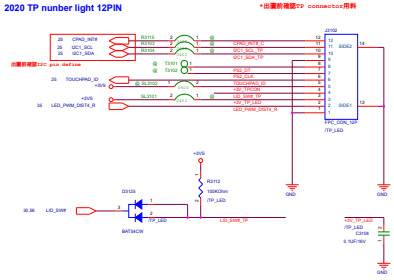
Red

Touch Pad Connector

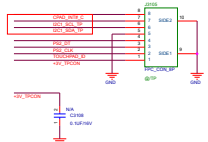
2020 TP nunber light 12PIN

*出圖前確認FPC connector用料

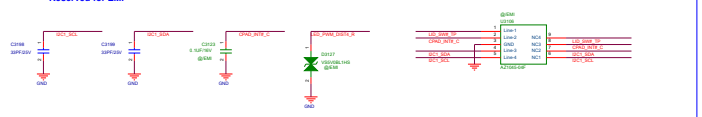
出圖前確認FPC pin define



SA555D-2400 8PIN(Normal TP)

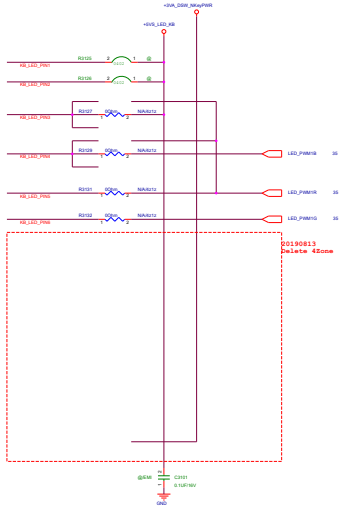


Reserved for EMI

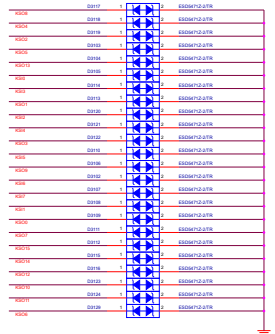


1zone

20190813
Delete 4Zone



For EMI



	RED-4pin	1zone RGB_8pin	4zone-16pin	per key-20pin
pin1	VCC	VCC green	VCC green	COM7
pin2	VCC	VCC red	VCC red	COM6
pin3	GND	VCC blue	VCC blue	COM5
pin4	GND	LED1 blue	LED1 blue	COM4
pin5		LED1 red	LED1 red	COM3
pin6		LED1 green	LED1 green	COM2
pin7		NC	LED2 blue	COM1
pin8		NC	LED2 red	COM0
pin9			LED2 green	GND
pin10			LED3 blue	GND
pin11			LED3 red	GND
pin12			LED3 green	VCC
pin13			LED4 blue	VCC
pin14			LED4 red	VCC
pin15			LED4 green	VDD-33
pin16			NC	NC
pin17				GCLK
pin18				SDI
pin19				DCLK
pin20				LE

G531GT P.31 差異

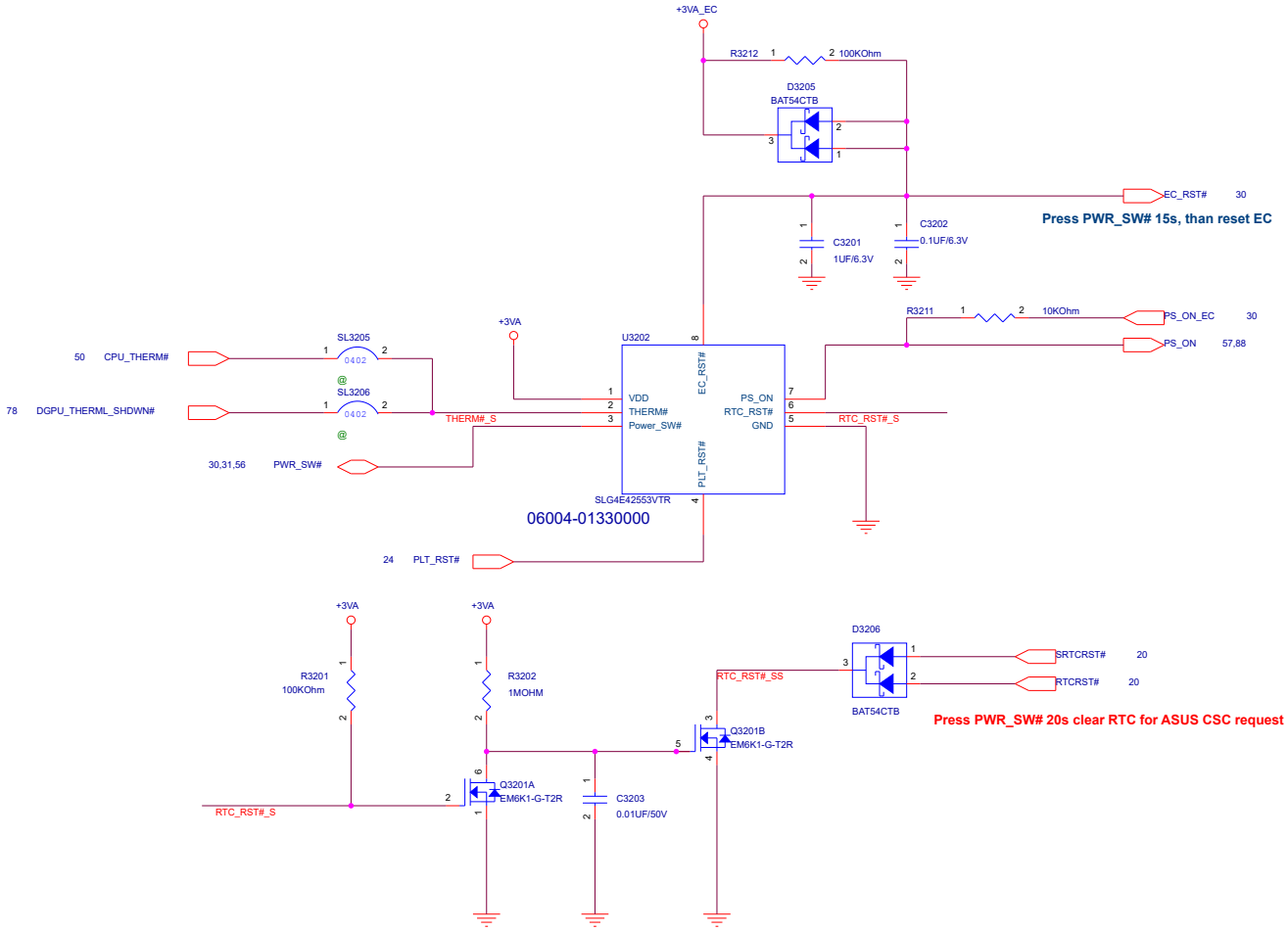
MP 60 PN	PCB	J3102	J3105	C3104	D3125	R3112
60NR01L0-MB3010	R1.4	12018-00102300	NA	11G232110411360	07G004069020	10G212100314010
60NR01L0-MB3210	R1.4	12018-00102300	NA	11G232110411360	07G004069021	10G-02147483648
60NR01L0-MB3310	R1.4	NA	12018-00212200	NA	NA	NA
60NR01L0-MB3410	R1.4	NA	12018-00212200	NA	NA	NA
60NR01L0-MB3110	R1.4	NA	12018-00212200	NA	NA	NA

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

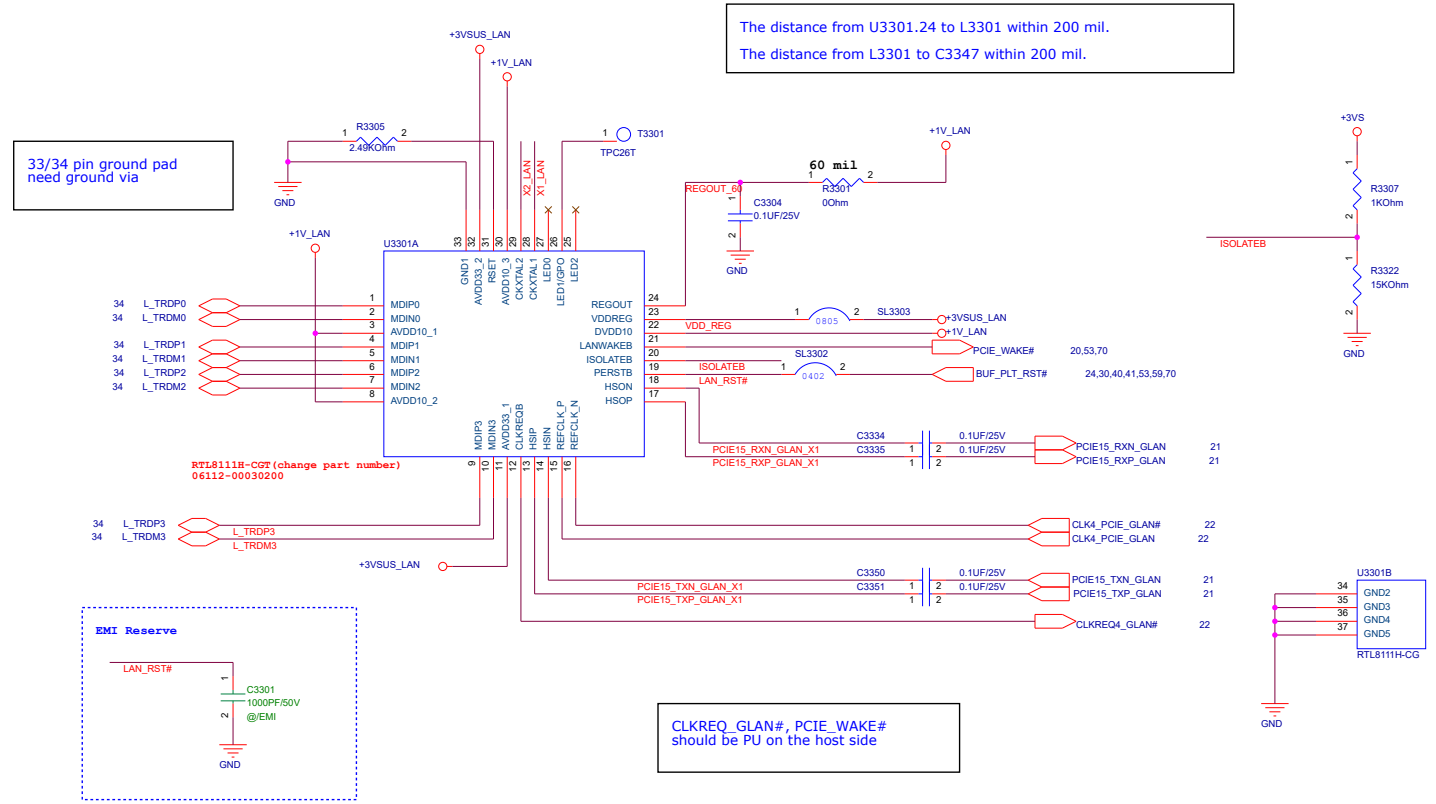
https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

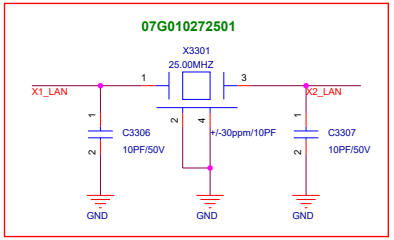
UX362FA R1.3 board will verify this circuit 7/E



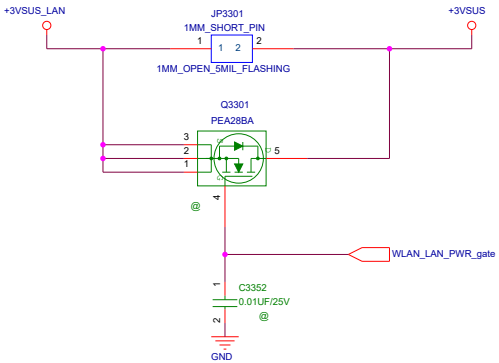
<Variant Name>

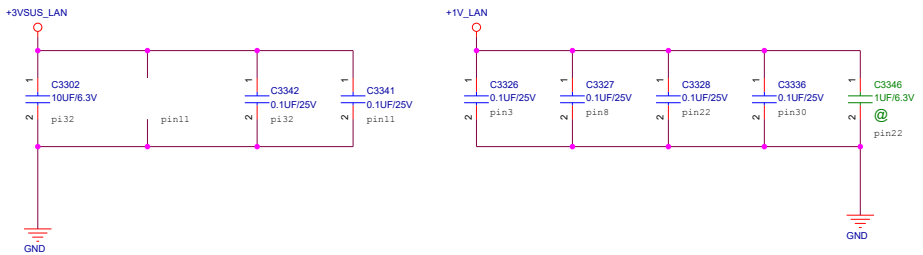
ASUSTeK COMPUTER	Title : RST_Reset Circuit	
	Engineer: Gaming RD	
Size: B	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 32 of 103	





Realtek suggests 3V_LAN raise time >1ms

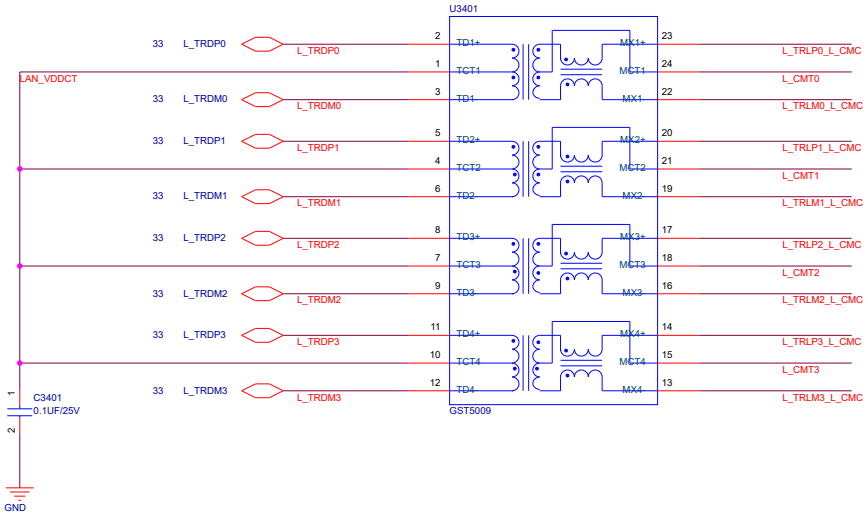


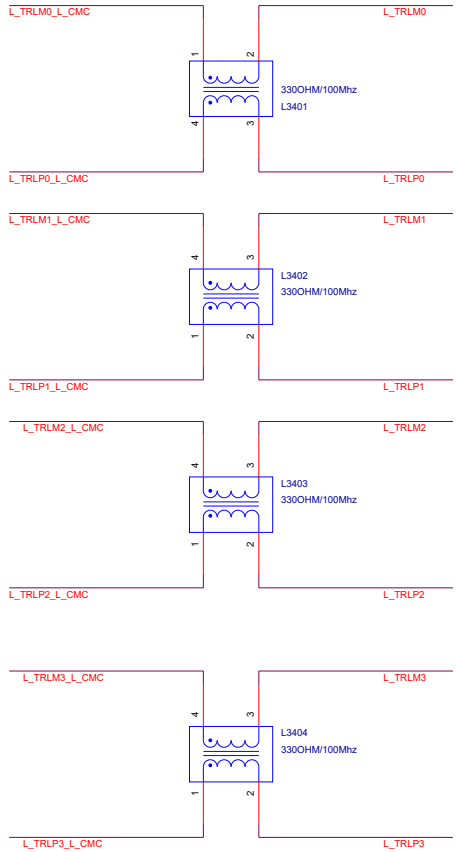


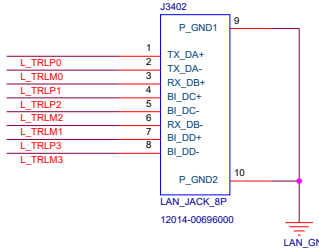
Project Name: G512LI			Rev: 1.0
Title: LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Monday, January 20, 2020	Sheet 33 of 103		

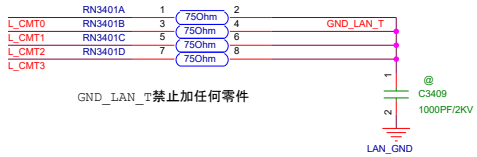
Main Board

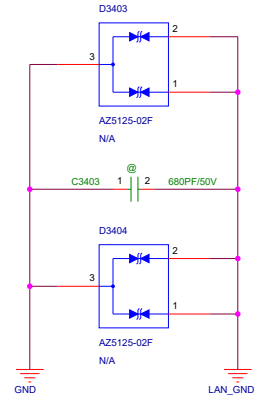
LAN Connector



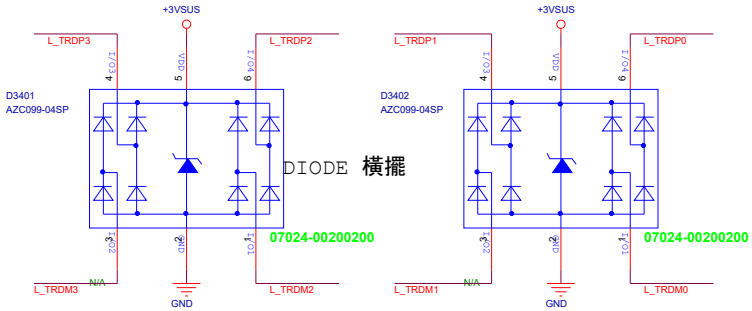








Place near chassis GND



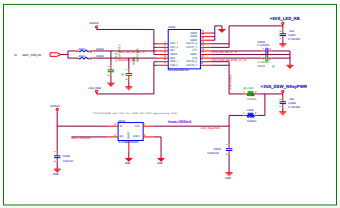
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

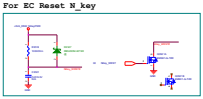
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: G512LI		Rev: 1.0
Title : LAN_RJ45_CON			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Monday, January 20, 2020	Sheet 34 of 103		

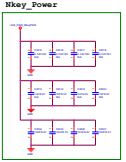
N_KEY_IT8299E



For EC Reset N_key



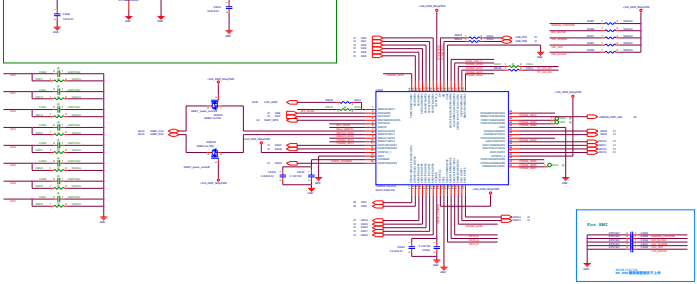
Nkey_Power



G531GW P.35 變異

WP 42 20	PCB	0.1419
498B0112-WB3510	R1.4	1-5021210310140L0
498B0112-WB3210	R1.4	1-5021210310140L0
498B0112-WB3310	R1.4	NA
498B0112-WB3410	R1.4	NA
498B0112-WB3110	R1.4	NA

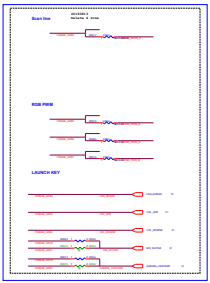
IT8299E



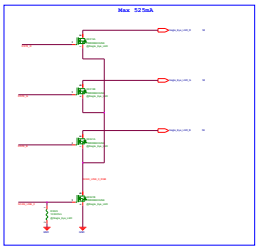
N-KEY Debug Connector

Debug Connector MP Remove

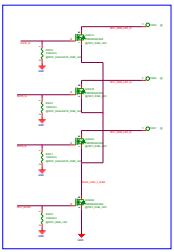
KB RGB co-layout



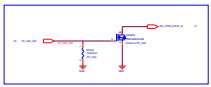
Eagle Eye LED



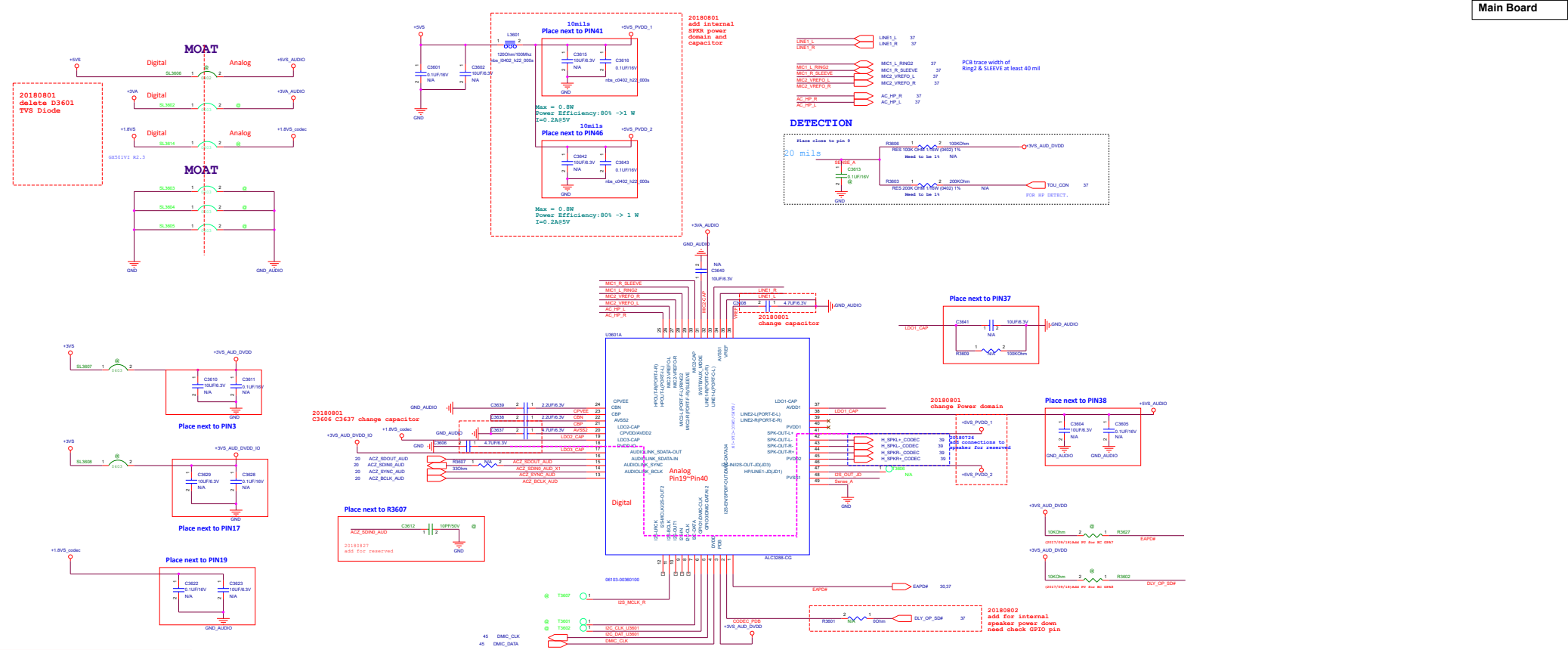
NFC RGB LED

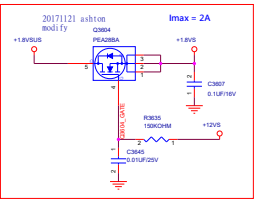


TP LED



KB RGB 1Zone LED





DVDD must lead AVDD2. Figure 4 illustrates the recommended power sequence.

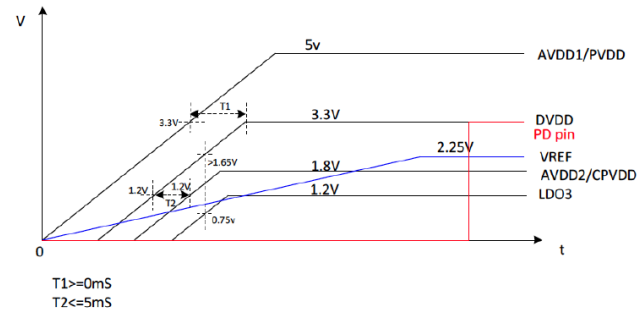
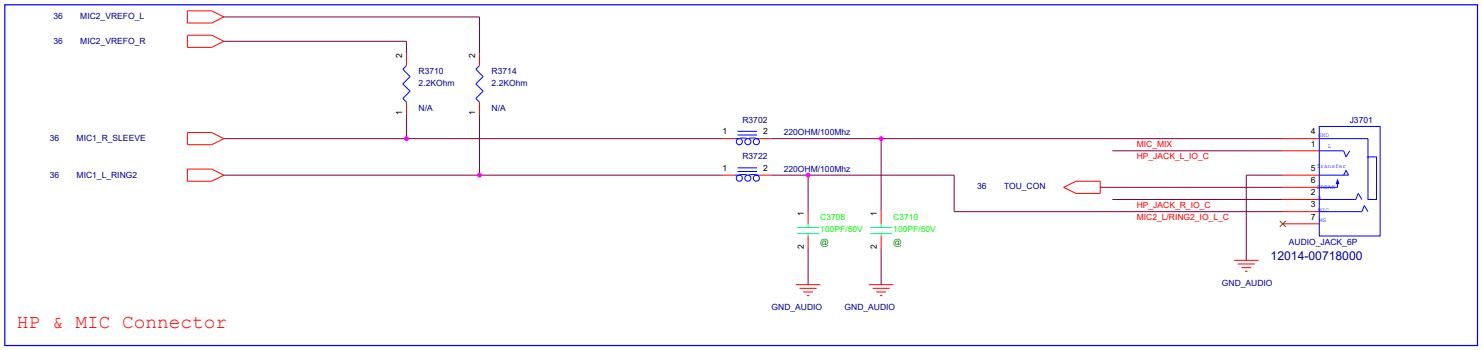
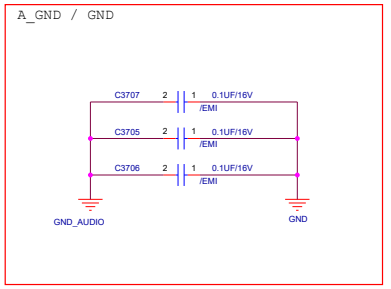


Figure 4. Power sequence

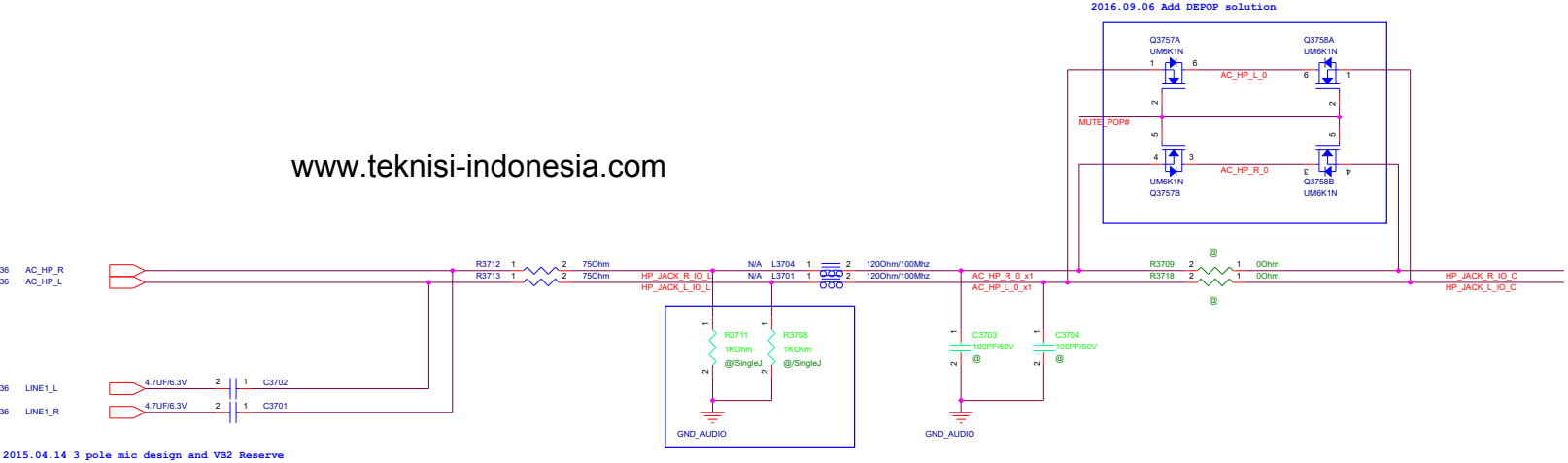
ASUS	Project Name: G512LI		Rev: 1.0
Title :	AUDIO ALC3236-CG/VB2		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Monday, January 20, 2020	Sheet: 36	of: 103	

Headphone&MIC





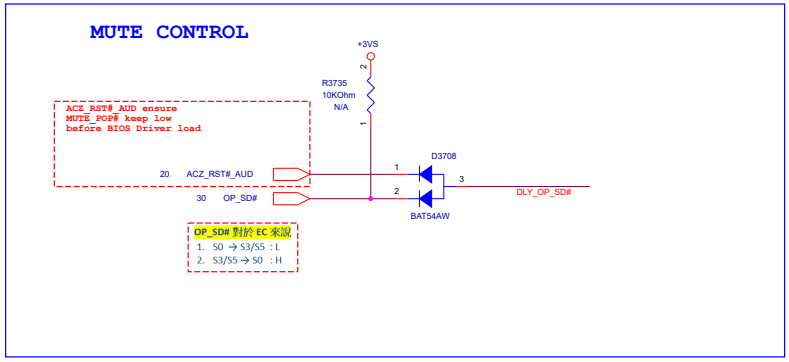
2016.09.06 Add DEPOP solution



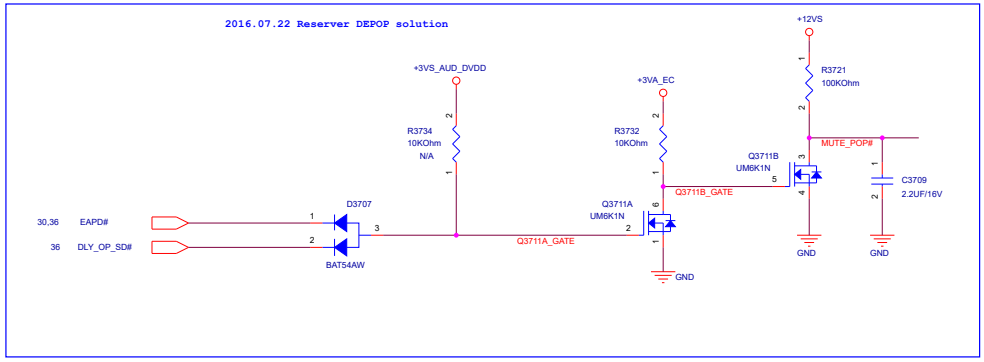
2015.04.14 3 pole mic design and VB2 Reserve

2015.08.07 Realtek Suggest

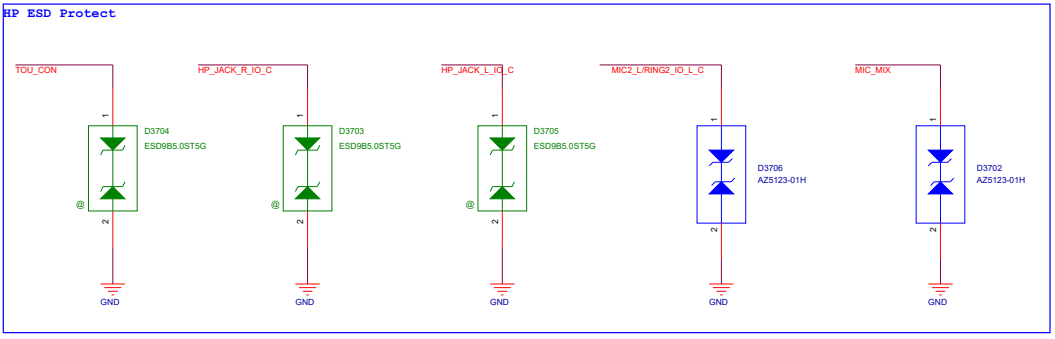
MUTE CONTROL



2016.07.22 Reserver DEPOP solution



HP ESD Protect



Project Name: G512LI		Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li
Date: Monday, January 20, 2020	Sheet 37 of 103	

20180801
delete 0ohm

36 H_SPKR+_CODEC
36 H_SPKR-_CODEC
36 H_SPKL+_CODEC
36 H_SPKL-_CODEC

L3901 1 2 220Ohm/100MHz
L3902 1 2 220Ohm/100MHz
L3903 1 2 220Ohm/100MHz
L3904 1 2 220Ohm/100MHz

Max = 2W / Channel (@PVDD=5V)
I = 0.55A (@Speaker : 7.4 Ohm(+-10%))

H_SPKR+_CON
C3948 2200PF/50V
GND
C3950 2200PF/50V
H_SPKR-_CON
H_SPKL+_CON
C3951 2200PF/50V
GND
C3953 2200PF/50V
H_SPKL-_CON

D3901 @EMC H_SPKR+_CON
D3902 @EMC H_SPKR-_CON
D3903 @EMC H_SPKL-_CON
D3904 @EMC H_SPKL+_CON
ESD9B5.0ST5G
GND

INTERNAL SPK Conn.

Speaker = 1.5W / channel

Check Pin1

J3901
H_SPKR+_CON
H_SPKR-_CON
H_SPKL-_CON
H_SPKL+_CON
SIDE2
SIDE1
WTOB_CON_4P
12017-00072500
GND

1113 change connector

<Variant Name>

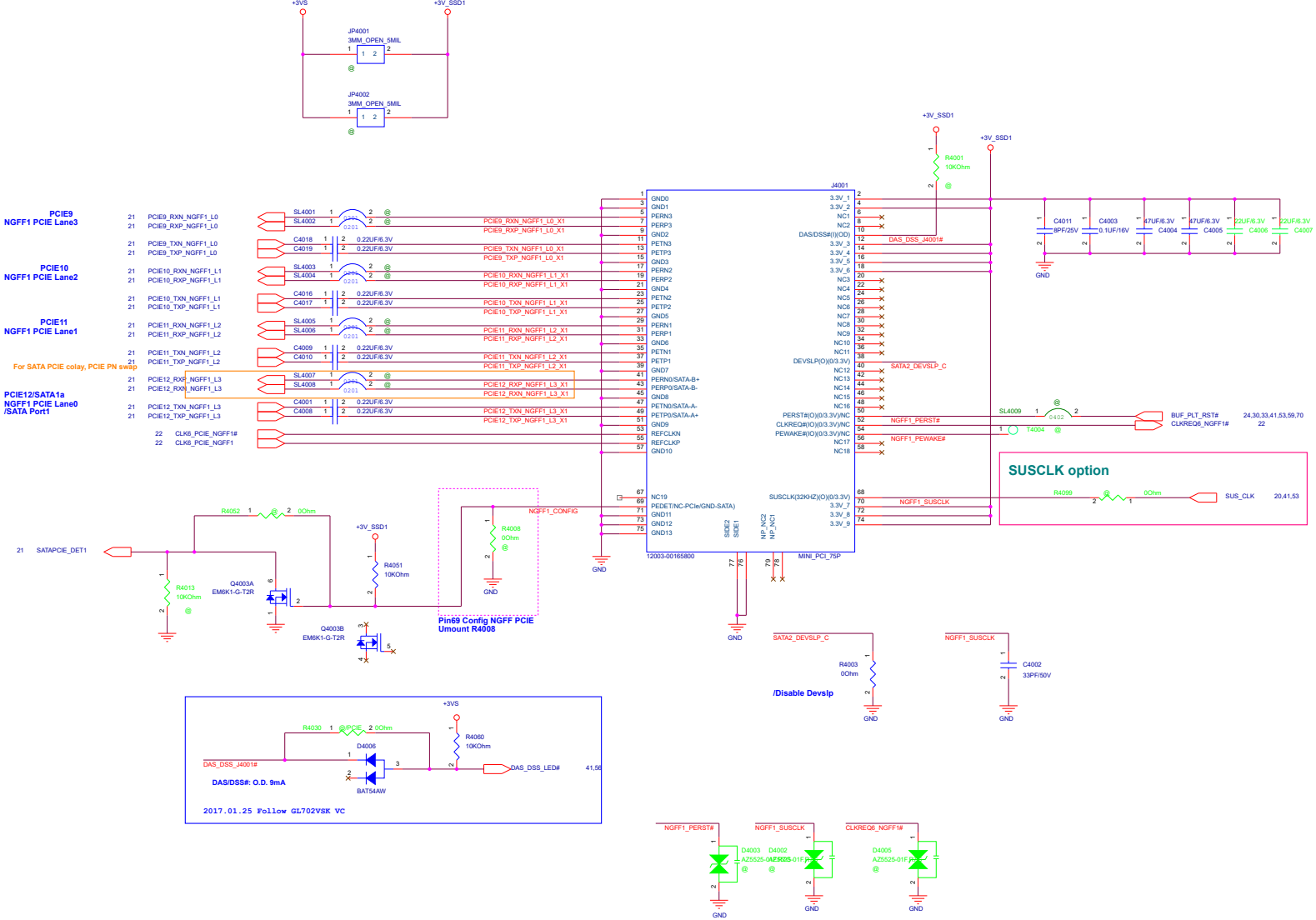
ASUSTeK COMPUTER INC. NB1

Title : Aud_Woofer_**
Engineer: EE

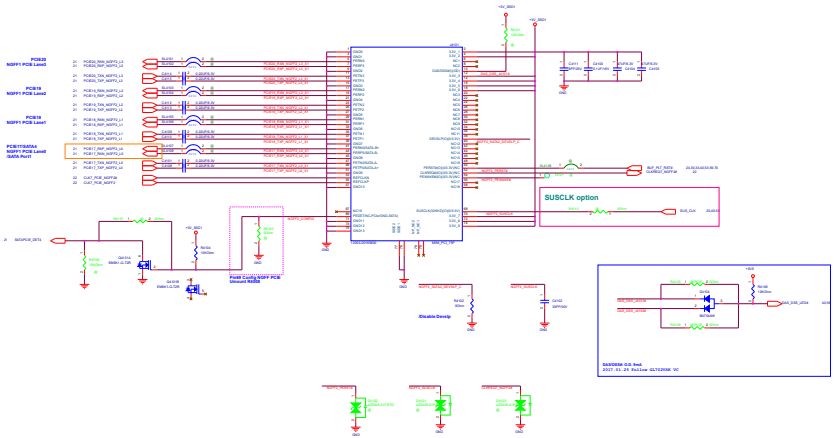
Size	Project Name	Rev
B	G512LI	1.0

Date: Monday, January 20, 2020 Sheet 39 of 103

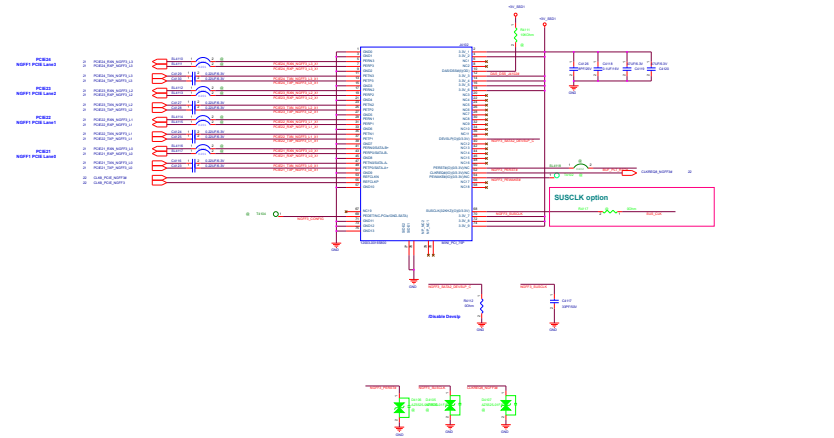
NGFF_SSD1


PCIE9
NGFF1 PCIE Lane3
PCIE10
NGFF1 PCIE Lane2
PCIE11
NGFF1 PCIE Lane1
For SATA PCIE colay, PCIE PN swap
PCIE12/SATA1a
NGFF1 PCIE Lane0
/SATA Port1
SUSCLK option
Pin69 Config NGFF PCIE
Umount R4008
/Disable Devslp
DAS/DSS#: O.D. 9mA
2017.01.25 Follow GL702VSK VC
12003-00165800
MINI_PCI_75P

NGFF_SSD2



NGFF_SSD3



ASUSTeK COMPUTER

Title : HDMI_DP_Switch

Engineer: Gaming RD

Size	Project Name	Rev
C	GS12LI	1.0

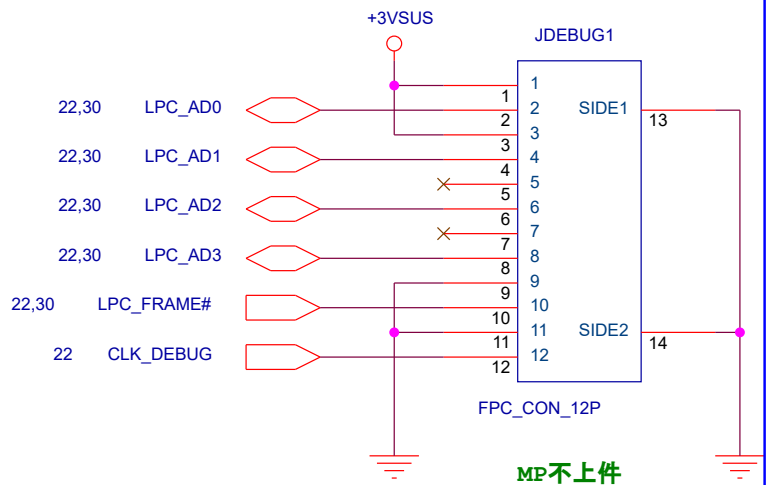
Date: Monday, January 20, 2020 Sheet 42 of 103

Main Board

ASUS	Project Name: G512LI	Rev: 1.0
Title : CB IO CON		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 43 of 103	

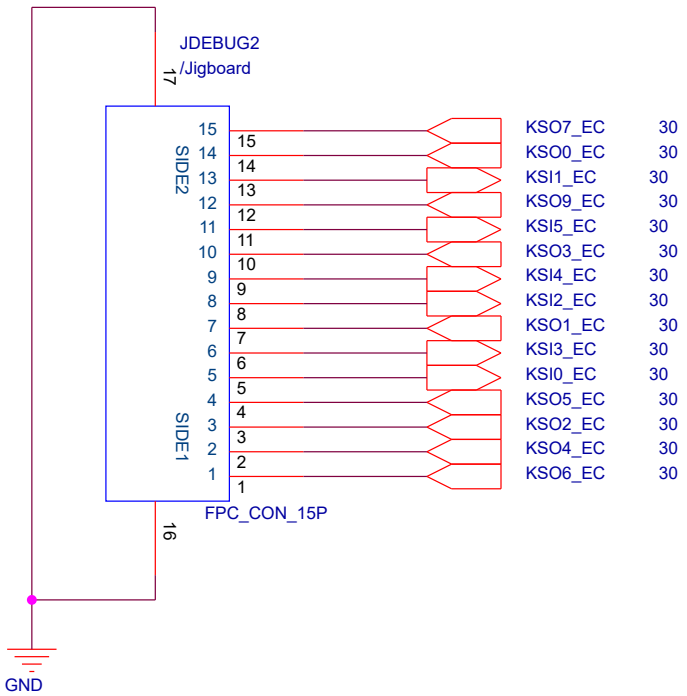
2017/11/10

LPC Debug Port



ER2 stuff

2017/11/10



<Variant Name>

ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: Gaming RD	
Size: A	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 44 of 103	

Imax=1port+1CC=3.6A

I2C Default Slave Address -> I2C_EC 0x42

Reserve to PCH

Connect to I2C ROM
Reserved for MUX I2C mode

MP remove

I2C ROM

EC

PD

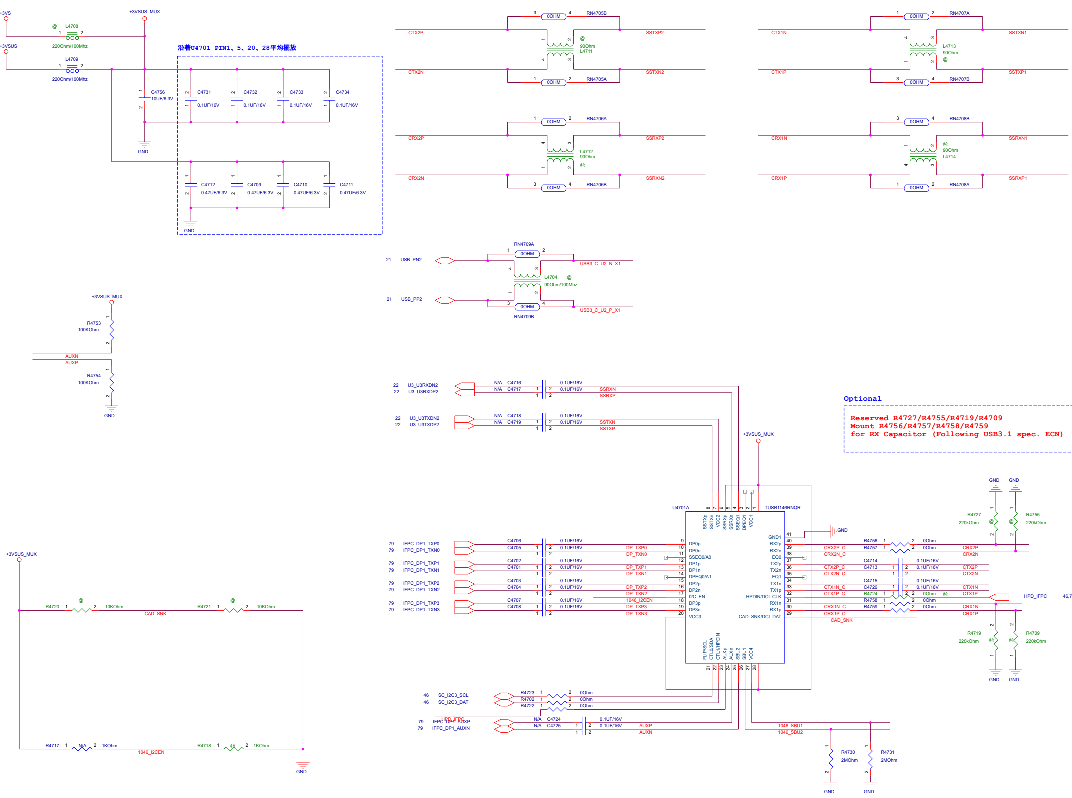
FW from PCH or APU

update I2C ROM to PD

Project Name: G512LI			Rev: 1.0
Title : PD_TPS65993AC			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP	
Date: Monday, January 20, 2020	Sheet 46 of 105		

USB EMI-Protection

TYPE-C USB3.1



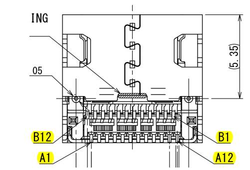
Optional

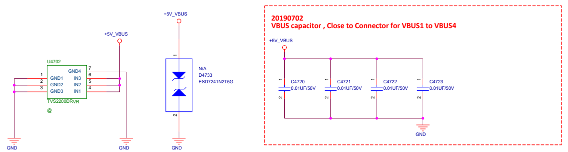
Reserved R4727/R4755/R4719/R4709
Mount R4756/R4757/R4758/R4759
for RX Capacitor (Following USB3.1 spec. ECN)

NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

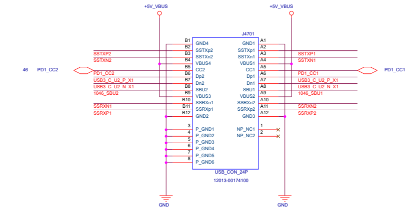
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.





TYPE-C Connector



USB ESD-Protection

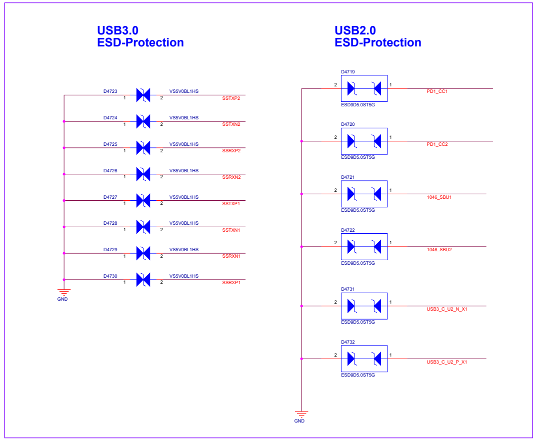


Table 2. GPIO Configuration Control

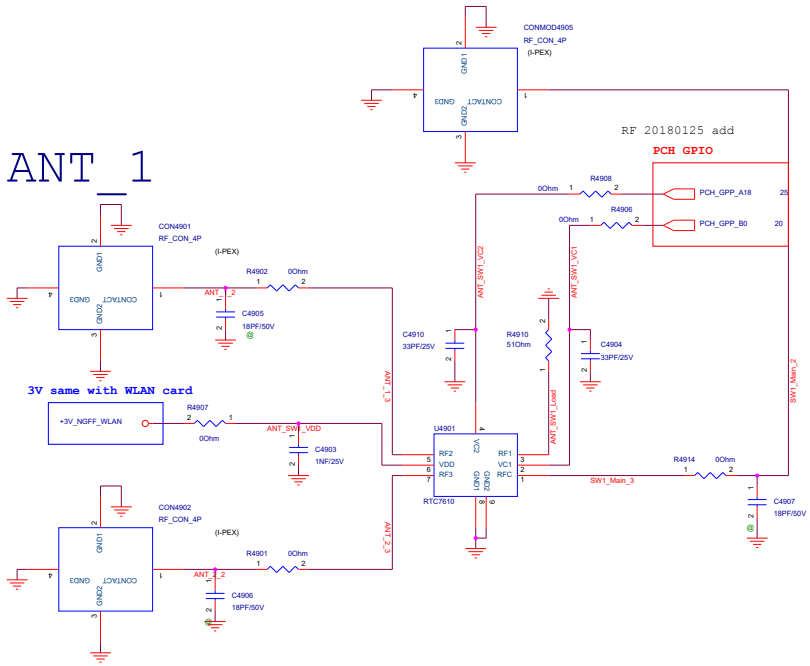
CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB1046A-DCI CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
L	H	H	One Port USB 3.1 – With Flip	—
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F

ASUS	Project Name: G512LI	Rev: 1.0
Title : USB3.1_TYPE-C_MUX_TI_1046A		
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP
Date: Monday, January 20, 2020	Sheet 47	of 105

AX201、9462NGW

WLAN Card	R5302	P49, All pages' components
AX201	unmount	mount
9462NGW	mount	unmount

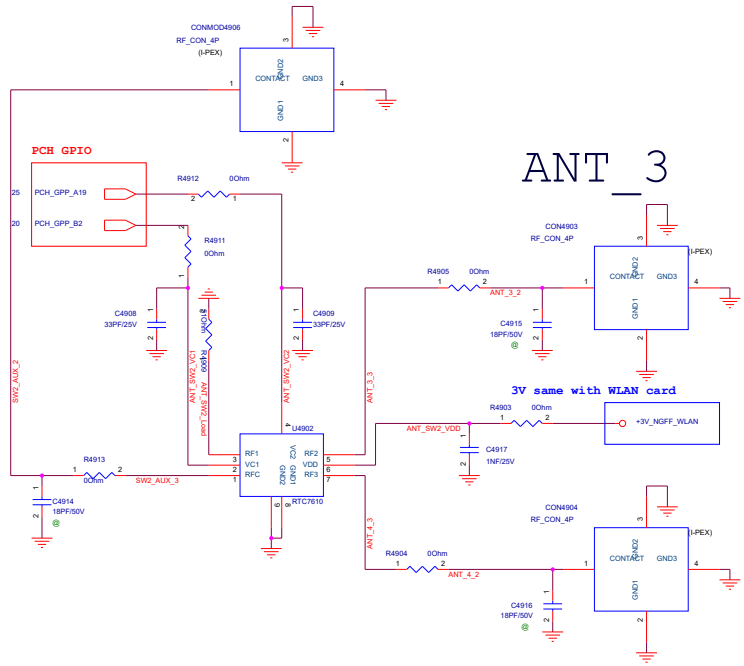
Module_AUX



U4901 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

Module_MAIN



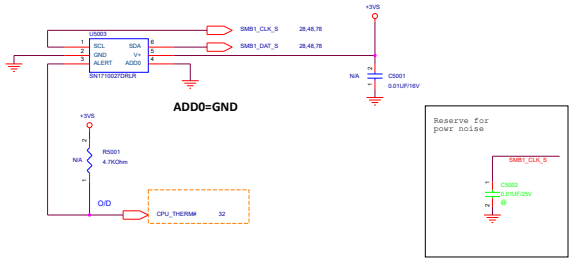
U4902 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

ASUS	Project Name: G512LI	Rev: 1.0
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Monday, January 20, 2020	Sheet 49 of 103	

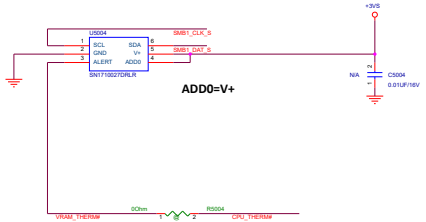
CPU Thermal Sensor



Near CPU

SMBUS addr=10010000 (90)

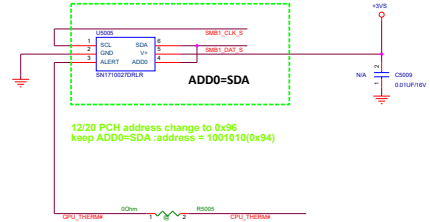
VRAM Thermal Sensor



Near VRAM

SMBUS addr=10010010 (92)

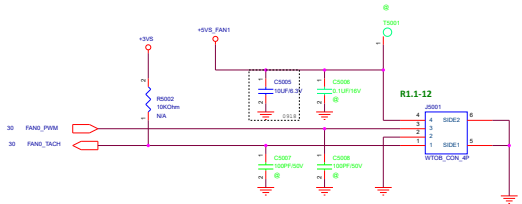
GPU



Near GPU

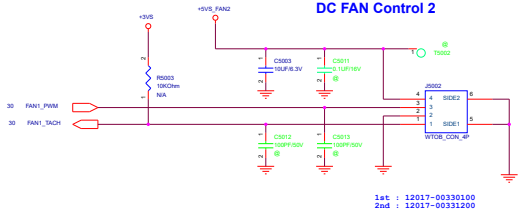
SMBUS addr=1001010 (94)

DC FAN Control 1



1st : 12017-00330100
2nd : 12017-00331200

DC FAN Control 2



1st : 12017-00330100
2nd : 12017-00331200

ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

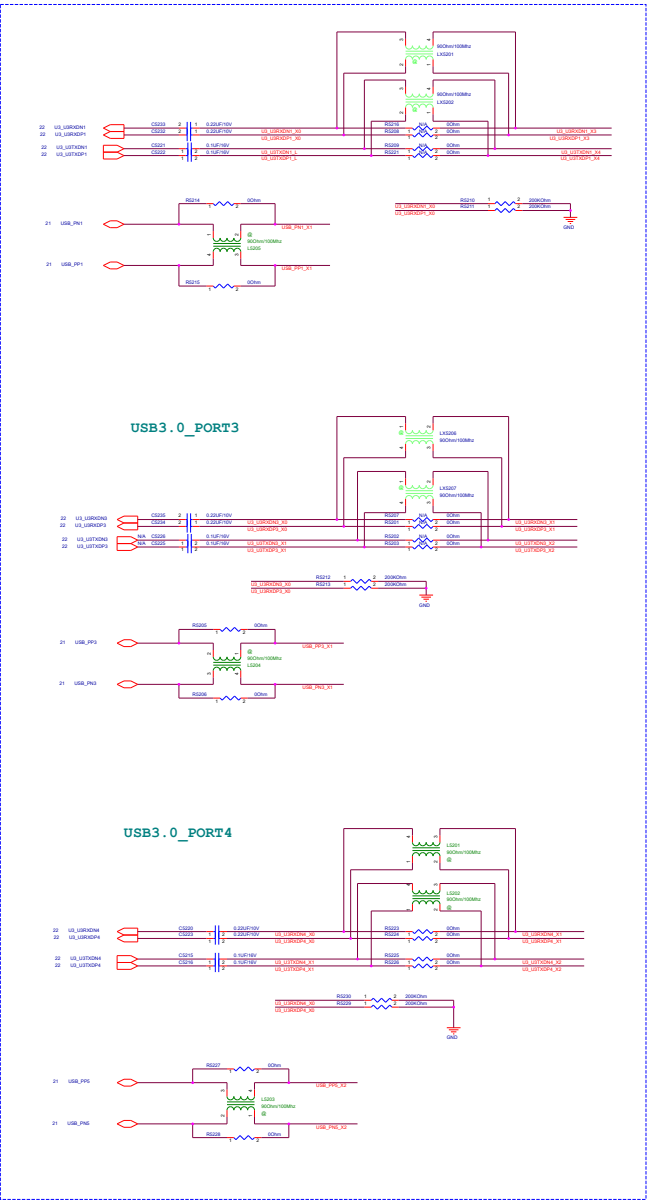
PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND

<Variant Name>

ASUSTeK COMPUTER	Title : XDD_HDD & ODD CON	
	Engineer: Gaming RD	
Size: A	Project Name: G512LI	Rev: R1.0
Date: Monday, January 20, 2020	Sheet 51 of 103	

USB3.0 EMI-Protection

09G092090400



USB3.0_PORT3

USB3.0_PORT4

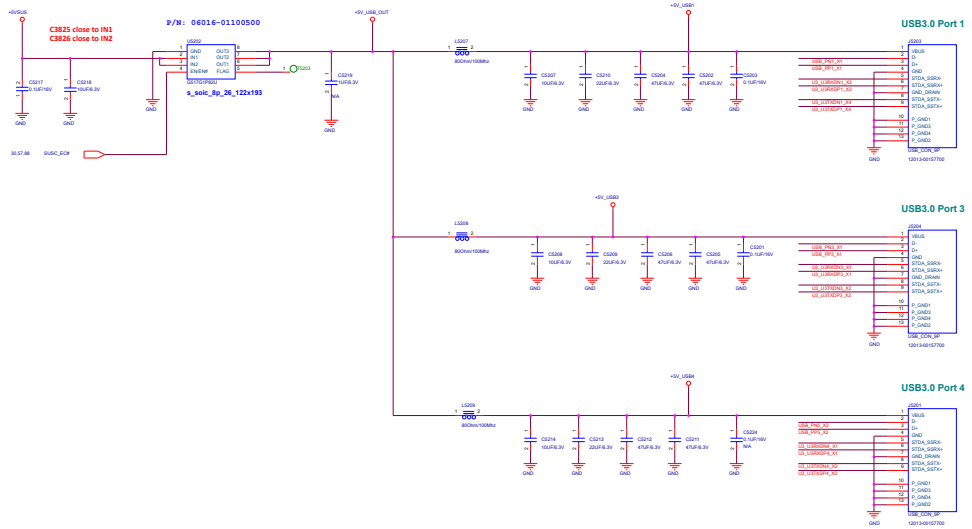
Notice:
US202要注意Footprint
s_soic_8p_26_122x193(使用此Footprint)
s_soic_8p_26_122x193_ns(No MASK, PIN脚未露铜, 不可使用)

J5201 USB3.0 Connector
1st Source: P/N:12013-00018300 FOXCONN/UEA1111-N40AM2-7H
2nd Source: P/N:12013-00080400 SINGATRON/2UB4006-310101F

C3825 close to IN1
C3826 close to IN2

P/N: 06016-01100500

s_soic_8p_26_122x193



USB2.0 ESD-Protection

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

USB3.0 Pin define	
1	VBUS
2	D-
3	D+
4	GND
5	RX-
6	RX+
7	GND
8	TX-
9	TX+

USB3.0 ESD-Protection

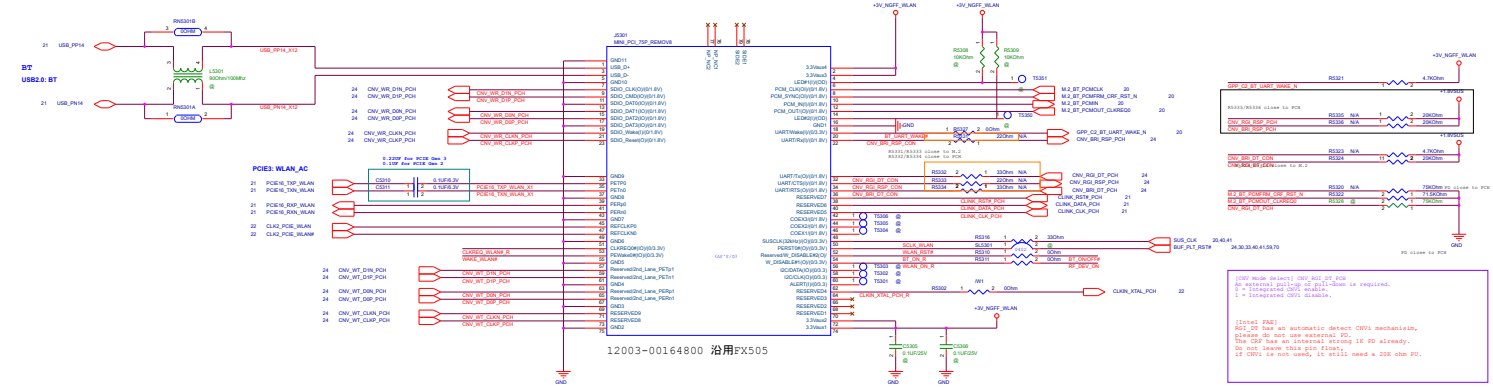
1st : 07G028076030 ESD PROTECTION AZ1045-04F
2nd : 07G028153010 ESD PROTECTION IP4284CZ10-TB

Title :	USB Charger		
Engineer:	Gaming RD		
Size	Project Name		Rev
D	G512LI		1.0
Date:	Monday, January 20, 2020	Sheet	52 of 59

R1.1-02

Main Board

NGFF M.2 TYPE_E-KEY WIFI



J5301_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

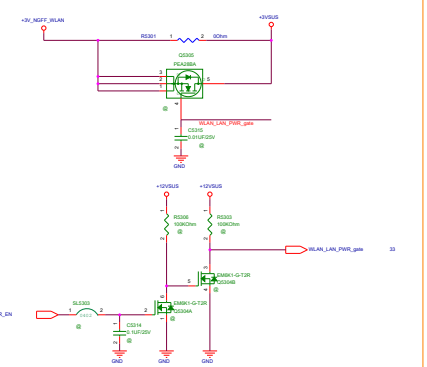
2nd Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FFB

3rd Source: P/N:12003-00075800 LOTES/APCI0062-P001A

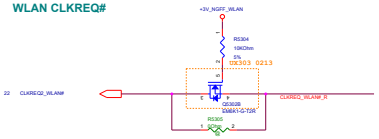
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

WLAN PWR to +3VSUS

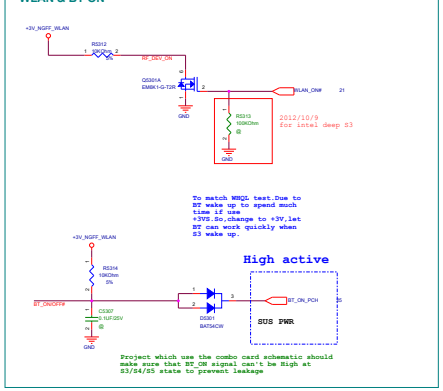


WLAN CLKREQ#

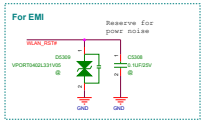


WLAN_Wake# Control

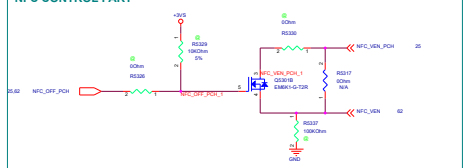
WLAN & BT ON



For EMI



NFC CONTROL PART



<Variant Name>

Title : IO Con. to MB

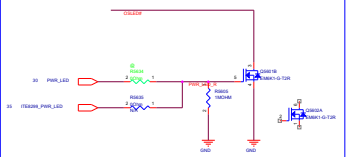
ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
Custom	**G512LI**	1.0

Date:	Monday, January 20, 2020	Sheet	55	of	103

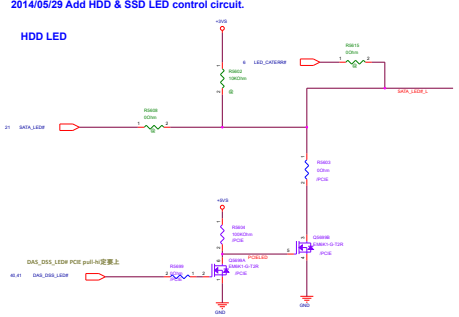
OS LED



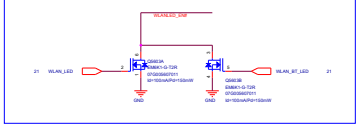
Charger LED

2014/05/29 Add HDD & SSD LED control circuit.

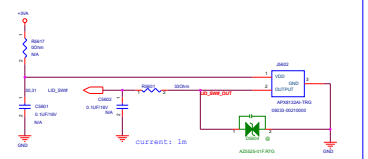
HDD LED



BT/WLAN LED

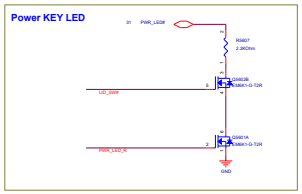


HALL SENSOR

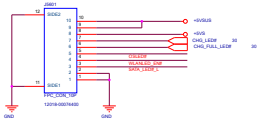


CAP LED

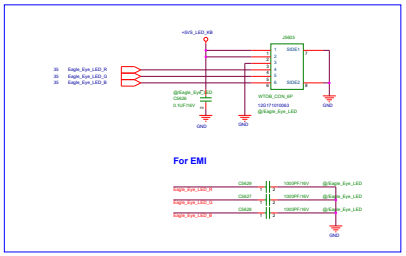
Power KEY LED



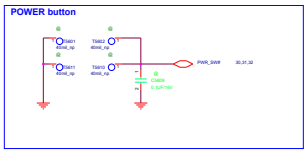
LED Board



Eagle Eye LED Conn

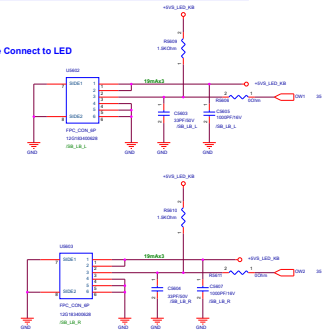


POWER button



2017.03.17 EMI Reserve

One-wire Connect to LED



G531GT P.56 差異

MP 60 PN	PCB	U5602/U5603	C5603/C5604/C5605/C5607
60NR01L0-MB3010	R1.4	12G183400628	11G232110211030
60NR01L0-MB3210	R1.4	12G183400628	11G232110211030
60NR01L0-MB3310	R1.4	12G183400628	11G232110211030
60NR01L0-MB3410	R1.4	12G183400628	11G232110211030
60NR01L0-MB3110	R1.4	NA	NA

<Standard Number>

ASUSTeK COMPUTER

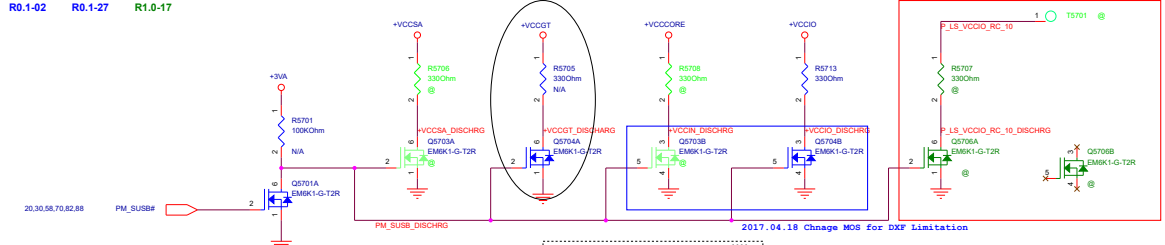
Title : LED & LID

Engineer: Gaming RD

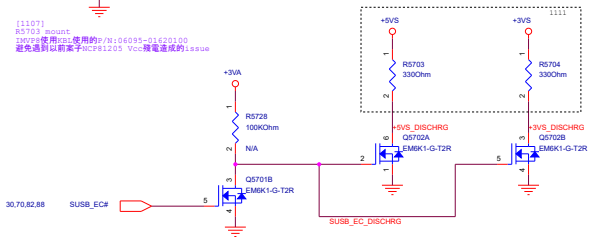
Size	Project Name	Rev
D	G512LI	1.0

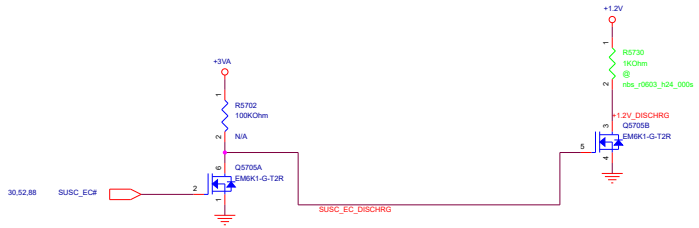
Date: Monday, January 20, 2020 Sheet 56 of 106

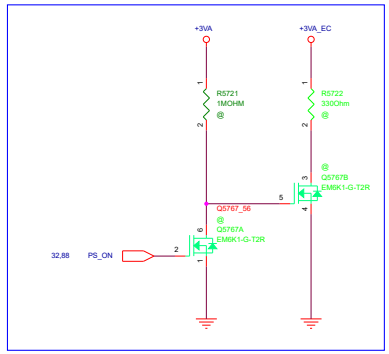
R0.1-02 R0.1-27 R1.0-17

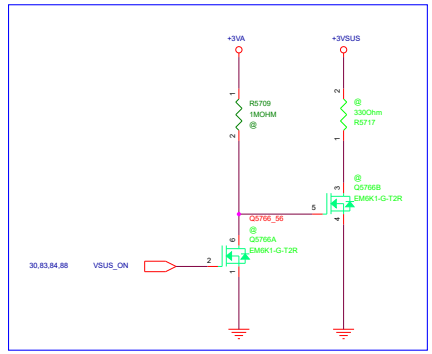


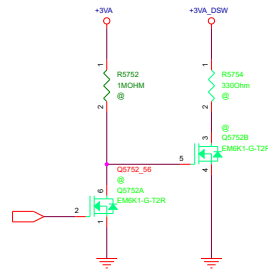
[1107]
R5703 mount
IMVP8使用KBL使用的P/N:06095-01620100
避免遇到以前率子NCP81205 Vcc殘電造成的issue

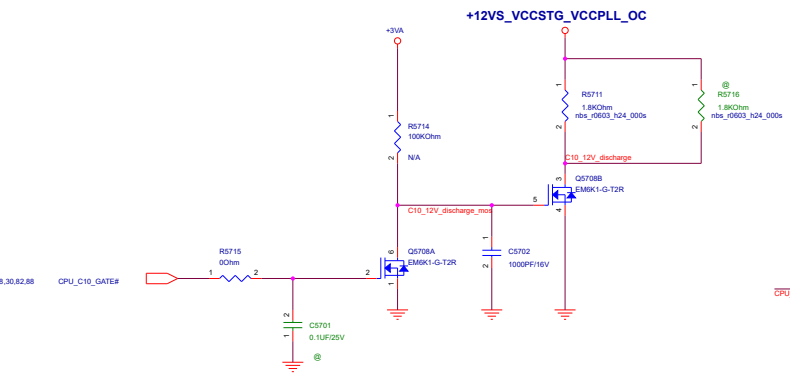


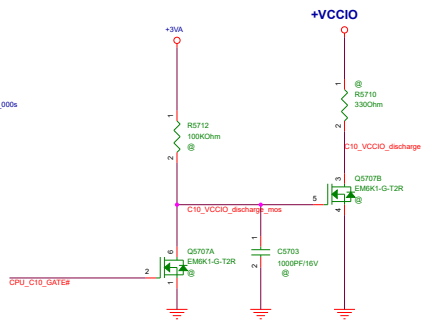


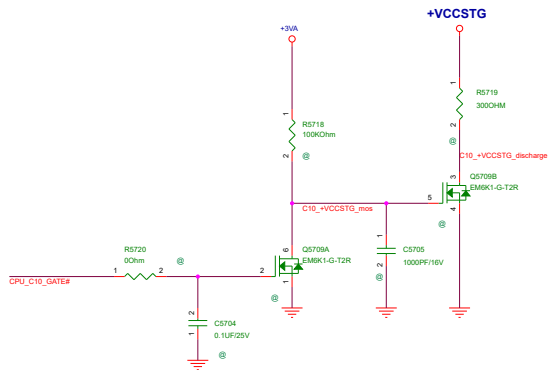






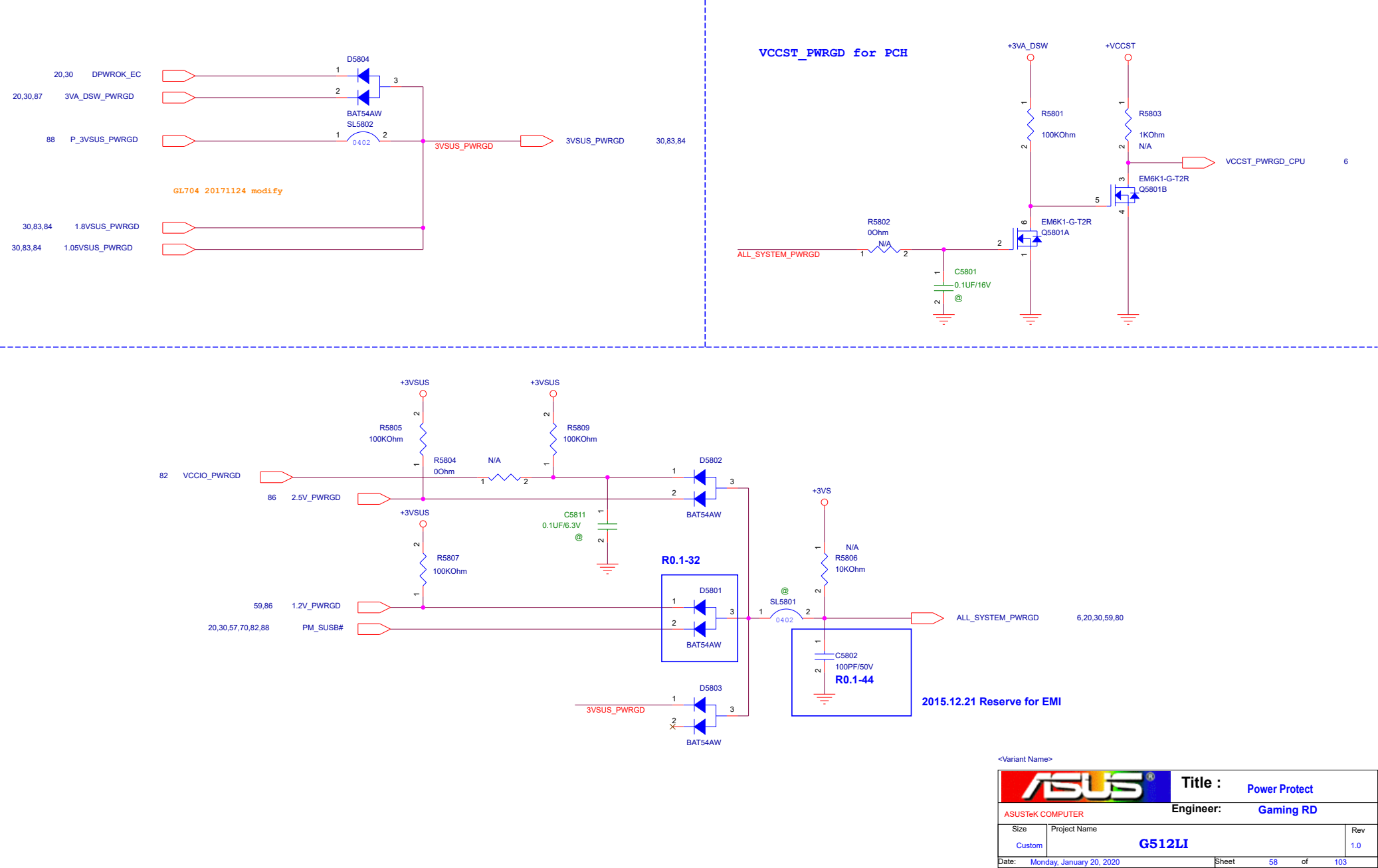






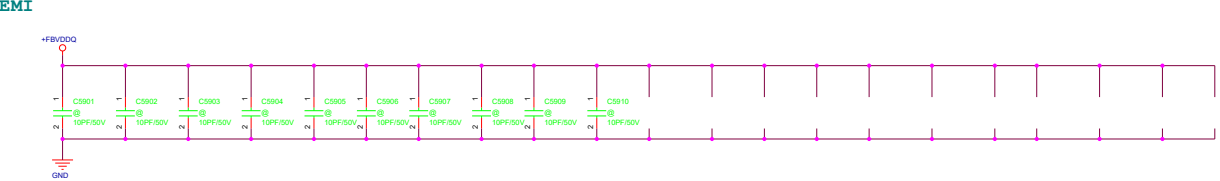
<Variant Name>

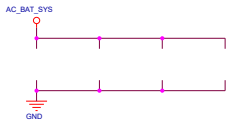
ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: Gaming RD	
Size: C	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 57 of 103	

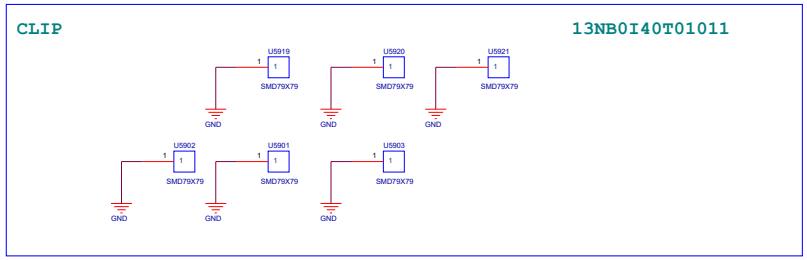


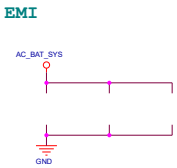
<Variant Name>

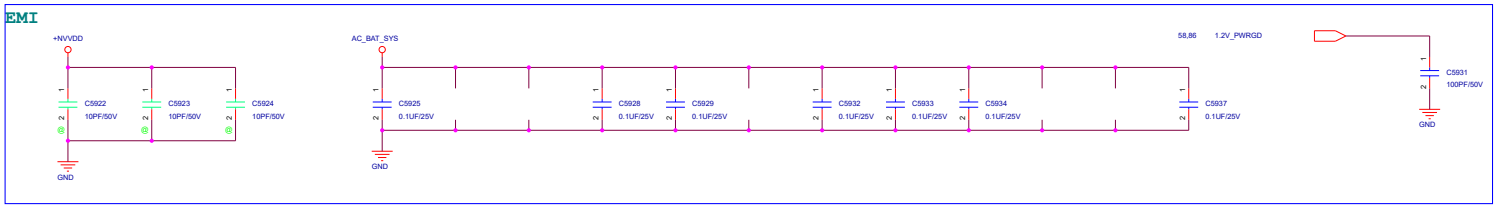
ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: Gaming RD	
Size: Custom	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 58 of 103	

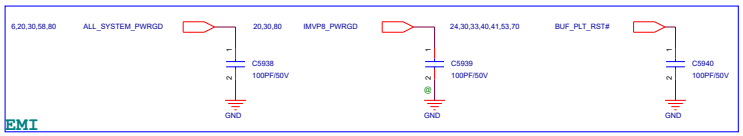


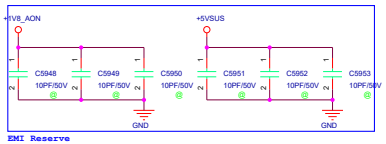


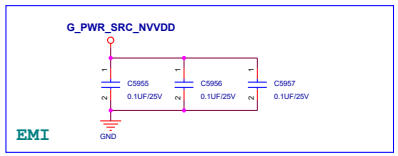


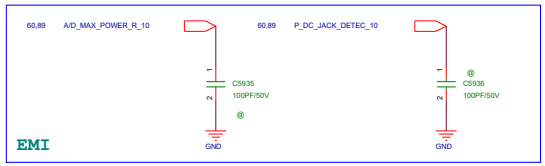








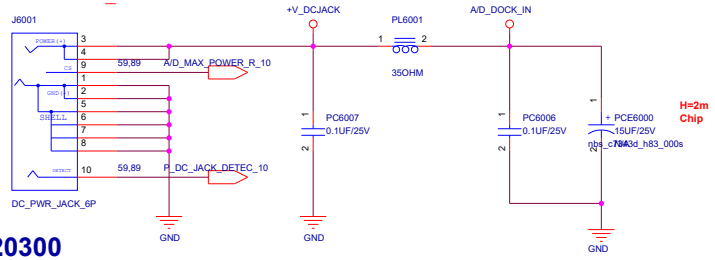




DC-IN Connector

DC Jack使用請詢用River_Hsu

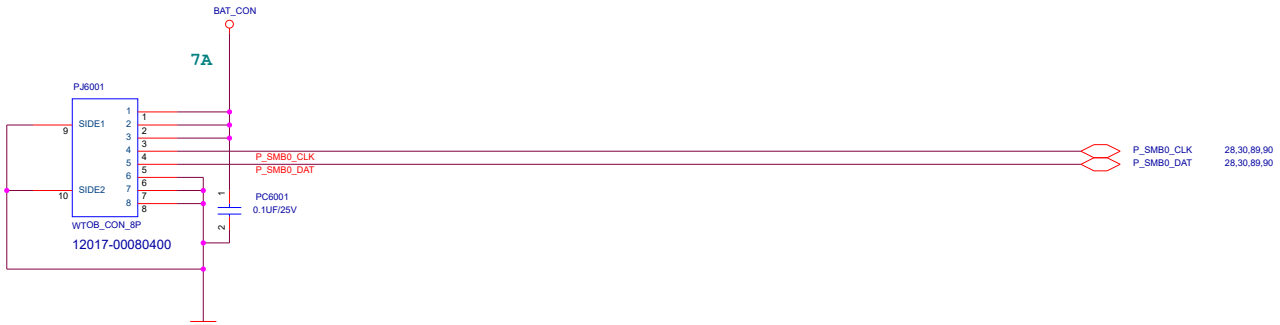
New 6 Phi 4 Pin DC_Jack



12033-00020300

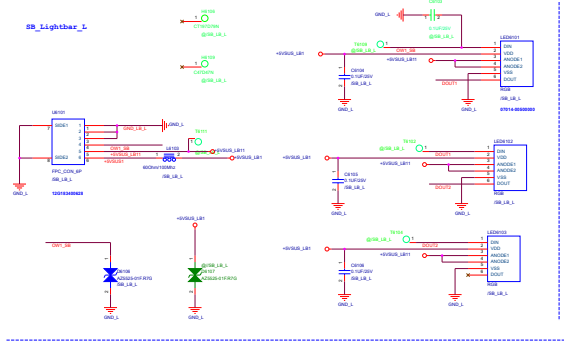
J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

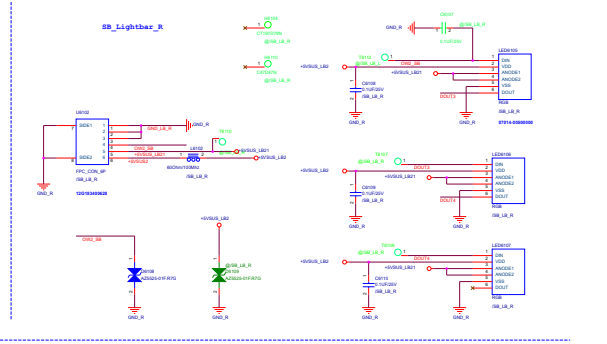
Battery Connector



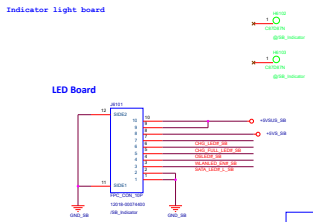
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

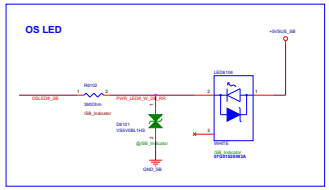
ASUS	Project Name: GX700		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Monday, January 20, 2020	Sheet 60 of 103		

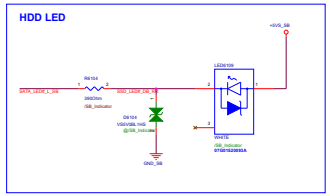

SB_Lightbar_L

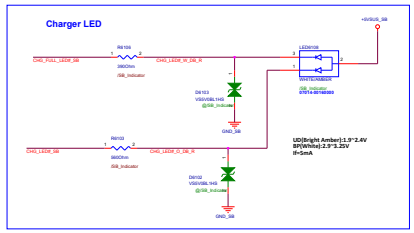


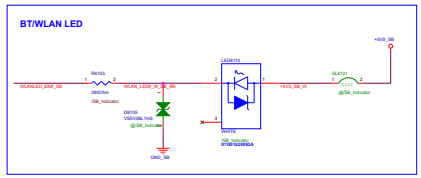
SB_Lightbar_R

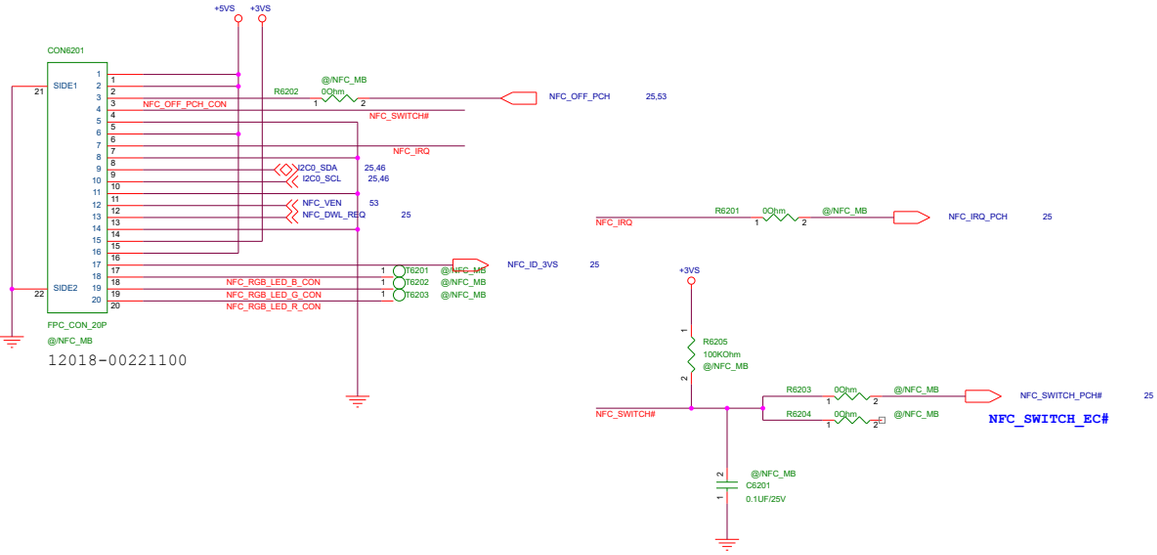

Indicator light board
LED Board


OS LED


HDD LED


Charger LED
LED(Bright Amber):1.0~2.4V
BR(White):2.9~3.25V
IF=5mA


BT/WLAN LED



<variant_name>

ASUSTeK COMPUTER	Title : USB3_*****	
	Engineer: Gaming RD	
Size: Custom	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 62 of 103	

<Variant Name>

Title :

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
C	**G512LI**	1.0

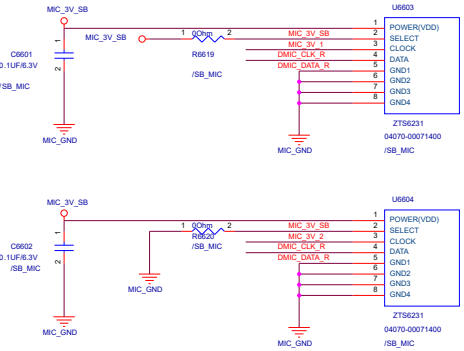
Date:	Monday, January 20, 2020	Sheet	63	of	103

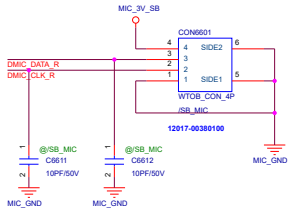
<Variant Name>

ASUSTeK COMPUTER	Title : USB3_*****	
	Engineer: Gaming RD	
Size: C	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 64 of 103	

U6603,U6604
Source:04070-00071400
04070-00072300

SB_DMIC





<Variant Name>

Title : I/O board FUNC key

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
Custom	**G711GW**	1.0

Date:	Monday, January 20, 2020	Sheet	67	of	103

<Variant Name>

	Project Name G512LI	Rev R1.0

Title : Thunderbolt

Size Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD

Date: Monday, January 20, 2020	Sheet 68 of 103

<Variant Name>

ASUSTeK COMPUTER	Title : OTH_EMI	
	Engineer: Gaming RD	
Size: C	Project Name: G512LI	Rev: 1.0
Date: Monday, January 20, 2020	Sheet 69 of 103	

Main Board

GPU POWER GOOD Signal

NVVDD POWER GOOD LOOPBACK

PCI EXPRESS_Graphics

REVERSED Type PCIE X16

GPU POWER SEQUENCE CONTROL

OD

PCH_GPP8

Inverter inside

06004-01490000

Optimus

DGPU_PWR_EN#	FUNCTION
H	GC OFF
L	GC ON

Page 58 need up high

20180719 follow EC CRB schematic Logic add

For EMI

Under GPU

Close GPU

Under GPU

Close GPU

Under GPU

C7511 Reserved for codesign with N17

teknisi indonesia

Table 5.11 GB4D-128 Package: Power Rail Filtering (Continued)

Rail (GPU Ball)	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	14 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) - - - - - - - - - - - - - - - - Alternate solution: 7 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603 X6S)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
PEX_DVDD	6	1.0V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) - - - - - - - - - - - - - - - - Alternate solution: 6 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603 X6S)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)

Confidential 19:06:03

ASUS	Project Name: G512LI		Rev: 2.0
Title : GPU_PCIE I/F			
Size: B	Dept.: Adustrive COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 70 of 100		

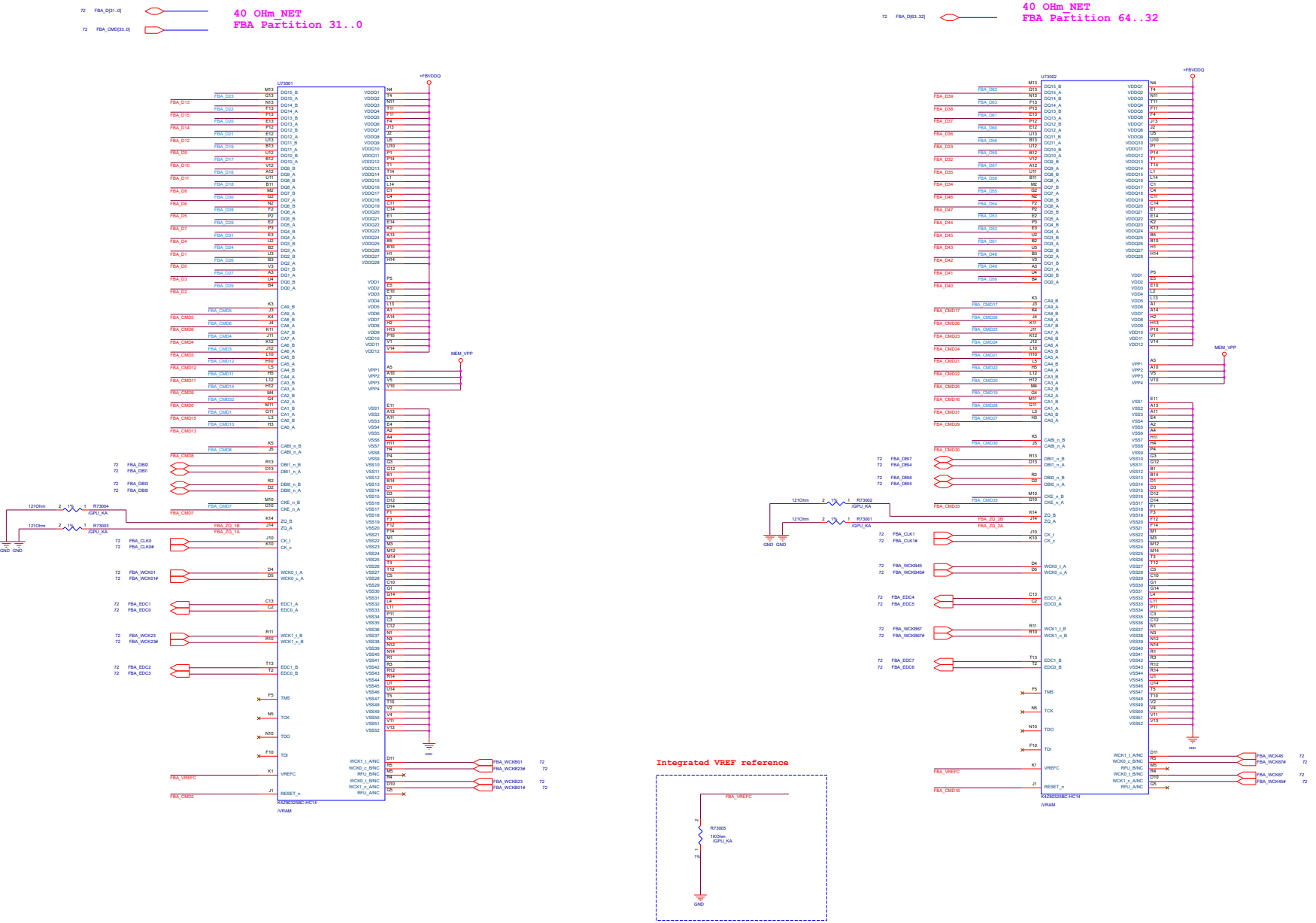


Table 4. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD[2]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD[2]	Full	Production candidate

Notes:
1. For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
2. Requires Production GDDR6 with a specific date code restriction. Exact date code is currently TBD.

ASUS	Project Name: G512LI		Rev: R1.0
Title : VRAM_Channel_A			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 73 of 103		

<Variant Name>

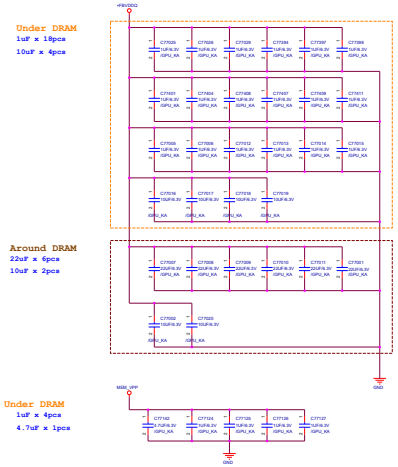
Title <Title>		
Size A1	Document Number G512LI	Rev R1.0
Date: Monday, January 20, 2020	Sheet 75 of 103	

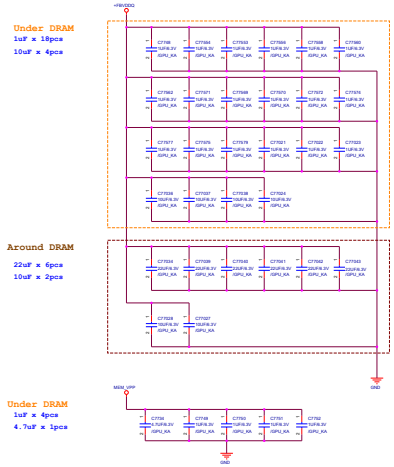
<Variant Name>

Title <Title>		
Size A1	Document Number G512LI	Rev R1.0
Date: Monday, January 20, 2020	Sheet 76 of 103	

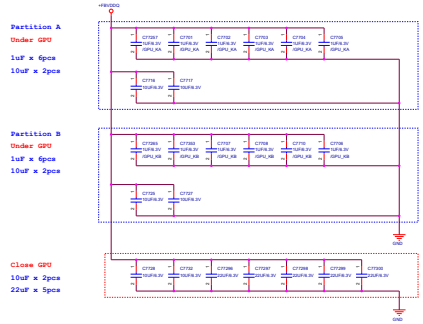
FBVDDQ/VPP (VRAM)

Channel A





FBVDDQ (GPU)



FBVDDQ (GPU side)[1]	1.35V 1.5V	24 x 0.47uF (0201W X6S) 4 x 10uF (0603 X6S) - - - - - - - - - - - - - - - - - Alternate solution: 12 x 1uF (0402 or 0201W, X6S)[3] 4 x 10uF (0603 X6S)	2 x 10uF (0603 X6S)[2] 5 x 22uF (0603 X6S)

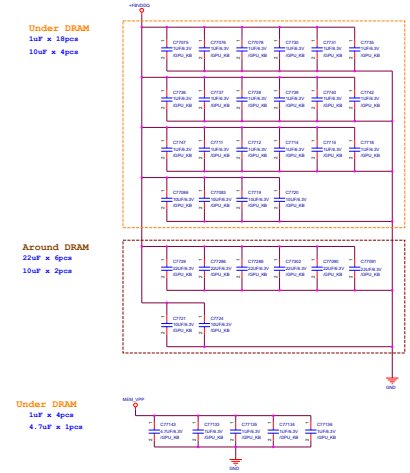
FBVDDQ GPU side (Ref sch)
A ch:
0.47uF x12
10uF x2
B ch:
0.47uF x12
10uF x2
Near GPU
10uF x2
22uF x5

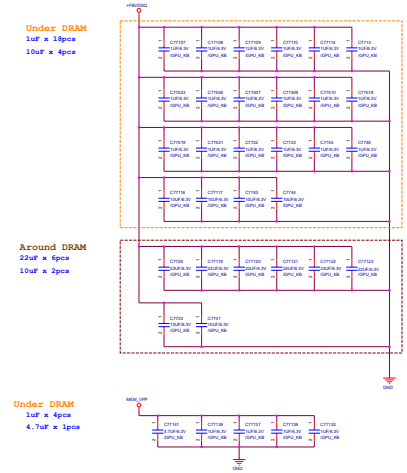
FBVDDQ VRAM side (Ref sch) per VRAM
Close VRAM:
0.47uF x36
10uF x4
0.47uF x8
Around DRAM
22uF x6
10uF x2

Table 8.12 DRAM-Side Decoupling

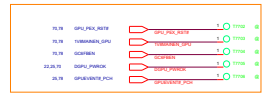
Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

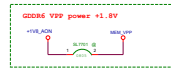
Channel B



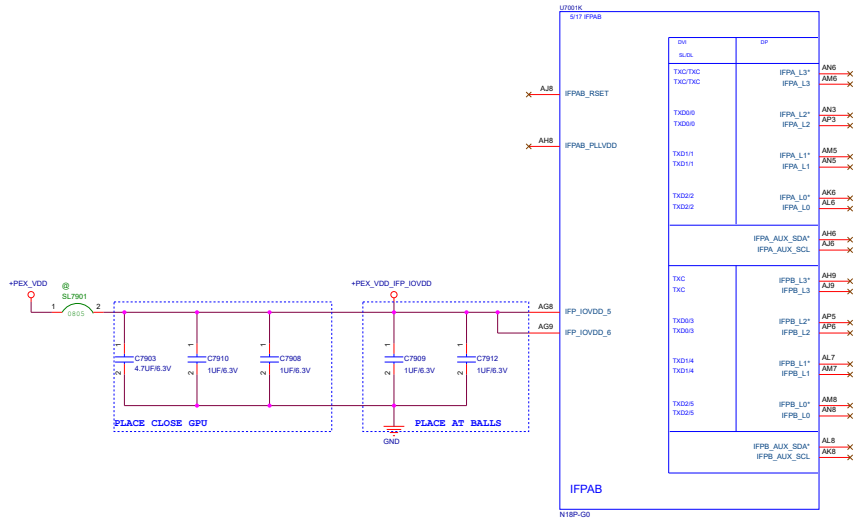


For power sequence measurement

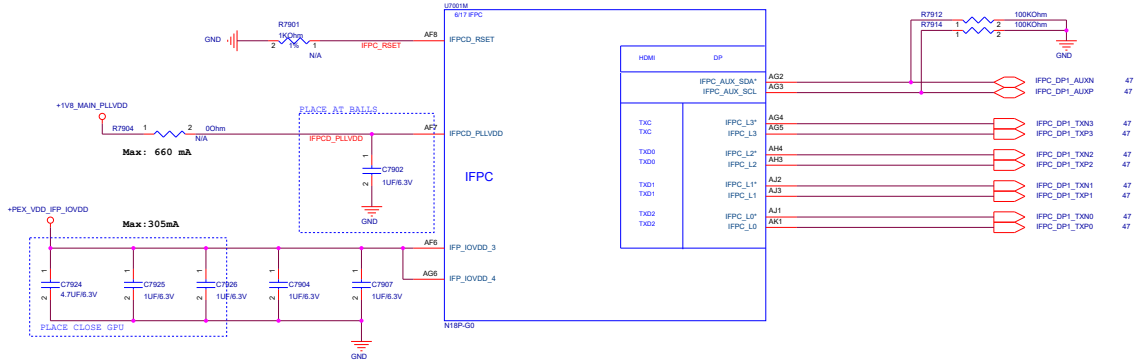




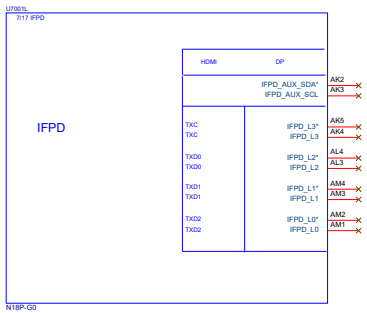
ASUS	Project Name: G512LI			Rev: R1.0
Title: VRM				
Size: A3	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD		
Date: Monday, January 30, 2023		Sheet: 77	of: 103	



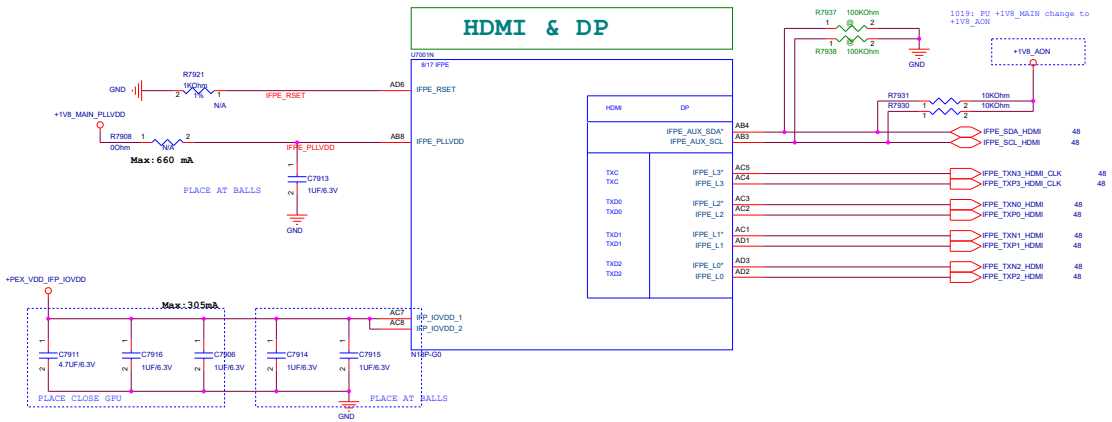
DP(Type-C)



EDP(4Lane Panel)



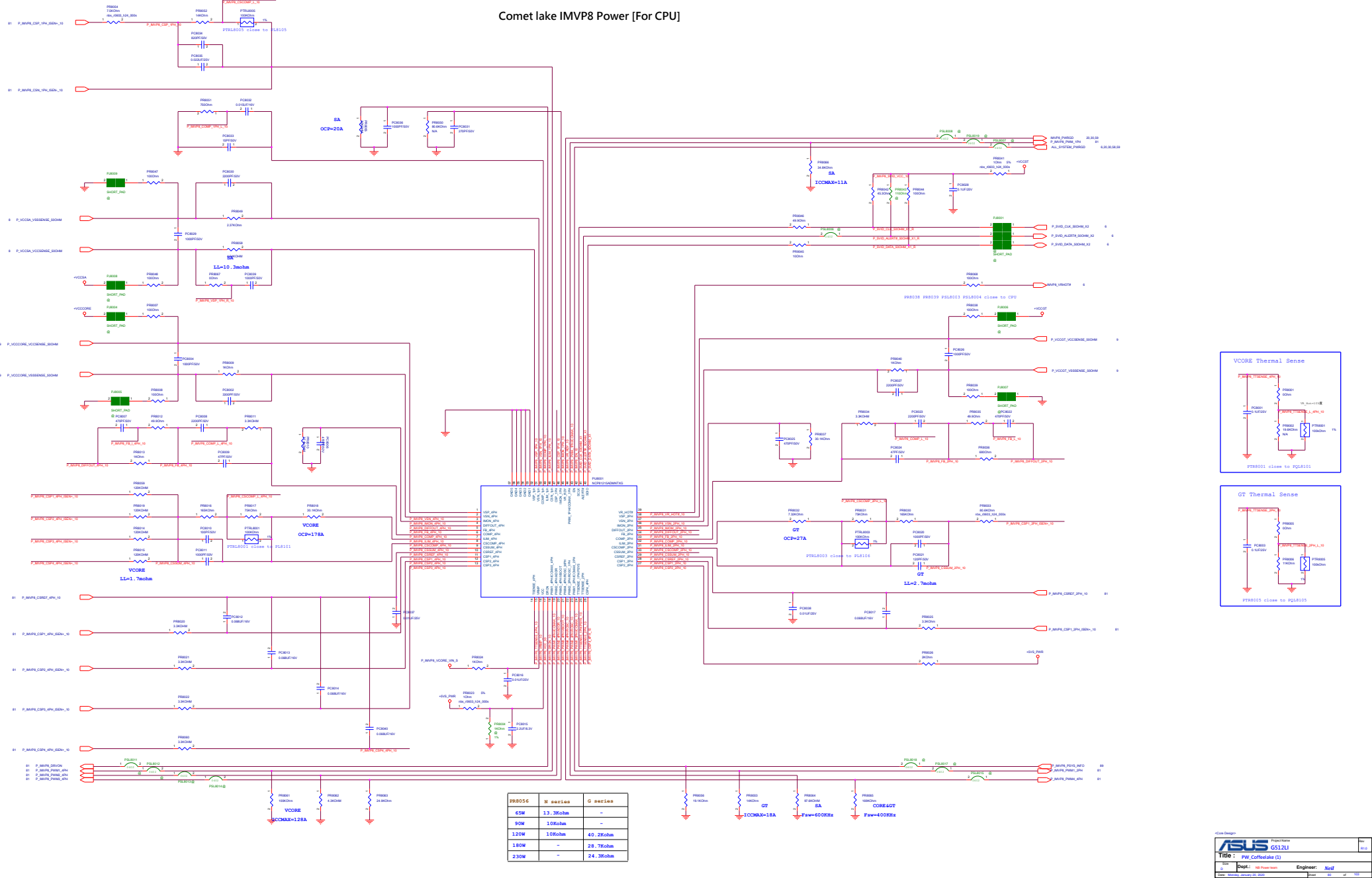
HDMI & DP



IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S, one per ball) - - - - - - - - - - - - - - - - - Alternate solution: 3 x 1uF (0402 or 0201W, X6S, one per ball)	1 x 4.7uF (0603 X6S) 1 x 22uF (0805 X6S) 1 x 30Ω bead (0603 max ESR 0.01 Ω)
IFPCD_PLLVDD	1			
IFPE_PLLVDD	1			
IFP_IOVDD	6	1.0V	6 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - - Alternate solution: 6 x 1uF (0402 or 0201W, X6S)	6 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) - - - - - - - - - - - - - - - - - Alternate solution: 3 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603, X6S)

ASUS	Project Name: G512LI		Rev: 2.0
Title : GPU_DP/EDP/HDMI			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 79 of 103		

Comet lake IMVP8 Power [For CPU]



<Variant Name>

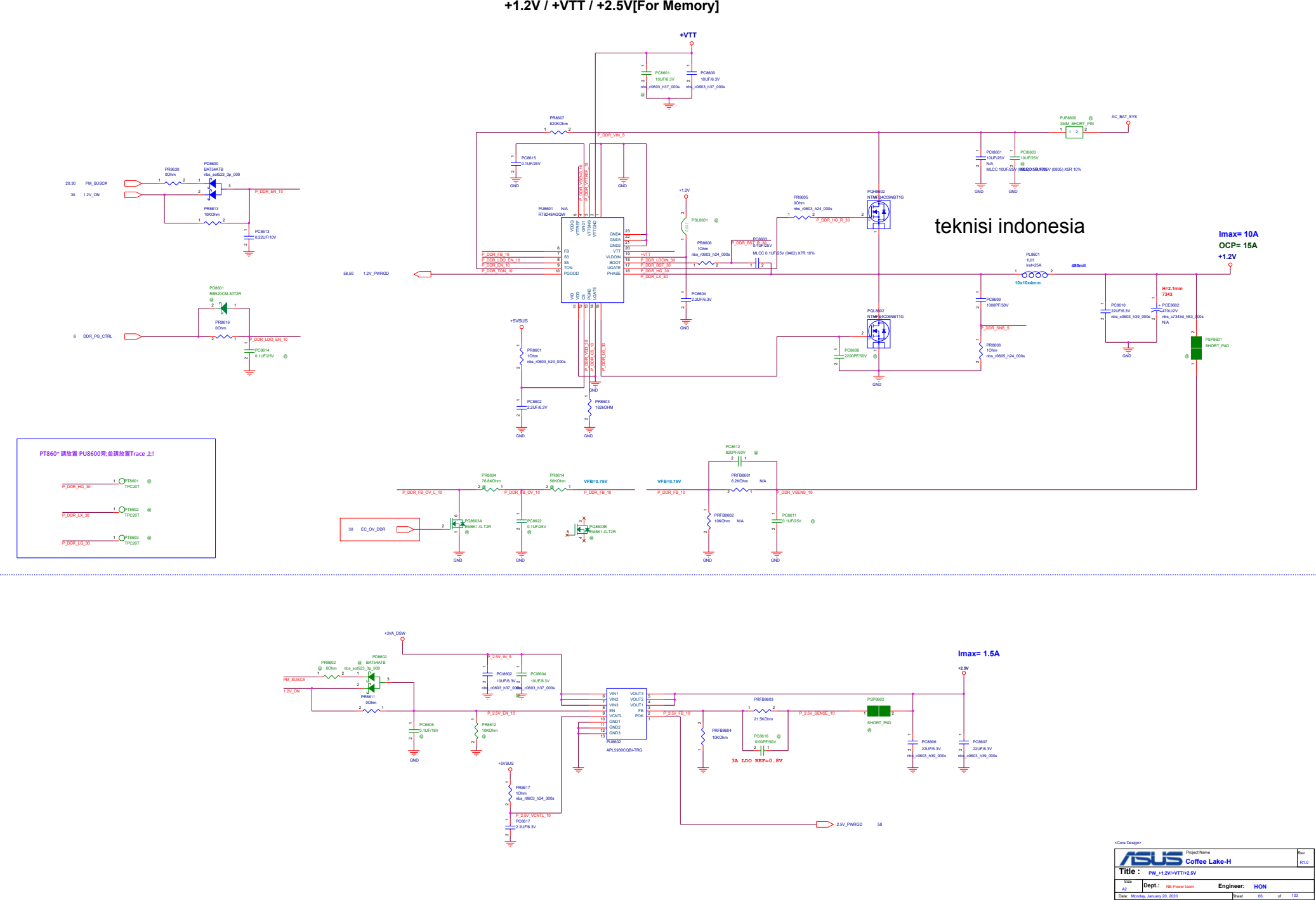
	Project Name GM531GX	Rev R1.0

Title : Thunderbolt

Size	Dept.:	Engineer:
Custom	ASUS Power Team	Joe

Date: Monday, January 20, 2020	Sheet 85	of	103

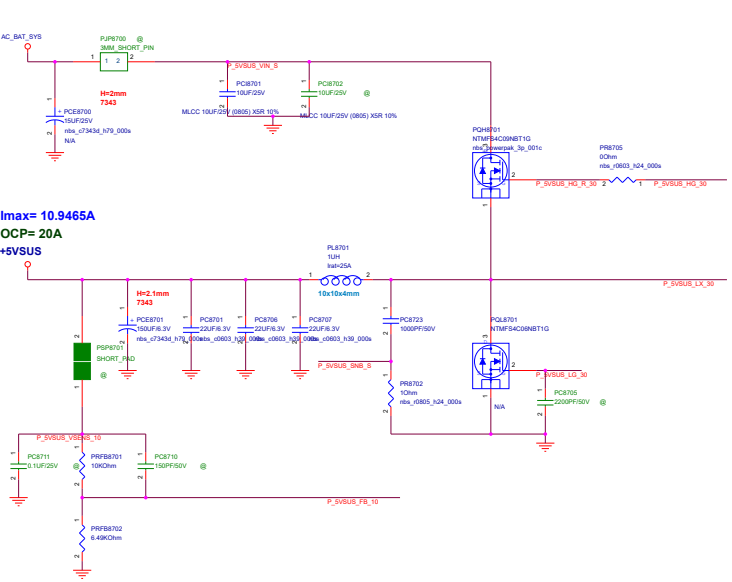
+1.2V / +VTT / +2.5V[For Memory]

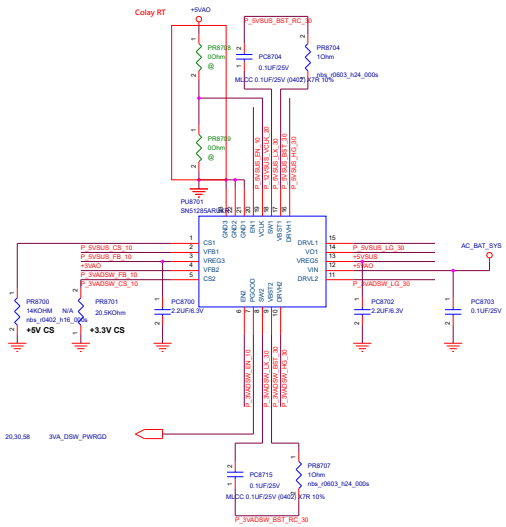


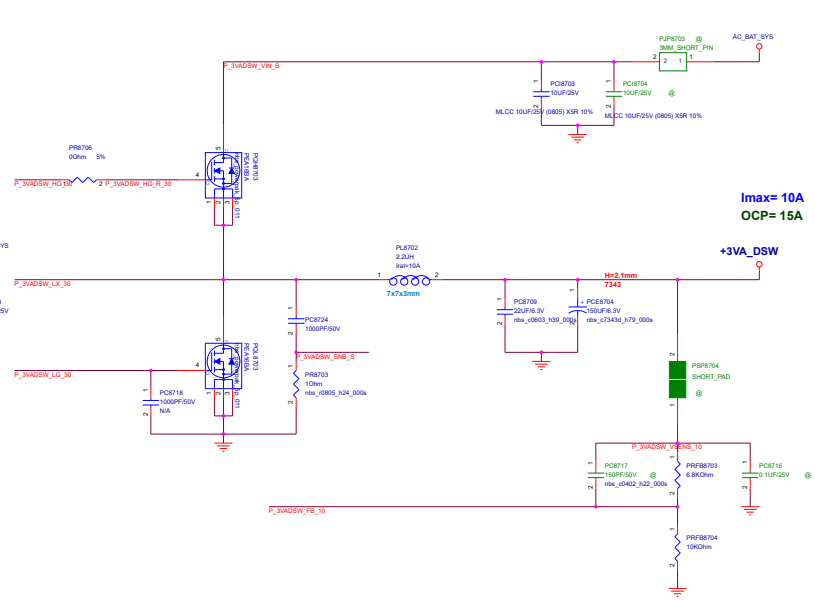
<Core Design>

ASUS	Project Name: Coffee Lake-H		Rev: R1.0
Title :	PW_+1.2V/+VTT/+2.5V		
Size: A2	Dept.: NB Power team	Engineer: HON	
Date: Monday, January 20, 2020		Sheet 86 of 103	

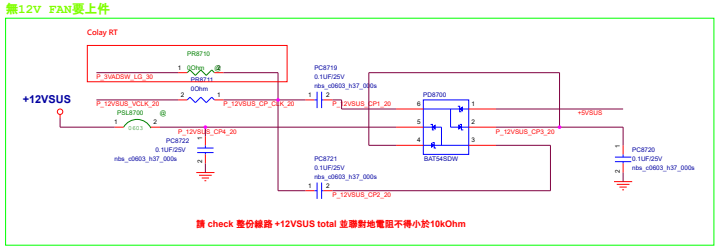
+3VA_DSW / +5VSUS [System Power]

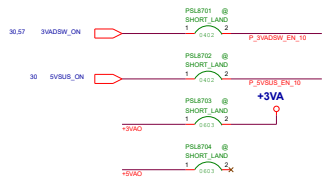






無12V FAN要上件



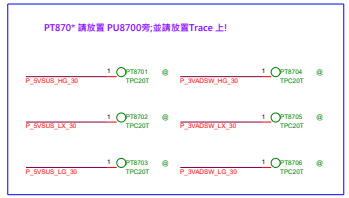


Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

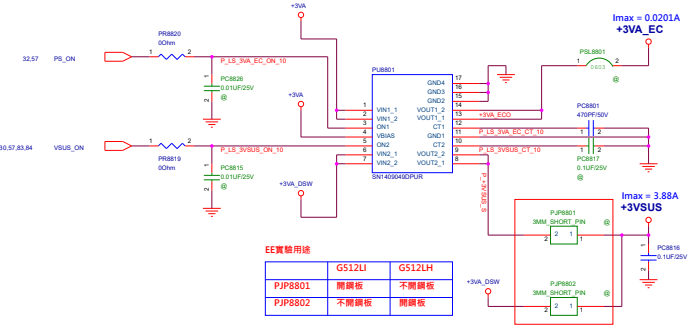
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

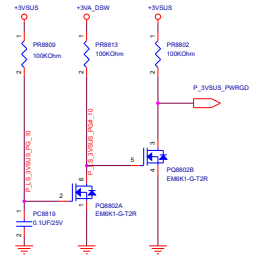


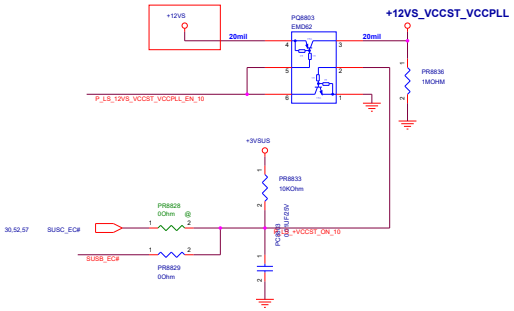
<Variant Name>
ASUS
Project Name: Coffelake-H
Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS
Size: A2
Dept.: NB Power team
Engineer: Joe
Date: Monday, January 20, 2020
Sheet 87 of 103

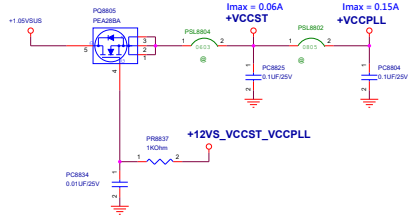
Load Switch

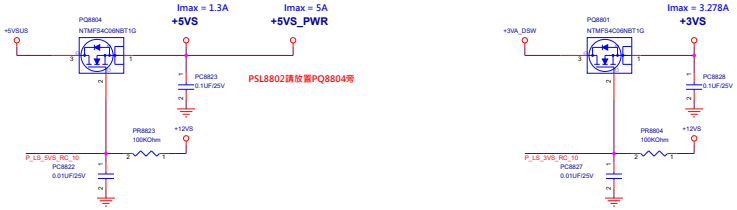
Main Board

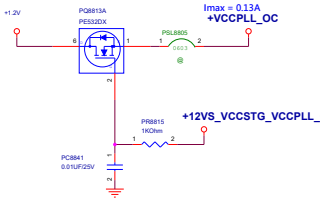


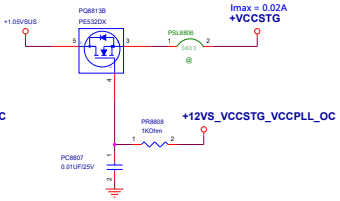






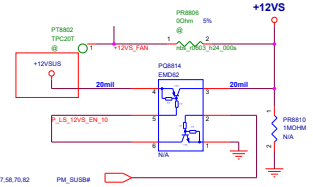


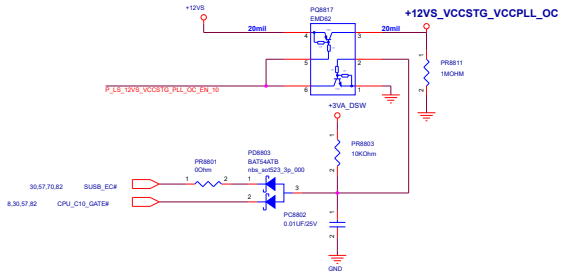




+12VS 的 Vin 對應 BOM 表

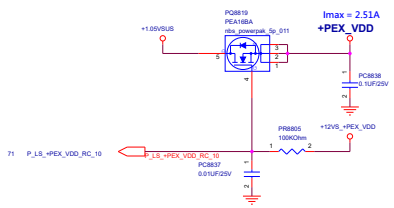
	+12VS_FAN	+12VSUS
PR8806	N/A	@
PR8810	@	N/A
PQ8814	@	N/A

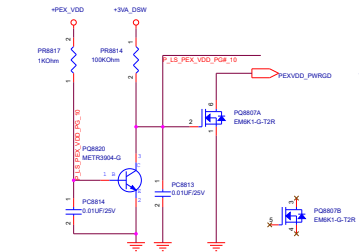


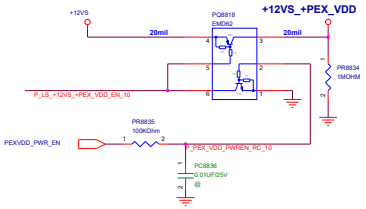


有獨立線路
P97：PW_PEX_VDD 時，
此處的線路請刪除

PQ8820 - 07G003598010
2nd：07003-00030800
07003-00030900
禁用：07G003000120



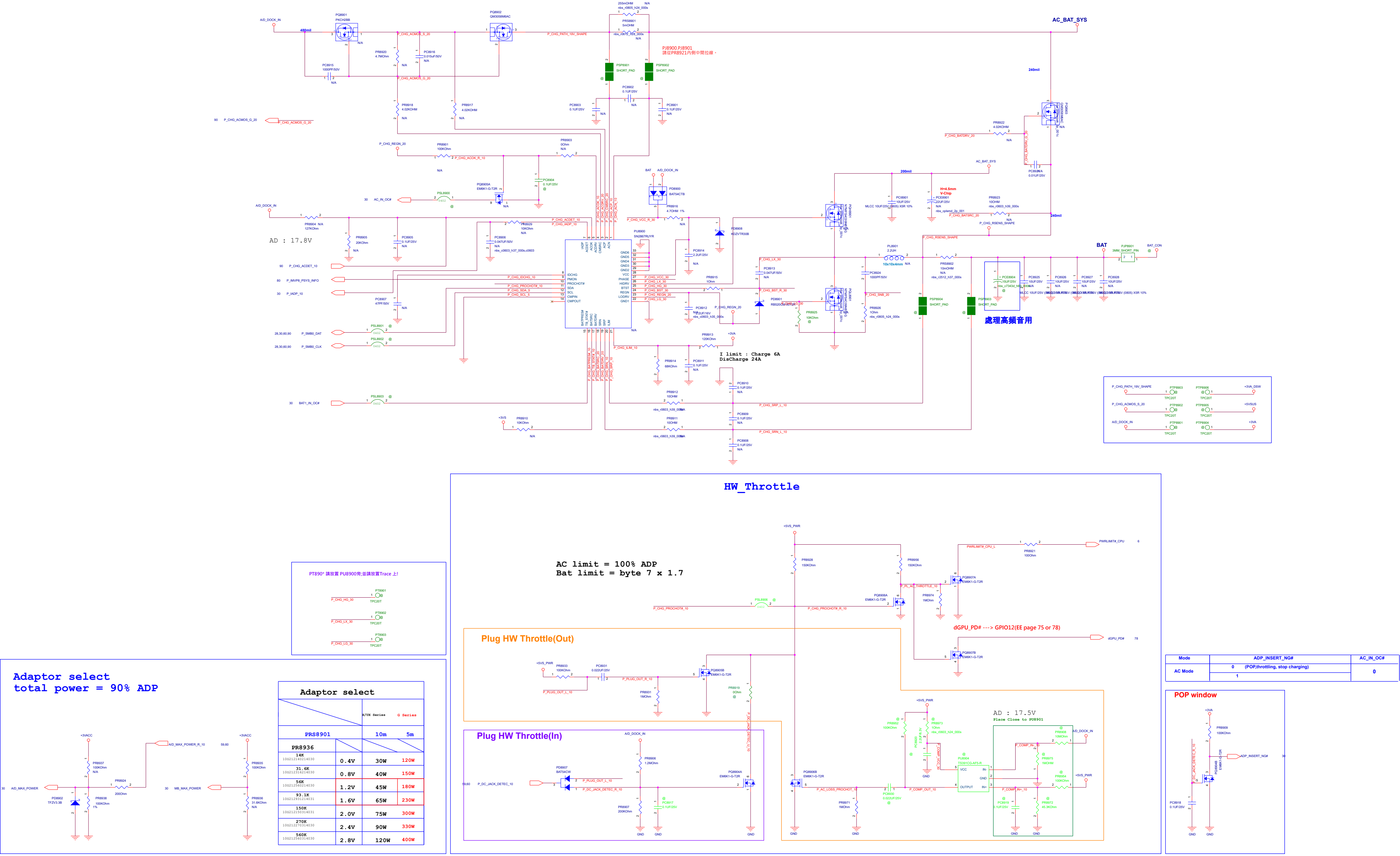




ASUS	Project Name: Coffeelake-H		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A2	Dept.: NB Power team	Engineer: Besnon	
Date: Monday, January 20, 2020	Sheet 88 of 103		

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0006B000	10108-0008B000

PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	10114-0018B000	10114-00221000	x	x	x	10114-00211000



Adaptor select

		X/UX Series	G Series
PRS8901		10m	5m
PR8936			
14K 10G212140214030	0.4V	30W	120W
31.6K 10G212316214030	0.8V	40W	150W
56K 10G212560214030	1.2V	45W	180W
93.1K 10G212931214031	1.6V	65W	230W
150K 10G212150314031	2.0V	75W	300W
270K 10G212270314030	2.4V	90W	330W
560K 10G212560314030	2.8V	120W	400W

Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	

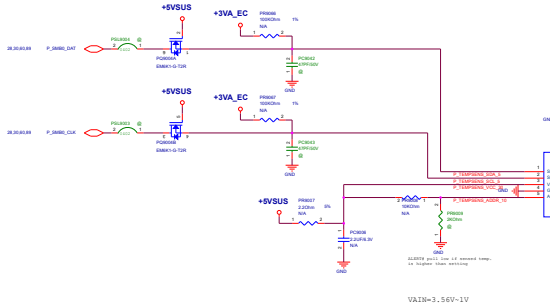
P90_PROTECTION

Address Selection Table

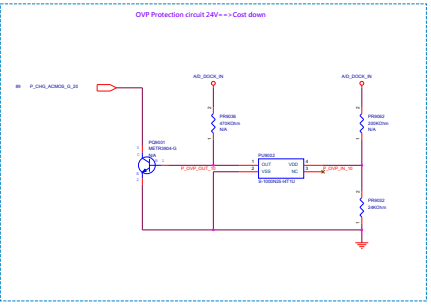
Address	0x18	0x19	0x1A	0x29	0x2A	0x4C	0x4D	0x4E
PSR001	GND	4.7k	2k	4.7k	4.7k	4.7k	4.7k	10k
PSR002	Open	4.7k	4.7k	4.7k	4.7k	4.7k	4.7k	10k

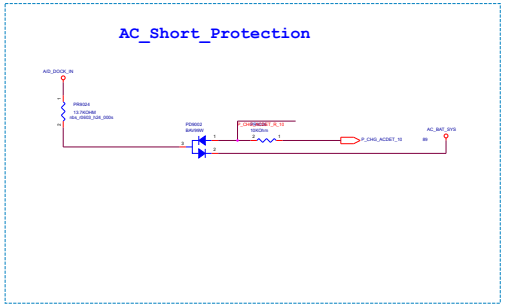
Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	R	W	W	R	R	R	R
Function		Temp. alert threshold setting		Sensed temp. data			bit 7 = 0 bit 5 = 0 bit 4 = 0 When ALERT# asserted



VAIN=3.56V~1V
NTC=115kohm~2.75kohm
(25度~125度)





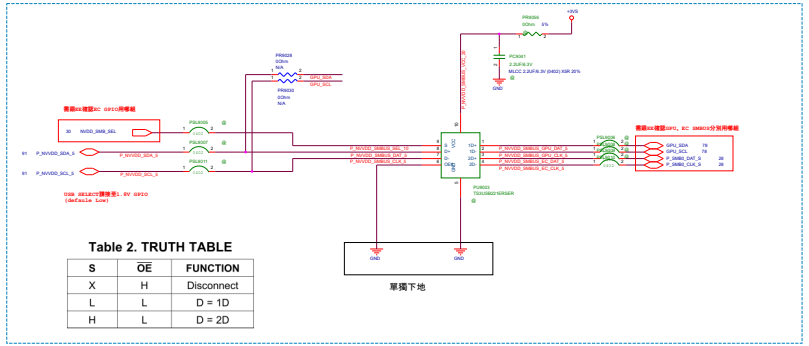


Table 2. TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

+NVVDD [For DGPU]

X50 Ti : PR9117不上件 / PR9115、PR9116上件
X50 : PR9117上件 / PR9115、PR9116不上件

teknisi indonesia

Vboot = 0.8V

Per Limit=70A

LL= 0 mohm

Total OC =230A

< HW Strap Function setting >
PWM2 : APL_Hys = 13.9A
PWM3 : VAPL1 = 16.7A (1 Phase)
PWM4 : VAPL2 = 34.1A (2 Phase)

請放靠近PU9101

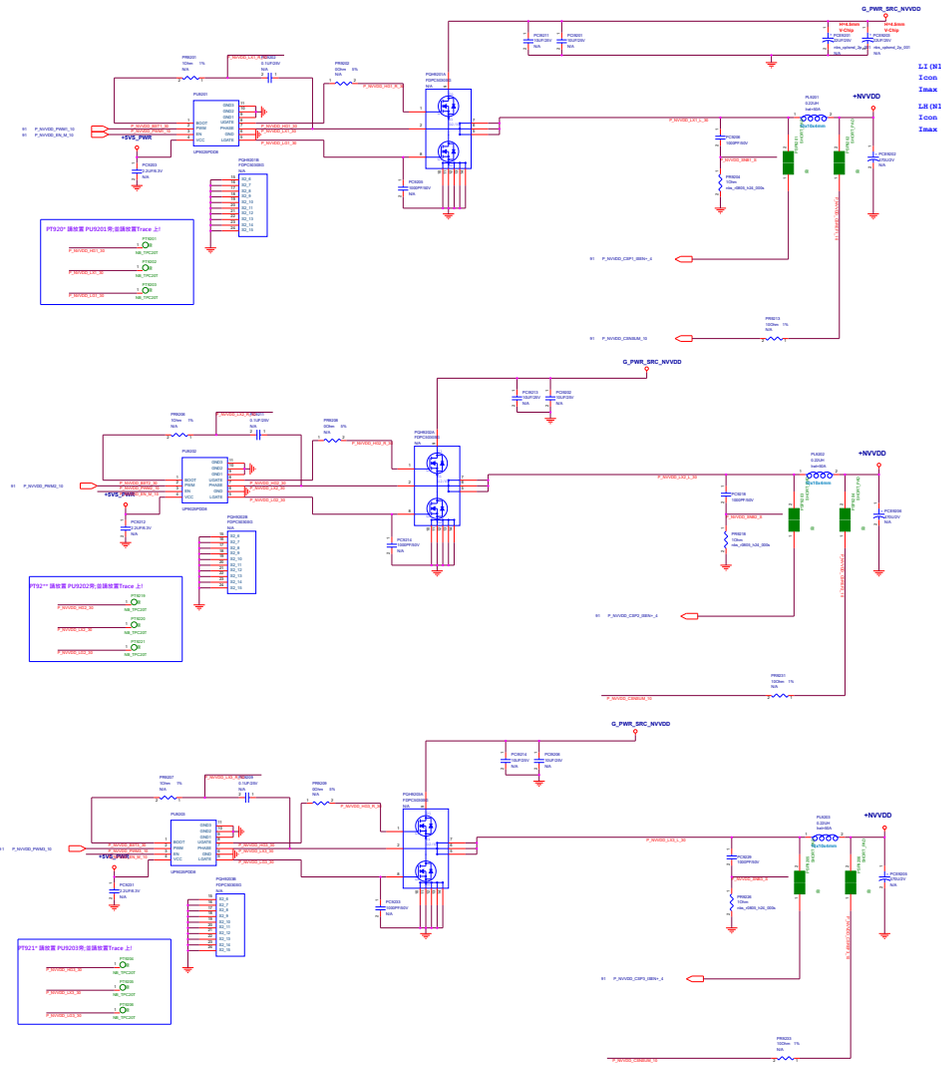
Phase訊號請和周圍線、Via盡量保持30mil

Phase訊號請和周圍線、Via盡量保持30mil

Phase訊號請和周圍線、Via盡量保持30mil

ASUS	Project Name: G711GW		Rev: 81.0
Title :	PW_+NVVDD (1)		
Size: Custom	Dept.: NB Power Team	Engineer: Neil	
Date: Monday, January 20, 2020	Sheet: 91	of: 103	

+NVVDD [For DGPU]



ASUSTeK Computer Inc.
Project Name: G711GW
Title: PM_+NVVDD (2)
Size: A3
Dept.: NB Power Team
Engineer: Neil
Date: Monday, January 03, 2020
Sheet: 93 of 120

<Variant Name>

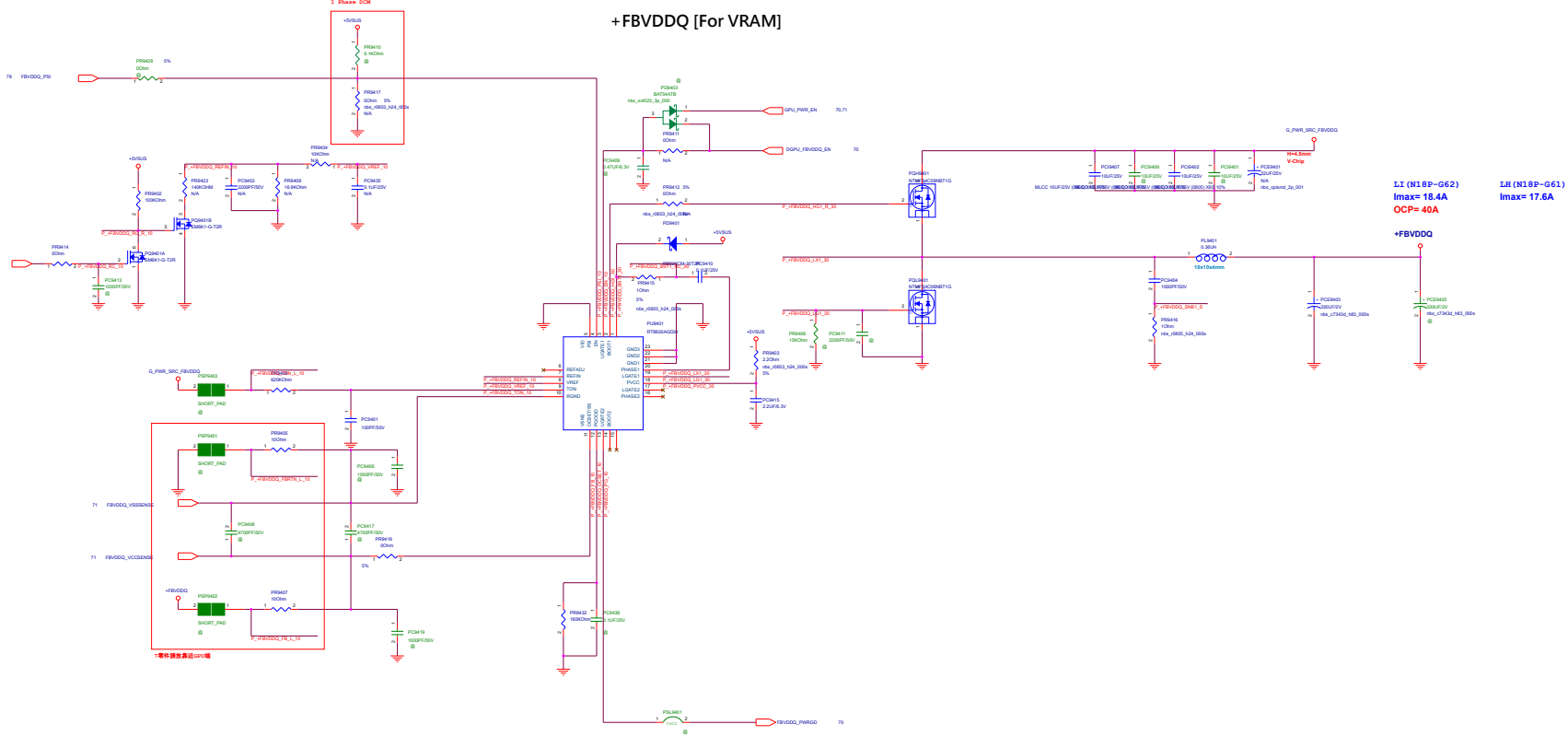
	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

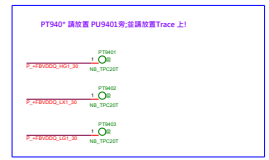
Size			
Custom	**Dept.:** NB Power Team	**Engineer:** Joe	
Date: Monday, January 20, 2020	Sheet 93	of 117	

+FBVDDQ [For VRAM]

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
PR9404	108Ohm	
PR9409	16.9KOhm	
PR9423	140Ohm	



PT940* 請放置 PU9401旁;並請放置Trace 上!



<Variant Name>

	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

Size			
Custom	**Dept.:** NB Power Team	**Engineer:** Joe	
Date: Monday, January 20, 2020	Sheet 95	of 117	

<Variant Name>

	Project Name **Coffeelake-H**	Rev R1.0

Title : PW_+12VS_FAN

Size			
B	**Dept.:** NB Power team	**Engineer:** Hon	
Date: Monday, January 20, 2020	Sheet 96	of 103	

Project Name

GX531GM

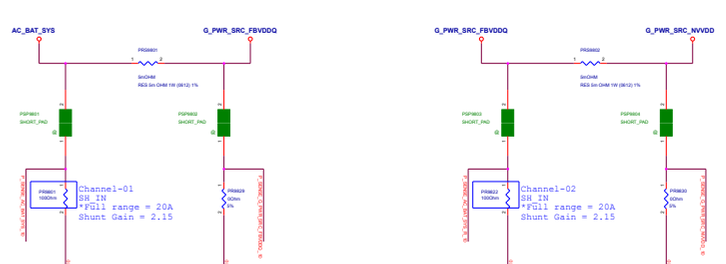
Rev

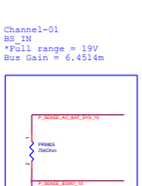
R1.0

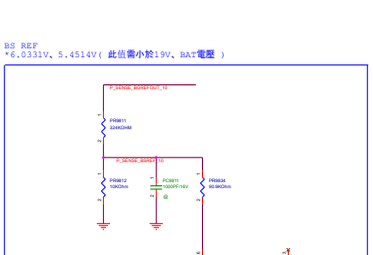
Title : Type C LDO 3V3

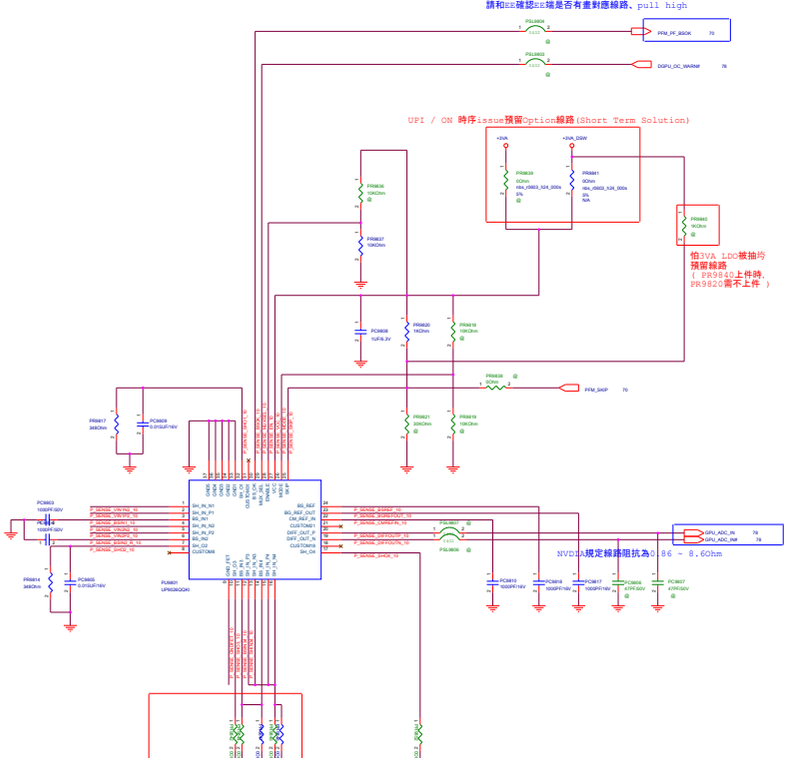
Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	Joe

Date:	Sheet		
Monday, January 20, 2020	97	of	103









N18E

150W+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G212100014010)	
PR9817	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9822	100Ω(10G212100014010)	
PR9814	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	143Ω (10G212143014010)	191Ω (10G212191014010)
PR9814	143Ω (10G212143014010)	191Ω (10G212191014010)

100W ~ 110W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	165Ω (10G212165014010)	221Ω (10G212221014010)
PR9822		
PR9814	165Ω (10G212165014010)	221Ω (10G212221014010)

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	215Ω (10102-00571000)	287Ω (10G212287014010)
PR9822		
PR9814	215Ω (10102-00571000)	287Ω (10G212287014010)

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822		
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)

N18P

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G212100014010)	
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822	100Ω(10G212100014010)	
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

150w+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	127Ω (10G212127014010)	
PR9822	200Ω(10G212200014010)	
PR9814	127Ω (10G212127014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	143Ω (10G212143014010)	
PR9822	200Ω(10G212200014010)	
PR9814	143Ω (10G212143014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	215Ω (10102-00571000)	
PR9822	200Ω(10G212200014010)	
PR9814	215Ω (10102-00571000)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

<Variant Name>

	Project Name **G512LI**	Rev R1.0

Title : PW_Input CAP

Size Custom	**Dept.:** Power Team	**Engineer:** Joe

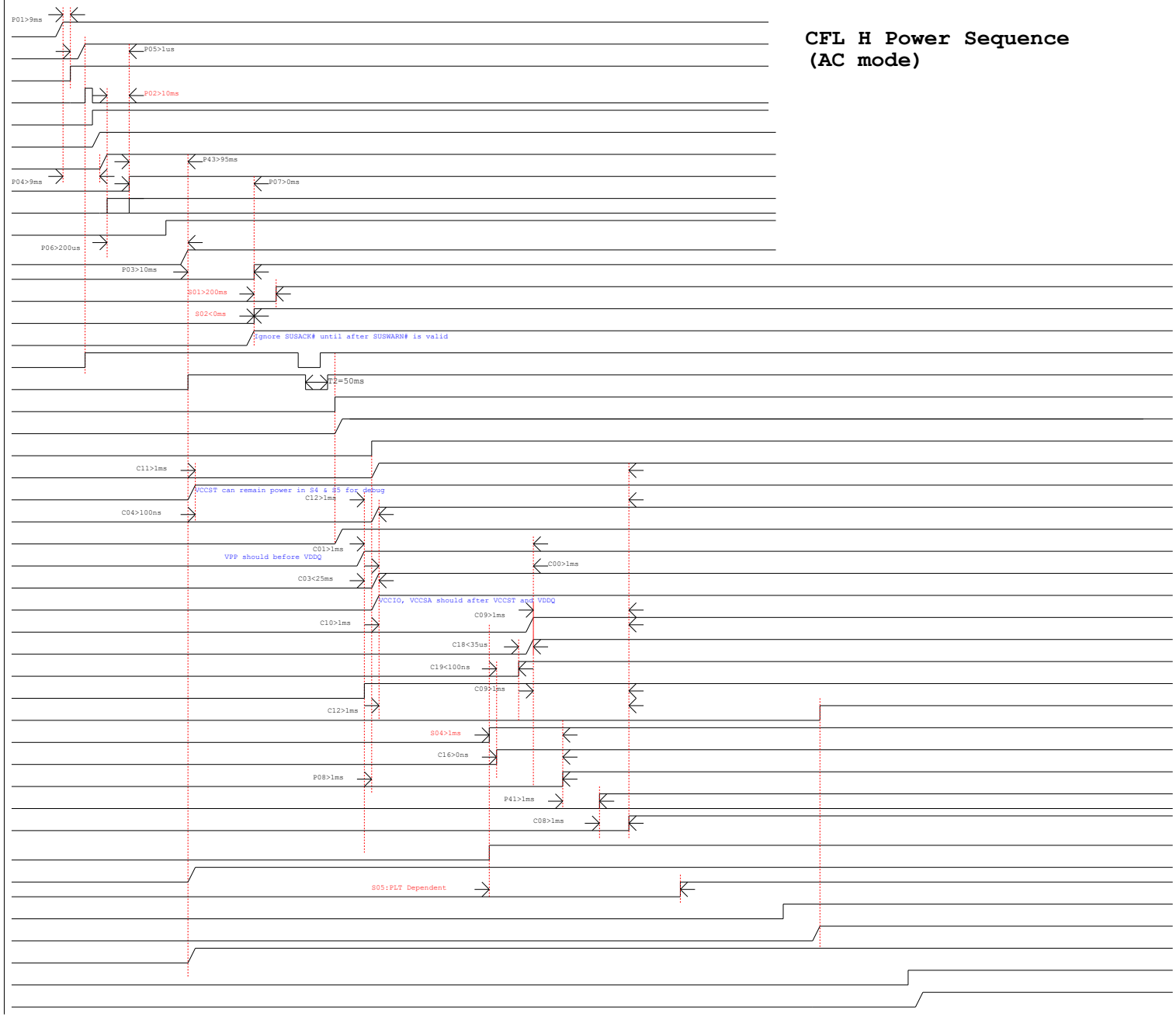
Date: Monday, January 20, 2020	Sheet 99	of	102

AC-IN Mode

CFL H Power Sequence (AC mode)

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



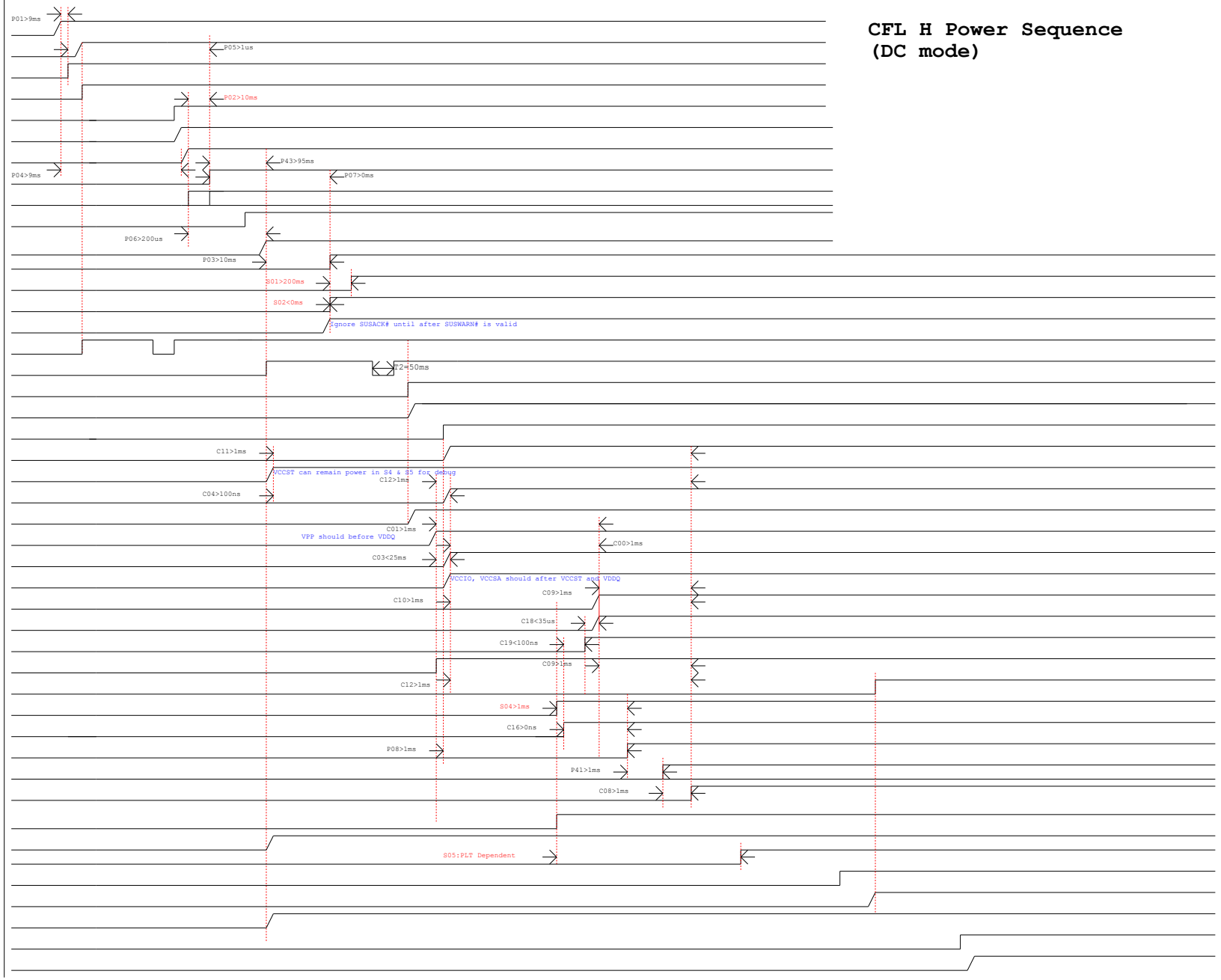
ASUS	Project Name: G512LI		Rev: R1.0
Title : Power On Timing–AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 100 of 103		

CFL H Power Sequence (DC mode)

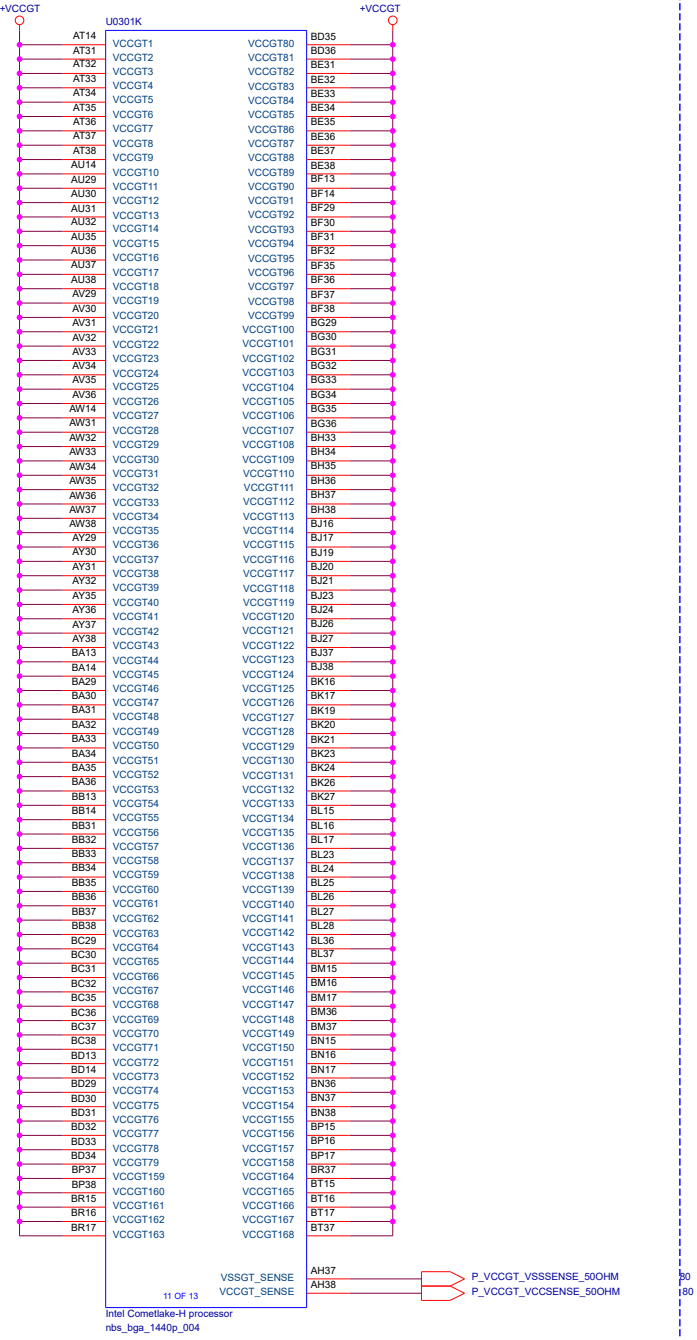
DC-IN Mode

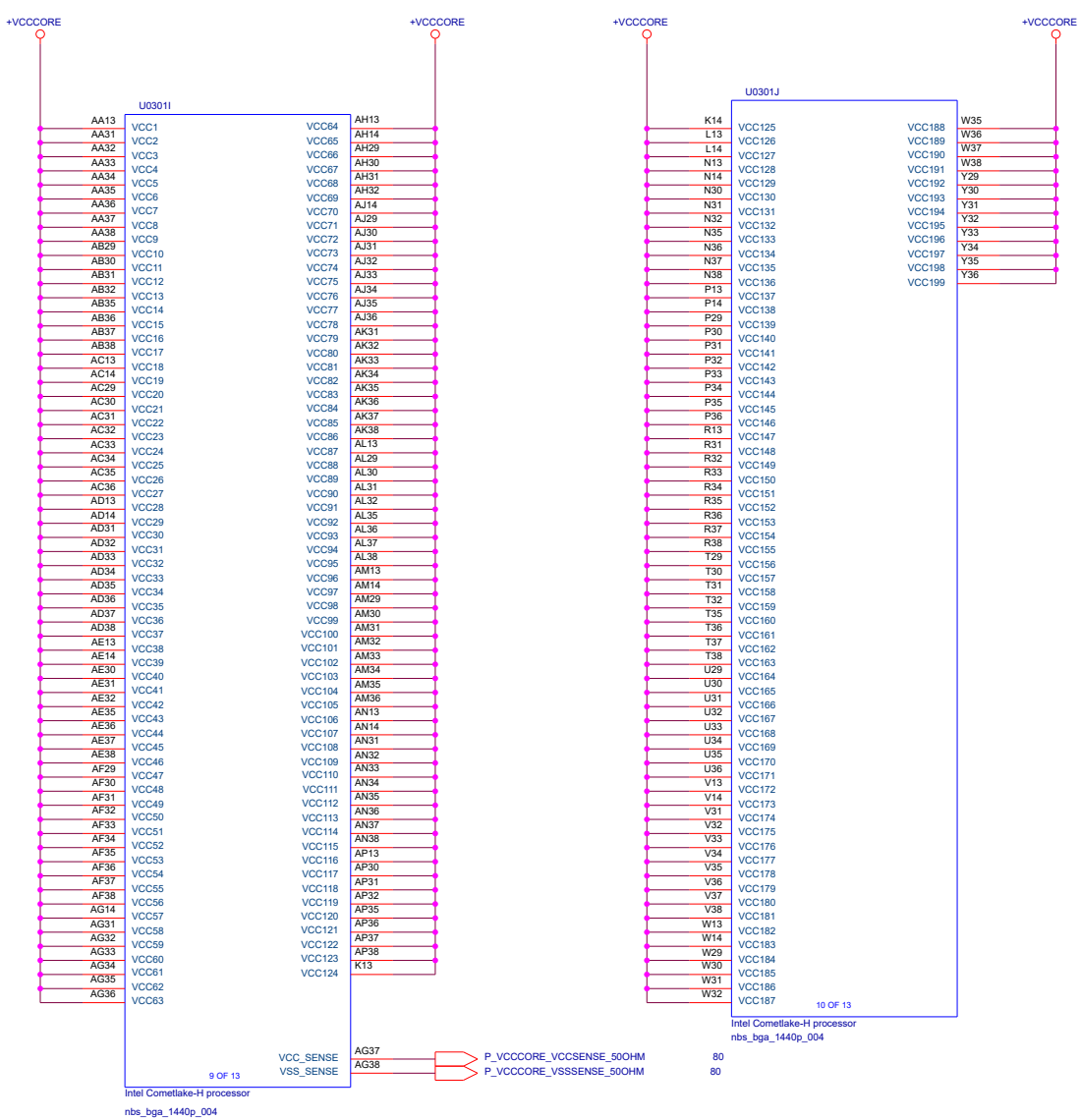
C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: G512LI		Rev: R1.0
Title : Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Monday, January 20, 2020	Sheet 101 of 103		





Project Name: G512LI		Rev: 1.0
Title: CPU_PWR		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Monday, January 20, 2020	Sheet 9 of 103	

Rev	Date	Description
R1.1	2019.06.17	1.Reseed on CPU_GX502 MB_MP_0419 2.Add Typec1 solution(GX502MB) 3.Add MOPP PCIE SSD*2
	2019.06.18	4.Change Type C solution MOS from Pericom 12DP4 to TI 3246
	2019.06.21	5.Update Power schematic GX502 PWR_R1E0-02_CML-Y-Line_ES_20190620 6.P31, Remove EMI connector 7.Update Power schematic GX502 PWR_R1E0-02_CML-Y-Line_ES_20190621
	2019.06.24	8.Update Power schematic GX502 PWR_R1E0-02_CML-Y-Line_ES_20190624
	2019.06.25	9.P48, Follow Design ID HDMI_REV010 change HDMI solution from 2785317RB to 2875302100RBJ
	2019.06.26	10.P39,P56 , Add thermal lighting LED control sch
	2019.06.27	11.P88,P87 , Change Type-C solution to TI PD65599S with 1046A
	2019.06.28	12.Update Power schematic GX502 PWR_R1E0-02_CML-Y-Line_ES_20190627
	2019.07.03	13.Update Type-C schematic TYPE-C_AIC_DDR3-102 = DP = DP_TI_20190703
	2019.07.04	14.P30 , follow Design ID add DDR PWR ON 15.P38,P52 , Add C9871, C9894, C9897, C9208 , C9209, C9210 Remove C9211, C9212 16.P20, Add R2926, R2970, R2971 for CML cost down 17.P48, Follow Design ID HDMI_REV010 Change R4801, R4802 Remove R4803,R4804 18.P57 , Change R4707, Q4708 optional from N/A to 0 because VCCGI solution change to converter
	2019.07.10	19.P72~P74, Change from GD25B5 to GD25B6 for R1E0-CM1/CM2 20.Update Power schematic GX502(S)_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190710 21.Update Type-C schematic TYPE-C_AIC_DDR3-102 = DP = DP_TI_20190710
	2019.07.16	22.P71~P79 , Check GPU sch with Ref. sch
	2019.07.17	23.Update Power schematic GX502(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190717 23.P30, delete D3003 because change CPU power solution
	2019.07.22	24.Update Power schematic GX502(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190722 1. 更改Q4707 4898(SH4N15ALLTCR)為4899(SH4N15ALLTCR-G0012800) 2. 新增 R4802/ R4F19/R-39 3. 更改電感值(PCB Layout)為4.4uH 25.Update Type-C schematic TYPE-C_AIC_DDR3-102 = DP = DP_TI_20190722 26.Update HDMI schematic HDMI_REV010
	2019.07.23	27.P85 ,follow Design ID update +VTR LCD, MIC_V, AC_BAT_SYS power solution(power solution by poly switch)P81 PS_ADJ@ 28.P7, Remove XDP reserved components 29.P30, change R2003 from 100ohm to 0 ohm , R2062, R2063 optional from N/A to 0 and PU to VCCSUS, R2065 from 1k ohm to 1k ohm and PU to GND 30.P39, P56, remove Q3501S, Q3510A, Q3511A, Q3512S, R3585, R3590, C5631, C5404 for MCU spp. delete thermal lighting LED 31.P56 , Change C5601 from EOMI to Ferrocerbox for EMI request (Ref. CML GX502M_ETX 20190715 C.DSB) 32.P20 ,following Design ID change CPU VRAM GPU(add) thermal sensor to MS7502(Ref. MS7502_REFERENCE_DSB_3618.DSB)
	2019.07.24	33.P56, Remove Q3509(follow GX52LB)
	2019.07.25	34.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190725.DSB 35.P56 , remove Q3606, R3606,add R3608 for EMI SCI 36.P38 , Change USB port power solution to GX4781EN22
	2019.07.29B	37.P34, Change Keyboard ID to GPP_B12, GPP_B13, GPP_E16 38.P20, follow Intel PDG remove R2062, R2063 for SCI
	2019.07.29A	39.P38~P52, change page 38 component to page 52 for EC sout policy 40.P41,P42, change page 39 component to page 53 for EC sout policy
	2019.07.29B	41.P20,P31, remove Q2005S , add T2015, T2016 (not support Deep Sx) 42.P39,Change C5530, C3529 from 1.0uF to 2.2uF for better PSRR 43.P35 Change R-Key IC 2SB2999 from EZ version to TA Version(R6557-00041100) 44.P35 Change 3TEB2R5 3V power excition from APL5930CKQBI-TRG to TLV75533PDBVR and output cap 2200pF to 1uF for better ESR 45.P49, Add R6525, R6526 for CML thermal module 46.P22 , Change R2401, R2402, R2404, R2405, R2406 from 33 ohm to 22 ohm for meet CML PDG
	2019.07.29C	47.P28 ,add R2917, R2918, R2920, R2921 for SPI to meet CML PDG 48.P30 , Change R3024, R3025, R3010 from 15 ohm to 75 ohm for meet CML PDG 49.P21 , change R2004 from 10k ohm to 100k ohm to meet CML SIO SUS 50.P30, remove C3024(no support Deep Sx)
	2019.07.29	51.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190729 52.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190729_R 53.P73,P74,P77 , remove C7701, R7701, R7702, R7703, R7706, R7705, R7706, add R7800, R7802A for CPU integrated VREF reference spec (SC-00780-301-703)

Rev	Date	Description
	2019.07.30	53.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190729_C 54.Change SKU from 16 lanes to 8 lanes
	2019.07.31	55.P70,P78, add R7048 for CPU_PEX_RSTB(OD), change R7842 from 10k to 0 ohm and connect 56.P40 , remove C4106, C4107, C4121, C4122 57.P39, remove R3589, R3590 58.P6, Short R6805, U6801, C6802, R6804, R6840 , connect R6850 for C8 (follow VC) 59.P92, Change USB power solution to G5170ZP02U(3.6A)
	2019.08.01	60.P56, add R5605, R5610 for ITE 8299 Stuid(Stuid) GO 61.P20 Remove R2089 for SO issue 62.P21 add R2109 for TypeC display port MUX
	2019.08.02A	63.P47, remove R4724, R4727, R4732, R4733 to meet TI reference Design 64.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190802
	2019.08.05	65.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190805_C 66.P63,P64, Remove MPC schematic to meet MET spec
	2019.08.06	67.P63,P64, add MPC board for MP request(DB only) 68.P40,P41, remove JS101, JS102 ,add JS002 for SSD power
	2019.08.07	69.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190807 70.P33, Change LAN chip part number to 06212-00300200
	2019.08.13A	71. P39,P51, Remove Q3514, Q3503, Q3511, Q3512, Q3513, Q3504, Q3519, Q3517, Q3520, Q3522, R3506, R3526, R3570, C3501C2, C3501C3, R3435, R3436, R3437, R3438, R3439, R3440, R3441, R3442, R3443, R3444, R3445, R3446 to meet MET spec (No mute_mic) and Remove Layout Note 72.P20,P41, Add R2123, R2124 and Remove R2125, R2126 73.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190813
	2019.08.14	74.P39, Add Q3501, C3552 to support modern standby(Reserve)
	2019.08.15	75.P61, add C6506, C6107, C6108, C6109 for ESD protection 76.P21, Change R2165 from connect to mount 77.P49, Change R6525, R6526 to 13020-05980100 78.P56, Change R3634 from 1k ohm to 49.9 ohm (Follow PDG) 79.P21, Change R2150 from 33 ohm to 22 ohm (Follow PDG) 80.P20, Change R2061, R2062 from mount to unmount (Follow PDG) 81.P24, Add R2412 and mount on CRT(Follow CML CRB)
	2019.08.16	82.P73,P74, Change V73001, V73002, V74001, V74002 part number to 03014-00310400
	2019.08.17	83.P31, Mount J3102, D3125, R3132, C3106 ,mount J3105 for default setting 84.P56, connect C3609 for EMI suggestion 85.P24,P29, Change R2405, R2406 from 22 ohm to 33 ohm,R2417, R2421 from 22 ohm to 0hm (Follow VC) 86.P72, Connect R7701, R7702, R7703, R7704, R7705, R7706, R7707, R7708, R7709 to GND 87.P22, Change C2201, C2202 part number from 1122030307002S0 to 1122032307002S0 88.P40,P41, Change C4032, C4102, C4117 part number from 1122030305038S0 to 1122030305807S 89.P63, Change R5533 from 4.7k ohm to 100k ohm(Follow CML check list)
	2019.08.20	90.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190820 91.P47, Add R4724 mount R4717, R4723, R4702, R4722, remount R4703, R4725, R4726, R4728 for TI 3246 MOS reference 327 mode default setting
	2019.08.21	92.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190821 93.P48, Swap EN#2_VGI^ & EN#2_VG^ for layout routing 94.P56, Change Q3511 source JS402 from GND to unmount (Follow VC) 95.P63, Change R5324 from 20k ohm to 100k ohm(Follow VC)
	2019.08.22	96.P66, Change U6603, U6604 from 04070-00071100(BOL) to 04070-00071400 97.P50, Change JS001, JS002 from 12017310068 to 12017-0039300 to meet CML PDG 98.P31, Change R3016 footprint from 0603 to 0402 99.P91, Change EMC BOM solution from 07024-01560000 to 07024-01580000 100.P56, add C3606 for EMC request **以下修改料件需確認是否為SR BOM(分開編)**
	2019.08.23	101.P35, Mount R3569 for TP LED(Red Light Touch) 102.P69, Reserved C6955, C6956 for EMC suppression
	2019.08.26	103.P56, Change C3630, C3632 to unmount(Modify again 20190905(BOM 2 only)) 104.P55,P62, Change MPC_BAT_LOW_R-SCI# from off page to test point 105.P72, Delete C7004 for optimized layout routing 106.P31, Delete R3113, R3114, R3115, R3116 for CPU
	2019.08.27	107.P71, Reserved C7167, C7157 for EVVOS
	2019.08.28	108.P68, Add C6856, C6857 for VCCIO deep
	2019.08.28B	109.P56, Change JS402 from 06040-00340000 to 06033-00210000 110.P56, Remount C6603, C6604 for correcting Lightbar behavior (GX52M)

Rev	Date	Description
	2019.08.29	111.P20, Change R2005 from 0.3k ohm to 2.2k ohm
	2019.08.29	112.P24, Add R2415 (Intel RF service)
	2019.08.30	113.P32, Change R3312, R3301 from 10Z2111035175S0 to 10Z2111040075S0 114.P32, Mount R3214, R3215, R3205, R3206, remove 18206, 18205
	2019.09.04	115.P39, Change L3901, L3902, L3903, L3904 from 09002-00134200 to 09002-00130300
	2019.09.06	116.P73,P74,P78, Change V73001, V73002, V74001, V74002, R7819, R7834 optional to 770ohm and 1/770ohm
	2019.09.09	117.P33, Mount R3333, R3306, R3304, C5314 for modern standby verify
	2019.09.10	118.P33, Mount Q3301, C3302 for modern standby verify
	2019.09.11	119.P53, Change R5324 from 100K to 20K(Intel CRB2 check list Rev7.1)
R1.1	2019.09.18	120.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20190918 1.更換R6305, R6815A, R6815C, R6815B電阻1.47W 10K 1/(09019031 1k (2022-09027006) 2.更換R6306 10K OHM 1/10W (0402) 1% (10Z0220201160S) 3.更換R6815B電阻 220 OHM 1/16W (0402) 5% (10Z0220201160S) 4.更換R6815C電阻 1.47K OHM 1/16W (0402) 1% (10Z0214301160S) 5.更換R6815A電阻 24.7K OHM 1/16W (0402) 1% (10Z0224301160S) 6.更換R6307 27.4K OHM 1/16W (0402)1% (10Z0232740240S) 7.更換R6308 10K OHM 1/16W (0402) 1% (10Z0210301160S) 具有入24.1mA (10千歐之事) 8.更換R6309 150K OHM 1/16W (0402) 1% (10Z0251501160S)
	2019.09.23	121.P33, P53, Change USB_PS21_USB_PS11 part name to USB_PS14,USB_PS16
	2019.09.24	122.P32, Change D3202 footprint from s_sod-fp_SY_123x95_ss to s_sod-fp_SY_122x195 for avoiding sn sash
	2019.09.25	123.P22, Change R2201 from 07009-00002000 to 07009-00067000(2nd-07009-00068800) to meet CML-S PDG spec(series resistance) 124.P24 ,Change C2413, C2442 footprint from 0K to 0R5 for EMC
	2019.10.04	125.P31, Change R3114, R3115, R3116, R3117, R3118, R3119, R3120 optional from 0 to N/A to avoiding USB 2C current event
	2019.10.09	126.P56, Change Coder part number from 06033-01560000 to 06033-00360100
	2019.10.14	127.P56, update Type-C schematic(TYPE-C_AIC_DDR3-102 = DP = DP_TI_20190926)
	2019.10.17	128.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191015
	2019.10.22	129.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191022 130.SANTAL_GX52LC_MB_20191021_1 for test
	2019.10.23	131.P48, Change R6840(1) from 2.2k ohm to 10k(R6824, R6825) (Re and also change footprint for R6840 2.0 protocal HFI-54 tuneing 132.P48, Mount L6801 ,connect R6840(2) for HFI-4: Inter-Rain Zone - Clock
	2019.10.24A	133.P53, add R5520 for SLAS (x1 or 2x2 options)
	2019.10.24B	134.P40, reserved R4891, R4892, R4893, R4894, R4922, R4926 for IZ2Z 135.P20, reserved V2016, V2015, V2016 136.P25, add R2504, R2505 for GO 3.0
	2019.10.24B	137.P20, remove V2016
	2019.10.25	138.P70, change V7004 from 06004-01450000 to 06004-01490000 for GPU sequence optimize 139.P70,P73,P78,P25, Mount R7014, remount R7021, C7186, C7187, C71381, C7804, R2536 for GPU sequence optimize
	2019.10.29	140.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191029 141.Update GB83.2 20G test board schematic GB83.2_20G_ES_20191029_1
	2019.10.30	142.Update GB83.2 20G test board schematic GB83.2_20G_ES_20191030_1
	2019.10.30A	143.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191030 144.P28, Change R6280S2 from 4.7k ohm to 1k (R2801, R2802)(Re for SM6801 rising time 145.P28, Change R3004, R3007 from 10k to 4.7k for SM6800 rising time
	2019.11.1	146.P20, Change R6202 from 2.2k to 2k(R201, R2040) for CRT spec 147.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191101 148.P56, add R5606, R5611 for EMC board reserved 149.P56, mount C5631, C5606 for EMC request 150.P47, Reserved C4709, C4910, C4911, C4912 for V2 3246 power noise 151.P30,P39, add R3009, R3022, R3505 to changing CAP_LEDS from EC(C38, S28)) to Key(C38S28)
	2019.11.4	152.P47, Change L4709 from 120 ohm to 220 ohm to meet reference schematic and minimize pulse time
	2019.11.6	153.P48 Mount C4820 for correct output voltage 153.P25, reserved R2533 to control New TP_LED 154.P56, Change C3609 from 10000/16V to 10000/25V 155.P47, add Q4707, Q4708, R4703, R4704, R4712, R4714 for VCCSA_VCCIO_S5 & VGIO discharge(C18)
	2019.11.6B	156.P56, Remark C3609, Change C3606, C3632 from CapV to V00 for EMC request
	2019.11.6C	157.P57, add for R4714, C4701 for 12V1 VCCSUS, VCCSA1.0C & VCCIO discharge(C18)
	2019.11.07B	158.P65,P66, Remove EDC schematic to meet MET spec
	2019.11.08	159.P57, R4704, R4705, R4706, R4707, R4708, R4710, R4711, R4712, R4713, R4716, R4717, R4718, R4721, R4722, R4724 for TI 3246 I2C only
	2019.11.08A	160.P39, Change C3946, C3951, C3953 from 1000PF to 2200 PF for EMC Request 161.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191108

Rev	Date	Description
	2019.11.11	162.P30, Add R3011, R3014, R3015, R3017 for EC pin ADP_INSERT_MOS to avoid boot up issue 163.P56, Connect C3603, C3604 for connect light bar behavior
	2019.11.11B	164.P29,P30, add R2909, R3907, mount R2907 for TP_LED_ON
	2019.11.11C	165.P30, Remove R3014, change EC_GPIO8 to EC_GA20 for power sch request
	2019.11.12	166.P49,P61, Change JS001, JS101, JS102 ESD M.2 connector part number from 12005-00072500 to 12003-00148500
	2019.11.13	167.P67, Update CML GX52(L) DDR32_20191113_1 schematic
	2019.11.13B	168.P57, change R6711, R6716 from 1.8k to 7.5k for meet charge pump output current spec 169.P67, Update CML GX52(L) DDR32_20191113_2 schematic
	2019.11.14	170.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191114 171.P67, Update DDR3.2 20G schematic CML GX52(L) DDR32_20191114_2
	2019.11.14B	172.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191114_b 173.P67, Update DDR3.2 20G schematic CML GX52(L) DDR32_20191114_2
	2019.11.14C	174.P67, Update DDR3.2 20G schematic CML GX52(L) DDR32_20191114_4
	2019.11.15	175.P71, Change R7145 from 22k to 0 ohm to meet GPU power sequence spec
	2019.11.15B	176.P67, Update DDR3.2 20G schematic CML GX52(L) DDR32_20191115_1
	2019.11.18	177.P83, remark P83_R22, P83_R81_R12 not exec to USB_PS14_R12, USB_PS14_R12 for meet EOS part setup
	2019.11.18B	178.P67, Update DDR3.2 20G schematic CML GX52(L) DDR32_20191118_1
		確認如下料件需手改入BOM
	2019.11.18C	179.P56, Change Coder 07M018 part number from 06033-03360000 to 06033-03360100
	2019.11.19	180.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20191119 (R6801/L6801)(R6802 change 249 ohm 1%)(follow CML) 181.P56, Change C5405, C5404 from 100pF to 33 pF for tuning light bar behavior 182.P57, remove C5711 for ES check 183.P67, Update DDR3.2 20G schematic CML GX52(L) DDR32_20191119_1
	2019.11.20	184.P49, Change R4930 and R4937 from 0 ohm to 120 ohm bead(09021120104) 185.P39, Change L3901, L3902, L3903, L3904 from 120 ohm to 220ohm(09002-00196400)
	2019.11.21	186.P70, Change C7004, C7201, C7202, C7203, C7802, C7886, C7887, C7810 C7882, C7884, C7824, C7827, C7828, C7823, C7833, C7842, C7813, C7814, C7815, C7816, C7825, C7826 from 0.47uF to 1uF
R1.2	2019.11.26	187.P29,P30, remove R2907 , remark R3907 for TP LED control 188.P47, Follow Design ID update VGBC-C_ALC SSD3-102 = DP = DP_TI_20191126, Reserved R4727, R4730, R4718, R4719 & Mount R4736, R4737, R4738, R4739 for TI reference (Following GB83.2 spec. SSD) 189.P67, Add C7152 for +1V8_VCCSUS, VCCPLL_OC discharge(C10 sequence)
	2019.12.03	190.P24, Change R2435, R2436 from 33 ohm to 62 ohm (Ref Intel MOW WW47) 191.P30, add R3016 for reserved DDR core voltage control 192.P30, change EC_GPI7 net name to WOKE_SMB_SEL(follow VC) 193.P47, Add C4733, C4734, C5705, R4716, R4734, R4735, Q4709 for VCCIO & VCCSUS 194.P30, Add R3020, remount R3021 (Follow VC GX52MB)
	2019.12.05	195.P39, add R3509, R3522, R3523, R3525, R3526 for changing EC_MUTE# to GPC3_ GB83_DB83SB8 to GPC3_ / EC_LED_2# to LED1
	2019.12.10	196.P63, follow Design ID updateGB373027_REFERENCE_DSB_1220.DSB, remove C6009 ADD2 from SDA to SCL
	2020.01.02	197.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20200102 198.P50, follow Design ID updateGB373027_REFERENCE_DSB_1220.DSB, remove R5604 ADD2 from SDA to SCL 199.P20, Connect R4300S0(SMD Battery connector)
	2020.01.06	200.P67, Change R6705 MOS for driver from TI 3246 to TI 3148(06090-01480000) 201.P67, Remove GB83.2 Gen2 3p 2 test board
	2020.01.07	202.P68, Remove C6800, C6852, C6850, C6851, R6823, R6829, R6805, R6820 for optimized EMMC power solution 203.P33, P53, Remove Q3301, C3352, C3304, R6305, R6306, C5314 (Follow CML VC)
	2020.01.08	204.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20200107
	2020.01.08	205.P45, remount Q4304 for optimized +VTR_LCD discharge scenario
	2020.01.10	206.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20200108 207.P52, Change DS201, DS203 power from +V5S02 to +5V_DSB_CPU(follow Design ID)
	2020.01.10	208.P68, Change L26802, L26803, L26804 from 0 ohm to common choke to meet intel pair spec 209.P56, Change L3901, L3902, L3903, L3904 from 09020-00052000 to 09002-00070000 for EMI request
	2020.01.14	210.P71, add Q7122, R7103, R7107 for GPU power sequence with CPU(06004-01490100)
	2020.01.15	211.P71, Change R7120, R7105 from 10K ohm to 30.7 ohm for V9_MAX discharge
	2020.01.16	212.Update Power schematic GX52(L)LB_PWR_R1E0-02(CML)_CML-Y-Line_ES_20200115 213.P57, Mount R5711, change R5714, R5712 from 100k ohm to 1.5k ohm(Follow VC) 214.Change CPU part number from temp_U 023569 to 01001-01860100(SQ) 215.Change PCH part number from temp_U 023570 to 01001-00752200(SQ)
	2020.01.17	216.P24, Reserved C2405 for GB83.2 Gen2 optimized

EE PART

G512LI,G512LH,G712LI SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							

1. CPU: INT I7-7700HQ 2.8G/6M SR32Q BGA 01001-01380600
CPU: INT I5-7300HQ 2.5G/6M SR32S BGA 01001-01380500

2. dGPU: nVidia N17E-G2-A1 FCBGA2152 02004-00480500

4. EC: ITE IT8995VG-128/DX --06037-00050800

5.onboard menory
8G_ Hynix 03012-00030400

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

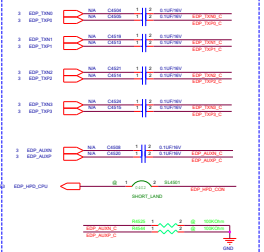
11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

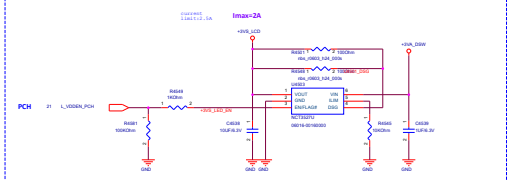
<Variant Name>

ASUSTeK COMPUTER	Title :	UX362_SKU Table_R1.0	
	Engineer:	Gaming RD	
Size: C	Project Name: G512LI		Rev: R1.0
Date: Monday, January 02, 2017	Sheet	of	103

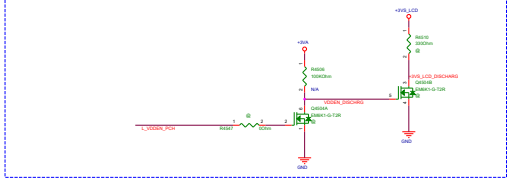
eDP from CPU



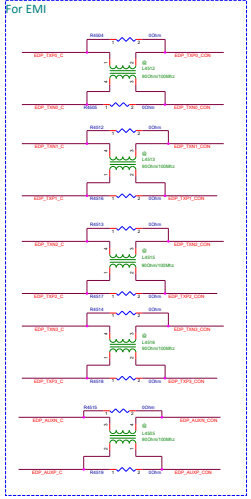
LCD Power switch



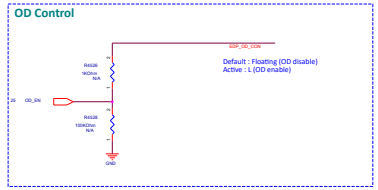
+3VS_LCD Discharge



For EMI

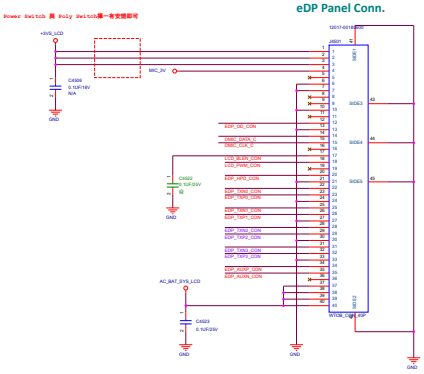


OD Control

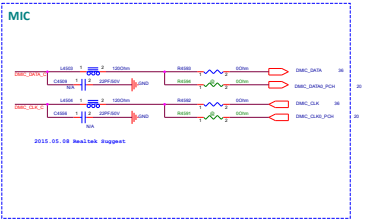


2017.05.03 Remove J4502 Pin 36 GND for Factory Issue

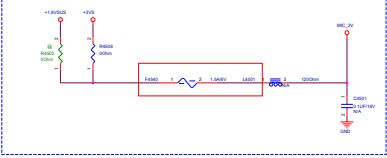
eDP Panel Conn.



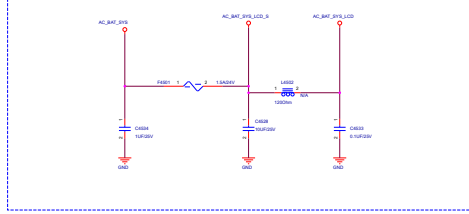
MIC



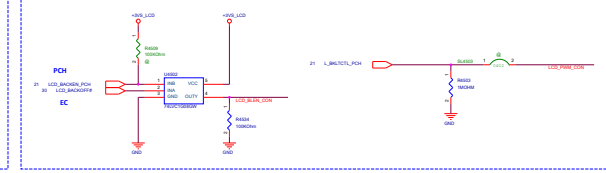
MIC module power



Panel BL Power



eDP_BL EN & eDP_BL PWM



ESD Protection

HDMI Active-Level Shift

Modify (20181018)

to GPU

Q4801只用07005-00660200與07005-00950000

From GPU

06106-00390100

SN75DP159RSBT

HDMI PWR_+5VS_HDMI

Remove SL4802 (20180927)

HDMI Conn.

20180810
R4816 change to 47Kohm

HDMI EMI

HDMI LDO 1.1VS

Imax = 0.35A

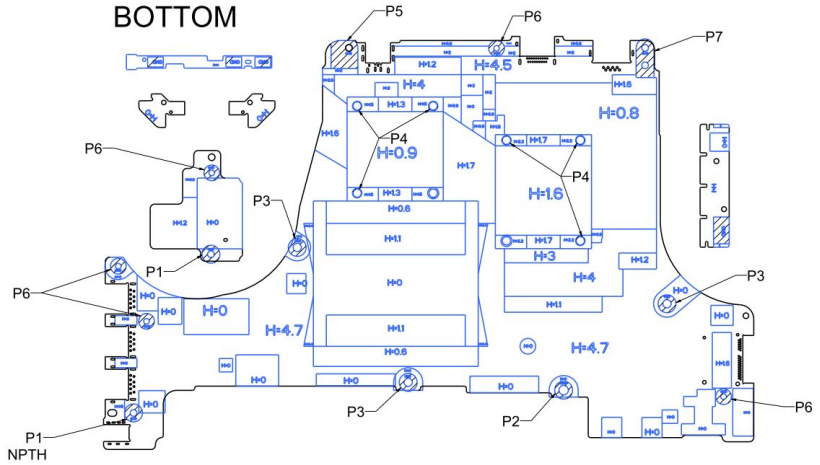
TLV75511PDQNR

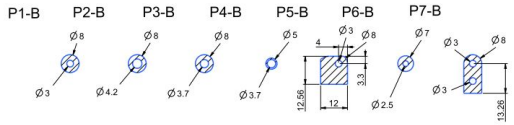
Imax = 0.35A

APL5930CQBI-TRG

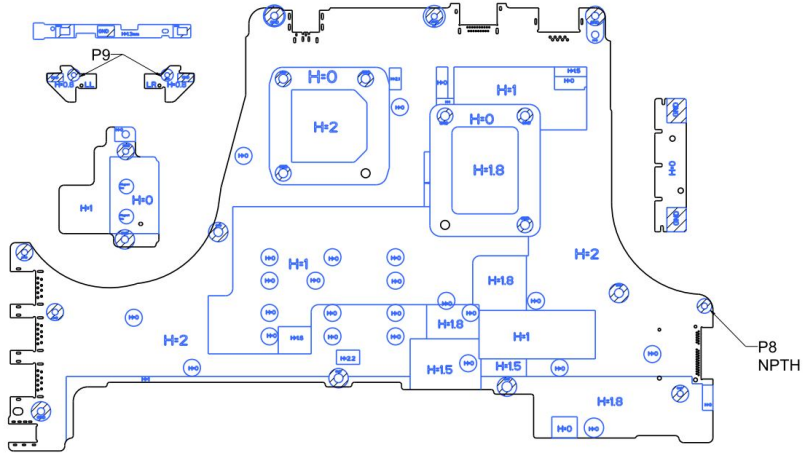
Project Name	G512LI
Rev	1.3
Title :	HDMI
Size	Custom
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	EE1_RD3
Date:	Monday, January 20, 2020
Sheet	48 of 103

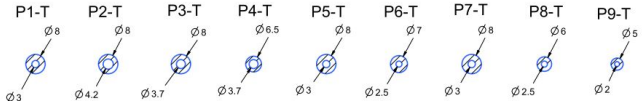
BOTTOM



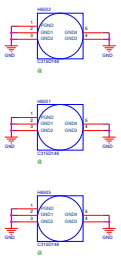


TOP

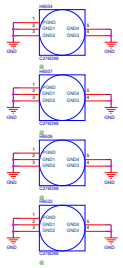




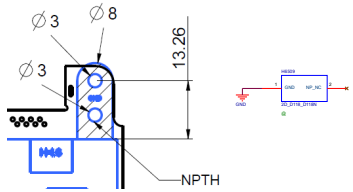
P3: PTH 8 /3.7mm



P6: PTH 7 /2.5mm

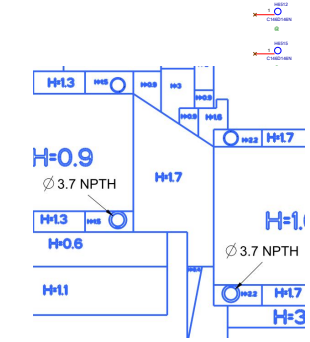


P7: PTH 8 /3mm+ NPTH 3mm

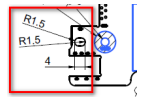


P4: PTH 6.5 /5 /3.7 mm

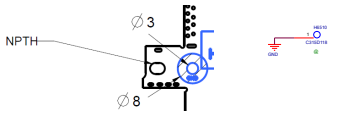
NPTH 3.7 mm



NPTH 1.5/ 4mm

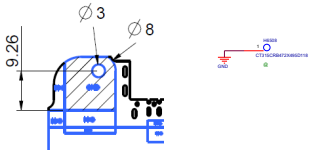


P1: PTH 8 /3 mm

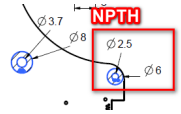


P2: PTH 8 /4.2 mm

P5: PTH 8/3mm (Ext.)



NPTH 6/ 2.5 mm



Title :	MC Screw Hole & Nut
Engineer:	Gaming RD
Project Name	G512LI

MEMORY: GPU FB Partition A

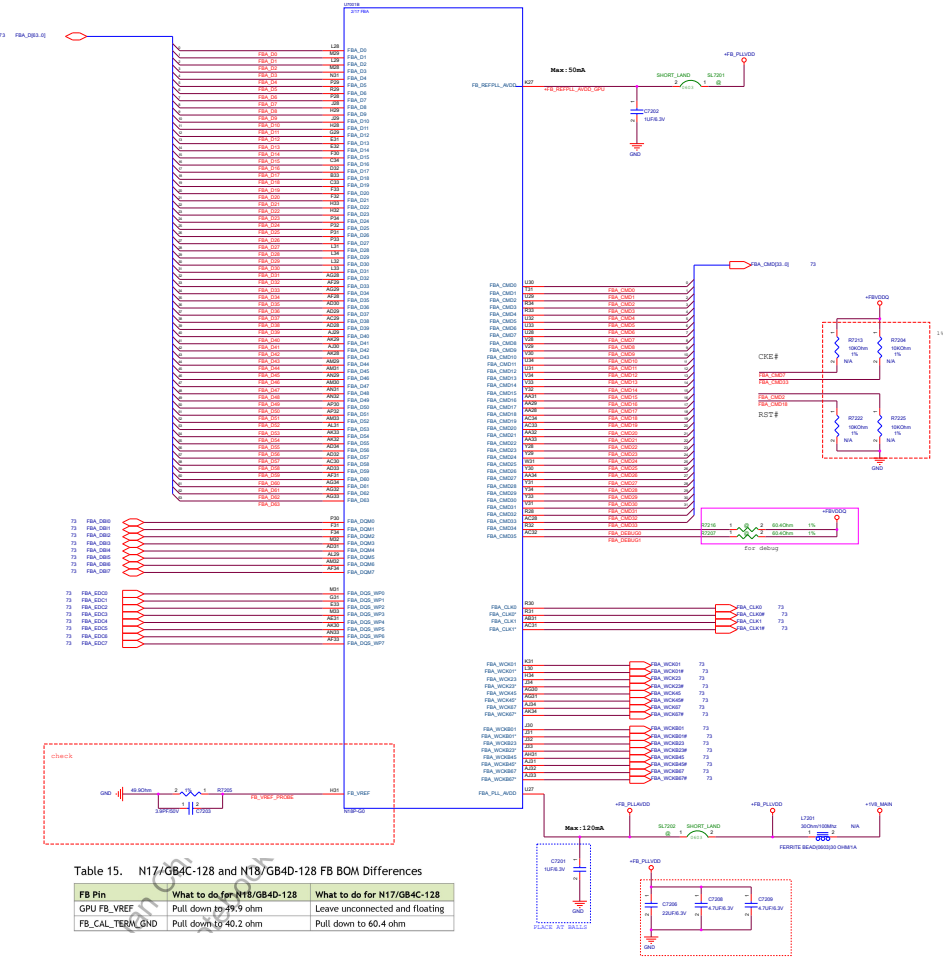
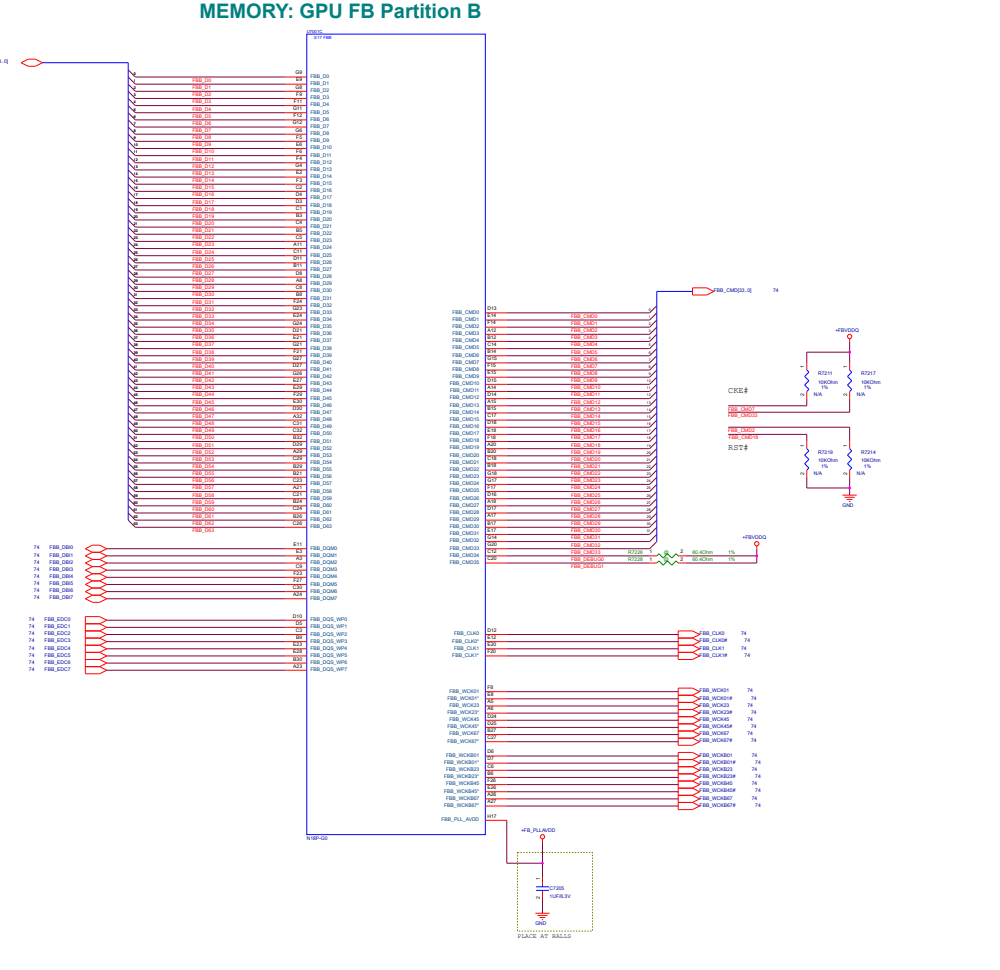


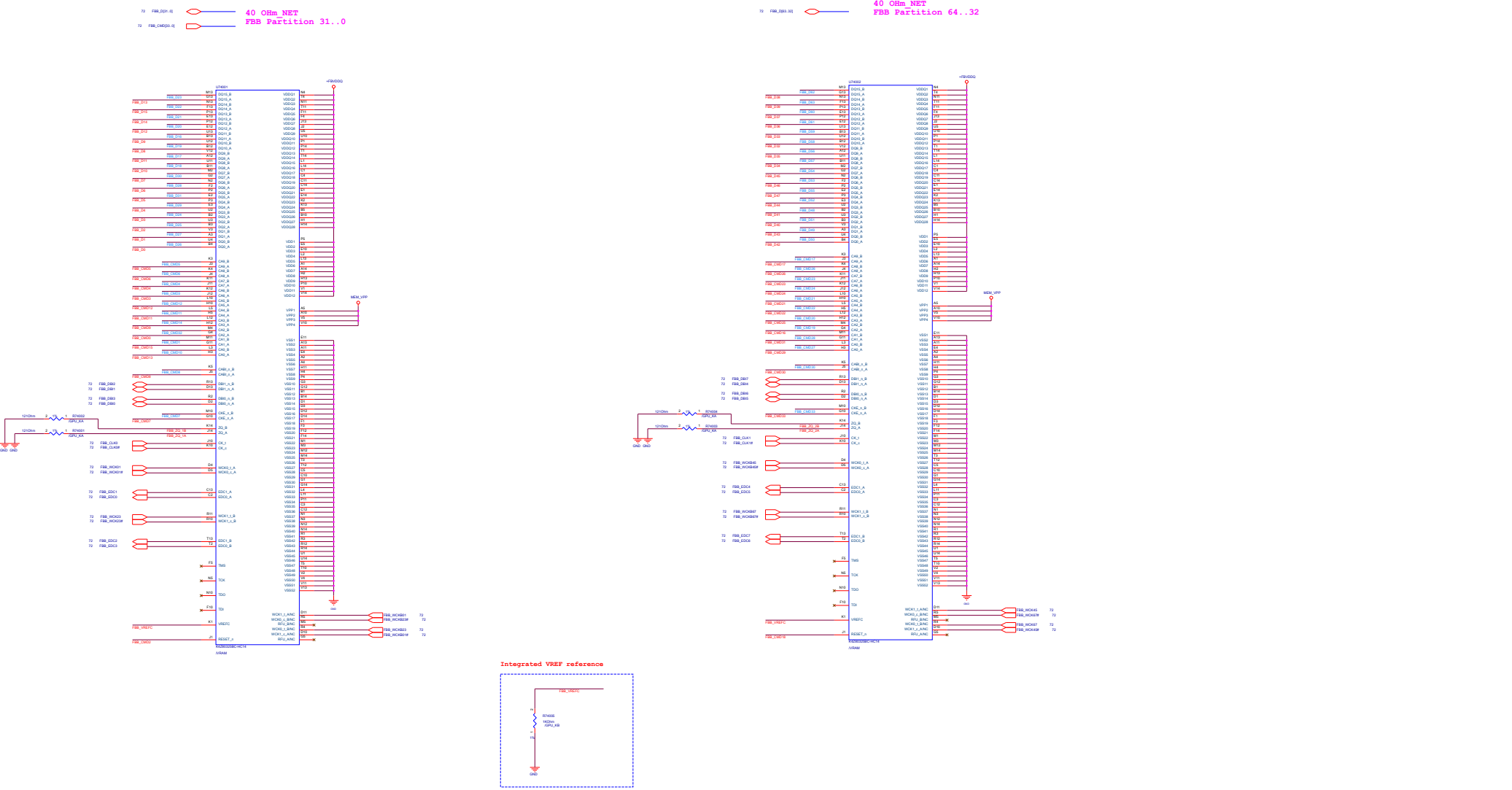
Table 15. N17-GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

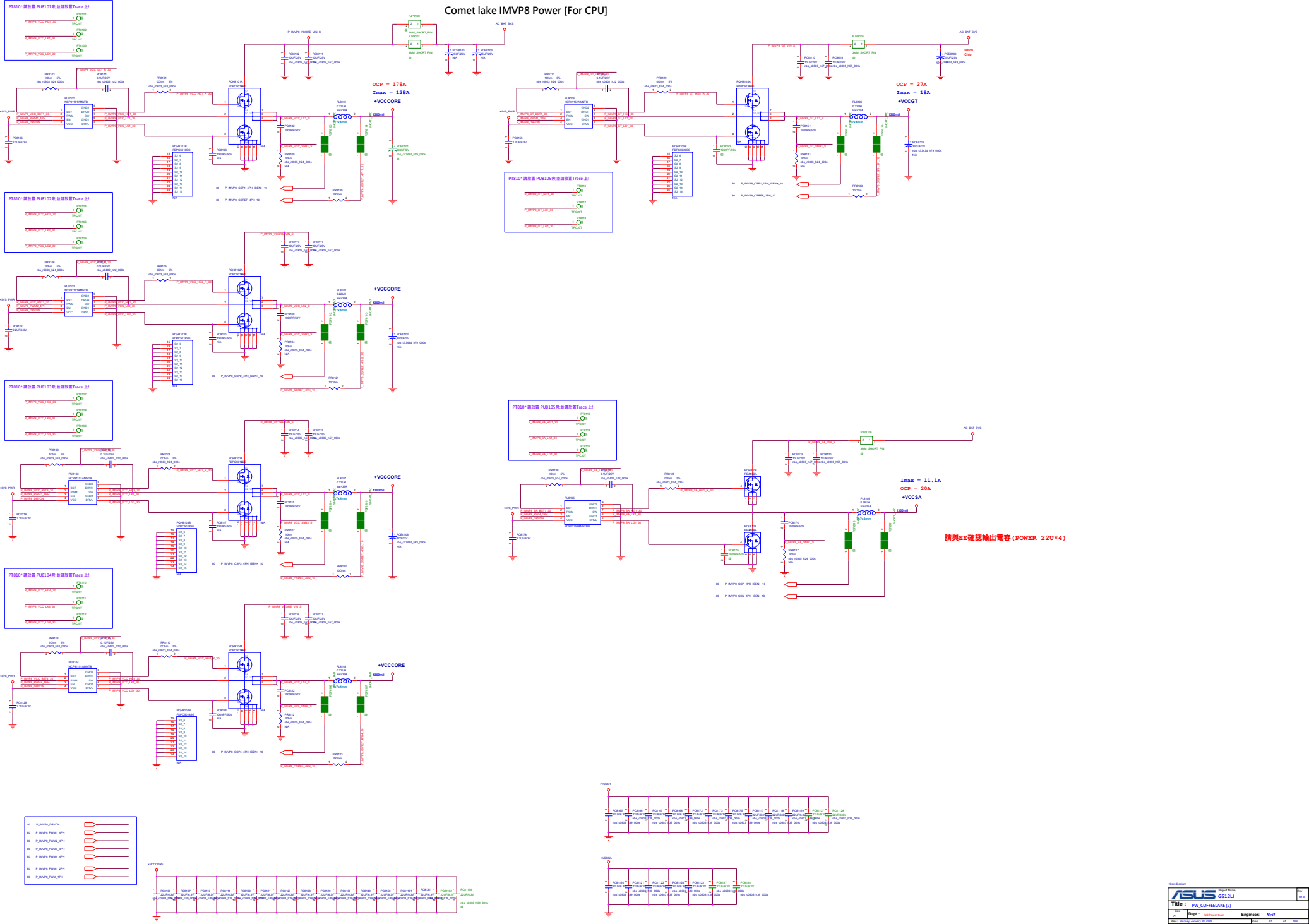
MEMORY: GPU FB Partition B



ASUS	Project Name: G512LI			Rev: R1.0
Title : GPU_FRAME BUFFER				
Size: _	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD		
Date: Monday, January 20, 2020	Sheet: 72	of: 193		

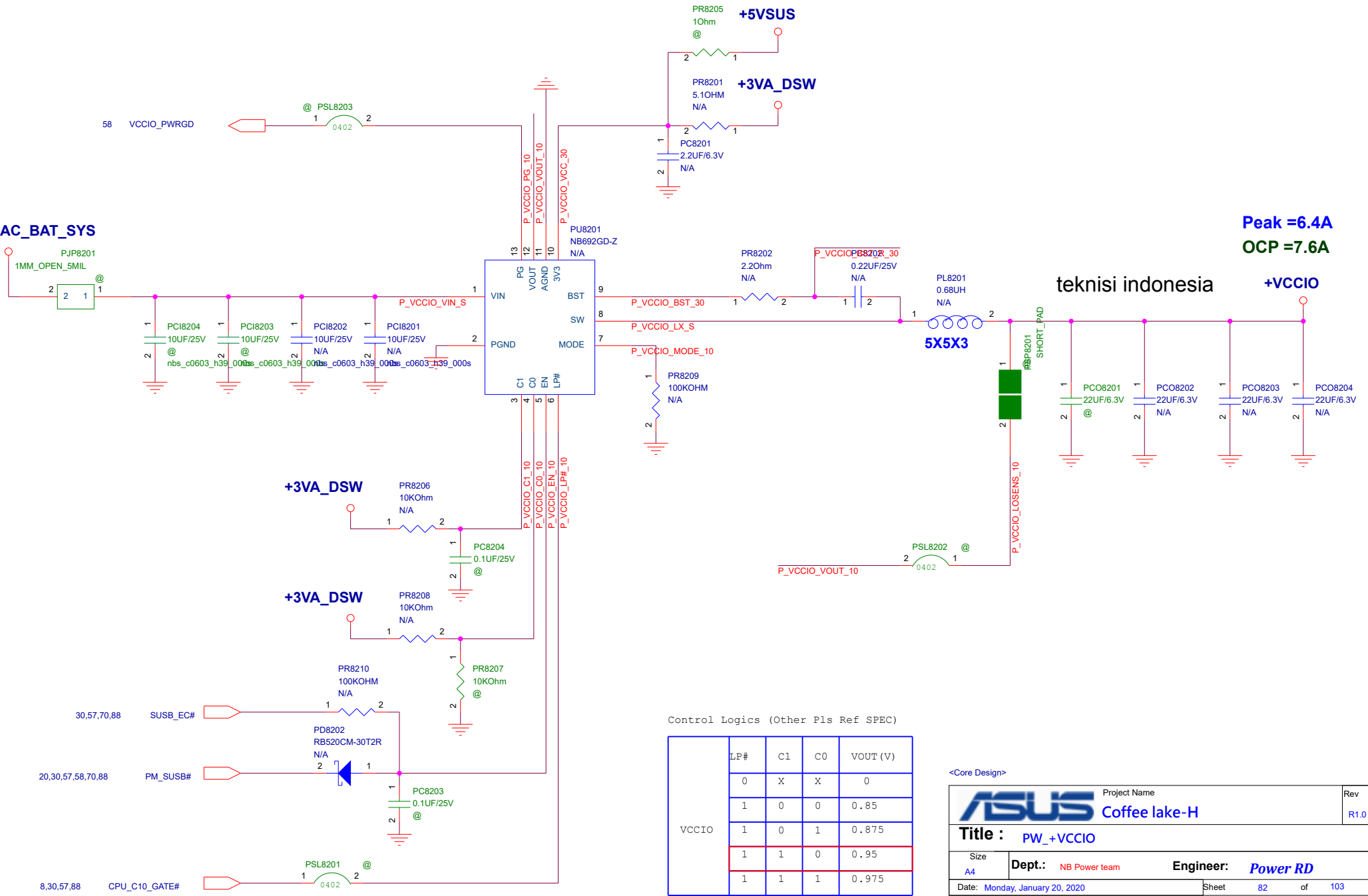

40 OHm_NET
FBB Partition 31..0
40 OHm_NET
FBB Partition 64..32
Integrated VREF reference

Comet lake IMVP8 Power [For CPU]



ASUS	Project Name: G512LI		Rev: R1.0
Title :	PW_COFFEELAKE (2)		
Size: A3	Dept.: NB Power team	Engineer: Neil	
Date: Monday, January 20, 2020		Sheet 91 of 103	

+VCCIO [For CPU]



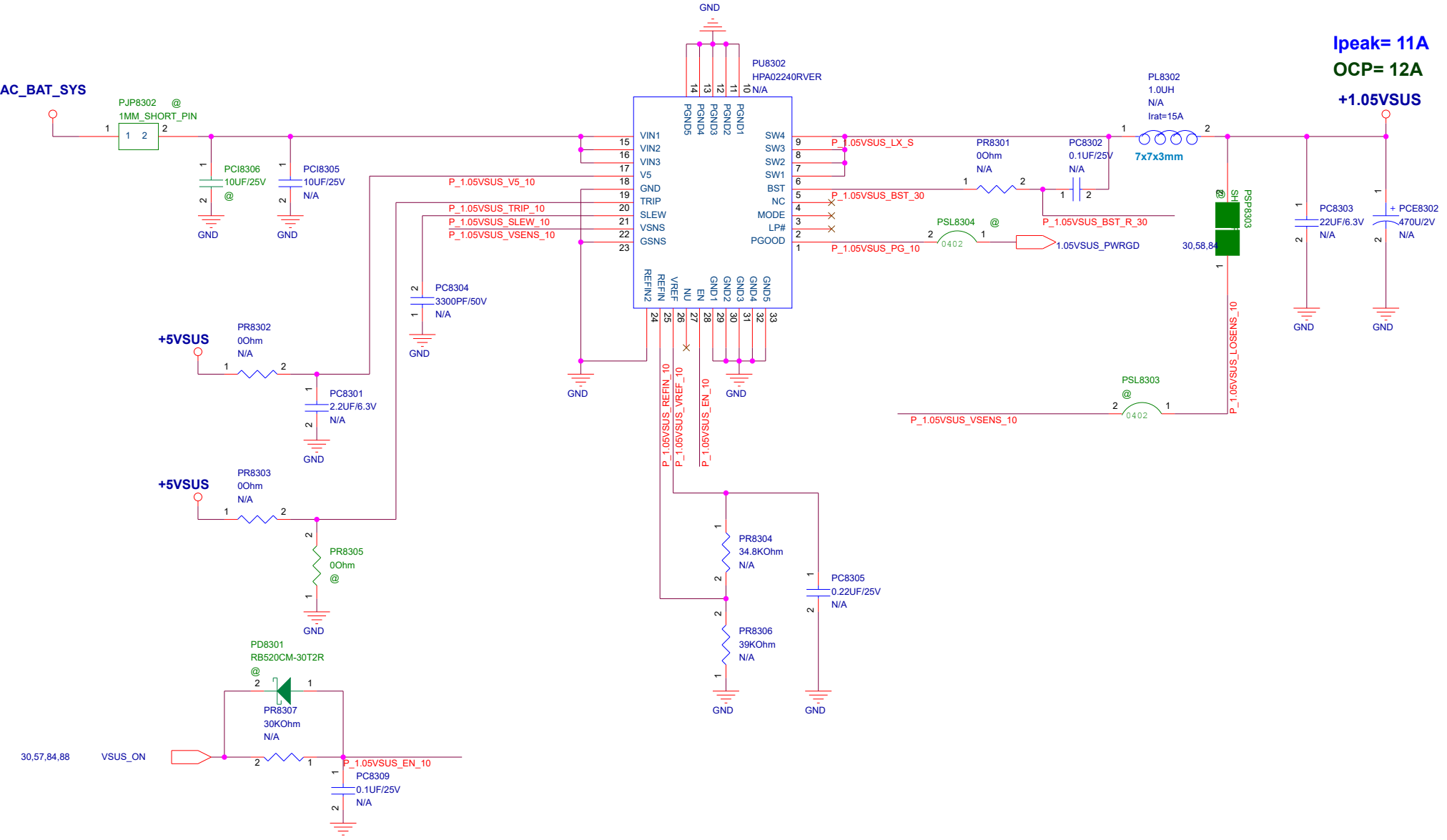
Control Logics (Other Pls Ref SPEC)

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

<Core Design>

Project Name: Coffee lake-H		Rev: R1.0
Title : PW_+VCCIO		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Monday, January 20, 2020	Sheet 82 of 103	

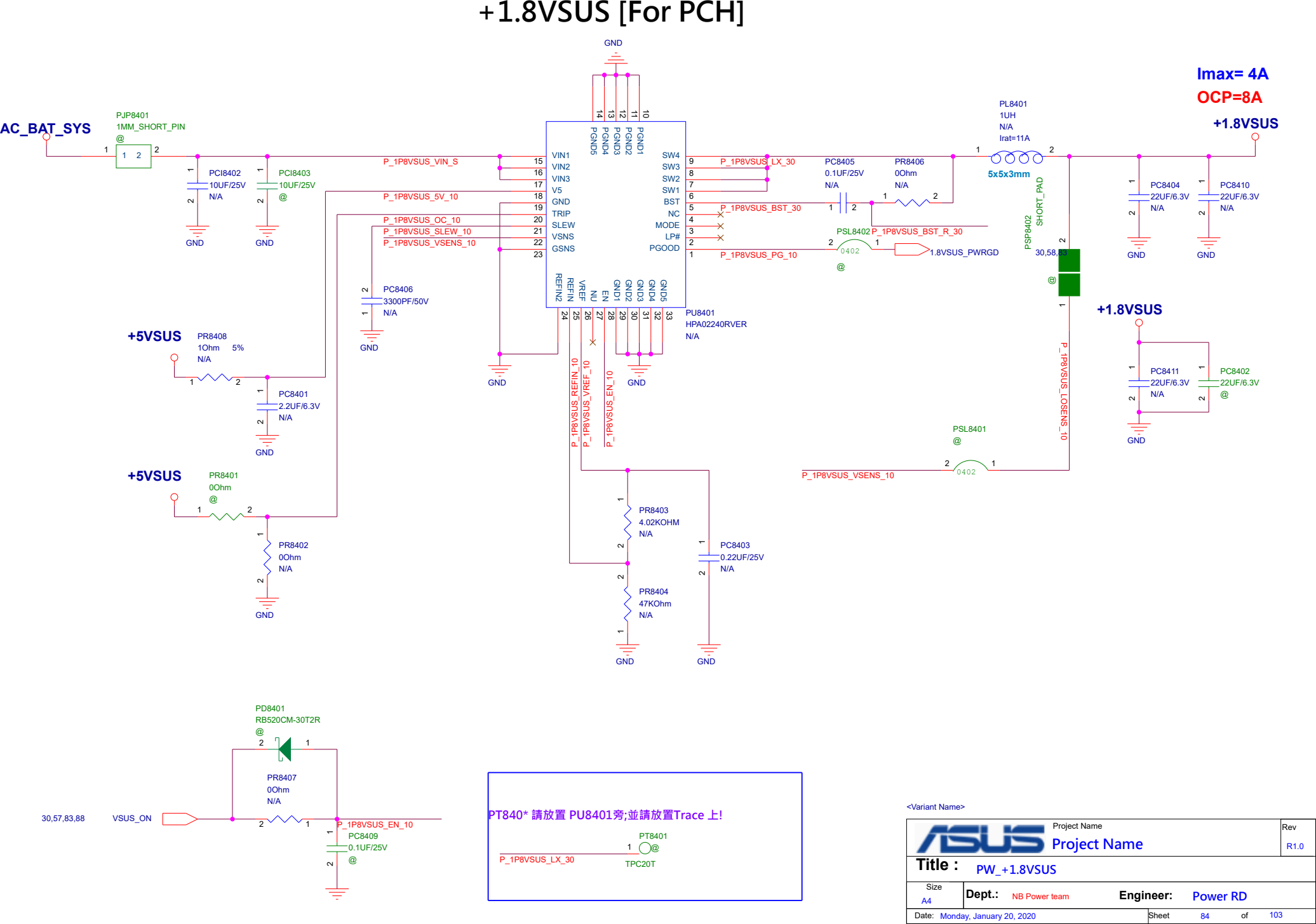
+1.05VSUS [For PCH]



PT840* 請放置 PU8401旁;並請放置Trace 上!

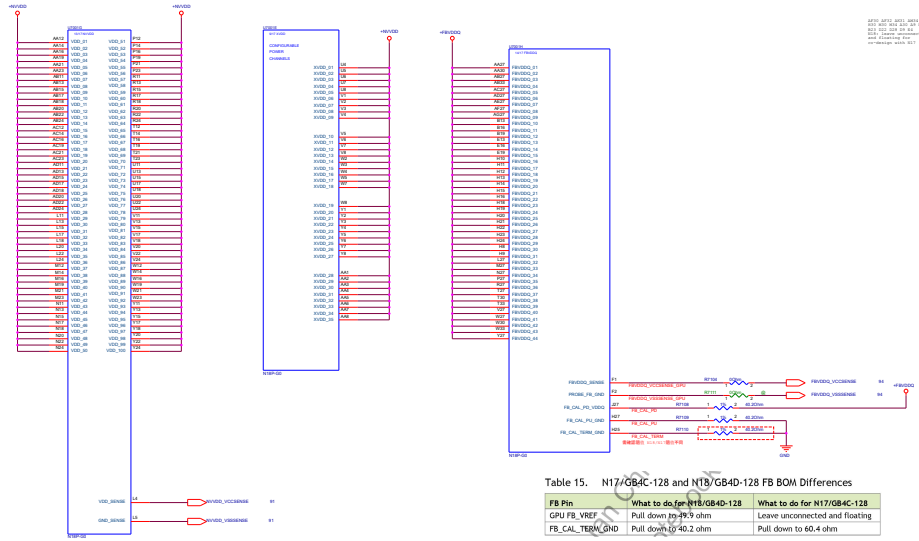
Project Name: Coffe Lake-H		Rev: R1.0
Title : PW_+1.0VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Monday, January 20, 2020	Sheet 83 of 103	

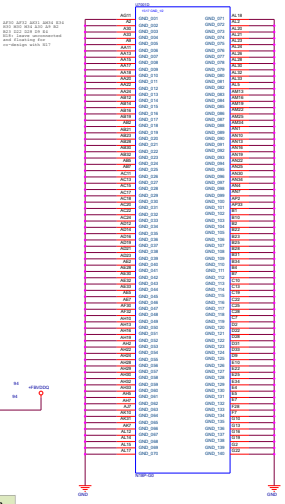
+1.8VSUS [For PCH]

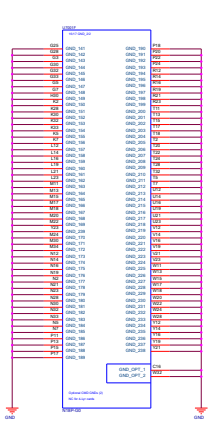


<Variant Name>

Project Name: Project Name		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Monday, January 20, 2020	Sheet 84 of 103	







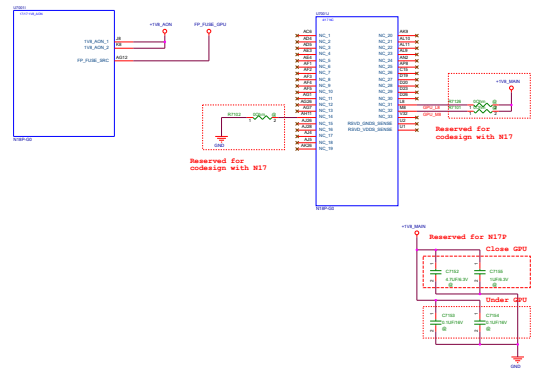
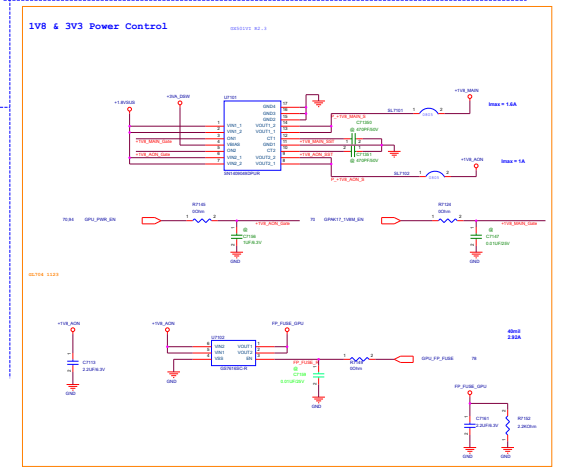
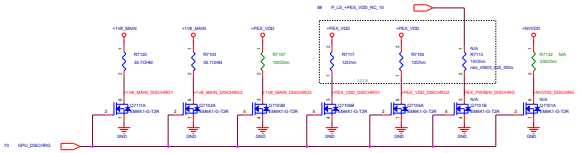


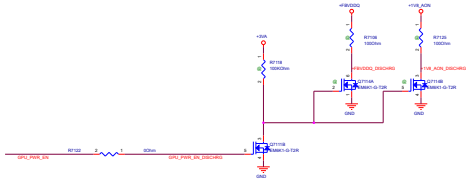
Table 15. N17-GB4C-128 and N18/GB4D-128 FB BOM Differences

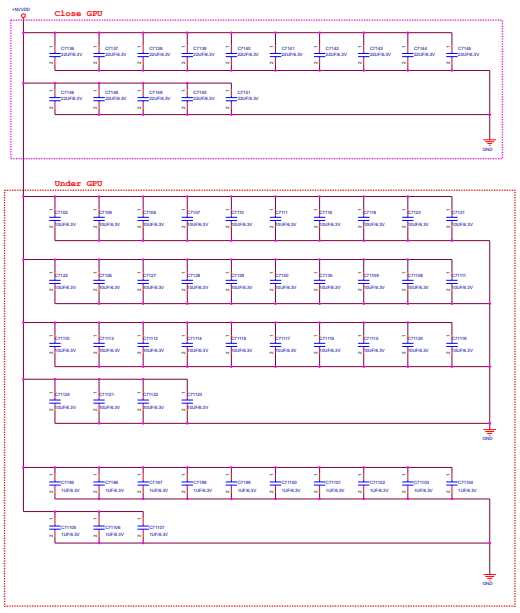
FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

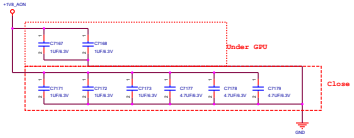


Discharge









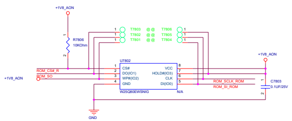
GB4D-128 Package				
NVVDD		Varies	26 x 0.47uF (0201W X6S) 34 x 10uF (0603 X6S) - - - - - - - - - - - - - - - - Alternate solution: 13 x 1uF (0402 or 0201W, X6S) [3] 34 x 10uF (0603 X6S)	15 x 22uF (0805 X6S)
1V8_AON	2	1.8V	4 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - Alternate solution: 2 x 1uF (0402 or 0201W, X6S) [3]	6 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) - - - - - - - - - - - - - - - - Alternate solution: 3 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603, X6S)

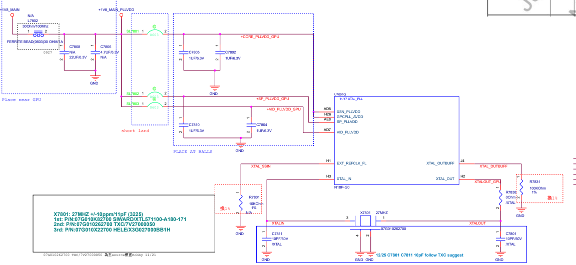
NVVDD CAP(Ref. sch)
22UF/6.3V x15
10UF/6.3V x34
0.47UF/6.3V x26

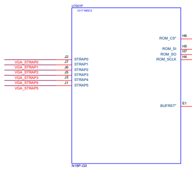
+1V8 AON CAP(Ref. sch)
0.47UF/6.3V x4
4.7UF/6.3V x3
0.47UF/6.3V x6

ASUS	Project Name: G512LI		Rev: 2.0
Title: GPU_POWER			
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ashton_yang	
Date: Monday, January 20, 2020		Sheet: 71 of 100	

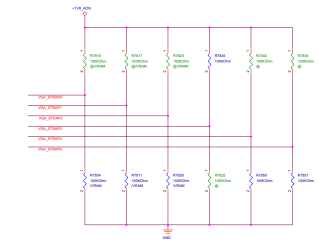
IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S, one per ball) - - - - - - - - Alternate solution: 3 x 1uF (0402 or 0201W, X6S, one per ball)	1 x 4.7uF (0603 X6S) 1 x 22uF (0805 X6S) 1 x 30Ω bead (0603 max ESR 0.01 Ω)
IFPCD_PLLVDD	1			
IFPE_PLLVDD	1			
GPCPLL_AVDDx XSN_PLLVDD	2		2 x 0.47uF (0201W X6S) - - - - - - - - Alternate solution: 2 x 1uF (0402 or 0201W, X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) - - - - - - - - Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) - - - - - - - - Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	

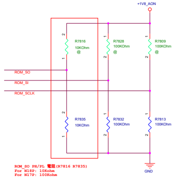






STRAP PIN





	Physical Configuration	
Level Option	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

Assorted Configuration Straps

1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2CS address 0x9E, "1" Dual GPU setting I2CS address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0"normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

for N18x

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

for N17x

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	is eDP Supported on: IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	See This Row of Table 5.4
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

Table 5. N18P-G62/G61 GDDR6 Recommended Memories

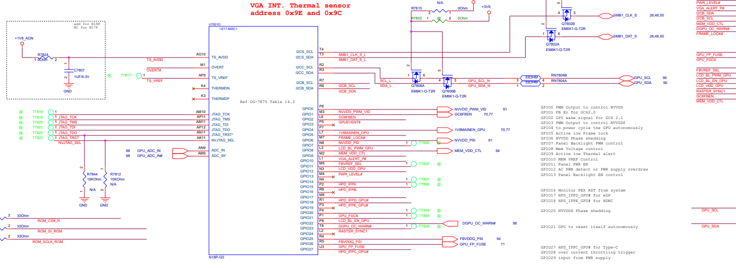
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.25V[3]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD[2, 4]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD[2, 5]	Full	Production candidate

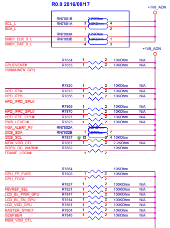
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

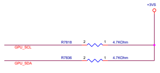
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

VGA INT. Thermal sensor address 0x9E and 0x9C

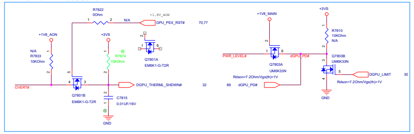




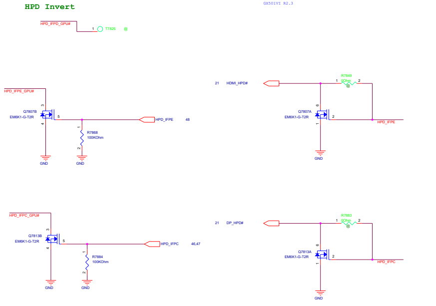


VGA EXT. Thermal Sensor

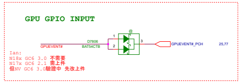
Thermal Protection



Level shift
HPD Invert



GPU GPIO INPUT



NVIDIA GC6 2.0 follow DG-07290-001_v01
GPU_GPIO 5 --> FRAME_LOCK# (Input, Open Drain)
High-->driver display ,Low Normal

FRAME_LOCK#_C Pull High +3VS_LCD at Panel side

Table 15.1 GPIO Descriptions for GB4D-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	No PU/PD
GPIO1	GC6: GC6_FB_EN	I/O	FB Enable for GC6 2.1	10 kΩ pull-down
GPIO2	GC6:GPU_EVENT	I/O	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	UNUSED	O		
GPIO4	GC6: 1V8_MAIN_EN	I	GPU power sequencing for GC6 2.1	10 kΩ pull-up to 1V8_AON
GPIO5	FRAME_LOCK*	O	Active low Frame Lock	10 kΩ pull-up to 1V8_AON
GPIO6	NVVDD_PSI*		Phase Shedding (see Section 15.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	LCD Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10K Pull Up to 1V8_AON
GPIO15	HPD_IFPB*	I	Hot Plug	10K Pull Up to 1V8_AON
GPIO16	UNUSED			
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10K Pull Up to 1V8_AON
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_AON
GPIO19	UNUSED	O		
GPIO20	GC6:NB_GC6	I/O		10K Pull Down
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100K Pull Down
GPIO22	INA_HT* / ADC_MUX_SEL			2.2K Pull Up See circuit
GPIO23	Reserved			100K Pull Down
GPIO24	UNUSED	I		
GPIO25	FBVDD_PSI*			PU/PD with series resistor depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot plug detect for IFPC	10K Pull Up to 1V8_AON

ASUS Project Name: G512LI		Rev 2.0
Title : GPU_CLOCK/STRAP/GPIO		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
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