MS-7A70

mATX:243*226

Ver: 10

Intel -KabyLake-S plamform

CPU:

LGA1151

*CPU POWER PAK *3 Phase*

*GT POWER PAK *2 Phase*

System Chipset:

SPT-H :B250 colay H270

Onboard Chip:

HD Audio Codec: ALC892

SIO: NCT6795D

Flash ROM: SPI 64 MB

PWM:

VCORE - RT3606

DDR - RT8125E

PCH(1.0V) - RT8125E

VCCSA - RT8125E

VCCIO - NB681(Converter)

VPP25 - MP2147

Main Memory:

*DDR4 * 4 (Dual Channel)*

LDO:

VCCSTPLL - GS7133

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+PN MOS

3VDSW:GS7133

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

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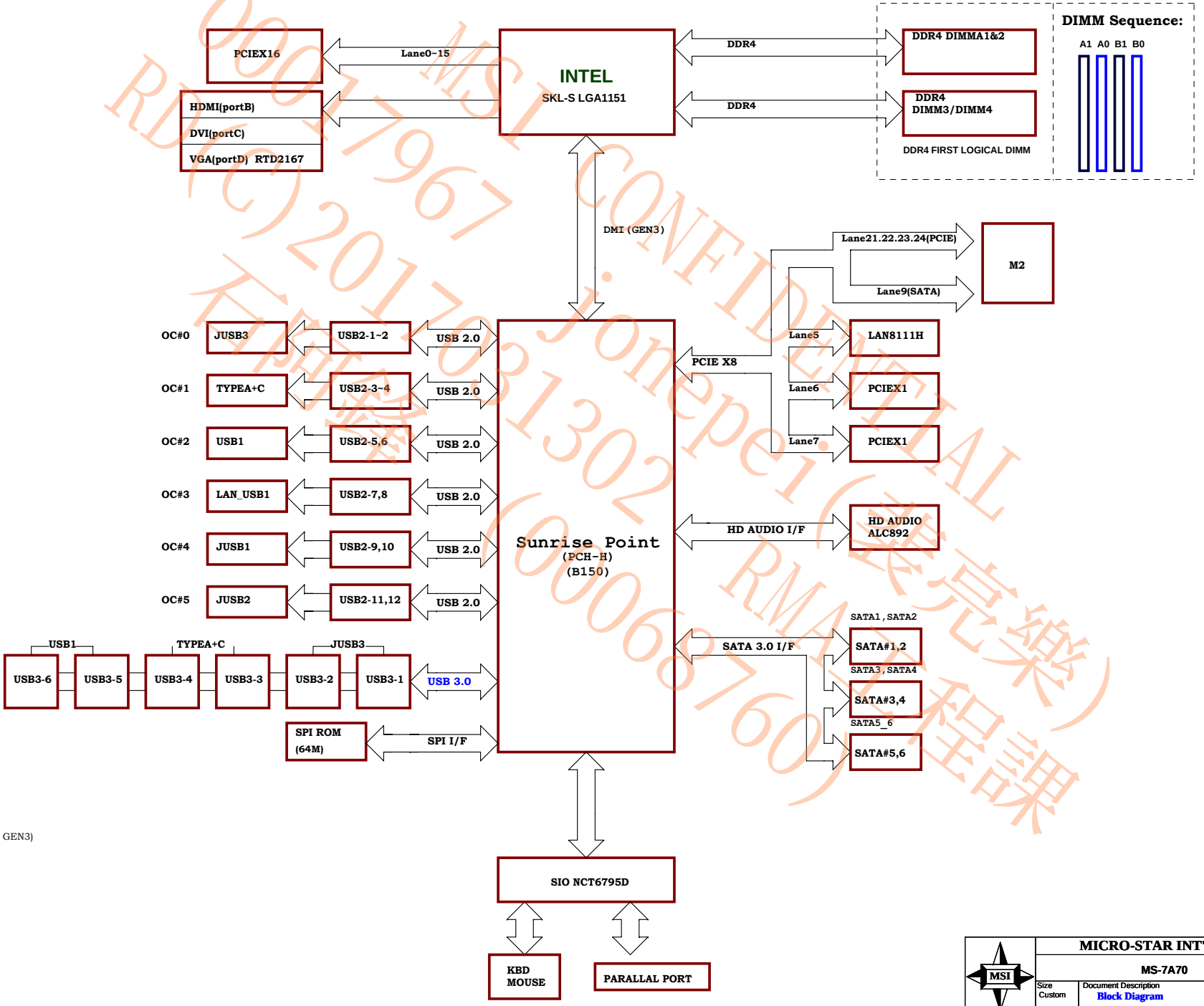
Size: Custom | Document Description: Cover Sheet | Rev: 10

Date: Monday, September 12, 2016 | Sheet 1 of 56

MS-7A70 Block Diagram



Slot Sequence:

PCIE X16	(By CPU GEN3)
PCIE X1	(By PCH GEN3)
PCIE X1	(By PCH GEN3)

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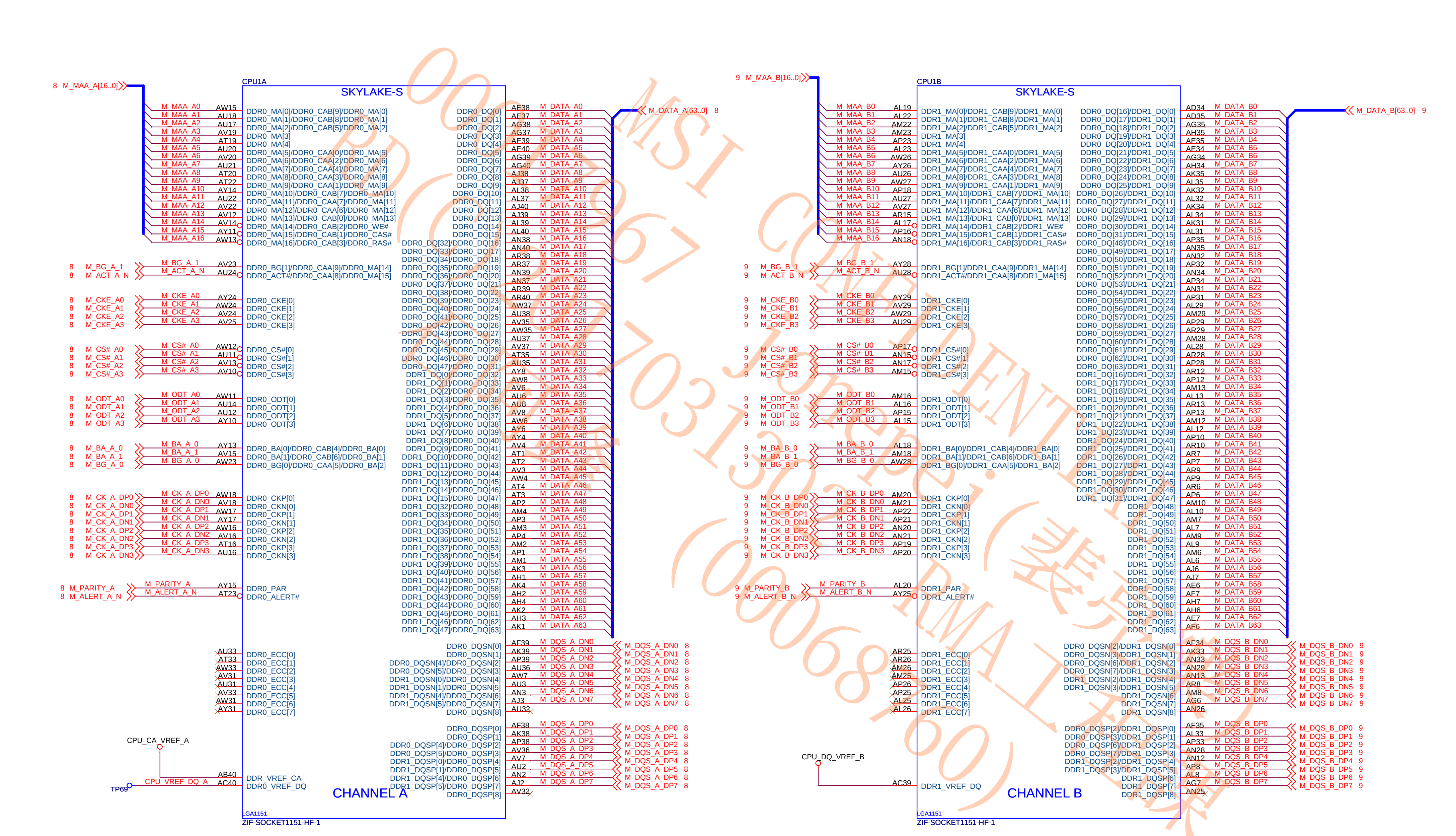
Size: Custom | Document Description: Block Diagram | Rev: 10

Date: Wednesday, September 14, 2016 | Sheet 2 of 56



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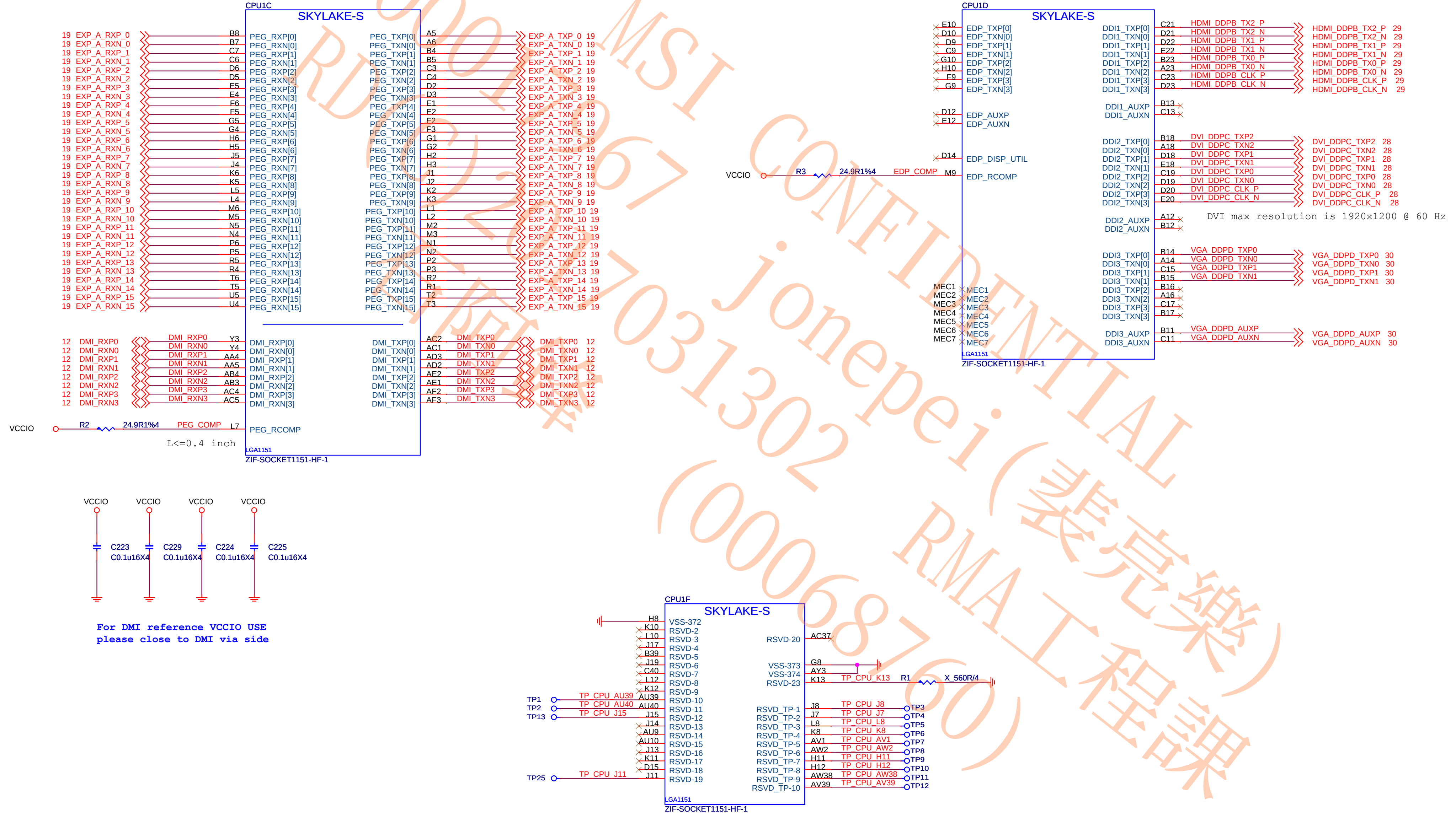
MS-7A70

Size	Document Description	Rev
Custom	CPU-Memory	10

Date: Monday, September 12, 2016 | Sheet 3 of 56

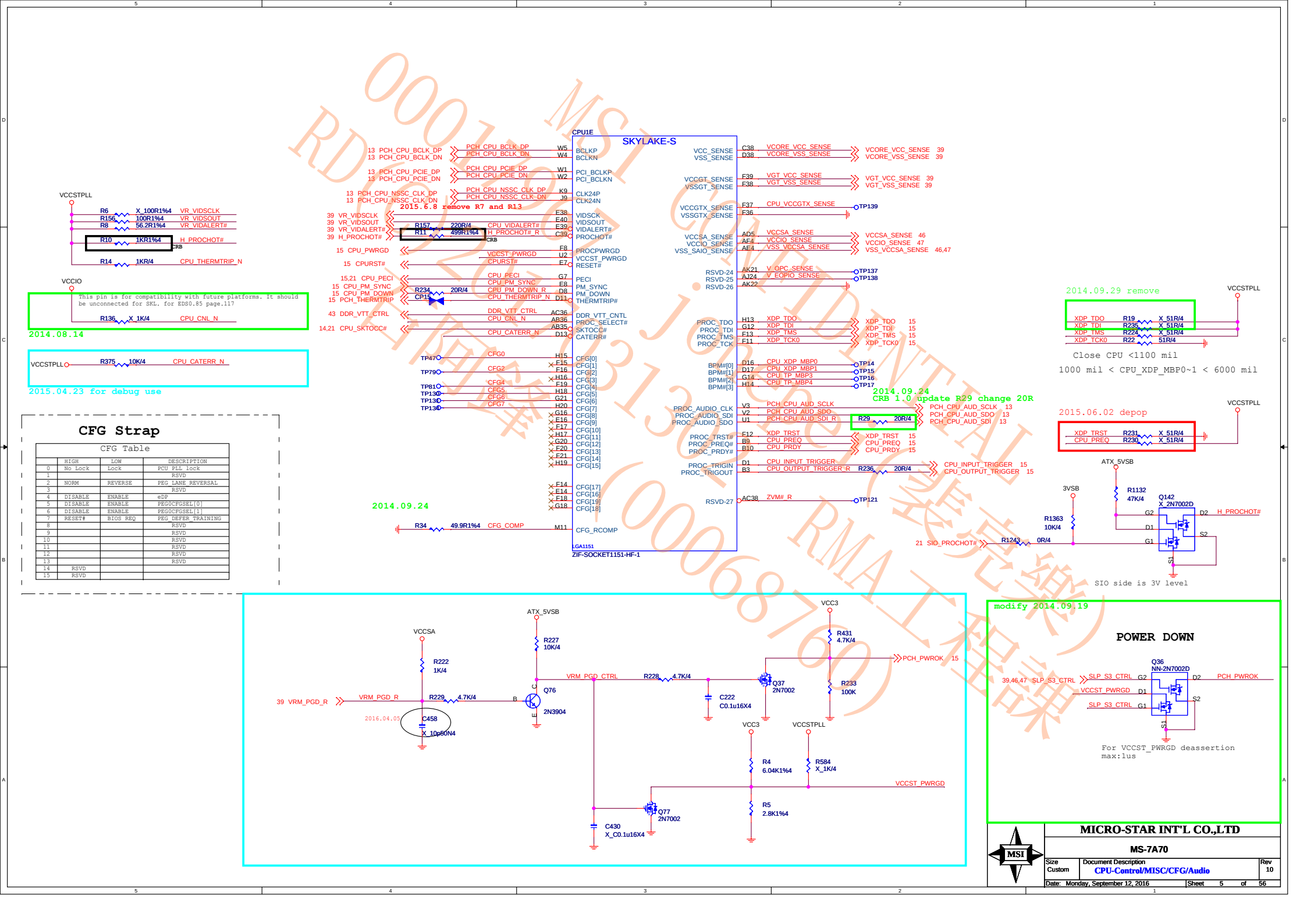


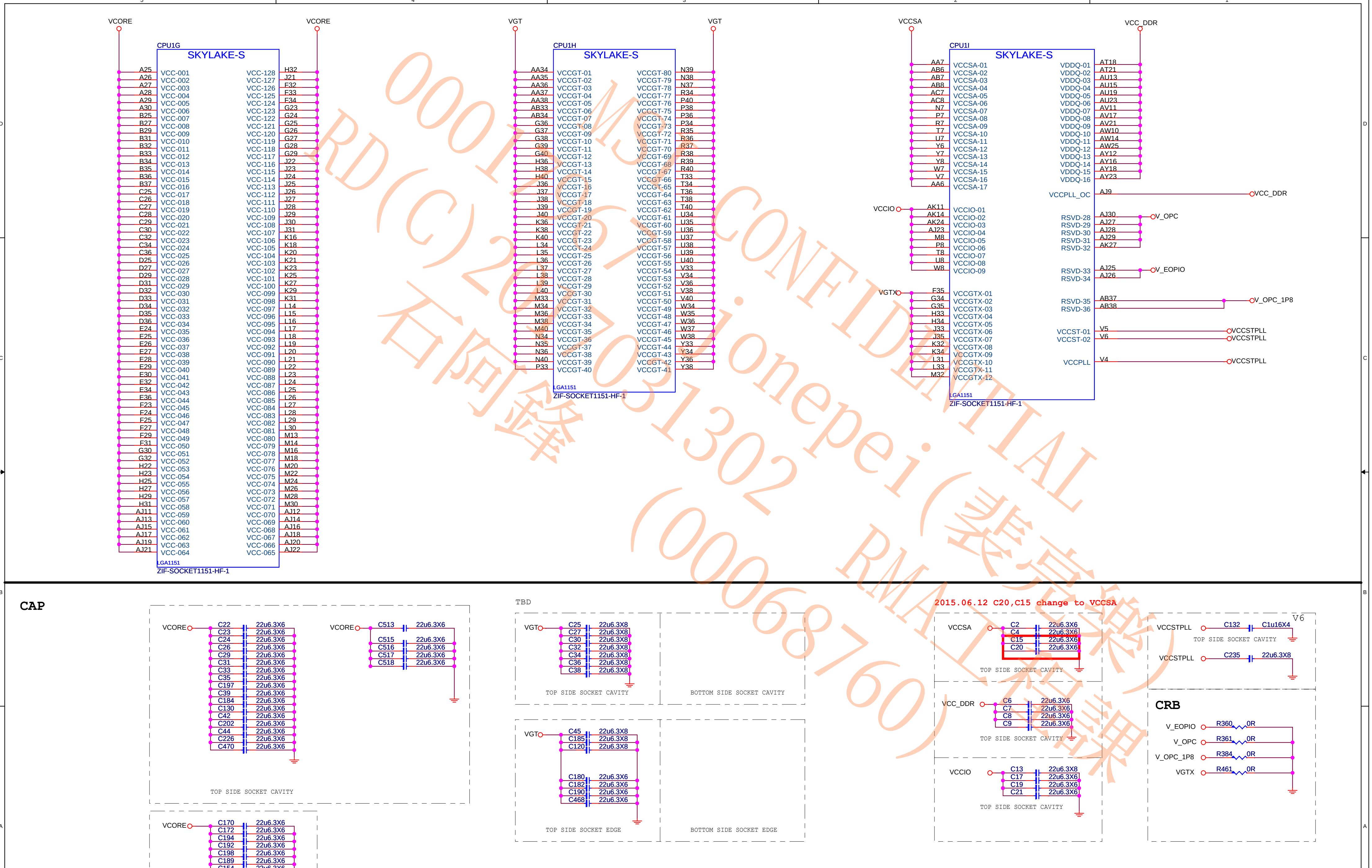
MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	CPU-PEG/Display	10

Date: Monday, September 12, 2016 Sheet 4 of 56


VCCSTPLL
R6 X_100R1%4 VR_VIDSCLK
R156 100R1%4 VR_VIDSOUT
R8 56.2R1%4 VR_VIDALERT#
R10 1KR1%4 H_PROCHOT#
CRB
R14 1KR/4 CPU_THERMTRIP_N
VCCIO
This pin is for compatibility with future platforms. It should be unconnected for SKL. for EDS0.85 page.117
R136 X_1K/4 CPU_CNL_N
2014.08.14
VCCSTPLL R375 10K/4 CPU_CATERR_N
2015.04.23 for debug use
CFG Strap
CFG Table
HIGH LOW DESCRIPTION
0 No Lock Lock PCU PLL lock
1 RSVD
2 NORM REVERSE PEG LANE REVERSAL
3 RSVD
4 DISABLE ENABLE eDP
5 DISABLE ENABLE PEG0CFGSEL[0]
6 DISABLE ENABLE PEG0CFGSEL[1]
7 RESET# BIOS REQ PEG DEFER TRAINING
8 RSVD
9 RSVD
10 RSVD
11 RSVD
12 RSVD
13 RSVD
14 RSVD
15 RSVD
CPU1E
SKYLAKE-S
13 PCH_CPU_BCLK_DP
13 PCH_CPU_BCLK_DN
BCLKP
BCLKN
13 PCH_CPU_PCIE_DP
13 PCH_CPU_PCIE_DN
PCI_BCLKP
PCI_BCLKN
13 PCH_CPU_NSSC_CLK_DP
13 PCH_CPU_NSSC_CLK_DN
CLK24P
CLK24N
2015.6.8 remove R7 and R13
39 VR_VIDSCLK
39 VR_VIDSOUT
39 VR_VIDALERT#
39 H_PROCHOT#
R157 220R/4
R11 499R1%4
CRB
VIDSCK
VIDSOUT
VIDALERT#
PROCHOT#
15 CPU_PWRGD
PROCPWRGD
VCCST_PWRGD
15 CPURST#
RESET#
15,21 CPU_PECI
15 CPU_PM_SYNC
15 CPU_PM_DOWN
15 PCH_THERMTRIP
R234 20R/4
CP15
PECI
PM_SYNC
PM_DOWN
THERMTRIP#
43 DDR_VTT_CTRL
DDR_VTT_CNTL
PROC_SELECT#
14,21 CPU_SKTOCC#
SKTOCC#
CPU_CATERR_N
CATERR#
TP47
TP79
TP81
TP130
TP131
TP134
CFG0
CFG2
CFG4
CFG5
CFG6
CFG7
CFG[0]
CFG[1]
CFG[2]
CFG[3]
CFG[4]
CFG[5]
CFG[6]
CFG[7]
CFG[8]
CFG[9]
CFG[10]
CFG[11]
CFG[12]
CFG[13]
CFG[14]
CFG[15]
CFG[16]
CFG[17]
CFG[18]
CFG[19]
2014.09.24
R34 49.9R1%4 CFG_COMP
CFG_RCOMP
LGA1151
ZIF-SOCKET1151-HF-1
VCC_SENSE
VSS_SENSE
VCORE_VCC_SENSE 39
VCORE_VSS_SENSE 39
VCCGT_SENSE
VSSGT_SENSE
VGT_VCC_SENSE 39
VGT_VSS_SENSE 39
VCCGTX_SENSE
VSSGTX_SENSE
CPU_VCCGTX_SENSE
TP139
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VCCSA_SENSE 46
VCCIO_SENSE 47
VSS_VCCSA_SENSE 46,47
RSVD-24
RSVD-25
RSVD-26
V_OPC_SENSE
V_EOPIO_SENSE
TP137
TP138
PROC_TDO
PROC_TDI
PROC_TMS
PROC_TCK
XDP_TDO 15
XDP_TDI 15
XDP_TMS 15
XDP_TCK0 15
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
CPU_XDP_MBP0
CPU_XDP_MBP1
CPU_TP_MBP3
CPU_TP_MBP4
TP14
TP15
TP16
TP17
2014.09.24
CRB 1.0 update R29 change 20R
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
PCH_CPU_AUD_SCLK
PCH_CPU_AUD_SDO
PCH_CPU_AUD_SDI_R
R29 20R/4
PCH_CPU_AUD_SCLK 13
PCH_CPU_AUD_SDO 13
PCH_CPU_AUD_SDI 13
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
XDP_TRST
CPU_PREQ
CPU_PRDY
XDP_TRST 15
CPU_PREQ 15
CPU_PRDY 15
PROC_TRIGIN
PROC_TRIGOUT
CPU_INPUT_TRIGGER
CPU_OUTPUT_TRIGGER_R
R236 20R/4
CPU_INPUT_TRIGGER 15
CPU_OUTPUT_TRIGGER 15
RSVD-27
AC38 ZVM#_R
TP121
2014.09.29 remove
XDP_TDO R19 X_51R/4
XDP_TDI R235 X_51R/4
XDP_TMS R224 X_51R/4
XDP_TCK0 R22 51R/4
Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil
2015.06.02 depop
XDP_TRST R231 X_51R/4
CPU_PREQ R230 X_51R/4
ATX_5VSB
3VSB
R1132 47K/4
Q142 X_2N7002D
R1363 10K/4
21 SIO_PROCHOT#
R1243 0R/4
H_PROCHOT#
SIO side is 3V level
VCCSA
R222 1K/4
ATX_5VSB
R227 10K/4
39 VRM_PGD_R
VRM_PGD_R
R229 4.7K/4
2016.04.05
C458 X_10p50N4
Q76 2N3904
VRM_PGD_CTRL
R228 4.7K/4
C222 C0.1u16X4
VCC3
R431 4.7K/4
Q37 2N7002
PCH_PWROK 15
R233 100K
VCC3
VCCSTPLL
R4 6.04K1%4
R584 X_1K/4
VCCST_PWRGD
R5 2.8K1%4
Q77 2N7002
C430 X_C0.1u16X4
modify 2014.09.19
POWER DOWN
Q36 NN-2N7002D
39,46,47 SLP_S3_CTRL
SLP_S3_CTRL
VCCST_PWRGD
PCH_PWROK
For VCCST_PWRGD deassertion max:1us
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size Custom
Document Description CPU-Control/MISC/CFG/Audio
Rev 10
Date: Monday, September 12, 2016
Sheet 5 of 56



MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	CPU-Power	10

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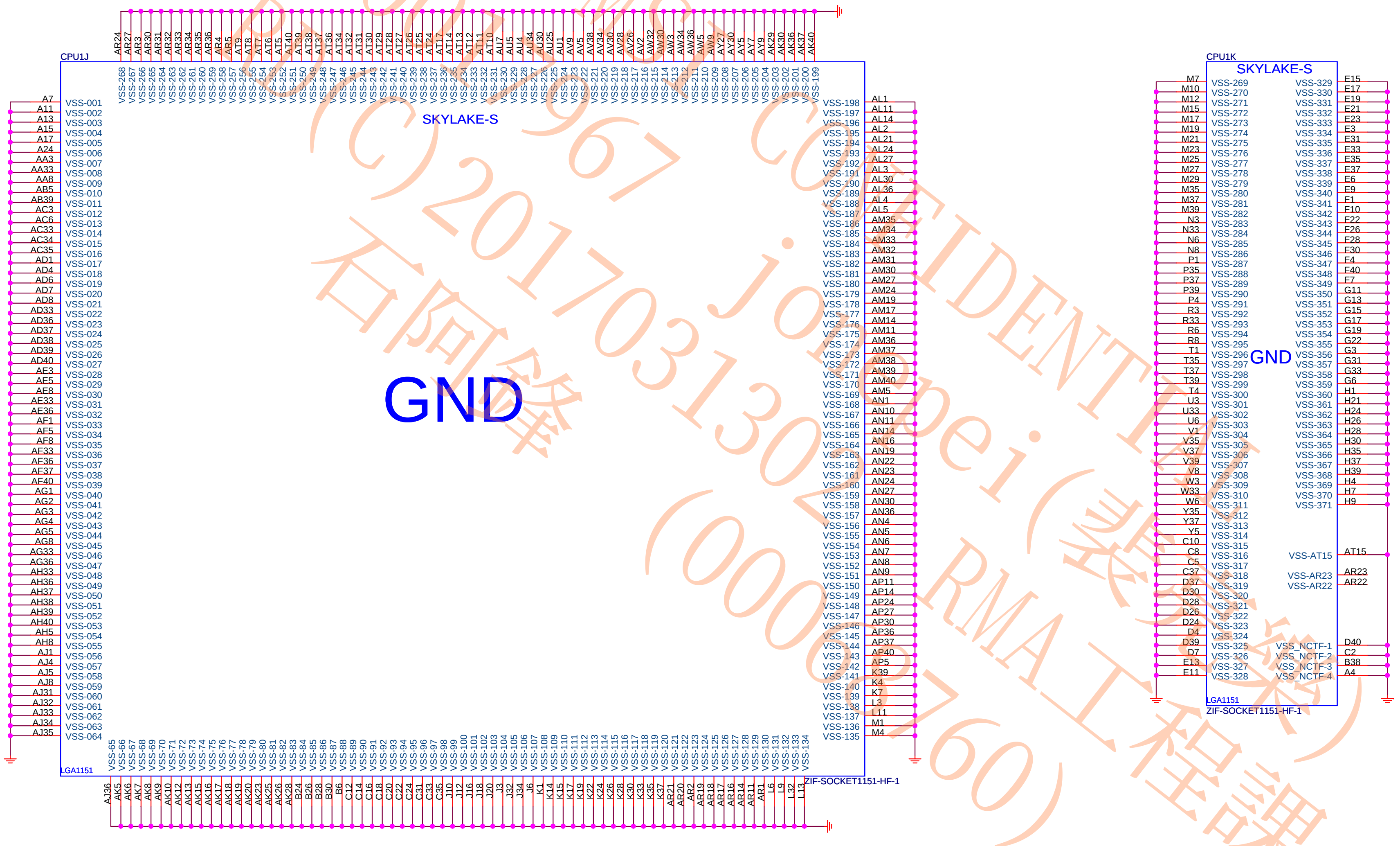
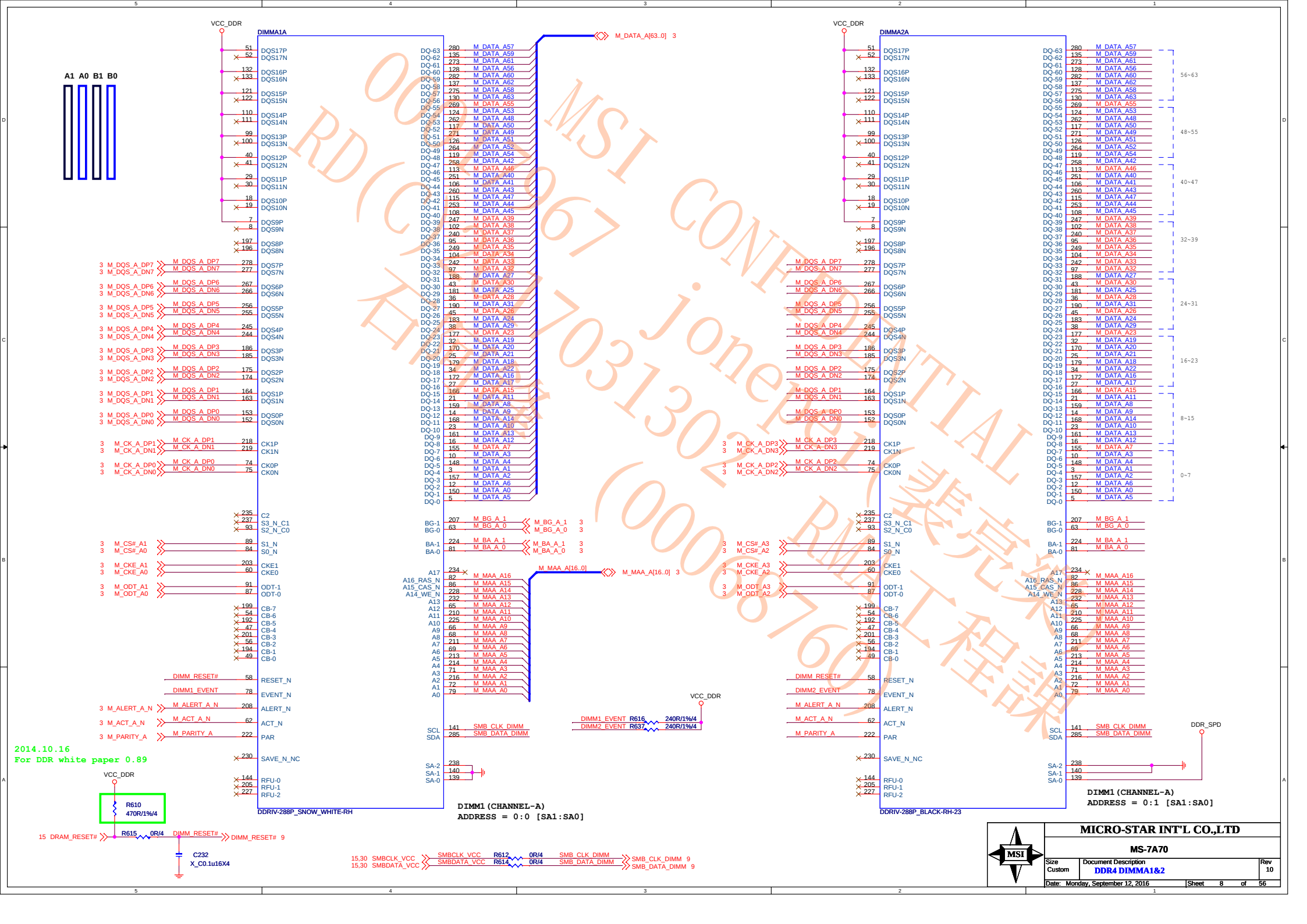


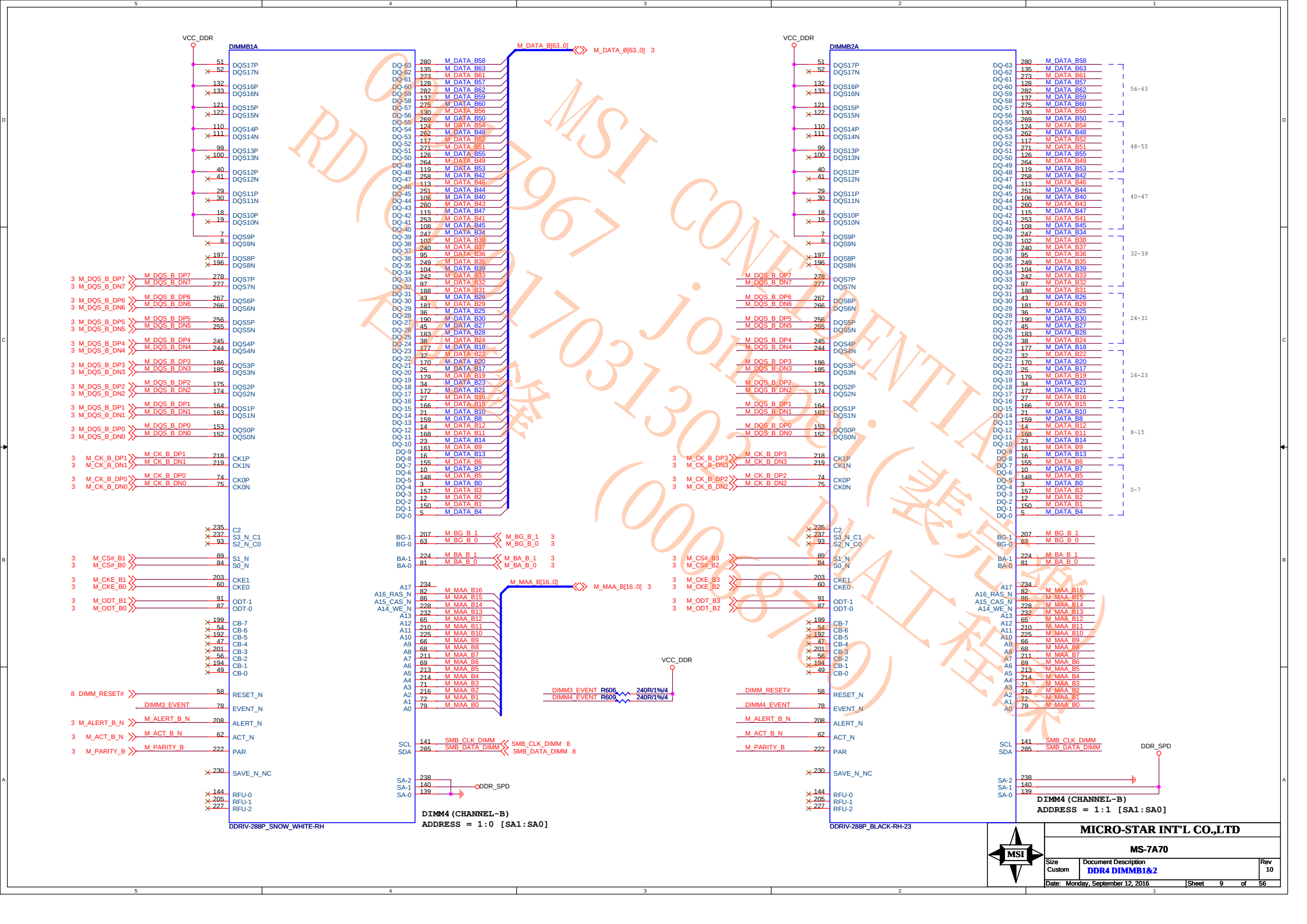
MICRO-STAR INT'L CO.,LTD

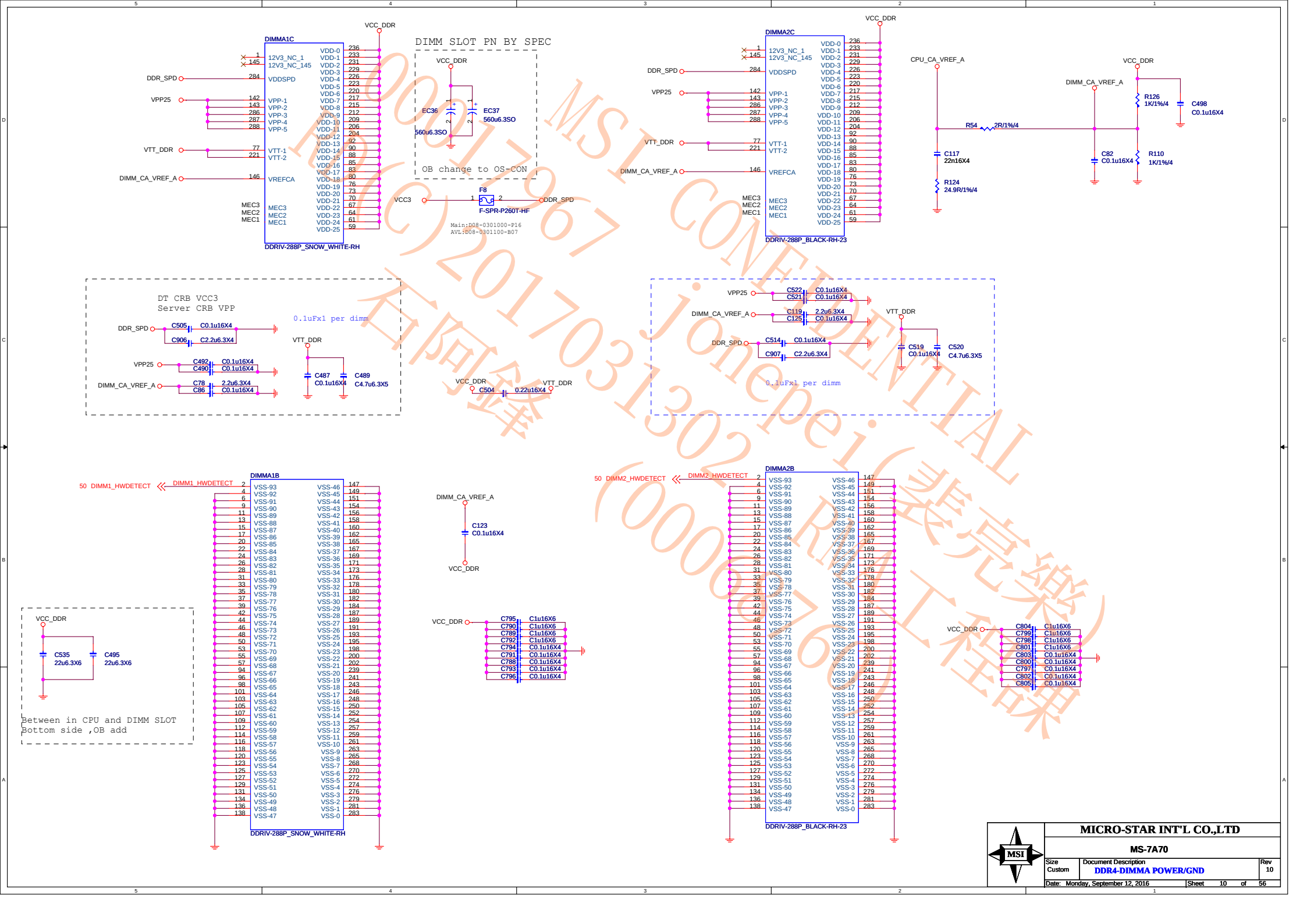
MS-7A70

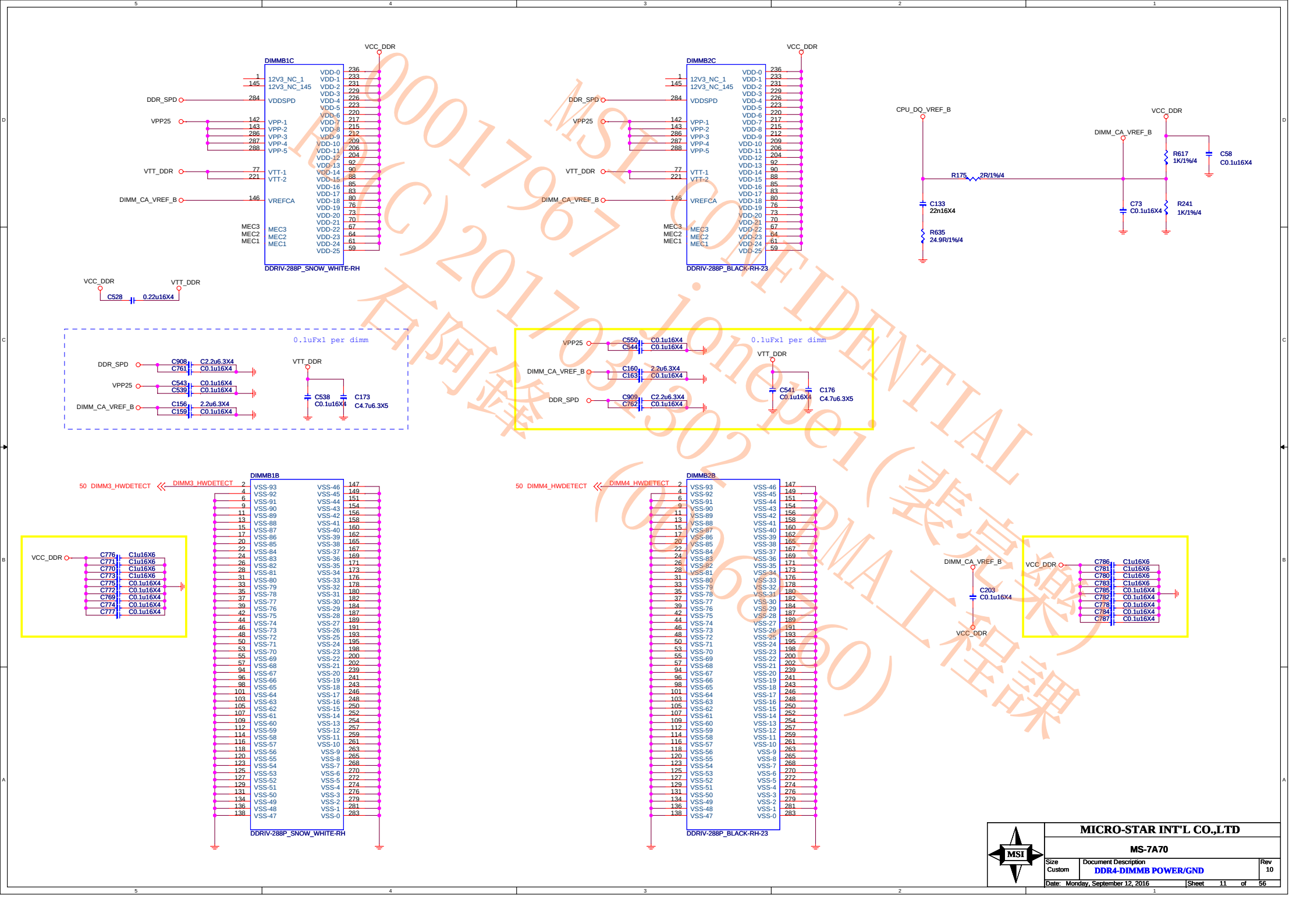
Size	Document Description	Rev
Custom	CPU-GND	10

Date: Monday, September 12, 2016 | Sheet 7 of 56


A1 A0 B1 B0
VCC_DDR
DIMMA1A
DDRIV-288P_SNOW_WHITE-RH
M_DATA_A[63..0] 3
M_MAA_A[16..0] 3
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMMA2A
DDRIV-288P_BLACK-RH-23
DIMM1 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
DDR_SPD
2014.10.16
For DDR white paper 0.89
R610 470R/1%/4
R615 0R/4
C232 X_C0.1u16X4
DIMM1_EVENT R616 240R/1%/4
DIMM2_EVENT R637 240R/1%/4
SMBCLK_VCC R612 0R/4
SMBDATA_VCC R614 0R/4
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size Custom
Document Description DDR4 DIMMA1&2
Rev 10
Date: Monday, September 12, 2016
Sheet 8 of 56


VCC_DDR
DIMMB1A
DDRIV-288P_SNOW_WHITE-RH
M_DATA_B[63..0]
M_MAA_B[16..0]
DIMM3_EVENT R606 240R/1%/4
DIMM4_EVENT R609 240R/1%/4
SMB_CLK_DIMM 8
SMB_DATA_DIMM 8
DDR_SPD
DIMM4(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
DIMMB2A
DDRIV-288P_BLACK-RH-23
DIMM4(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size Custom
Document Description DDR4 DIMMB1&2
Rev 10
Date: Monday, September 12, 2016
Sheet 9 of 56


DIMMA1C
DDRIV-288P_SNOW_WHITE-RH
DIMM SLOT PN BY SPEC
OB change to OS-CON
F-SPR-P260T-HF
Main:D08-0301000-P16
AVL:D08-0301100-B07
DIMMA2C
DDRIV-288P_BLACK-RH-23
DT CRB VCC3
Server CRB VPP
0.1uFx1 per dimm
DIMMA1B
DIMMA2B
Between in CPU and DIMM SLOT
Bottom side ,OB add
MICRO-STAR INT'L CO.,LTD
MS-7A70
DDR4-DIMMA POWER/GND
Monday, September 12, 2016


DIMMB1C
DDRIV-288P_SNOW_WHITE-RH
DIMMB2C
DDRIV-288P_BLACK-RH-23
VCC_DDR
VTT_DDR
DDR_SPD
VPP25
DIMM_CA_VREF_B
CPU_DQ_VREF_B
0.1uFx1 per dimm
DIMMB1B
DIMMB2B
DIMM3_HWDETECT
DIMM4_HWDETECT
MICRO-STAR INT'L CO.,LTD
MS-7A70
DDR4-DIMMB POWER/GND
Rev 10
Monday, September 12, 2016
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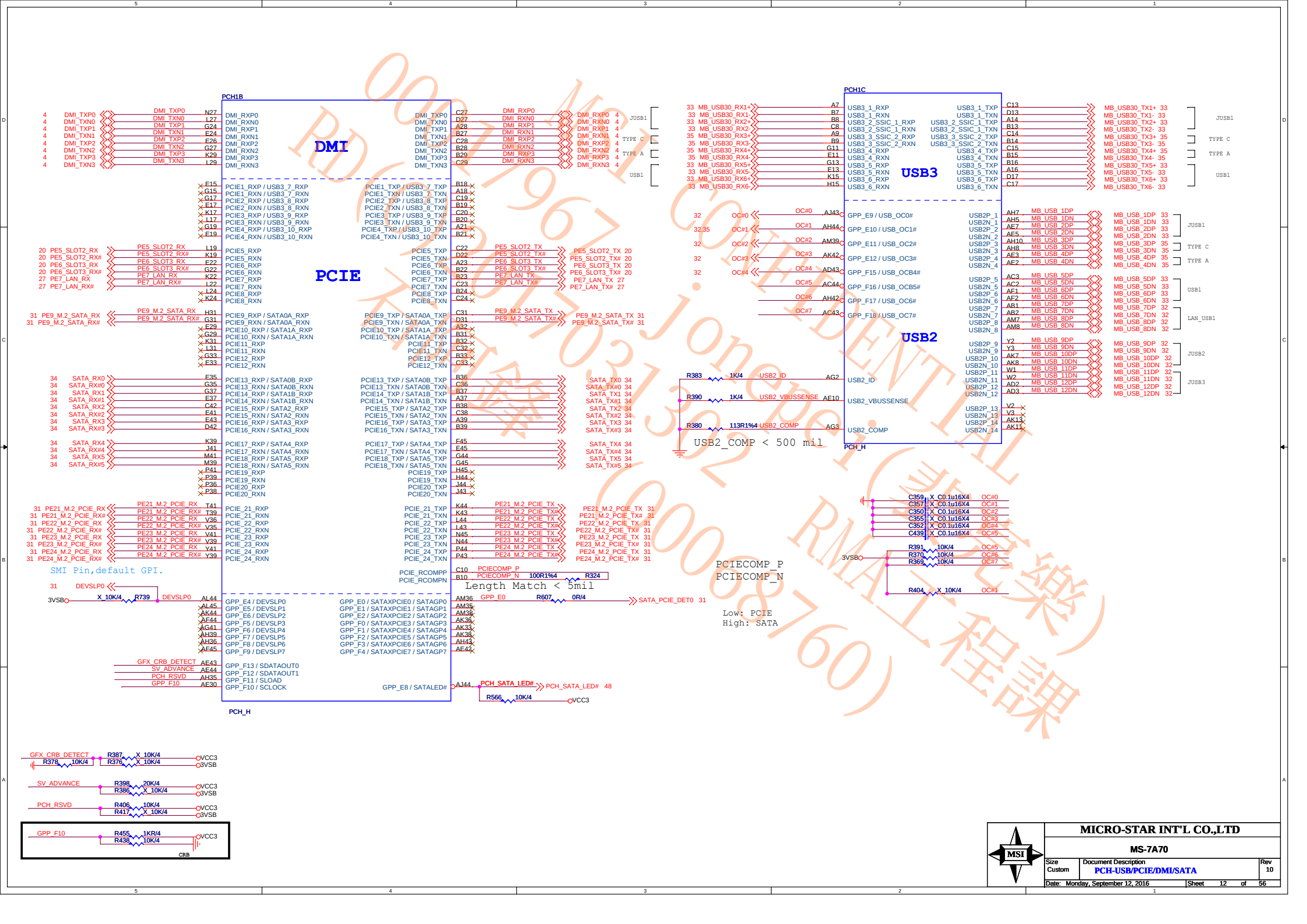
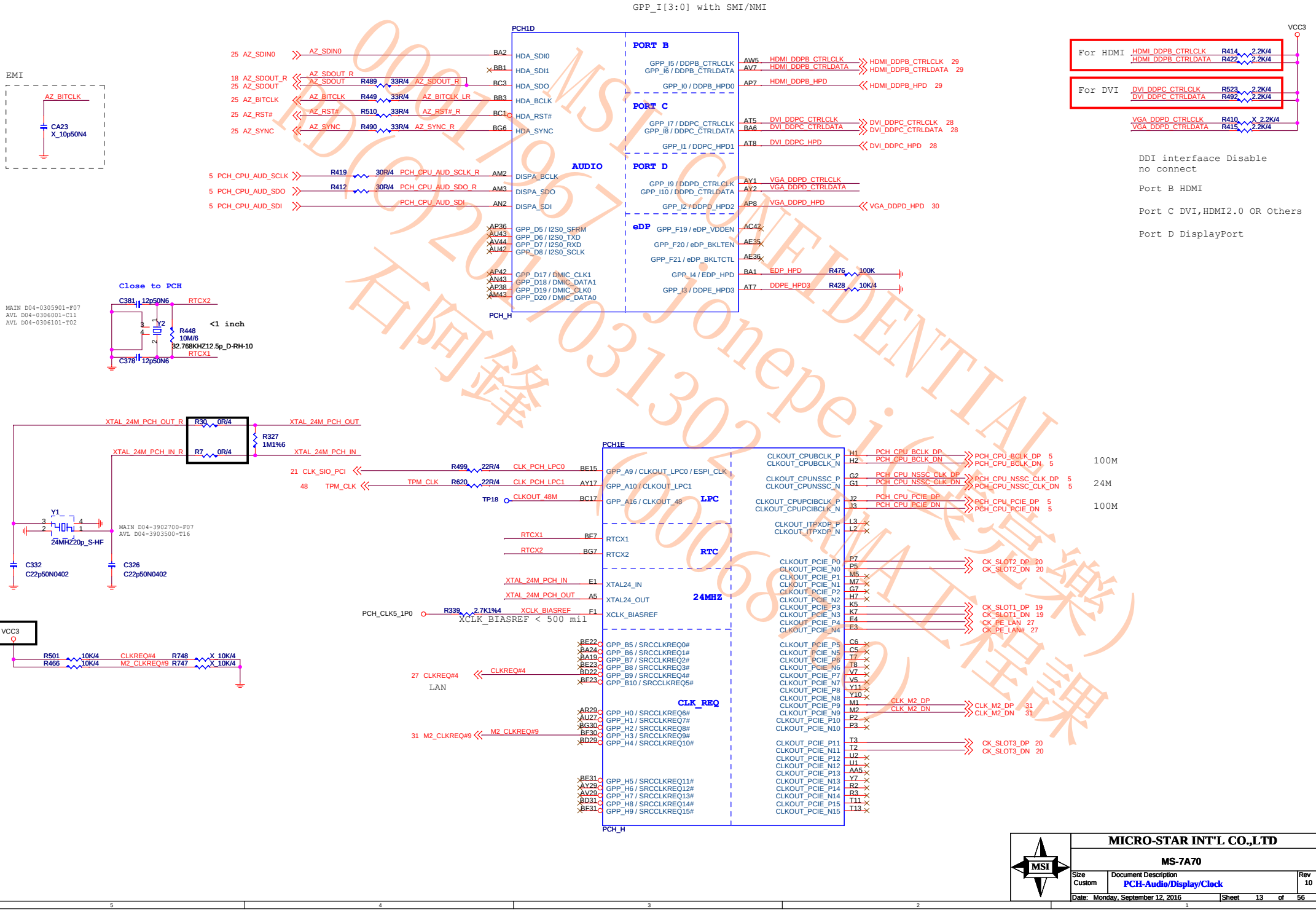

PCH1B
DMI
PCIE
GPP_E4 / DEVSLP0
GPP_E5 / DEVSLP1
GPP_E6 / DEVSLP2
GPP_F5 / DEVSLP3
GPP_F6 / DEVSLP4
GPP_F7 / DEVSLP5
GPP_F8 / DEVSLP6
GPP_F9 / DEVSLP7
GPP_F13 / SDATAOUT0
GPP_F12 / SDATAOUT1
GPP_F11 / SLOAD
GPP_F10 / SCLOCK
GPP_E8 / SATALED#
PCH_H
SMI Pin,default GPI.
PCH1C
USB3
USB2
PCH_H
USB2_COMP < 500 mil
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
Low: PCIE
High: SATA
MICRO-STAR INT'L CO.,LTD
MS-7A70
PCH-USB/PCIE/DMI/SATA
Monday, September 12, 2016


GPP_I[3:0] with SMI/NMI
PCH1D
AUDIO
PORT B
PORT C
PORT D
eDP
PCH_H
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_BCLK
HDA_RST#
HDA_SYNC
DISPA_BCLK
DISPA_SDO
DISPA_SDI
GPP_I5 / DDPB_CTRLCLK
GPP_I6 / DDPB_CTRLDATA
GPP_I0 / DDPB_HPD0
GPP_I7 / DDPC_CTRLCLK
GPP_I8 / DDPC_CTRLDATA
GPP_I1 / DDPC_HPD1
GPP_I9 / DDPD_CTRLCLK
GPP_I10 / DDPD_CTRLDATA
GPP_I2 / DDPD_HPD2
GPP_F19 / eDP_VDDEN
GPP_F20 / eDP_BKLTEN
GPP_F21 / eDP_BKLTCTL
GPP_I4 / EDP_HPD
GPP_I3 / DDPE_HPD3
GPP_D5 / I2S0_SFRM
GPP_D6 / I2S0_TXD
GPP_D7 / I2S0_RXD
GPP_D8 / I2S0_SCLK
GPP_D17 / DMIC_CLK1
GPP_D18 / DMIC_DATA1
GPP_D19 / DMIC_CLK0
GPP_D20 / DMIC_DATA0
EMI
AZ_BITCLK
CA23
X_10p50N4
Close to PCH
C381 12p50N6
C378 12p50N6
Y2
R448
10M/6
32.768KHZ12.5p_D-RH-10
RTCX1
RTCX2
<1 inch
MAIN D04-0305901-F07
AVL D04-0306001-C11
AVL D04-0306101-T02
XTAL_24M_PCH_OUT_R
XTAL_24M_PCH_IN_R
R30 0R/4
R7 0R/4
R327
1M1%6
XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
Y1
24MHZ20p_S-HF
MAIN D04-3902700-F07
AVL D04-3903500-T16
C332
C22p50N0402
C326
C22p50N0402
PCH1E
LPC
RTC
24MHZ
CLK_REQ
GPP_A9 / CLKOUT_LPC0 / ESPI_CLK
GPP_A10 / CLKOUT_LPC1
GPP_A16 / CLKOUT_48
RTCX1
RTCX2
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
GPP_B5 / SRCCLKREQ0#
GPP_B6 / SRCCLKREQ1#
GPP_B7 / SRCCLKREQ2#
GPP_B8 / SRCCLKREQ3#
GPP_B9 / SRCCLKREQ4#
GPP_B10 / SRCCLKREQ5#
GPP_H0 / SRCCLKREQ6#
GPP_H1 / SRCCLKREQ7#
GPP_H2 / SRCCLKREQ8#
GPP_H3 / SRCCLKREQ9#
GPP_H4 / SRCCLKREQ10#
GPP_H5 / SRCCLKREQ11#
GPP_H6 / SRCCLKREQ12#
GPP_H7 / SRCCLKREQ13#
GPP_H8 / SRCCLKREQ14#
GPP_H9 / SRCCLKREQ15#
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUPCIBCLK_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_ITPXDP_P
CLKOUT_ITPXDP_N
CLKOUT_PCIE_P0
CLKOUT_PCIE_N0
CLKOUT_PCIE_P1
CLKOUT_PCIE_N1
CLKOUT_PCIE_P2
CLKOUT_PCIE_N2
CLKOUT_PCIE_P3
CLKOUT_PCIE_N3
CLKOUT_PCIE_P4
CLKOUT_PCIE_N4
CLKOUT_PCIE_P5
CLKOUT_PCIE_N5
CLKOUT_PCIE_P6
CLKOUT_PCIE_N6
CLKOUT_PCIE_P7
CLKOUT_PCIE_N7
CLKOUT_PCIE_P8
CLKOUT_PCIE_N8
CLKOUT_PCIE_P9
CLKOUT_PCIE_N9
CLKOUT_PCIE_P10
CLKOUT_PCIE_N10
CLKOUT_PCIE_P11
CLKOUT_PCIE_N11
CLKOUT_PCIE_P12
CLKOUT_PCIE_N12
CLKOUT_PCIE_P13
CLKOUT_PCIE_N13
CLKOUT_PCIE_P14
CLKOUT_PCIE_N14
CLKOUT_PCIE_P15
CLKOUT_PCIE_N15
PCH_CLK5_1P0
R339 2.7K1%4
XCLK_BIASREF < 500 mil
CLKREQ#4
M2_CLKREQ#9
LAN
VCC3
R501 10K/4
R466 10K/4
R748 X_10K/4
R747 X_10K/4
For HDMI
For DVI
VGA_DDPD_CTRLCLK
VGA_DDPD_CTRLDATA
DDI interfaace Disable
no connect
Port B HDMI
Port C DVI,HDMI2.0 OR Others
Port D DisplayPort
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size Custom
Document Description PCH-Audio/Display/Clock
Rev 10
Date: Monday, September 12, 2016
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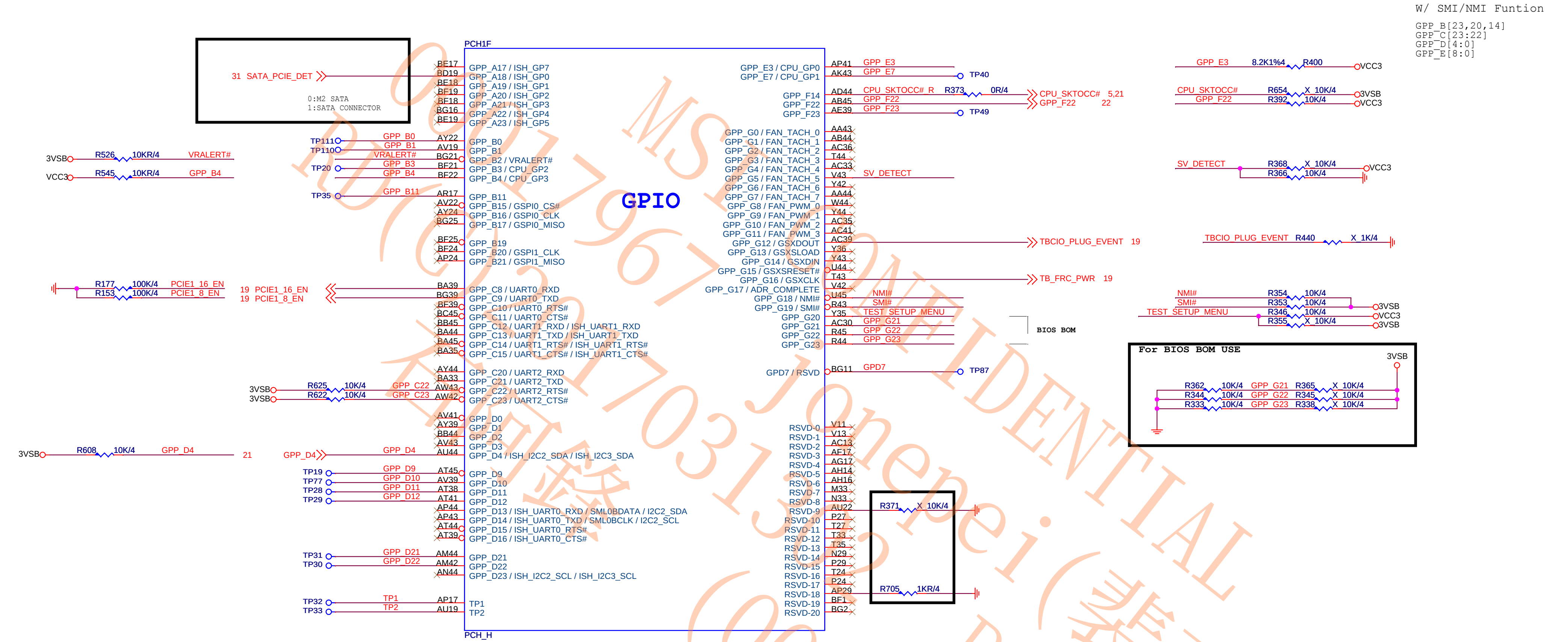

2014.10.16 PCH cOM BACK test

CRB

GPP_B11 default GPO to LOW

If an AMT capable Intel WLAN device is not implemented
then this signal can be left as NO CONNECT (NC).

For BIOS BOM USE

	GPP_G21	GPP_G22	GPP_G23
B250M BAZOOKA	0	0	0
B250M BAZOOKA PLUS	0	0	1

MICRO-STAR INT'L CO.,LTD

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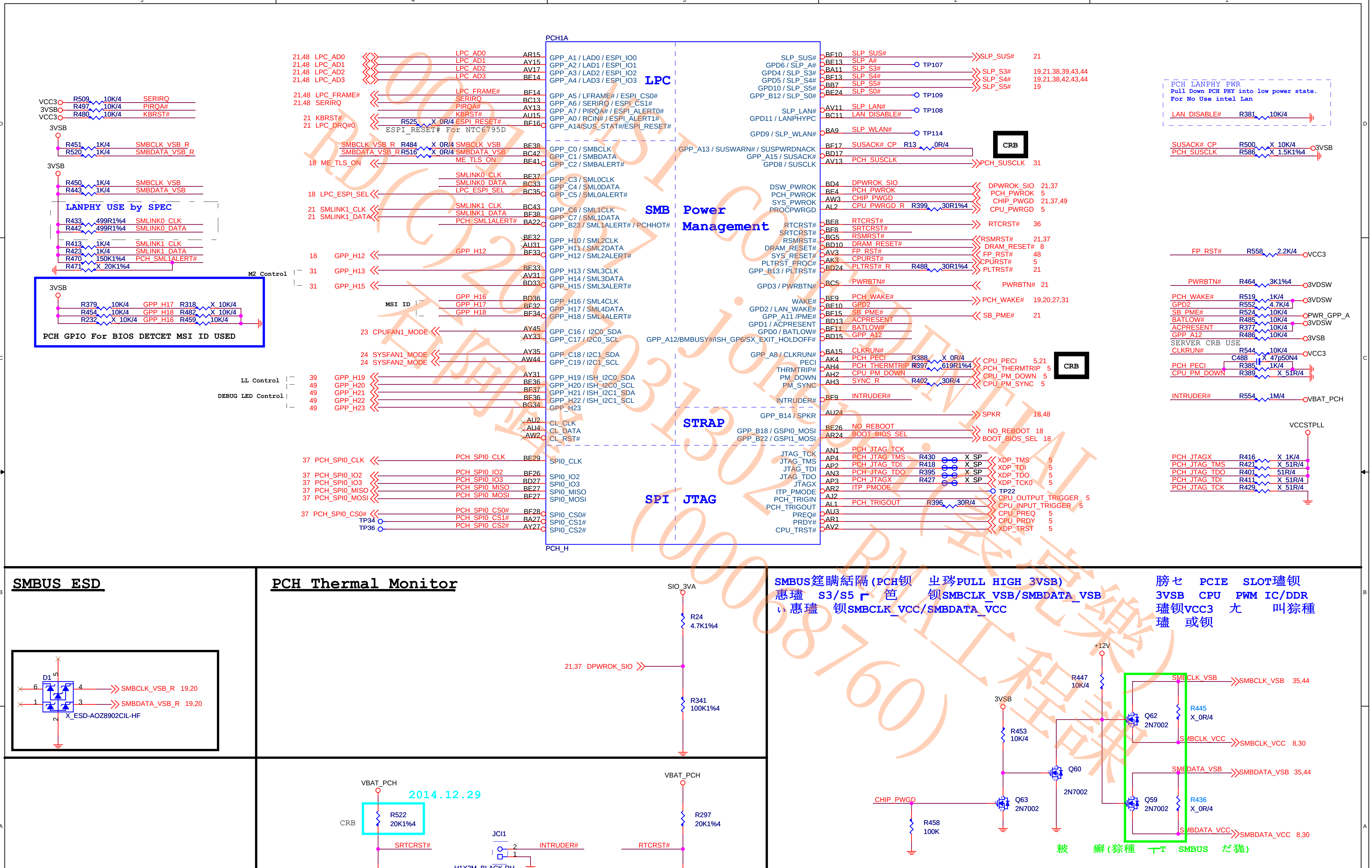
Size	Document Description	Rev
Custom	PCH-GPIO/USBOC#/SATASTRAP	10

Date: Monday, September 12, 2016 Sheet 14 of 56

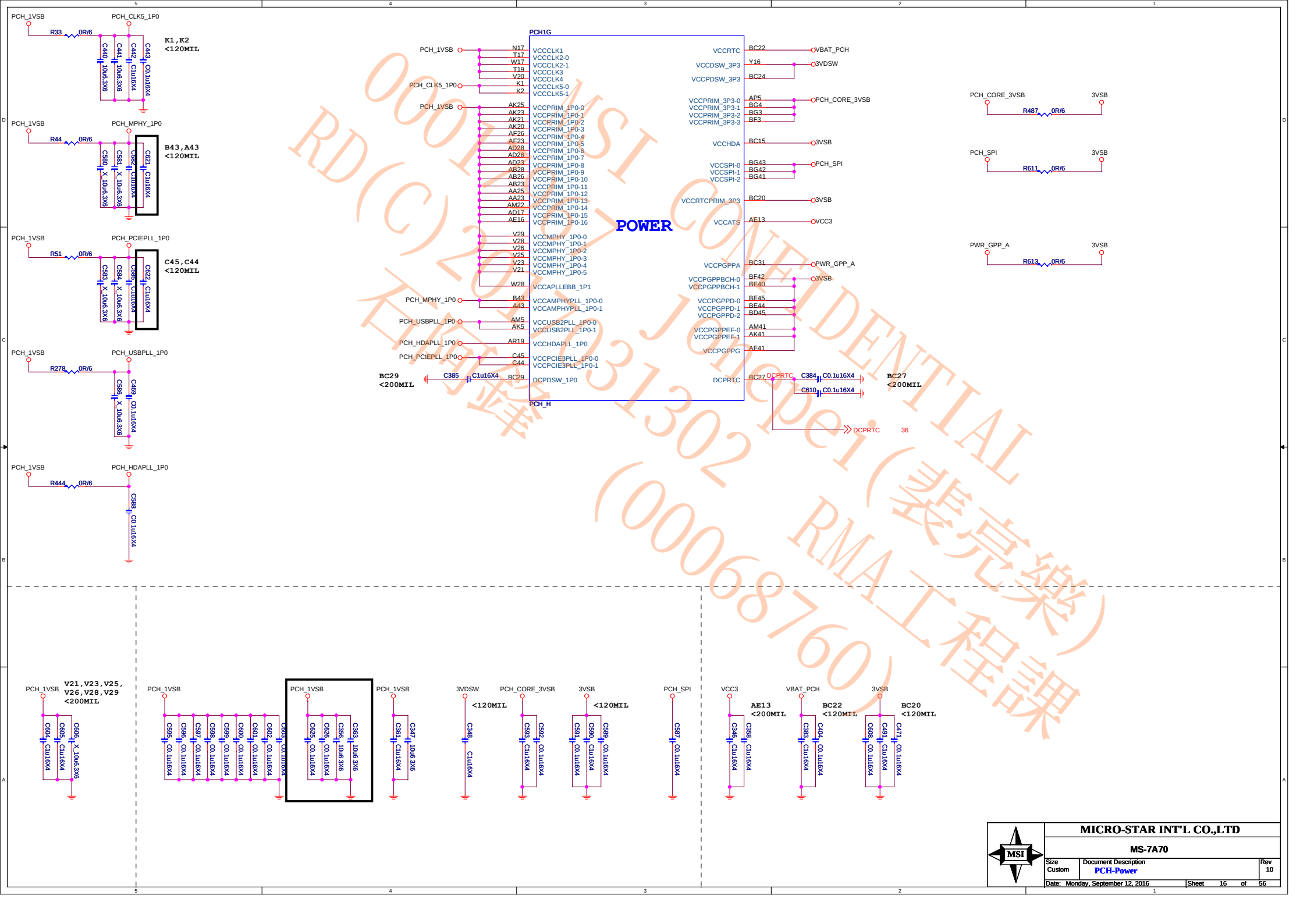


MICRO-STAR INT'L CO.,LTD

MS-7A70

Size: Custom | Document Description: PCH-LPC/SPI/SMBUS/MISC | Rev: 10

Date: Monday, September 12, 2016 | Sheet 15 of 56


PCH_1VSB
PCH_CLK5_1P0
R33 0R/6
C440 10u6.3X6
C441 10u6.3X6
C442 C1u16X4
C443 C0.1u16X4
K1,K2
<120MIL
PCH_MPHY_1P0
R44 0R/6
C580 X_10u6.3X6
C581 X_10u6.3X6
C582 C1u16X4
C621 C1u16X4
B43,A43
<120MIL
PCH_PCIEPLL_1P0
R51 0R/6
C583 X_10u6.3X6
C584 X_10u6.3X6
C585 C1u16X4
C622 C1u16X4
C45,C44
<120MIL
PCH_USBPLL_1P0
R278 0R/6
C586 X_10u6.3X6
C469 C0.1u16X4
PCH_HDAPLL_1P0
R444 0R/6
C588 C0.1u16X4
PCH1G
POWER
PCH_H
VCCCLK1
VCCCLK2-0
VCCCLK2-1
VCCCLK3
VCCCLK4
VCCCLK5-0
VCCCLK5-1
VCCPRIM_1P0-0
VCCPRIM_1P0-1
VCCPRIM_1P0-2
VCCPRIM_1P0-3
VCCPRIM_1P0-4
VCCPRIM_1P0-5
VCCPRIM_1P0-6
VCCPRIM_1P0-7
VCCPRIM_1P0-8
VCCPRIM_1P0-9
VCCPRIM_1P0-10
VCCPRIM_1P0-11
VCCPRIM_1P0-12
VCCPRIM_1P0-13
VCCPRIM_1P0-14
VCCPRIM_1P0-15
VCCPRIM_1P0-16
VCCMPHY_1P0-0
VCCMPHY_1P0-1
VCCMPHY_1P0-2
VCCMPHY_1P0-3
VCCMPHY_1P0-4
VCCMPHY_1P0-5
VCCAPLLEBB_1P1
VCCAMPHYPLL_1P0-0
VCCAMPHYPLL_1P0-1
VCCUSB2PLL_1P0-0
VCCUSB2PLL_1P0-1
VCCHDAPLL_1P0
VCCPCIE3PLL_1P0-0
VCCPCIE3PLL_1P0-1
DCPDSW_1P0
VCCRTC
VCCDSW_3P3
VCCPDSW_3P3
VCCPRIM_3P3-0
VCCPRIM_3P3-1
VCCPRIM_3P3-2
VCCPRIM_3P3-3
VCCHDA
VCCSPI-0
VCCSPI-1
VCCSPI-2
VCCRTCPRIM_3P3
VCCATS
VCCPGPPA
VCCPGPPBCH-0
VCCPGPPBCH-1
VCCPGPPD-0
VCCPGPPD-1
VCCPGPPD-2
VCCPGPPEF-0
VCCPGPPEF-1
VCCPGPPG
DCPRTC
VBAT_PCH
3VDSW
PCH_CORE_3VSB
PCH_SPI
3VSB
VCC3
PWR_GPP_A
BC29 <200MIL
BC27 <200MIL
C385 C1u16X4
C384 C0.1u16X4
C610 C0.1u16X4
R487 0R/6
R611 0R/6
R613 0R/6
V21,V23,V25,
V26,V28,V29
<200MIL
AE13 <200MIL
BC22 <120MIL
BC20 <120MIL
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size Custom
Document Description PCH-Power
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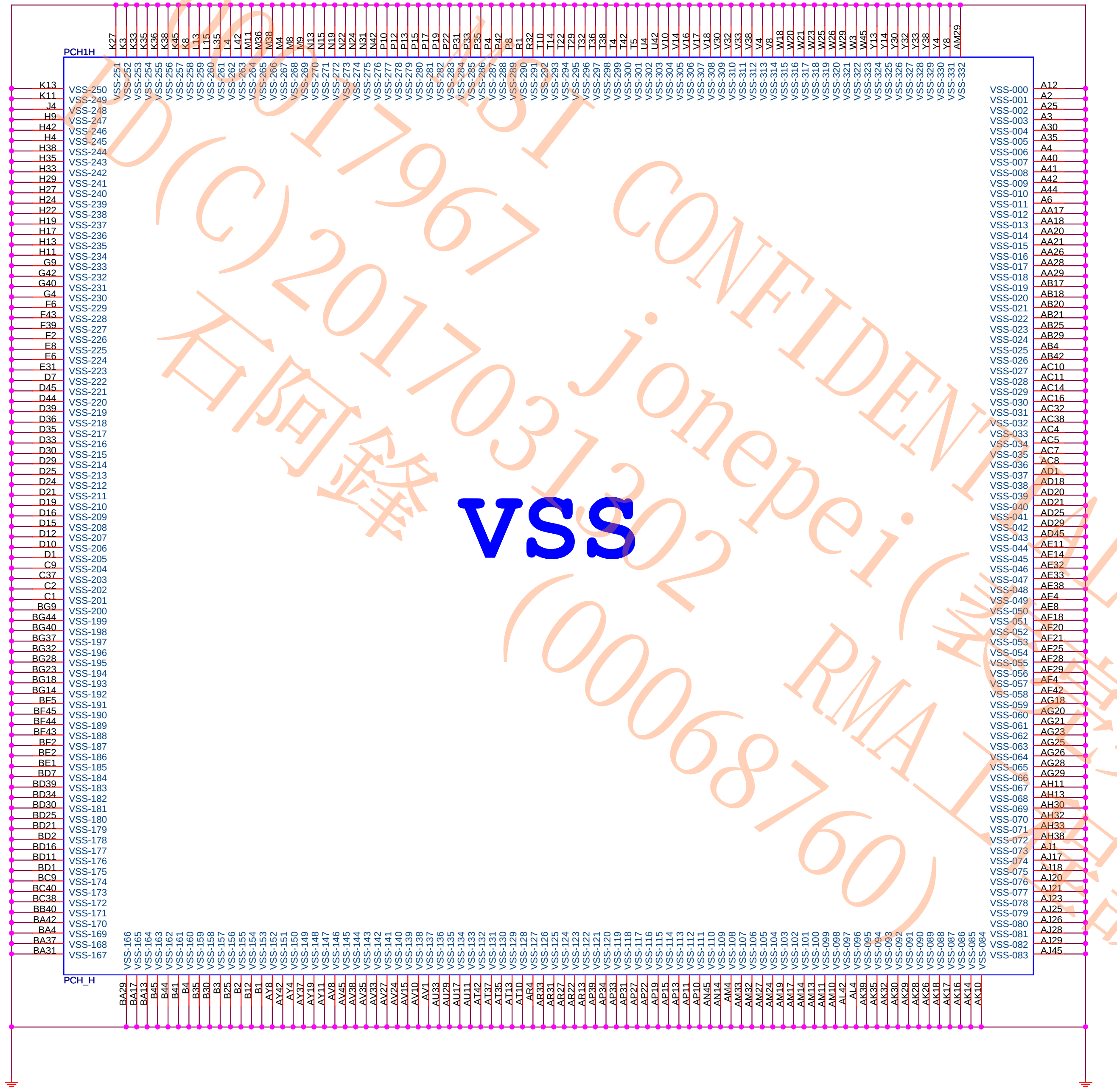

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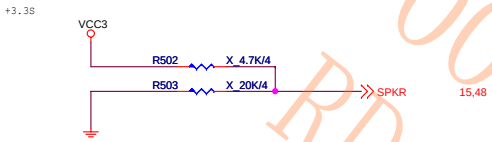
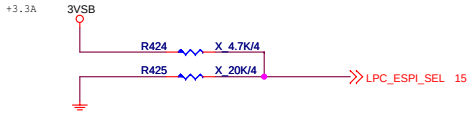
TOP Swap



Internal pull-down 20K is disabled after PLTRST#

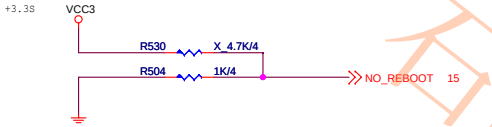
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

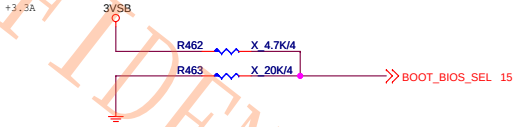
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

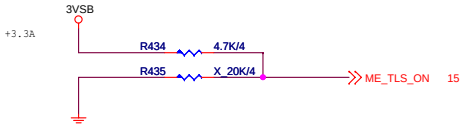
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

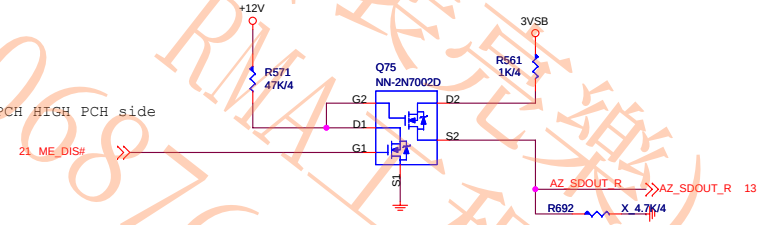
AMT and SBA with confidentiality



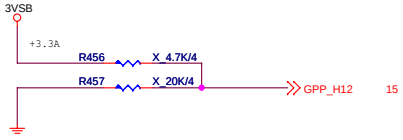
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

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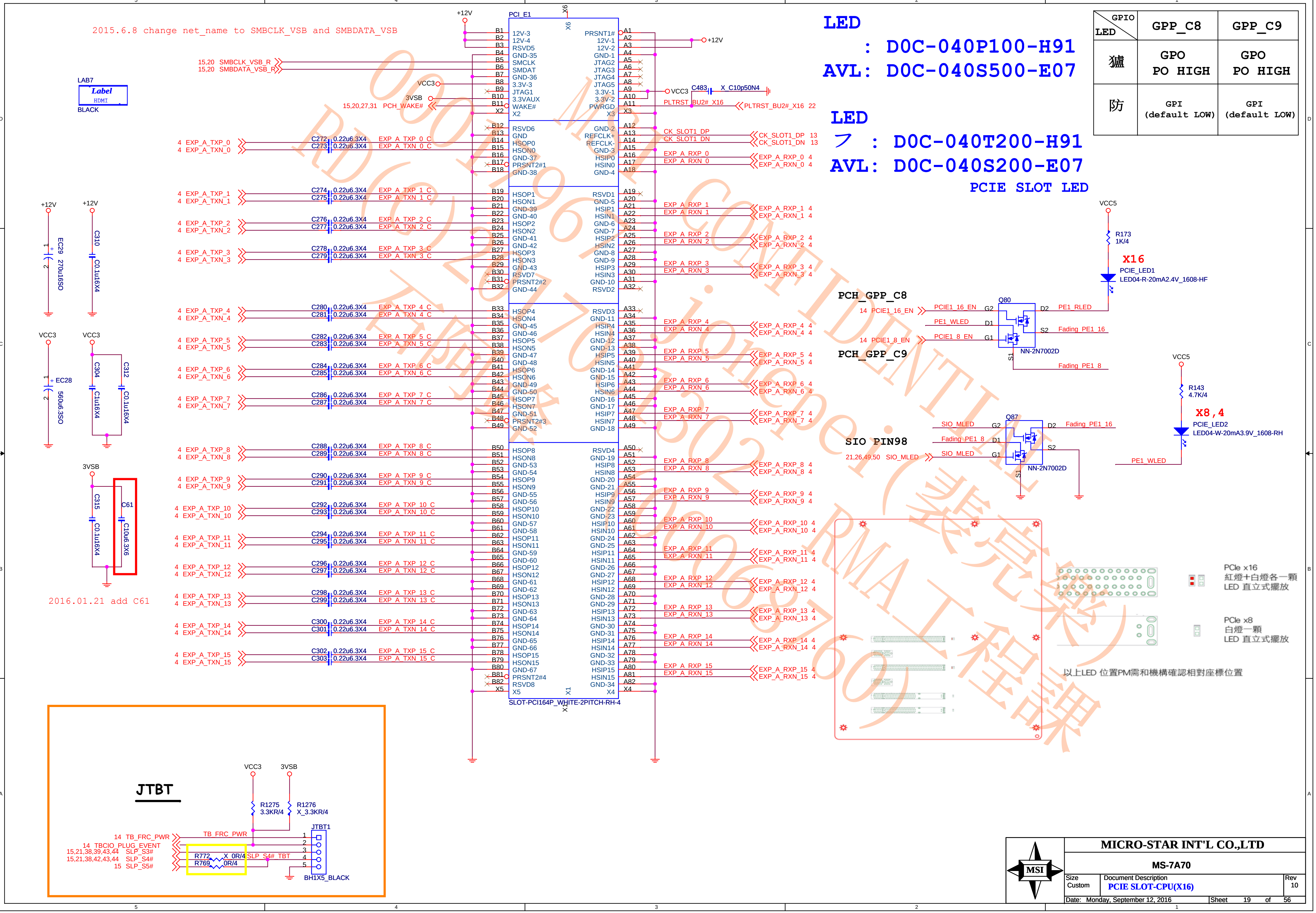
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB
PCI_E1
SLOT-PCI164P_WHITE-2PITCH-RH-4
LED
: DOC-040P100-H91
AVL: DOC-040S500-E07
LED
: DOC-040T200-H91
AVL: DOC-040S200-E07
PCIE SLOT LED
GPIO
LED
GPP_C8
GPP_C9
GPO
PO HIGH
GPI
(default LOW)
PCH_GPP_C8
PCH_GPP_C9
SIO PIN98
X16
X8,4
PCIE_LED1
LED04-R-20mA2.4V_1608-HF
PCIE_LED2
LED04-W-20mA3.9V_1608-RH
NN-2N7002D
2016.01.21 add C61
JTBT
JTBT1
BH1X5_BLACK
PCIe x16
紅燈+白燈各一顆
LED 直立式擺放
PCIe x8
白燈一顆
LED 直立式擺放
以上LED 位置PM需和機構確認相對座標位置
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size
Custom
Document Description
PCIE SLOT-CPU(X16)
Rev
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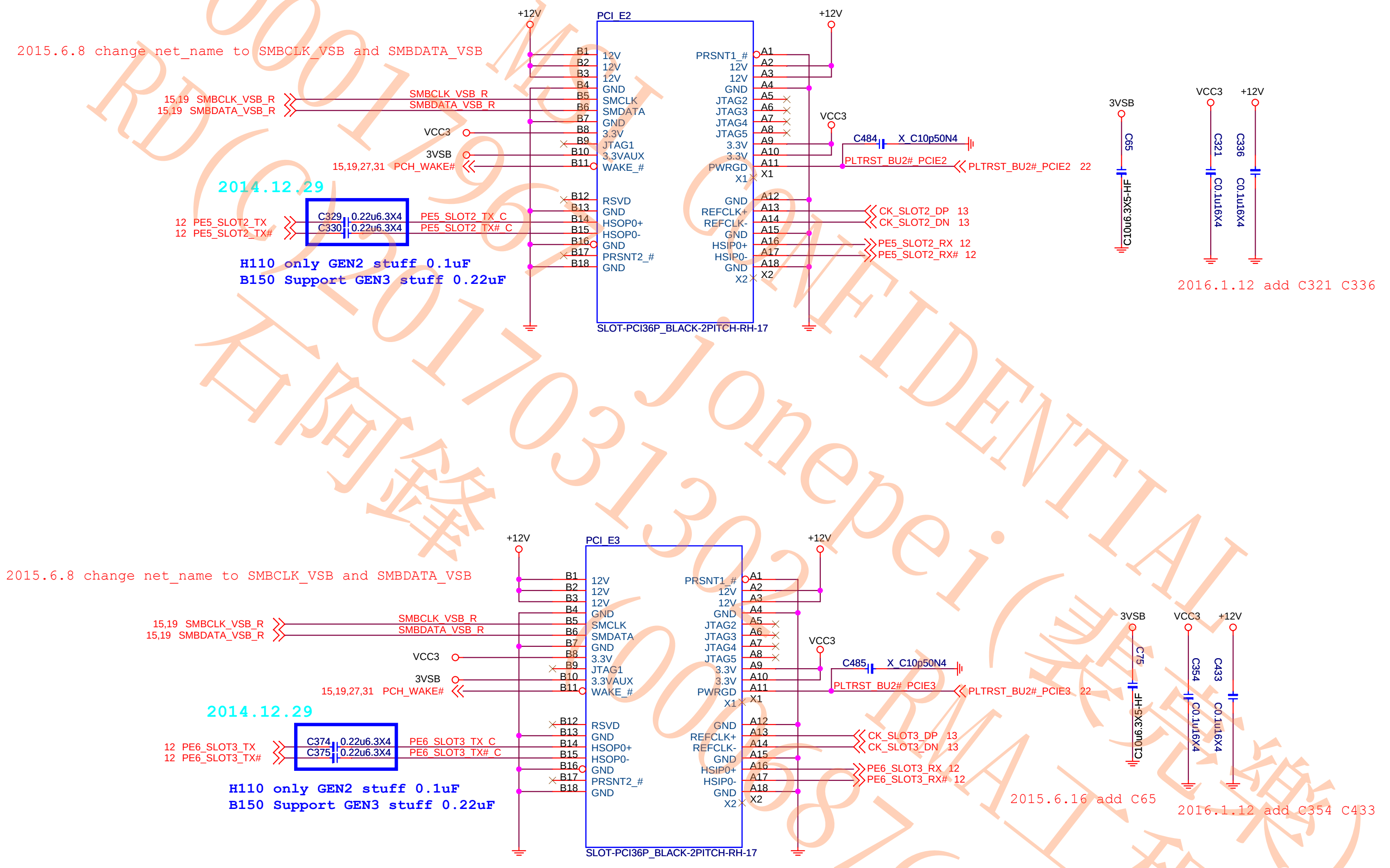

MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	10

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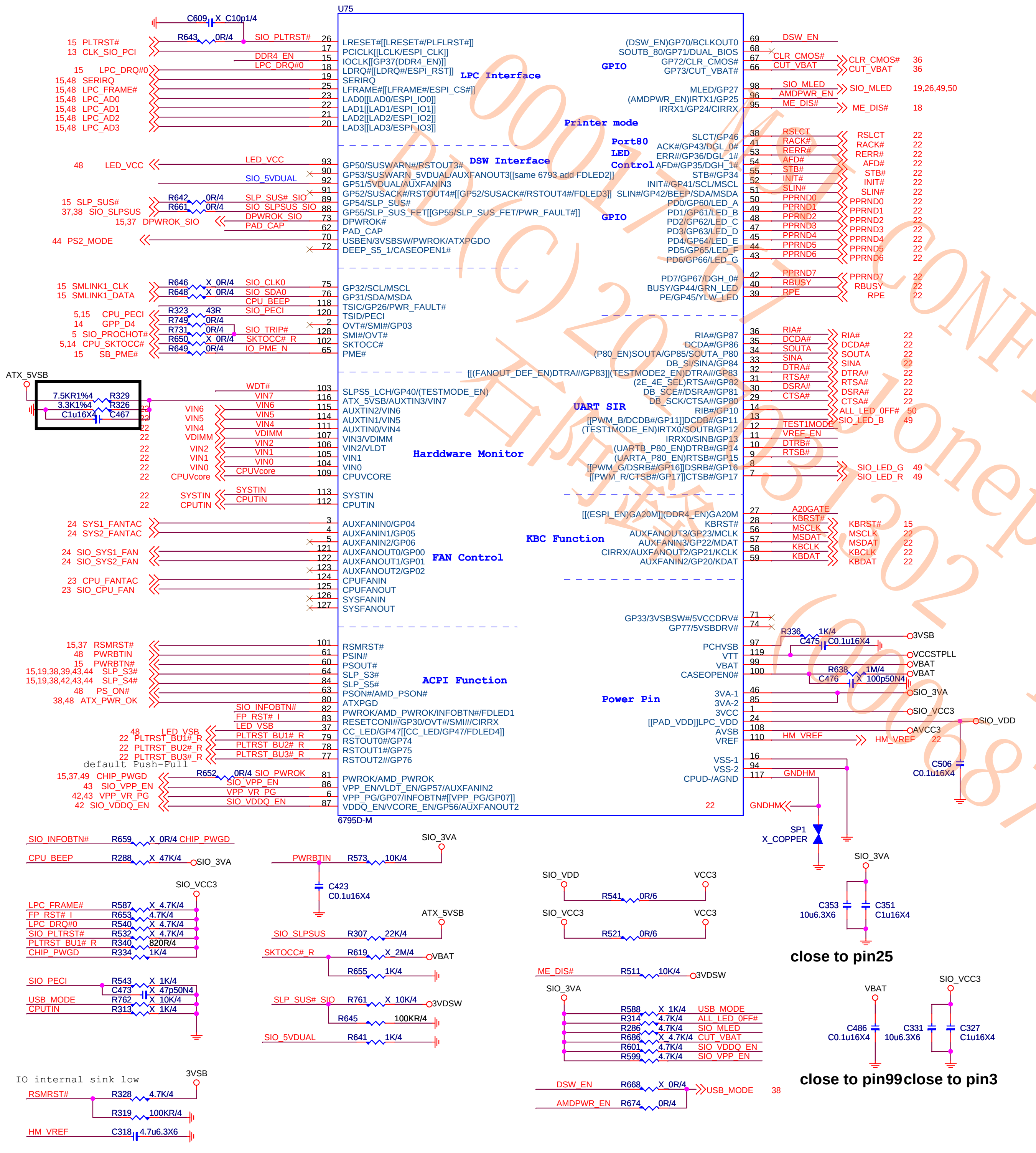


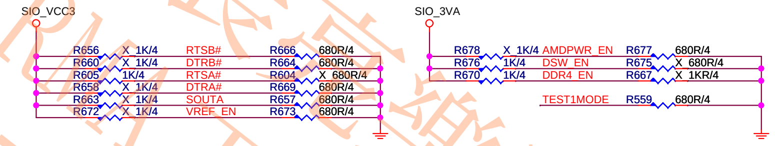
POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

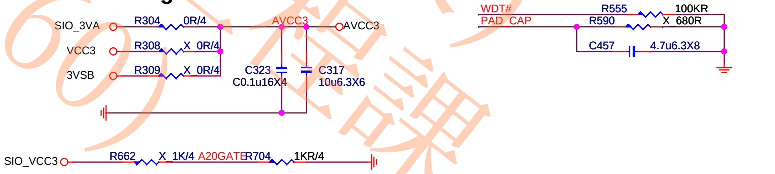
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable



3V Analog Power



MICRO-STAR INT'L CO.,LTD
MS-7A70
Size: Custom | Document Description: SIO-NCT6795D-1 | Rev: 10
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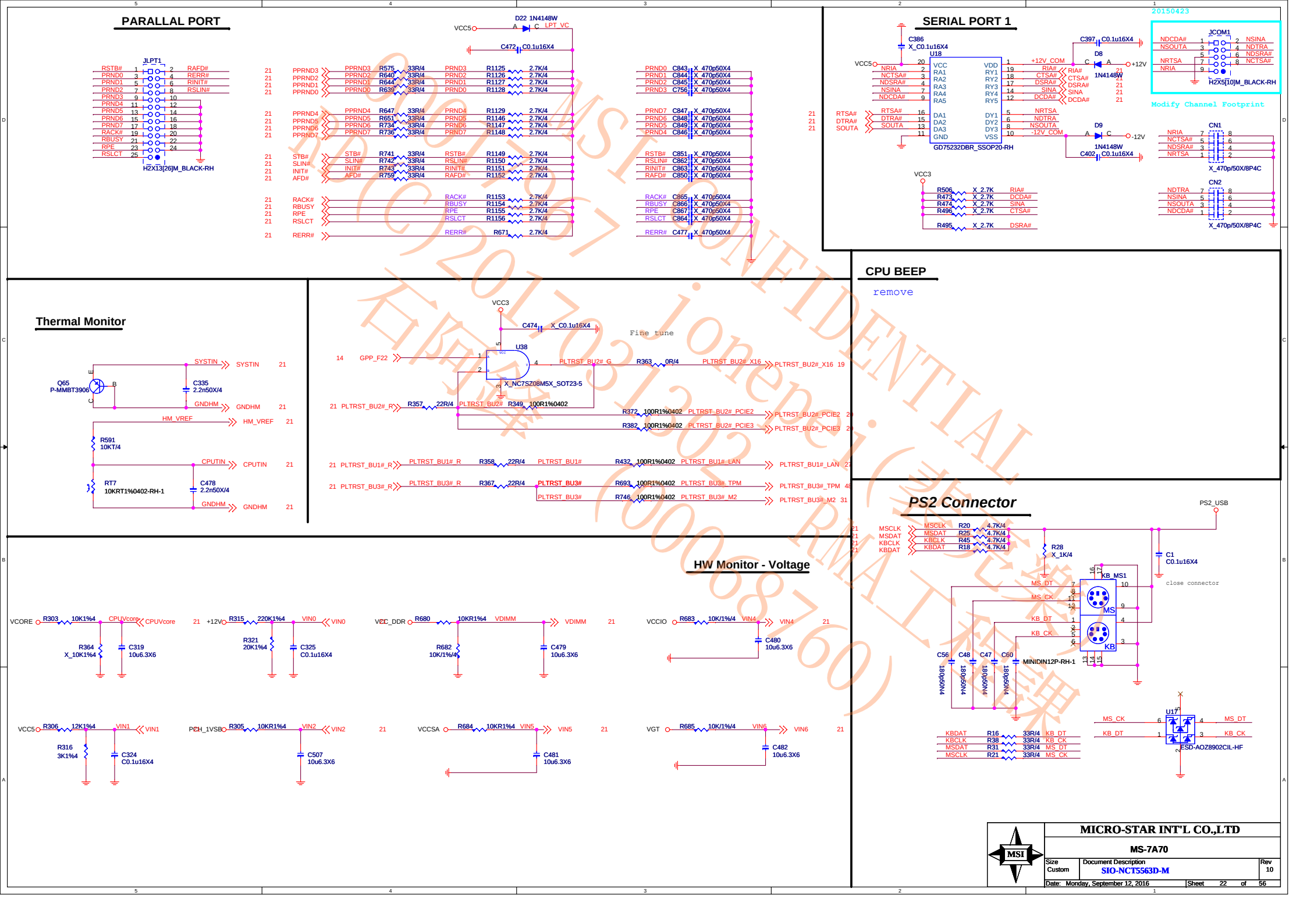
PARALLAL PORT
JLPT1
H2X13[26]M_BLACK-RH
D22 1N4148W
C472 C0.1u16X4
SERIAL PORT 1
20150423
JCOM1
H2X5[10]M_BLACK-RH
Modify Channel Footprint
U18
GD75232DBR_SSOP20-RH
1N4148W
CN1
CN2
X_470p/50X/8P4C
Thermal Monitor
Q65
P-MMBT3906
C335
2.2n50X/4
R591
10KT/4
RT7
10KRT1%0402-RH-1
C478
2.2n50X/4
U38
X_NC7SZ08M5X_SOT23-5
Fine tune
CPU BEEP
remove
PS2 Connector
PS2_USB
KB_MS1
MINIDIN12P-RH-1
ESD-AOZ8902CIL-HF
close connector
HW Monitor - Voltage
MICRO-STAR INT'L CO.,LTD
MS-7A70
SIO-NCT5563D-M
Size
Custom
Document Description
Rev
10
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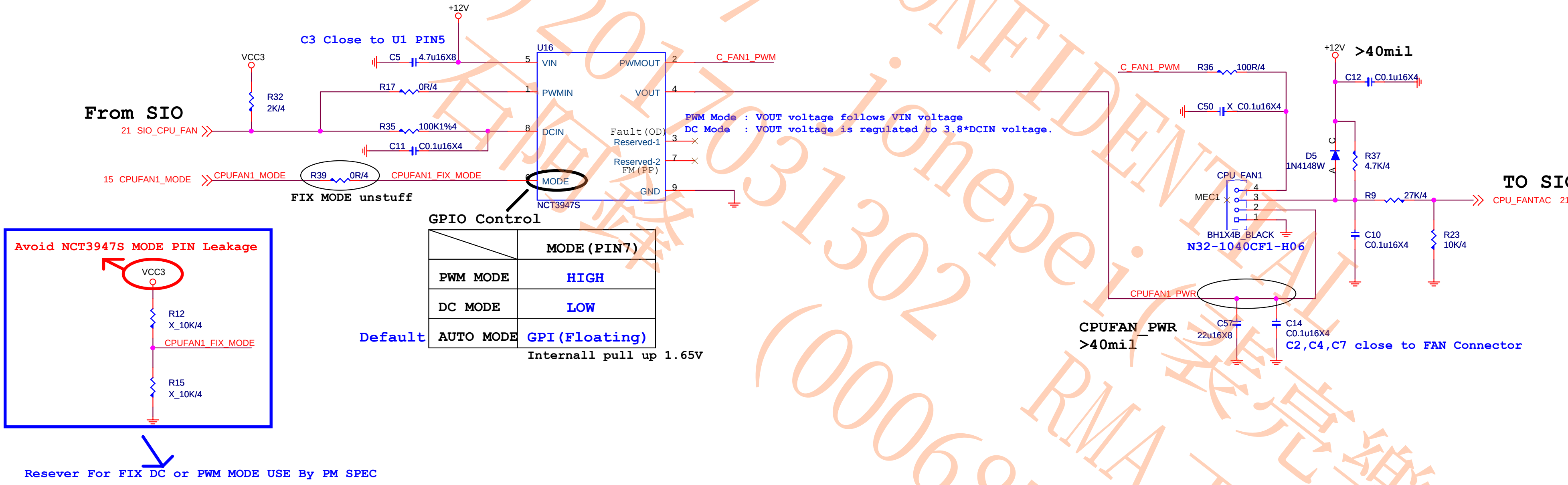
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBIOSち传 PWM/DC MODE

TYPE K



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default: AUTO MODE

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	FAN CONTROLLOR	10

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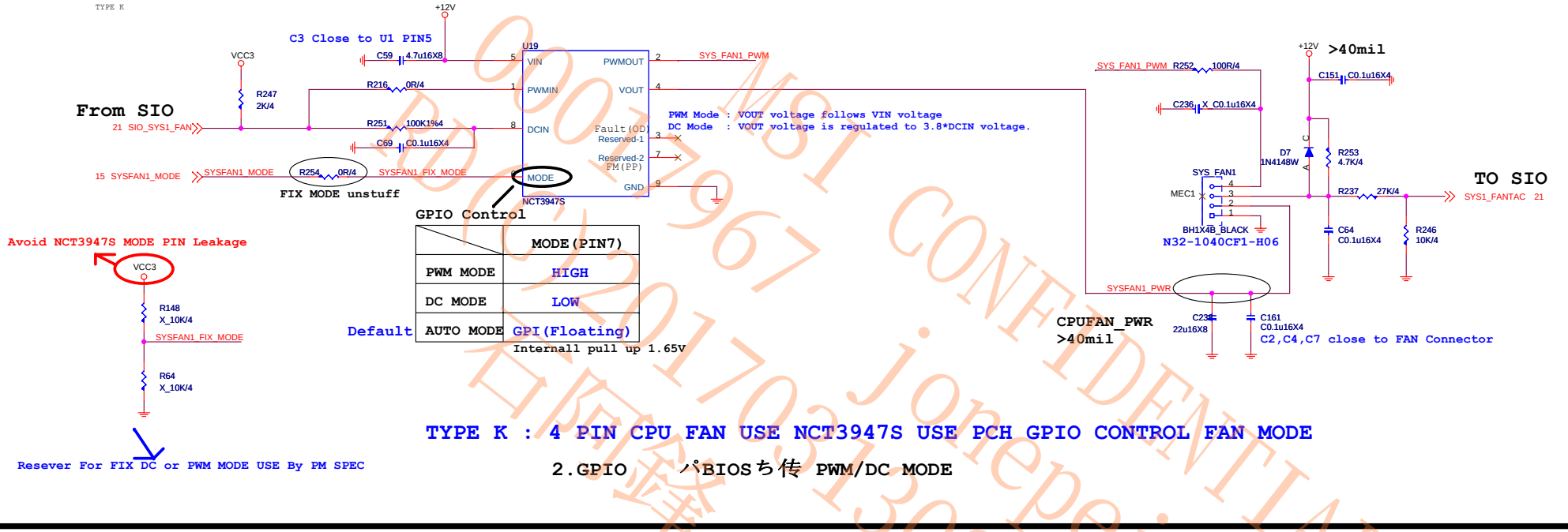
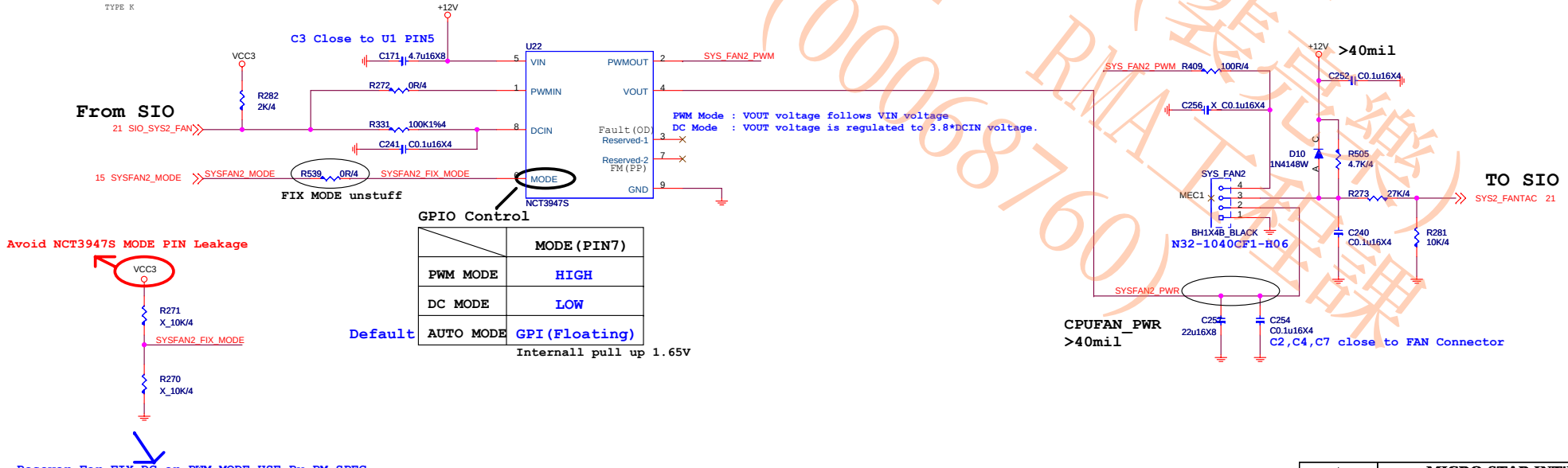


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBIOSち传 PWM/DC MODE

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パBIOSち传 PWM/DC MODE



MICRO-STAR INT'L CO.,LTD	
MS-7A70	
Size: Custom	Document Description: FAN CONTROLLOR — Rev: 10
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Type B:
ALC892/887

2014.09.15

CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38

11mA
Closed Codec
VCC3 3VSB
CA28 10u6.3X6
CA18 C0.1u16X4
VOUT
CA30 C0.1u16X4
CA14 22u6.3X8
CA31 10u6.3X6

3VSB
CA37 C0.1u16X4
CA19 22u6.3X8
2016.01.21 ADD

SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

2015.05.22 change to OSC

UA1
26 EAPD
EAPD
SPDIF-OUT
13 AZ_SDOUT
13 AZ_SDIN0
13 AZ_SYNC
13 AZ_RST#
RA21 33R/4 SDIN0
SDATA-OUT
SDATA-IN
SYNC
RESET#
13 AZ_BITCLK
R697 0R/4
BCLK
AZ_SDIN0
2016,01,26 ADD
CA22 X_10p50N4
REGREF
CA24 10u6.3X6
SENSE_A
SENSE_B
Sense A
Sense B
MIC1_V_R
MIC2_VREFO
MIC1_V_L
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
45.8mA
LDOVDD
LINE2_VREFO
VREF_AUDIO
LDO-IN
LINE2-VREFO
VREF
Sense C
JDREF
CA16 X_C0.1u16X4
CA17 10u6.3X6
RA23 20K1%4
BEEP
Closed Codec
CA29.CA30 close to Pin27
EPAD/SPDIF-IN
SPDIF-OUT
GPIO0/DMIC-CLK/SPDIF-OUT2
GPIO1/DMIC-DATA
ALC887-VD2-CG-HF
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
AVSS1
AVSS2
DVSS
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
A_LOUT_R ECA3 100u10EL5 LOUT_R
A_LOUT_L ECA4 100u10EL5 LOUT_L
A_LINE_IN_R CA8 4.7u6.3X8 LINE_IN_R
A_LINE_IN_L CA9 4.7u6.3X8 LINE_IN_L
A_LINE2_R ECA1 100u10EL5 LINE2_R
A_LINE2_L ECA2 100u10EL5 LINE2_L
A_MIC1_R CA10 4.7u6.3X8 MIC1_R
A_MIC1_L CA11 4.7u6.3X8 MIC1_L
A_MIC2_R CA12 4.7u6.3X8 MIC2_R
A_MIC2_L CA13 4.7u6.3X8 MIC2_L

LIN_OUT
LOUT_R RA9 75R LOUT_RA
LOUT_L RA12 75R LOUT_LA
FRONT_JD
AUDIO1B
DA1 ESD-SFI0402
DA2 ESD-SFI0402
JACK-AUDIOX3F_PK/LIME/LIGHT BU-RH
N54-13F0251-F02

LIN_IN
LINE_IN_R RA5 75R LINE_IN_RA
LINE_IN_L RA7 75R LINE_IN_LA
LINE1_JD
AUDIO1A
CA3 100p50N4
CA4 100p50N4
JACK-AUDIOX3F_PK/LIME/LIGHT BU-RH
N54-13F0251-F02

D LIN_IN
E LIN_OUT
F MIC1
N54-13F0271-K06

2.2k for better recording quality
MIC1_V_L RA6 2.2K/4 MIC1_LA
MIC1_V_R RA2 2.2K/4 MIC1_RA
MIC1_R RA8 75R MIC1_RA
MIC1_L RA3 75R MIC1_LA
MIC1_JD
MIC1
AUDIO1C
CA1 100p50N4
CA2 100p50N4
JACK-AUDIOX3F_PK/LIME/LIGHT BU-RH
N54-13F0251-F02
for rear I/O 6port:
887VD/892:1k
for rear I/O 3port:
887VD/892:75R

26 LOUT_LA
26 LOUT_RA
LOUT_LA
LOUT_RA
RA4 22K/4
RA1 22K/4

EMI
CA6 X_C0.1u16X4
CA5 X_1000p50N4
CPA1 X_COPPER
CPA2 X_COPPER

MIC2_R RA28 75R F_MIC2_R
MIC2_L RA24 75R F_MIC2_L
LINE2_L RA34 75R F_LINE2_L
LINE2_R RA32 75R F_LINE2_R

DA8
LINE2_VREFO
S-BAT54A_SOT23
DA4
MIC2_VREFO
S-BAT54A_SOT23
RS79 4.7K4
RS81 4.7K4
RS80 4.7K4

F_MIC2_L
F_MIC2_R
F_LINE2_R
SENSE_B
F_LINE2_L
RA26 47R
JAUD1
MIC
GND
MICPWR
PRESENCE#
FLINE OUTR
LINE NEXT R
HPON
FLINE OUTL
LINE NEXT L
H2X5[8]M_BLACK-RH
MIC2_JD
LINE2_JD
DA5 ESD-SFI0402
DA6 ESD-SFI0402
DA7 ESD-SFI0402
DA9 ESD-SFI0402
CA35 1000p16X4
N31-2051411-H06
RA27 39.2K1%4
RA25 20K1%4
Close to Front panel
For HDA/AC97 front cable.

Closed Codec
SENSE_A
RA17 5.1K1%4 FRONT_JD
RA18 10K1%4 LINE1_JD
RA16 20K1%4 MIC1_JD

0R for cost down
ATX_5VSB
LA1 0R/8
LDOVDD
DA3 X_TVS
CA32 C0.1u16X4
CA33 10u6.3X6
CA23,CA24 close to LA1

26 F_LINE2_L
26 F_LINE2_R
F_LINE2_L
F_LINE2_R
RA33 22K/4
RA31 22K/4

Varister --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

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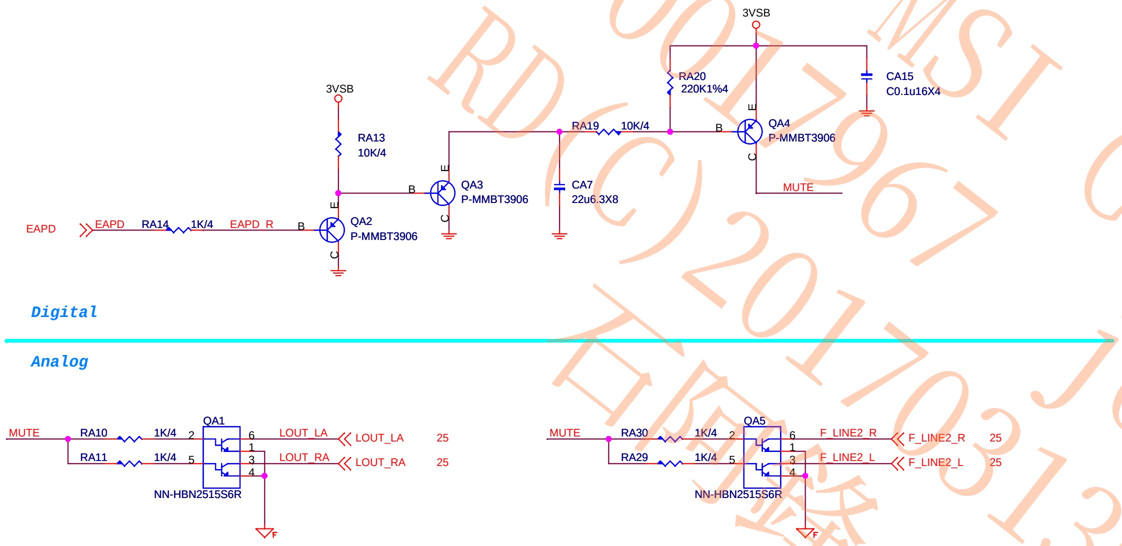
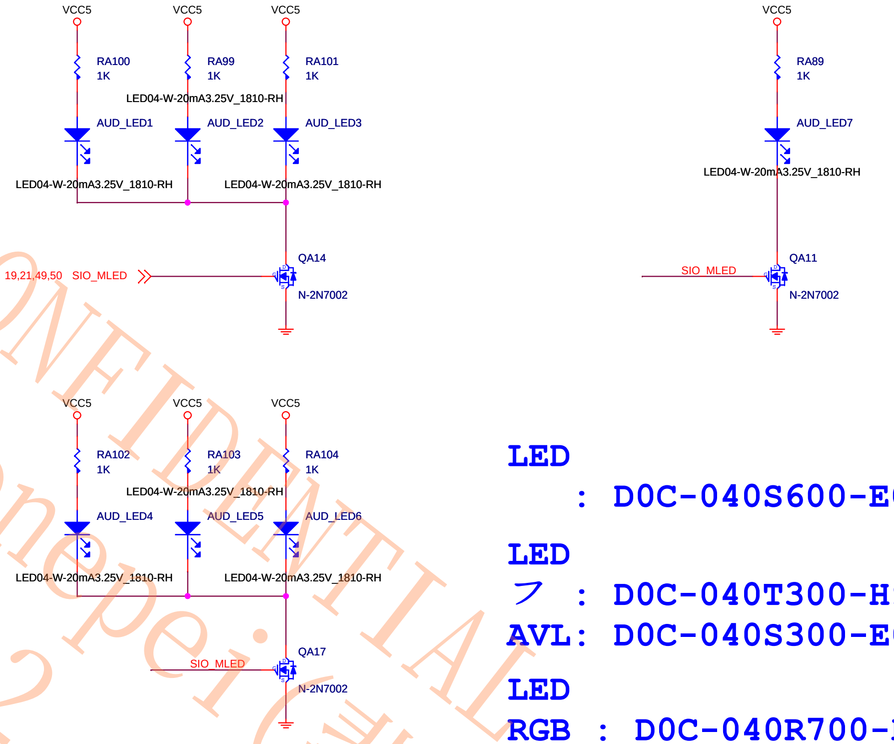
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



AUDIO LED



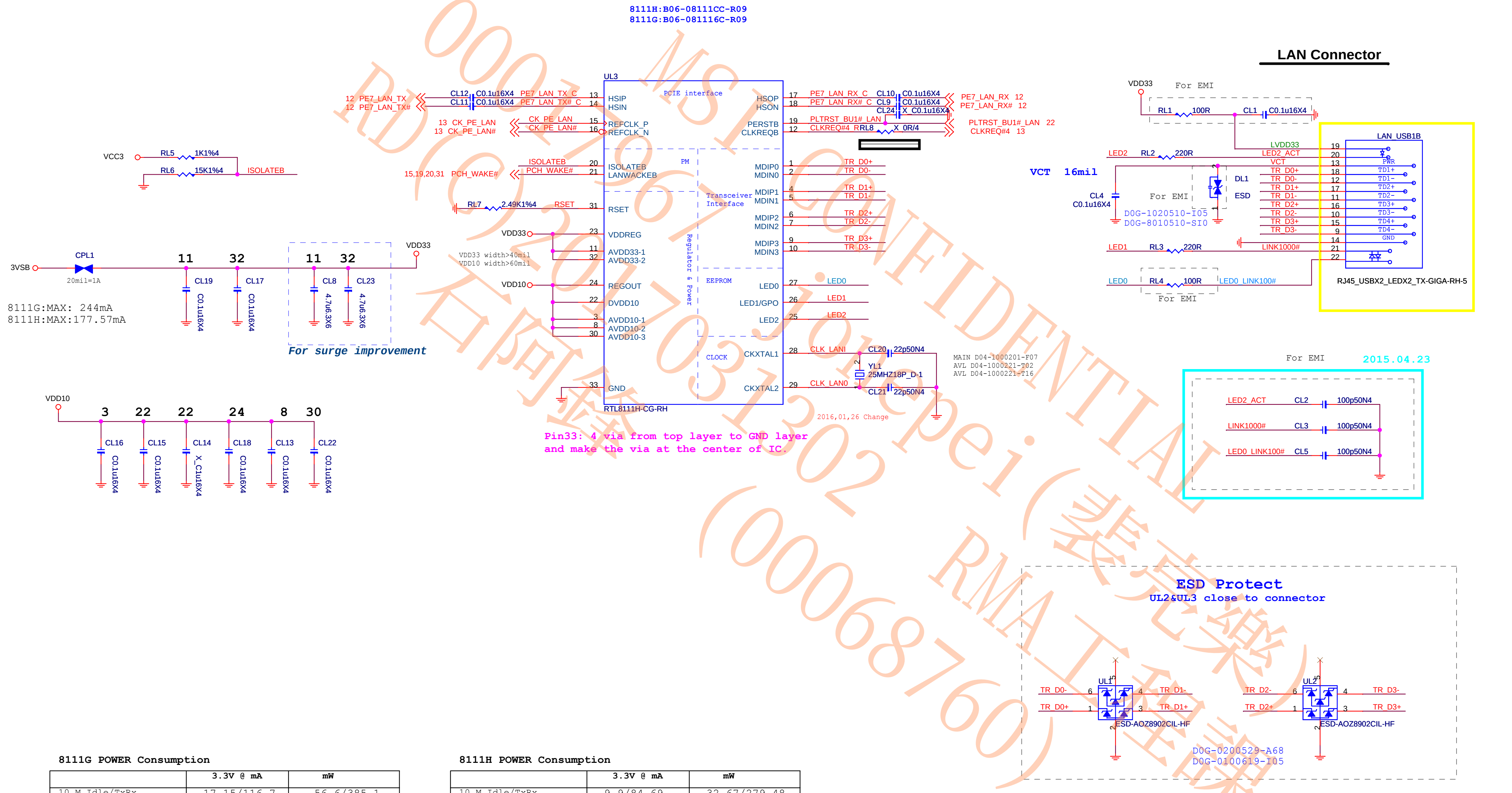
LED
: D0C-040S600-E07

LED
フ : D0C-040T300-H91
AVL: D0C-040S300-E07

LED
RGB : D0C-040R700-H91

MICRO-STAR INT'L CO.,LTD		
MS-7A70		
Size: Custom	Document Description: AUDIO - depop circuit	Rev: 10
Date: Monday, September 12, 2016	Sheet 26 of 56	

RTL8111G/RTL8111H Giga LAN



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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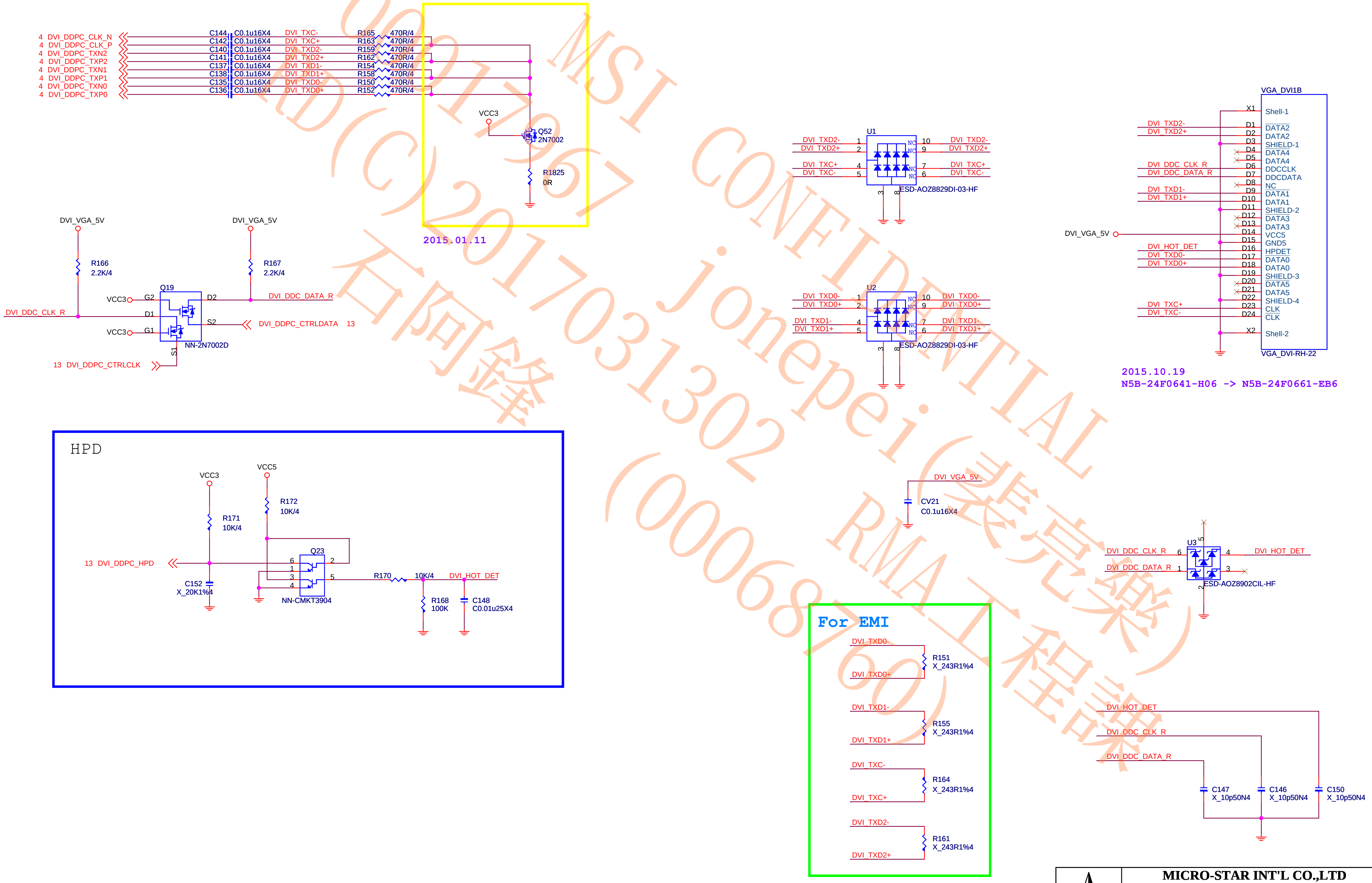
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



MICRO-STAR INT'L CO.,LTD			
MS-7A70			
Size: Custom	Document Description: DVI		Rev: 10
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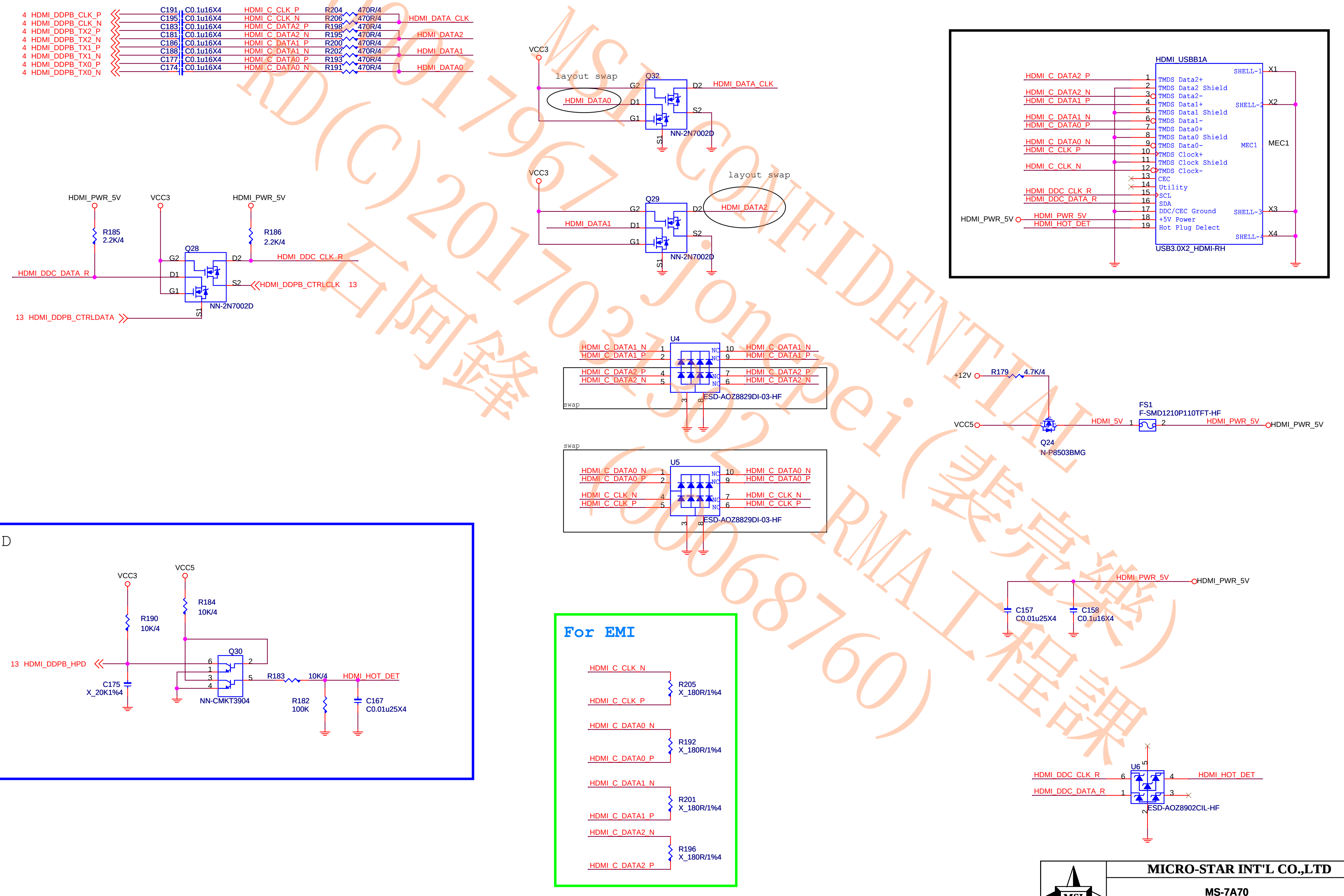
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



MICRO-STAR INT'L CO.,LTD

MS-7A70

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Custom	HDMI Connector	10

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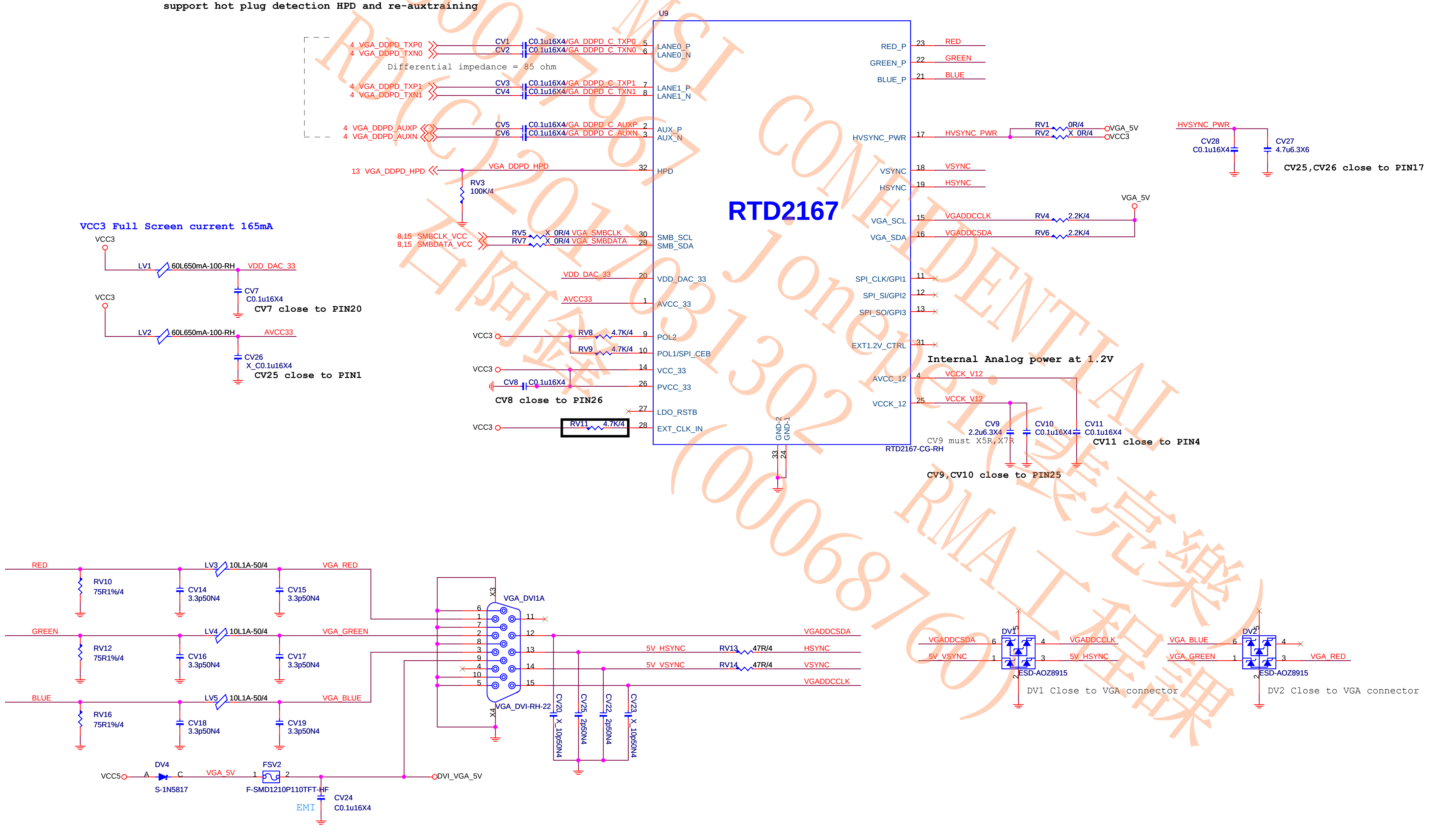
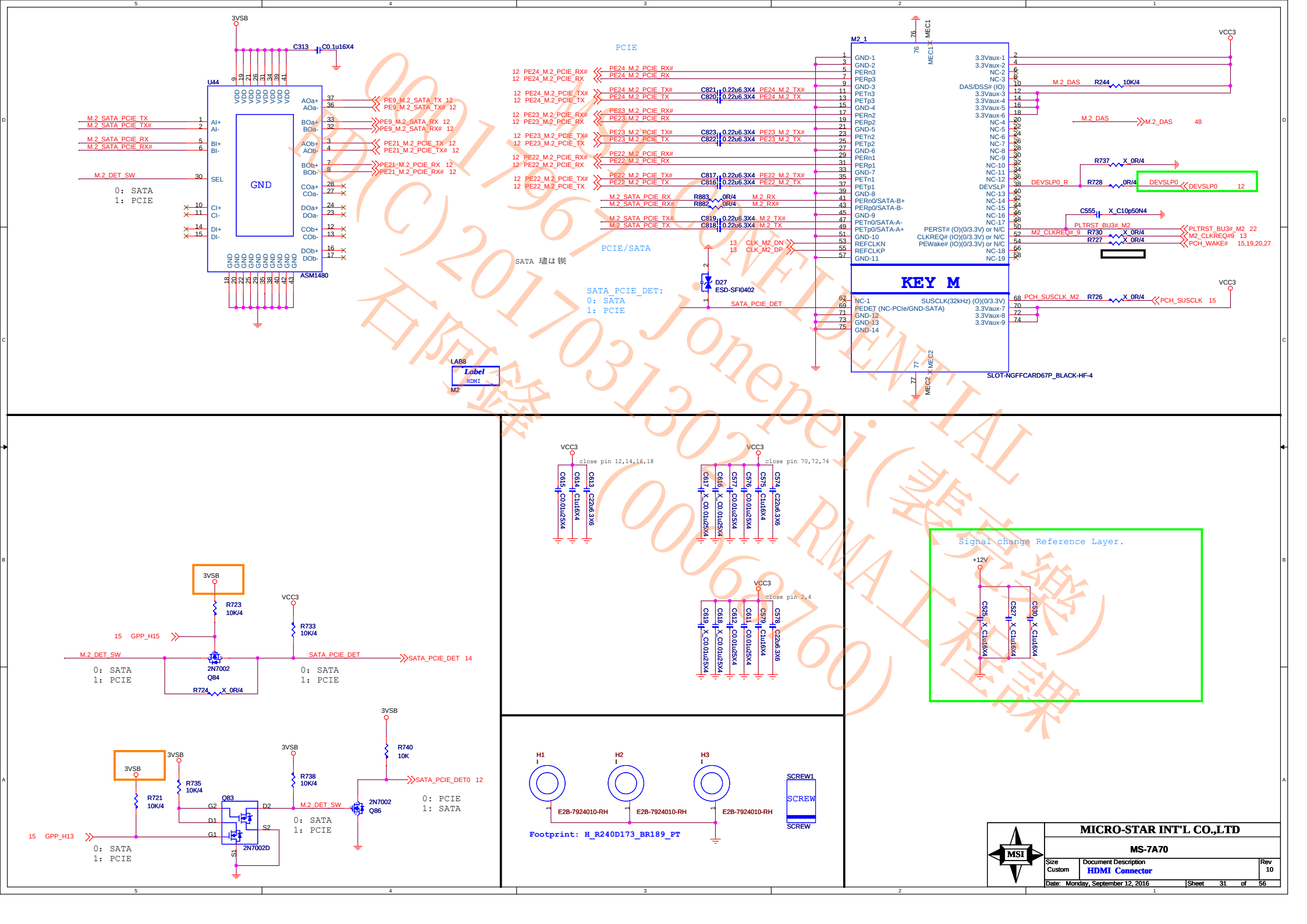
MAX Resolution:1920x1440@60Hz,RB

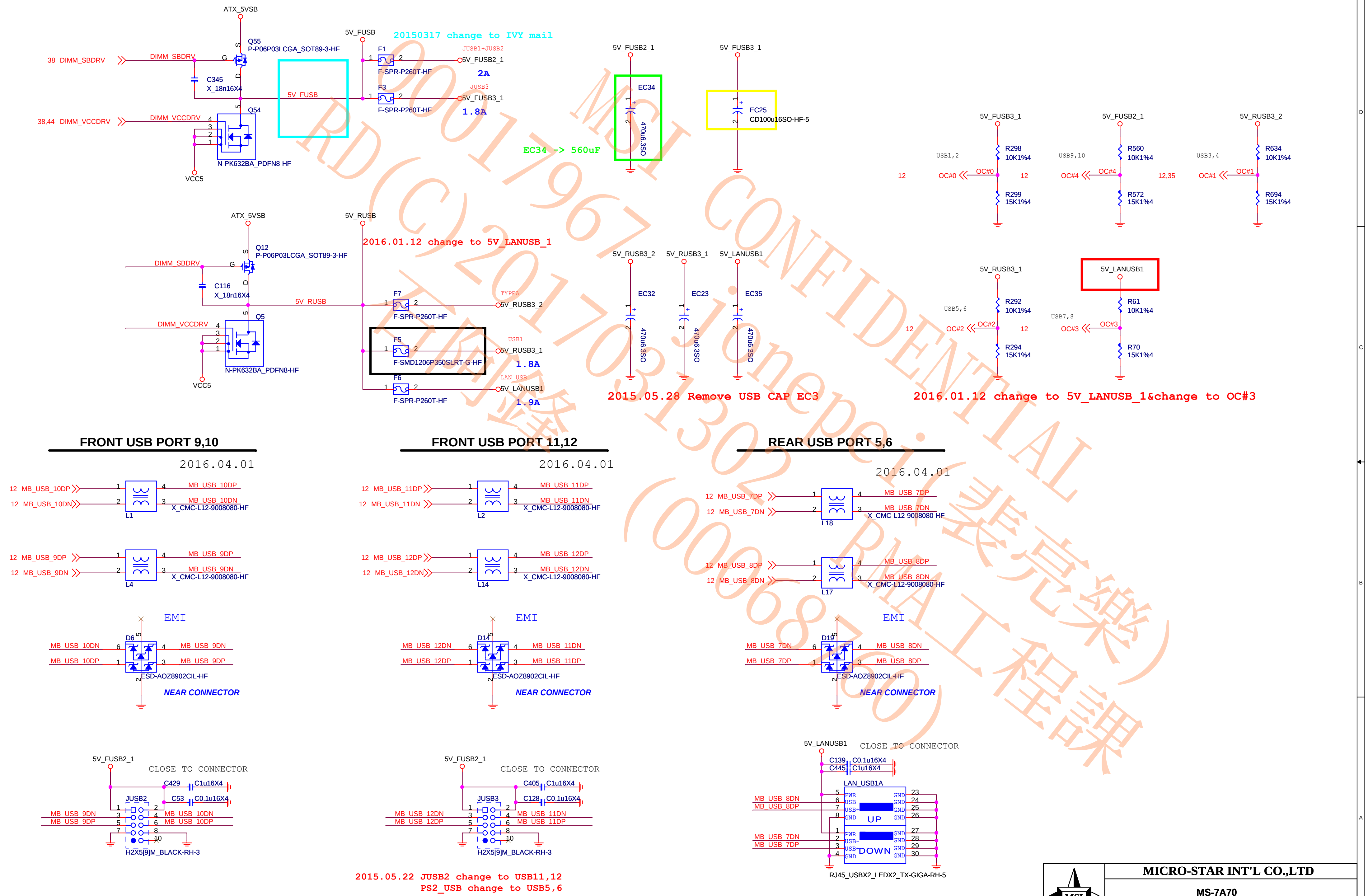
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

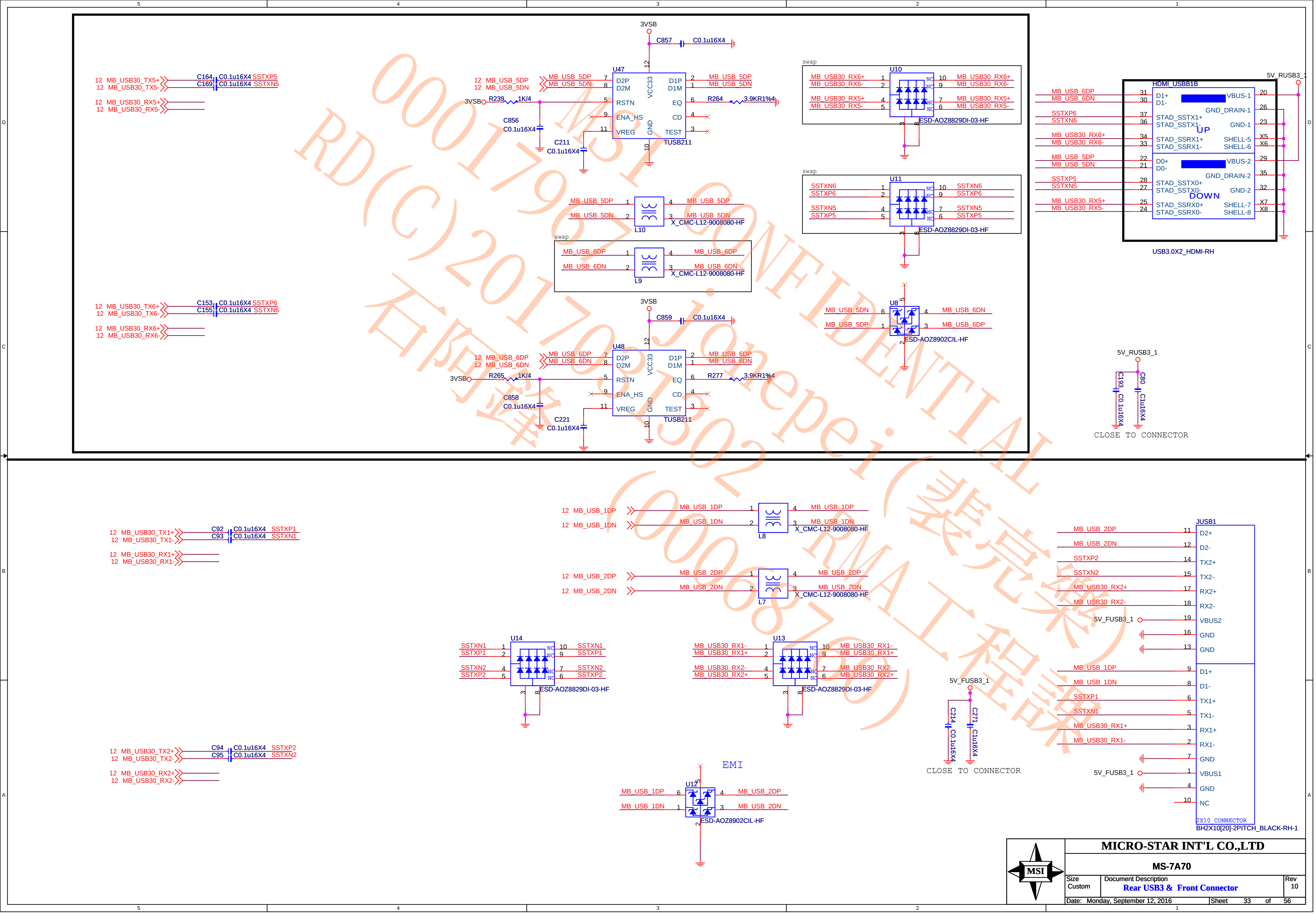


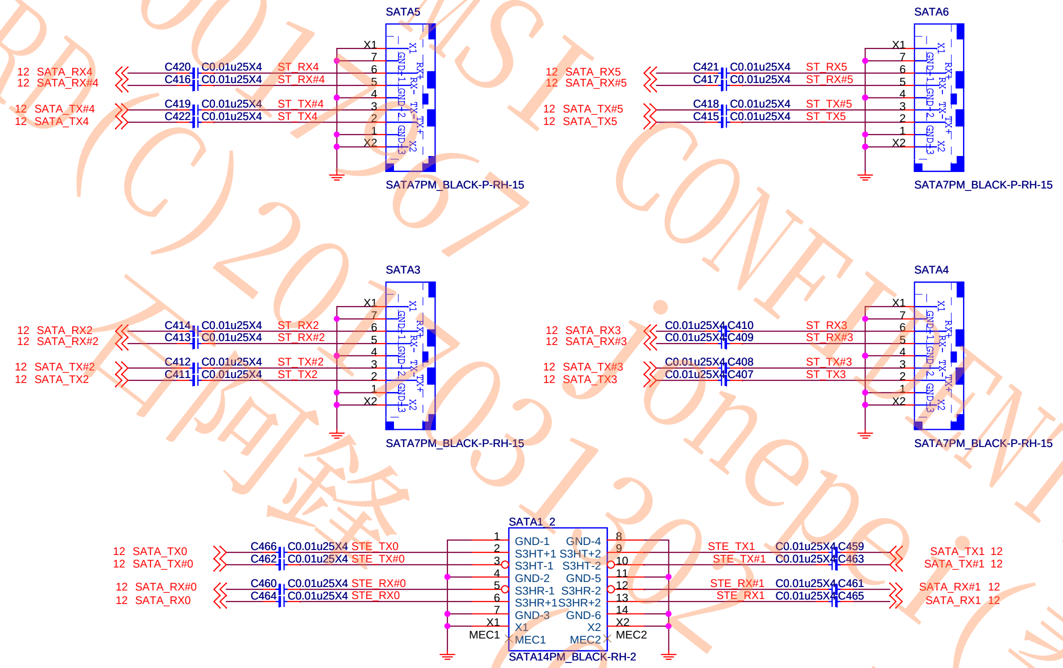
MICRO-STAR INT'L CO.,LTD				
Size: Custom	Document Description: VGA Connector			Rev: 10
Date: Monday, September 12, 2016		Sheet 30	of 56	


U44
ASM1480
GND
M.2_SATA_PCIE_TX
M.2_SATA_PCIE_TX#
M.2_SATA_PCIE_RX
M.2_SATA_PCIE_RX#
M.2_DET_SW
0: SATA
1: PCIE
C313
C0.1u16X4
PCIE
PCIE/SATA
SATA 璀は钡
SATA_PCIE_DET:
0: SATA
1: PCIE
D27
ESD-SFI0402
M2_1
KEY M
SLOT-NGFFCARD67P_BLACK-HF-4
M.2_DAS
R244
10K/4
R737
X_0R/4
R728
0R/4
DEVSLP0
C555
X_C10p50N4
R730
R727
R726
PCH_SUSCLK
LAB8
Label
HDMI
M2
R723
10K/4
R733
10K/4
R724
X_0R/4
2N7002
Q84
SATA_PCIE_DET
R721
10K/4
R735
10K/4
R738
10K/4
R740
10K
Q83
2N7002D
2N7002
Q86
SATA_PCIE_DET0
GPP_H15
GPP_H13
close pin 12,14,16,18
close pin 70,72,74
close pin 2,4
Signal change Reference Layer.
+12V
H1
H2
H3
E2B-7924010-RH
SCREW1
SCREW
Footprint: H_R240D173_BR189_PT
MICRO-STAR INT'L CO.,LTD
MS-7A70
Size
Custom
Document Description
HDMI Connector
Rev
10
Date: Monday, September 12, 2016
Sheet 31 of 56



MICRO-STAR INT'L CO.,LTD		
MS-7A70		
Size: Custom	Document Description: USB2.0 Connector	Rev: 10
Date: Monday, September 12, 2016	Sheet 32 of 56	



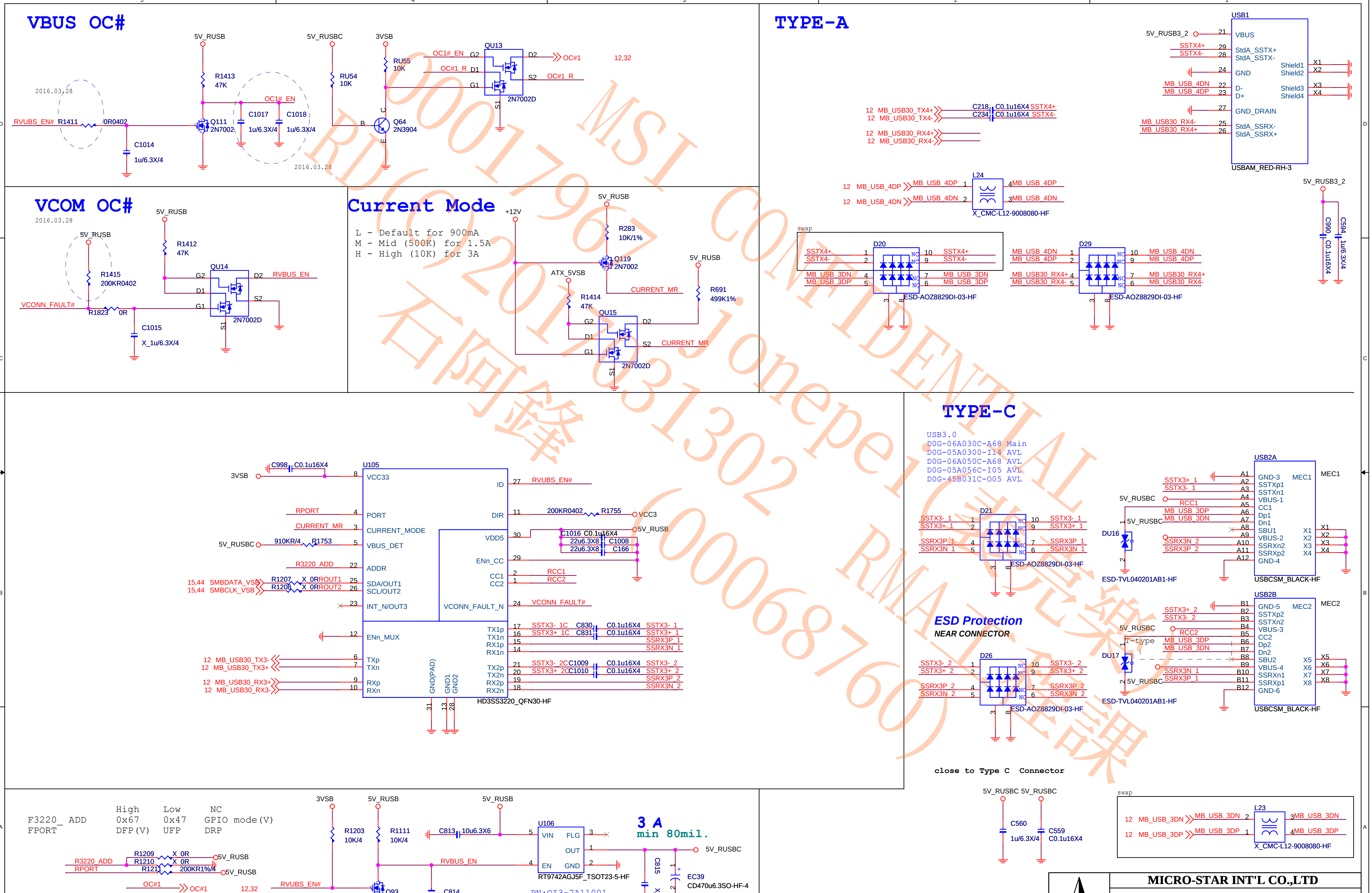


MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	SATA connector	10

Date: Monday, September 12, 2016 | Sheet 34 of 56



MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	CUT_VABT circuit	10

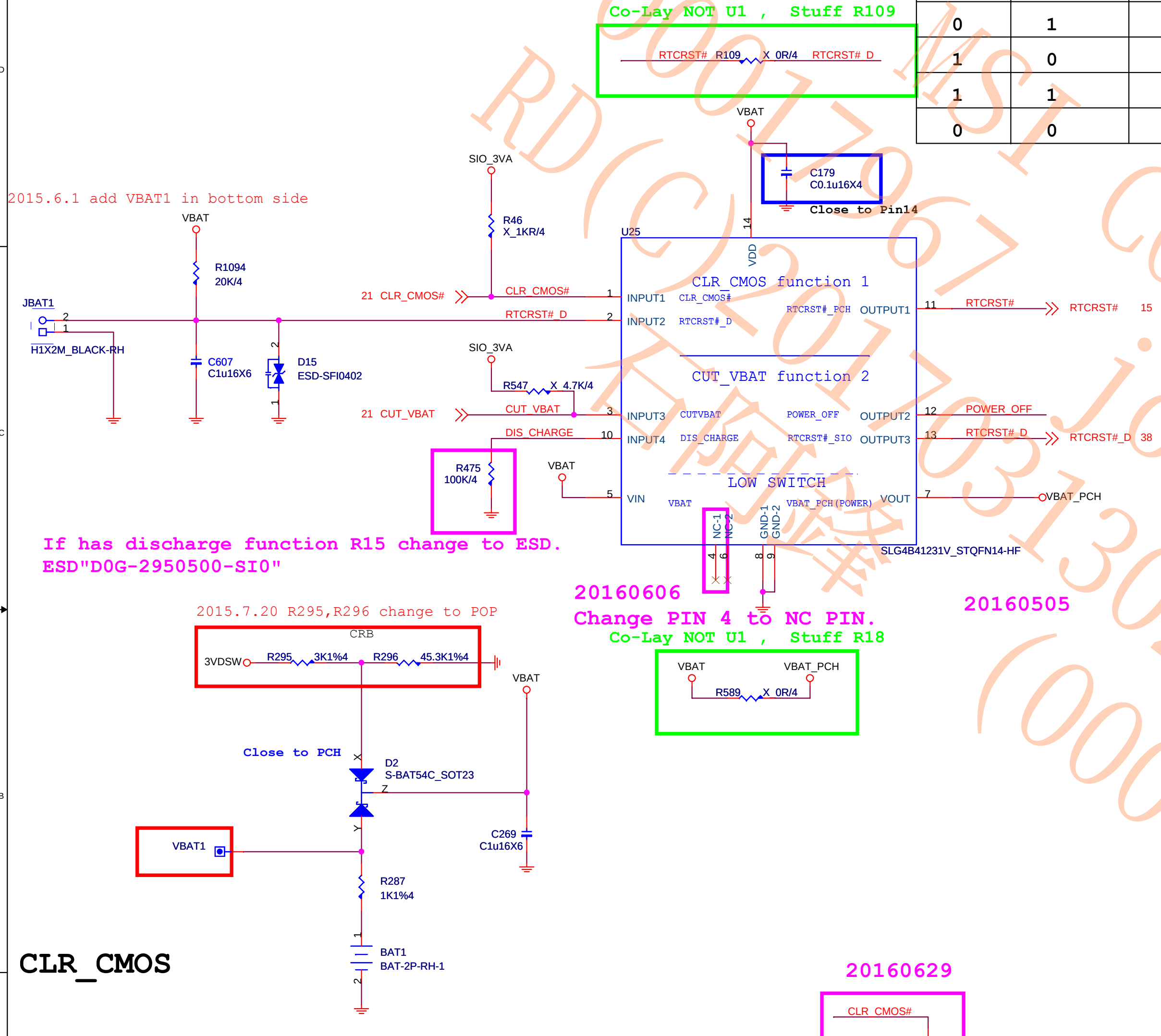
Date: Monday, September 12, 2016 Sheet 35 of 56

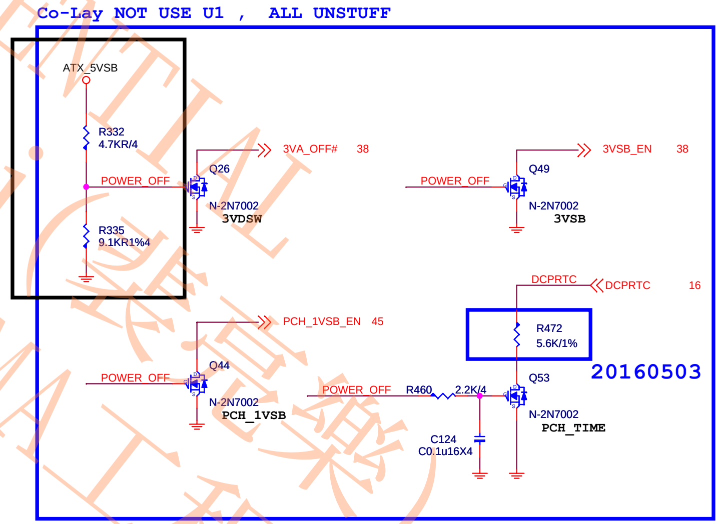
Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

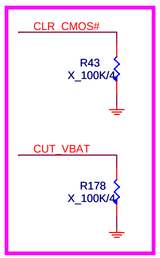
Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default





20160629

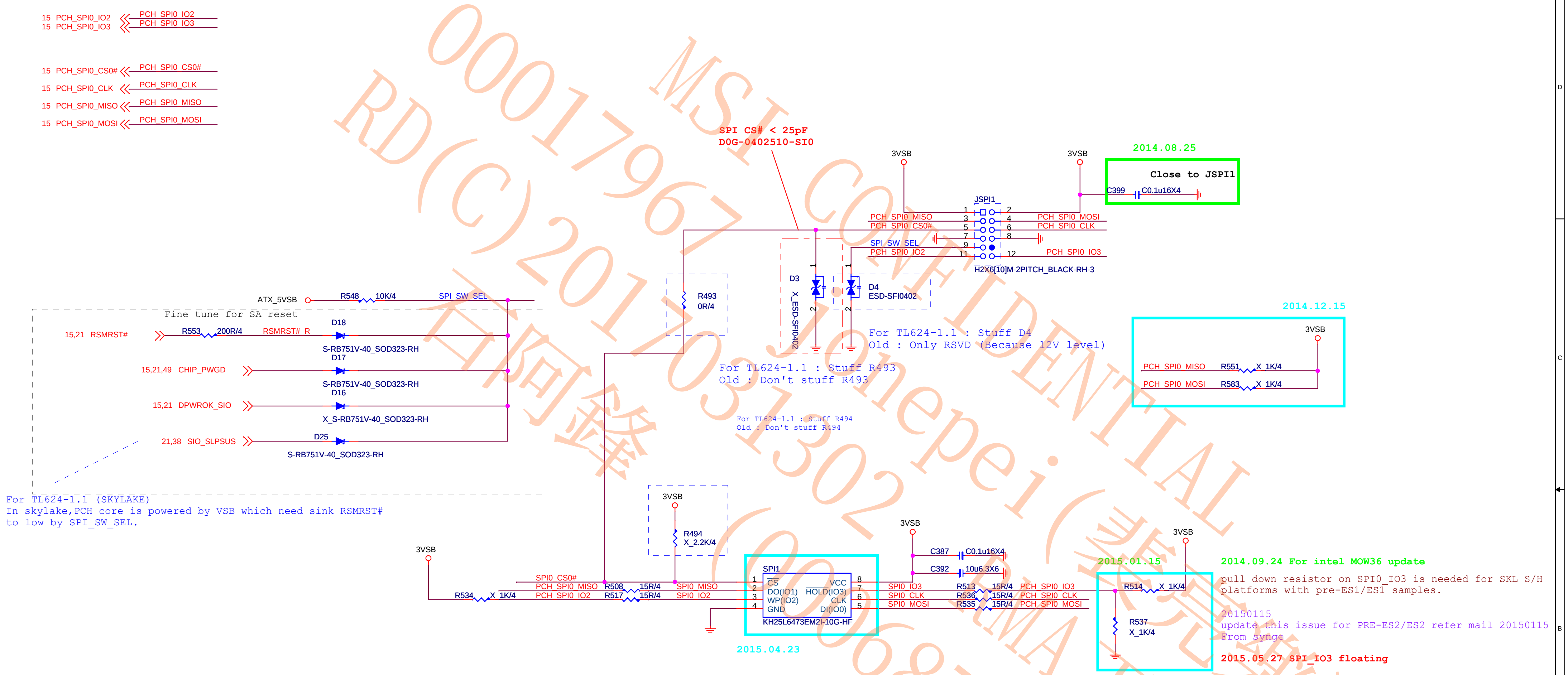


MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	CUT_VABT circuit	10

Date: Monday, September 12, 2016 Sheet 36 of 56



* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component Q14.G Pull-high to ATX_5VSB , Q14 must select "Vth" under 1V (Component Suggestion as below)

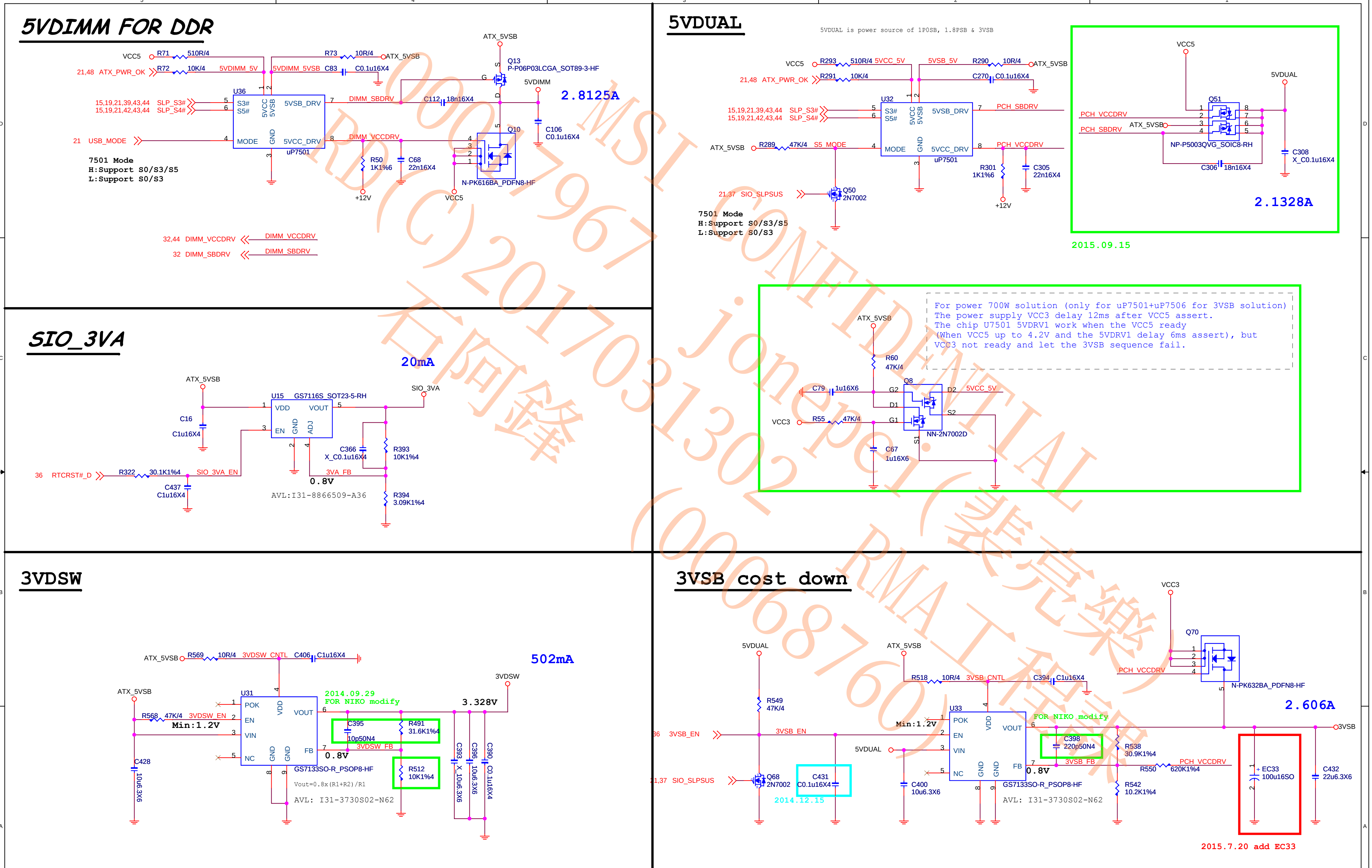
D03-0341409-A68 / D03-0230019-A30

MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	BIOS ROM	10

Date: Monday, September 12, 2016 Sheet 37 of 56



MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	ACPI CONTROLLER	10

Date: Monday, September 12, 2016 Sheet 38 of 56

Vcpu (SVID)=100A
VGT (SVID)=48A

CRB 1.0 update
RSVD R582
2014.09.24

2015.7.20 R90 change to 36.5K

2014.12.15

2015.08.04 change to C11-4757322-S02

For drvirer Gate Mos Use

Close to PWM

OCP:100A

OCP:75A

SLP_S3# assertion to IMVP VRM_EN deassertion max:1us

close to phase1 CHOKE

close to phase1 CHOKE

OFFSET MODE 0.7V enable
Internal 1.7V系耕竟
MAX:600mV
Fequency 400K

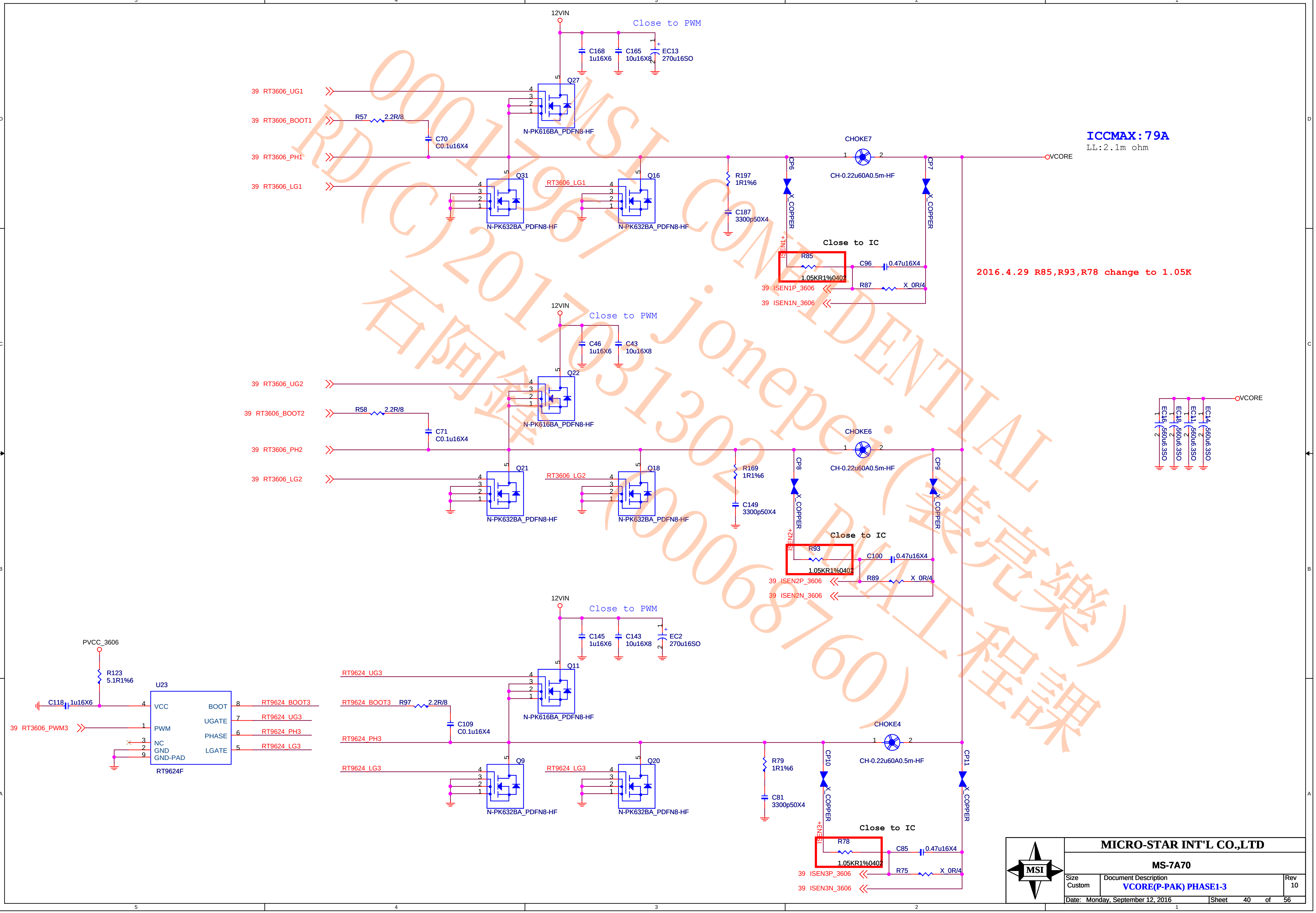
パpin3 and pin43桔

2015.6.16 R621 change to short pad

2015.7.20
R129 change to 150K
R139 change to 15K

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
SET3 control VR address
SETA1 cintrol ICCMAX,OCP setting
SETA2 control Internal compensation

MICRO-STAR INT'L CO.,LTD			
MS-7A70			
Size: Custom	Document Description: PWM-RT3606BC		Rev: 10
Date: Monday, September 12, 2016		Sheet 39 of 56	

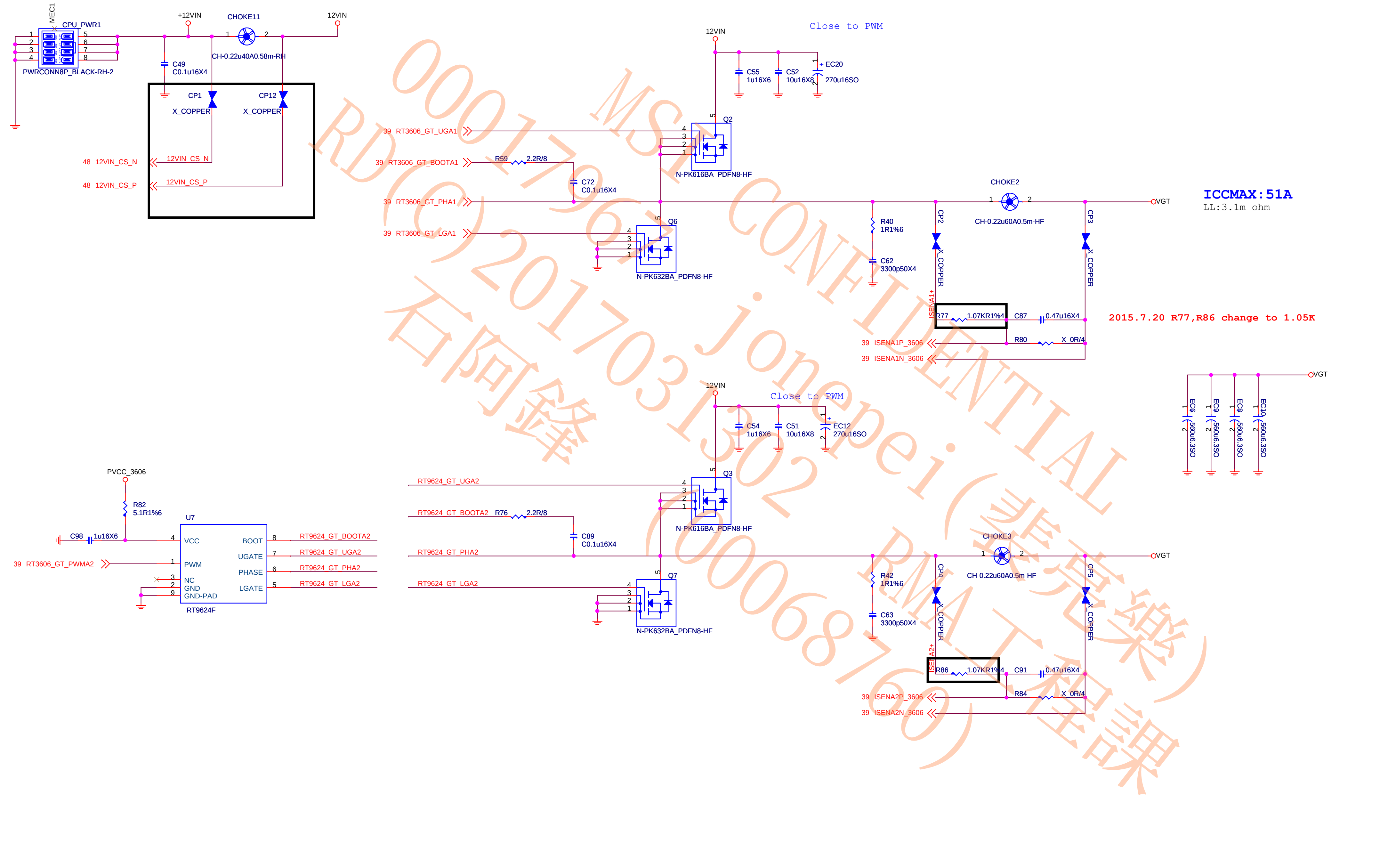


MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	VCORE(P-PAK) PHASE1-3	10

Date: Monday, September 12, 2016 Sheet 40 of 56



MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	VGT(P-PAK) PHASE1-2	10

Date: Monday, September 12, 2016 | Sheet 41 of 56

DDR4_1.2V
2.5A+9.5A+1.2A=13.2A
1.2A FOR DDR VTT

9.5A FOR 4DIMM

2.5A FOR CPU

OCP =13.2A*1.5=19.8A
Rocs(R95)=OCP*Rdson[Low side]/10uA
=19.8A*4.6mohm/10uA
=9.108K

20151230 Update

Pull up change by layout

uP1504 & RT8125
VCC Input Range : 4.5V to 13.2V

2015.07.14 Add +12V loading

RT8125C R65->10R
up1540 R65->2.2R

2015.07.14 update to 0603

EN:2.4V

U37 RT8125EGQW_WDFN10-HF

FB:0.8V
Vout=0.8*(1+R1/R2)

Vout=0.8V*(1+R70/R79)=0.8V*(1+1k/2.15k)=1.172V

Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A

(OS-CON CAP)

2015.05.12 Remove H/L side

1.2V,13.2A

Datasheetそ入瑣衡
Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

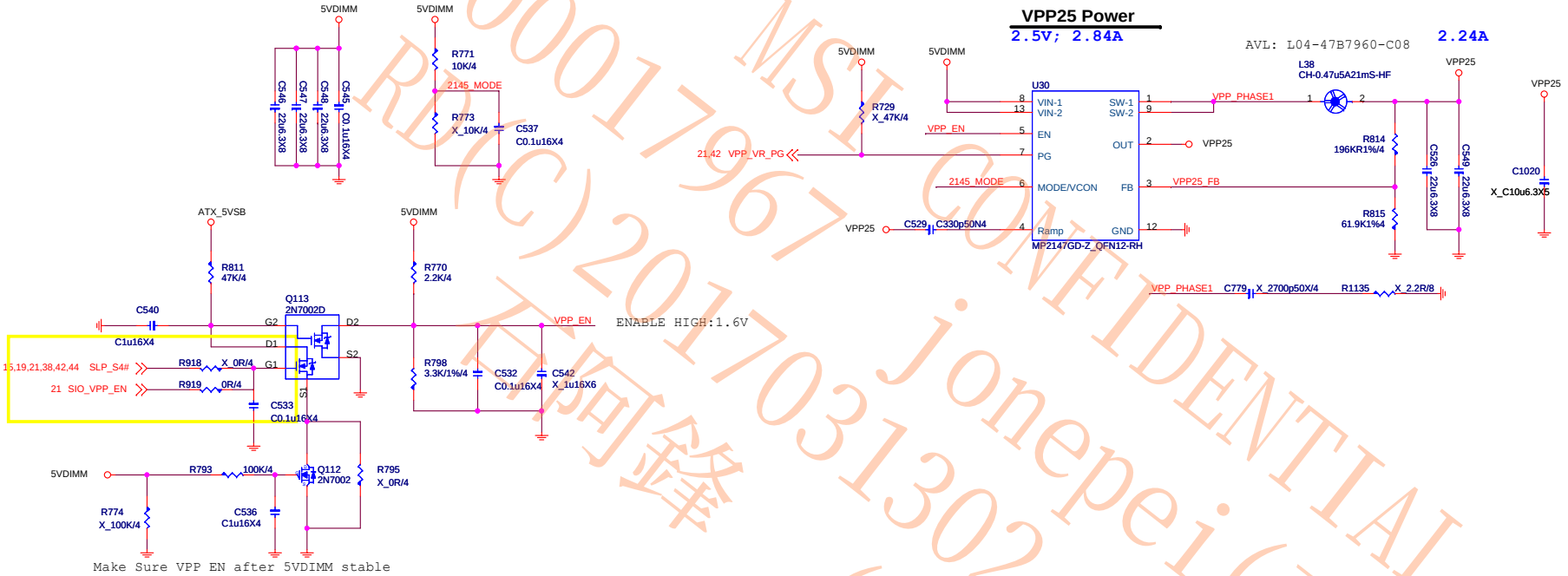
瑣肢 CAP ESR瑣衡,0.2432uH≦L≦1.2897uH

From SIO pin 87
2015.05.19 Stuff

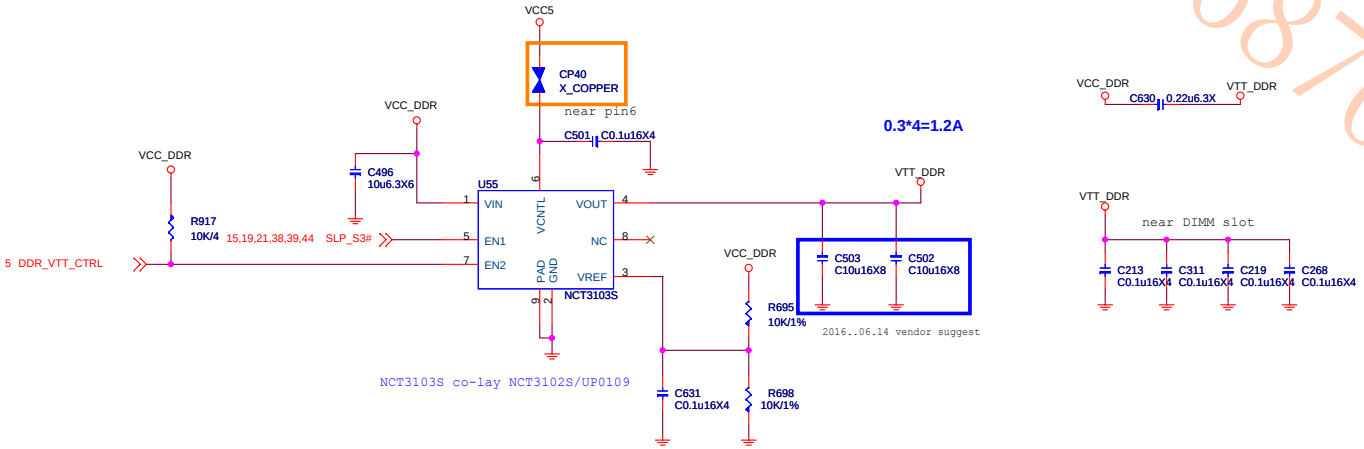
MICRO-STAR INT'L CO.,LTD	
MS-7A70	
Size: Custom	Document Description: DDR POWER-RT8125C-1PHASE
Rev: 10	
Date: Monday, September 12, 2016	Sheet 42 of 56

4DIMM :2.84A FOR DDR VPP2.5V

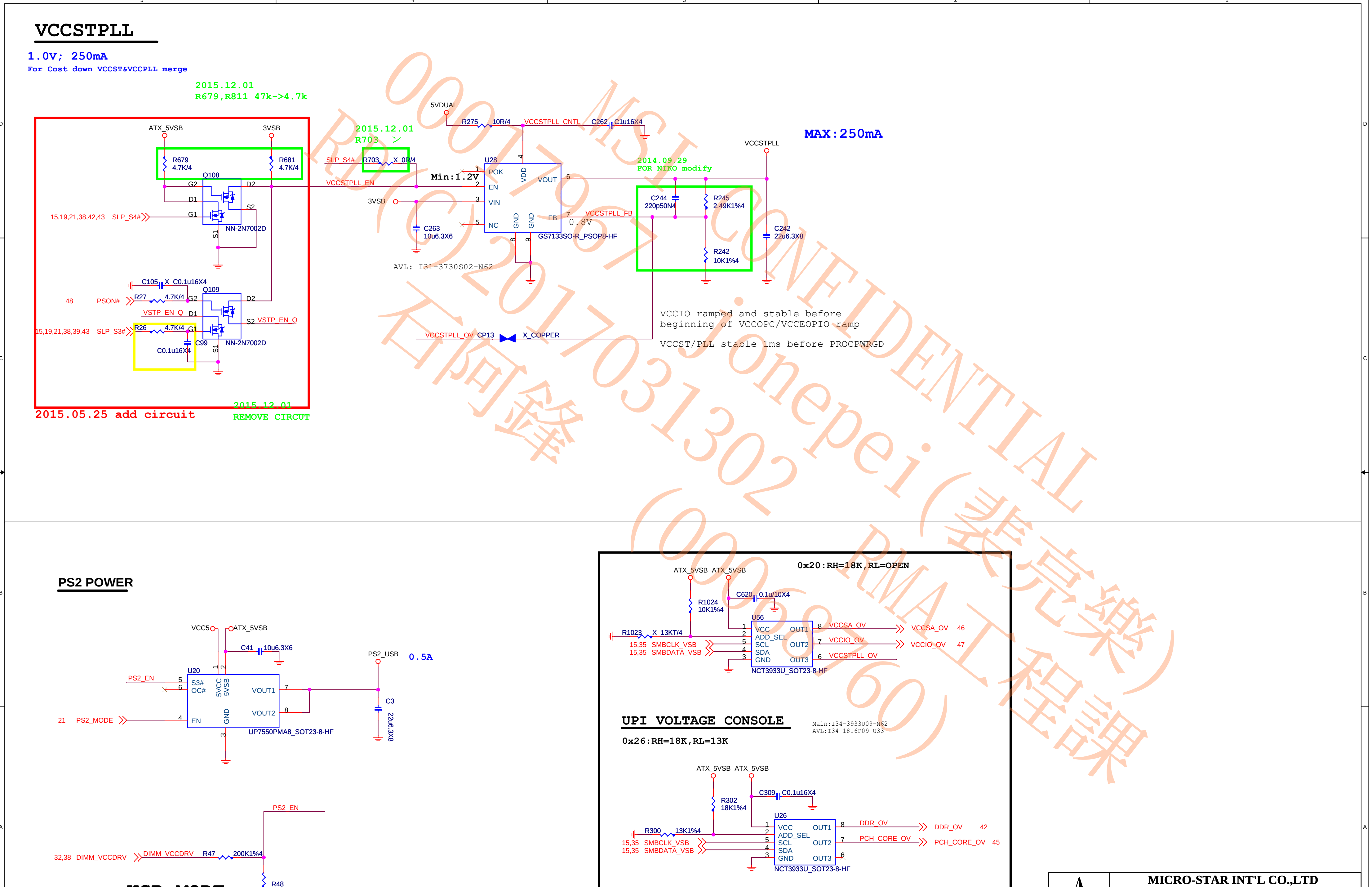
OCP=2.24A*1.5=3.36A????



DDR VTT Power



MICRO-STAR INT'L CO.,LTD		
MS-7A70		
Size: Custom	Document Description: DDR-MP2147-VPP25	Rev: 10
Date: Monday, September 12, 2016	Sheet 43 of 56	



MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	CPU PWR_ST/PLL	10

Date: Monday, September 12, 2016 | Sheet 44 of 56

PCH_1VSB

1.0V; 11A

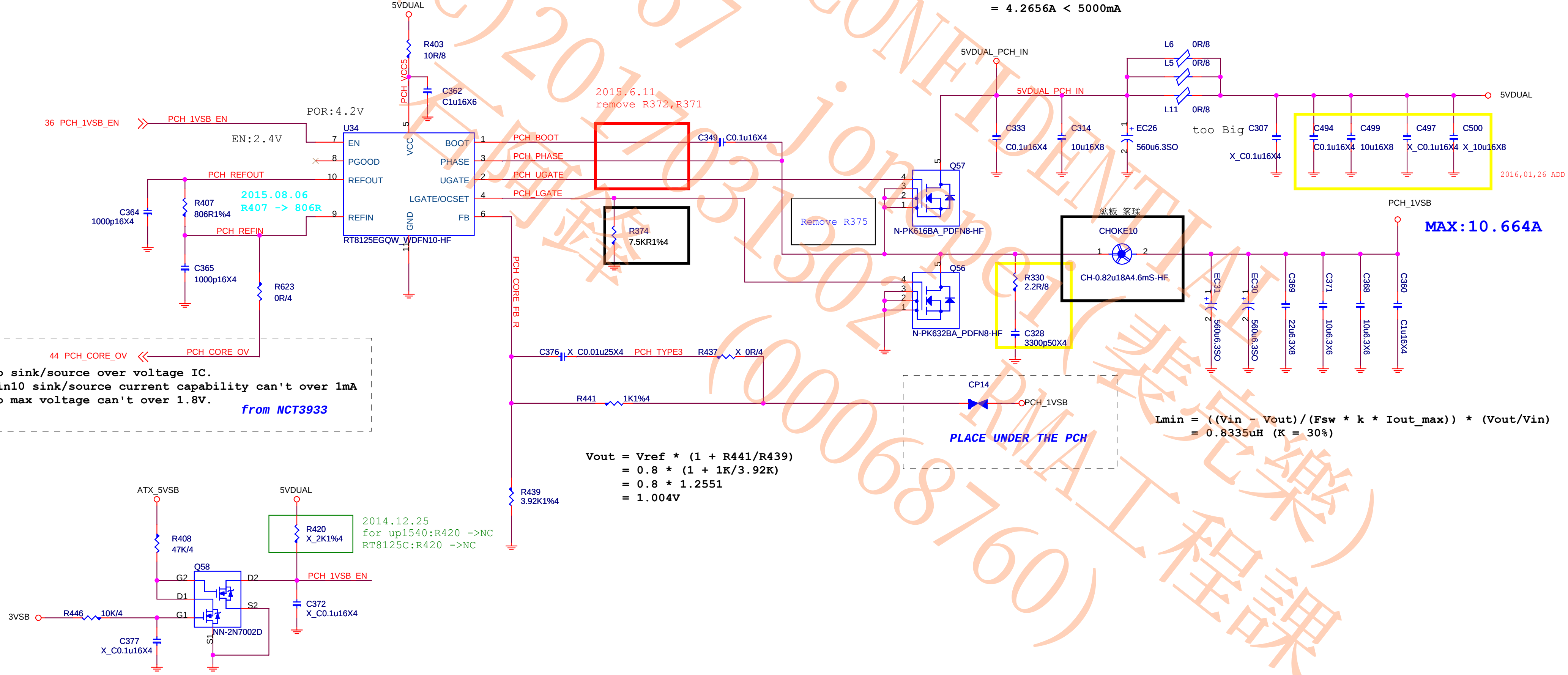
OCP = 11A*1.5=16.5A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11A * 4.6mohm / 10uA
= 7.59K

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

2015.04.23 change to UP1540

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA



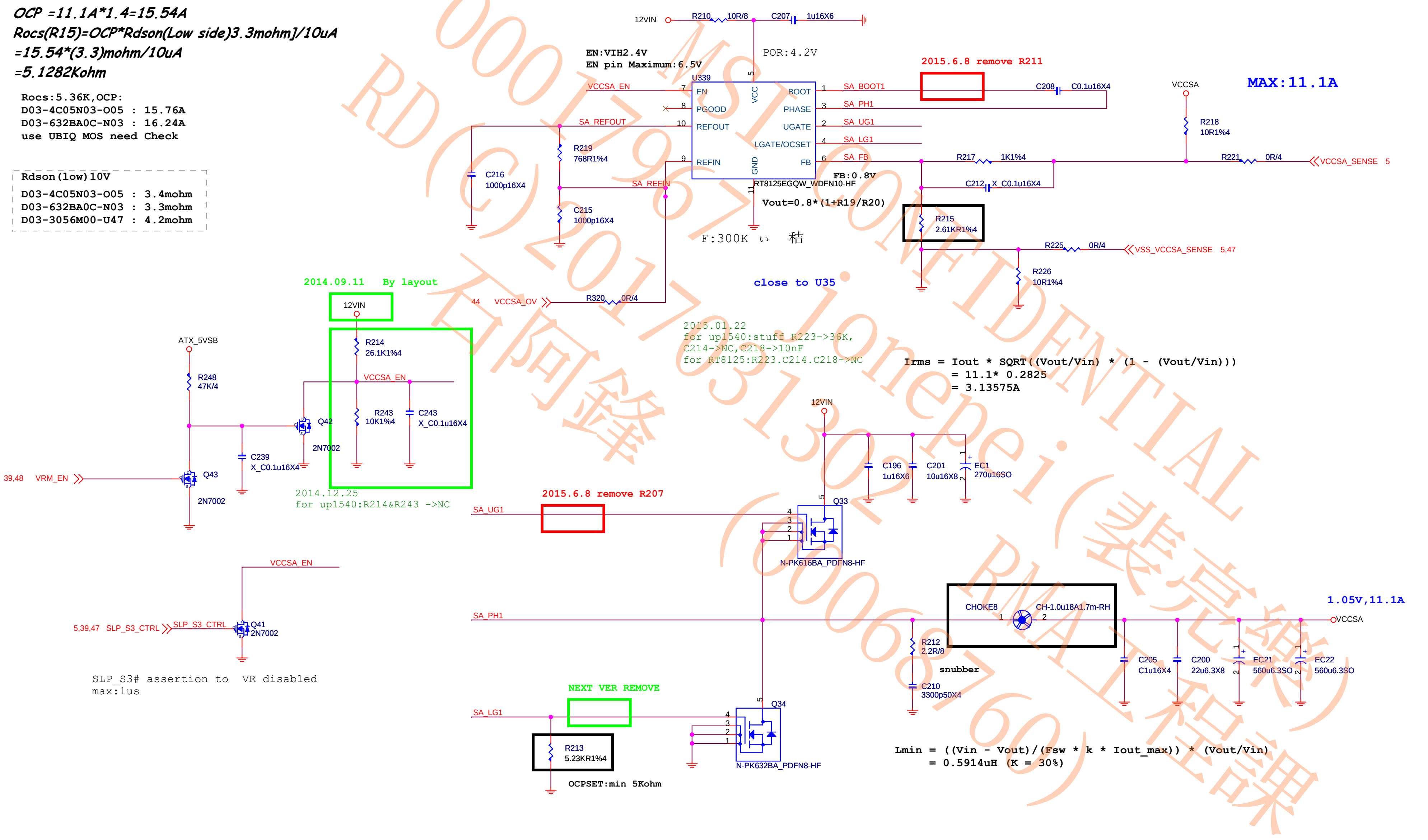
to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

Vout = Vref * (1 + R441/R439)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

MICRO-STAR INT'L CO.,LTD		
MS-7A70		
Size: Custom	Document Description: PCH Core power	Rev: 10
Date: Monday, September 12, 2016	Sheet 45 of 56	

SA Power:1.05V,11.1A



OCP =11.1A*1.4=15.54A
Rocs(R15)=OCP*Rdson(Low side)3.3mohm)/10uA
=15.54*(3.3)mohm/10uA
=5.1282Kohm
Rocs:5.36K,OCP:
D03-4C05N03-005 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check
Rdson(low)10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm
12VIN
R210 10R/8
C207 1u16X6
EN:VIH2.4V
EN pin Maximum:6.5V
POR:4.2V
U339
VCCSA_EN
EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB
RT8125EGQW_WDFN10-HF
SA_BOOT1
SA_PH1
SA_UG1
SA_LG1
SA_FB
SA_REFOUT
SA_REFIN
2015.6.8 remove R211
C208 C0.1u16X4
VCCSA
MAX:11.1A
R218 10R1%4
R217 1K1%4
R221 0R/4
VCCSA_SENSE 5
C212 X_C0.1u16X4
FB:0.8V
Vout=0.8*(1+R19/R20)
R215 2.61KR1%4
R225 0R/4
VSS_VCCSA_SENSE 5,47
R226 10R1%4
R219 768R1%4
C216 1000p16X4
C215 1000p16X4
F:300K
close to U35
2014.09.11 By layout
12VIN
R214 26.1K1%4
VCCSA_EN
R243 10K1%4
C243 X_C0.1u16X4
44 VCCSA_OV
R320 0R/4
2015.01.22
for up1540:stuff R223->36K,
C214->NC,C218->10nF
for RT8125:R223.C214.C218->NC
ATX_5VSB
R248 47K/4
Q42 2N7002
C239 X_C0.1u16X4
39,48 VRM_EN
Q43 2N7002
2014.12.25
for up1540:R214&R243 ->NC
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.2825
= 3.13575A
12VIN
C196 1u16X6
C201 10u16X8
EC1 270u16SO
2015.6.8 remove R207
SA_UG1
Q33
N-PK616BA_PDFN8-HF
VCCSA_EN
5,39,47 SLP_S3_CTRL
SLP_S3_CTRL
Q41 2N7002
SLP_S3# assertion to VR disabled
max:1us
SA_PH1
CHOKE8
CH-1.0u18A1.7m-RH
1.05V,11.1A
VCCSA
R212 2.2R/8
snubber
C210 3300p50X4
C205 C1u16X4
C200 22u6.3X8
EC21 560u6.3SO
EC22 560u6.3SO
NEXT VER REMOVE
SA_LG1
Q34
N-PK632BA_PDFN8-HF
R213 5.23KR1%4
OCPSET:min 5Kohm
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

MICRO-STAR INT'L CO.,LTD

MS-7A70

Size	Document Description	Rev
Custom	VCCSA - POWER RT8125E	10

Date: Monday, September 12, 2016 Sheet 46 of 56

VCCIO

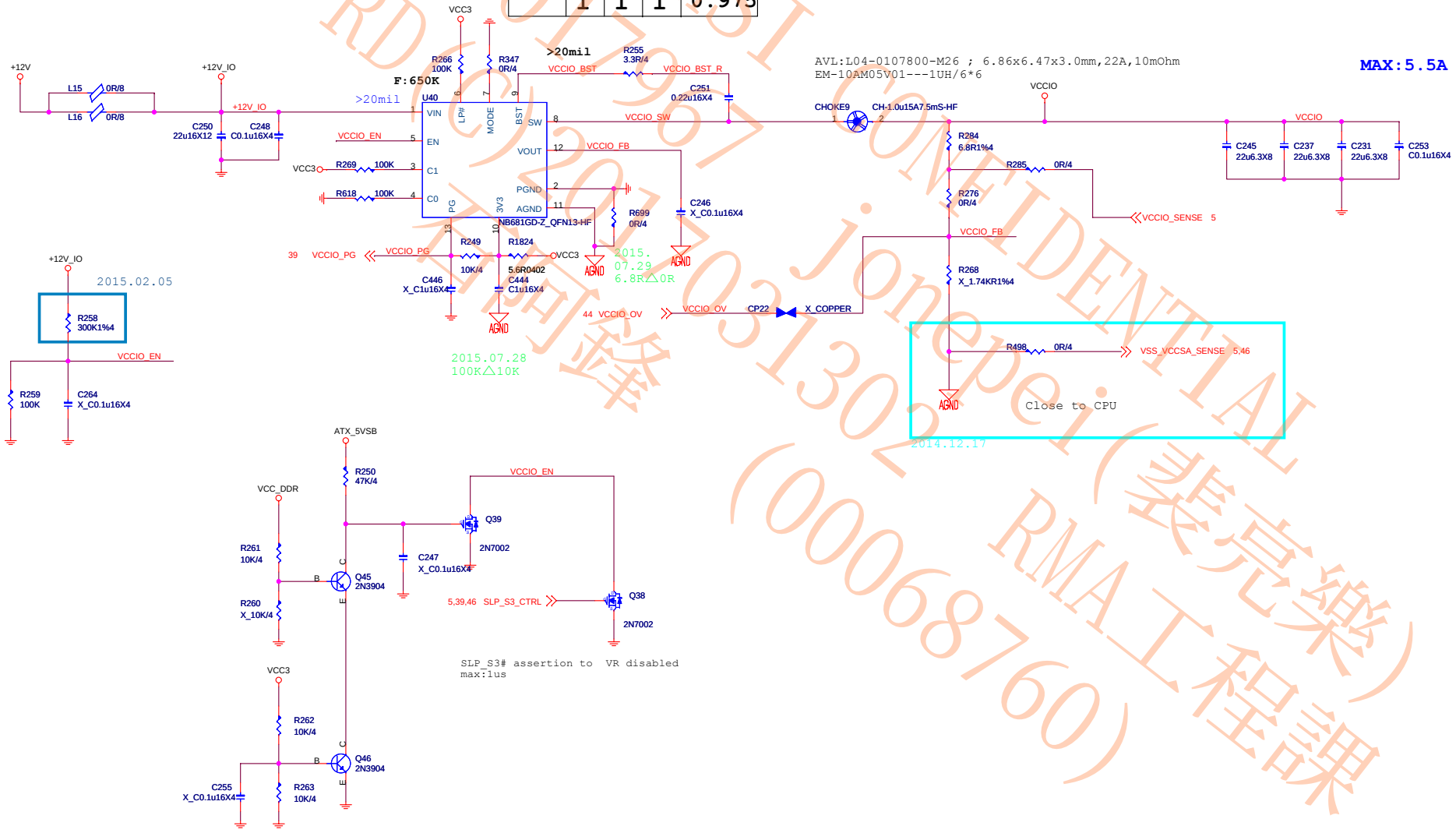
0.95V; 5.5A

IMAX 6A

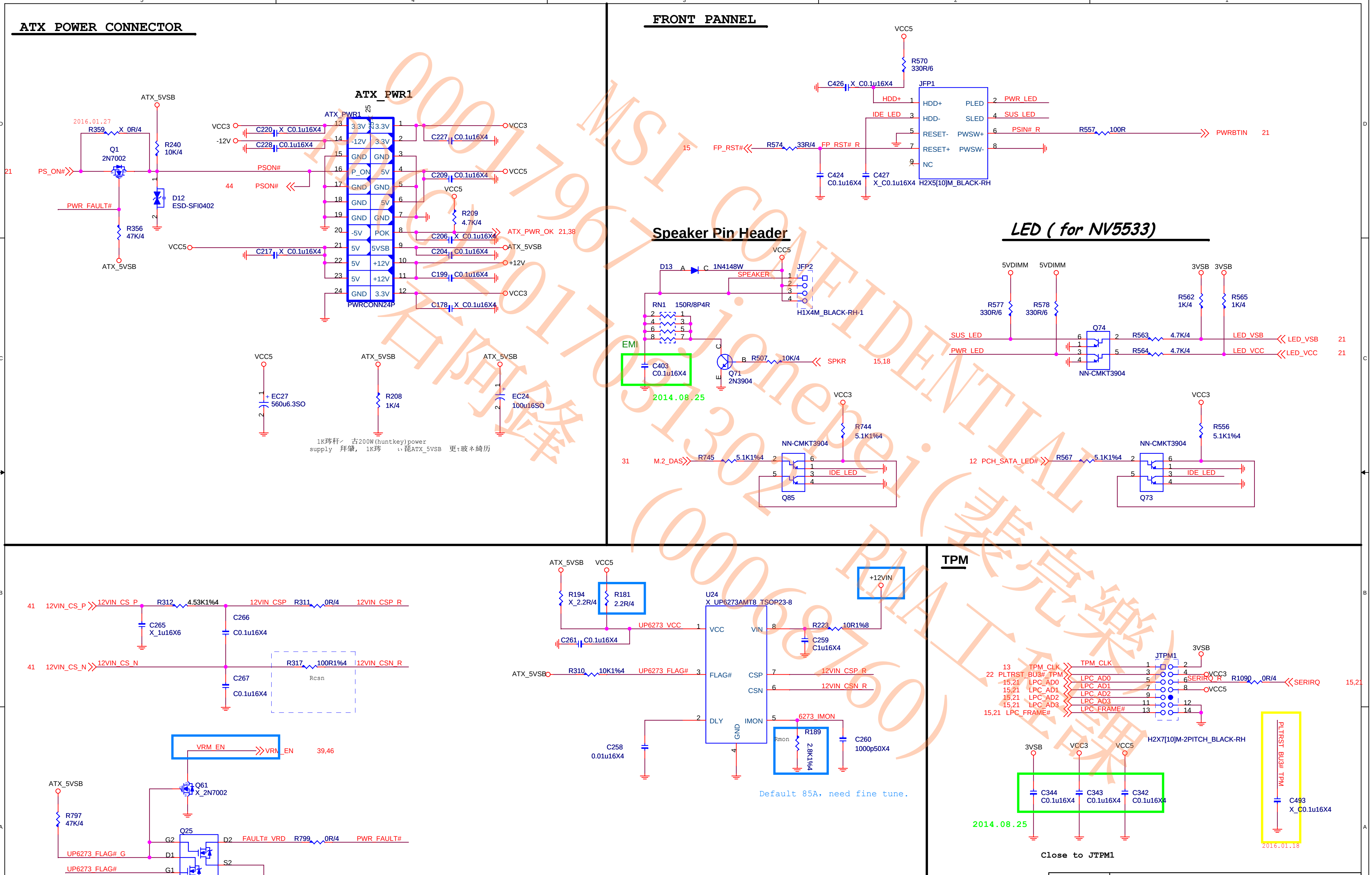
ILIMIT=8.5~9A

OCP=5.5A*1.5=8.25A

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



MICRO-STAR INT'L CO.,LTD	
MS-7A70	
Size: Custom	Document Description: VCCIO - POWER NB671
Rev: 10	
Date: Monday, September 12, 2016	Sheet 47 of 56



MICRO-STAR INT'L CO.,LTD

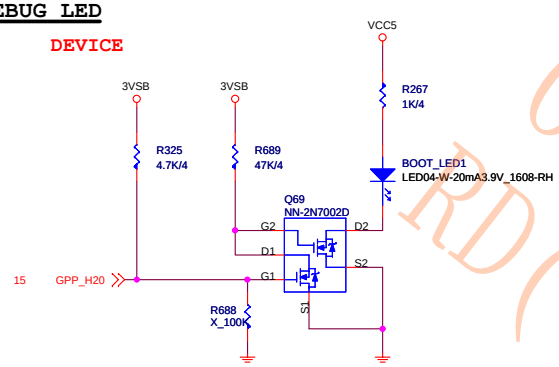
MS-7A70

Size	Document Description	Rev
Custom	ATX F_Panel/TPM/PWR FAULT	10

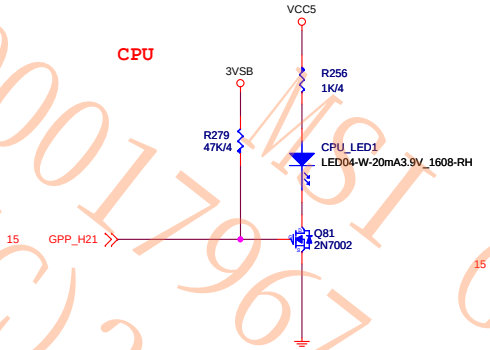
Date: Monday, September 12, 2016 Sheet 48 of 56

DEBUG LED

DEVICE

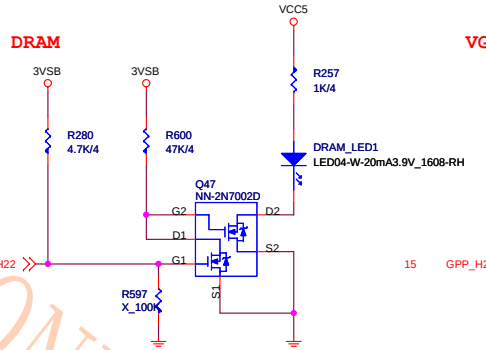


CPU



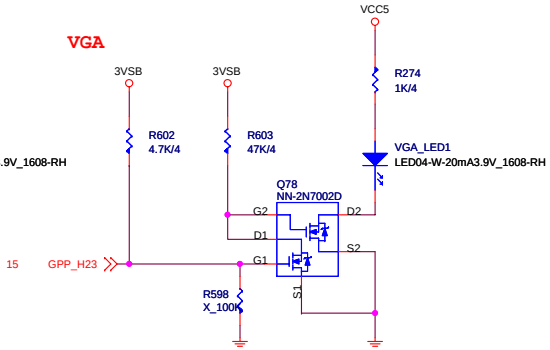
2015.6.8 remove R559 R286 R278

DRAM

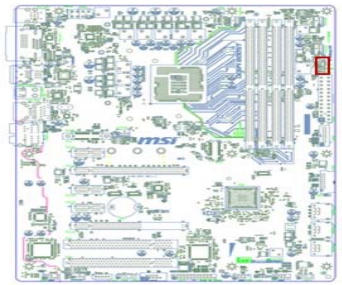


2015.6.8 remove R601 R323

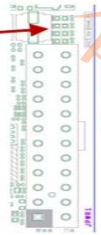
VGA



2015.6.8 remove R604 R326



EZ Debug
必須需位於
JPWR1上方



LED方向 &
文字面樣式

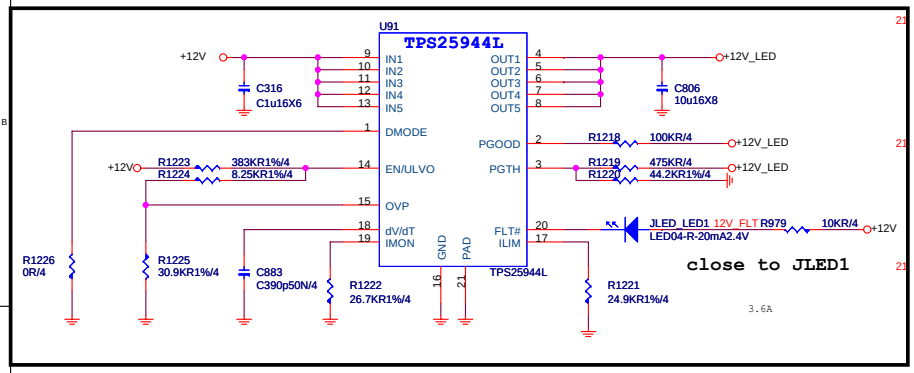
LED
：D0C-040P100-H91
AVL: D0C-040S500-E07

LED
ア：D0C-040T200-H91
AVL: D0C-040S200-E07

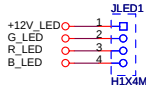
GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
獵	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

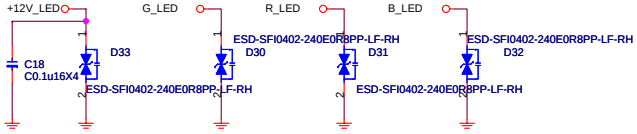
RGB_LED Connector

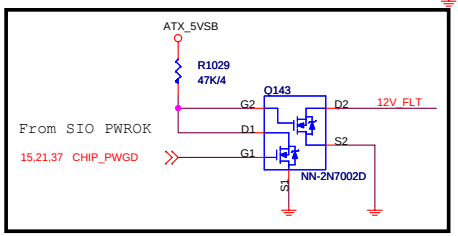
2016.07.06 Use TPS25944L

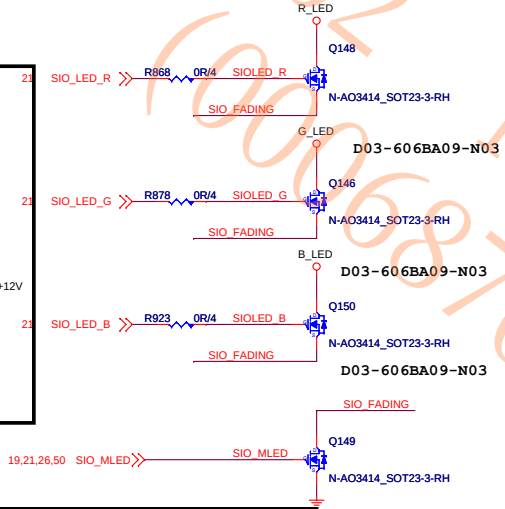


N31-1040321-P05

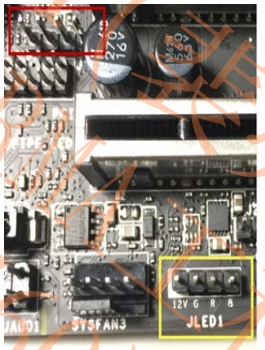






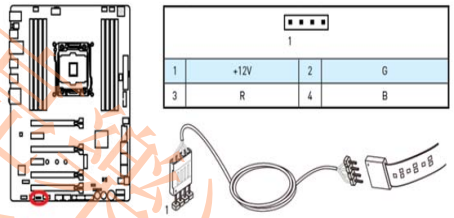


D03-606BA09-N03
D03-606BA09-N03
D03-606BA09-N03



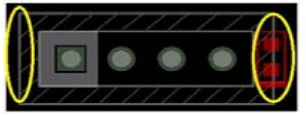
JLED1: RGB LED connector

This connector allows you to connect the RGB LED strip.



Important

- This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.
- Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.
- Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.



JLED1電源暫不提請現在有例

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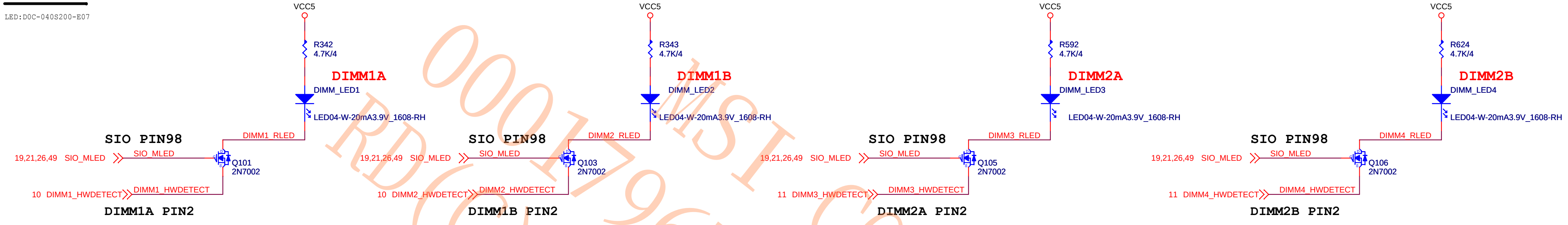
DIMM LED

LED:D0C-040S200-E07

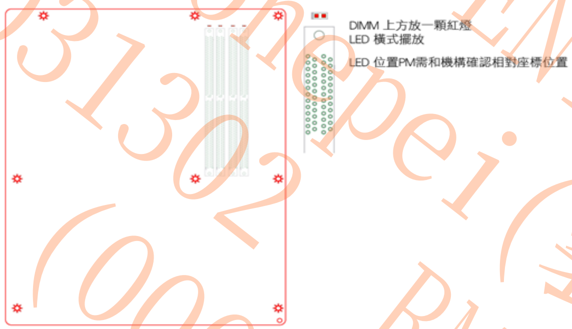


LED
: D0C-040P100-H91
AVL: D0C-040S500-E07

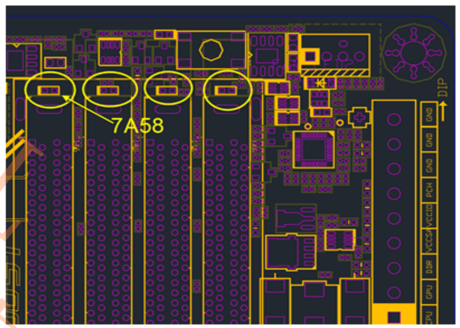
LED
フ : D0C-040T200-H91
AVL: D0C-040S200-E07

需做紅白LED colay 線路，因VF值不一樣，供電的電壓要特別注意

無上鐵蓋作法 - 參考7A16



上鐵蓋做法 - 參考7A58

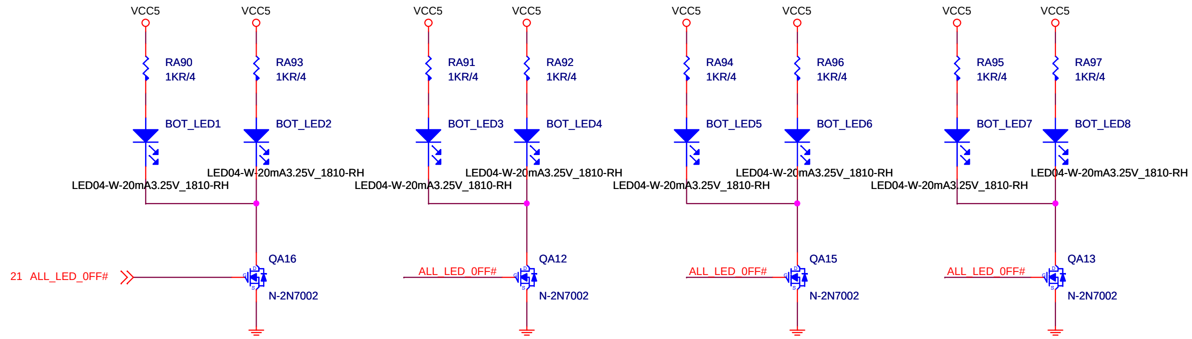


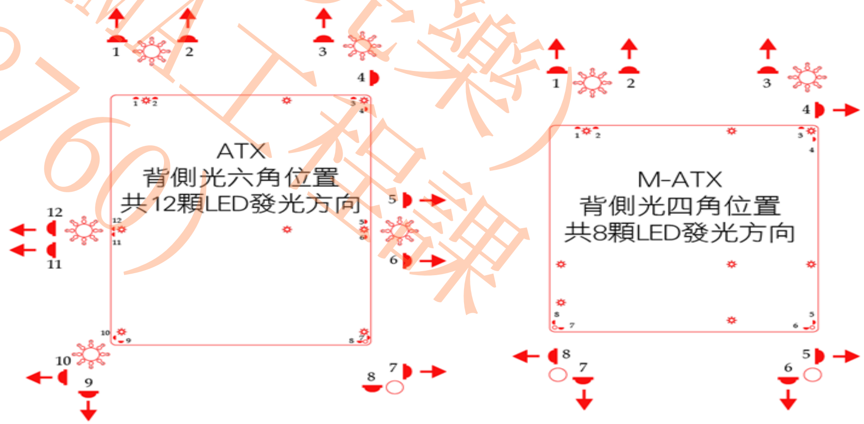
BOTTOM LED

LED:D0C-040S300-E07

LED
フ : D0C-040T300-H91
AVL: D0C-040S300-E07

LED
: D0C-040S600-E07





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MS-7A70		
Size: Custom	Document Description: DIMM LED&BOTTOM LED	Rev: 10
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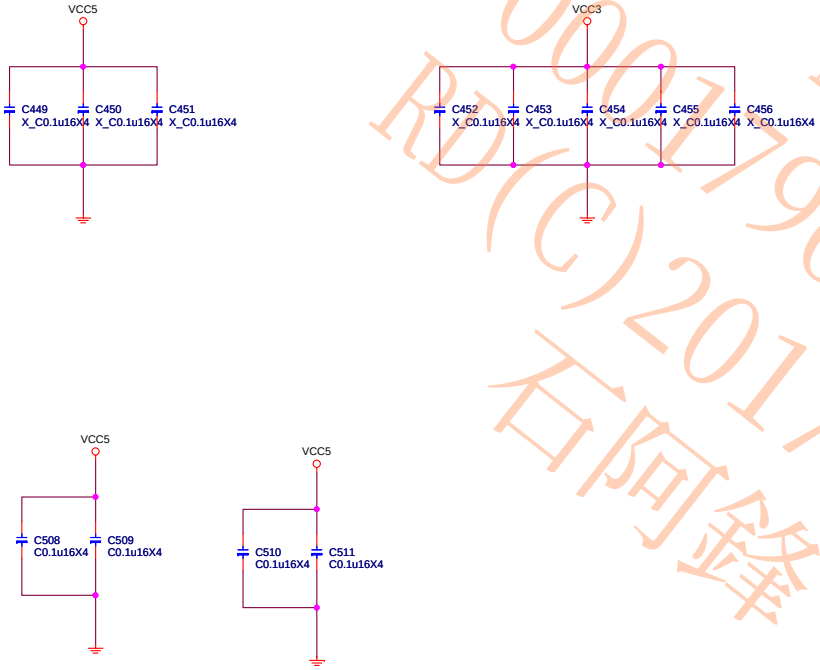
EMI CAP



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A70	
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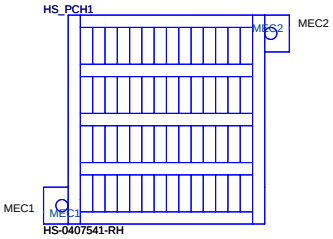
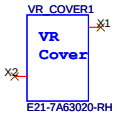
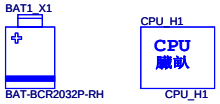
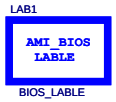


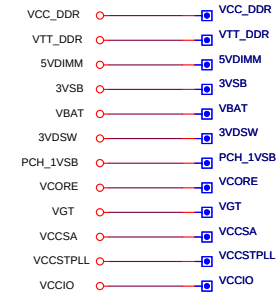




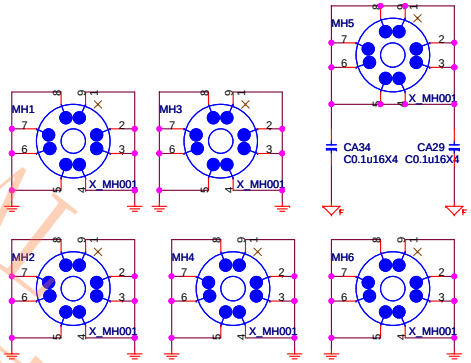


MAIN:PD0-07A7010-G37
AVL:PD0-07A7010-E48

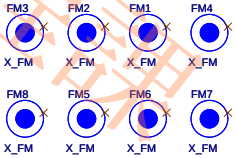
Test points



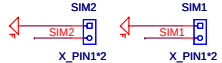
Mounting Holes



Optical Fiducial Marks-120



Simulation



MSI

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