PRAHA (SRI)

CPU : Intel Merom (800MHz)
Chip Set : RS600ME & SB600
Remarks : Mobility Platform

Model Name : PRAHA
PBA Name : MAIN
PCB Code : TPT : BA41-00791A
GCE : BA41-00792A
NAN : BA41-00811A
Dev. Step : MP1.0 (8-Layer)
Revision : 1.0
T.R. Date : 2007.07.02

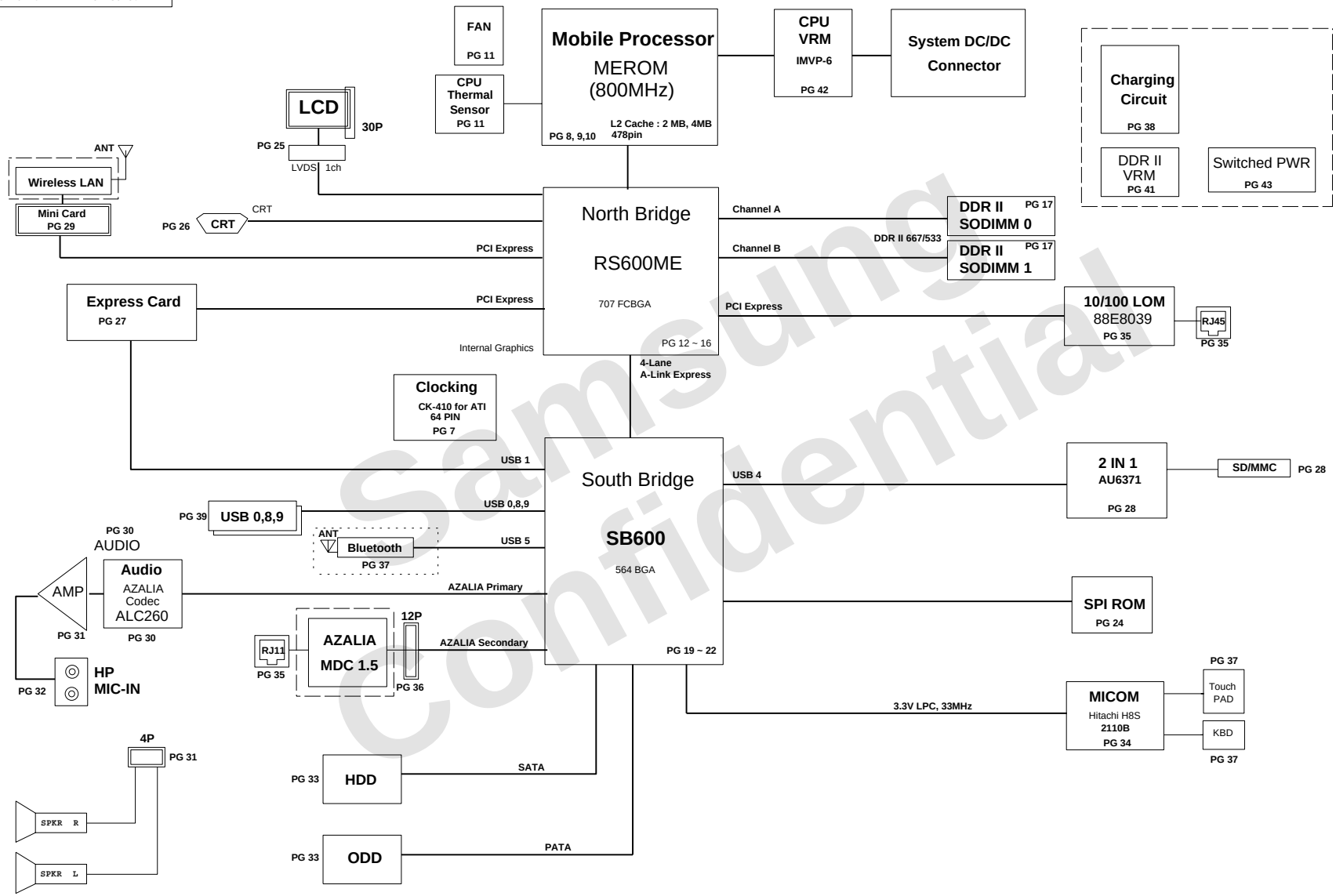
DRAW	CHECK	APPROVAL

■ *Owner : SEC Mobile R & D* *Signature :* *X*

Table of Contents

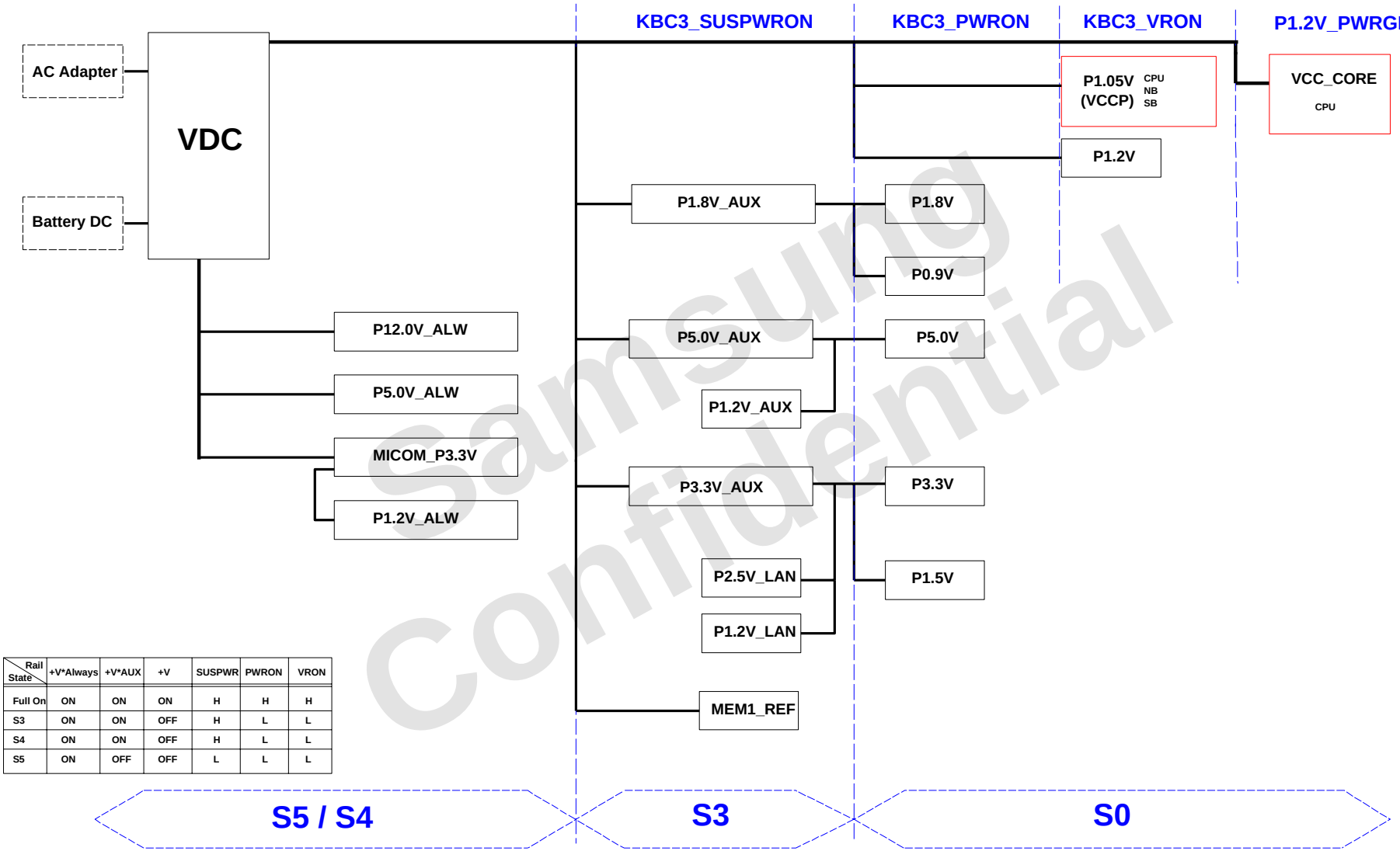
USE ICT PORT

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) COVER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 1 OF 47	



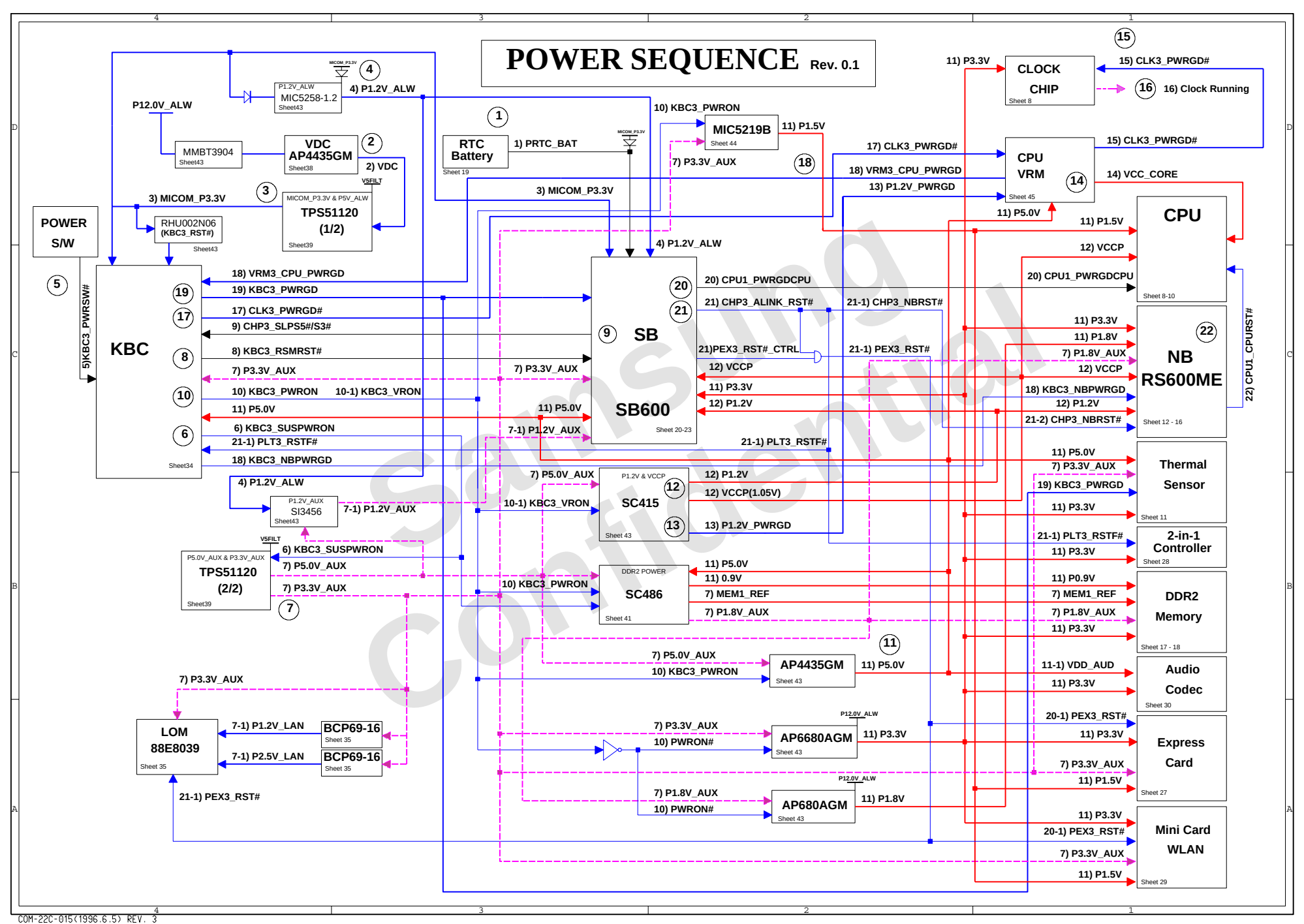
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN OPERATION BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 2 OF 47	

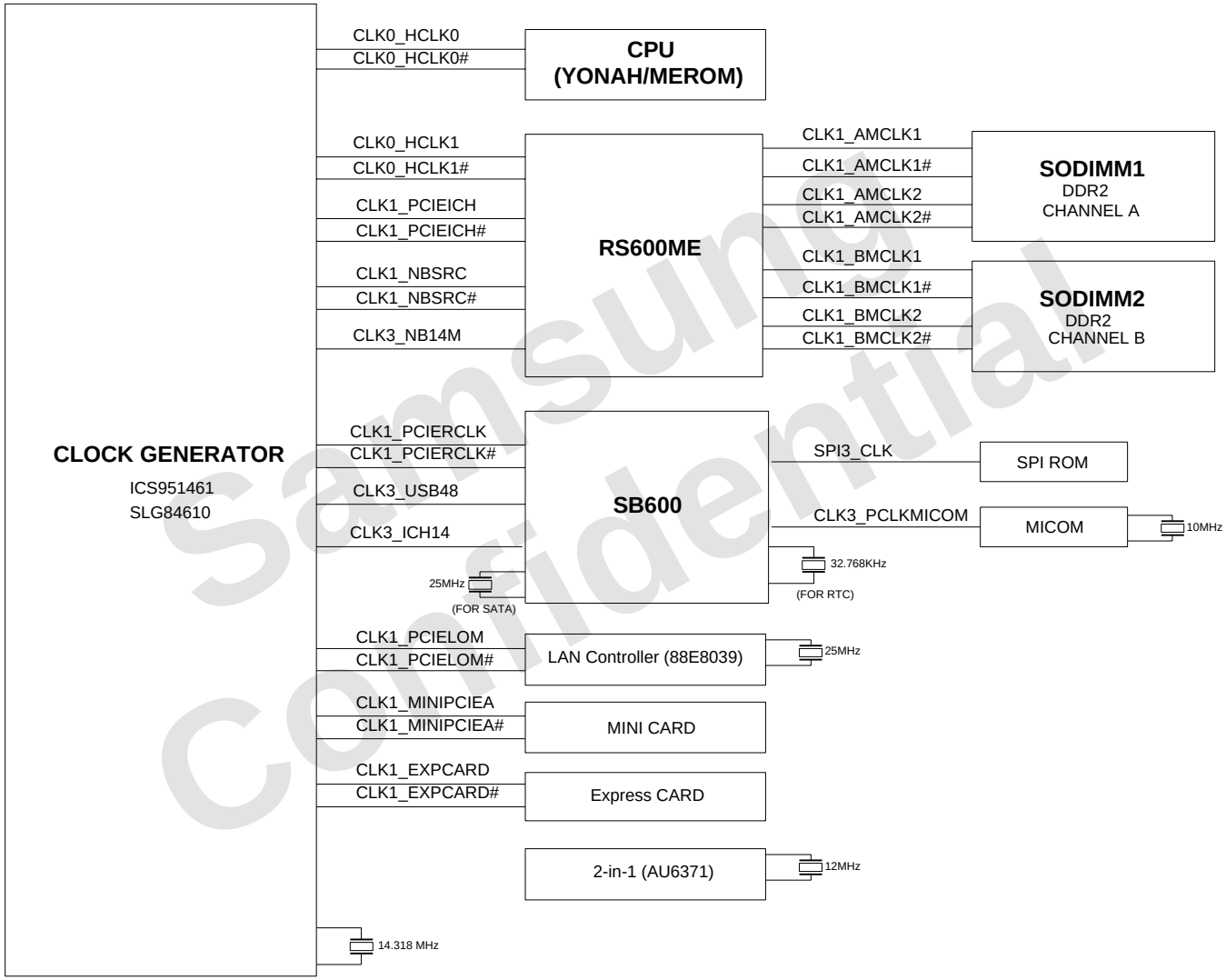
Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 3 OF 47	


POWER SEQUENCE Rev. 0.1
POWER S/W
KBC
Sheet34
SB
SB600
Sheet 20-23
RTC Battery
Sheet 19
MIC5219B
Sheet 44
MIC5258-1.2
Sheet43
MMBT3904
Sheet43
VDC AP4435GM
Sheet38
RHU002N06 (KBC3_RST#)
Sheet43
TPS51120 (1/2)
Sheet39
TPS51120 (2/2)
Sheet39
SI3456
Sheet43
SC415
Sheet 43
SC486
Sheet 41
AP4435GM
Sheet 43
AP6680AGM
Sheet 43
AP6680AGM
Sheet 43
LOM 88E8039
Sheet 35
BCP69-16
Sheet 35
BCP69-16
Sheet 35
CLOCK CHIP
Sheet 8
CPU VRM
Sheet 45
CPU
Sheet 8-10
NB RS600ME
Sheet 12 - 16
Thermal Sensor
Sheet 11
2-in-1 Controller
Sheet 28
DDR2 Memory
Sheet 17 - 18
Audio Codec
Sheet 30
Express Card
Sheet 27
Mini Card WLAN
Sheet 29
P12.0V_ALW
4) P1.2V_ALW
10) KBC3_PWRON
11) P1.5V
1) PRTC_BAT
7) P3.3V_AUX
3) MICOM_P3.3V
2) VDC
5)KBC3_PWRSW#
18) VRM3_CPU_PWRGD
19) KBC3_PWRGD
17) CLK3_PWRGD#
9) CHP3_SLPS5#/S3#
8) KBC3_RSMRST#
10) KBC3_PWRON
10-1) KBC3_VRON
11) P5.0V
6) KBC3_SUSPWRON
21-1) PLT3_RSTF#
18) KBC3_NBPWRGD
7-1) P1.2V_AUX
6) KBC3_SUSPWRON
7) P5.0V_AUX
7) P3.3V_AUX
20) CPU1_PWRGDCPU
21) CHP3_ALINK_RST#
21-1) CHP3_NBRST#
21)PEX3_RST#_CTRL
21-1) PEX3_RST#
12) VCCP
11) P3.3V
12) P1.2V
12) VCCP(1.05V)
13) P1.2V_PWRGD
11) P0.9V
7) MEM1_REF
7) P1.8V_AUX
11) P1.8V
10) PWRON#
7-1) P1.2V_LAN
7-1) P2.5V_LAN
21-1) PEX3_RST#
17) CLK3_PWRGD#
18) VRM3_CPU_PWRGD
13) P1.2V_PWRGD
14) VCC_CORE
15) CLK3_PWRGD#
16) Clock Running
22) CPU1_CPURST#
19) KBC3_PWRGD
11-1) VDD_AUD
20-1) PEX3_RST#
Samsung Confidential
COM-22C-015(1996.6.5) REV. 3



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 5 OF 47	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB	AD30(internal)		
Hub to PCI	AD31(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD31(internal)		
AC Link	-		

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	H8S-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM
Crystal	12MHz	2-in-1	2-in-1 (SD/MMC)

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (0~1.5V)
VCCP	YONAH Processor System Bus(PSB) Termination (1.05V)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P1.8V_ALWS	1.8V power rail (Always On)
P2.5V_LAN	2.5V power rail (off in S4-S5)
MICOM_P3.3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P5.0V_ALWS	5.0V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 **1** **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

I²C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
SODIMM0	1010 0100	A4h	-
SODIMM1	1010 0110	A6h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	Left side USB Port
1	USB Express Card
4	2-in-1 Memory Card
5	Bluetooth
8, 9	Rear side USB Port

System Power States

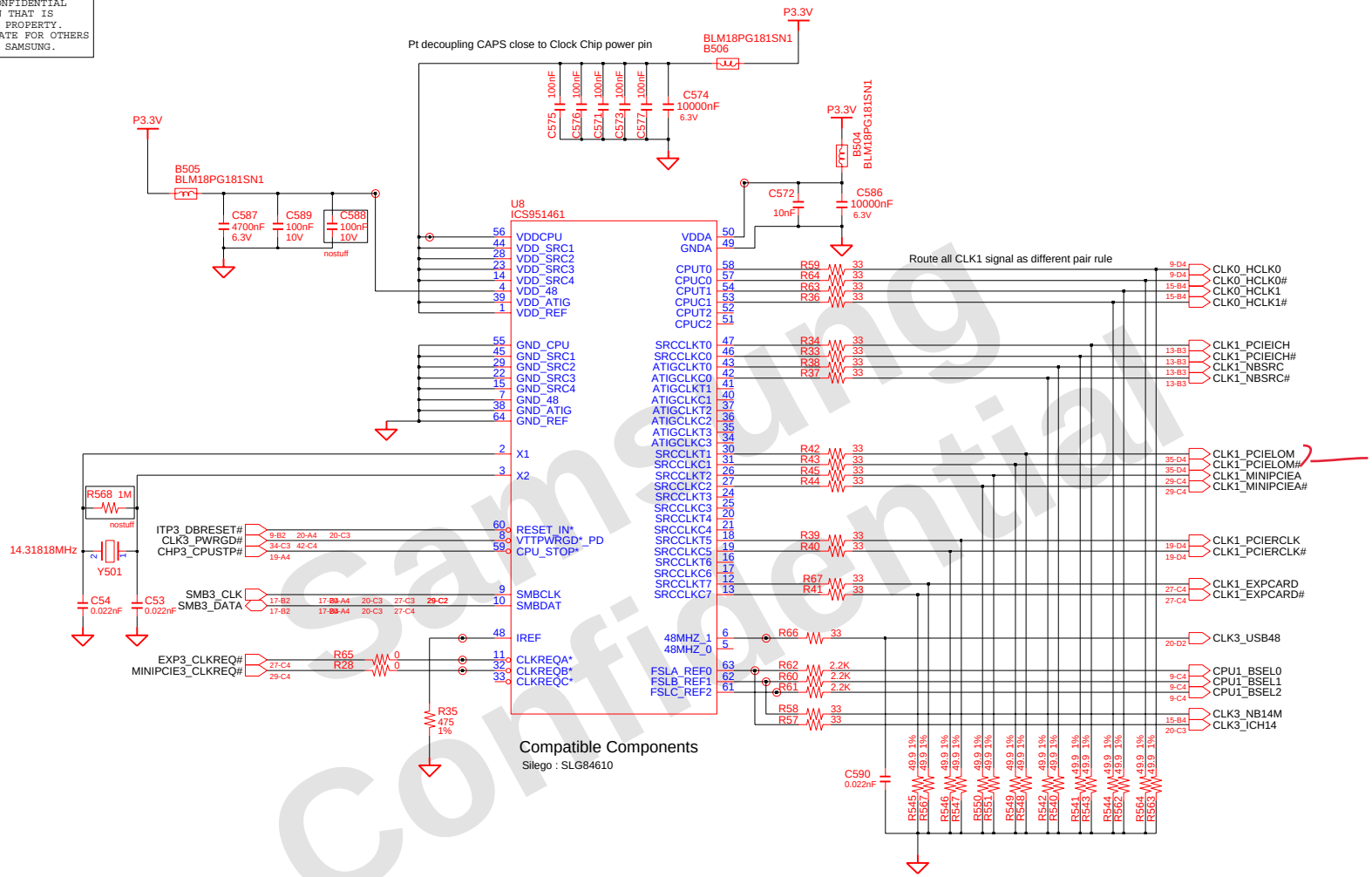
CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00791A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 6 OF 47	



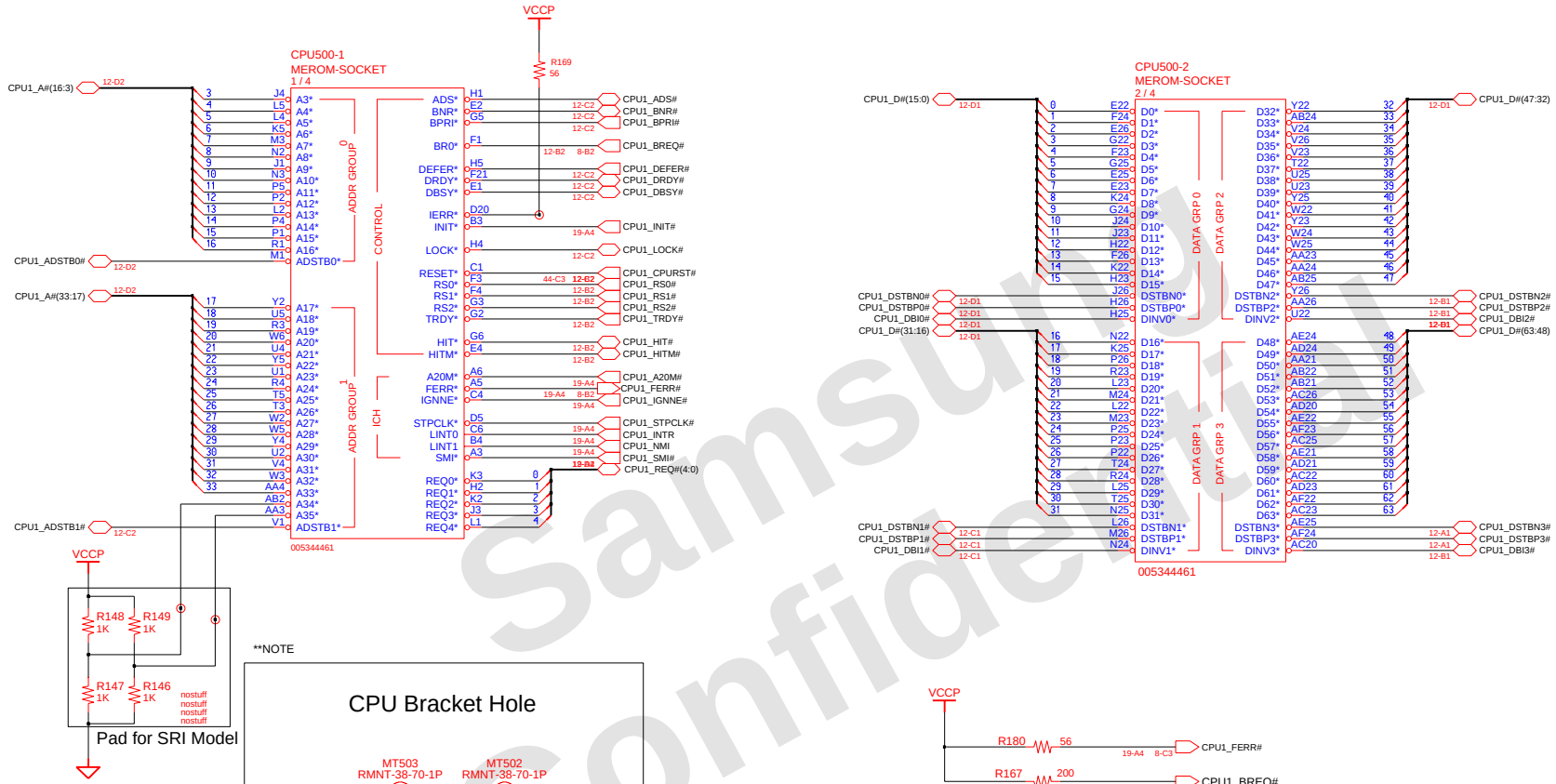
Place all te serias termination resistor as close as Clock Chip as possible

FSA, FSB, FSC of Clock chip are low thershold inputs
Vih_fs_min = 0.7V
Vil_fs_max - 0.35V

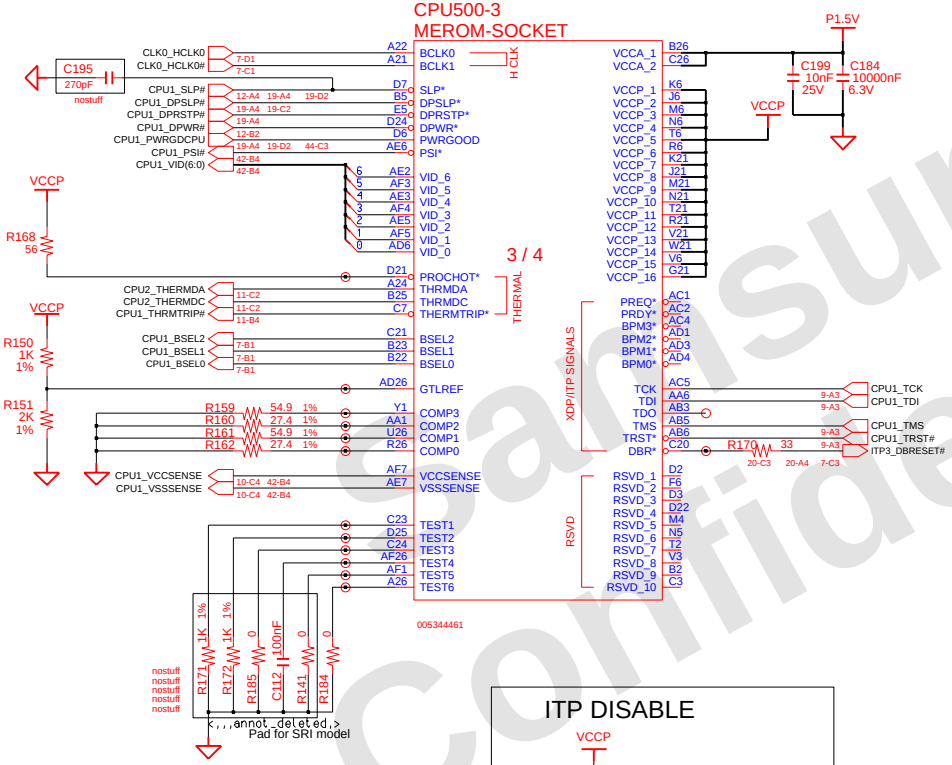
CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK	
	0	0	0	266 MHz	
	0	0	1	333 MHz	
	0	1	0	200 MHz	Merom 800MHz
	0	1	1	400 MHz	
	1	0	0	133 MHz	Celeron 533MHz
	1	0	1	100 MHz	
	1	1	0	166 MHz	Merom 667MHz
	1	1	1	RSVD	

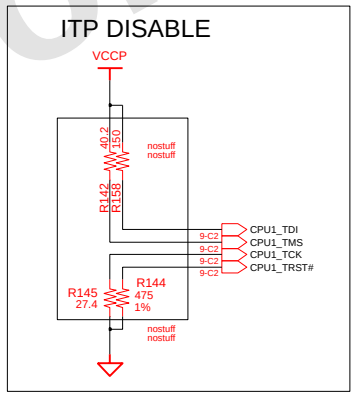
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00791A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 7 OF 47	

d:/users/mobile62/mentor/Praha/Santa/Praha_SRI_MP10_order_070625



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN MEROM CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00791A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 8 OF 47	





GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 **1** **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp

DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

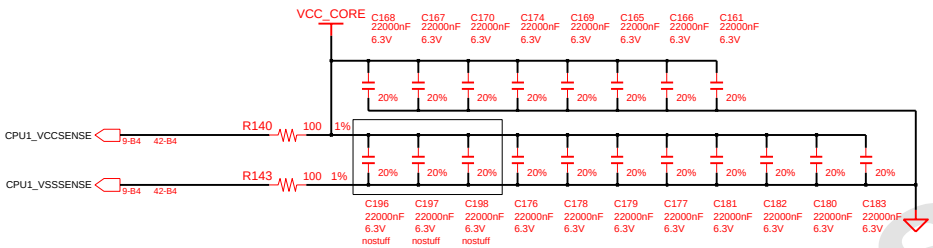
DRAW	TERMI	DATE	7/2/2007
CHECK	HJ KIM	DEV. STEP	MP
APPROVAL	SJ PARK	REV	1.0
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM

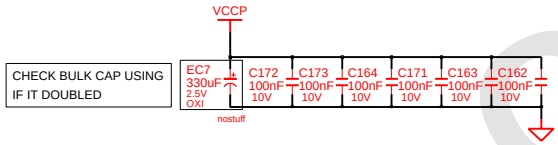
TITLE: PRAHA (SRI) MAIN MEROM CPU(2/3)

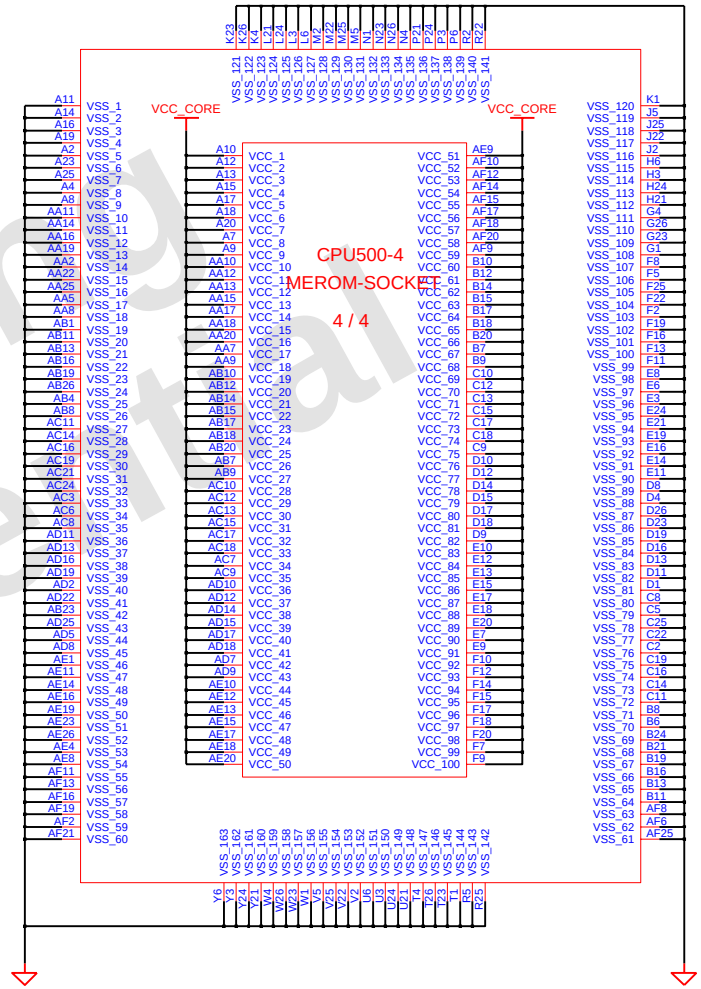
SAMSUNG ELECTRONICS

PART NO. BA41-00791A

Deleted 13 De-cap (Only use 19pcs out of 32)





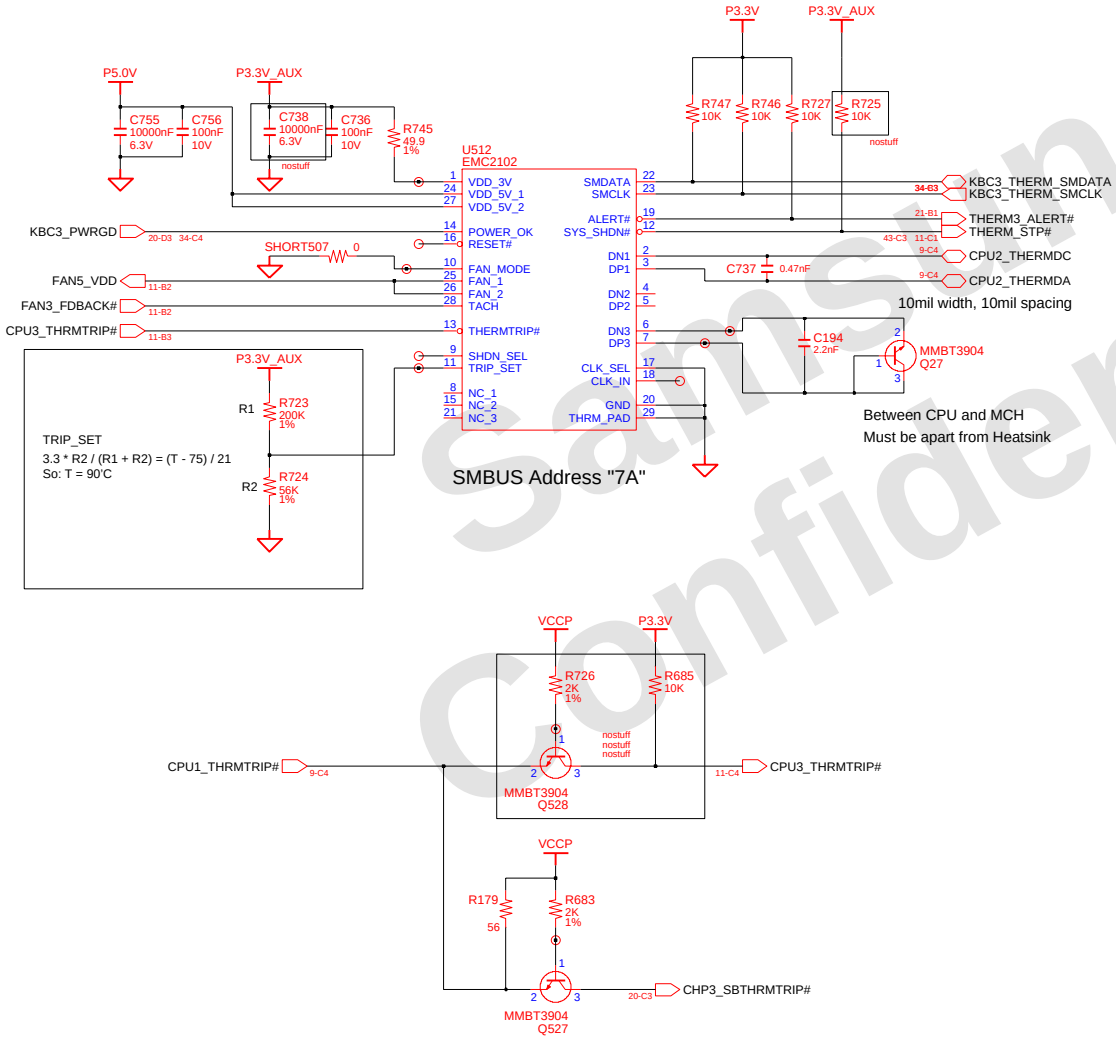


DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN MEROM CPU(3/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 10 OF 47	

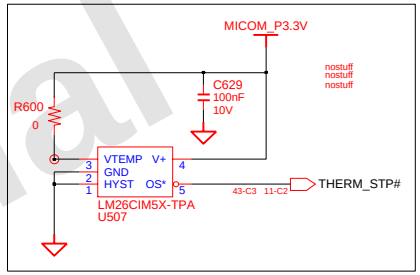
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

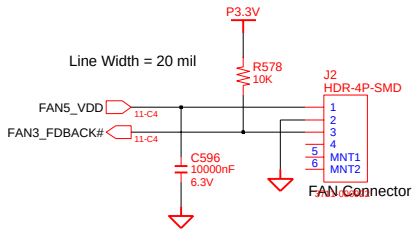
Thermal Monitor



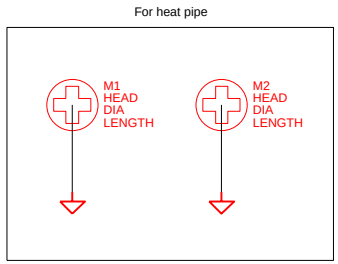
OTP (NOSTUFF)



FAN Control



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN THERMAL SENSOR/FAN CNTRL	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 11 OF 47	



U506-1
RS600ME
1 OF 5

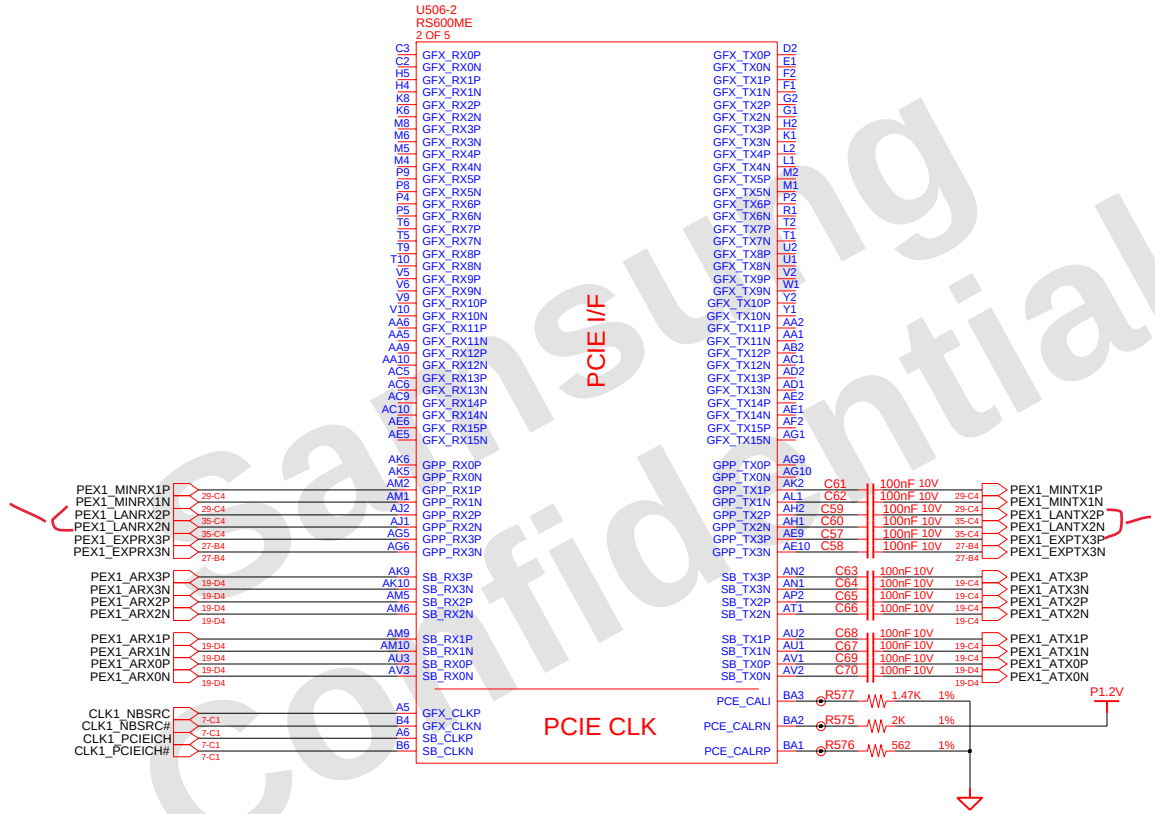
P-4 AGTL + I/F

CPU1_A#(33:3)
CPU1_REQ#(4:0)
CPU1_ADSTB0#
CPU1_ADSTB1#
CPU1_ADS#
CPU1_BNR#
CPU1_BPRI#
CPU1_DEFER#
CPU1_DRDY#
CPU1_DBSY#
CPU1_LOCK#
CPU1_CPURST#
CPU1_RS2#
CPU1_RS1#
CPU1_RS0#
CPU1_BREQ#
CPU1_TRDY#
CPU1_HIT#
CPU1_HITM#
CPU1_DPWR#
CHP3_SUSSTAT#
KBC3_NBPWRGD
CHP3_NBRST#
CPU_COMP_P
CPU_COMP_N
THERMALDIODE_P
THERMALDIODE_N
IOPLLVDD18
IOPLLVDD12
IOPLLVSS
CPUSLP#_RESERVED1
CPU_VREF
TESTMODE
CPU_RESERVED
CPUA32#_NC
CPUA33#_NC
ADDR.GROUP 0
ADDR.GROUP 1
CONTROL
MISC

CPU1_D#(63:0)
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
CPU1_DBI0#
CPU1_DSTBN0#
CPU1_DSTBP0#
CPU1_DBI1#
CPU1_DSTBN1#
CPU1_DSTBP1#
CPU1_DBI2#
CPU1_DSTBN2#
CPU1_DSTBP2#
CPU1_DBI3#
CPU1_DSTBN3#
CPU1_DSTBP3#

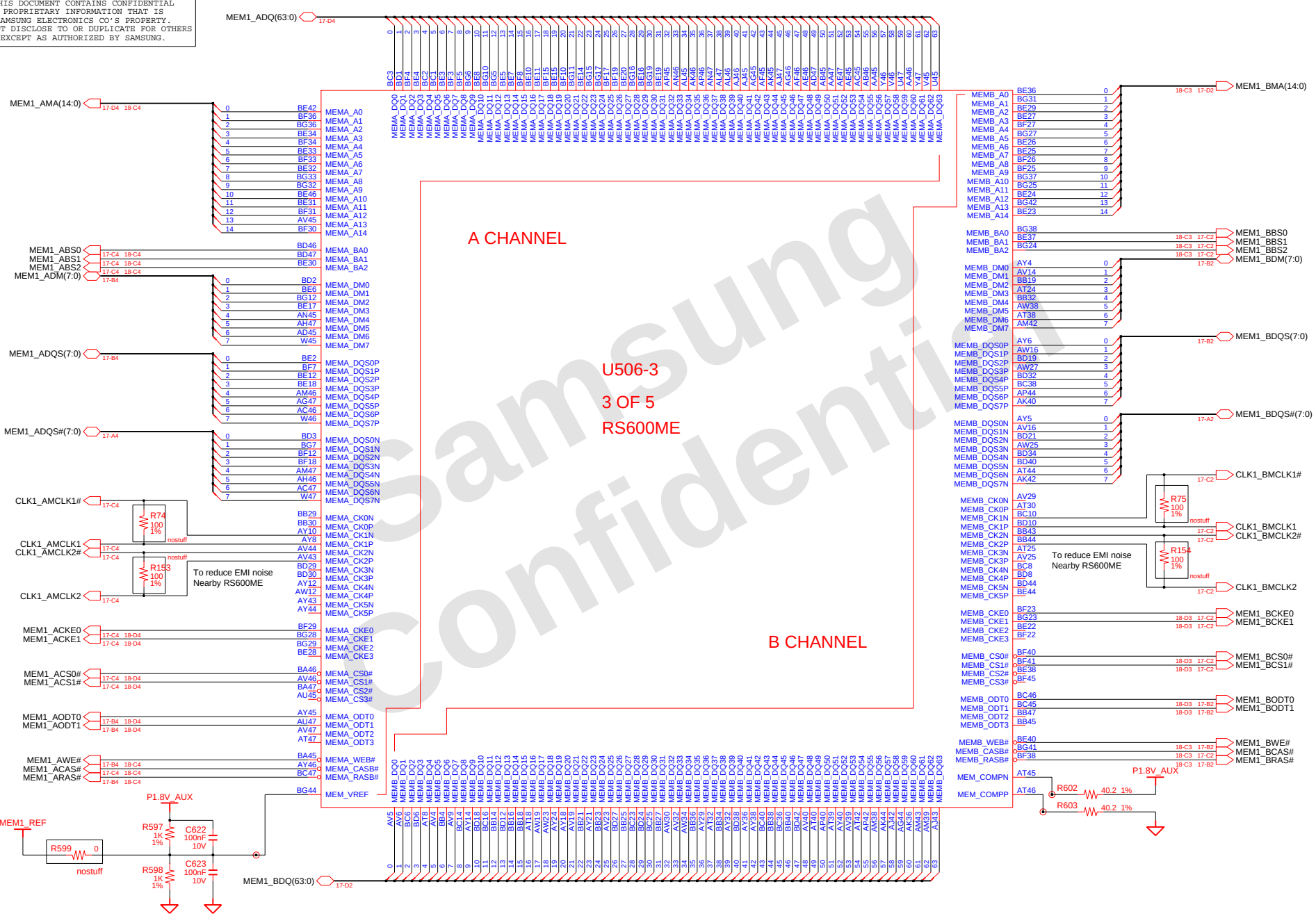
P1.8V_AUX
R73 4.7K nostuff
R72 0 nostuff
R71 1K 1% nostuff
R588 49.9 1%
R108 24.9 1%
VCCP
P1.8V
P1.2V
SHORT8
Q15
RHU002N06
B22 BLM18PG181SN1
B23 BLM18PG181SN1
C119 2200nF 10V
C122 2200nF 10V
P3.3V_NB
R76 4.7K
R82 20K 1%
Q17 MMBT3904
Q16 MMBT3904
R77 2.2K
CPU1_SLP#
R110 61.9 1%
R109 127 1%
C607 1000nF 6.3V
C606 270pF
R86 4.7K
PLACE CLOSE TO NB
USE 10/10MIL WIDTH/SPACE

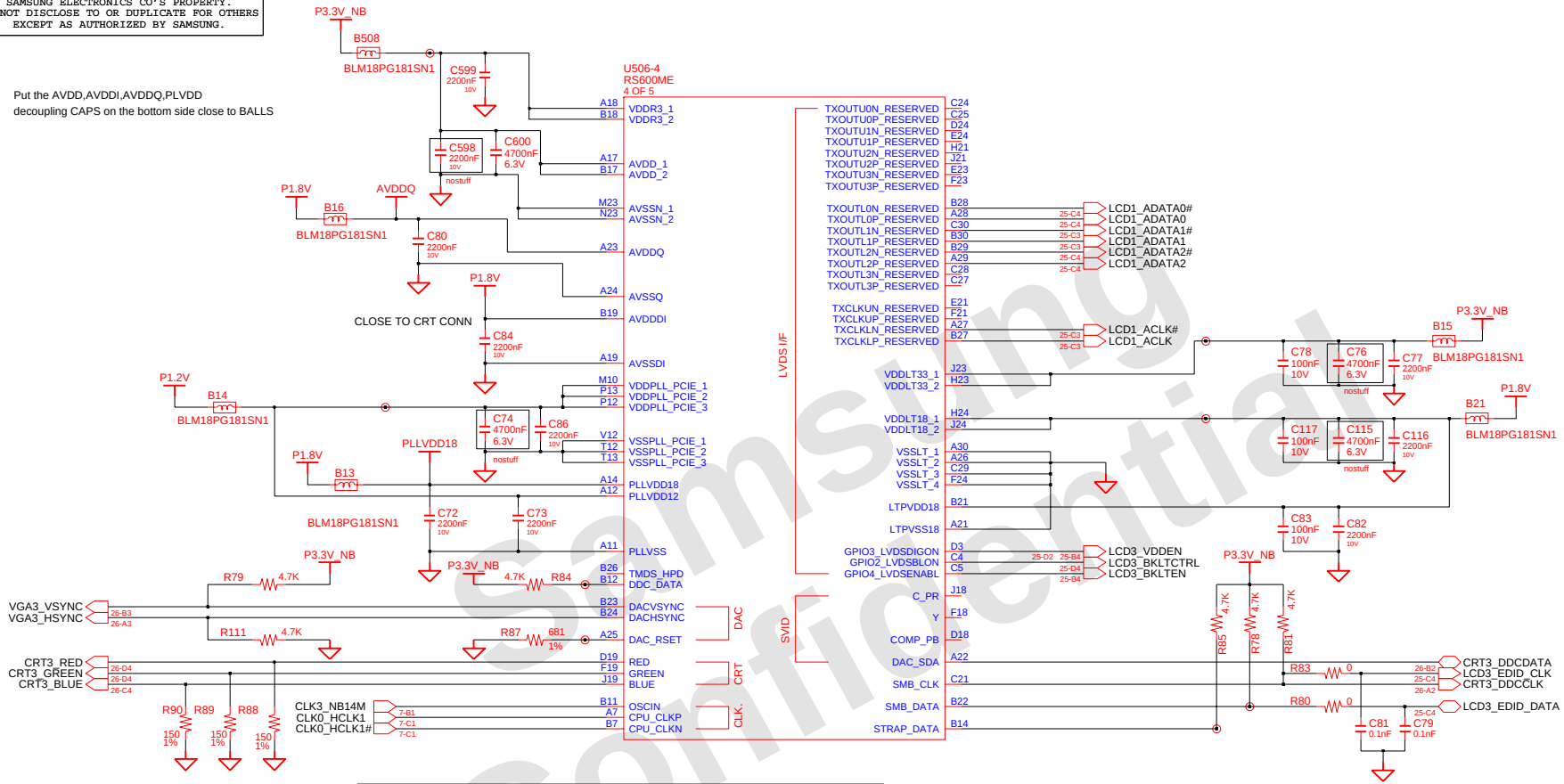
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN RS600ME(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 12 OF 47	

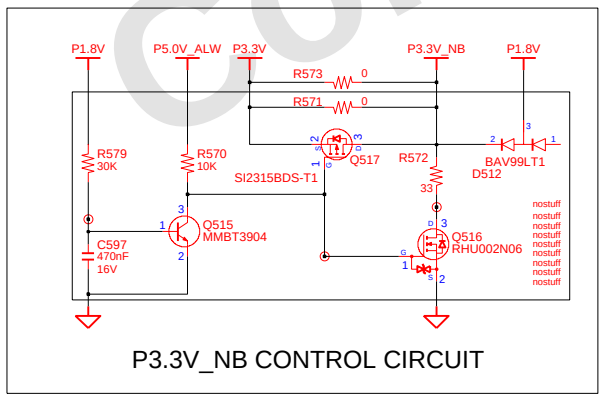


PEX1_MIN	Mini Card I/F
PEX1_LAN	LOM I/F
PEX1_EXP	Express Card I/F

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN RS600ME(2/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 13 OF 47	





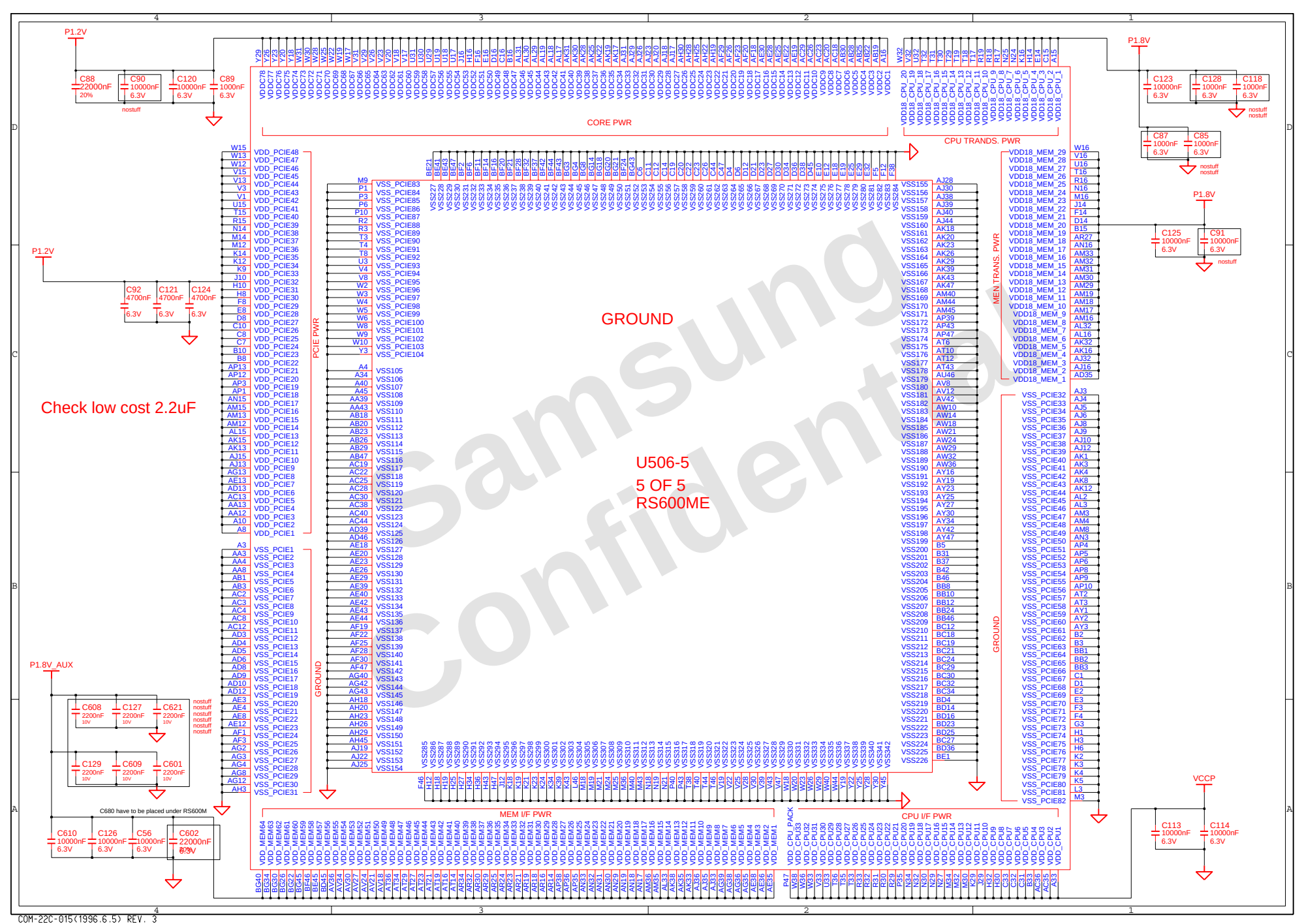


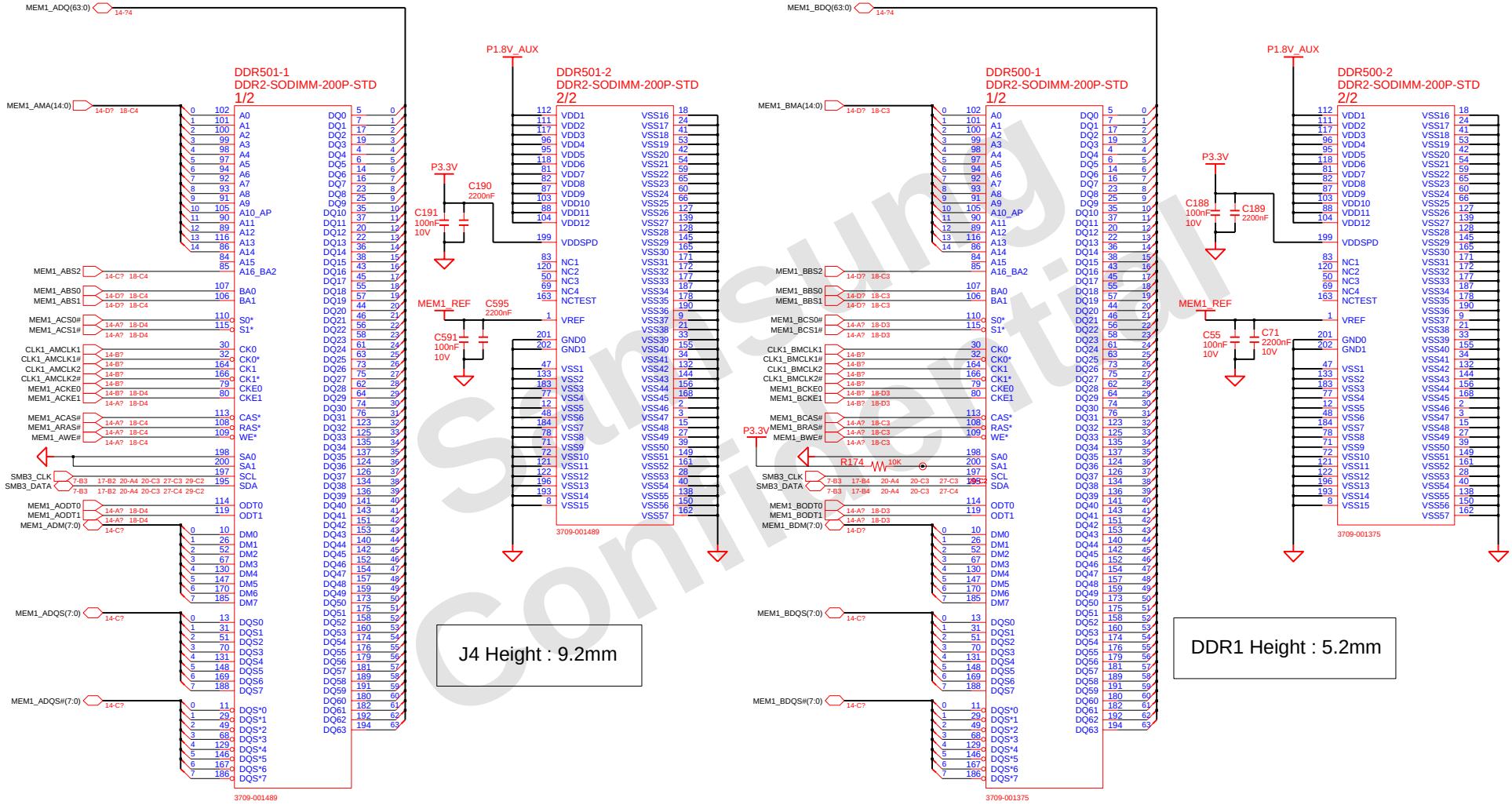
P3.3V_NB CONTROL CIRCUIT

STRAP DEFINITIONS FOR THE RS600M

STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS600M
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN RS600ME(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 15 OF 47	

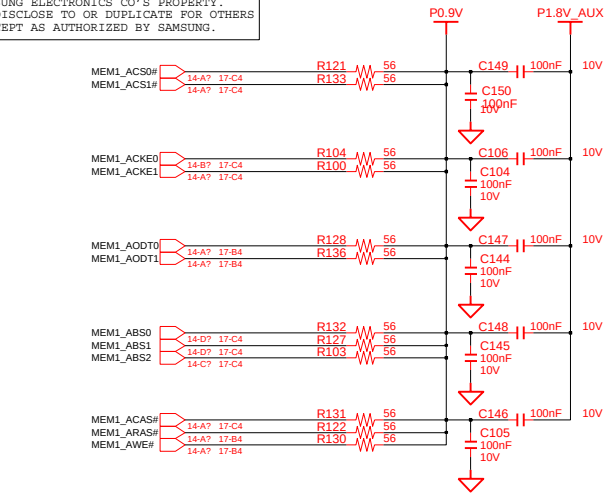

GROUND
U506-5
5 OF 5
RS600ME
CORE PWR
CPU TRANDS. PWR
MEM TRANS. PWR
PCIE PWR
GROUND
MEM I/F PWR
CPU I/F PWR
Check low cost 2.2uF
P1.2V
P1.8V
P1.8V_AUX
VCCP
Samsung Confidential

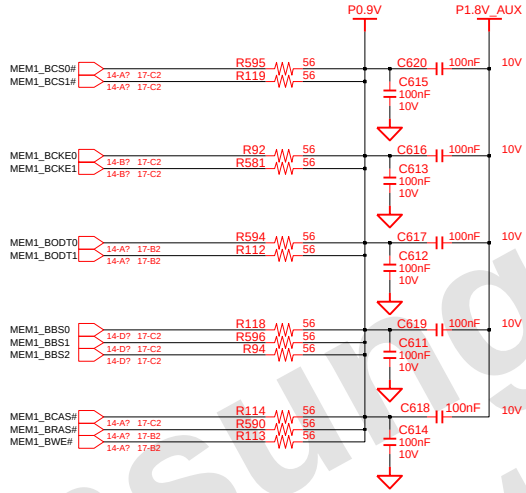


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN DDR2 - SODIMM
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	17 OF 47

SAMSUNG ELECTRONICS

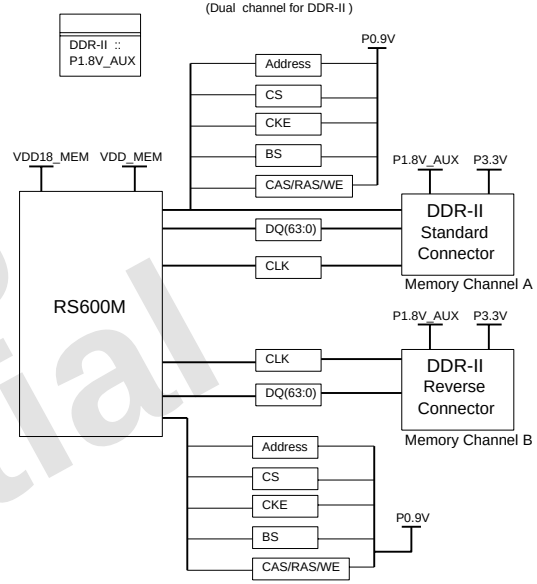
PART NO. BA41-00791A

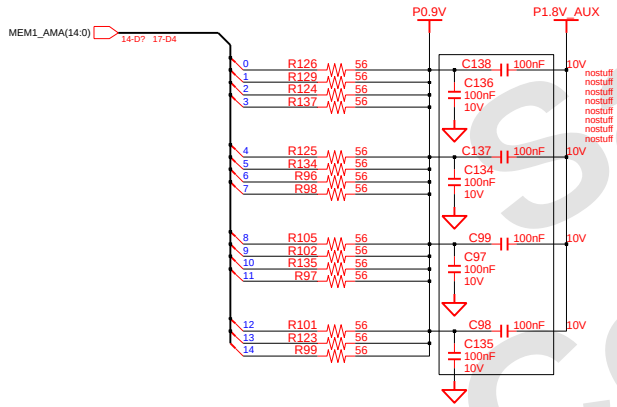


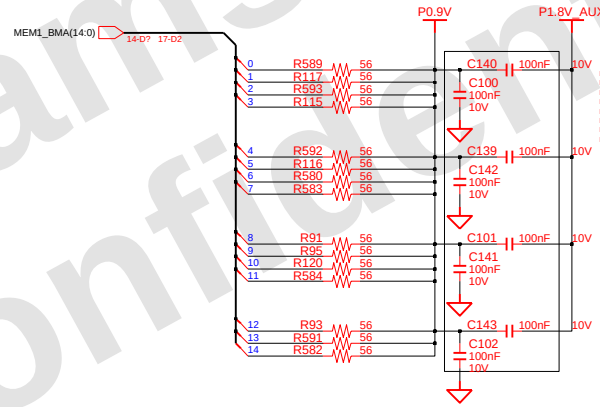


Memory Topology

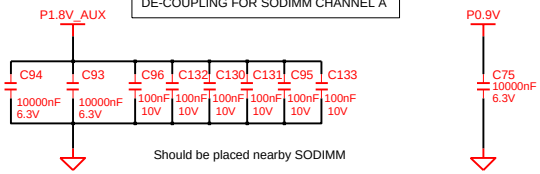
(Dual channel for DDR-II)





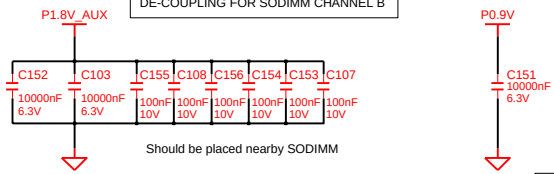


DE-COUPLING FOR SODIMM CHANNEL A



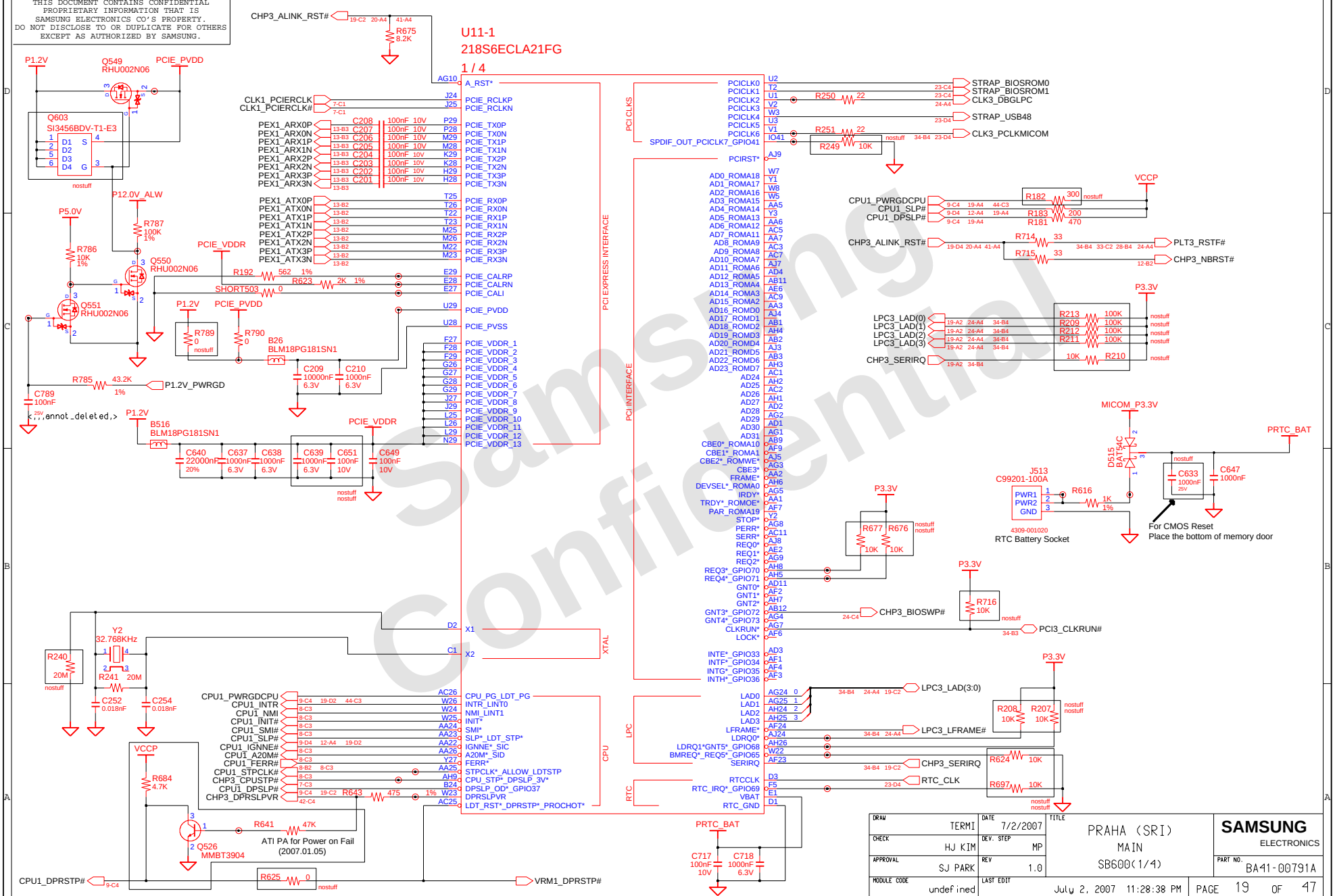
Should be placed nearby SODIMM

DE-COUPLING FOR SODIMM CHANNEL B



Should be placed nearby SODIMM

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN DDR2 - TERMINATION	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 18 OF 47	



USB Port 0 : Left side USB Port
USB Port 1 : Express Card
USB Port 4 : 2-in-1 Memory Card
USB Port 5 : Bluetooth I/F
USB Port 8, 9 : Rear side USB Port

U11-2
218S6ECLA21FG
2 / 4

GPIO7(#A23)
Pull Up : Santa Rosa
Pull Down : NAPA Refresh

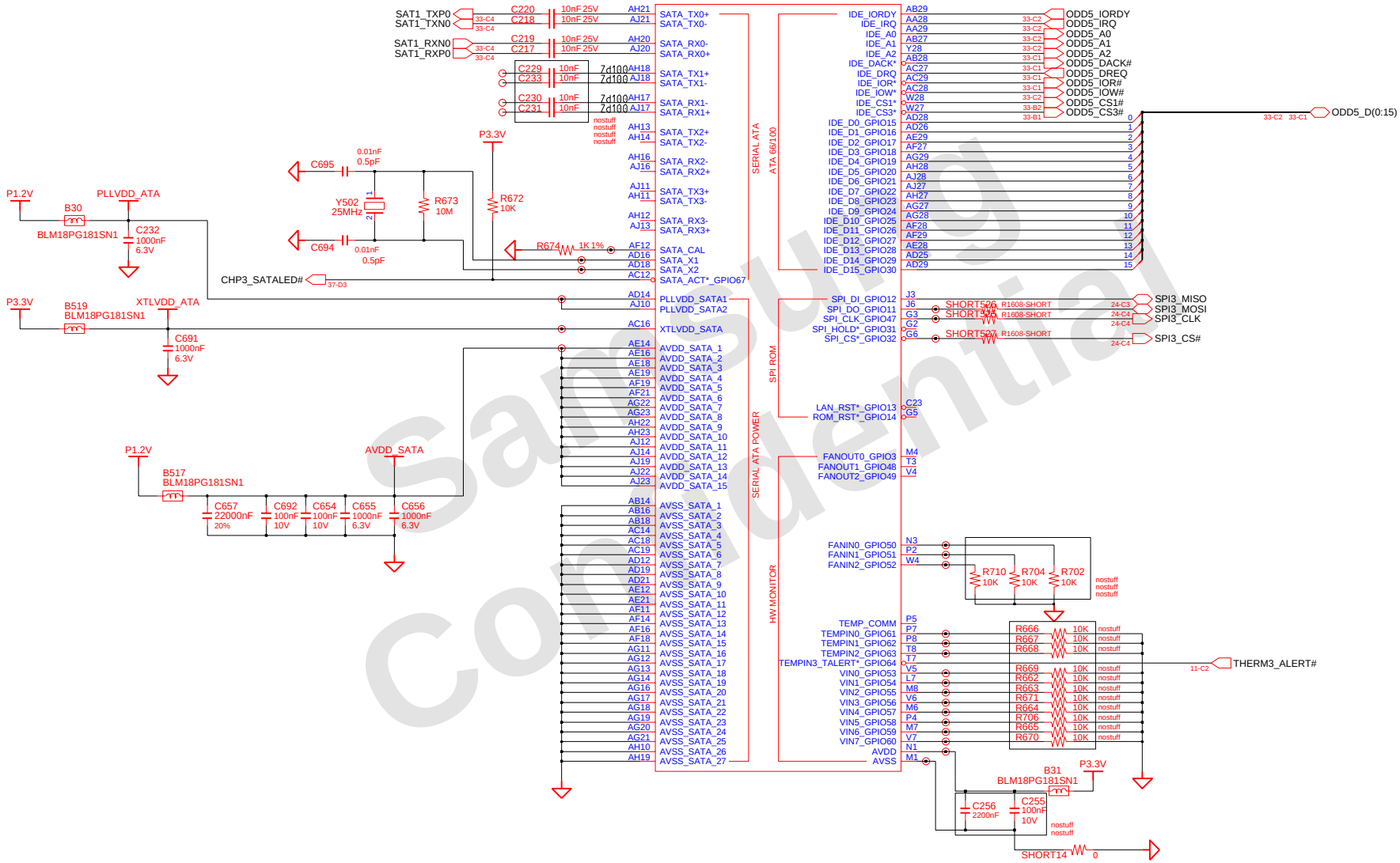
Add Choke coil to reduce EMI noise (2007.04.16)

Place on the upper side

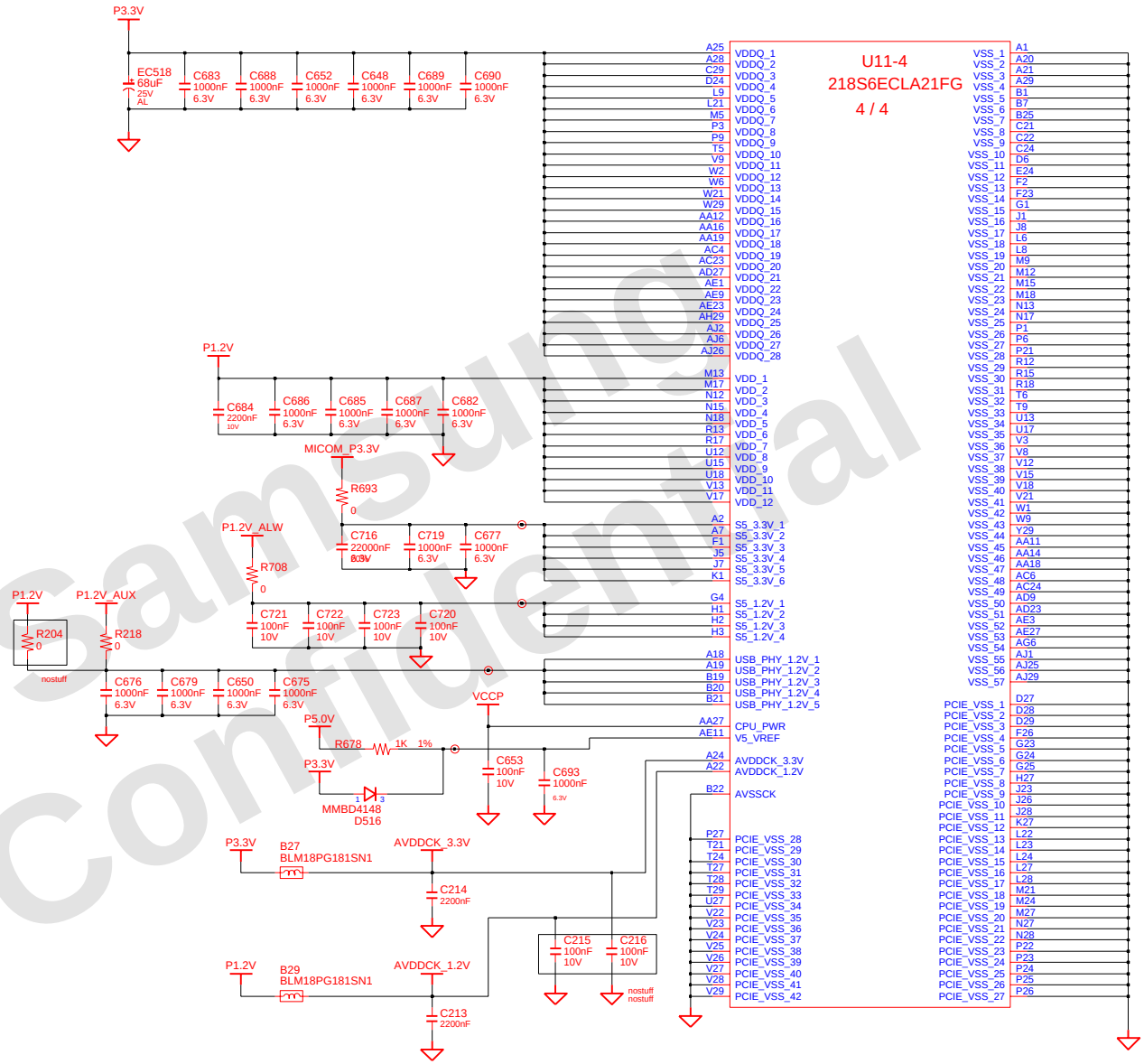
DRAW	TERMI	DATE 7/2/2007	TITLE PRAHA (SRI) POWER SB600(2/4)
CHECK	HJ KIM	DEV. STEP MP	SAMSUNG ELECTRONICS
APPROVAL	SJ PARK	REV 1.0	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT July 2, 2007 11:28:38 PM	PAGE 20 OF 47

d:/users/mobile62/mentor/Praha/Santa/Praha_SRI_MP10_order_070625

U11-3
218S6ECLA21FG
3 / 4



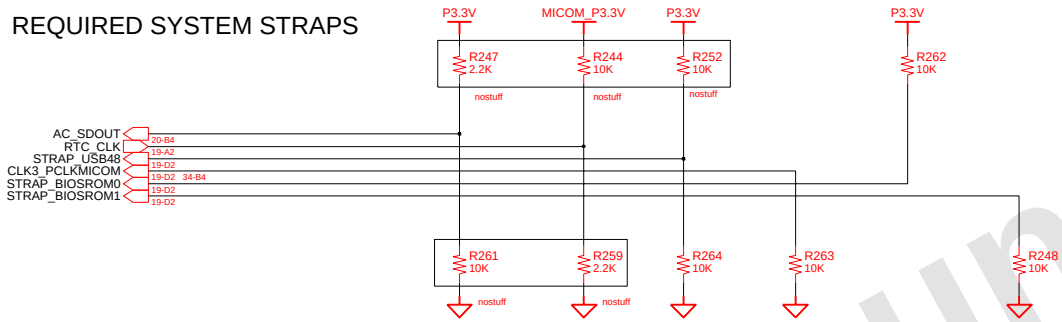
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN SB600(3/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 21 OF 47	



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN SB600(4/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 22 OF 47	

SB600 HAS AN INTERNAL PD FOR AC_SDOUT
SB600 HAS AN INTERNAL PU FOR RTC_CLK

REQUIRED SYSTEM STRAPS

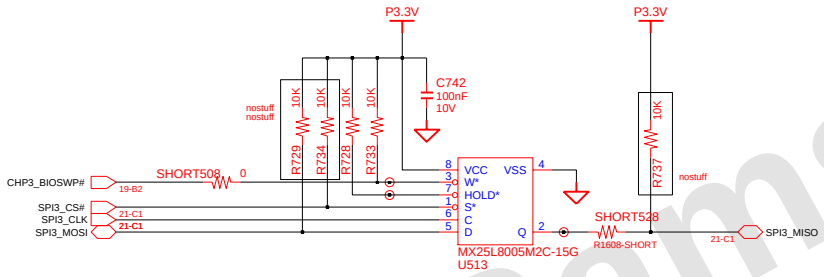


	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0 PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	

DEBUG STRAPS

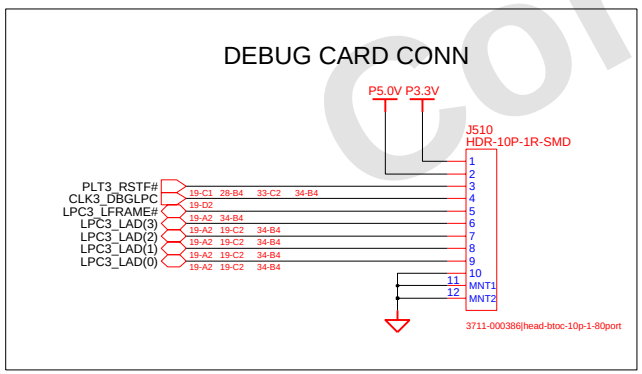
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	STRAPS	PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 23 OF 47	



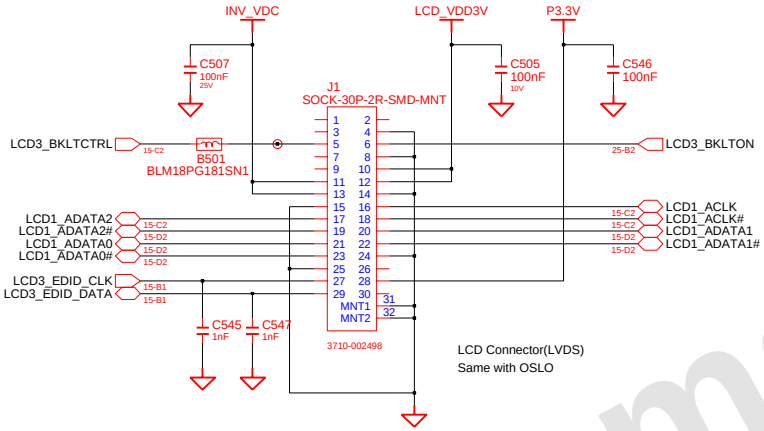
SPI3_CS#

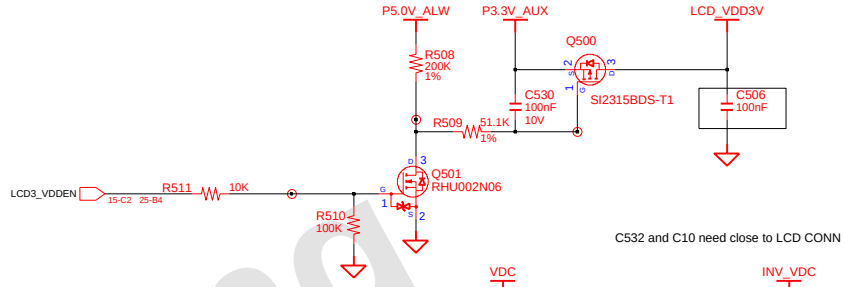
SB600 prior to A21 : Pulled up to P3.3V_ALW with 1Kohm resistor.
SB600 A21 and newer : No external pull-up resistor required.

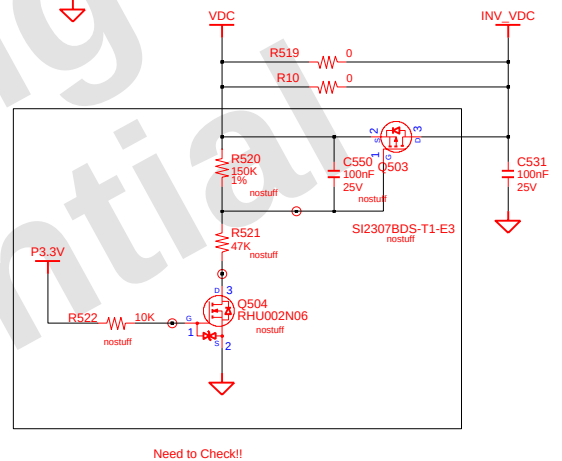


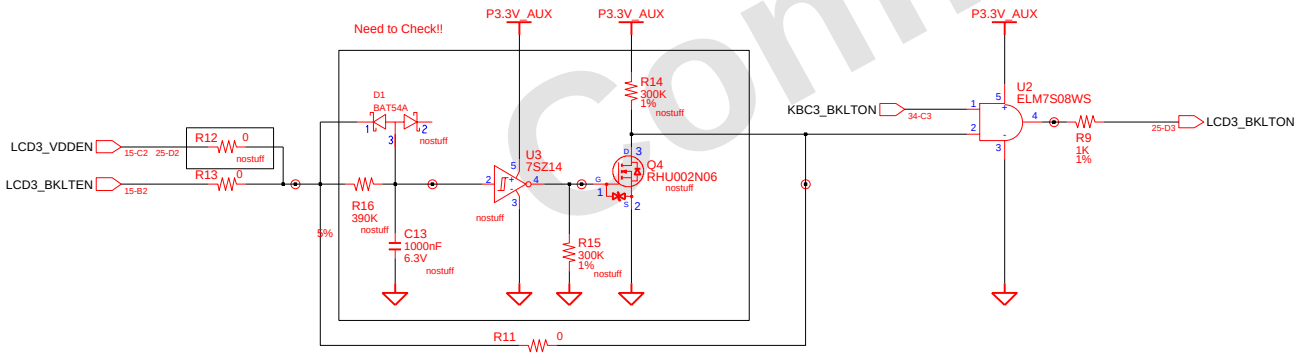
02	VERIFY REAL MODE
03	DISABLE NMI
04	GET CPU TYPE
06	INIT. SYSTEM H/W
08	INIT. CHIPSET REG.
09	SET IN POST FLAG
0A	INIT CPU.REG
0B	CPU CACHE ON
0C	INIT.CACHE TO POST
OE	INIT. I/O VALUE
0F	ENABLE THE L-BUS IDE
10	INIT. POWER MANAGER
11	LOAD ALTERNATE REG.
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE
14	INIT. KEYBOARD CONTROLLER
16	CHECK CHECKSUM
18	8254 TIMER INIT.
1A	8237 DMA CONTROLLER INIT.
1C	RESET INTERRUP CONTROLLER
20	TEST DRAM REFRESH
22	TEST 8742 KEYBOARD CONTROLLER
24	SET ES SEGMENT REG. TO 4GB
26	ENABLE A20
28	AUTO SIZING DRAM
32	COMPUTE THE CPU SPEED
34	TESET CMOS RAM
38	SHADOW SYSTEM BIOS ROM
3A	AUTO SIZING CACHE
3C	CONFIGURE ADVANCED CHIPSET REG.
3D	LOAD ALTER REG. WITH CMOS VALUE
42	INIT. INTERRUPT VECTOR
44	INIT. BIOS INTERRUPT
46	CHECK ROM COPYRIGHT NOTICE
47	INIT. I20 SUPPORT IF INSTALLED
48	CHECK VIDEO CONFIGURE AGAINST CMOS
49	INIT. PCI BUS AND DEVICE
4A	INIT. ALL VIDEO BIOS ROM
4C	SHADOW VIDEO BIOS ROM
50	DISPLAY CPU TYPE AND SPEED
52	TEST KEYBOARD
54	SET KEYCLICK IF ENABLED
56	ENABLE KEYBOARD
58	TEST FOR UNEXPECTED INTERRUPTS
5A	DISPLAY " PRESS ..... SETUP"
5C	TEST RAM GETWEEN 512K AND 640K
60	TEST EXTENDED MEMORY
62	TEST EXTENDED MEMORY ADDRESS LINE
64	JUMP TO USER PATCH 1
66	CONFIGURE ADVANCE CACHE REG.
6A	DISPLAY EXTERNAL CACHE SIZE
6C	DISPLAY SHADOW MESSAGE
6E	DISPLAY NON-DISPOSABLE SEGMENT
70	DISPLAY ERROR MESSAGE
72	CHECK FOR CONFIGURATION ERROR
74	TEST REAL-TIME CLOCK
76	CHECK FOR KEYBOARD EERROR
7C	SETUP HARDWARE INTERRUPT VECTOR
7E	TEST COPROCESSER IF PRESENT
80	DISABLE ON-BOARD I/O PORT
82	DETECT AND INSTALL EXT.RS232C
84	DETECT AND INSTALL EXT.PARALLEL
86	RE-INIT. ON-BOARD I/O PORT
88	INIT. BIOS DATA ROM
8A	INIT.EXTENDED BIOS DATA AREA
8C	INIT. FDD CONTROLLER
9A	SHADOW OPTION ROMS
9C	SETUP POWER MANAGEMENT
9E	ENABLE H/W INTERRUPT
A0	SET TIME OF DAY
A4	INIT. TYPEMATIC RATE
A8	ERASE F2 PROMPT
AA	SCAN FOR F2 KEY STROKE
AC	ENTER SETUP
AE	CLEAR IN POST FLAG
B0	CHECK FOR ERRORS
B2	POST DONE-PREPARE TO BOOT O/S
B4	ONE BEEP
B6	CHECK PASSWORD (OPTION)
B7	ACPI INIT
BA	DMI INIT
BE	CLEAR SCREEN
C0	TRY BOOT WITH INT19
D0	INTERRUPT HANDLER ERROR
D2	UNKNOWN INTERRUPT ERROR
D4	PENDING INTERRUPT ERROR
D6	SHUTDOWN 5
D8	SHUTDOWN ERROR
DA	EXTENDED BLOCK MOVE
DC	SHUTDOWN 10
89	ENABLE NMI
90	INIT. HDD CONTROLLER
91	INIT. LOCAL BUS HDD CONTROLLER
92	JUMP TO USER PATCH 2
94	DISABLE A20 ADDRESS LINE
96	CLEAR HUGE ES SEGMENT REG.
98	SEARCH FOR OPTION ROMS

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN SPI ROM & DEBUG PORT	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 24 OF 47	

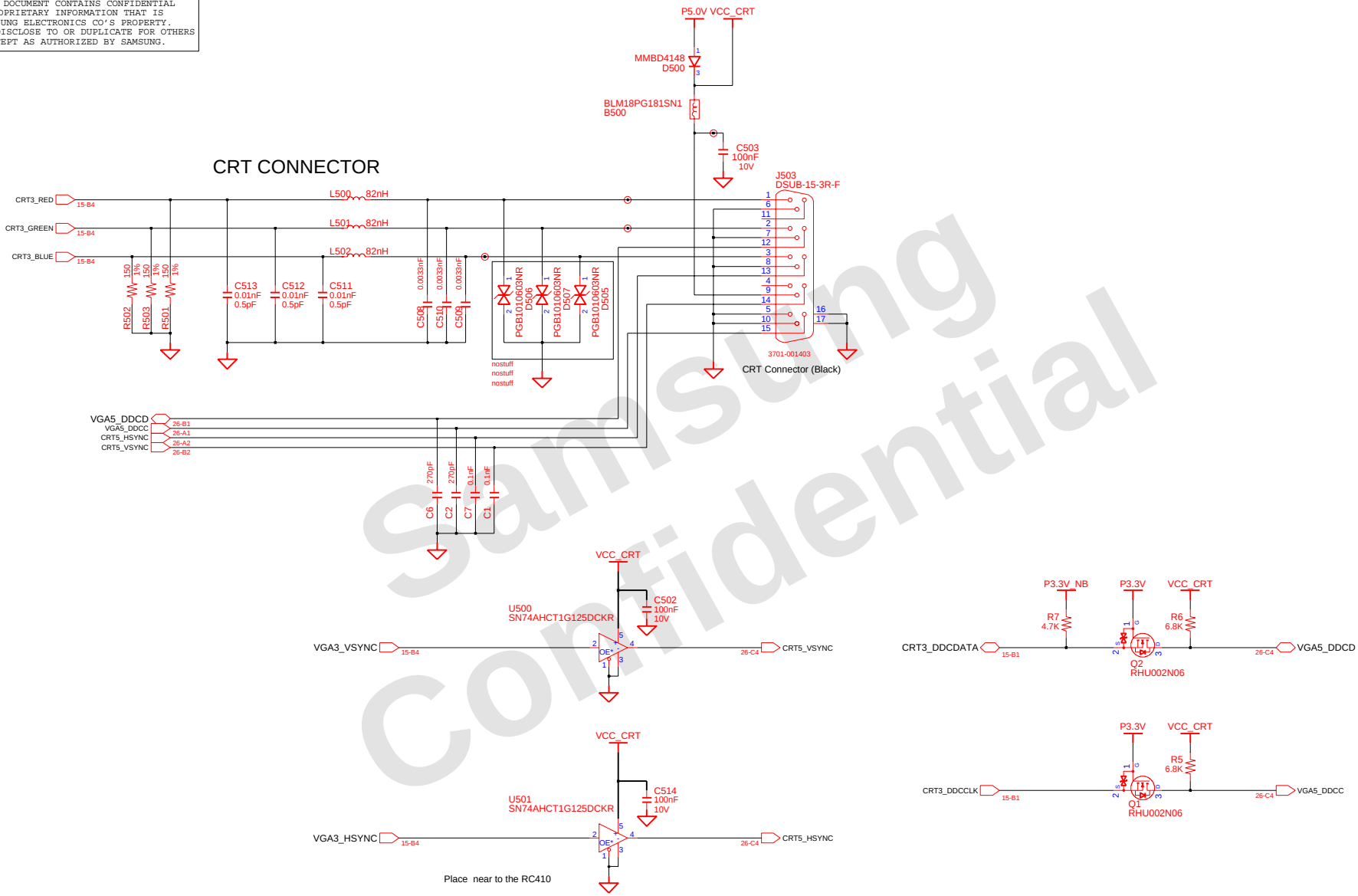




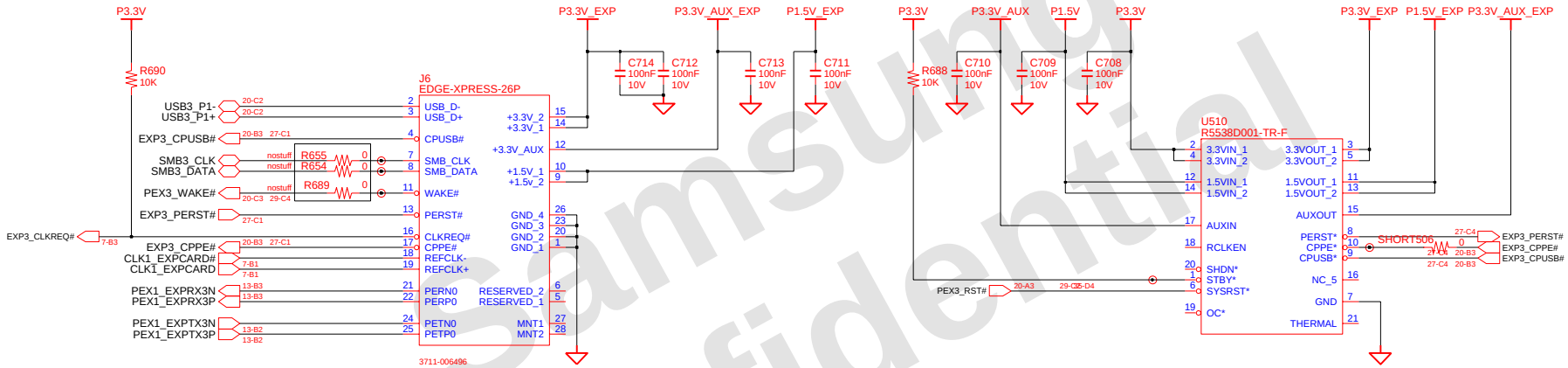


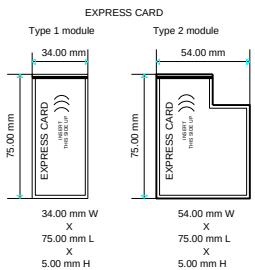


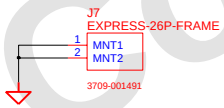
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) LCD Connector & SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 25 OF 47	



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	CRT	PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 26 OF 47	

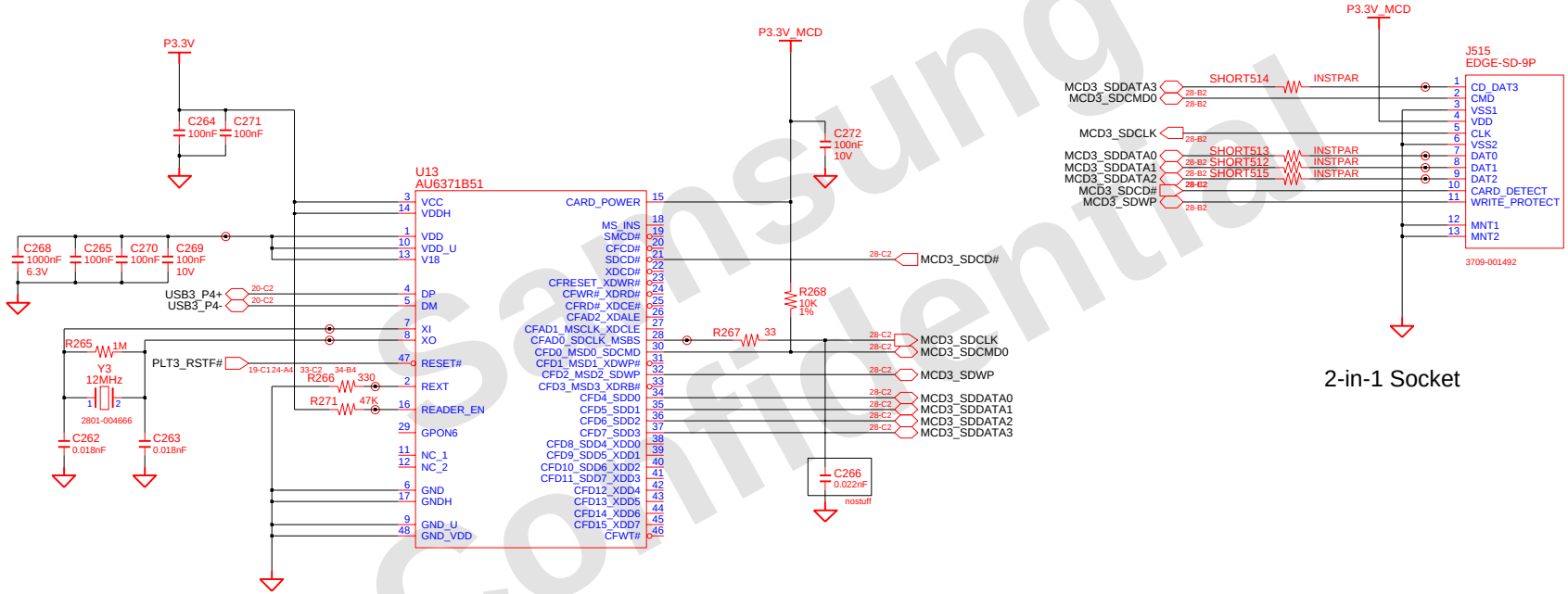






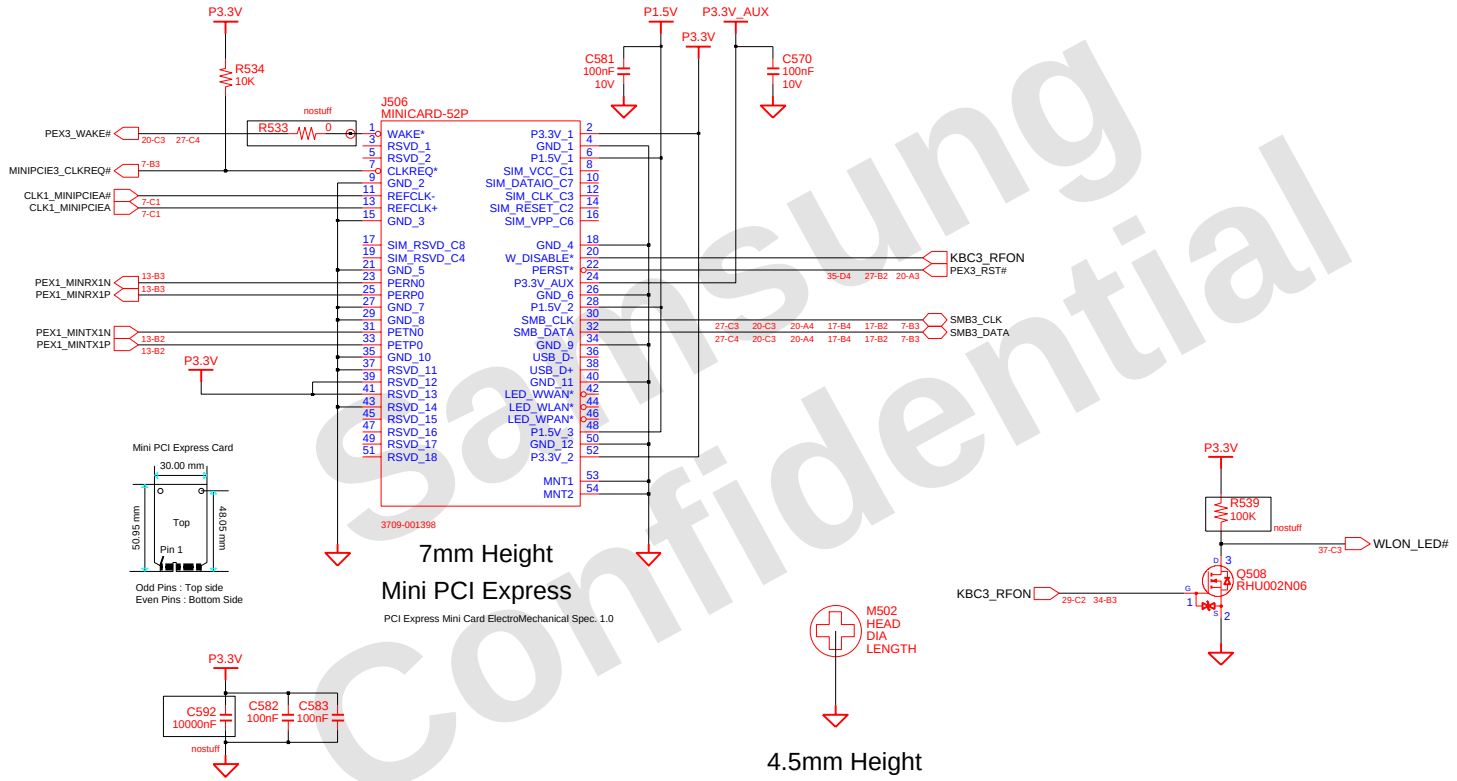
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	EXPRESS CARD	PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 27 OF 47	

2 IN 1 CARD



2-in-1 Socket

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	2 in 1 Socket	PART NO.: BA41-00791A
MODULE CODE:	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 28 OF 47	



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN MINI CARD	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 29 OF 47	

1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
3.AGND_MIC IS MIC GROUND
4.AGND_CHS IS CHASS GROUND

ALL TYPE IS 1608

C626 10nF G_AUD
C631 10nF G_AUD
C733 10nF G_AUD
R757 0 G_AUD
R756 0 G_AUD
C641 10nF G_AUD
C658 10nF G_AUD

P3.3V
C768 10000nF
C769 100nF 10V
C771 100nF 10V

U518
ALC262-GR

DVDD_CORE0 1
DVDD_CORE1 9
GPIO0 43
GPIO1 44
GPIO2 2
GPIO3 3
SDATA_OUT 5
BCLK 6
SDATA_IN 8
SYNC 10
RESET* 11
BEEP 12
CD_L 18
CD_GND 19
CD_R 20
SPDIF_EAPD 47
SPDIFO 48
DCVOL 33
JDREF 40
SENSE_A 13
SENSE_B 34
DVSS_CORE0 4
DVSS_CORE1 7
LINE_OUT_R_D 36
LINE_OUT_L_D 35
HP_OUT_R_A 41
HP_OUT_L_A 39
MIC1_R_B 22
MIC1_L_B 21
MIC2_R_F 17
MIC2_L_F 16
LINE1_R_C 24
LINE1_L_C 23
LINE1_VREFO 29
LINE2_R_E 15
LINE2_L_E 14
LINE2_VREFO 31
MONO_OUT 37
NC0 45
NC1 46
MIC2_VREFO 30
MIC1_VREFO_R 32
MIC1_VREFO_L 28
VREF 27
AVSS1 26
AVSS2 42
AVDD1 25
AVDD2 38

AUD3_EAPD# 31-C1
GPIO1 32-B4
R743 10K
CHP3_AZ_AUD_SDO 20-B4
CHP3_AZ_AUD_BCLK 20-B4
CHP3_AZ_SDI0 20-B4
CHP3_AZ_AUD_SYNC 20-B4
CHP3_AZ_AUD_RST# 20-B4 32-B4
AUD3_PCBEEP# 30-B1
R755 22
C767 1000nF
C770 0.022nF
JCK_SENS_A 30-B2
R744 20K
SHORT510 INSTPAR
SHORT511 INSTPAR
VDD_AUD
C747 100nF 10V
C754 100nF 10V
C749 10000nF
G_AUD

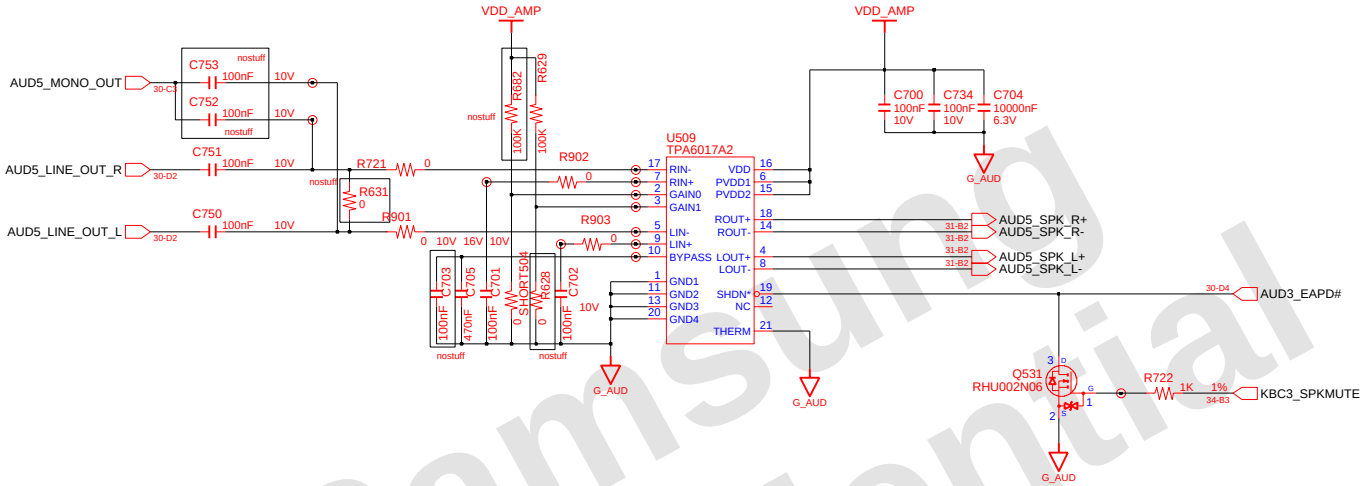
AUD5_LINE_OUT_R 31-C4
AUD5_LINE_OUT_L 31-C4
EC51100uF 16V AS
EC8 100uF 16V AS
R607 56
R177 56
HP_OUT_R 32-B2
HP_OUT_L 32-B2
C746 1000nF
C745 1000nF
MIC1 32-D2
MIC2 32-D2
R178 20K
R605 20K
G_AUD
R742 2.2K
R739 2.2K
AUD5_MONO_OUT 31-D4

JCK_SENS_A 30-C4
R740 H/P 39.2K
JCK_SENS_HP# 32-B2
R741 MIC 20K
JCK_SENS_MIC# 32-D2

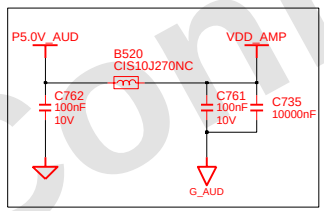
PC BEEP
VDD_AUD
R752 20K
AUD3_PCBEEP# 30-C4
CHP3_SPKR 20-C3
R751 1K
Q537 RHU002N06
R753 1K
C764 4.7nF
G_AUD

P5.0V_AUD
VDD_AUD
C766 1000nF 6.3V
C763 100nF 10V
SHORT529 R1608-SHORT
U519 MIC5252-4.75BM5
IN
GND
EN
OUT
BYPASS
C765 100nF 10V
C748 10000nF
C760 1000nF
LDO
G_AUD

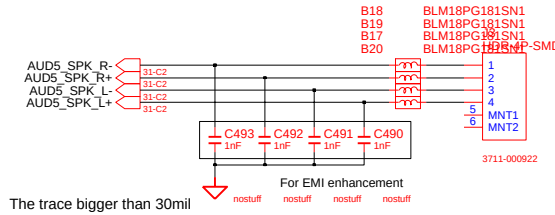
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 30 OF 47	



AMP_VDD



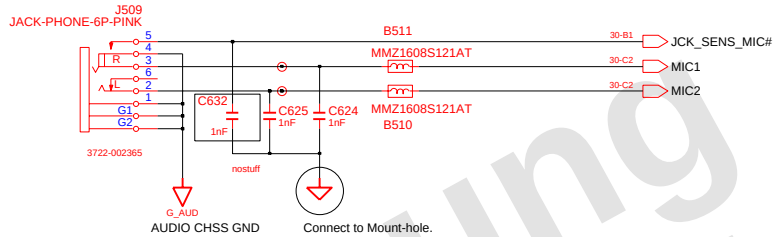
INTERNAL STEREO SPEAKERS



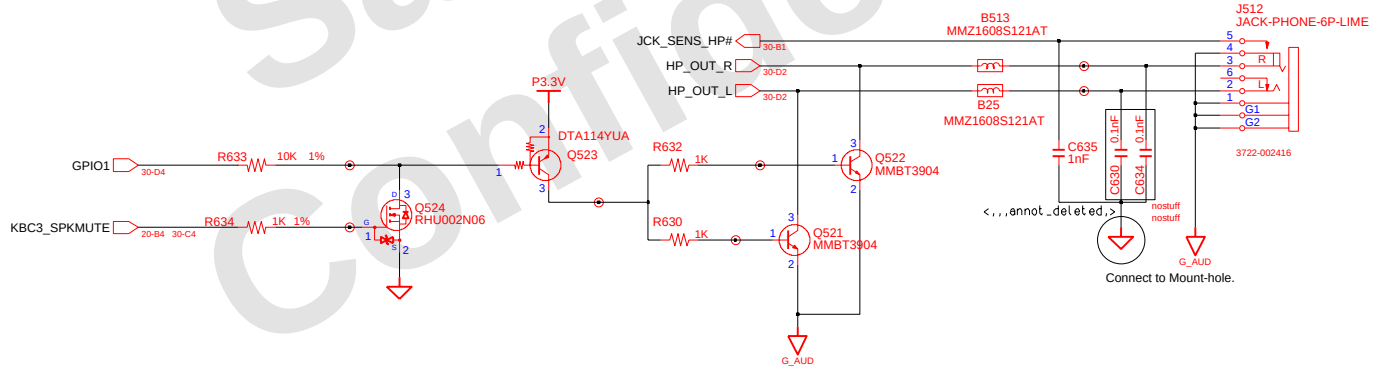
The trace bigger than 30mil

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 31 OF 47	

MIC JACK



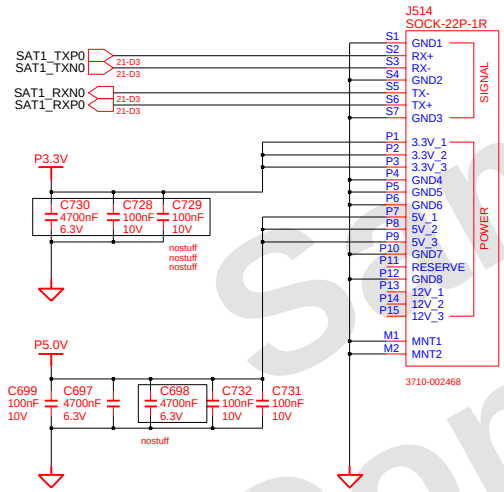
HEADPHONE



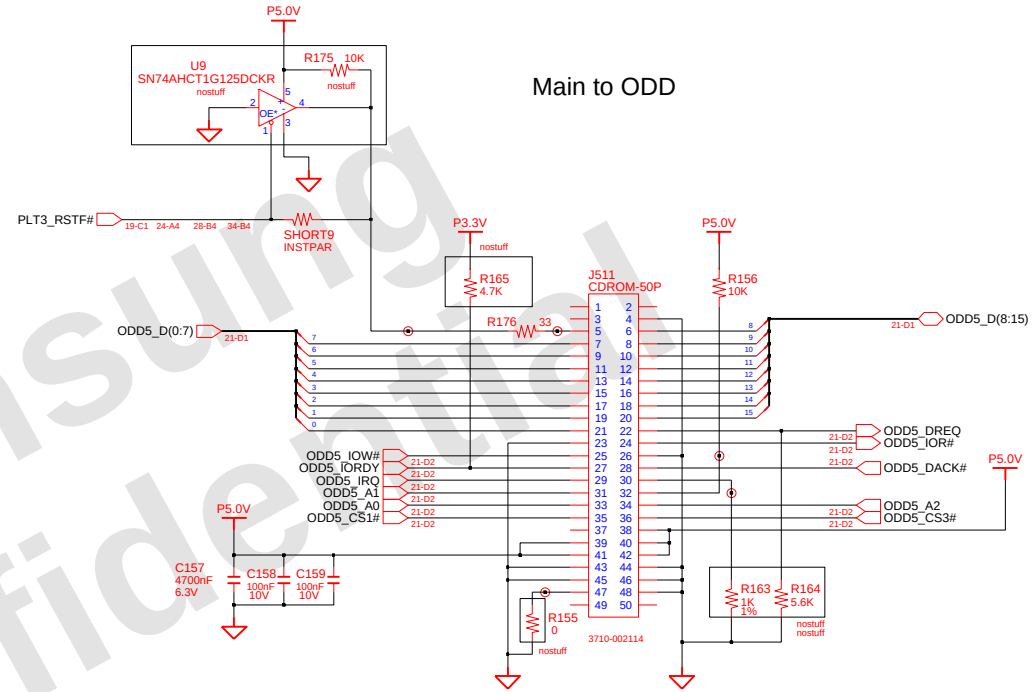
The traces led to Audio Jacks have the width over 10mil

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN MIC & HEADPHONE	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 32 OF 47	

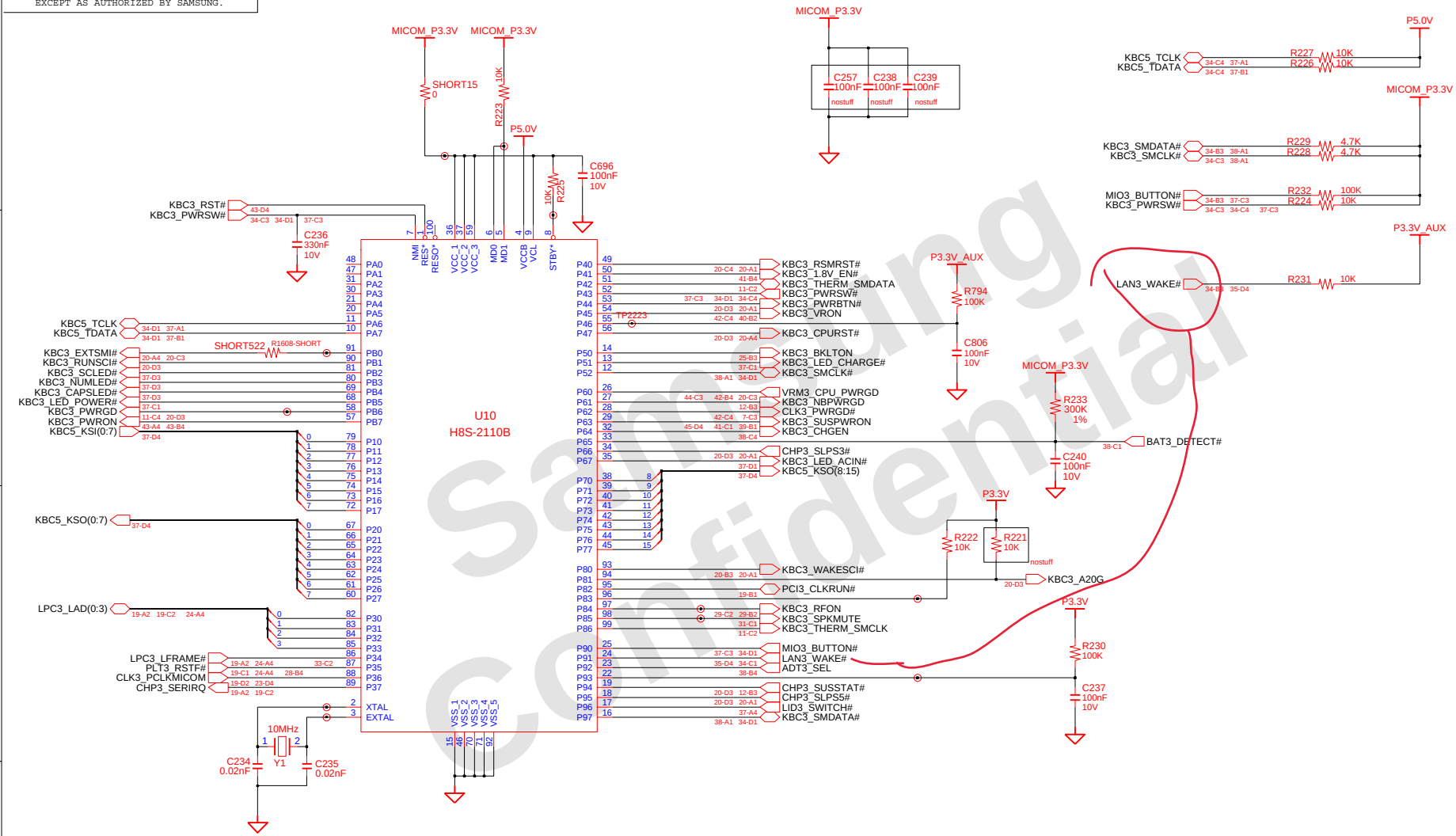
Main to HDD



Main to ODD



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00791A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 33 OF 47	



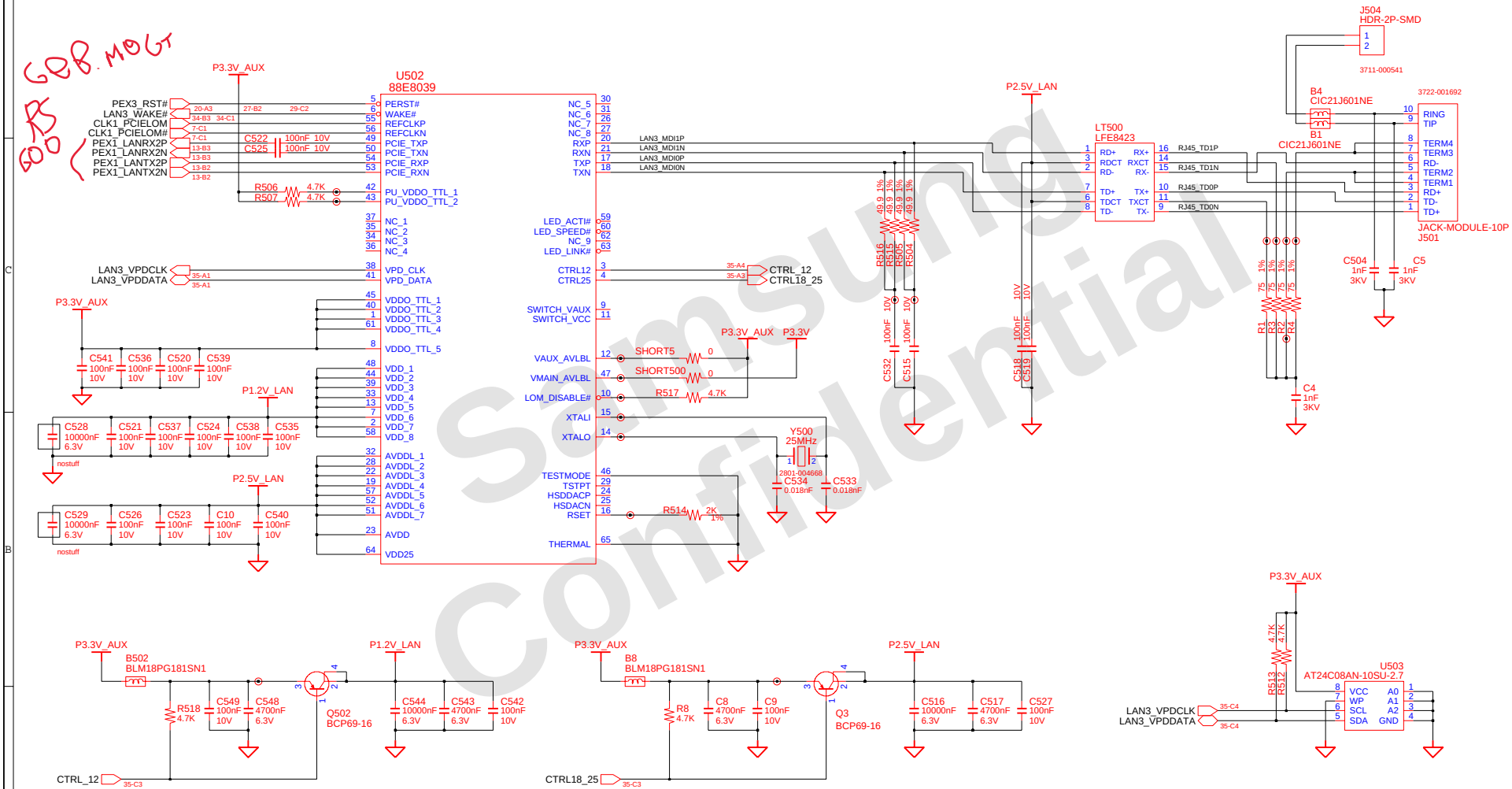
MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

The removed signal compaired from 144pin

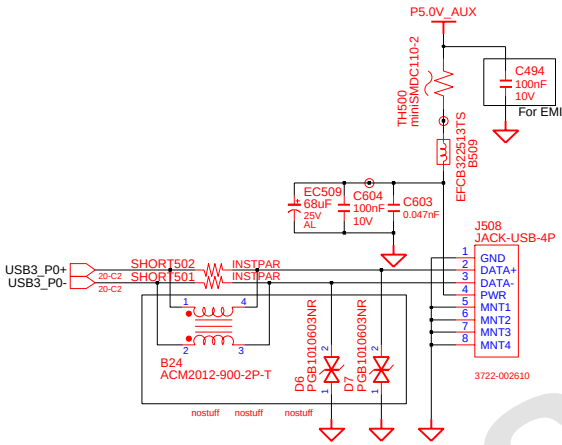
- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) POWER MICOM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 34 OF 47	



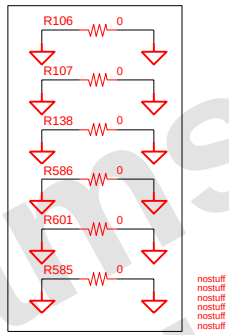
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN LAN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 35 OF 47	

Side USB Connecter



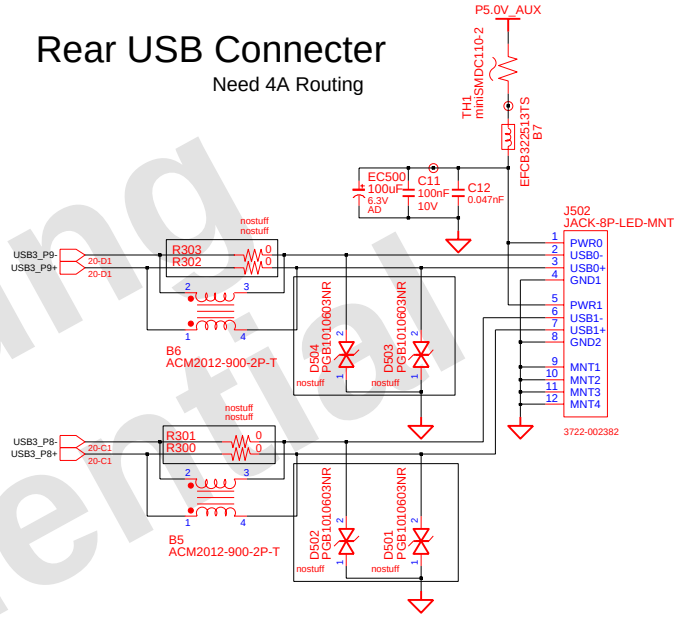
Connect left side USB GND with CPU GND

Top : 3EA Bottom : 3EA

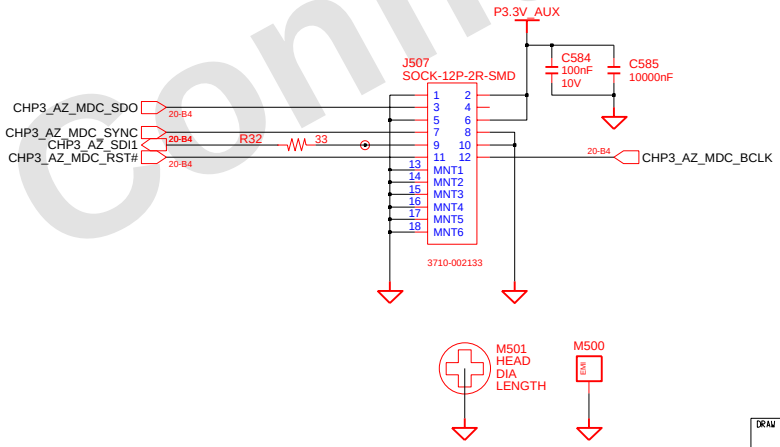


Rear USB Connecter

Need 4A Routing



MDC Connecter

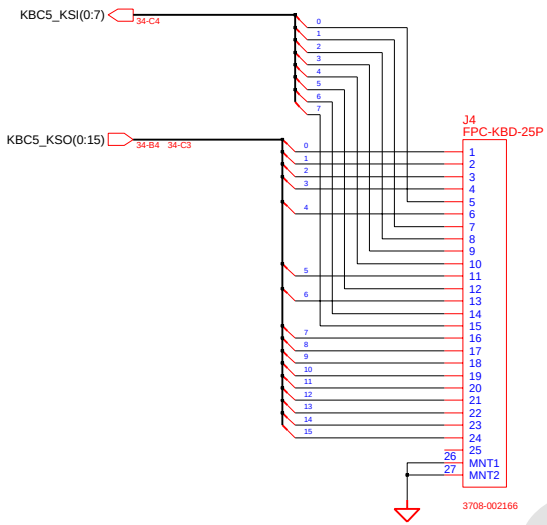


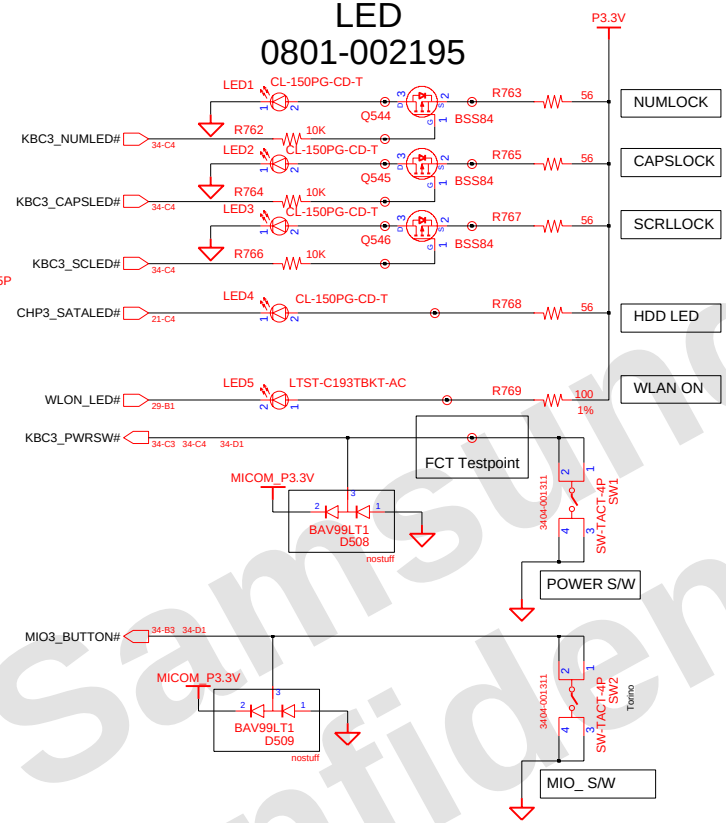
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN USB PORT & MDC Conn.
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	36 OF 47

SAMSUNG ELECTRONICS
PART NO. BA41-00791A

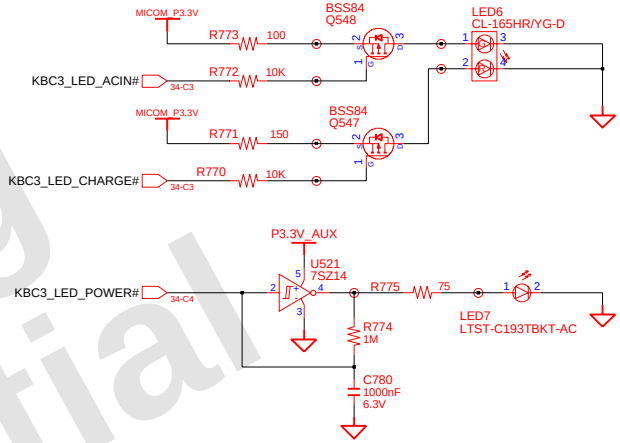
LED
0801-002195

KEYBOARD

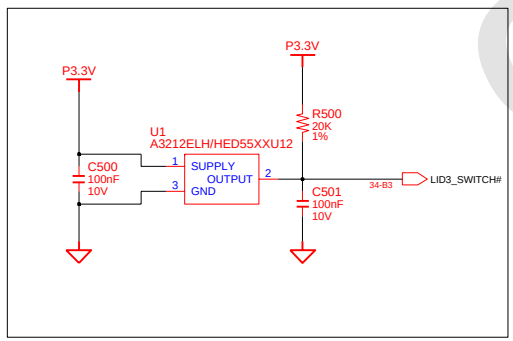




ADAPTERIN/CHARGING LED

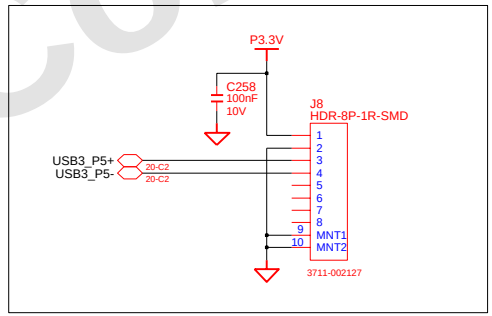


LID SWITCH

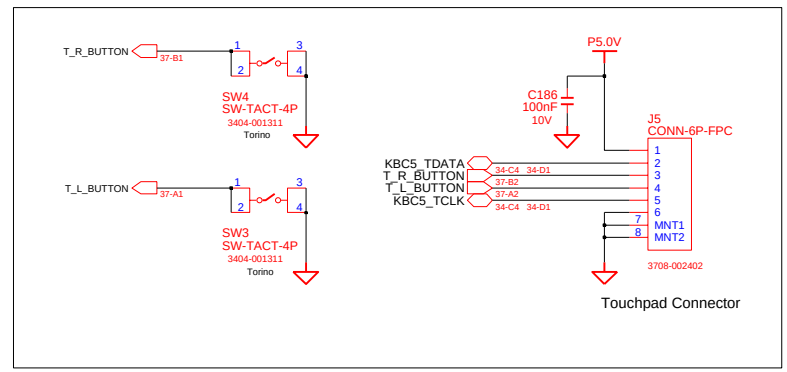


Bluetooth Interface

Factory Option



TOUCHPAD

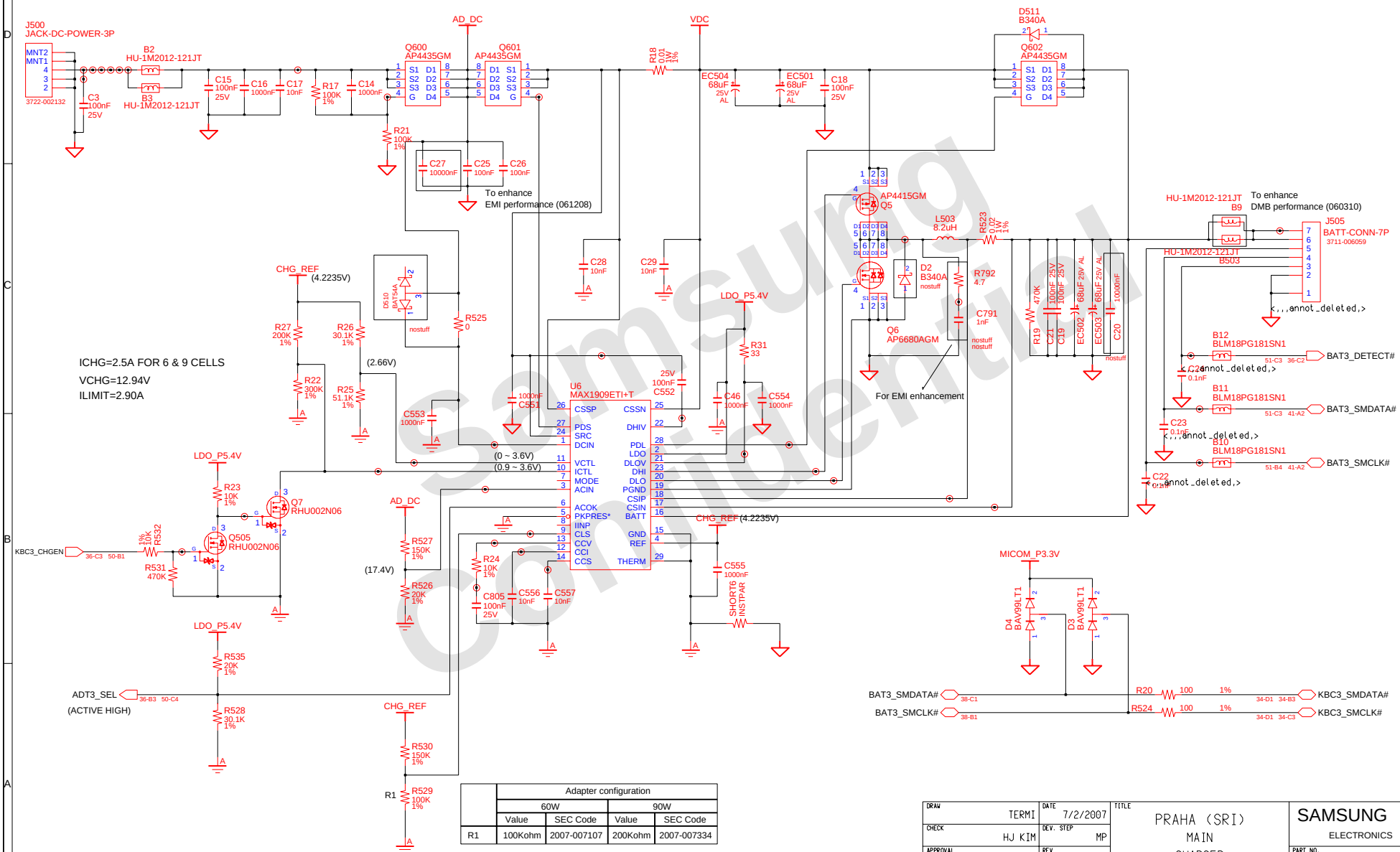


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) LED & BLUETOOTH TOUCHPAD & KBD & LID S/W
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	37 OF 47

SAMSUNG ELECTRONICS

PART NO. BA41-00791A

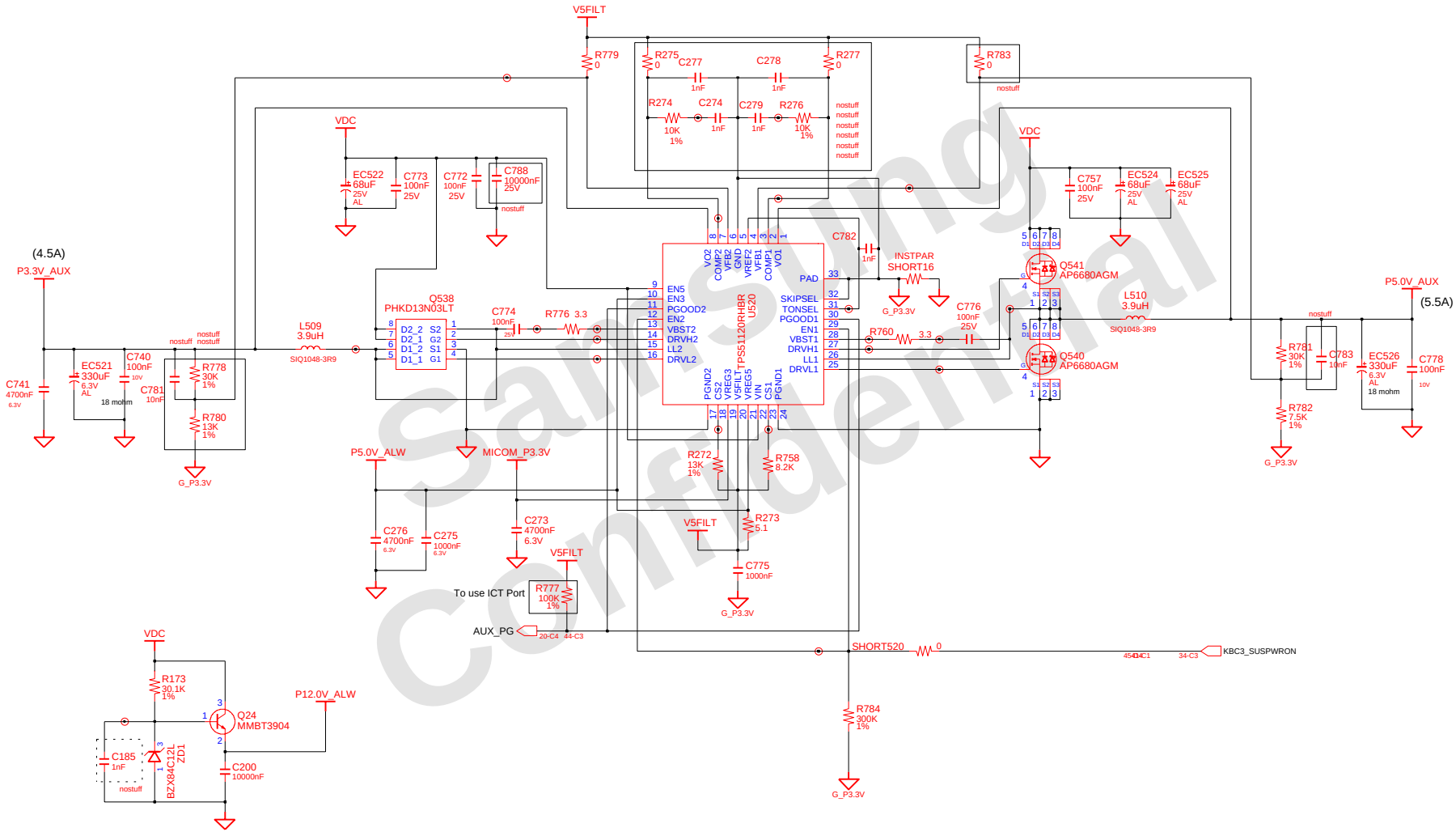
CHARGER & POWER MANAGEMENT



	Adapter configuration			
	60W		90W	
	Value	SEC Code	Value	SEC Code
R1	100Kohm	2007-007107	200Kohm	2007-007334

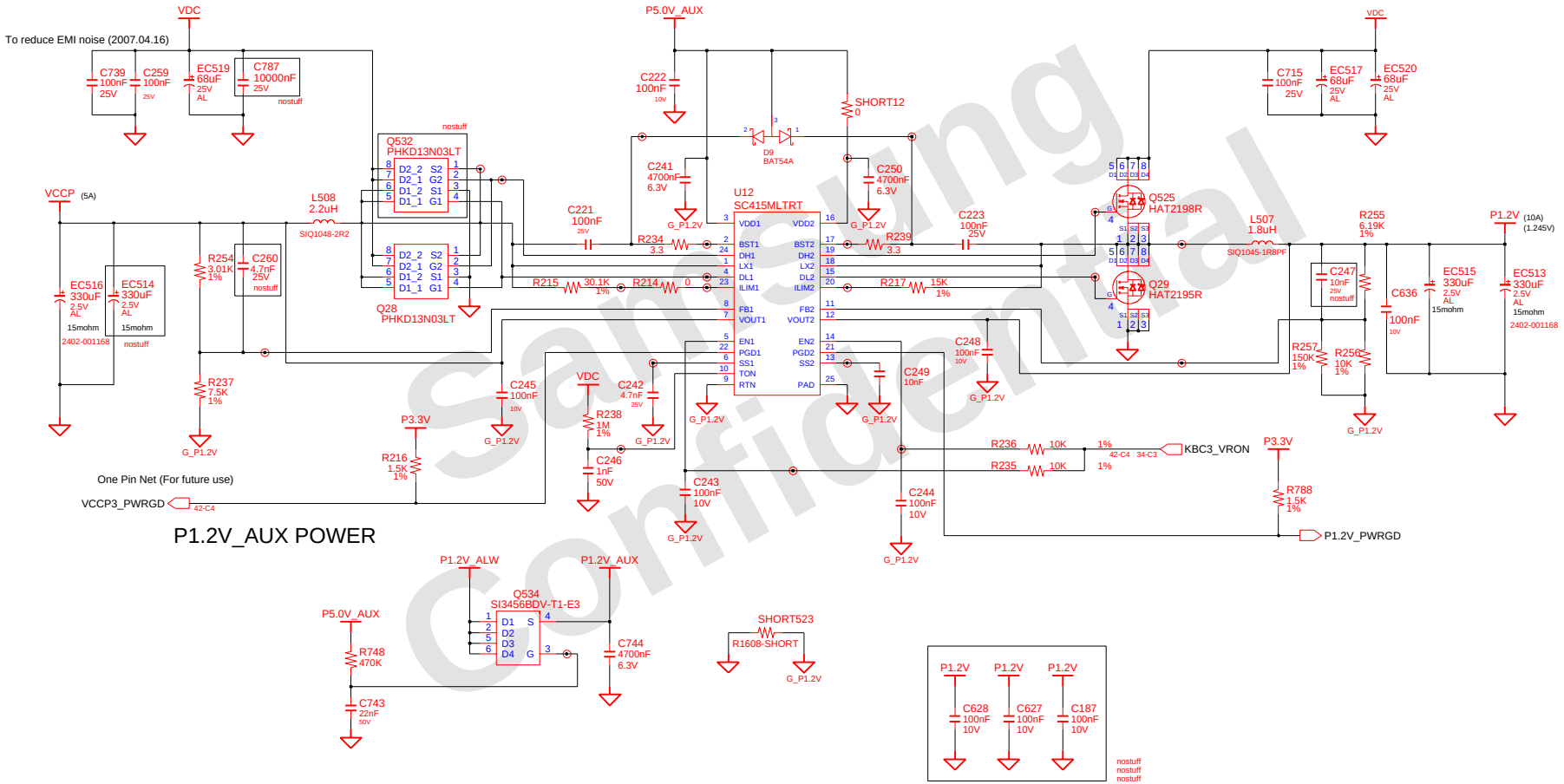
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 38 OF 47	

P3.3V_AUX & P5V_AUX



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) POWER P3.3V_AUX & P5V_AUX	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 39 OF 47	

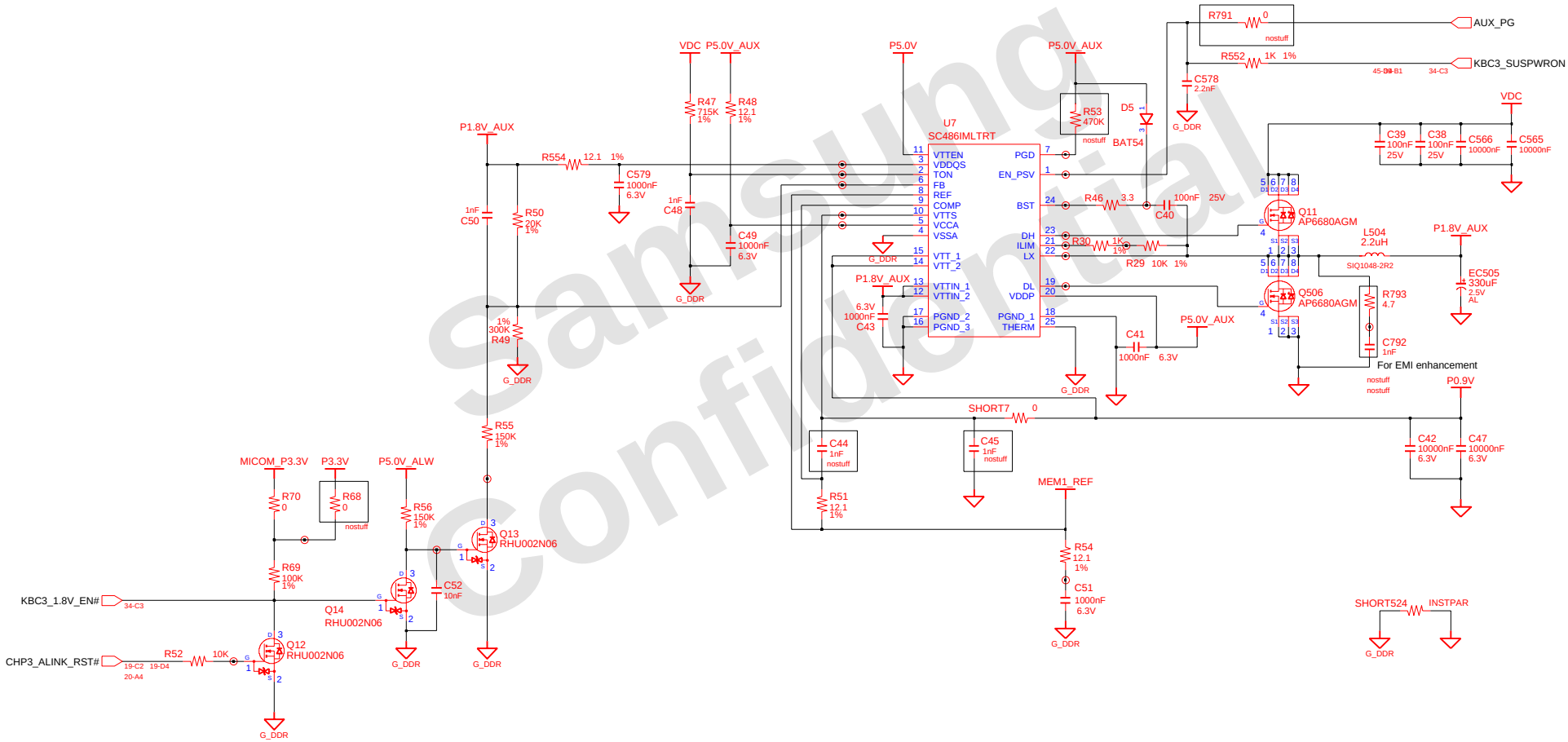
P1.2V & VCCP _CORE(1.05V)



P1.2V_AUX POWER

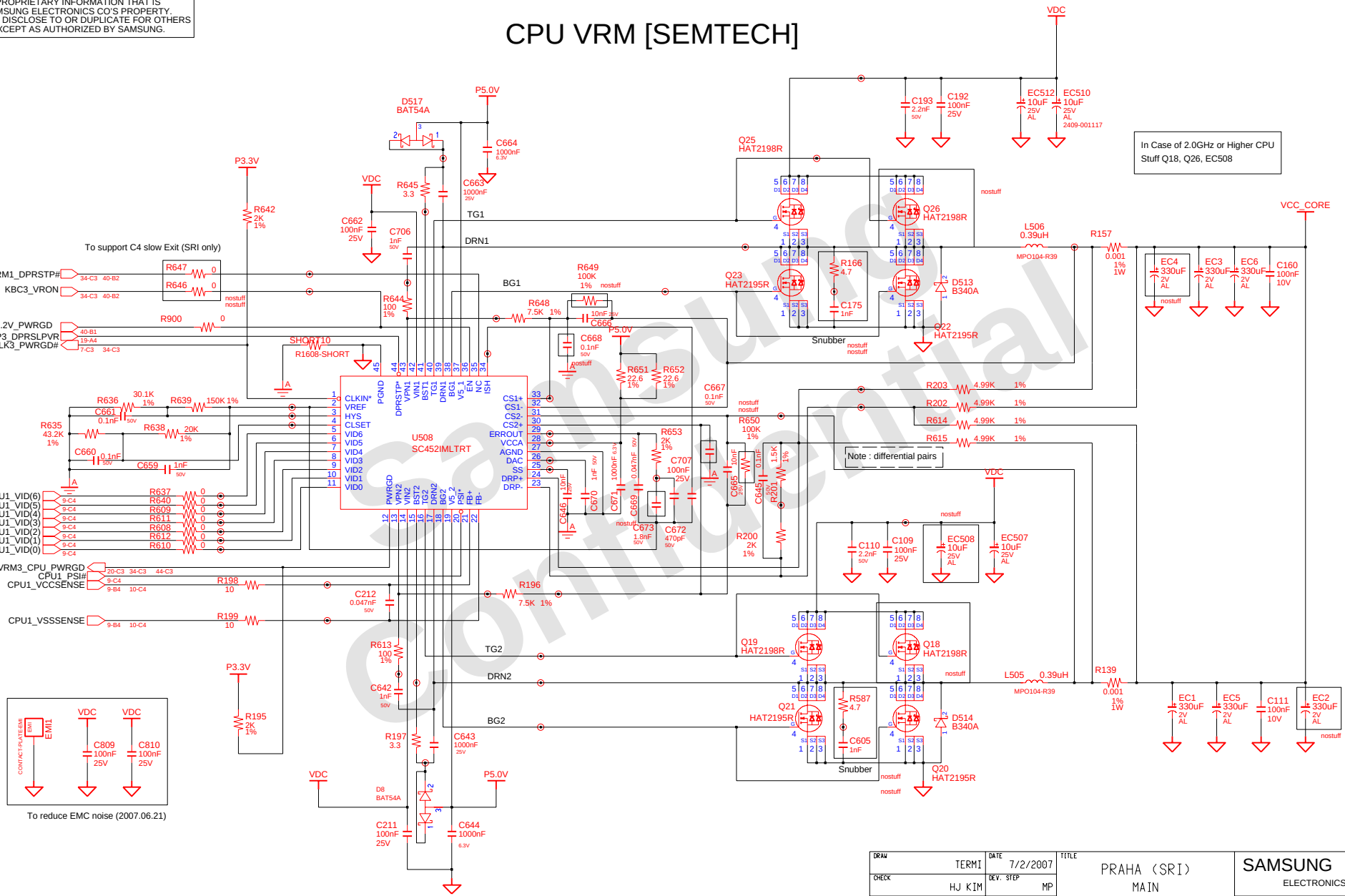
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) POWER P1.2V & P1.2V_AUX &VCCP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 40 OF 47	

DDR2 Power



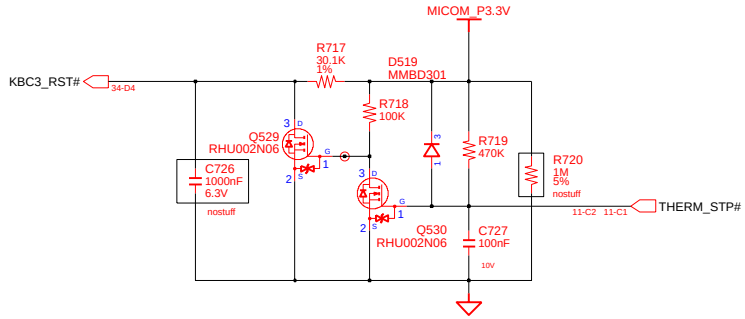
DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 41 OF 47	

CPU VRM [SEMTECH]

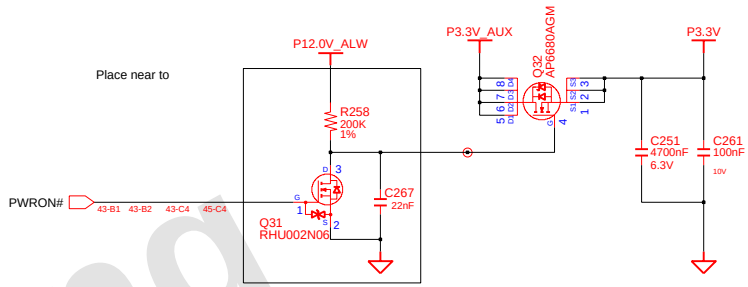


DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN CPU VRM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO: BA41-00791A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 42 OF 47	

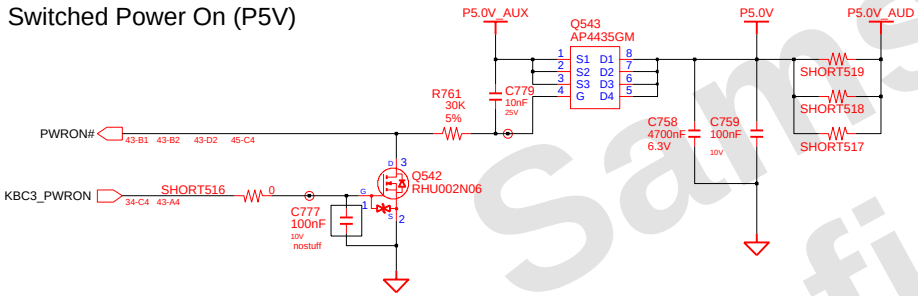
MICOM RESET



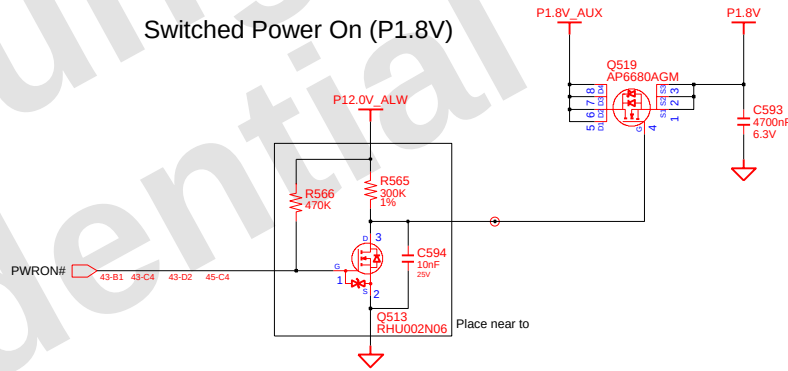
Switched Power On (P3.3V)



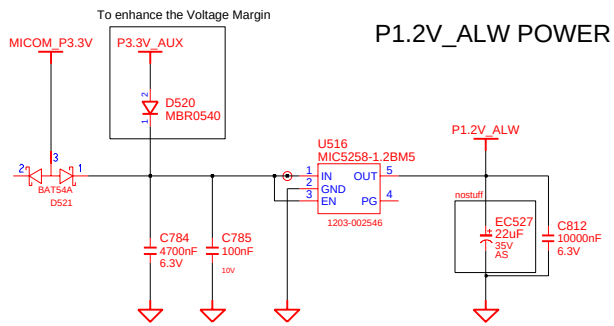
Switched Power On (P5V)



Switched Power On (P1.8V)

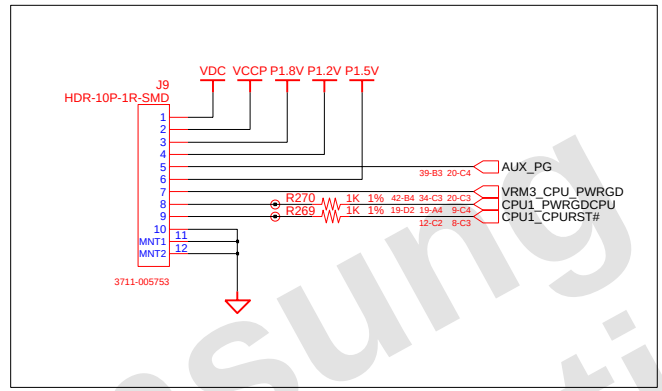


P1.2V_ALW POWER

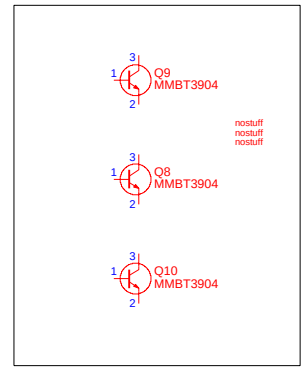


DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 43 OF 47	

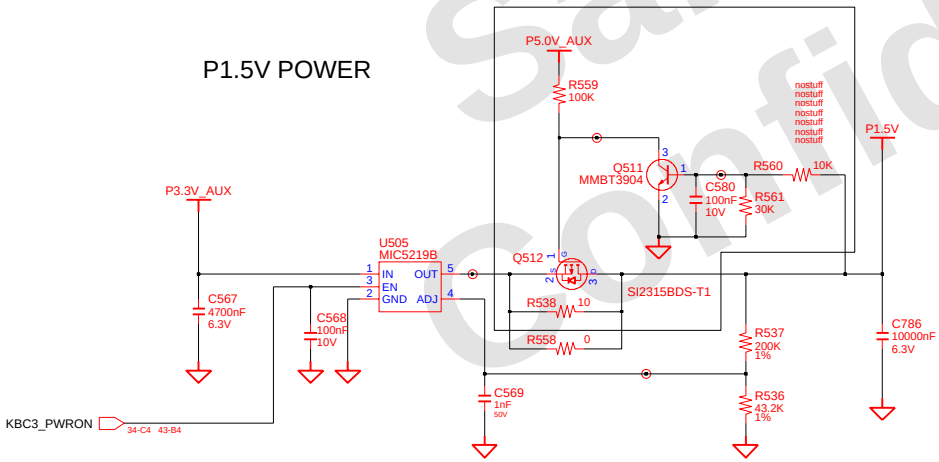
ICT PORT



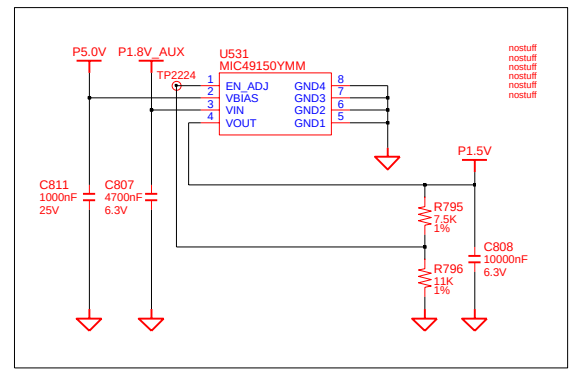
For Debugging



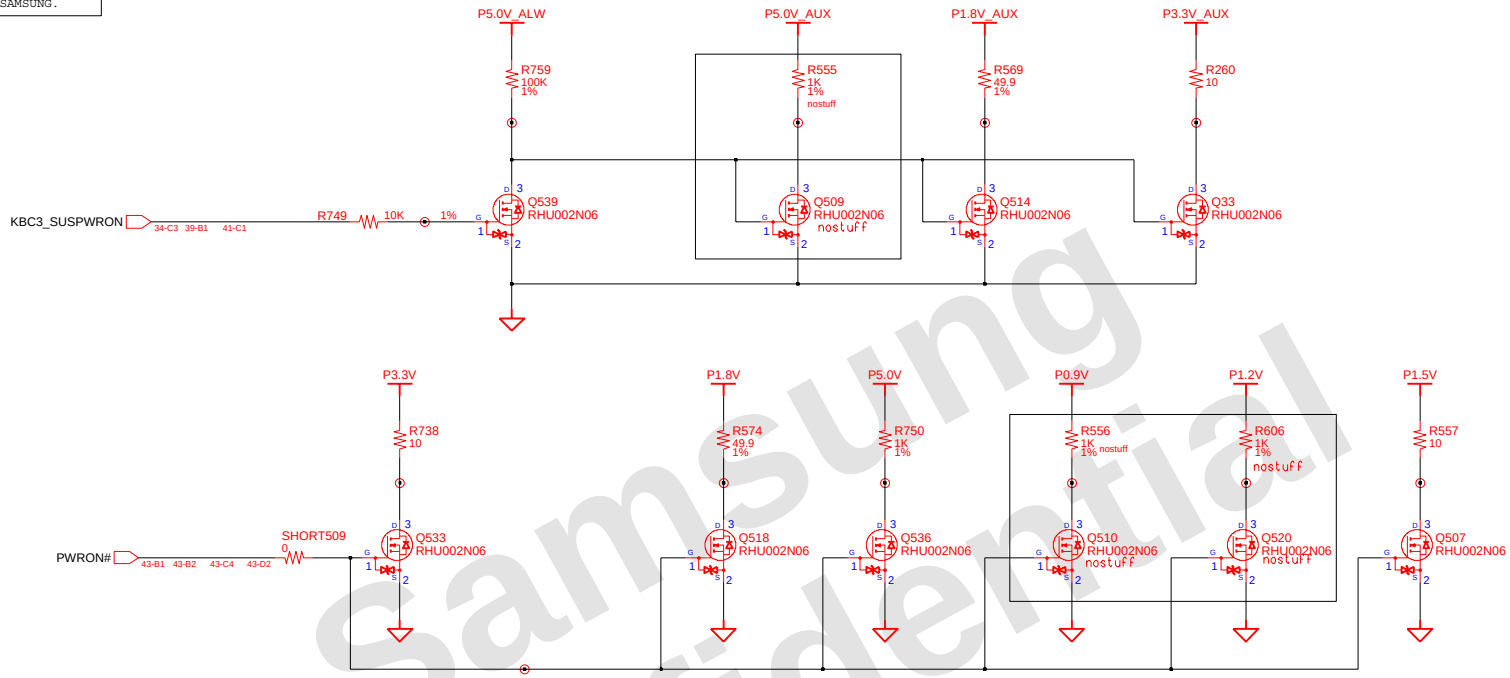
P1.5V POWER



To make up PCI Express 1.5V rail current margin (nostuff)

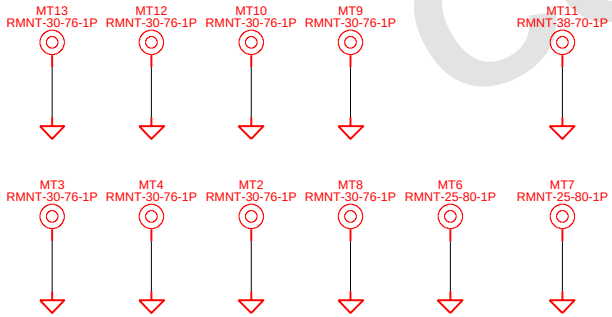


DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	ICT PORT	PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 44 OF 47	

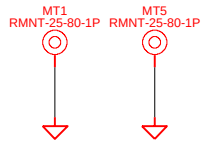


System

Located in lower left corner of PCB



Board



DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI) MAINBD POWER DRAW & MNT HOLE	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 45 OF 47	

REV1

PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)
CHECK	HJ KIM	DEV. STEP	MP		TP
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM		

SAMSUNG ELECTRONICS

PART NO. BA41-00791A

- AC_SDOUT
- ADT3_SEL
- AUD3_EAPD#
- AUD3_PCBEEP#
- AUD5_LINE_OUT_L
- AUD5_LINE_OUT_R
- AUD5_MONO_OUT
- AUD5_SPK_L+
- AUD5_SPK_L-
- AUD5_SPK_R+
- AUD5_SPK_R-
- AUX_PG
- BAT3_DETECT#
- BAT3_SMCLK#
- BAT3_SMDATA#
- CHP3_ALINK_RST#
- CHP3_AZ_AUD_BCLK
- CHP3_AZ_AUD_RST#
- CHP3_AZ_AUD_SDO
- CHP3_AZ_AUD_SYNC
- CHP3_AZ_MDC_BCLK
- CHP3_AZ_MDC_RST#
- CHP3_AZ_MDC_SDO
- CHP3_AZ_MDC_SYNC
- CHP3_AZ_SDI0
- CHP3_AZ_SDI1
- CHP3_BIOSWP#
- CHP3_DPRSLPVR
- CHP3_NBRST#
- CHP3_SATALED#
- CHP3_SBPME#
- CHP3_SBTHRMTRIP#
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS5#
- CHP3_SPKR
- CHP3_SUSSTAT#
- CPU1_A20M#
- CPU1_ADS#
- CPU1_BNR#
- CPU1_BPRI#
- CPU1_BREQ#
- CPU1_BSEL0
- CPU1_BSEL1
- CPU1_BSEL2
- CPU1_CPURST#
- CLK3_DBGLPC
- CLK3_ICH14
- CLK3_NB14M
- CLK3_PCLKMICOM
- CLK3_PWRGD#
- CLK3_USB48
- CPU1_DBSY#
- CPU1_DEFER#
- CPU1_DPRSTP#
- CPU1_DPSLP#
- CPU1_DPWR#
- CPU1_DRDY#
- CPU1_FERR#
- CPU1_HIT#
- CPU1_HITM#
- CPU1_IGNNE#
- CPU1_INIT#
- CPU1_INTR
- CPU1_LOCK#
- CPU1_NMI
- CPU1_PSI#
- CPU1_PWRGDCPU
- CPU1_RS0#
- CPU1_RS1#
- CPU1_RS2#
- CPU1_SLP#
- CPU1_SMI#
- CPU1_TCK
- CPU1_TDI
- CPU1_THRMTRIP#
- CPU1_TMS
- CPU1_TRDY#
- CPU1_TRST#
- CPU1_VCCSENSE
- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CPU1_VSSSENSE
- CPU2_THERMDA
- CPU2_THERMDC
- CPU3_THRMTRIP#
- CRT3_BLUE
- CRT3_DDCCLK
- CRT3_DDCDATA
- CRT3_GREEN
- CRT3_RED
- CRT5_HSYNC
- CRT5_VSYNC
- CTRL18_25
- CTRL_12
- EXP3_CLKREQ#
- EXP3_CPPE#
- EXP3_CPUSB#
- EXP3_PERST#
- FAN3_FDBACK#
- FAN5_VDD
- GPIO1
- HP_OUT_L
- HP_OUT_R
- ITP3_DBRESET#
- ITP3_SYSRST#
- JCK_SENS_A
- JCK_SENS_HP#
- JCK_SENS_MIC#
- KBC3_1.8V_EN#
- KBC3_A20G
- KBC3_BKLTON
- KBC3_CAPSLED#
- KBC3_CHGEN
- KBC3_CPURST#
- KBC3_EXTSMI#
- KBC3_LED_ACIN#
- KBC3_LED_CHARGE#
- KBC3_LED_POWER#
- KBC3_NBPWRGD
- KBC3_NUMLED#
- KBC3_PWRBTN#
- KBC3_PWRON
- KBC3_RSMRST#
- KBC3_RST#
- KBC3_RUNSCI#
- KBC3_SCLED#
- KBC3_SMCLK#
- KBC3_SMDATA#
- KBC3_SUSPWRON
- KBC3_THERM_SMCLK
- KBC3_THERM_SMDATA
- KBC3_VRON
- KBC3_WAKESCI#
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- KBC5_TCLK
- KBC5_TDATA
- LAN3_VPDCLK
- LAN3_VPDDATA
- LAN3_WAKE#
- LCD3_BKLTCTRL
- LCD3_BKLTEN
- LCD3_BKLTON
- LCD3_EDID_CLK
- LCD3_EDID_DATA
- LCD3_VDDEN
- LID3_SWITCH#
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- LPC3_LFRAME#
- MCD3_SDCD#
- MCD3_SDCLK
- MCD3_SDCMD0
- MCD3_SDDATA0
- MCD3_SDDATA1
- MCD3_SDDATA2
- MCD3_SDDATA3
- MCD3_SDWP
- MIC1
- MIC2
- MINIPCIE3_CLKREQ#
- MIO3_BUTTON#

DRAW: TERMI	DATE: 7/2/2007	TITLE: PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00791A
MODULE CODE: undefined	LAST EDIT: July 2, 2007 11:28:38 PM	PAGE 47 OF 47