Compal Confidential

Schematics Document

Intel Chief River Platform

U5

LA-7822P

2012-02-23

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: *Cover Sheet*

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U5

Fan Control
Page 31

ZZZ1 PCB-MB
PCB P/N for Load BOM

ZZZ2 45@ PCB-CRT/B
PCB P/N for 45 CRT/B

DDR3 1333/1600MHz 1.5V
Dual Channel

DDR3-SO-DIMM X 2
BANK 0, 1, 2, 3
+1.5V, +0.75VS
Page 10, 11

Mobile
Ivy Bridge
Processor
rPGA 988B Socket
Page 4 ~ 9
+VCC_CORE, +VCCP, +VCC_GFXCORE_AVG, +1.5V_CPU_VDDQ, +1.8VS, _VCCSA

FDI x8 (UMA) 100MHz 2.7GT/s

DMI x4 100MHz 5GB/s

Intel PANTHER-POINT PCH
HM77
FCBGA 989 Balls
Page 12 ~ 19
+1.05VS, +1.8VS, +3VS, +3V_PCH, +5V_PCH, +RTCVCC, +VCCAFDI_VRM

LCD conn Page 20 — LVDS, EDID, DISPOFF#, PWM
CRT Conn Page 23 — RGB, HV Sync, DDC
HDMI Page 21 — HDMI, DDC

USB2.0
port 2,3 → USB conn x2 (USB Board) Page 30
port 4 → Camera Page 26
port 9 → USB conn x1 Page 25
port 10 → Touch Panel Page 20
port 13 → BT (MiniCard-1) Page 26
port 12 → RF Module Page 26
port 3,4 → USB conn x2 (USB Board) Page 30

USB3.0
port 1 → USB conn x1 (CRT Board) Page 23
port 2
port 0 → USB conn x1 Page 30
port 1

Thunderbolt
mDP CONN Page 33 — CIO — Cactus Ridge Page 32-35 — DisplayPort
port 5-8

PCI-e
port 4 → Card Reader (Realtek RTS5209) Page 22 → Memory Card Slot (MS / SD / SDxC) Page 22
port 3 → LAN/CRT Board 10/100/1000 LAN Realtek GbE (RTL8111F) Page 23
port 2 → Mini Card-1 (WLAN) Page 26

Azalia → Realtek ALC275Q-GR Audio CKT Page 24
- Audio Jack (HP) Page 24
- Audio Jack (MIC) Page 24
- Speaker Connector Page 24

SATA
port 0 → Mini Card SSD Page 26
port 1 → 2.5" SATA HDD Connector Page 27
port 2 → SATA ODD Connector Page 27

SPI → SPI ROM 8MB Page 12

LPC BUS

Touch Pad CONN. Page 29
ENE KB9012QF (+3VLP/+3VALW) page 28
Int. KBD Page 29

SPI ROM 256KB Page 28

DC/DC Interface CKT. Page 32

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Title: Block Diagram
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VALW +3VALW	+3V_PCH +5V_PCH	+VCCP	+1.5V	+5VS +3VS +1.5VS +VCC_GFXCORE +VCCP +CPU_CORE +1.8VS +0.75VS +VCCSA +1.5V_CPU_VDDQ
S0	O	O	O	O	O	O	O
S3 / DC	O	O	O	O	X	O	X
S3 / AC	O	O	O	O	X	O	X
S3 / S4 / S5 WoLAN	O	O	O	O	X	X	X
S5 S4/AC	O	O	O	O	X	X	X
S5 S4/ Battery only	O	O	O	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

PD@ : means Parade PS8710BT
PC@ : means PERICOM PI3EQX7502IZDEX
TB@ : means Thunderbolt
@ : means just reserve , no build
CONN@ : means ME part.

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

U5

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

	Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
U5 ES0	0	0	0 V	0 V	0 V
U5 ES1	1	26.1K +/- 5%	0.6191 V	0.683 V	0.7526 V
U5 ES2	2	34.8K +/- 5%	0.7745 V	0.8519 V	0.9358 V
U5 PP	3	46.4K +/- 5%	0.9801 V	1.0459 V	1.1133 V
U5 IRT	4	56.2K +/- 5%	1.1136 V	1.1873 V	1.2627 V
	* 5	71.5K +/- 5%	1.2918 V	1.3758 V	1.4615 V
	6	NC	2.500 V	3.300 V	3.300 V
	7				

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	3.3K +/- 5%	0.0908 V	0.1054 V	0.121 V
2	6.8K +/- 5%	0.1817 V	0.2101 V	0.2422 V
3	10K +/- 5%	0.2601 V	0.3 V	0.3448 V
4	15K +/- 5%	0.3746 V	0.4304 V	0.4927 V
5	20K +/- 5%	0.4974 V	0.55 V	0.6076 V
6	NC	2.500 V	3.300 V	3.300 V
7				

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	EC-KB930	Cactus Ridge	PCH	Smart Charge
SMB_EC_CK1 SMB_EC_DA1	EC	V	X	X	X	X	X	V
SMBCLK SMBDATA	PCH	X	V	V	X	X	X	X
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	V	X	X	X

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Title: **Notes List**

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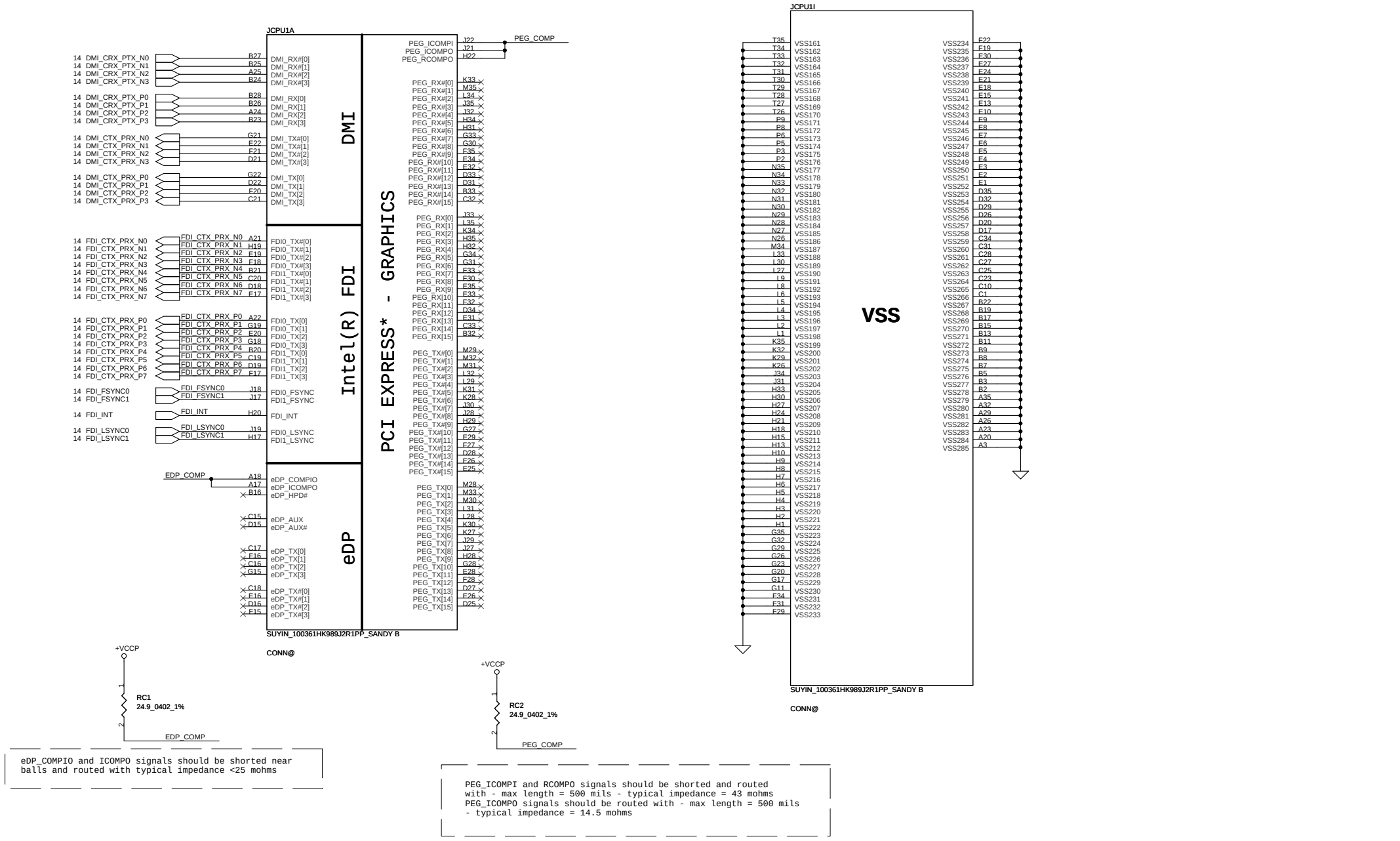

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Compal Electronics, Inc.			
Title: PROCESSOR(1/6) DMI,FDI,PEG			
Size: Custom	Document Number: LA-7822P		Rev: B
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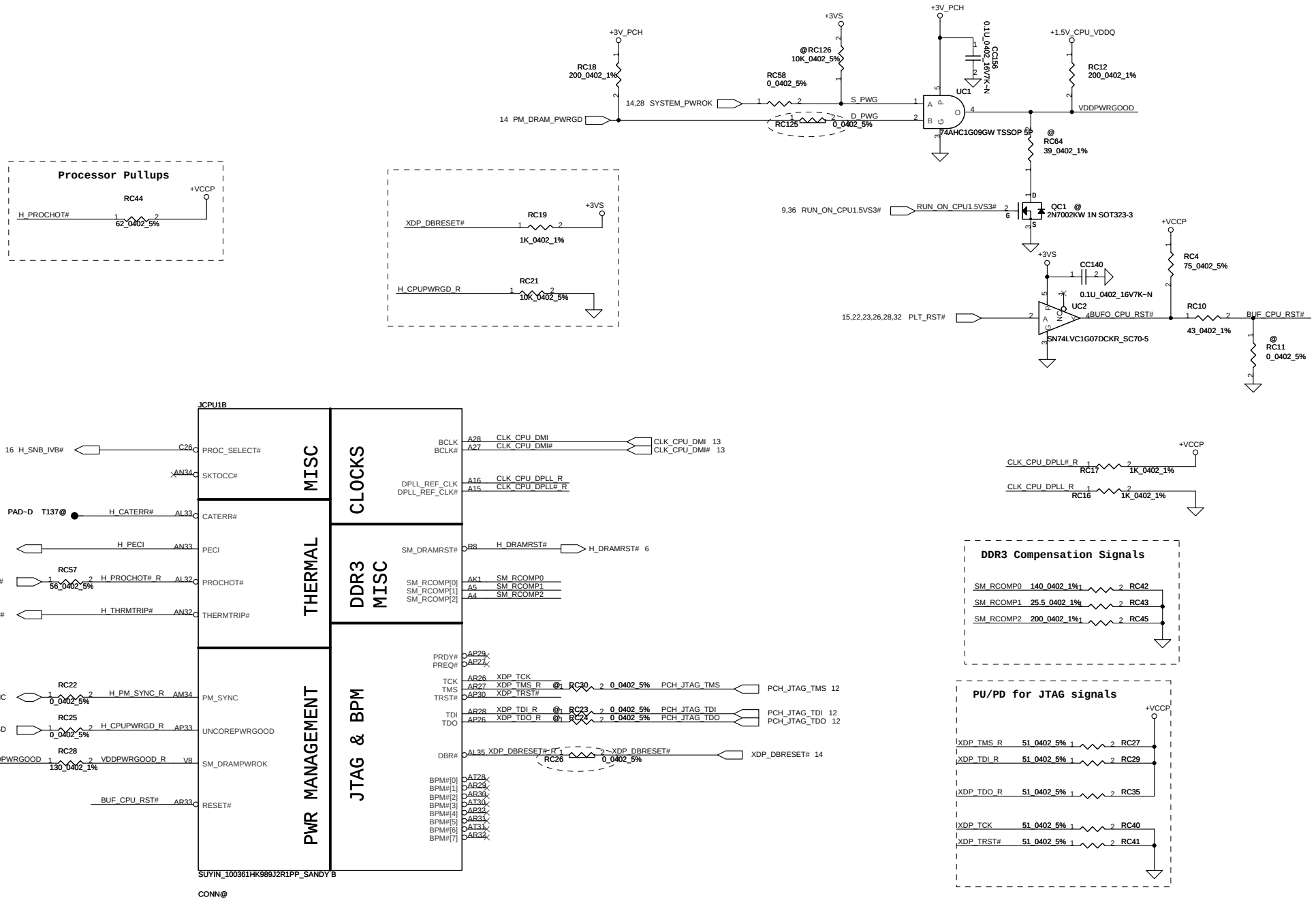

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Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.			
Title: PROCESSOR(2/6) PM,XDP,CLK			
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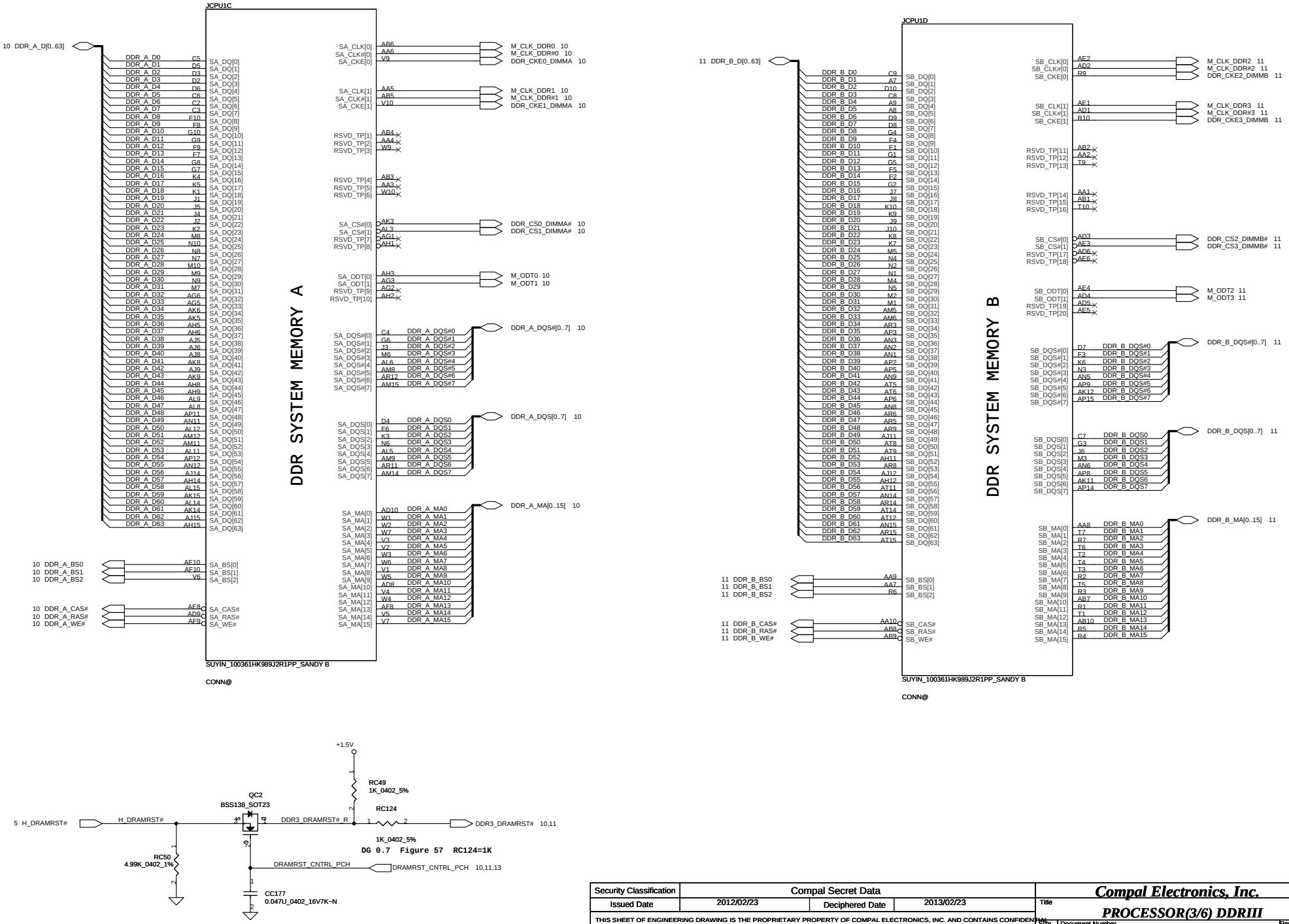

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Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: **PROCESSOR(3/6) DDRIII**

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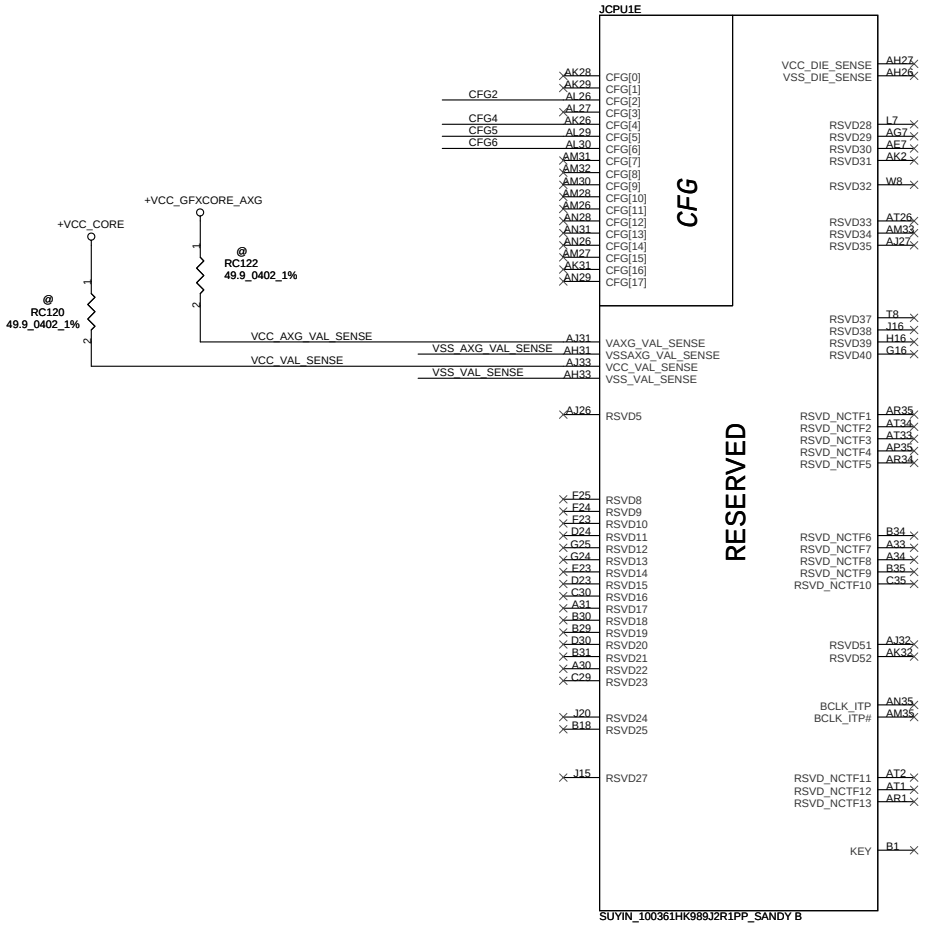
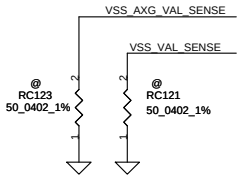
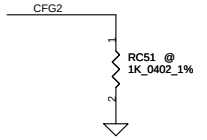


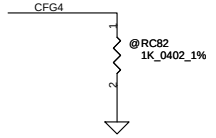


INTEL 12/28 recommand
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1

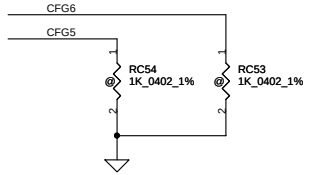
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Compal Electronics, Inc.			
Title: PROCESSOR(4/6) RSVD,CFG			
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POWER

JCPU1F

+VCC_CORE

94A

CORE SUPPLY

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AE35	VCC11
AE34	VCC12
AE33	VCC13
AE32	VCC14
AE31	VCC15
AE30	VCC16
AE29	VCC17
AE28	VCC18
AE27	VCC19
AE26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

8.5A

+VCCP

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

+VCCP

CC49 0.1U_0402_16V7K-N

RC60 75_0402_5%

RC61 43_0402_1%

H_CPU_SVIDCLK — RC56 0_0402_5% — VR_SVID_CLK 44

Place the PU resistors close to CPU

VIDALERT#	AJ29	H_CPU_SVIDALRT#
VIDSCLK	AJ30	H_CPU_SVIDCLK
VIDSOUT	AJ28	H_CPU_SVIDDAT

VR_SVID_ALRT# 44

+VCCP

Place the PU resistors close to CPU

RC63 130_0402_1%

CC50 0.1U_0402_16V7K-N

H_CPU_SVIDDAT — RC65 0_0402_5% — VR_SVID_DAT 44

SENSE LINES

+VCC_CORE

RC66 100_0402_1%

VCC_SENSE	AJ35	VCCSENSE 44
VSS_SENSE	AJ34	VSSSENSE 44

RC96 10_0402_1% — +VCCP

VCCIO_SENSE	B10	VCCIO_SENSE 41
VSS_SENSE_VCCIO	A10	VSSIO_SENSE 41

RC70 100_0402_1%

RC97 10_0402_1%

RC66, RC70 near to JCPU1

SUYIN_100361HK989J2R1PP_SANDY B

CONN@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

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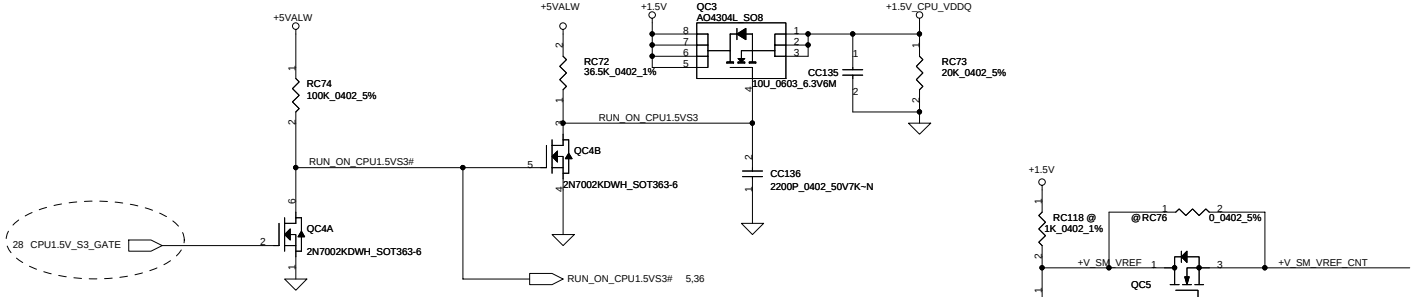
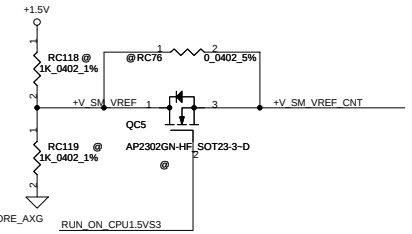
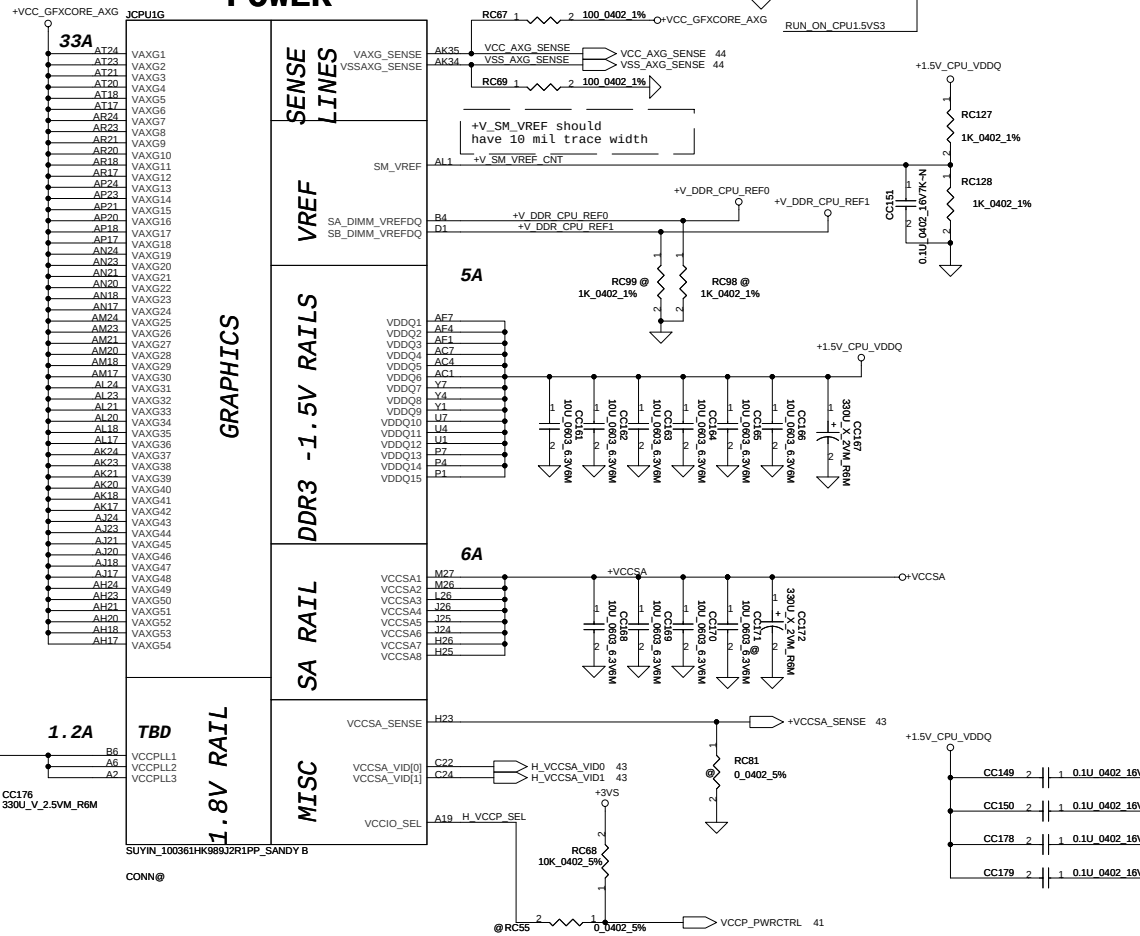
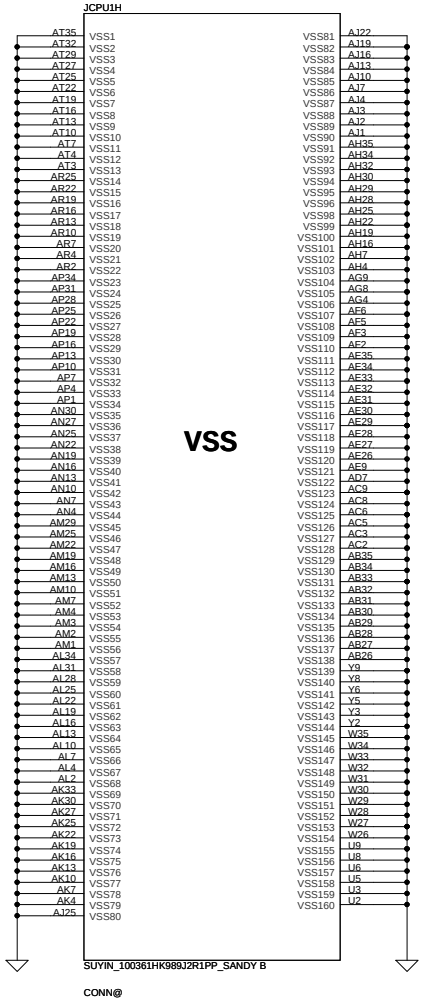
+1.5V_CPU_VDDQ Source 5A

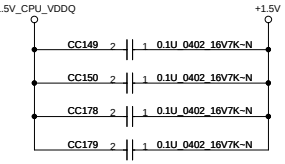




POWER







IVY Bridge drives VCCSA_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

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Compal Electronics, Inc.

Title: **PROCESSOR(6/6) PWR,VSS**

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3.56A

JDIMMA H=5.2

6 DDR_A_DQS#[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_D[0..63]
6 DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

JDIMM1

CONN@

Close to pin200, 202
CD48,CD47 close to PIN200,202

M3 circuit

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Compal Electronics, Inc.

Title: **DDRIII DIMMA**

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JDIMMB H=9.2

3.56A

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM2

Layout Note: Place near JDIMM2.203,204

M3 circuit

CD49,CD50 close to PIN200,202

JDIMM2

CONN@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDRIII DIMMB

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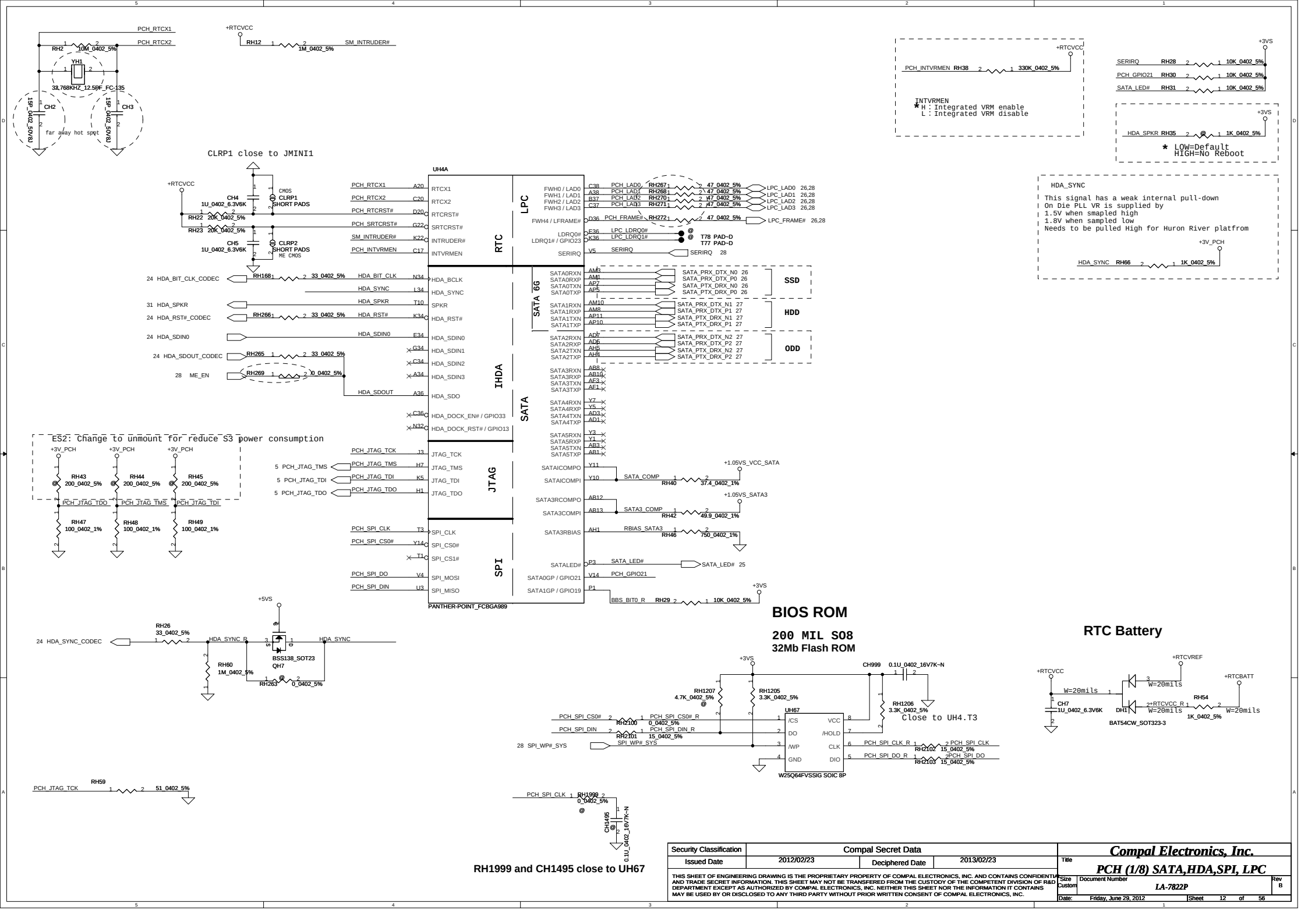

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Compal Electronics, Inc.			
Title: PCH (1/8) SATA,HDA,SPI, LPC			
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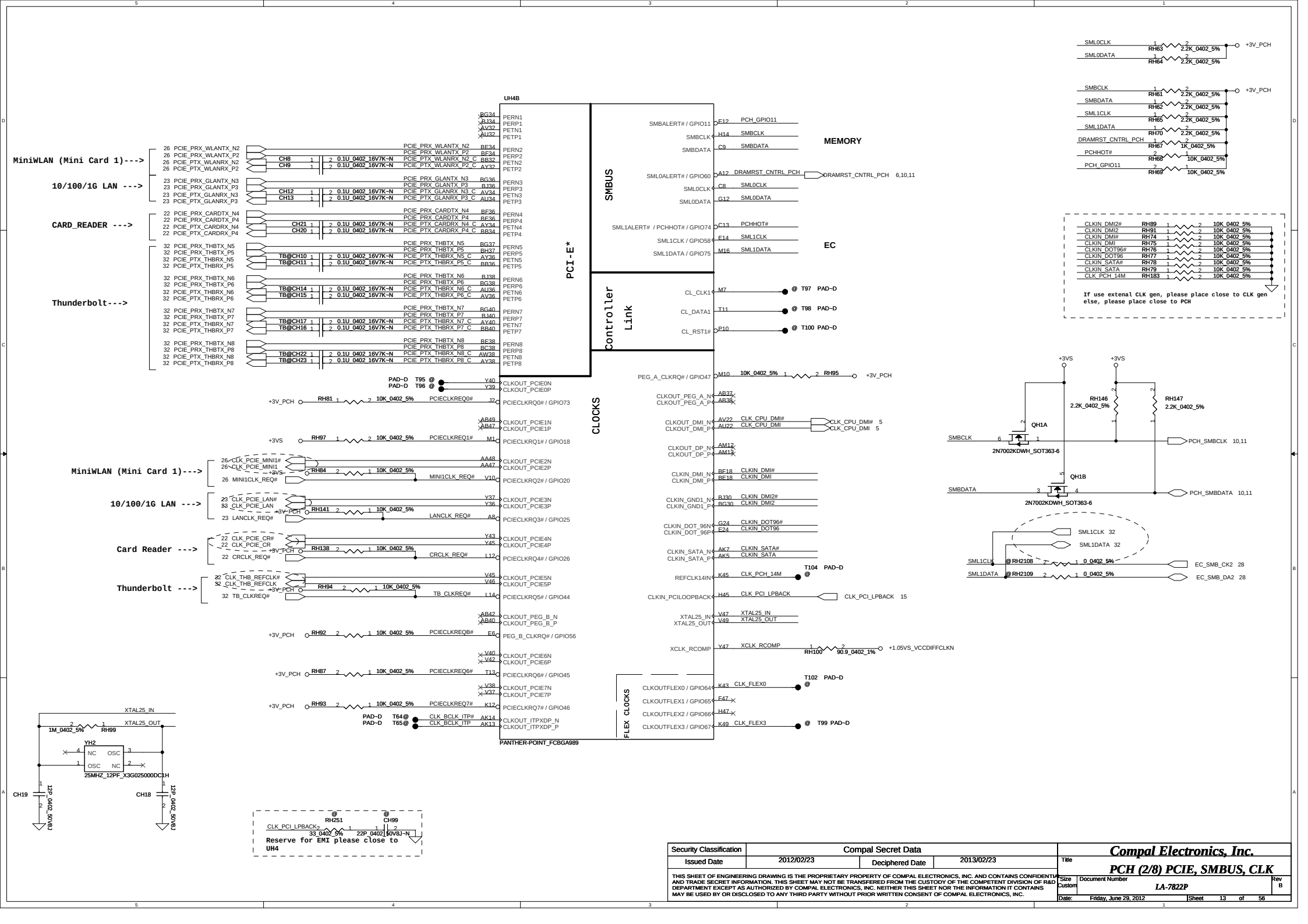

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Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
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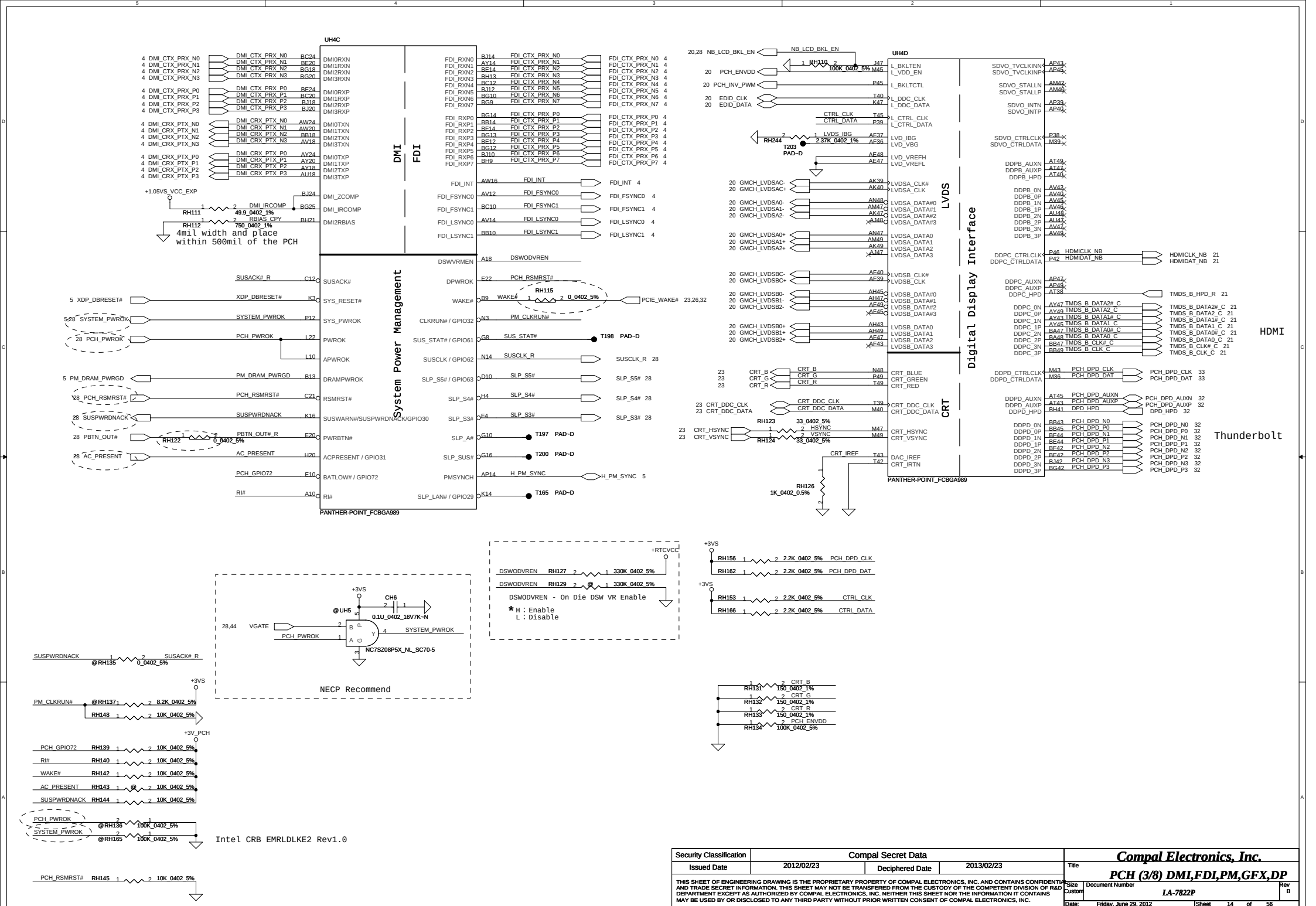

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
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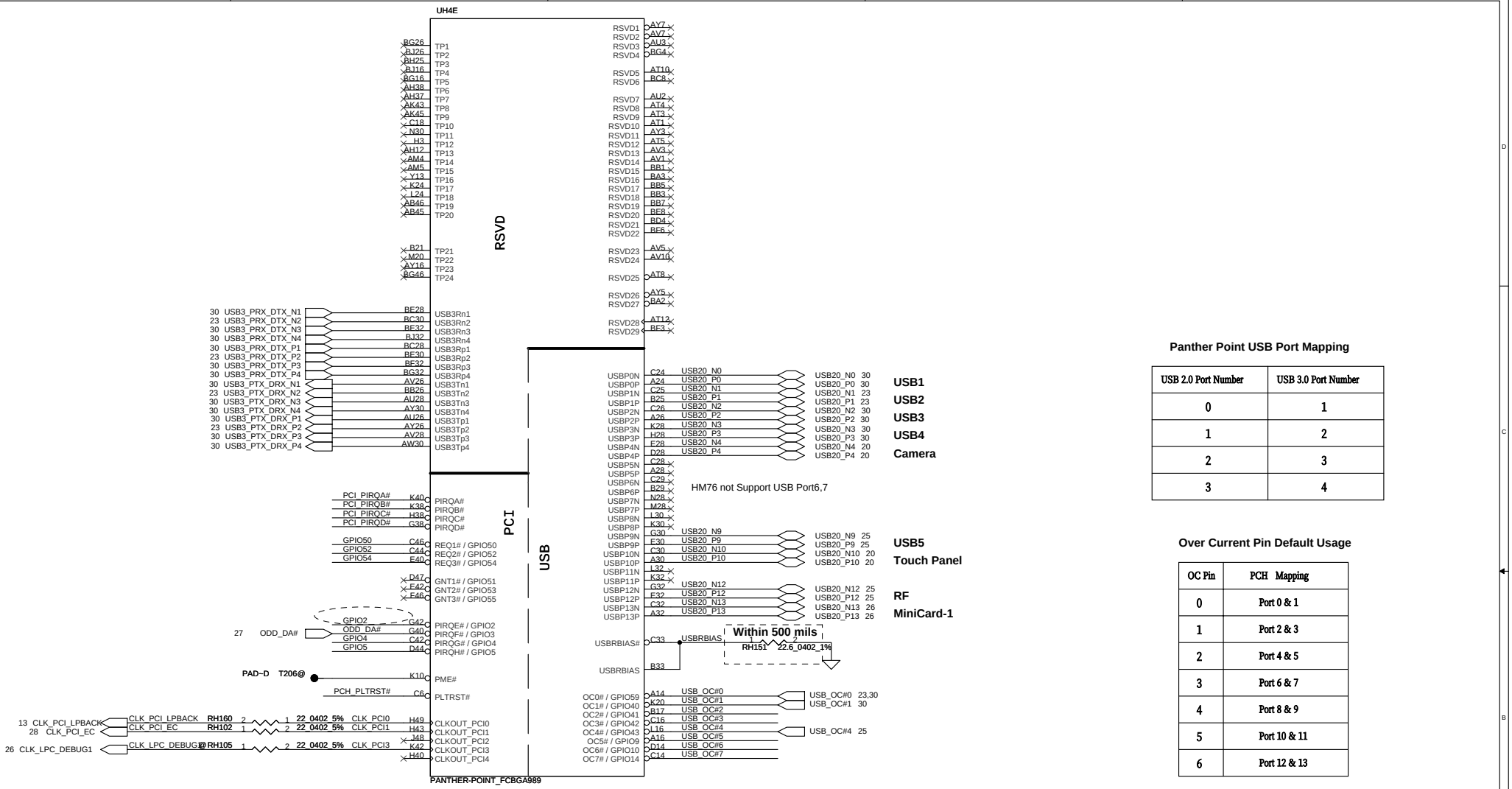
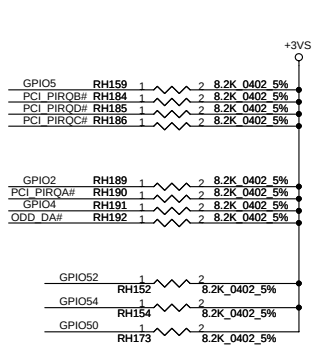


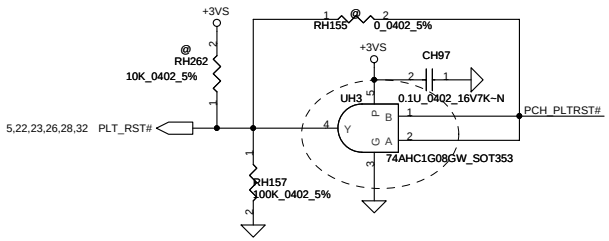
Panther Point USB Port Mapping

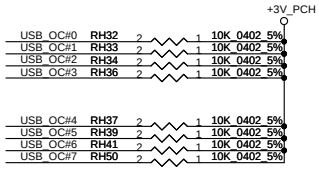
USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13







Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	PCH (4/8) PCI, USB, NVRAM
Size: Custom	Document Number: LA-7822P
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GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

@RH238 1K_0402_5% PCH_GPIO28

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE

* LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

RH174 100K_0402_5% PCH_GPIO37

NECP Recommend

PCH_GPIO27 Intel HR_SCH_CHKLST_Rev1.2

@RH241 10K_0402_5% PCH_GPIO27

UH4F

GPIO

32 TB_PLUG_EVENT	TB_PLUG_EVENT	T7	BMBUSY# / GPIO0		
	PCH_GPIO1	A42	TACH1 / GPIO1		
	PCH_GPIO6	H36	TACH2 / GPIO6		
28 EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7		
28 EC_SMI#	EC_SMI#	C10	GPIO8		
	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12		
28 EC_LID_OUT#	EC_LID_OUT#	G2	GPIO15		
	PCH_GPIO16	U2	SATA4GP / GPIO16		
32 TB_FORCE_PWR	TB_FORCE_PWR	D40	TACH0 / GPIO17		
	PCH_GPIO22	T5	SCLOCK / GPIO22		
		E8	GPIO24		
	PCH_GPIO27	E16	GPIO27		
	PCH_GPIO28	P8	GPIO28		
	STP_PCI#	K1	STP_PCI# / GPIO34		
PAD~D T195@	PCH_GPIO35	K4	GPIO35		
27 ODD_DETECT#	ODD_DETECT#	V8	SATA2GP / GPIO36		
	PCH_GPIO37	M5	SATA3GP / GPIO37		
	PCH_GPIO38	N2	SLOAD / GPIO38		
	PCH_GPIO39	M3	SDATAOUT0 / GPIO39		
	PCH_GPIO48	V13	SDATAOUT1 / GPIO48		
	PCH_GPIO49	V3	SATA5GP / GPIO49 / TEMP_ALERT#		
	PCH_GPIO57	D6	GPIO57		

CPU/MISC

			TACH4 / GPIO68	C40	ODD_EN# → ODD_EN# 27
			TACH5 / GPIO69	B41	LAN_LOW_PWR
			TACH6 / GPIO70	C41	
			TACH7 / GPIO71	A40	
			A20GATE	P4	→ GATEA20 28
			PECI	AU16	PCH_PECI_R → @T142 PAD~D
			RCIN#	P5	KB_RST# → KB_RST# 28
			PROCPWRGD	AY11	→ H_CPUPWRGD 5
			THRMTRIP#	AY10	H_THERMTRIP#_R — 390_0402_5% — RH161 — H_THERMTRIP# → H_THRMTRIP# 5
			INIT3_3V#	T14	
			DF_TVS	AY1	DF_TVS
			TS_VSS1	AH8	
			TS_VSS2	AK11	
			TS_VSS3	AH10	
			TS_VSS4	AK10	
			NC_1	P37	@T141 PAD~D

NCTF

		A4	VSS_NCTF_1		
		A44	VSS_NCTF_2		
		A45	VSS_NCTF_3		
		A46	VSS_NCTF_4		
		A5	VSS_NCTF_5		
		A6	VSS_NCTF_6		
		B3	VSS_NCTF_7		
		B47	VSS_NCTF_8		
		BD1	VSS_NCTF_9		
		BD49	VSS_NCTF_10		
		BE1	VSS_NCTF_11		
		BE49	VSS_NCTF_12		
		BF1	VSS_NCTF_13		
		BF49	VSS_NCTF_14		
			VSS_NCTF_15	BG2	
			VSS_NCTF_16	BG48	
			VSS_NCTF_17	BH3	
			VSS_NCTF_18	BH47	
			VSS_NCTF_19	BJ4	
			VSS_NCTF_20	BJ44	
			VSS_NCTF_21	BJ45	
			VSS_NCTF_22	BJ46	
			VSS_NCTF_23	BJ5	
			VSS_NCTF_24	BJ6	
			VSS_NCTF_25	C2	
			VSS_NCTF_26	C48	
			VSS_NCTF_27	D1	
			VSS_NCTF_28	D49	
			VSS_NCTF_29	E1	
			VSS_NCTF_30	E49	
			VSS_NCTF_31	F1	
			VSS_NCTF_32	F49	

PANTHER-POINT_FCBGA989

+3VS — RH158 10K_0402_5% — GATEA20

+1.8VS — RH149 2.2K_0402_5% — DF_TVS — 1K_0402_5% — RH150 — H_SNB_IVB# 5

CLOSE TO THE BRANCHING POINT

+3VS

LAN_LOW_PWR	RH178	4.7K_0402_5%
ODD_EN#	RH176	10K_0402_5%
PCH_GPIO1	@ RH163	10K_0402_5%
TB_PLUG_EVENT	@ RH232	10K_0402_5%
PCH_GPIO6	RH164	10K_0402_5%
PCH_GPIO38	RH182	10K_0402_5%
PCH_GPIO39	RH167	10K_0402_5%
TB_FORCE_PWR	RH172	10K_0402_5%

+3V_PCH

PCH_GPIO28	RH169	10K_0402_5%
PCH_GPIO57	RH170	10K_0402_5%
PCH_GPIO12	RH177	1K_0402_5%
EC_SMI#	RH71	10K_0402_5%
EC_LID_OUT#	RH72	10K_0402_5%

+3VS

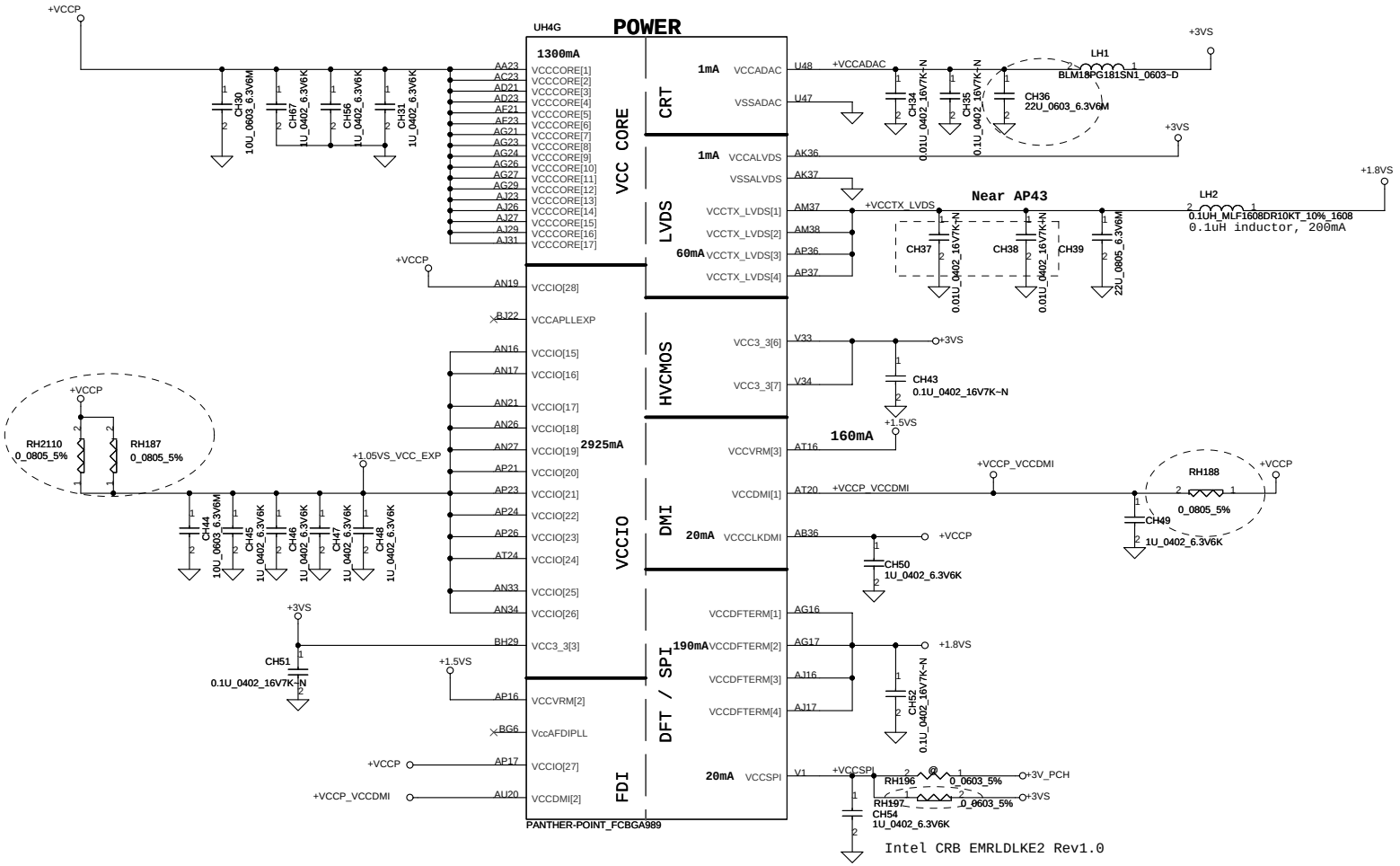
ODD_DETECT#	RH171	200K_0402_1%
PCH_GPIO16	RH249	10K_0402_5%
STP_PCI#	RH180	10K_0402_5%
KB_RST#	RH203	10K_0402_5%
PCH_GPIO48	RH175	10K_0402_5%
PCH_GPIO22	RH179	10K_0402_5%
PCH_GPIO49	RH181	10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: Custom	Document Number: LA-7822P	Rev: B
Date: Friday, June 29, 2012	Sheet 16 of 56	



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04
DcpSus	1.05	0.12

Compal Electronics, Inc.

Title: PCH (6/8) PWR

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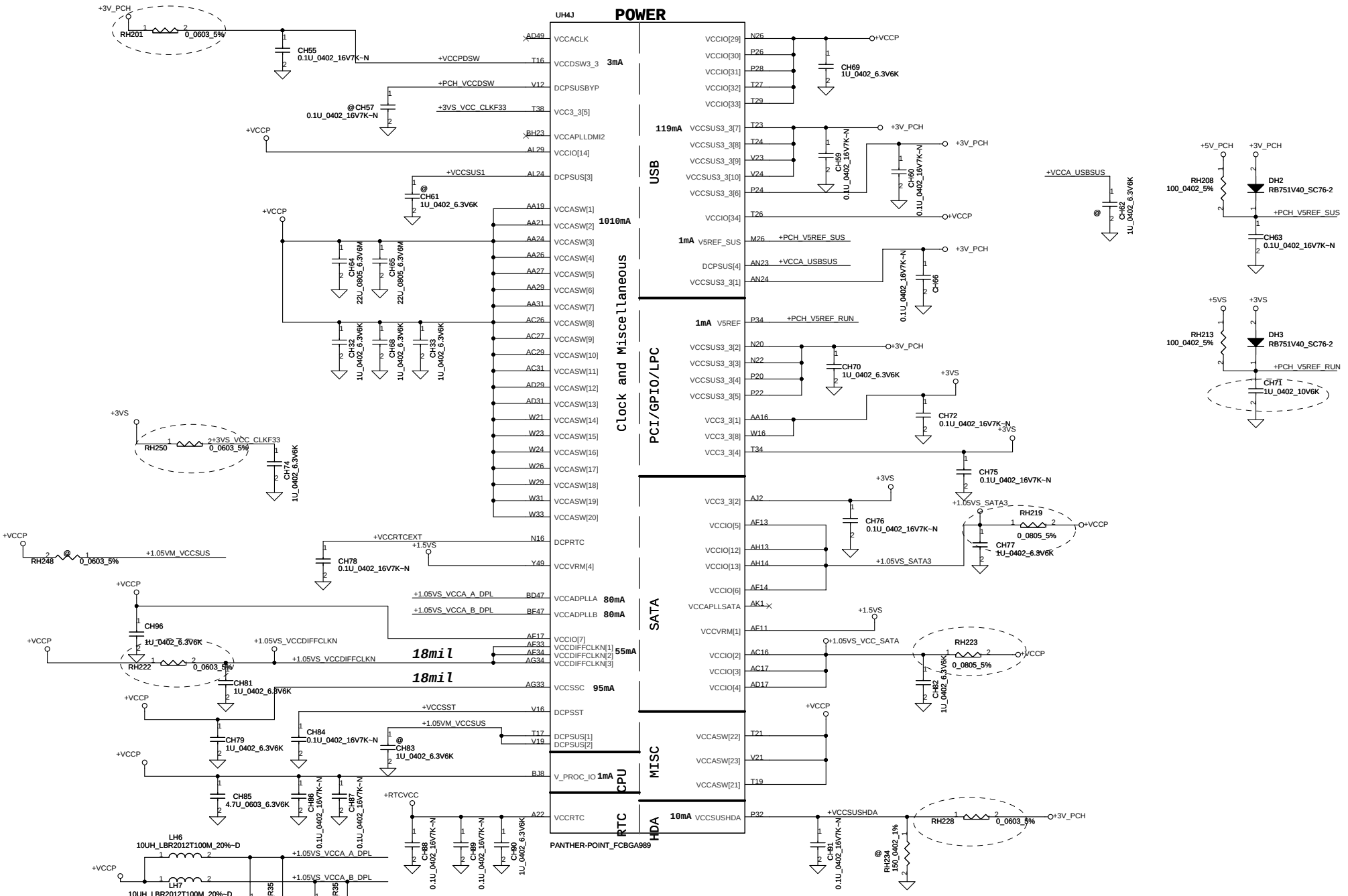
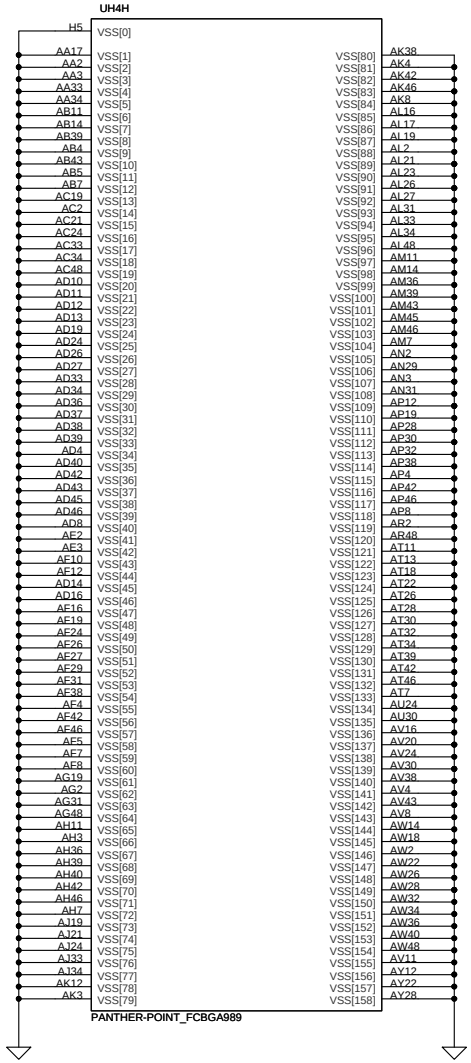
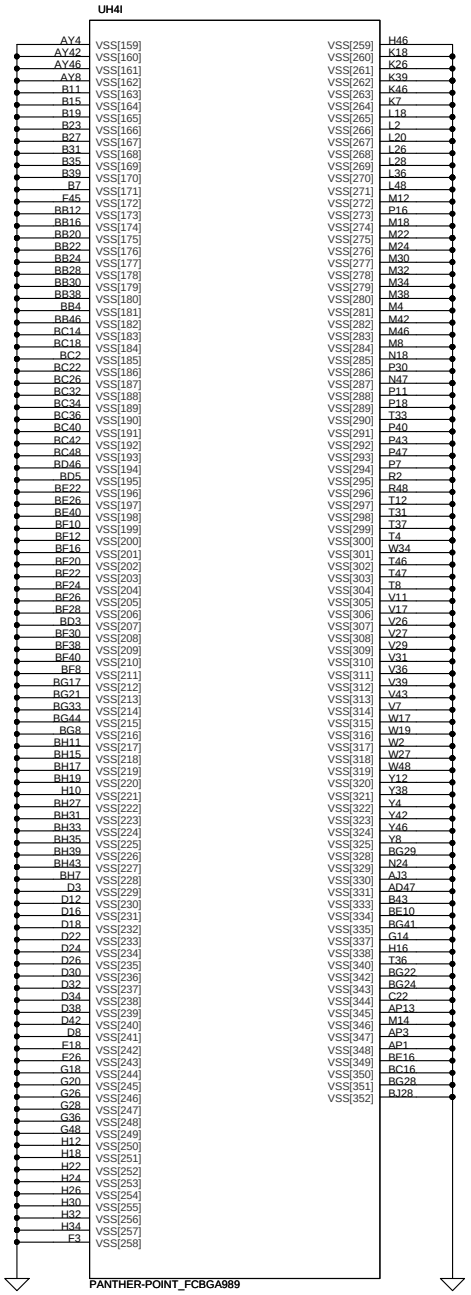


Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.		
Title: PCH (7/8) PWR		
Size: Custom	Document Number: LA-7822P	Rev: B
Date: Friday, June 29, 2012	Sheet 18 of 56	





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Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

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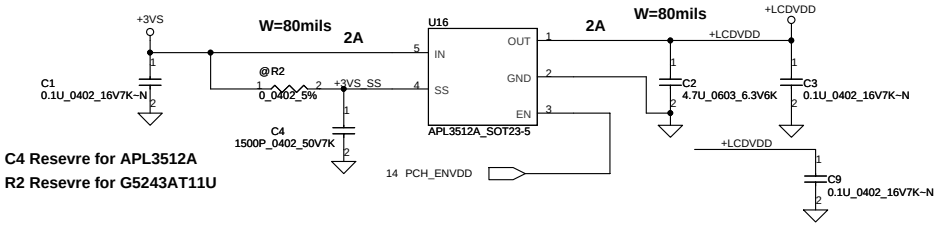
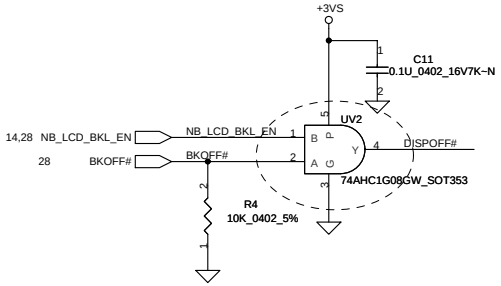
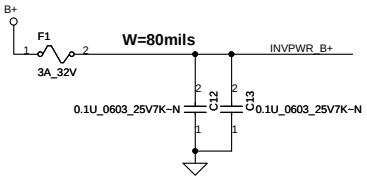
L C D

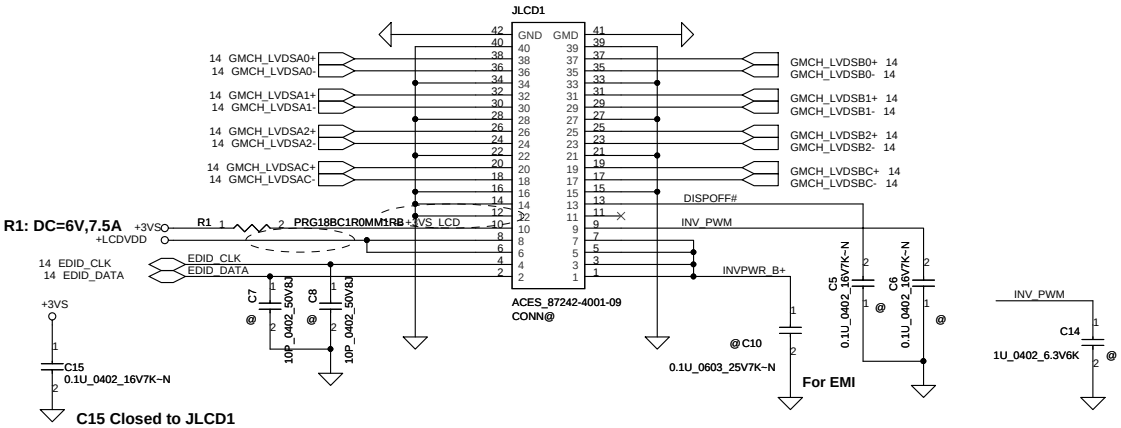
LCD POWER CIRCUIT

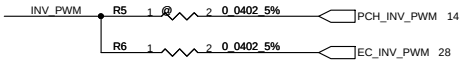


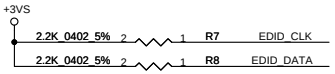
C4 Resevre for APL3512A
R2 Resevre for G5243AT11U



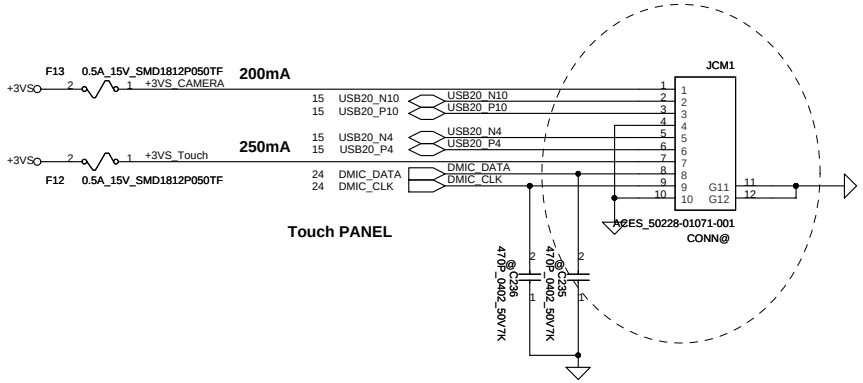


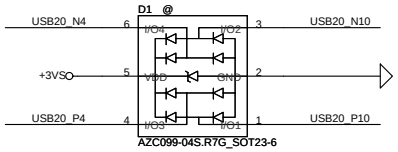






CAMERA





ESD

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: LCD Conn

Size: Custom | Document Number: LA-7822P | Rev: B

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EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommanded)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB

0824 EMI requirement

Follow Intel Feedback putting 2.2K ohm

FOR EMI

ASM1442 QFN 48P

2N7002KW 1N SOT323-3

100mA

Co-lay for EMI

ACM2012H-900-2P-T00_4P

HDMI Connector

2009/07 Modify

JHDMI1

TAITW_PDVBR9-19FLBS4NN4N1

CONN@

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: HDMI LS & Conn.

Size	Document Number	Rev
Custom	LA-7822P	B

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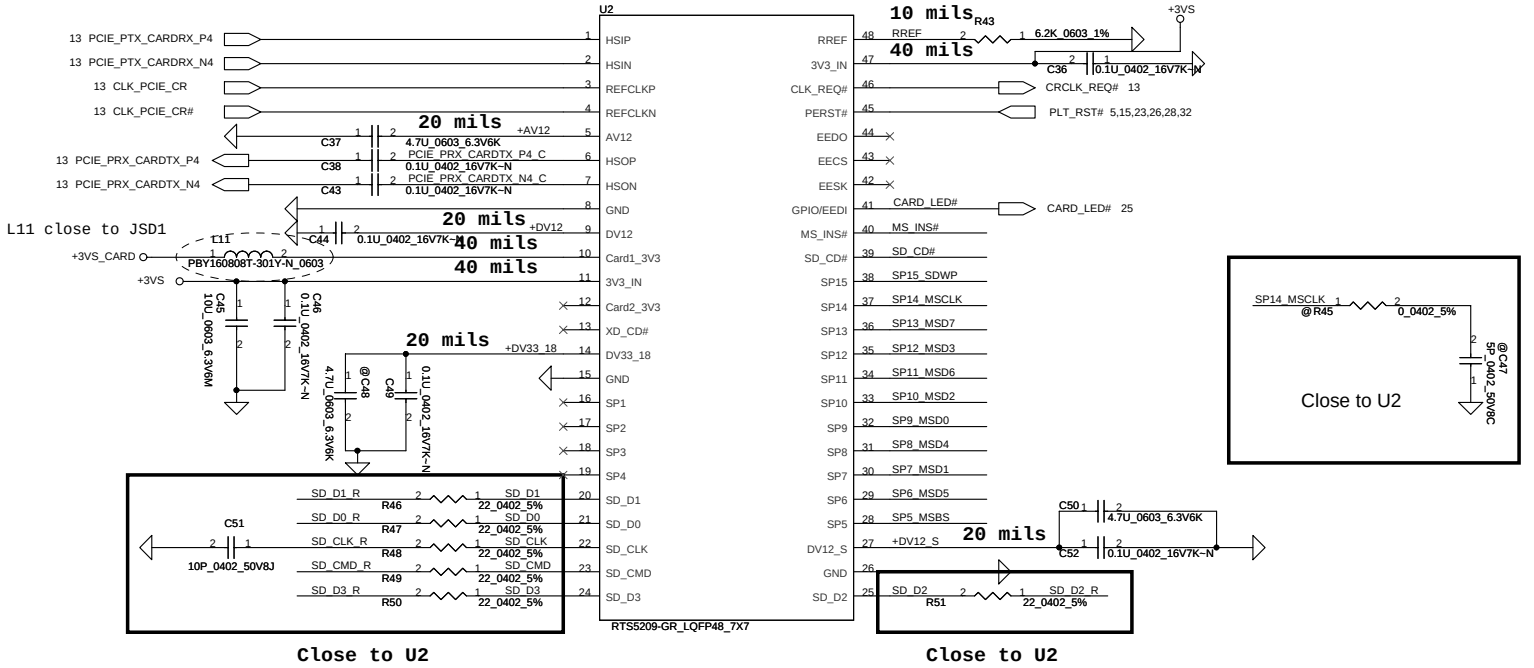
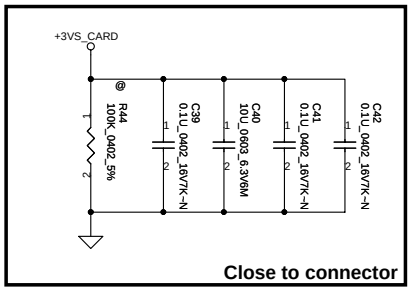
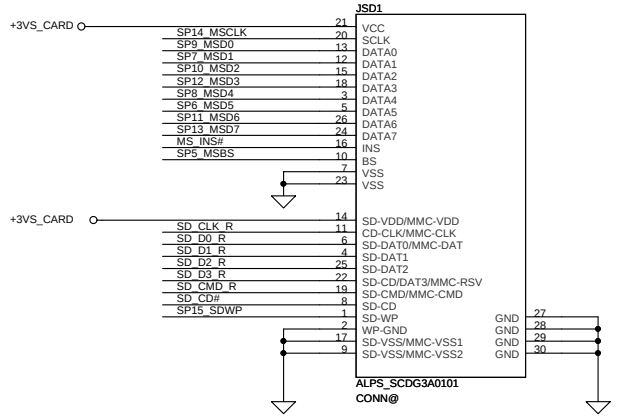
Card Reader







Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.			
Title: RTS5209 LQFP_Card RD			
Size: Custom	Document Number: LA-7822P		Rev: B
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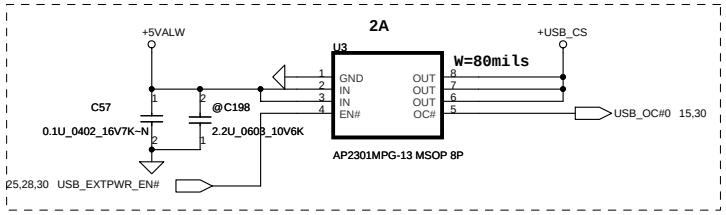
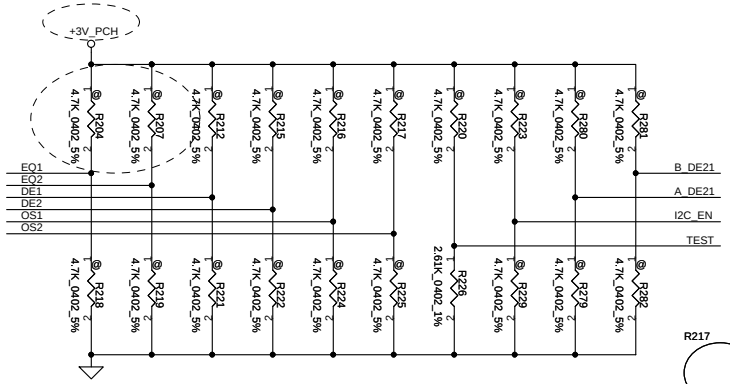
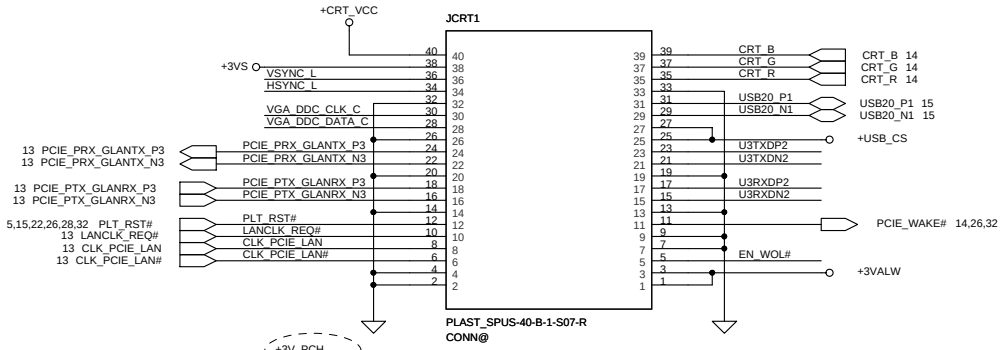
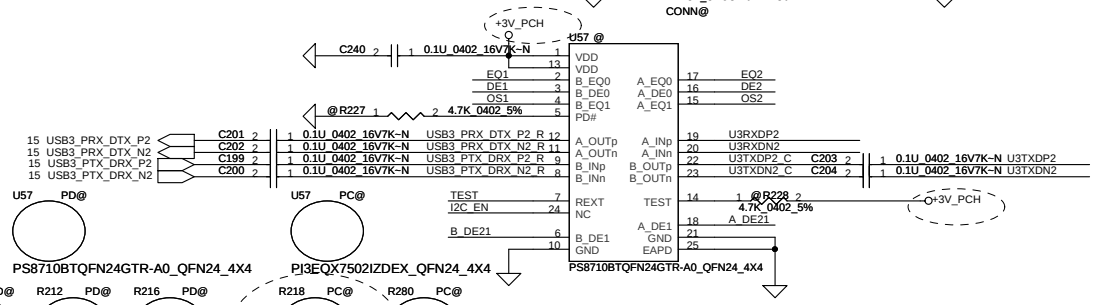
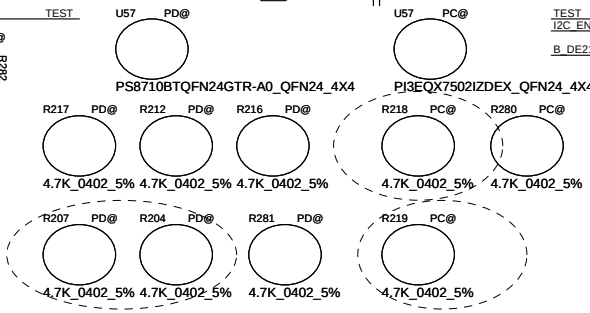
LAN / CRT CONN



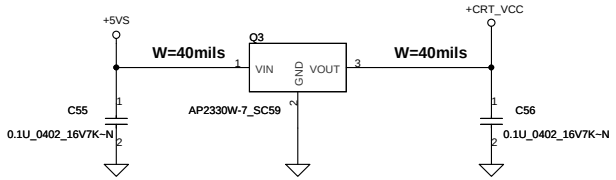






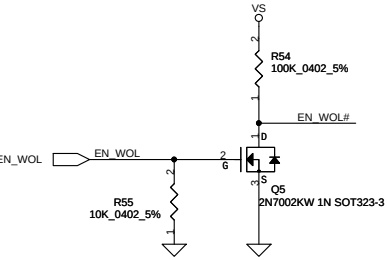


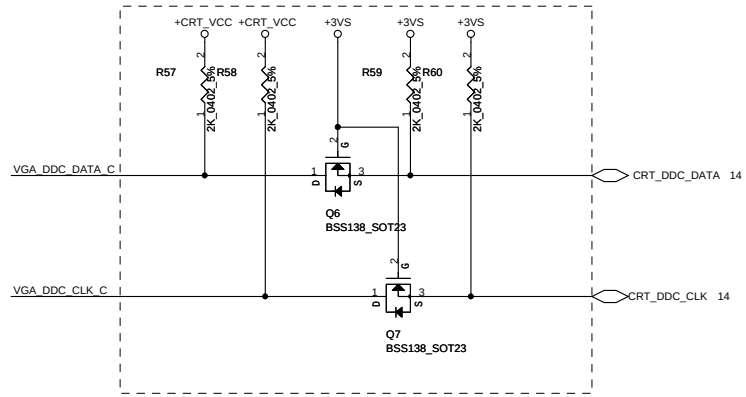
Parade	B channel Port2 (TX)	A channel Port2 (RX)
DE	5 dB B_DE1 / B_DE0 (H H)	3.5 dB A_DE1 / A_DE0 (L L)
EQ	11.5 dB B_EQ1 / B_EQ0 (H H)	11.5 dB A_EQ1 / A_EQ0 (H H)

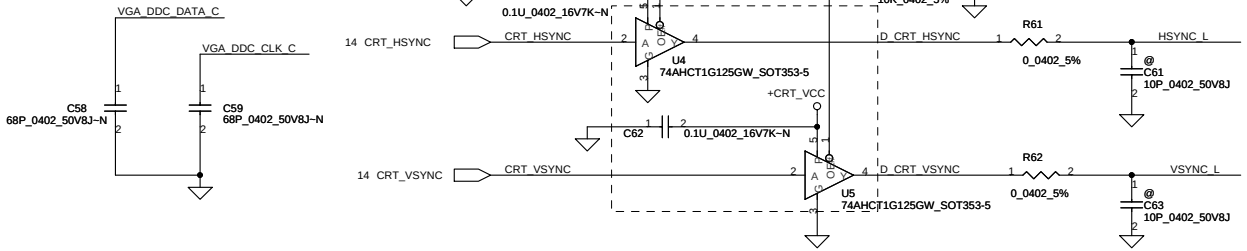


	R212	R216	R280	R281	R218	R219	R204	R207
PD@	4.7K	4.7K	@	4.7K	@	@	4.7K	4.7K
PC@	@	@	4.7K	@	4.7K	4.7K	@	@

Pericom	B channel Port2 (TX)	A channel Port2 (RX)
DE	-3.5 dB B_DE0 (open)	-3.5 dB A_DE0 (open)
EQ	3 dB B_EQ0 (0)	3 dB A_EQ0 (0)







Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: LAN / CRT CONN

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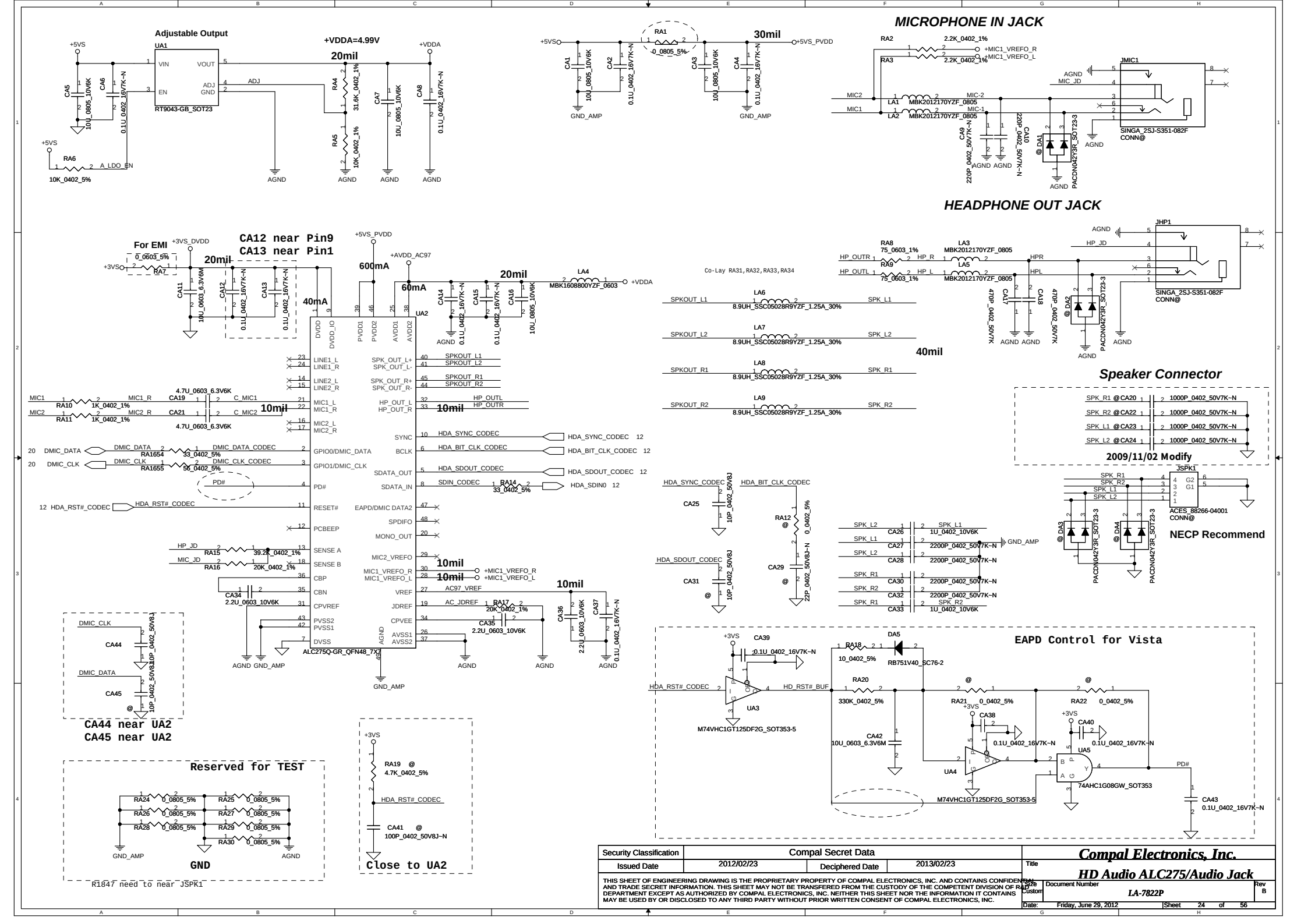
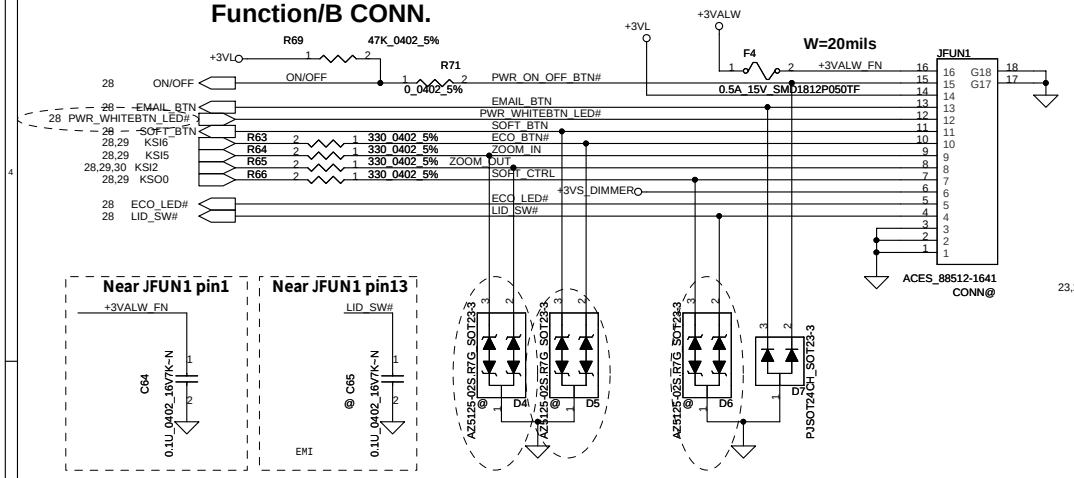
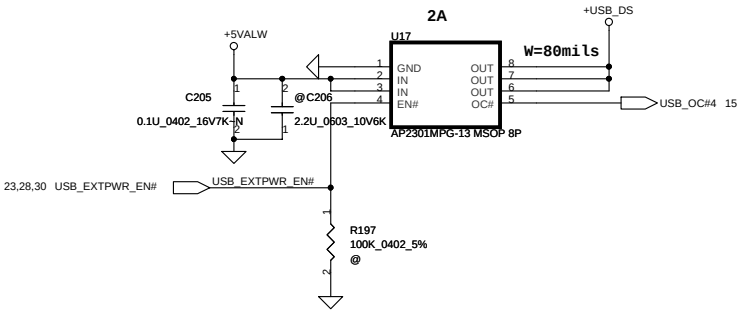
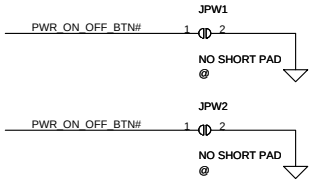

Adjustable Output
UA1
RT9043-GB_SOT23
+VDDA=4.99V
20mil
30mil
RA1
0_0805_5%
MICROPHONE IN JACK
JMIC1
SINGA_2SJ-S351-082F
CONN@
HEADPHONE OUT JACK
JHP1
SINGA_2SJ-S351-082F
CONN@
Speaker Connector
2009/11/02 Modify
JSPK1
ACES_88266-04001
CONN@
NECP Recommend
For EMI
CA12 near Pin9
CA13 near Pin1
600mA
60mA
40mA
20mil
10mil
40mil
Co-Lay RA31,RA32,RA33,RA34
ALC275Q-GR_QFN48_7X7
CA44 near UA2
CA45 near UA2
EAPD Control for Vista
Reserved for TEST
GND
R1847 need to near JSPK1
Close to UA2
Security Classification
Compal Secret Data
Issued Date
2012/02/23
Deciphered Date
2013/02/23
Compal Electronics, Inc.
HD Audio ALC275/Audio Jack
LA-7822P
Rev B
Friday, June 29, 2012
Sheet 24 of 56

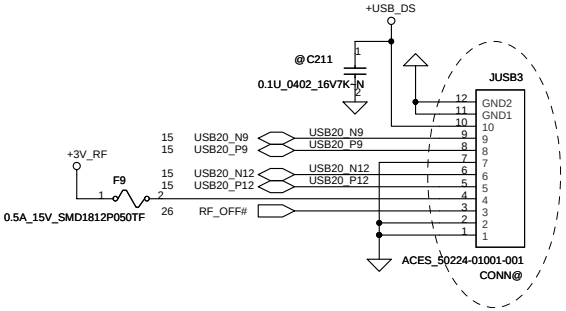
Function/B CONN.



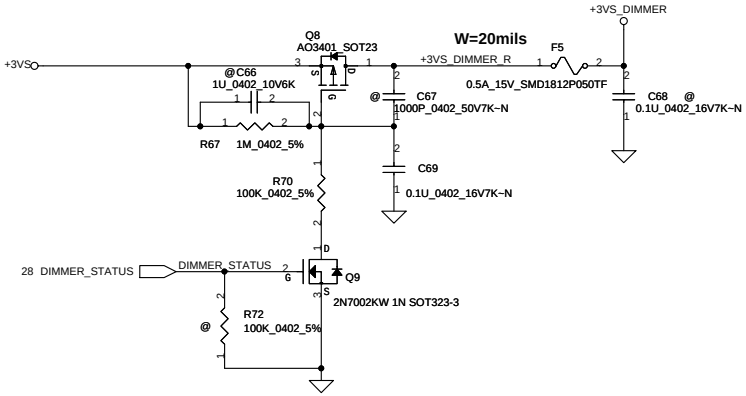
USB2.0/B CONN.

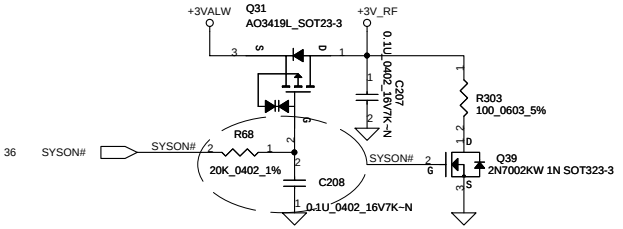


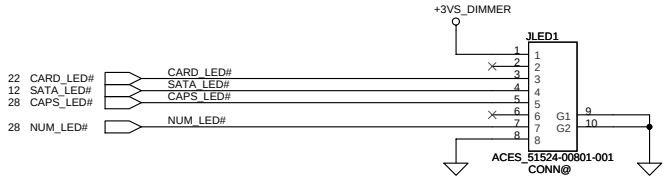




LED Circuit







Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.	
Title	PWR_OK/FN_B/LED
Size: Custom	Document Number: LA-7822P
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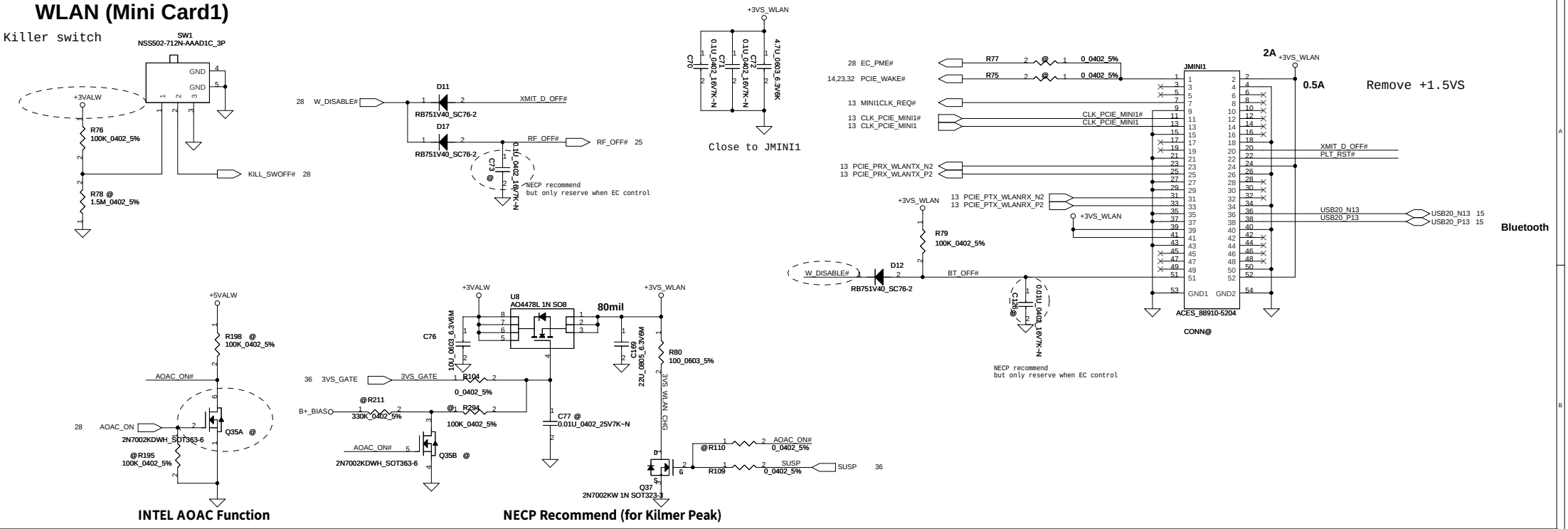
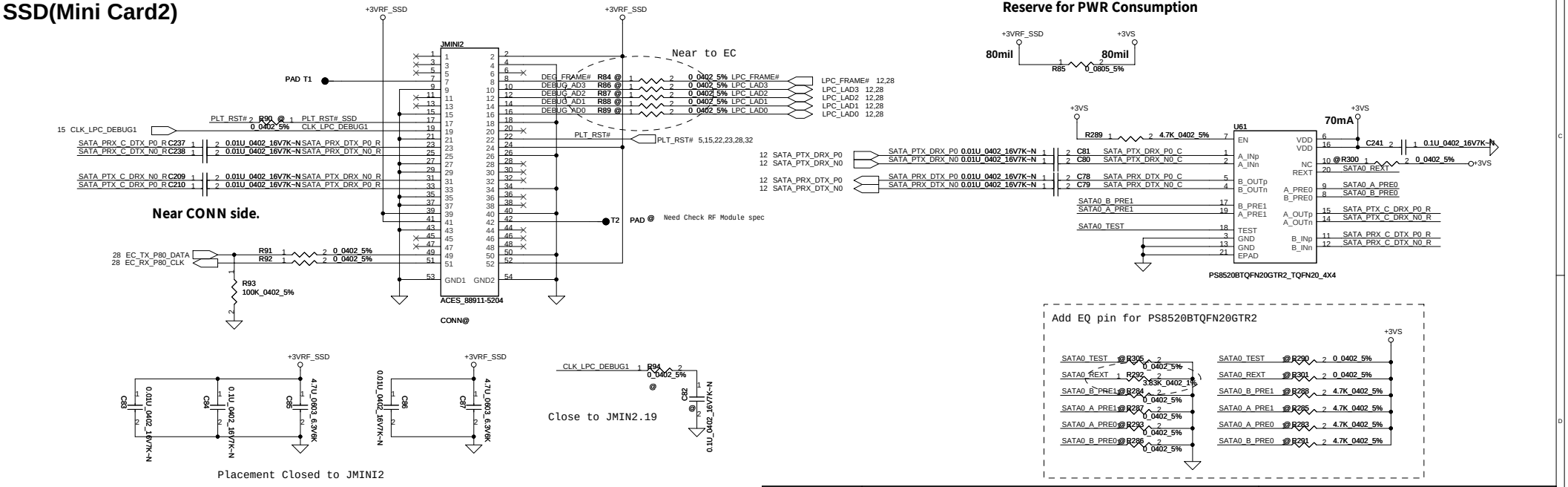
WLAN (Mini Card1)



SSD(Mini Card2)



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Compal Electronics, Inc.			
Title	WLAN/SSD		
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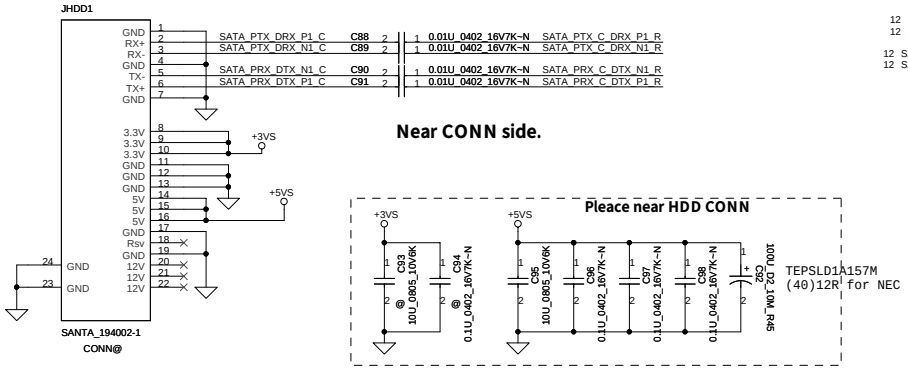
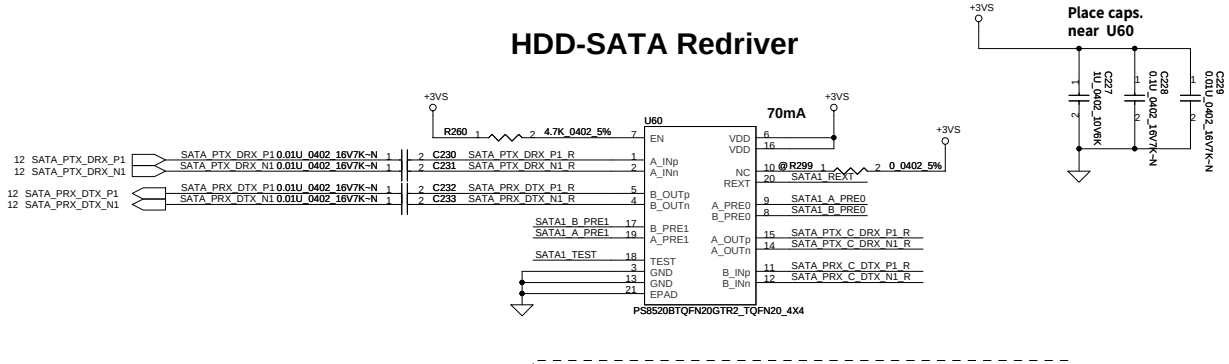
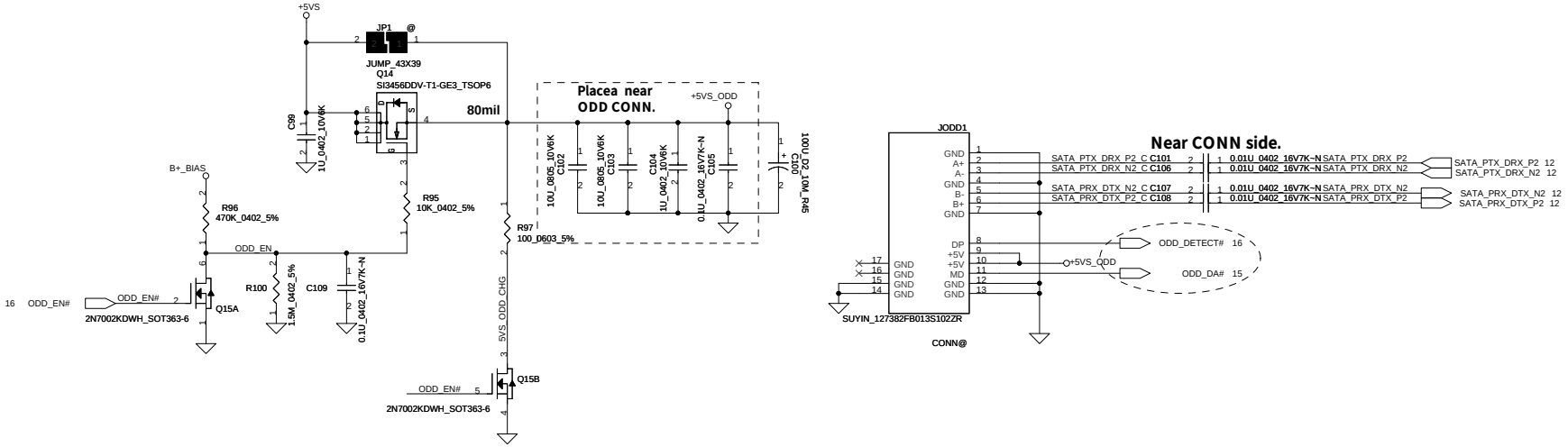
SATA HDD CONN.



HDD-SATA Redriver



SATA ODD CONN.



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Title: **HDD/ODD**

Size	Document Number	Rev
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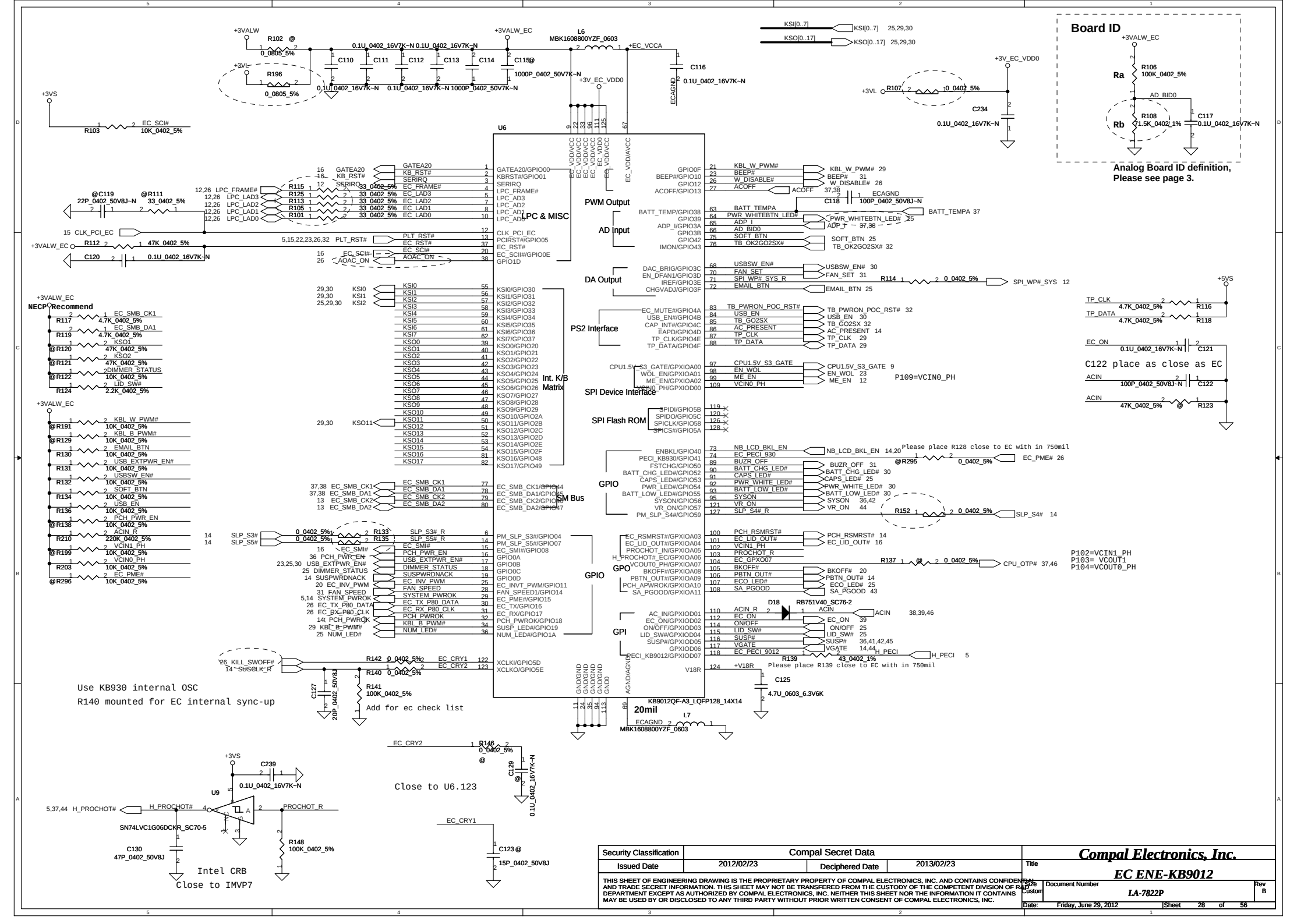
Board ID
Analog Board ID definition,
Please see page 3.
U6
KB9012QF-A3_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
NECP Recommend
Use KB930 internal OSC
R140 mounted for EC internal sync-up
Add for ec check list
20mil
Close to U6.123
Close to IMVP7
Intel CRB
SN74LVC1G06DCKR_SC70-5
Please place R128 close to EC with in 750mil
Please place R139 close to EC with in 750mil
C122 place as close as EC
P102=VCIN1_PH
P103= VCOUT1
P104=VCOUT0_PH
P109=VCIN0_PH
Security Classification
Compal Secret Data
Issued Date
2012/02/23
Deciphered Date
2013/02/23
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EC ENE-KB9012
Size
Custom
Document Number
LA-7822P
Rev
B
Date:
Friday, June 29, 2012
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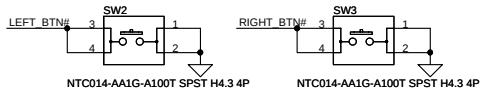
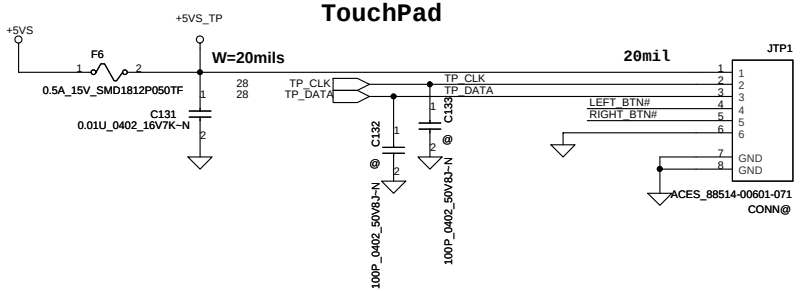
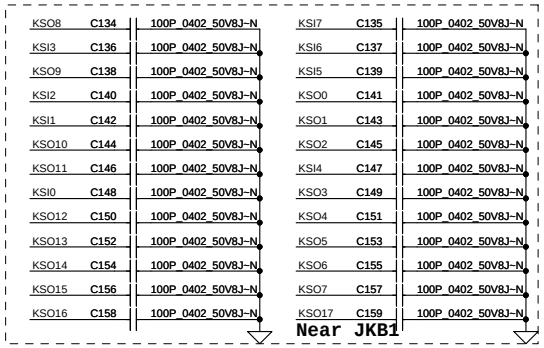
28
of
56

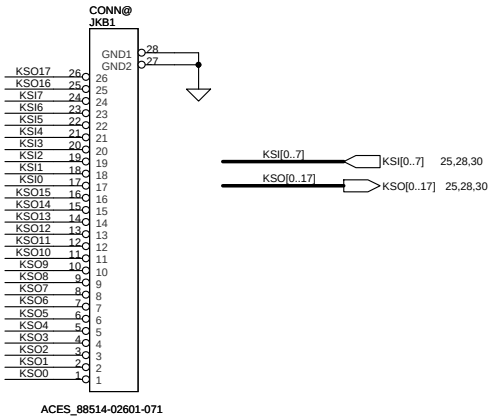


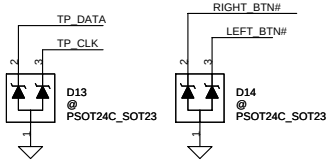
TouchPad



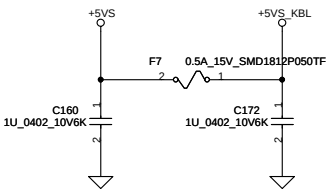
INT_KBD CONN.



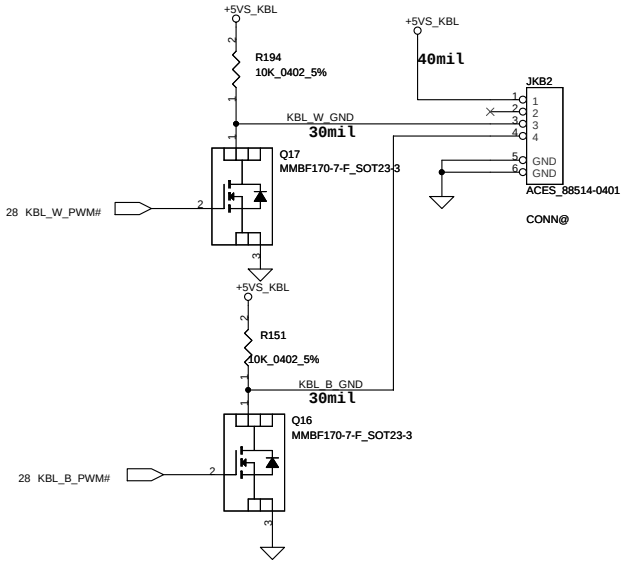




KB BackLight Control



NECP Recommend



Compal Electronics, Inc.		
Title: KB/TP/KC3810		
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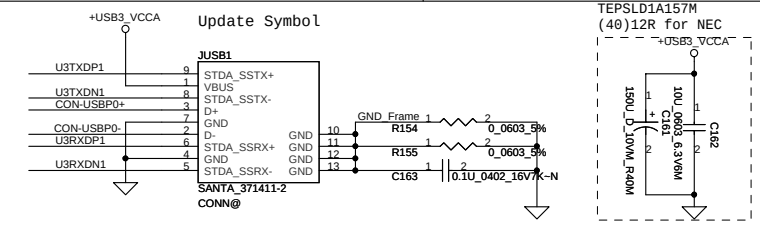
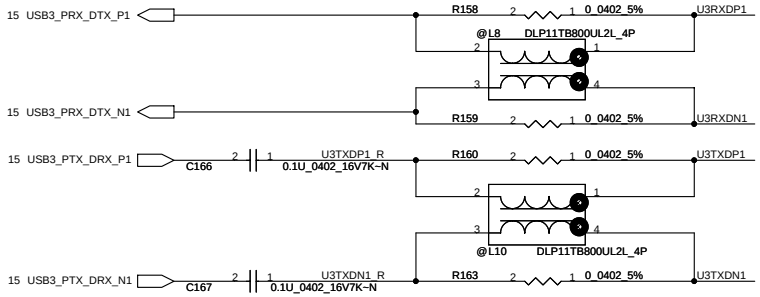
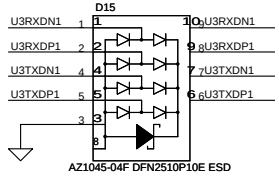
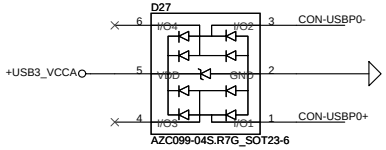
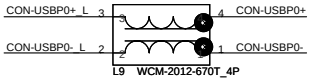
IPOD USB PWR SW



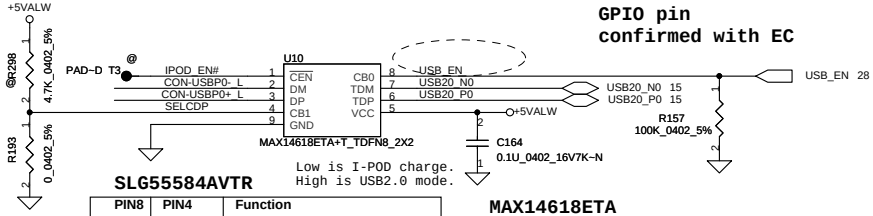








0821 EMI requirement



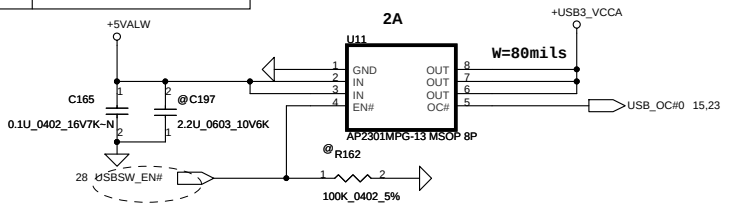
GPIO pin
confirmed with EC

SLG55584AVTR

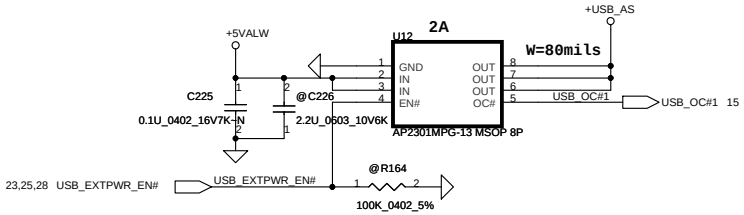
PIN8	PIN4	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

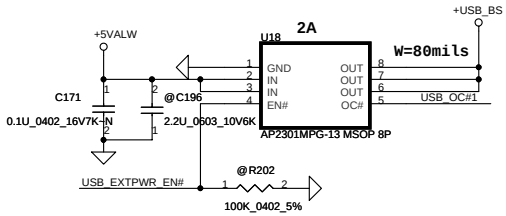
MAX14618ETA

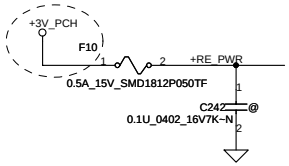
CB0=0	Auto detection charger identification active
CB0=1	Connect DP/DM to TDP/TDM

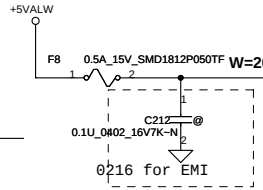


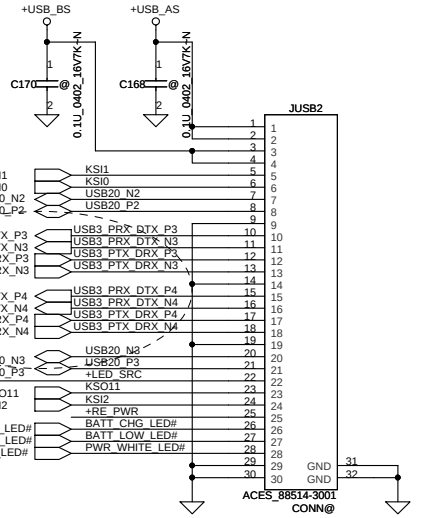
USB Sub Board CONN.











Security Classification	Compal Secret Data		
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Title: USB3.0/iPODcharger/Felica			
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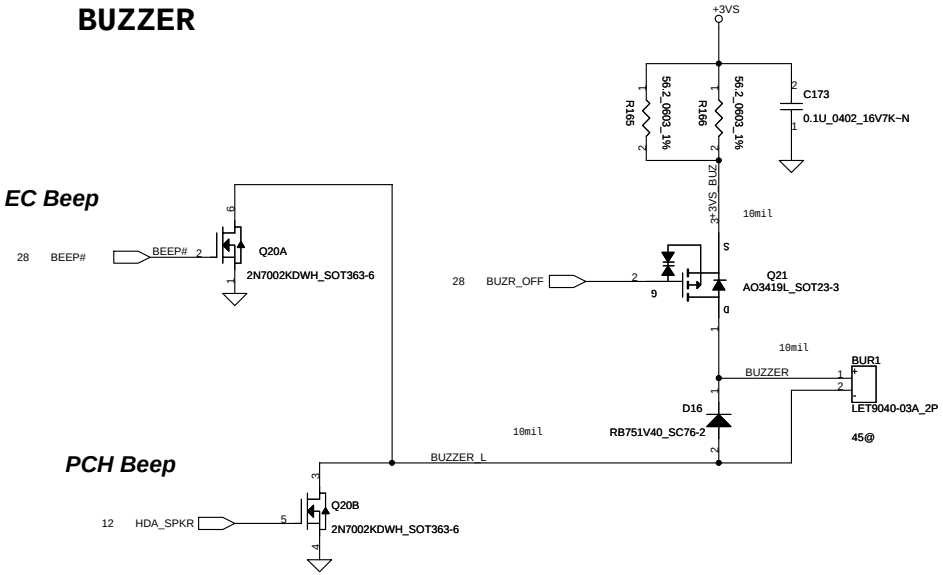
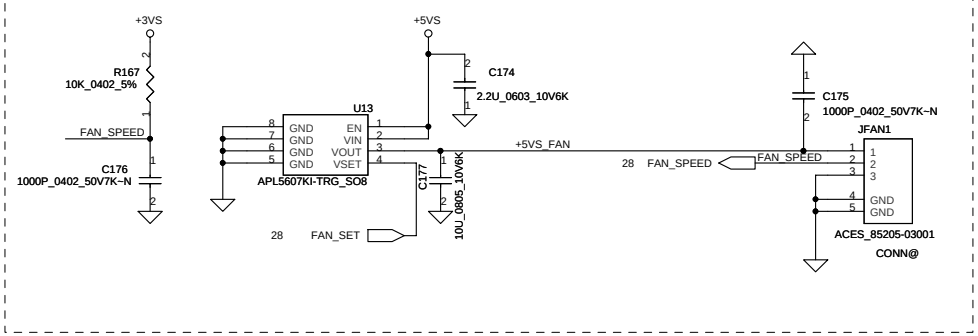
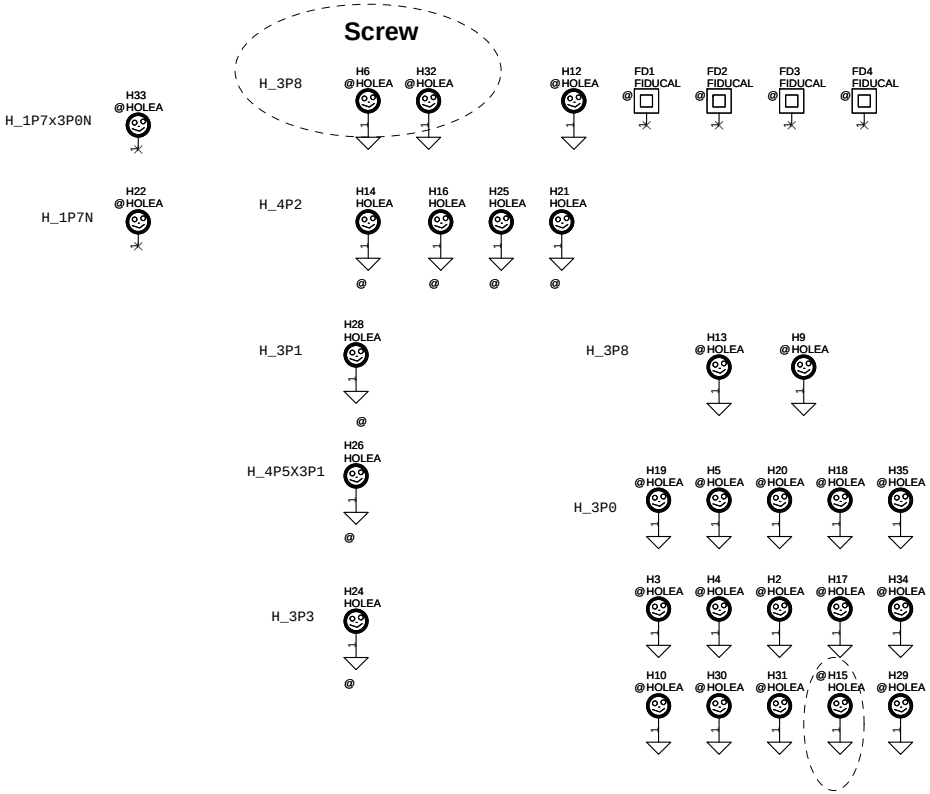
BUZZER



Fan Control Circuit



Screw



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Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: **Buzzer/FAN/Bluetooth/Screw**

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need to check connect to +3VS_LC or +3VS_POC

RT77 and CT120 close to UT2

intra pair skew: 5 mil.
inter pair skew: 10 mil

EEPROM

ATMEL:AT25256B, AT25512
CAT:CAT25256
ST:M95256-W6, M95512-W6
MICROCHIP:25AA256, 25LC256

AT25256B-SSHL-T_SO8

Trigger after SUSP# asserted for 30ms

TB@ CACTUS-RIDGE_FCBGA288

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: Cactus Ridge(1/4) DP / PCIE

Size: Custom | Document Number: LA-7822P | Rev: B

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Function	SEL/HPD_SEL /AUX_SEL
Part A is active	L
Part B is active	H

UT3 TB@ — PI3VEDP212ZLEX_TQFN32_6X3~D

HPD	CFG2	CFG1	LSrx	CableType	Comments
0	X	0	X	NONE	W/O Cable
1	0	0	X	DP	
1	1	X	X	DVI/HDMI	
0	0	1	1	TBT	TBT operation

UT1B — CACTUS-RIDGE_FCBGA288 TB@ — CIO

Route Thunderbolt traces as 85 Ohm control impedance.
Match inside pair 2 mil.
Match between lanes NA
Thunderbolt lenght must be between 0.8 inch to 2 inch

All Thunderbolt TX traces have pi filter when embedded capacitors before and after inductor should be 0.45pF

NECP Recommend — @DT4 L15ESDL5V0NA-4 SLP2510P8; @DT5 L15ESDL5V0NA-4 SLP2510P8

NECP Recommend — @DT8 L15ESDL5V0NA-4 SLP2510P8; @DT6 L15ESDL5V0NA-4 SLP2510P8; DT7 @ AZC199-02SPR7G_SOT23-3

UT6 TB@ — TPS2980RGPR_VQFN20_4X4

2011-11-03 Intel recommend: from TI's IC limitation, need extra resistor to fine tune

PA_CFG1_LSEO0, PA_CFG2_LSOE0 should be used by GPU as the DP CONFIG1/CONFIG2 inputs, if required

mDP CONN — JMDP1 — JAE_DP3R020RU32JQ CONN@

2011-11-03 Intel recommend: JAE connector no need 12.1 ohm in GND of mDP connector

VCC_DP@3V, max current 500mA
VCC_DP@12V, max current 0.8A

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: Cactus Ridge(2/4) HOST /mDP CONN

Size: Custom | Document Number: LA-7822P | Rev: B

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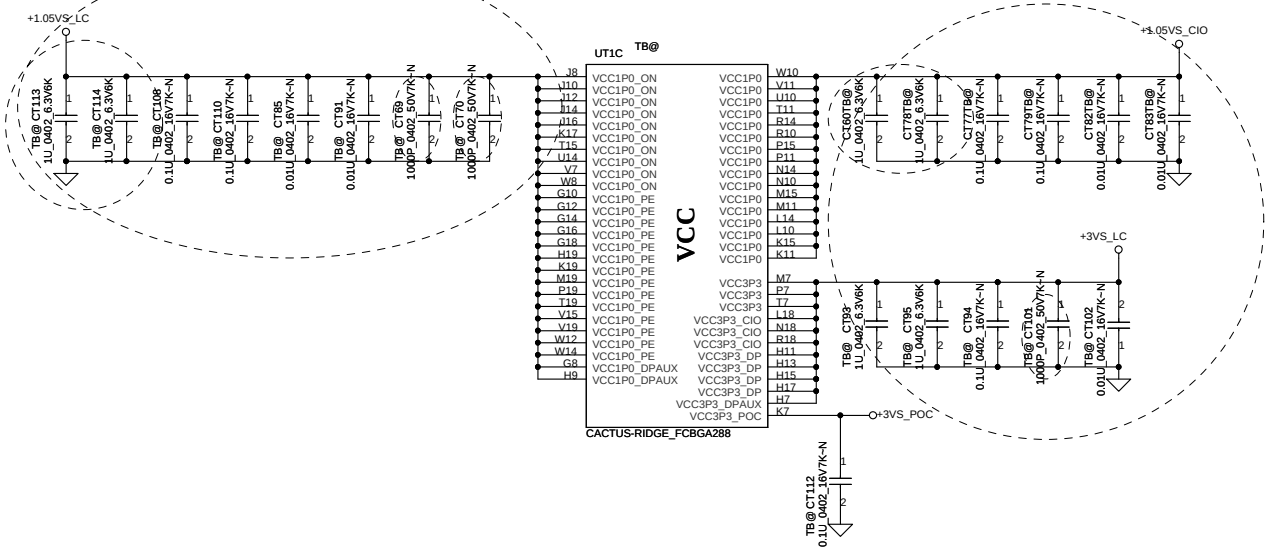
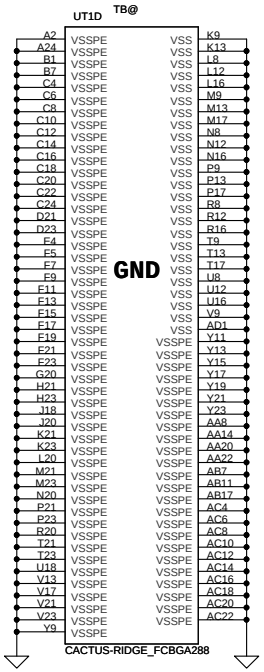
Change quantity of capacitors (follow Intel reference schematic Rev 1.13)





Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.			
Title: Cactus Ridge(3/4) HOST /mDP CONN			
Size: Custom	Document Number: LA-7822P		Rev: B
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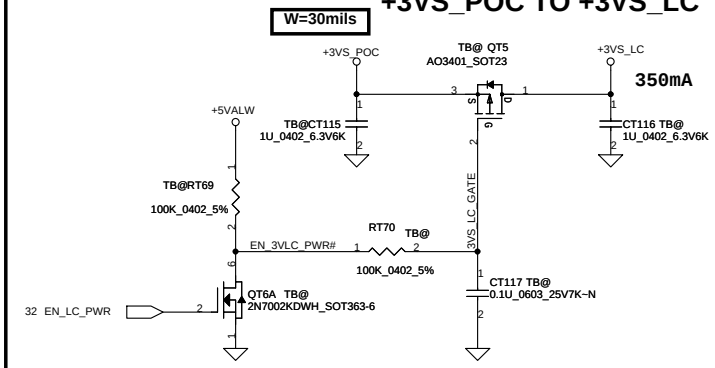
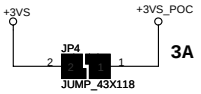
+3VS_POC TO +3VS_LC



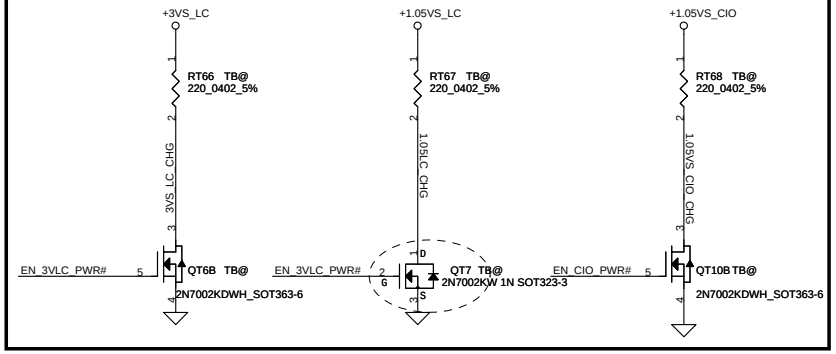
VCC3V3_LC max current 350mA

+3VS TO +3VS_POC

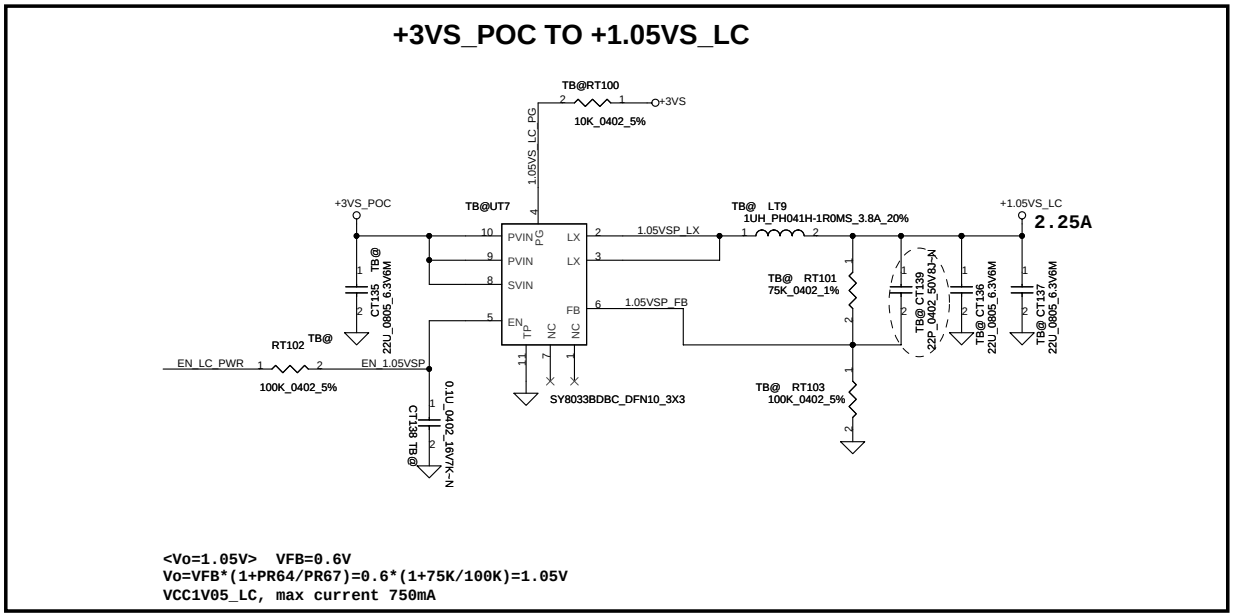


VCC3V3POC, IC CONN max current 500mA ,
VCC3V3POC, DP CONN max current 500mA ,
VCC3V3POC to VCC3V3 max current 350mA,

Discharge circuit

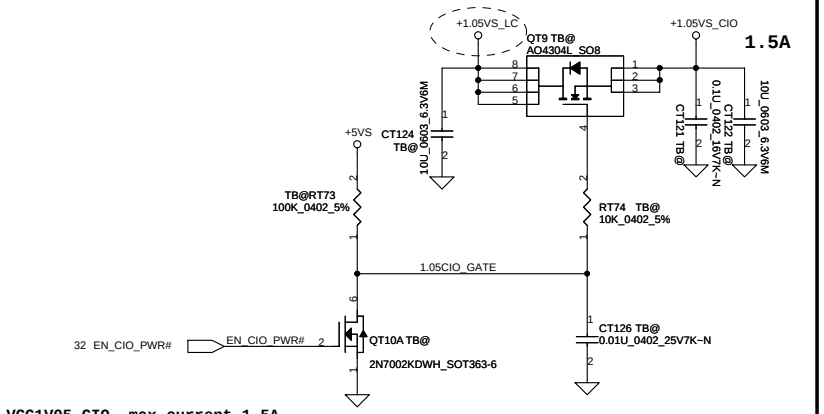


+3VS_POC TO +1.05VS_LC

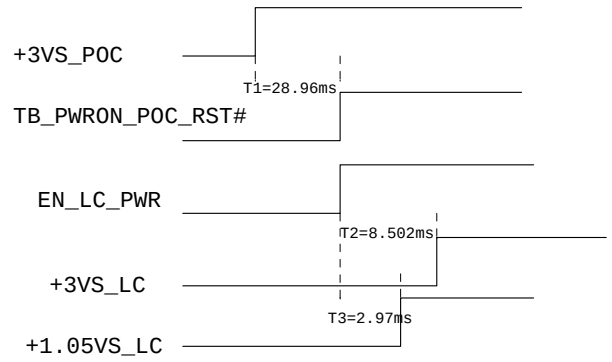


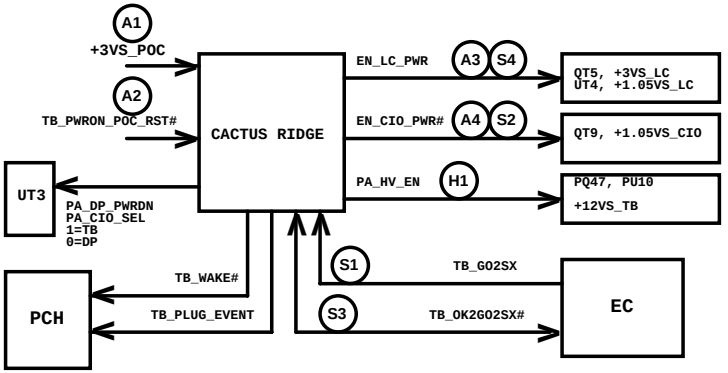
<Vo=1.05V> VFB=0.6V
Vo=VFB*(1+PR64/PR67)=0.6*(1+75K/100K)=1.05V
VCC1V05_LC, max current 750mA

+1.05VS_LC TO +1.05VS_CIO



VCC1V05_CIO, max current 1.5A





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Cactus Ridge(4/4) DC/DC

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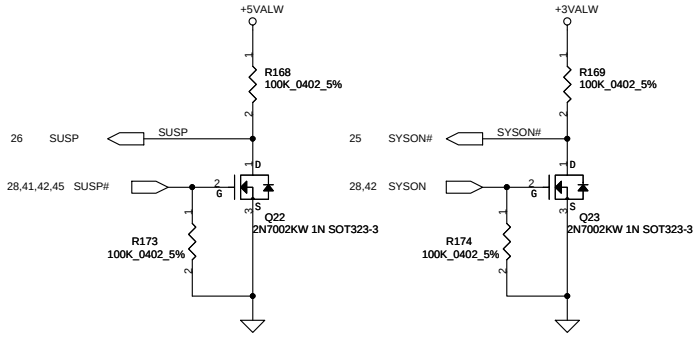
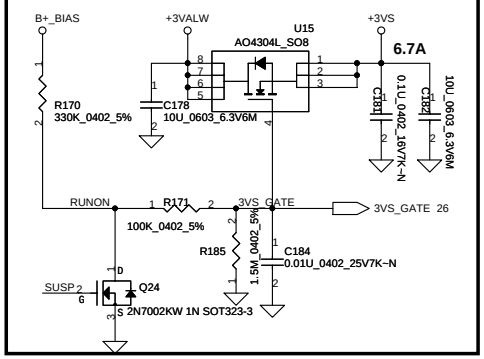
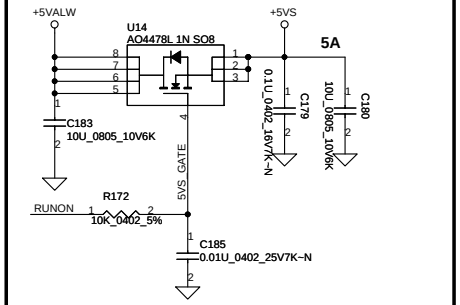


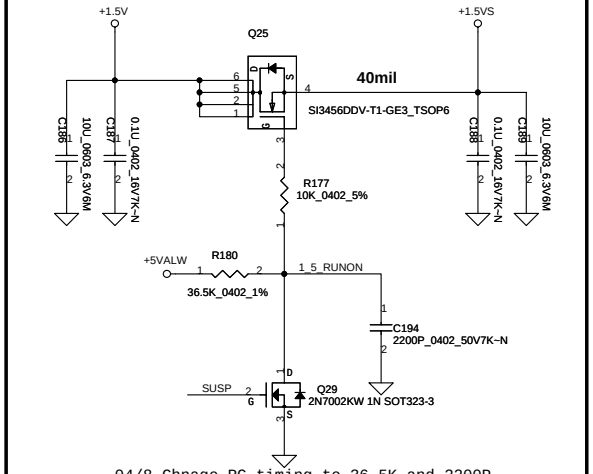
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

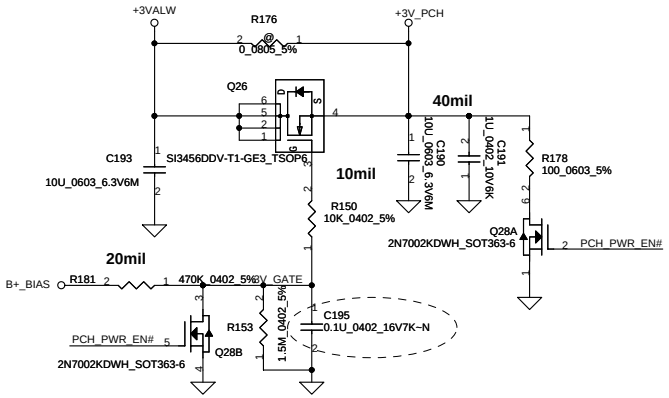


+1.5V to +1.5VS Transfer

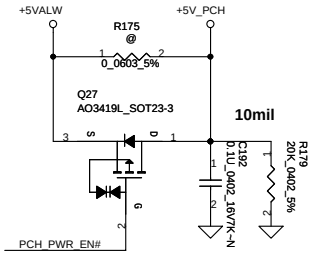


04/8 Chnage RC timing to 36.5K and 2200P

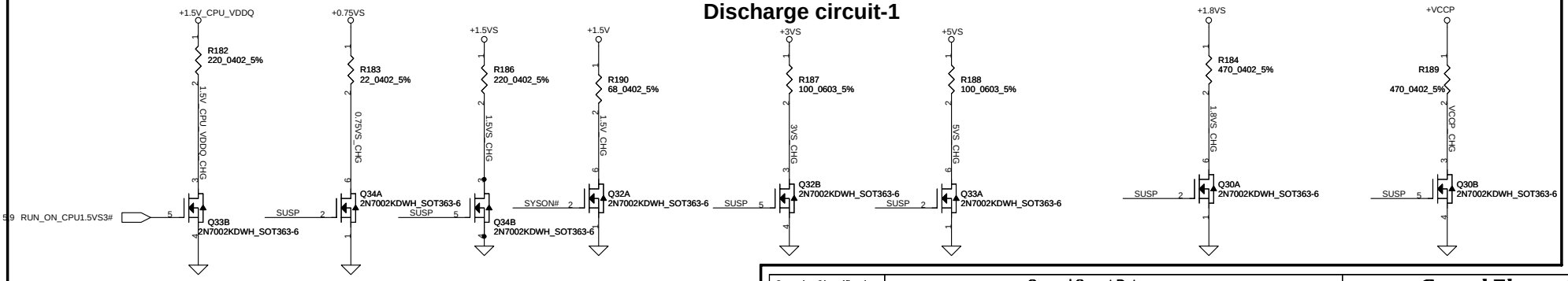
+3VALW TO +3VALW_PCH(PCH AUX Power)



+5VALW TO +5VALW_PCH(PCH AUX Power)



Discharge circuit-1



Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.			
Title: DC/DC Interface			
Size: Custom	Document Number: LA-7822P		Rev: B
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PF1:90W/19V=4.74A
4.74A/0.8/0.9 = 6.58A

CPU OTP

PH1 under CPU botten side :
CPU thermal protection at 90 degree C

Active Point: ADP>120W, ADP_I=1.26V

PF2;60W/12V=5A
5A/0.8/0.9=6.9A

SMB MLCC by NECP
HW design standard

9012 short

SMART Battery:

9.BAT+
8.BAT+
7.ID
6.B/I
5.TS
4.SMD
3.SMC
2.GND
1.GND

RTC Battery

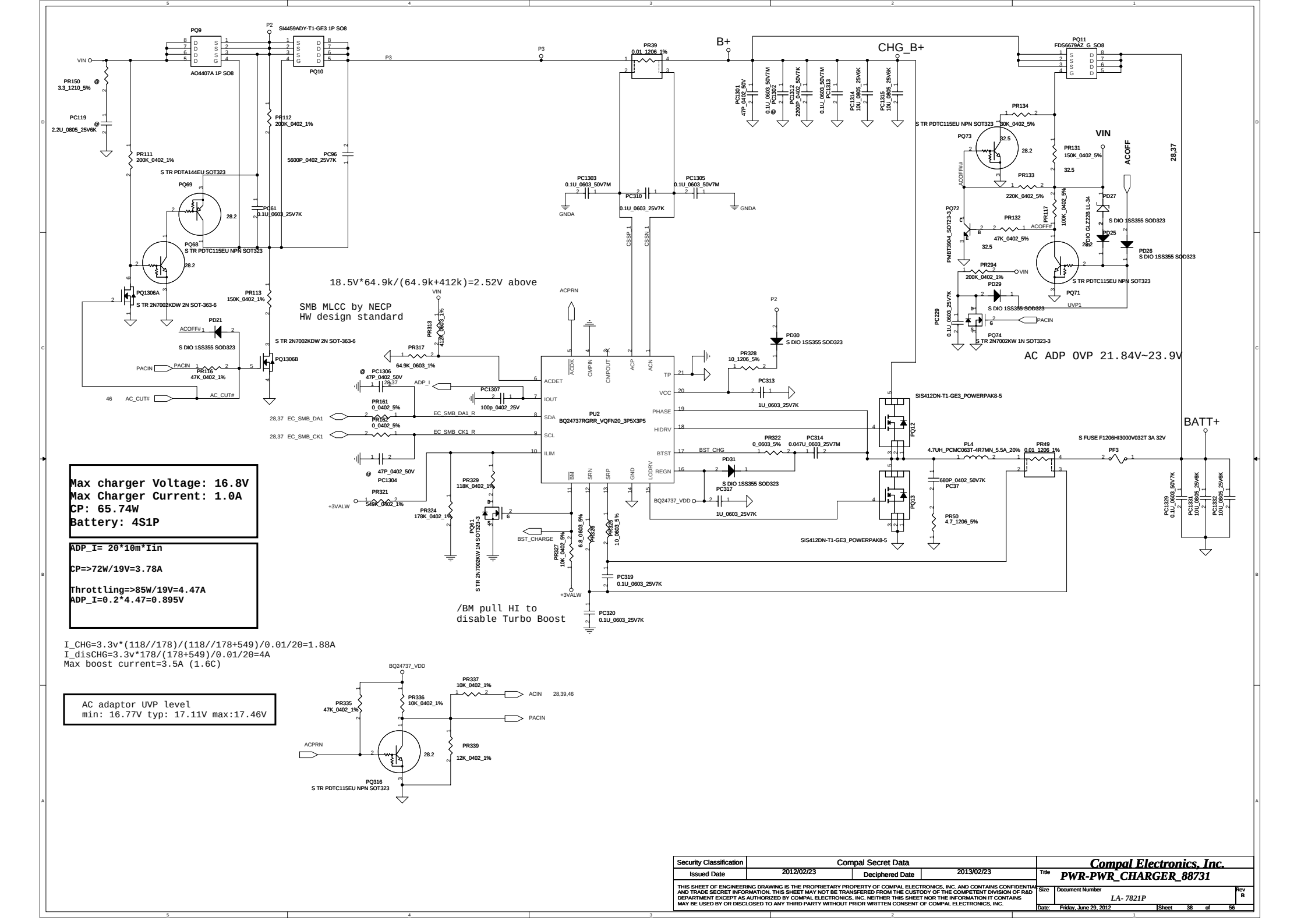
Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size: D | Document Number: LA- 7821P | Rev: B

Date: Friday, June 29, 2012 | Sheet 37 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.			
Title	PWR-PWR_CHARGER_88731		
Size	Document Number		Rev
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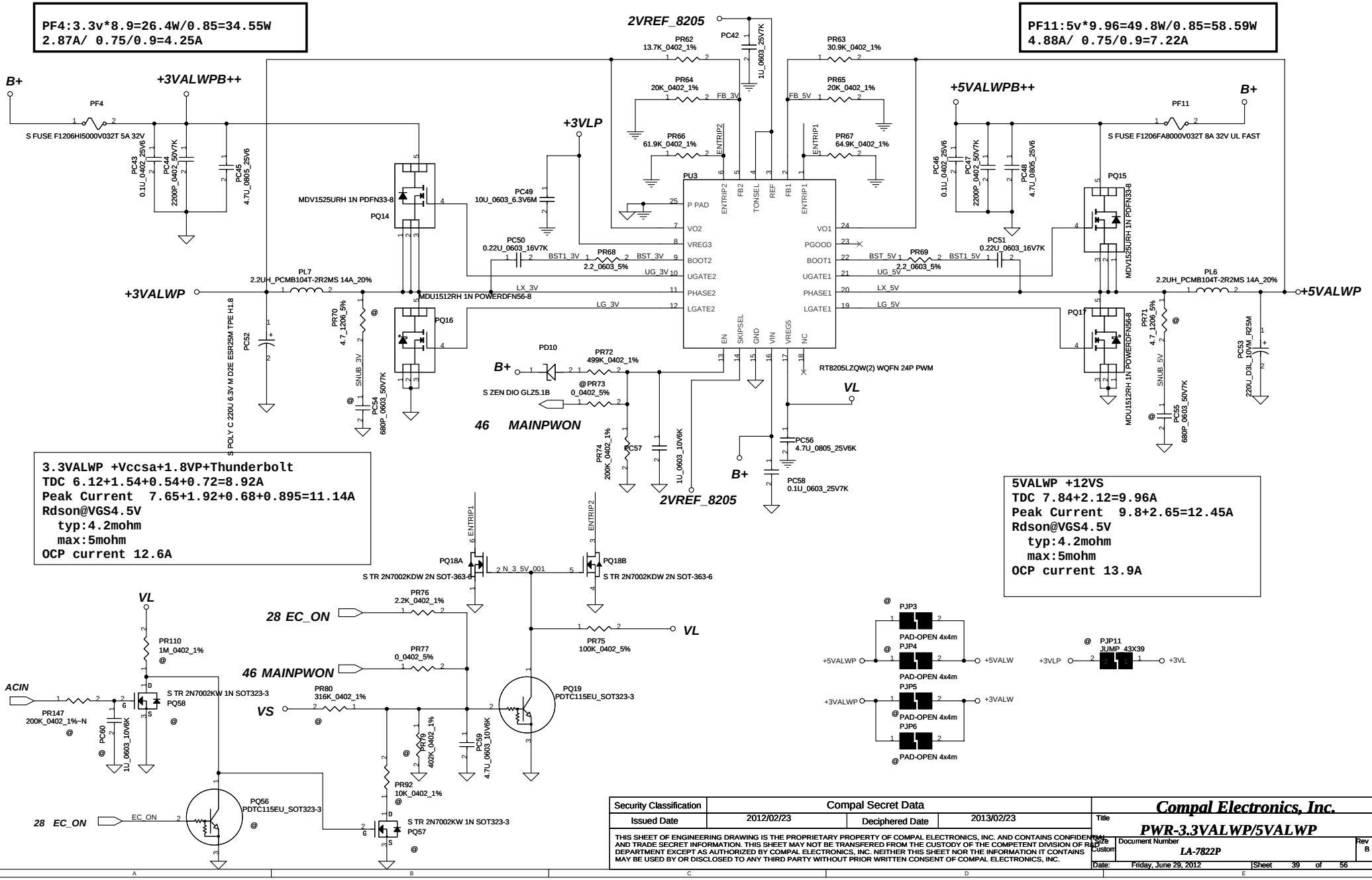
PF4:3.3v*8.9=26.4W/0.85=34.55W
2.87A/ 0.75/0.9=4.25A

PF11:5v*9.96=49.8W/0.85=58.59W
4.88A/ 0.75/0.9=7.22A



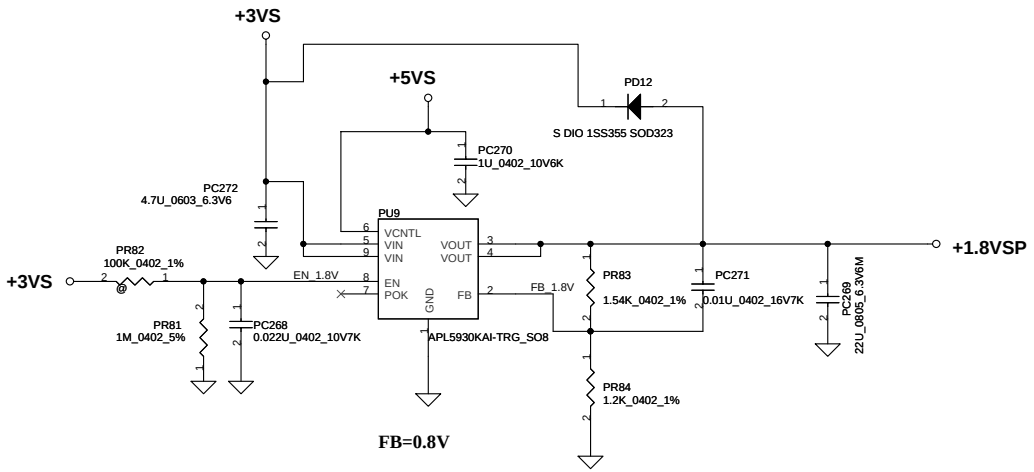
Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: Custom | Document Number: LA-7822P | Rev: B

Date: Friday, June 29, 2012 | Sheet 39 of 56



+1.8VSP
TDC = 0.99A
Peak Current = 1.24A
OCP =4.7 A

@

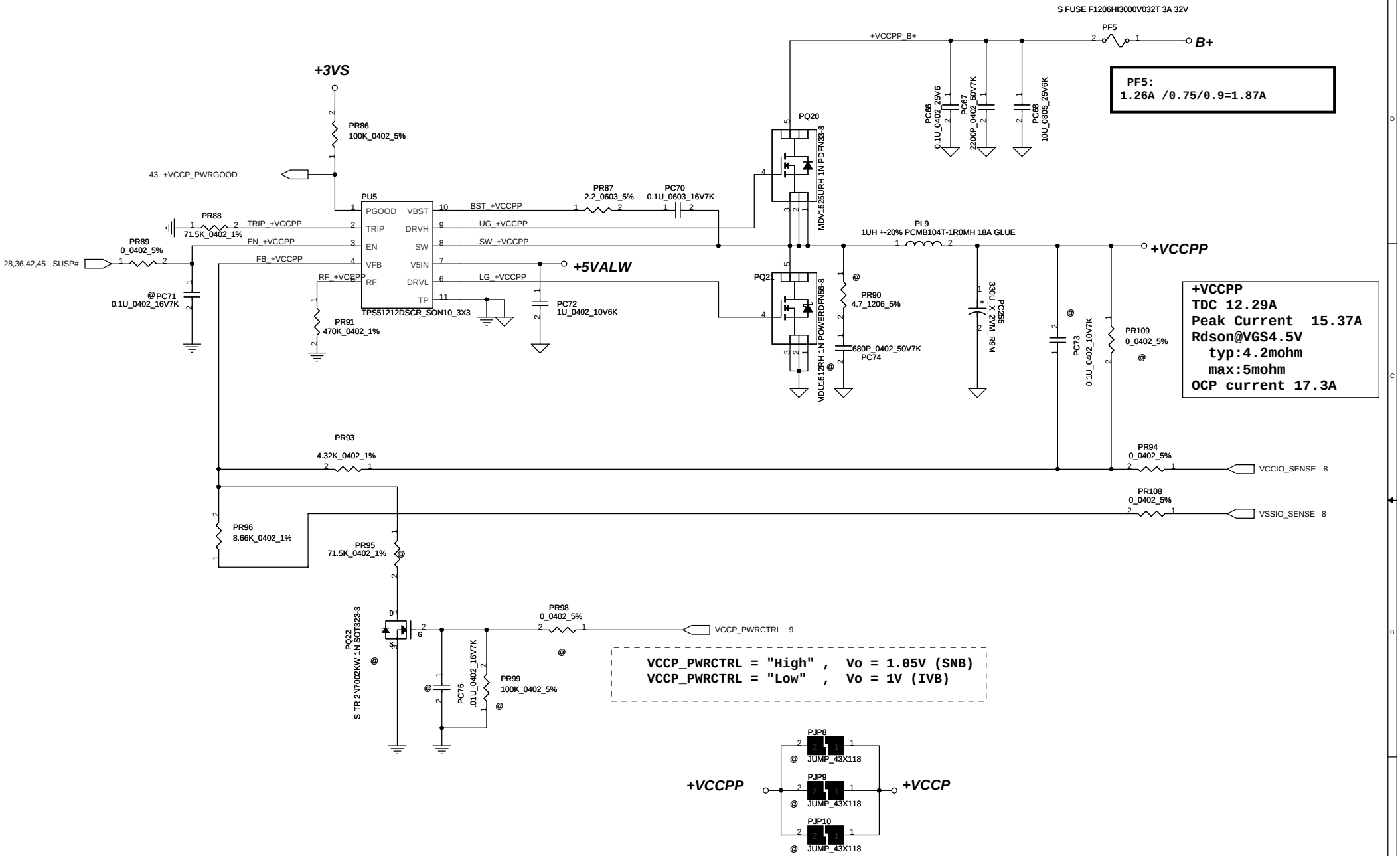
Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PWR-1.8VSP

Size: B | Document Number: LA-7821P | Rev: B

Date: Friday, June 29, 2012 | Sheet 40 of 56



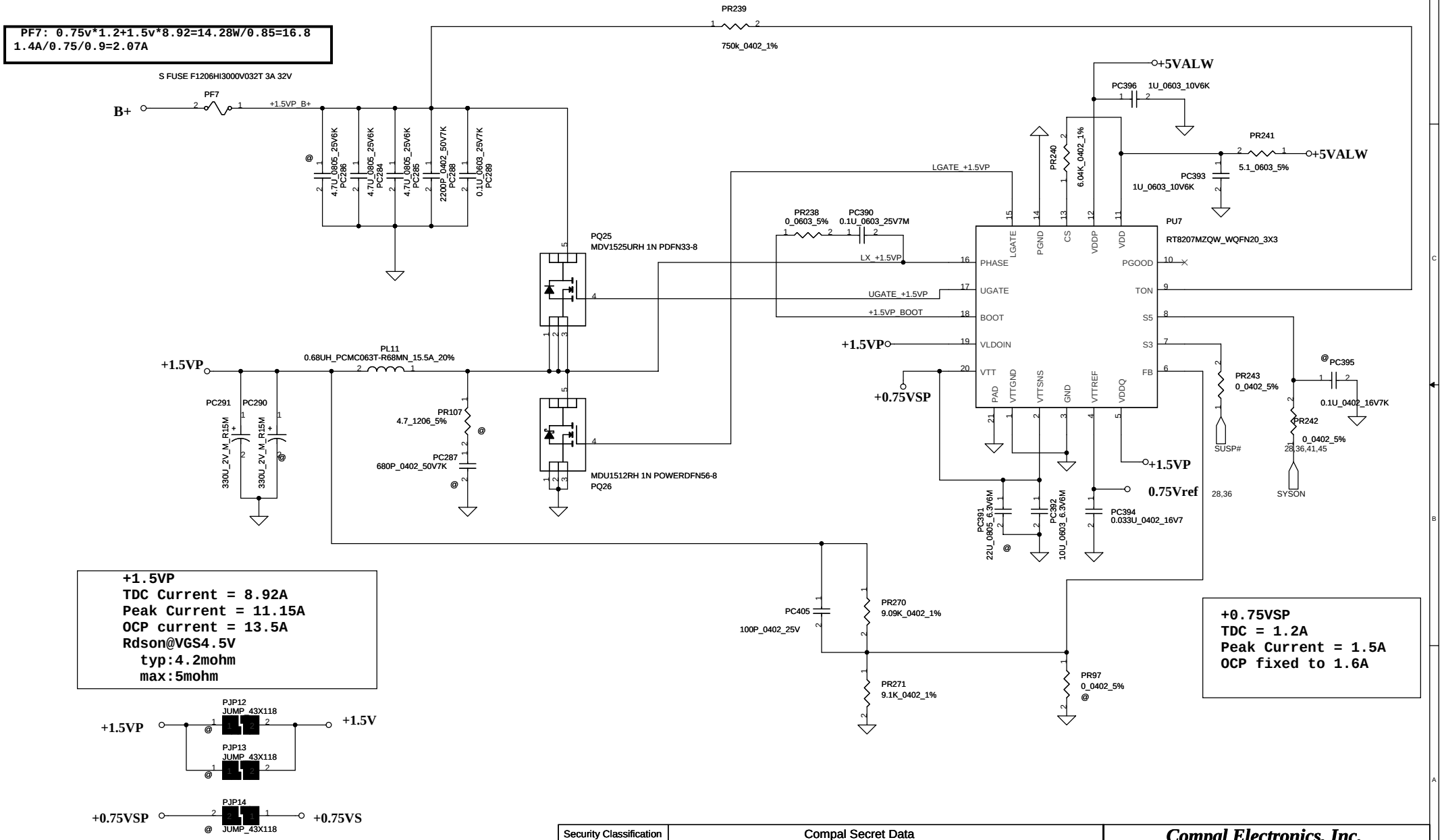
Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: **PWR-VCCPP**

Size: Custom | Document Number: LA-7821P | Rev: B

Date: Friday, June 29, 2012 | Sheet 41 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PWR-1.5VP/0.75VSP

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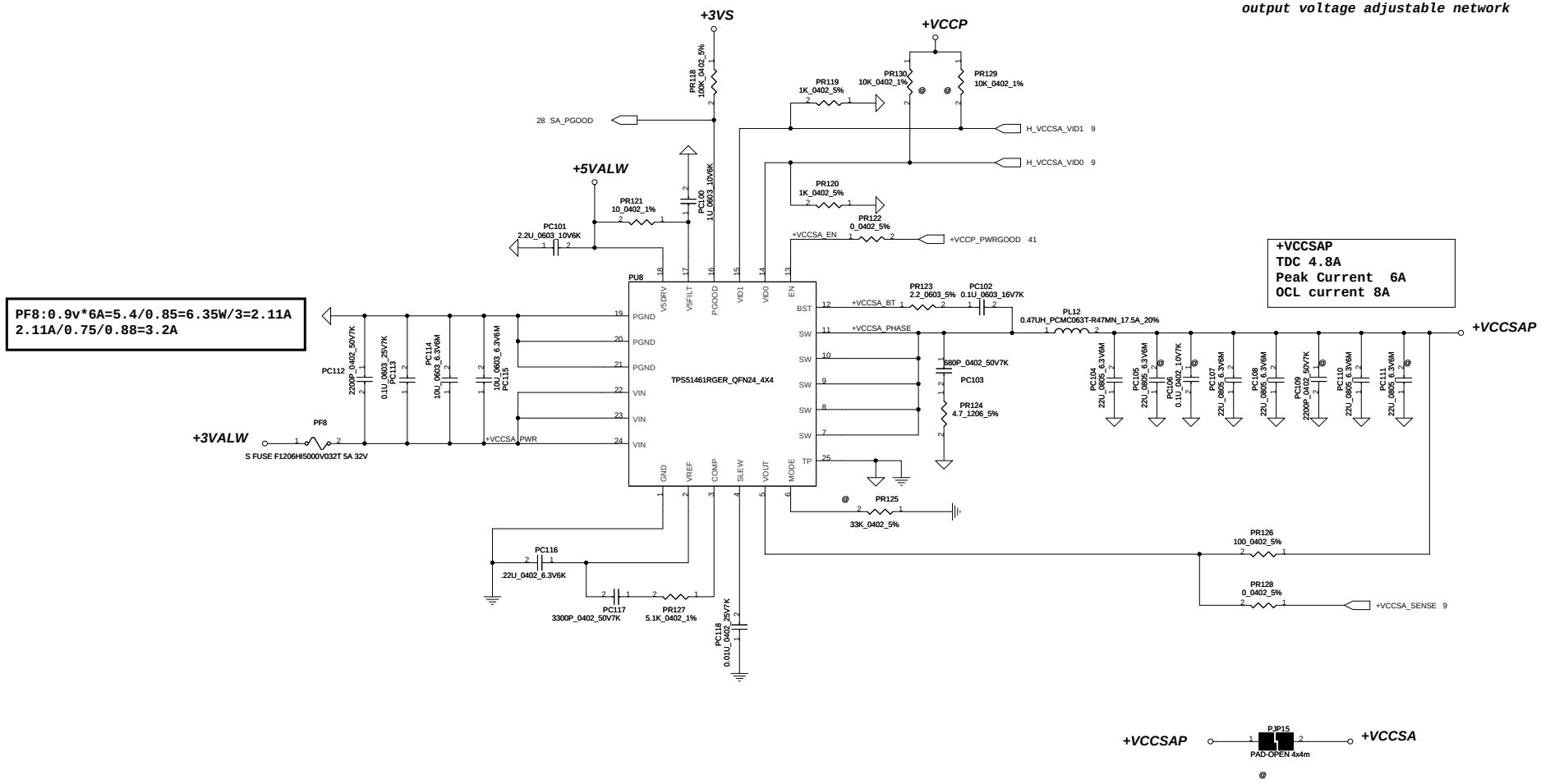
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

PF8:0.9v*6A=5.4/0.85=6.35W/3=2.11A
2.11A/0.75/0.88=3.2A

+VCCSAP
TDC 4.8A
Peak Current 6A
OCL current 8A



Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size	Document Number	Rev
C	LA-7821P	B

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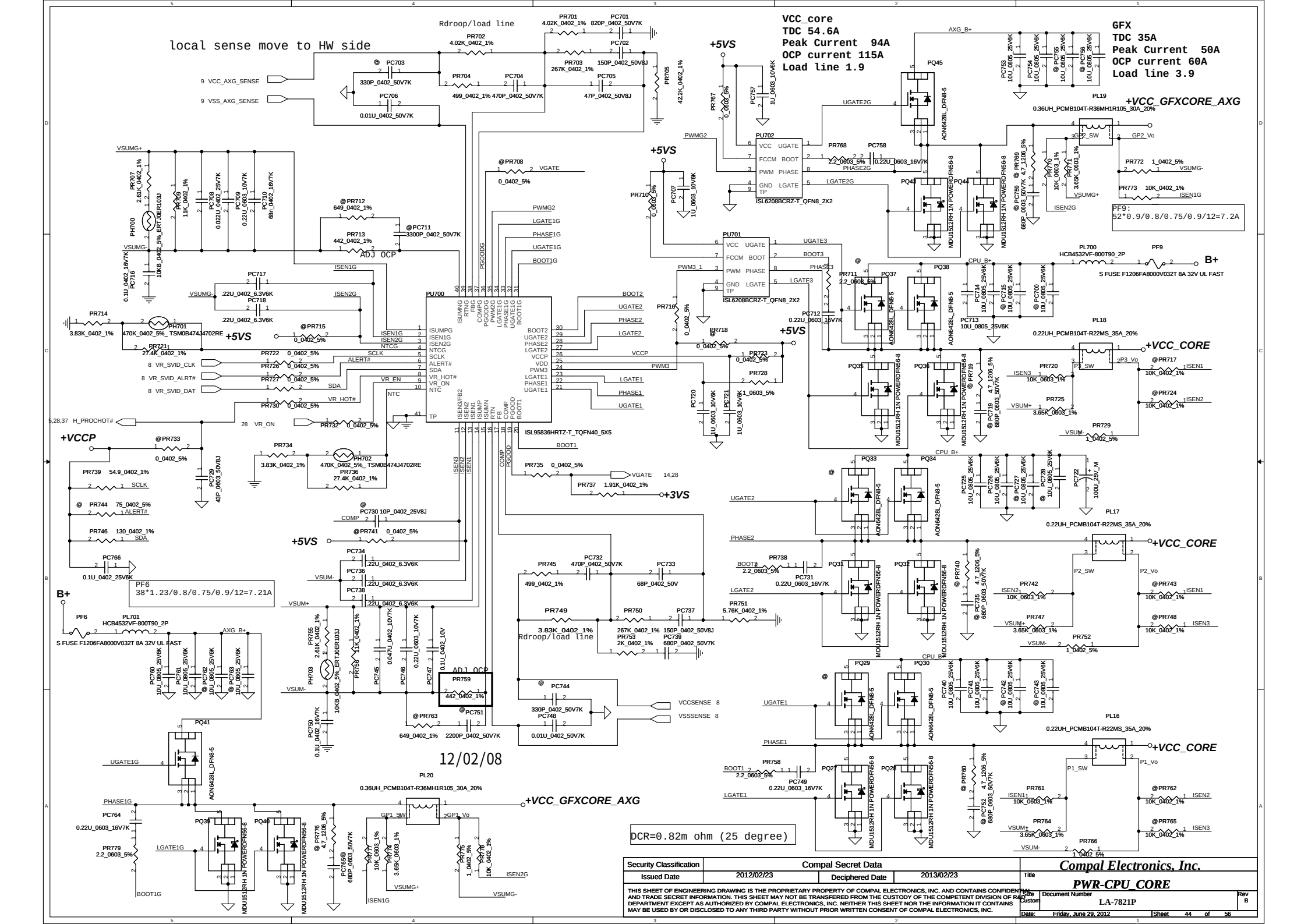
local sense move to HW side
Rdroop/load line
VCC_core
TDC 54.6A
Peak Current 94A
OCP current 115A
Load line 1.9
GFX
TDC 35A
Peak Current 50A
OCP current 60A
Load line 3.9
+VCC_GFXCORE_AXG
+VCC_CORE
+5VS
+3VS
B+
+VCCP
ADJ OCP
PF9:
52*0.9/0.8/0.75/0.9/12=7.2A
PF6
38*1.23/0.8/0.75/0.9/12=7.21A
DCR=0.82m ohm (25 degree)
12/02/08
ISL6208BCRZ-T_QFN8_2X2
ISL95836HRTZ-T_TQFN40_5X5
S FUSE F1206FA8000V032T 8A 32V UL FAST
0.36UH_PCMB104T-R36MH1R105_30A_20%
0.22UH_PCMB104T-R22MS_35A_20%
Security Classification
Compal Secret Data
Issued Date
2012/02/23
Deciphered Date
2013/02/23
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Compal Electronics, Inc.
Title
PWR-CPU_CORE
Size
Custom
Document Number
LA-7821P
Rev
B
Date:
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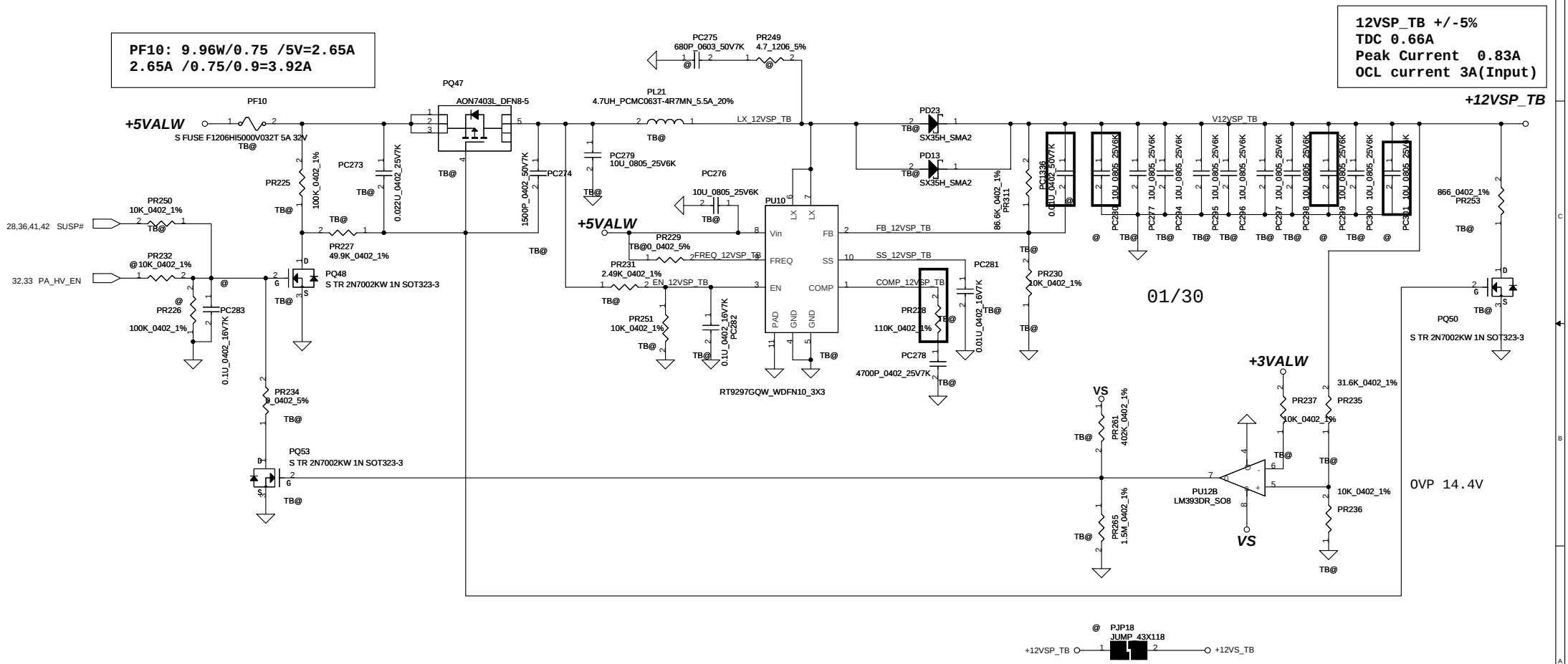
of
56



Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.			
Title	PWR-+12VSP_TB		
Size: Custom	Document Number: LA-7822P		Rev: B
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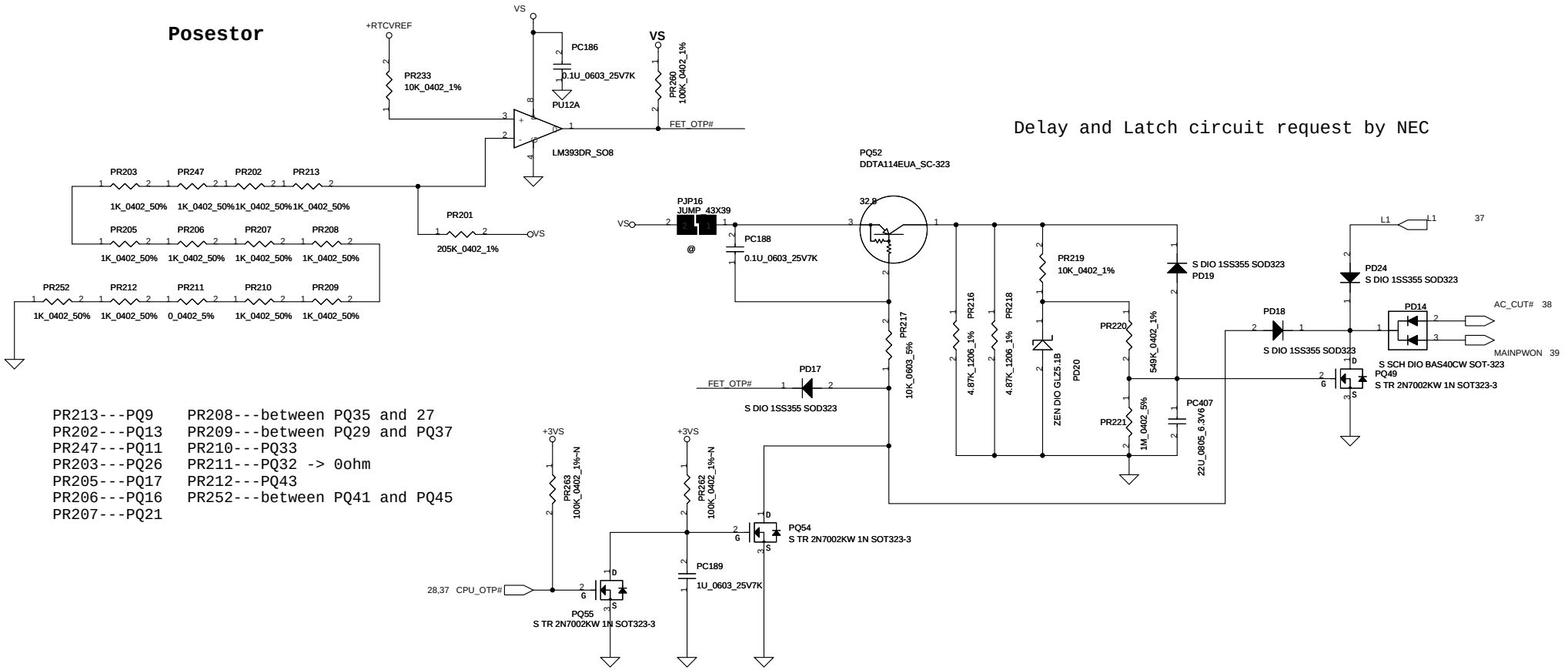
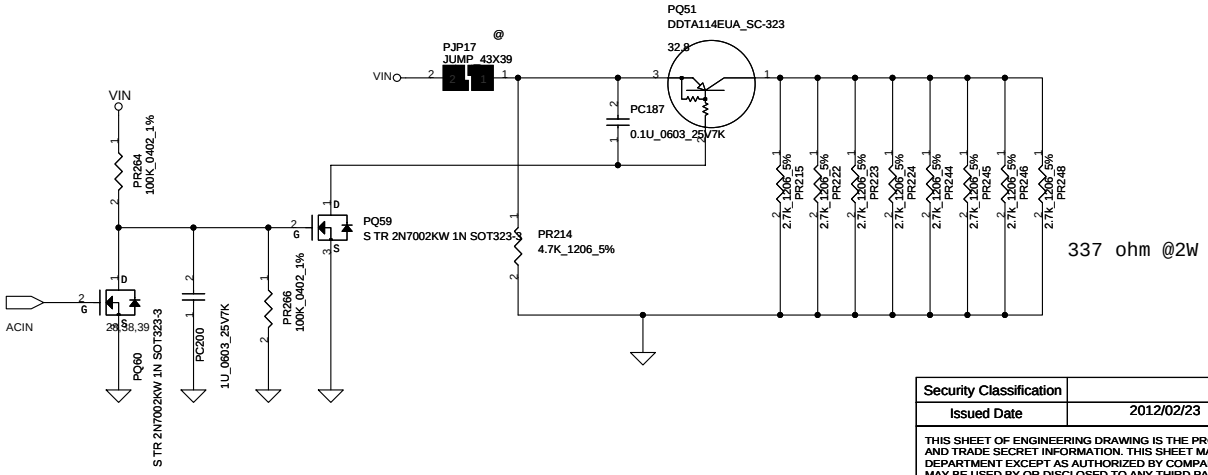
Posestor



Delay and Latch circuit request by NEC

PR213---PQ9 PR208---between PQ35 and 27
PR202---PQ13 PR209---between PQ29 and PQ37
PR247---PQ11 PR210---PQ33
PR203---PQ26 PR211---PQ32 -> 0ohm
PR205---PQ17 PR212---PQ43
PR206---PQ16 PR252---between PQ41 and PQ45
PR207---PQ21



Remaining voltage discharge circuit request by NEC

337 ohm @2W

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: **PWR-PROSESTOR**

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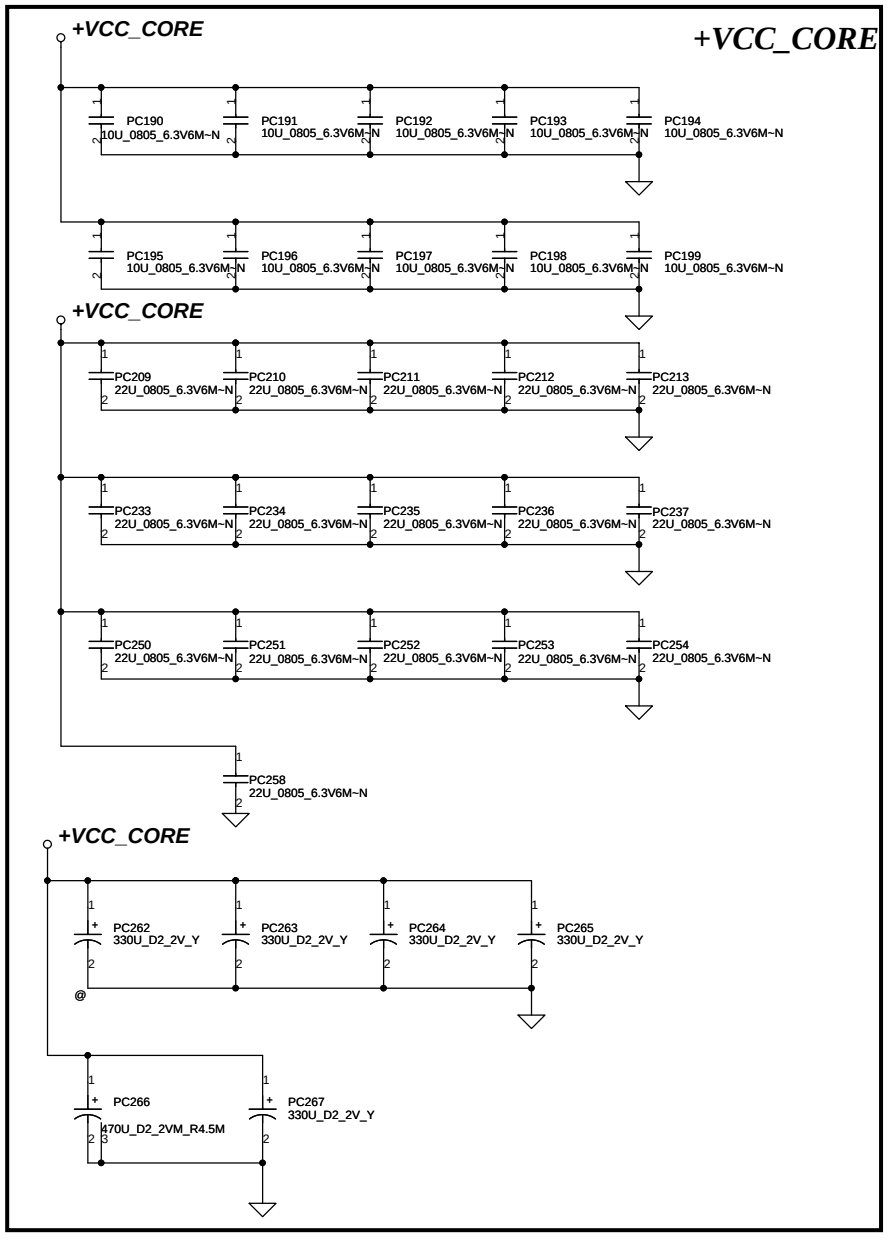
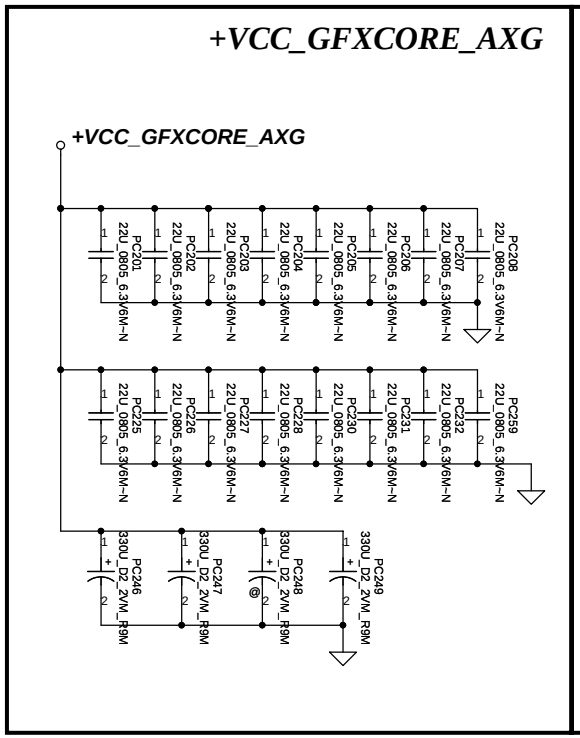
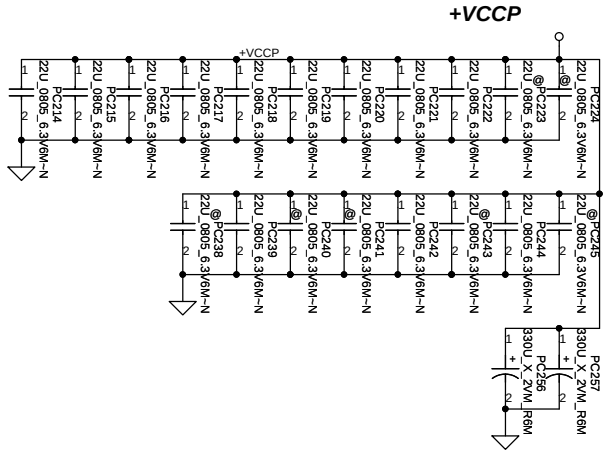




Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size	Document Number	Rev
Custom	LA-7822P	B

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DCIN / BATT CONN	11' 08/23	Compal_Aaron	remove PR11,PR21		
2	44	CPU_VORE	11' 08/23	Compal_Aaron	change LS MOS	Change (SB00000P300 S TR AON6788 1N DFN) to (SB00000SY00 S TR MDU1512RH 1N POWERDFN56-8) Location :PQ27,28,31,32,35,36,39,40,43,44	
3	44	CPU_CORE	11' 08/23	Compal_Aaron	change HS MOS	Change (SB00000NW00 S TR AON6414AL 1N DFN) to (SB00000S600 S TR MDV1525URH 1N PDFN33-8) Location :PQ29,33,37,39,41,45	
4	42	1.05VSP	11' 08/23	Compal_Aaron	adjust OCP	Change (SD034374280 S RES 1/16W 37.4K +-1% 0402) to (SD034100380 RES 1/16W 100K +-1% 0402) Location :PR101	
5	39	3.3VALWP/5VALWP	11' 08/23	Compal_Aaron	adjust OCP	Change (SD034140380 S RES 1/16W 140K +-1% 0402) to (SD034154380 S RES 1/16W 154K +-1% 0402) Location :PR66	
6	40	1.8VSP	11' 08/23	Compal_Aaron	for current limit	Change (SD028000080 S RES 1/16W 0 +-1% 0402) to (SD034100280 RES 1/16W 10K +-1% 0402) Location :PR82	
7	39	3.3VALWP/5VALWP	11' 08/23	Compal_Aaron	adjust OCP	Change (SD034178380 RES 1/16W 178K +-1% 0402) to (SD034200380 RES 1/16W 200K +-1% 0402) Location :PR67	
8	44	CPU_CORE	11' 08/26	Compal_Aaron	add PF6	add PF6	
9	38	CHARGER	11' 08/29	Compal_Aaron	solve can not power on issue	connect PR1313 pin 2 from P3 to VIN	
10	46	PROSESTOR	11' 08/29	Compal_Aaron	solve can not power on issue	connect PR262 pin 1 from VIN to 3VS	
11	37	CHARGER	11' 08/29	Compal_Aaron	adjust snubber	change PC37 form 1000pF to 680pF	
12	43	VCCSAP	11' 08/29	Compal_Aaron	adjust snubber	change PC103 form 1000pF to 680pF	
13	41	VCCP	11' 08/29	Compal_Aaron	adjust snubber	change PC74 form 1000pF to 680pF	
14	44	CPU_CORE	11' 08/29	Compal_Aaron	for current rating	change PF9 form 5A to 8A	
15	45	12VSP_TB	11' 08/29	Compal_Aaron	for current rating	change PF11 form Little to AEM	
16	44	CPU_CORE	11' 08/29	Compal_Aaron	adjust AXG OCP	change PR713 from 412 ro 442 ohm	
17	39	3.3VALWP/5VALWP	11' 08/29	Compal_Aaron	adjust OCP	Change PR66 form 154k to 174k	
18	39	3.3VALWP/5VALWP	11' 08/29	Compal_Aaron	adjust OCP	Change PR67 form 200k to 182k	
19	38	CHARGER	11' 08/31	Compal_Aaron	for protection	add PD28	

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Title: PWR-PIR

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
20	45	12VSP-TB	11' 08/31	Compal_Aaron	add 0.01uF for transient	add PC1336	
21	46	PROSESTOR	11' 08/31	Compal_Aaron	add PR248	add PR248	
22	38	CHARGER	11' 09/01	Compal_Aaron	by FAE review	change PR1331 10ohm to 0ohm	
23	38	CHARGER	11' 09/01	Compal_Aaron	for current limit	add PR1332	
24	45	12VSP_TB	11' 09/01	Compal_Aaron	for power sequence	connect PR231 pin 1 to PQ47 pin5	
25	38	CHARGER	11' 09/01	Compal_Aaron	add 0 ohm	add PR1333	
26	45	12VSP_TB	11' 09/02	Compal_Aaron	add 10kohm	add PR250	
27	38	CHARGER	11' 09/02	Compal_Aaron	change CHG IC to BQ24737	add CHG circuit	
28	39	3.3VALWP/5VALWP	11' 09/03	Compal_Aaron	adjust ocp	change PR66 to 61.9k	
29	39	3.3VALWP/5VALWP	11' 09/03	Compal_Aaron	adjust ocp	change PR67 to 64.9k	
30	39	3.3VALWP/5VALWP	11' 09/03	Compal_Aaron	for current design	change PL7 form SH00000IC00 3.3uH to SH00000O600 2.2uH	
31	42	1.5VSP	11' 09/03	Compal_Aaron	adjust ocp	change PR240 to 6.04k	
32	41	VCCPP	11' 09/03	Compal_Aaron	adjust ocp	change PR88 to 71.5k	
33	38	CHARGER	11' 09/03	Compal_Aaron	CHARGER Solution	change CHG circuit form ISL88731C to BQ24737	
34	38	CHARGER	11' 09/03	Compal_Aaron	for current design	change PL4 form 10uH to 4.7uH	
35	45	12VSP_TB	11' 09/06	Compal_Aaron	for EN pin	add PR251 10kohm	
36	38	CHARGER	11' 09/06	Compal_Aaron	change net	change BQ24737_VDD from PD31 pin1 to PC317 pin2	
37	47	PROSESTOR	11' 09/08	Compal_Aaron	add prosestor by NEC	add PR252	
38	47	PROSESTOR	11' 11/01	Compal_Aaron	for Overshoot	add PR265, PR266	

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Title: PWR-PIR

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Version Change List (P. I. R. List) Page 3

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
39	40	1.8VSP	11' 11/01	Compal_Aaron	for power sequency	change PU9 EN form SUSP# to 3VS	
40	44	CPU / AXG	11' 11/01	Compal_Aaron	adjust transient	change PR261 form 100kohm to 402kohm	
41	44	CPU / AXG	11' 11/01	Compal_Aaron	adjust transient	change PR313 form 432kohm to 412kohm	
42	44	CPU / AXG	11' 11/01	Compal_Aaron	adjust over shoot	change PL16,17,18 form 0.36uH to 0.22uH	
43	38	CHARGER	11' 11/01	Compal_Aaron	adjust current limit	change PR321 form 750k to 549k ohm	
44	38	CHARGER	11' 11/01	Compal_Aaron	adjust current limit	change PR324 form 95.3k to 100k ohm	
45	47	PROCESSOR DECOUPLING	11' 11/03	Compal_Aaron	for AXG ripple	add PC230, PC231, PC 232, PC259	
46	44	CPU / AXG	11' 11/03	Compal_Aaron	remove MOS	remove PQ30 PQ34 PQ38 PQ46 PQ42	
47	38	CHARGER	11' 11/03	Compal_Aaron	adapter change to 90W	change PF1 form 12A to 8A	
48	37	DCIN / BATT / OTP	11' 12/07	Compal_Aaron	adjust ADP protection >120W	change PR4 form 27.4K to 15K ohm	
49	38	CHARGER	11' 12/07	Compal_Aaron	for I_dischg current to 4A	change PR324 form 100k to 178k ohm	
50	38	CHARGER	11' 12/07	Compal_Aaron	for I_dischg current to 4A	change PR329 form 215k to 118k ohm	
51	42	1.5VSP	11' 12/07	Compal_Aaron	for dynamic voltage (IDLE test)	pop PR270, PR271	
52	42	1.5VSP	11' 12/07	Compal_Aaron	for dynamic voltage (IDLE test)	depop PR97	
52	45	12VSP_TB	11' 12/07	Compal_Aaron	for discharge circuit	change PR227 from 100k to 49.9k ohm	
53	39	5VALWP/ 3VALWP	11' 12/16	Compal_Aaron	for KB9012	change PR76 from 10k to 2.2k ohm	
54	40	1.8VSP	11' 12/19	Compal_Aaron	for power sequency	unmount PR82	
55	40	1.8VSP	11' 12/19	Compal_Aaron	for power sequency	change PC268 from 0.22uF to 0.022uF	
56	40	1.8VSP	11' 12/19	Compal_Aaron	for power sequency	change PR81 from 4.7k to 1M ohm	

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Title: PWR-PIR

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
57	37	DCIN / BATT / OTP	11' 12/19	Compal_Aaron	change 90W BATT to 60W	change PF2 form 12A to 8A	
58	45	12VSP_TB	11' 12/19	Compal_Aaron	add capacitors	add PC302~309, PC311, PC312	
59	45	12VSP_TB	11' 12/20	Compal_Aaron	add capacitors	add PC723,PC724	
59	45	12VSP_TB	11' 12/20	Compal_Aaron	add discharge R	add PR253	
60	45	12VSP_TB	11' 12/20	Compal_Aaron	for discharge MOS	change PQ50 MOS AO4466 to 2N7002	
61	44	VCORE / AXG	11' 12/22	Compal_Aaron	for thermal	add MOS PQ30,PQ34,PQ38	
62	45	12VSP_TB	11' 12/22	Compal_Aaron	by NEC request	change PR253 from 200k to 866 ohm	
63	44	VCORE / AXG	12' 01/02	Compal_Aaron	for TP thermal	mount MOS PQ30,PQ34,PQ38 to AON6428L	
64	44	VCORE / AXG	12' 01/02	Compal_Aaron	for TP thermal	unmount MOS PQ29,PQ33,PQ37	
65	44	VCORE / AXG	12' 01/02	Compal_Aaron	for MOS quality	change MOS PQ41,PQ45 from AON6514 to AON6428L	
66	45	12VSP_TB	12' 01/30	Compal_Aaron	remove capacitors	delete PC302~309, PC311, PC312, PC723, PC724	
67	45	12VSP_TB	12' 01/30	Compal_Aaron	for dynamic test	unmount PC1336, PC280 ,PC299 ,PC301	
68	45	12VSP_TB	12' 01/30	Compal_Aaron	for dynamic test	change PR228 from 10k to 110k	
69	44	VCORE / AXG	12' 02/08	Compal_Aaron	for VCORE OCP	change PR759 from 430 to 442 ohm	
70				Compal_Aaron			
71				Compal_Aaron			
72				Compal_Aaron			
73				Compal_Aaron			
74				Compal_Aaron			

Security Classification	Compal Secret Data		
Issued Date	2012/02/23	Deciphered Date	2013/02/23

Compal Electronics, Inc.

Title: PWR-PIR

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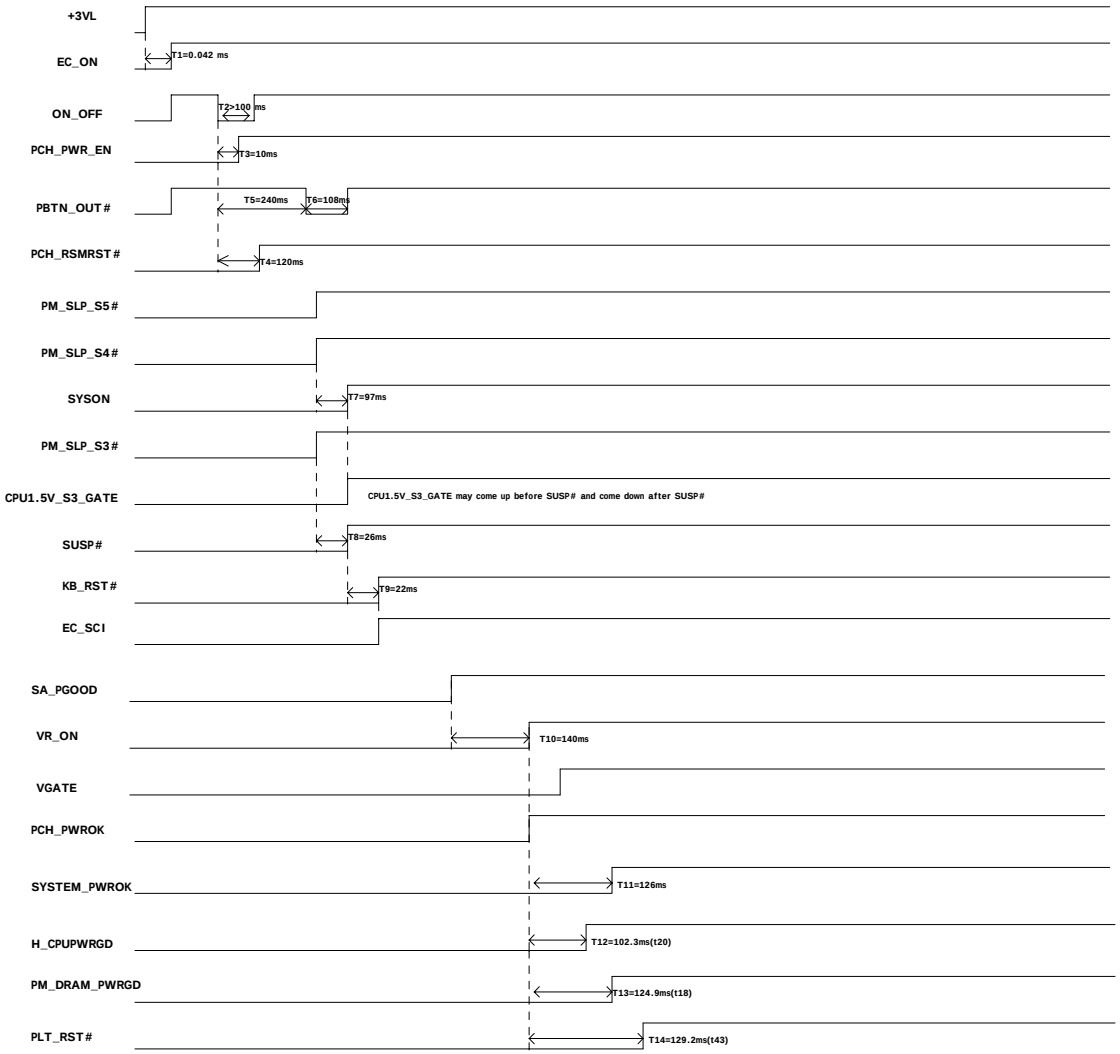
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.01	20	Modify JLCD1 NET	08/22	
2		HW Design	0.01	09,35,36	Change AO4430L to AO4304L location:QC3 QT9 U14 U15	08/22	
3		HW Design	0.01	27,36	Change SI3456BDV to SI3456DDV location:Q14 Q25 Q26	08/22	
4		HW Design	0.01	27,36	Change SI3456BDV to SI3456DDV location:Q14 Q25 Q26	08/22	
5		NECP Recommend	0.01	29	Change JTP1 to 12PIN	08/23	
6		NECP Recommend	0.01	26	Remove WLAN JMINI1 +1.5VS	08/23	
7		HW Design	0.01	34	Change CT113 CT114 CT60 CT78 to 1U	08/23	
8		ME Recommend	0.02	34	SWAP JTP1 Pin define	08/28	
9		ME Recommend	0.02	20	Update JLCD1 and JCM1 footprint	08/29	
10		ME Recommend	0.02	24	Update JHP1 and JMIC1 footprint	08/29	
11		NECP Recommend	0.02	28,23,26 14,30	Add 0.1U in U9,U57,U61,UH5,U58,U59	08/30	
12		NECP Recommend	0.02	22	R44 change to un mount	08/30	
13		NECP Recommend	0.02	26	Mount R114	08/30	
14		NECP Recommend	0.03	26	Add Circuit for INTEL AOAC Fucntion	08/31	
15		NECP Recommend	0.03	28	Add R295 R296 for INTEL AOAC Fucntion	08/31	
16		HW Design	0.03	14	Add RH148 pull down Change R269 R290 pull high	09/01	
17		HW Design	0.03	33	Add JMDP1 footprint	09/01	
18		EC Recommend	0.03	12,28	Change net name ME_FLASH to ME_EN	09/01	
19		HW Design	0.03	15	Pull high GPIO2	09/01	
20		NECP Recommend	0.04	20	D1 Pin 6 connect to USB20_N4 D1 Pin 4 connect to USB20_P4	09/02	
21		NECP Recommend	0.04	29	Update JTP1 PIN Define	09/02	
22		NECP Recommend	0.04	12	Change RH2100 from 15ohm to 0ohm	09/02	
23		Power Design	0.04	28	mound C113 Add R297 for BST_CHARGE	09/02	
24		HW Design	0.04	16	Remove RH159 PCH PECI for Layout routing	09/02	
25		HW Design	0.05	26,27 30 23	Change R270, R292 to 2.61k Change R236, R249 to 2.61k Unmount R273,R277 Change R226 to 2.61k	09/06	
26		HW Design	0.05	32	Add CT140,CT141 close to UT1	09/07	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.07	34 33	Change CT69,CT70,CT101 to 0.001U Change RT39 to 348K and RT94 to 35.7K	09/08	
2		HW Design	0.11	28	Change R210 to 220K	09/22	
3		HW Design	0.11	26 ,27	Change R270 and R292 to 3.83K	09/29	
4		HW Design	0.11	24	Change CA19 and CA21 footprint from 0805 to 0603	09/29	
5		HW Design	0.11	13 ,32	Change YH2 and YT1 from SJ100009B00 to SJ10000B700	09/30	
6		HW Design	0.11	9 ,17	Change CC135 ,CC161 ,CC162 ,CC163 ,CC164 ,CC165 ,CC166 ,CC168 ,CC169 ,CC170 ,CC171 ,CC173 ,CH30 ,CH44 footprint from 0805 to 0603	10/03	
7		HW Design	0.11	12	Change YH1 to FC-135 Change CH2 and CH3 to 15PF	10/04	
8		HW Design	0.11	5 ,21 ,23 ,25 ,26 ,32 ,35 ,36	Change SB000009610 to SB000009620 QC1,Q1,Q5,Q9,Q37,QT11,QT12,QT7,Q22,Q23,Q24,Q29,Q36	10/12	
9		HW Design	0.11	31, 36	Change Q27 from AO3413L to AO3419L Change Q21 from AO3413 to AO3419L	10/12	
10		HW Design	0.11	20	Change JCM1 to ACES_87213-1200G	10/18	
11		HW Design	0.11	25	Change JUSB3 to ACES_87036-1001-CP	10/18	
12		HW Design	0.11	15	Change RPH1 to RH32-RH36 Change RPH2 to RH37,RH39,RH41,RH50 Change RPH3 to RH159,RH184,RH185,RH186 Change RPH5 to RH189,RH190,RH191,RH192	10/19	
13		EMI Recommend	0.11	24	Remove RA31,RA32,RA33,RA34 Add LA6,LA7,LA8,LA9 Add CA26,CA27,CA28,CA30,CA32,CA33	10/20	
14		HW Design	0.11	09	Change CC176 to 330U 6.3V M D2E ESR25M	10/24	
15		HW Design	0.11	05	Remove RC130,RC129	10/27	
16		HW Design	0.11	06	Remove RC48	10/27	
17		HW Design	0.11	28	Remove R105 R125 R126 R127 R142 R143 R144 R145 U7 Remove C126 R147 C128 R128 R193	10/27	
18		HW Design	0.11	30	Add R193,D27 Change D15 to YSCLAMP0524P_SLP2510P8-10-9	10/27	
19		HW Design	0.11	36	POP C193 Q26 R150 C190 C191 R178 Q28 C915 R153 POP Q27 C192 R179 Q36 R200 UNPOP R175 R176	10/27	
20		HW Design	0.11	28	Change R108 to 46.4K	10/27	
21		Intel Design	0.11	33	Add CT143, UT8 Add QT15 , RT105, RT104 Add CT142	10/19	
22		HW Design	0.11	32	Change YT1 to X3G025000DC1H	10/19	
23		NECP Recommend	0.11	26 25	Add R105 D17 Change Net USB20_N12 and USB20_P12 to JUSB3 Add Net RF_OFF# to JUSB3	10/28	
24		NECP Recommend	0.11	24	Pop CA44 10pF Change RA1654 to 33 ohm and RA1655 to 56ohm	10/28	
25		HW Design	0.11	25 28	Remove 930@ C126 D9 D10 R105 R125 R126 R127 R128 R142 R143 R144 R145 R193 U7	10/28	
26		NECP Recommend	0.12	25 26	Remove R105 Change RF power from +5vs to +3vs	10/31	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.12	30	Add F10 C242 for USB3.0 Redriver Add R298 R193	10/31	
2		HW Design	0.12	26 27	Add R299 R302 Add R300 R301	11/01	
3		EMI Recommend	0.12	22	Change R46~R51 to 22ohm and C51 to 10pF	11/01	
4		EMI Recommend	0.12	30	Change D15 to AZ1045-04F DFN2510P10E ESD Add D27	11/01	
5		HW Design	0.12	29	Change SW2 and SW3 to NTC014-AA1G-A100T SPST H4.3 4P	11/01	
6		HW Design	0.12	17,36 27,30,24	Change CH36,C186,C189,C190,C193,C27,CA11,CA42,C162 Footprint from 0805 to 0603	11/01	
7		HW Design	0.12	21,23,25 36,26,05 35,32	Change Q1 Q5 Q9 Q22 Q23 Q24 Q29 Q36 Q37 QC1 QT7 QT11 QT12 to 2N7002KW 1N SOT323-3	11/01	
8		HW Design	0.12	29,36,24 25,27,18	Change C160, C172, C191, CA26, CA33, C66, C227, CH71 C104, C99 Footprint from 0603 to 0402	11/01	
9		HW Design	0.13	25	Add Q31 C207 R303 Q39 C208 R68	11/01	
10		HW Design	0.13	30	Modify netname LED_SRC to +LED_SRC Modify netname RE_PWR to +RE_PWR	11/02	
11		EMI Recommend	0.13	22	Delete Net SP14_MSCLK_R	11/02	
12		Intel recommend	0.14	33	Delete RT98,RT99,RT55,RT58,RT59 Add RT106,RT107	11/03	
13		USB3.0 fine tune	0.14	23	Remove R281	11/03	
14		Thailand floods material issue	0.2	30	Change U10 to MAX14618ETA+T Change C161 to SANYO 150U 10V M D3L TPB LESR40M 2.8	11/09	
15		Thailand floods material issue	0.2	33	Change CT133 to SANYO 100U 6.3V M B2 LESR35M	11/09	
16		Thailand floods material issue	0.2	15,32	Change UH3 and UT5 74AHC1G08GW	11/09	
17		HW Design	0.21	15,32	Change H15 to 3P_1	12/01	
18		HW Design	0.21	26,27	Add R304 R305 for Pericom Repeater	12/01	
19		ME Recommend	0.21	25	Change JUSB3 to SP02000TR00(50224-01001-001)	12/01	
20		ME Recommend	0.21	20	Change JCM1 to ACES_50224-01001-001	12/01	
21		ME Recommend	0.21	33	Change UT8 to MC74VHC1GT50 Change RT93 RT94 RT106 RT107 to 17.8K Change EC PIN64 Net to PWR_WHITEBTN_LED#	12/01	
22		NECP Recommend	0.21	12 28	Add RH267 RH268 RH270 RH271 RH272 for LPC Add R115 R125 R113 R105 R101 for LPC	12/01	
23		NECP Recommend	0.21	25	Change R68 to20K Change C208 to 0.1U	12/01	
24		NECP Recommend	0.21	16 26	Add C73 C126 Delete net BT_DIS#	12/01	
25		NECP Recommend	0.21	24	Change RA20 to 330K	12/01	
26		HW Design	0.21	30	Delete USB3.0 Redriver U58 U59 Add R205,R206,R208,R209 Add R213,R233,R214,R232	12/01	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.21	12	Change CH2 CH3 to 18P	12/15	
2		HW Design	0.21	26 28	Add Net KILL_SWOFF# and Add R142 for WLAN Issue	12/15	
3		HW Design	0.21	36	Change C195 to 0.1U	12/18	
4		NECP Recommend	0.22	22	Add L11 for CardReader	12/18	
5		EMI Recommend	0.22	36	Add D6 FOR EMI	12/19	
6		HW Design	0.23	15 20 24	Change UH3 UV2 and UA5 to 74AHC1G08GW Change UA4 to M74VHC1GT125DF2G	12/20	
7		HW Design	0.21	36	Change UH4 to BD82HM77 QPRG C1 BGA 989P	12/21	
8		Intel Recommend	0.23	33	Add QT16,QT17,QT18,QT19,QT20 for following Intel DDC	12/21	
9		Intel Recommend	0.3	32	Change UT2 to AT25256B-SSHL-T	12/21	
10	LPC EA FAIL	Fine tune the damping value for EA PASS	0.31	12,28	Change RH267 RH268 RH270 RH271 RH272 to 47ohm for LPC Change R115 R125 R113 R105 R101 to 33ohm for LPC	1/12	
11	Thunderbolt Lane1 Fail	Follow INTEL Thunderbolt CRB	0.31	33	Remove RT53 RT57 and RT63 Add DT8	2/2	
12	RF WAKE FAIL at S3	KILL_SWOFF# keep low at S3	0.31	26	Change +3VS_WLAN to +3VALW for SW1	2/2	
13	USB3.0 HDD lost issue S3 resume Fail	U57 USB3.0 Redriver PWR is +3VS	0.31	23	Change U57 PWR to +3V_PCH	2/3	
14	USB3.0 HDD lost issue S3 resume Fail	USB3.0 Redriver PWR is +3VS	0.31	30	Change F10 PWR to +3V_PCH	2/3	
15	RTC timing delay in 40 degree	Change YH1 CAP to samll value	0.31	12	Change CH2 CH3 to 15P	2/3	
16	Pericom USB3.0 Port 2 FAIL	Fine tune Redriver strap setting for Pericom	0.31	23	Add R218 R219 for Pericom USB3.0 Strap	2/3	
17	Thunderbolt Lane1 Fail	Intel Recommend	0.32	32	Add RT24,RT43.RT31,RT19 Remove RT21 RT22 CT140 CT141	2/7	
18		ME Design	0.32	31	Change H6 and H32 to 3P_8	2/8	
19		ME Design	0.33	20	Change JCM1 to ACES_50228	2/9	
20		Cysteal EA Report Recommend	0.33	20	Change CT9 CT10 to 12pF	2/9	
21	CRT ripple issue	PCH change stepping, CRT ripple worse than ES2	1.0	17	Change CH36 to 22uF	2/23	
22							
23							
24							
25							
26							

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Compal Electronics, Inc.

Title: Power Sequence

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