COMPAL CONFIDENTIAL

MODEL NAME :CDM60

PCB NO : LA-E071P

BOM P/N :

BR12 KBL-U UMA

Kabylake U

2016-11-07

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DAA000CO000	PCB 1SR LA-E071P REV0 MB 1

Layout Dell logo

REV:X00
PWB: 9RJMF

Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-E071P | Rev: 1.0

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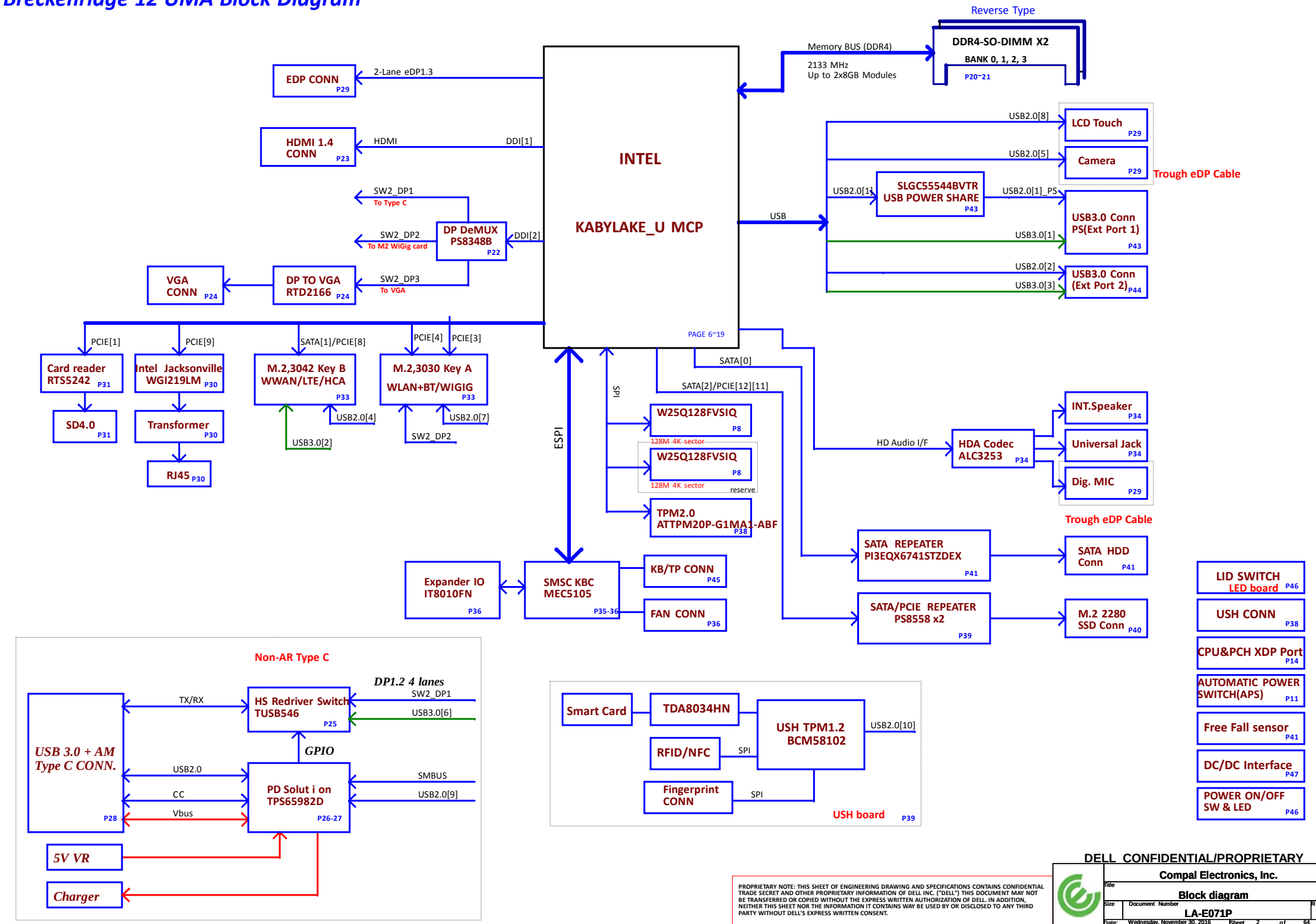
Breckenridge 12 UMA Block Diagram



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Title: Block diagram

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For Breckenridge12/14/15 UMA

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

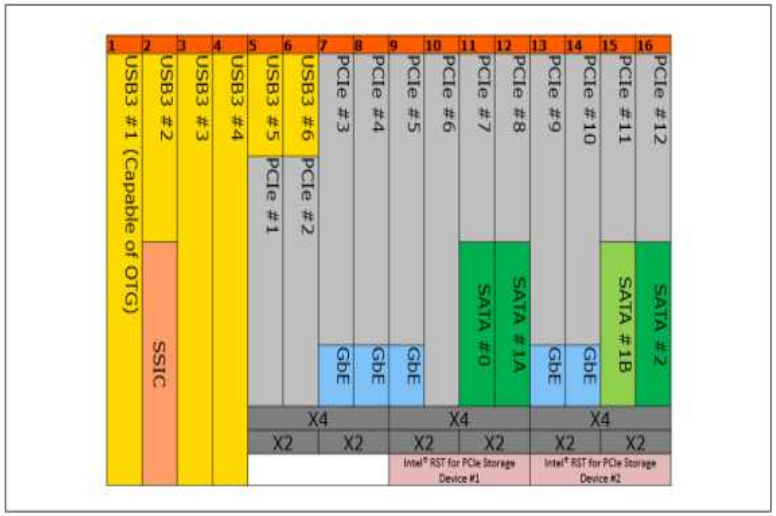
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.6
		3.8	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.7	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.6	Prepreg	1080H x2 orPP2116HRC	4.2
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.8	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.6
			Add Plating		
			SolderMask	IT-158	0.5
Overall Thickness (1.2mm ± 10%)					47.68000
					1.211072

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t
USB3.0-4				JUSB3-->Rear Lef t
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		Type-C Port
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	M.2 3042(SATA Cache or HCA)
		PCIE-9		LOM
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	JUSB3-->Rear Lef t
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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Title: Port assignment

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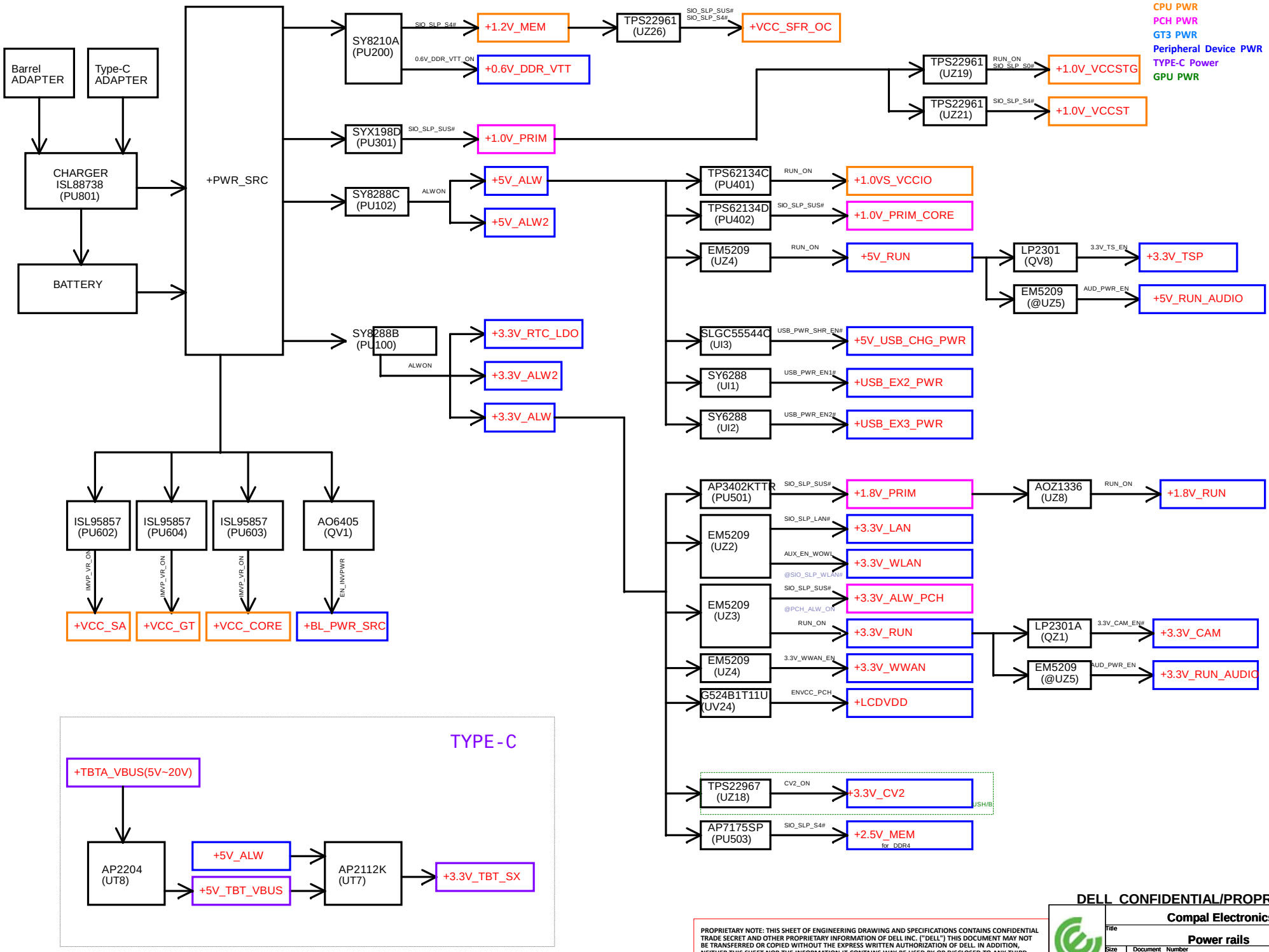

Compal Electronics, Inc.

Title: Power rails

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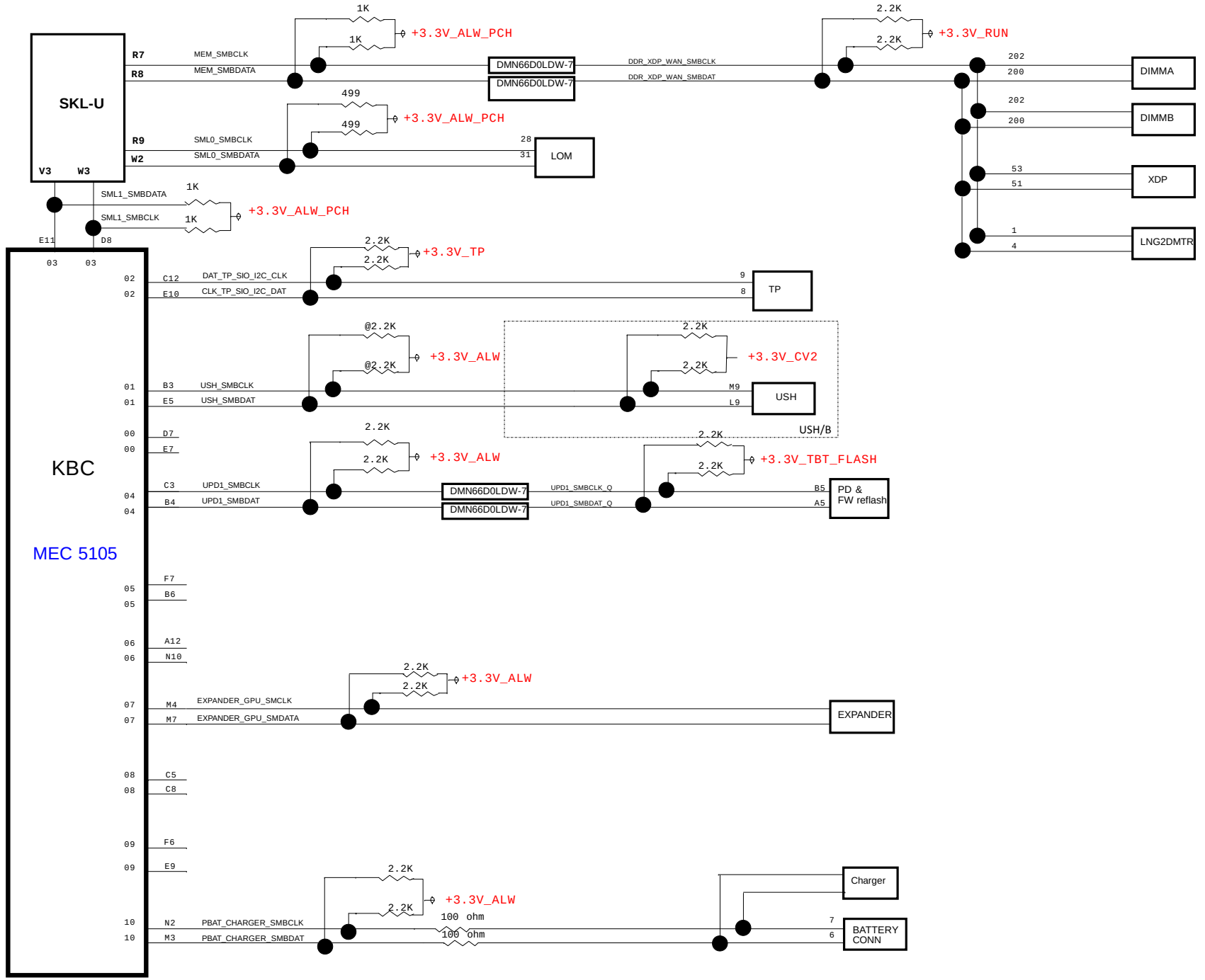
Date: Wednesday, November 30, 2016 | Sheet 4 of 64



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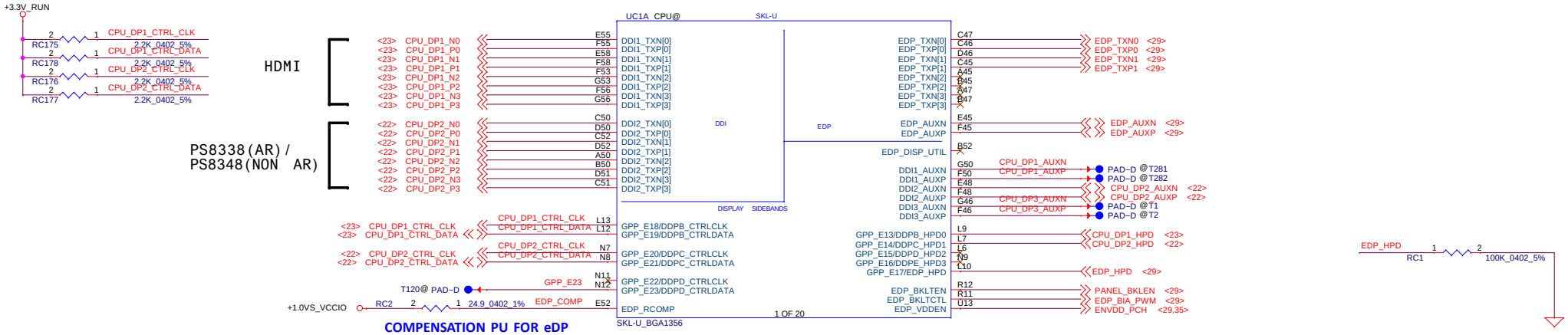
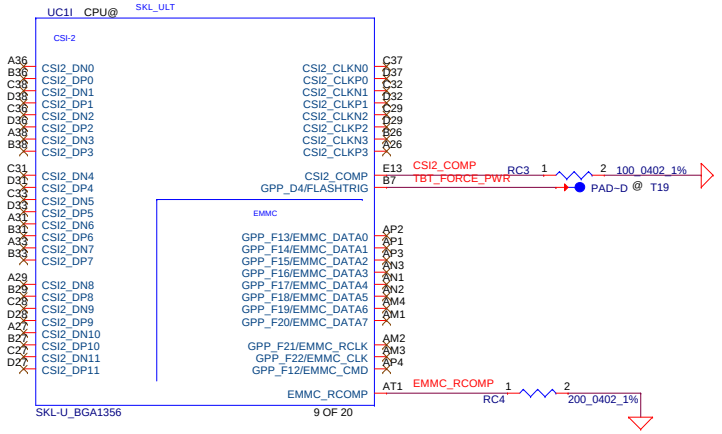
For 2LANE EDP,BR/SB12



COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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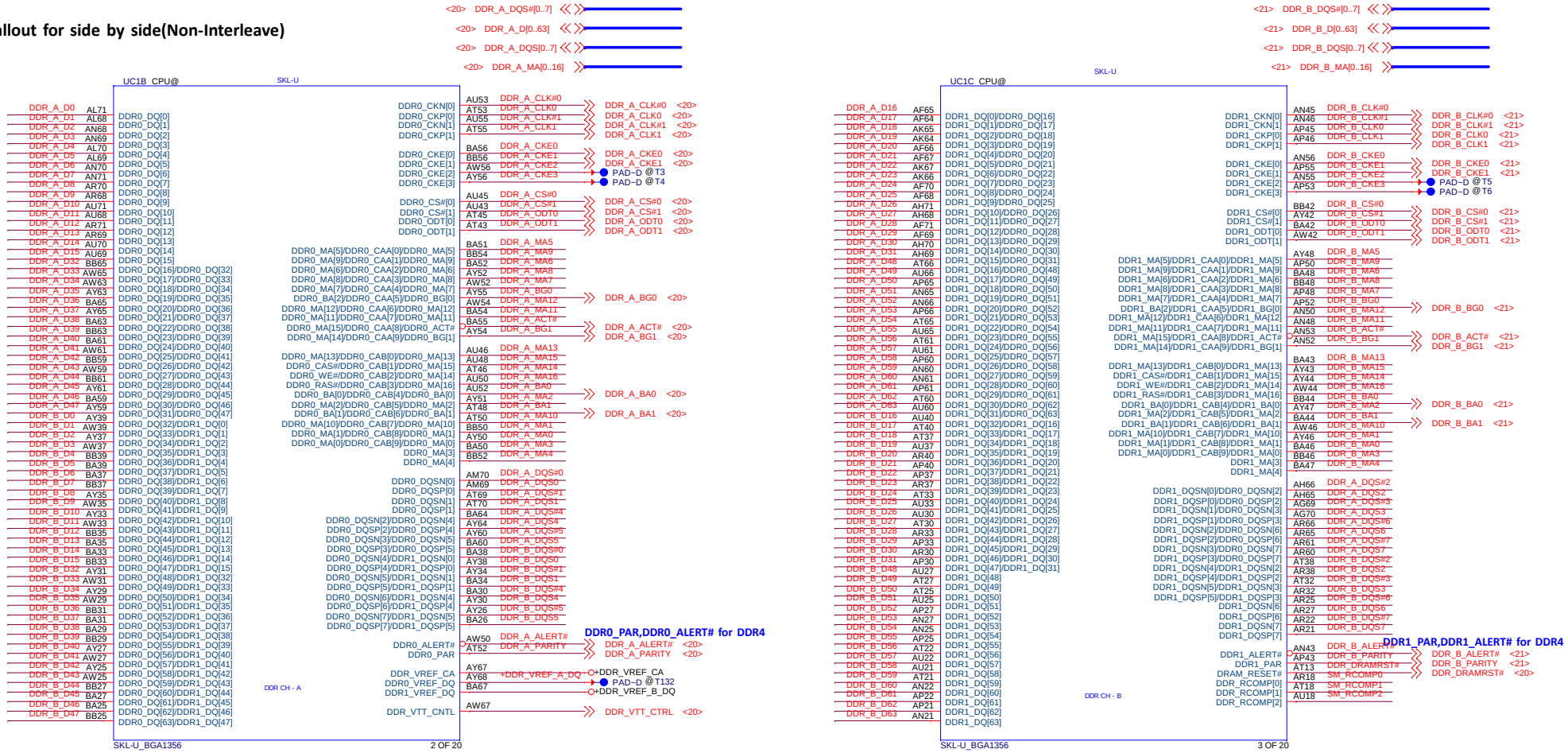
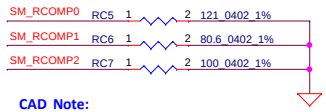
For DDR4

DDR4, Ballout for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ SKL-U

SPI - FLASH

SPI - TOUCH

C LINK

SMBUS, SMLINK

LPC

SKL-U_BGA1356

5 OF 20

SOFTWARE TAA

RF Request

Place close CPU side

128Mb Flash ROM

W25Q128FVSIQ_SO8

JSPI1

E-T_6705K-Y20N-00L

CONN@

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

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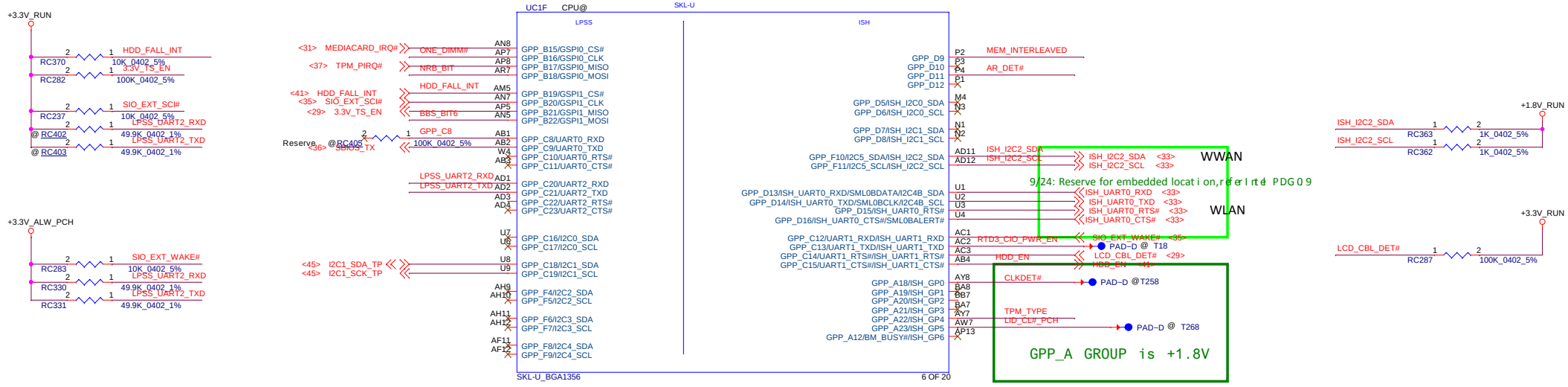
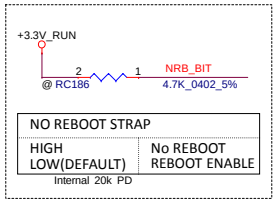
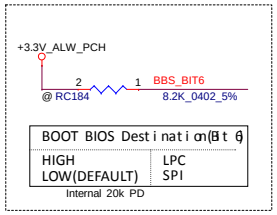
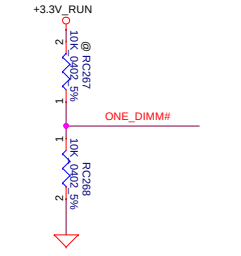
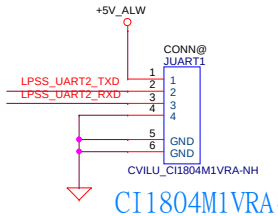
For BR/SB UMA



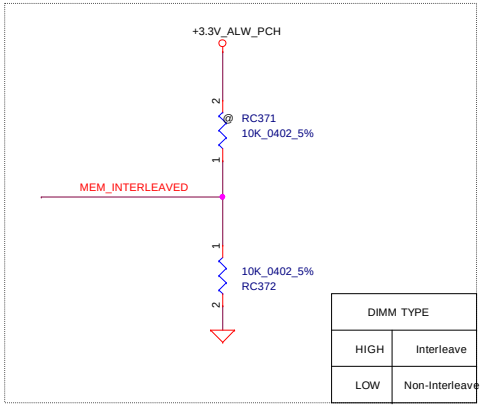


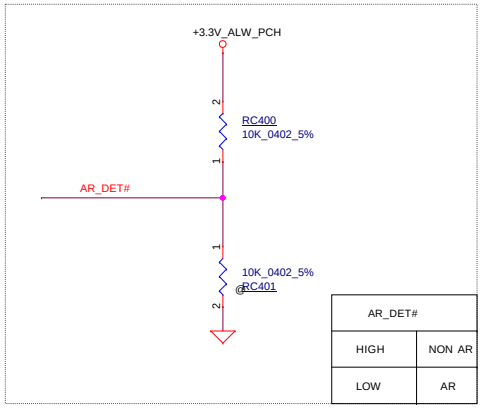


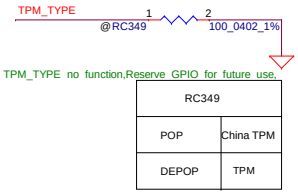




CI1804M1VRA-NH LINK DONE







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Title: CPU (4/14)

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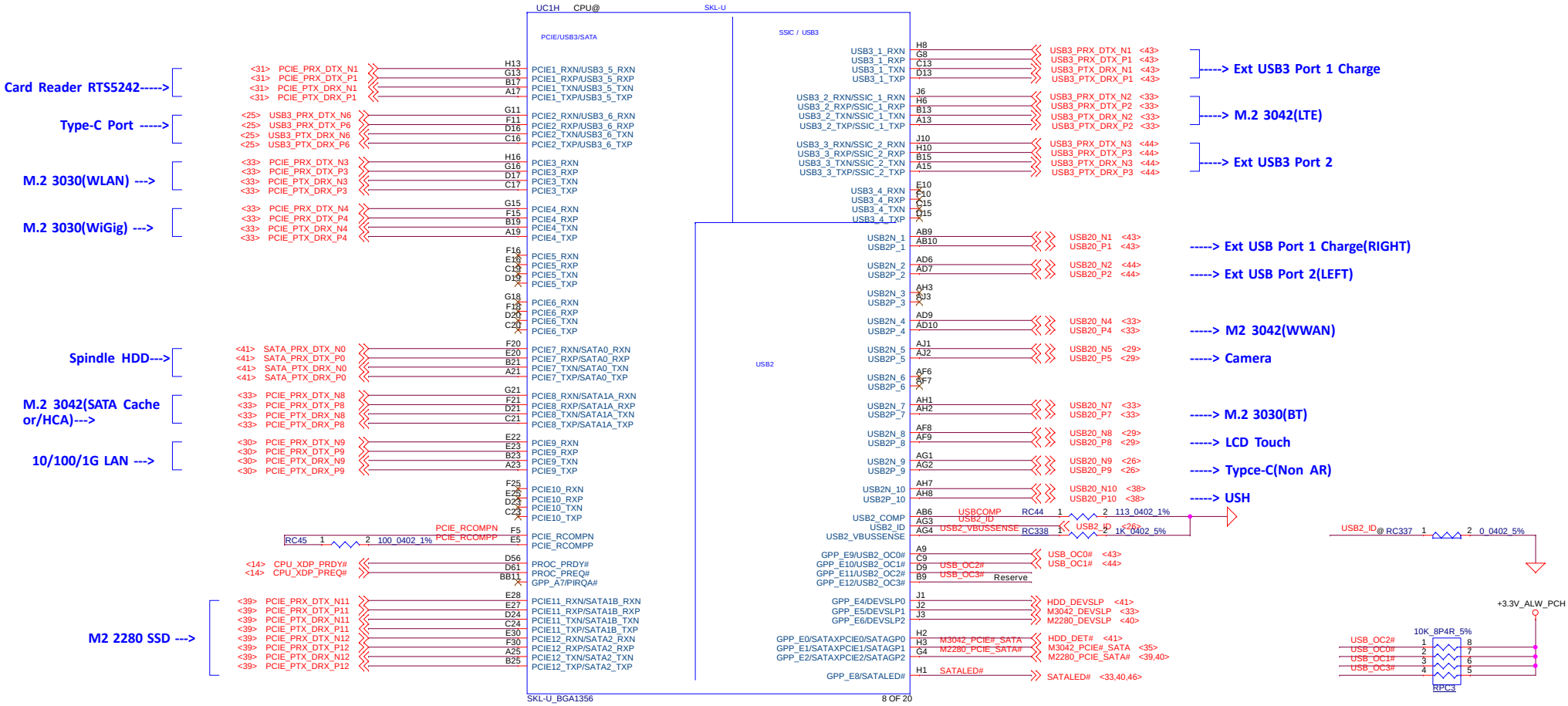
For NON AR, Breckenridge 12/14/15 UMA



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Title	CPU (5/14)
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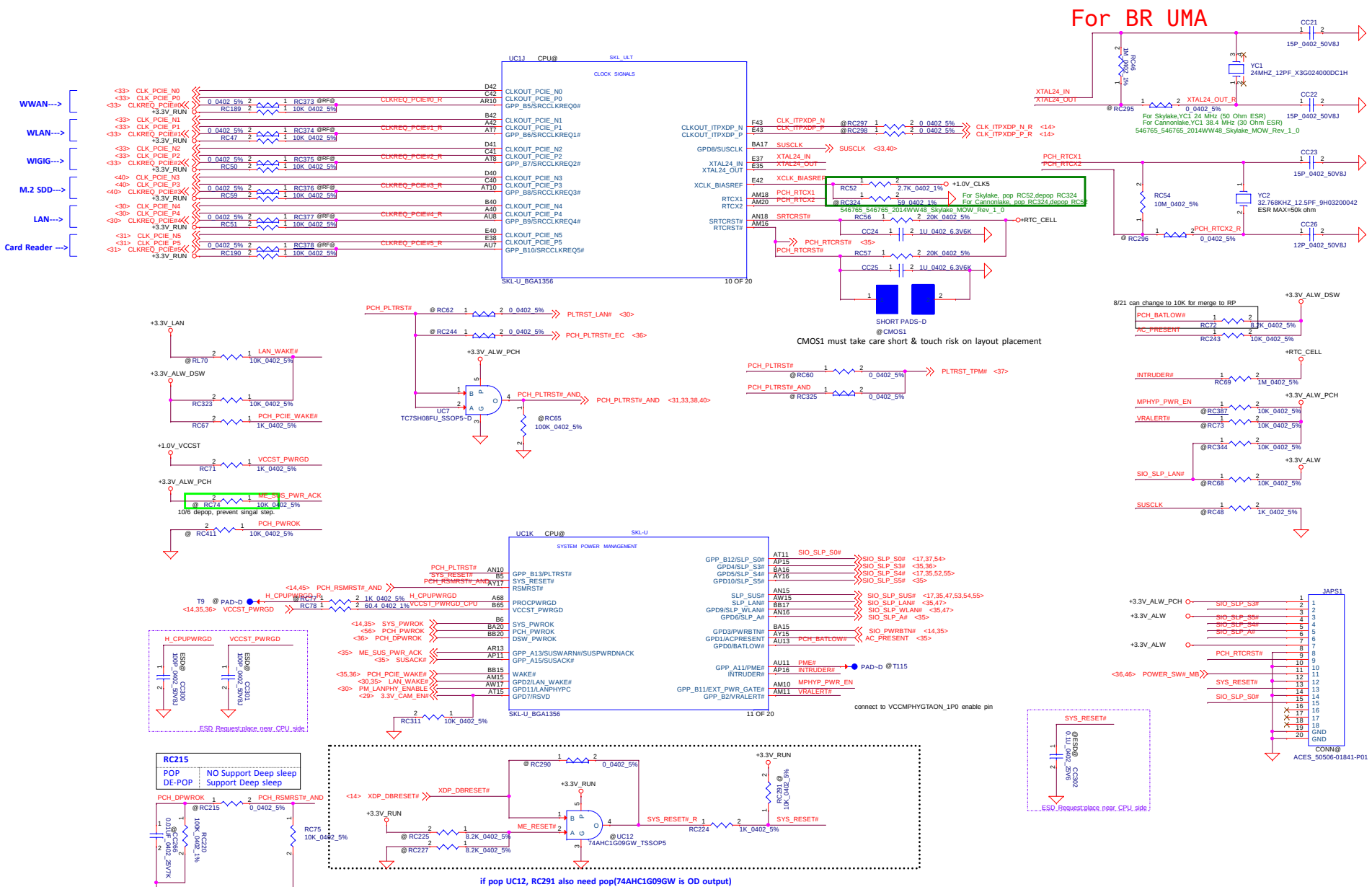
For BR UMA
WWAN--->
WLAN--->
WIGIG--->
M.2 SDD--->
LAN--->
Card Reader --->
UC1J CPU@ SKL_ULT
CLOCK SIGNALS
SKL-U_BGA1356
10 OF 20
YC1 24MHZ_12PF_X3G024000DC1H
YC2 32.768KHZ_12.5PF_9H03200042 ESR MAX=50k ohm
For Skylake,YC1 24 MHz (50 Ohm ESR)
For Cannonlake,YC1 38.4 MHz (30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0
SHORT PADS~D @CMOS1
CMOS1 must take care short & touch risk on layout placement
UC7 TC7SH08FU_SSOP5~D
UC1K CPU@ SKL-U
SYSTEM POWER MANAGEMENT
SKL-U_BGA1356
11 OF 20
connect to VCCMPHYGTAON_1P0 enable pin
ESD Request place near CPU side
RC215
POP DE-POP
NO Support Deep sleep Support Deep sleep
UC12 74AHC1G09GW_TSSOP5
if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)
JAPS1
CONN@ ACES_50506-01841-P01
8/21 can change to 10K for merge to RP
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CPU (6/14)
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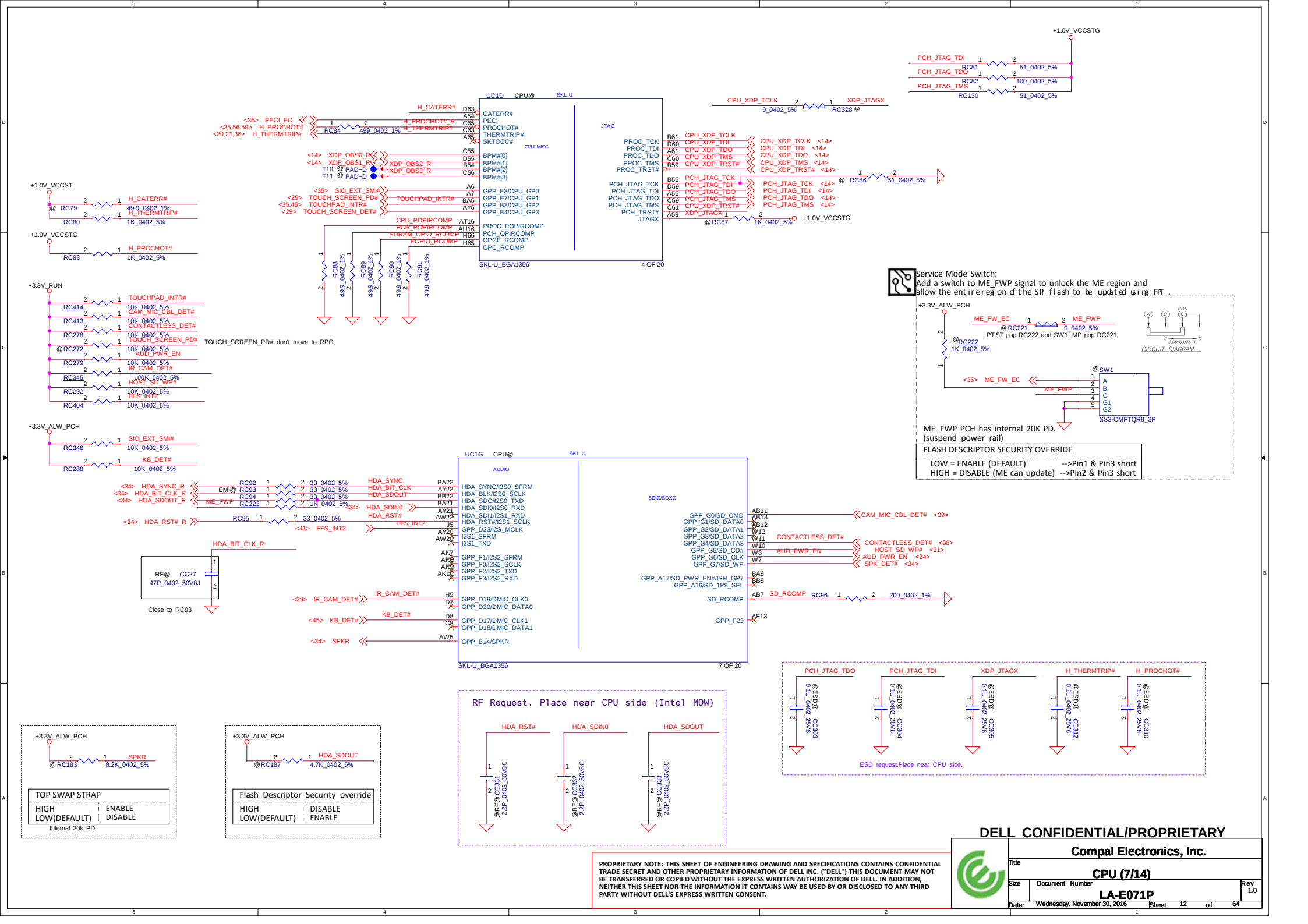

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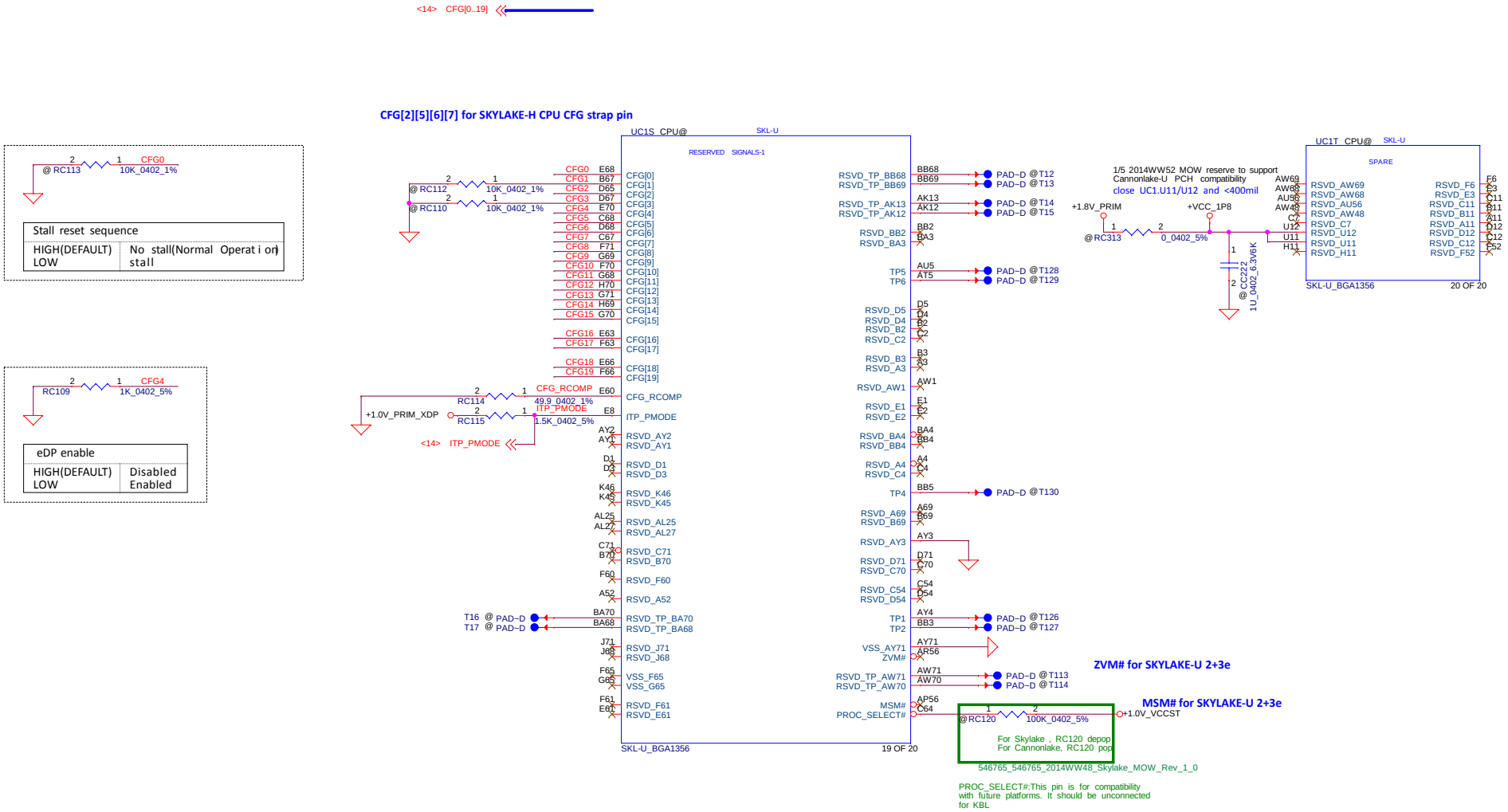

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Title: CPU (8/14)

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CPU XDP

+1.0V_PRIM
+1.0V_PRIM_XDP
@RC216 1 2 0_0603_1%

+1.0V_PRIM_XDP
0.1U_0201_10V6K @CC28
0.1U_0201_10V6K @CC29
Place near JXDP1

RC5 need to close to JCPU1

+1.0V_PRIM_XDP
XDP_PRSNT_PIN1
CXDP@ RC121 1 2 CFG3 0_0402_5%
@RC122 1 2 0_0402_5%
JXDP1
SAMTE_BSH-030-01-L-D-A CONN@

<13> CFG[0..19]

<10> CPU_XDP_PREQ#
<10> CPU_XDP_PRDY#
<12> XDP_OBS0_R
<12> XDP_OBS1_R
CXDP@ RC239 1 2 0_0402_5% XDP_OBS0
CXDP@ RC240 1 2 0_0402_5% XDP_OBS1

<11,35,36> VCCST_PWRGD
@RC123 1 2 1K_0402_5%
<11,45> PCH_RSMRST#_ANC
CXDP@ RC1241 2 1K_0402_5%
H_VCCST_PWRGD_XDP

FIVR_EN
@RC2171 2 0_0402_5%
CFG0
@RC1261 2 1K_0402_5%
<8> PCH_SPI_DO_XDP
<11,35> SYS_PWROK
CXDP@ RC1281 2 0_0402_5%
@RC1291 2 0_0402_5%
<11,35> SIO_PWRBTN#
FIVR_EN_R
RESET_OUT#_R

<8,20,21,41> DDR_XDP_WAN_SMBDAT
<8,20,21,41> DDR_XDP_WAN_SMBCLK
<12> PCH_JTAG_TCK
<12> CPU_XDP_TCLK
CPU_XDP_TCLK

CLK_ITPXDP_P_R <11>
CLK_ITPXDP_N_R <11>
ITP_PMODE
XDP_DBRESET# <13>
XDP_DBRESET# <11>
TDO_XDP
TRST#_XDP
TDI_XDP
TMS
PCH_SPI_DO2_XDP <8>

+3.3V_RUN
CC30 2 1 0.1U_0201_10V6K
UC8
74CBTLV3126BQ_DHVQFN14_2P5X3

TDO_XDP
TDI_XDP
XDP_TMS
TRST#_XDP
<35> RUNPWROK

CPU_XDP_TDO <12>
CPU_XDP_TDI <12>
CPU_XDP_TMS <12>
CPU_XDP_TRST# <12>

+1.0VS_VCCIO
RC132 2 1 FIVR_EN_R 150_0402_5%
+1.0V_VCCST
@RC218 2 1 FIVR_EN 150_0402_5%
@RC219 2 1 FIVR_EN 10K_0402_5%

+3.3V_RUN
RC137 2 1 XDP_DBRESET# 3K_0402_5%
+1.0V_PRIM_XDP
@RC138 2 1 CPU_XDP_PREQ# 51_0402_5%

+3.3V_ALW_PCH
CXDP@RC133 1.5K_0402_5%
PCH_SPI_DO_XDP
RESET_OUT#_R
0.1U_0402_25V6 @CC33
Place near JXDP1.47

Place near JXDP1.48
XDP_DBRESET#
CXDP@ CC32 0.1U_0402_25V6

+3.3V_ALW_DSW
1.5K_0402_5% @RC241
SIO_PWRBTN#
0.1U_0402_25V6 @CC269
Place near JXDP1.41

+1.0V_VCCSTG
CPU_XDP_TMS RC131 1 2 51_0402_5%
CPU_XDP_TDI RC134 1 2 51_0402_5%
CPU_XDP_TDO RC135 1 2 100_0402_5%
CPU_XDP_TRST# @RC136 1 2 51_0402_5%
CPU_XDP_TCLK RC139 1 2 51_0402_5%

XDP_TMS @RC228 1 2 0_0402_5% PCH_JTAG_TMS <12>
TDI_XDP @RC229 1 2 0_0402_5% PCH_JTAG_TDI <12>
TDO_XDP @RC230 1 2 0_0402_5% PCH_JTAG_TDO <12>

TDO_XDP
@ESD@ 0.1U_0402_25V6 CC306
ESD request,Place near JXDP1 side.

H_VCCST_PWRGD_XDP
@ESD@ 0.1U_0402_25V6 CC307

CPU_XDP_TRST#
@ESD@ 0.1U_0402_25V6 CC308
ESD request,Place near UC8 side.

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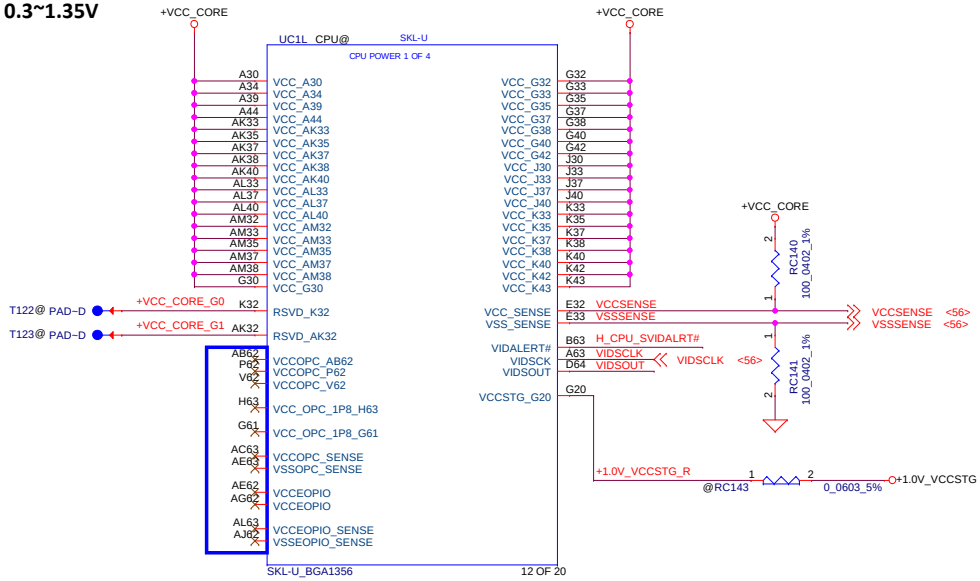
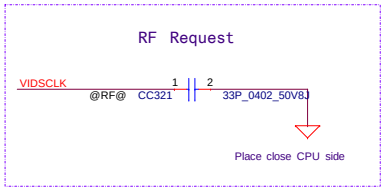
+VCC_CORE: 0.3~1.35V

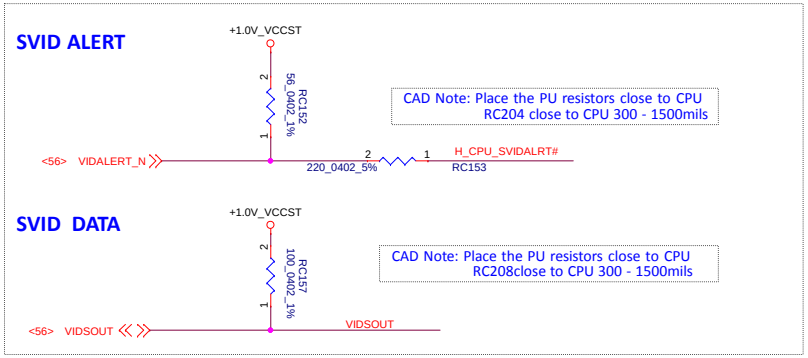


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e (w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source





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Title: CPU (10/14)

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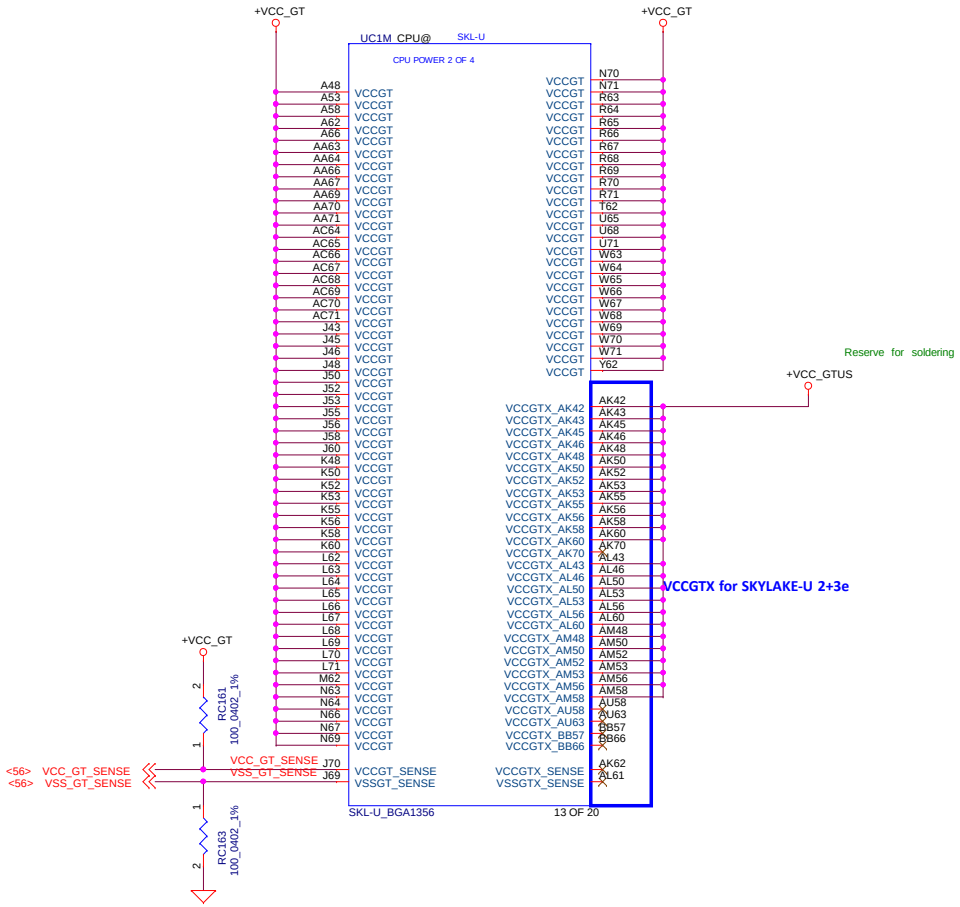
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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Title: CPU (11/14)

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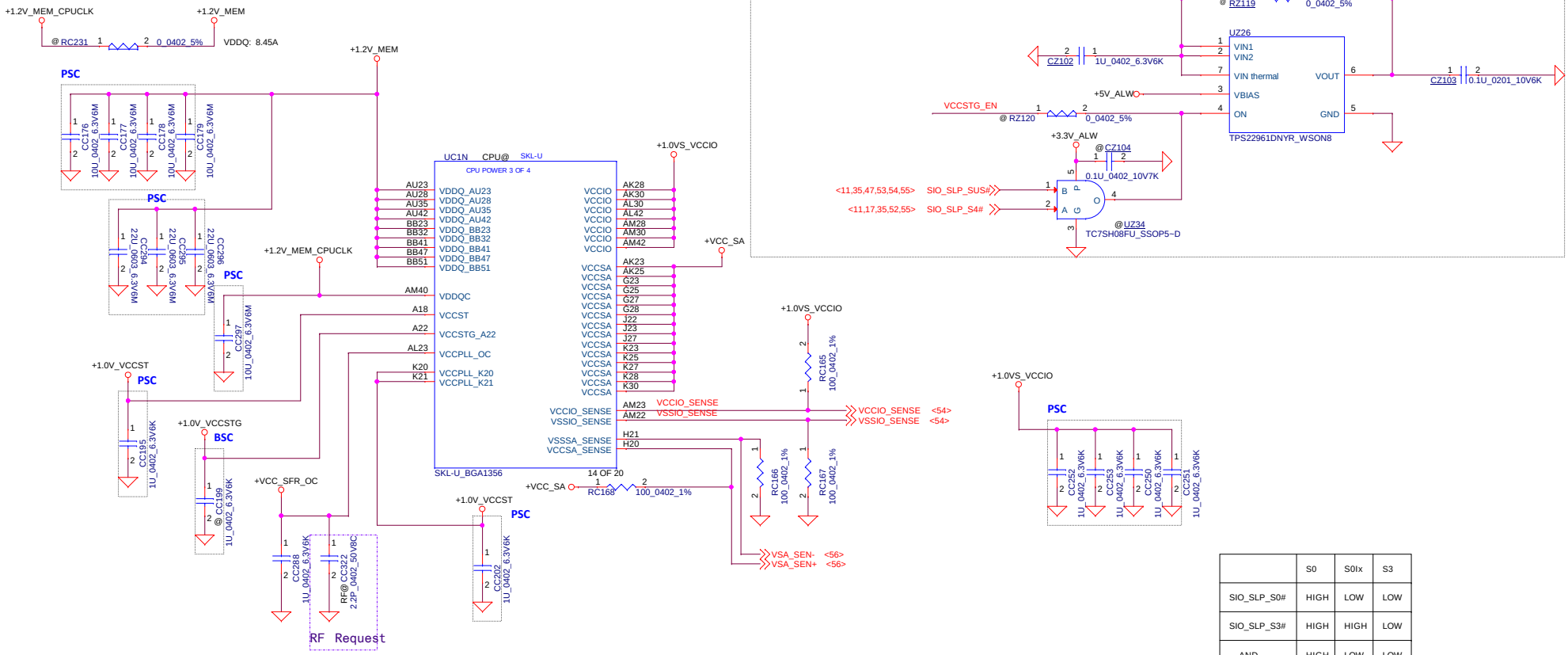
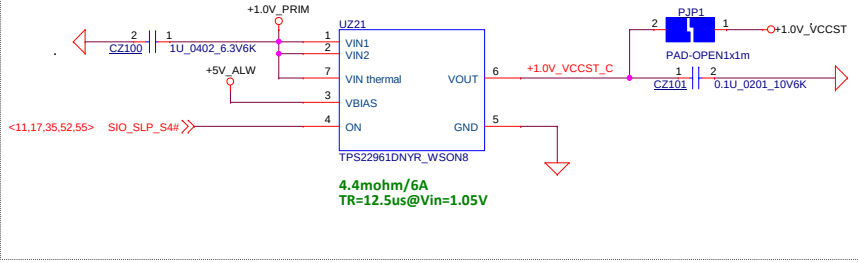


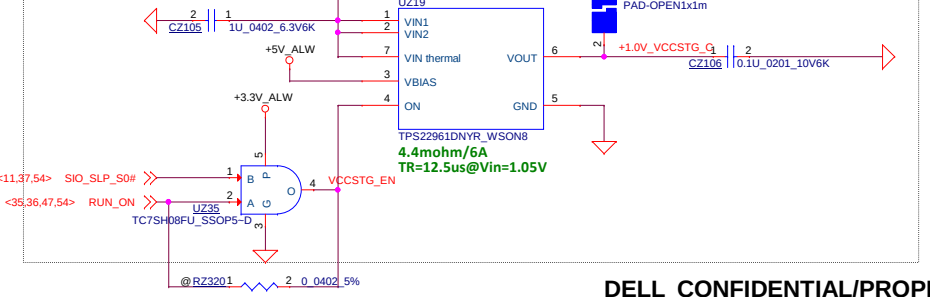
+VCCPLL_OC source

	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

+1.0V_VCCST source



+1.0V_VCCSTG source



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Title: CPU (12/14)

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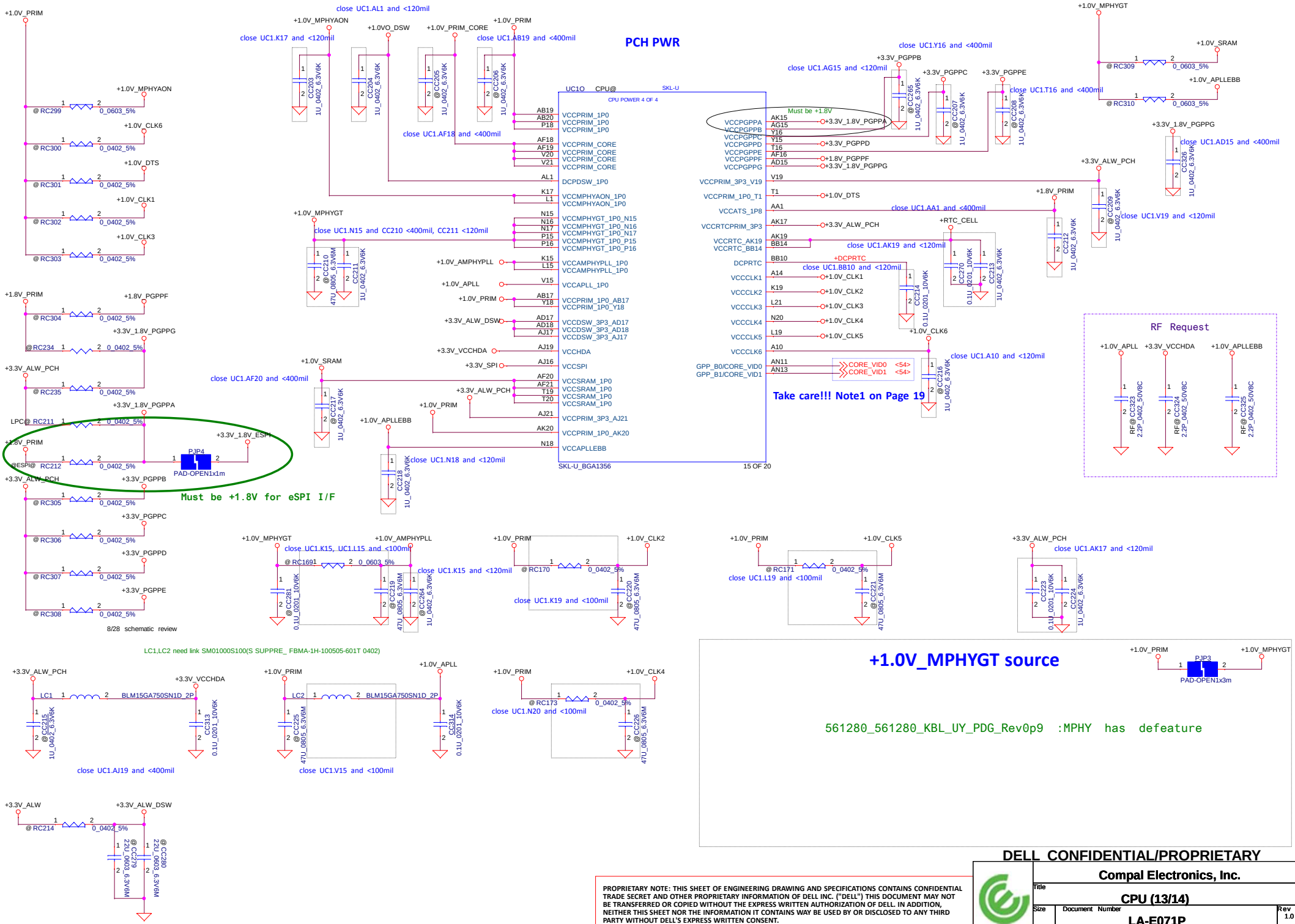
PCH PWR
UC1O CPU@ SKL-U
CPU POWER 4 OF 4
SKL-U_BGA1356
15 OF 20
close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.AF18 and <400mil
close UC1.N15 and CC210 <400mil, CC211 <120mil
close UC1.AF20 and <400mil
close UC1.N18 and <120mil
close UC1.Y16 and <400mil
close UC1.AG15 and <120mil
close UC1.T16 and <400mil
close UC1.AD15 and <400mil
close UC1.AA1 and <400mil
close UC1.V19 and <120mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
Must be +1.8V
+DCPRTC
Take care!!! Note1 on Page 19
Must be +1.8V for eSPI I/F
RF Request
close UC1.K15, UC1.L15 and <100mil
close UC1.K15 and <120mil
close UC1.K19 and <100mil
close UC1.L19 and <100mil
close UC1.AK17 and <120mil
close UC1.AJ19 and <400mil
close UC1.V15 and <100mil
close UC1.N20 and <100mil
LC1,LC2 need link SM01000S100(S SUPPRE_ FBMA-1H-100505-601T 0402)
8/28 schematic review
+1.0V_MPHYGT source
561280_561280_KBL_UY_PDG_Rev0p9 :MPHY has defeature
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CPU (13/14)
LA-E071P
Rev 1.0
Wednesday, November 30, 2016
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CPU@
UC1P SKL-U

GND 1 OF 3

A5	VSS	VSS	AL65
A67	VSS	VSS	AL66
A70	VSS	VSS	AM13
AA2	VSS	VSS	AM21
AA4	VSS	VSS	AM25
AA65	VSS	VSS	AM27
AA68	VSS	VSS	AM43
AB15	VSS	VSS	AM45
AB16	VSS	VSS	AM46
AB18	VSS	VSS	AM55
AB21	VSS	VSS	AM60
AB8	VSS	VSS	AM61
AD13	VSS	VSS	AM68
AD16	VSS	VSS	AM71
AD19	VSS	VSS	AM8
AD20	VSS	VSS	AN20
AD21	VSS	VSS	AN23
AD62	VSS	VSS	AN28
AD8	VSS	VSS	AN30
AE64	VSS	VSS	AN32
AE65	VSS	VSS	AN33
AE66	VSS	VSS	AN35
AE67	VSS	VSS	AN37
AE68	VSS	VSS	AN38
AE69	VSS	VSS	AN40
AF1	VSS	VSS	AN42
AF10	VSS	VSS	AN58
AF15	VSS	VSS	AN63
AF17	VSS	VSS	AP10
AF2	VSS	VSS	AP18
AF4	VSS	VSS	AP20
AF63	VSS	VSS	AP23
AG16	VSS	VSS	AP28
AG17	VSS	VSS	AP32
AG18	VSS	VSS	AP35
AG19	VSS	VSS	AP38
AG20	VSS	VSS	AP42
AG21	VSS	VSS	AP58
AG71	VSS	VSS	AP63
AH13	VSS	VSS	AP68
AH6	VSS	VSS	AP70
AH63	VSS	VSS	AR11
AH64	VSS	VSS	AR15
AH67	VSS	VSS	AR16
AJ15	VSS	VSS	AR20
AJ18	VSS	VSS	AR23
AJ20	VSS	VSS	AR28
AJ4	VSS	VSS	AR35
AK11	VSS	VSS	AR42
AK16	VSS	VSS	AR43
AK18	VSS	VSS	AR45
AK21	VSS	VSS	AR46
AK22	VSS	VSS	AR48
AK27	VSS	VSS	AR5
AK63	VSS	VSS	AR50
AK68	VSS	VSS	AR52
AK69	VSS	VSS	AR53
AK8	VSS	VSS	AR55
AL2	VSS	VSS	AR58
AL28	VSS	VSS	AR63
AL32	VSS	VSS	AR8
AL35	VSS	VSS	AT2
AL38	VSS	VSS	AT20
AL4	VSS	VSS	AT23
AL45	VSS	VSS	AT28
AL48	VSS	VSS	AT35
AL52	VSS	VSS	AT4
AL55	VSS	VSS	AT42
AL58	VSS	VSS	AT56
AL64	VSS	VSS	AT58

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CPU@
UC1Q SKL-U

GND 2 OF 3

AT63	VSS	VSS	BA49
AT68	VSS	VSS	BA53
AT71	VSS	VSS	BA57
AU10	VSS	VSS	BA6
AU15	VSS	VSS	BA62
AU20	VSS	VSS	BA66
AU32	VSS	VSS	BA71
AU38	VSS	VSS	BB18
AV1	VSS	VSS	BB26
AV68	VSS	VSS	BB30
AV69	VSS	VSS	BB34
AV70	VSS	VSS	BB38
AV71	VSS	VSS	BB43
AW10	VSS	VSS	BB55
AW12	VSS	VSS	BB6
AW14	VSS	VSS	BB60
AW16	VSS	VSS	BB64
AW18	VSS	VSS	BB67
AW21	VSS	VSS	BB70
AW23	VSS	VSS	C1
AW26	VSS	VSS	C25
AW28	VSS	VSS	C5
AW30	VSS	VSS	D10
AW32	VSS	VSS	D11
AW34	VSS	VSS	D14
AW36	VSS	VSS	D18
AW38	VSS	VSS	D22
AW41	VSS	VSS	D25
AW43	VSS	VSS	D26
AW45	VSS	VSS	D30
AW47	VSS	VSS	D34
AW49	VSS	VSS	D39
AW51	VSS	VSS	D44
AW53	VSS	VSS	D45
AW55	VSS	VSS	D47
AW57	VSS	VSS	D48
AW6	VSS	VSS	D53
AW60	VSS	VSS	D58
AW62	VSS	VSS	D6
AW64	VSS	VSS	D62
AW66	VSS	VSS	D66
AW8	VSS	VSS	D69
AY66	VSS	VSS	E11
B10	VSS	VSS	E15
B14	VSS	VSS	E18
B18	VSS	VSS	E21
B22	VSS	VSS	E46
B30	VSS	VSS	E50
B34	VSS	VSS	E53
B39	VSS	VSS	E56
B44	VSS	VSS	E6
B48	VSS	VSS	E65
B53	VSS	VSS	E71
B58	VSS	VSS	F1
B62	VSS	VSS	F13
B66	VSS	VSS	F2
B71	VSS	VSS	F22
BA1	VSS	VSS	F23
BA10	VSS	VSS	F27
BA14	VSS	VSS	F28
BA18	VSS	VSS	F32
BA2	VSS	VSS	F33
BA23	VSS	VSS	F35
BA28	VSS	VSS	F37
BA32	VSS	VSS	F38
BA36	VSS	VSS	F4
F68	VSS	VSS	F40
BA45	VSS	VSS	F42
		VSS	BA41

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CPU@
UC1R SKL-U

GND 3 OF 3

F8	VSS	VSS	L18
G10	VSS	VSS	L2
G22	VSS	VSS	L20
G43	VSS	VSS	L4
G45	VSS	VSS	L8
G48	VSS	VSS	N10
G5	VSS	VSS	N13
G52	VSS	VSS	N19
G55	VSS	VSS	N21
G58	VSS	VSS	N6
G6	VSS	VSS	N65
G60	VSS	VSS	N68
G63	VSS	VSS	P17
G66	VSS	VSS	P19
H15	VSS	VSS	P20
H18	VSS	VSS	P21
H71	VSS	VSS	R13
J11	VSS	VSS	R6
J13	VSS	VSS	T15
J25	VSS	VSS	T17
J28	VSS	VSS	T18
J32	VSS	VSS	T2
J35	VSS	VSS	T21
J38	VSS	VSS	T4
J42	VSS	VSS	U10
J8	VSS	VSS	U63
K16	VSS	VSS	U64
K18	VSS	VSS	U66
K22	VSS	VSS	U67
K61	VSS	VSS	U69
K63	VSS	VSS	U70
K64	VSS	VSS	V16
K65	VSS	VSS	V17
K66	VSS	VSS	V18
K67	VSS	VSS	W13
K68	VSS	VSS	W6
K70	VSS	VSS	W9
K71	VSS	VSS	Y17
L11	VSS	VSS	Y19
L16	VSS	VSS	Y20
L17	VSS	VSS	Y21

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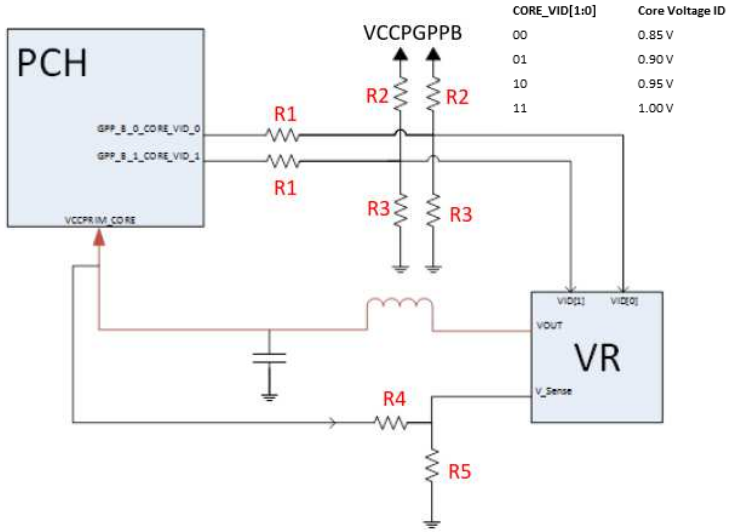
Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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Title: CPU (14/14)

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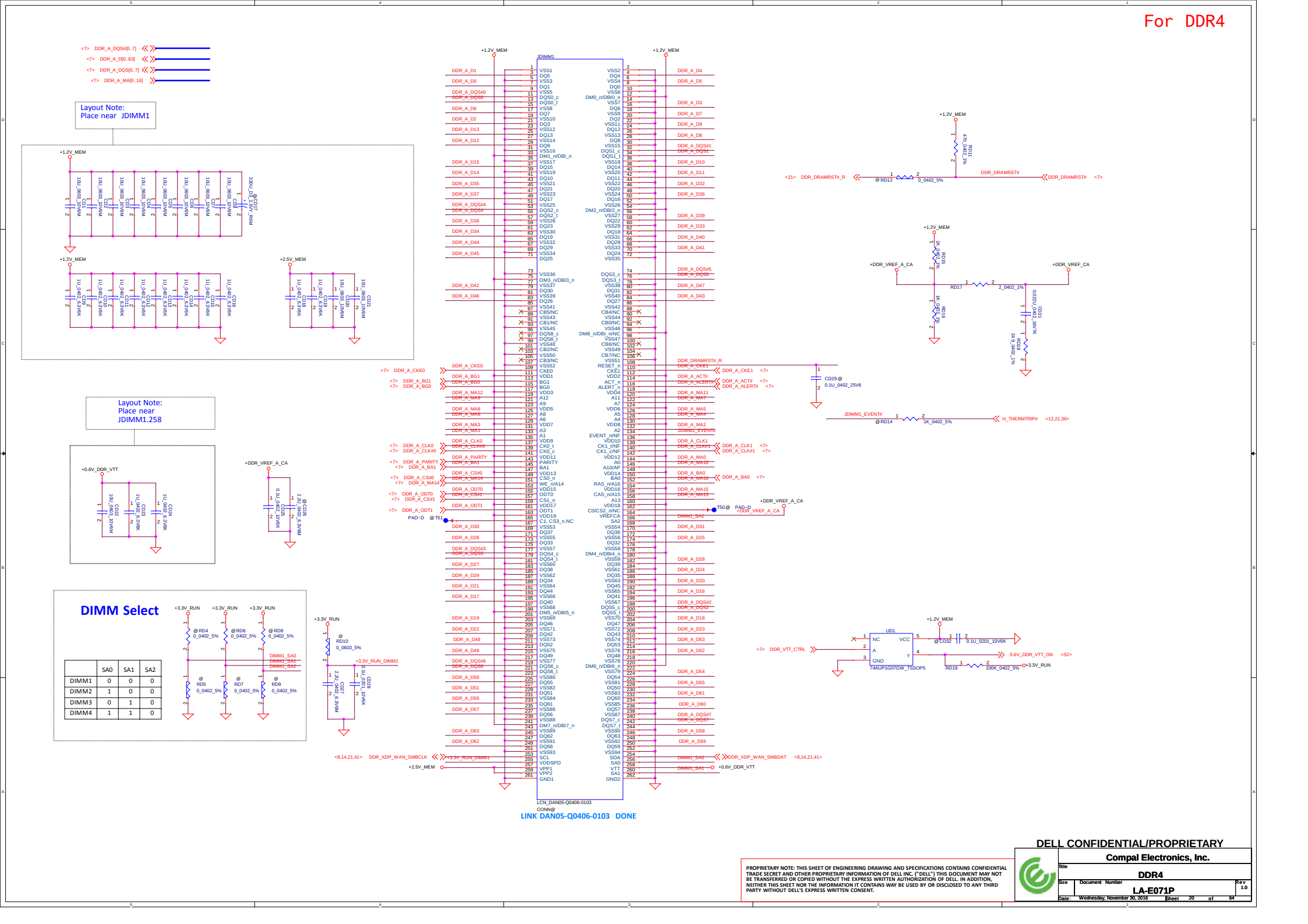
For DDR4



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Title: DDR4

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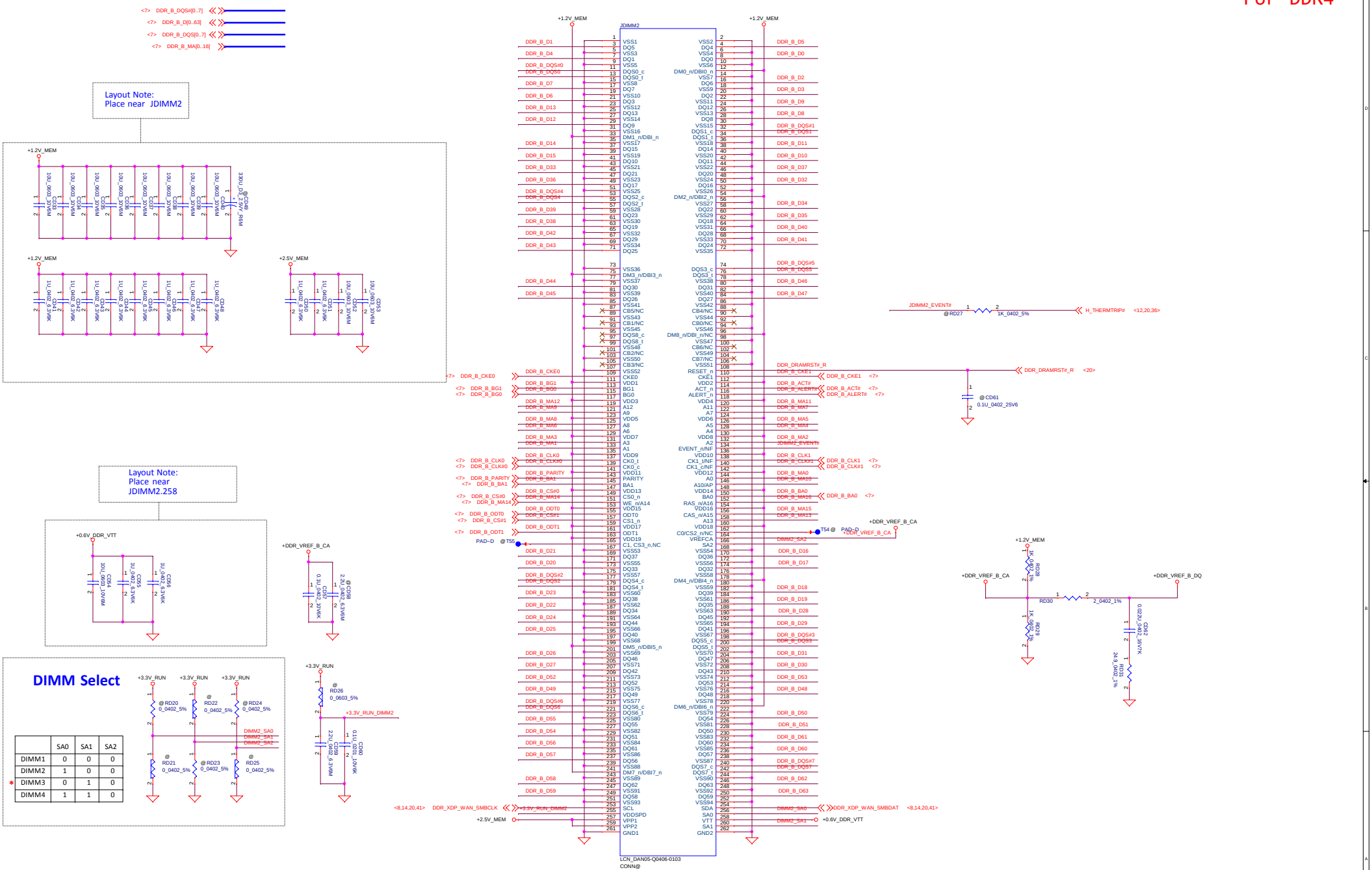
Date: Wednesday, November 30, 2016 Sheet 20 of 64

For DDR4



	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0

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Title: DDR4

Size: Document Number: LA-E071P Rev: 1.0

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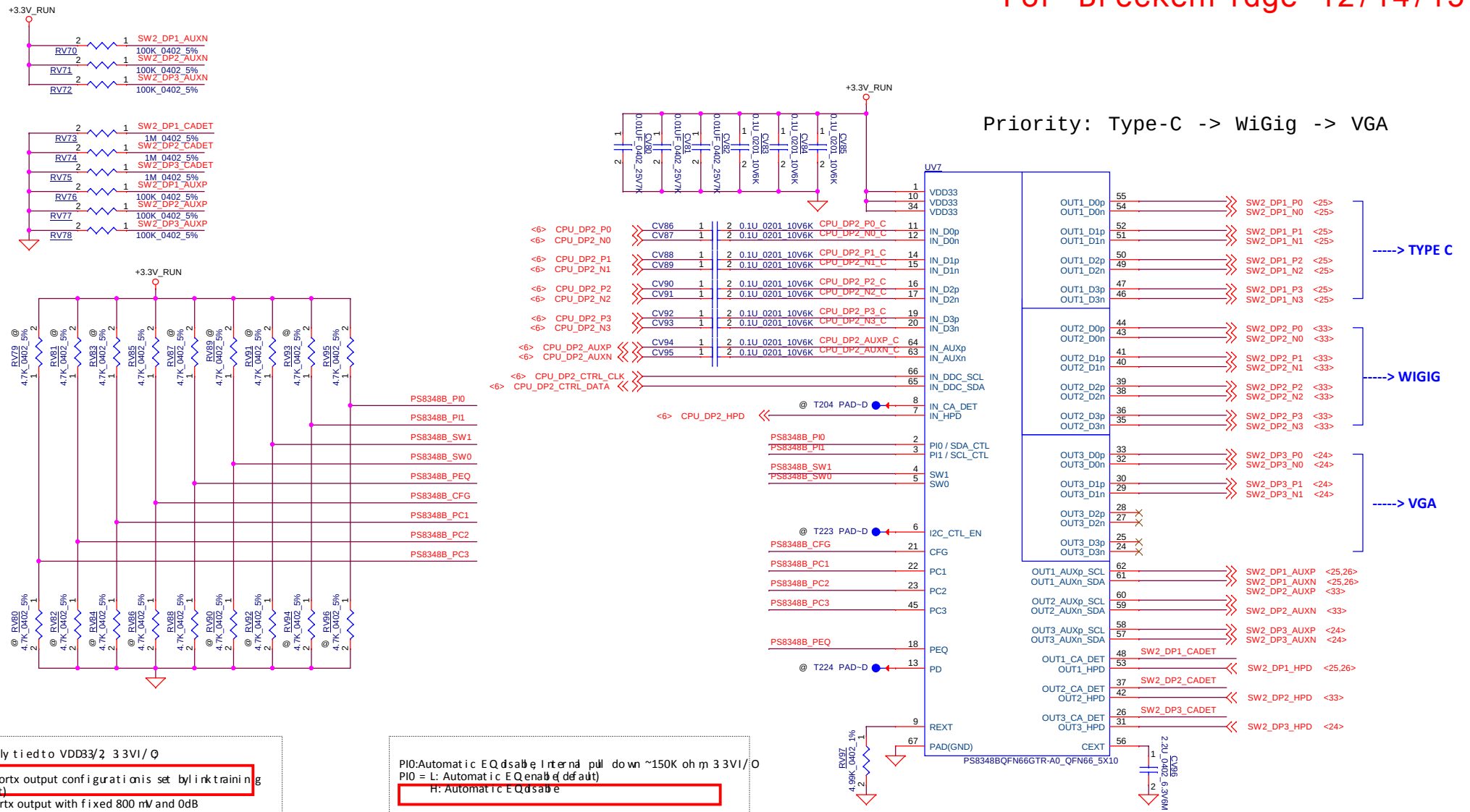
For Breckenridge 12/14/15



Internally tied to VDD33/2, 3.3V I/O
PCx =
M:Portx output configuration is set by link training (default)
H:Portx output with fixed 800 mV and 0dB
L:Portx output with fixed 400 mV and 0dB
x=1, 2, 3

PI0:Automatic EQ disable, Internal pull down ~150K ohm 3.3V I/O
PI0 = L: Automatic EQ enable (default)
H: Automatic EQ disable

Internally pull down ~150K.3.3V I/O
For Control Switching Mode (CFG = L):
[SW1,SW0]= [L,L], Port1 is selected (default)
[SW1,SW0]= [L,H], Port2 is selected
[SW1,SW0]= [H,L], Port3 is selected
[SW1,SW0]= [H,H], Port3 is selected
For Automatic Switching Mode (CFG0= H):
[SW1,SW0]= [L,L], Port1 >Port2 >Port3 (default)
[SW1,SW0]= [L,H], Port1 >Port3 >Port2
[SW1,SW0]= [H,L], Port3 >Port2 >Port1
[SW1,SW0]= [H,H], Port3 >Port1 >Port2
[SW1,SW0]= [L,M], Port2 >Port1 >Port3
[SW1,SW0]= [M,M], Port2 >Port3 >Port1

Internally tied to VDD33/2, 3.3V I/O
PEQ =
M:default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H:HEQ, compensate channel loss up to 14.5dB @ HBR2
L:LLEQ, compensate channel loss up to 8.5dB @ HBR2

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Title: DP SW2 PS8348B

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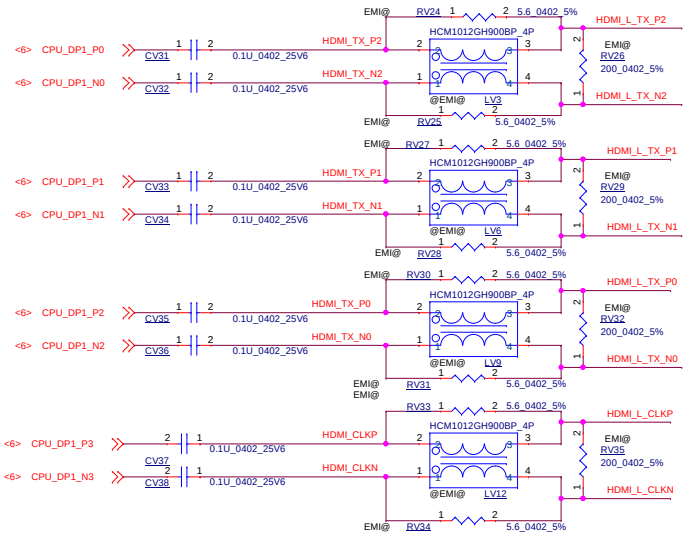
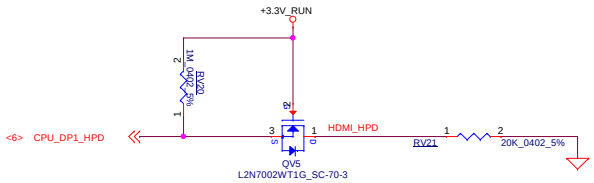
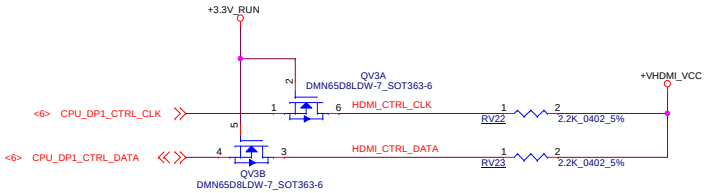
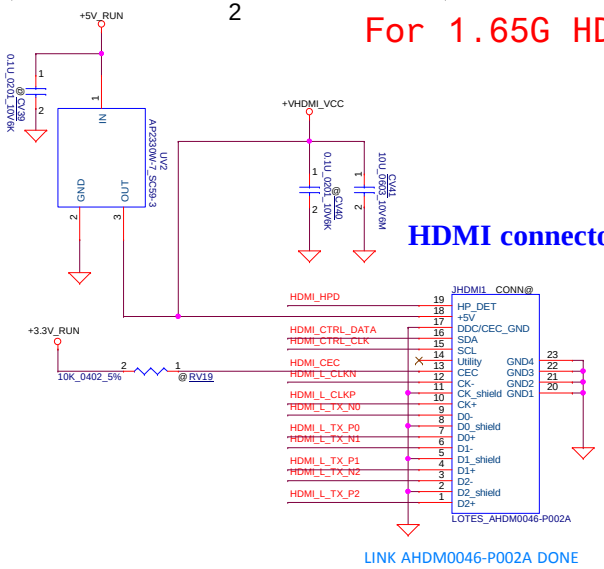
For 1.65G HDMI from CPU

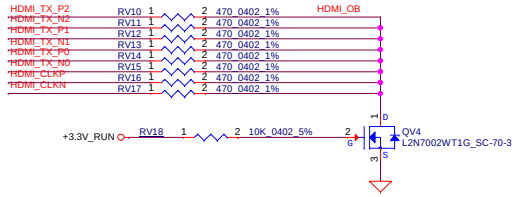








LINK AHDM0046-P002A DONE



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Title: HDMI CONN

Size: | Document Number: LA-E071P | Rev: 1.0

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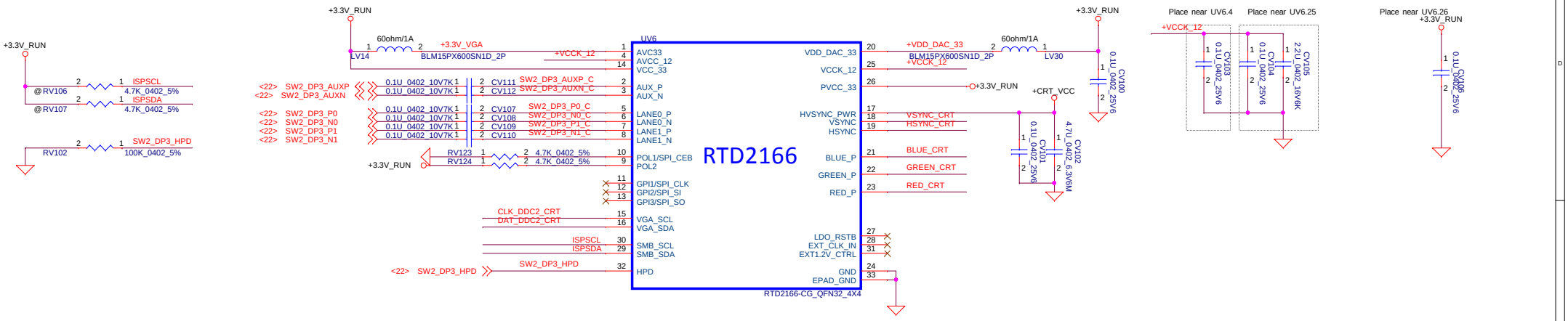
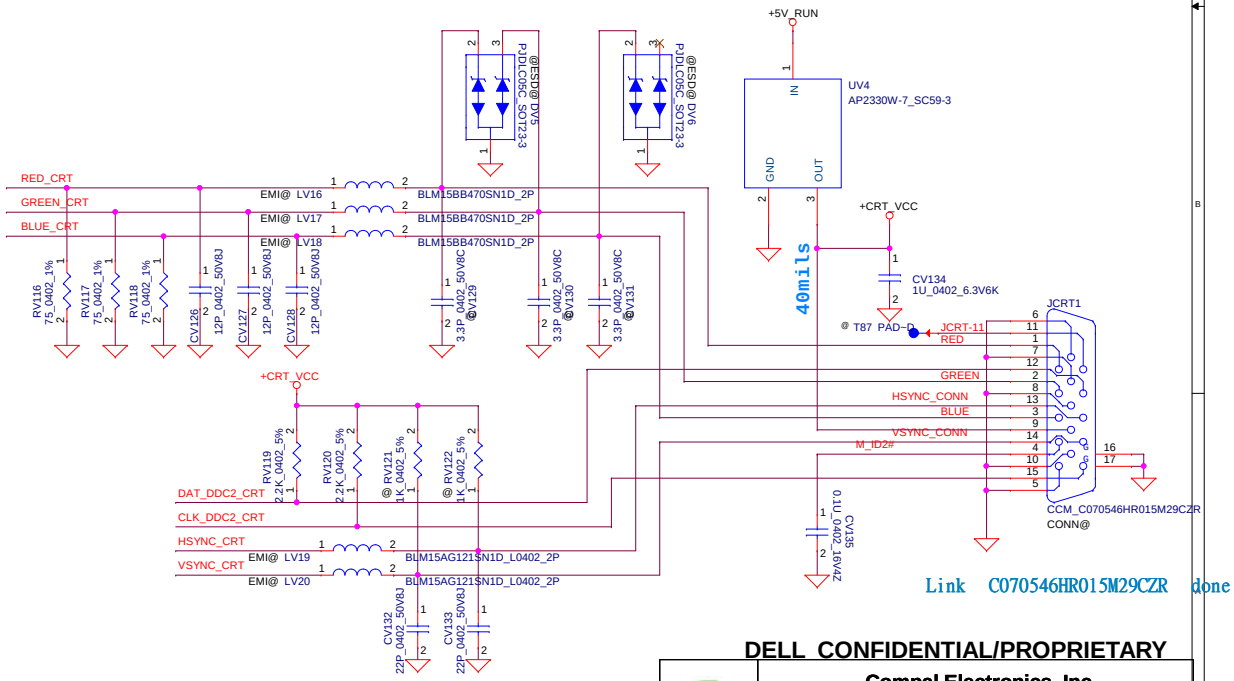
For Breckenridge 12/14/15
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



Link C070546HR015M29CZR done

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Title: DP to VGA & VGA Conn

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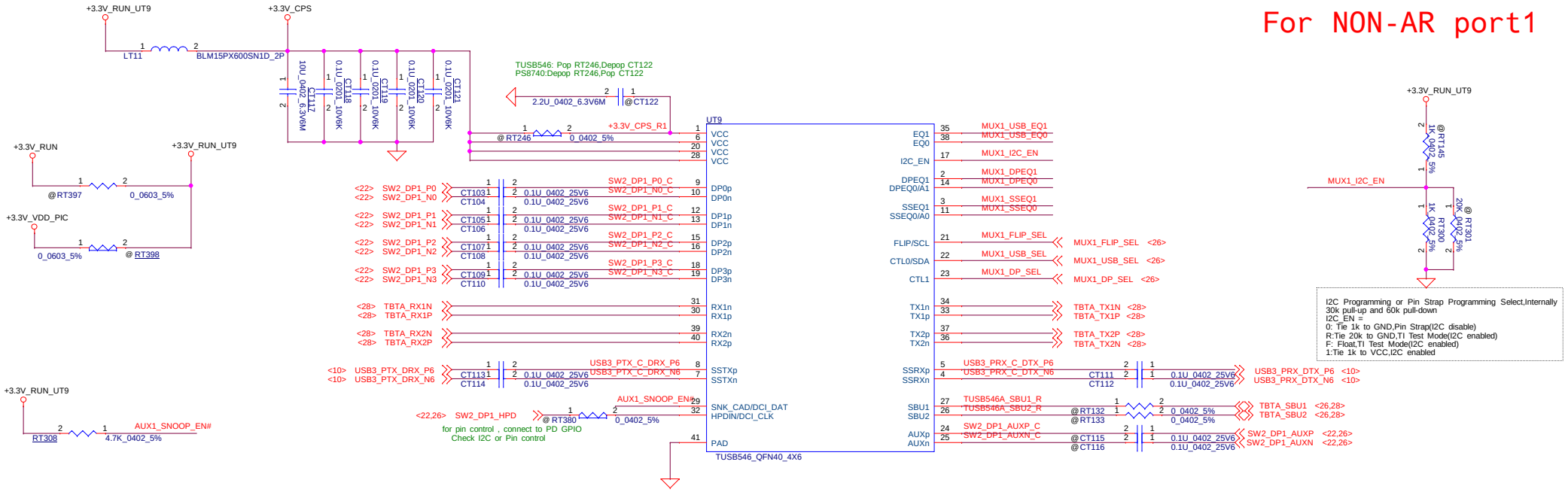
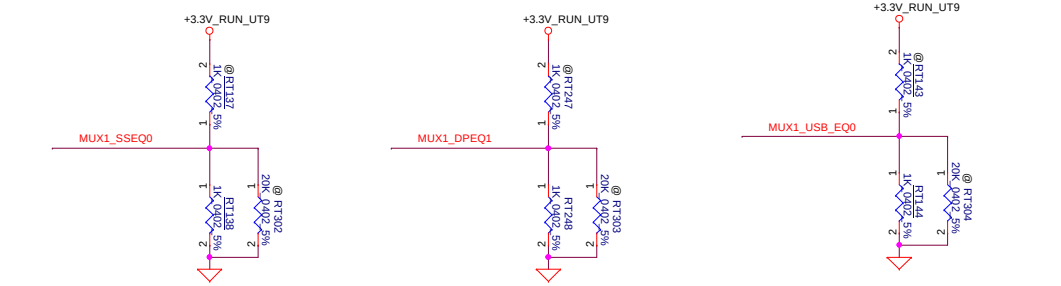
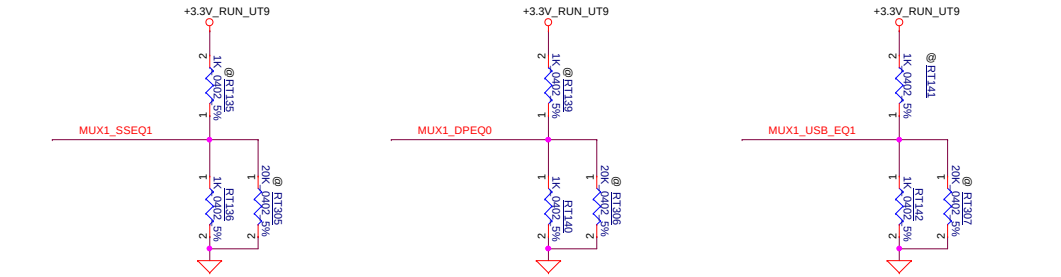
For NON-AR port1







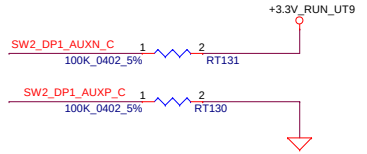


Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Compal Electronics, Inc.

Title: DP/USB3 Repeater SW TUSB546

Size: | Document Number: LA-E071P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 25 of 64

For NON-AR port1

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Route in pass through manner so AUX can be snooped by 546

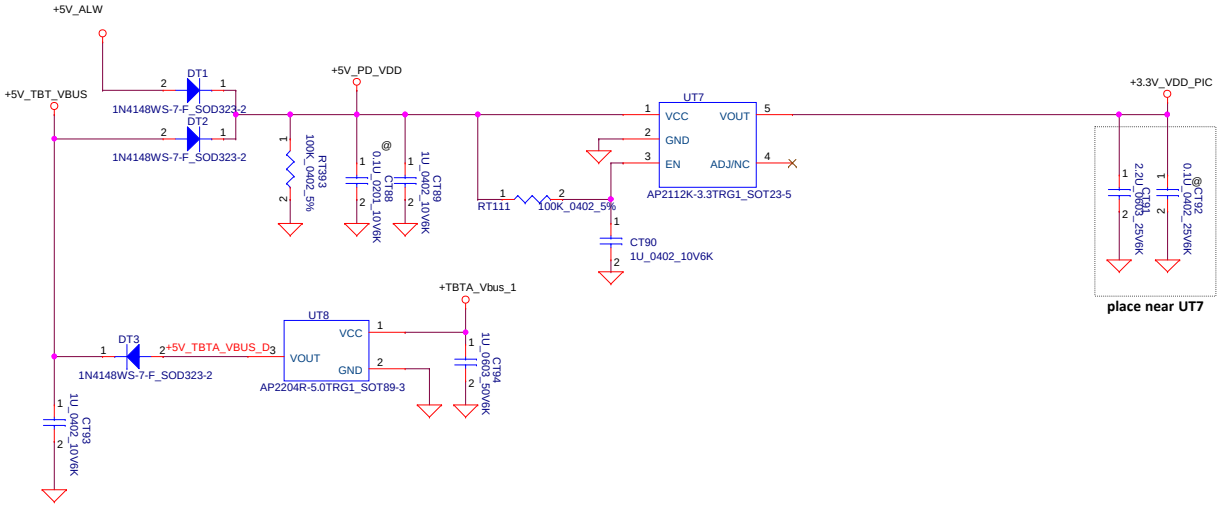
Link TPS65982D (from SA00009W200 to SA00009W210) 08/04

Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size: | Document Number: LA-E071P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 26 of 64



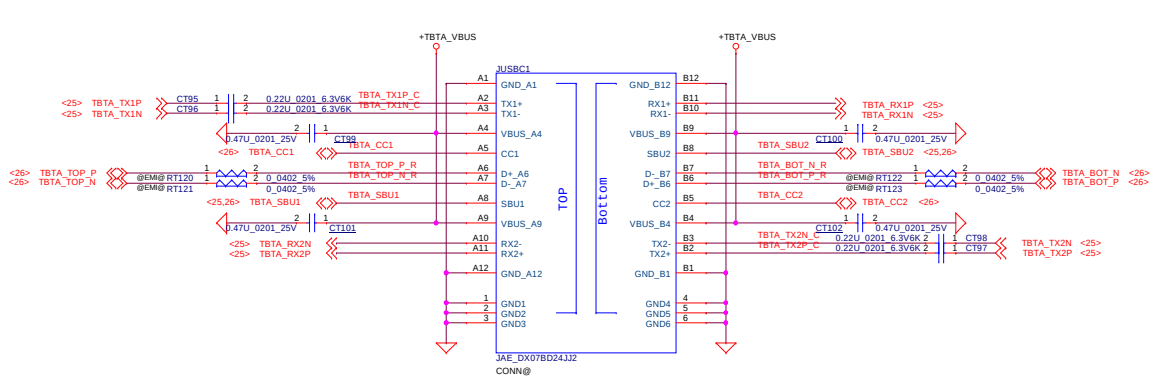
Compal Electronics, Inc.

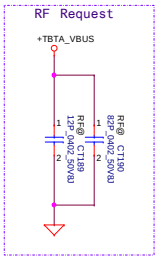
Title: [Type C]PD Power

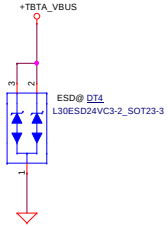
Size | Document Number: LA-E071P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 27 of 64

For NON AR Config

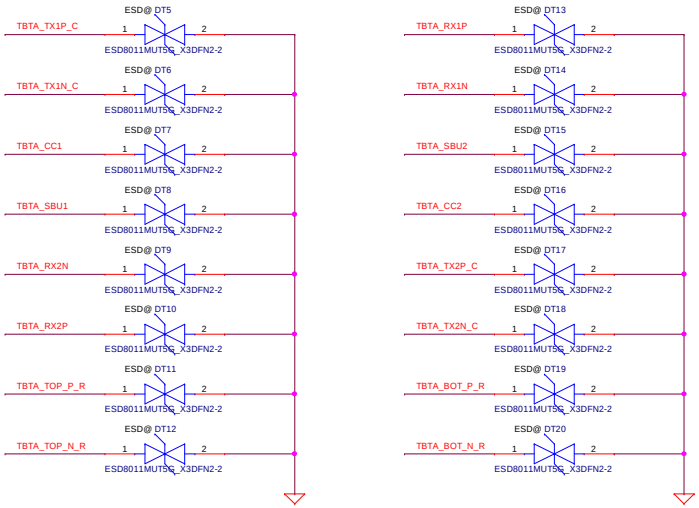


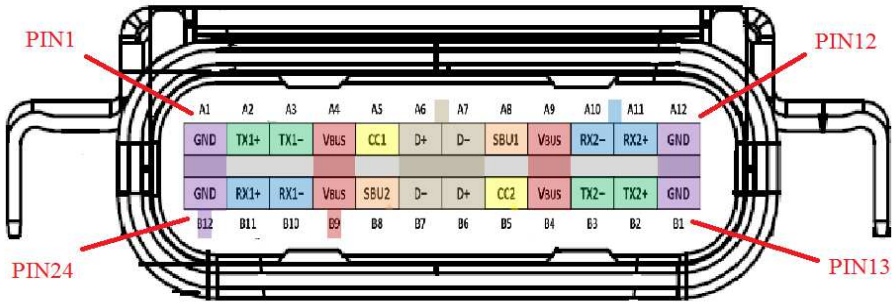




DX07BD24JJ2 LINK DONE

Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B





Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-E071P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 28 of 64

For 2LANE EDP &3.3V_TSP
For Breckenridge&Steamboat 12

LINK 50398-04041-001 DONE

JEDP1
ACES_50398-04041-001
CONN@

TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events

LV27 EMI@
EXC24CQ900U_4P

DV4 @ESD@ AZC199-02SPR7G_SOT23-3
ESD depop locat i on

EMI Request

RF Request

If touch panel, GPIO Low-> Touch Mic. EQ ; others the GPIO is High -> Non-Touch Mic. EQ

JIR1
ACES_50208-0060N-P01
CONN@
Link ACES_50208-0060N-P01 done

DV1 BAT54CW_SOT323-3
DV2 BAT54CW_SOT323-3

For Touchscreen
For Breckenridge 12

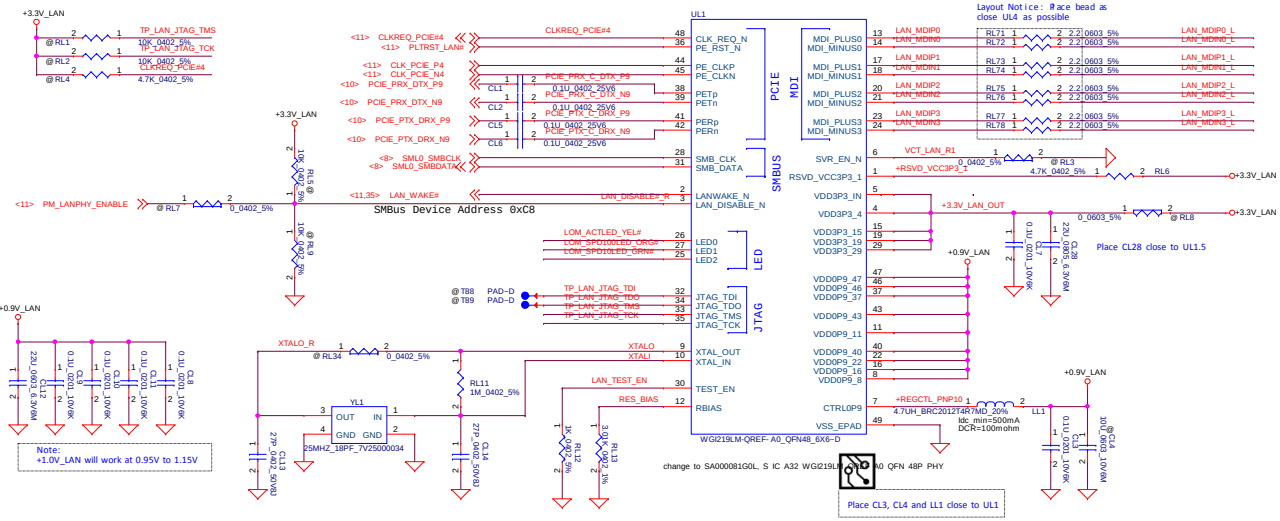
QV8 LP2301ALT1G_SOT23-3
QV7 L2N7002WT1G_SC-70-3

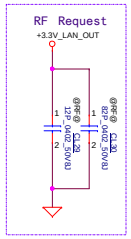
WebCAM
QZ1 LP2301ALT1G_SOT23-3
LZ1 EMI@ EXC24CQ900U_4P

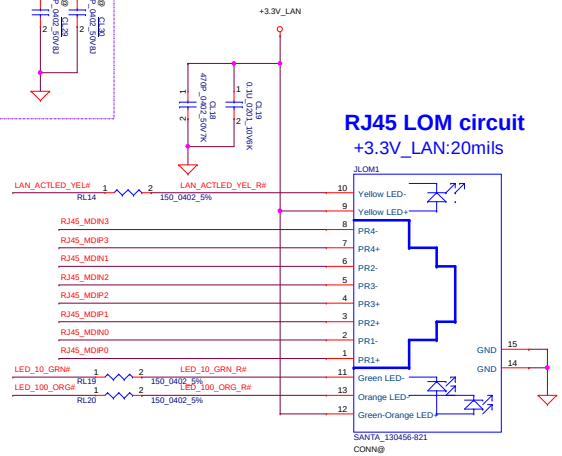
Backlight POWER
QV1 AO6405_TSOP6
QV2 L2N7002WT1G_SC-70-3
PJP13 PAD-OPEN1x2m
Co-lay: Short PJP13;Depop RZ90

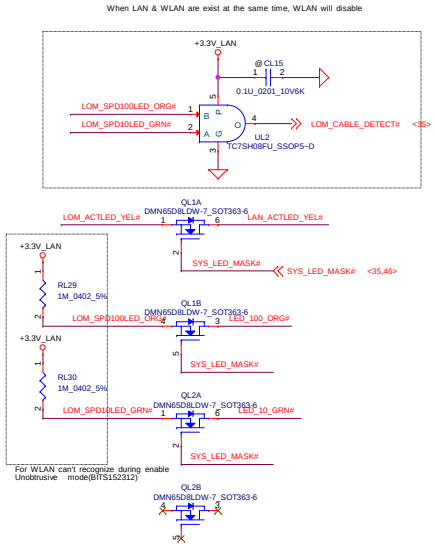
LCDVDD POWER
PJP12 PAD-OPEN1x1m
UV24 G524B1T11U_SOT23-5
DV3 BAT54CW_SOT323-3
Co-lay: Short PJP12;Depop RZ93

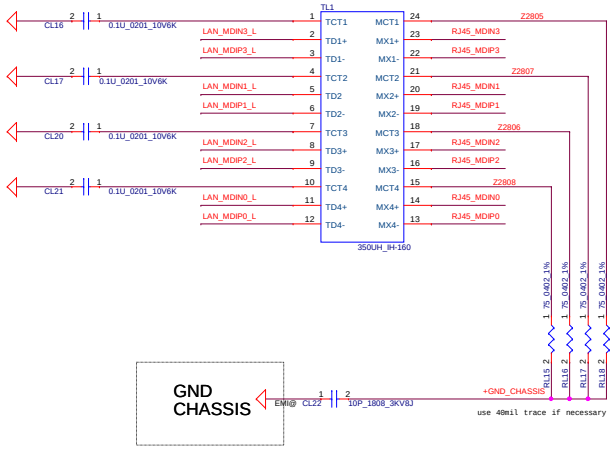
Compal Electronics, Inc.
Title: eDP CONN & Touch screen
Size: Document Number: LA-E071P
Rev: 1.0
Date: Wednesday, November 30, 2016
Sheet 29 of 64











DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	LAN Clarkvillie & RJ45
Size	Document Number: LA-E071P
Rev	1.0
Date:	Wednesday, November 30, 2016
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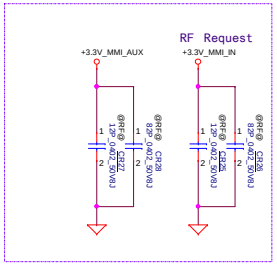
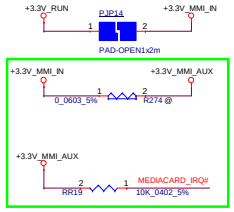
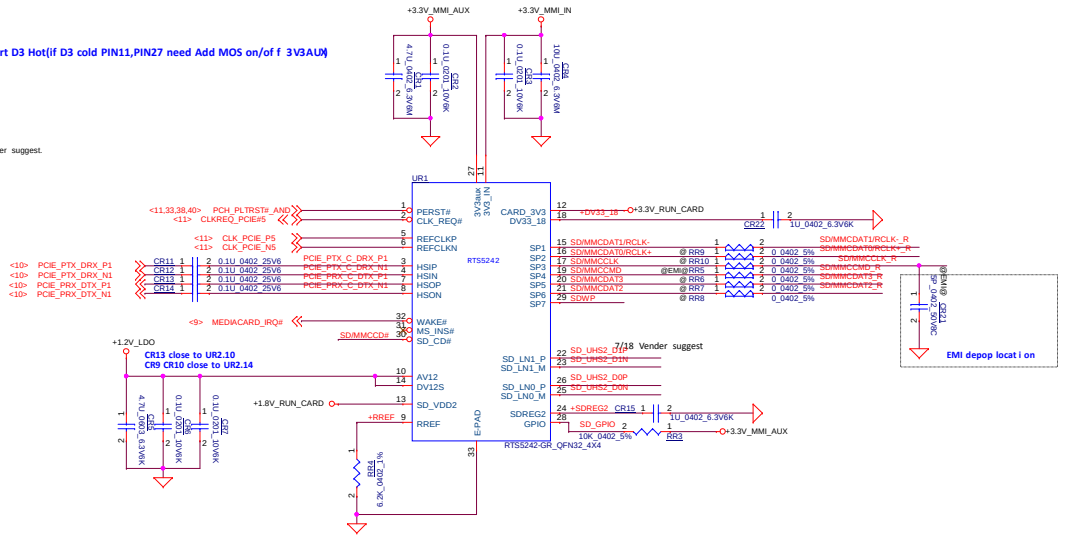
For PCIE Interface



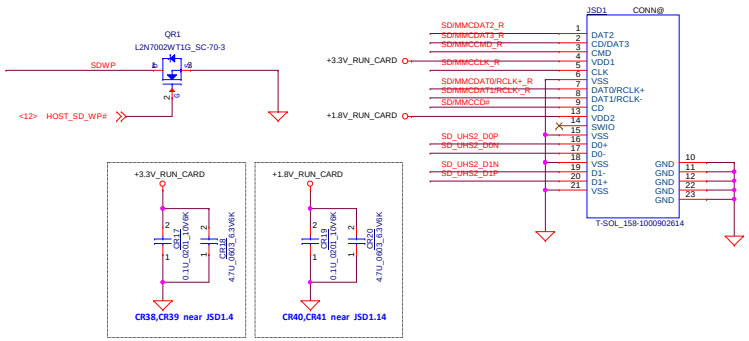


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



Compal Electronics, Inc.

Title: Card Reader RTS5242

Size: | Document Number: LA-E071P | Rev: 1.0

Date: Wednesday, November 30, 2016 | Sheet 31 of 64

NO SUPPORT

Compal Electronics, Inc.

Title: PCIE REPEATER for M.2 3042

Size | Document Number: LA-E071P | Rev: 1.0

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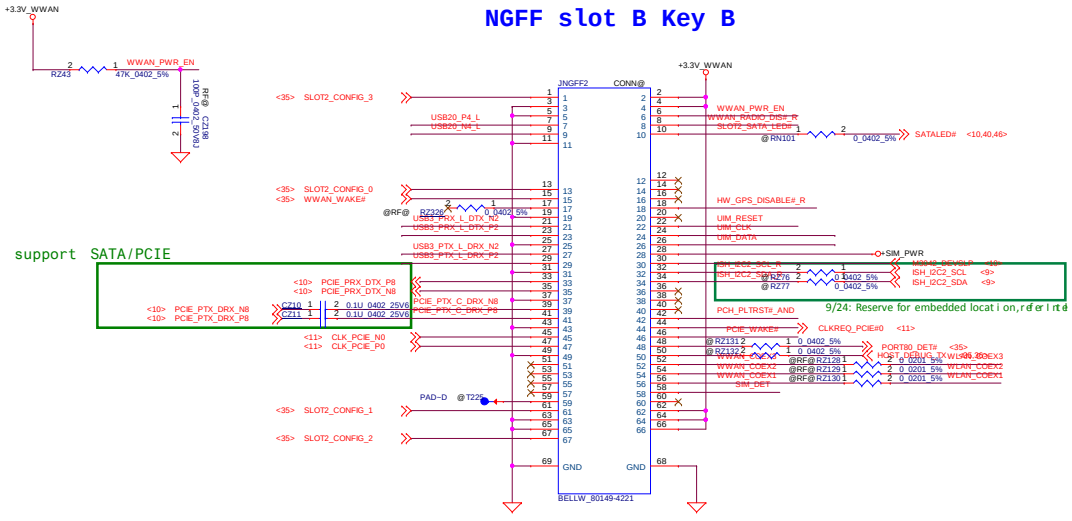
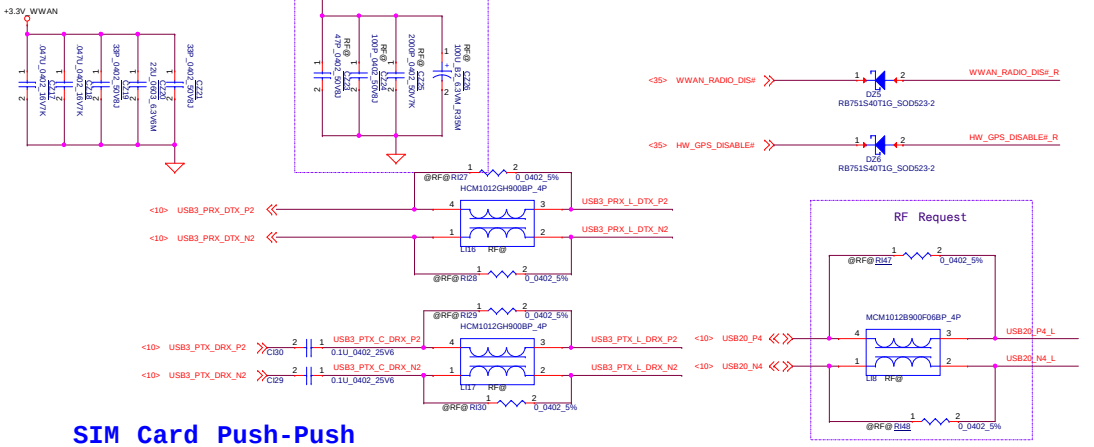
NGFF slot B Key B



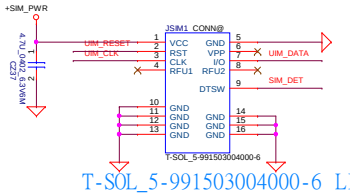
support SATA/PCIE

9/24: Reserve for embedded location, refer to PDG 0.9

BELLW_80149-4221 LINK DONE

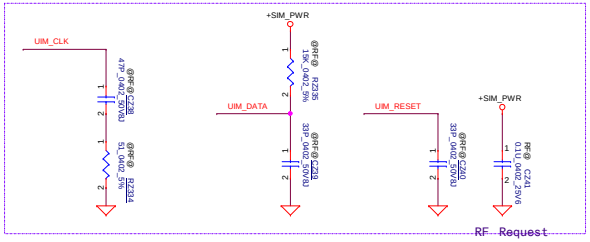


SIM Card Push-Push



T-SOL_5-991503004000-6 LINK DONE

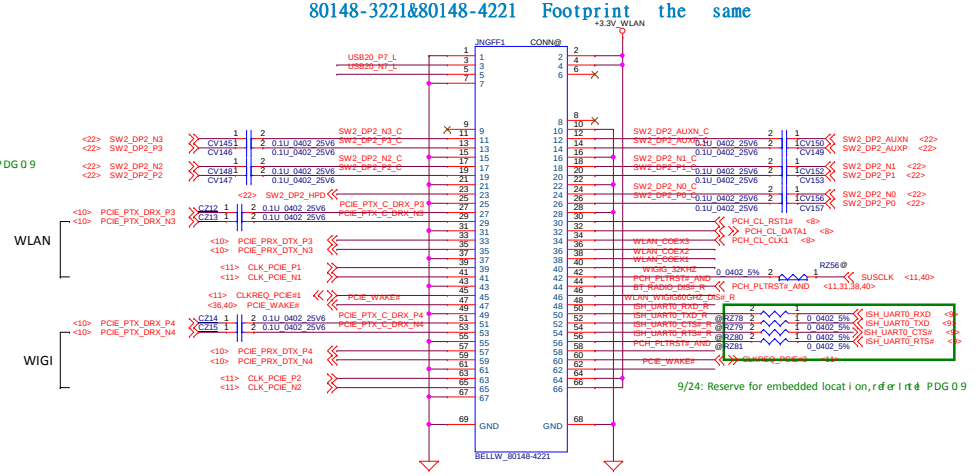
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low



for no AR,Brekenridge 12/14/15 UMA/Steamboat

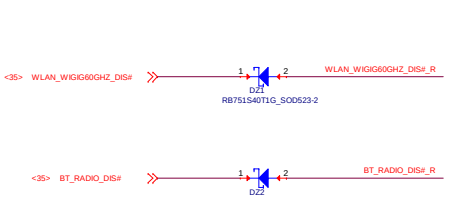
NGFF slot A Key A

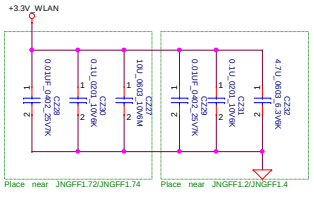
80148-3221&80148-4221 Footprint the same

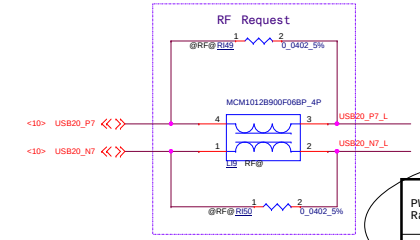


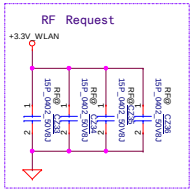
BELLW_80148-4221 LINK DONE

9/24: Reserve for embedded location, refer to PDG 0.9









Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Compal Electronics, Inc.

Title: NGFF Card

Size: Document Number: LA-E071P Rev: 1.0

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

Link 50271-0060N-001 DONE

	SPK_DET#
PK23000UO00M1 (FG-CPL088000)	Low
PK23000UO00M2 (PB2610KFG04T-033-9MG1)	High

Close to UA1 pin6

place close to UA1 pin6

Place closely to Pin 14.

Add for solve pop noise and detect issue

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

place at AGND and DGND plane

need link SM01000NS00
Realtek suggest rated current : 2A

Close to UA1

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

SLEEVE/RING2 please keep 40 mils trace width

Place CA29 close to Codec

Add this Filter to avoid other components/chips be influenced

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC

Global Headset
Universal Jack

Normal Open

Link 2SJ3095-085111F DONE

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.8V_RUN

Reserve for support D3 cold

2.5A

500mA

RF Request

Compal Electronics, Inc.

Title: Codec ALC3253

Size: | Document Number: LA-E071P | Rev: 1.0

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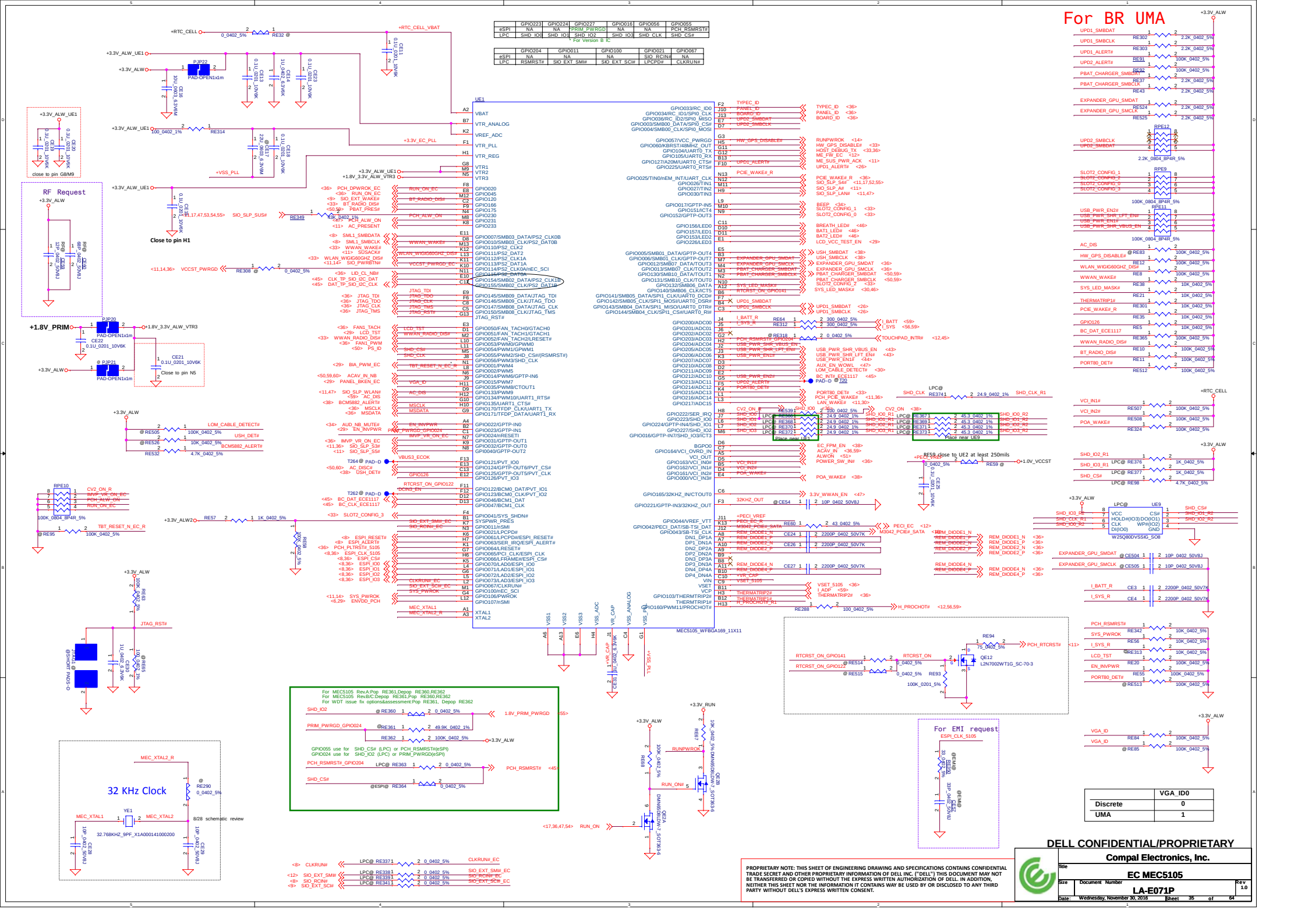

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	NA	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

VGA_ID0	
Discrete	0
UMA	1

For BR UMA

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

JXT_FP241AH-010GAAM LINK DONE

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

WDT option	
MEC5105 rev.B	Pop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348 Depop RE362, RE536, RE537
MEC5105 rev.C	Pop RE362, RE536, Depop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348, RE537

CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V

GPIO223 is OD. When EC fetches the code, set GPIO223 to Low.

To prevent backdrive to PCH_DPWROK_EC when AC is plugged before +3.3V_ALW ramps up.

In DC mode, ACAV_IN is LOW. This circuit doesn't affect PCH_DP WROK
In AC mode, 1. ACAV_IN is high. GPIO223 is tri-state. QE13B is ON. QE13A can prevent backdrive to PCH_DPWROK.
2. EC fetches code and the drives GPIO223 to LOW to turn off QE13B. When QE13B is off, un-plugging AC will not affect DSW_DPWRO
3. When WDT occurs, GPIO223 is tri-state (EC reset). ACAV_IN changes CE503. When AC is removed, ACAV_IN goes LOW immediately.
QE13B still keeps on according to RC discharging rate. PCH_DP WROK is LOW because ACAV_IN is LOW

Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Write
R/W = 1 = Read

SMBus address 0x40

RF Request

RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
* 240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

PD_ACE_DET# rise time is measured from 5%~68%

BOARD_ID rise time is measured from 5%~68%

PANEL_ID rise time is measured from 5%~68%

Rest=1.58K , Tp=96 degree???

Link 50271-0040N-001 DONE

JXT_FP241AH-010GAAM LINK DONE

Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

Compal Electronics, Inc.
Title: MEC5105 Support
Size: Document Number: LA-E071P
Rev: 1.0
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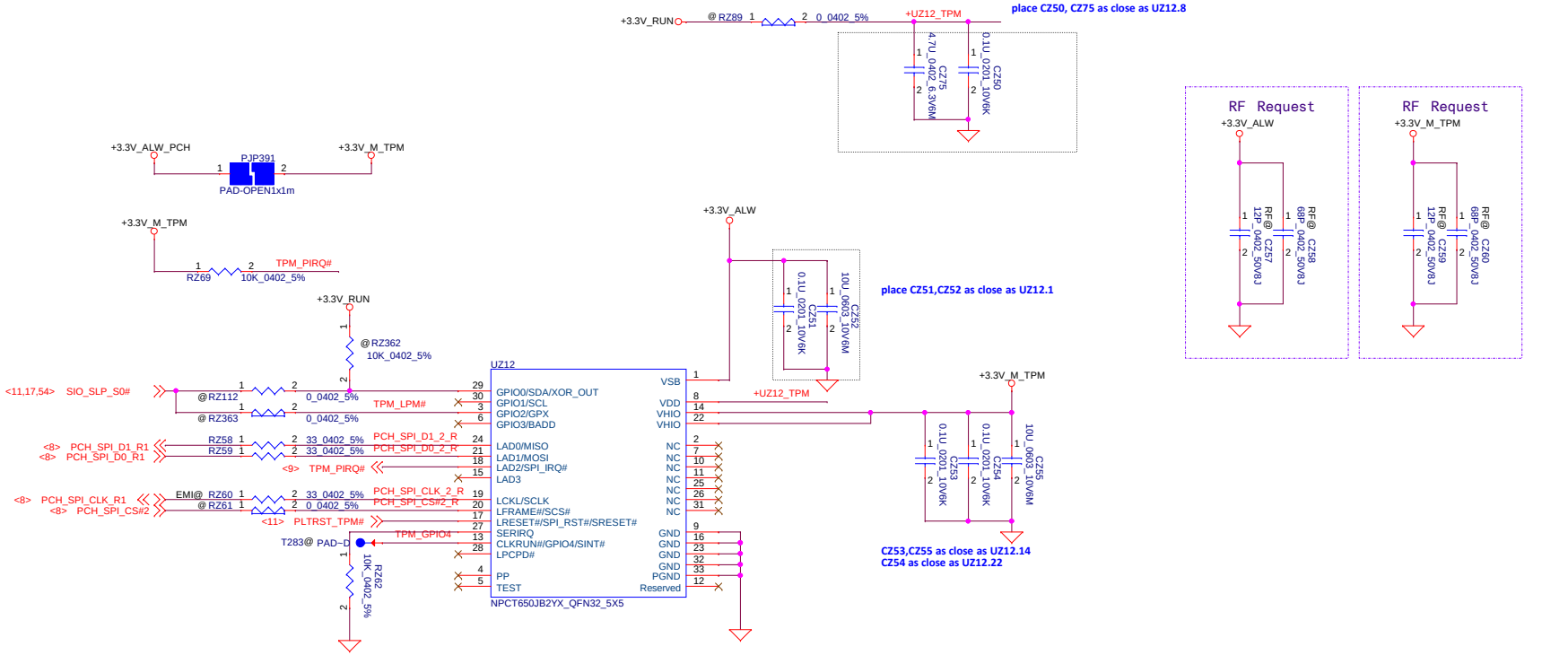
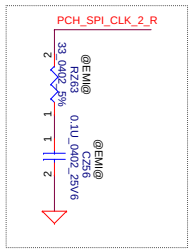
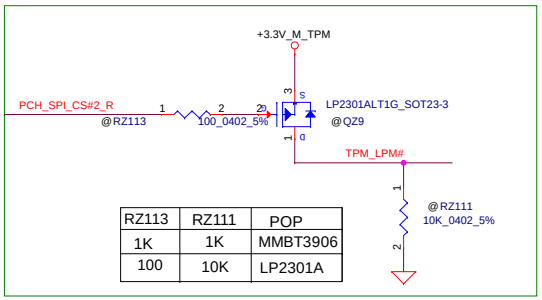
For NUVOTON TPM



JB2YX change to VB2YX 09/08





RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

Compal Electronics, Inc.

Title: USH & TPM

Size | Document Number: LA-E071P | Rev: 1.0

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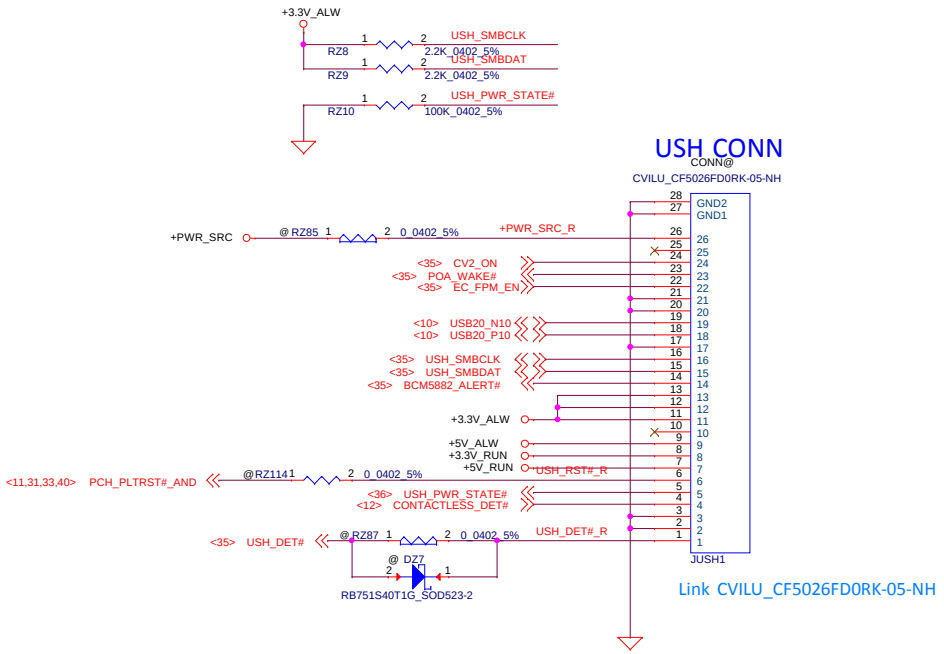
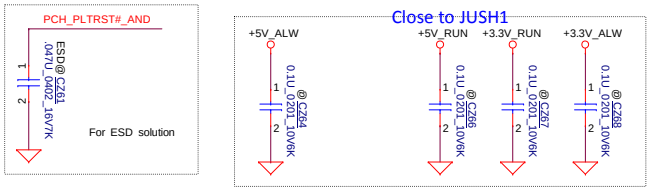
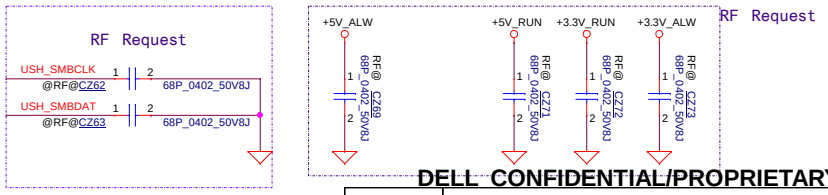
For ATMEL TPM







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Compal Electronics, Inc.

Title: USH & TPM

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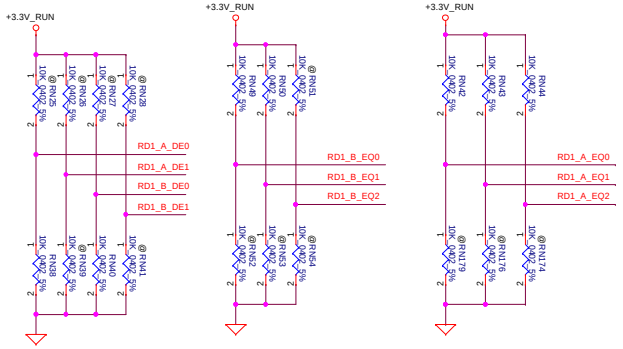
For Parade 2 Lane solution

	PCIE/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check



Programmable output de-emphasis level setting for channel A
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
- LL: -2dB
- HL: -7.5dB
- LH: -3.5dB (default)
- HH: -6dB

Programmable output de-emphasis level setting for channel B
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

[B_DE1,B_DE0] ==
- LL: -2dB
- HL: -7.5dB
- LH: -3.5dB (default)
- HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

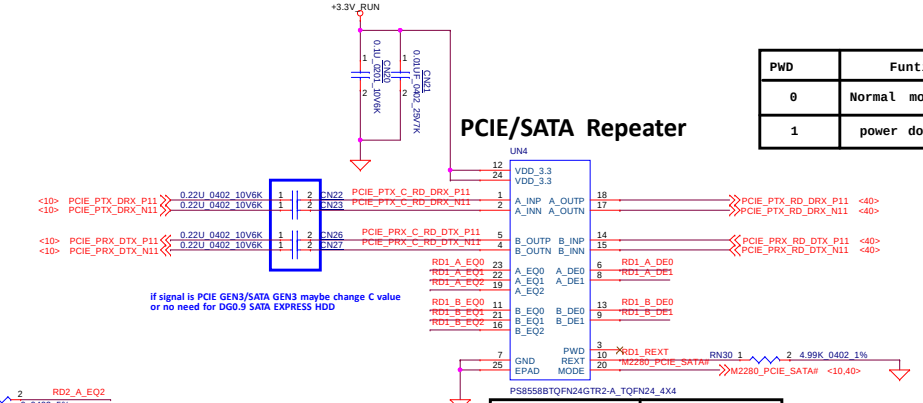
[A_EQ2,A_EQ1,A_EQ0] ==
- LLL: For channel loss up to 17dB (default)
- LHL: For channel loss up to 14dB
- HLL: For channel loss up to 19dB
- HHL: For channel loss up to 21dB
- LLH: For channel loss up to 18dB
- LHH: For channel loss up to 10dB
- HLH: For channel loss up to 16dB
- HHH: For channel loss up to 20dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

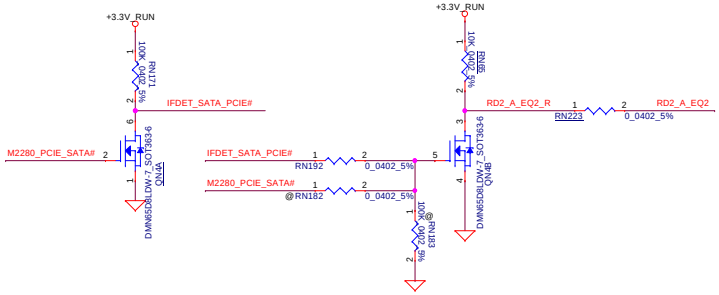
[B_EQ2,B_EQ1,B_EQ0] ==
- LLL: For channel loss up to 17dB (default)
- LHL: For channel loss up to 14dB
- HLL: For channel loss up to 19dB
- HHL: For channel loss up to 21dB
- LLH: For channel loss up to 18dB
- LHH: For channel loss up to 10dB
- HLH: For channel loss up to 16dB
- HHH: For channel loss up to 20dB

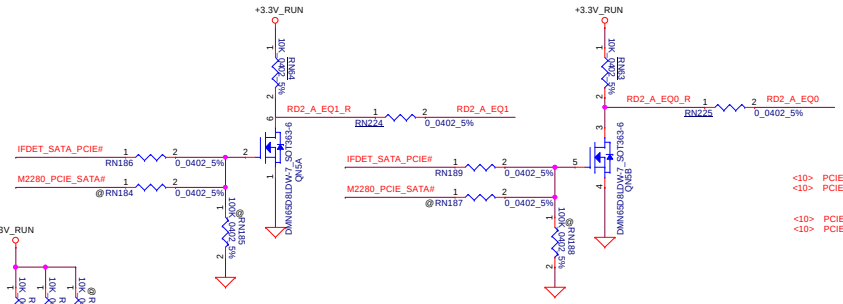
PCIE/SATA Repeater

PWD	Funtion
0	Normal mode(default)
1	power down mode

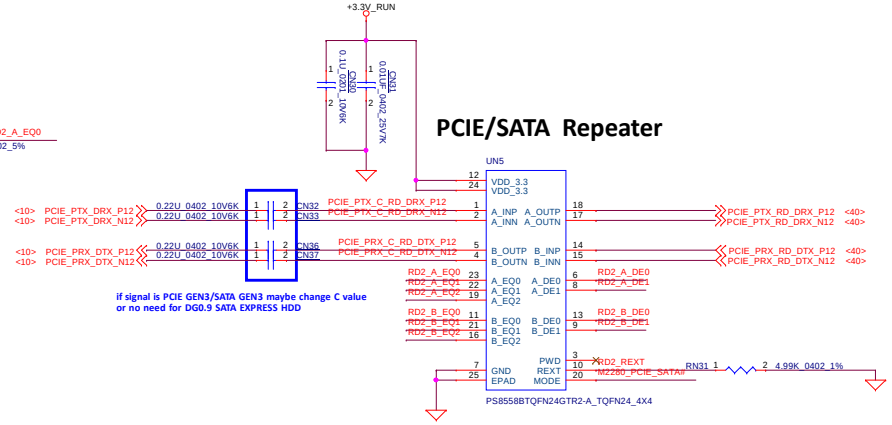


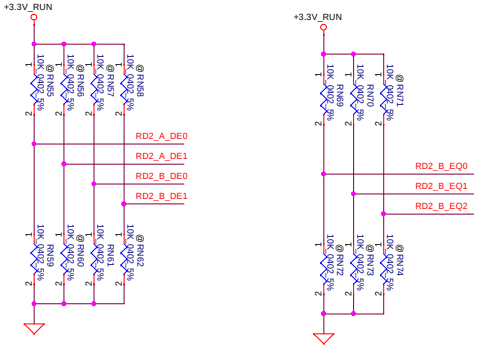
M2280_PCIE_SATA#	DEVICE interface
0	SATA
1	PCIE





PCIE/SATA Repeater





SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Compal Electronics, Inc.

Title: SATA/PCIE REPEATER for M.2 2280

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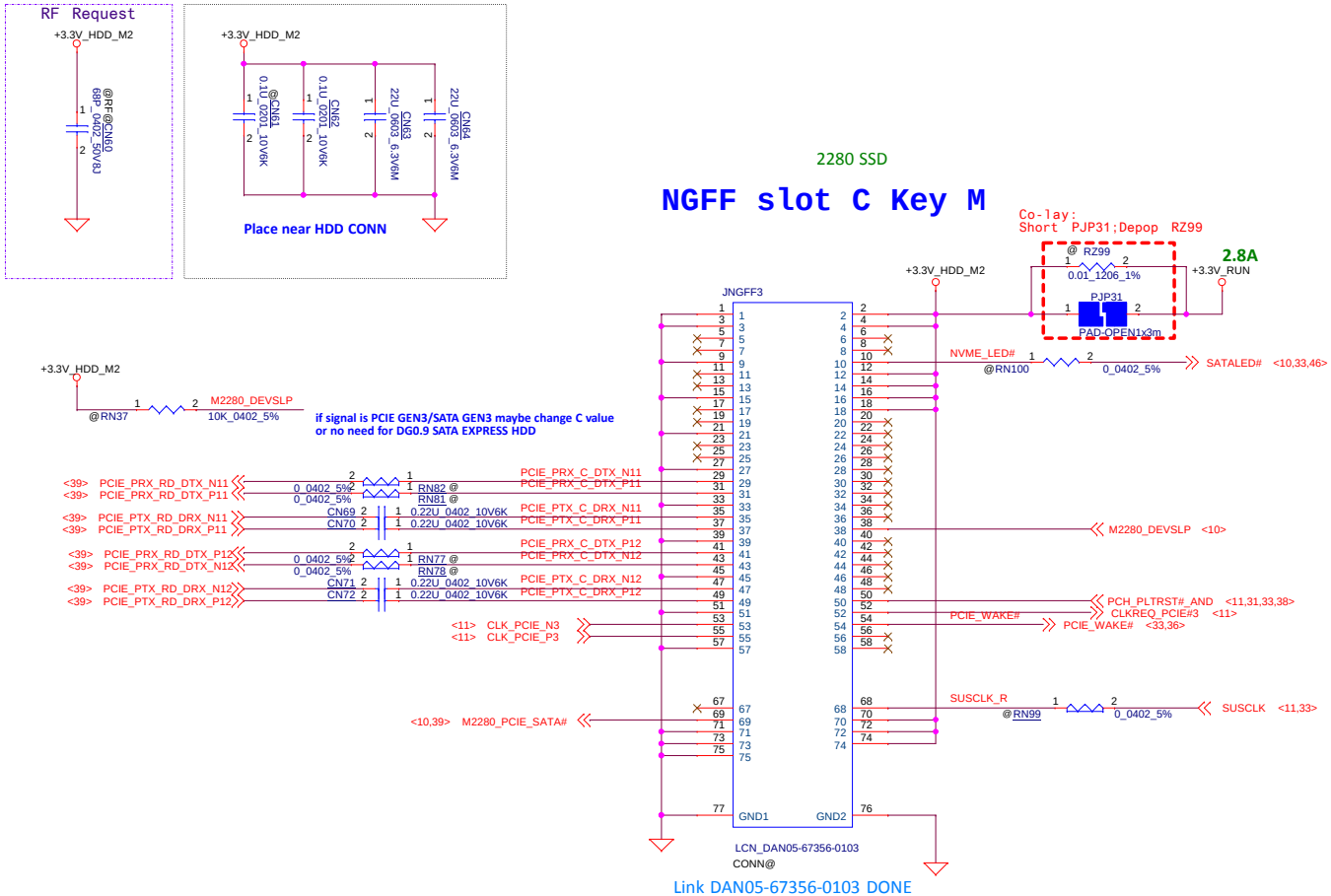
For Brekenridge 12/14/15 UMA/Steamboat



Compal Electronics, Inc.

Title: M2 2280 Socket

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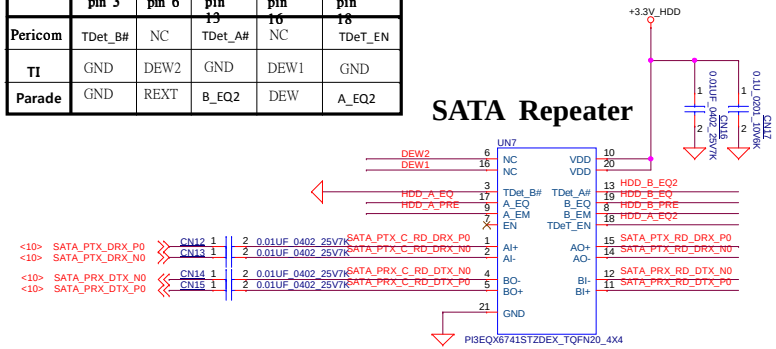
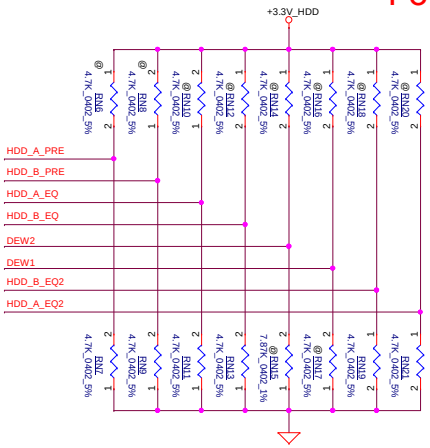
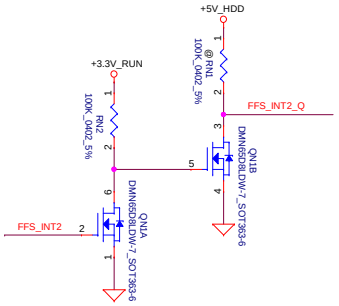
For Breckenridge 12/14/15 UMA

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater





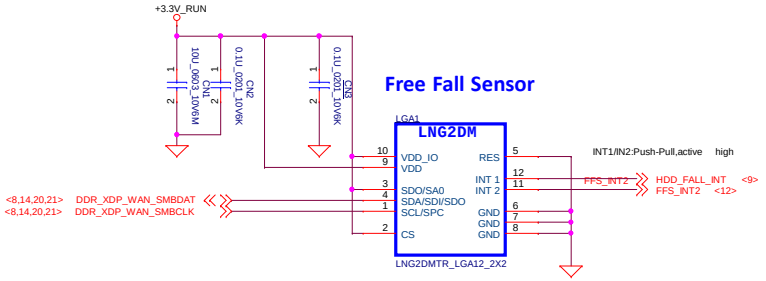


	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)	NC (1/2 VDD)

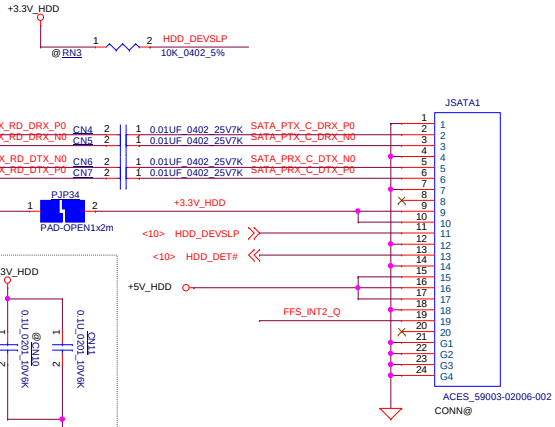
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2)	A_EQ	B_EQ		A_EM	B_EM
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

* red color is current setting

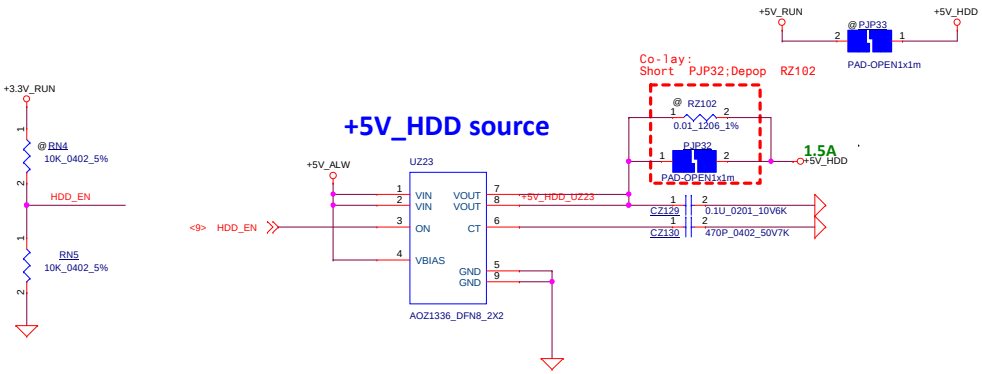
Free Fall Sensor

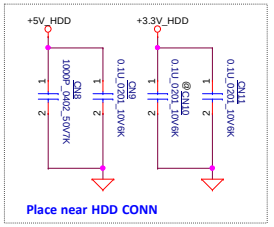


Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



Link SP010023HA0 DONE





Compal Electronics, Inc.

Title: SATA Repeater&HDD CONN

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NO SUPPORT

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Compal Electronics, Inc.

Title: USB3.0 Repeater

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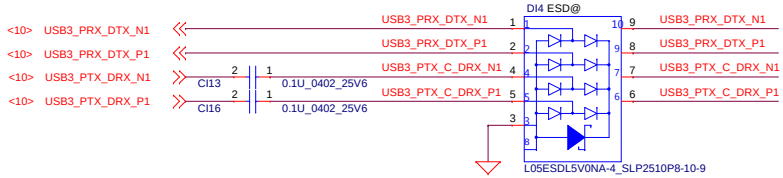
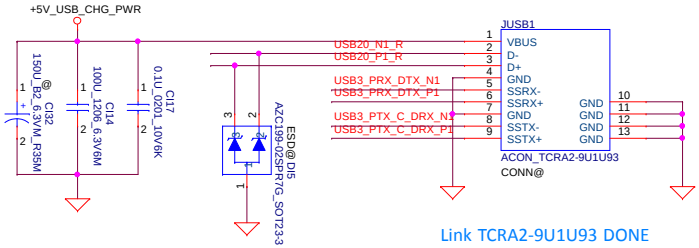
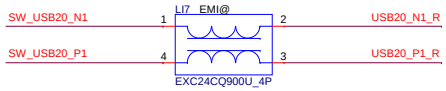
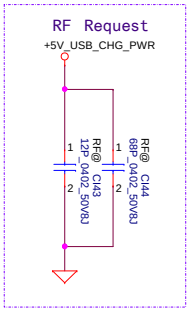
For w/o Repeater

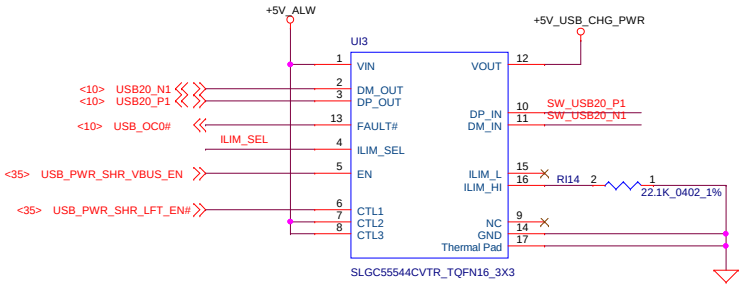




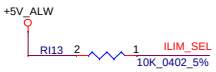
Link TCRA2-9U1U93 DONE

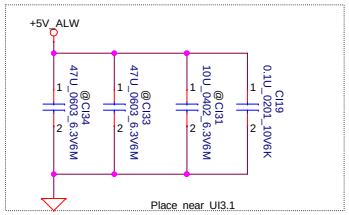






Link Seligro SA000097E10 Done
MAIN:SLGC55544CVTR





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Compal Electronics, Inc.

Title: JUSB1+PS

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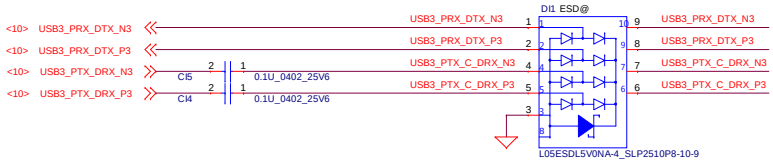
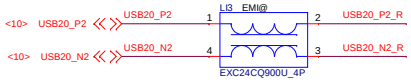
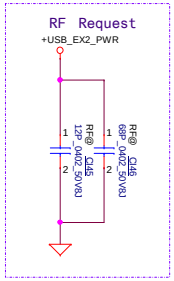
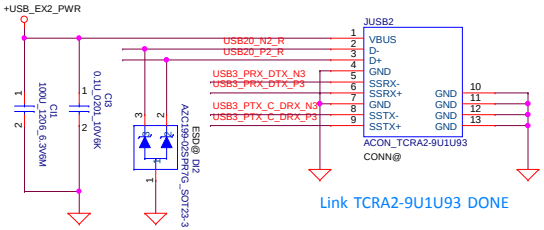
For Breckenridge/Steamboat 12&Kirkwood

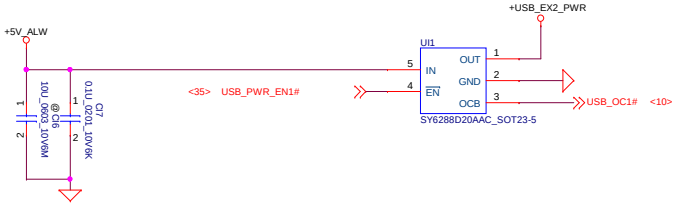




DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm







Compal Electronics, Inc.

Title: JUSB2

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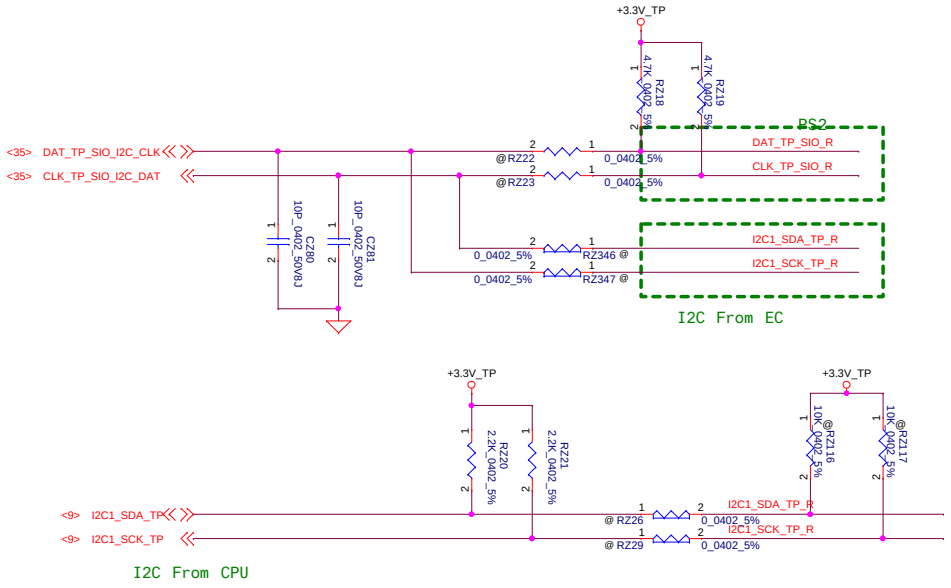
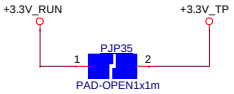
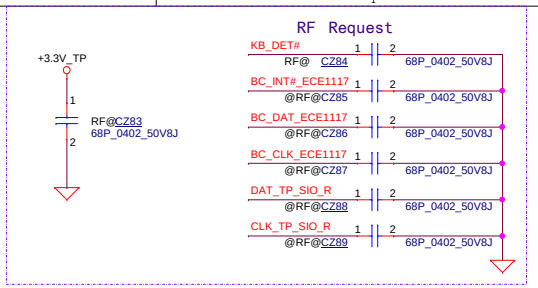
Touch Pad

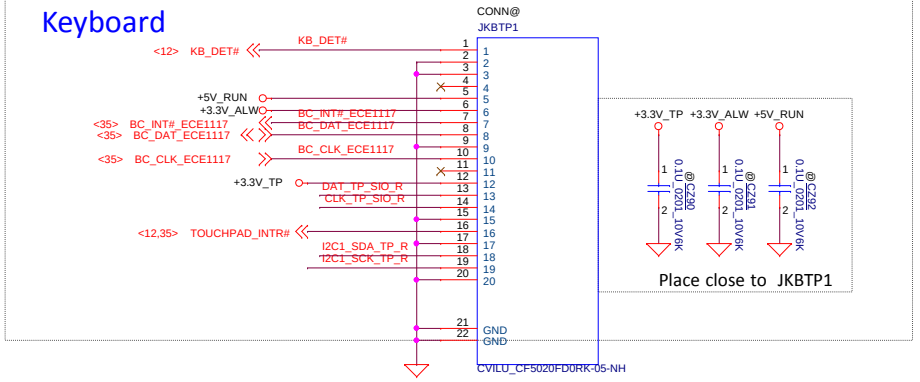


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



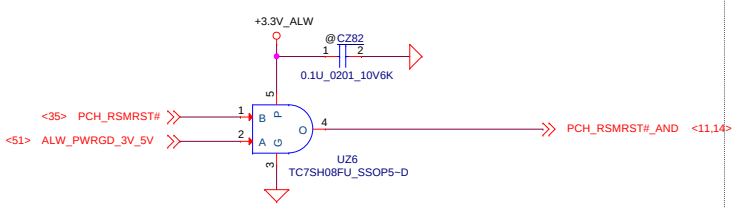


Keyboard



Link HRS_TF49-20S-0P5SH done

RSMRST circuit



Compal Electronics, Inc.

Title: Keyboard

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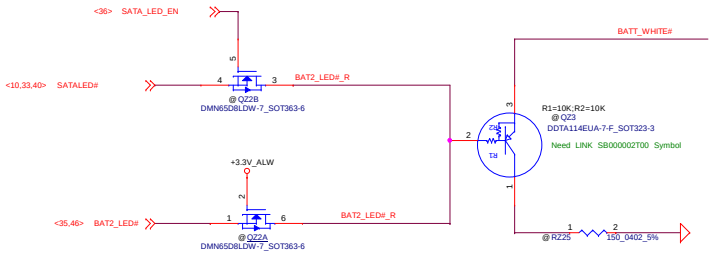
Bat t ery LE D

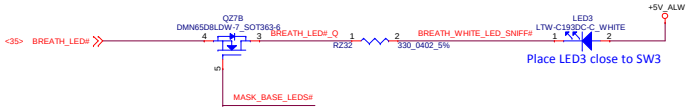
HDD LED MUX

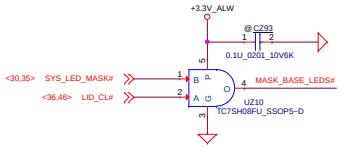
means EC can switch battery white led and HDD LED by hot key " Fn+F



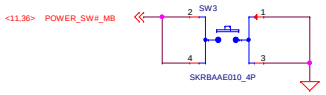
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

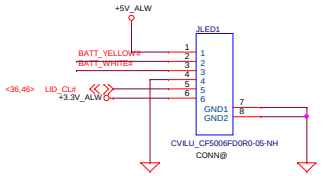




POWER & INSTANT ON SWITCH



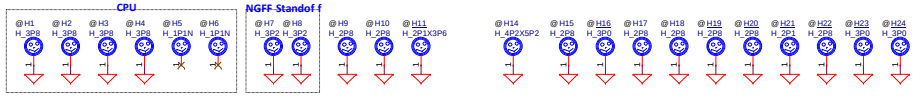
LED board CONN

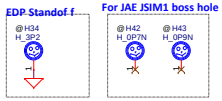


Fiducial Mark

@ FD1 FIDUCIAL MARK~D
@ FD2 FIDUCIAL MARK~D
@ FD3 FIDUCIAL MARK~D
@ FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





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Compal Electronics, Inc.

Title: PAD, LED

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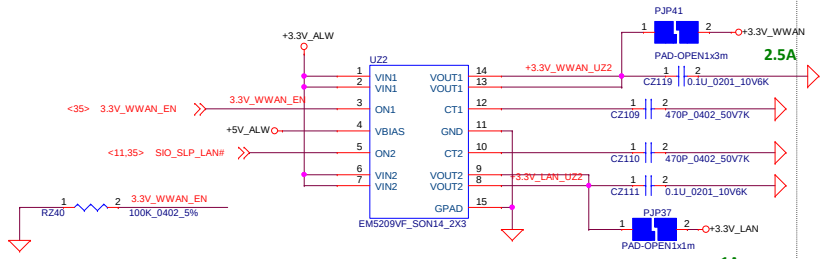
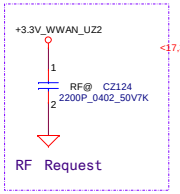
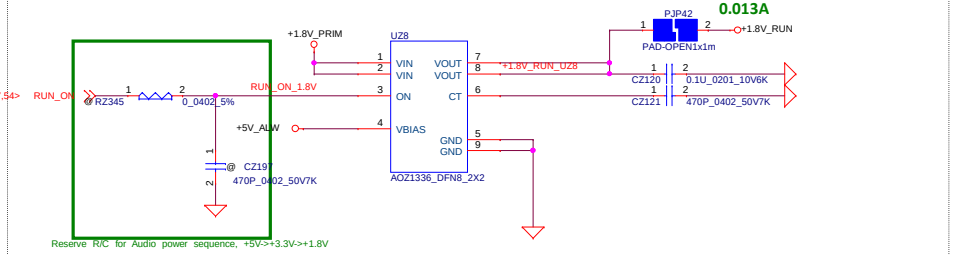
+3.3V_WWAN/+3.3V_LAN source

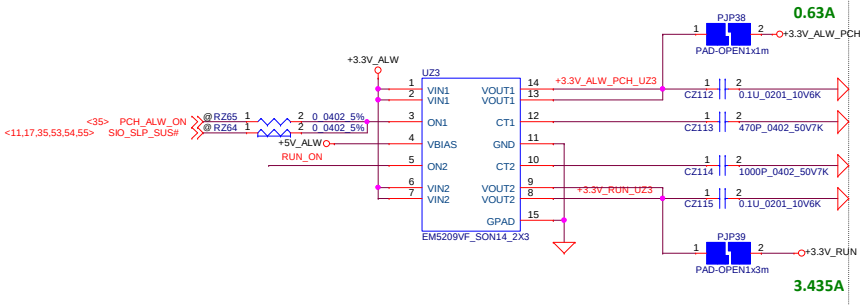




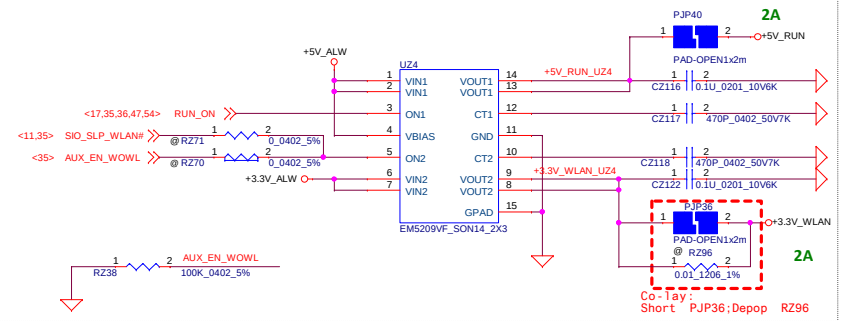
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WLAN source



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Compal Electronics, Inc.		
Title: Power control		
Size	Document Number: LA-E071P	Rev: 1.0
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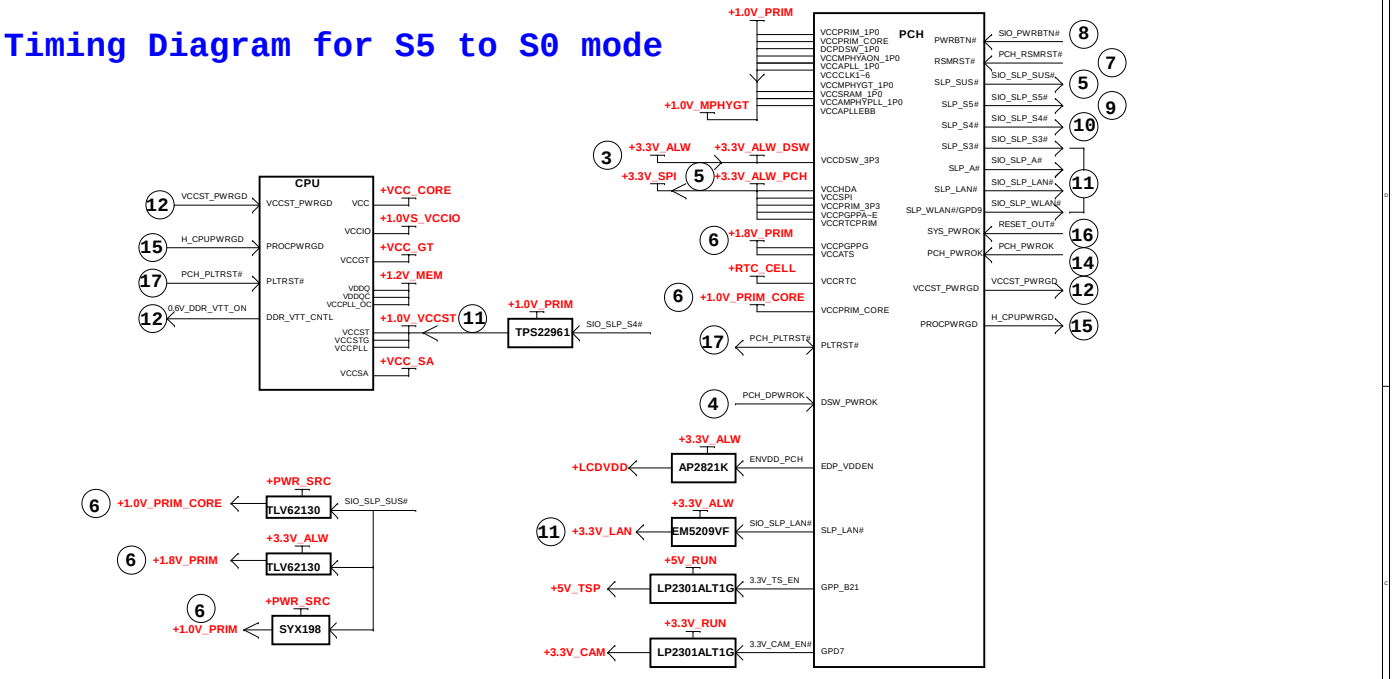
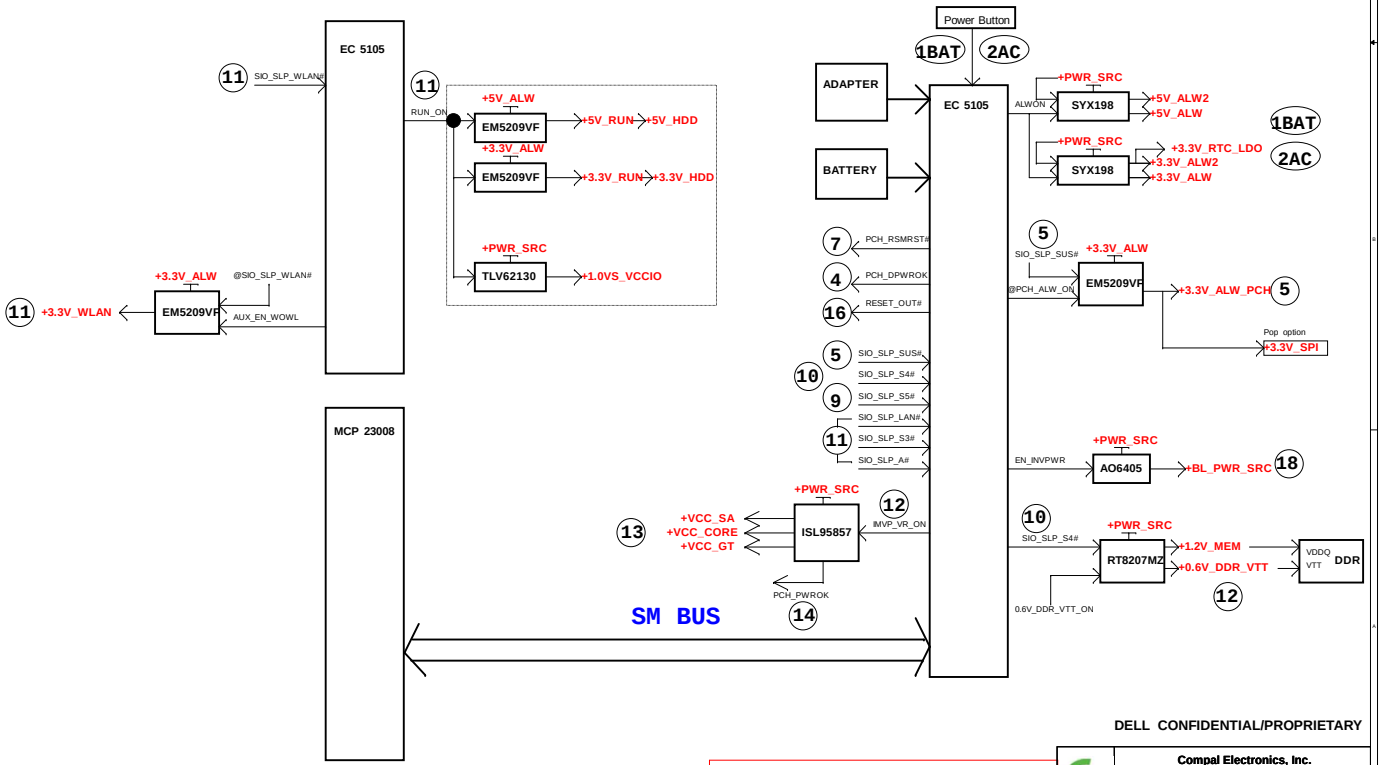
Timing Diagram for S5 to S0 mode





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Compal Electronics, Inc.

Title: Power Sequence

Size: Document Number: LA-E071P — Rev: 1.0

Date: Wednesday, November 30, 2016 — Sheet 48 of 64

1

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay time(ps/inch)	25 ± 2.5 ohm single-end	35 ± 3.5 ohm single-end	39 ± 3.9 ohm single-end	43 ± 4.3 ohm Single-end	45 ± 4.5 ohm Single-end	48 ± 4.8 ohm single-end	50 ± 5 ohm Single-end	52 ± 5.2 ohm Single-end	50 ± 5 ohm Diff.	70 ± 7 ohm Diff.	75 ± 7.5 ohm Diff.	80 ± 8 ohm Diff.	83 ± 83 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	100 ± 10 ohm Diff.	Ref	100 ± 10 ohm Diff.	Ref	90 ± 9 ohm Diff.	Ref
			SolderMask	IT-158	0.5		trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)					
			Add Plating												SE 25	SE 40	SE 43	SE 48		SE 50	SE 52			SE 50	SE 50	SE 52								
1	Top		Copper foil	0.5oz+plating	1.6	149.18	13.4	8	6.6	5.5	5	4.4	4	3.7	13.5/X	6.6/5.2	5.5/4.5	4.4/3.7	3.9/3.5	4/4.1	3.7/3.6			4/5	4/5.7	3.7/4.7	3/3.3	3.5/4.2	3.5/8.3	L2	9/4.5	no Ref	10/5	L3
		3.8	Prepreg	1080	2.6		24.98	34.95	39.05	43.06	45.2	48.08	50.23	52	蝕法做對	69.98	75	79.85	82.85	84.88	85.11			88.12	90.04	89.99	89.92	89.96	100.02		99.28		89.49	
2	GND		Copper foil	1oz	1.25																												
		3.7	Core	4mil	3.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48							
3	IN 1		Copper foil	1oz	1.25	161.77	11.4	6.8	5.6	4.7	4.3	3.7	3.5	3.3	11.4/X	5.6/3.9	4.8/3.8	4.3/4.1	3.6/3.5	3.5/3.6	3.3/3.3	3.7/4.1	4.3/6.2	3.5/4.3	3.5/4.9	3.3/4.3	3.7/5.7		3/6.5	L2/L4	9.5/6	no Ref			
		3.7	Prepreg	2116H	4.3		24.92	34.99	39.12	42.94	44.9	48.22	49.45	51.84	蝕法做對	69.94	74.93	79.85	83.31	84.76	85.01	85.13	85.05	87.88	89.98	89.97	89.99		99.94		99.81			
4	GND/PWR		Copper foil	1oz	1.25																												
		3.7	Core	4mil	3.87										SE 25	SE 40	SE 43	SE 48		SE 50	SE 52	SE 48		SE 50	SE 50	SE 52								
5	IN 2		Copper foil	1oz	1.23	160.76	15.5	9.3	7.7	6.5	5.9	5.2	4.6	4.4	15.5/12	7.7/5	6.5/4.6	5.2/3.7	4.8/3.8	4.8/4.3	4.4/3.6	5.2/5.2		4.8/5.2	4.8/5.9	4.4/4.7			4.0/7.0	L4/L7	8.5/6	no Ref		
		3.6	Prepreg	1080H x2 or PP2116HRC	4.2		24.88	34.96	39.08	42.88	45.09	48.01	49.87	51.88	49.1	70.2	75.38	80.01	83.17	85.27	85.09	85.35		88.39	90.32	89.95			100.26		100.69			
6	IN 3		Copper foil	1oz	1.25		15.5	9.2	7.7	6.5	5.9	5.2	4.6	4.4	15.5/12	7.7/5	6.5/4.6	5.2/3.7	4.8/3.8	4.8/4.3	4.4/3.6	5.2/5.2		4.8/5.2	4.8/5.9	4.4/4.7			4.0/7.0	L4/L7	8.5/6	no Ref		
		3.7	Core	4mil	3.87																												
7	GND/PWR		Copper foil	1oz	1.25																												
		3.8	Prepreg	2116H	4.3										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48							
8	IN 4		Copper foil	1oz	1.25		11.4	6.8	5.6	4.7	4.3	3.7	3.5	3.3	11.4/X	5.6/3.9	4.8/3.8	4.3/4.1	3.6/3.5	3.5/3.6	3.3/3.3	3.7/4.1	4.3/6.2	3.5/4.3	3.5/4.9	3.3/4.3	3.7/5.7		3/6.5	L7/L9	9.5/6	no Ref		
		3.7	Core	4mil	3.87		24.92	34.99	39.12	42.94	44.9	48.22	49.45	51.84	蝕法做對	69.94	74.93	79.85	83.31	84.76	85.01	85.13	85.05	87.88	89.88	89.97	89.99		99.94		99.94			
9	GND		Copper foil	1oz	1.25																												
		3.8	Prepreg	1080	2.6																												
10	Bottom		Copper foil	0.5oz+plating	1.6		13.4	8	6.6	5.5	5	4.4	4	3.7	13.5/X	6.6/5.2	5.5/4.5	4.4/3.7	3.9/3.5	4/4.1	3.7/3.6			4/5	4/5.7	3.7/4.7	3/3.3	3.5/4.2	3.5/8.3	L9	9/4.5	no Ref		
			Add Plating				24.98	34.95	39.05	43.06	45.2	48.08	50.23	52	蝕法做對	69.98	75	79.85	82.85	84.88	85.11			88.12	90.04	89.99	89.92	89.96	100.02		99.75			
			SolderMask	IT-158	0.5																												
Overall Thickness (1.2mm ± 10%)					47.68000																												
					1.211072																												

Compal Electronics, Inc.

Title: Stack-up

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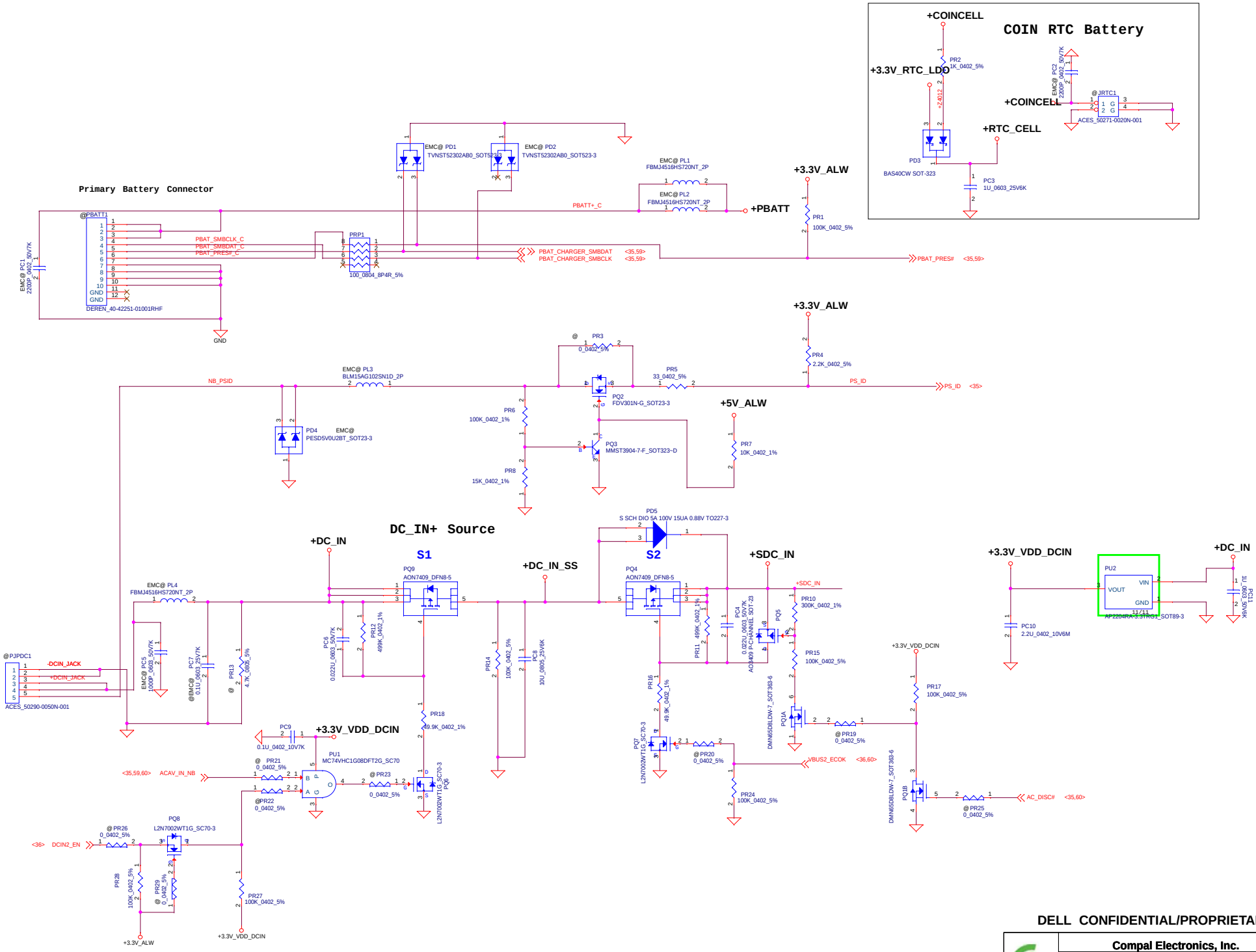

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Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-E071P	Rev: 0.5
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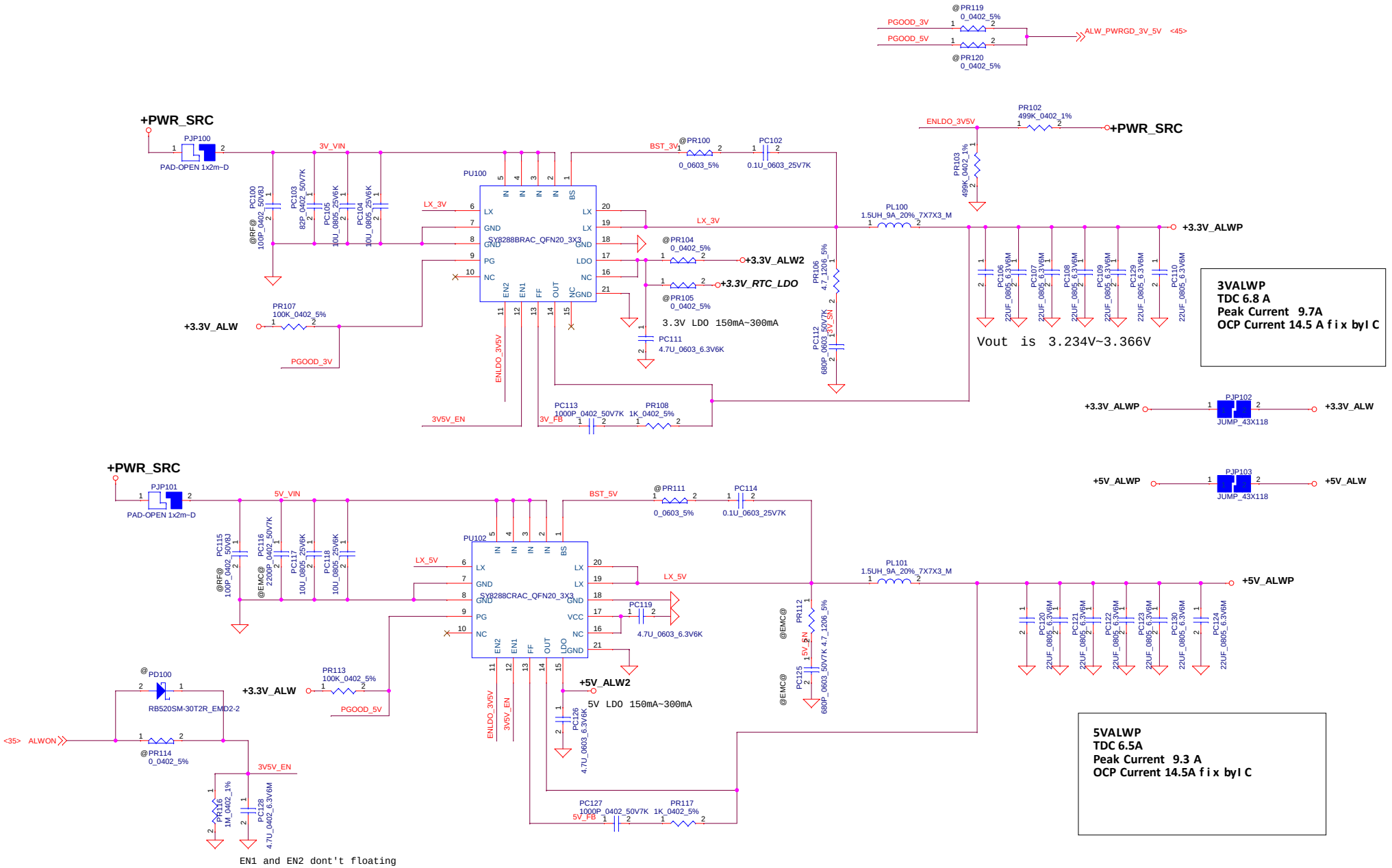
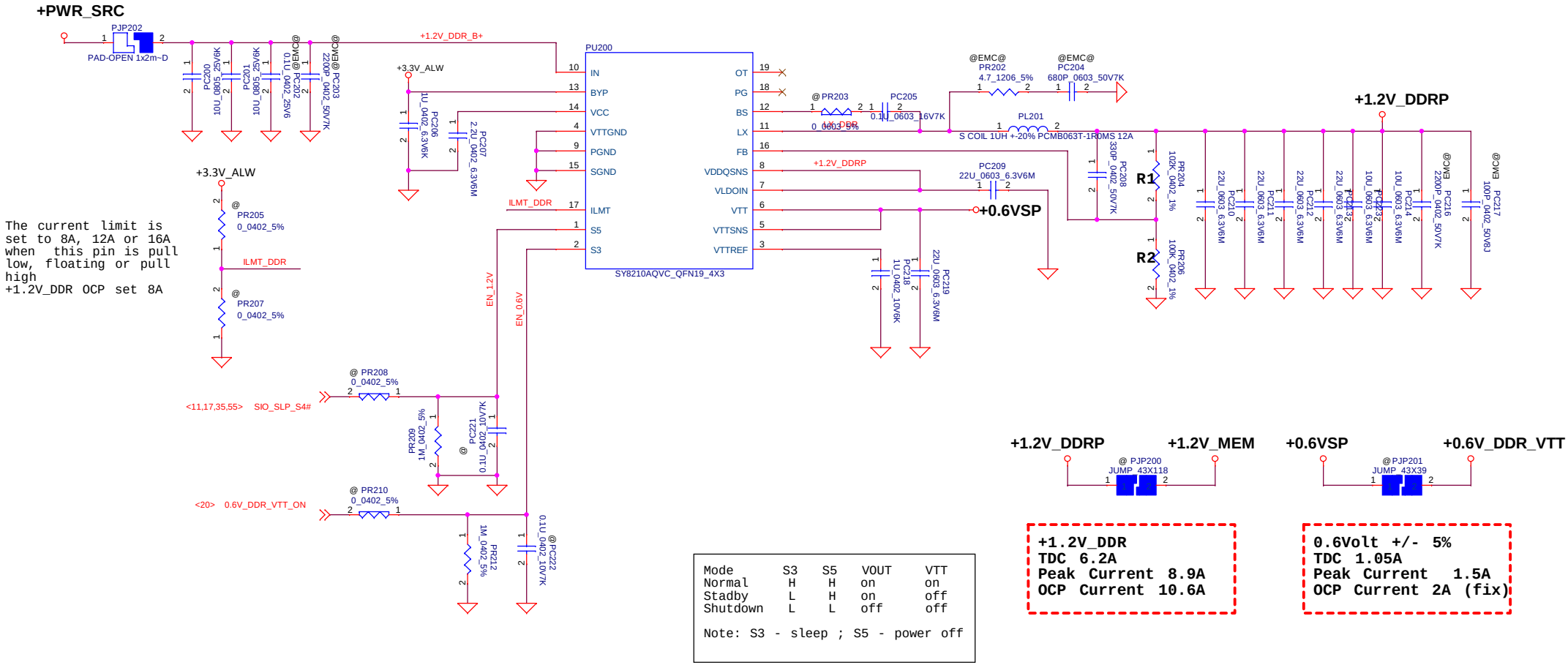


Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size: | Document Number: LA-E071P | Rev: 0.5

Date: Wednesday, November 30, 2016 | Sheet 51 of 63



Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.2A
Peak Current 8.9A
OCP Current 10.6A

0.6Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 2A (fix)

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Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

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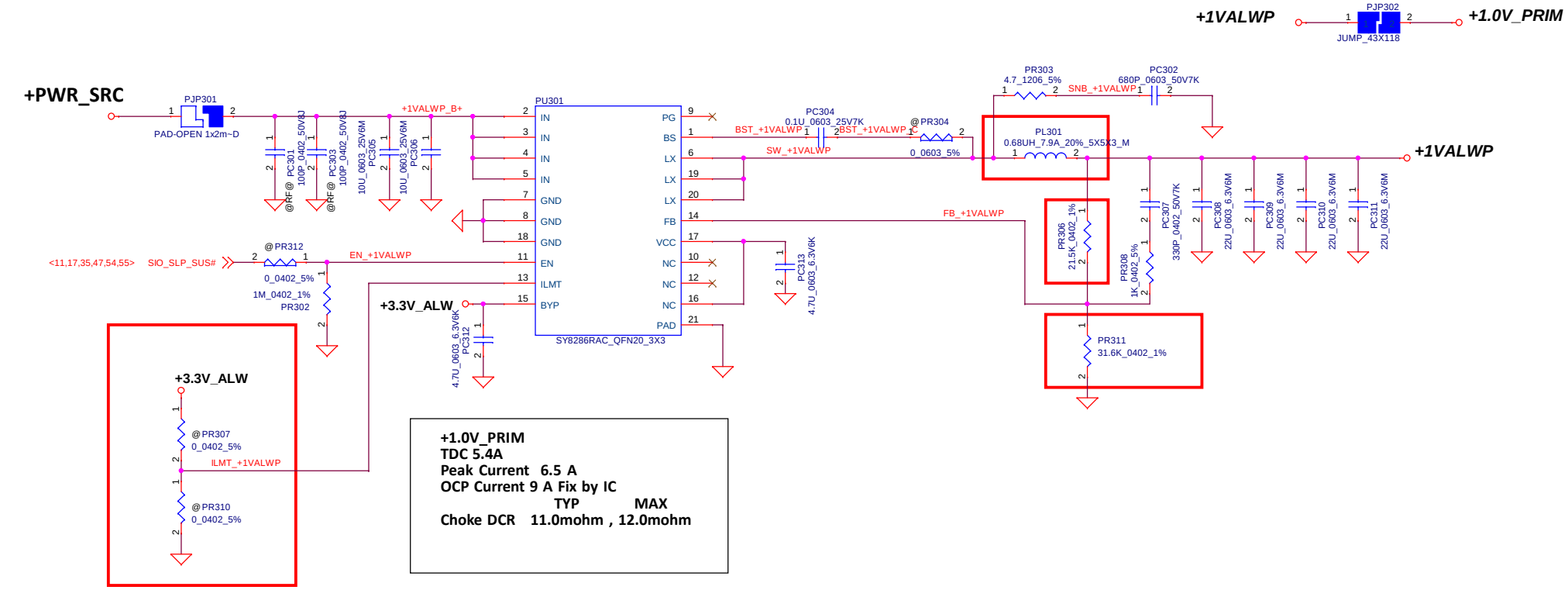

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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Compal Electronics, Inc.	
Title	+1VALWP
Size	Document Number: LA-E071P
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Date:	Wednesday, November 30, 2016
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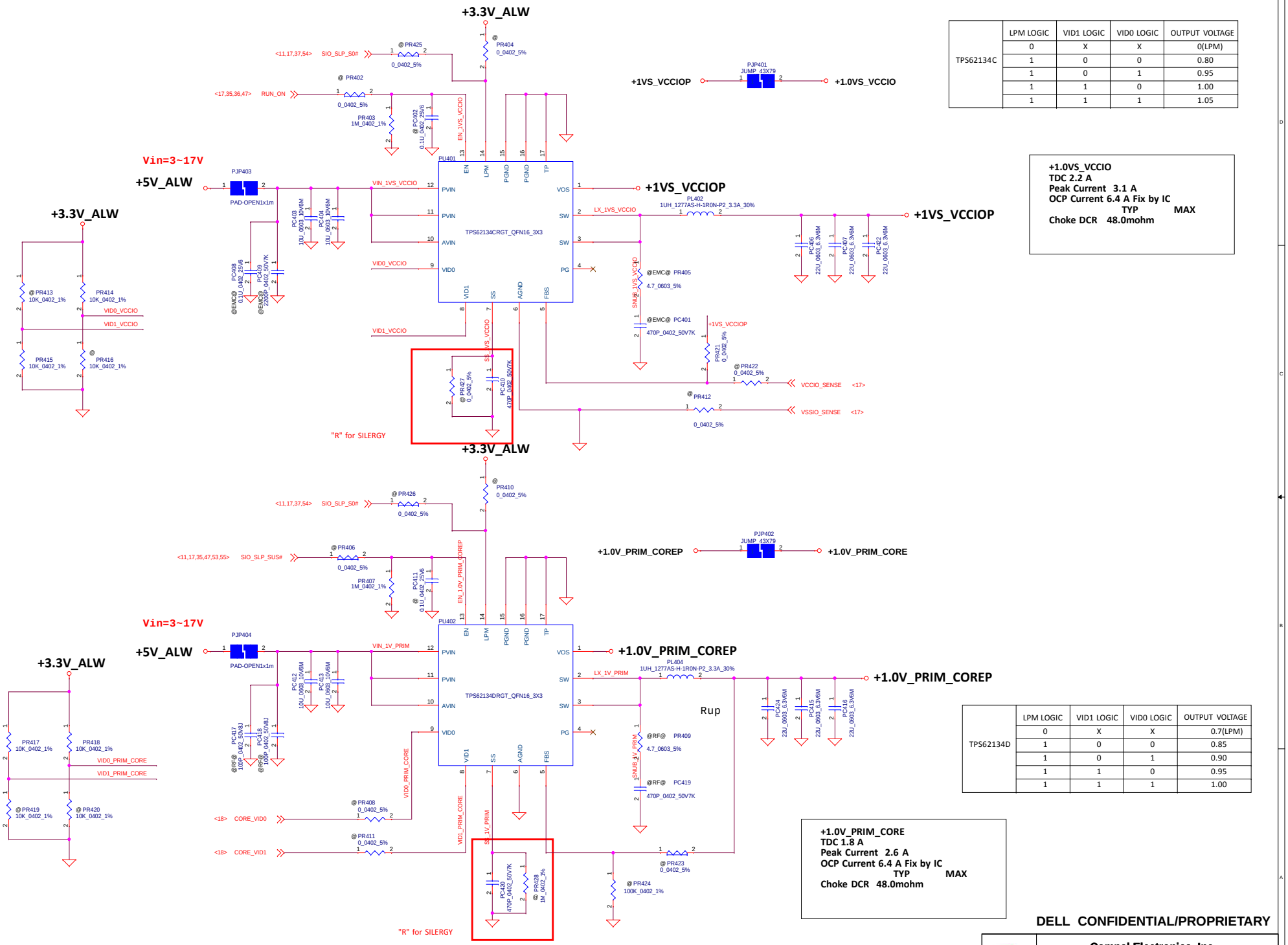

TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 2.2 A
Peak Current 3.1 A
OCP Current 6.4 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 6.4 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

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Compal Electronics, Inc.

Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

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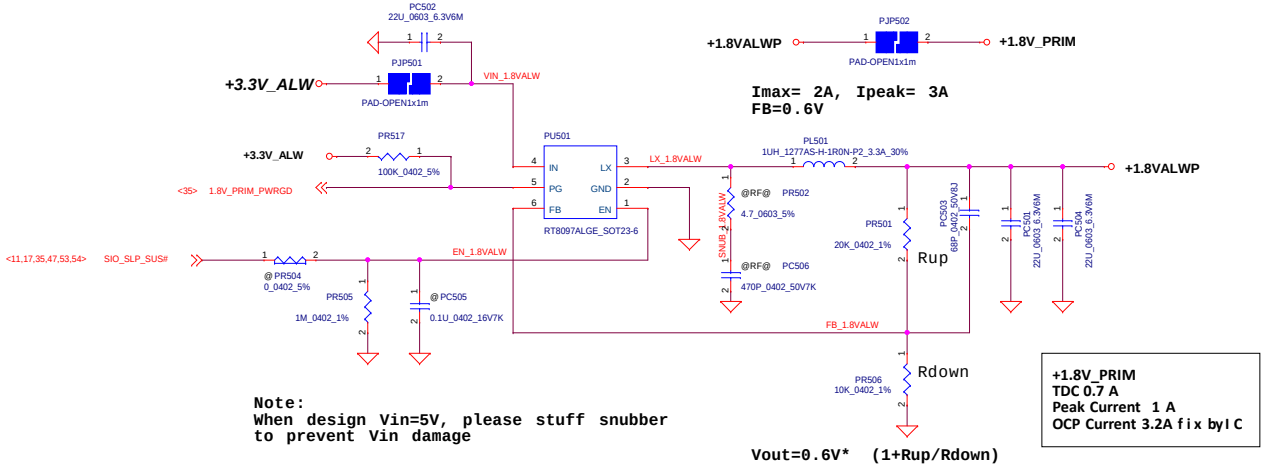

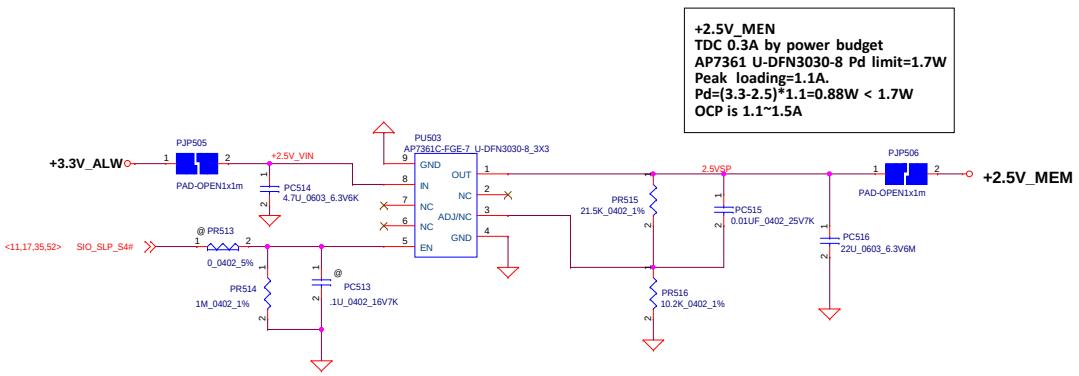

Compal Electronics, Inc.

Title: +1.8VALWP/+1.5VSP

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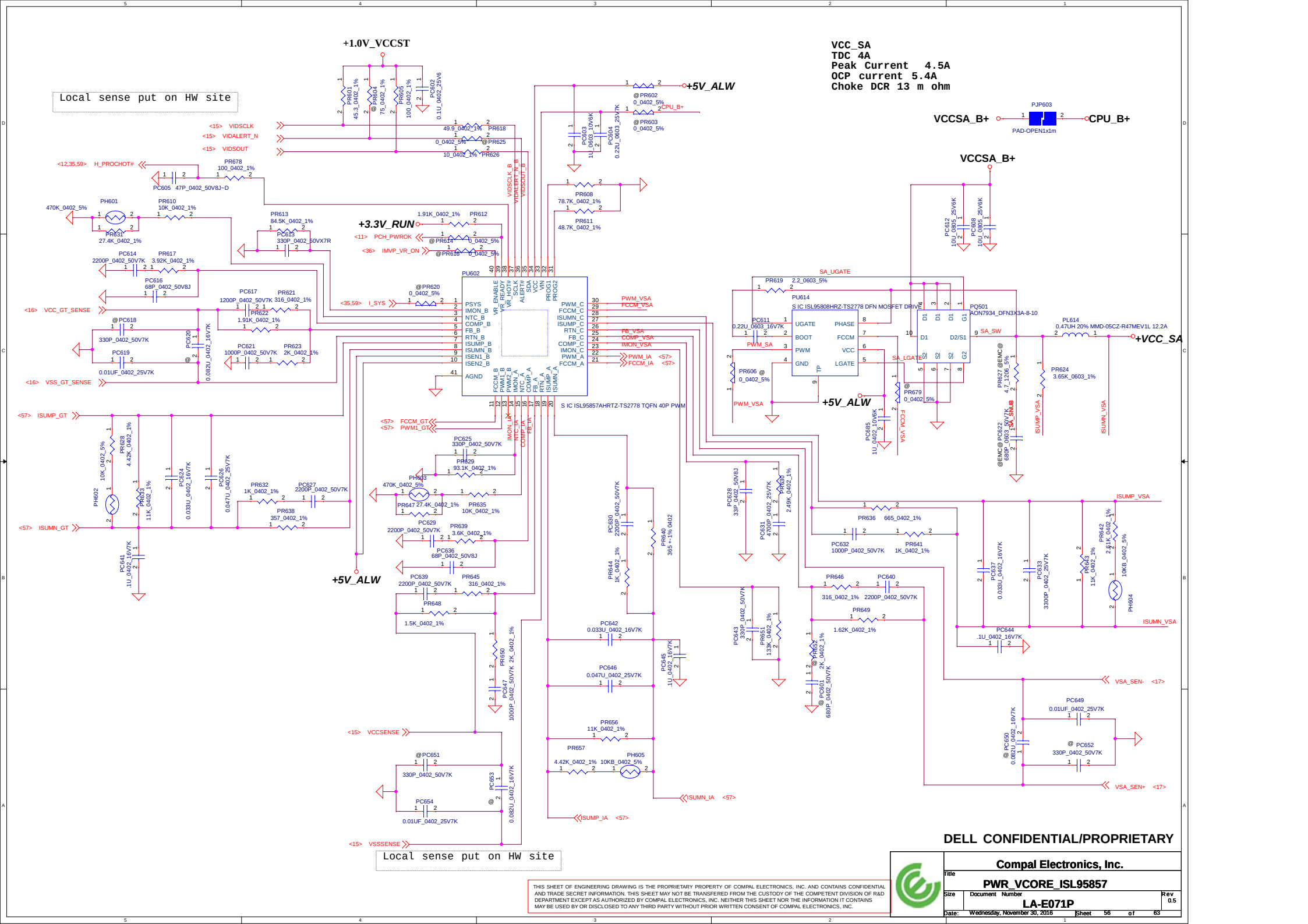
VCC_SA
TDC 4A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm
Local sense put on HW site
+1.0V_VCCST
+5V_ALW
+3.3V_RUN
VCCSA_B+
CPU_B+
PJP603
PAD-OPEN1x1m
PU602
S IC ISL95857AHRTZ-TS2778 TQFN 40P PWM
PU614
S IC ISL95808HRZ-TS2778 DFN MOSFET DRIVE
PQ501
AON7934_DFN3X3A-8-10
+VCC_SA
Local sense put on HW site
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Compal Electronics, Inc.
Title
PWR_VCORE_ISL95857
Size
Document Number
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Rev
0.5
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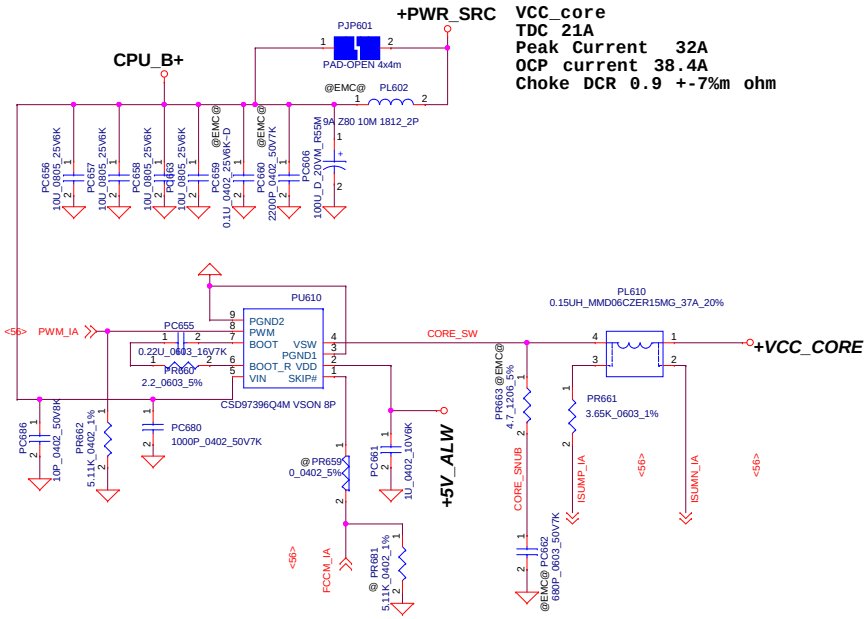
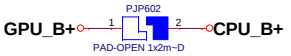
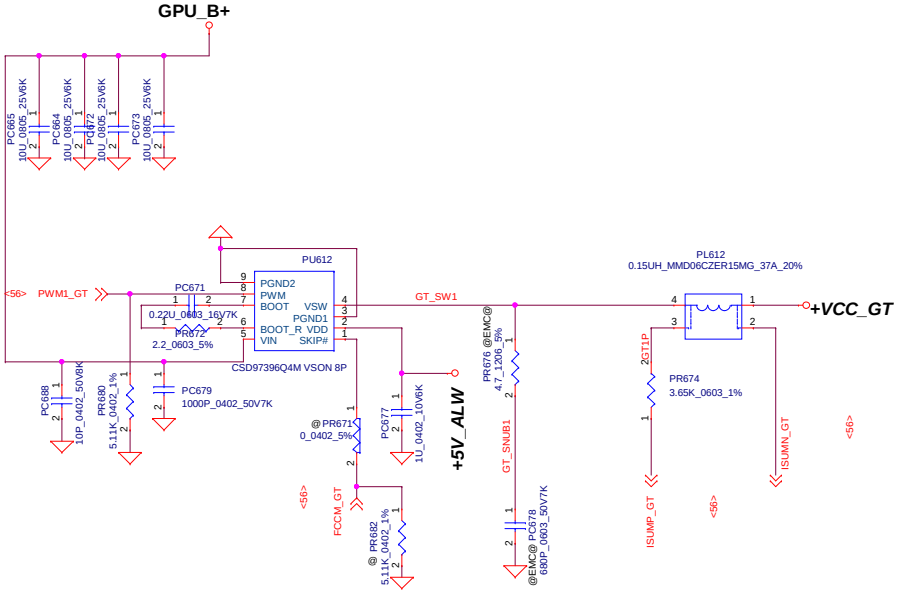


VCC_core
TDC 21A
Peak Current 32A
OCP current 38.4A
Choke DCR 0.9 +-7%m ohm

VCC_GT
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-7%m ohm





Compal Electronics, Inc.

Title: **PWR_VCORE_ISL95857**

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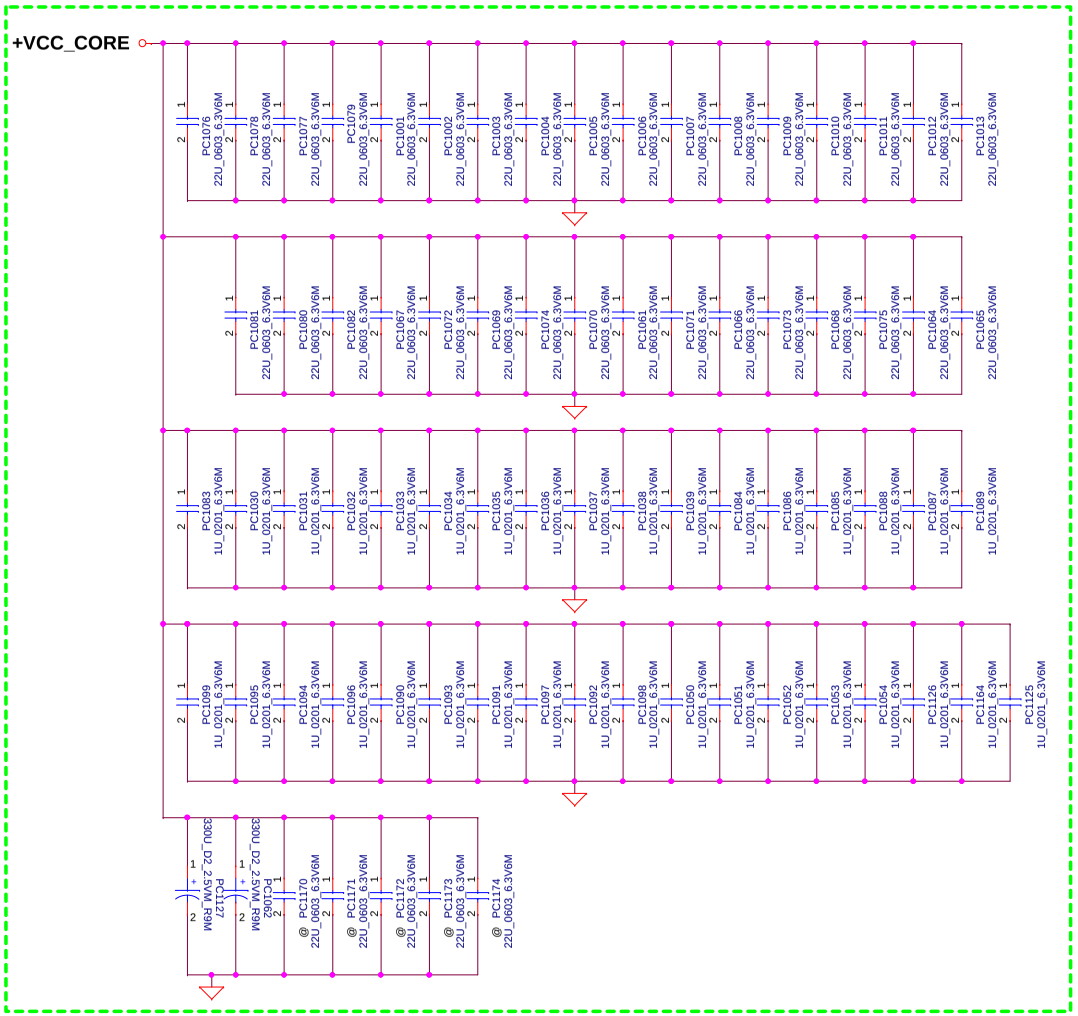
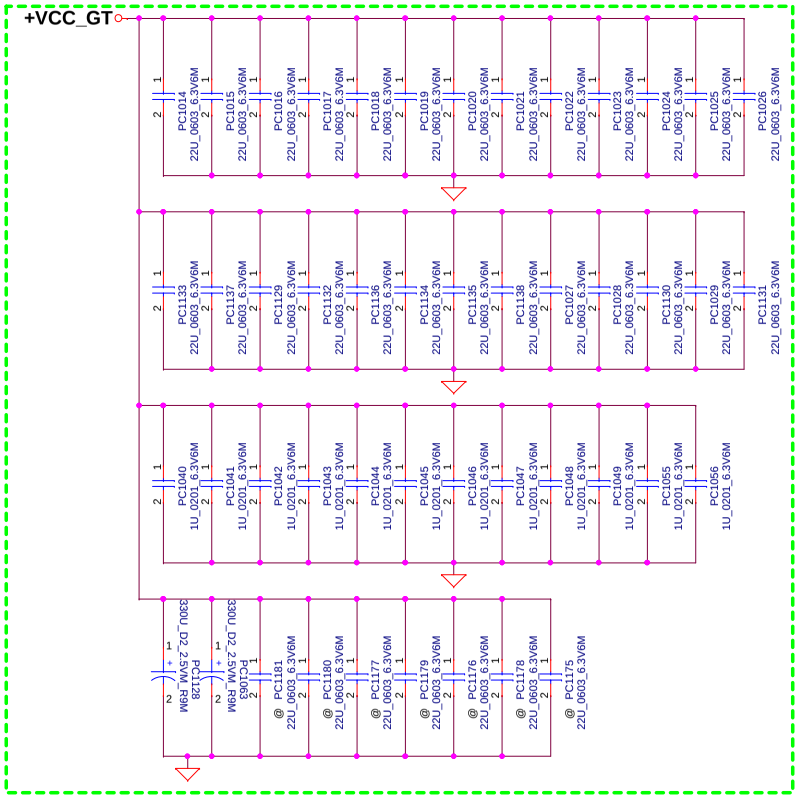
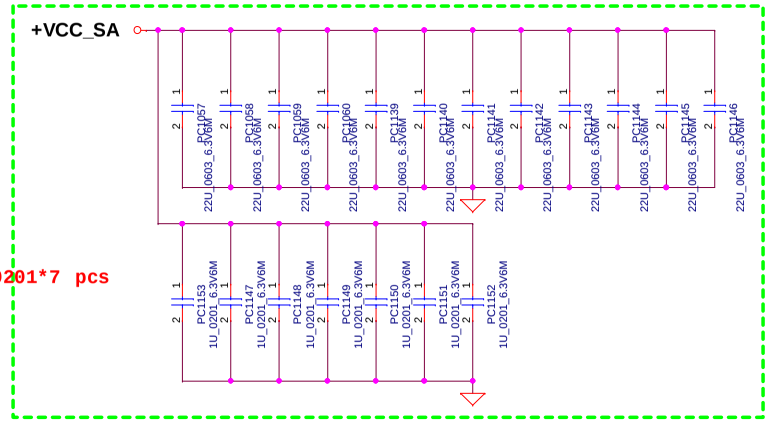
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs



VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs





VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

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Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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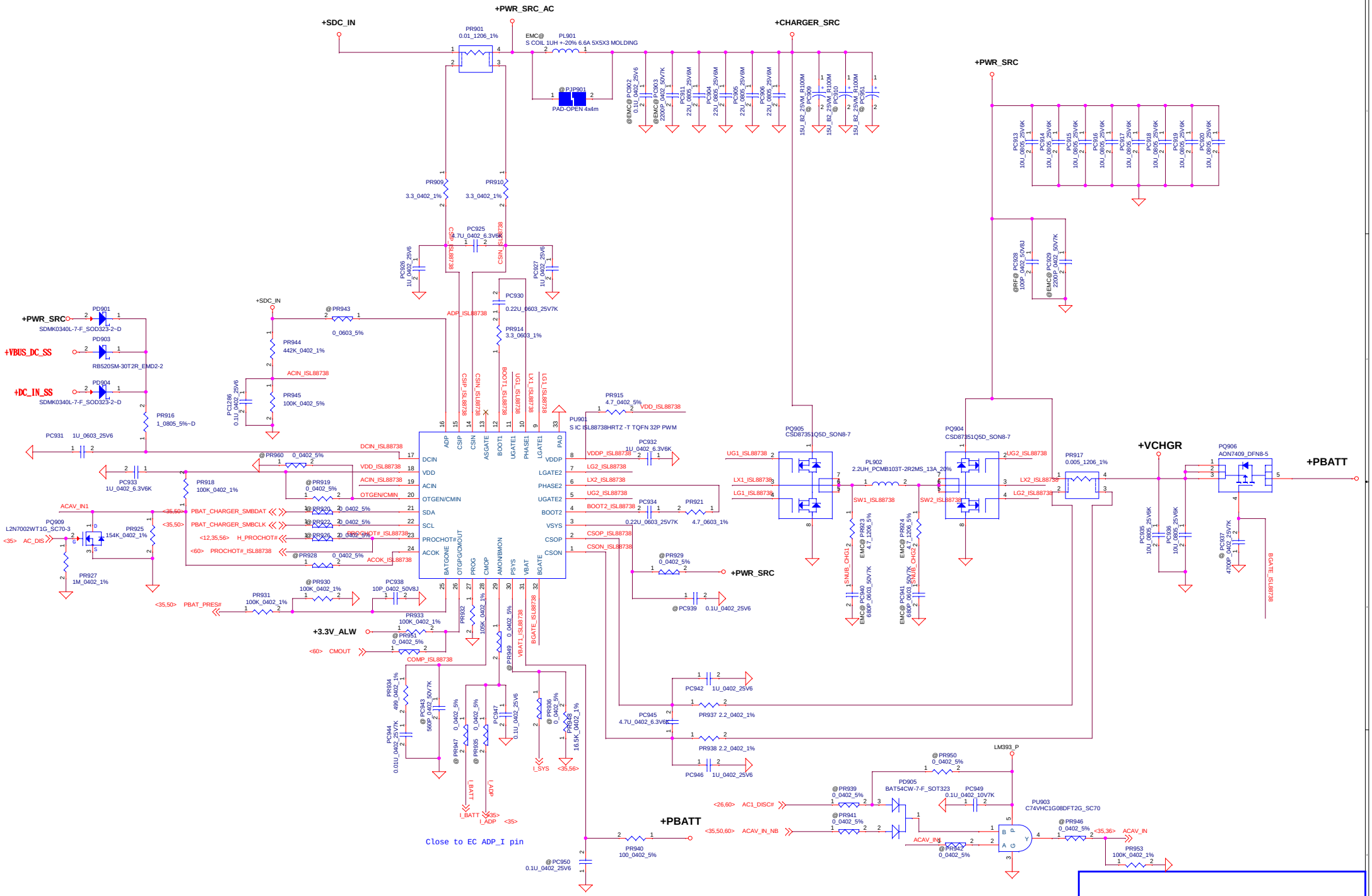
+SDC_IN
+PWR_SRC_AC
+CHARGER_SRC
+PWR_SRC
+VBUS_DC_SS
+DC_IN_SS
+3.3V_ALW
+PBATT
+VCHGR
PU901
S IC ISL88738HRTZ -T TQFN 32P PWM
PQ901
PQ902
2.2UH_PCMB103T-2R2MS_13A_20%
PQ904
CSD87351Q5D_SON8-7
PQ905
CSD87351Q5D_SON8-7
PQ906
AON7409_DFN8-5
PU903
C74VHC1G08DFT2G_SC70
LM393_P
Close to EC ADP_I pin
Compal Secret Data
Issued Date 2014/10/24
Deciphered Date 2015/08/31
Compal Electronics, Inc.
P47-PWR CHARGER ISL9237 (Colay)
LA-E071P
Rev 0.5
Wednesday, November 30, 2016
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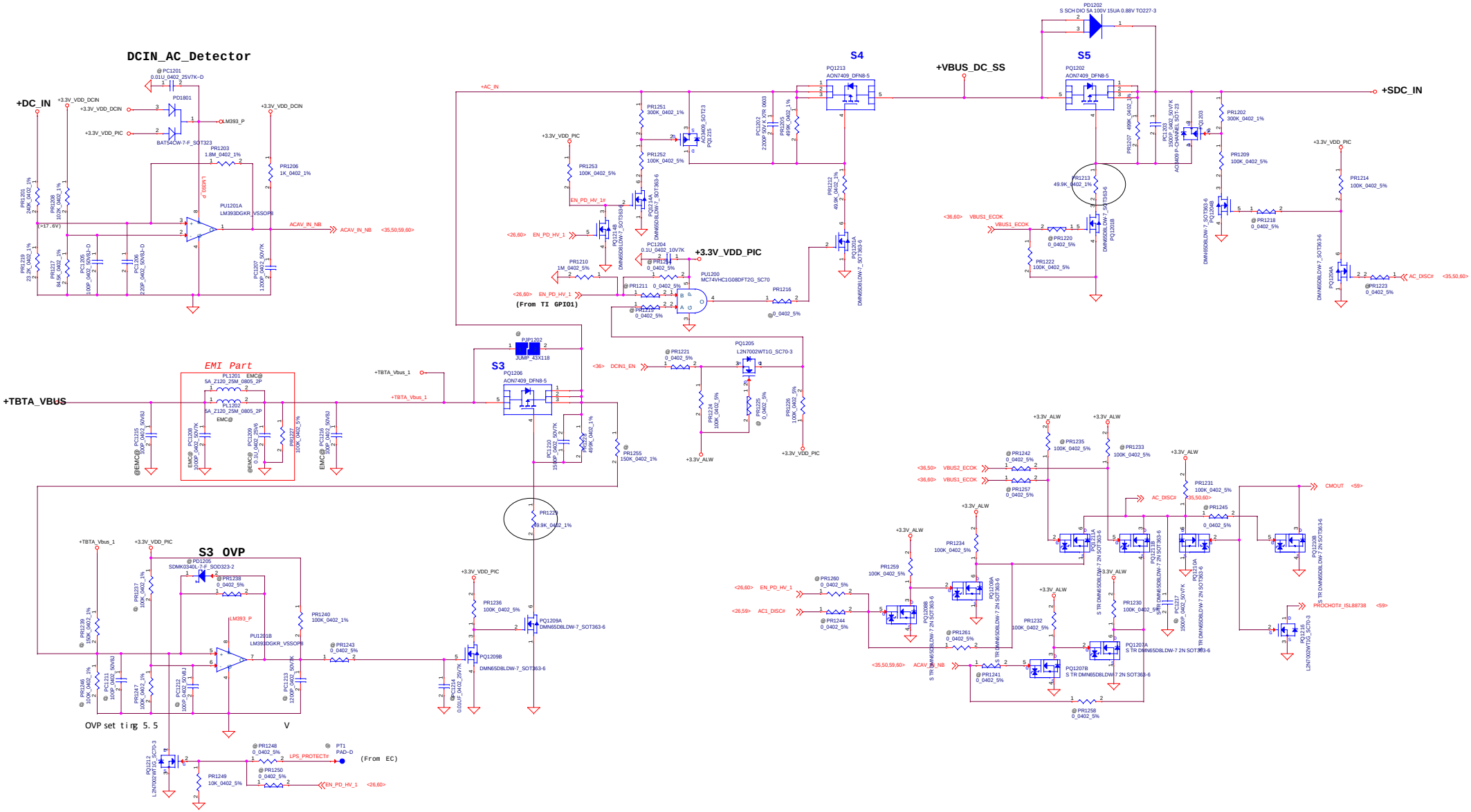

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Compal Electronics, Inc.	
Title	ParkCity_TypeC_PD
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	PU501 PG connect to +1.8V_RPIM_PWRGD & Pull high to 3.3V	modify power rail PU501, pull high to 3.3V and connect netname +1.8V_PRIM_PWRGD	X00
2	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 03/03	Compal	remove +1.5V_RUN	remove PU502 power rail	X00
3	52	+1.2V_MEM/ +0.6V_DDR	2016 03/07	Compal	remove 1.2V_DDR_PG	remove 1.2V_DDR_PG,remove PR201	X00
4	60	1Type-C PD Selector	2016 03/14	Compal	ESD part repeat with PD1204 and DT4	remove PD1204	X00
5	60	1Type-C PD Selector	2016 03/17	Compal	to add S4 quick turn off	add PQ1214 and PD1801	X00
6	56	+VCCSA_ISL95857	2016 05/24	Compal	change solution version to fix PS4 funciton issue	change PU602 to ISL95857AHRTZ-T	X00
7	59 60	CHARGER 1Type-C PD Selector	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Charger: Add PR960 and depop PR919 let the PU901.20 CMIN connect to GND. Add 1 net PROCHOT#_ISL88738 TypeC: Add PQ1216 to drive the PROCHOT# and PC1217 to do the reserve.	X01
8	60	1Type-C PD Selector	2016 05/30	Compal	Change the S4 fast turn off circuit to avoid the leakage	Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN	X01
9	60	1Type-C PD Selector	2016 06/13	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	PR1219 change from 22.6K to 23.2K. SD034232280	X01
10	56~ 57	VCCSA_ISL95857 VCC_CORE/ GT_ISL95857	2016 06/13	Compal	location alignment	VCCSA change the PU606 to PU614 and PL601 to PL614 IA change the PU603 to PU610 and PL603 to PL610 GT change the PU604 to PU612 and PL604 to PL612	X01
11	59	CHARGER	2016 06/13	Compal	To decrease the charger input leakage voltage for TypeC AC	Change the PD903 from SCS0340L010 to SCS00006C00.	X01
12	50 60	+DCIN 1Type-C PD Selector	2016 06/17	Compal	To solve the MOS leakage problem to avoid the error active	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR10, PR1251 and PR1202 change to 300K from 100K ohm.	X01
13	51,53 59	5V/3.3V CHARGER	2016 06/17	Compal	EMI/RF solution	RF:PC103 change to 82pF,PR106,PC112,PR303,PC302 pop EMI:PL602 depop,PR914 0 ohm change to 3.3 ohm,PR921 2.2ohm change to 4.7 ohm ,PR923,PR924,PC940,PC941 pop	X01
14	53	1VALWP	2016 06/27	Compal	Change the SY8286 for cost down plan	Change the power solution to SY8286R from SYX196D	X01
15	59	CHARGER	2016 07/01	Compal	Change charger version	Change the charger version to B version from A version.	X01
16	60	1Type-C PD Selector	2016 07/01	Compal	Reserve the OVP function to protect the typeC device.,	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212, PD1205 PC1213, PC1214 and PR1248 Change the PR1247 from 200K_0402_1% to 100K_0402_5% ohm Re-modify the S11 OVP description to S3 OVP.	X01
17	56	VCCSA_ISL95857	2016 07/01	Compal	Regulate VR load line	PR640 change to 365 ohm SD034365080,PR636 change to 1.27k ohm SD034127180 PR638 change to 357 ohm SD034357080,PC633 depop PC647,PC621 change to 1000pF	X01

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1	34	HW	2016/05/24	COMPAL	For Schematic align	Remove RA2	0.2(X01)
2	35	HW	2016/05/24	COMPAL	Symbol pin name change	UE1.C1 pin name change to GPIO024/nRESETI	0.2(X01)
3	9	HW	2016/05/24	COMPAL	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
4	25	HW	2016/05/24	COMPAL	Symbol pin name change	UT9.20 pin name change to SNK_CAD/DCI_DAT, UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
5	6	HW	2016/05/24	COMPAL	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
6	25	HW	2016/05/24	COMPAL	Disable AUX snoop feature	Pop RT308	0.2(X01)
7	33,40	HW	2016/05/24	COMPAL	Remove HDD LED MUX feature	Depop RN100/RN101	0.2(X01)
8	35	HW	2016/05/24	COMPAL	PORT80_DET#	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
9	6	HW	2016/05/24	COMPAL	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
10	17	HW	2016/05/24	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
11	46	HW	2016/05/24	COMPAL	For DFX request	H1/H2/H3/H4/H7/H8/H34 footprint remove "-G"	0.2(X01)
12	25	HW	2016/05/27	COMPAL	For Schematic align	SW2_DP1_HPD Add RT380 place near TUSB546	0.2(X01)
13	30	HW	2016/06/01	INTEL	Intel reviwe result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
14	37,38	HW	2016/06/07	DELL	change to Nuvoton TPM form ATMEL TPM	Delete ATMEL TPM circuit, Add Nuvoton TPM circuit	0.2(X01)
15	12	HW	2016/06/07	INTEL	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
16	33	HW	2016/06/07	INTEL	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
17	33	HW	2016/06/07	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
18	35	HW	2016/06/07	COMPAL	For MEC5105K-D1-TN sample	1.UE1 change to SA00009GL00(S IC MEC5105K-D1-TN WFBGA 169P EC) 2.Depop RE361,Pop RE360,RE362	0.2(X01)
19	41	HW	2016/06/17	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	Depop RN5	0.2(X01)
20	38,45	HW	2016/06/20	COMPAL	ME request	1.JKBTP1 change from HRS_TF49-20S-0P5SH_20P-T to CVILU_CF5020FD0RK-05-NH_20P-T 2.JUSH1 change from HRS_TF49-26S-0P5SH_26P-T to CVILU_CF5026FD0RK-05-NH_26P-T	0.2(X01)

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21	34	HW	2016/06/20	COMPAL	Base on Audio EA result	RA7,RA8 change from 24.9 to 16.2 ohm(SD00001U900)	0.2(X01)
22	30	HW	2016/06/22	COMPAL	EMI request	CL22 change from 1500pF to 10pF (SE167100J80 S CER CAP 10P 3KV J NPO 1808 AC250V X2Y3)	0.2(X01)
23	30	HW	2016/06/22	COMPAL	ESD request	Reserve DL1 SCA00000T00 (S ZEN ROW PESD5V0U2BT 3P C/C SOT23 ESD)	0.2(X01)
24	29	HW	2016/06/22	COMPAL	EMI request	Change LV1 from SM01000BV00 to SM01000NY00	0.2(X01)
25	29	HW	2016/06/22	COMPAL	ME request	JIR1 change from SP010023D00 to SP010013W20	0.2(X01)
26	35	HW	2016/06/22	DELL	The posibility of GPIO map update,RTCRST_ON change from GPIO141 to GPIO122	Add RE514(@),RE515 for RTCRST_ON	0.2(X01)
27	36	HW	2016/06/22	COMPAL	For pre-config TPM	POP RZ363, De-POP RZ112,RZ113,RZ111,QZ9	0.2(X01)
28	29	HW	2016/06/22	COMPAL	RF request	CC27 pop 47pF	0.2(X01)
29	38	HW	2016/06/29	COMPAL	X8 have no difference JUSH1 pin define concern	Depop DZ7,Pop RZ87	0.2(X01)
30	38	HW	2016/06/29	COMPAL	Let USH_PWR_STATE# keep low at S5	RZ10 change from 1M to 100k ohm	0.2(X01)
31	36	HW	2016/06/29	COMPAL	Foe X01 Board ID	RE79 change from 240k to 130k ohm	0.2(X01)
32	24	HW	2016/07/04	COMPAL	For VGA test result	Pop RV121/RV122/CV132/CV133	0.2(X01)
33	41	HW	2016/06/29	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)
34	35, 36	HW	2016/08/04	COMPAL	Vendor schematic review	1. Add net WRST# to UE2.4 and CE500 1uf (SE000000K80) 2. Add RE523 0 ohm for UE2 power pin soft start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT 5. Change RPE12.2 to RE525 (10Kohm) for EXPANDER_GPU_SMCLK 6. Reserve CE504~CE505 for EXPANDER_GPU_SMDAT/CLK to GND.	0.3(X02)
35	14	HW	2016/08/04	COMPAL	Intel suggestion	RC137 change from 1K to 3K	0.3(X02)
36	27	HW	2016/08/04	COMPAL	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
37	45	HW	2016/08/04	COMPAL	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
38	26	HW	2016/08/04	COMPAL	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
39	33, 38	HW	2016/08/09	COMPAL	DFB request	SMT concern DZ1, DZ2, DZ5, DZ6 PCB pad is too small, suggest use the symbol "RB520SM-30T2R_EMD2-2" follow PD903	0.3(X02)
40	34, 36	HW	2016/08/10	COMPAL	Footprint align	DA8, DE1 follow symbol "RB520SM-30T2R_EMD2-2"	0.3(X02)
41	46	HW	2016/08/11	COMPAL	ME request	H9 footprint change from "H_2P8-G" to "H_2P8"	0.3(X02)
42	36	HW	2016/08/11	COMPAL	schematic align	add power rail +3.3V_ALW_UE2 for UE2	0.3(X02)

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43	31	HW	2016/08/30	COMPAL	[ME] SD card issue	1. change JSD1 form "T-SOL_156-2000302608" to "T-SOL_158-1000902614" 2. QR1.3 connect GND	0.4(X02)
44	35	HW	2016/08/30	COMPAL	battery life	USH_DET# reserve RE526 (10K) PU to +3.3V_Run, follow X7	0.4(X02)
45	37	HW	2016/09/08	COMPAL	TPM change to NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.5(X03)
46	35, 36	HW	2016/09/08	COMPAL	Expander I/O change from ITE8010 to MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.5(X03)
47	35	HW	2016/09/08	COMPAL	Board ID	Change RE79 to 33kohm (SD028330280)	0.5(X03)
48	35	HW	2016/09/08	COMPAL	schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.5(X03)
49	35	HW	2016/09/08	COMPAL	EC request for power consumption	Add RE505 PU to +3.3V_ALW for LOM_CABLE_DETECT# (Reserve) Add RE532 PU to +3.3V_ALW for BCM5882_ALERT#	0.5(X03)
50	38	HW	2016/09/08	COMPAL	USH/B de-pop, pop on MB side	POP RZ8,RZ9 for USH SMBus	0.5(X03)
51	36	HW	2016/09/20	COMPAL	DELL request	Add RE536/RE537 for resistors for PCH_DPWROK circuit	0.5(X03)
52	35	HW	2016/09/20	COMPAL	WDT schematic option 2	use Option2: pop RE361 / depop RE362	0.5(X03)
53	34	HW	2016/09/20	COMPAL	EMI request	1. L6~L9 change to 80ohm bead (BLM15PD800SN1D, SM01000N000) for BR14/15 2. depop CA2, CA3 3. RA55,RA56 need to netin for changing location(LA15, LA16) with 33ohm bead (BLM15PX330SN1D,SM01000NA00)	0.5(X03)
54	36	HW	2016/10/09	COMPAL	BITS294007 - Sometimes need to press power button twice to power on system.	CE12 change to 2.2u (SE000008880) RE33 change to 1K (SD028100180)	0.5(X03)
55	24	HW	2016/10/09	COMPAL	U-line VGA EA PASS	depop RV121/RV122	0.5(X03)
56	26	HW	2016/10/09	COMPAL	TI CC pin for ESD request	CT85,CT86 change to 470p.(SE074471k80)	0.5(X03)
57	26	HW	2016/10/31	COMPAL	TI CC pin for EA	CT85,CT86 change to 820p.(SE000003W80)	1.0(A00)
58	26	HW	2016/10/31	COMPAL	EC watchdog reserve	add QE13,RE530,CE503	1.0(A00)
59	26	HW	2016/10/31	COMPAL	UE1.H8 to prevent EOS issue on MEC5105	Add RE539(100ohm) to CV2_ON	1.0(A00)
60	36	HW	2016/10/31	COMPAL	BOARD ID	Change RE79 to 4.3k ohm(SD028430180)	1.0(A00)
61	36	HW	2016/10/31	COMPAL	Change R1 to R3 for MP part	Change UL1 CP/N to SA000081G1L Change UE1 CP/N to SA00009GL30	1.0(A00)
62	36	HW	2016/10/31	COMPAL	For DFB request.	Close solder mask CMOS1 (-NPM) and other co-lay part	1.0(A00)
63	36	HW	2016/10/31	COMPAL	Service Mode Switch remove	Depop SW1 and RC222 and RC221 change to short pad	1.0(A00)
64	36	HW	2016/10/31	COMPAL	RE374 change BS to LPC@	RE374 change BS to LPC@	1.0(A00)
65	36	HW	2016/10/31	COMPAL	For MEC5105 rev. C	Pop RE362,RE536; Depop RE361,QE13,CE503,RE530,UE7,CE5,CE6,RE348,RE537	1.0(A00)