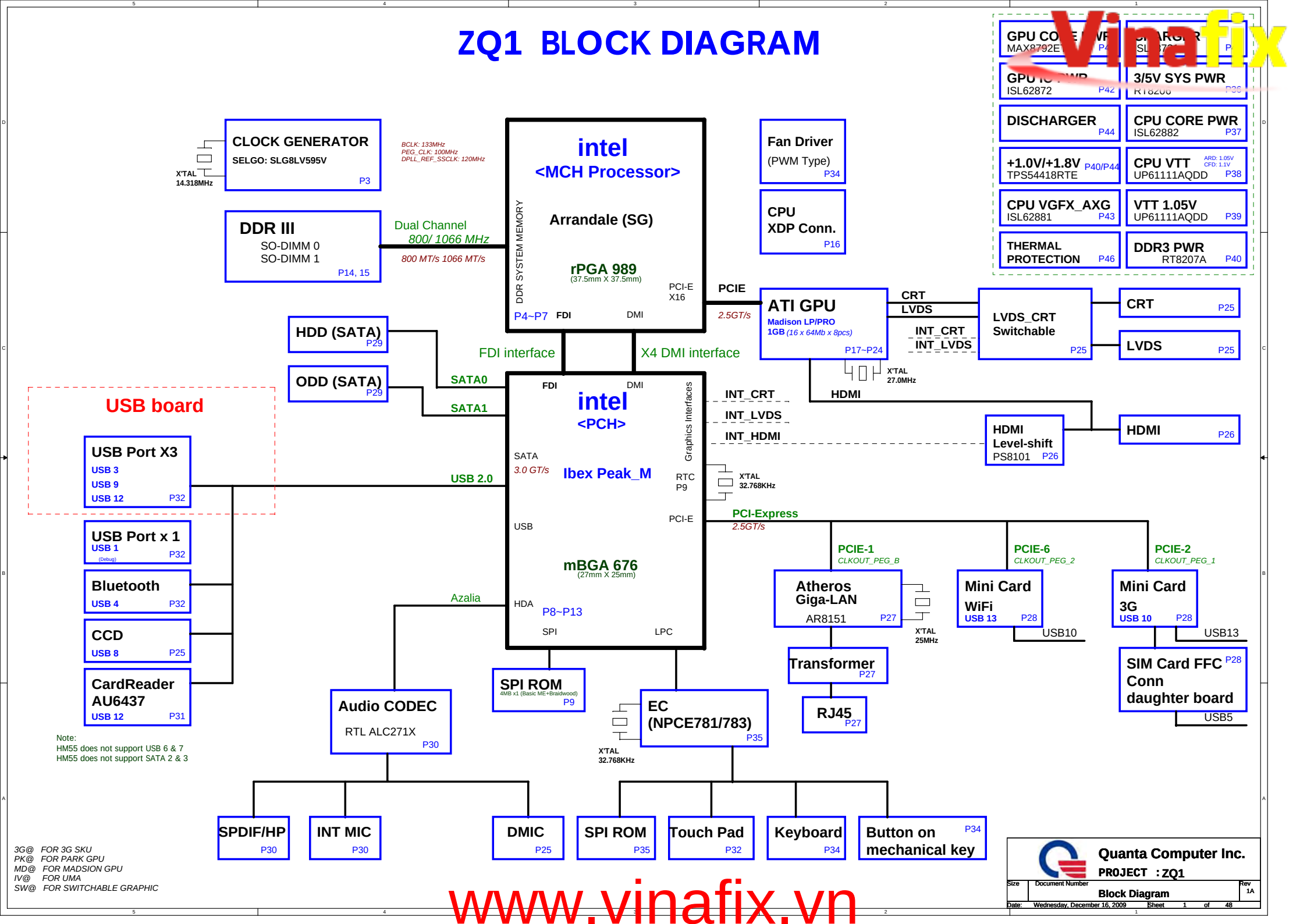
ZQ1 BLOCK DIAGRAM



3G@ FOR 3G SKU
PK@ FOR PARK GPU
MD@ FOR MADSION GPU
IV@ FOR UMA
SW@ FOR SWITCHABLE GRAPHIC

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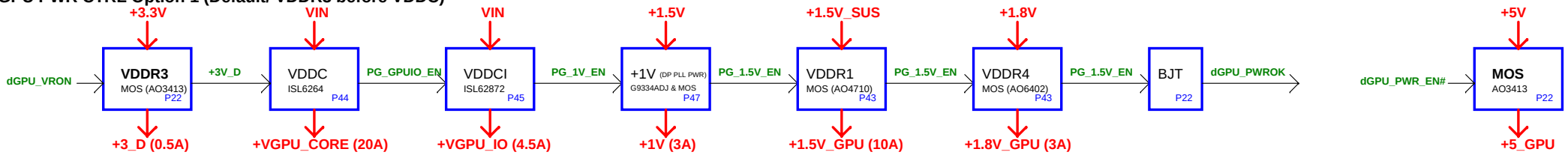
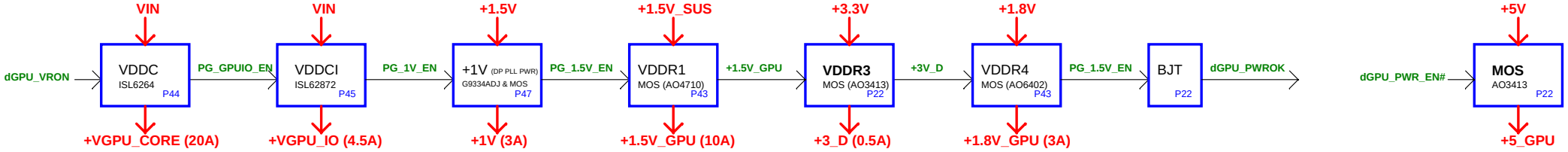
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



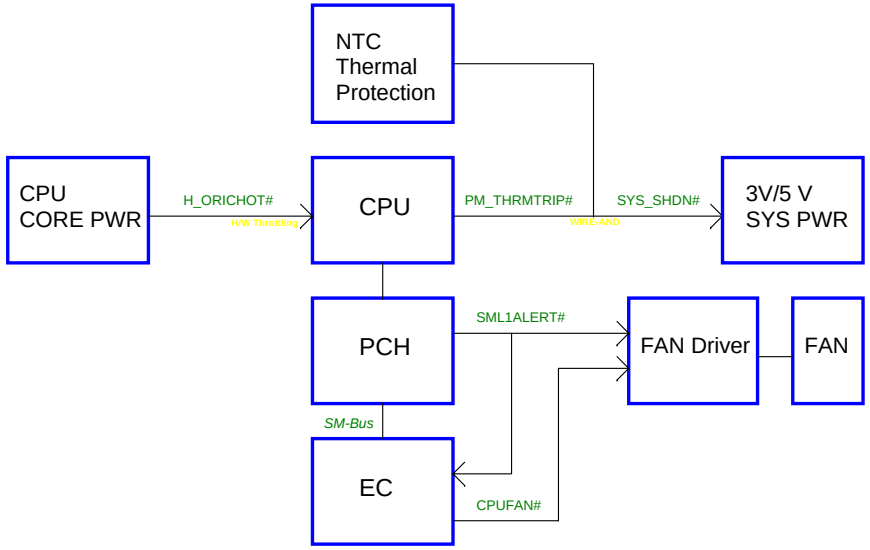
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5V_SUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

Thermal Follow Chart



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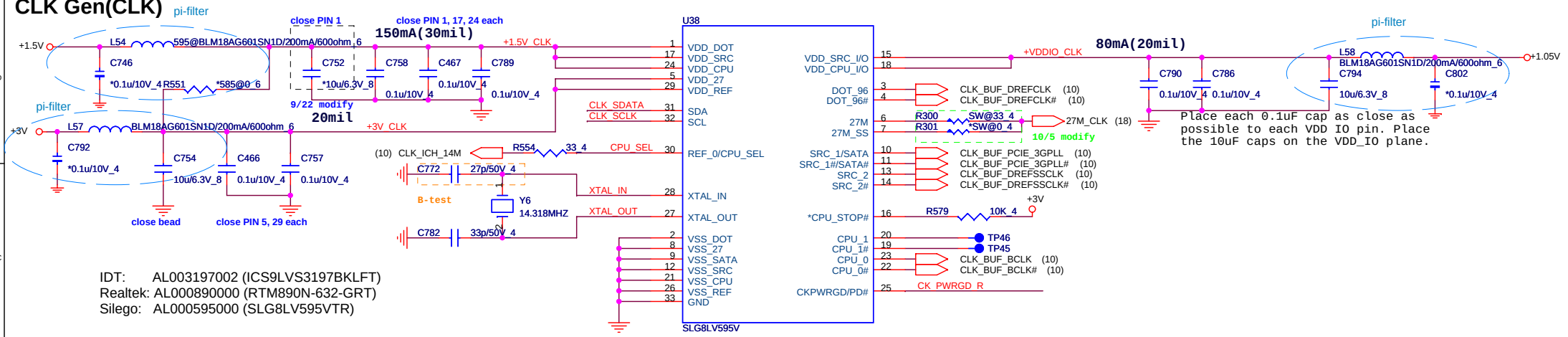
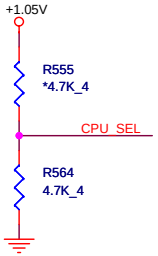
CLK Gen(CLK)



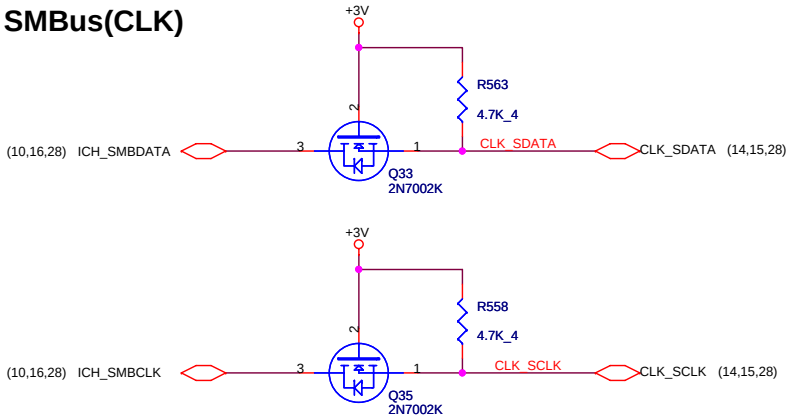
IDT: AL003197002 (ICS9LVS3197BKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select(CLK)

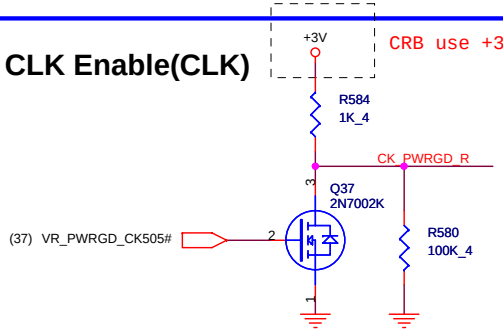


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



CLK Enable(CLK)



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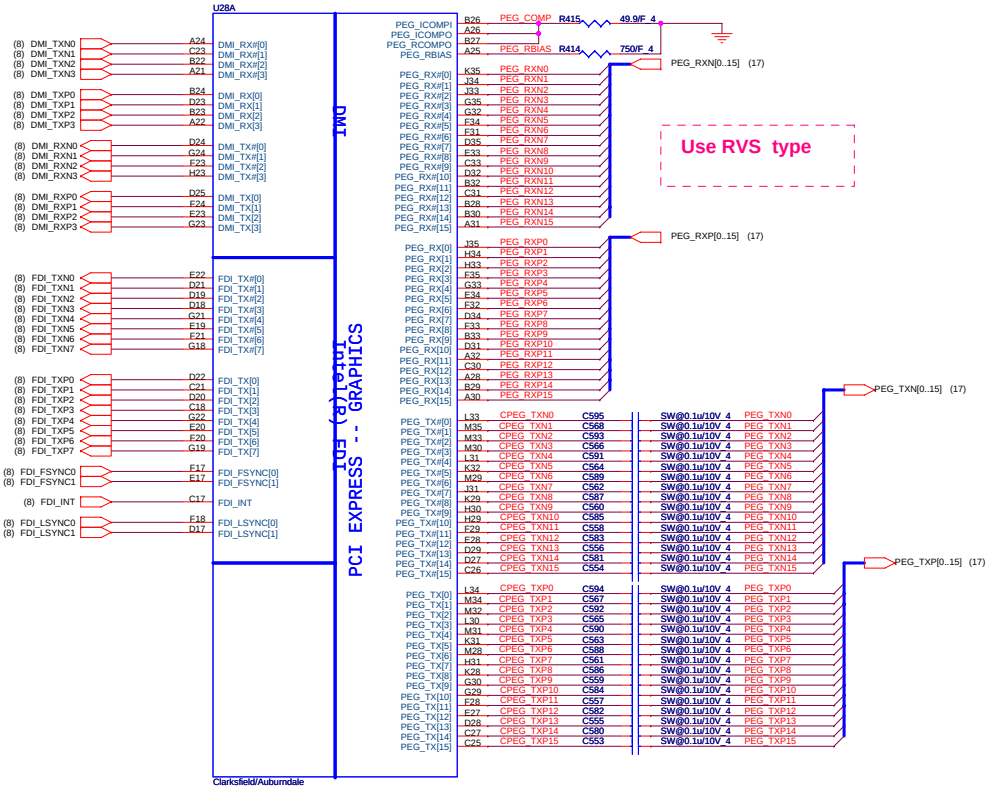
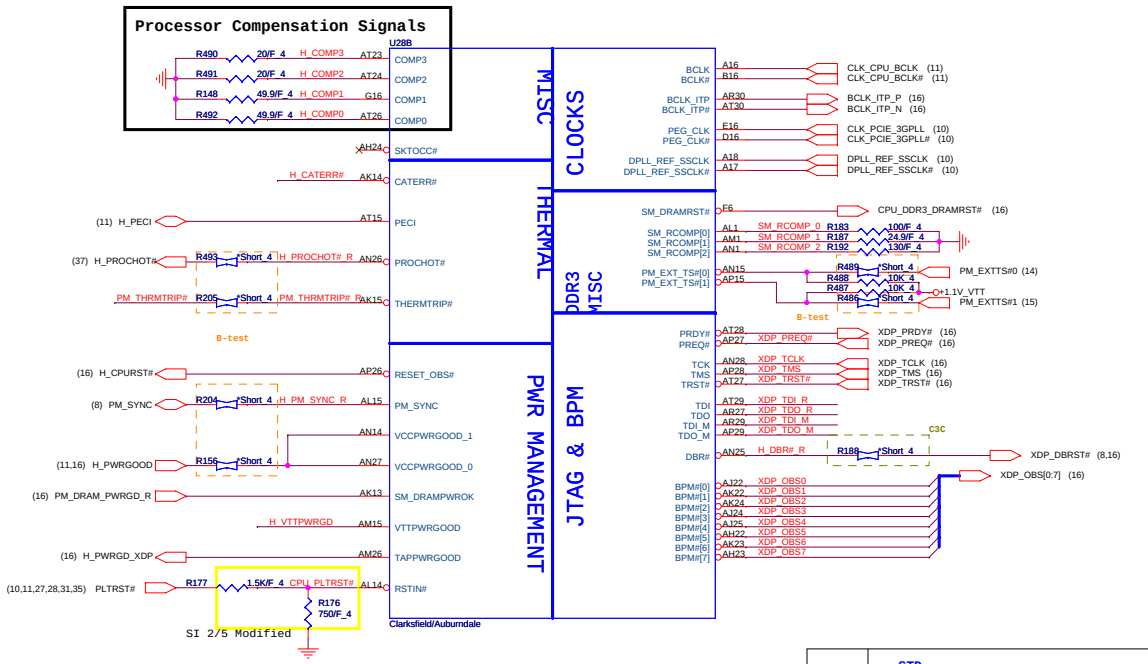
Arrandale_1(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



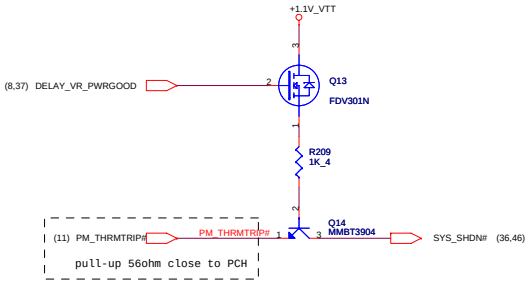
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



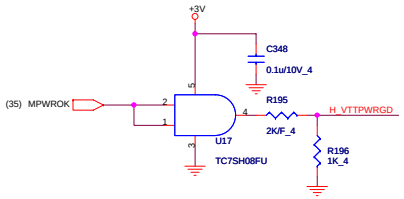
	STD
FOX	DGG^9000024
LTS	DGG^9000022
SUY	
MLX	

Standard: rpga989-aca-zif-069-k01-socket
Reverse: PZ98927-364R-01F-SOCKET

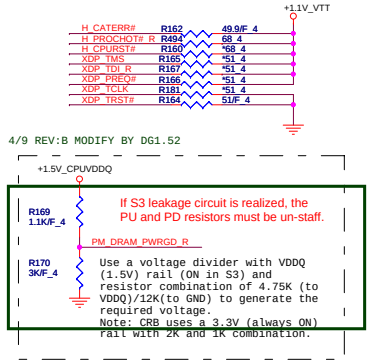
Thermaltrip protect(CPU)



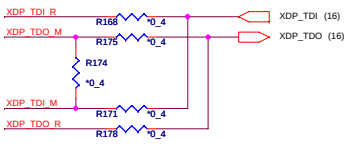
VTT PWR_Good(CPU)



Processor pull-up(CPU)



JTAG MAPPING(CPU)



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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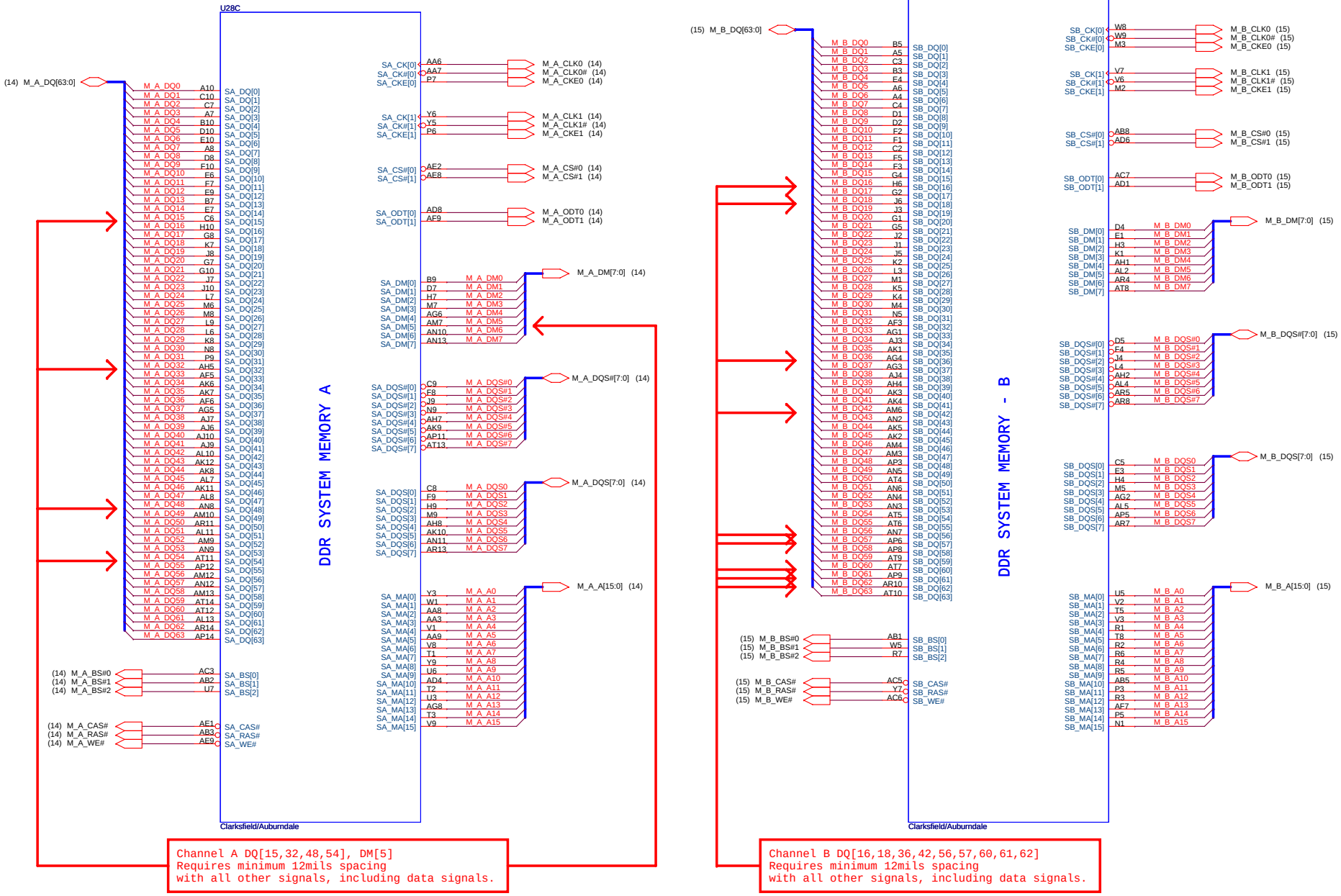
Arrandale_2(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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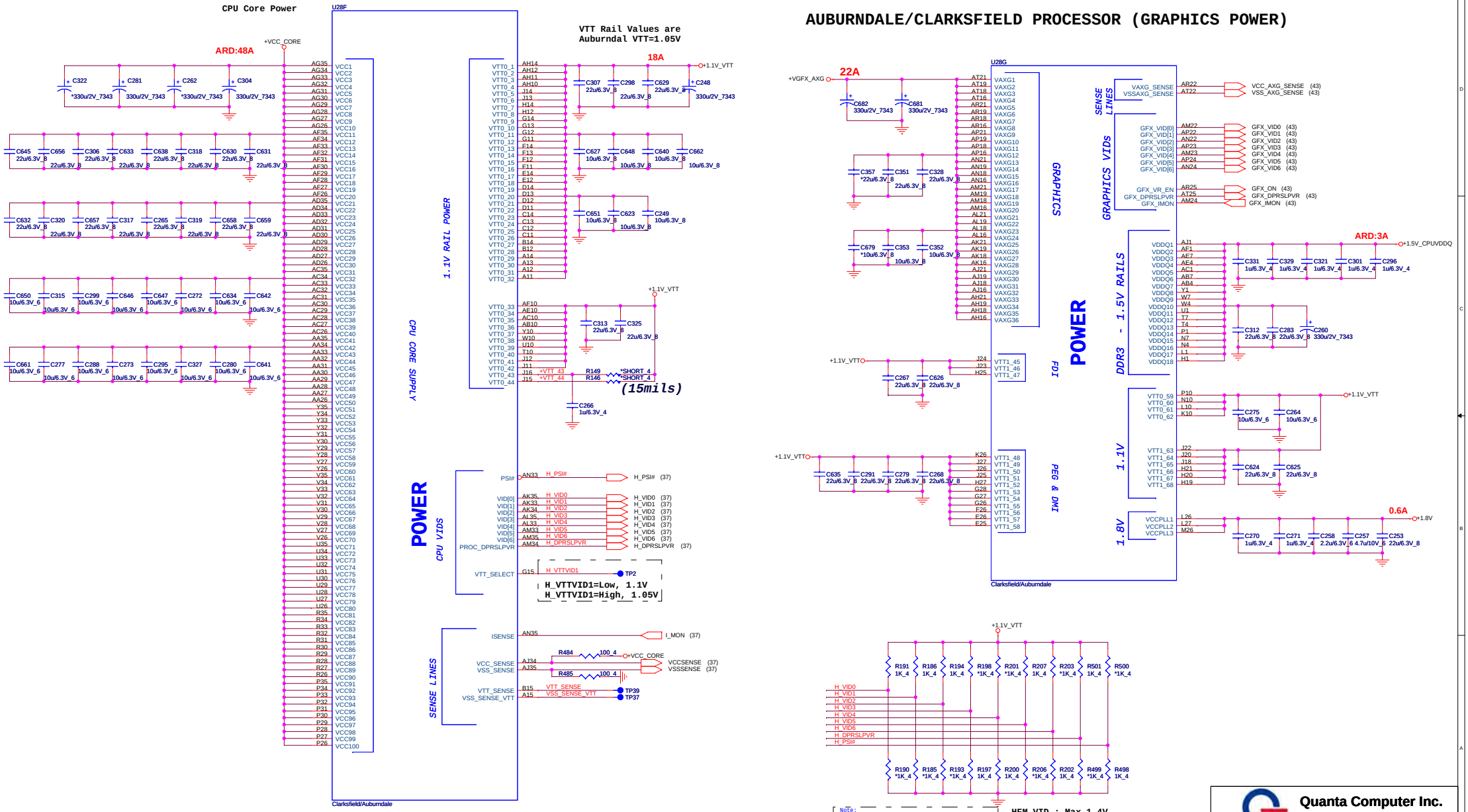
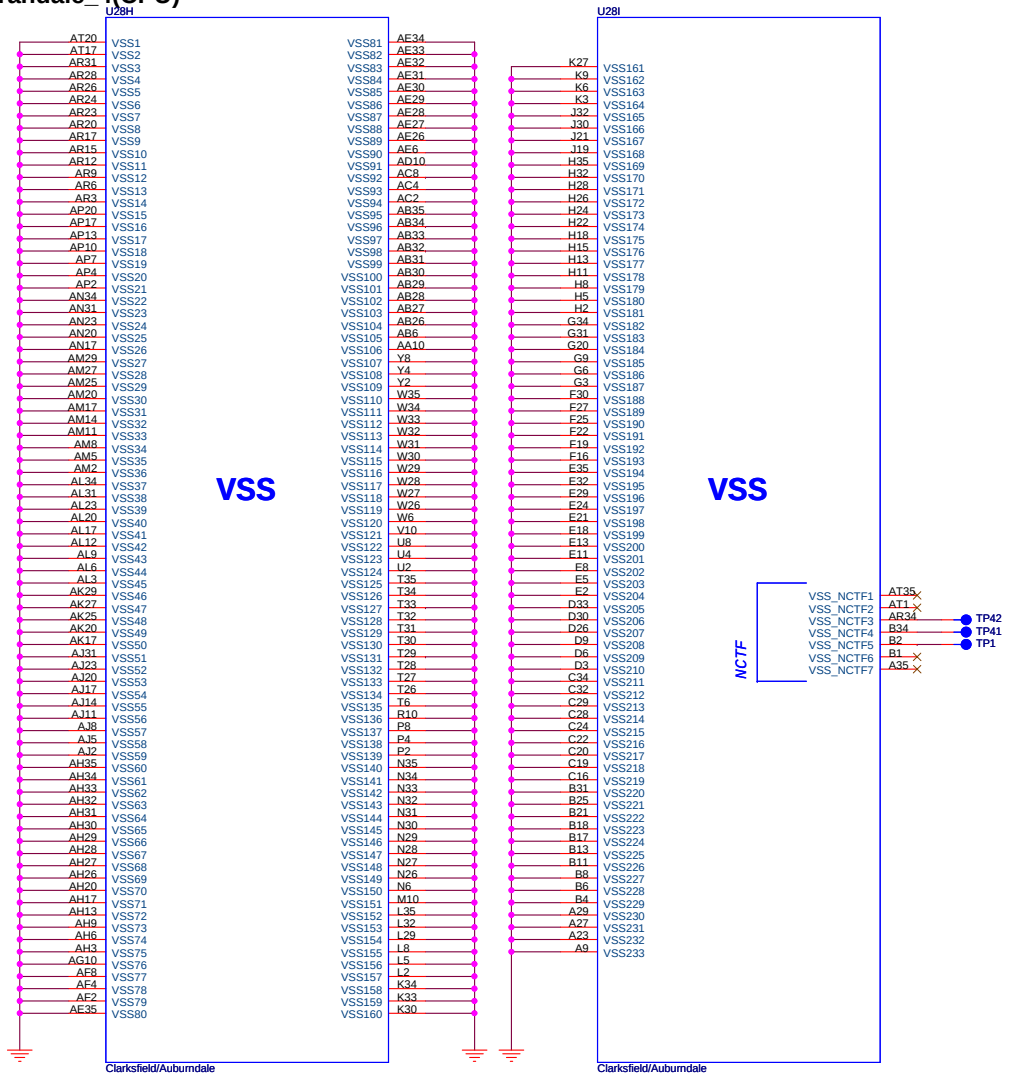
Arrandale_3(CPU)

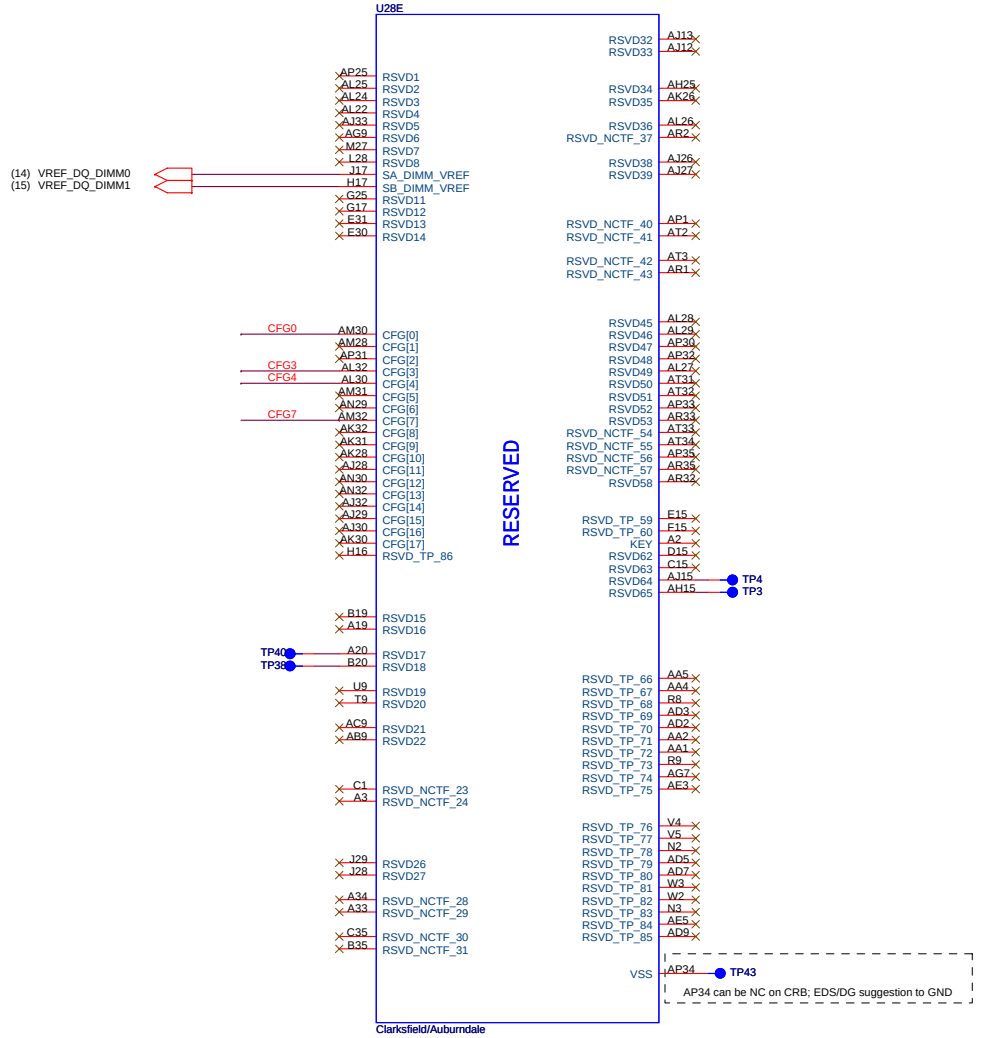


Arrandale_4(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

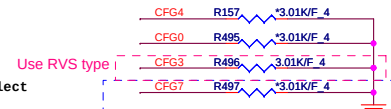


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```



Use RVS type

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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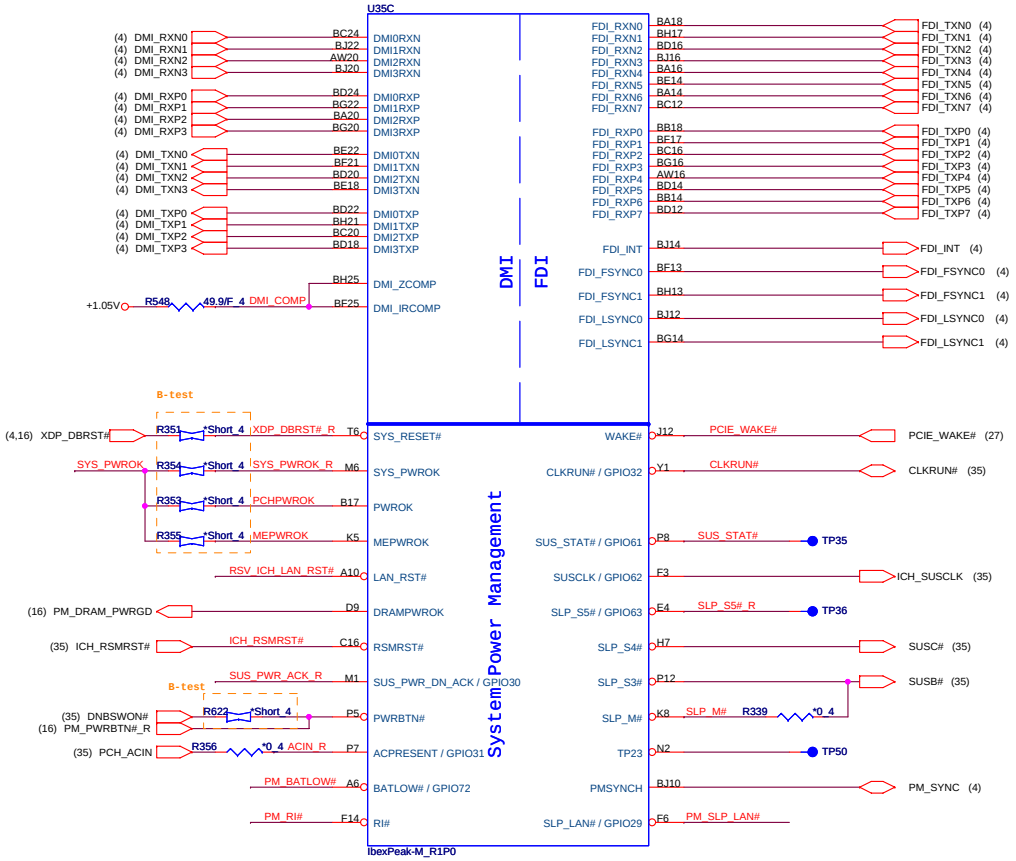
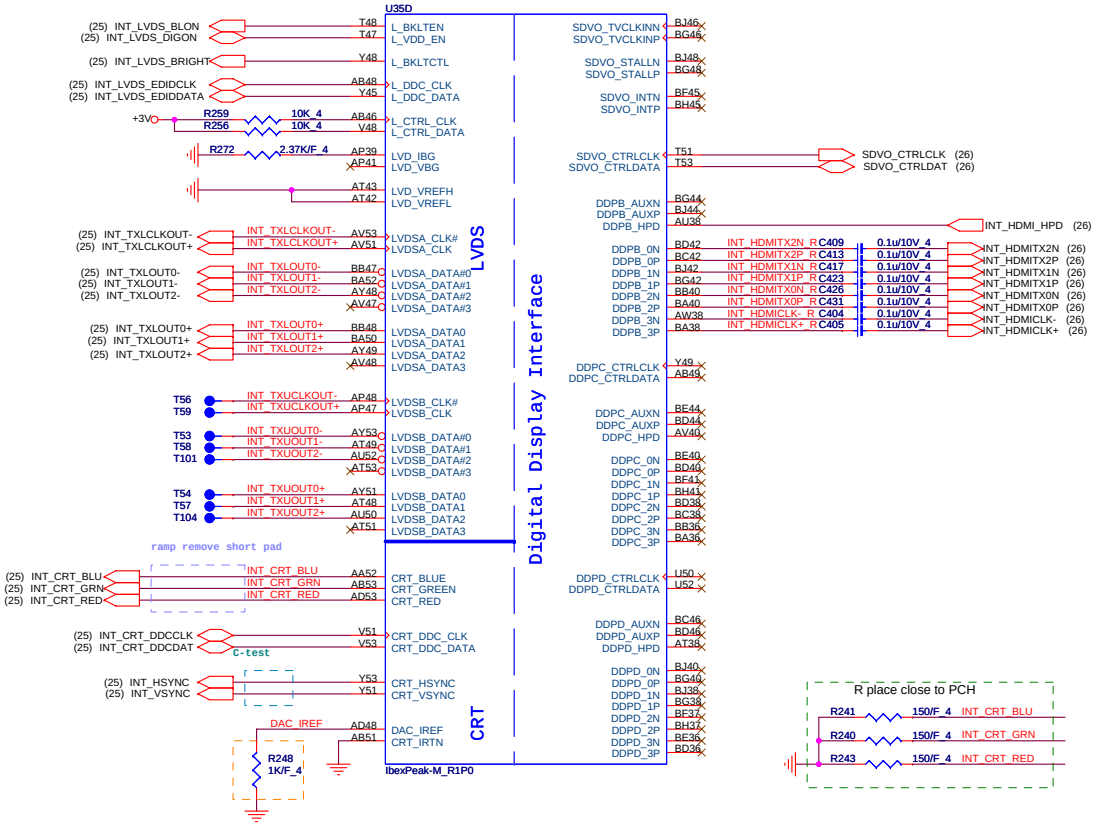
PCH1(CLG)

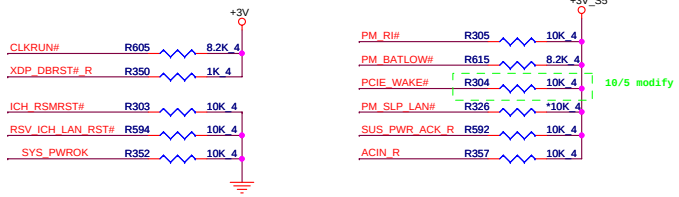
IBEX PEAK-M (DMI,FDI,GPIO)



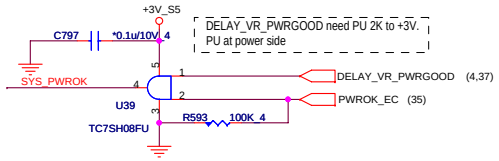
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low(CLG)



System PWR_OK(CLG)



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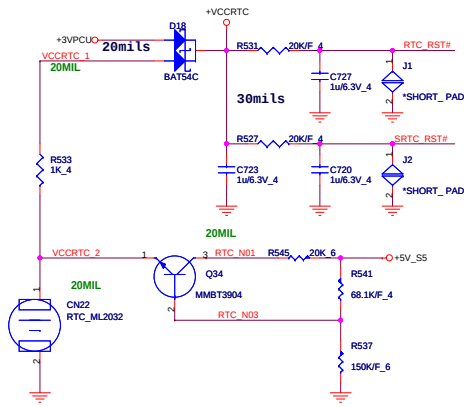
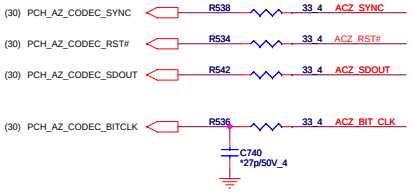
RTC Circuitry(RTC)

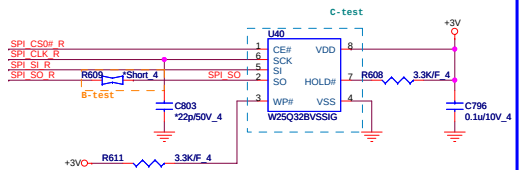


HDA Bus(CLG)



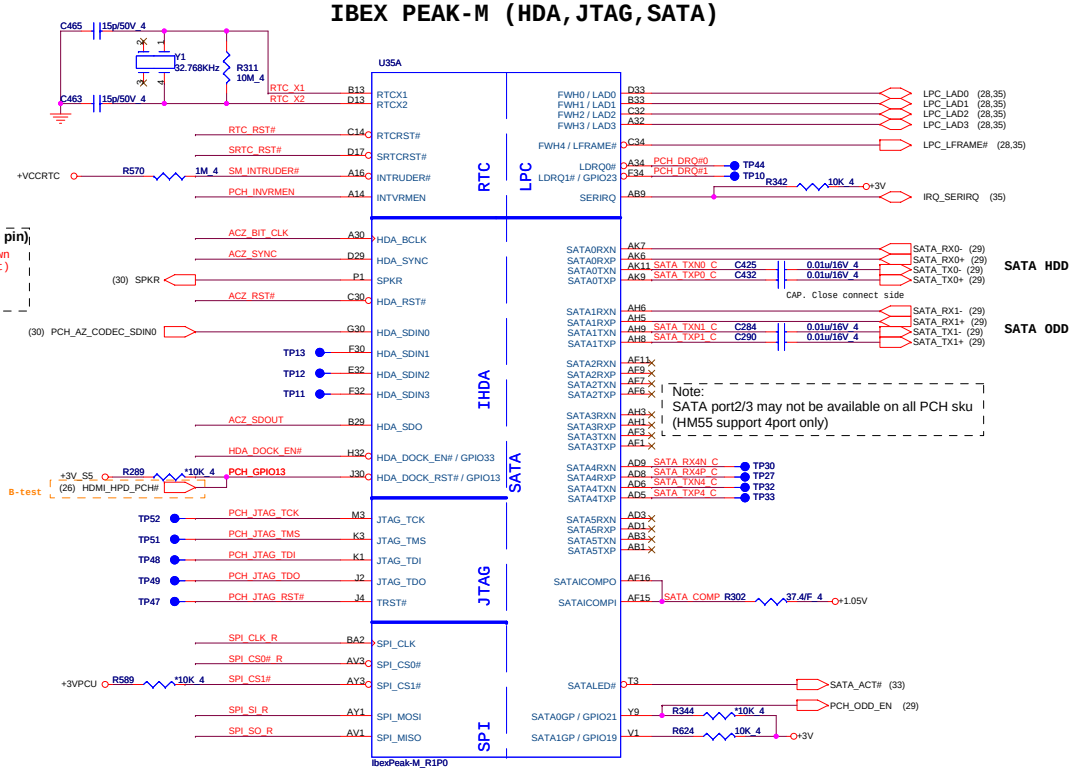
Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)



PCH2(CLG)

IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZQ1 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R601 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R517 *10K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R567 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R249 1K_4 R245 1K_4 C-test R255 *1K_4 R254 *1K_4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R590 *1K_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R591 *1K_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R277 *1K_4 R273 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R627 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R340 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	R349 1K_4 CR_WAKE# (11)

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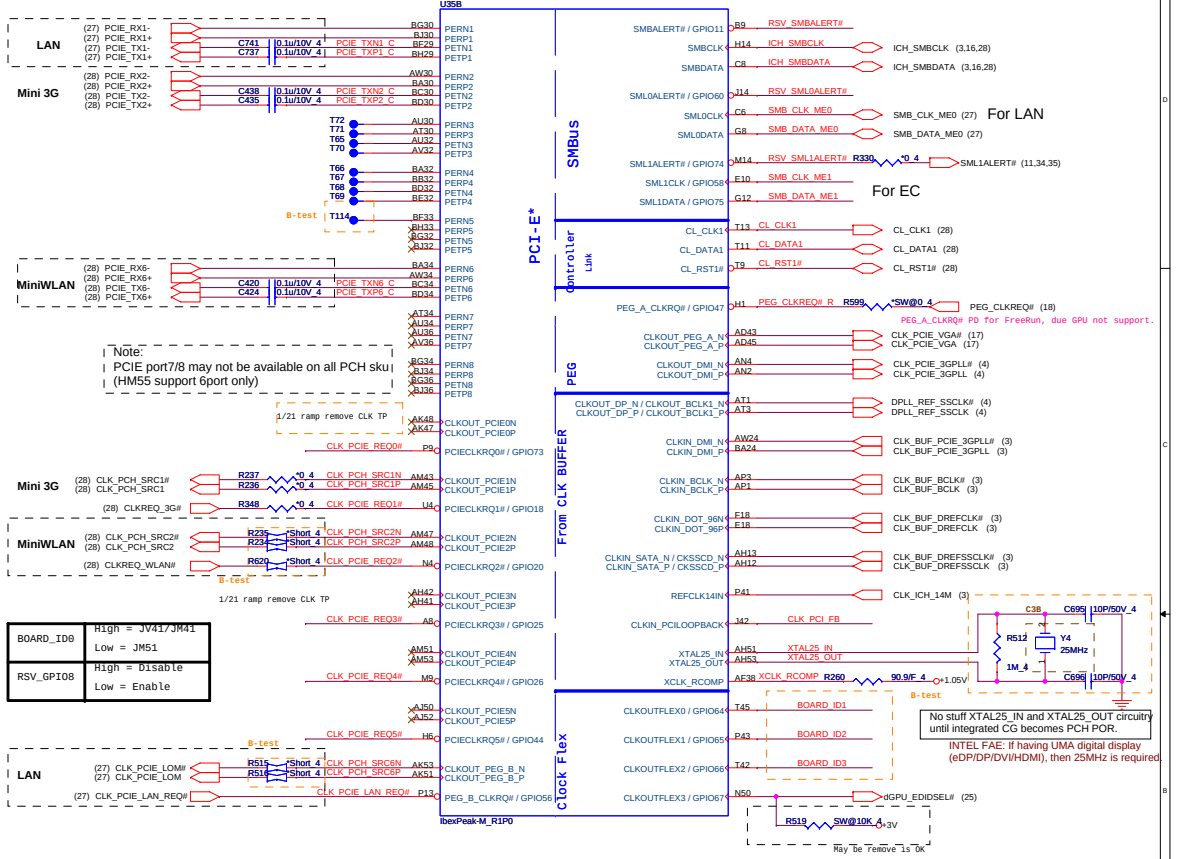
PCH3(CLG)

IBEX PEAK-M (PCI,USB,NVRAM)

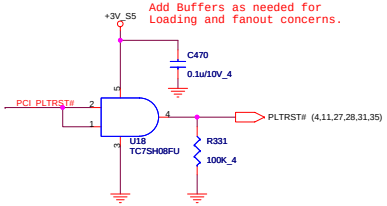
IBEX PEAK-M (PCI-E,SMBUS,CLK)

8/13 Swap Lan and WLAN/ Lan chagne to port 1

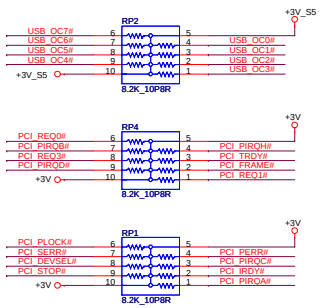


BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

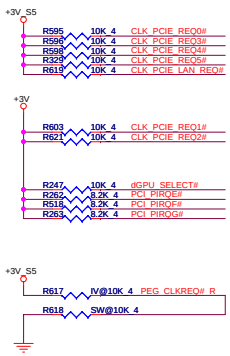
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap

GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

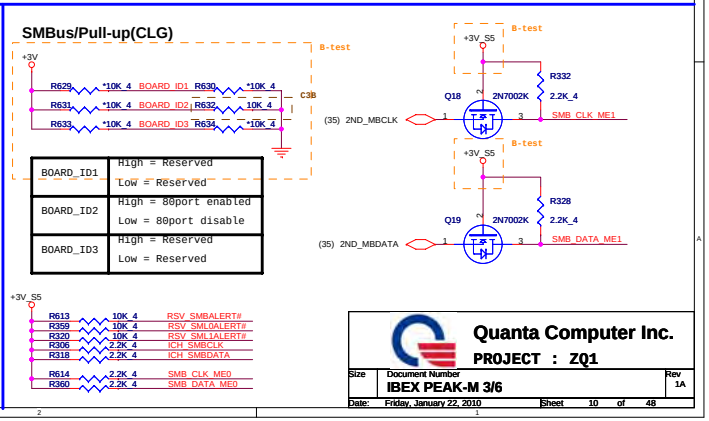
Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up(CLG)



BOARD_ID1	High = Reserved Low = Reserved
BOARD_ID2	High = 80port enabled Low = 80port disable
BOARD_ID3	High = Reserved Low = Reserved

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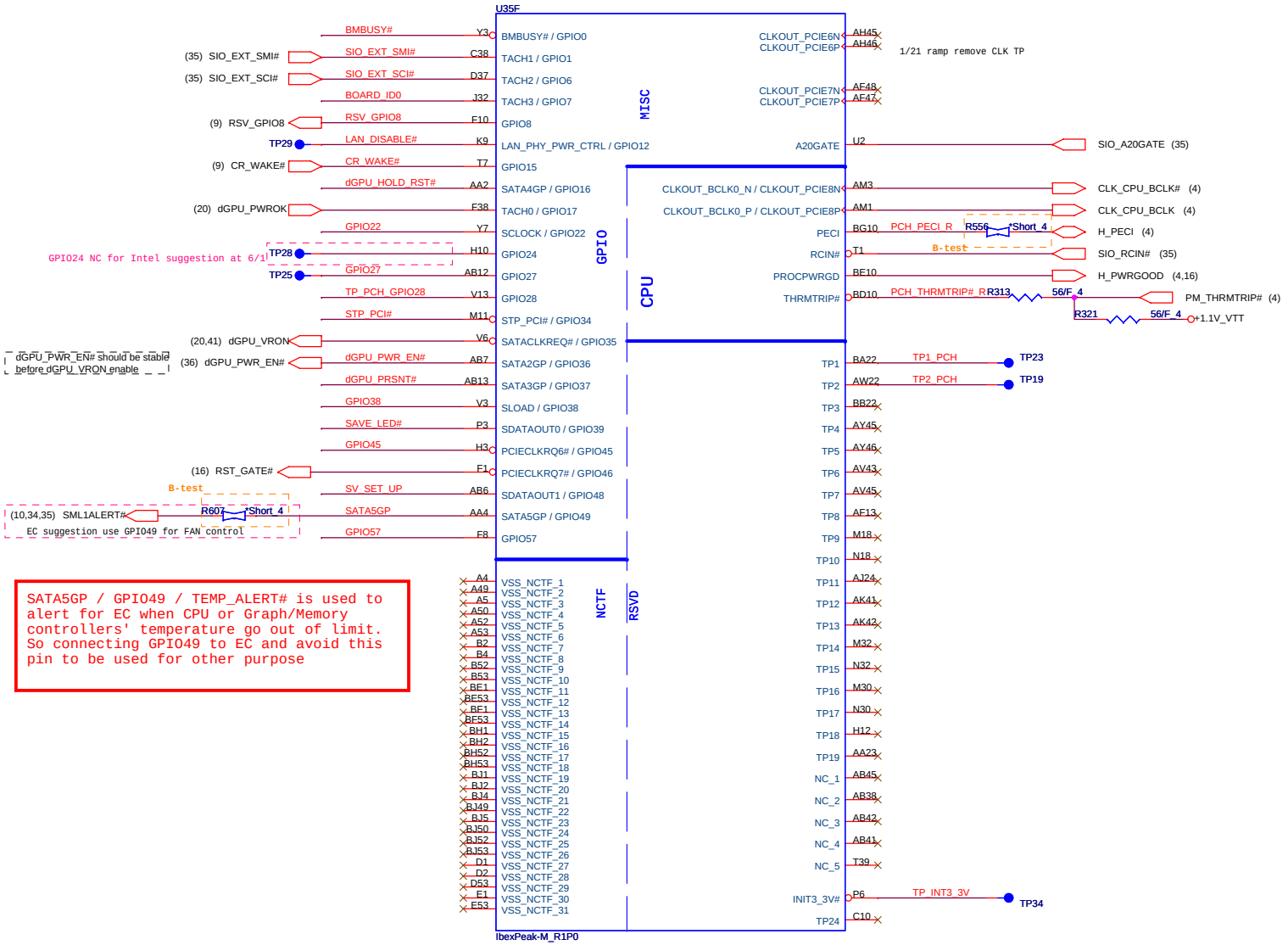
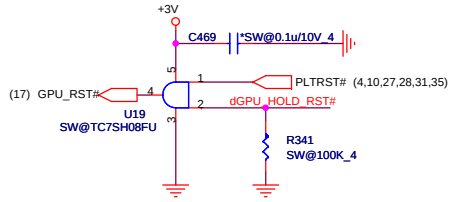
PCH4(CLG)

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

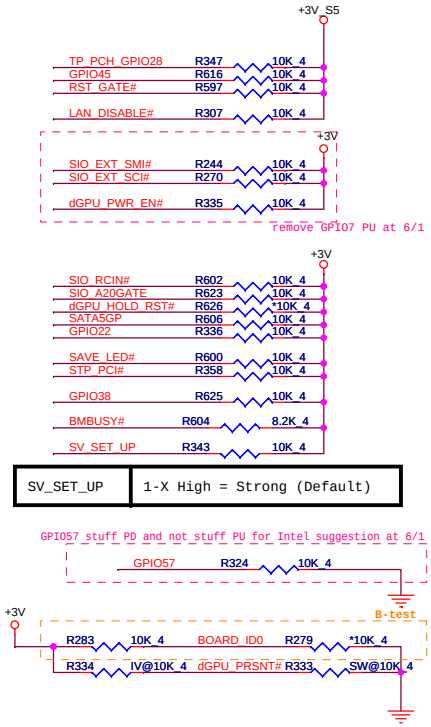


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#(CLG)



GPIO Pull-up/Pull-down(CLG)



SV_SET_UP	1-X High = Strong (Default)

BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

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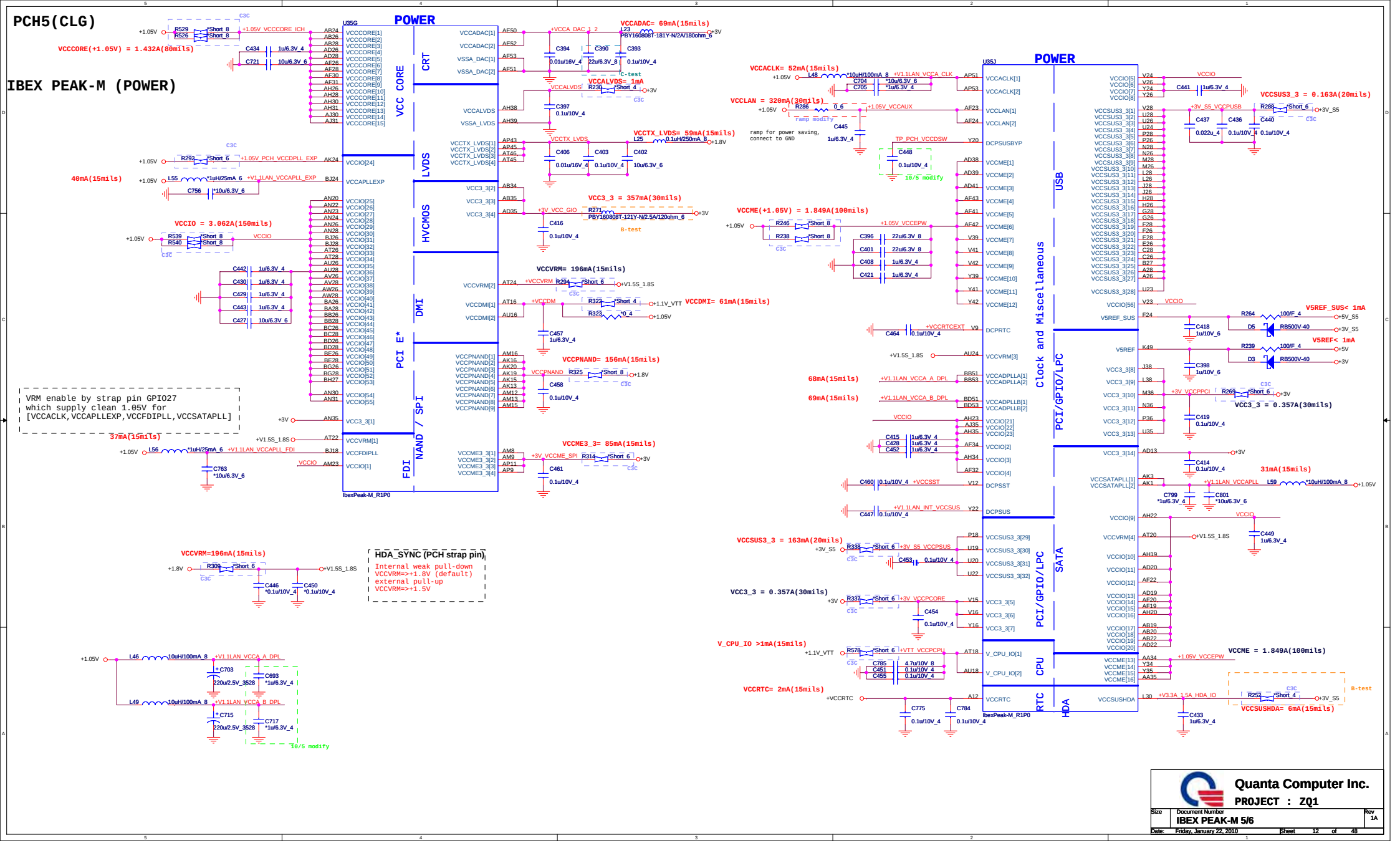
PCH5(CLG)

IBEX PEAK-M (POWER)



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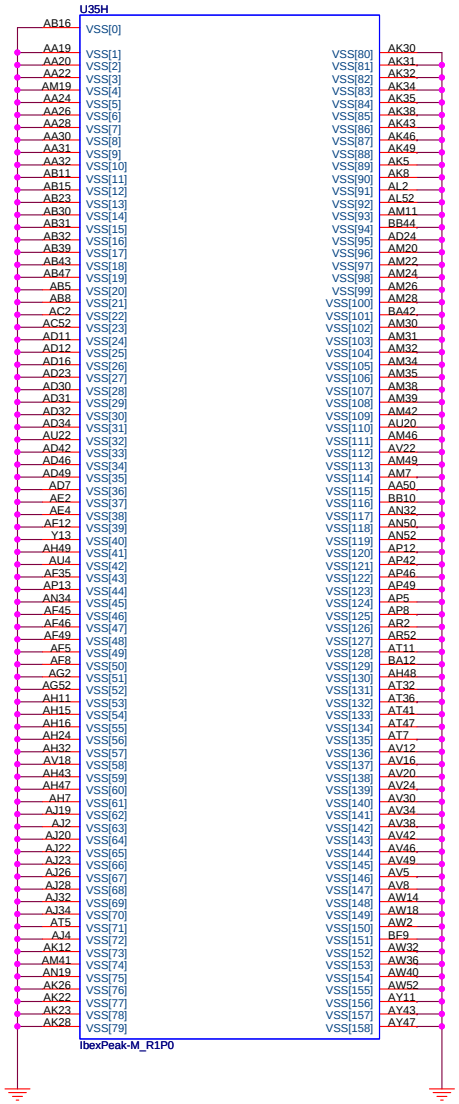
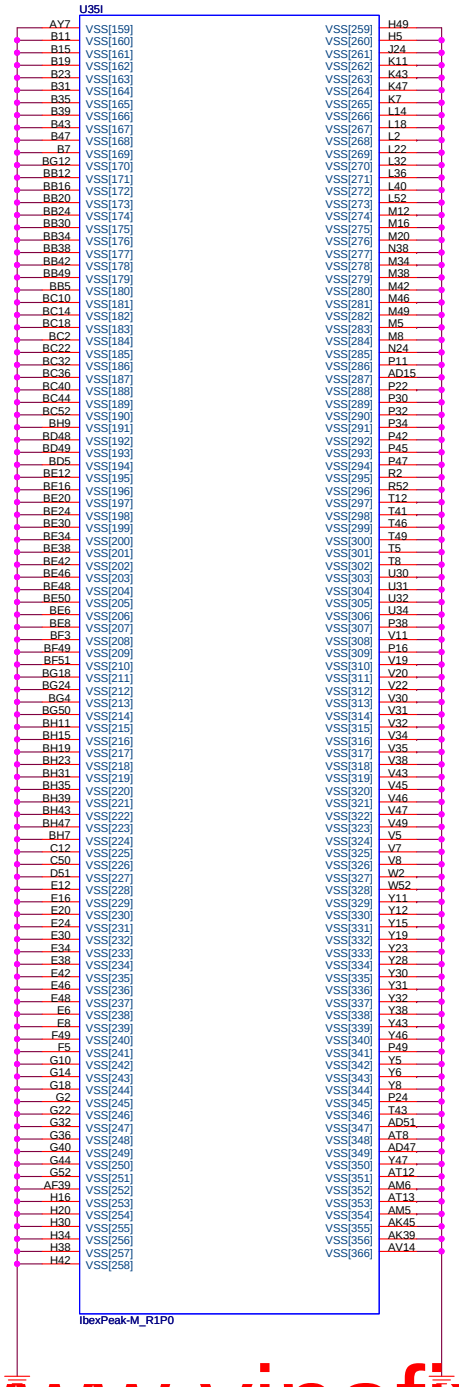
IBEX PEAK-M (GND)





Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
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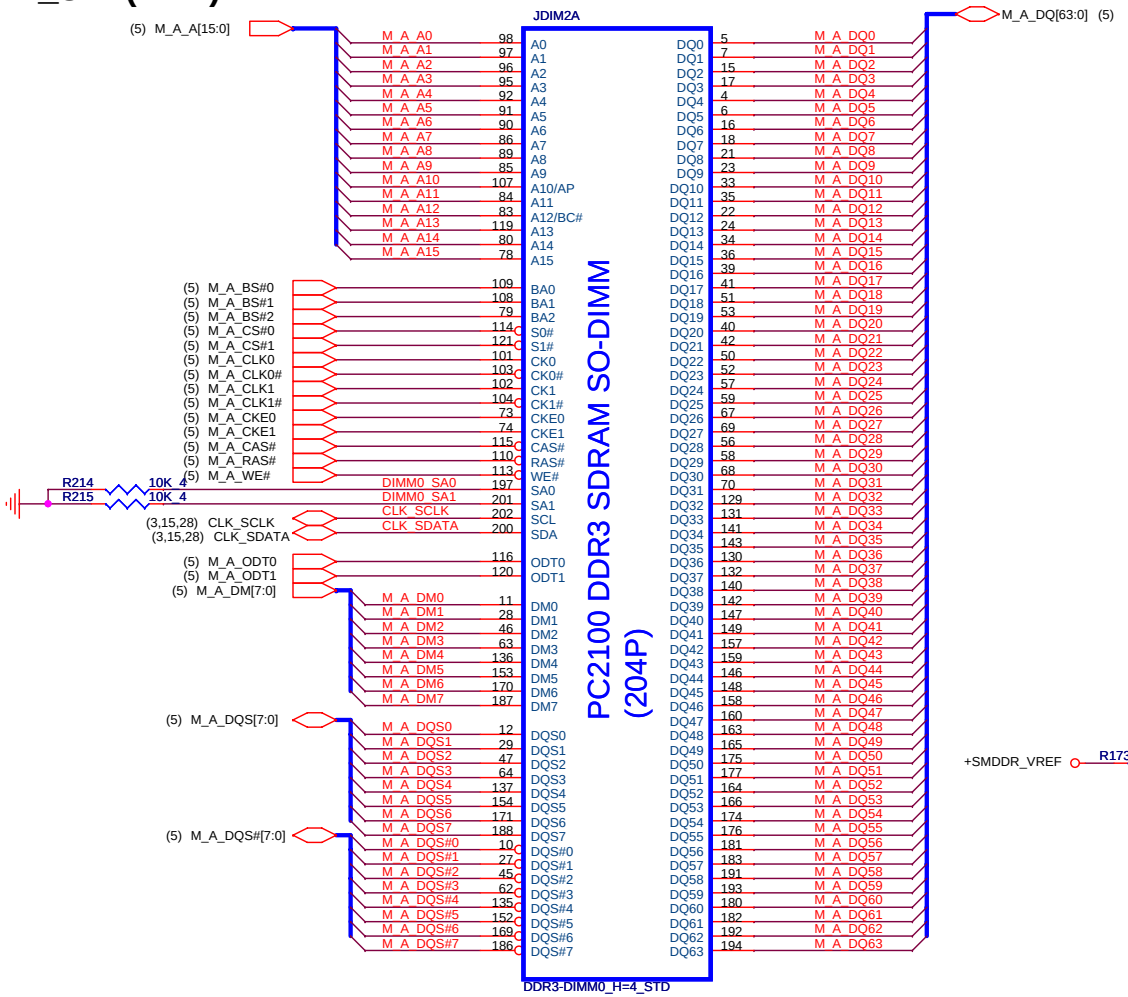
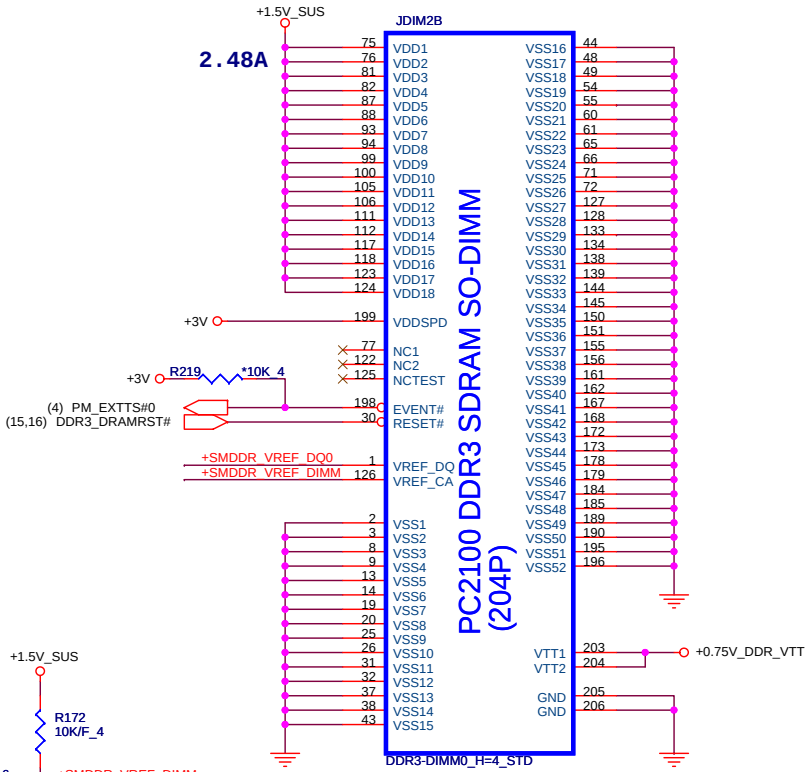
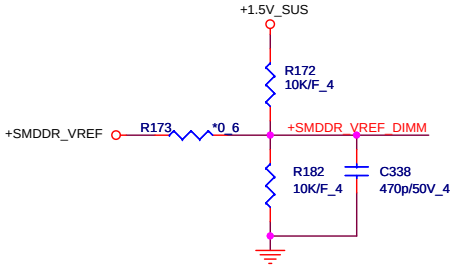
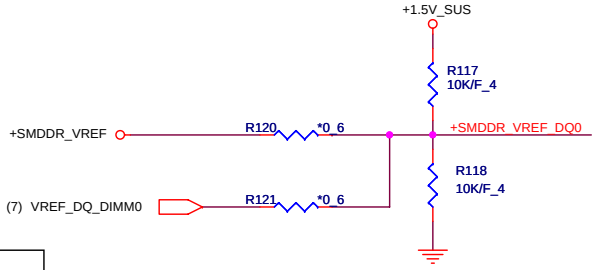
DDR_STD(DDR)

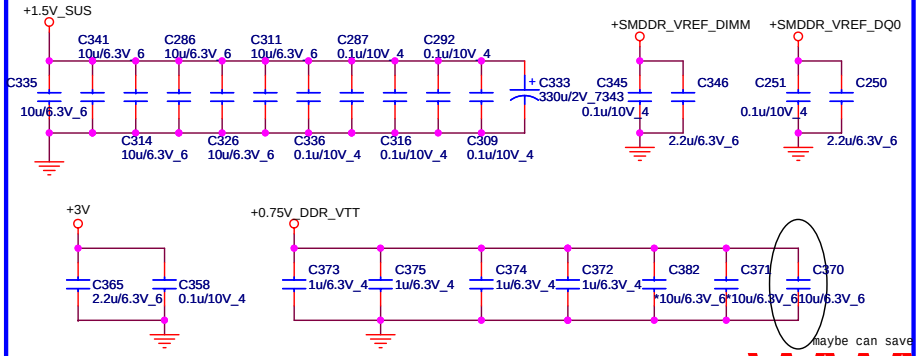








Place these Caps near So-Dimm0.



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR3-2013289-204p

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

Quanta Computer Inc.
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Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
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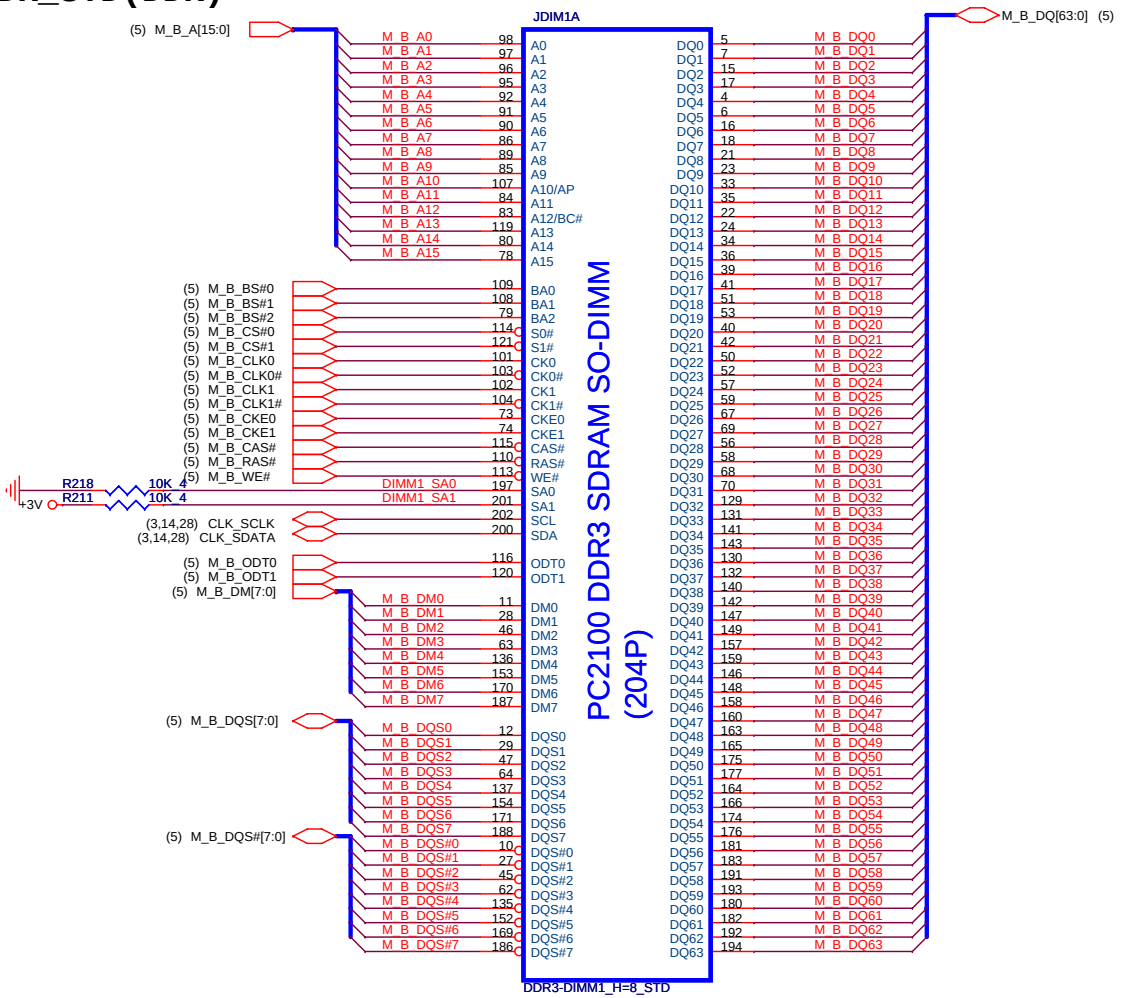
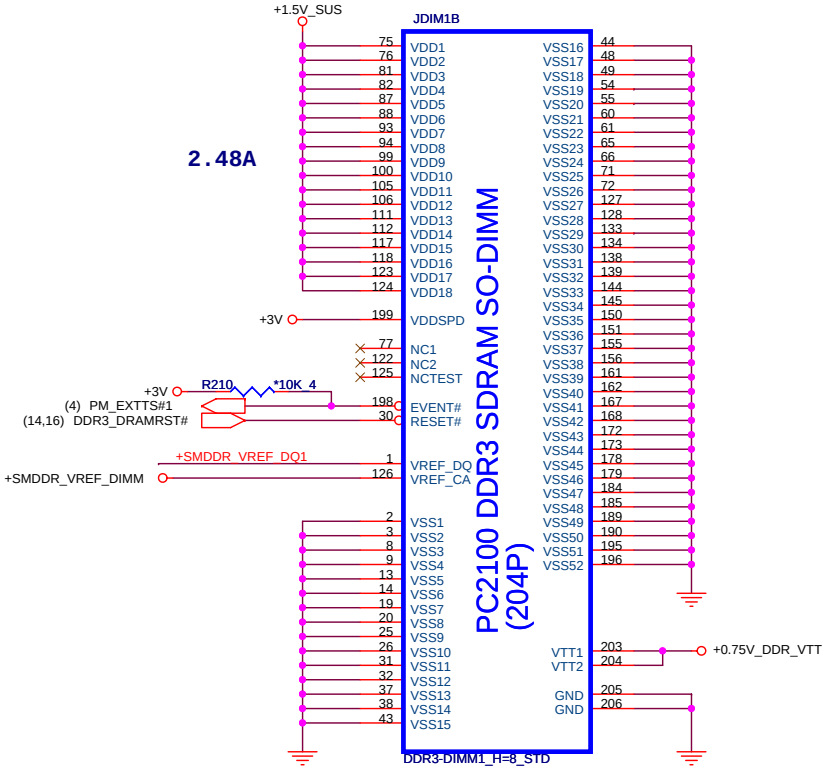
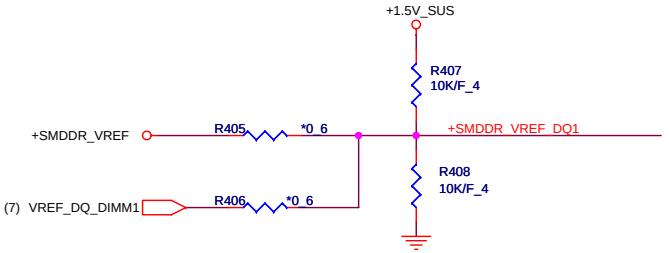
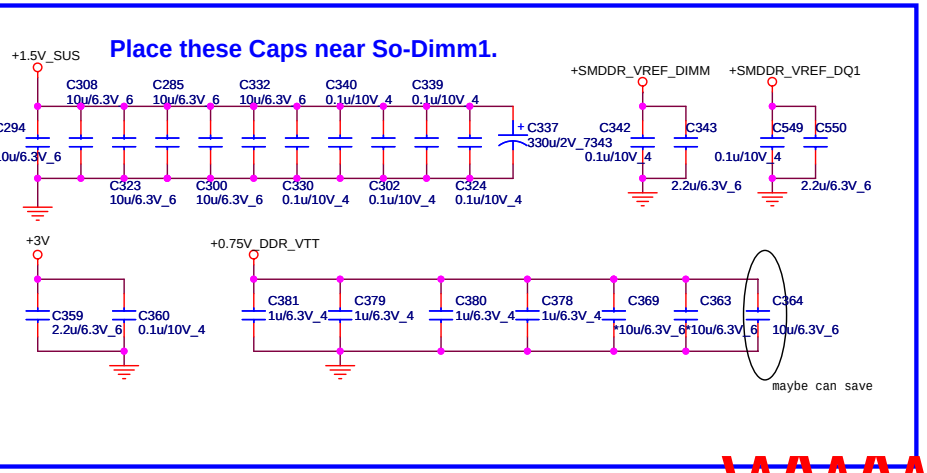
DDR_STD(DDR)









	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8Gbyte.DDR3.2013310.2.p.1		

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

Quanta Computer Inc.
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	DDRIII SO-DIMM-1	1A
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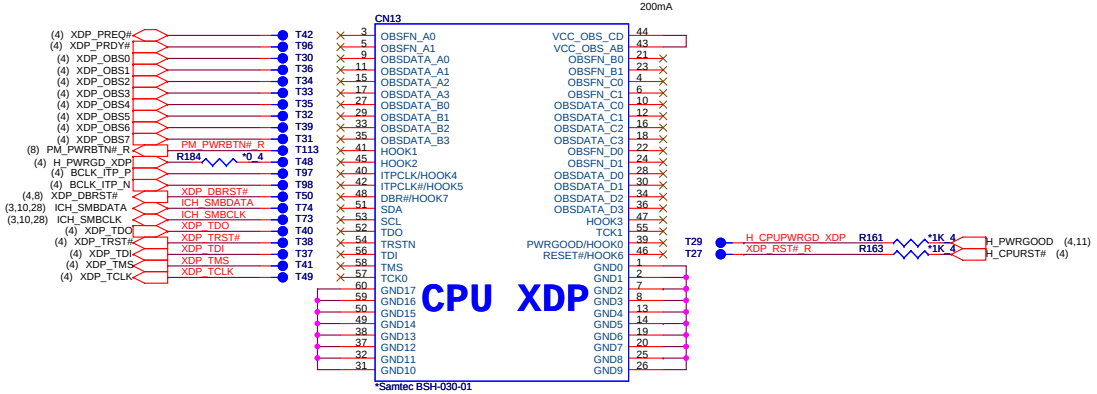
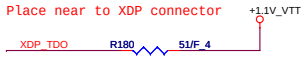
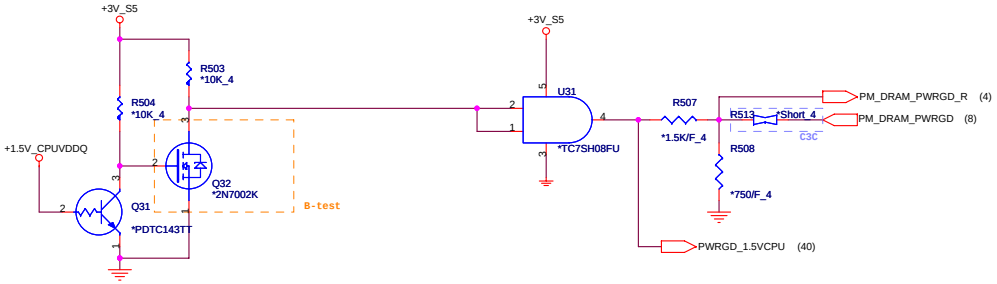
CPU XDP Connector(CPU)

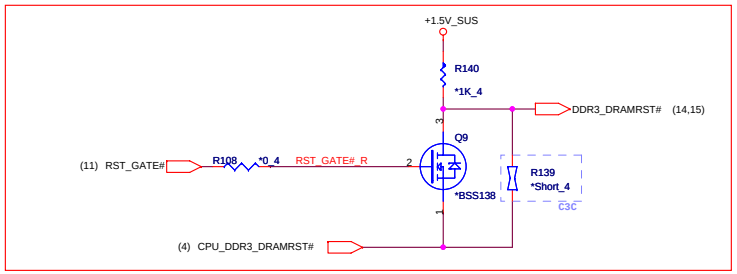


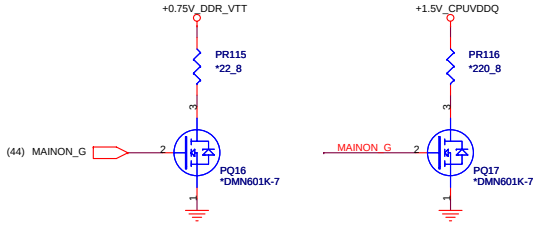
Place near to XDP connector

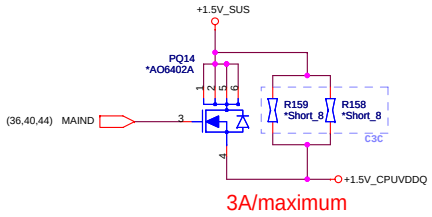


S3 leakage solution(CLG)









Quanta Computer Inc.
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	XDP	1A
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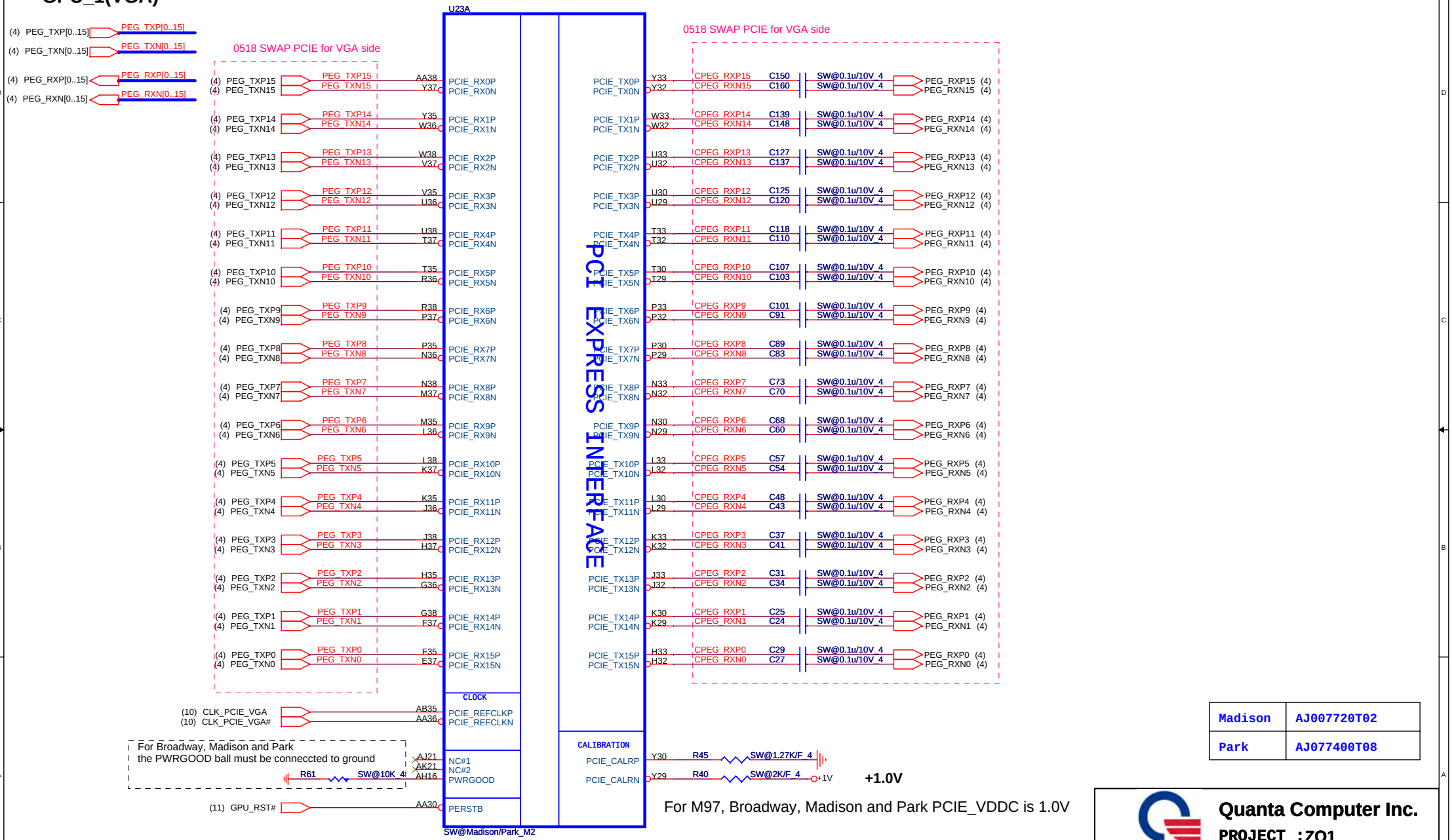
GPU_1(VGA)



Madison	AJ007720T02
Park	AJ077400T08

Quanta Computer Inc.
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Size	Document Number	Rev
	Madison/Park M2-PCIE I/F	1A

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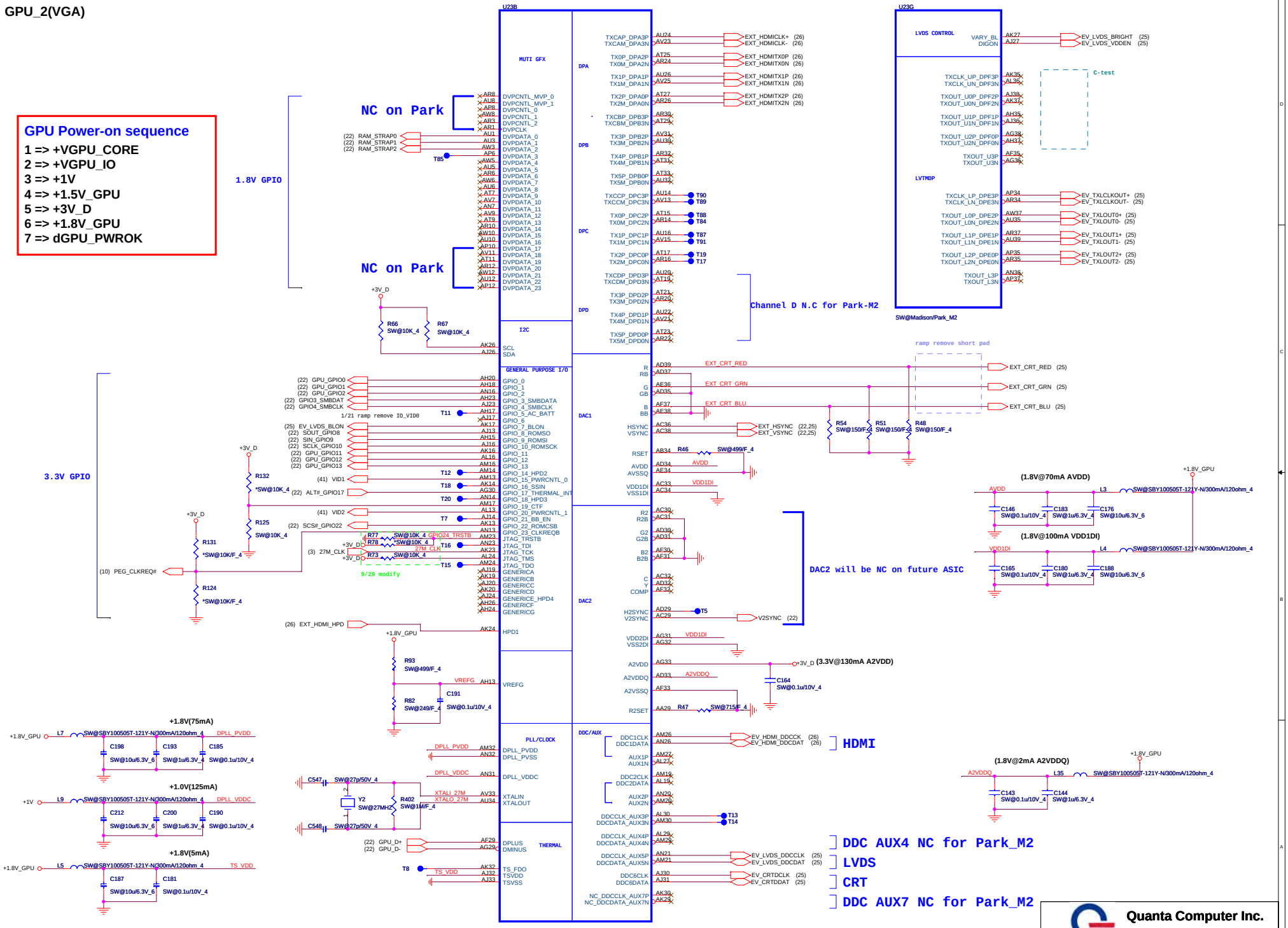
GPU_2(VGA)

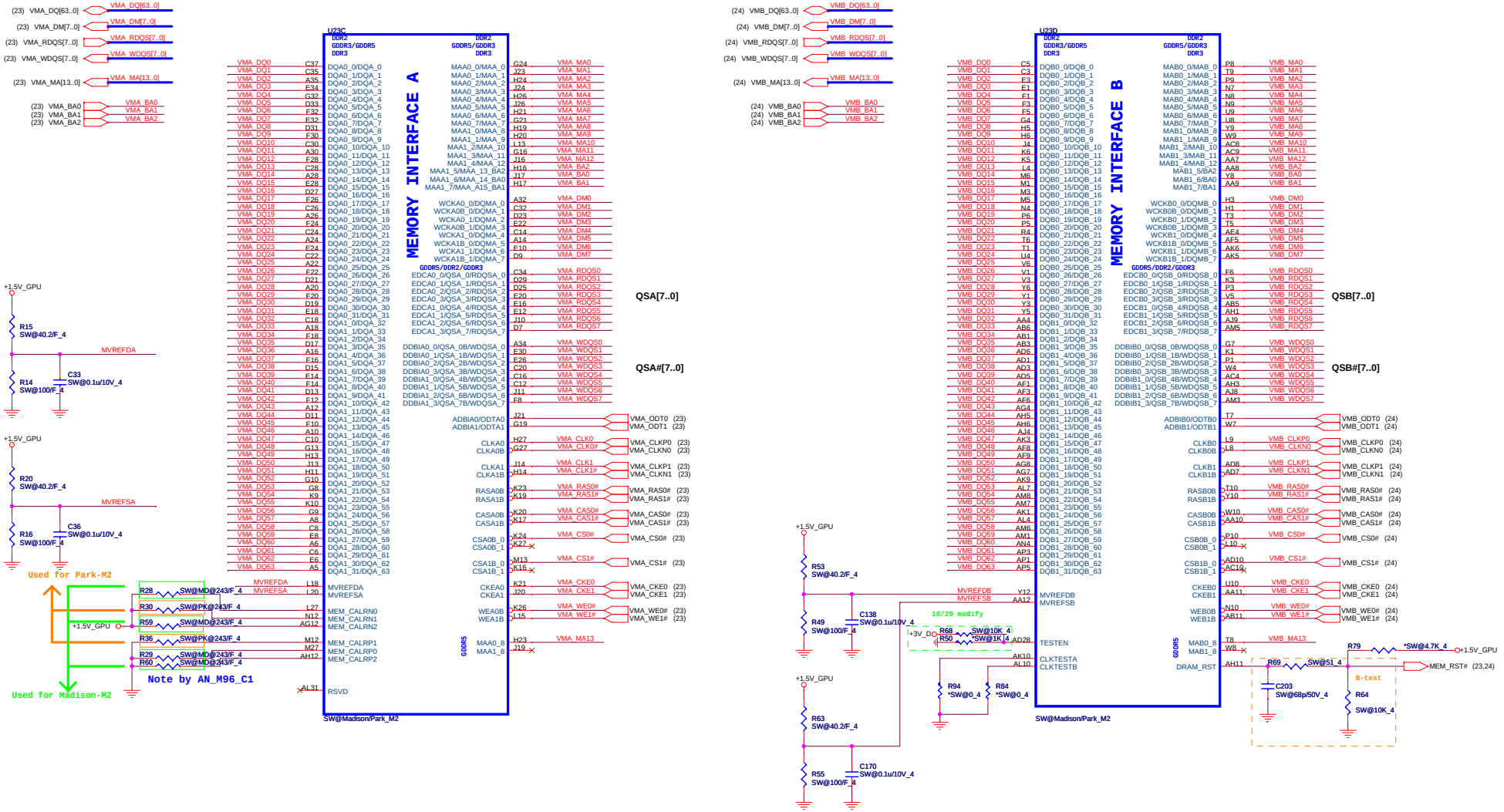
GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK



GPU_3(VGA)

Park M2-channel B used(S3 package use Channel A)



Quanta Computer Inc.		
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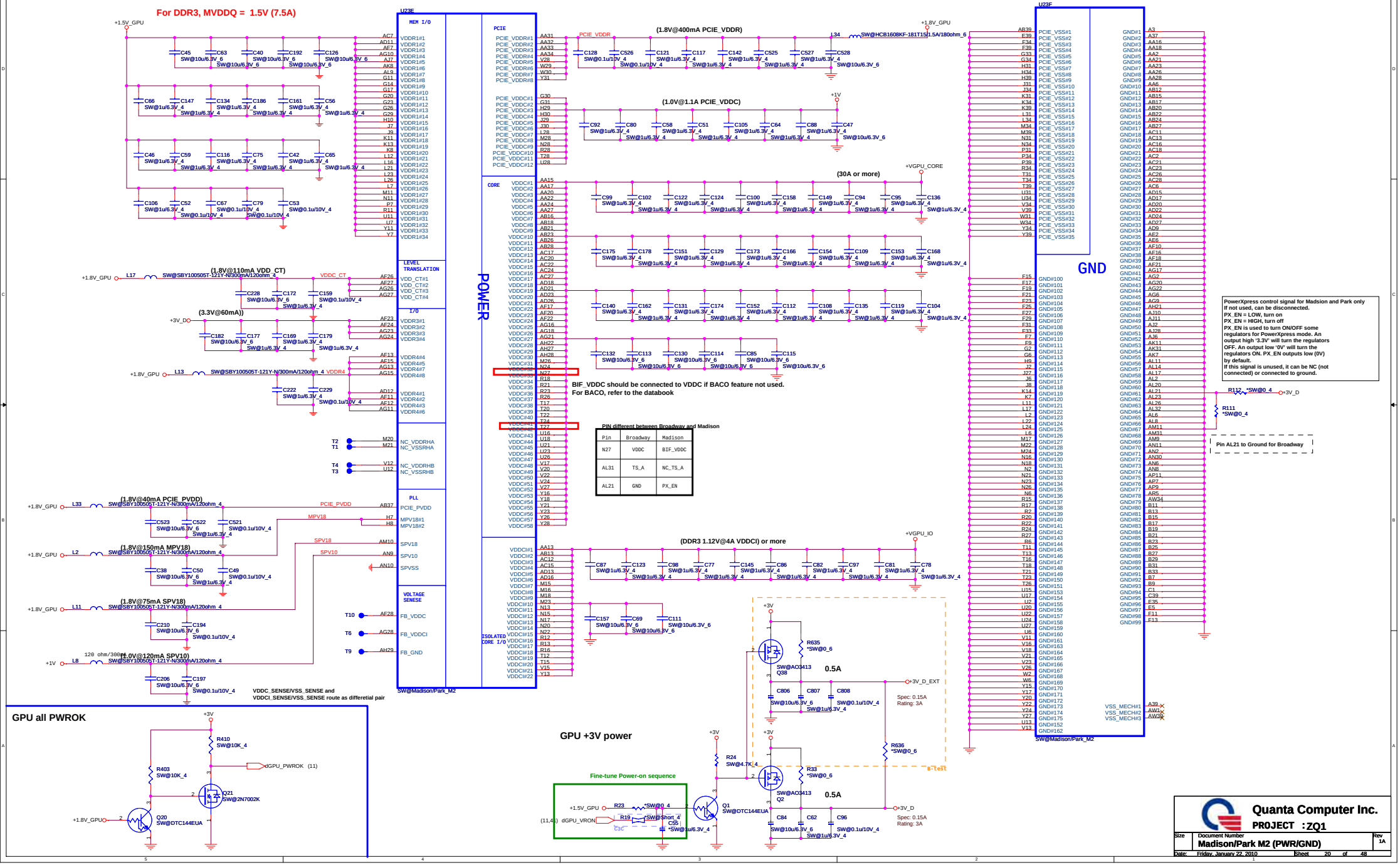
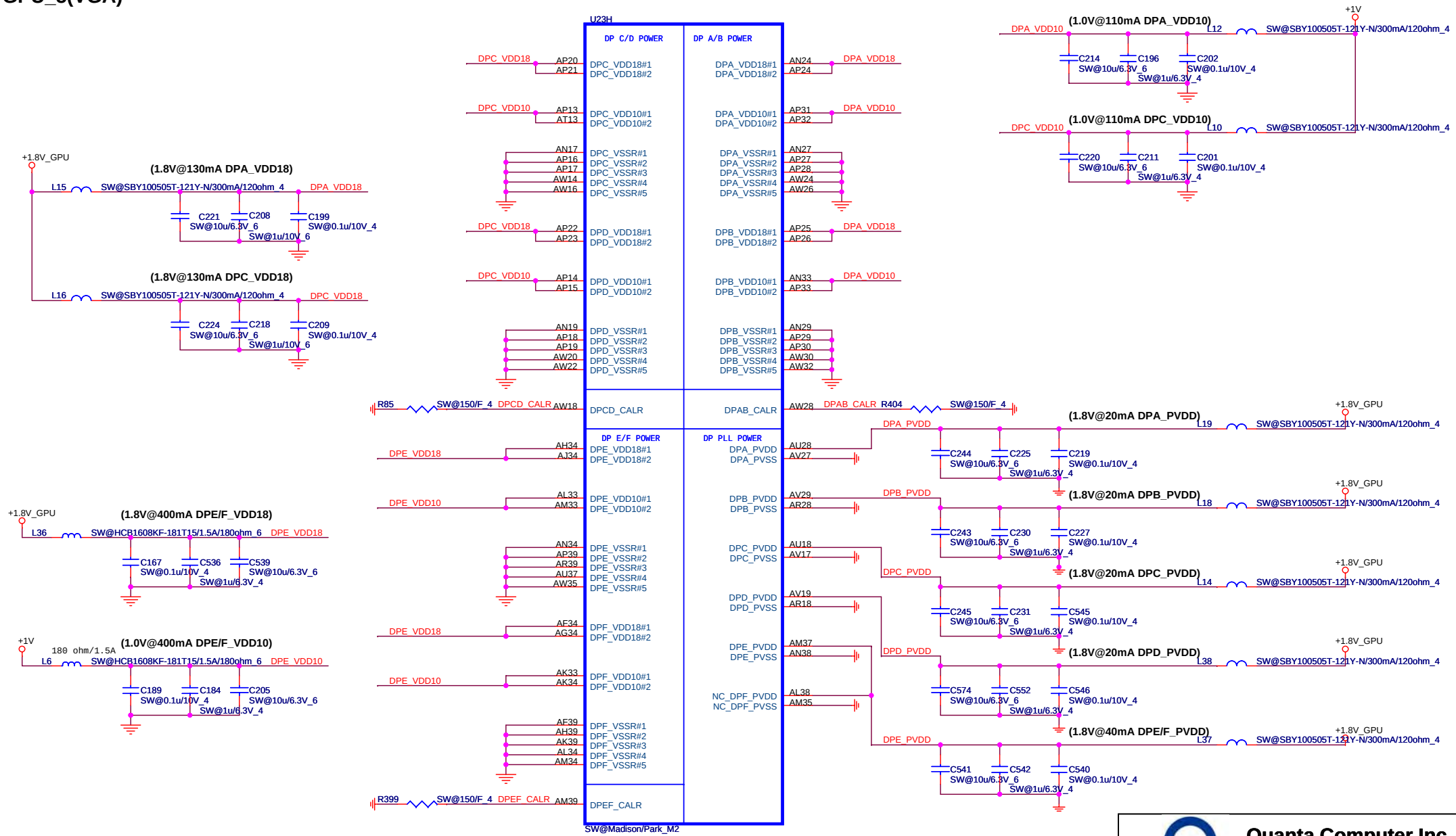
GPU_4(VGA)



GPU_5(VGA)



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PROJECT : ZQ1		
Size	Document Number: Madison/Park M2 (DP_PWR/GND)	Rev 1A
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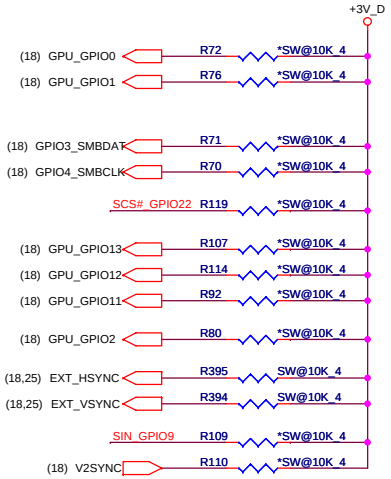
PIN STRAPS(VGA)



ROM Table		
Manufacturer	Part Number	Code
Numonyx ST Microelectronics	M25P05A	100
	M25P10A	101
	M25P20	101
	M25P40	101
	M25P80	101
Chingis PMC	Pm25LV512A	100
	Pm25LV010A	101

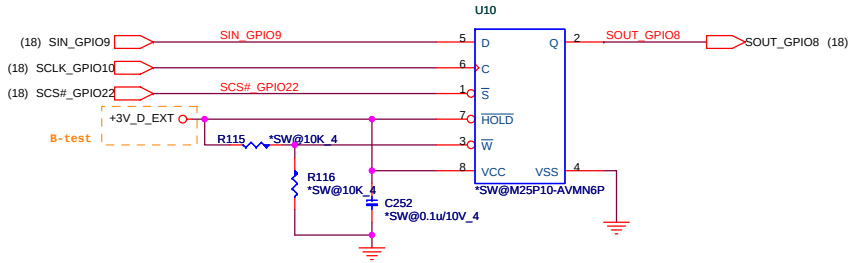
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	1	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	101	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

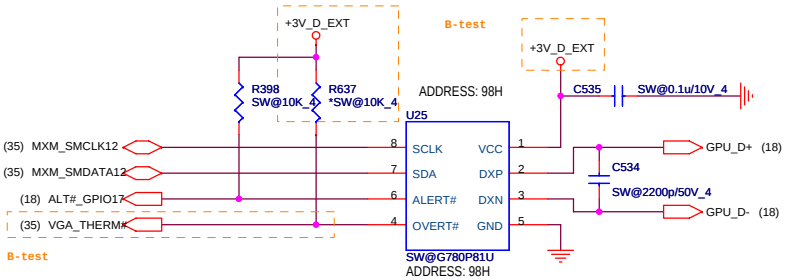
EEPROM(VGA)



Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

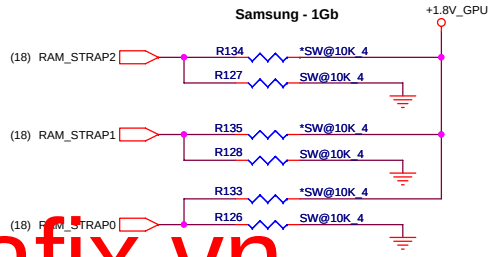
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory Aperture size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			512Mb	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1Gb	1	0	0
			2Gb	1	0	1
Samsung			512Mb			
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1Gb	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	1Gb	0	1	0

C-test



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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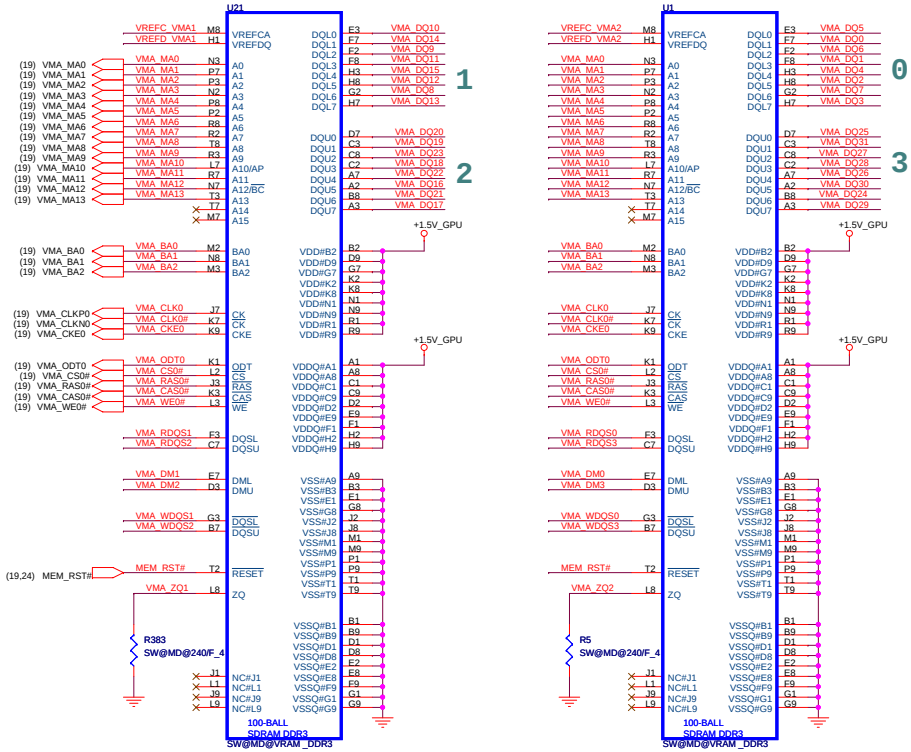
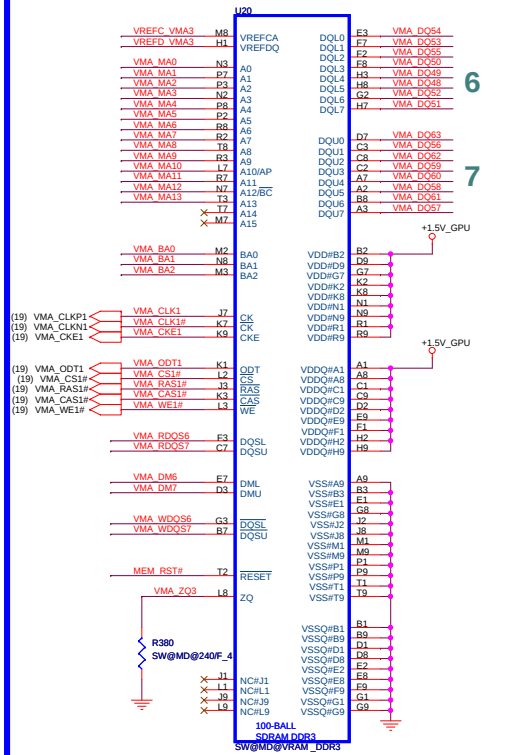
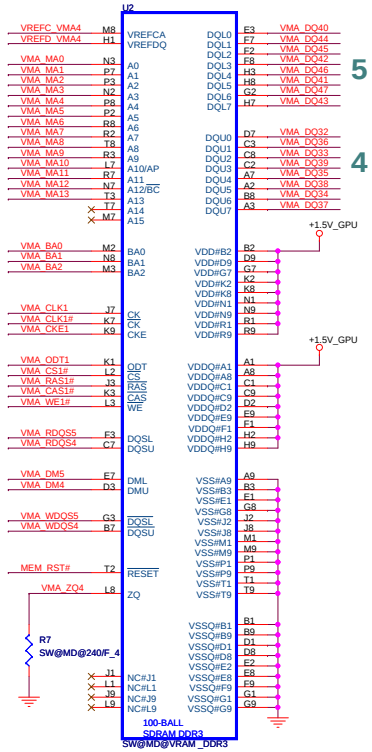
CHANNEL A: 512MB DDR3 (16*64M*4pcs)

Park, M92M Use Channel B Memory Interface Only

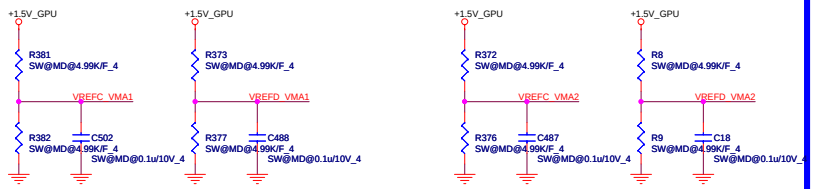
(19) VMA_DQ[63..0] — VMA_DQ[63..0]
(19) VMA_DM[7..0] — VMA_DM[7..0]
(19) VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
(19) VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]



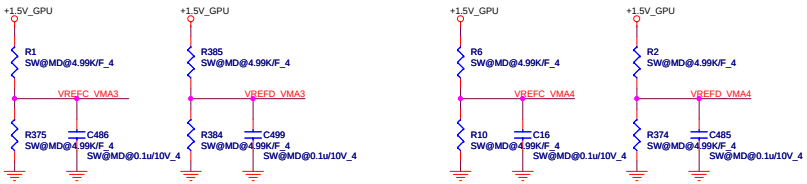




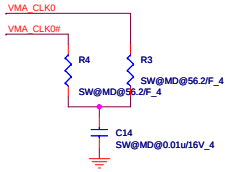
Group-A0 VREF



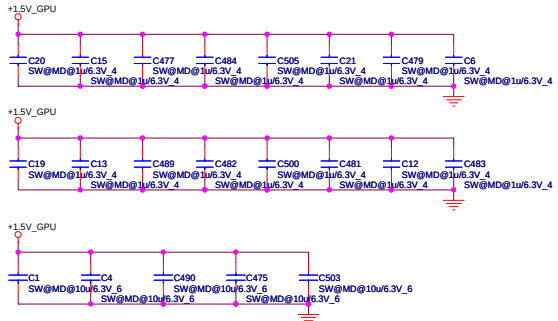
Group-A1 VREF



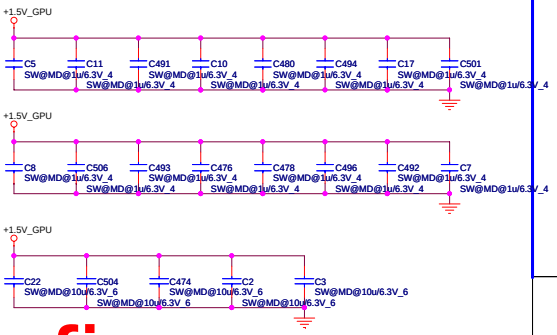
MEM_A0 CLK



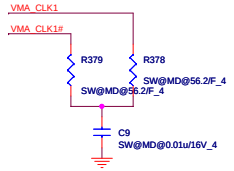
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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MEMORY 1 channel A | 1A
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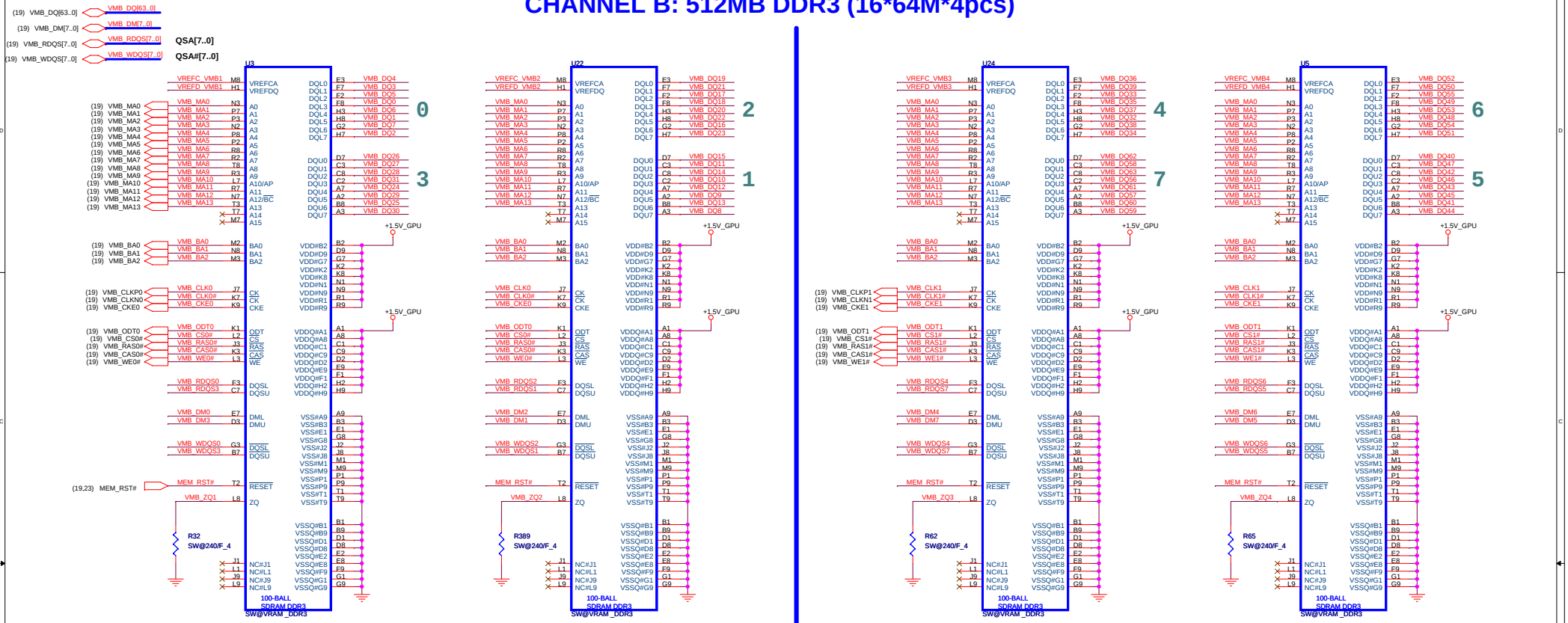
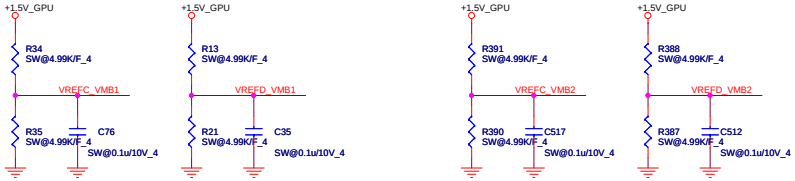
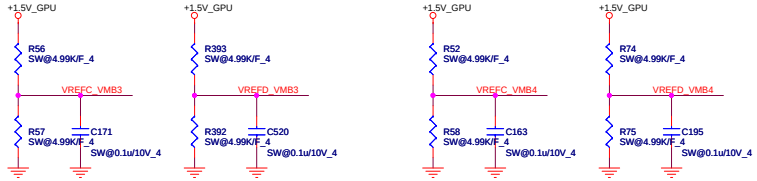
CHANNEL B: 512MB DDR3 (16*64M*4pcs)



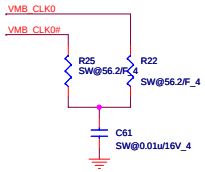
Group-B0 VREF



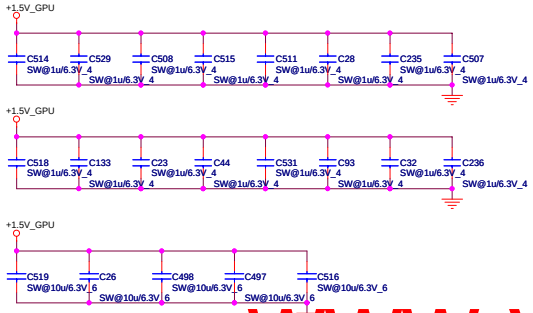
Group-B1 VREF



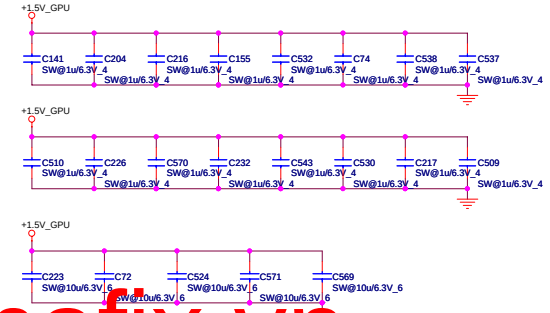
MEM_B0 CLK



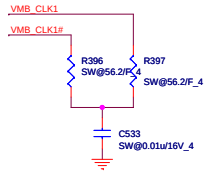
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



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	MEMORY 2 channel B	1A
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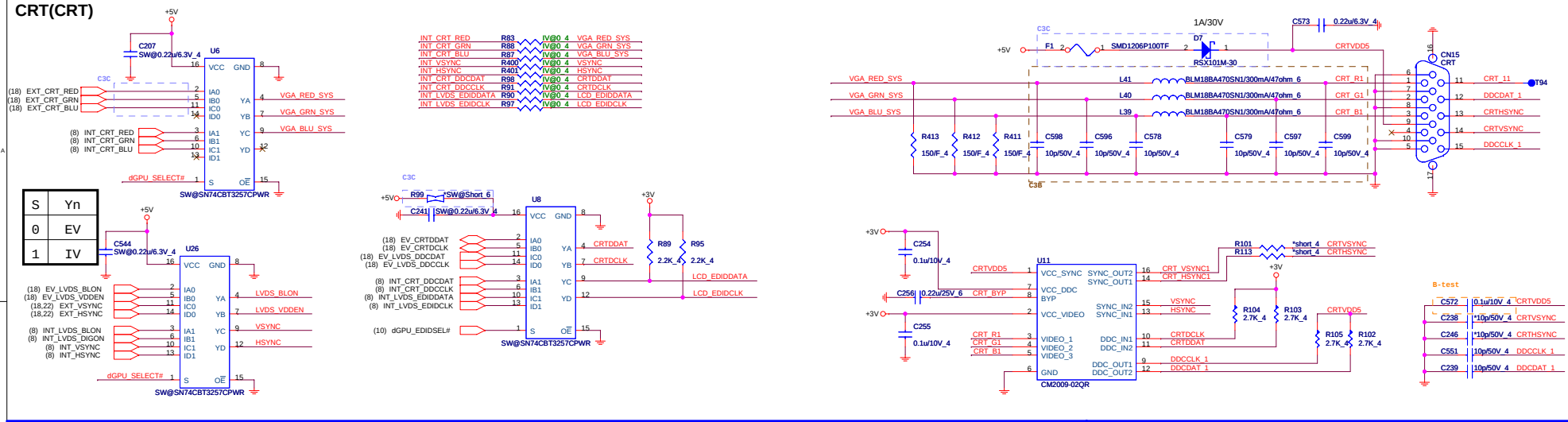
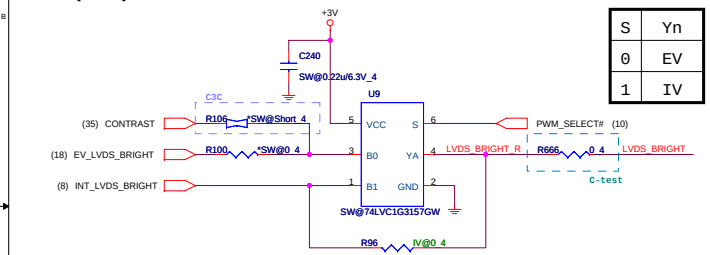
CRT(CRT)

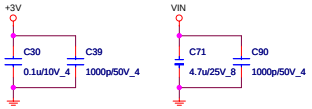


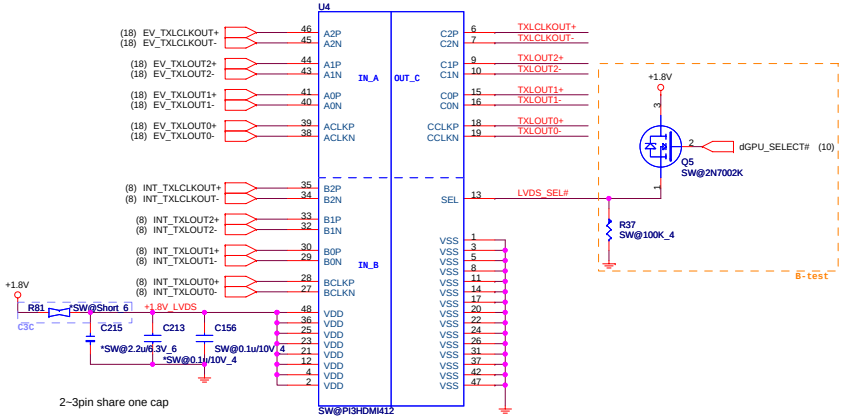
S	Yn
0	EV
1	IV

LVDS(LDS)

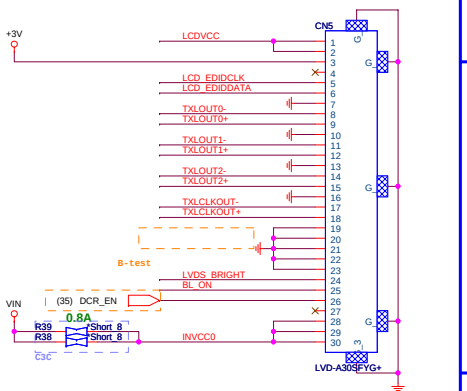


S	Yn
0	EV
1	IV

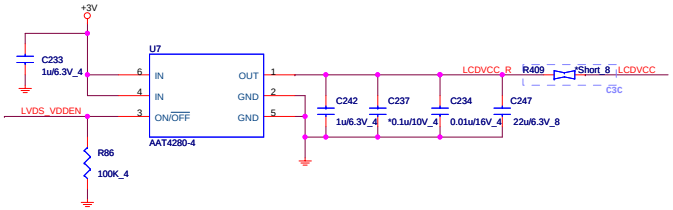




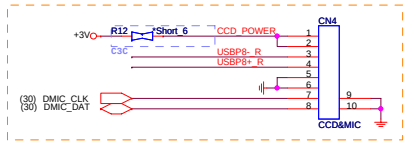
2~3pin share one cap



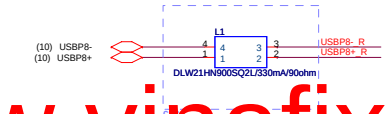
LCD Power(LDS)



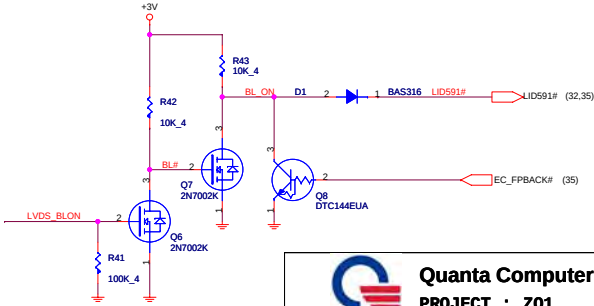
CCD&DMIC Conn.(CCD)



CAMERA Module(CCD)

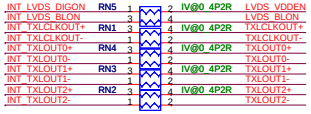


Backlight Control(LDS)



TI	AL3DV421V00
Pericom	AL000412W00

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

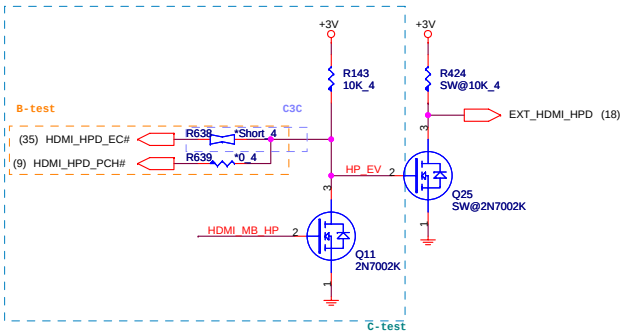


Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	CRT/LVDS	1A

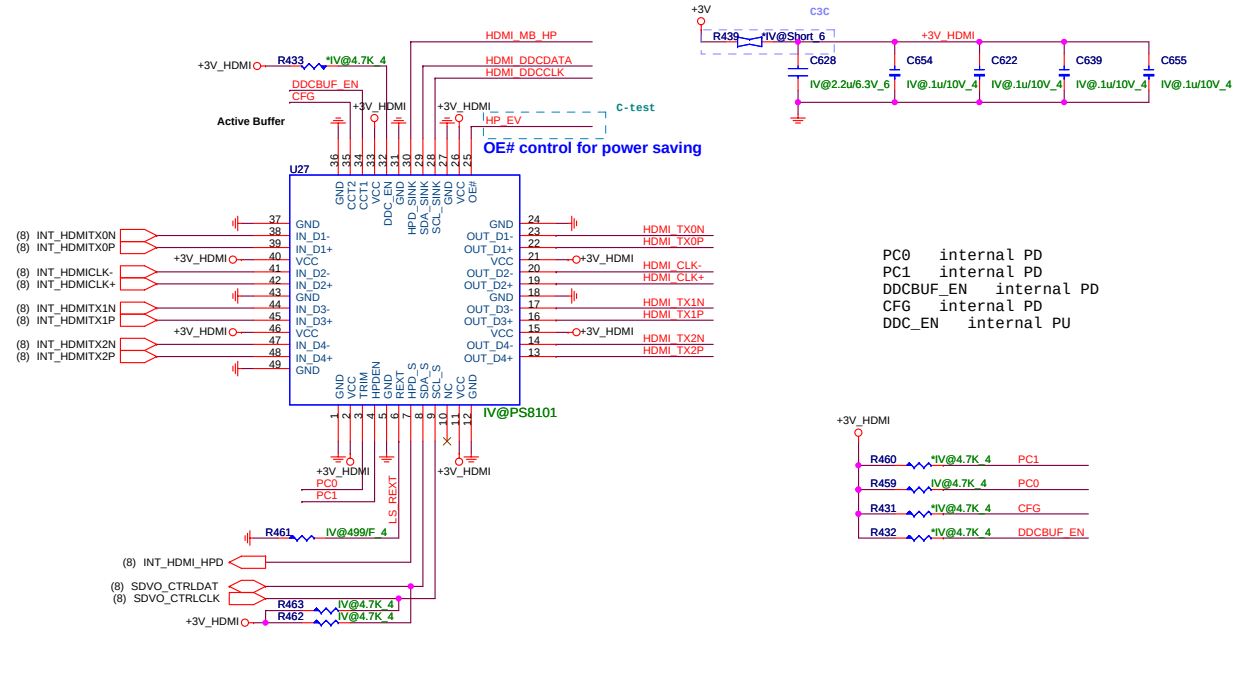
Date: Friday, January 22, 2010 Sheet 25 of 48

HDMI HPD(HDM)



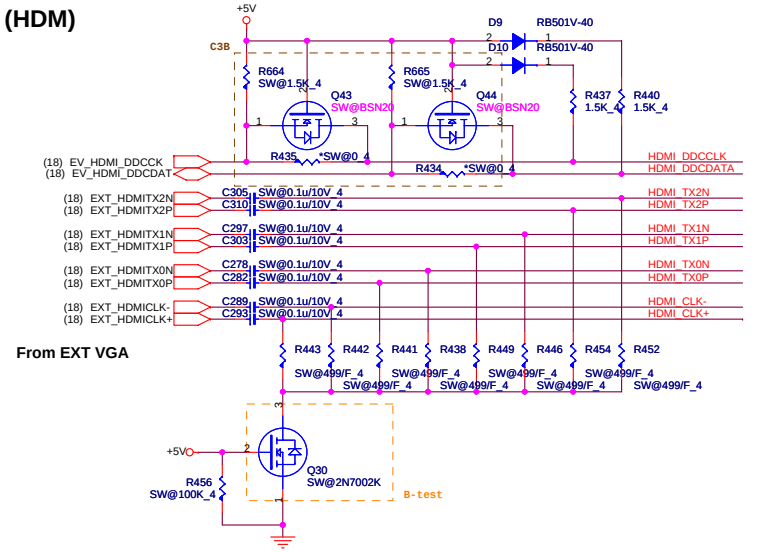
HDMI LEVEL SHIFTER(HDM)

PS8101 :: AL008101000

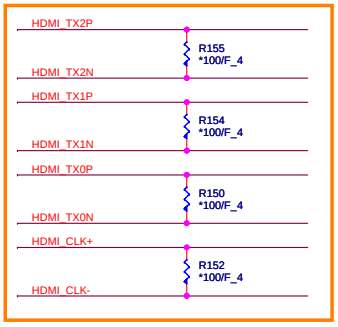


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

(HDM)

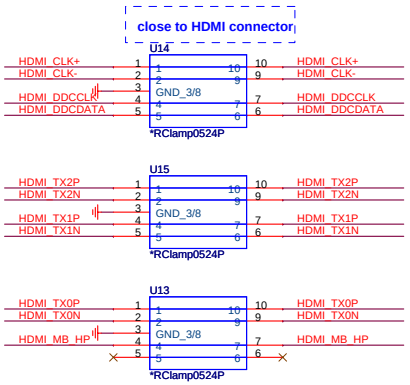


EMI reserve for HDMI(HDM)

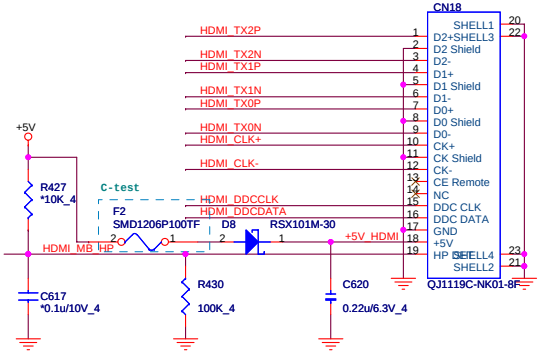


Close connector

ESD Protect

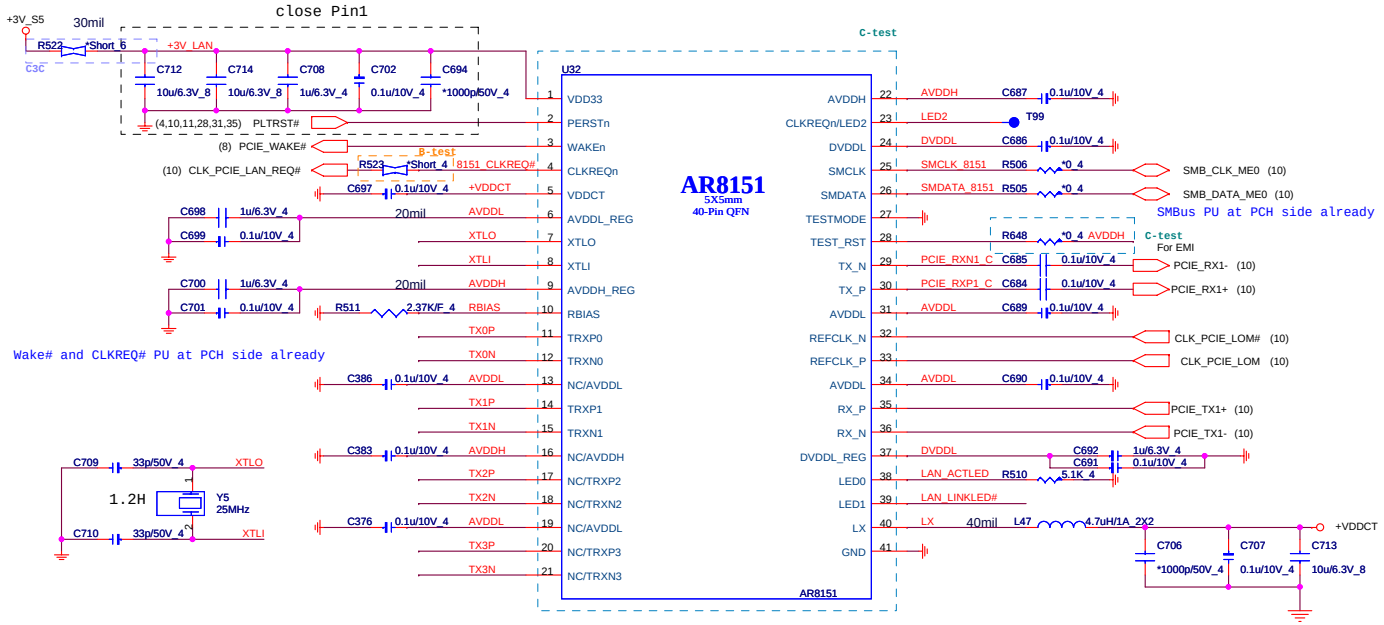


HDMI connector(HDM)

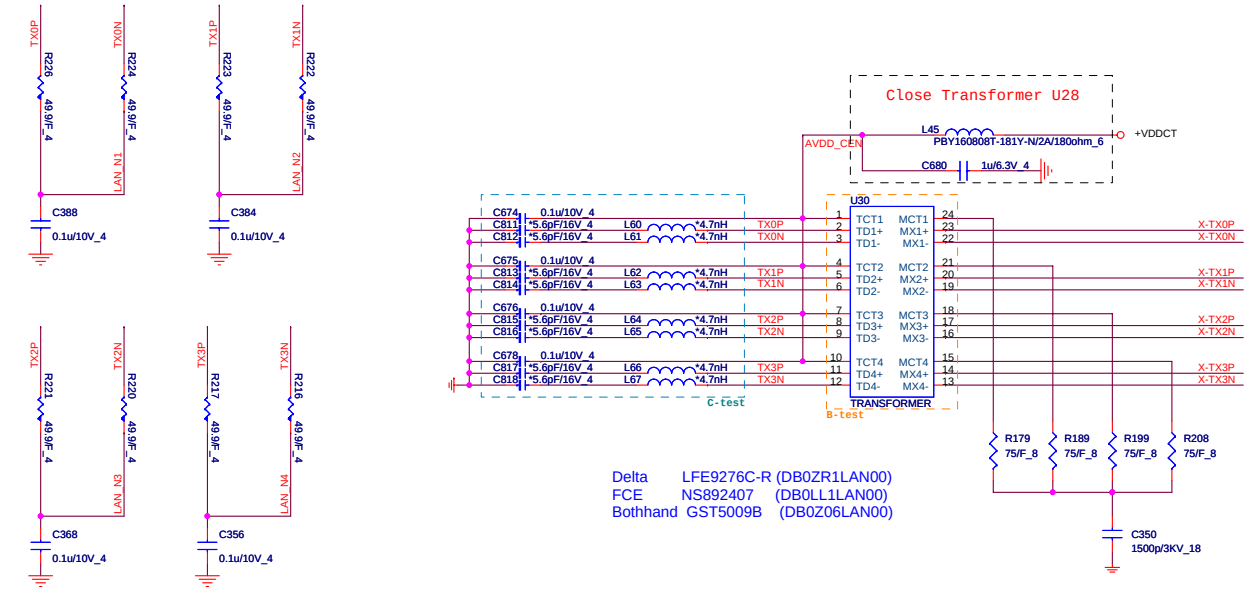


Quanta Computer Inc. PROJECT : ZQ1		
Size	Document Number: HDMI	Rev: 1A
Date: Friday, January 22, 2010	Sheet 26 of 48	

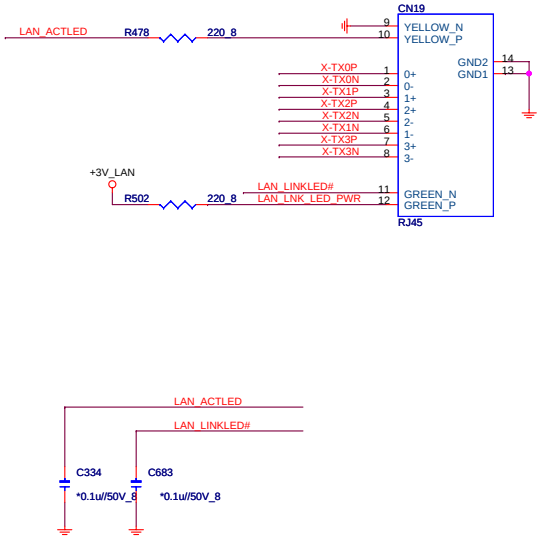
Giga-LAN AR8151(LAN)



TRANSFORMER(LAN)



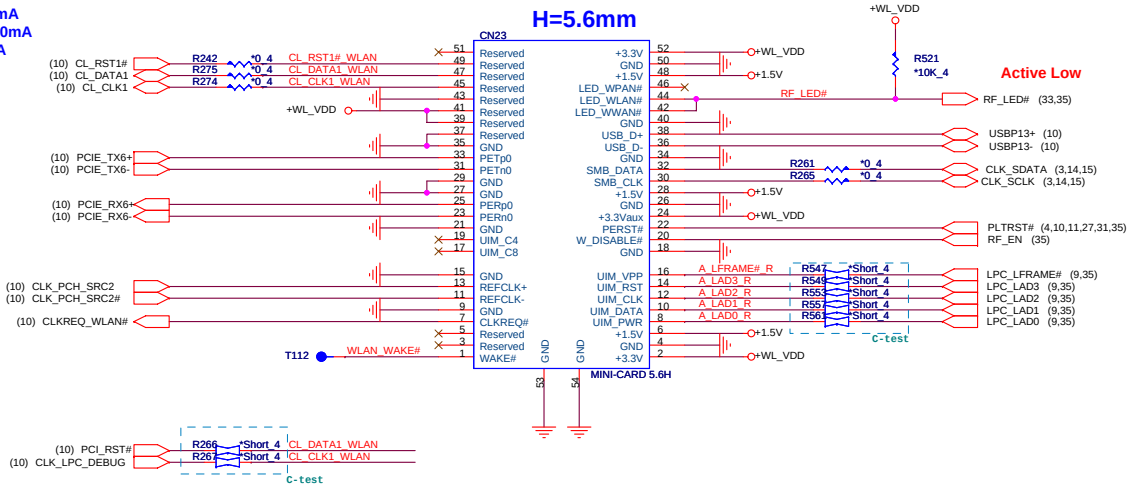
RJ45(LAN)

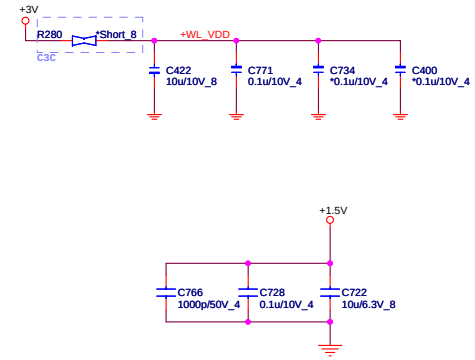


Quanta Computer Inc.			
PROJECT : ZQ1			
Size	Document Number		Rev
	LAN (AR8151)		1A
Date: Friday, January 22, 2010		Sheet 27 of 48	

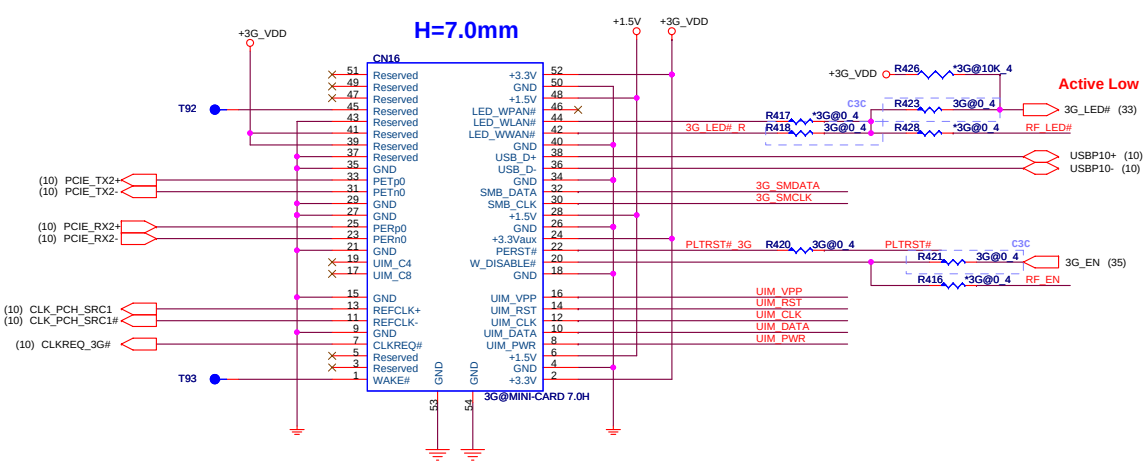
MINI-CARD WLAN(MPC)

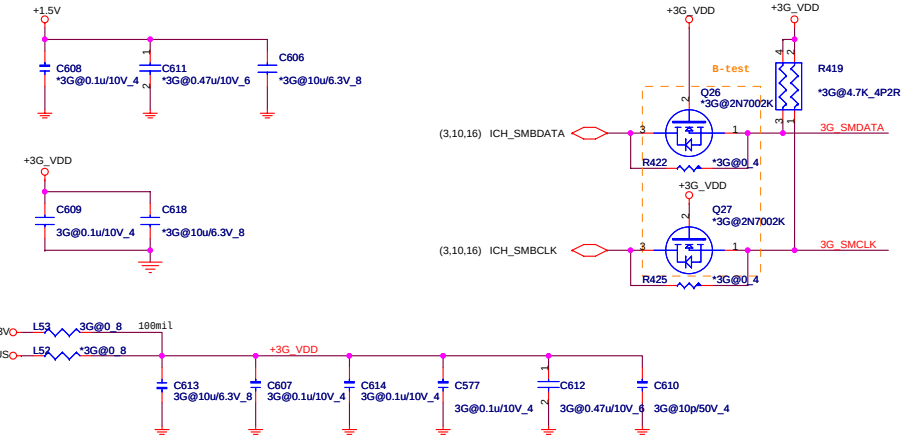
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



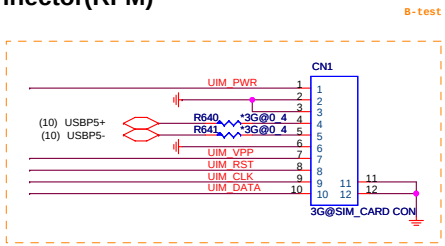


MINI-CARD 3G(MNC)Reserve for JV41-CP





SIM CARD FFC connector(RFM)



Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A

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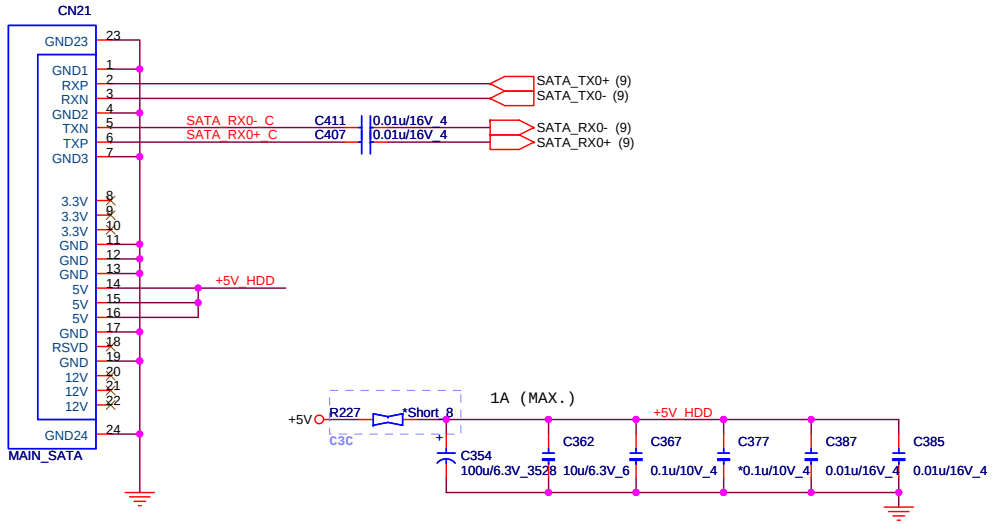
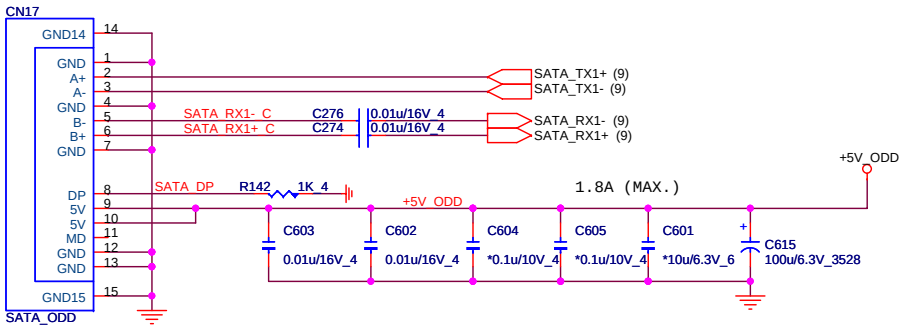
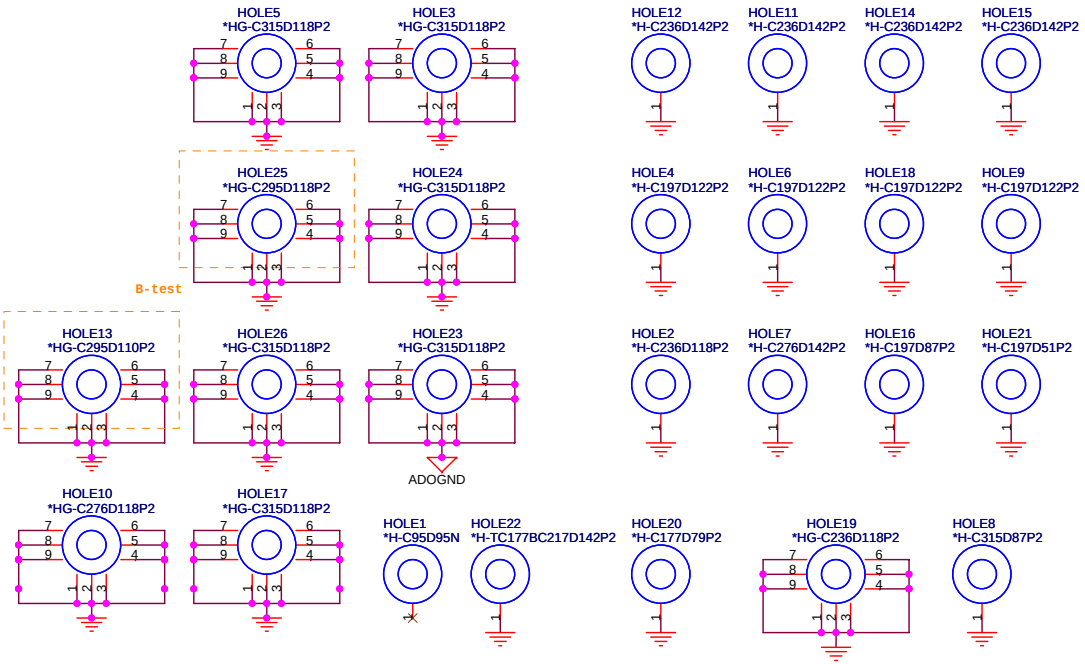
SATA HDD(HDD)



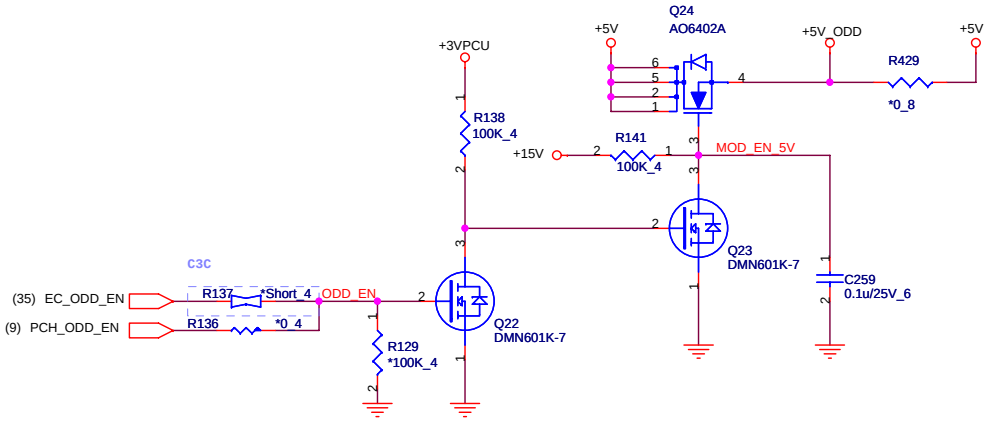
SATA ODD (ODD)



HOLE(OTH)



ODD POWER(ODD)



Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
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Codec(ADO)

U37 ALC271X (Vista Premium Version)

ANALOG — Spilt by AGND

DIGITAL

Place next to pin 38 / Place next to pin 39 / Place next to pin 46 / Place next to pin 1 / Place next to pin 27 / Place next to pin 25 / Place next to pin 9

Spilt by PGND

Spilt by DGND

reverse R441

reverse R429

Placement near Audio Codec

PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion

1.6Vrms

If either HDA device io power use +1.5V,
all device IO power change to +1.5V

0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer

Close to codec

C3C

LINE-OUT/SPDIFO(AMP)

LINEOUT_JD:
HP not insert->H
HP insert->L

Normal OPEN Jack

Near CN25

apply for codec suggestion

MIC(AMP)

Max. 100mVrms input for Mic-IN

Normal OPEN Jack

Near CN28

Power (ADO)

Demodulation Filter L65 Place close to Codec

C730, C787 close U37 pin3 and L65

Vset =1.25V
Vout =Vset[1+AR(1,2)/AR(2,GND)]

Mute(ADO)

ramp change to +5V

ramp reserve R568 for codec

apply for codec suggestion

Internal Speaker(AMP)

40mil for each signal

Speak CN1

Speak CN2

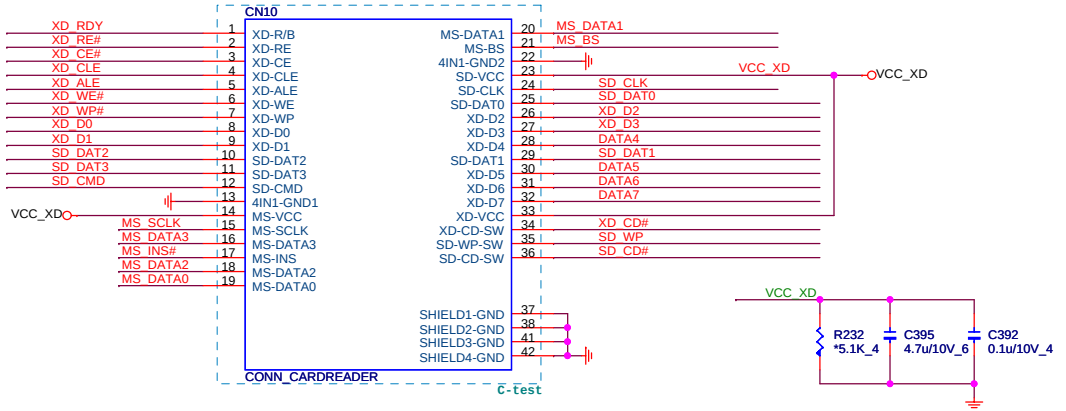
GND_EARTH don't coupling AGND and SPK signals

Tied at one point only under the
ALC269 or near the ALC269

Quanta Computer Inc.
PROJECT : ZQ1
ALC271X / AMP / SPK
Rev 1A
Date: Friday, January 22, 2010
Sheet 30 of 48

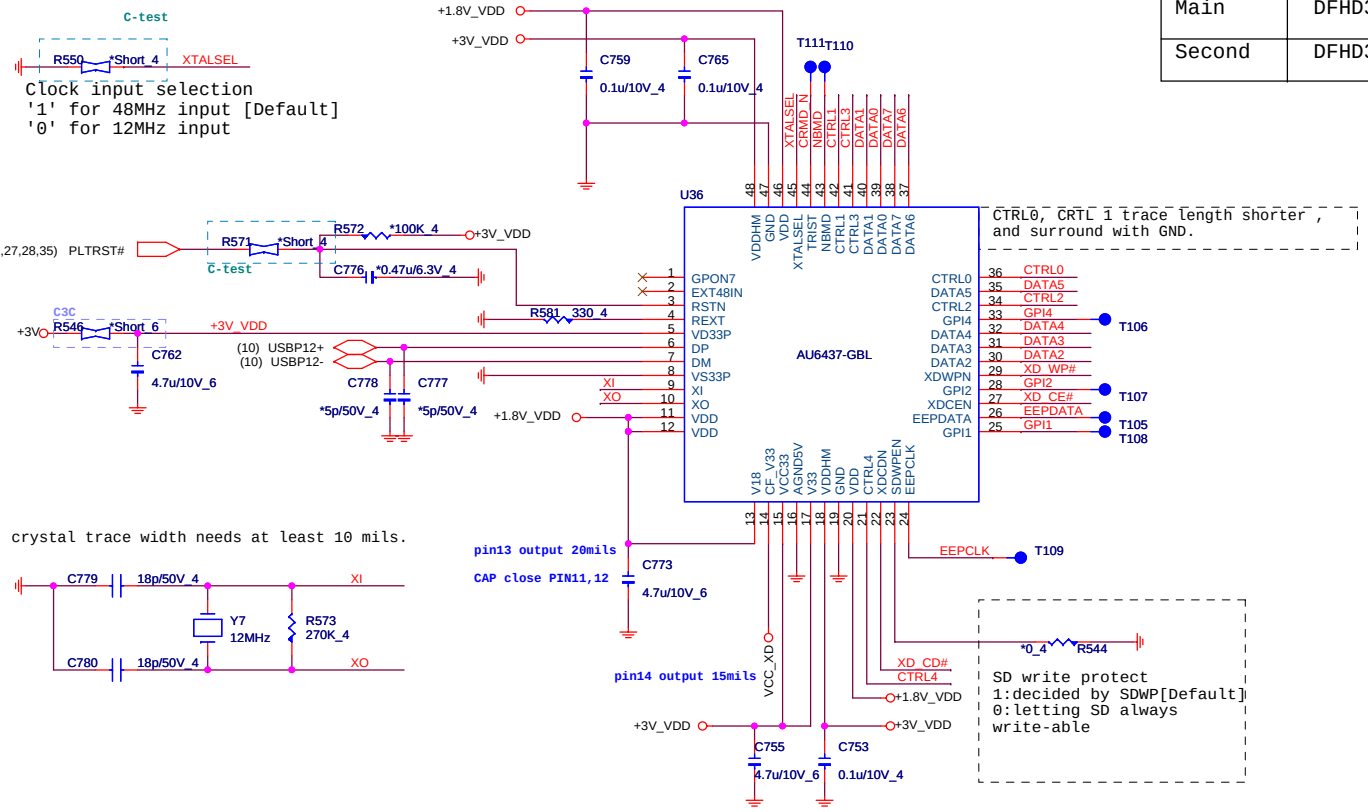
Cardreader(MMC)

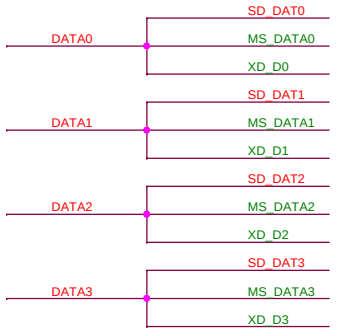
4 IN 1 CARD READER (MMC)



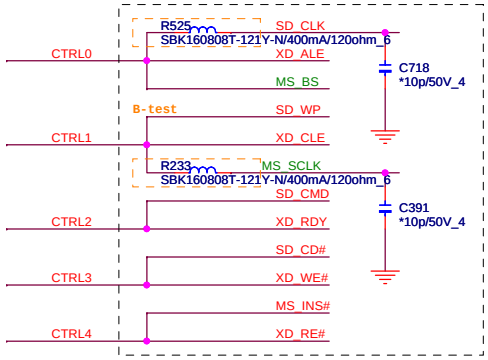
Main	DFHD36MS012
Second	DFHD38MS013

Close to CN14 pin 14 & pin23
4.7u CAP close to pin23





Close to connector



Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	AU6437 CardReader	1A

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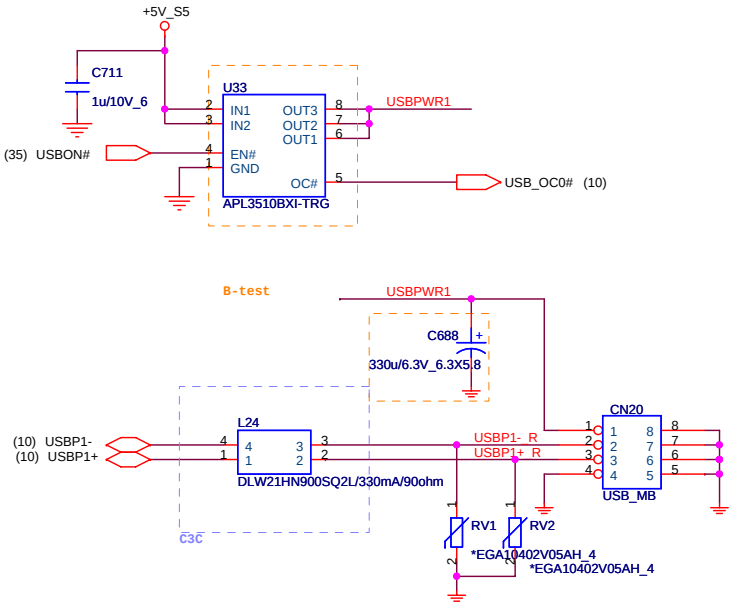
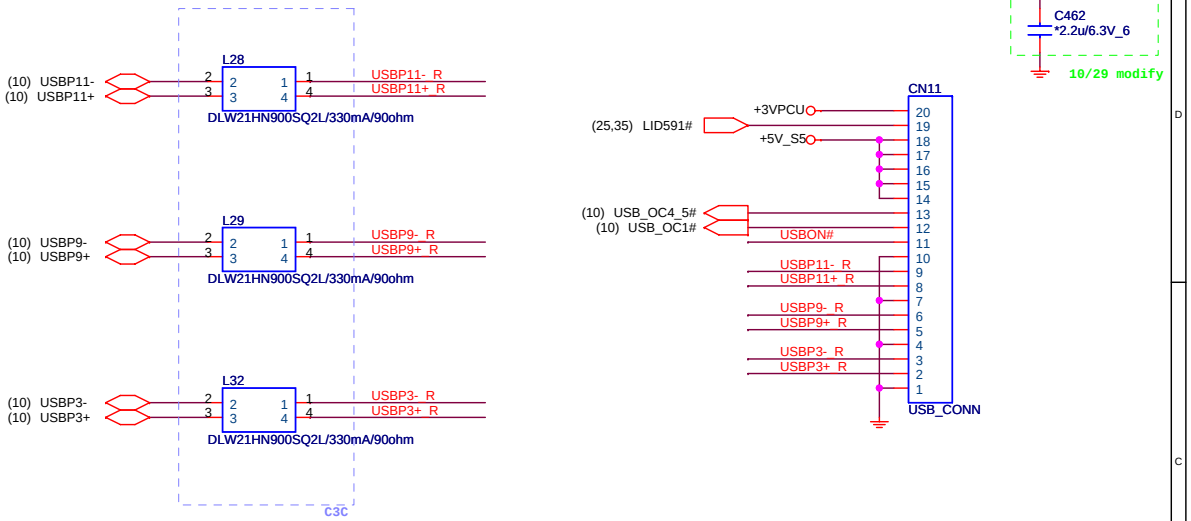
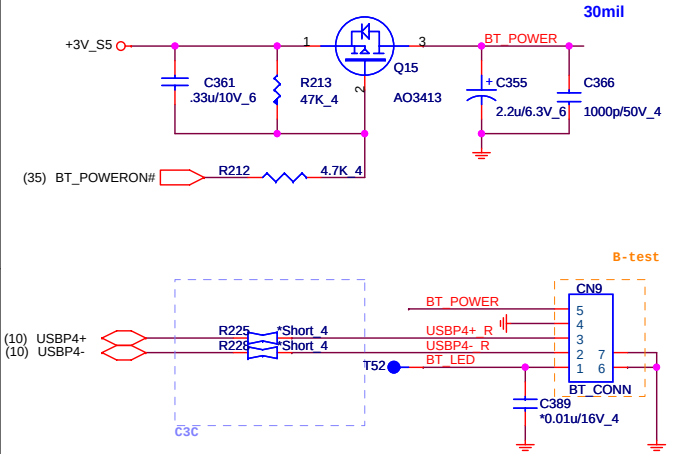
USB PORT(USB)



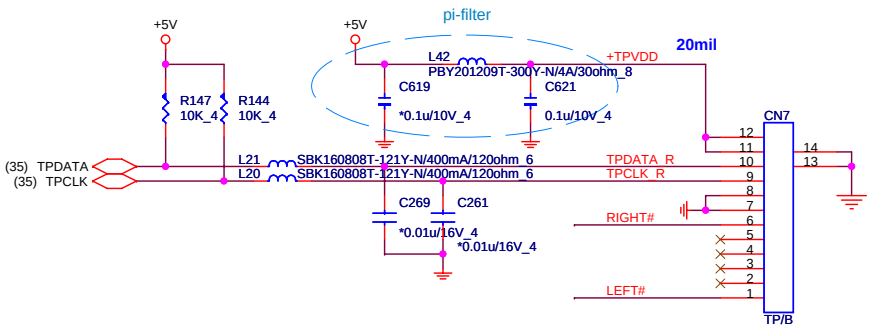
USB BOARD CONN(USB)



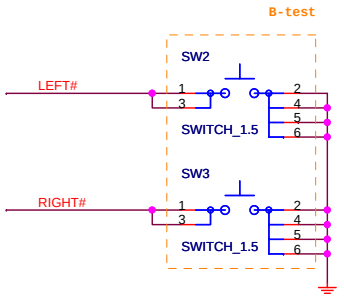
BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)

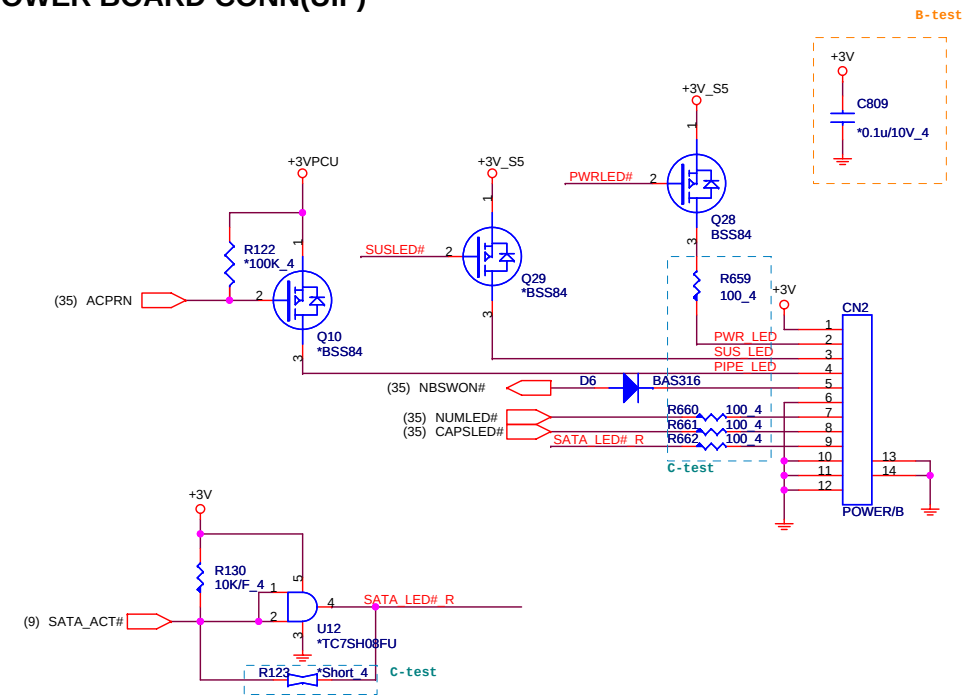


TP SWITCH(UIF)

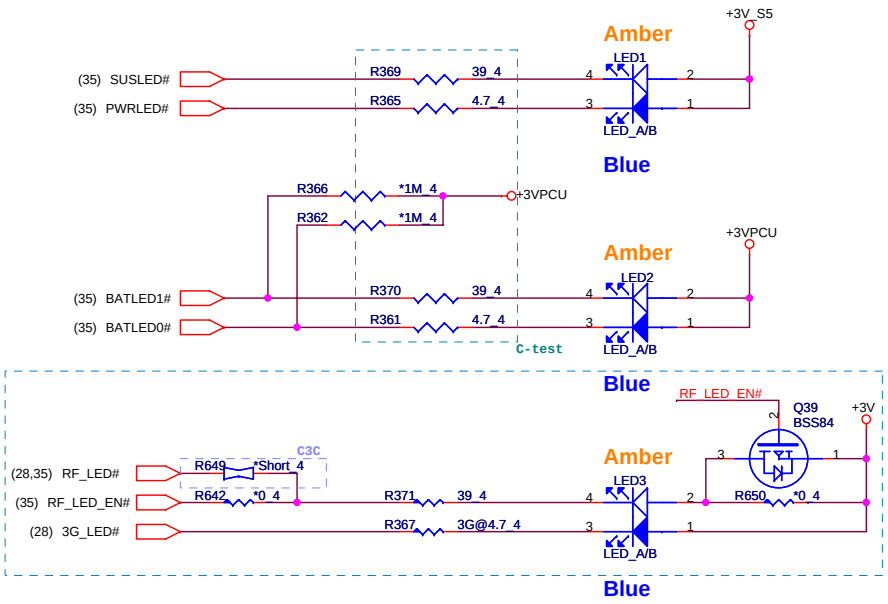


Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number	Rev
	eSATA/USB	1A
Date: Friday, January 22, 2010	Sheet 32 of 48	

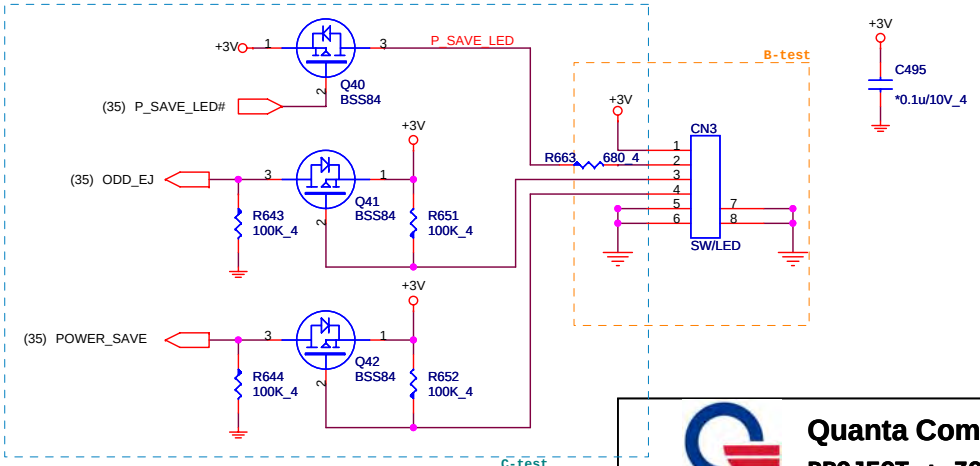
POWER BOARD CONN(UIF)



LED(UIF)



SW BOARD CONNECTOR(UIF)



Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	POWER BOARD/LED/SW DB	1A

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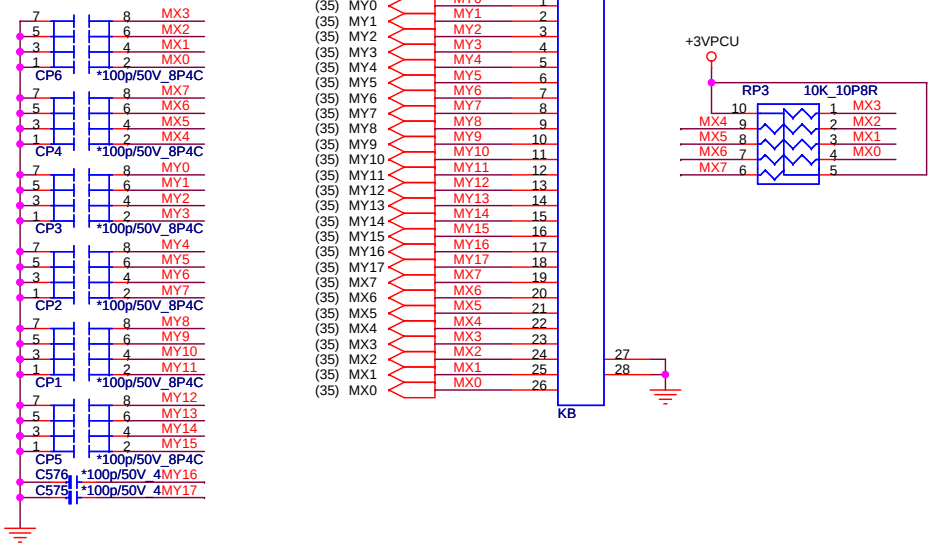
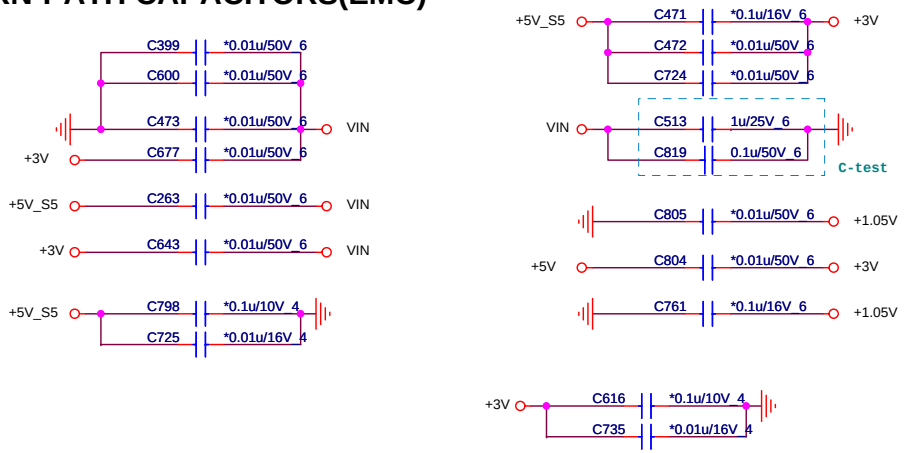
14" K/B(KBC)

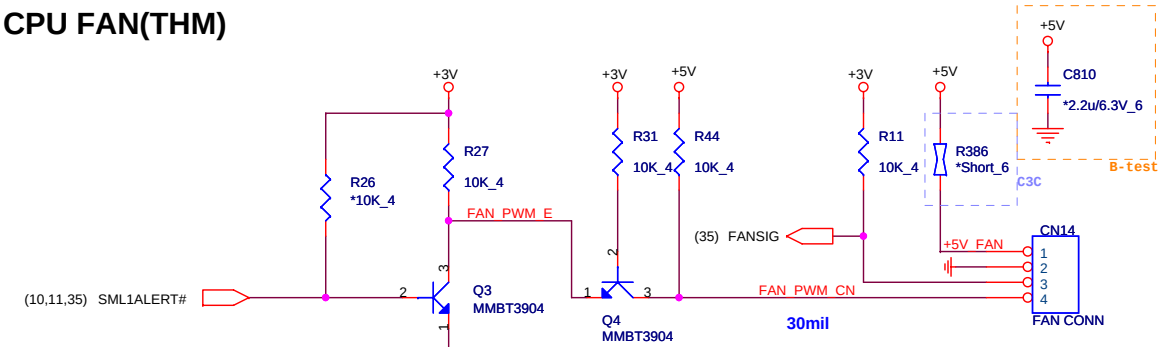


EE RETURN-PATH CAPACITORS(EMC)



STITCHING for LPC

CPU FAN(THM)



Quanta Computer Inc.

PROJECT : ZQ1

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A

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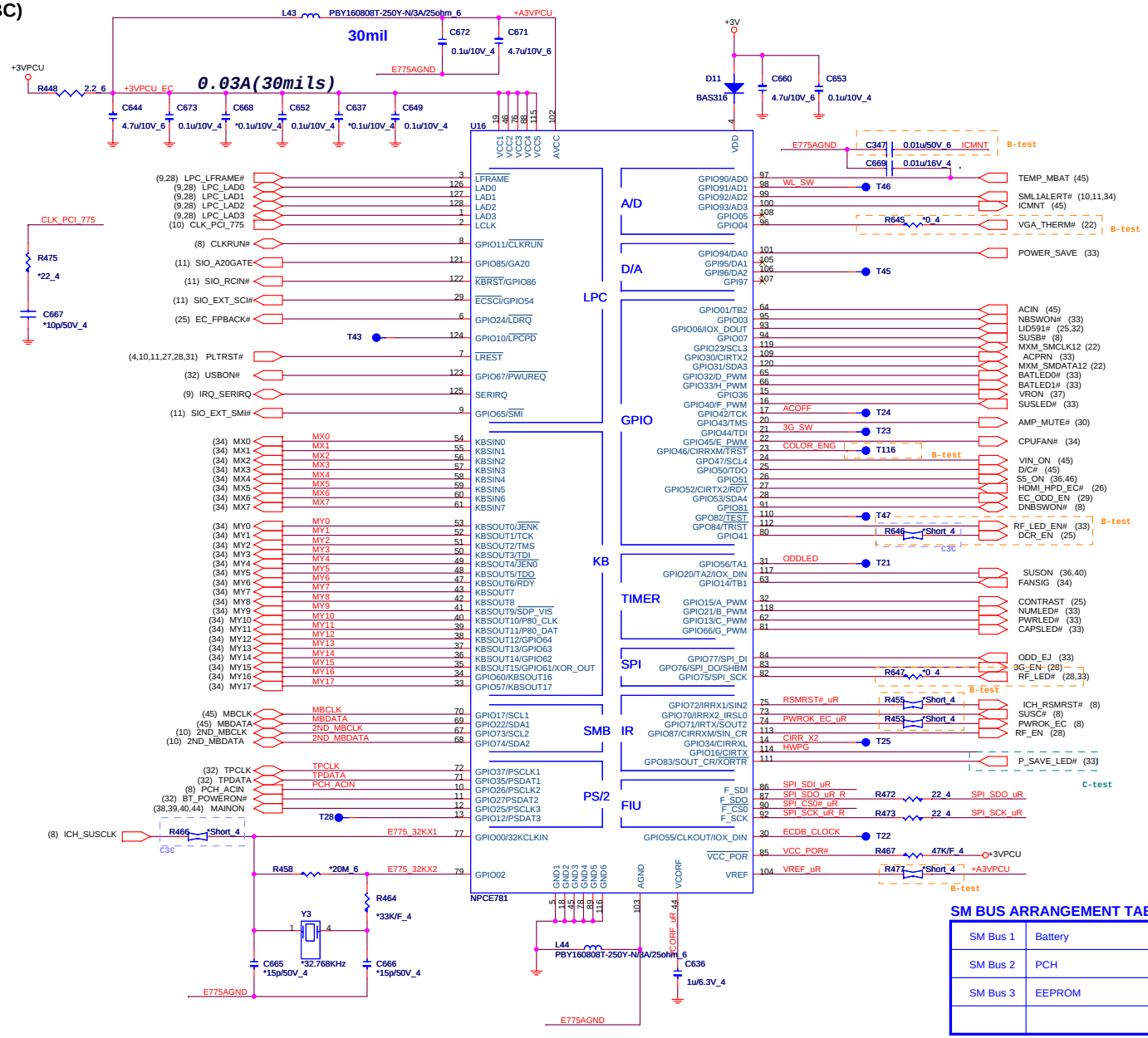
EC(KBC)



SM BUS ARRANGEMENT TABLE

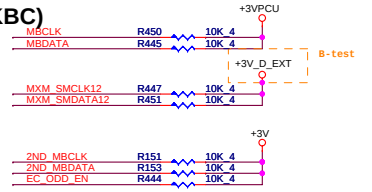
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	EEPROM

I/O ADDRESS SETTING(KBC)

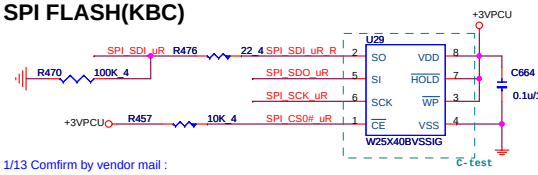
SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

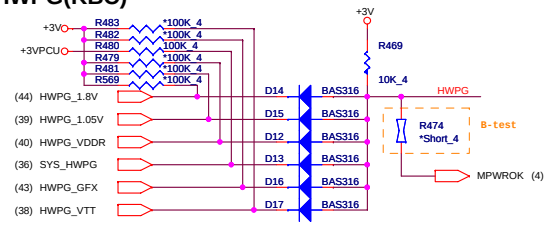


SPI FLASH(KBC)

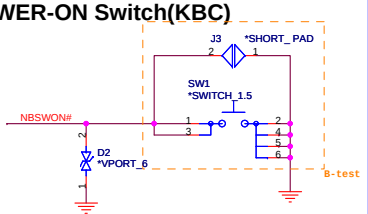


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

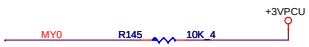
HWPG(KBC)



POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)



Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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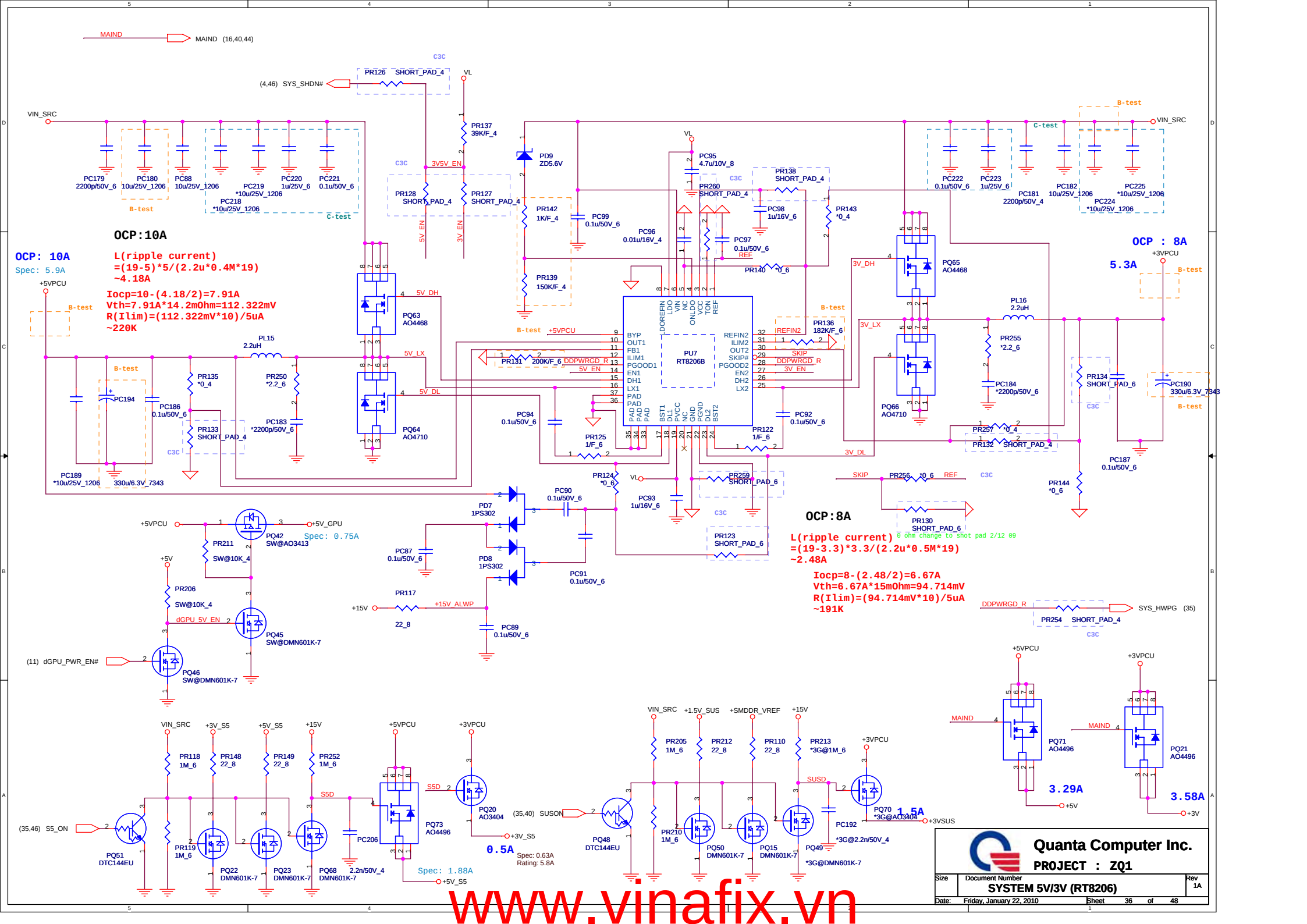
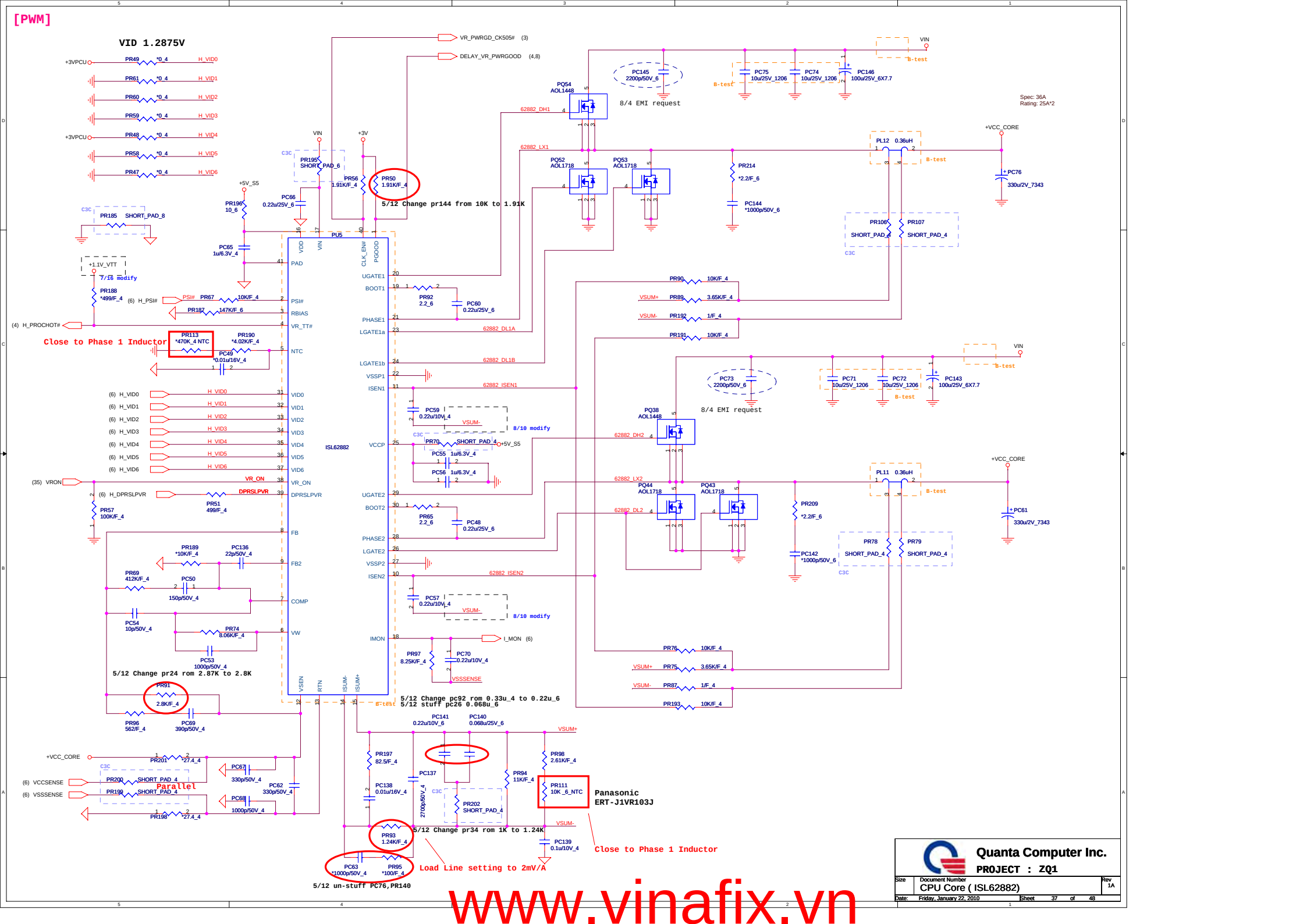
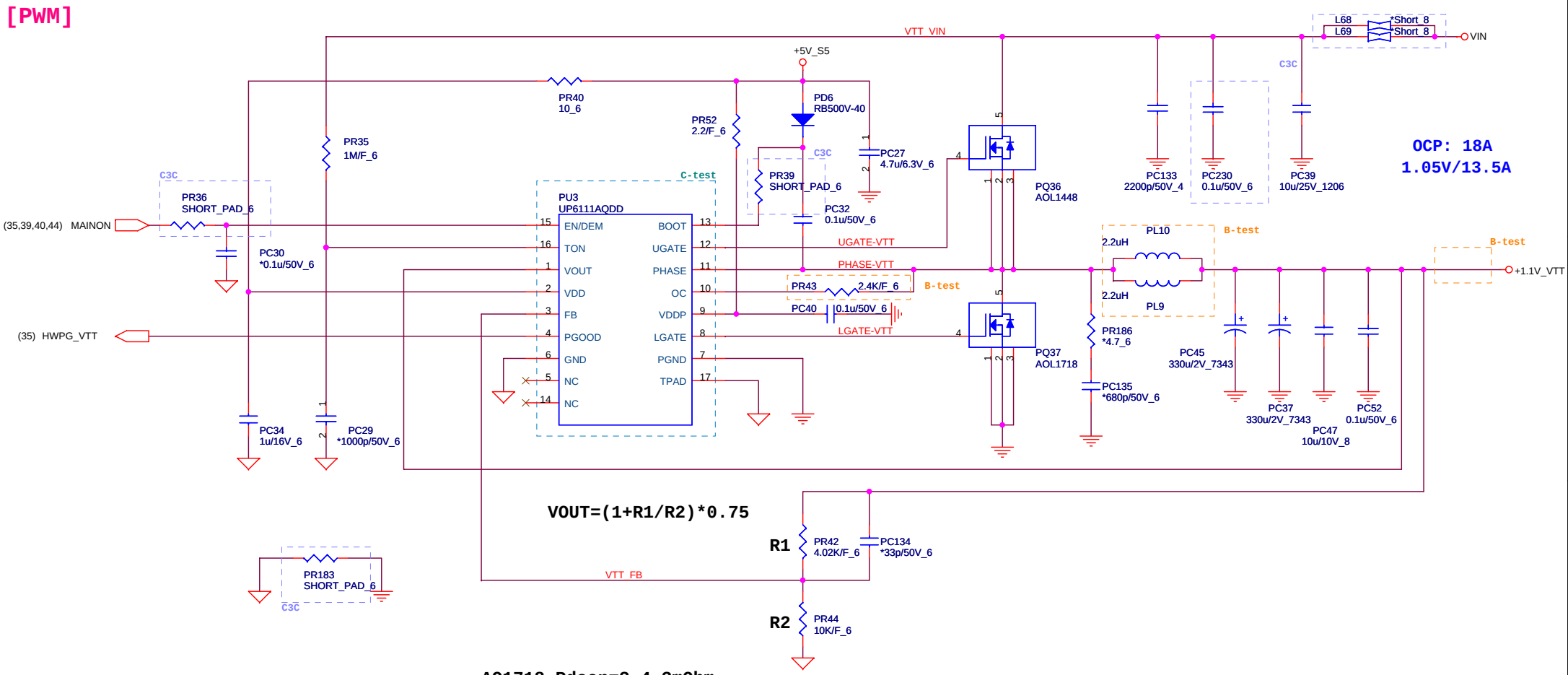

MAIND
MAIND (16,40,44)
(4,46) SYS_SHDN#
PR126 SHORT_PAD_4
VL
VIN_SRC
PR137 39K/F_4
PD9 ZD5.6V
PR142 1K/F_4
PR139 150K/F_4
PC99 0.1u/50V_6
PC96 0.01u/16V_4
PC95 4.7u/10V_8
PR260 SHORT_PAD_4
PR138 SHORT_PAD_4
PC98 1u/16V_6
PR143 *0_4
PR140 *0_6
PC97 0.1u/50V_6
REF
3V5V_EN
5V_EN
3V_EN
PR128 SHORT_PAD_4
PR127 SHORT_PAD_4
PC179 2200p/50V_6
PC180 10u/25V_1206
PC88 10u/25V_1206
PC219 *10u/25V_1206
PC218 *10u/25V_1206
PC220 1u/25V_6
PC221 0.1u/50V_6
PC222 0.1u/50V_6
PC223 1u/25V_6
PC181 2200p/50V_4
PC182 10u/25V_1206
PC225 *10u/25V_1206
PC224 *10u/25V_1206
B-test
C-test
C3C
OCP:10A
OCP: 10A
Spec: 5.9A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP : 8A
5.3A
+3VPCU
+5VPCU
PQ63 AO4468
PQ64 AO4710
PQ65 AO4468
PQ66 AO4710
5V_DH
5V_LX
5V_DL
3V_DH
3V_LX
3V_DL
PL15 2.2uH
PL16 2.2uH
PR135 *0_4
PR250 *2.2_6
PR183 *2200p/50V_6
PR133 SHORT_PAD_4
PC194
PC186 0.1u/50V_6
PC189 *10u/25V_1206
330u/6.3V_7343
PR255 *2.2_6
PC184 *2200p/50V_6
PR134 SHORT_PAD_6
PC190 330u/6.3V_7343
PR251 *0_4
PR132 SHORT_PAD_4
PC187 0.1u/50V_6
PR144 *0_6
PU7 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
BST1
DLI
PVCC
NC
GND
DL2
BST2
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
DDPWRGD_R
SKIP
REFIN2
PR136 182K/F_6
PR131 200K/F_6
PC94 0.1u/50V_6
PC92 0.1u/50V_6
PR125 1/F_6
PR122 1/F_6
PR124 *0_6
PC93 1u/16V_6
PR259 SHORT_PAD_6
PR123 SHORT_PAD_6
PR256 *0_6
PR130 SHORT_PAD_6
0 ohm change to shot pad 2/12 09
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PD7 1PS302
PD8 1PS302
PC90 0.1u/50V_6
PC91 0.1u/50V_6
PC87 0.1u/50V_6
PC89 0.1u/50V_6
PR117 22_8
+15V_ALWP
+15V
+5V_GPU
PQ42 SW@AO3413
Spec: 0.75A
PR211 SW@10K_4
PR206 SW@10K_4
dGPU_5V_EN
PQ45 SW@DMN601K-7
PQ46 SW@DMN601K-7
(11) dGPU_PWR_EN#
DDPWRGD_R
SYS_HWPG (35)
PR254 SHORT_PAD_4
VIN_SRC
+3V_S5
+5V_S5
+15V
PR118 1M_6
PR148 22_8
PR149 22_8
PR252 1M_6
S5D
PQ73 AO4496
PQ20 AO3404
PC206
PQ51 DTC144EU
PQ22 DMN601K-7
PQ23 DMN601K-7
PQ68 DMN601K-7
2.2n/50V_4
(35,46) S5_ON
+3V_S5
0.5A
Spec: 0.63A
Rating: 5.8A
Spec: 1.88A
+5V_S5
+1.5V_SUS
+SMDDR_VREF
PR205 1M_6
PR212 22_8
PR110 22_8
PR213 *3G@1M_6
SUSD
PQ48 DTC144EU
PR210 1M_6
PQ50 DMN601K-7
PQ15 DMN601K-7
PQ49 *3G@DMN601K-7
PQ70 *3G@AO3404
PC192 *3G@2.2n/50V_4
(35,40) SUSON
+3VSUS
1.5A
MAIND
PQ71 AO4496
PQ21 AO4496
3.29A
3.58A
+5V
+3V
Quanta Computer Inc.
PROJECT : ZQ1
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Friday, January 22, 2010
Sheet 36 of 48
www.vinafix.vn


[PWM]
VID 1.2875V
ISL62882
5/12 Change pr144 from 10K to 1.91K
Close to Phase 1 Inductor
5/12 Change pr24 rom 2.87K to 2.8K
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
5/12 Change pr34 rom 1K to 1.24K
5/12 un-stuff PC76,PR140
Load Line setting to 2mV/A
Close to Phase 1 Inductor
Panasonic
ERT-J1VR103J
Parallel
8/4 EMI request
8/4 EMI request
8/10 modify
8/10 modify
7/16 modify
Spec: 36A
Rating: 25A*2
Quanta Computer Inc.
PROJECT : ZQ1
CPU Core (ISL62882)
Friday, January 22, 2010
www.vinafix.vn



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Quanta Computer Inc. PROJECT : ZQ1		
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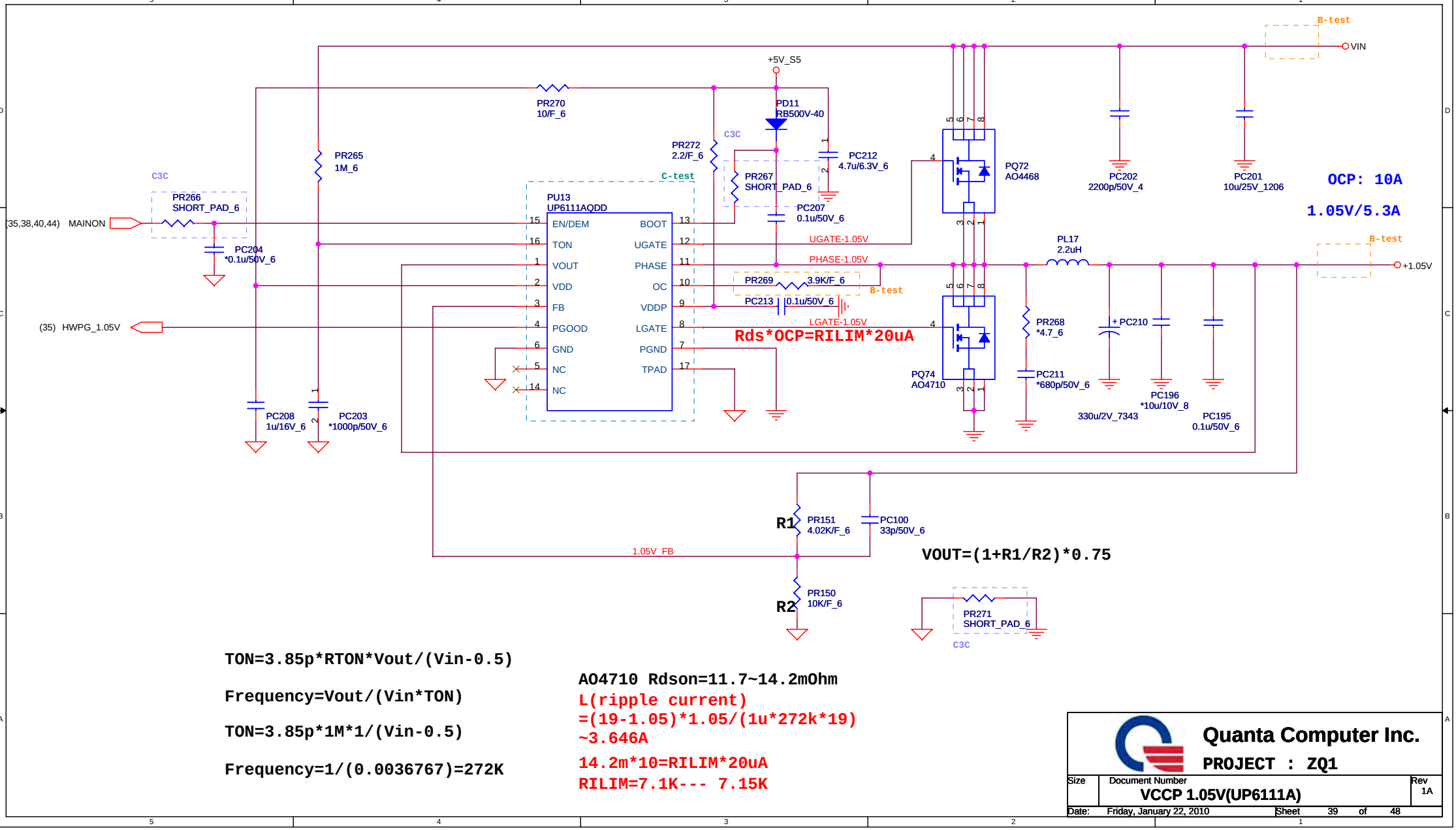


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

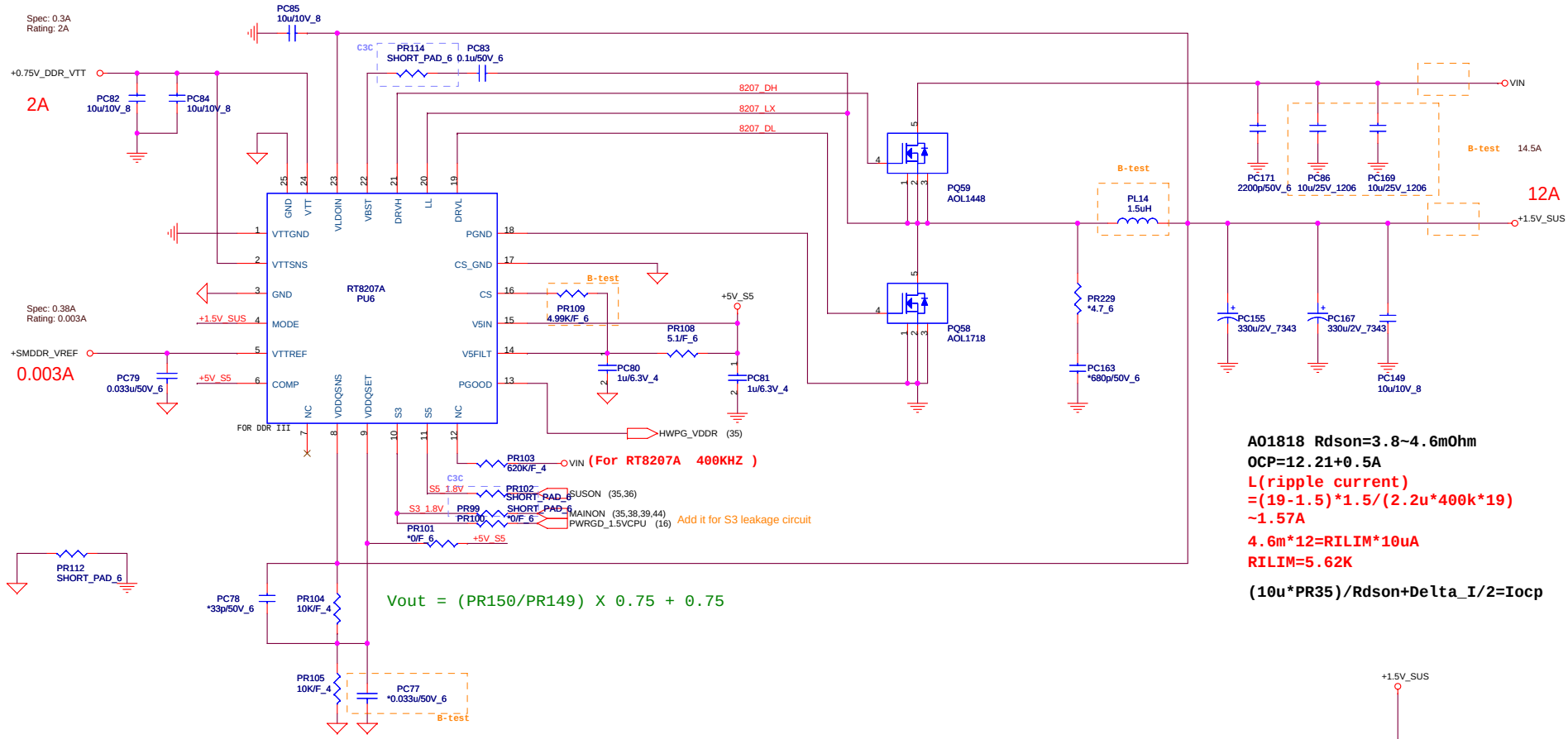
AO4710 Rdson=11.7~14.2mOhm

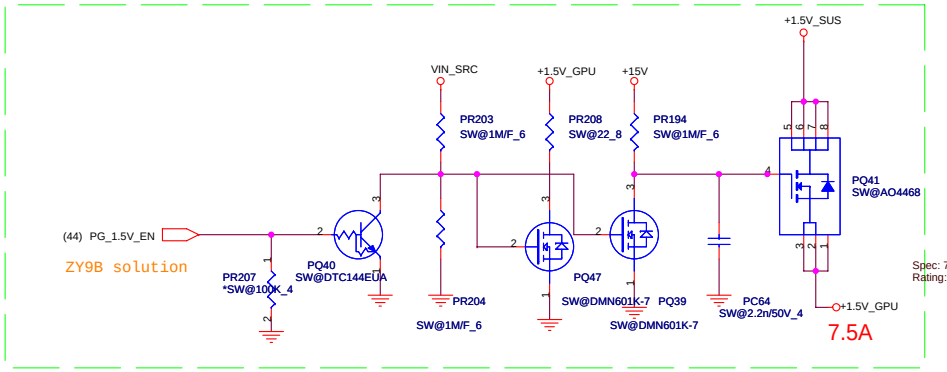
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

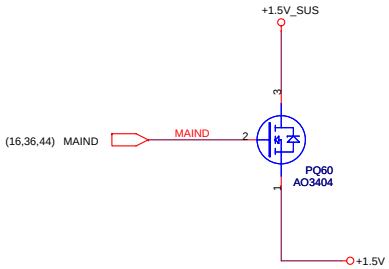
14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Friday, January 22, 2010	Sheet 39 of 48	







Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	DDR III 1.5V(TPS51116)	1A

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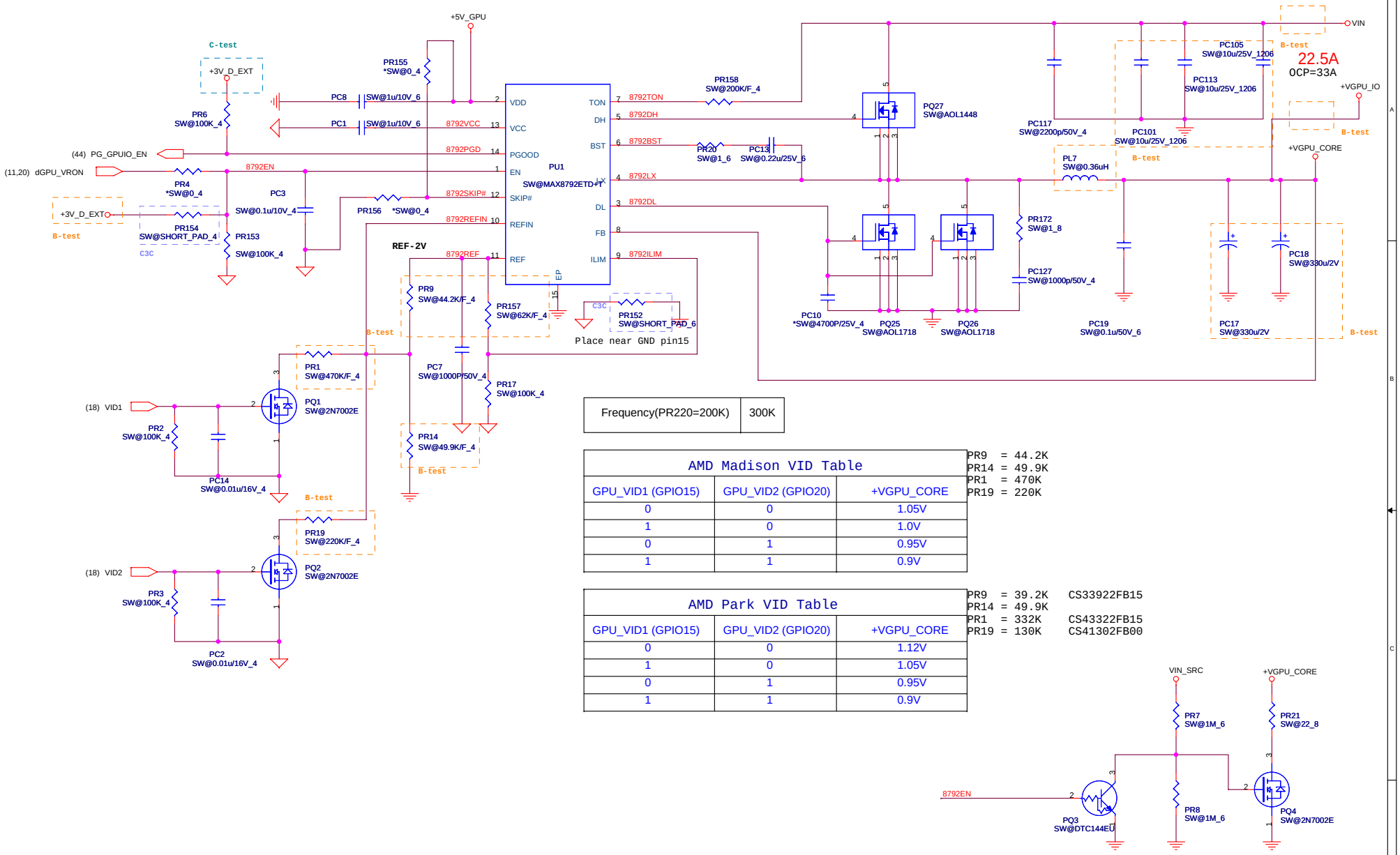

Frequency(PR220=200K)	300K

AMD Madison VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

PR9 = 44.2K
PR14 = 49.9K
PR1 = 470K
PR19 = 220K

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

PR9 = 39.2K CS33922FB15
PR14 = 49.9K
PR1 = 332K CS43322FB15
PR19 = 130K CS41302FB00

Quanta Computer Inc.
PROJECT : ZQ1

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	GPU CORE(MAX8792)	1A

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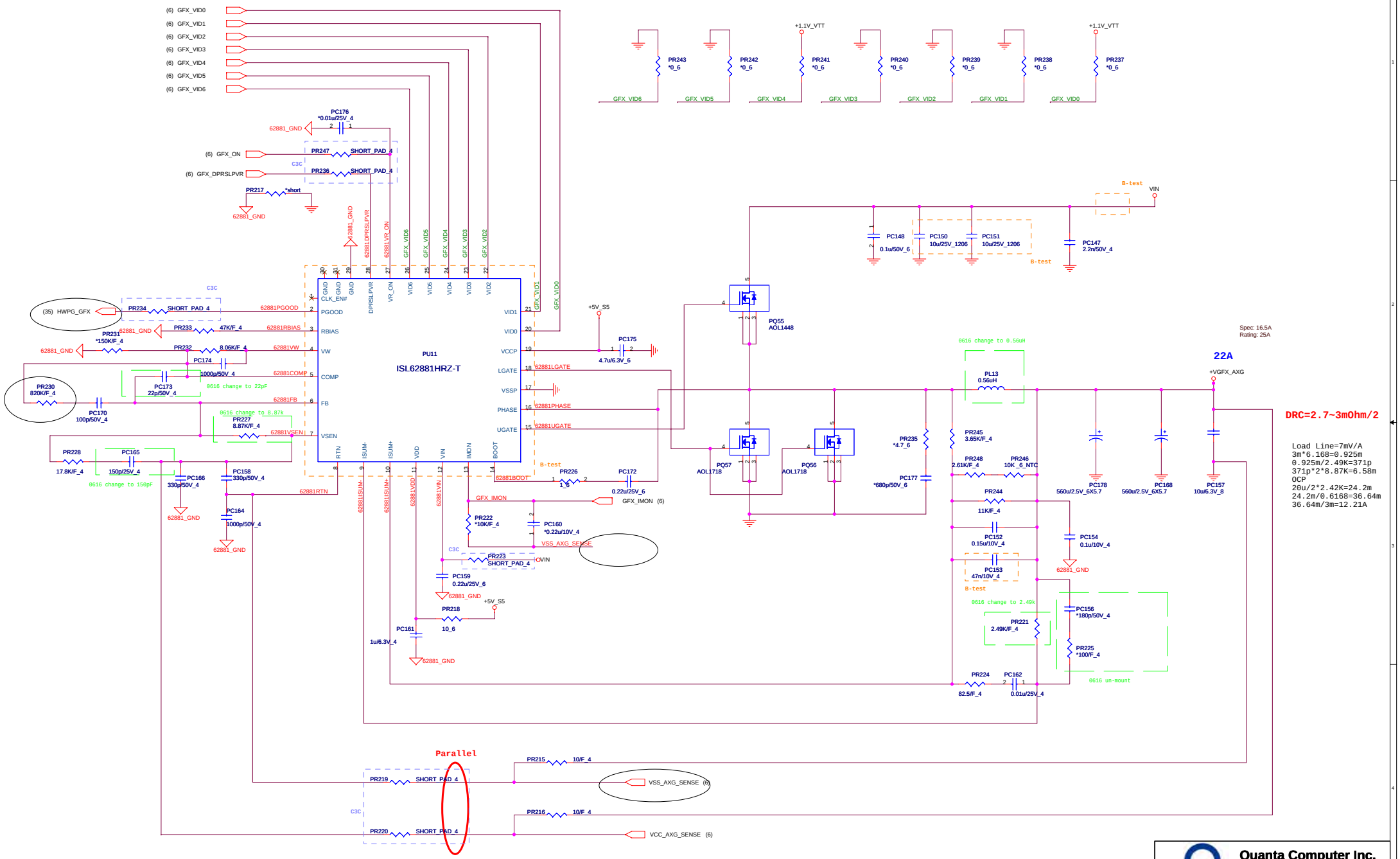
Int_VGA [PWM]



Quanta Computer Inc.
PROJECT : ZQ1

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

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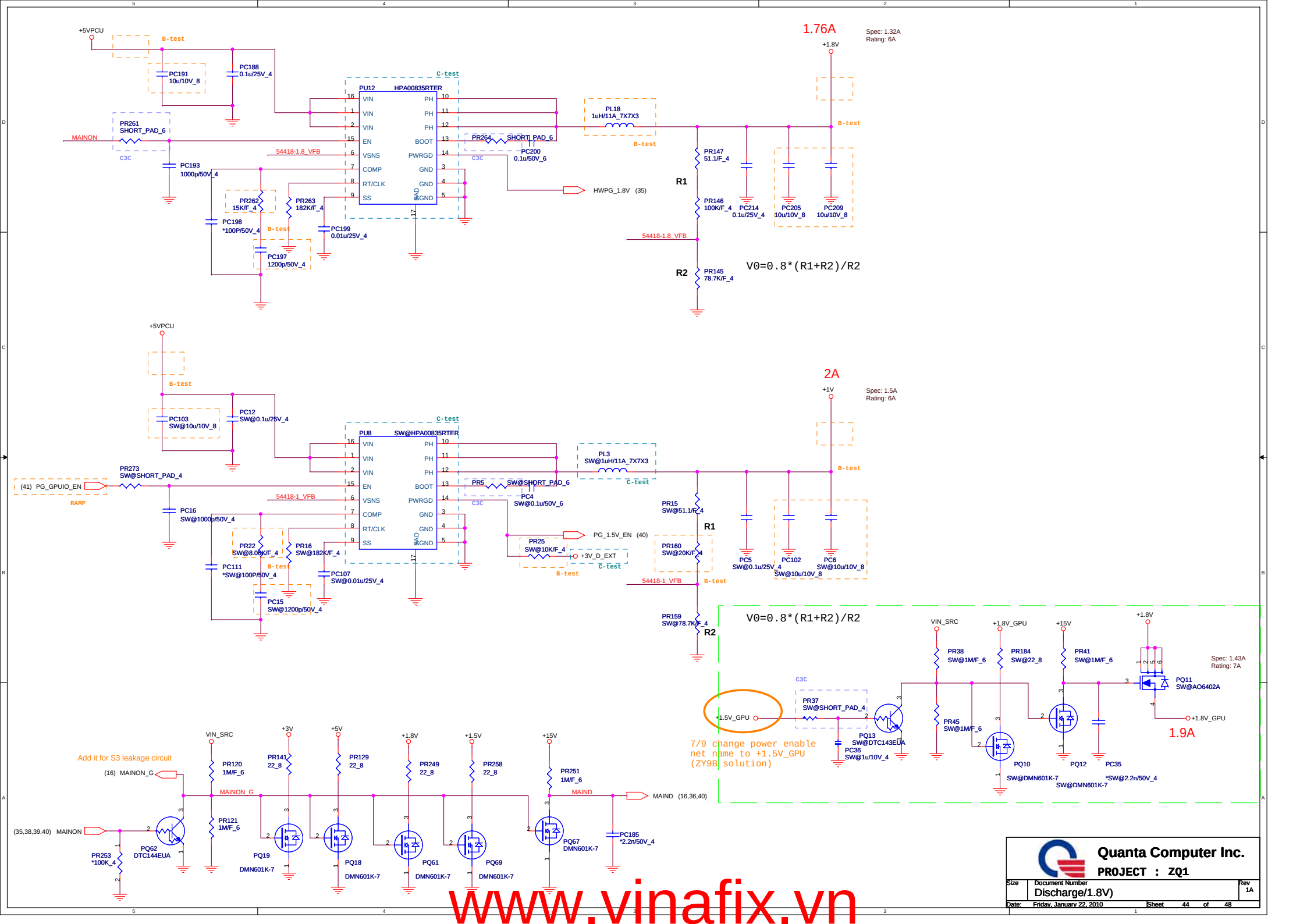
1.76A
Spec: 1.32A
Rating: 6A
+5VPCU
B-test
PC191 10u/10V_8
PC188 0.1u/25V_4
C-test
PU12 HPA00835RTER
VIN
PH
EN
BOOT
VSNS
PWRGD
COMP
GND
RT/CLK
SS
PAD
PR261 SHORT_PAD_6
MAINON
C3C
PC193 1000p/50V_4
54418-1.8_VFB
PR262 15K/F_4
PR263 182K/F_4
PC198 *100P/50V_4
PC199 0.01u/25V_4
PC197 1200p/50V_4
PR264 SHORT_PAD_6
PC200 0.1u/50V_6
PL18 1uH/11A_7X7X3
HWPG_1.8V (35)
+1.8V
PR147 51.1/F_4
R1
PR146 100K/F_4
PC214 0.1u/25V_4
PC205 10u/10V_8
PC209 10u/10V_8
R2
PR145 78.7K/F_4
V0=0.8*(R1+R2)/R2
2A
Spec: 1.5A
Rating: 6A
+1V
PC103 SW@10u/10V_8
PC12 SW@0.1u/25V_4
PU8 SW@HPA00835RTER
PR273 SW@SHORT_PAD_4
(41) PG_GPUIO_EN
RAMP
PC16 SW@1000p/50V_4
54418-1_VFB
PR22 SW@8.06K/F_4
PR16 SW@182K/F_4
PC111 *SW@100P/50V_4
PC107 SW@0.01u/25V_4
PC15 SW@1200p/50V_4
PR5 SW@SHORT_PAD_6
PC4 SW@0.1u/50V_6
PL3 SW@1uH/11A_7X7X3
PG_1.5V_EN (40)
PR25 SW@10K/F_4
+3V_D_EXT
PR15 SW@51.1/F_4
PR160 SW@20K/F_4
PR159 SW@78.7K/F_4
PC5 SW@0.1u/25V_4
PC102 SW@10u/10V_8
PC6 SW@10u/10V_8
V0=0.8*(R1+R2)/R2
VIN_SRC
+1.8V_GPU
+15V
PR38 SW@1M/F_6
PR184 SW@22_8
PR41 SW@1M/F_6
PR37 SW@SHORT_PAD_4
+1.5V_GPU
PQ13 SW@DTC143EUA
PC36 SW@1u/10V_4
PR45 SW@1M/F_6
PQ10 SW@DMN601K-7
PQ12 SW@DMN601K-7
PC35 *SW@2.2n/50V_4
PQ11 SW@AO6402A
Spec: 1.43A
Rating: 7A
1.9A
7/9 change power enable net name to +1.5V_GPU (ZY9B solution)
Add it for S3 leakage circuit
(16) MAINON_G
MAINON_G
PR120 1M/F_6
PR121 1M/F_6
PR253 *100K_4
PQ62 DTC144EUA
(35,38,39,40) MAINON
+3V
+5V
+1.8V
+1.5V
+15V
PR141 22_8
PR129 22_8
PR249 22_8
PR258 22_8
PR251 1M/F_6
MAIND
MAIND (16,36,40)
PQ19 DMN601K-7
PQ18 DMN601K-7
PQ61 DMN601K-7
PQ69 DMN601K-7
PQ67 DMN601K-7
PC185 *2.2n/50V_4
Quanta Computer Inc.
PROJECT : ZQ1
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Discharge/1.8V)
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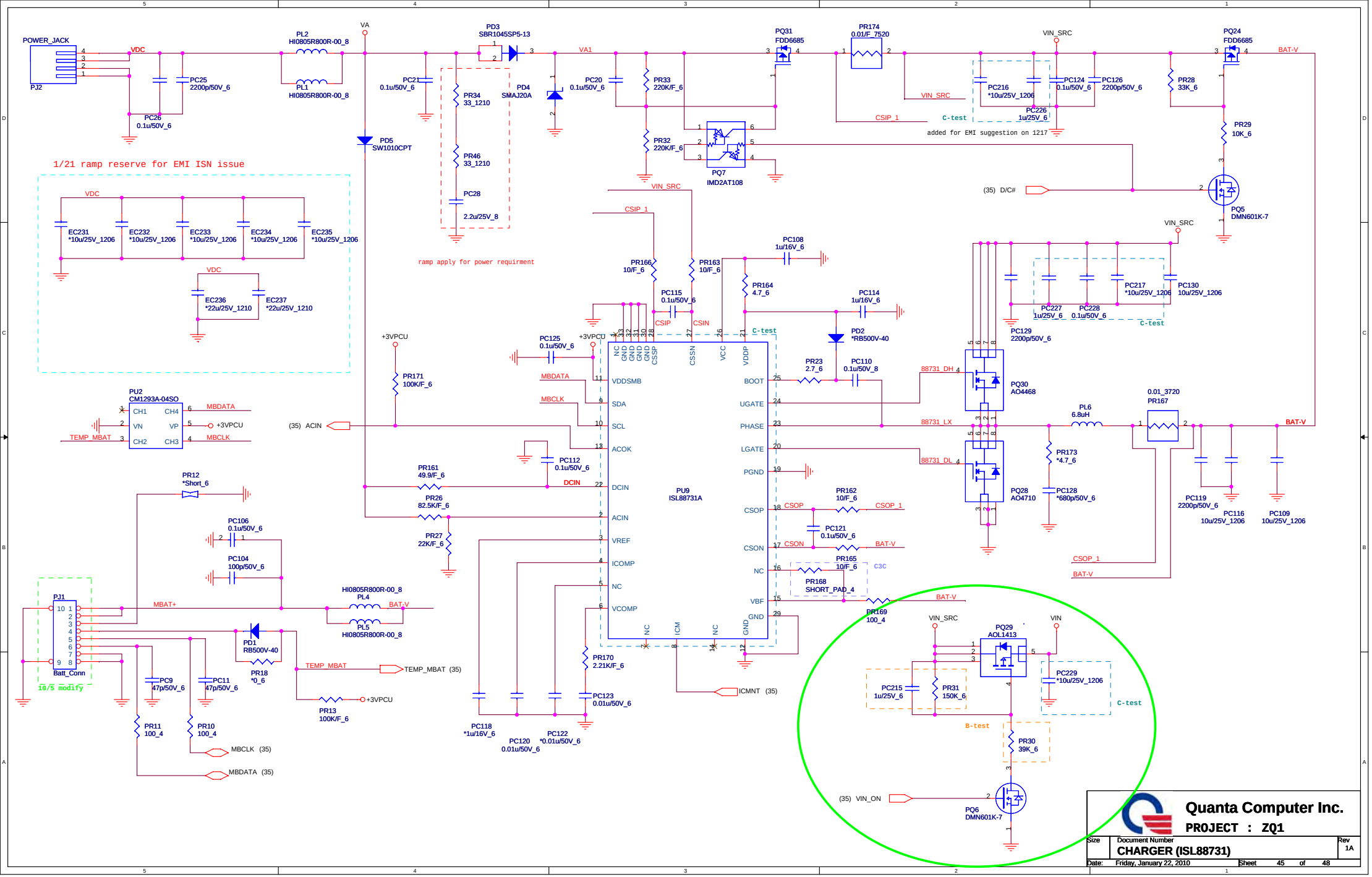

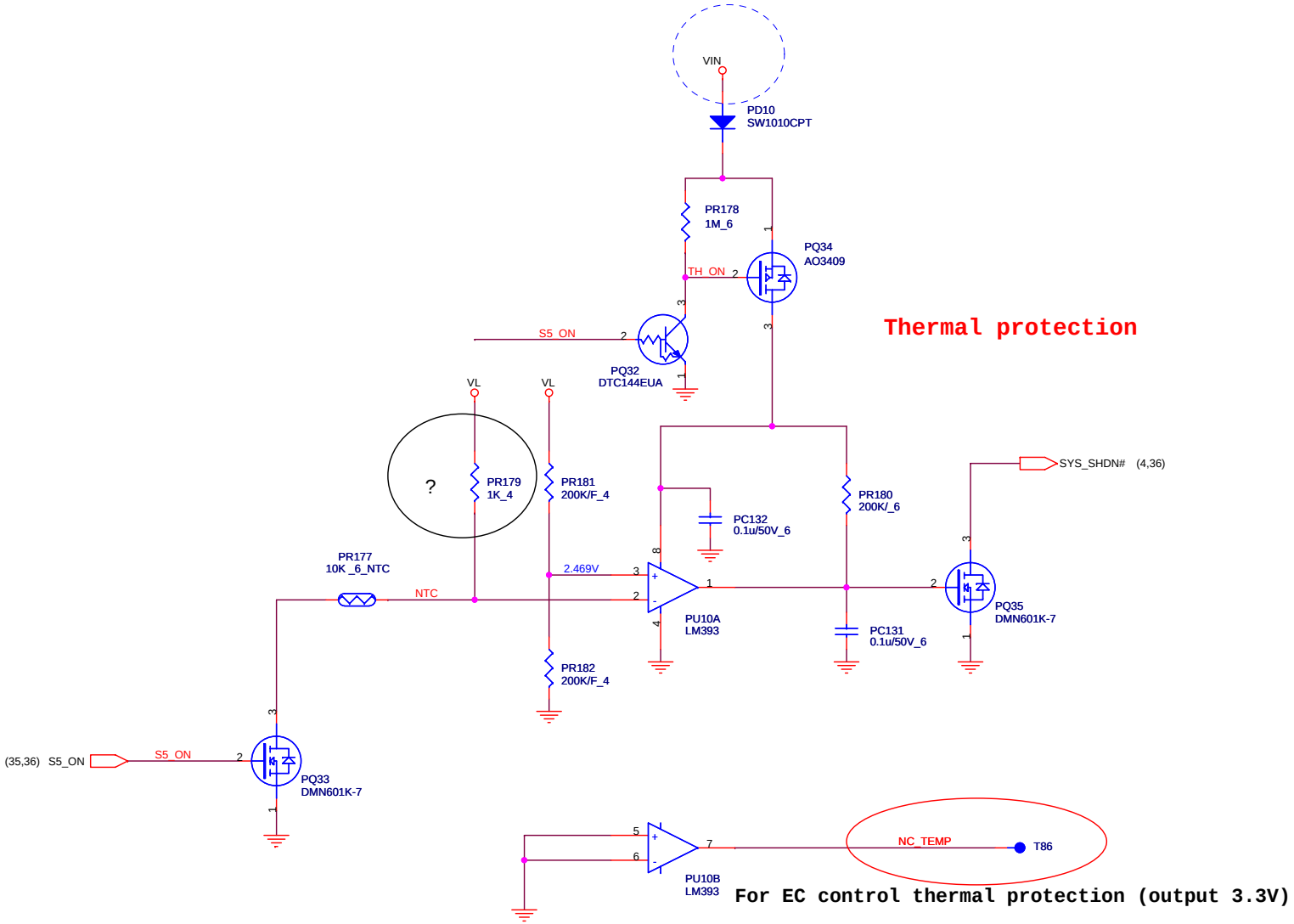

Quanta Computer Inc.		
PROJECT : ZQ1		
Size	Document Number: Thermal Protection	Rev: 1A
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