Project Name :GK5KN6Z

Platform : CFL_H+N17E-G1

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39. +1.0VA_PCH/VCCIO
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57. BIOS,XTAL ,External SS ,M
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59. STRAP
60. SV3H612V 3D VOL
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62. change list2
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M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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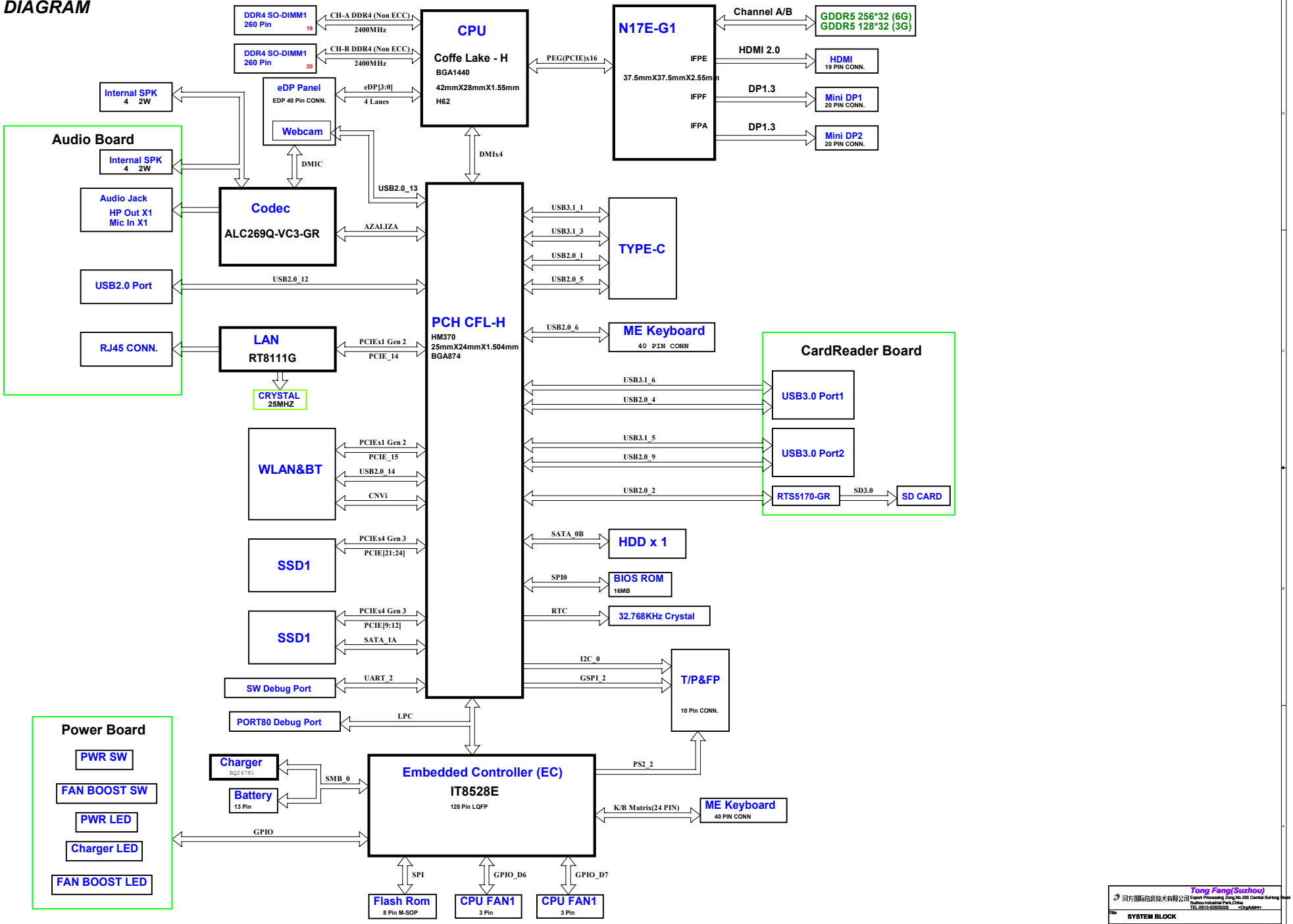
SYSTEM BLOCK DIAGRAM



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Title: SYSTEM BLOCK

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POWER ON SEQUENCE

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Title: POWER DIAGRAM & SEQUENCE

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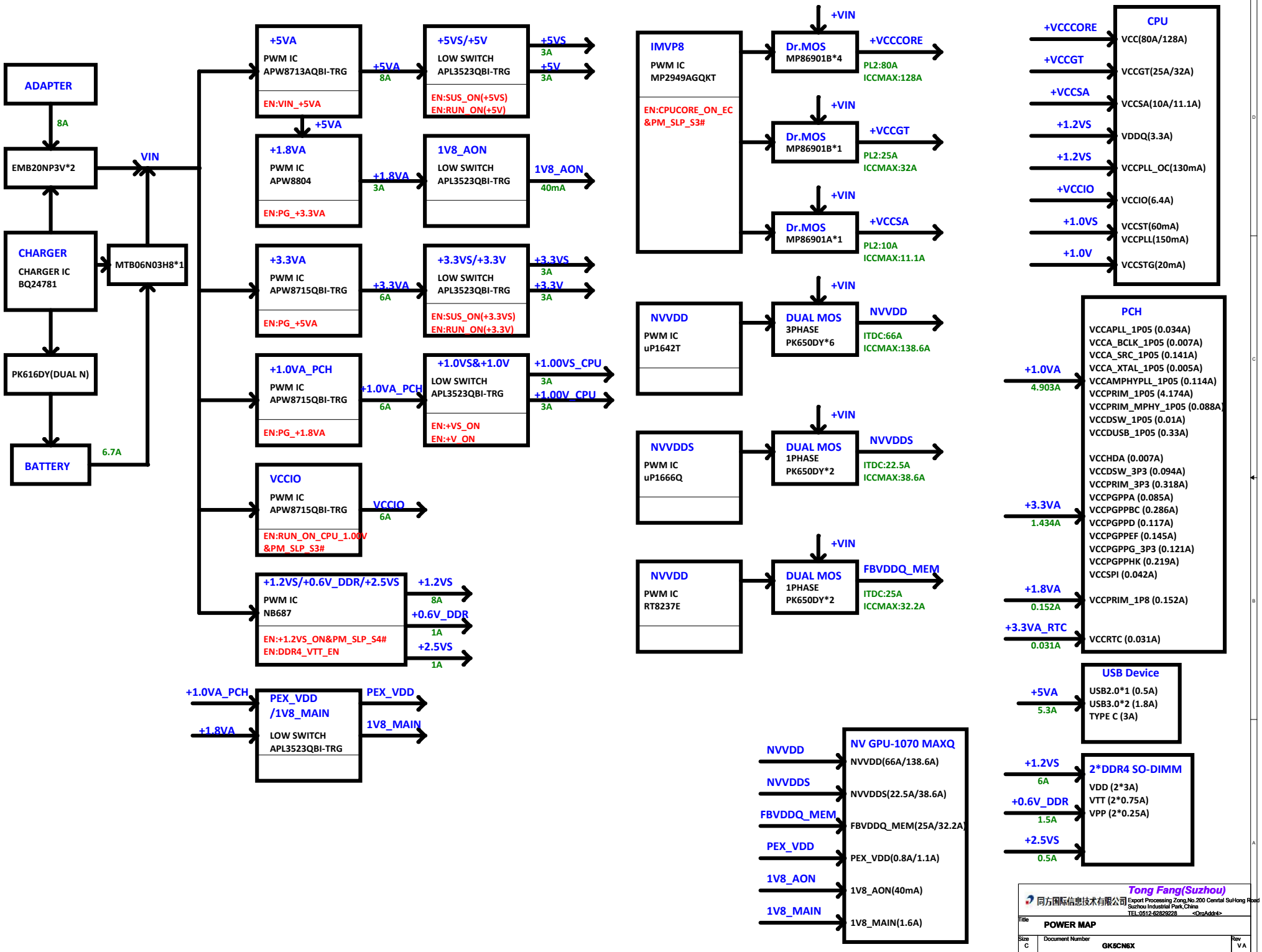

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Title	POWER MAP	
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GPP_F21	PCH_BL_PWM	DEL
GPP_F20	T/P LED_PWM	
GPP_F19	PWM_KB BLUE	
GPA3	PWM_KB RED	
GPA4	PID_1 CHG_R_LED	
GPA5	PID_2 PWR_LED	
GPA6	ME_KB_LED	
GPA7	Board ID	

GH5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R_LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	ME_KB_LED	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	EG_DA	
GPE2	EG_Cycle start	
GPE3	EG_CLK	
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	PANEL_VCC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC remove	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3		Dn/GPI/ID3
GPH4		Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6		Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	PANEL_DETECT	/GPI/Z
GPI2	PCIE_WAKE#	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

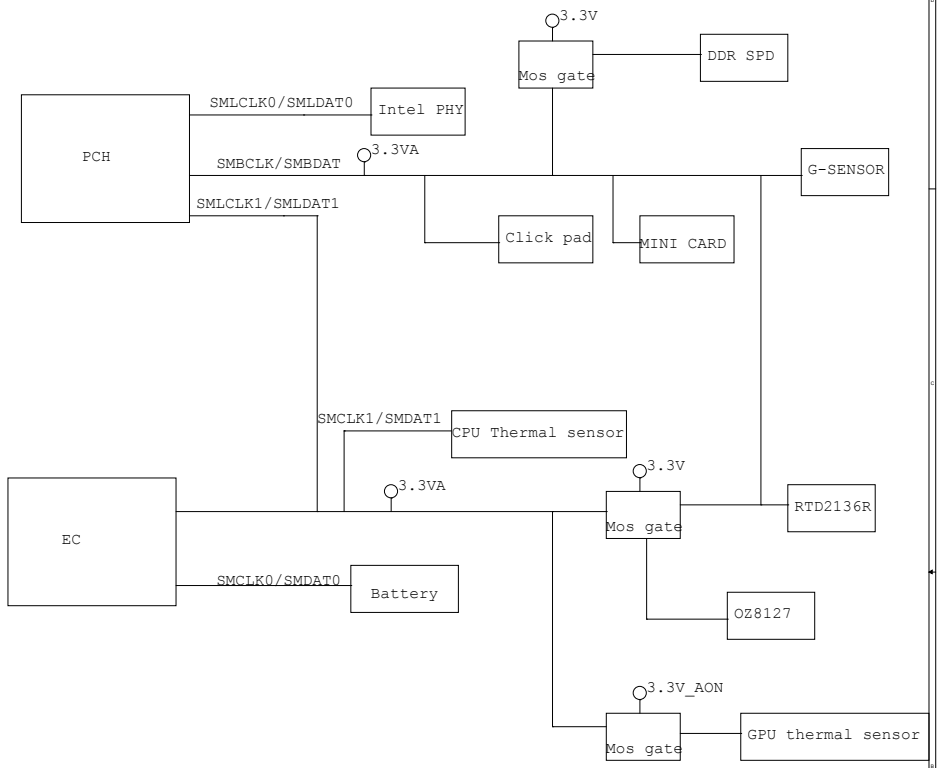
GI5KN

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R_LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	PM_RSMRST#	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / GPI
GPB4	BAT_SMBDAT	Z / GPI
GPB5	H_A20GATE	Z / GPO
GPB6	H_RCIN#	UP / GPI
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	LAN_PWR	Dn / GPI
GPC1	SMBCLK_EC	Z / GPI
GPC2	SMBDAT_EC	Z / GPI
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	Boost FAN_EN1	Dn / GPO
GPC7	+2.5VS_ON	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	ME_WE#	UP / GPO
GPD6	FAN0_detect	Dn / GPO
GPD7	FAN1_detect	Dn / GPO
GPE0	LID#	Dn / GPI
GPE1	+1.2VS_ON	Dn / GPI
GPE2	PWR_USB#	Dn / GPO
GPE3	EXT_WIFI_ON	Dn / GPO
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	DGPU_EN_EC	UP / GPO
GPF1	PCH_PWROK	UP / GPI
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	RUN_ON	UP / GPI
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC remove	Dn/GPO/ID7
GPG2	CPUCORE_ON	Z/ GPO
GPG6	WEBCAM_ON/SUS_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PCH_BL_EN	Dn/GPO/ID1
GPH2	ID_DET	Dn/GPI/ID2
GPH3	DGPU_EN_EC_Keep	Dn/GPI/ID3
GPH4	Dgpu_RST_EC#	Dn/GPI/ID4
GPH5	HYB_ON#	Dn/GPI/ID5
GPH6	Clear CMOS	Dn/GPI/ID6
GPI0	Boost FAN_EN	/GPI/Z
GPI1	EC_OVERT_NVVDD#	/GPI/Z
GPI2	PCIE_WAKE#/Dgpu_RST_EC#_keep	/GPI/Z
GPI3	FAN_enable1	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT	/GPOI/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	/GPI/Z
GPM1	LPC_AD1	/GPI/Z
GPM2	LPC_AD2	/GPI/Z
GPM3	LPC_AD3	/GPI/Z
GPM4	CLK_EC_LPC	/GPI/Z
GPM5	LPC_FRAME#	/GPI/Z
GPM6	INT_SERIRQ	/GPI/Z

EXT EC

ITE8302 GPIO		Default Pull/Mode
GPIO4	EXT_WIFI_ON	UP / GPO
GPIO5	EC_OVERT_NVVDD#	UP / GPO
GPIO7	Dgpu_RST_EC#_keep	UP / GPO
GPIO9	SUS_ON	UP / GPO
GPIO11	CTL3	UP / GPO
GPIO13	CTL2	UP / GPO
GPIO18	EXT_Q_key0	UP / GPO
GPIO20	EXT_Q_key1	UP / GPO
GPIO22	PWR_USB#	UP / GPI
GPIO24	+1.2VS_ON	UP / GPI
GPIO26	LID1#	Dn / GPI
GPIO27	Dgpu_RST_EC#	Z / GPI
GPIO29	PM_RSMRST#	Z / GPI
GPIO31	DGPU_EN_EC_Keep	Z / GPO
GPIO33	DGPU_EN_EC	UP / GPI
GPIO35	Clear CMOS	Dn / GPI

SMBUS BLOCK



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Title: GPIO & SMBUS Block

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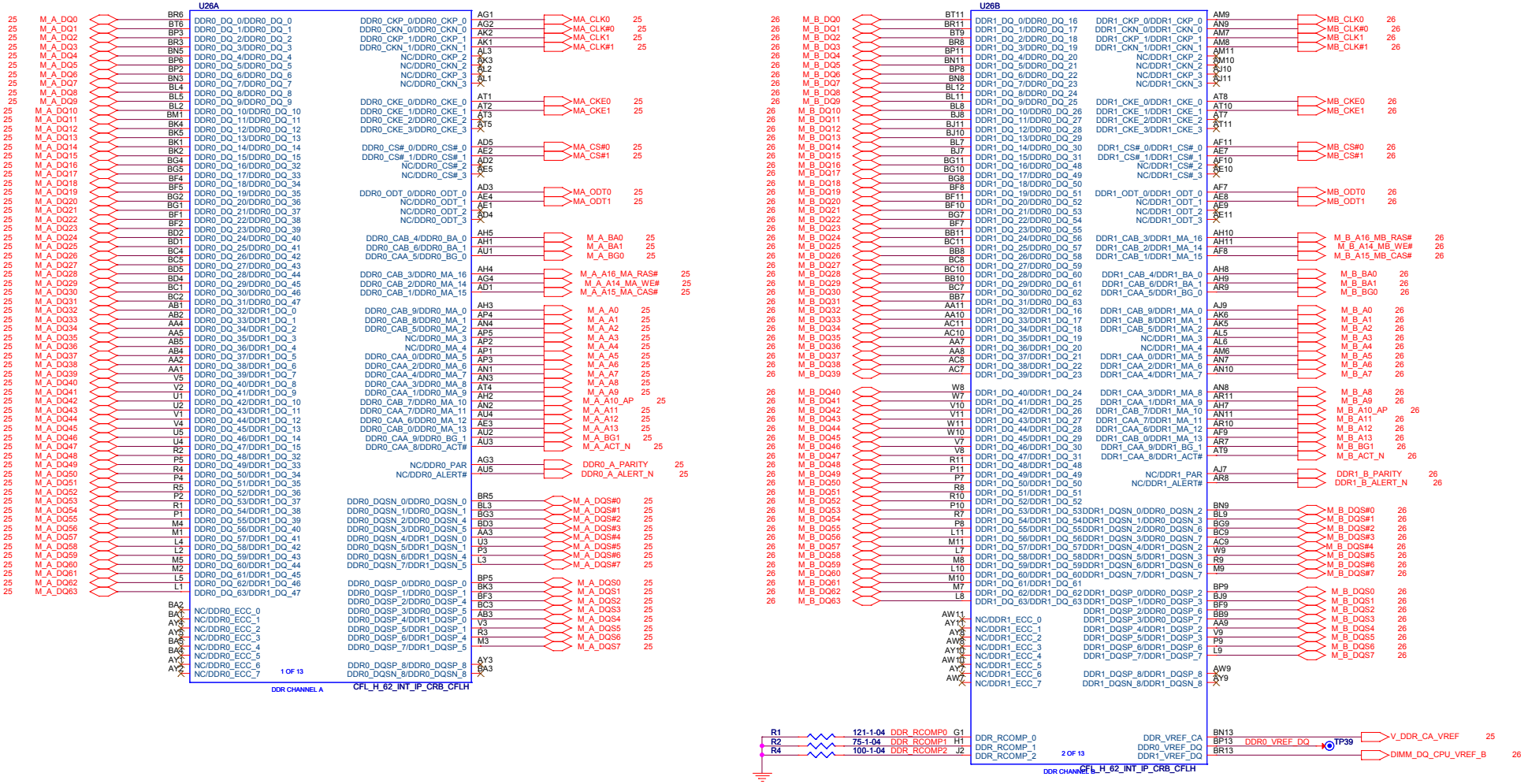

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Title: CPU CFL-H : DDR4 CH-A/CH-B

Size	Document Number	Rev
Custom	GK5CN6X	V A

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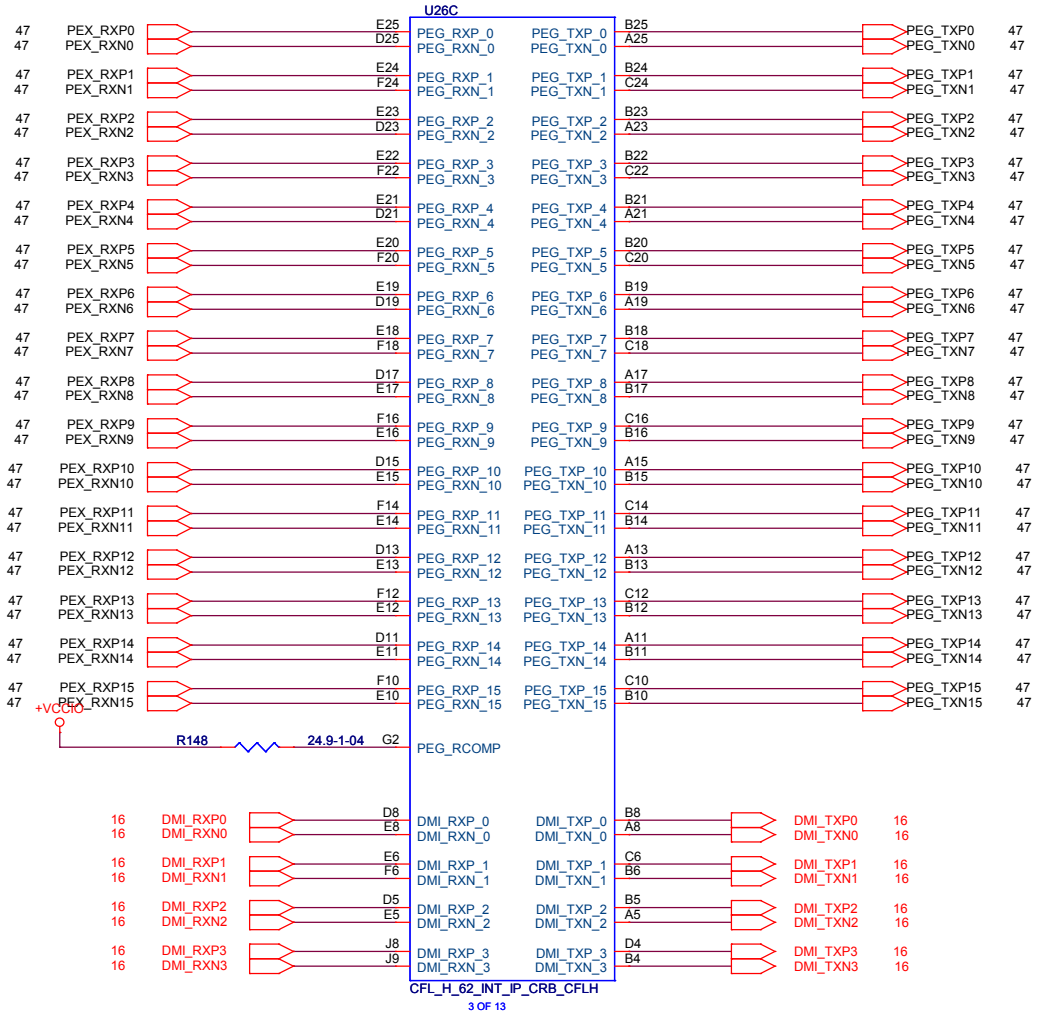

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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Title	CPU CFL-H : PEG/DMI		
Size B	Document Number GK5CN6X		Rev V A
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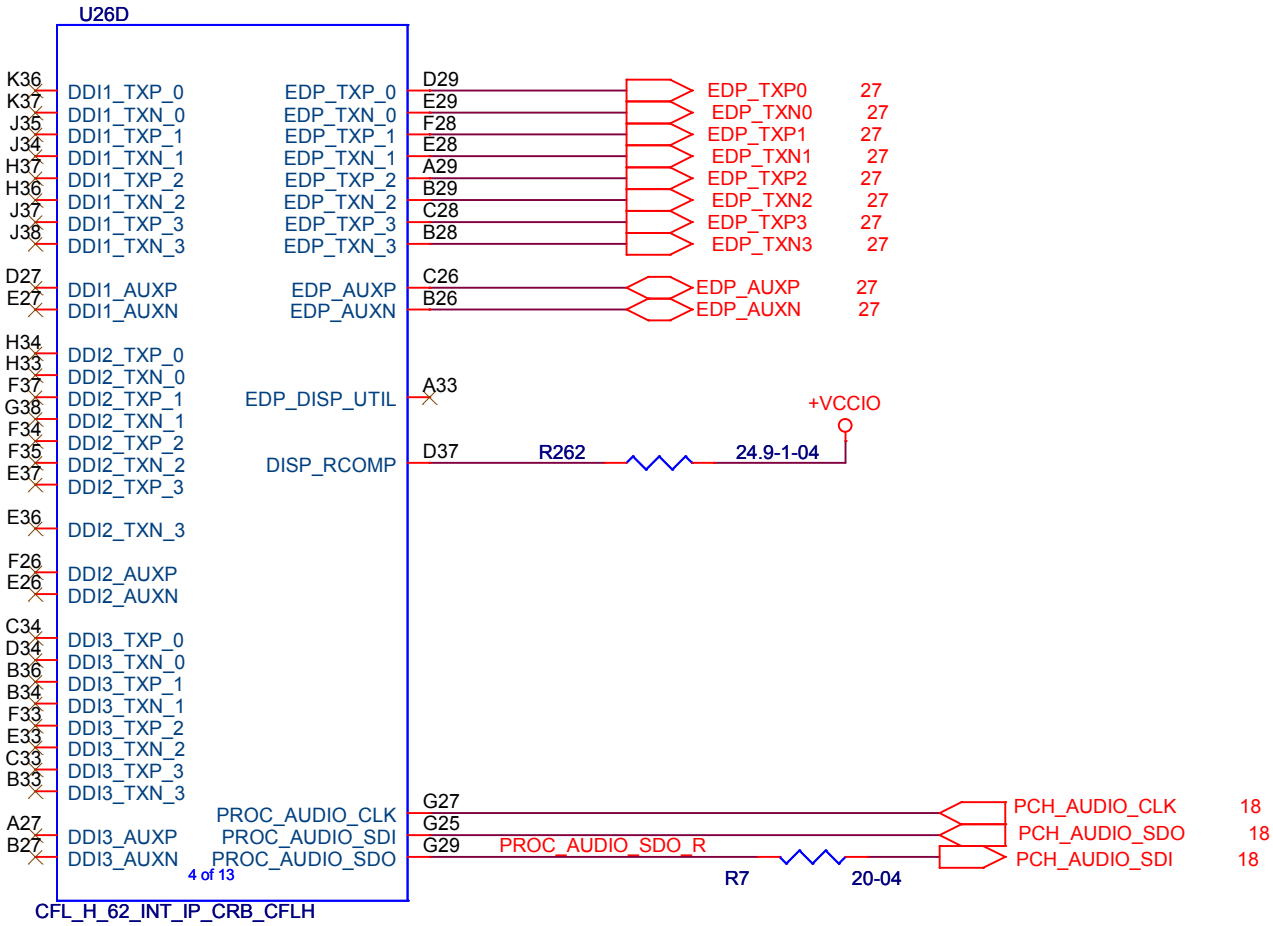

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Title	CPU CFL-H : DDI/EDP	
Size A	Document Number GK5CN6X	Rev V A
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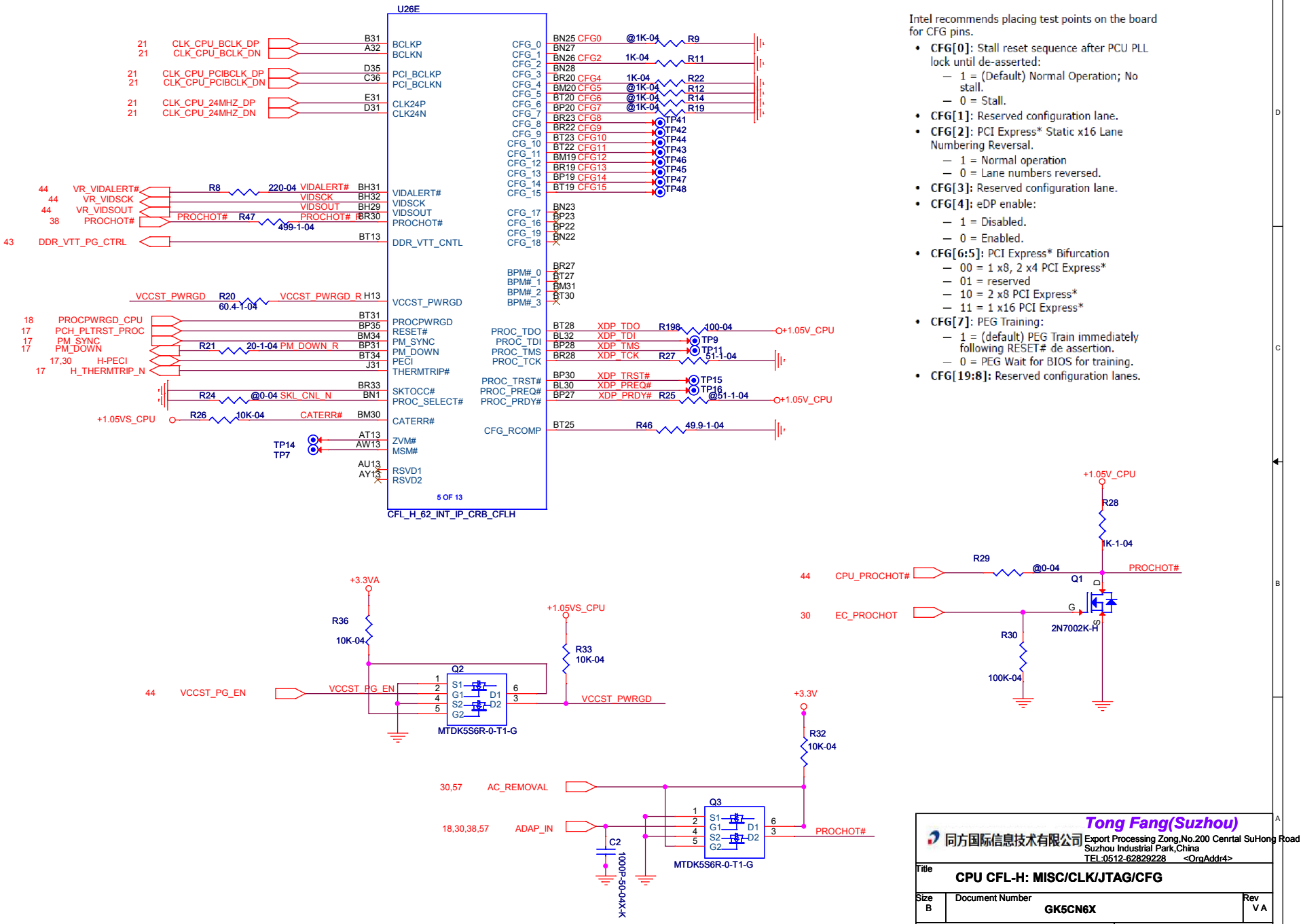

Intel recommends placing test points on the board for CFG pins.

- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

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Title	CPU CFL-H: MISC/CLK/JTAG/CFG	
Size B	Document Number GK5CN6X	Rev V A
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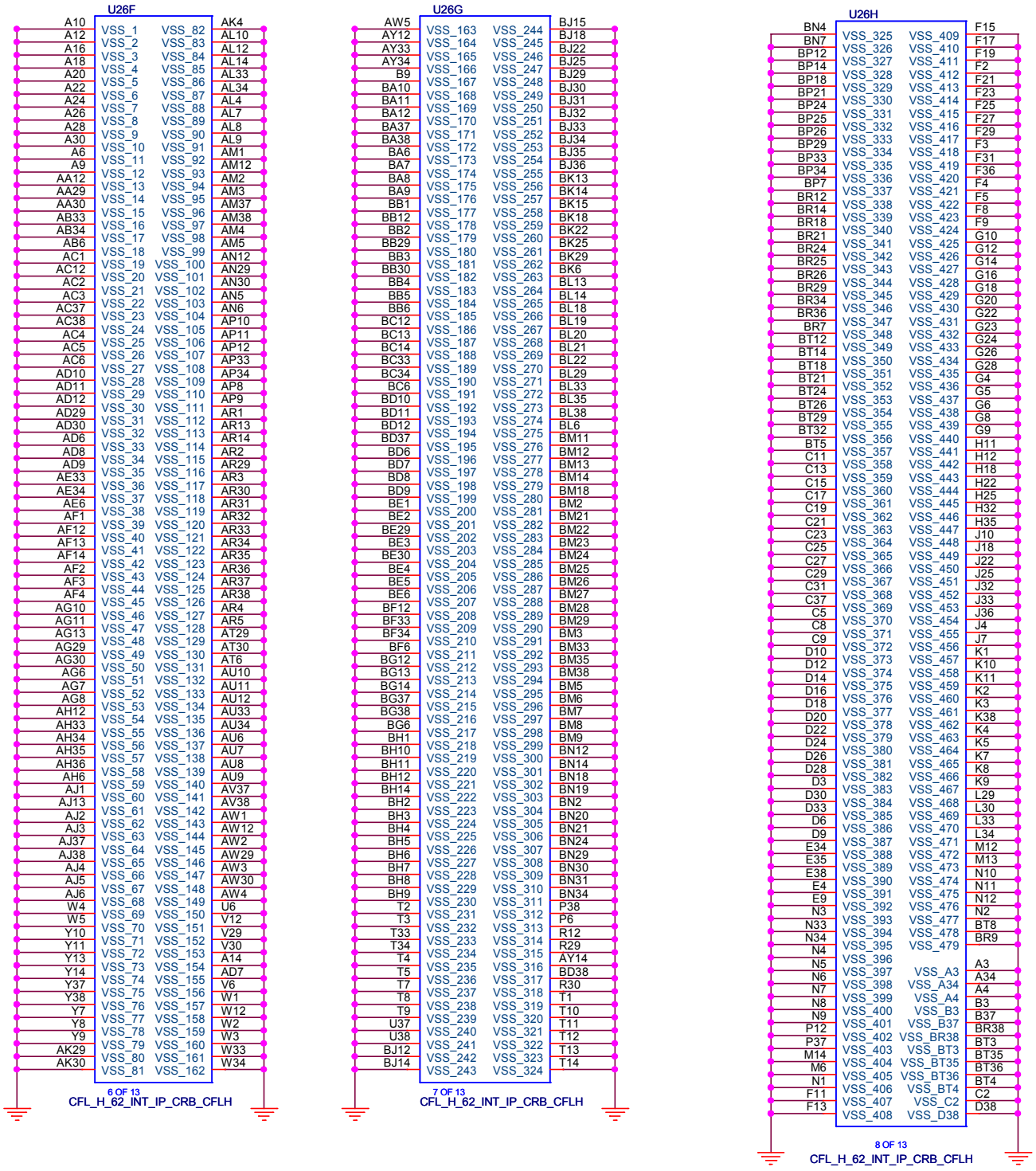

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Title	CPU CFL-H : GND	
Size: Custom	Document Number: GK5CN6X	Rev: V A
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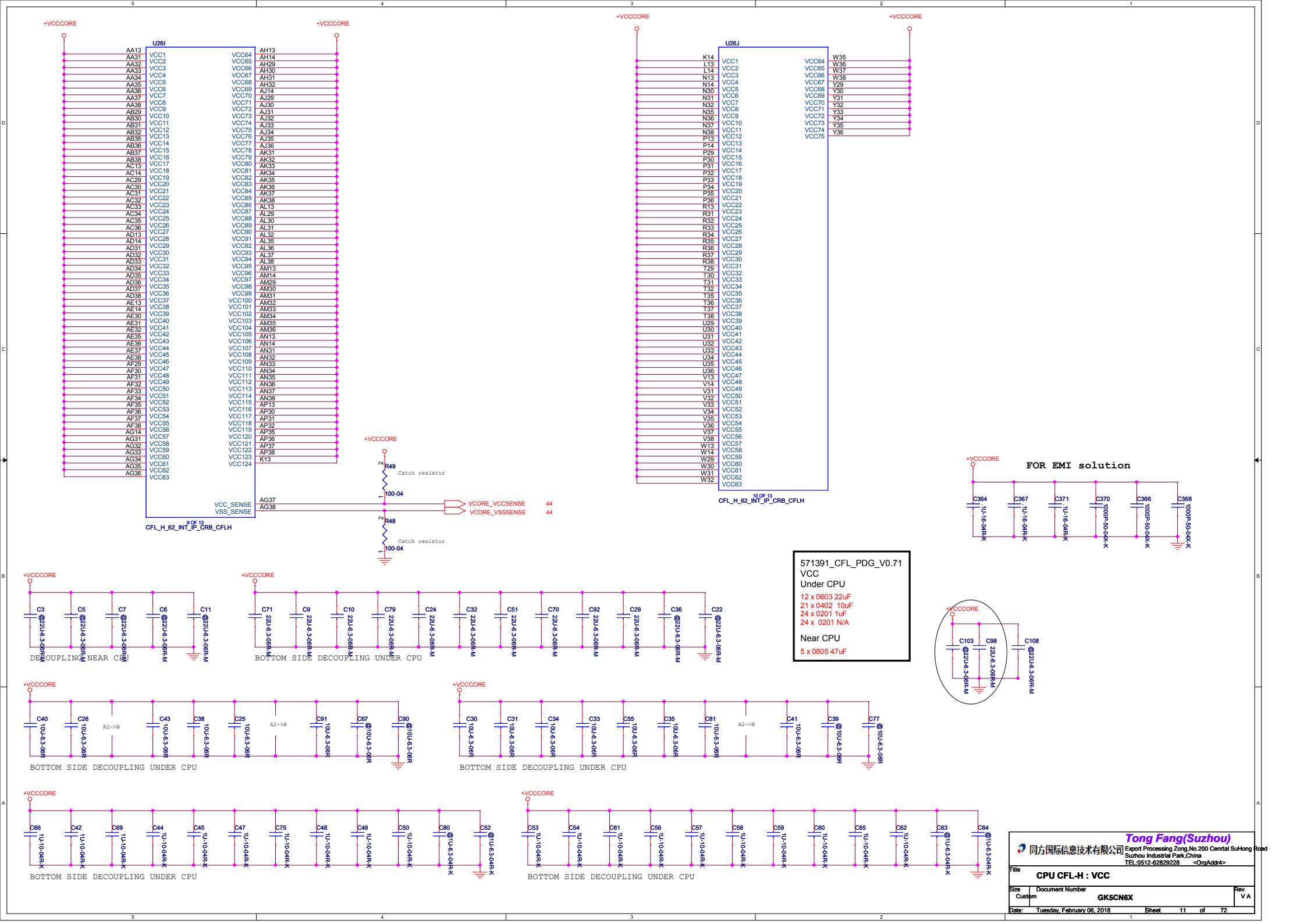

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Title	CPU CFL-H : VCC	
Size: Custom	Document Number: GK5CN6X	Rev: V A
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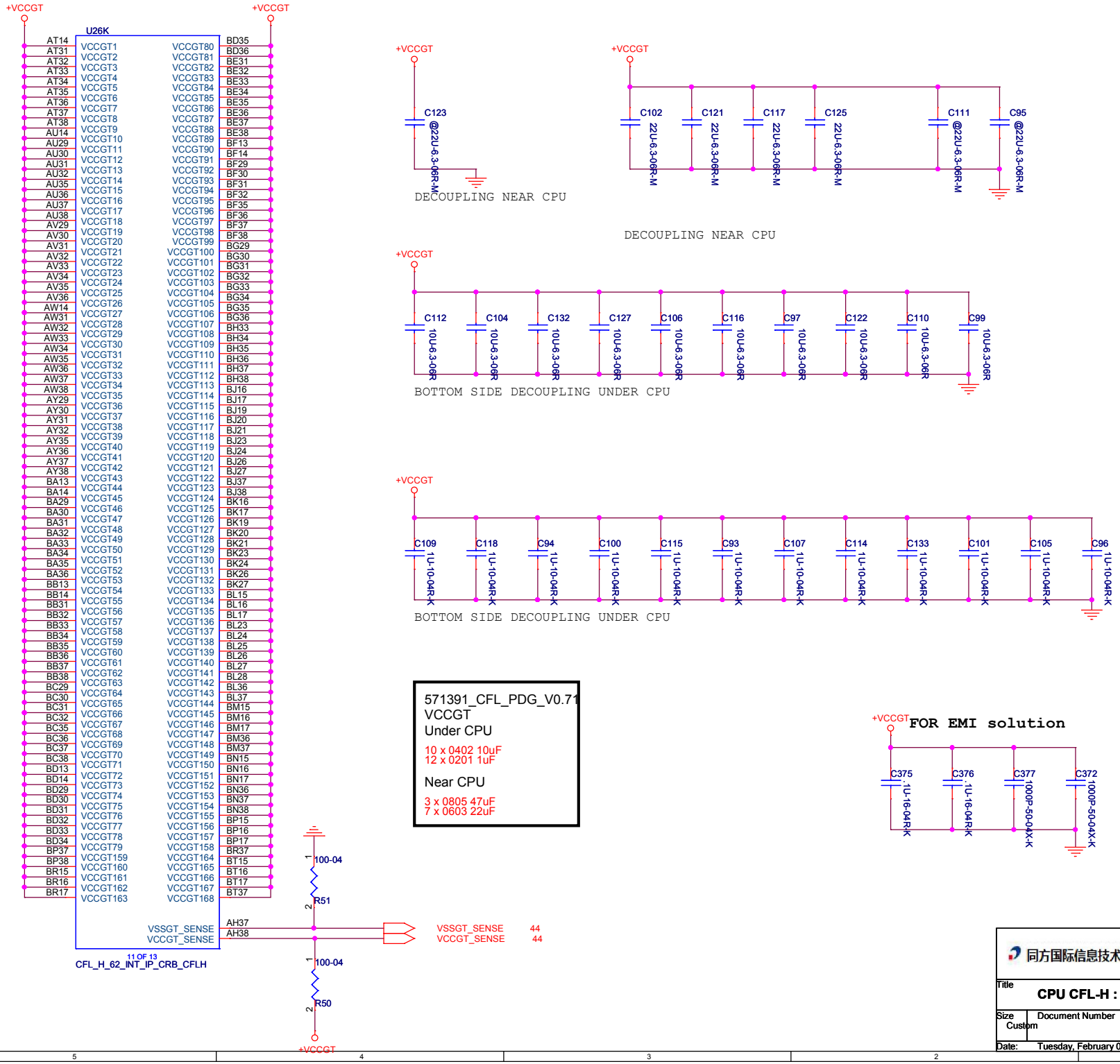

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Title	CPU CFL-H : VCCGT	
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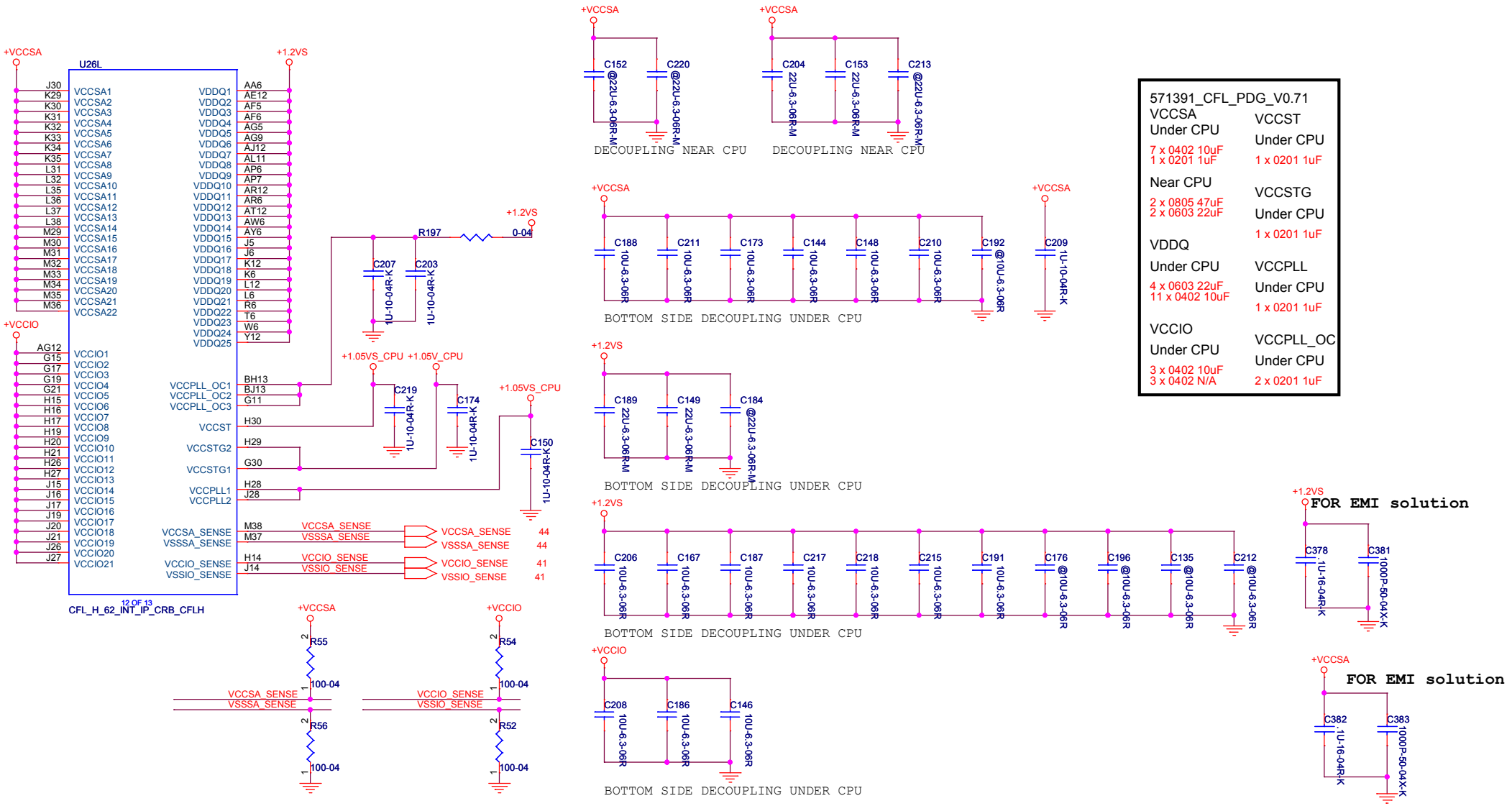

571391_CFL_PDG_V0.71

VCCSA Under CPU	VCCST Under CPU
7 x 0402 10uF 1 x 0201 1uF	1 x 0201 1uF
Near CPU	VCCSTG Under CPU
2 x 0805 47uF 2 x 0603 22uF	1 x 0201 1uF
VDDQ Under CPU	VCCPLL Under CPU
4 x 0603 22uF 11 x 0402 10uF	1 x 0201 1uF
VCCIO Under CPU	VCCPLL_OC Under CPU
3 x 0402 10uF 3 x 0402 N/A	2 x 0201 1uF

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Title	CPU CFL-H : VCCSA/VCCIO/VDDQ	
Size B	Document Number GK5CN6X	Rev V A
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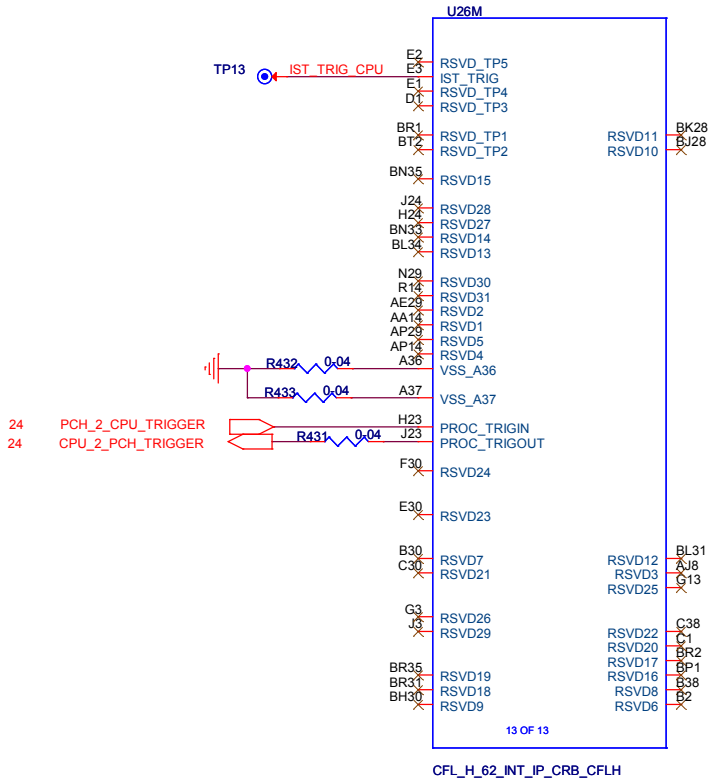

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Title	CPU CFL-H : TRIG/RSVD	
Size B	Document Number GK5CN6X	Rev V A
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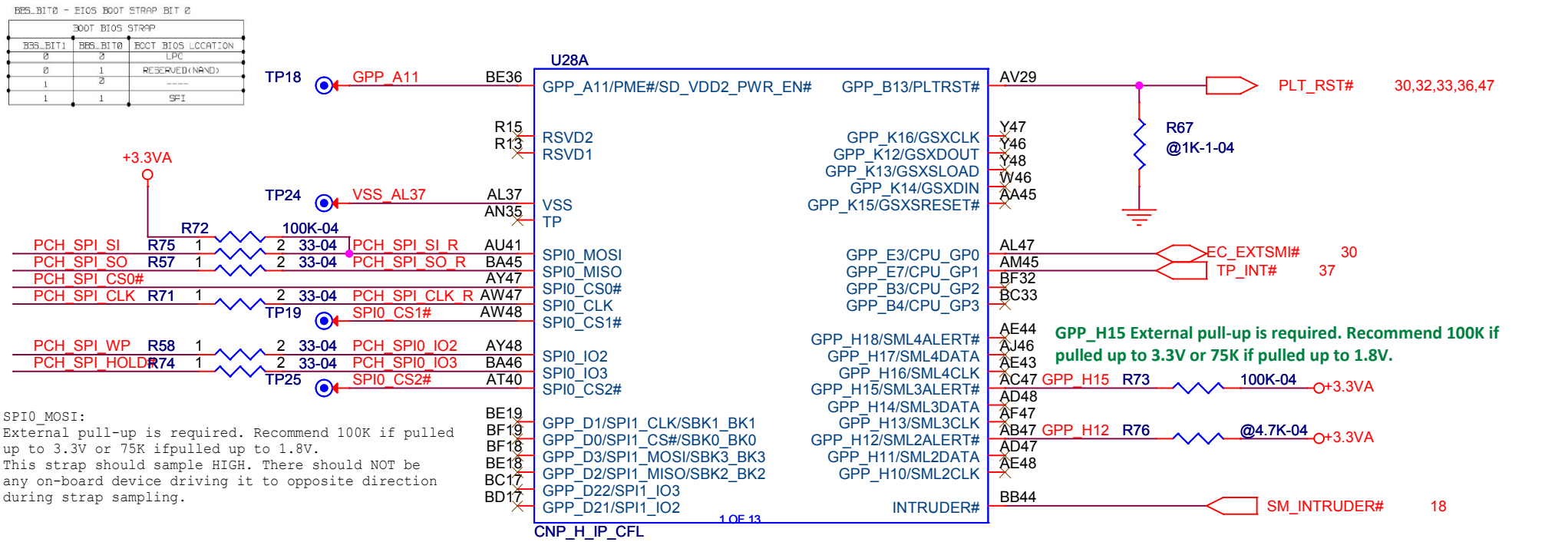
BBS_BIT0 - BIOS BOOT STRAP BIT 0

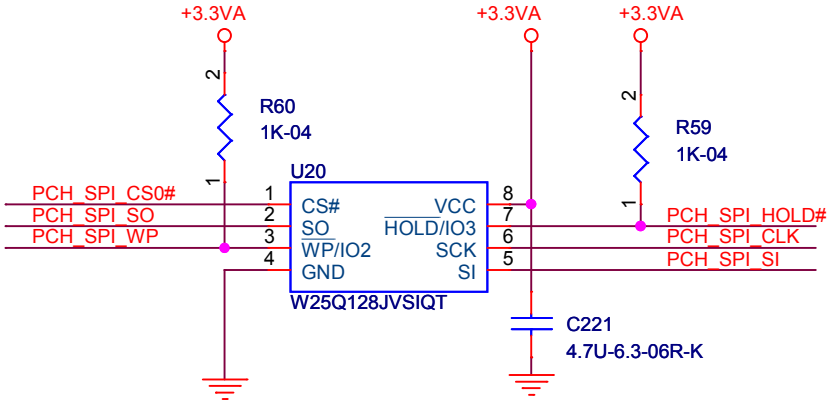
BOOT BIOS STRAP		
BBS_BIT1	BBS_BIT0	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	-----
1	1	SPI



SPI0_MOSI:
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K ifpulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_H15 External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

GPP_H12 eSPI Flash Sharing Mode
0:Master Attached Flash Sharing (MAFS) enabled (internal pull down)
1:Slave Attached Flash Sharing (SAFS) enabled



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Title: PCH CFL-H : SPI

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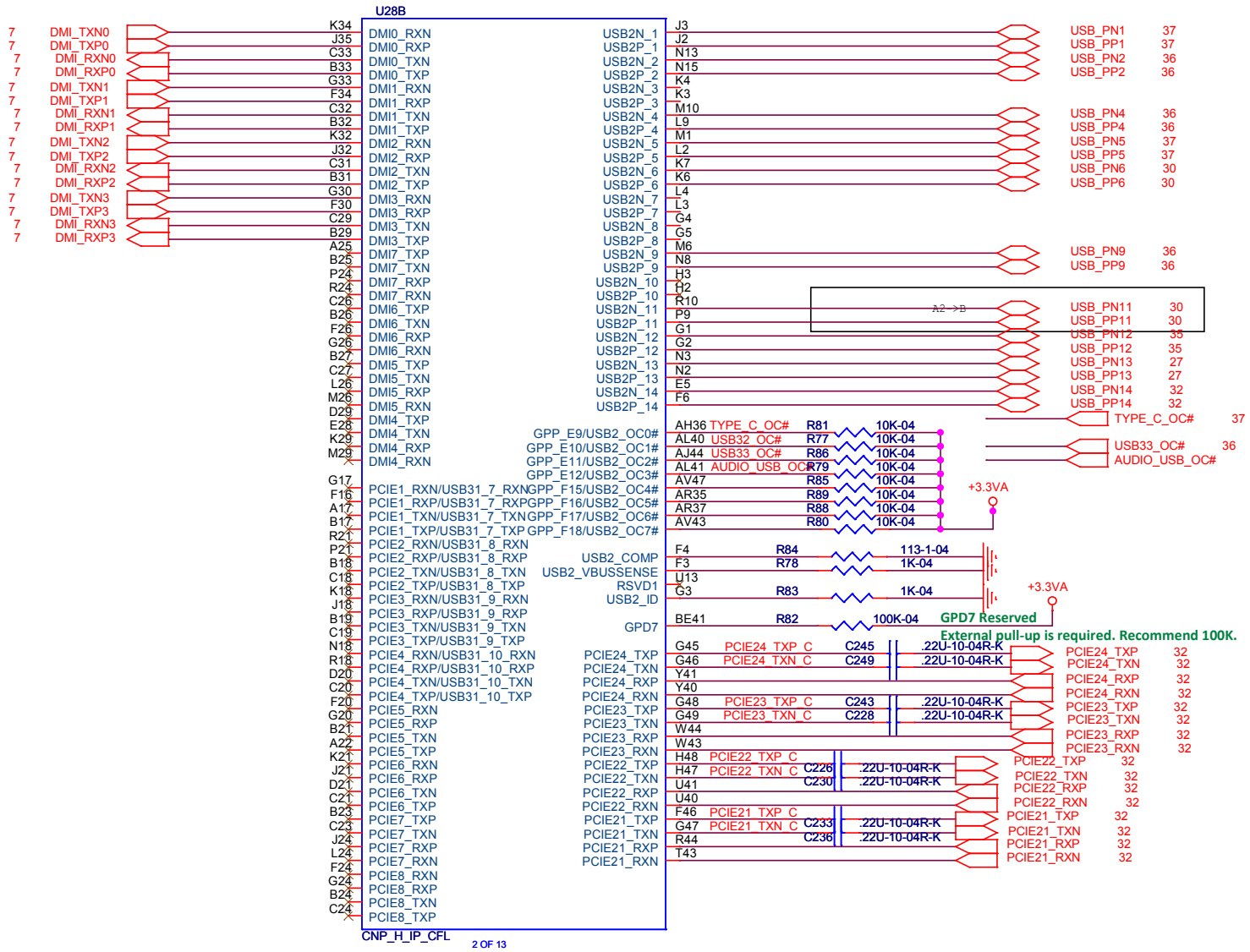

USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	N/A
USB11	USB3.0 Port1 on USB3.0 DB
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

USB OC Configuration Table	
OC0	TYPE_C_OC#
OC1	N/A
OC2	USB3.0 DB
OC3	AUDIO_USB DB
OC4	N/A
OC5	N/A
OC6	N/A
OC7	N/A

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Title: PCH CFL-H : DMI/USB2.0

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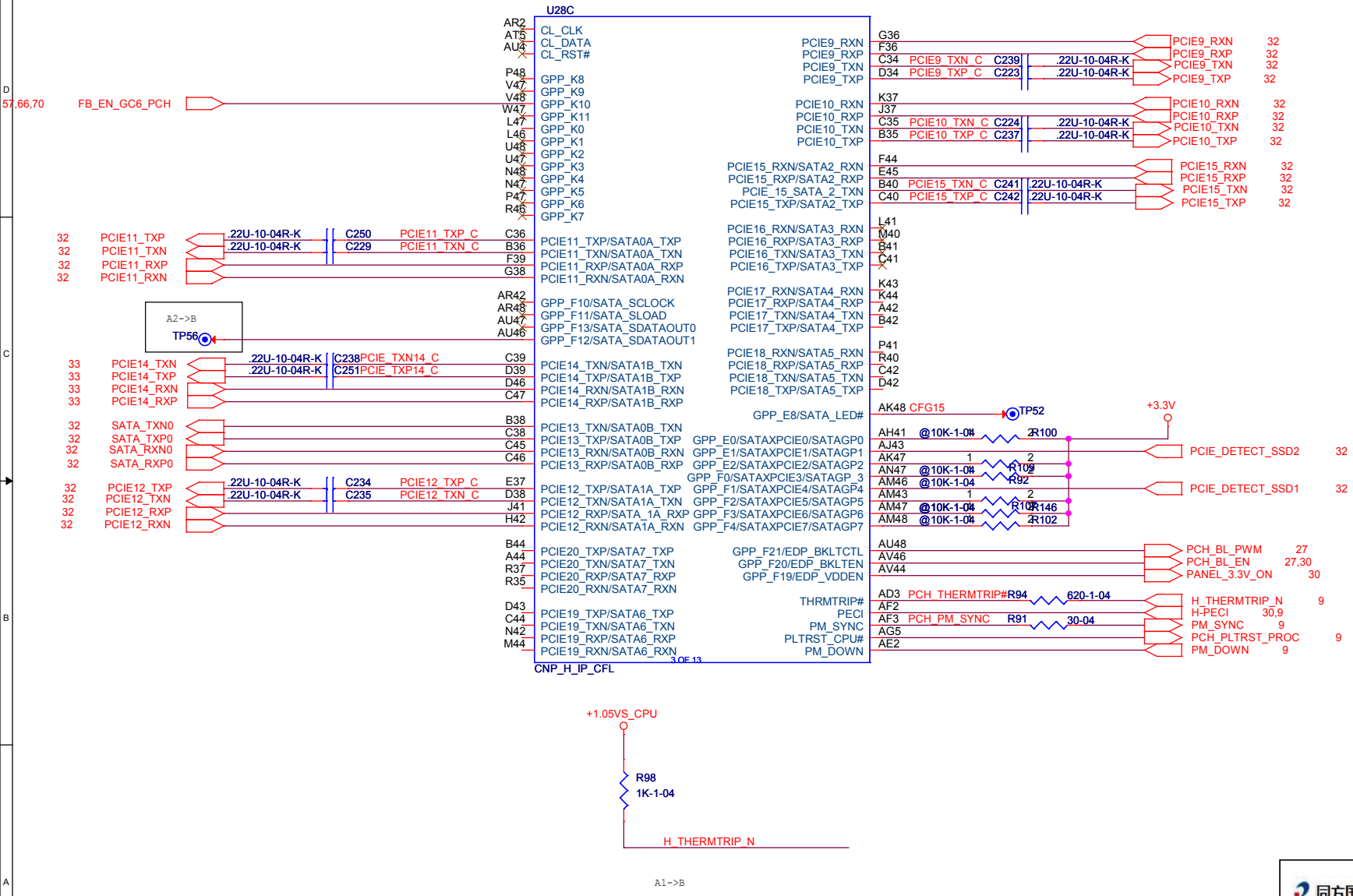

PCIE Configuration Table			
PCIE1	No function	PCIE13	SATA HDD
PCIE2	No function	PCIE14	LAN
PCIE3	No function	PCIE15	WLAN
PCIE4	No function	PCIE16	N/A
PCIE5	N/A	PCIE17	PCIE SSD1
PCIE6	N/A	PCIE18	PCIE SSD1
PCIE7	No function	PCIE19	PCIE SSD1
PCIE8	No function	PCIE20	PCIE SSD1
PCIE9	PCIE SSD2	PCIE21	N/A
PCIE10	PCIE SSD2	PCIE22	N/A
PCIE11	PCIE SSD2	PCIE23	N/A
PCIE12	PCIE SSD2	PCIE24	N/A

SATA Configuration Table	
SATA0	SATA HDD
SATA1	SATA SSD2
SATA2	No Function
SATA3	No Function
SATA4	SATA SSD1
SATA5	N/A
SATA6	No Function
SATA7	No Function

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Title: PCH CFL-H : SATA/PCIE

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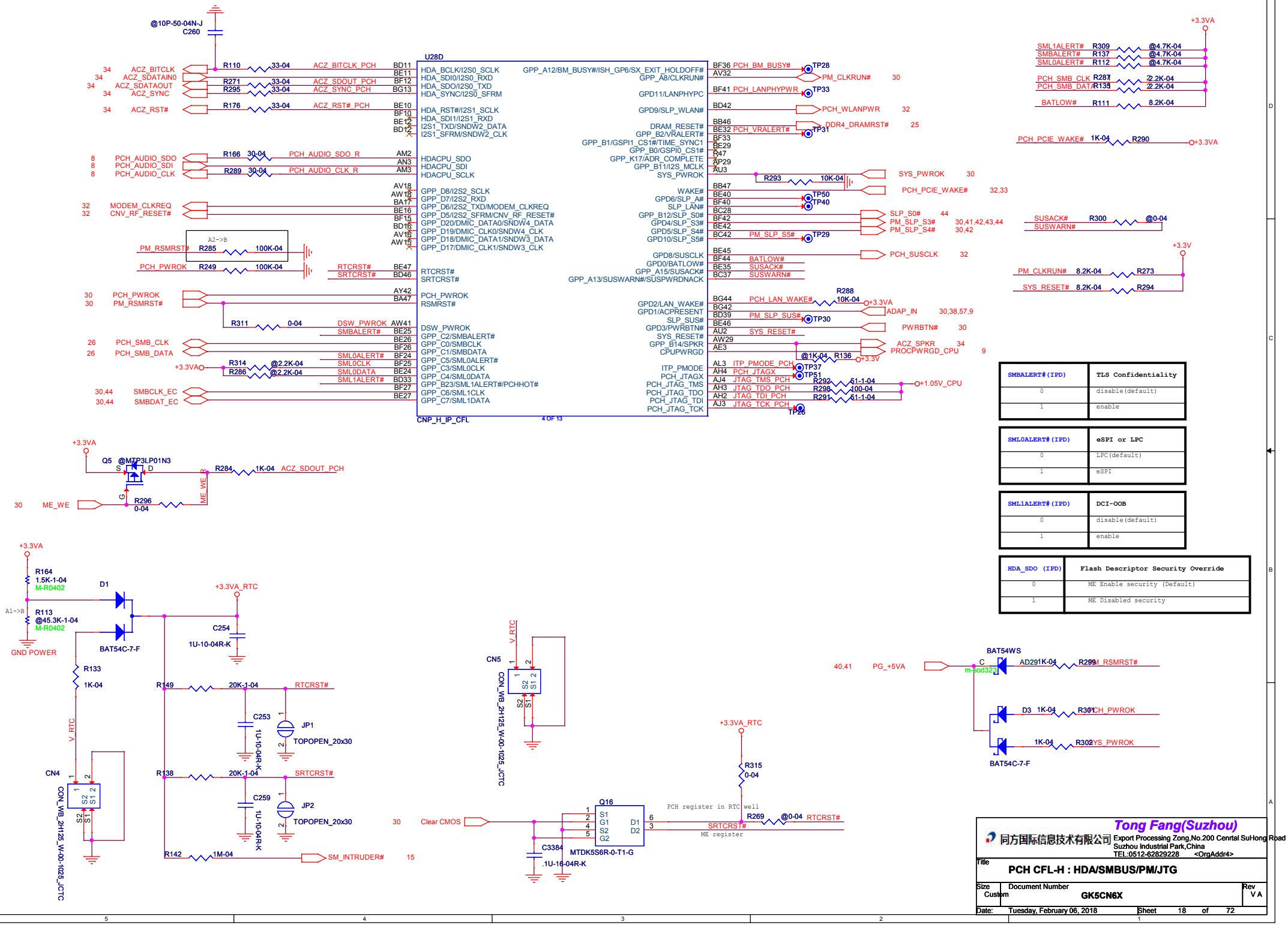
U28D
CNP_H_IP_CFL
4 OF 13
@10P-50-04N-J
C260
R110 33-04 ACZ_BITCLK_PCH
R271 33-04 ACZ_SDOUT_PCH
R295 33-04 ACZ_SYNC_PCH
R176 33-04 ACZ_RST#_PCH
R166 30-04 PCH_AUDIO_SDO_R
R289 30-04 PCH_AUDIO_CLK_R
R285 100K-04
R249 100K-04
R311 0-04
R314 @2.2K-04
R286 @2.2K-04
R293 10K-04
R288 10K-04
R136 @1K-04
R284 1K-04 ACZ_SDOUT_PCH
R296 0-04
TP28
TP33
TP31
TP50
TP40
TP29
TP30
TP37
TP51
TP26
R292 51-1-04
R298 100-04
R291 51-1-04
+1.05V_CPU
+3.3VA
+3.3V
SML1ALERT# R309 @4.7K-04
SMBALERT# R137 @4.7K-04
SML0ALERT# R112 @4.7K-04
PCH_SMB_CLK R287 2.2K-04
PCH_SMB_DATA R135 2.2K-04
BATLOW# R111 8.2K-04
PCH_PCIE_WAKE# 1K-04 R290
SUSACK# R300 @0-04
SUSWARN#
PM_CLKRUN# 8.2K-04 R273
SYS_RESET# 8.2K-04 R294
SMBALERT# (IPD) TLS Confidentiality
0 disable(default)
1 enable
SML0ALERT# (IPD) eSPI or LPC
0 LPC(default)
1 eSPI
SML1ALERT# (IPD) DCI-OOB
0 disable(default)
1 enable
HDA_SDO (IPD) Flash Descriptor Security Override
0 ME Enable security (Default)
1 ME Disabled security
Q5 @MTP3LP01N3
R164 1.5K-1-04 M-R0402
R113 @45.3K-1-04 M-R0402
D1
BAT54C-7-F
GND POWER
+3.3VA_RTC
C254 1U-10-04R-K
R133 1K-04
R149 20K-1-04 RTCRST#
C253 1U-10-04R-K
JP1 TOPOPEN_20x30
R138 20K-1-04 SRTCRST#
C259 1U-10-04R-K
JP2 TOPOPEN_20x30
R142 1M-04 SM_INTRUDER#
CN4
CON_WB_2H125_W-00-1025_JCTC
CN5
CON_WB_2H125_W-00-1025_JCTC
Q16
MTDK5S6R-0-T1-G
C3384 .1U-16-04R-K
Clear CMOS
R315 0-04
R269 @0-04 RTCRST#
PCH register in RTC well
ME register
BAT54WS
D3 1K-04 R301 PCH_PWROK
1K-04 R302 SYS_PWROK
BAT54C-7-F
PG_+5VA
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Title
PCH CFL-H : HDA/SMBUS/PM/JTG
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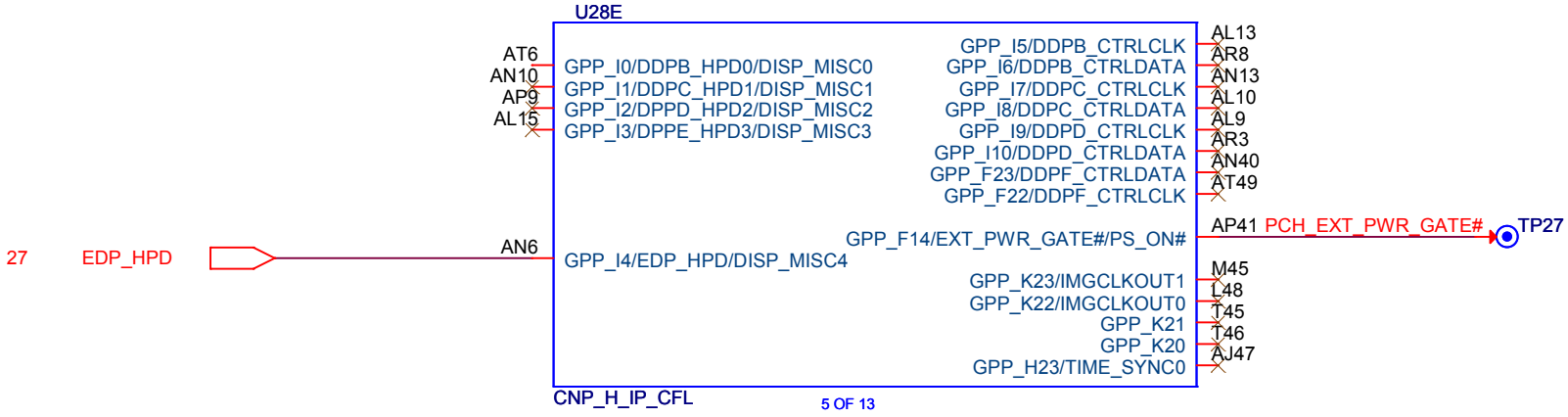

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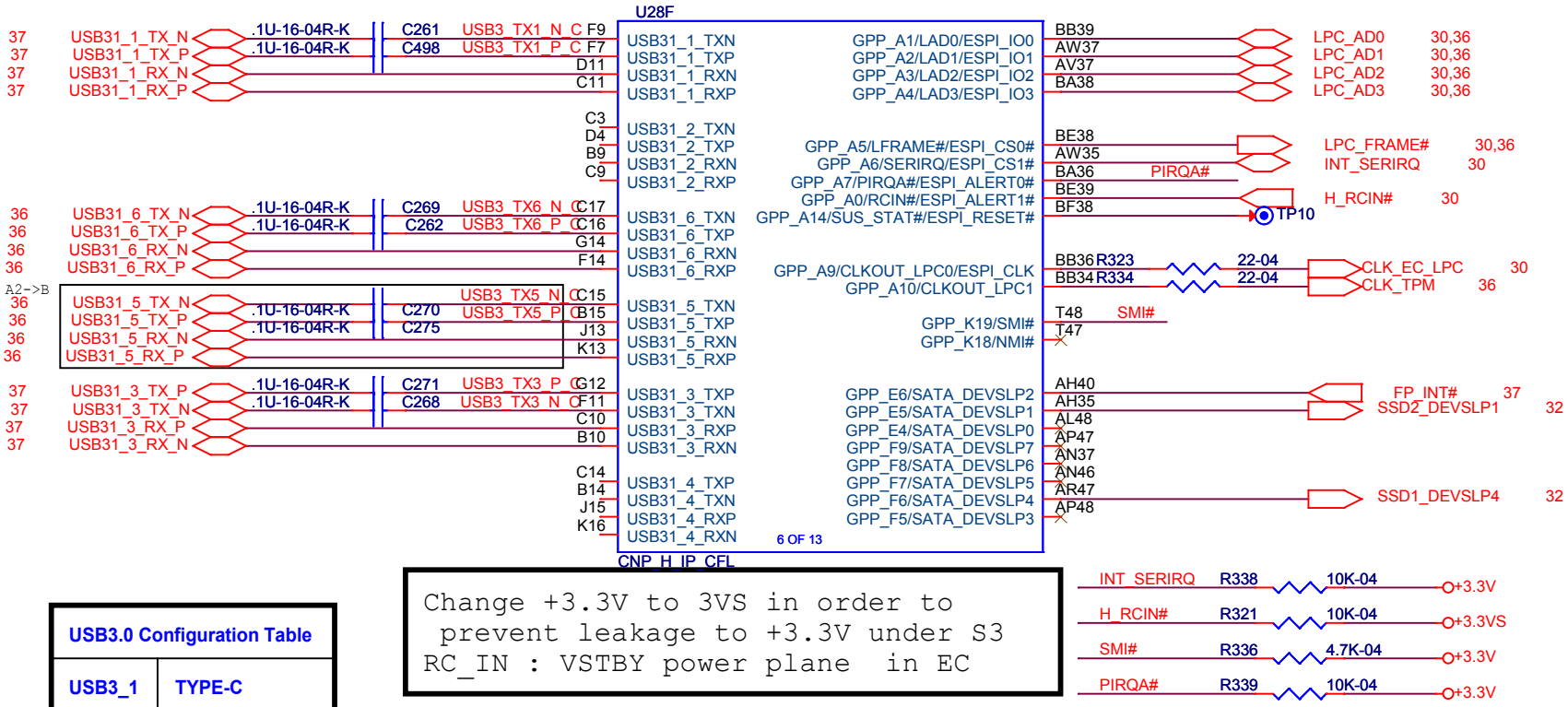

Change +3.3V to 3VS in order to prevent leakage to +3.3V under S3
RC_IN : VSTBY power plane in EC

USB3.0 Configuration Table	
USB3_1	TYPE-C
USB3_2	N/A
USB3_3	TYPE-C
USB3_4	N/A
USB3_5	USB3.0 Port2
USB3_6	USB3.0 Port1
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

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Title: PCH CFL-H : USB3.0/LPC

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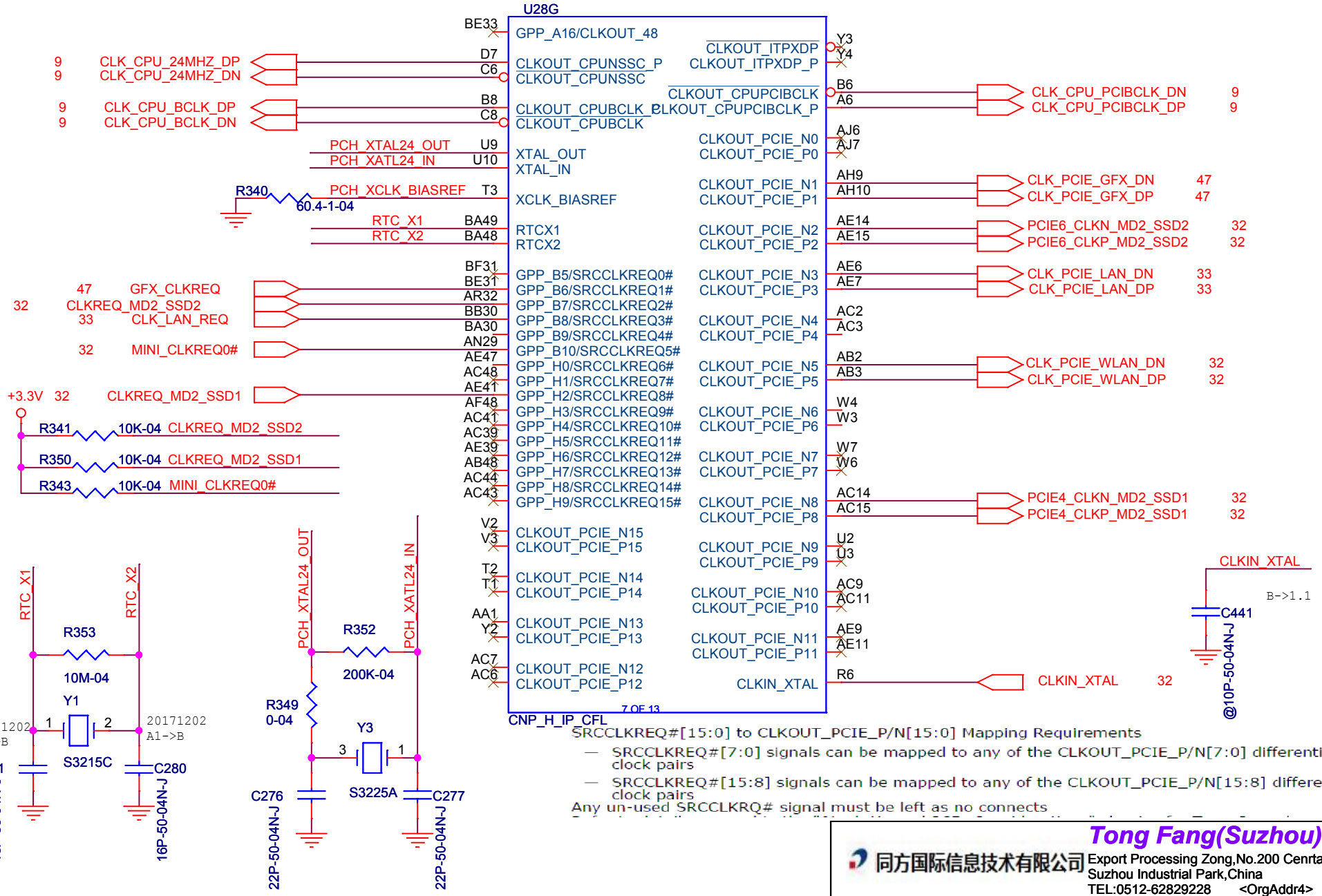

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Title	PCH CFL-H : CLK		
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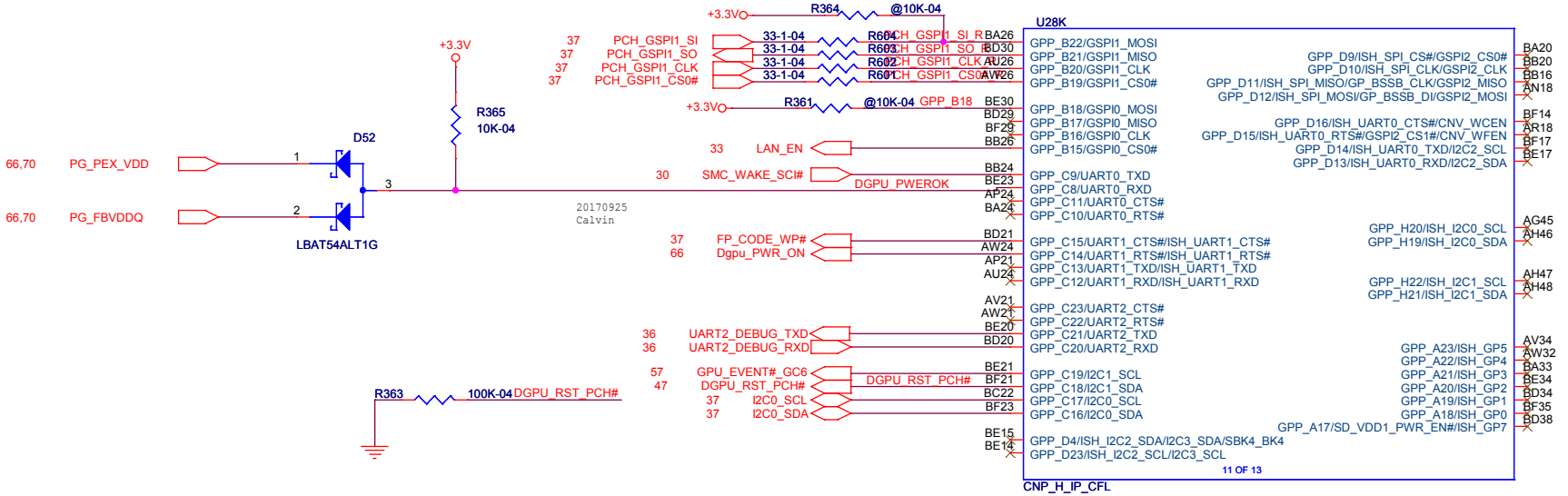
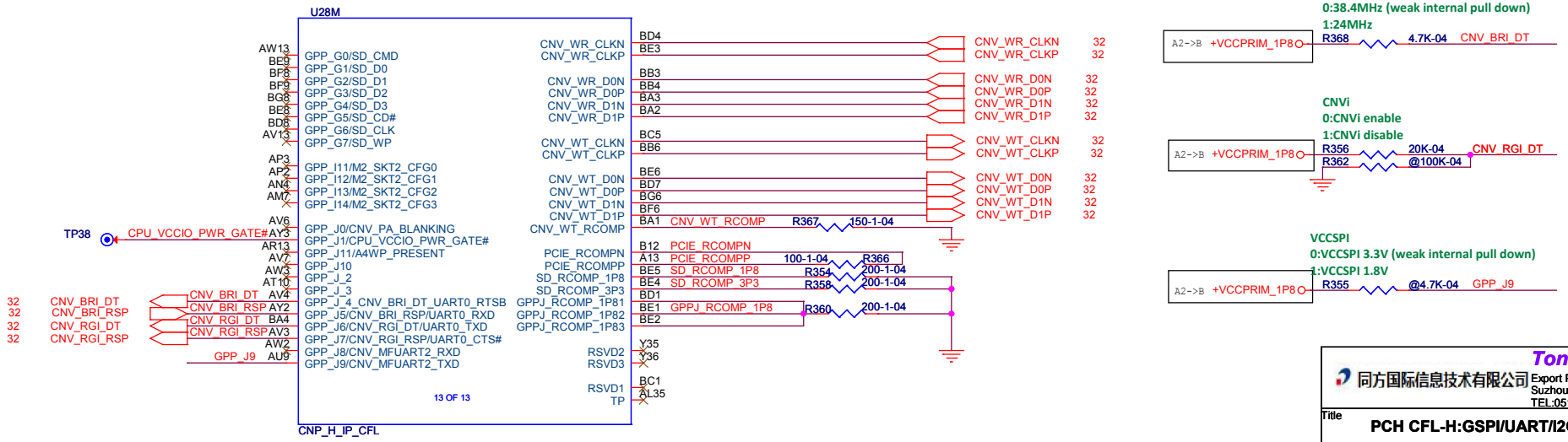
GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Strap Bit
0(weak internal pull down)	SPI
1	LPC

GPP_B18/GSPI0_MOSI(IPD)	No Reboot
0	Disable "No Reboot" mode. (Default)
1	Enable "No Reboot" mode





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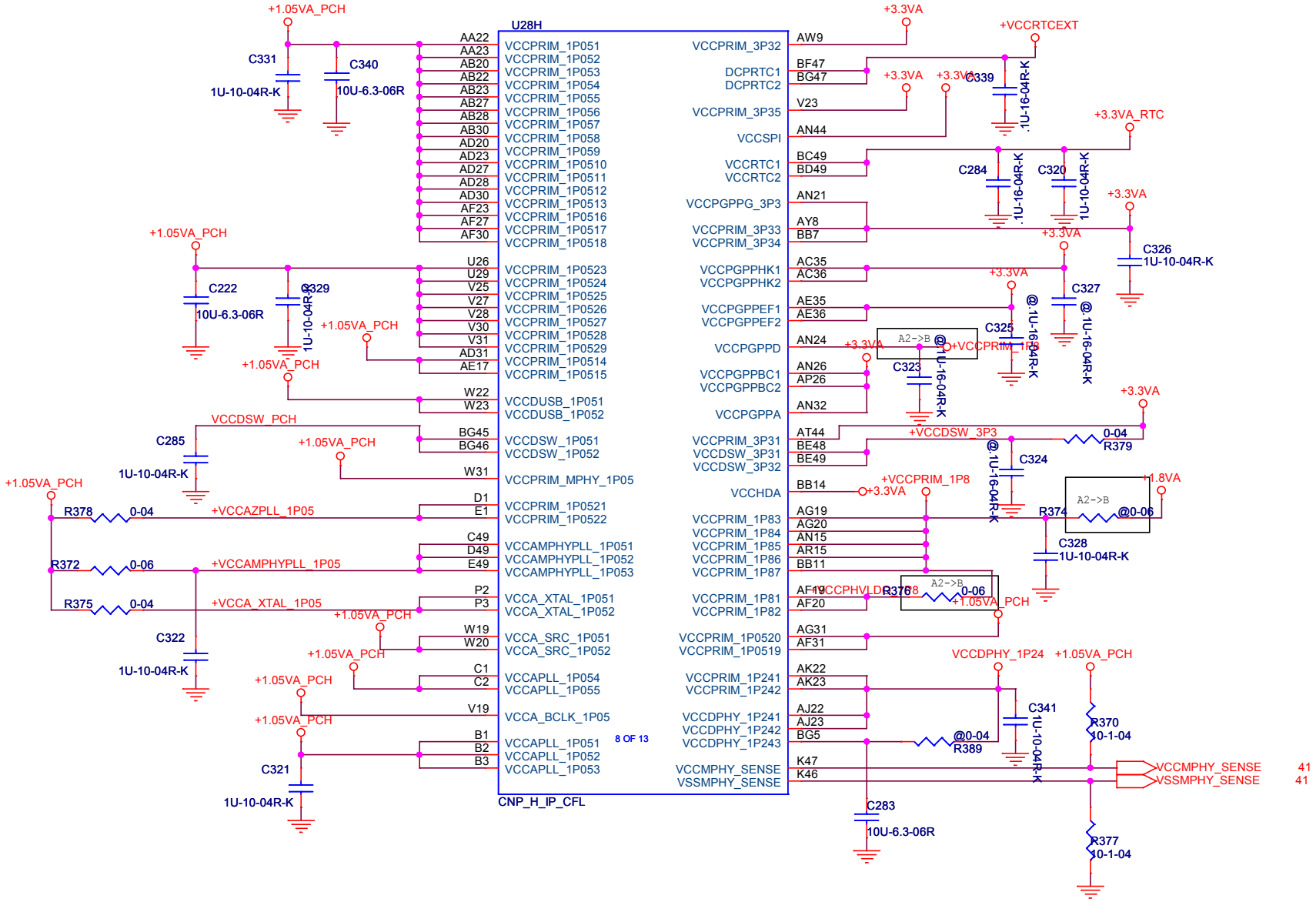
Title	PCH CFL-H:GSPI/UART/I2C/CNVi	
Size B	Document Number GK5CN6X	Rev V A
Date: Tuesday, February 06, 2018	Sheet 22 of 72	



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Title: PCH CFL-H : POWER		
Size: Custom	Document Number: GK5CN6X	Rev: V A
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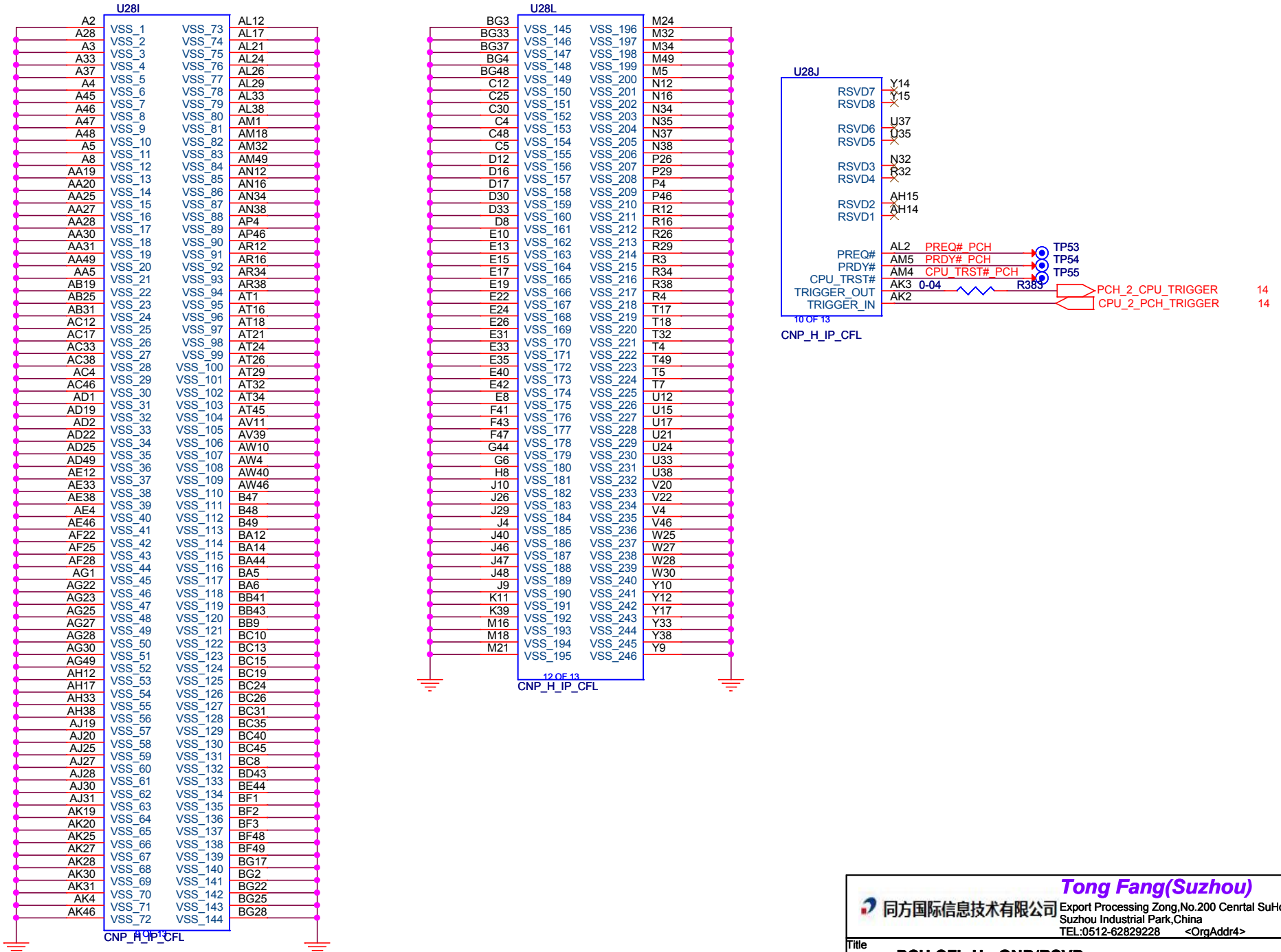

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Title: PCH CFL-H : GND/RSVD

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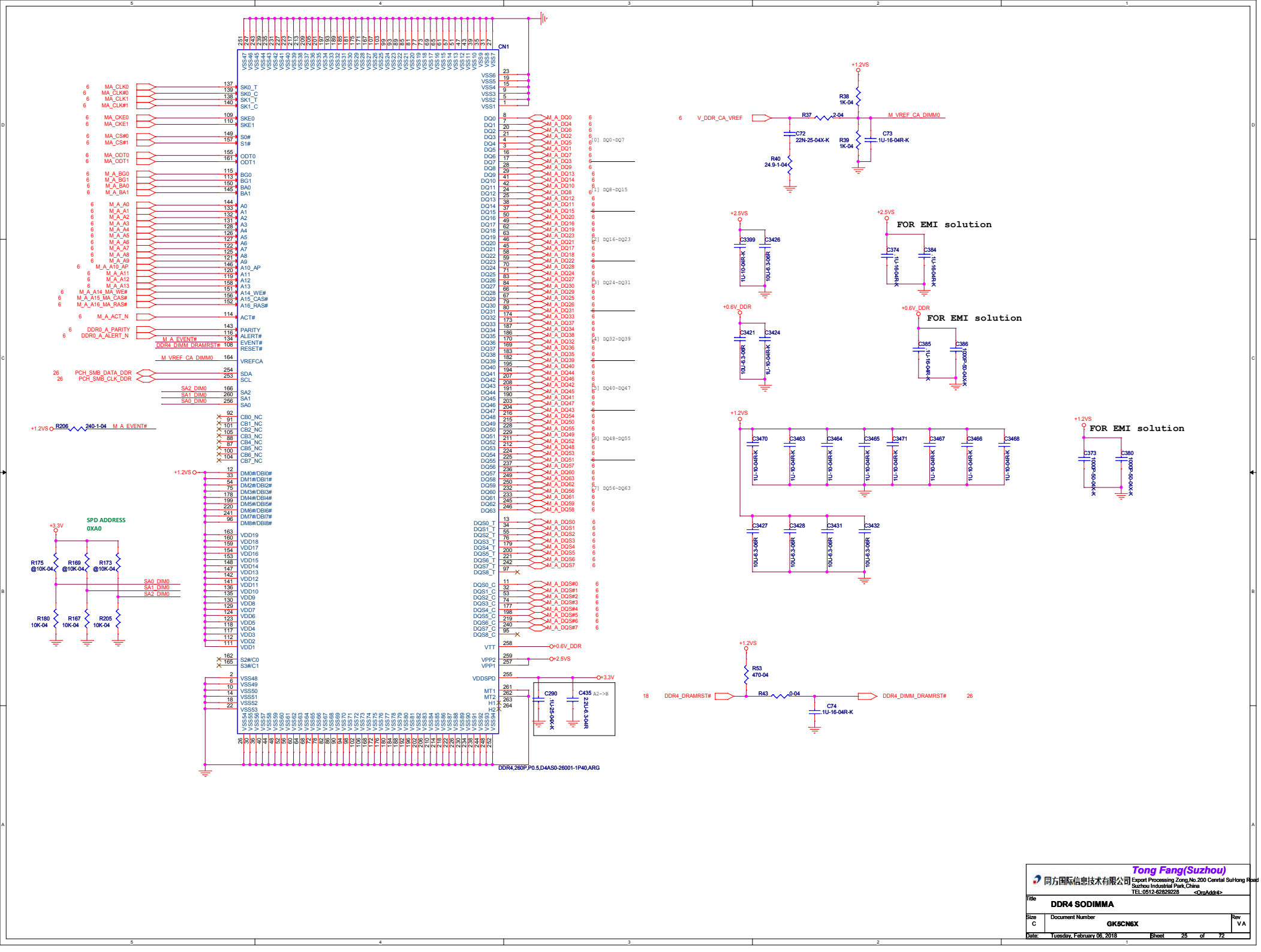
CN1
DDR4_260P.P0.5,D4AS0-26001-1P40,ARG
SPD ADDRESS
0XA0
FOR EMI solution
FOR EMI solution
FOR EMI solution
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<OrgAddr4>
Title
DDR4 SODIMMA
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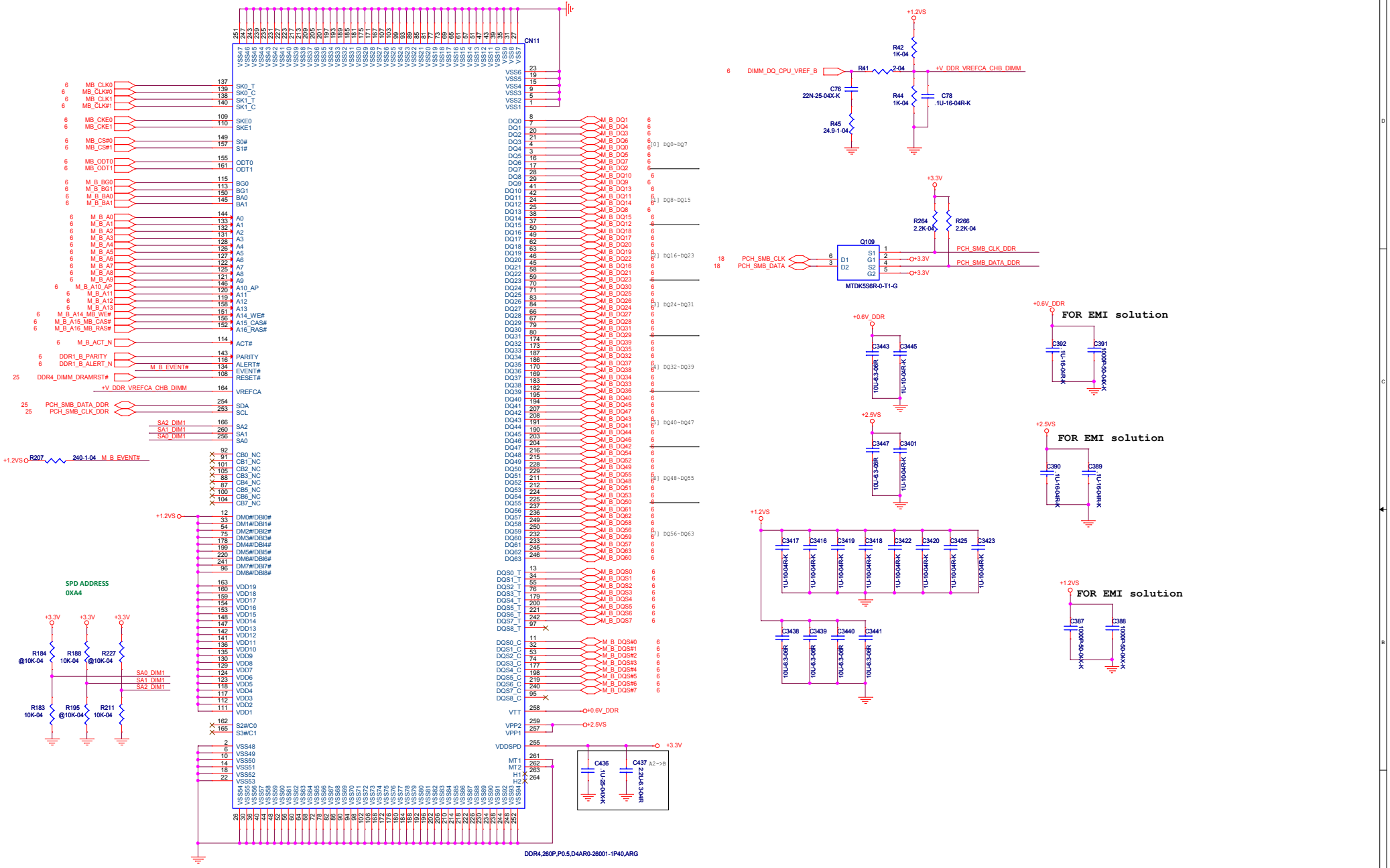

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Title	DDR4 SODIMMB		
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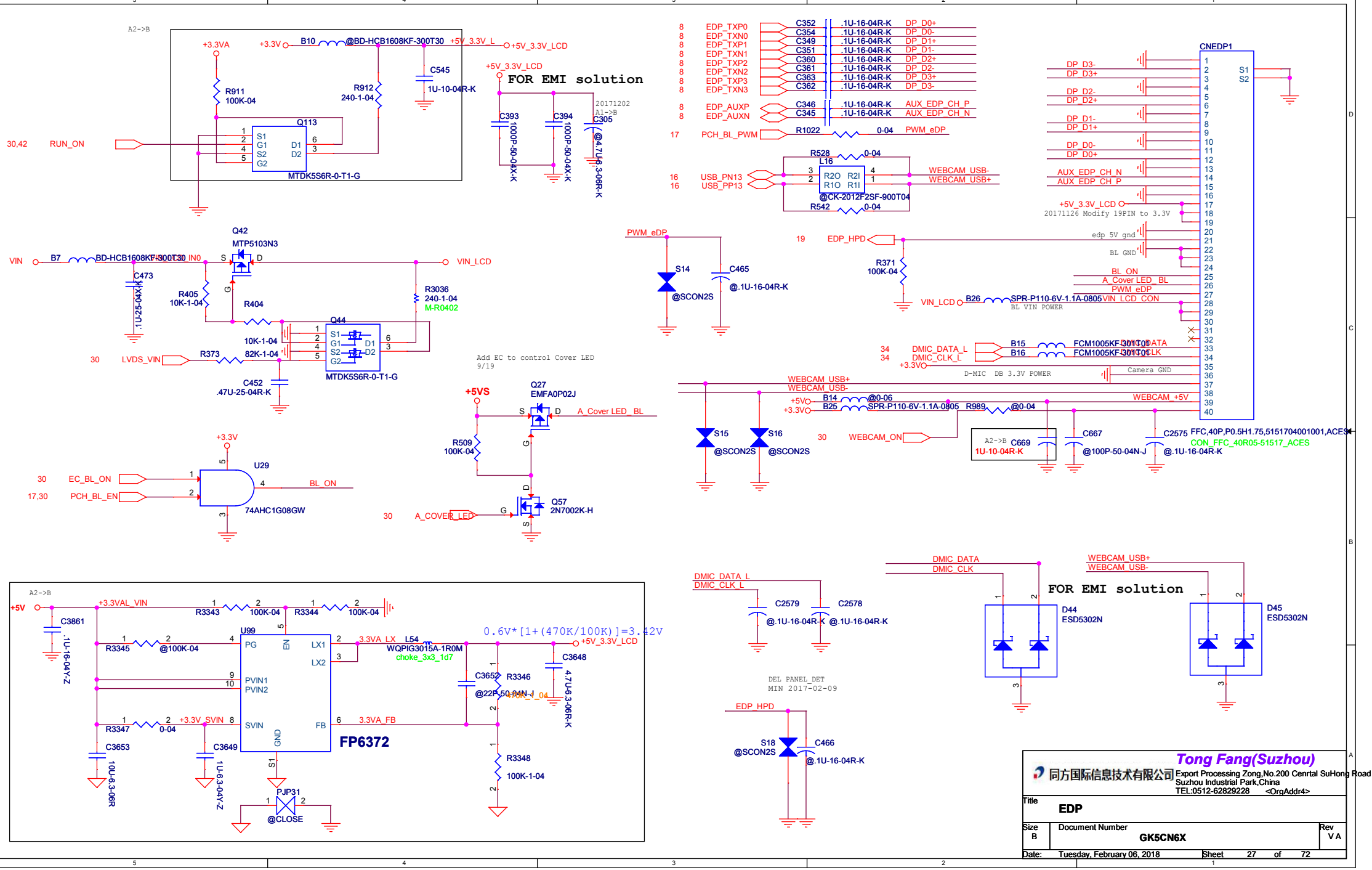
FOR EMI solution
20171202
A1->B
MTDK5S6R-0-T1-G
Q42
MTP5103N3
VIN
VIN_LCD
Q44
MTDK5S6R-0-T1-G
Add EC to control Cover LED
9/19
Q27
EMFA0P02J
Q57
2N7002K-H
U29
74AHC1G08GW
CNEDP1
FFC,40P,P0.5H1.75,5151704001001,ACES
CON_FFC_40R05-51517_ACES
20171126 Modify 19PIN to 3.3V
D-MIC DB 3.3V POWER
FOR EMI solution
D44
ESD5302N
D45
ESD5302N
FP6372
0.6V*[1+(470K/100K)]=3.42V
DEL PANEL_DET
MIN 2017-02-09
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EDP
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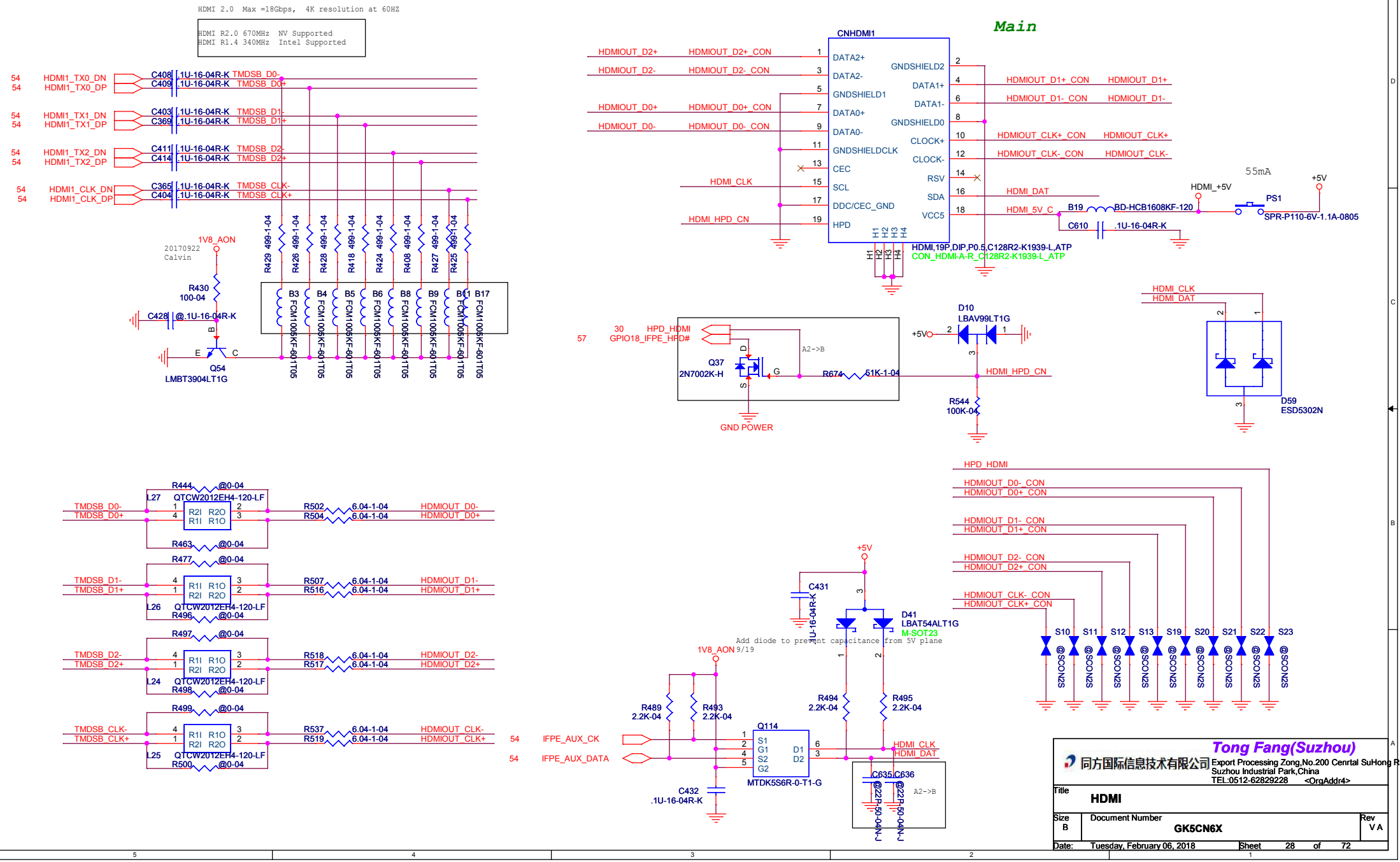
HDMI CONN



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Title: HDMI			
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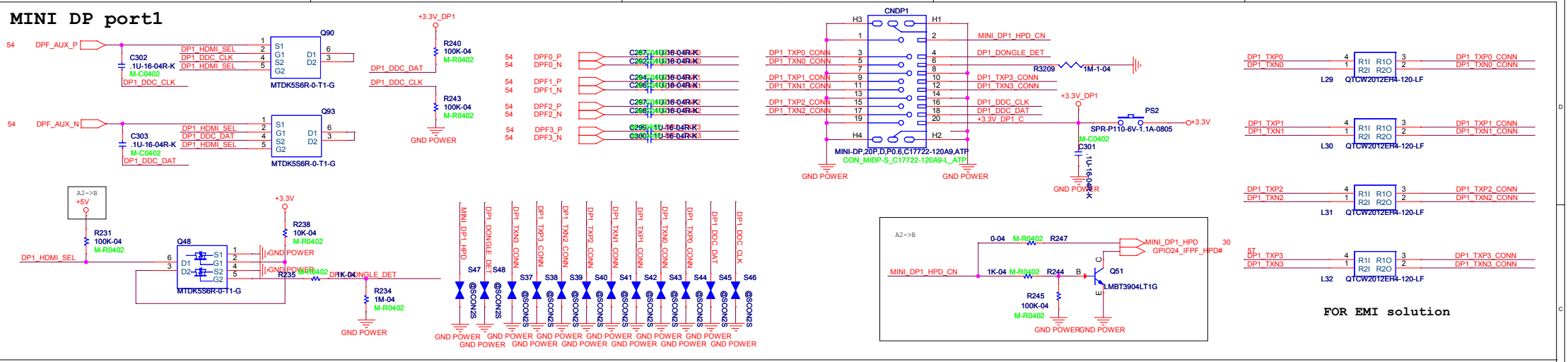
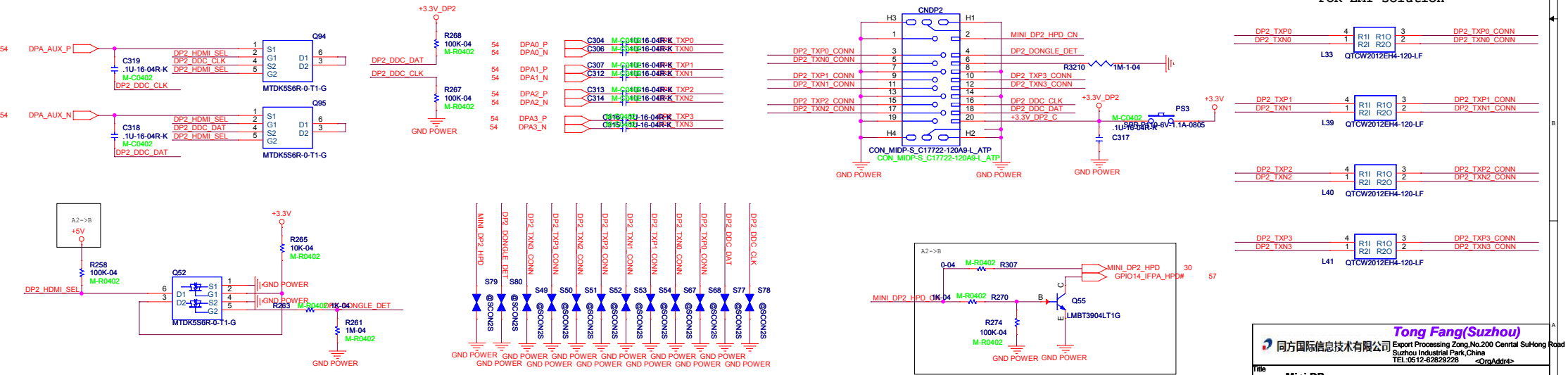
MINI DP port1



MINI DP port2



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Title	Mini DP	
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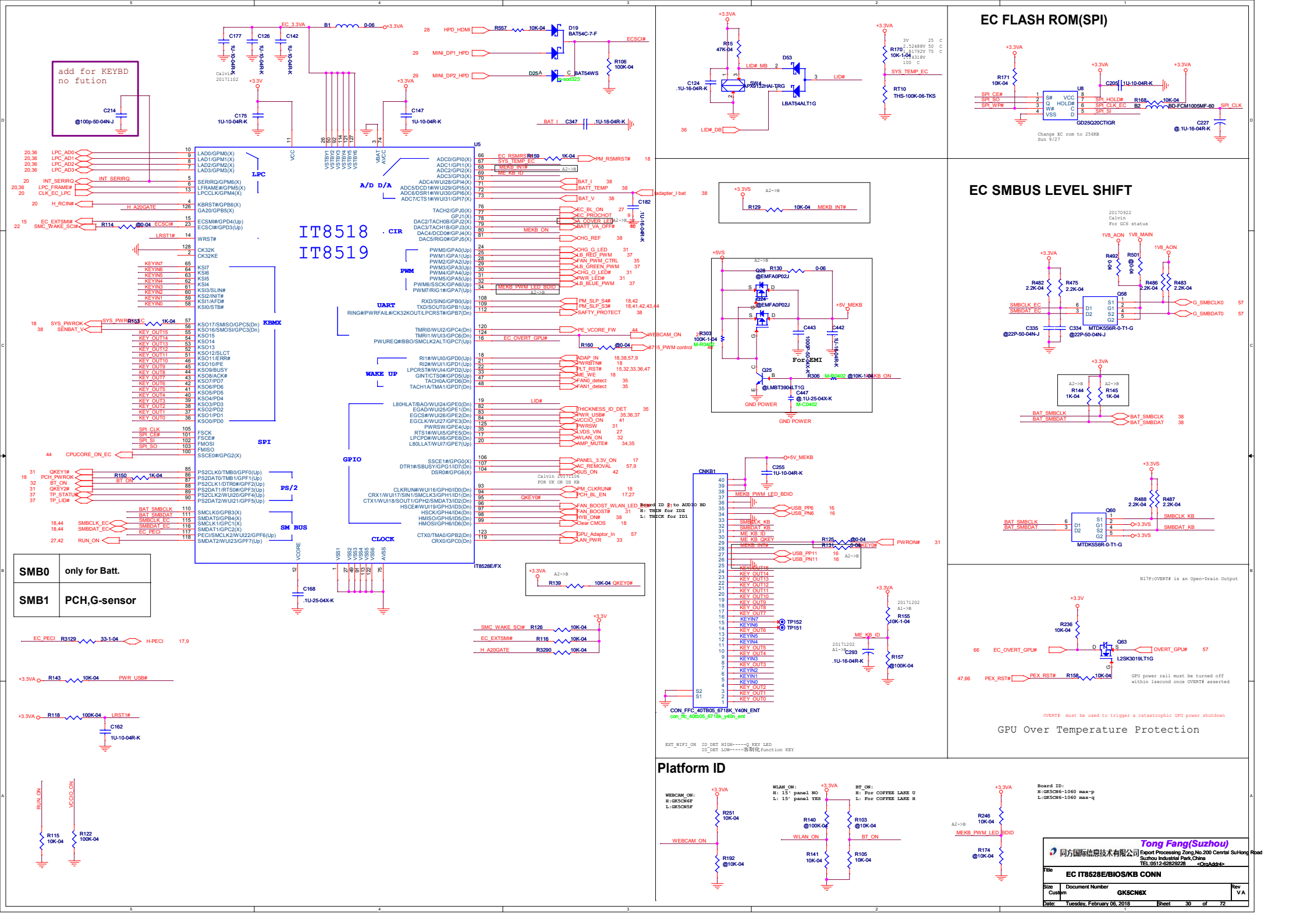
add for KEYBD no futions
IT8518
IT8519
LPC
A/D D/A
CIR
PWM
UART
WAKE UP
KBMX
SPI
GPIO
PS/2
SM BUS
CLOCK
IT8528E/FX
SMB0 only for Batt.
SMB1 PCH,G-sensor
EC FLASH ROM(SPI)
EC SMBUS LEVEL SHIFT
GPU Over Temperature Protection
Platform ID
CON_FFC_40TB05_6718K_Y40N_ENT
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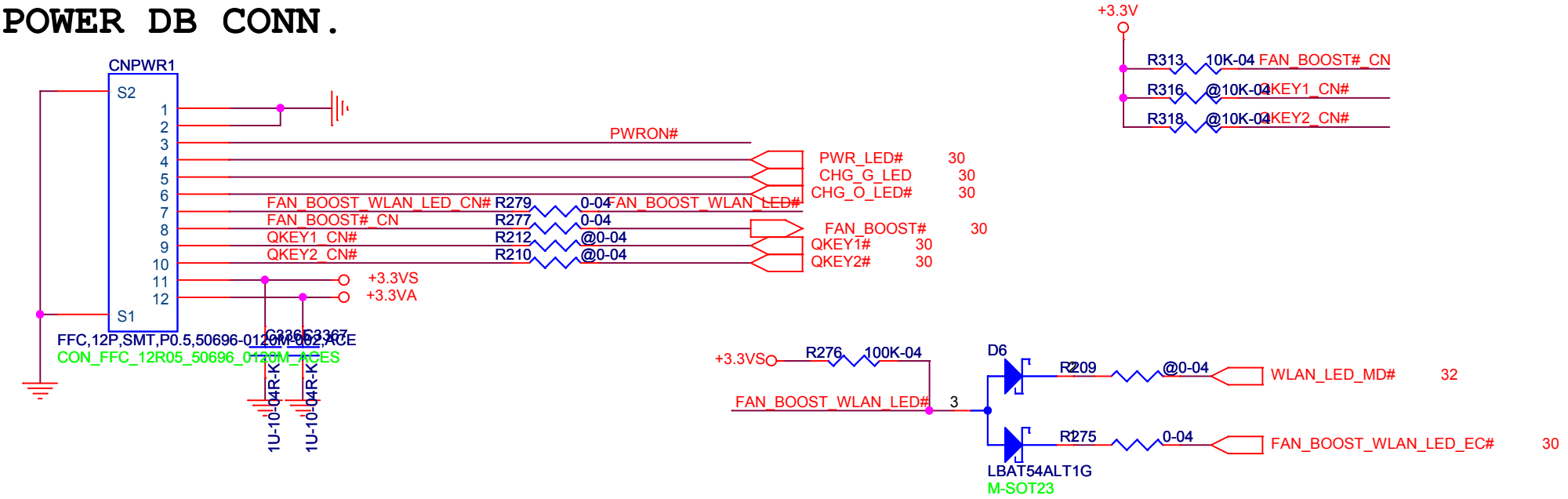
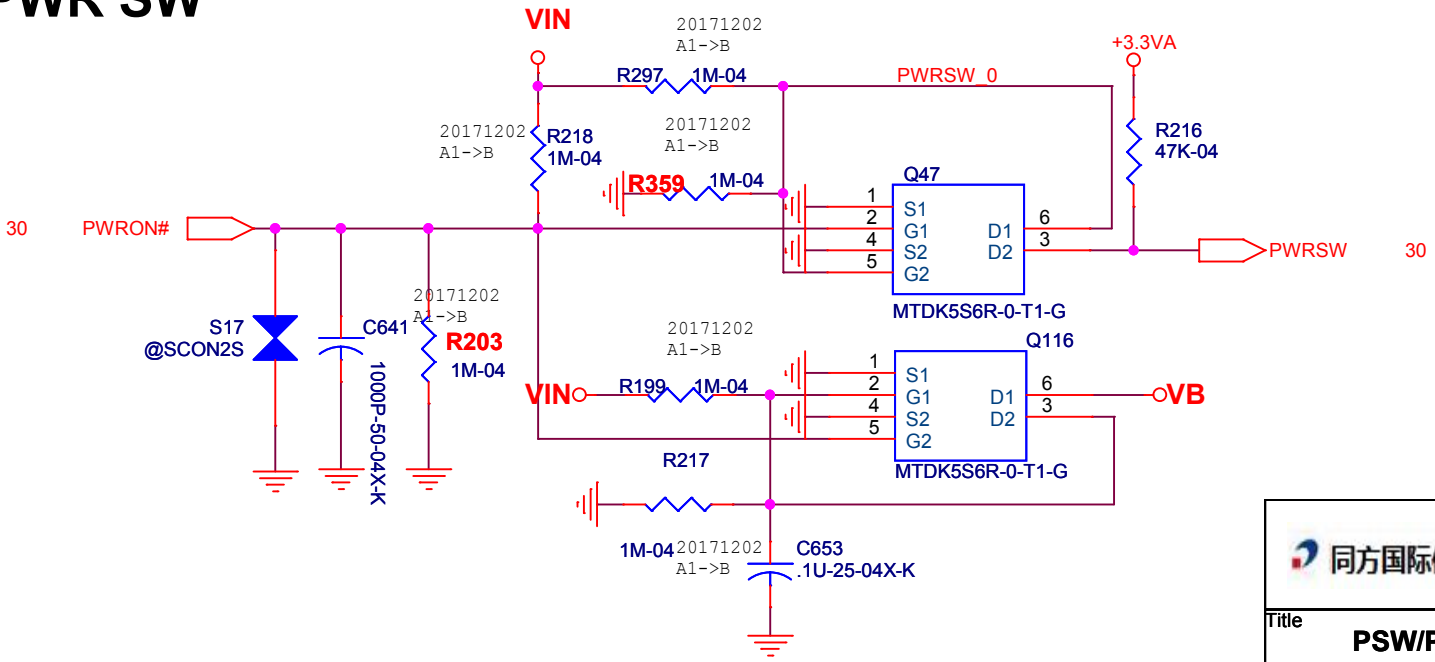
EC IT8528E/BIOS/KB CONN
GK5CN6X

POWER DB CONN.



PWR SW



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Title	PSW/PWR DB CON	
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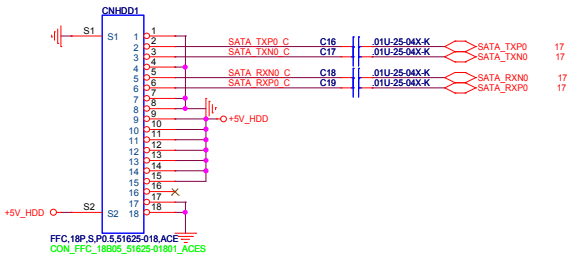
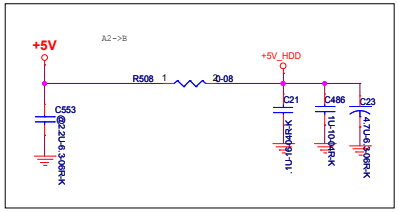
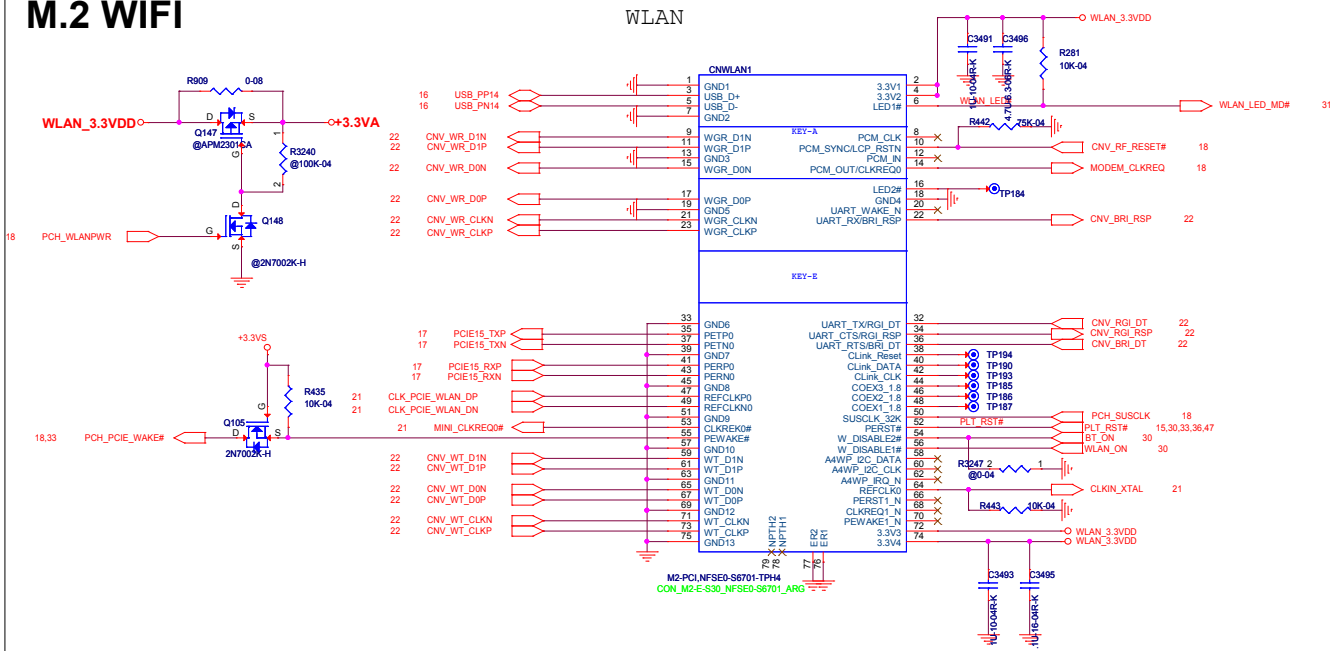
SATA-HDD

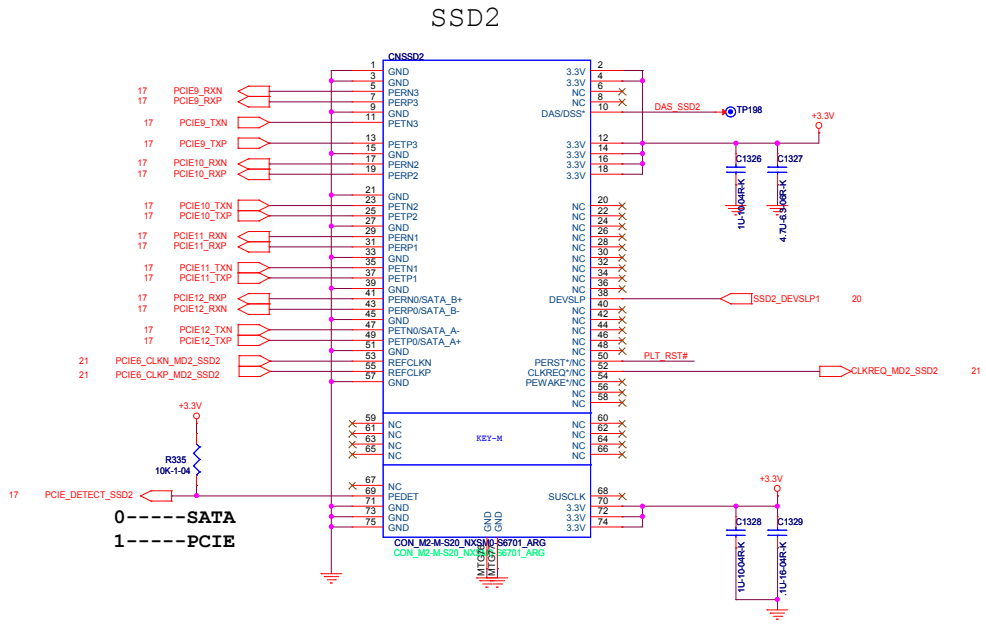


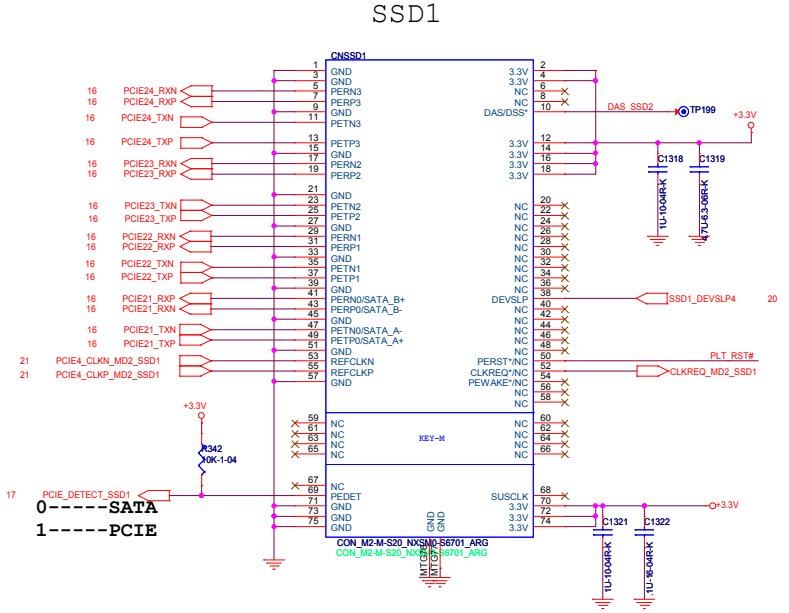


M.2 WIFI



M.2 SSD





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Title	LAN RTL8111	
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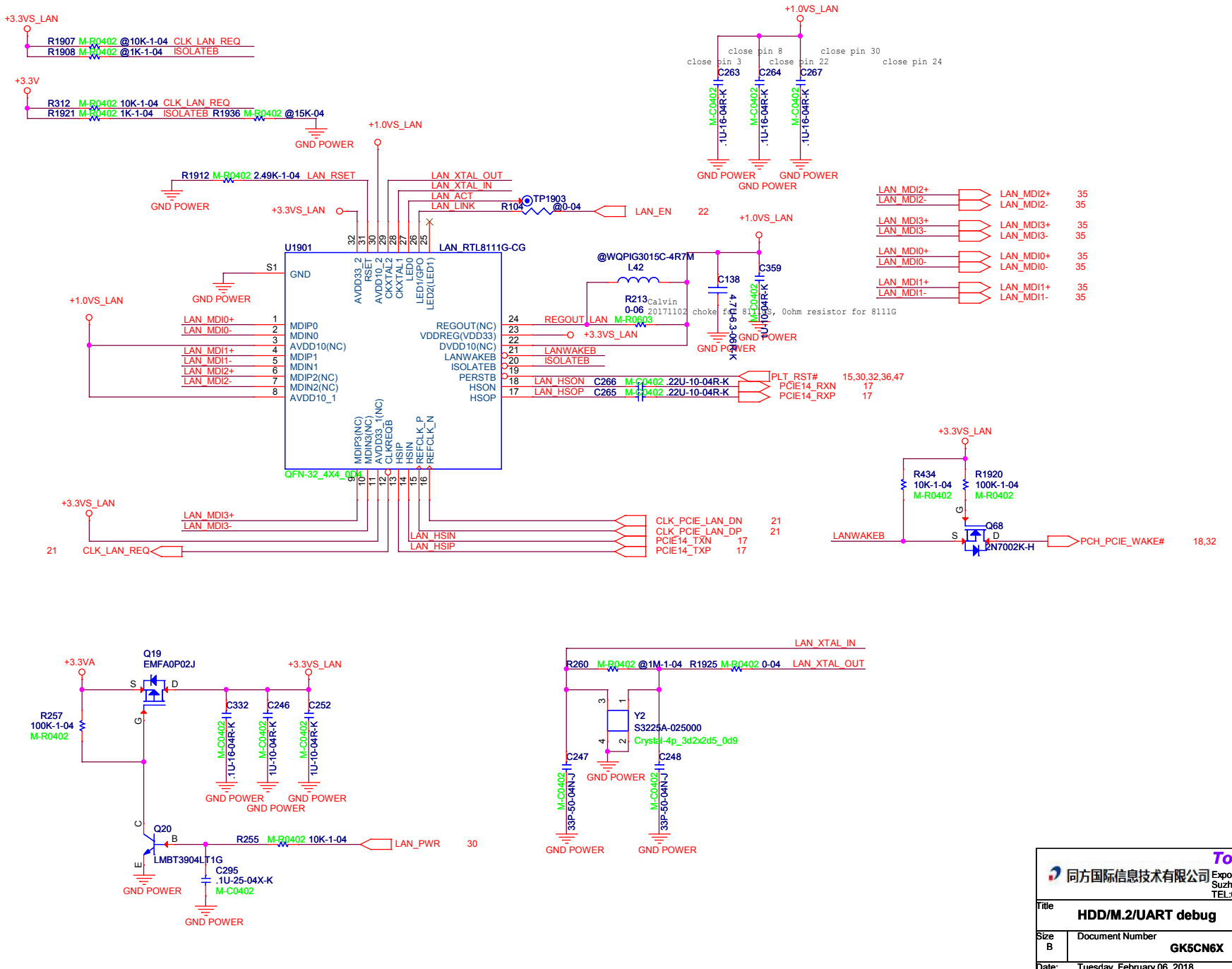

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Title	HDD/M.2/UART debug	
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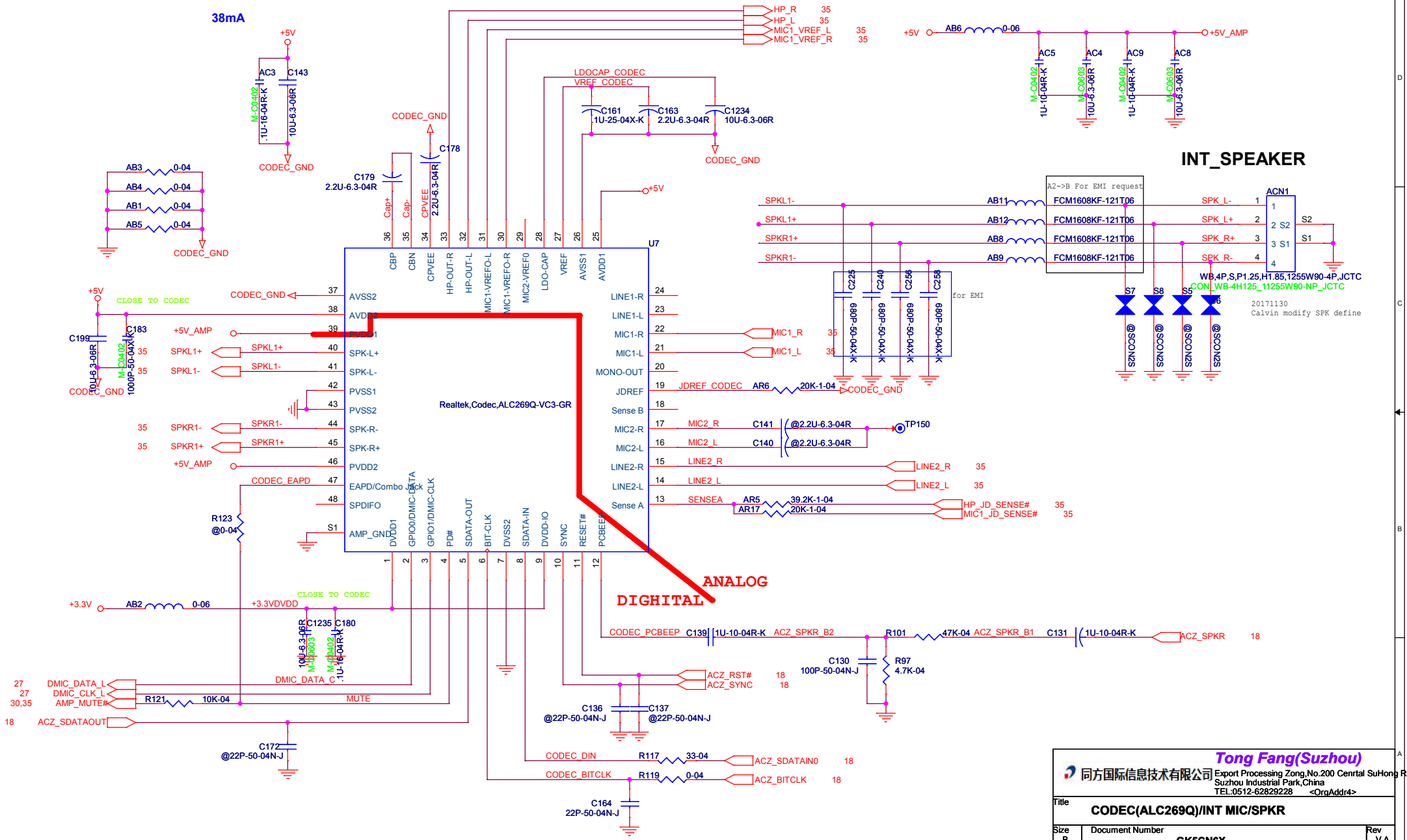
CODEC ALC269Q

38mA

AMP VDD

INT_SPEAKER



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Title	CODEC(ALC269Q)/INT MIC/SPKR	
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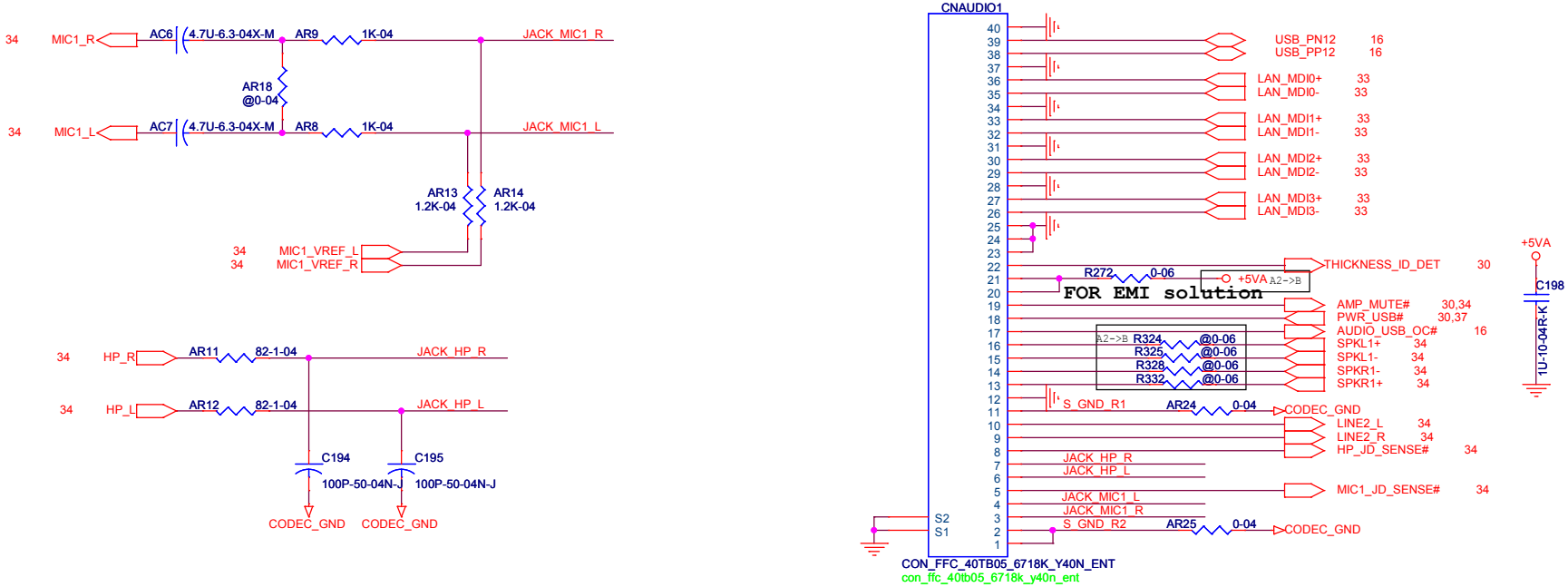
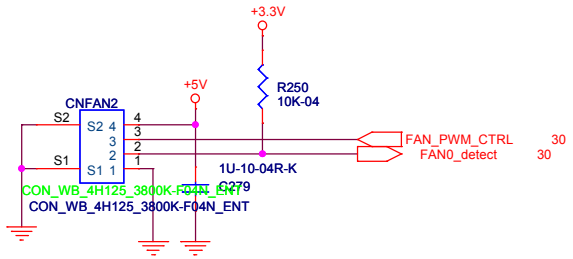
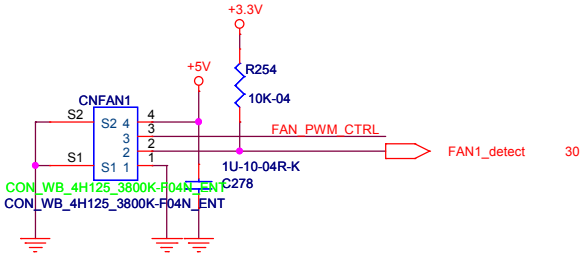
EXT MIC / EXT LINE IN / EXT USB JACK



FAN CONTROLLER 0



FAN CONTROLLER 1



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Title	EXT_AUDIO/EXT_USB/FAN	
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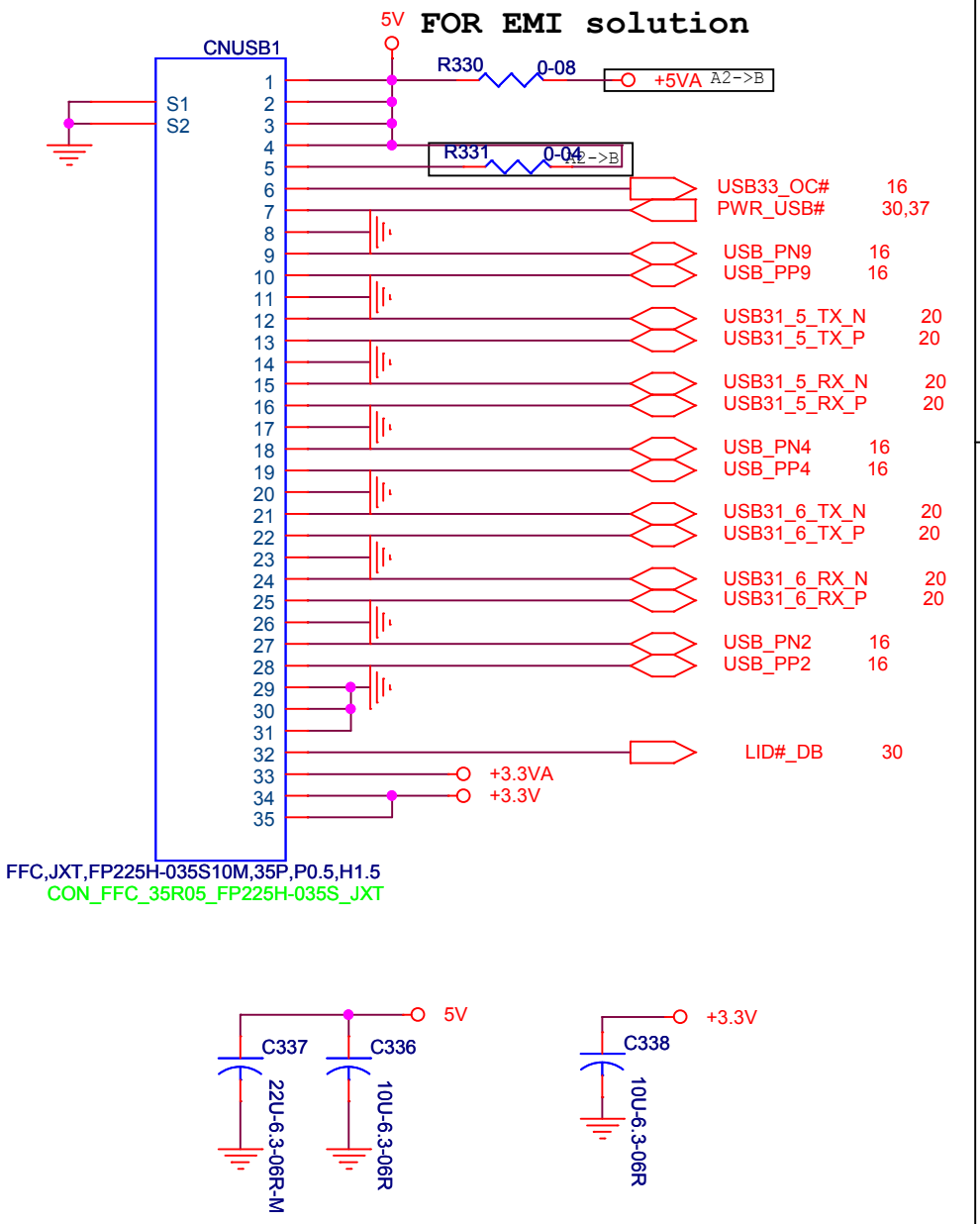
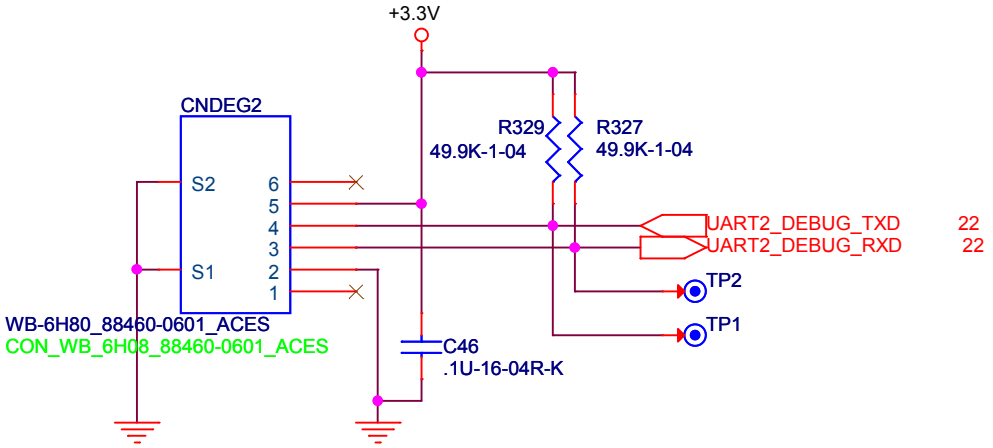
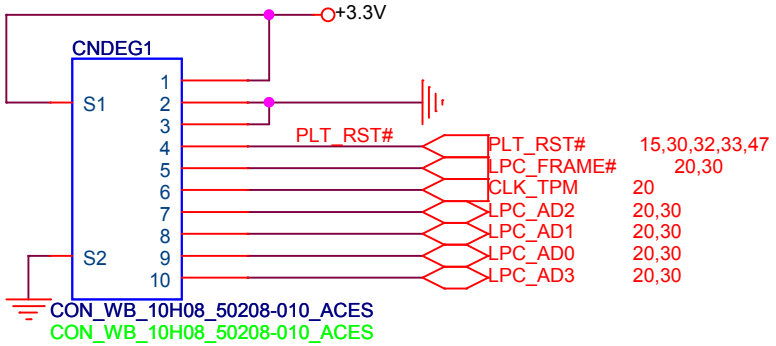
EXT USB3.1 DB



UART debug port



LPC debug port



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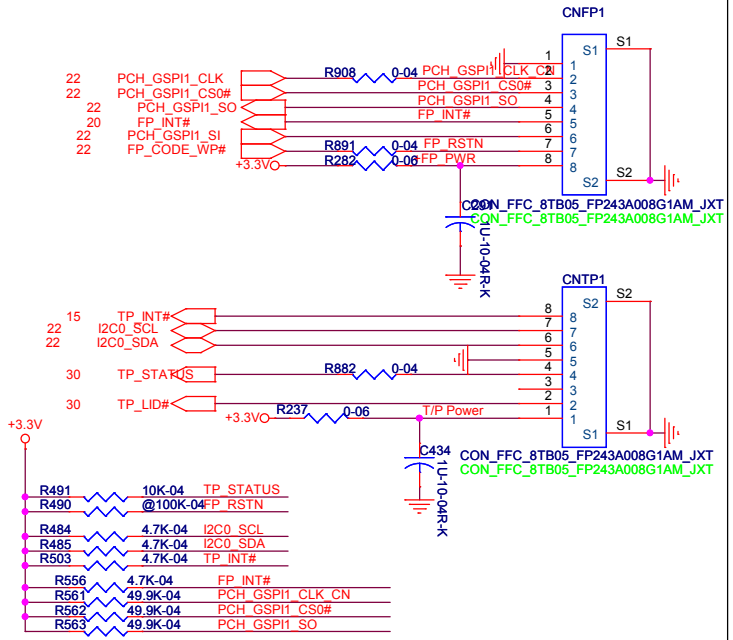
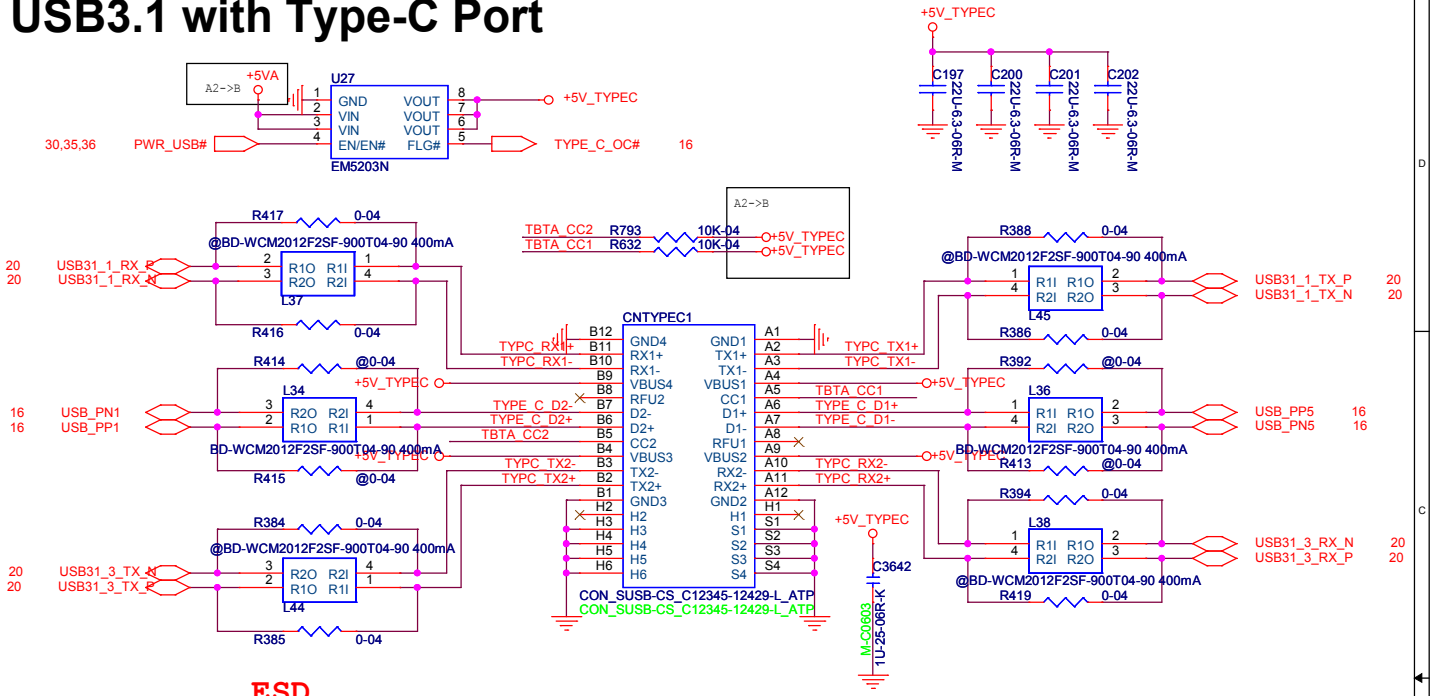
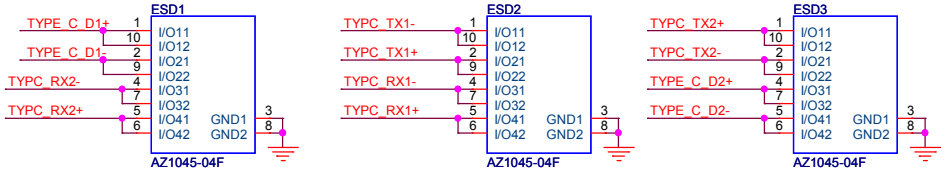
Touch Pad&Finger Print



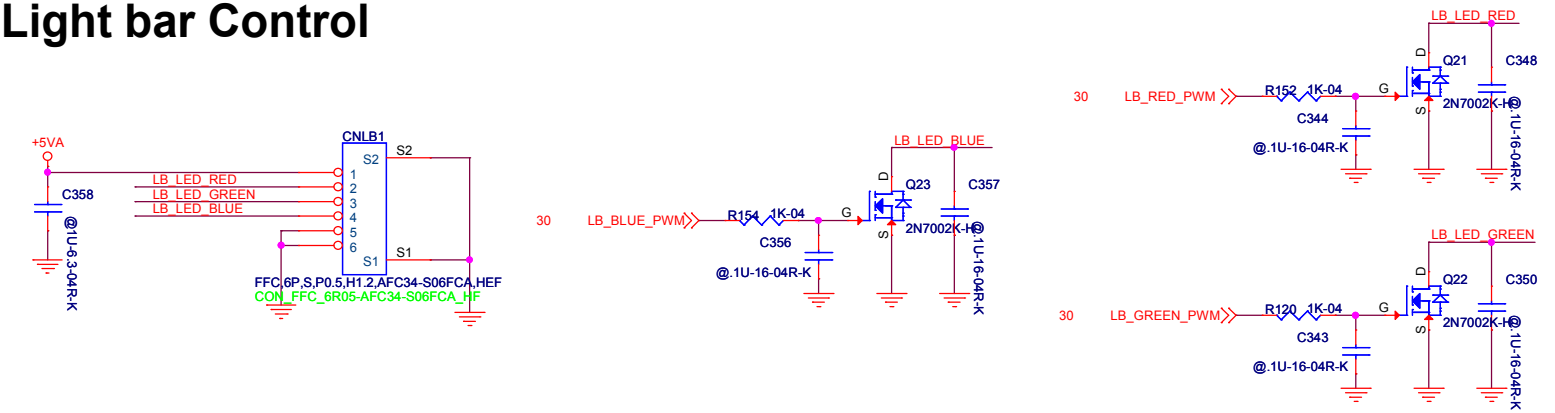
USB3.1 with Type-C Port



ESD



Light bar Control



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Title: TP/USB/TYPEC		
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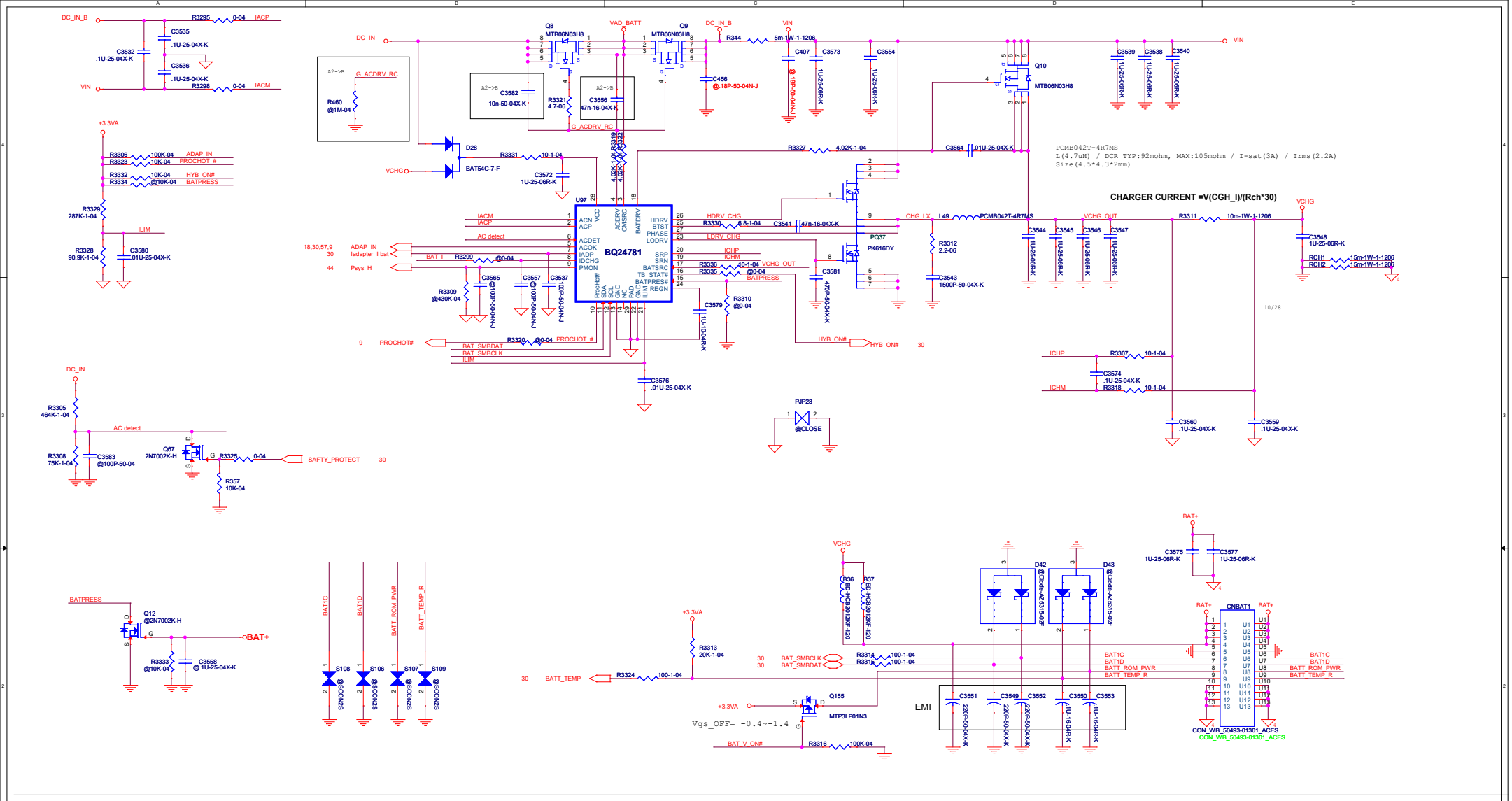
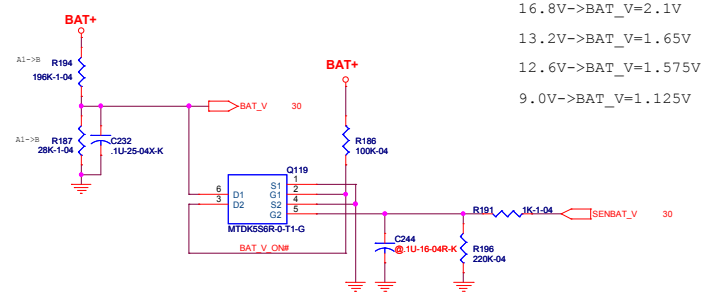


Battery Voltage Detect



17.6V->BAT_V=2.2V

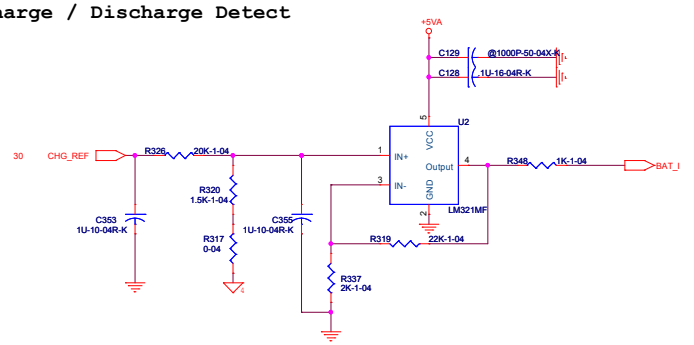
16.8V->BAT_V=2.1V

13.2V->BAT_V=1.65V

12.6V->BAT_V=1.575V

9.0V->BAT_V=1.125V

Charge / Discharge Detect



BAT_I	ICHG (0.0837V/1A)
2.0092V	4A
1.8418V	2A
1.7581V	1A
1.6744V	0A
1.5907V	-1A
1.507V	-2A
1.3396V	-4A
1.1722V	-6A
1.0048V	-8A
0.8374V	-10A

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Title: BATT IN/CHARGER(BQ24781)

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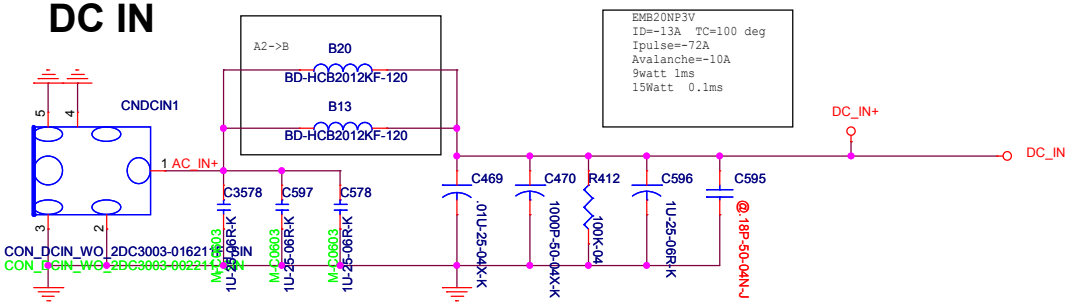
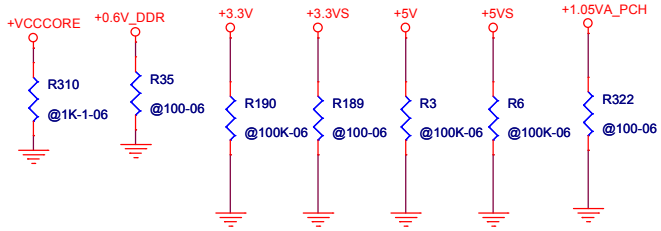
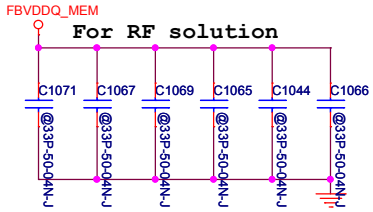
DC IN



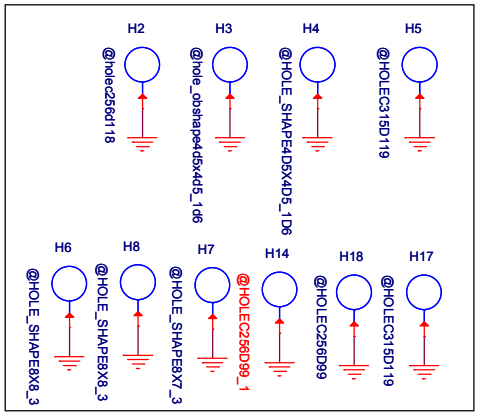
Discharge Resistor



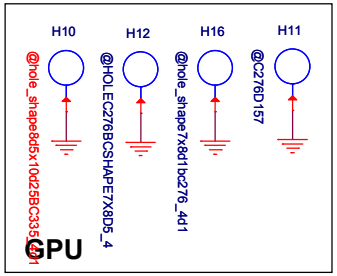
HIGH-SPEED CAP

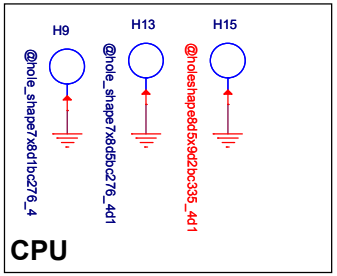


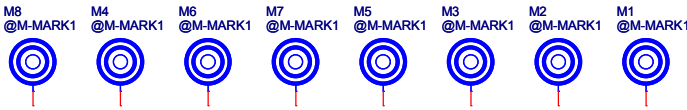
PCB HOLE



THERMAL HOLE







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Title	DC IN/TPM/D-Resis/HOLE	
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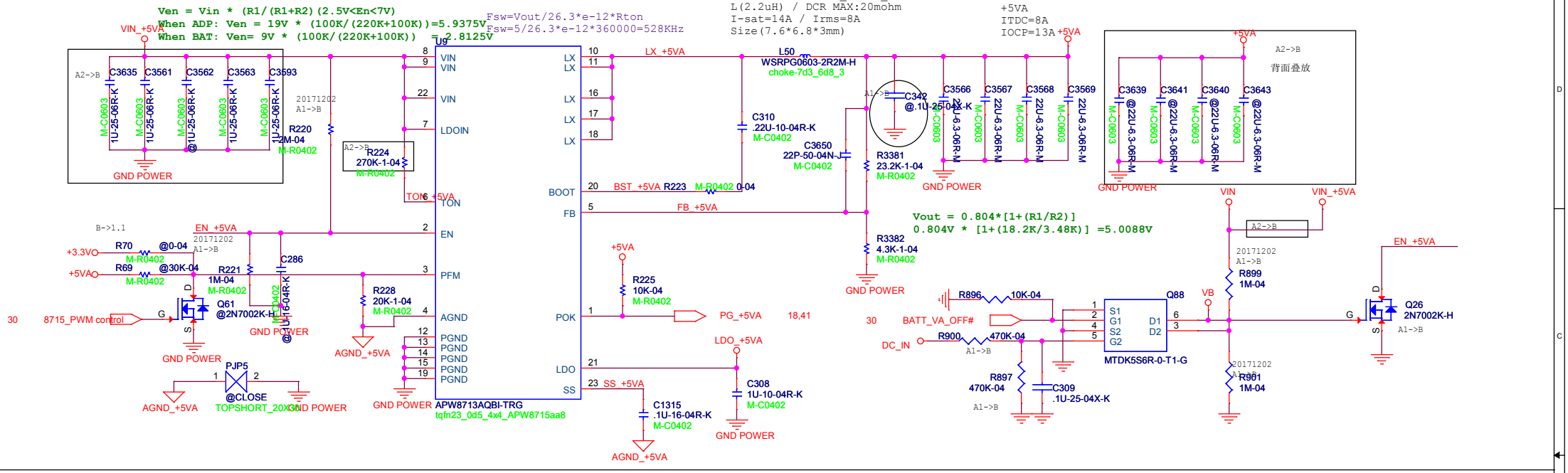
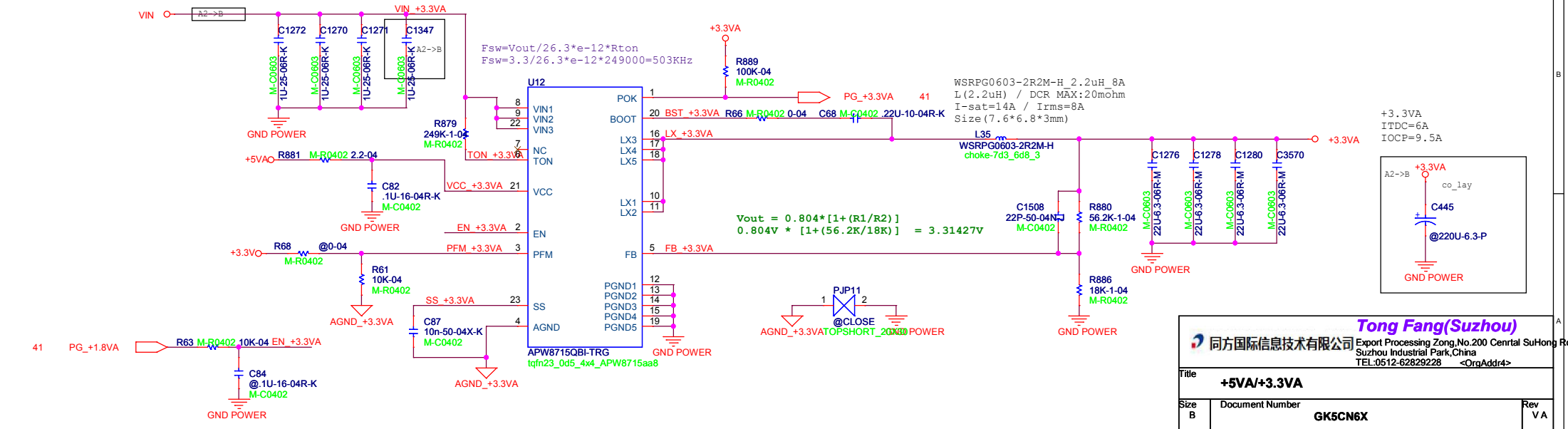
5VAL Converter





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Title	+5VA/+3.3VA	
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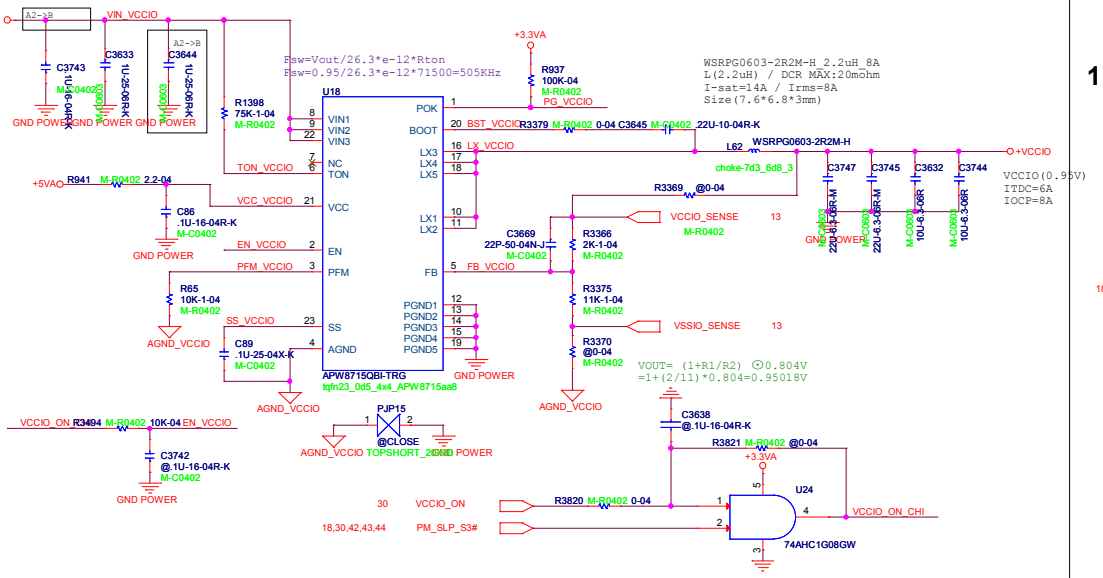
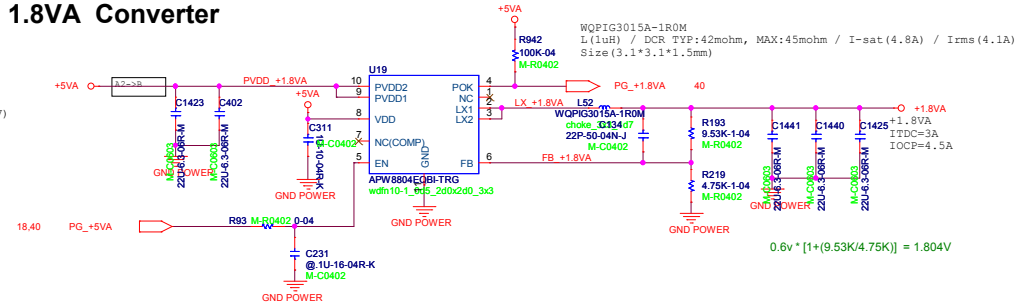
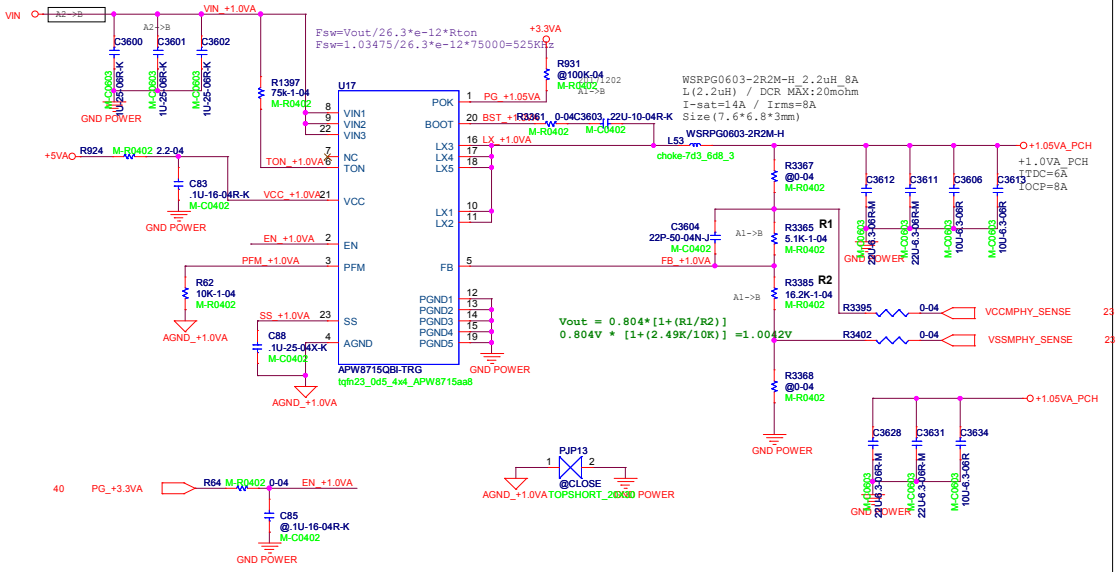
VCCIO Converter



1.8VA Converter



1.05VA Converter



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Title	+1.0VA_PCH/VCCIO/+1.8VA	
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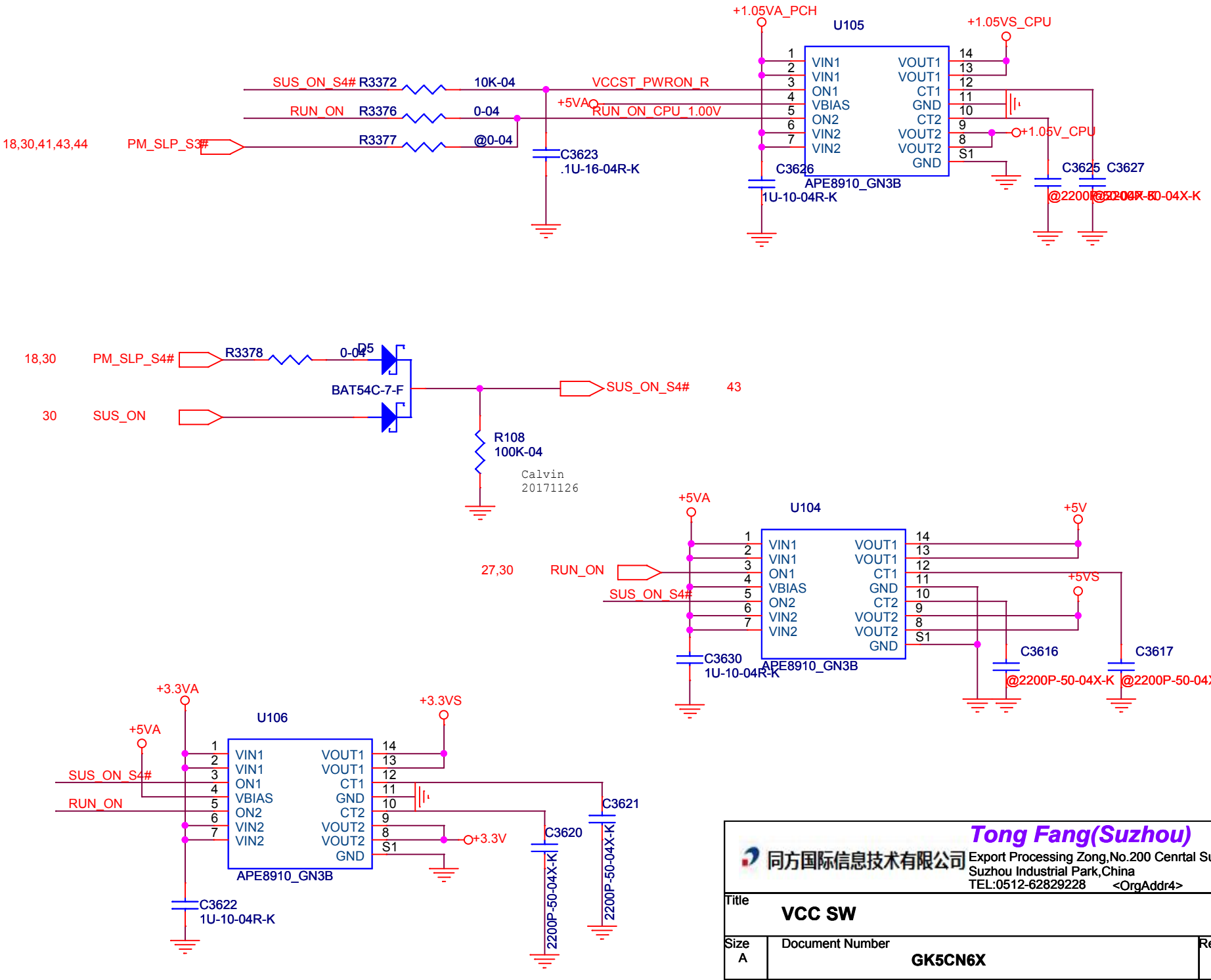

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Title	VCC SW	
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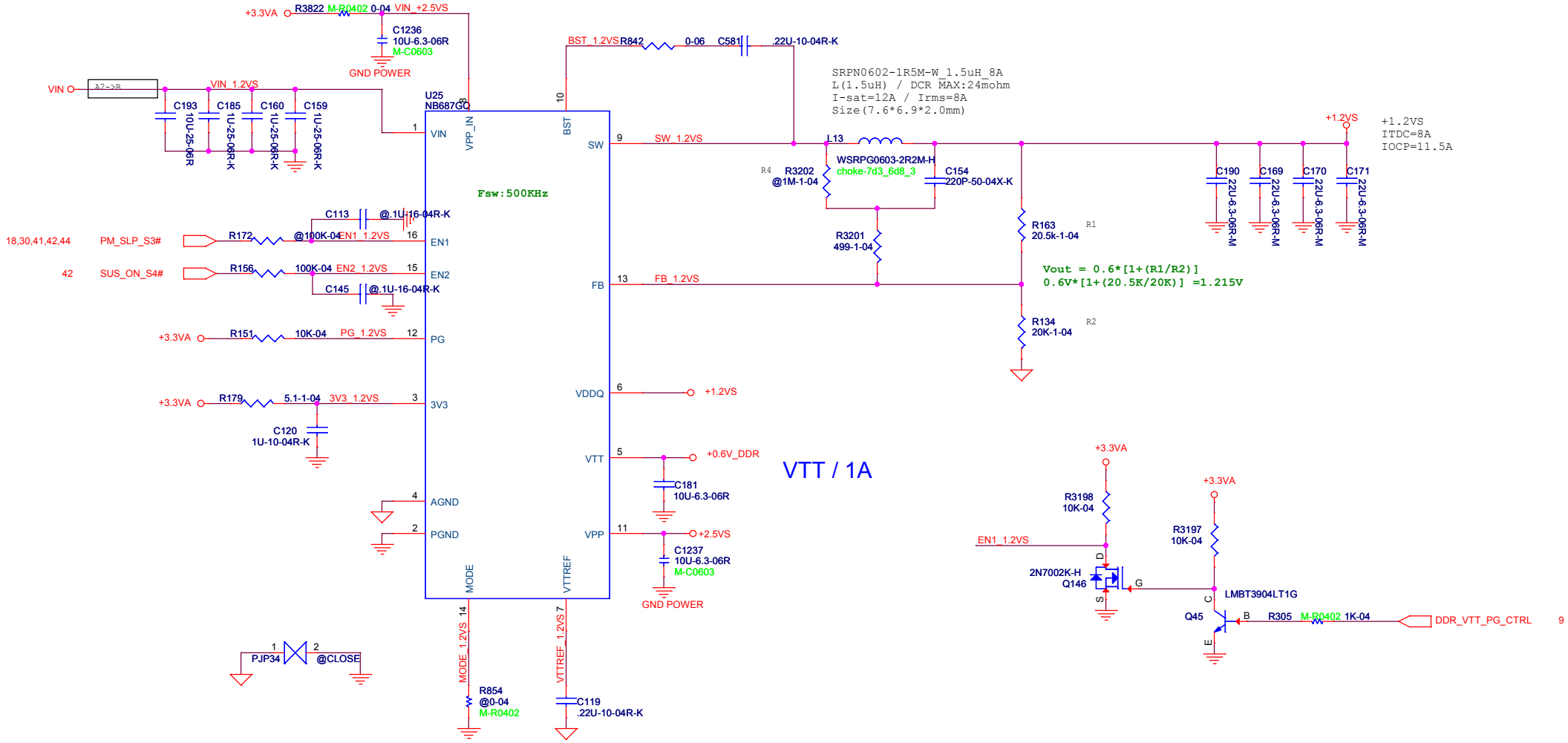
1.2VS/VTT/2.5VS



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Title: +1.2VS/+2.5VS		
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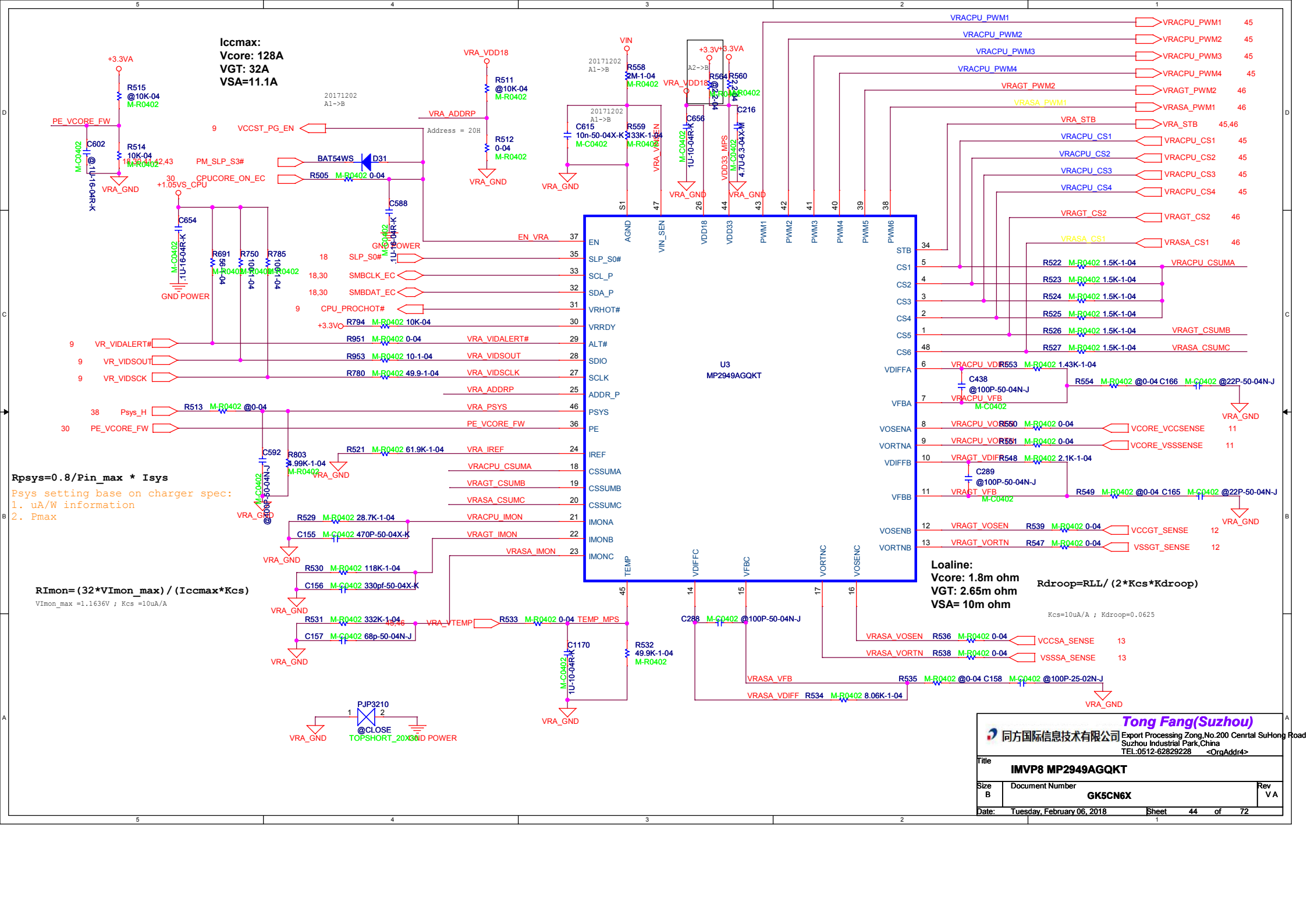
Iccmax:
Vcore: 128A
VGT: 32A
VSA=11.1A
U3
MP2949AGQKT
Rpsys=0.8/Pin_max * Isys
Psys setting base on charger spec:
1. uA/W information
2. Pmax
RImon=(32*VImon_max)/(Iccmax*Kcs)
VImon_max =1.1636V ; Kcs =10uA/A
Loaline:
Vcore: 1.8m ohm
VGT: 2.65m ohm
VSA= 10m ohm
Rdroop=RLL/(2*Kcs*Kdroop)
Kcs=10uA/A ; Kdroop=0.0625
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Title
IMVP8 MP2949AGQKT
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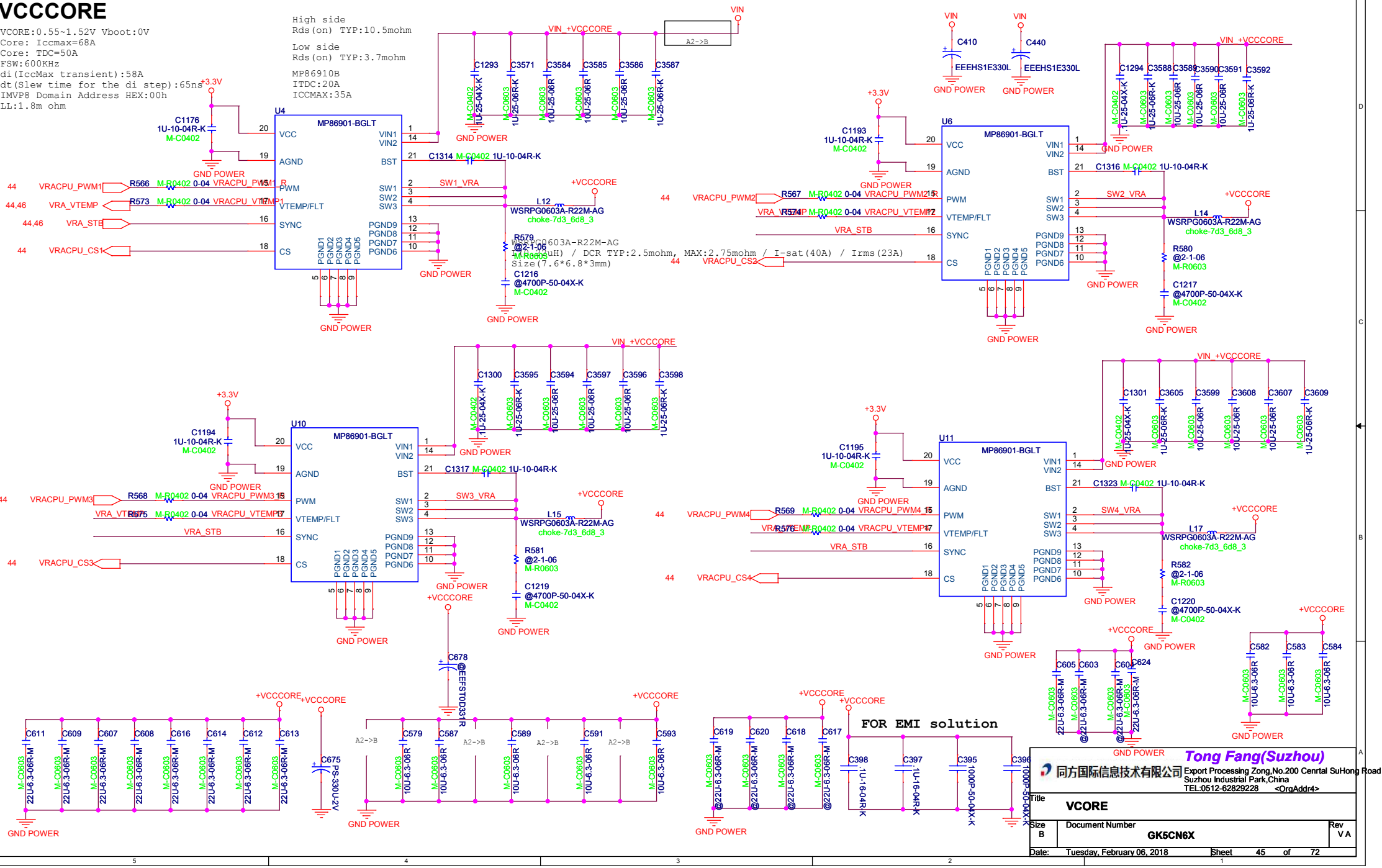
VCCCORE

VCORE:0.55~1.52V Vboot:0V
Core: Iccmax=68A
Core: TDC=50A
FSW:600KHz
di(IccMax transient):58A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:00h
LL:1.8m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



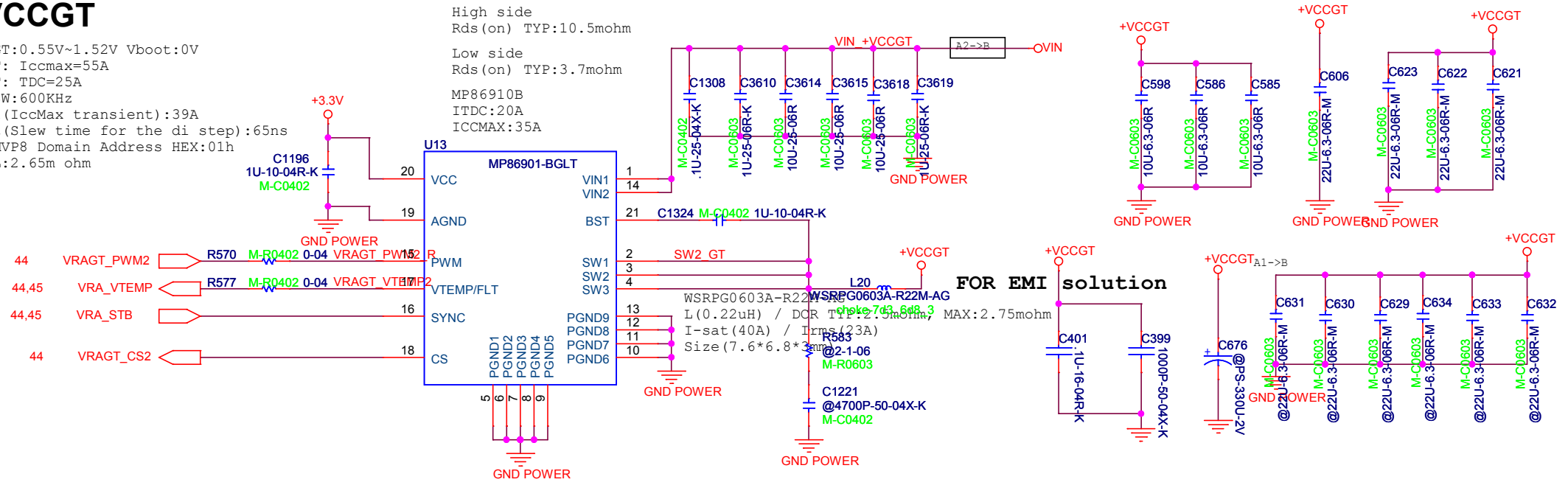
VCCGT

VGT:0.55V~1.52V Vboot:0V
GT: Iccmax=55A
GT: TDC=25A
FSW:600KHz
di(IccMax transient):39A
dt(Slew time for the di step):65ns
IMVP8 Domain Address HEX:01h
LL:2.65m ohm

High side
Rds(on) TYP:10.5mohm

Low side
Rds(on) TYP:3.7mohm

MP86910B
ITDC:20A
ICCMAX:35A



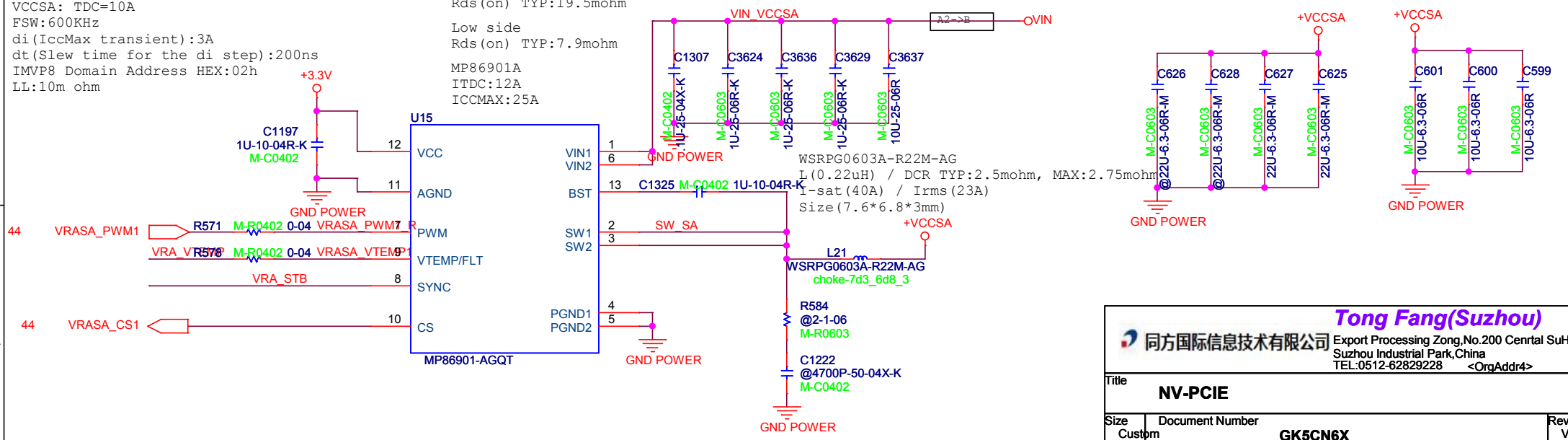
VCCSA

VCCSA:0.55~1.52V Vboot:1.05V
VCCSA: Iccmax=11.1A
VCCSA: TDC=10A
FSW:600KHz
di(IccMax transient):3A
dt(Slew time for the di step):200ns
IMVP8 Domain Address HEX:02h
LL:10m ohm

High side
Rds(on) TYP:19.5mohm

Low side
Rds(on) TYP:7.9mohm

MP86901A
ITDC:12A
ICCMAX:25A



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Title	NV-PCIE	
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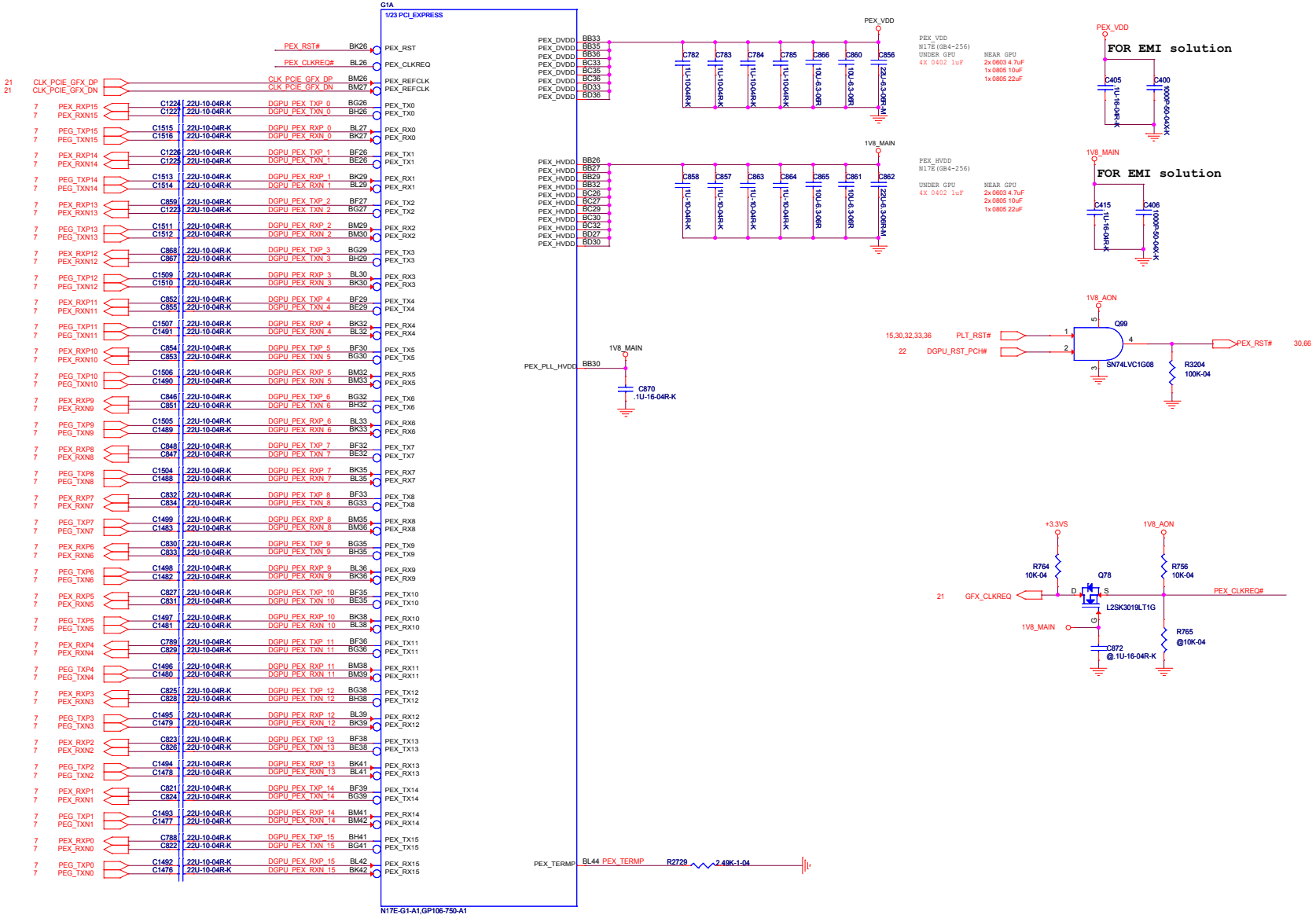

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Title	NV-PCIE
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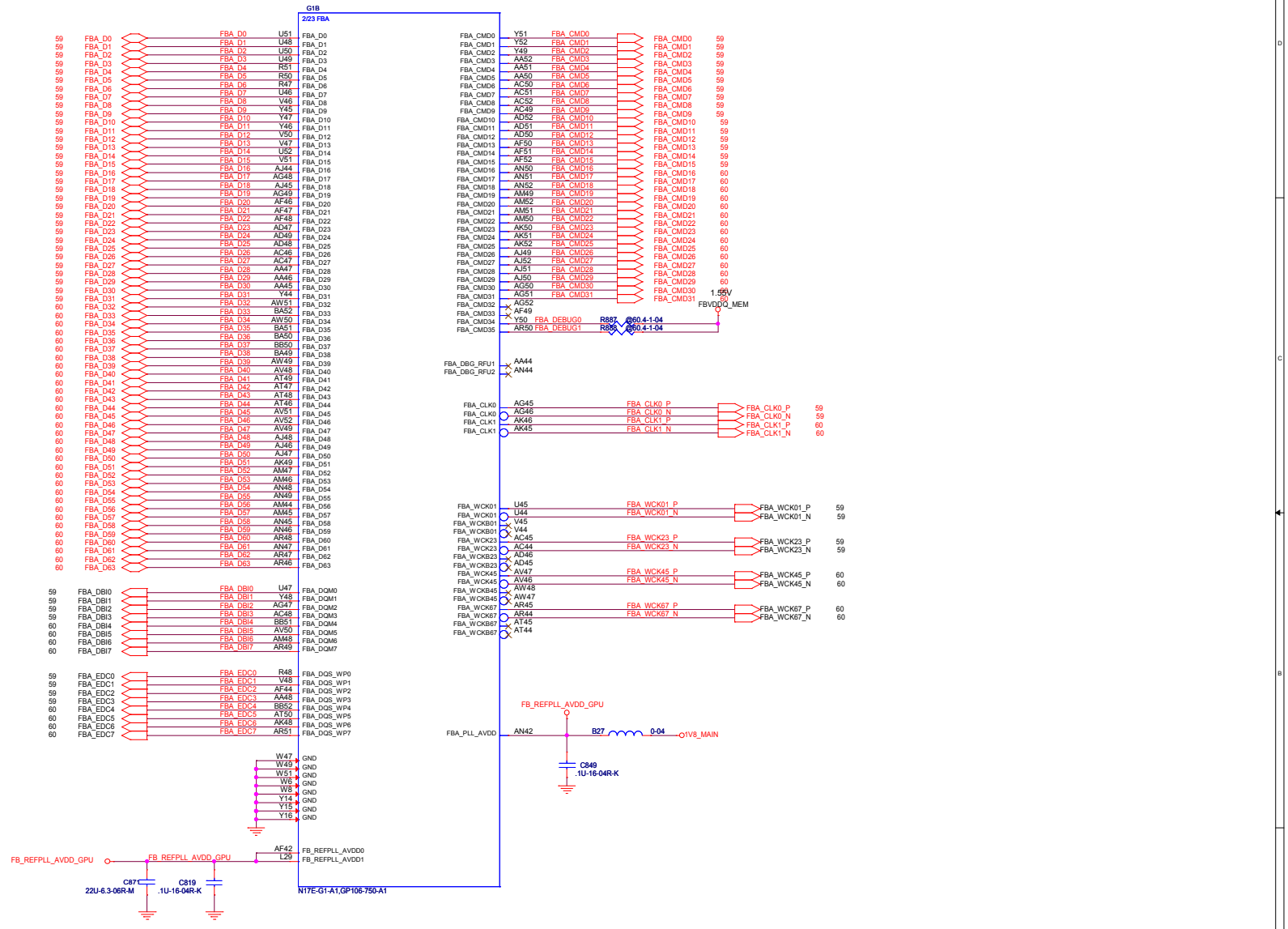

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Title	NV-BIOS/XTAL		
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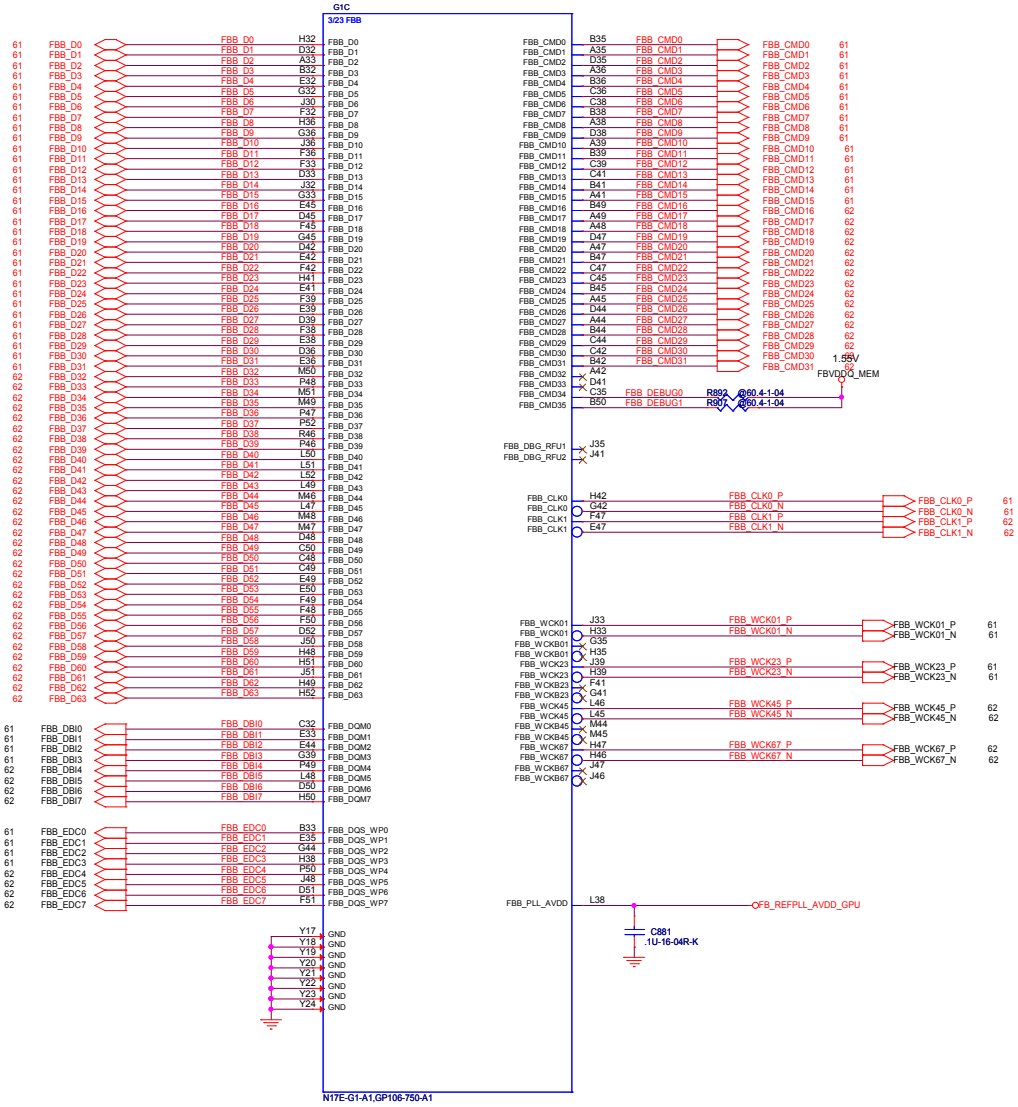

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Title	NV-Frame Buffer B	
Size C	Document Number GK5CN6X	Rev V A
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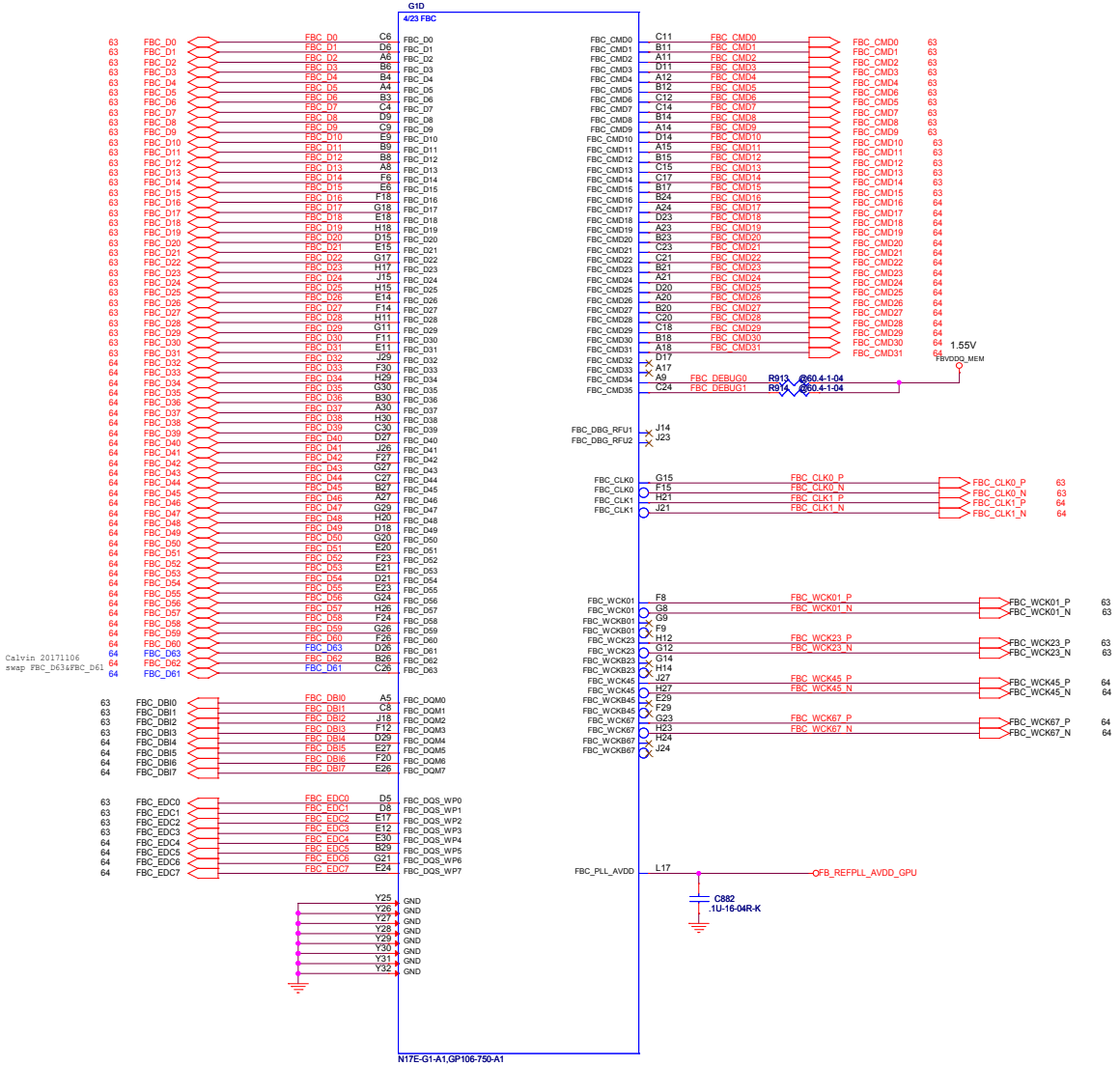

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Title	NV-Frame Buffer C	
Size C	Document Number GK5CN6X	Rev V A
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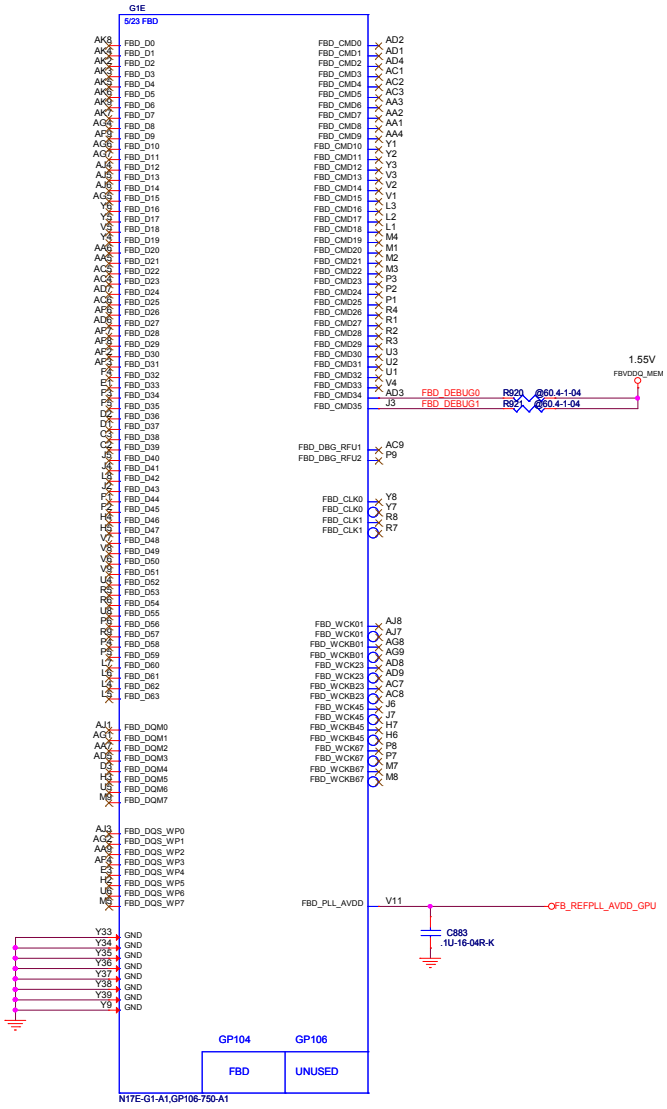

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Title	NV-Frame Buffer D	
Size C	Document Number GK5CN6X	Rev V A
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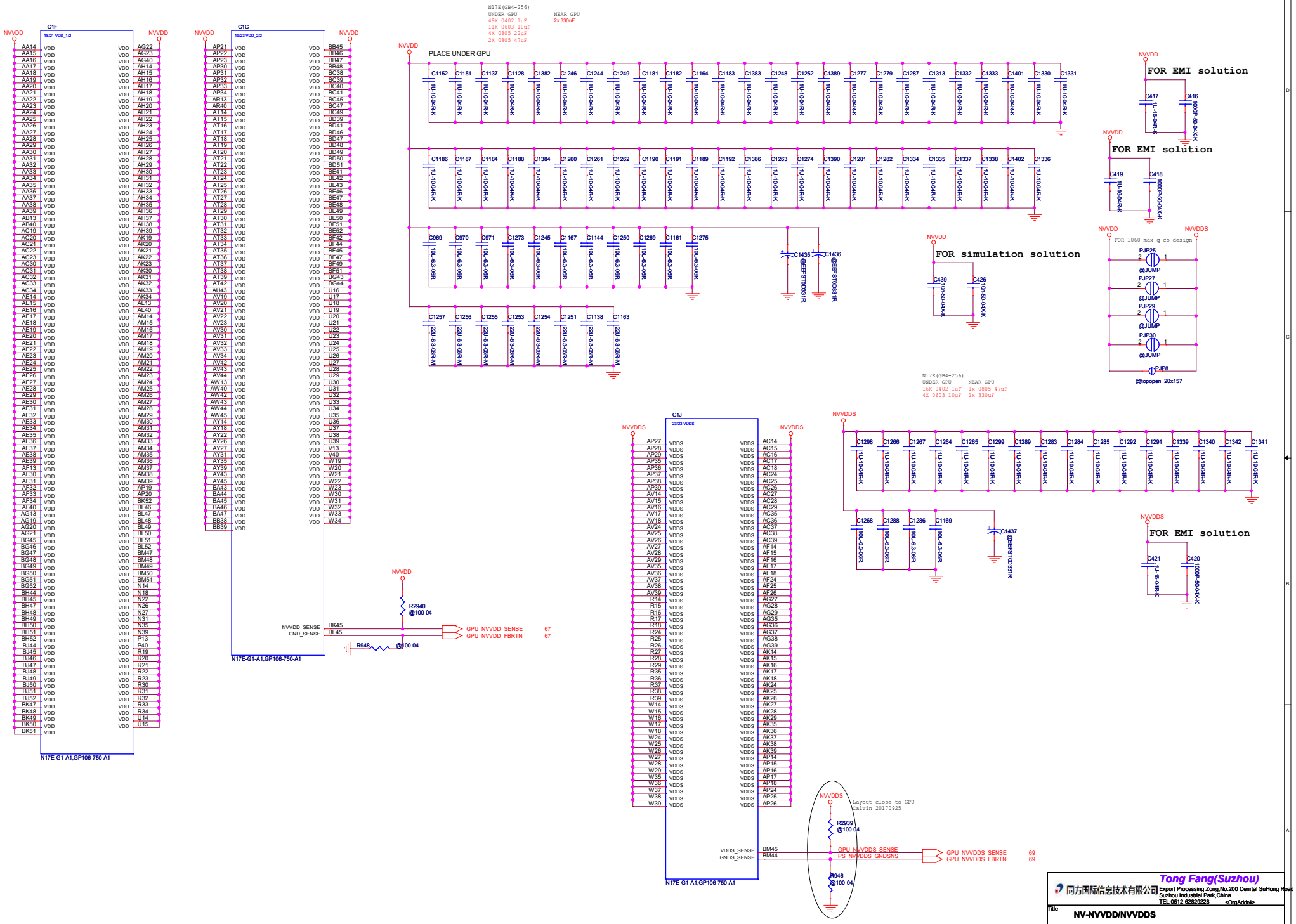

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Title	NV-NVVDD/NVVDDS		
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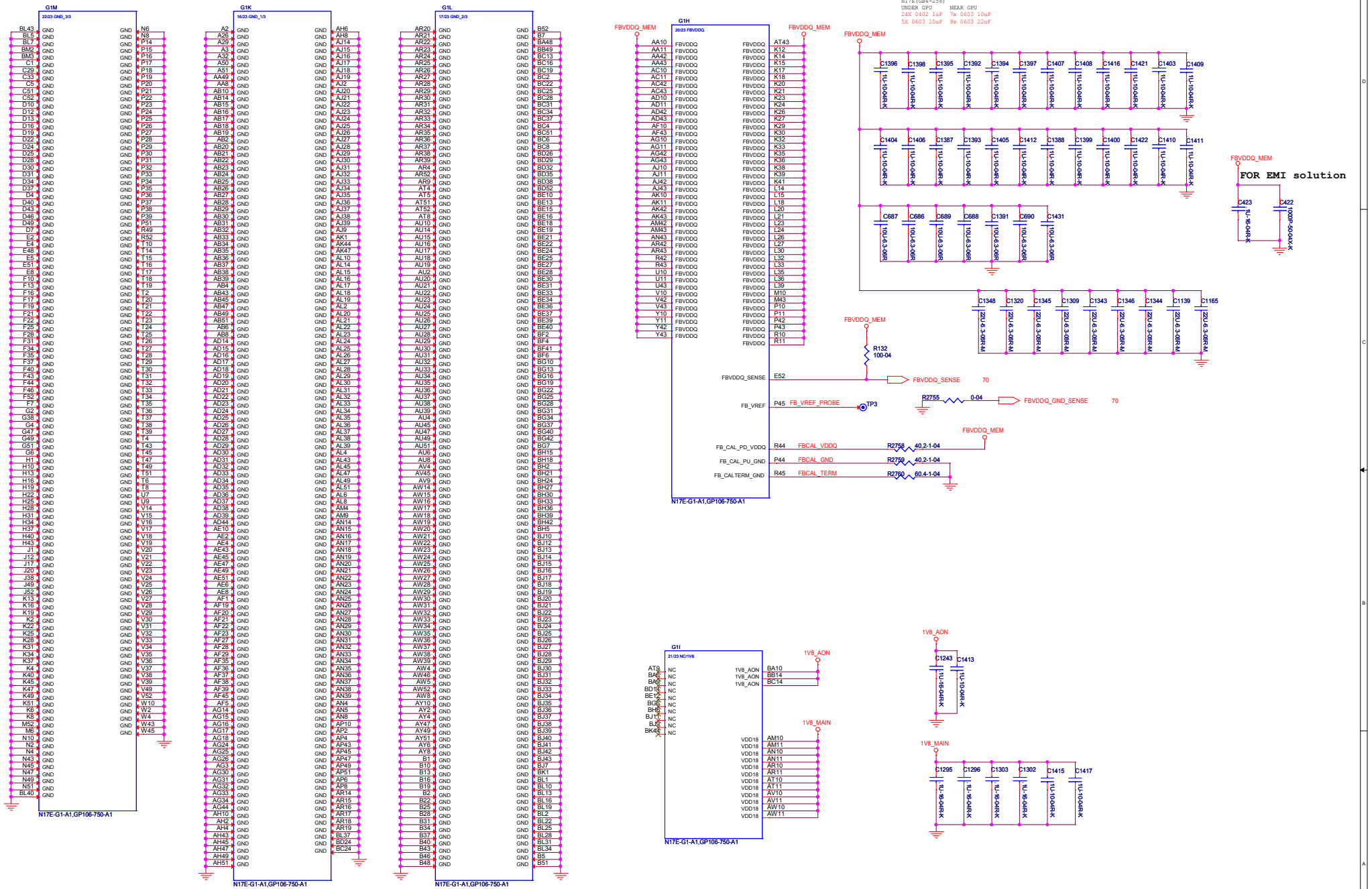

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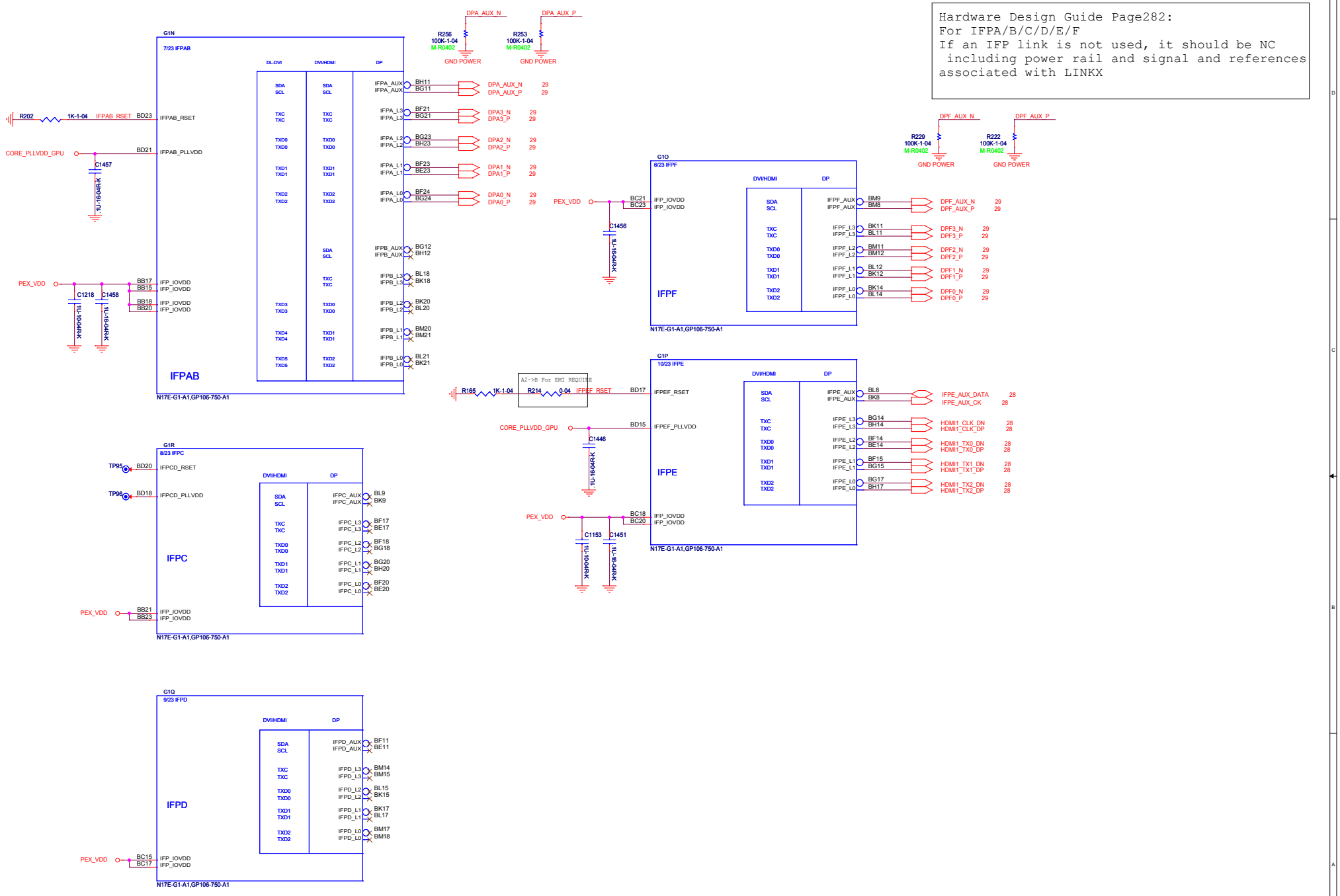
Title	NV-FBVDDQ_MEM/GND		
Size C	Document Number GK5CN6X	Rev V A	
Date: Tuesday, February 06, 2018	Sheet 53 of 72		


Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX
G1N
7/23 IFPAB
IFPAB
N17E-G1-A1,GP106-750-A1
G1O
6/23 IFPF
IFPF
N17E-G1-A1,GP106-750-A1
G1P
10/23 IFPE
IFPE
N17E-G1-A1,GP106-750-A1
G1R
8/23 IFPC
IFPC
N17E-G1-A1,GP106-750-A1
G1Q
9/23 IFPD
IFPD
N17E-G1-A1,GP106-750-A1
DL-DVI
DVI/HDMI
DP
DPA_AUX_N
DPA_AUX_P
DPF_AUX_N
DPF_AUX_P
GND POWER
IFPAB_RSET
IFPAB_PLLVDD
IFPCD_RSET
IFPCD_PLLVDD
IFPEF_RSET
IFPEF_PLLVDD
PEX_VDD
CORE_PLLVDD_GPU
IFP_IOVDD
A2->B For EMI REQUIRE
IFPE_AUX_DATA
IFPE_AUX_CK
HDMI1_CLK_DN
HDMI1_CLK_DP
HDMI1_TX0_DN
HDMI1_TX0_DP
HDMI1_TX1_DN
HDMI1_TX1_DP
HDMI1_TX2_DN
HDMI1_TX2_DP
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<OrgAddr4>
Title
NV-IPFA_B_C_D_E_F
Size C
Document Number
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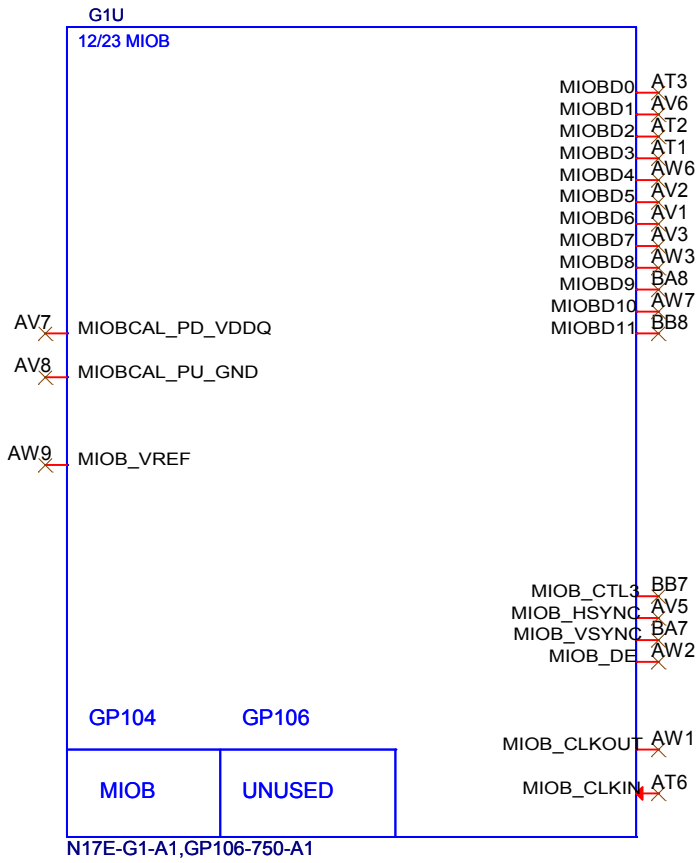

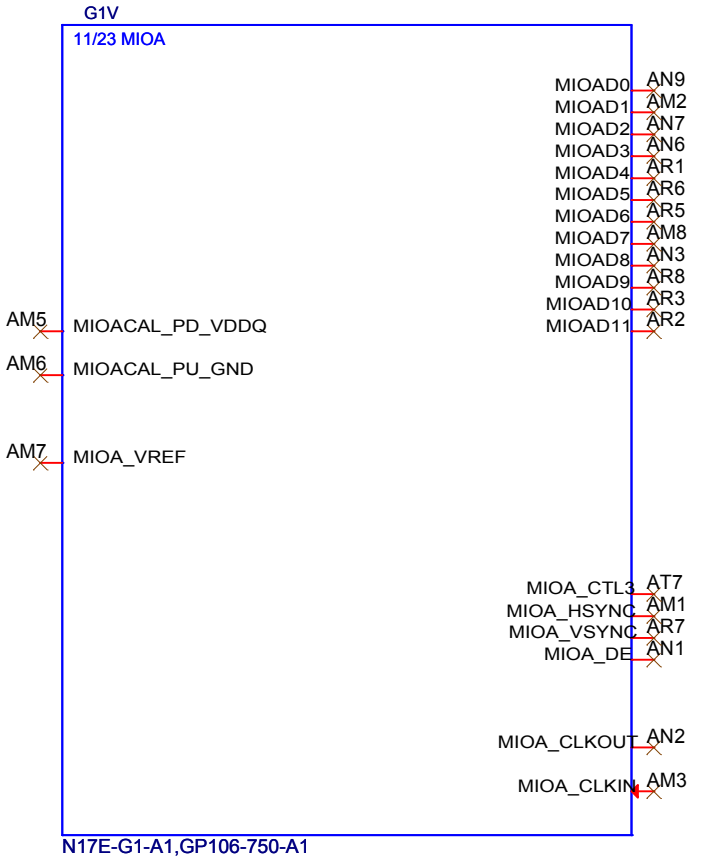

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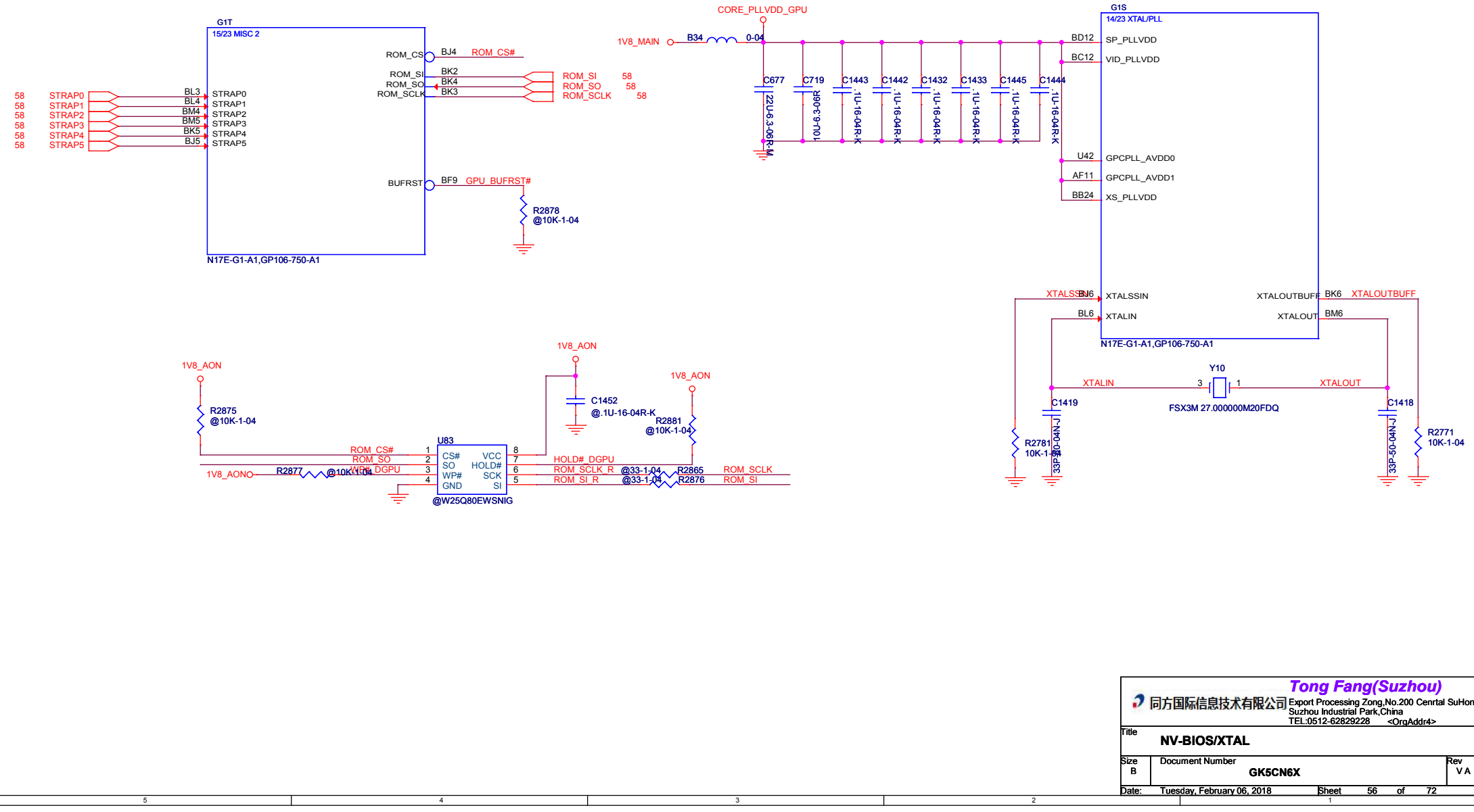
Title	NV-MIO	
Size A	Document Number GK5CN6X	Rev V A
Date: Tuesday, February 06, 2018	Sheet 55 of 72	



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Title	NV-BIOS/XTAL	
Size B	Document Number GK5CN6X	Rev V A
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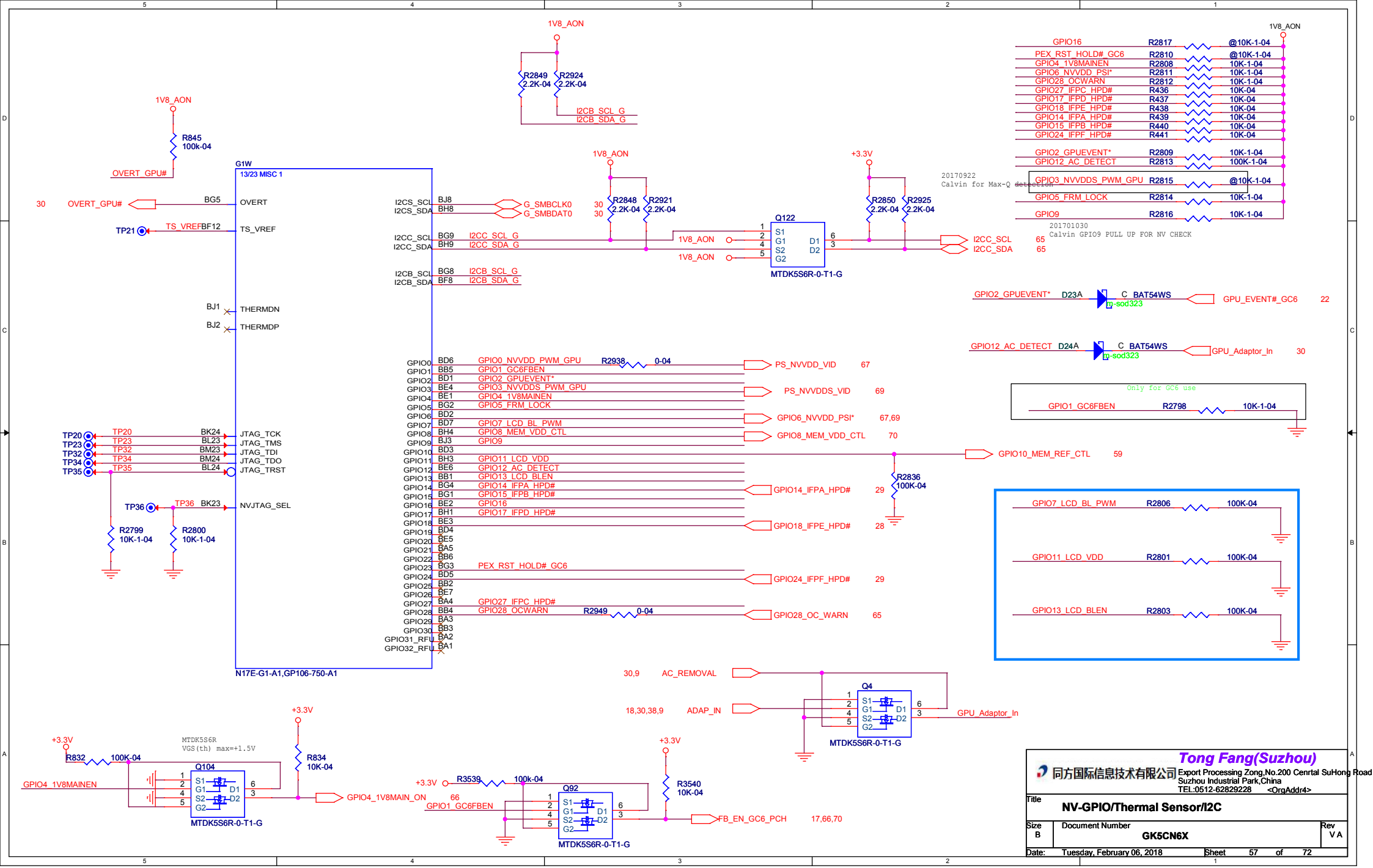
1V8_AON
R2849 2.2K-04
R2924 2.2K-04
I2CB_SCL_G
I2CB_SDA_G
R845 100k-04
OVERT_GPU#
G1W
13/23 MISC 1
30 OVERT_GPU# BG5 OVERT
TP21 TS_VREF BF12 TS_VREF
BJ1 THERMDN
BJ2 THERMDP
I2CS_SCL BJ8 G_SMBCLK0
I2CS_SDA BH8 G_SMBDAT0
I2CC_SCL BG9 I2CC_SCL_G
I2CC_SDA BH9 I2CC_SDA_G
I2CB_SCL BG8 I2CB_SCL_G
I2CB_SDA BF8 I2CB_SDA_G
R2848 2.2K-04
R2921 2.2K-04
Q122
MTDK5S6R-0-T1-G
+3.3V
R2850 2.2K-04
R2925 2.2K-04
I2CC_SCL 65
I2CC_SDA 65
20170922
Calvin for Max-Q detection
201701030
Calvin GPIO9 PULL UP FOR NV CHECK
GPIO16 R2817 @10K-1-04
PEX_RST_HOLD#_GC6 R2810 @10K-1-04
GPIO4_1V8MAINEN R2808 10K-1-04
GPIO6_NVVDD_PSI* R2811 10K-1-04
GPIO28_OCWARN R2812 10K-1-04
GPIO27_IFPC_HPD# R436 10K-04
GPIO17_IFPD_HPD# R437 10K-04
GPIO18_IFPE_HPD# R438 10K-04
GPIO14_IFPA_HPD# R439 10K-04
GPIO15_IFPB_HPD# R440 10K-04
GPIO24_IFPF_HPD# R441 10K-04
GPIO2_GPUEVENT* R2809 10K-1-04
GPIO12_AC_DETECT R2813 100K-1-04
GPIO3_NVVDDS_PWM_GPU R2815 @10K-1-04
GPIO5_FRM_LOCK R2814 10K-1-04
GPIO9 R2816 10K-1-04
GPIO2_GPUEVENT* D23A C BAT54WS GPU_EVENT#_GC6 22
GPIO12_AC_DETECT D24A C BAT54WS GPU_Adaptor_In 30
m-sod323
GPIO0 BD6 GPIO0_NVVDD_PWM_GPU R2938 0-04 PS_NVVDD_VID 67
GPIO1 BB5 GPIO1_GC6FBEN
GPIO2 BD1 GPIO2_GPUEVENT*
GPIO3 BE4 GPIO3_NVVDDS_PWM_GPU PS_NVVDDS_VID 69
GPIO4 BE1 GPIO4_1V8MAINEN
GPIO5 BG2 GPIO5_FRM_LOCK
GPIO6 BD2 GPIO6_NVVDD_PSI* 67,69
GPIO7 BD7 GPIO7_LCD_BL_PWM
GPIO8 BH4 GPIO8_MEM_VDD_CTL GPIO8_MEM_VDD_CTL 70
GPIO9 BJ3 GPIO9
GPIO10 BD3 GPIO10_MEM_REF_CTL 59
GPIO11 BH3 GPIO11_LCD_VDD
GPIO12 BE6 GPIO12_AC_DETECT
GPIO13 BB1 GPIO13_LCD_BLEN
GPIO14 BG4 GPIO14_IFPA_HPD# GPIO14_IFPA_HPD# 29
GPIO15 BG1 GPIO15_IFPB_HPD#
GPIO16 BE2 GPIO16
GPIO17 BH1 GPIO17_IFPD_HPD#
GPIO18 BE3 GPIO18_IFPE_HPD# GPIO18_IFPE_HPD# 28
GPIO19 BD4
GPIO20 BE5
GPIO21 BA5
GPIO22 BB6
GPIO23 BG3 PEX_RST_HOLD#_GC6
GPIO24 BD5 GPIO24_IFPF_HPD# GPIO24_IFPF_HPD# 29
GPIO25 BB2
GPIO26 BE7
GPIO27 BA4 GPIO27_IFPC_HPD#
GPIO28 BB4 GPIO28_OCWARN R2949 0-04 GPIO28_OC_WARN 65
GPIO29 BA3
GPIO30 BB3
GPIO31_RFU BA2
GPIO32_RFU BA1
R2836 100K-04
Only for GC6 use
GPIO1_GC6FBEN R2798 10K-1-04
GPIO7_LCD_BL_PWM R2806 100K-04
GPIO11_LCD_VDD R2801 100K-04
GPIO13_LCD_BLEN R2803 100K-04
N17E-G1-A1,GP106-750-A1
TP20 TP20 BK24 JTAG_TCK
TP23 TP23 BL23 JTAG_TMS
TP32 TP32 BM23 JTAG_TDI
TP34 TP34 BM24 JTAG_TDO
TP35 TP35 BL24 JTAG_TRST
TP36 TP36 BK23 NVJTAG_SEL
R2799 10K-1-04
R2800 10K-1-04
30,9 AC_REMOVAL
18,30,38,9 ADAP_IN
Q4
MTDK5S6R-0-T1-G
GPU_Adaptor_In
+3.3V
R832 100K-04
MTDK5S6R
VGS(th) max=+1.5V
Q104
MTDK5S6R-0-T1-G
R834 10K-04
GPIO4_1V8MAINEN
GPIO4_1V8MAIN_ON
R3539 100K-04
66 GPIO1_GC6FBEN
Q92
MTDK5S6R-0-T1-G
R3540 10K-04
FB_EN_GC6_PCH 17,66,70
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Title
NV-GPIO/Thermal Sensor/I2C
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	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

ROW INDEX	STRAP PIN		
	ROM_SO	ROM_SI	ROM_SCLK
15	L	L	L
14	L	L	H
13	L	H	L
12	L	H	H
11	H	L	L
10	H	L	H
8	H	H	H
0	H	H	M

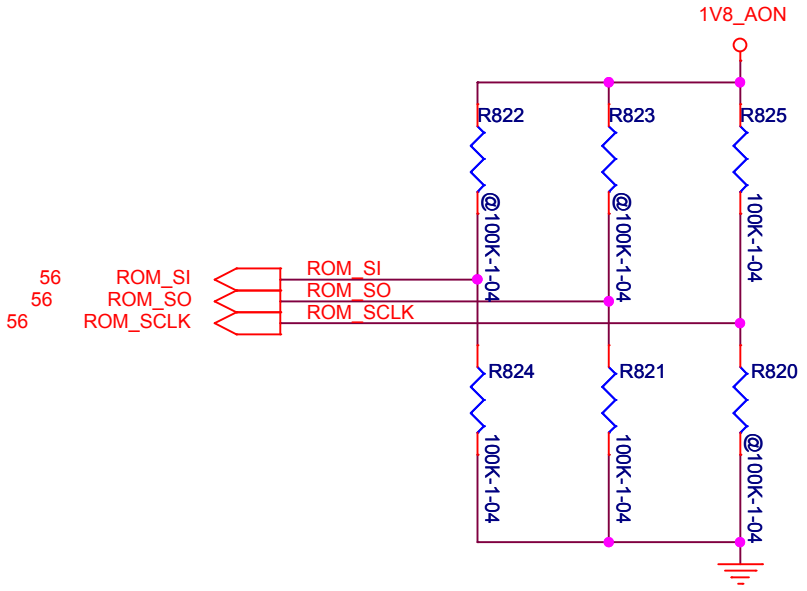
Display Link 15

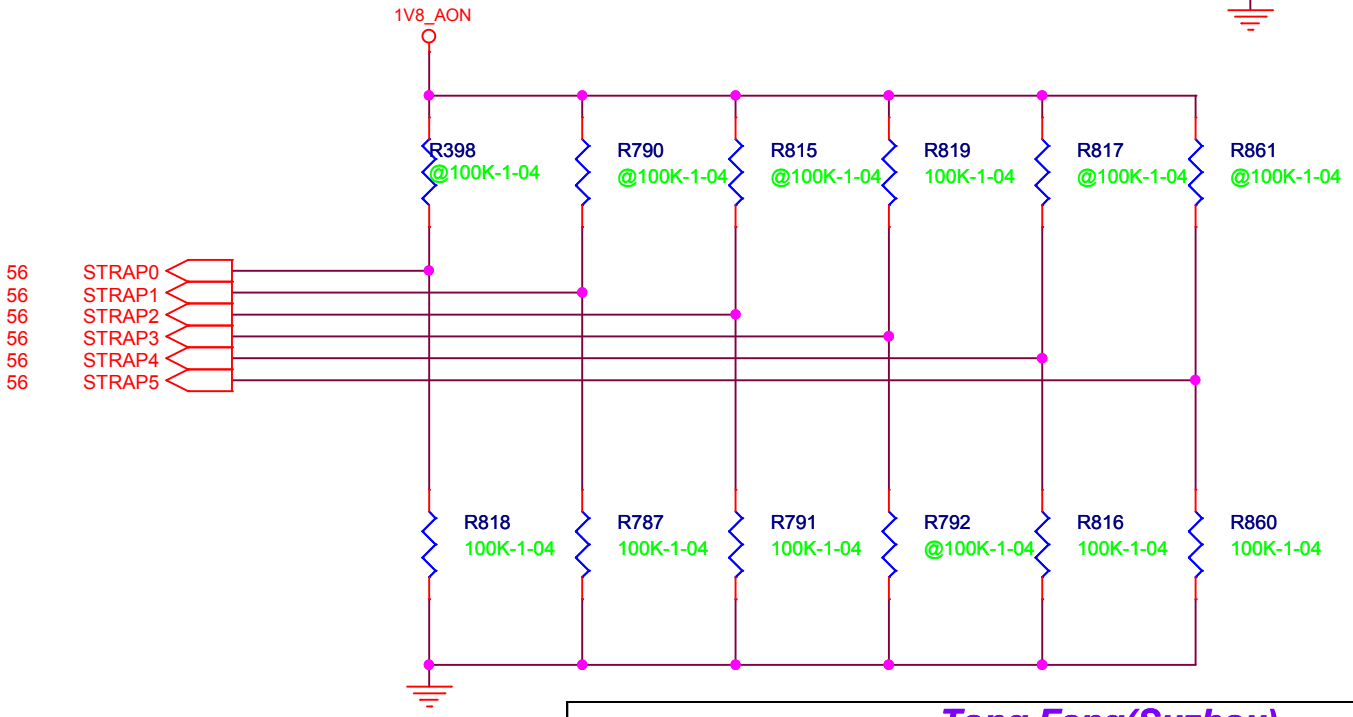
TOTAL LINK	TOTAL EN AUDIO	ROW INDEX
4	4	15
3	3	14
2	2	12
3	2	12
4	3	13

Based on RVL_07916_001_V10 JUNE 2017

GDDR5							
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0	
8Gb	Samsung	K4G80325FB-HC25 B-die	0X0	L	L	L	1.35V/1.55V
8Gb	Micron	MT51J256M32HF-80:A A-die	0X1	L	L	H	1.35V/1.50V
8Gb	Hynix	H5GQ8H24MJR-R4C M-die	0X2	L	H	L	1.35V/1.55V
4Gb	Samsung	K4G41325FE-HC25 E-die	0X7	H	H	H	1.35V/1.55V
4Gb	Hynix	H5GQ4H24AJR-R4C A-die	0X6	H	H	L	1.35V/1.55V
4Gb	Micron						

POWER





Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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Title: **STRAP**

Size: A | Document Number: **GK5CN6X** | Rev: V A

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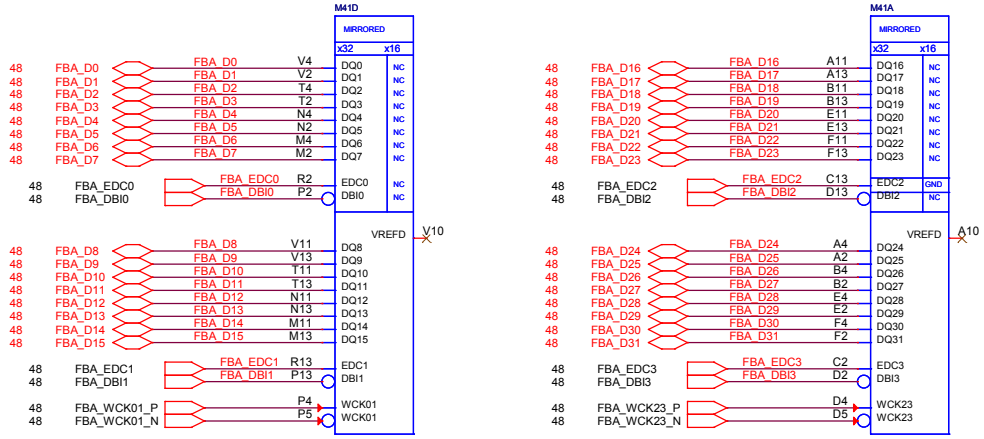
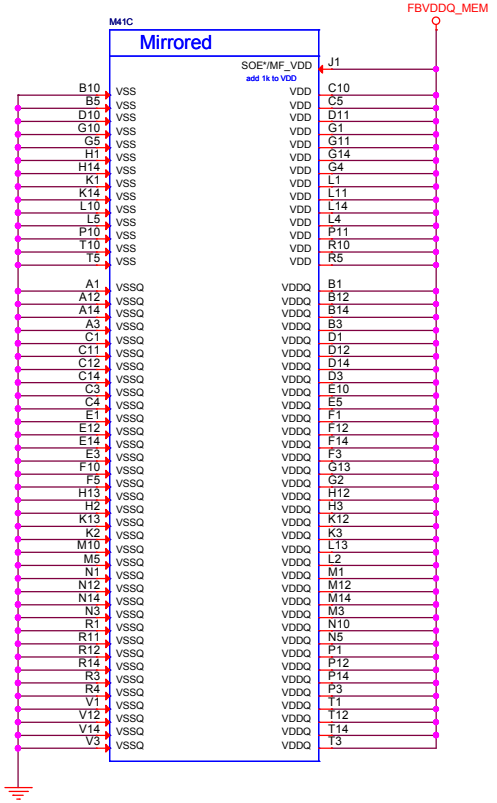
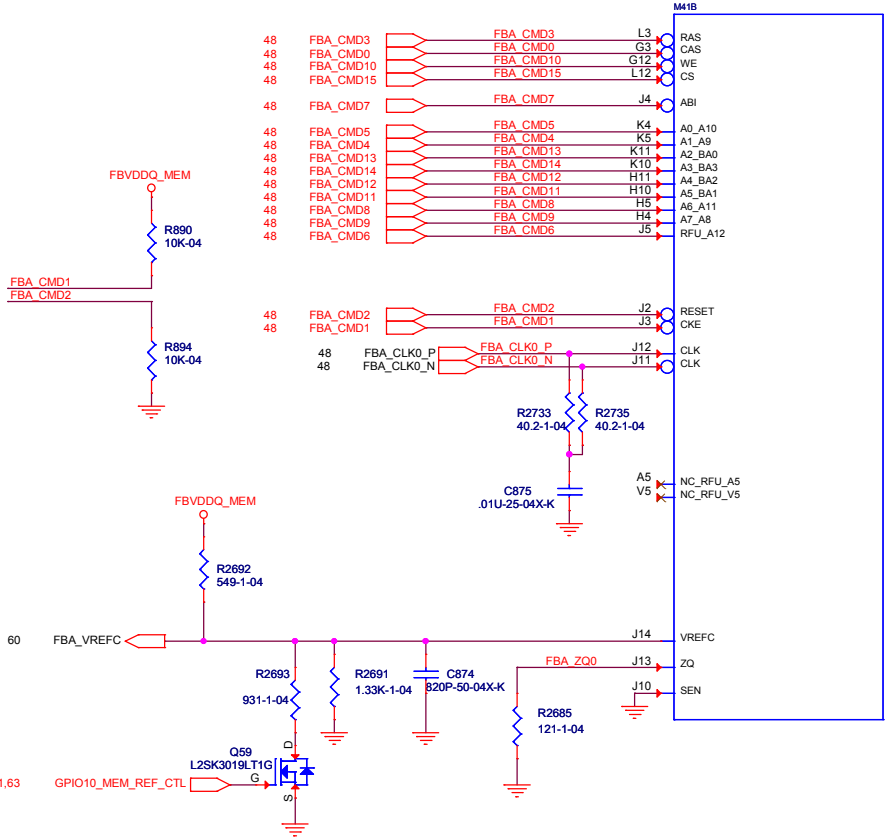
MEM_FBA[31_0]

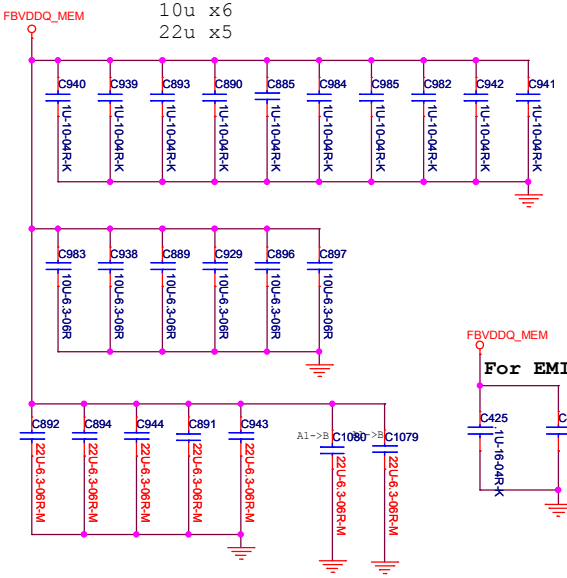
Maximum VRAM case Temp is 85 celsius degree



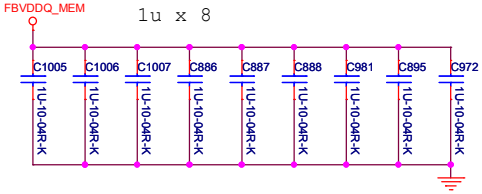




Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8



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Title	Frame Buffer A0-VRAM	
Size: Custom	Document Number: GK5CN6X	Rev: V A
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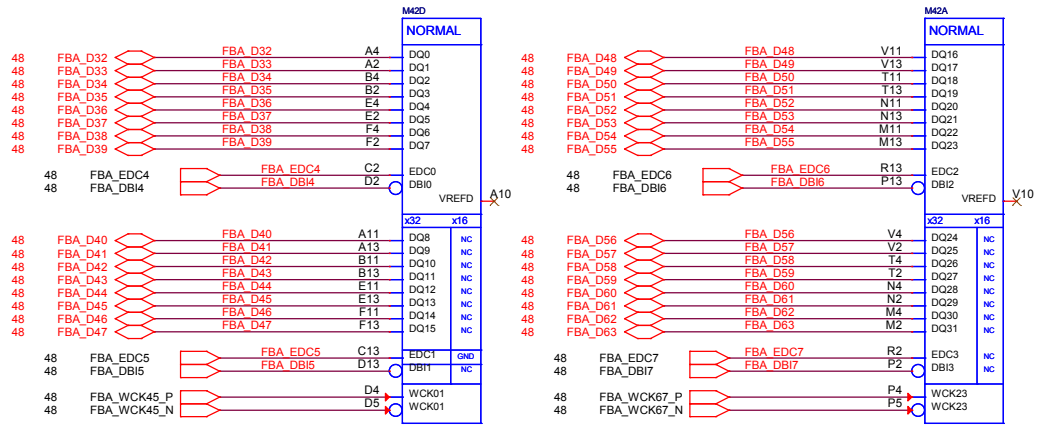
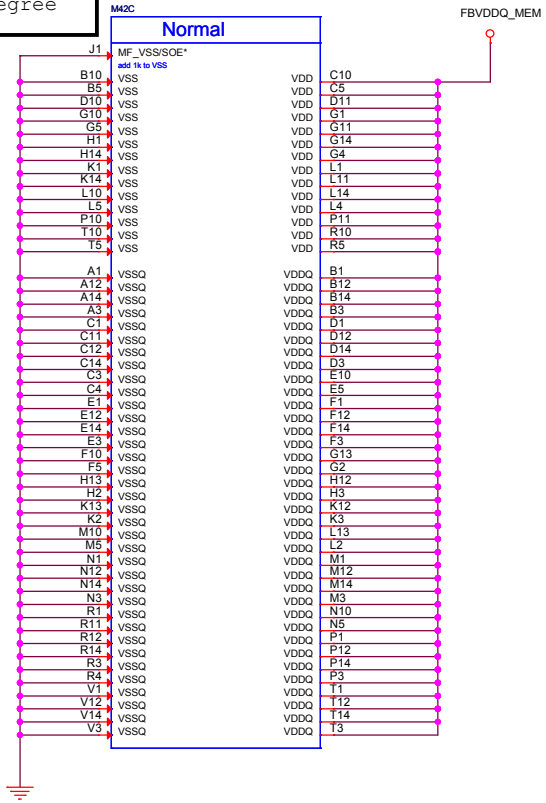
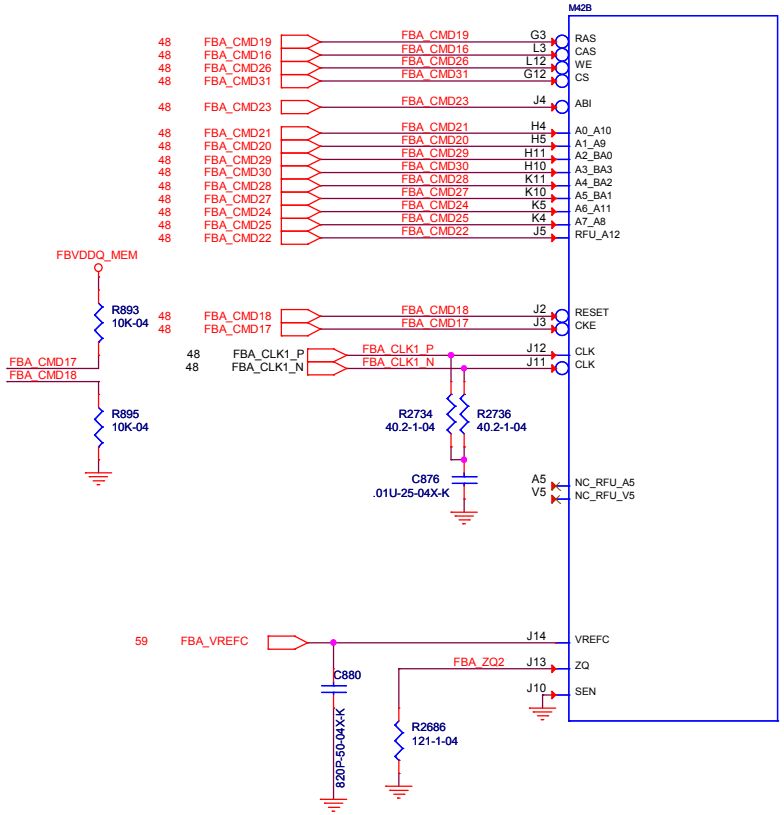
MEM_FBA[63_32]

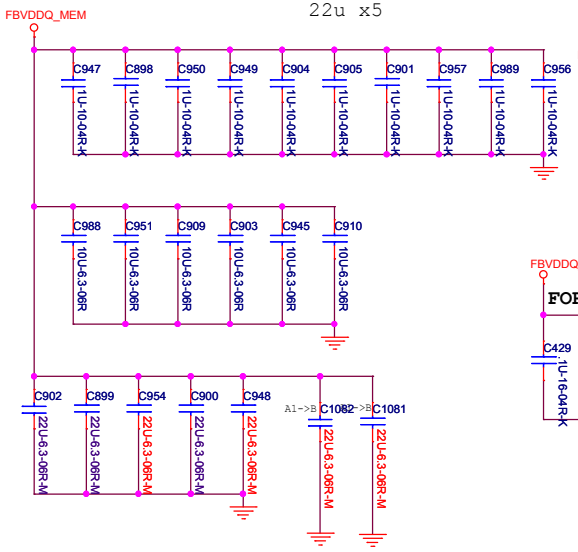
Maximum VRAM case Temp is 85 celcisus degree



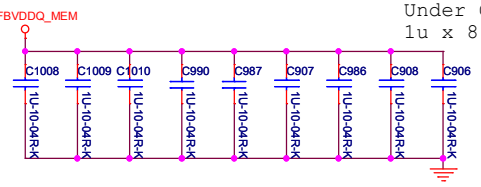


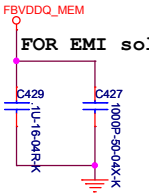


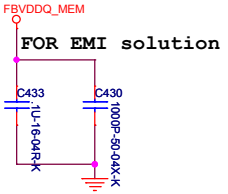
Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8







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Title: Frame Buffer A1-VRAM

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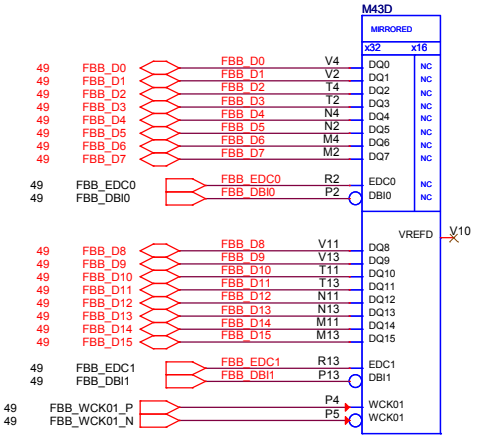
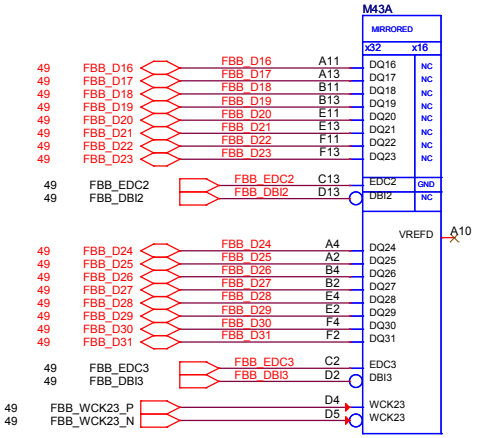
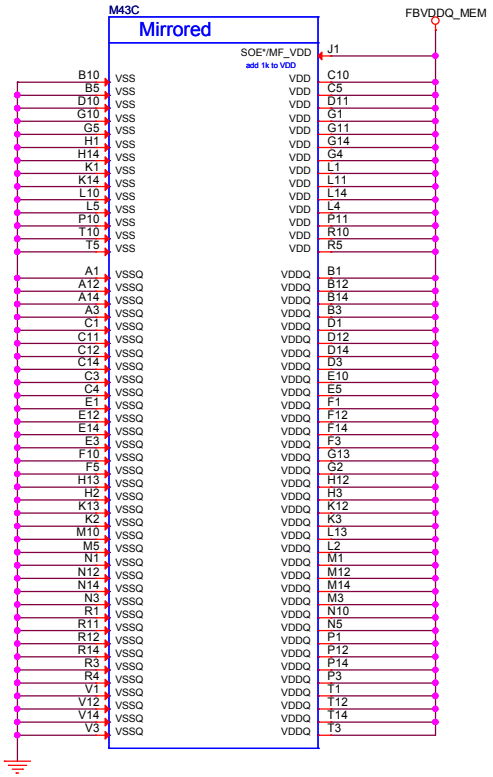
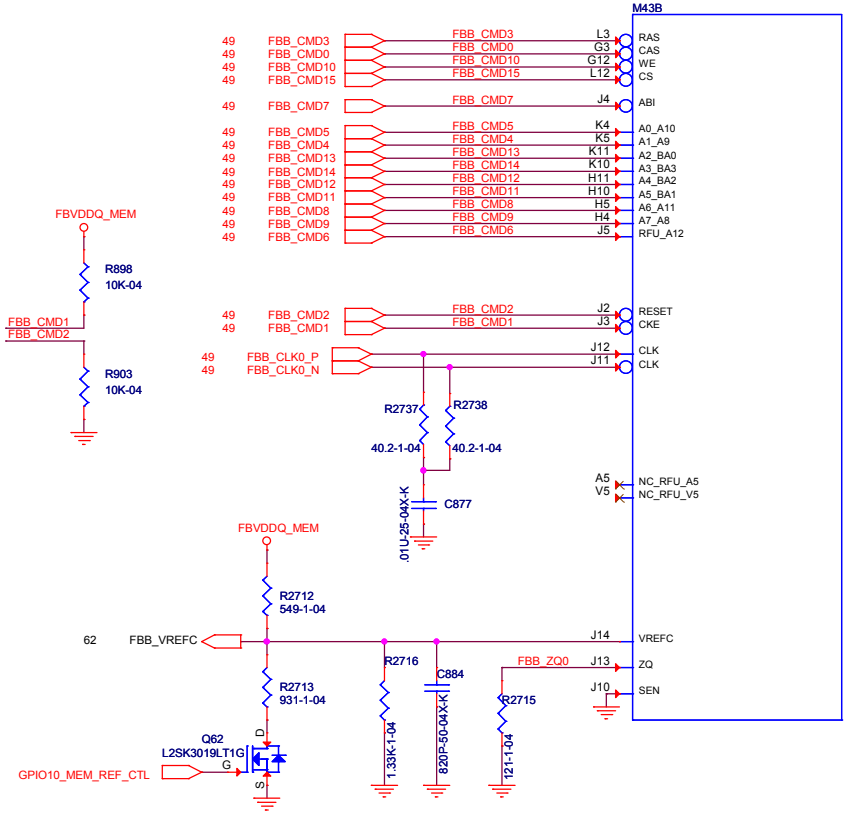
MEM_FBB[31_0]

Maximum VRAM case Temp is 85 celcisus degree

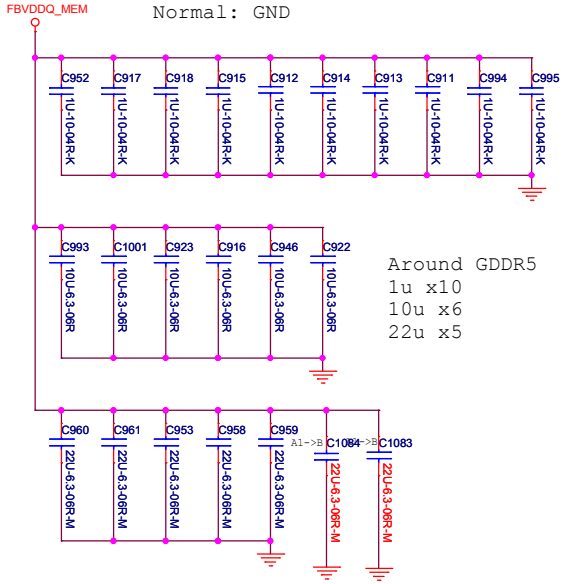






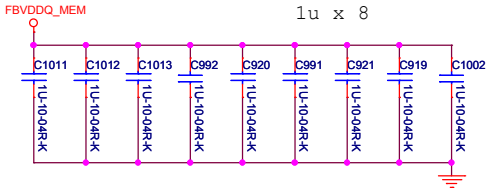


Mirrored: Pull high to VDDQ
Normal: GND



Around GDDR5
1u x10
10u x6
22u x5

Under GDDR5
1u x 8



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Title: Frame Buffer B0-VRAM

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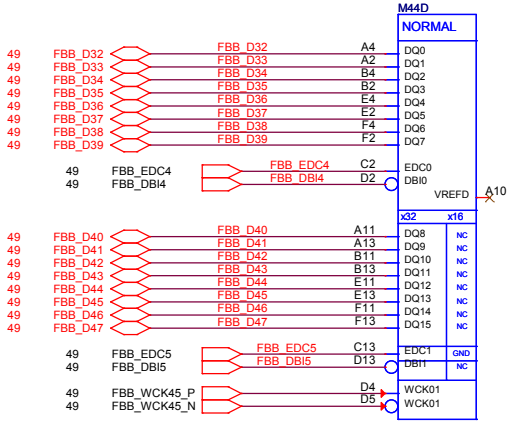
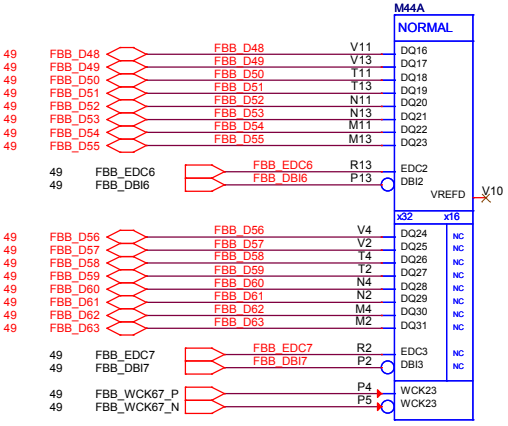
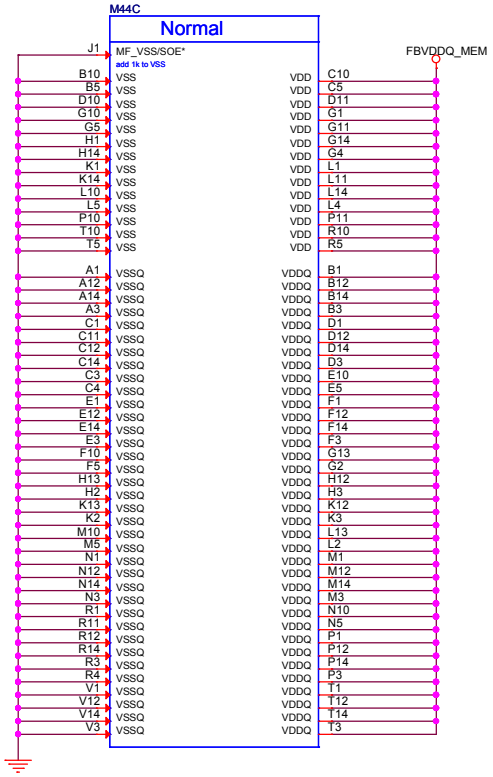
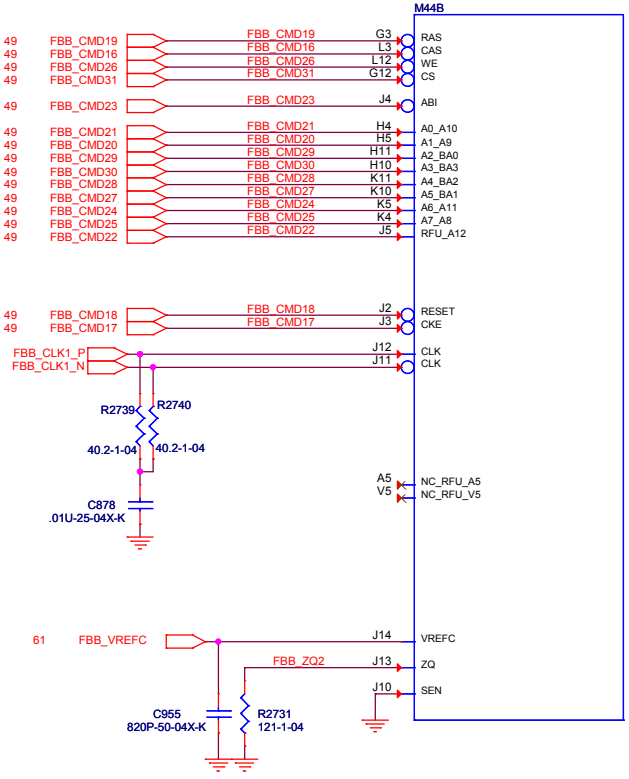
MEM_FBB[63_32]

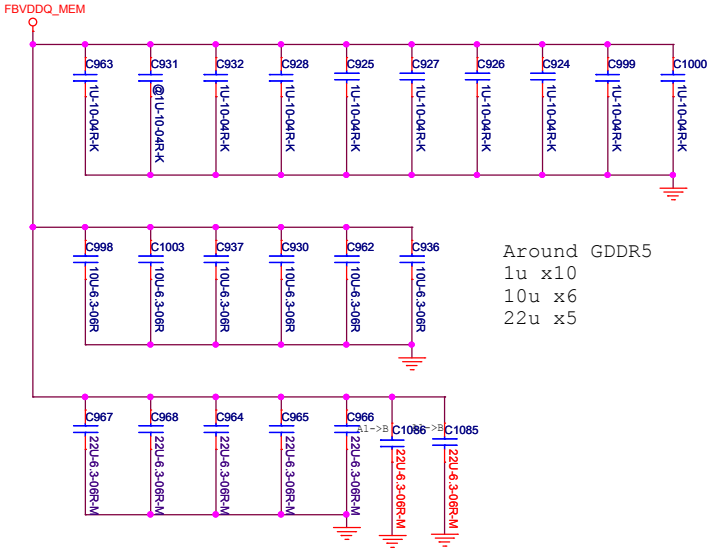
Maximum VRAM case Temp is 85 celcisus degree



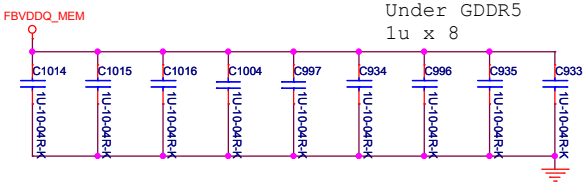








Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8

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Title: Frame Buffer B1-VRAM			
Size: Custom	Document Number: GK5CN6X		Rev: V A
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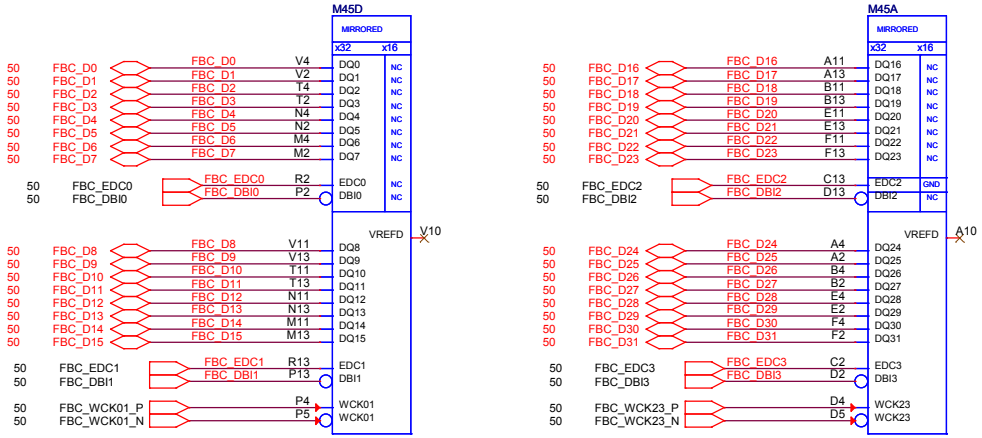
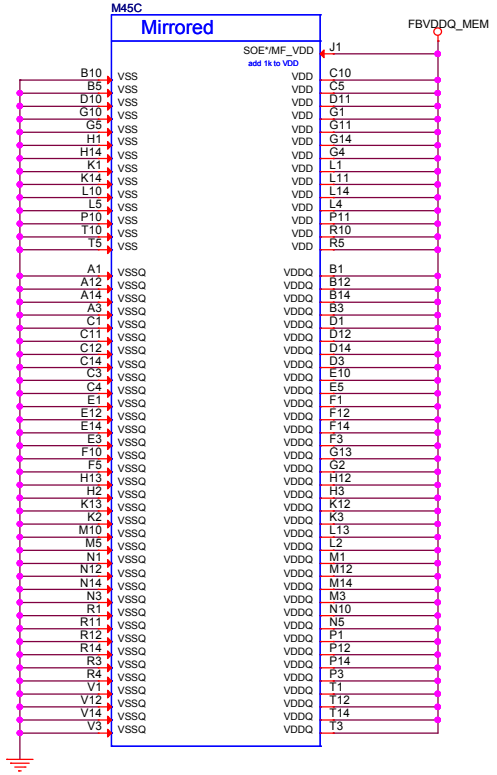
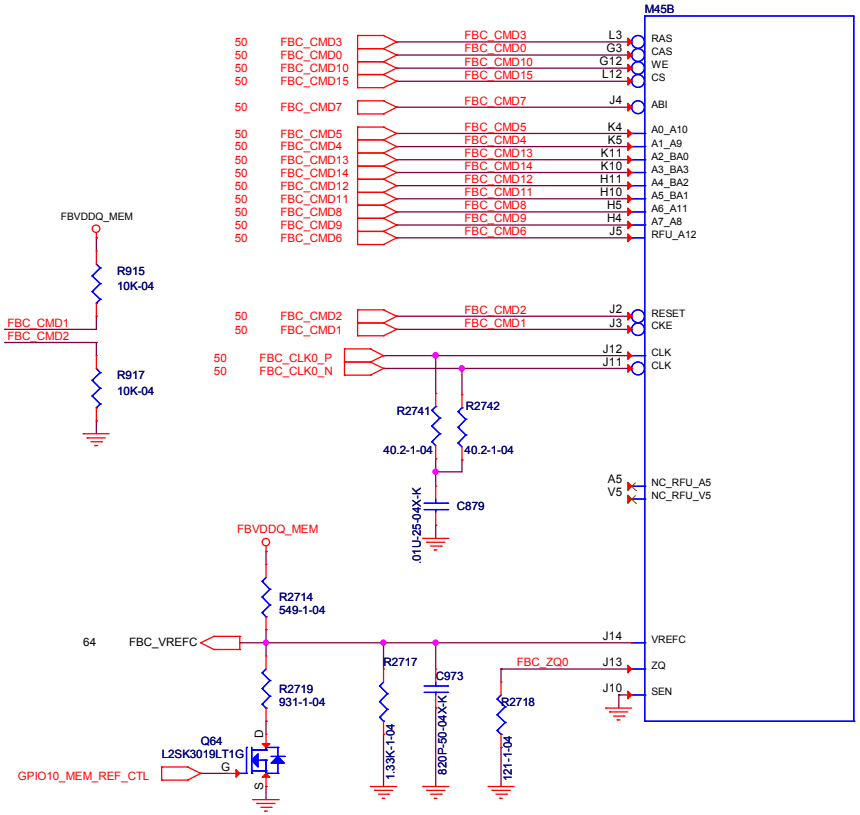
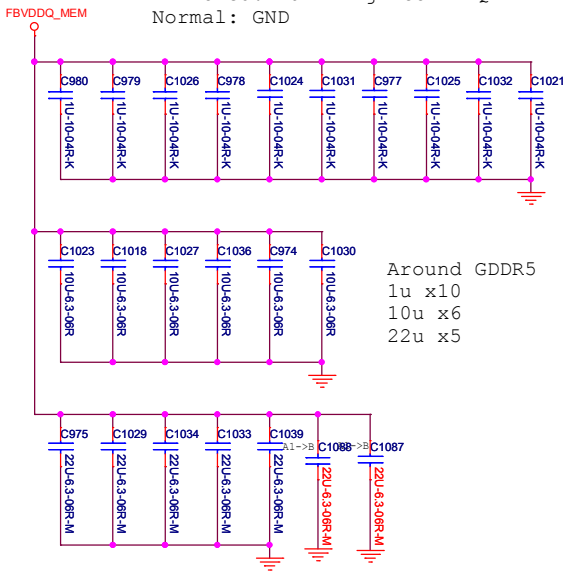
MEM_FBC[31_0]



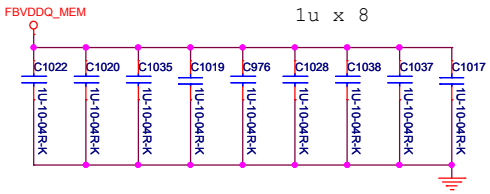




Mirrored: Pull high to VDDQ
Normal: GND



Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8

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Title: Frame Buffer C0-VRAM

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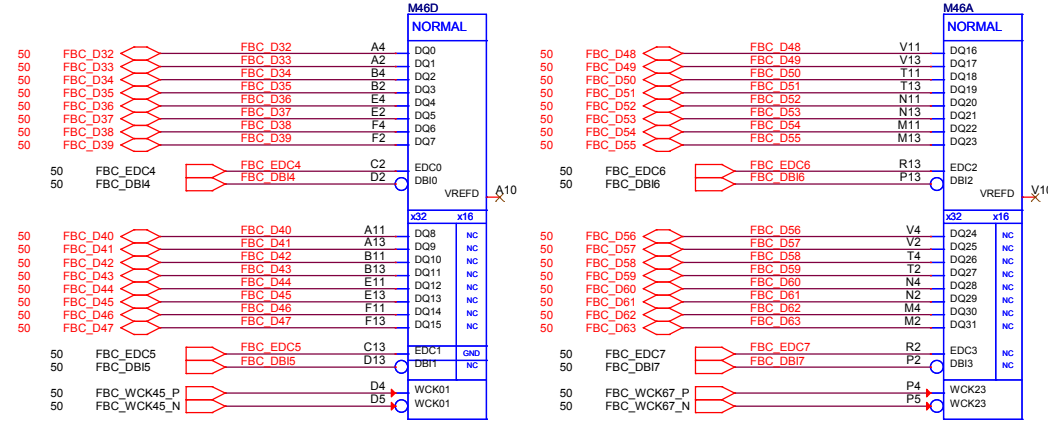
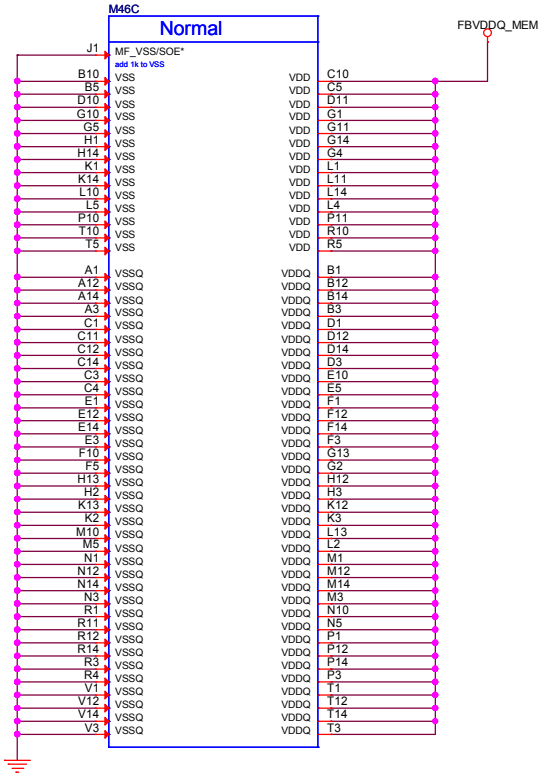
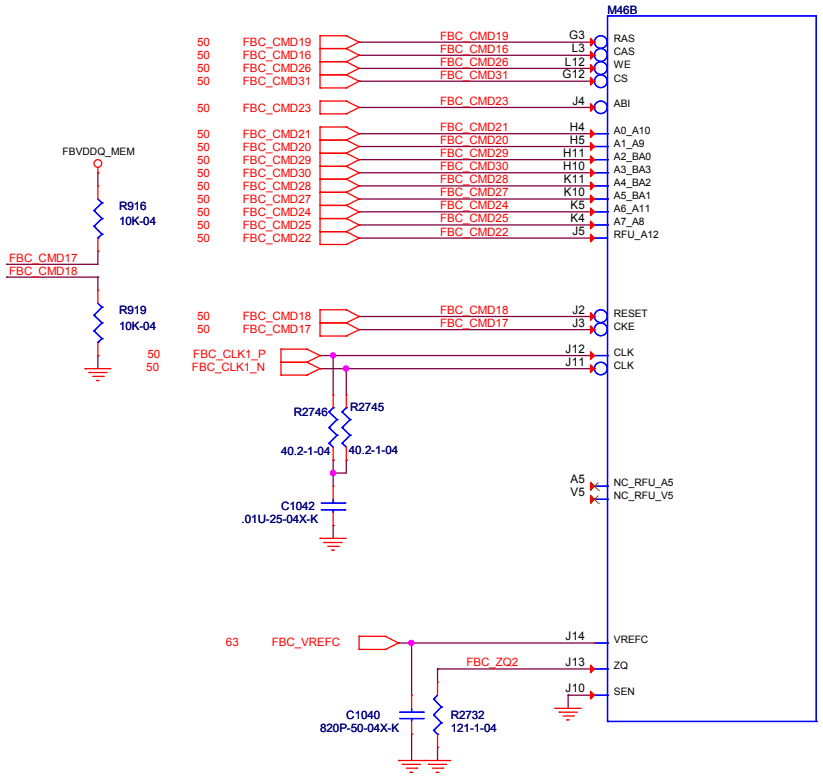
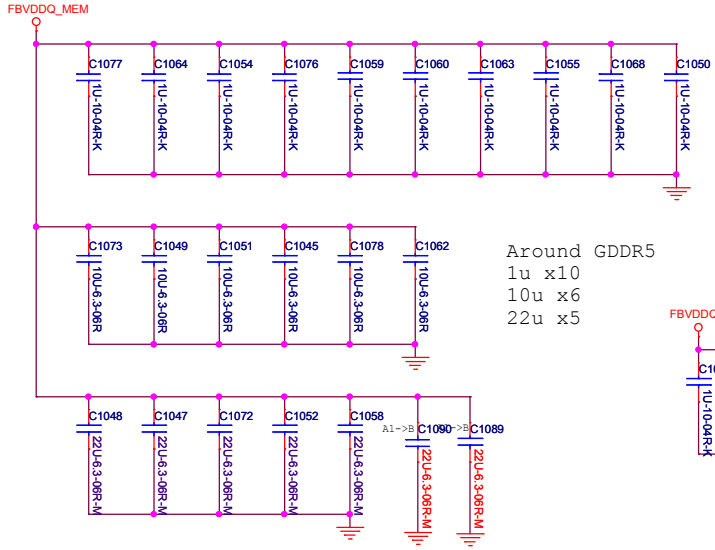
MEM_FBC[63_32]

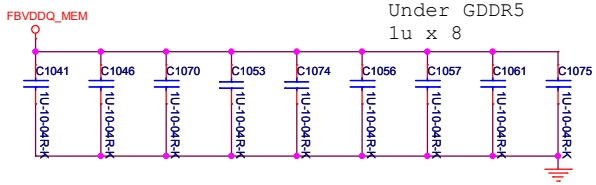








Around GDDR5
1u x10
10u x6
22u x5



Under GDDR5
1u x 8

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Title: **Frame Buffer C1-VRAM**

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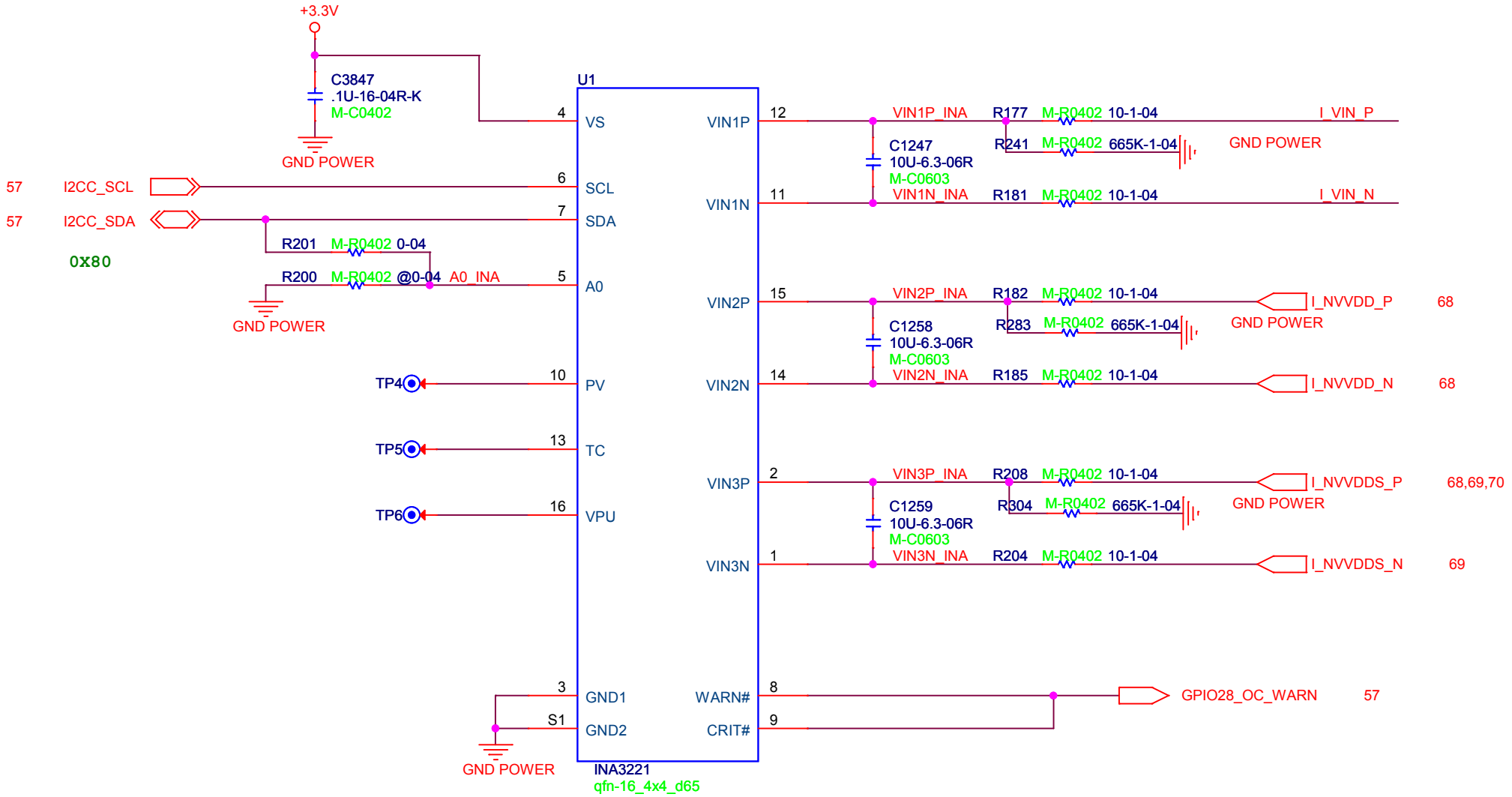

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Title: **PWR MEASUREMENT**

Size	Document Number	Rev
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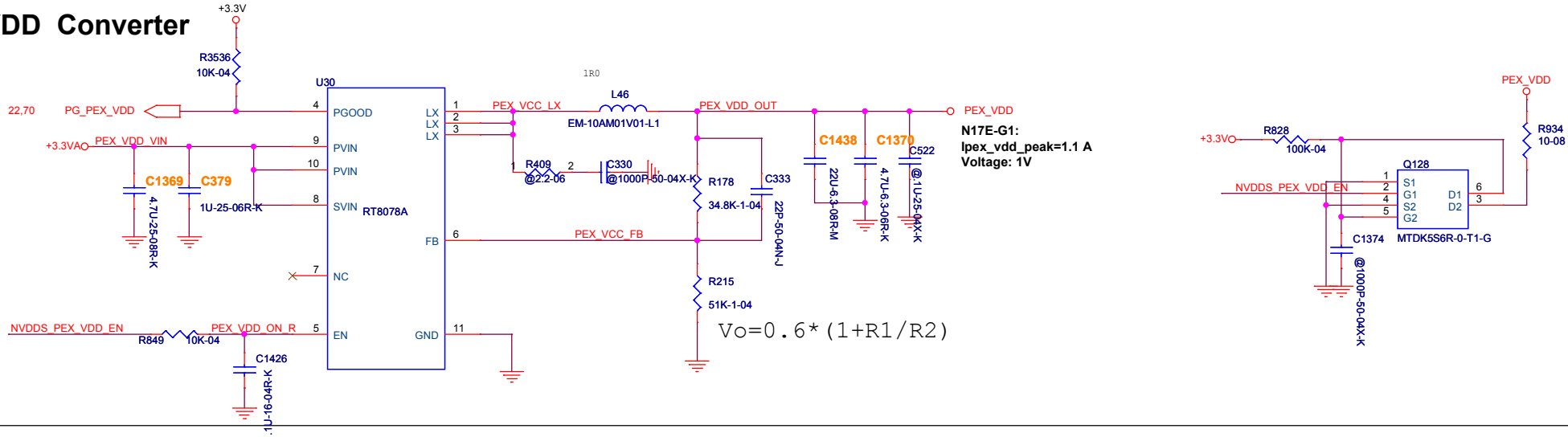
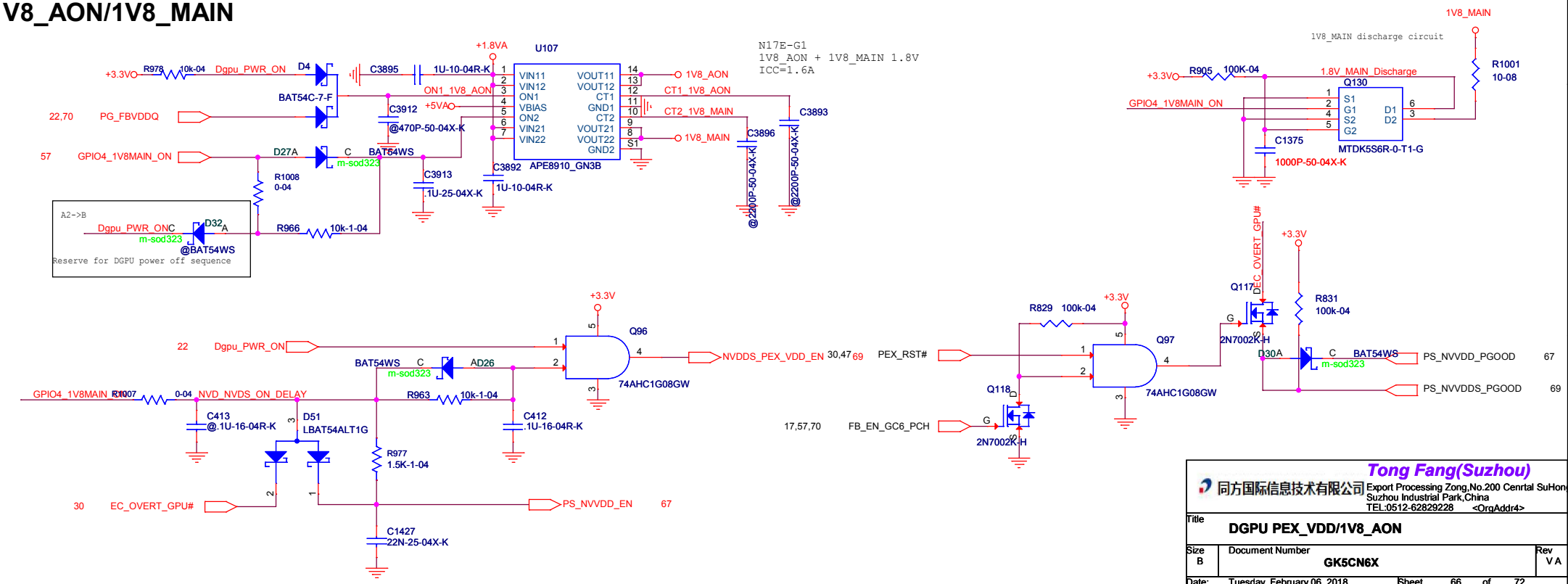
PEX_VDD Converter



1V8_AON/1V8_MAIN



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Title	DGPU PEX_VDD/1V8_AON	
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BOM option

uP9509	UP1642T
R971=300K R955=15Kohm C2552=1000pF R950=30K R2880=22K R979=1Kohm R984=1Kohm R985=510ohm	R971=82K R955=16Kohm C2552=4700pF R950=NC R2880=NC R979=11.3Kohm R984=11.3Kohm R985=11.3Kohm

PSI	Mode
1.8V	Full phase CCM
0.9V	single phase CCM
0	Single-Phase DCM

20171128
Calvin

VEN_L<=0.6V

VEN_H>=1.2V

PVCC POR Threshold=4.1V

TON:Set the on-time of the upper MOSFET

U722 uP1642T OPENVREG

PWM VID:
VID=0% Vout=0.7V(MIN)
VID=100% Vout=1.2V(MAX)

VREF=2V
Isource=10mA

REFIN=Vcore

Rg2	slew rate
15K	150us
20K	500us
30K	1ms
Open	1.5ms

Place Near Power chip

Place Near Power chip

2 Phase design
R99: Mount
R985: NC

Layout:
close to controller

20170922
Calvin

20170925
Calvin

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Title		
DGPU NVVDD IC		
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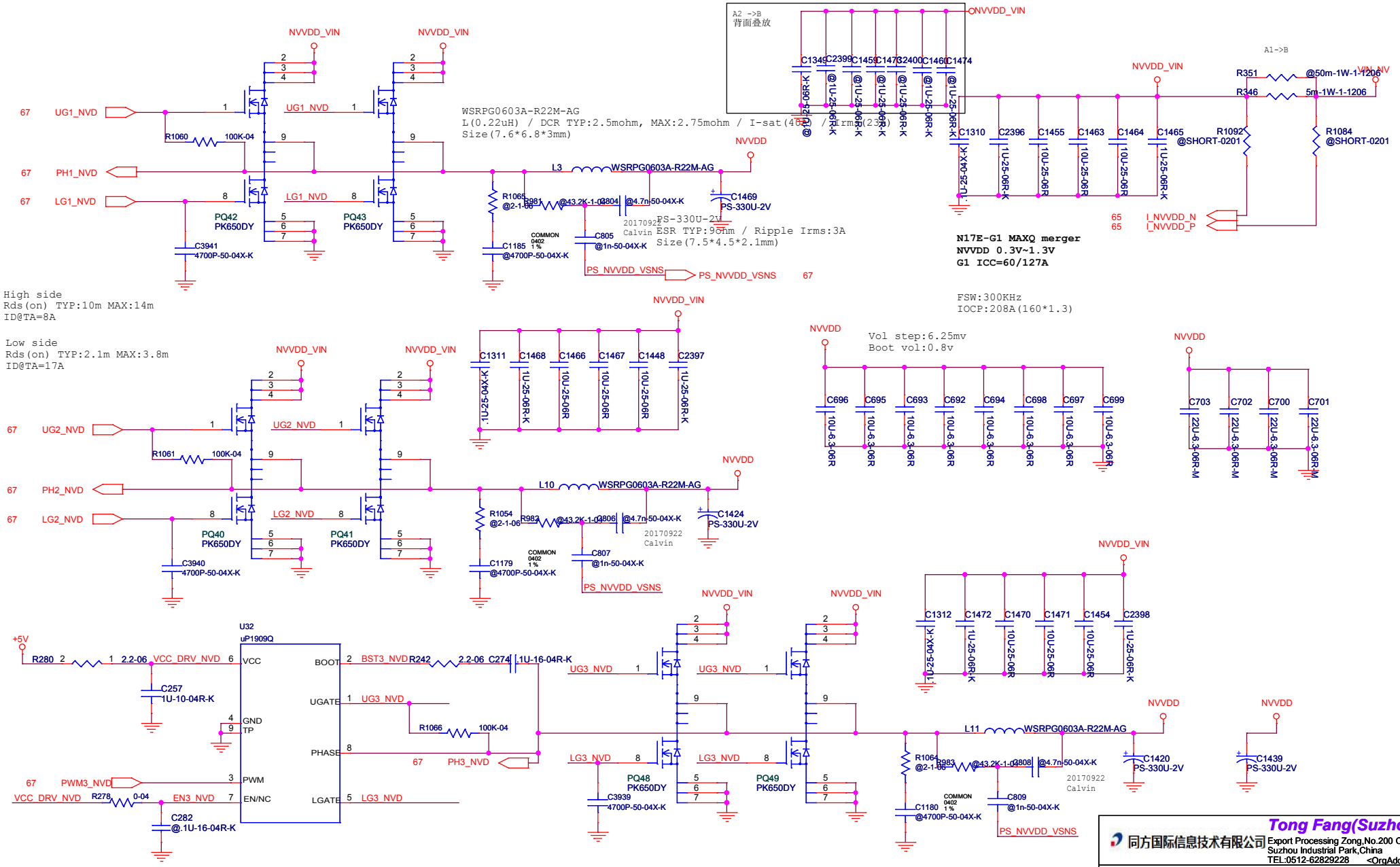

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Title	DGPU NVVDD POWER	
Size B	Document Number GK5CN6X	Rev V A
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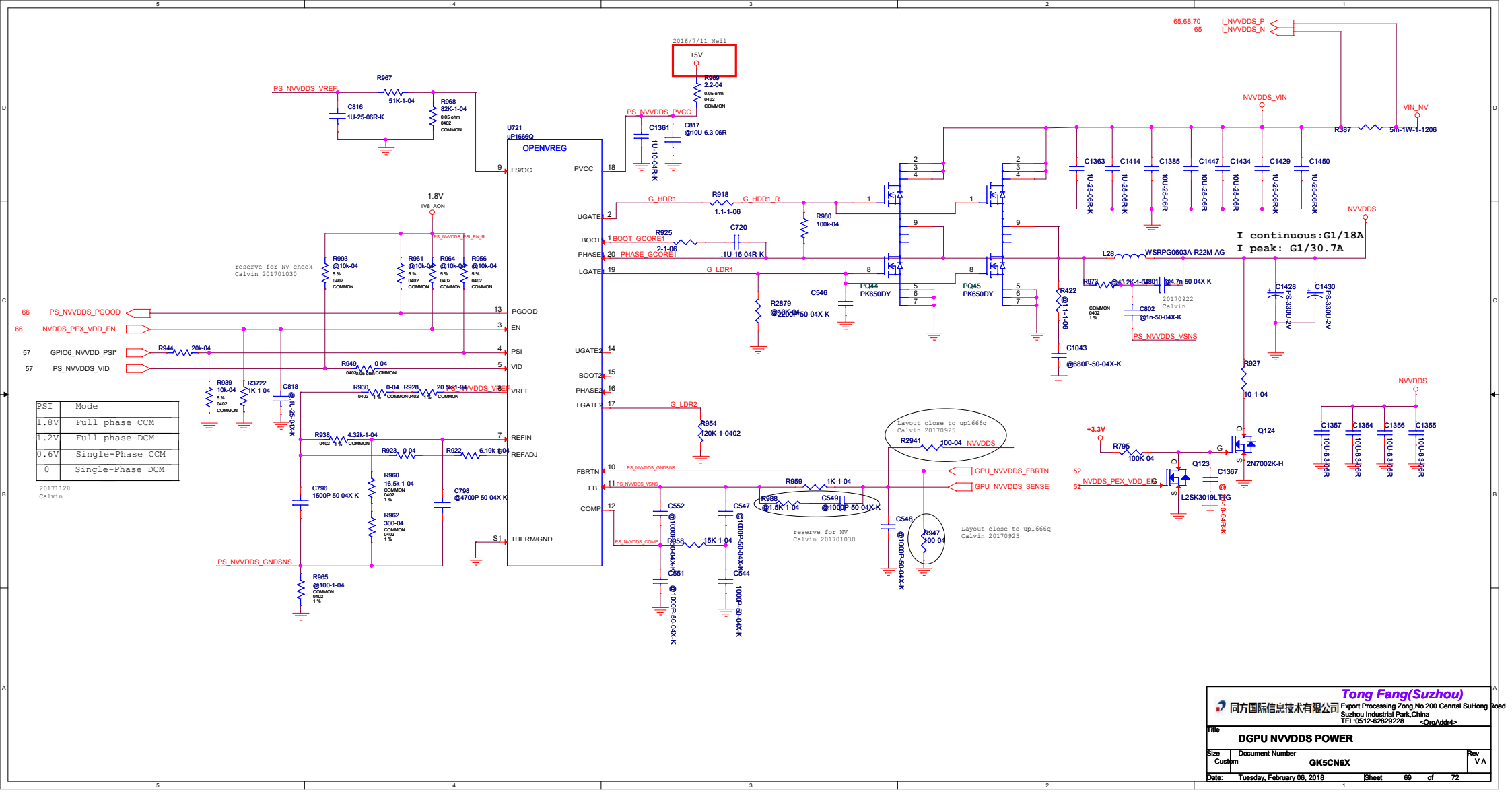

PSI	Mode
1.8V	Full phase CCM
1.2V	Full phase DCM
0.6V	Single-Phase CCM
0	Single-Phase DCM

20171128
Calvin

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Title: DGPU NVVDDS POWER

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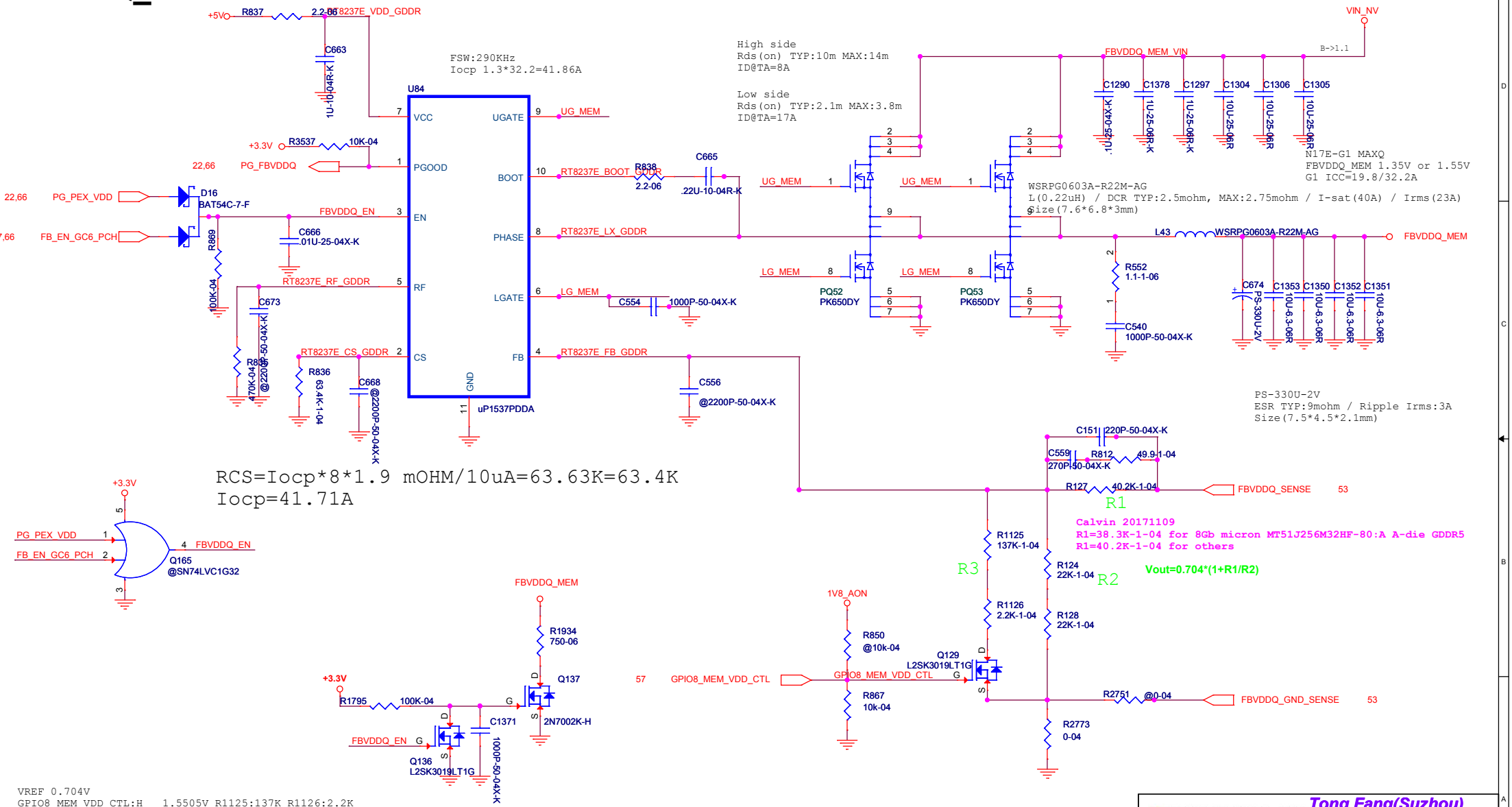
FBVDDQ_MEM



VREF 0.704V
GPIO8_MEM_VDD_CTL:H 1.5505V R1125:137K R1126:2.2K
GPIO8_MEM_VDD_CTL:H 1.5044V R1125:180K R1126:0K
GPIO8_MEM_VDD_CTL:L 1.3472V

NOTE! If use Micron 8Gb MT51J256M32HF-80:A GPIO8_MEM_VDD_CTL:H 1.5V

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Title	DGPU FBVDDQ_MEM	
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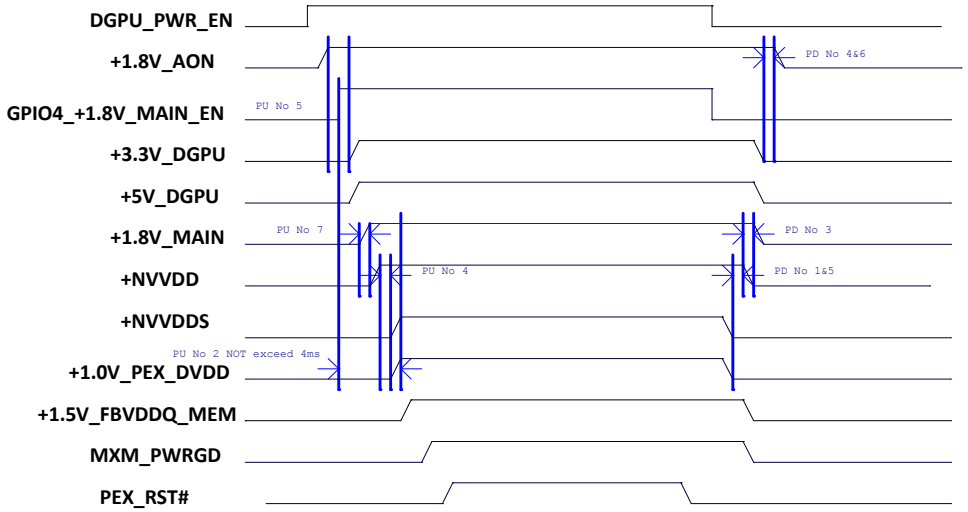
POWER SEQUENCE



POWER UP sequence is required:+1.8V_AON->+1.8V_MAIN->+NVVDD->+NVVDDS/+1.0V_PEX_DVDD->+1.5V_FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.t1 From +1.8V_MAIN_EN to +1.0V_PEX_DVDD/+NVVDD_PGOOD) must NOT exceed 4ms.
3.The ramp-up overshoot should not exceed the silicon reliability limit voltage
4.Power up +NVVDD must be 90% before +1.0V+PEX_DVDD and NVVDDS can start ramp up.
5.Power up +1.8V_AON must be 90% before 3.3V ramp up.
6.All 3.3V devices that connect to the GPU must be powered after +1.8V_AON ; GPU can't have any 3.3V leakage path before +1.8V_AON present.
7.The propagation delay between +1.8V_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.

POWER DOWN sequence is required
1.+NVVDDS/+1.0V_PEX_DVDD must ramp down before NVVDD.
2.All other power rails can ramp down together with NVVDD.
3.+1.8V_MAIN must power down after NVVDD power down
3.The progapation delay between +1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down NVVDDS and +1.0V_PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down 3.3V must be less than 10% before +1.8V_AON can start ramp down.

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Title	DGPU POWER SEQUENCING	
Size C	Document Number GK5CN6X	Rev V A
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Date

Chang History

20171026
Modify +1.0VA_PCH to +1.05VA_PCH
Modify +1.05VS_CPU to +1.05VS_CPU
Modify +1.00V_CPU to +1.05V_CPU
Correct VCCIO enable

20171027
Modify LAN from PCIE PORT5 TO PCIE PORT14
Modify WIFI from PCIE PORT6 TO PCIE PORT15

20171028
Correct Q123 enable to NVDDS_PEX_VDD_EN
P31 ADD FAN_BOOST# CN pull up,reserve QKEY1_CN#,QKEY2_CN# pull up
P65 remove VIN1N,VIN2N,VIN3N 665K resistor
P67 reserve NVDD remote sense pull low pull high close to controller

20171030
P30 modify GPE1 to board id 2 for ID1&ID2
P43 modify C193 to 10 uf
P30,35 Modify FAN to 4PIN,modify FAN_PWM_CTRL
P69 reserve R988&C549&R993 for NV check
P57 GPIO9 PULL UP FOR NV CHECK

20171031
P72 correct EDP VIN ON OFF

20171102
P30 ADD ECSCI# pull low resistor
P33 reserve L42 for 8111GS,ADD 4.7u CAP

20171106
swap FBC_D63&FBC_D61
P28 HDMI ADD B3.B4,B5,B6,B8,B11,B17 FOR NV REQUEST
remove 1.2VS_DDR_PG
ADD PE_VCORE_FW
P46 change VCCSA From MP86901-BGLT to MP86901-AGQT
P17 Modify thermtrip
ADD US/UK KB solution

20171108
ADD C3628,C3631,C3634 for 1.05VA
Modify CPUCORE IMON,GTCORE IMON

20171109
P39 DCIN Modify bead to fuse
DEL saftty protect 3*3 MOS
P70,58 ADD MICRON 8Gb 1.35/1.50V power information
P57 PEX_RST_HOLD#_GC6 Can be NC(unstuff 10K now)
P57 Routing out GPIO16 pull up to 1V8_AON
P66 ADD NVVDD/NVVDDS PGOOD loopback circuit

20171110
P39 remove H1
P34 modify speaker output EMI CAP location
P18 ADD SUB battery connector for ID1,ID2
P39 modify H2,H10,H13,H15,H16 footprint
P30 ADD EDS solution for KB to EC

20171113
P68 ADD 330uf for NVVDD

20171126
P27 modify EDP connector PIN19 to 3.3V power
P42 ADD SUS_ON_S4# pull low 100Kohm
P28 change R430/Q54 for HDMI signal
P40 change 5VA input CAP 10+10+1+1
P68 remove NVVDD snubber P67 R239 to 4.7ohm

20171128
P66/42 modify APL3523QBI-TRG to APE8910_GN3B

20171129
P44 remove PE_VCORE_FW pull high

20171130
P52 ADD 2pcs 10nf CAP for simulation solution
P34 modify SPK define

20171201
P32/16 change SSD PCIE form port17,18,19,20 to port 21,22,23,24 for suppot NVME
P42 Reserve 0ohm for PM_SLP_S4#
P9 R249 ON
P44 modify reserve PE_VCORE_FW pull high to +3.3VA,modify R514 to 10K-04

20171202
P30 ADD R150,R153,R159 1K-04
P18 clear cmos solution modify to 5VA_PG from 1.05V_PG,@R931
P44 R558,R559 modify value
P30 R155 10K-04->10K-1-04,ADD C293 Seperate KB power for ME KB power saving
P21 C281,C280 to 16pf
P27 RESERVE C305 4.7uf for +5V_3.3V_LCD
P40 ADD 5VA VIN 1UF
P32 modify CNHDD1 S2 to +5V_HDD
P38 R194 to 196K-1-04/R187 to 28K-1-04

20171204
P17 H_THERMTRIP_N modify
P40 AUX_OFF modify
ADD FBVDDQ 22*12 pcs for Memory margin issue
ADD 50mohm-1w-1206 *3 for DGPU performance issue

20171205
RESERVE 5VA FB 0.1UF CAP
modify H14 footprint
DEL R1085,R1093

20171206
modify EC ROM to GD25Q20CTIGR

20180114
P28 Modify HDMI detect
P20 Modify USB3 port5
P29 Modify MINI DP EDID BUS,detect
P66 Reserve for DGPU power off sequence
P39 Cancel DC-IN fuse
P30 Modify ME KB
P38 Modify PA MOS GATE CAP
P18 Modify PM_RSMRST# pull low 100K on

20180115
P37 +5V TO +5V_TYPEC,+5VS to +5VA
P35 AUDIO +5VS TO +5VA
P36 CNUSB1 +5VS to +5VA ADD PIN5 to USB 5V POWER
P40 remove +5VA/+3VA jumper
P41 remove 1.05/VCCIO/1.8V jumper
P22/23 modify CNVI POWER to internal 1.8V
P44 modify 2949A 3.3VA to 3.3V as same as driver power
P45 remove CPUCORE VIN jumper
P46 REMOVE VCCGT/VCCSA VIN jumper
P43 REMOVE 1.2VS VIN JUMPER

20180116
P30 REMOVE ALL ME ESD
P32 REMOVE HDD RESERVE SCH
P46 RESERVE 330U FOR GT

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Title: History

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