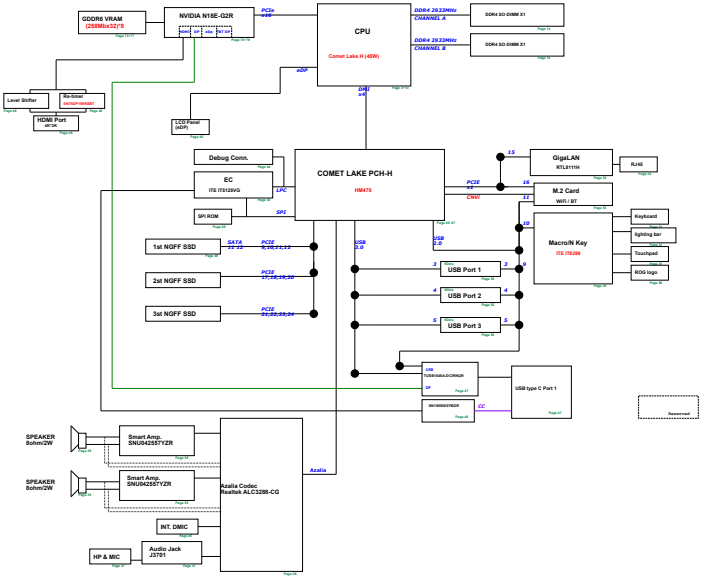
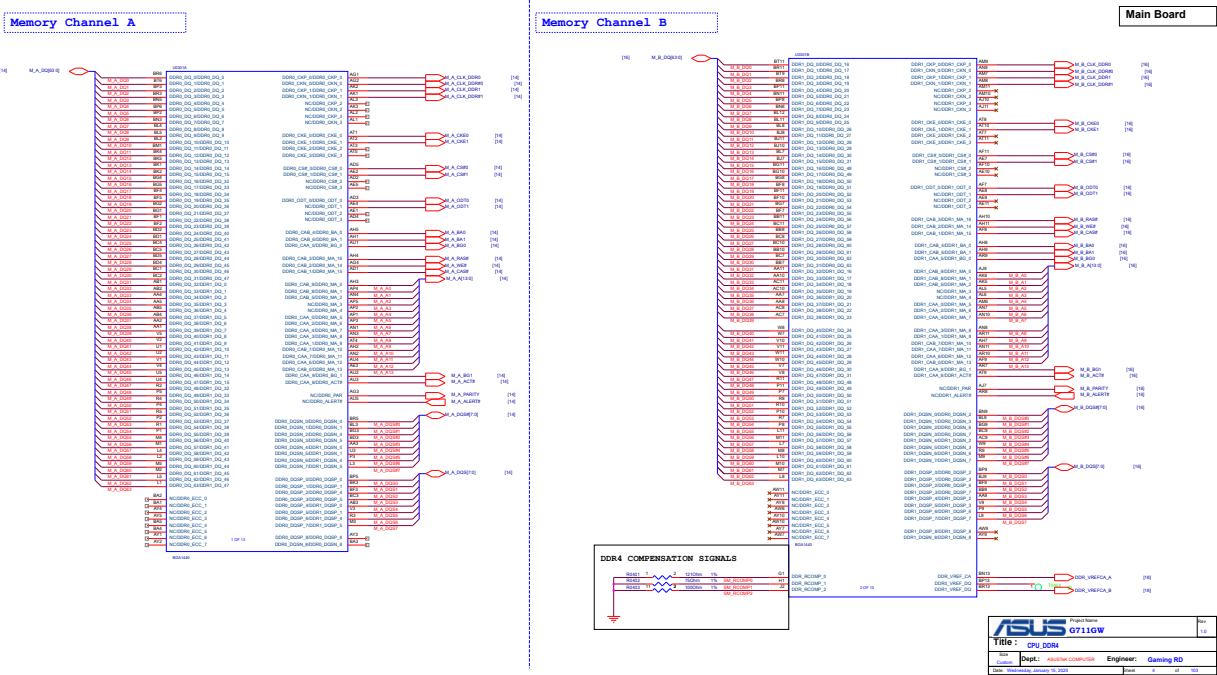
G532/G512/G732/G712 LWS/LW/LV/LU Block Diagram

Comet Lake H Refresh Platform



ASUS	Compal Electronics, Inc.		
Title:	Block Diagram	Size:	Document Number: G532LW/B
Date:	Sheet of	Rev:	


Memory Channel A
Memory Channel B
Main Board
DDR4 COMPENSATION SIGNALS
ASUS
G711GW
CPU_DDR4
Gaming RD
Wednesday, January 16, 2019

	Project Name G711GW	Rev R1.3

Title : CYPRESS CCG4

Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER	Gaming RD

Date: Wednesday, January 15, 2020	Sheet	12	of	103

<Variant Name>

ASUSTeK COMPUTER	Title : *****	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 19 of 103	

PCIEG

確認是否改為by16

CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8

Display

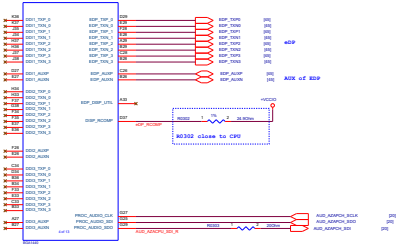


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CFL-H PDG P.363 (Doc:571391)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio Interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQ0#_X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_GLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/NV_GPU_EVENT#		PU 10K(@)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/NV_GC6_FB_EN		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2			
GPP_C3	SML0CLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(@)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 1K	
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT		PU 10K	+VCC3V3_SX
GPP_D1	GPI	GPO	GPIO_3_FORCE_PWR		PD 10K	
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#			
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID			
GPP_D12	GPI	Strap	TOUCH_PANEL_ID			
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(@)	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET2		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)			
GPP_E4	GPI	Native	NGFF0_DEVSLP			
GPP_E5	GPI	Native	(N.C)			
GPP_E6	GPI	Native	NGFF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(@)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1			
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1			
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_USB31#_X1		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 100K	
GPP_I1	GPI	Native	(N.C)		PD 100K	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	Native	(N.C)			
GPP_I4	GPI	Native	GPP_I4		PD 100K	
GPP_I5	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)		PU 2.2K(@)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	NKey_WRST	PD 10k	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4/INTB#	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN#_wCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K(@)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH		
GPG4	GPI		EC_SI/EC_SI_PCH		
GPG5	GPI		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VBUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K(@)	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	KB_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
on board memory CHA		
SO-DIMM B(0)	A4h	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
VGA Thermal Sensor	96h	
CPU Thermal Sensor	90h	
Power Thermal Sensor	7Eh	

Device Identification

CPU Thermal Sensor		
1st	06G023123010	NCT7717U
2nd		

GX501VIPCIE & USB Function define

Kabylake HM175

HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 MB Port1(Charger)	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02	USB3.0 Port3	
04	USB3#04	USB3.0 Port4	
05	USB3#05		
06	USB3#06		
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE		
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA*1 SSD port0	
16	PCIE#10 / SATA#1	PCIE*4 SSD	SRC6
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4
USB2_06	
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

#	Lane	Alt 1	Alt 2	Width	Width	Use
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1		x 2	x 4	NA
8	USB3 #8	PCIE #2				
9	USB3 #9	PCIE #3		x 2		
10	USB3 #10	PCIE #4	GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0"	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1"				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	PCIE #17	SATA #4		x 2	x 4	Intel IRST PCIE Storage Device #3
24	PCIE #18	SATA #5				
25	PCIE #19	SATA #6		x 2		
26	PCIE #20	SATA #7				

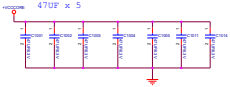
SKL PCH-H H170 HSIO

#	Lane	Alt 1	Alt 2	Width	Width	Use
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7					
8	USB3 #8					
9	PCIE #3			x 2	NA	NA
10	PCIE #4		GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0"	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1"				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			NA	NA	NA
24	SATA #5					
25	PCIE #19			x 2		
26	PCIE #20					

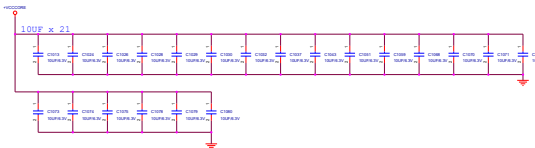
SKL PCH-H HM170 HSIO

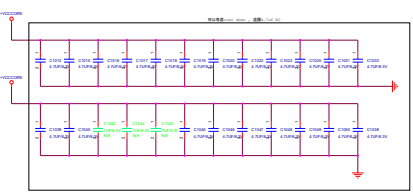
#	Lane	Alt 1	Alt 2	Width	Width	Use
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1		x 2	x 4	NA
8	USB3 #8	PCIE #2				
9	PCIE #3			x 2		
10	PCIE #4		GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0"	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1"				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23				NA	NA	NA
24						
25				NA		
26						

+VCCORE near CPU



+VCCORE DECAPS Place Back Side (TOP)

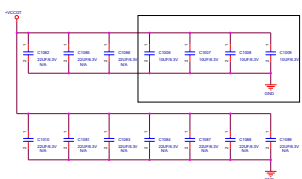




Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

+VCCGT cap near CPU

22uF x14



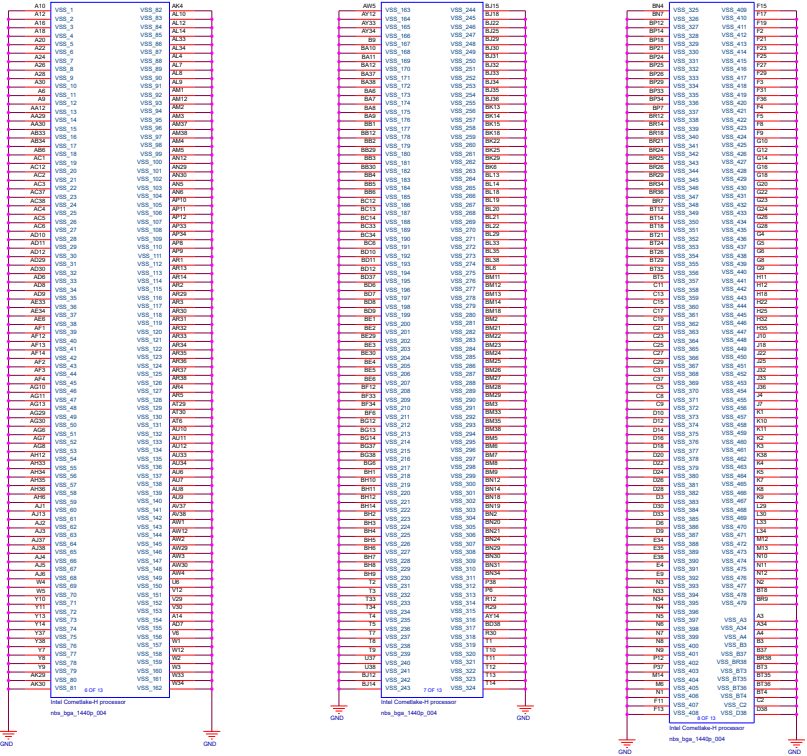
ASUS	Project Name: G711GW		Rev: 1.0
Title :	010_CPU_POWER_CAP		
Size:	Document Number:		
Date: Wednesday, January 15, 2020	Sheet 16 of 109	Engineer:	Gaming RD

	Project Name G711GW	Rev R1.0

Title : TBT_Alpine-Ridge

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER	Gaming RD

Date: Wednesday, January 15, 2020	Sheet	11	of 103



ASUS	Project Name: G711GW		Rev: 1.0
Title :	CPU_CFG,RSVD,GND		
Size: B	Dept.: ASUSTeK.COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 15, 2020	Sheet 5 of 103		

<Variant Name>

ASUSTeK COMPUTER	Title : DDR4_TERMINATION	
	Engineer: Gaming RD	
Size: Custom	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 13 of 103	

CFG

Boundary Scan

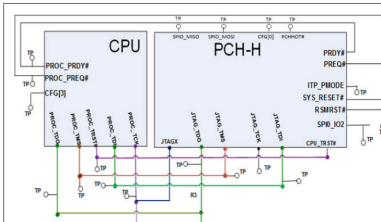
Next close to CPU

Plase close to CPU

Put CPU states check

Close to CPU

Figure 421. Connector Less Routing Topology



– Stubs on JTAG nets should not more than 200ps
– R1, R2, R3 should be placed to within 200ps of CPU PROC_TCK pin. PCH JTAG_TDO, CPU PROC_PREQ# respectively
– Note that it is not need to include the pull up (R3) for CPU PROC_PREQ# if the Trace length between CPU PROC_PREQ# and PCH PREQ# can be kept to within 200ps (approx 1100mil or 28mm)

– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPI0_IO2 VCCIOBB_AB (PCH V1.0 A), GND pins (2)
– TP should be placed to within 250ps of the respetive pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
– TP = Test Point Pad (size - 18 mil min. 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

CFG Straps for Processor
6065/99-cml-eds-vol1-rev0p9 page116

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane
Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes
Reserved Configuration Lane

CFG[4] : eDP Enable
- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation
- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : (Reserved)
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes
Reserved Configuration Lanes

CFG Straps

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

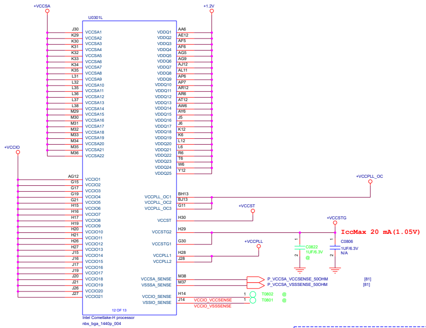
VTT Enable

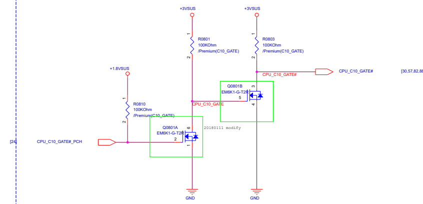
06004-00020000

2nd source: 06004-00051800

CPU SIDEBAND SIGNALS

ASUS	Project Name: G711GW		Rev: 1.0
Title : CPU XDP			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 15, 2020	Sheet 7 of 103		





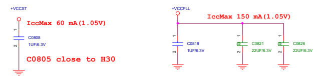
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)



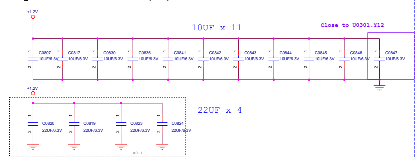
CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines

Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H IBP#571391 and CFL-U IBP#571021 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.

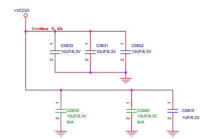
An additional capacitor 0805 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.

This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

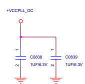
+VDDQ DECAPS Place Back Side (TOP)



+VCCIO DECAPS Place Back Side (TOP)

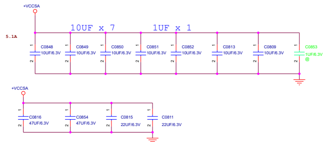


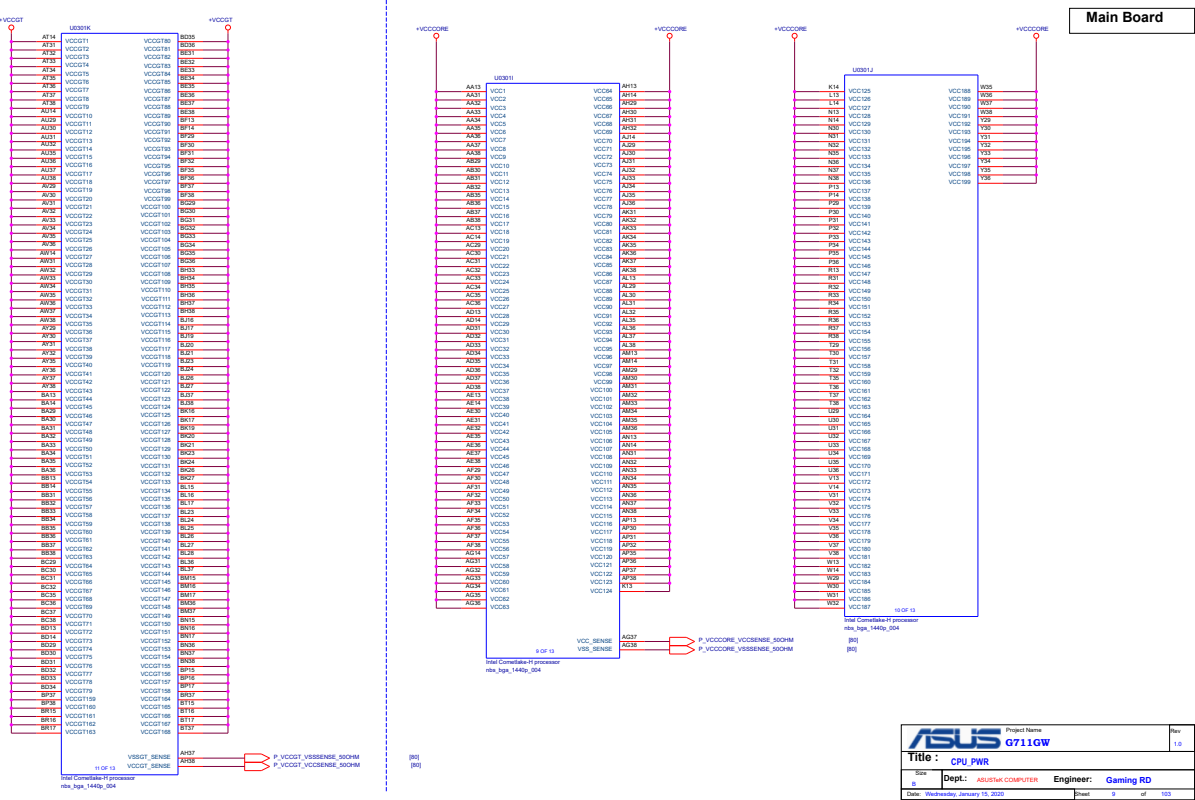
+VCCPLL_OC DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)

+VCCSA near CPU





Project Name	G711GW		Rev 1.0
Title :	CPU_PWR		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer:	Gaming RD
Date: Wednesday, January 15, 2020	Sheet 9	of 103	

<Variant Name>

ASUSTeK COMPUTER	Title : DDR4_ON-BOARD_A2	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 15 of 103	

<Variant Name>

ASUSTeK COMPUTER	Title : NB_****	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 17 of 103	

HPD0 to DP

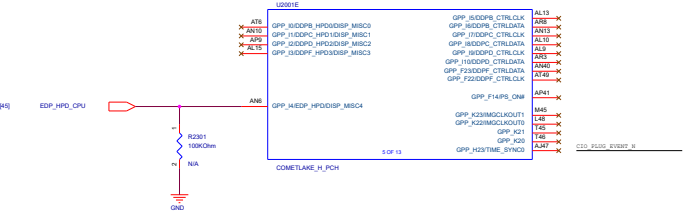
HPD1 to HDMI

HPD2 to TBT

HPD3 to VGA

HPD4 to EDP Panel

DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected



ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 15, 2020	Sheet 23 of 103		

ASUS	Project Name: G711GW	Rev: 1.0
Title : PCH-XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, January 15, 2020	Sheet 29 of 103	

The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

Main Board

U3301A

CLKREQ0#_GLAN#
CLK_PCIE_GLAN
CLK_PCIE_GLAN#

C3301 0.1UF/25V
C3302 0.1UF/25V
PCIE1S_TXP_GLAN_X1
PCIE1S_TXN_GLAN_X1

C3303 0.1UF/25V
C3304 0.1UF/25V
PCIE1S_RXP_GLAN_X1
PCIE1S_RXN_GLAN_X1

PCIE_WAKE#

SLI3302
LAN_RST#

LANWAKE#
PERST#

SMDIN3 SMDIP3 SMDIN2 SMDIP2 SMDIN1 SMDIP1 SMDIN0 SMDIP0

L_TRDIN3 [34]
L_TRDIP3 [34]
L_TRDIN2 [34]
L_TRDIP2 [34]
L_TRDIN1 [34]
L_TRDIP1 [34]
L_TRDIN0 [34]
L_TRDIP0 [34]

CKXTAL1 CKXTAL2

XO_LAN
XI_LAN

LED0
LED1/SPD
LED2

T3301
DRC2u7

ISOLATE#

RSET

REGOUT

60 mil
C3304 1UF/25V

VDDREG
AVDD33_1
AVDD33_2

SLI3303 SI2302
+3VSUS_LAN

AVDD10_1 AVDD10_2 AVDD10_3 DVDD10

+TV_LAN

GND21

RTL8111H-CGT

U3301B
34 GND2
35 GND3
36 GND4
37 GND5

GND

EMI Reserve
LAN_RST#
C3301 1000PF/16V

CLKREQ_GLAN#, PCIE_WAKE# should be PU on the host side

07G010272501
X3301
25.000MHZ
C3306 10PF/50V
+/-30ppm/10PF
C3307 10PF/50V
XI_LAN
XO_LAN
X3301: 25MHZ +/-30ppm/10pF (3225)
1st: P/N:07G010272501 TXC/7V25000011
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms

+3VSUS
+3VSUS_LAN
R3302 0Ohm N/A
Q3301 FDC6506
WLAN_LAN_PWR_gate [32]
C3302 0.1UF/25V

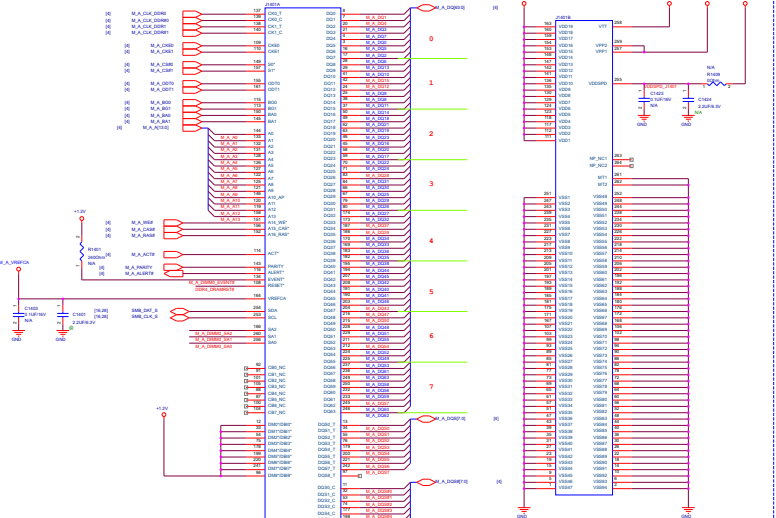
+3VSUS_LAN
C3322 10UF/6.3V
C3342 0.1UF/25V
C3361 0.1UF/25V
+TV_LAN
C3336 0.1UF/25V
C3337 0.1UF/25V
C3338 0.1UF/25V
C3339 0.1UF/25V
C3344 10UF/6.3V

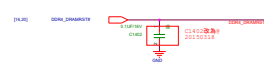
ASUS	Project Name: GX5/GX2/GX		Rev: 1.0
Title : LAN RTL8111GUX-CG			
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Wednesday, January 19, 2011		Sheet 33 of 70.0	

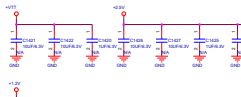
Chris

Main Board

SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

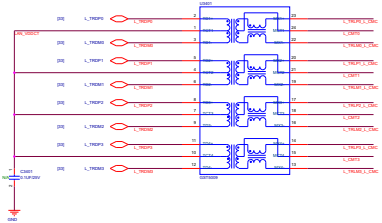


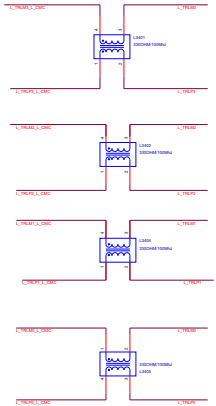




Project Name	G711GW	Rev	R0.0
Title :	DIM_DDR4 SO-DIMM A1		
Custom	Dept.: ASUSTeK COMPUTER	Engineer:	Gaming RD
Date: Wednesday, January 15, 2020	Sheet 19 of 100		

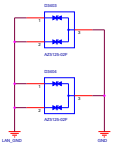
Main Board

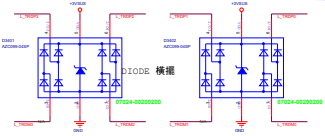




LAN Connector

Place near chassis GND





DIODE 橫握

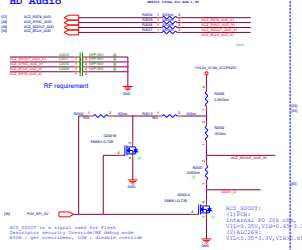
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP,R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

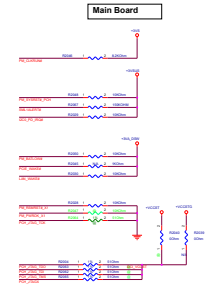
ASUS	Project Name: GX502GX			Rev: 1.0
Title : LAN_RJ45_CON				
Size: C	Dept.: ASUSTeK COMPUTER	Engineer:	NB1 RD2 EE1	
Date: Wednesday, January 08, 2020	Sheet: 58 of 103			

HD Audio



EMI

Main Board

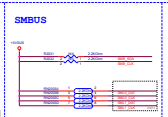


Power failure solution (S0-->G3,S5-->G3):

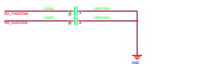
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VALO	+3VA	+3VA_EC	
	+3VSUS	+3VSUS_PCH	+V3.3A_VS, +V3.3A_VSUSG	
	+3VA_SUM			
	+3VB			

eSPI or LPC

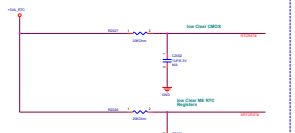
SMBUS



EMI-GX501GI



RTC battery

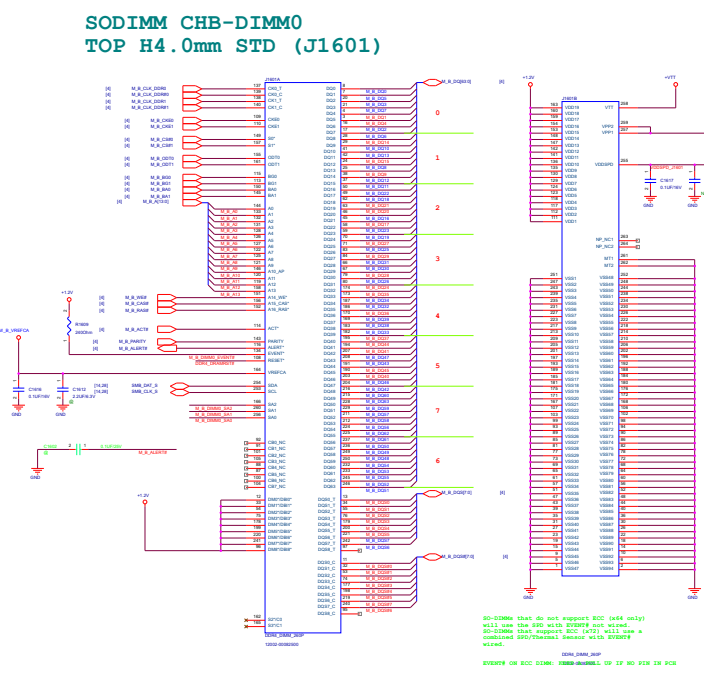


Power failure solution (S0-->G3,S5-->G3):

Deep SX discharge (S0-->DSX,S5-->DSX)

Title :	PCH-OPT1/SATA,SIGA,RTC,JTAG		
Size:	Project:	Wistron ComalCRB	Engineer: Gaming RD
Date:	Wednesday, January 16, 2019	Sheet 15 of 103	

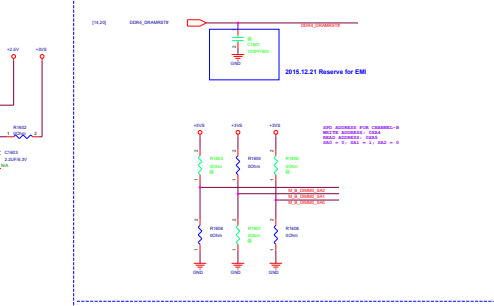
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

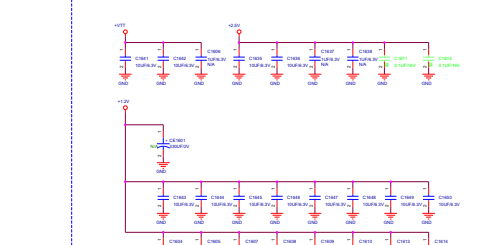


SO-DIMMs that do not support ECC (x4 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: TIED directly UP IF NO PIN IN PCH

Main Board





Project Name	G711GW
Title :	DIM_DDR4 SO-DIMM B1
Size: Custom	
Dept.:	ASUSTeK COMPUTER
Engineer:	Gaming RD
Date:	Wednesday, January 18, 2023
Sheet	19 of 100
Rev	1.0

Main Board

PCIe Setting

GX501GI PCIE/SATA Function define

CNL HM370

HSIO Capabilities	Function
PCIE0 (From CPU)	
PCIEX1 - USB1 1#07	
PCIEX2 - USB1 1#08	
PCIEX3 - USB1 1#09	
PCIEX4 - USB1 1#10	
PCIEX5	
PCIEX6	
PCIEX7	
PCIEX8	
PCIEX9	PCIE*4 SSD
PCIEX10 - SATA-0/x	
PCIEX11 - SATA-1x	
PCIEX12 - SATA-1x	
PCIEX13 - SATA-0/x	
PCIEX14 - SATA-1/x	
PCIEX15 / SATA#2	
PCIEX16 / SATA#3	WLAN
PCIEX17 / SATA#4	
PCIEX18 / SATA#5	
PCIEX19 / SATA#6	
PCIEX20 / SATA#6	
PCIEX21	TBT (x4)
PCIEX22	
PCIEX23	
PCIEX24	

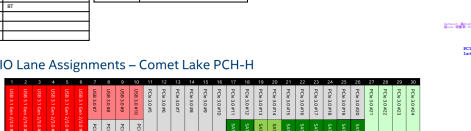
	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	CR
CLKREQ-3	WLAN
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

USB Setting GX501GI USB Function define CNL HM370

USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4(Charger)
USB2_06	TBT
USB2_07	
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

USB 3.0	Function
USB3.1#01	USB3.1MB Port1 (Support Gen2)
USB3.1#02	USB3.0 MB Port2 Support Gen2)
USB3.1#03	USB3.0 MB Port3 (Support Gen2)
USB3.1#04	USB3.0 MB Port4 (Support Gen2)
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

HSIO Lane Assignments – Comet Lake PCH-H



SKU

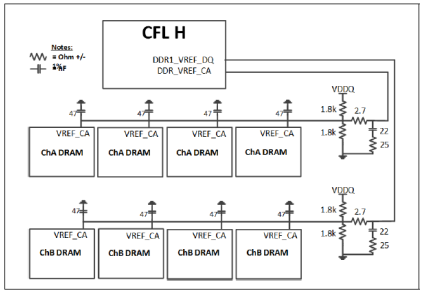
H81x270	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
Q370/Q470	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
W480/E	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	USB3.1	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe

Intel® RST for PCIe Storage part configurable at M.2 x1/x4

High => SATA I/F
Low => PCIE I/F

Project Name	G713GW
Title :	PCH-CFIO1 PCIE,CLK,USB
Size :	Document Number :
Date :	Wednesday, January 15, 2020
Sheet :	21 of 101
Engineer :	Gaming BD
Rev :	2

Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview



Vref for CHA_DIMM0

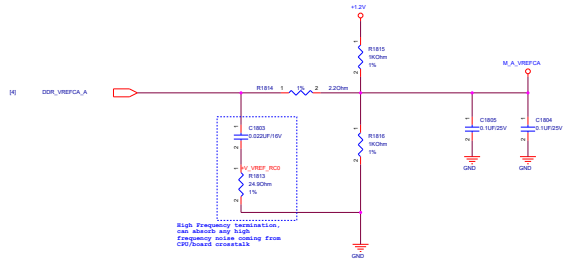
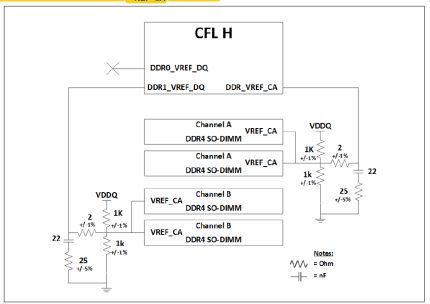
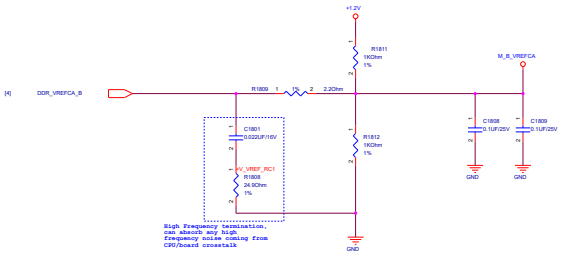


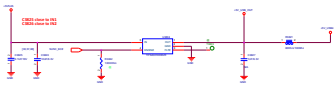
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

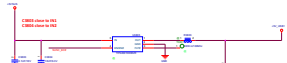


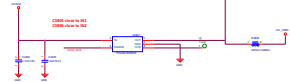
Vref for CHB_DIMM0



ASUS	Project Name: G711GW		Rev: 1.0
Title : DIM_CA/DQ Voltage			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 15, 2020	Sheet 16 of 103		







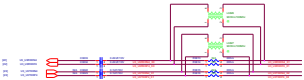
USB3.0_PORT4 (Support USB Charge Circuit)

J3009 USB3.0 Connector
1st Source: P/N:C201L00D1E00 FOXCONN/USB3.0 T/H/ 90D/AMD T/H
2nd Source: P/N:12410-00006400 SINOSTRON/C2B6400 2.54/180°

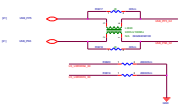
USB3.0 Pin define	
1-	VBUS-
2-	D--
3-	D+-
4-	GND-
5-	RX--
6-	RX+-
7-	GND-
8-	TX--
9-	TX+-

USB Charge Circuit (For PORT 4)

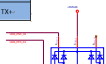
USB3.0_PORT4



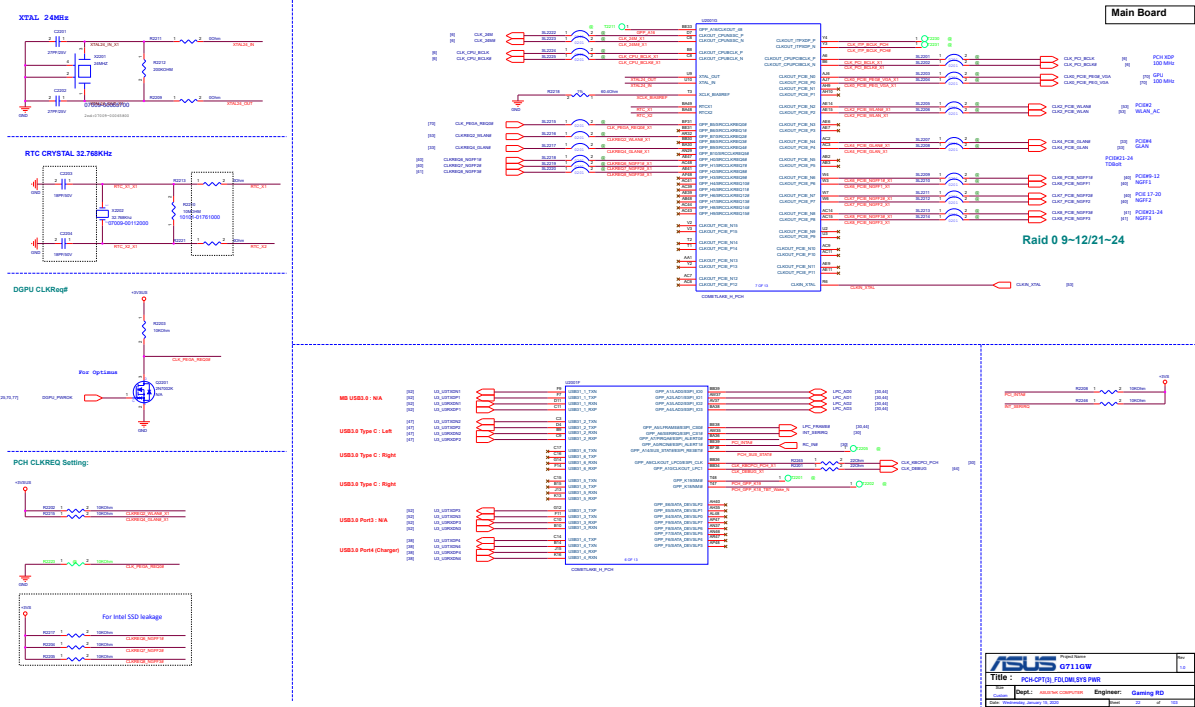
USB3.0 ESD-Protection



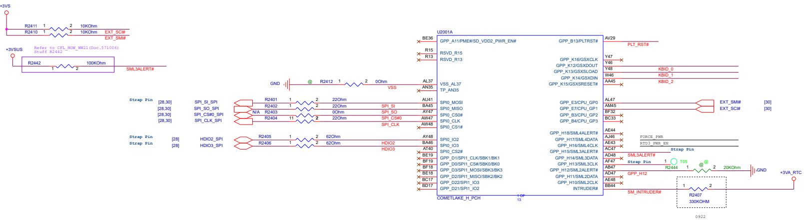
1st : 0TG0280TR020
ESD PROTECTION AZ1045-04F
2nd : 0TG0281S0018
ESD PROTECTION PI4IOE4C210-TB



D3002 ESD Diode
1st Source: P/N:ST0214-00D00200 AMAZING/CAZC048-04UP/TG
2nd Source: P/N:ST024-00T10000 ASP/PJ0B2302

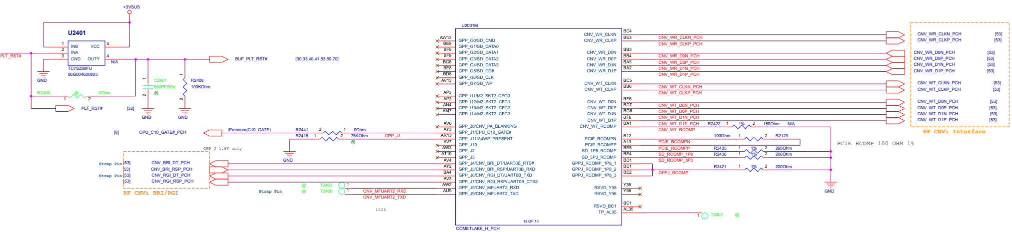

Main Board
XTAL 24MHz
RTC CRYSTAL 32.768KHz
DGPU CLKReq#
For Optimus
PCH CLKREQ Setting:
For Intel SSD leakage
MB USB3.0 : N/A
USB3.0 Type C : Left
USB3.0 Type C : Right
USB3.0 Type C : Right
USB3.0 Port3 : N/A
USB3.0 Port4 (Charger)
Raid 0 9~12/21~24
PCH XDP 100 MHz
GPU 100 MHz
PCIE#2 WLAN_AC
PCIE#4 GLAN
PCIE#21-24 TDBolt
PCIE#9-12 NGFF1
PCIE 17-20 NGFF2
PCIE#21-24 NGFF3
Title : PCH-CPT(3)_FDLDMLSYS PWR
Project Name : G711GW
Rev : 1.0
Dept.: ASUSTeK COMPUTER
Engineer: Gaming RD
Date: Wednesday, January 15, 2020
Sheet 22 of 103

Main Board



Strap => Mount R2443

This strap should sample high,
if sample low will cause boot up fail.



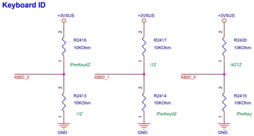
GPP_J6:
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.

[CNV Mode Select] CNV_RGI_DT_PCH
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
[Intel FAE]
RGI_DT has an automatic detect CNVi mechanisim,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU

GPP_J9:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

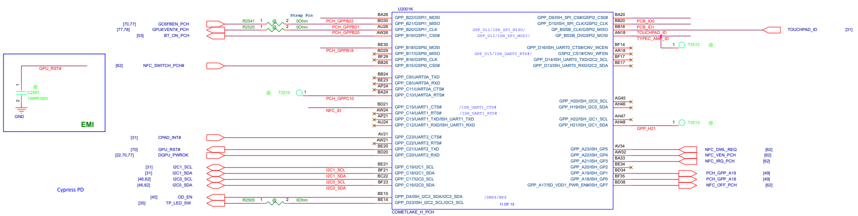
Keyboard ID

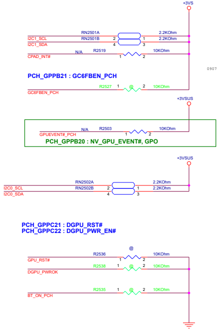


KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

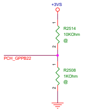
ASUS	Project Name: G711GW	Rev 1.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, January 15, 2020	Sheet 24	of 103

Main Board



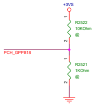


Boot BIOS Strap Bit BBS



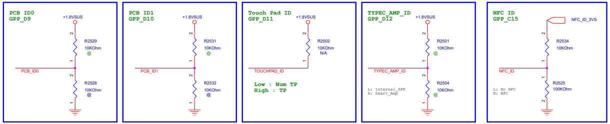
PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

No Reboot



NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)



X-tal Frequency Select

Cannon Lake PCH-LP

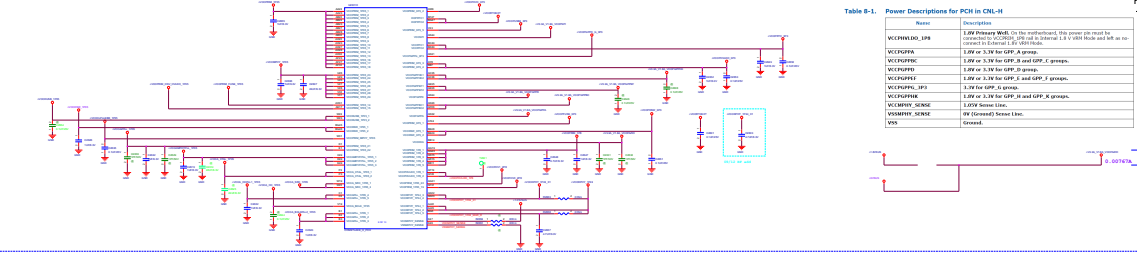
- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

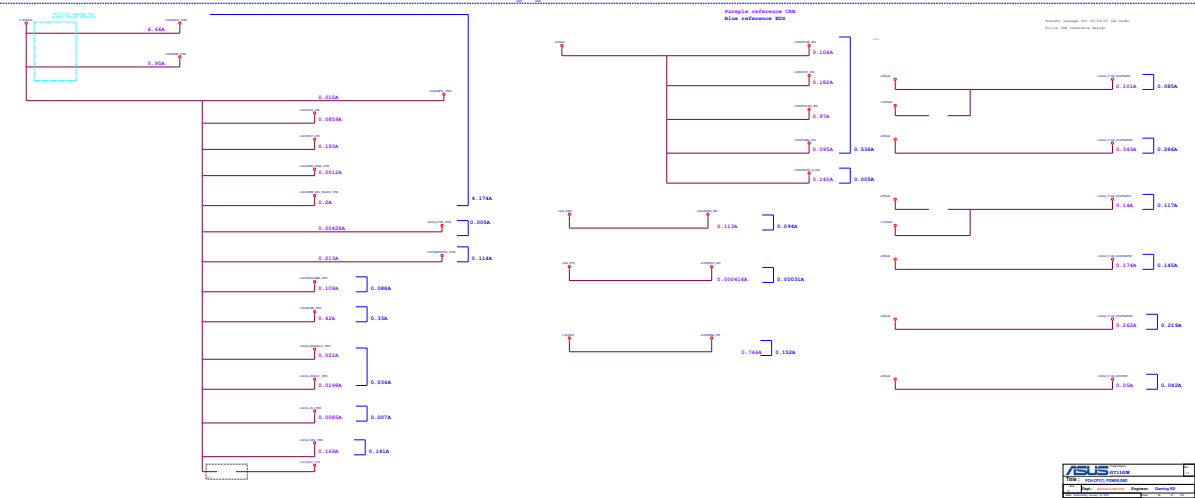
Cannon Lake PCH-H

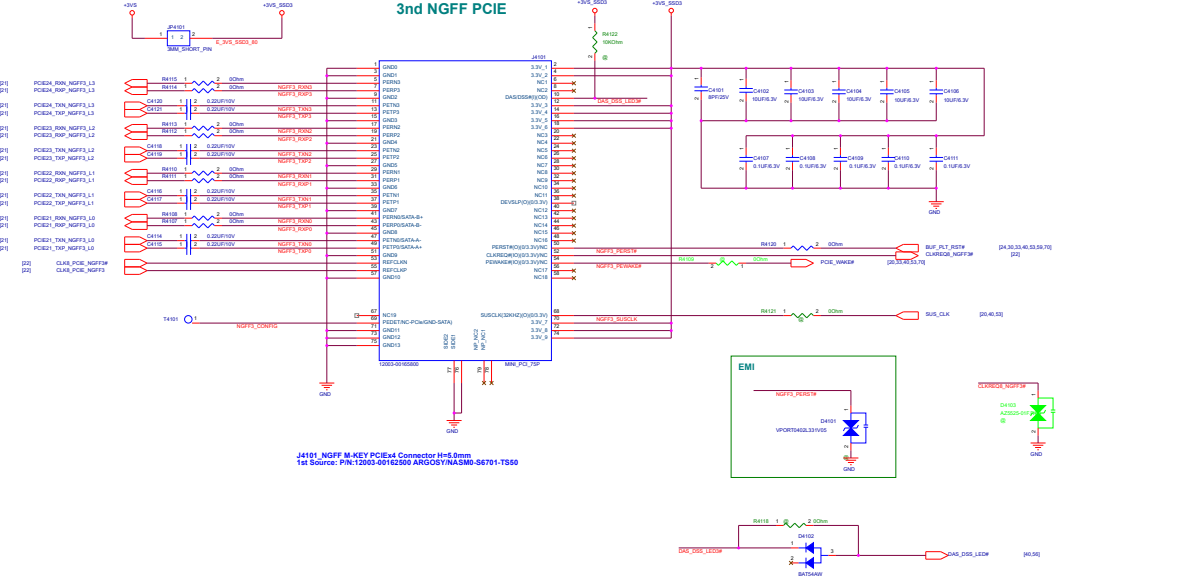
- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPHYLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_1P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.







<Core Design>

ASUS	Project Name: G703GI	Rev: R1.0
Title : NGFF_SSD_SATA_CON		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: NB1 RD2 EE1	
Date: Wednesday, January 15, 2020	Sheet 41 of 103	

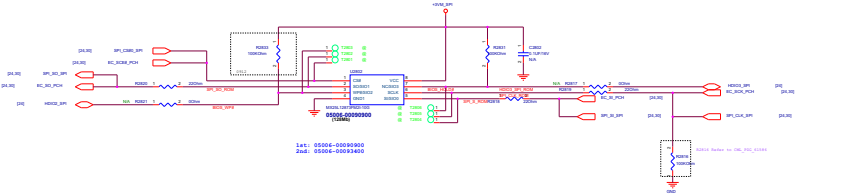
Project Name: G711GW			Rev: 1.0
Title: PCH-CPT(8)_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 15, 2020	Sheet 27 of 103		

SPI Power

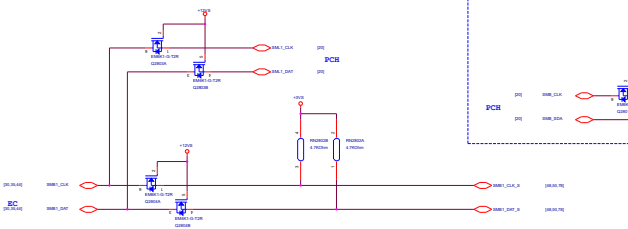
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

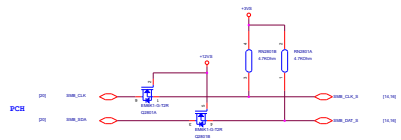
Main Board

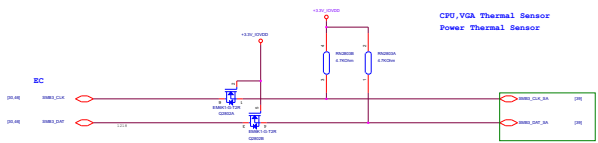


System Management Interface

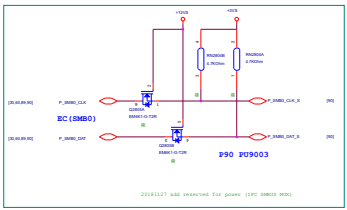


SMBus Interface





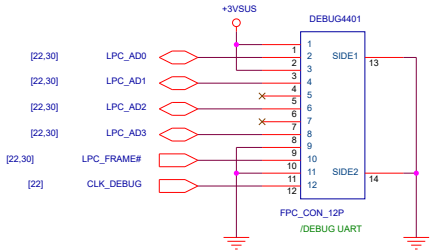
CPU,VGA Thermal Sensor
Power Thermal Sensor



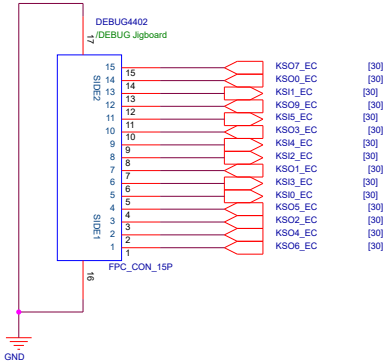
ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size:	Dept.: MB/SYNC/COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 25, 2017		Sheet 35 of 103	

ASUS	Project Name: G711GW	Rev: 1.0
Title : CB IO CON		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, January 15, 2020	Sheet 43 of 103	

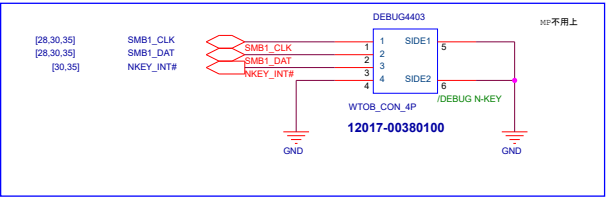
LPC Debug Port



ER2 stuff



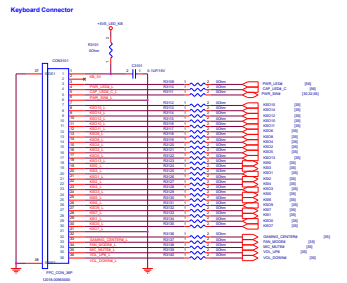
N-KEY Debug Connector



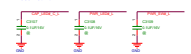
<Variant Name>

ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 44 of 103	

Keyboard Connector

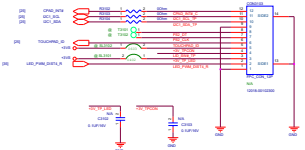


Reserved for EMI

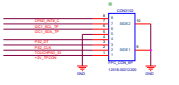


Touch Pad Connector

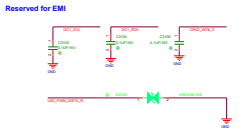
2020 TP nunber light 12PIN



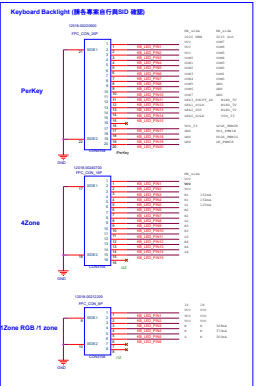
SA555D-2400 8PIN



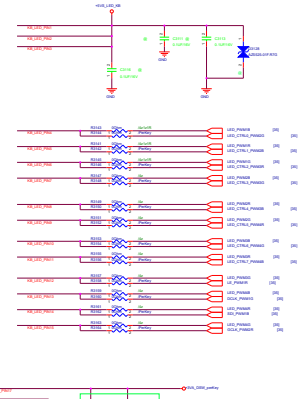
Reserved for EMI



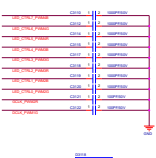
Keyboard Backlight (顯色專業級台灣與SID 建製)

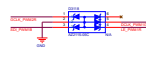


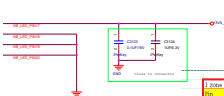
RED, 4zone,1zone, PerKey Co-layout



For EMI







1 zone		1 zone RGB		4 zone RGB		socket	form	to	
Pin	Name	Pin	Name	Pin	Name	NOTE		Pin	Name
1	BLED_5V	1	BLED_5V	1	BLED_5V	VCC		1	BLED_5V
2	BLED_5V	2	BLED_5V	2	BLED_5V	VccB		2	BLED_5V
3	BLED_5V	3	BLED_5V	3	BLED_5V	VccB		3	BLED_5V
4	Cathode LED1	4	Cathode LED1_B	4	Cathode LED1_B			4	COM0
5	Cathode LED1	5	Cathode LED1_R	5	Cathode LED1_R			5	COM1
6	Cathode LED1	6	Cathode LED1_G	6	Cathode LED1_G			6	COM2
7	NC	7	NC	7	Cathode LED2_B			7	COM3
8	NC	8	NC	8	Cathode LED2_R			8	COM4
				9	Cathode LED2_G			9	COM5
				10	Cathode LED3_B			10	COM6
				11	Cathode LED3_R			11	COM7
				12	Cathode LED3_G			12	LB
				13	Cathode LED4_B			13	DCLK
				14	Cathode LED4_R			14	SDI
				15	Cathode LED4_G			15	DCLK
				16	NC			16	NC
								17	VDD_33
								18	GND
								19	GND
								20	GND

1 zone sku follow 1 zone RGB

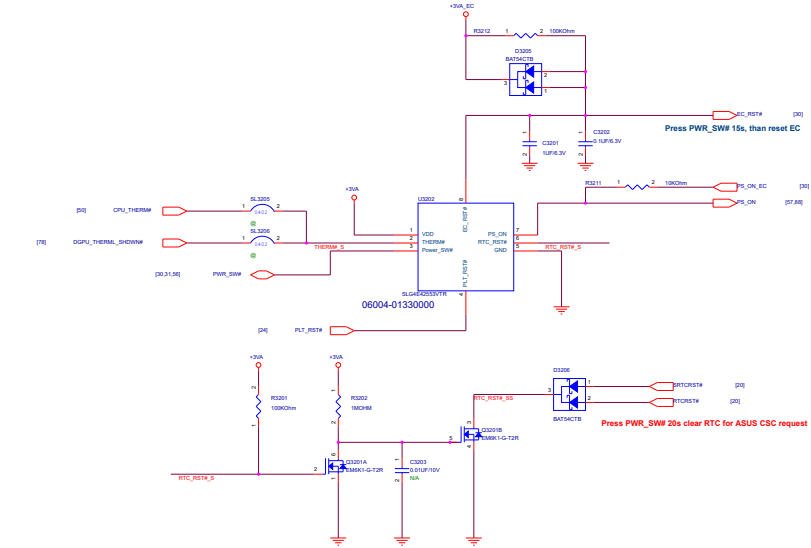
Compal Electronics, Inc.
G711GW
Title : KBC, KB & TP
Size: Document Number: Rev: 0.0.0
Date: Wednesday, January 15, 2020 Sheet of
Engineer: Gaming RD

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

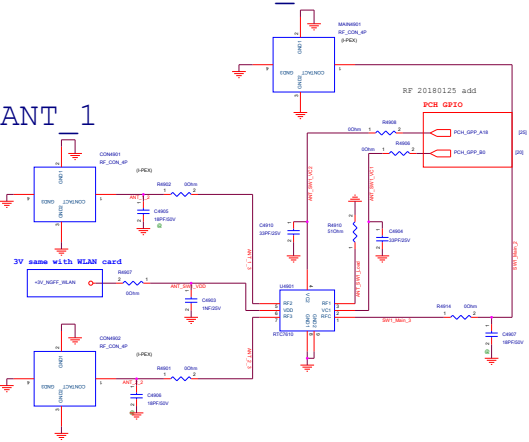
UX362FA R1.3 board will verify this circuit 7/E



<Variant Name>

ASUSTeK COMPUTER	Title :	RST_Reset Circuit
	Engineer:	Gaming RD
Size: B	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 32 of 103	

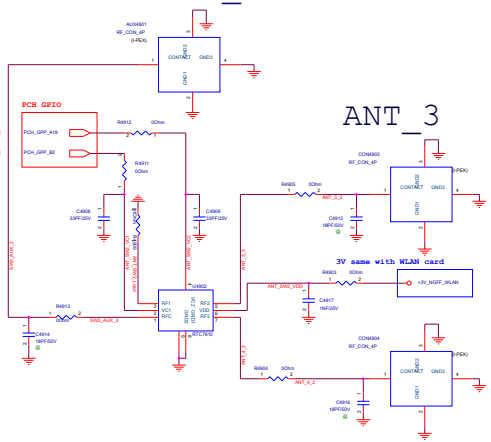
Module_MAIN



U4901 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

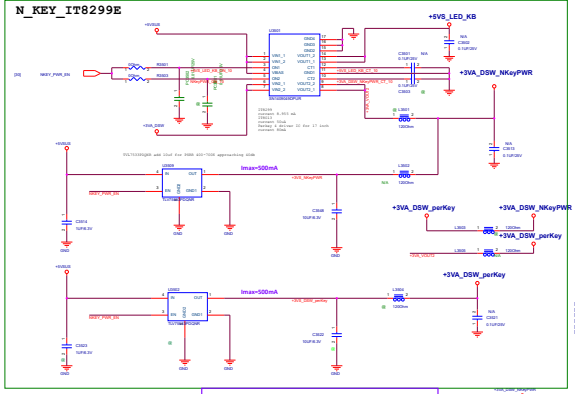
Module_AUX



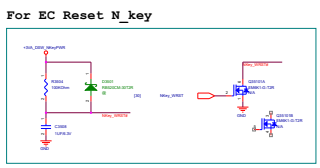
U4902 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

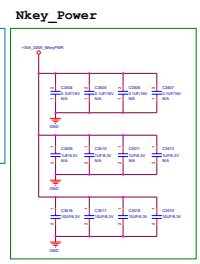
N_KEY_IT8299E

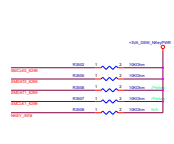


For EC Reset N_key

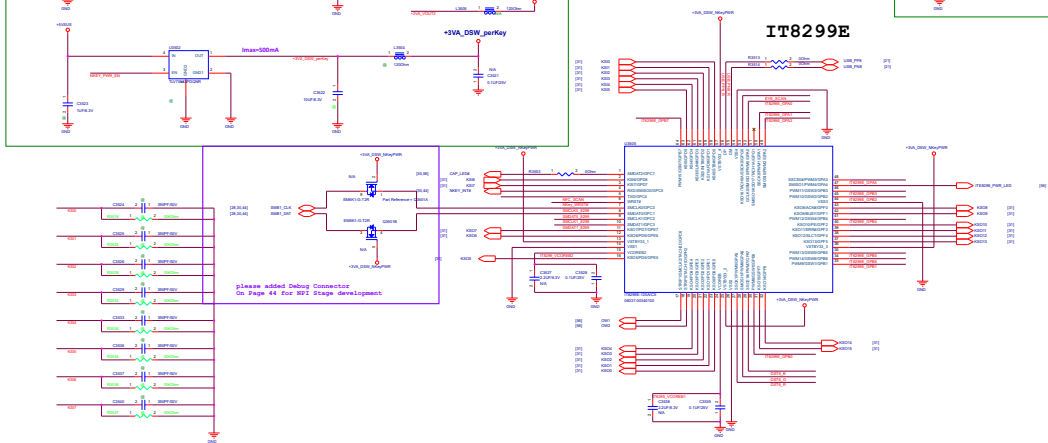


Nkey_Power

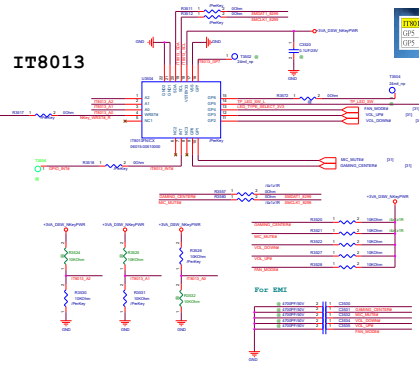




IT8299E

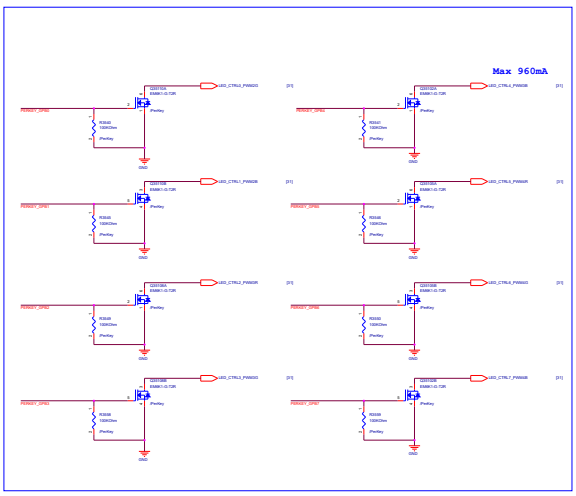


IT8013

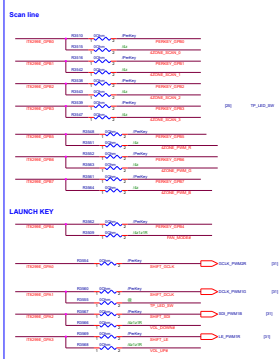


IT8013	LED_TYPE: SELECT_3V1	KB Type
GP5	H	PerKey
GP5	L	4 Zone/1 Zone RGB

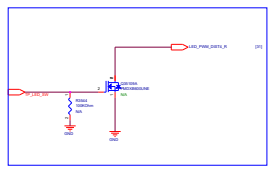
KB RGB Per Key LED



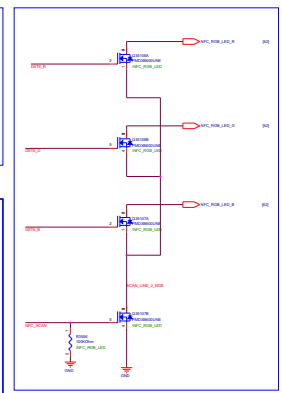
KB RGB co-layout



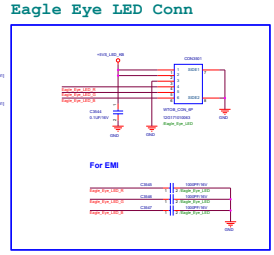
TP LED



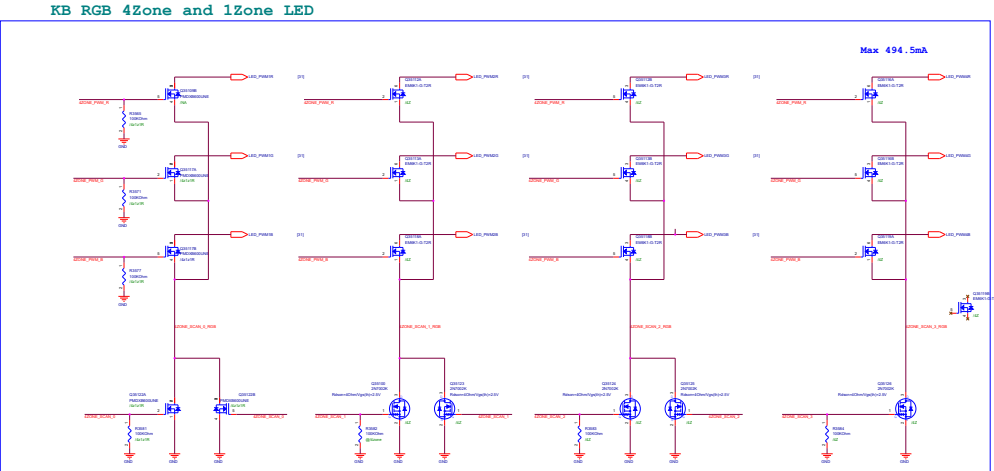
NFC RGB LED



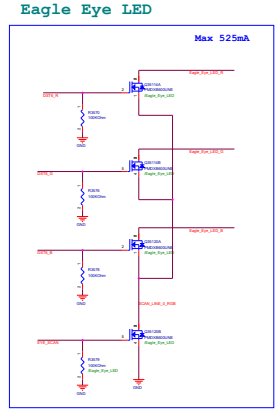
Eagle Eye LED Conn



KB RGB 4Zone and 1Zone LED



Eagle Eye LED



Title :	LAN *****		
Engineer:	Gaming RD		
Size	Project Name	Rev	
Custom	G711GW	1.0	
Date: Wednesday, January 15, 2020	Sheet 53 of 103		

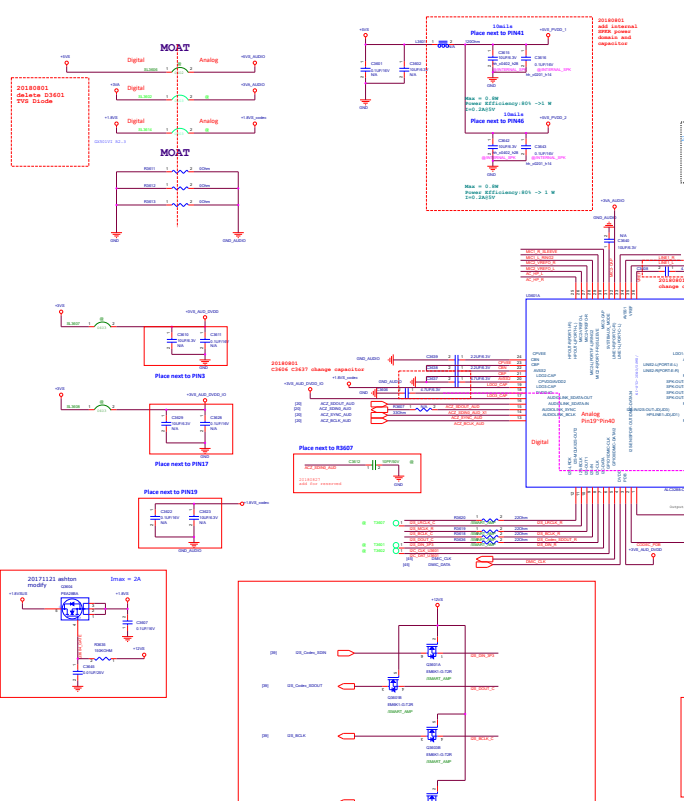


Figure 4. Power sequence

Title :	AUDIO ALC3236-CG/VB2	Project Name	G711GW
Size	Custom	Engineer:	Marshall Li
Date:	Wednesday, January 16, 2019	Sheet	of 100

PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND

<Variant Name>

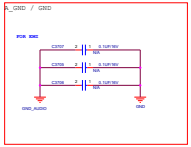
ASUSTeK COMPUTER	Title : XDD_HDD & ODD CON	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: R1.0
Date: Wednesday, January 15, 2020	Sheet 51 of 103	

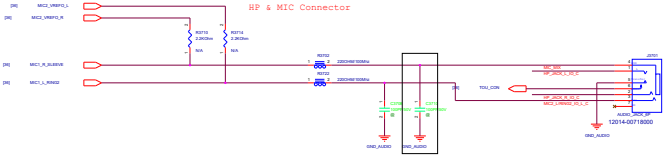
<Variant Name>

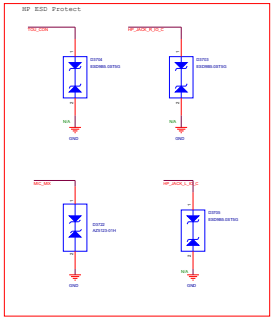
ASUSTeK COMPUTER	Title : IO Con. to MB	
	Engineer: Gaming RD	
Size: Custom	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 55 of 103	

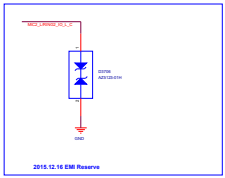
Headphone&MIC

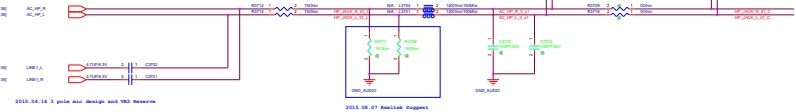
Main Board

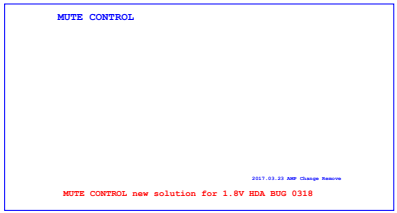


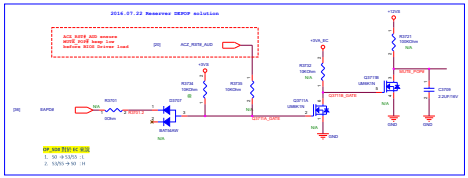




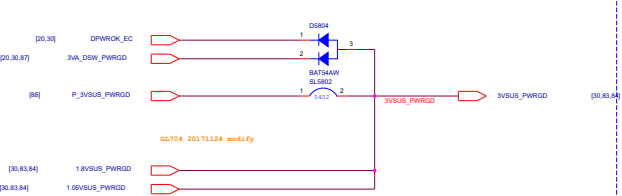


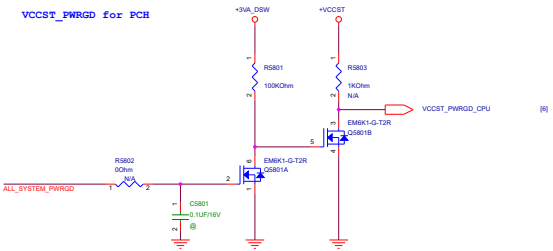


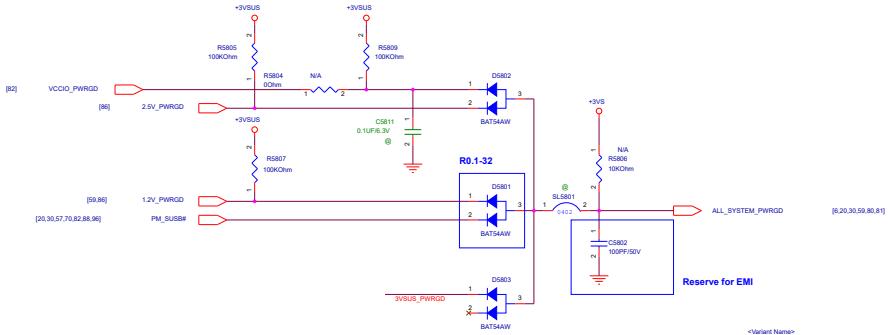




ASUS	Project Name: G711GW		Rev: 3.0
Title :	AUDIO ALC3236-CG/VB2 Jack		
Size: C	Dept.: AXSYM_COMPUTER INC.	Engineer:	Marshall Li
Date: Wednesday, January 15, 2020	Sheet: 37 of 103		

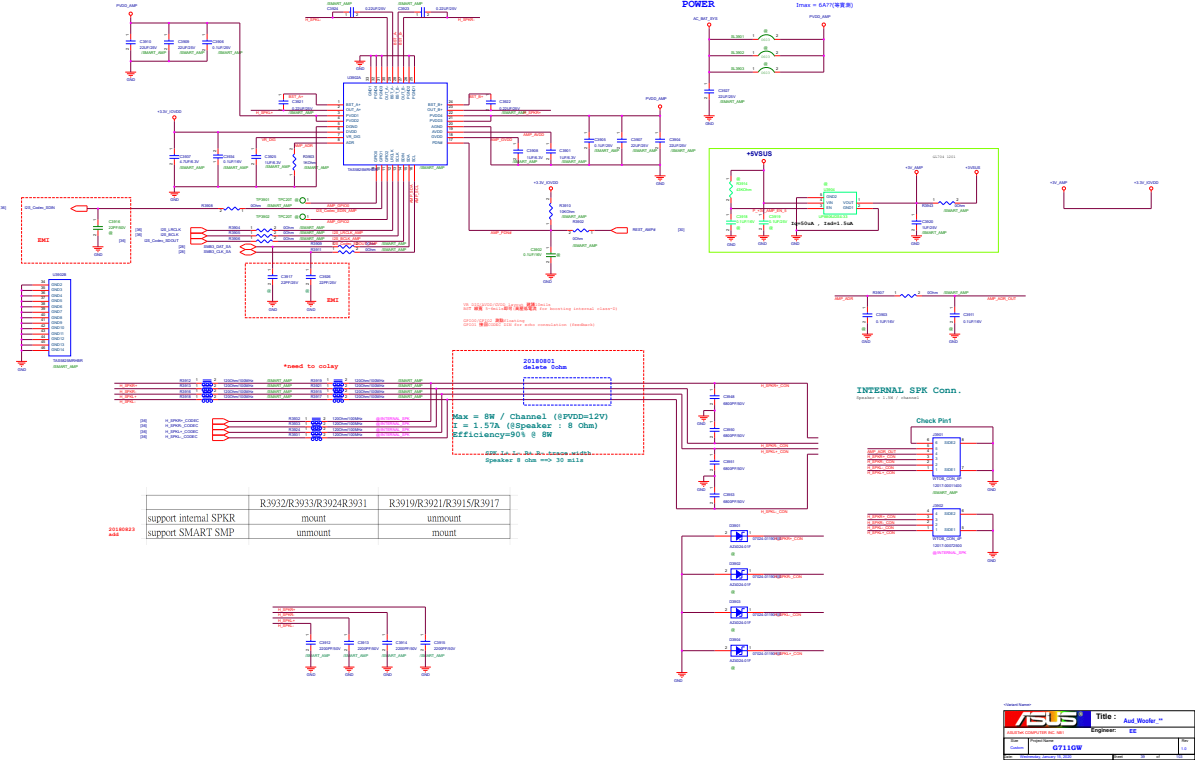






<Variant Name>

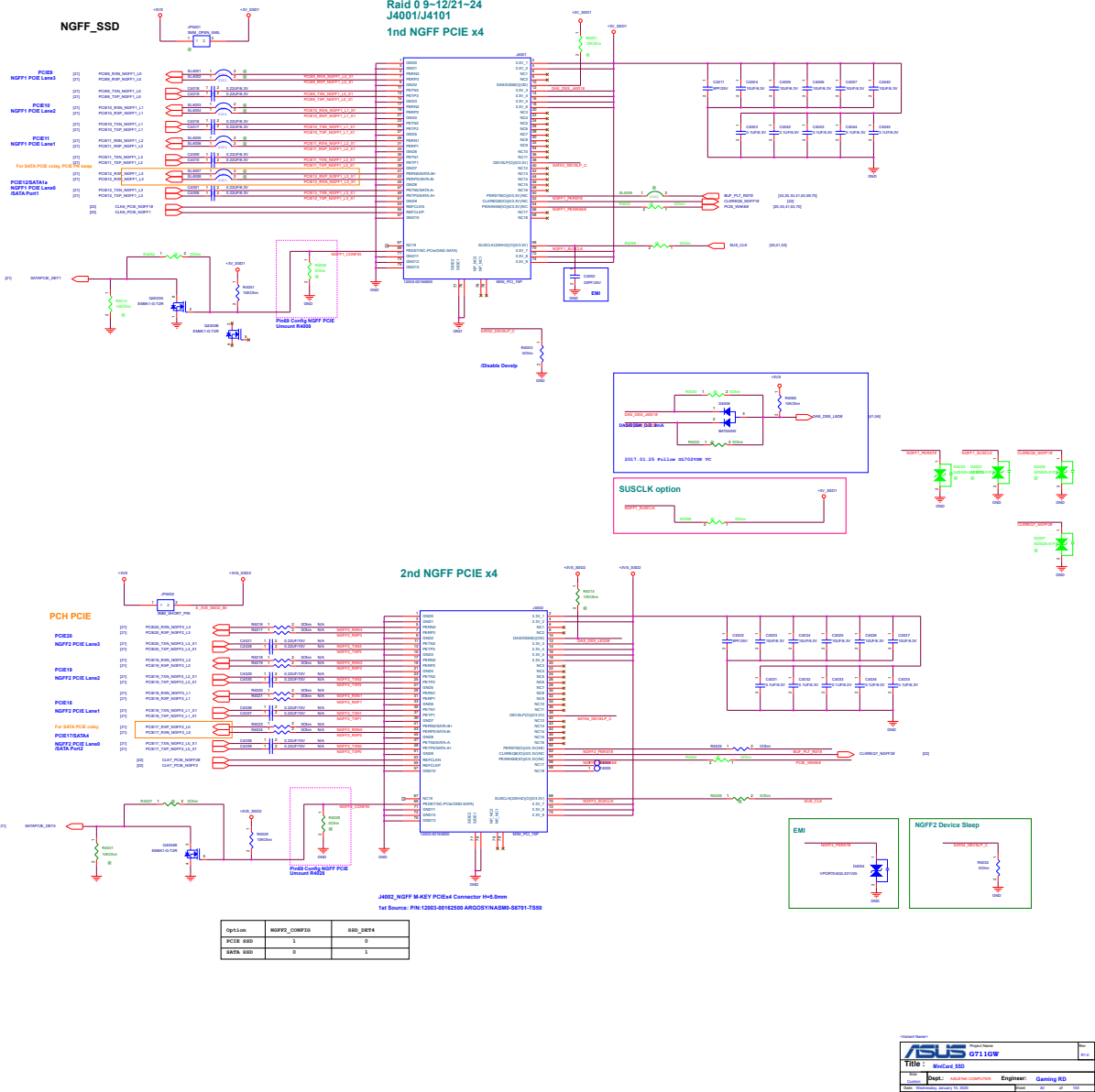
ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: Gaming RD	
Size: Custom	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 58 of 103	



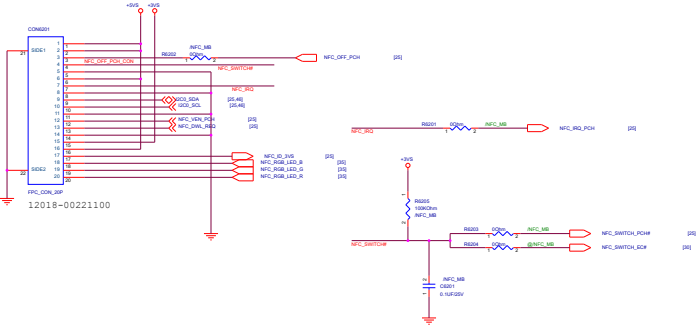
	R3932/R3933/R3924R3931	R3919/R3921/R3915/R3917
support internal SPKR	mount	unmount
support SMART SMP	unmount	mount

20180823
add

Title :	Aud Woofer *#		
ASUSTeK COMPUTER INC. NB1	Engineer:	EE	
Size	Project Name		Rev
Custom	G711GW		1.0
Date: Wednesday, January 15, 2020	Sheet 39 of 103		



Option	NGFF2_CONFIG	SSD_DET4
PCIE SSD	1	0
SATA SSD	0	1


+5VS
+3VS
CON6201
SIDE1
SIDE2
FFC_CON_20P
12018-00221100
NFC_OFF_PCH_CON
R6202
INFC_MB
NFC_OFF_PCH
[25]
NFC_SWITCH#
NFC_IRQ
R6203
R6204
NFC_SWITCH_PCH#
NFC_SWITCH_EC#
[25]
[30]
R6201
NFC_IRQ
NFC_IRQ_PCH
[25]
R6205
100KOhm
C6201
0.1UF/25V

<Variant Name>

ASUSTeK COMPUTER	Title :	
	Engineer: Gaming RD	
Size: D	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 66 of 103	

<Variant Name>

ASUSTeK COMPUTER	Title : I/O board FUNC key	
	Engineer: Gaming RD	
Size: E	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 67 of 103	

<Variant Name>

	Project Name G711GW	Rev R1.0

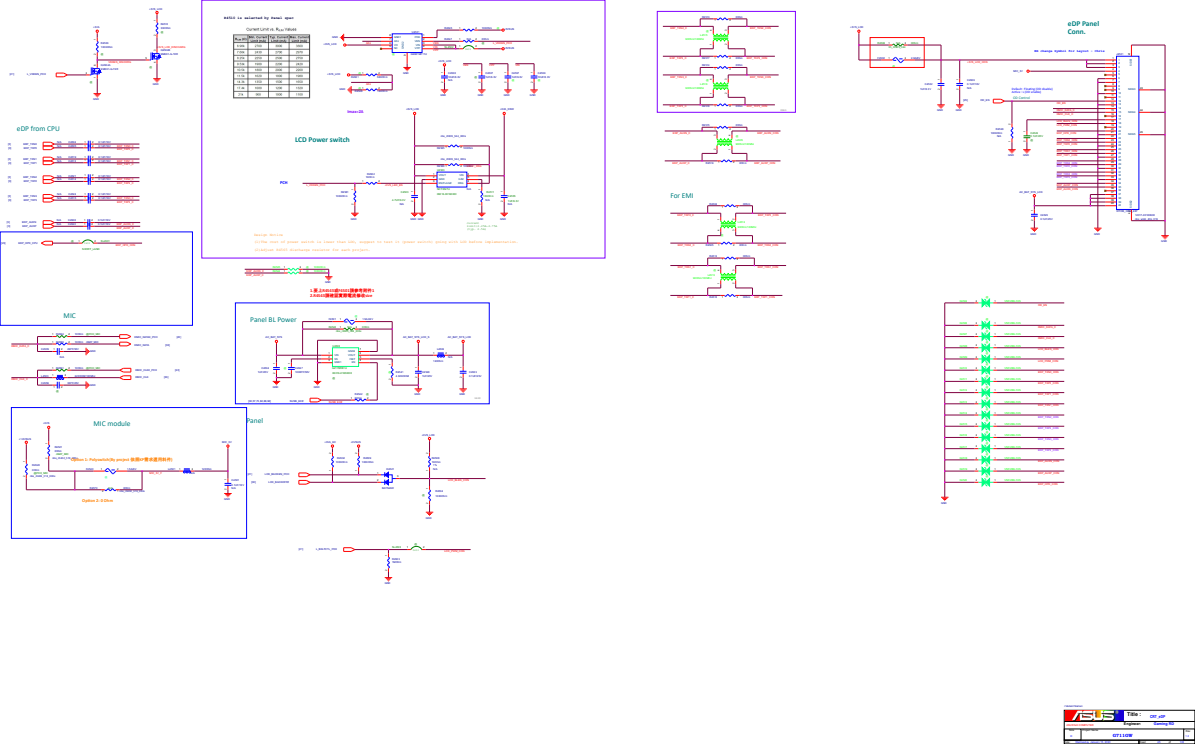
Title : Thunderbolt

Size Custom	**Dept.:** ASUSTeK COMPUTER	**Engineer:** Gaming RD

Date: Wednesday, January 15, 2020	Sheet	68	of	103

<Variant Name>

ASUSTeK COMPUTER	Title : HDMI_DP_Switch	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 42 of 103	


eDP from CPU
MIC
MIC module
Panel
LCD Power switch
Panel BL Power
eDP Panel Conn.
For EMI
Option 1: Polyswitch(By pin)
Option 2: 0 Ohm
Title :
DRT_EDP
Engineer:
Shaoning Shi
Size:
A3
Number:
027-11038
Revision:
1.0
Date:
Sheet
of

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[0,3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI[0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

Power

R1.0-29

2017.03.21 AMP Change SMLH4825555

N key

Thermal sensor

Battery

IT5125VG-128/CX

EMI-GX501GI

For EMI

IMVP8 SA Power Good Robby 0613

ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000
	06037-00370000

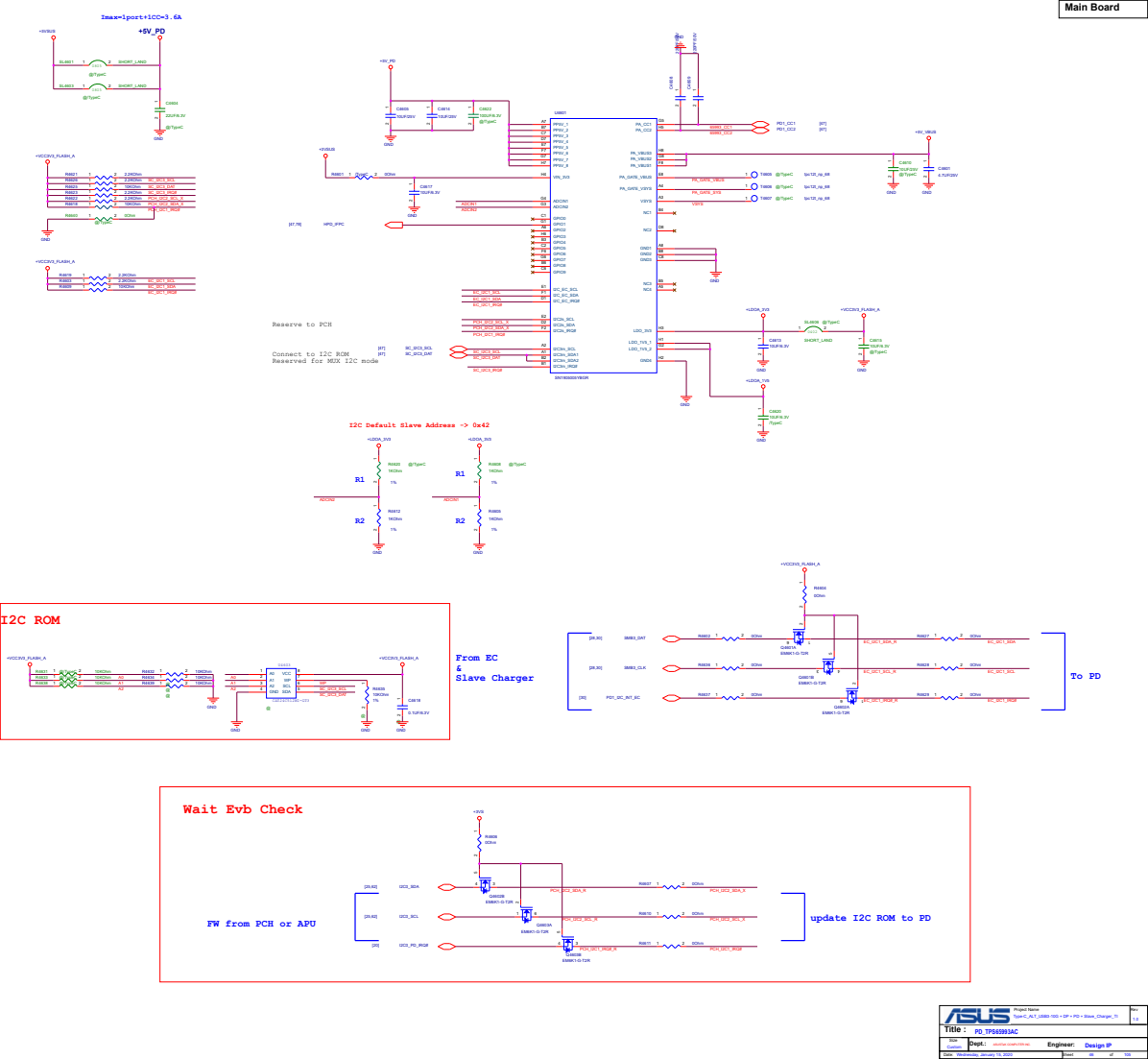
CORE PWRGood	0	1	0	1
SA PWRGood	0	0	1	1
IMVP8_PWRGD	0	0	0	1

R1.0-34

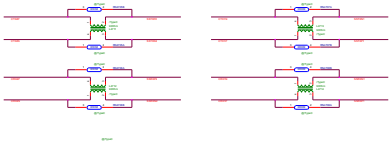
PU/PD

for load code

Title : CR_KBC_IT8521
Engineer: Gaming RD
ASUSTeK COMPUTER
Size: Custom | Project Name: G711GW | Rev: 1.0
Date: Wednesday, January 16, 2019 | Sheet: 50 of 100


Imax=1port+1CC=3.6A
+5V_PD
Reserve to PCH
Connect to I2C ROM
Reserved for MUX I2C mode
I2C Default Slave Address -> 0x42
I2C ROM
From EC
&
Slave Charger
To PD
Wait Evb Check
FW from PCH or APU
update I2C ROM to PD

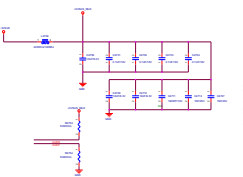
USB EMI-Protection

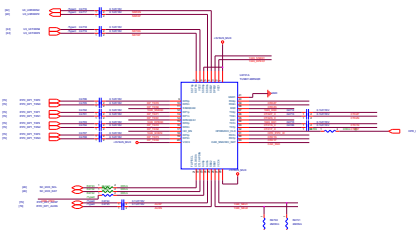


NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

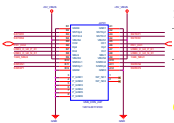
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISSOLSHED.





TYPE-C Connector



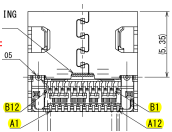
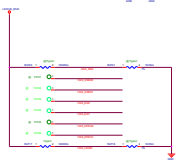
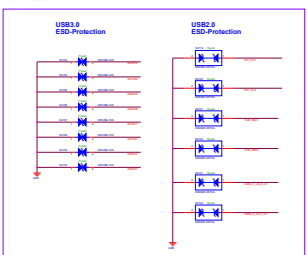


Table 2. GPIO Configuration Control

CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB1046A-DCI CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
L	L	L	Power Down	---
L	L	H	Power Down	---
L	H	L	One Port USB 3.1 – No Flip	---
L	H	H	One Port USB 3.1 – With Flip	---
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F



USB ESD-Protection



Main Board

HDMI Active-Level Shift

Modify (20181018)

to GPU

From GPU

Q4801只用07005-00660200與07005-00950000

HDMI PWR_+5VS_HDMI

HDMI Conn.

HDMI EMI

HDMI LDO 1.1VS

Imax = 0.35A

Imax = 0.35A

Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = 0, fastest data rate
SLEW_CTL = L, 5 pS slow
SLEW_CTL = No Connect, 10 pS slow

HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L, 2 dB de-emphasis level
PRE_SEL = No Connect
PRE_SEL = H: Reserved

I2C_EN/PIN = High: puts device into I2C control mode
I2C_EN/PIN = Low: puts device into pin strap mode

Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

Thermal Sensor : SN170027

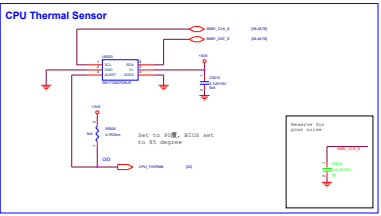
power rail : 3.3V

SMBUS1 to EC

ALERT/SDA/SCL: Open-drain output; pullup resistor 8Kohm

Pin function Supply voltage: 1.62 V to 3.6 V

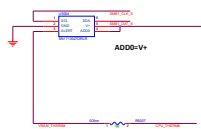
CPU Thermal Sensor



Near CPU

SMBUS addr=10010000 (90)

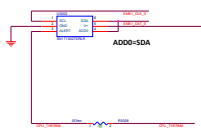
VRAM



Near VRAM

SMBUS addr=10010001 (91)

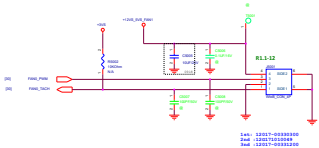
GPU



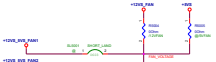
Near GPU

SMBUS addr=10010010 (92)

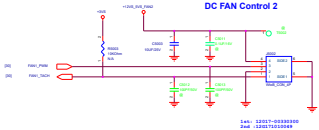
DC FAN Control 1



1st: 12017-00330300
2nd :120171010069
3rd :12017-00331200

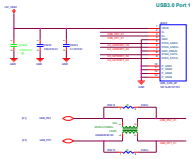


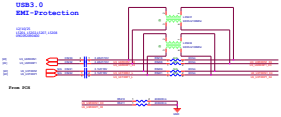
DC FAN Control 2

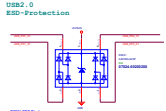


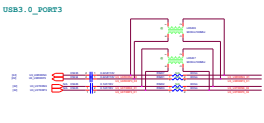
1st: 12017-00330300
2nd :120171010069

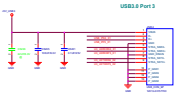
Main Board





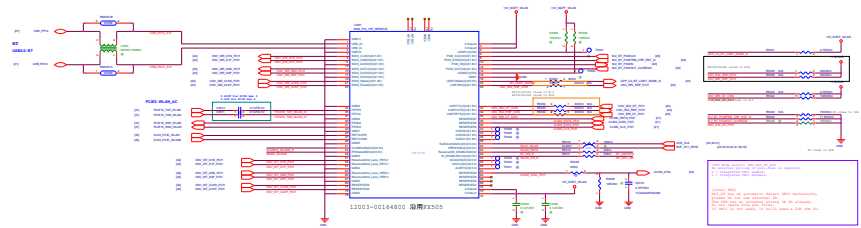


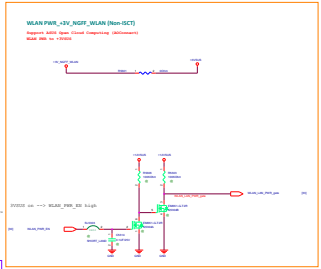


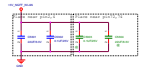


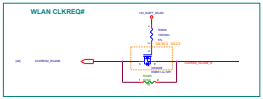
Title : USB Charger			
Engineer: Genning XU			
Size	Document Number		Rev
C	G7Z1UCM		
Date: Wednesday, January 08, 2014		Sheet 1 of 1	

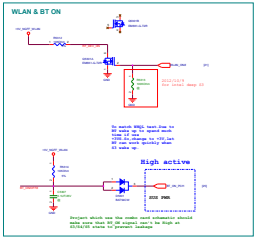
NGFF M.2 TYPE_E-KEY WIFI

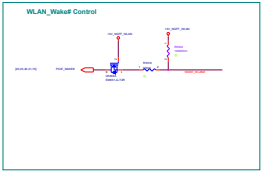












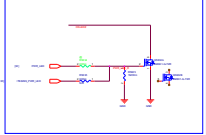
Title :	NGFF/WiMax		
Engineer :	SD		
Size	Document Number		Rev
GX502GS/E			
Date:	Sheet	of	

<Variant Name>

ASUSTeK COMPUTER	Title : USB3_*****	
	Engineer: Gaming RD	
Size: Custom	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 54 of 103	

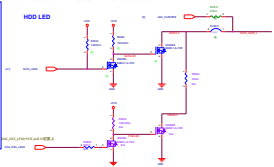
2014/05/29 Add HDD & SSD LED control circuit.

OS LED

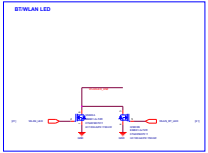


Charger LED

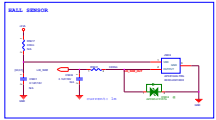
HDD LED



BTWLAN LED

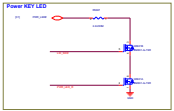


WALL SENSOR

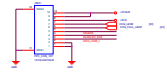


CAP LED

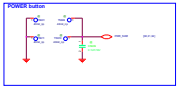
Power KEY LED



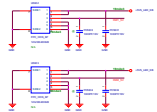
LED Board

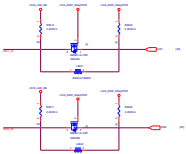


POWER button

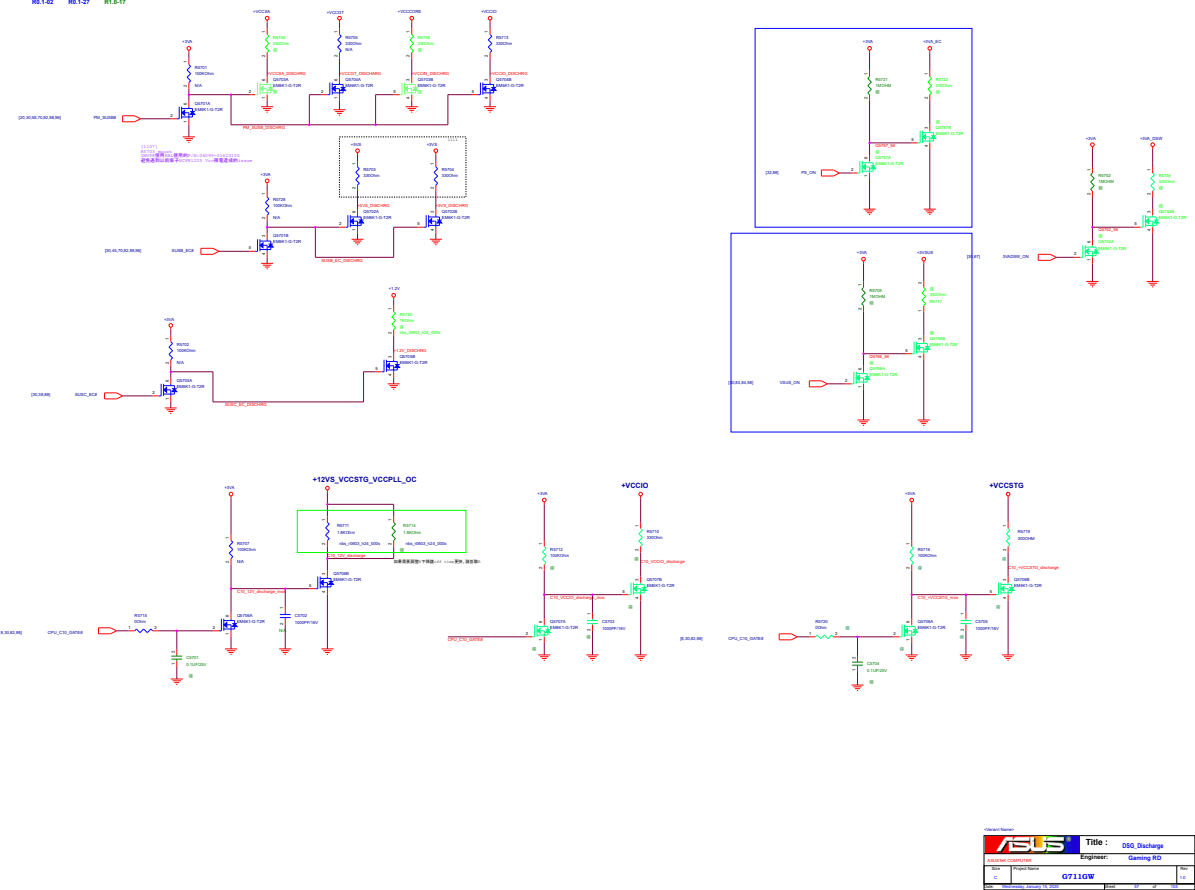


One-wire Connect to LED

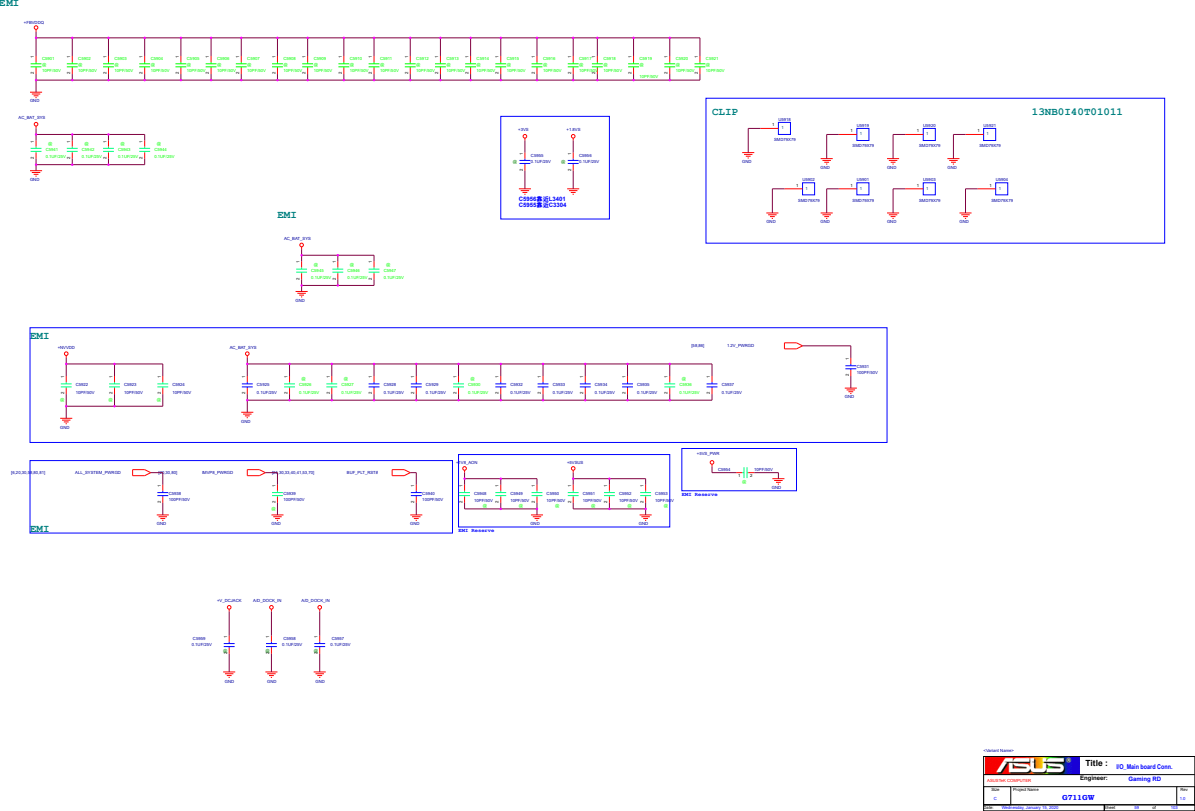




Title :	LED & LID		
Engineer:	Sandy Hi		
Size	Document Number		Rev
B	0171.LIDW		
Date: 2017-05-17	Sheet 1	of 1	

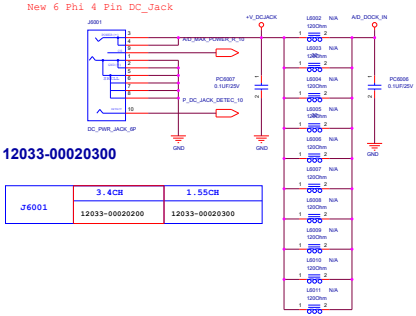


Title :	DSG_Discharge		
Engineer:	Gaming RD		
Size	Project Name		Rev
C	G711GW		1.0
Date:	Wednesday, January 19, 2022	Sheet	of



DC-IN Connector

DC Jack使用請詢用River_Hsu



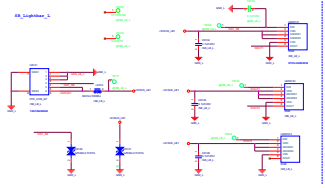
12033-00020300

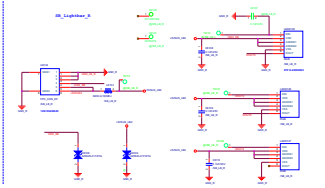
	3.4CH	1.55CH
J6001	12033-00020200	12033-00020300

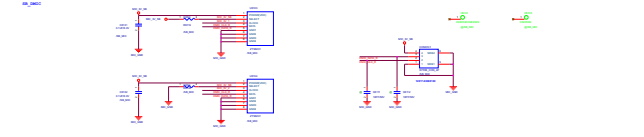
Battery Connector

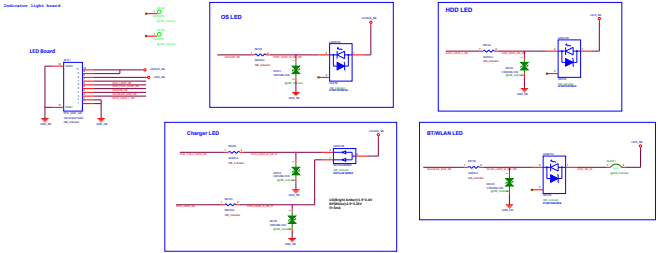
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GX700		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Wednesday, January 15, 2020	Sheet 60 of 103		

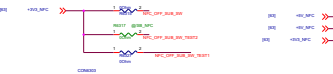


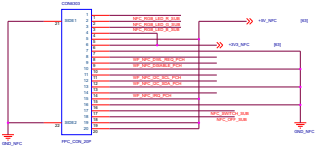


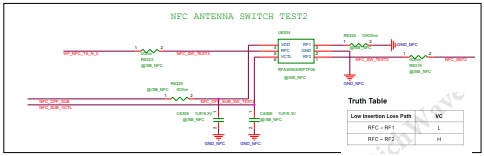




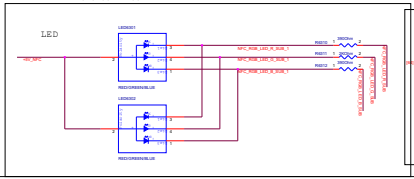
Quanta Computer Inc.		Title :	SB_Lightbar_BMC		
Size	Document Number	Rev	Engineer :	Samuel.Hsu	
A3	GT3	1.0W			
Date: Wednesday, January 16, 2013		Sheet 1 of 1			

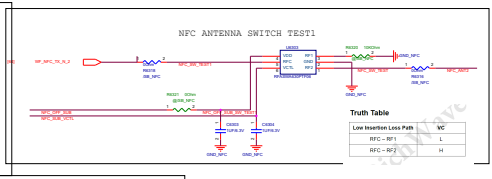


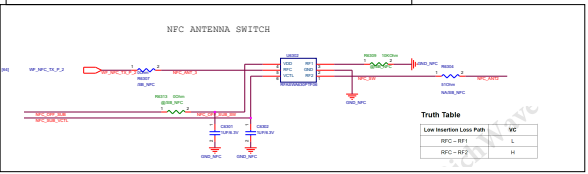


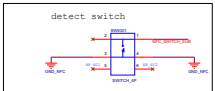


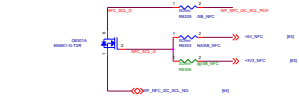
12018-00221100

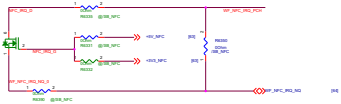


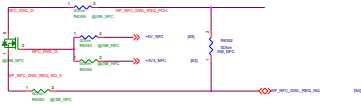


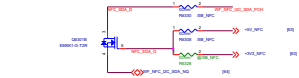


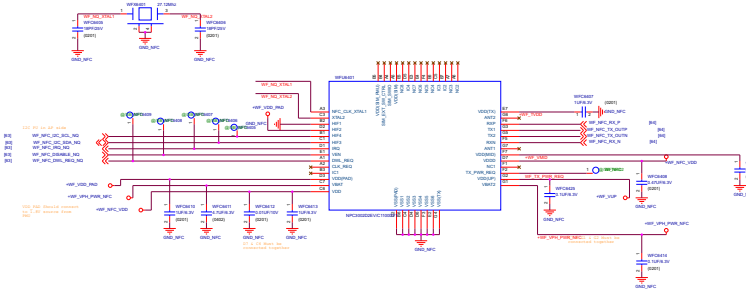




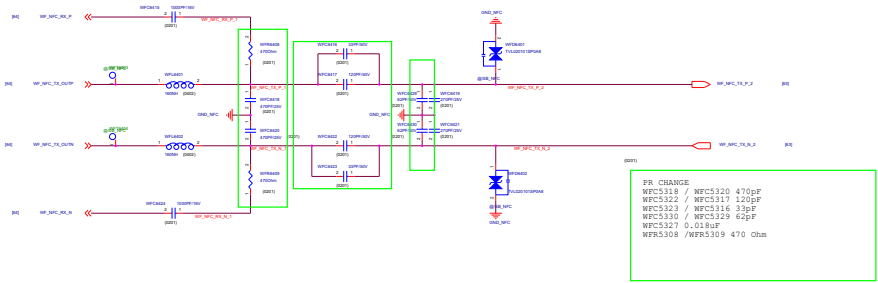




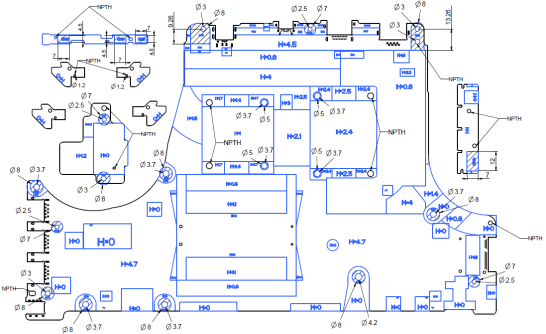




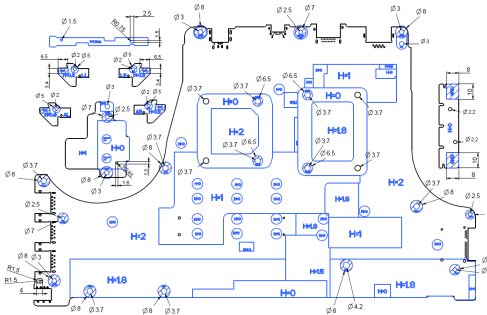
NFC Matching



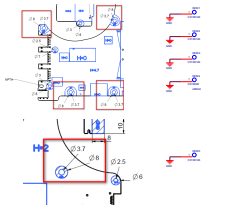
BOTTOM



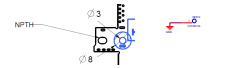
TOP



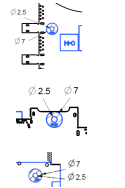
PTH 8 /3.7mm



PTH 8 /3 mm

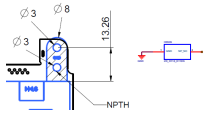


PTH 7 /2.5mm

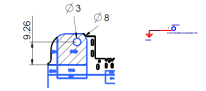


PTH 8 /4.2 mm

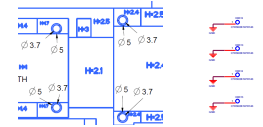
PTH 8 /3mm+ NPTH 3mm



PTH 8/3mm (Ext.)

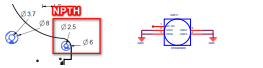


PTH 6.5 /5 /3.7 mm

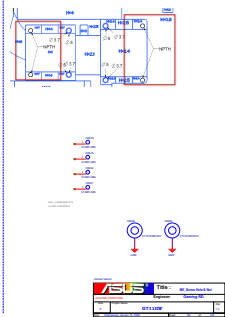


NPTH 1.5/ 4mm

NPTH 6/ 2.5 mm

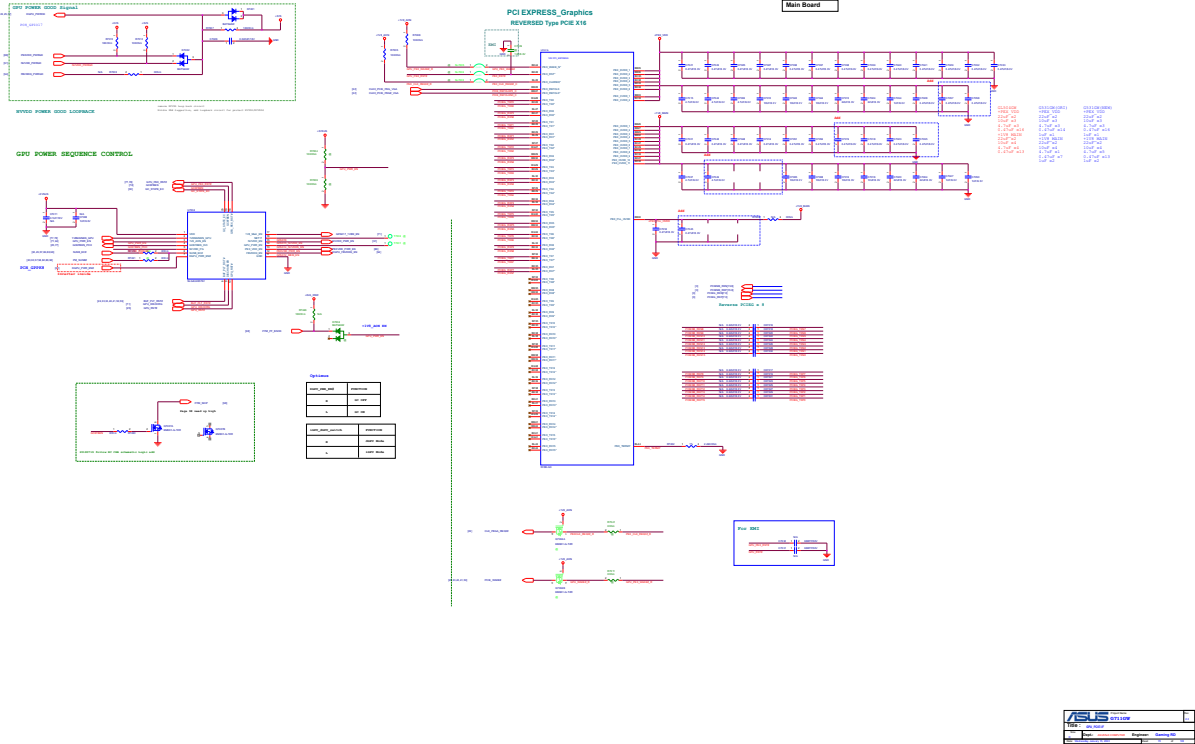


NPTH 3.7 mm



<Variant Name>

ASUSTeK COMPUTER	Title : OTH_EMI	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, January 15, 2020	Sheet 69 of 103	

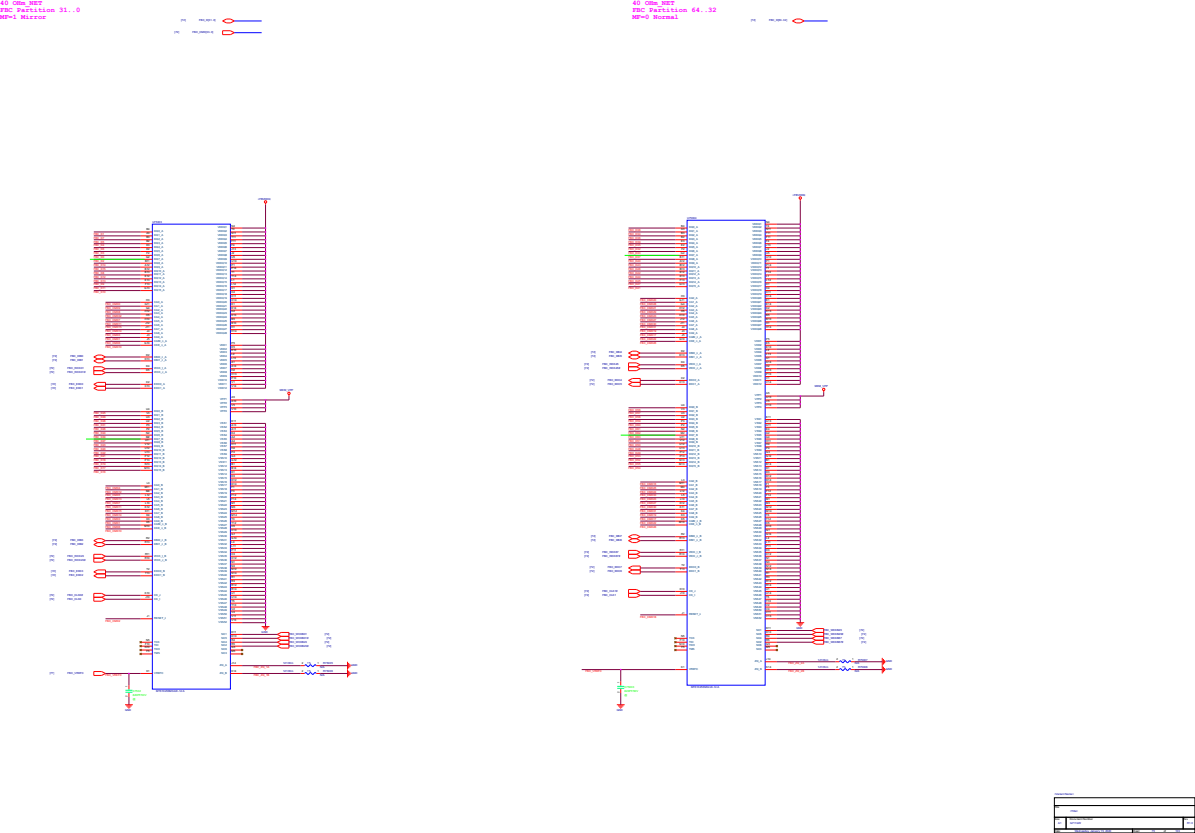

Main Board
GPU POWER GOOD Signal
PCI EXPRESS_Graphics
REVERSED Type PCIE X16
SYSTEM POWER GOOD SEQUENCE
GPU POWER SEQUENCE CONTROL
PCH_GPIO58
Options
Reverse PCIE0 to 0
Fan SEC
Title: ROG MAXIMUS XI HERO (WI-FI)
Size: A3
Date: Monday, March 04, 2019
Engineer: Gaming RD
Sheet 1 of 1

40 CHs_NET
FBB Partition 31..0
MF=1 Mirror

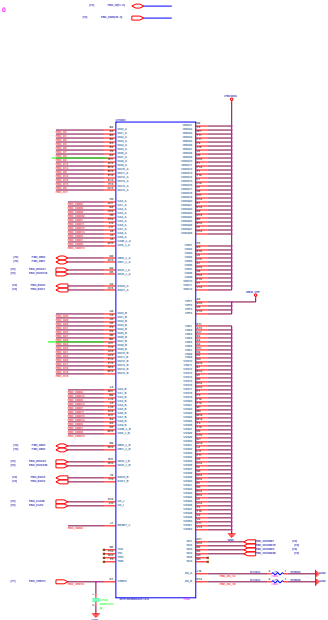
40 CHs_NET
FBB Partition 64..32
MF=0 Normal

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror

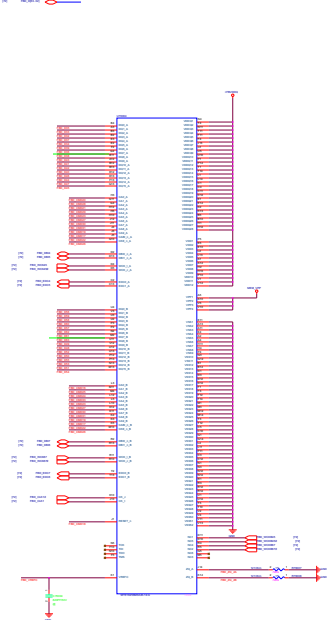
40 OHm_NET
FBC Partition 64..32
MF=0 Normal

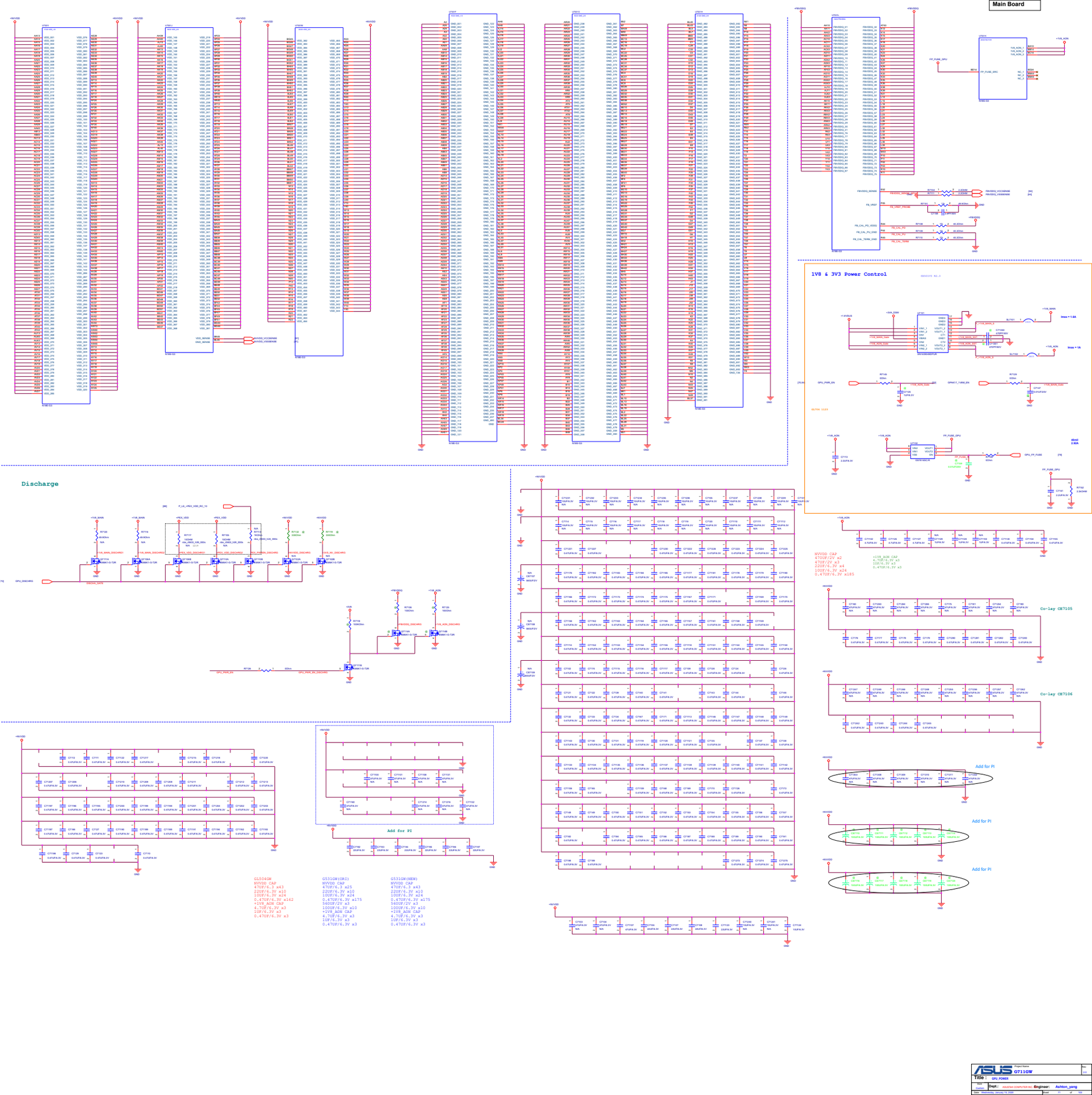


40 OMa_NET
FPS0 Partition 31..0
MF=1 Mirror

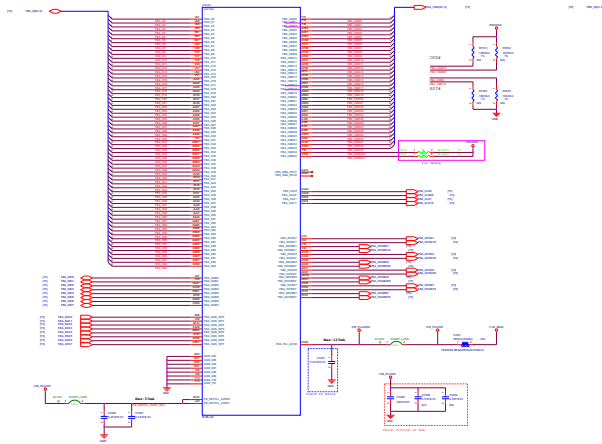


40 OMa_NET
FPS0Partition 64..32
MF=0 Normal

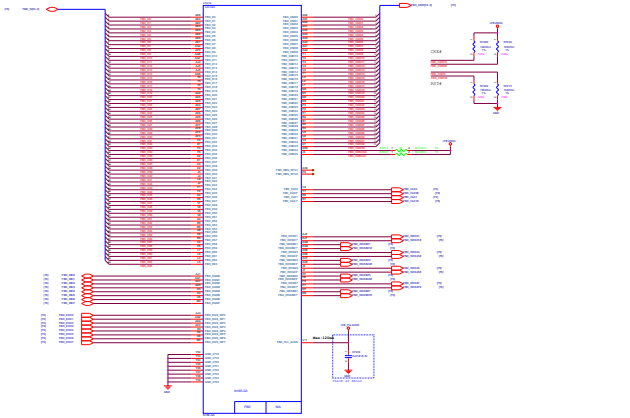



Main Board
1V8 & 3V3 Power Control
Discharge
Add for PI
Add for PI
Add for PI
Add for PI
Co-lay CM7105
Co-lay CM7106
GPU_PWR_EN
GPU_FF_FUSE
GPU_DISCHRG
NVVDD CAP
470UF/2V x2
470UF/2V x3
220UF/6.3V x4
100UF/6.3V x24
0.47UF/6.3V x185
+1V8 AON CAP
470UF/2V x3
100UF/6.3V x3
0.47UF/6.3V x3
GL504GW
NVVDD CAP
470UF/6.3 x43
220UF/6.3V x10
100UF/6.3V x24
0.47UF/6.3V x162
+1V8 AON CAP
4.7UF/6.3V x3
10UF/6.3V x3
0.47UF/6.3V x3
G531GW(ORI)
NVVDD CAP
470UF/6.3 x25
220UF/6.3V x10
100UF/6.3V x24
0.47UF/6.3V x175
560UF/2V x3
100UF/6.3V x10
+1V8 AON CAP
4.7UF/6.3V x3
10UF/6.3V x3
0.47UF/6.3V x3
G531GW(NEW)
NVVDD CAP
470UF/6.3 x43
220UF/6.3V x10
100UF/6.3V x24
0.47UF/6.3V x175
560UF/2V x3
100UF/6.3V x10
+1V8 AON CAP
4.7UF/6.3V x3
10UF/6.3V x3
0.47UF/6.3V x3
ASUS
Project Name: G711GW
Title: GPU_POWER
Dept.: ASUSTeK COMPUTER INC
Engineer: Ashton_yang

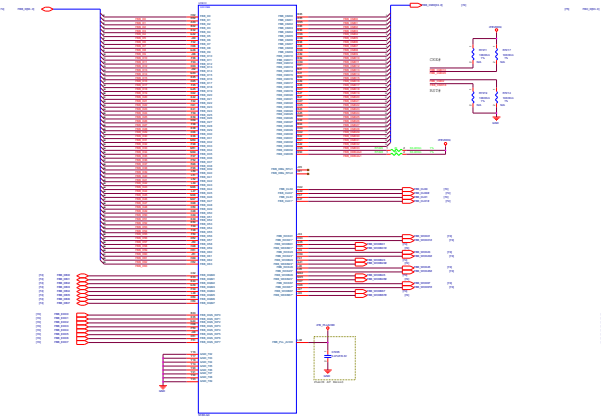
MEMORY: GPU FB Partition A



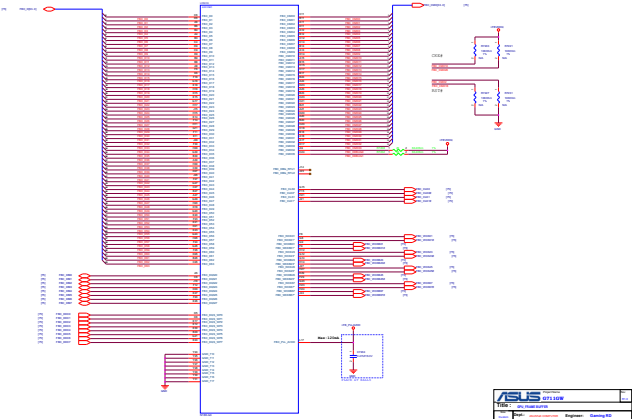
MEMORY: GPU FB Partition D

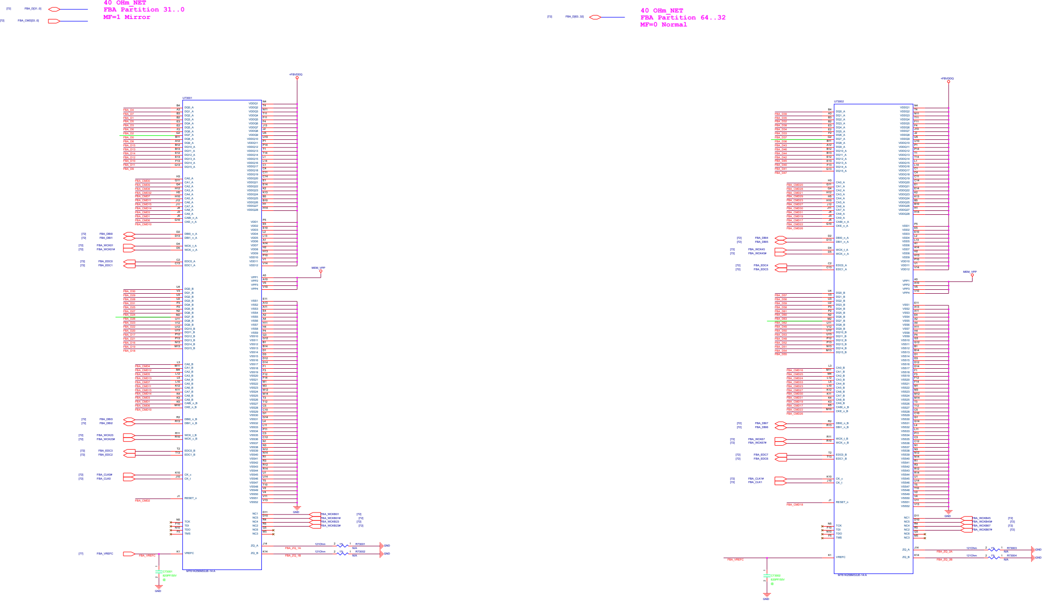


MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C

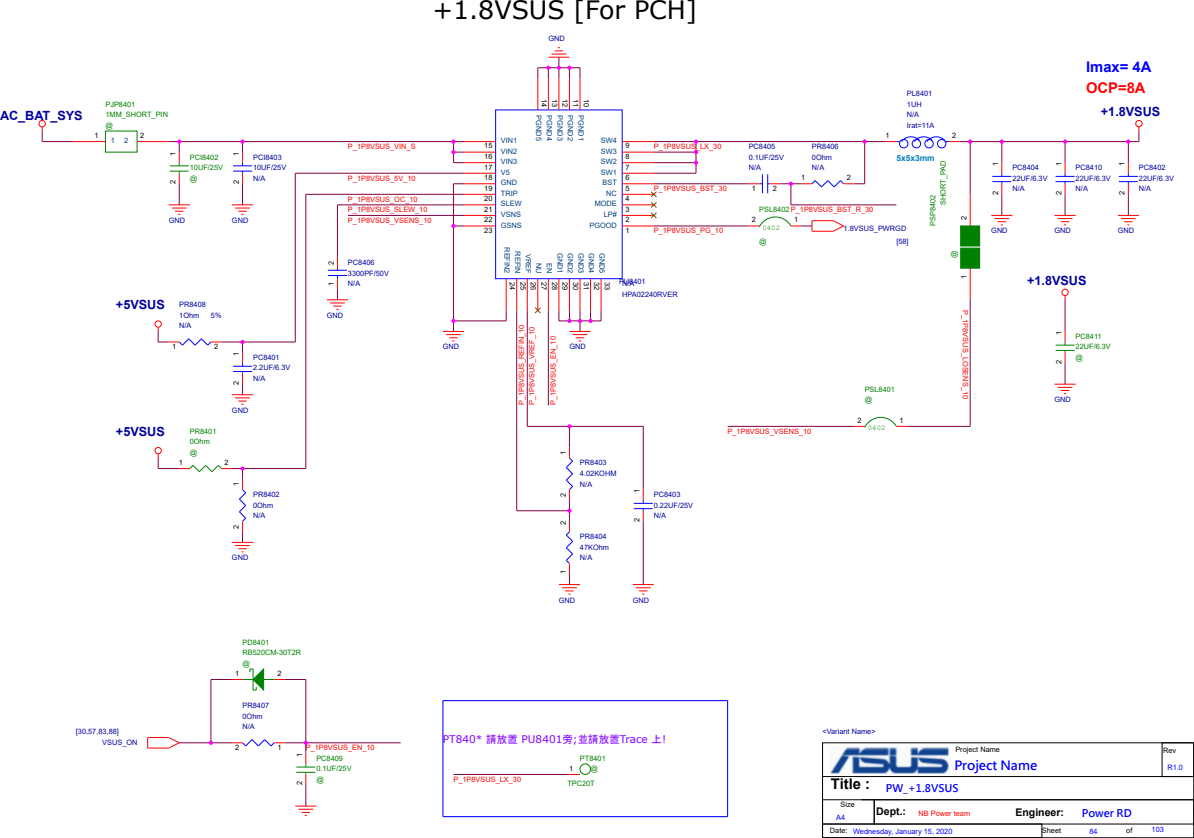




<Variant Name>

Title	<Title>	
Size A1	Document Number G711GW	Rev R1.0
Date: Wednesday, January 15, 2020	Sheet 73 of 103	

+1.8VSUS [For PCH]



<Variant Name>

ASUS	Project Name: Project Name	Rev: R1.0
Title : PW_+1.8VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Wednesday, January 15, 2020	Sheet 84 of 103	

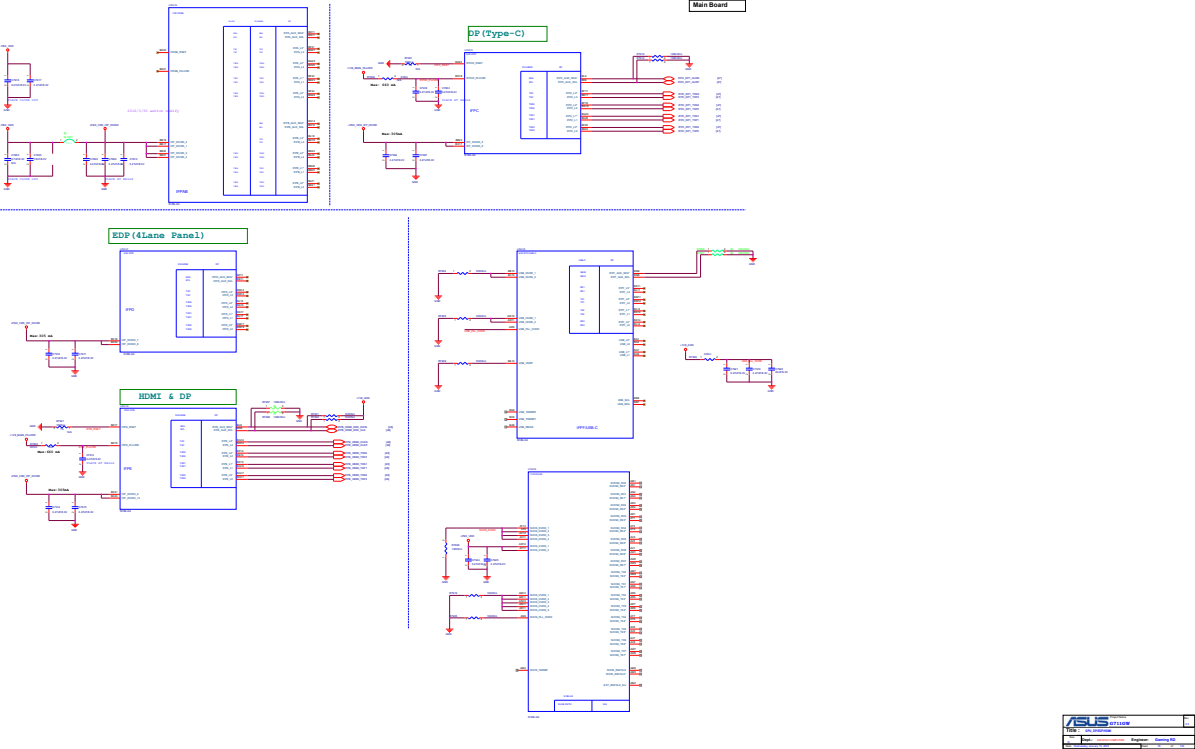
<Variant Name>

	Project Name GM531GX	Rev R1.0

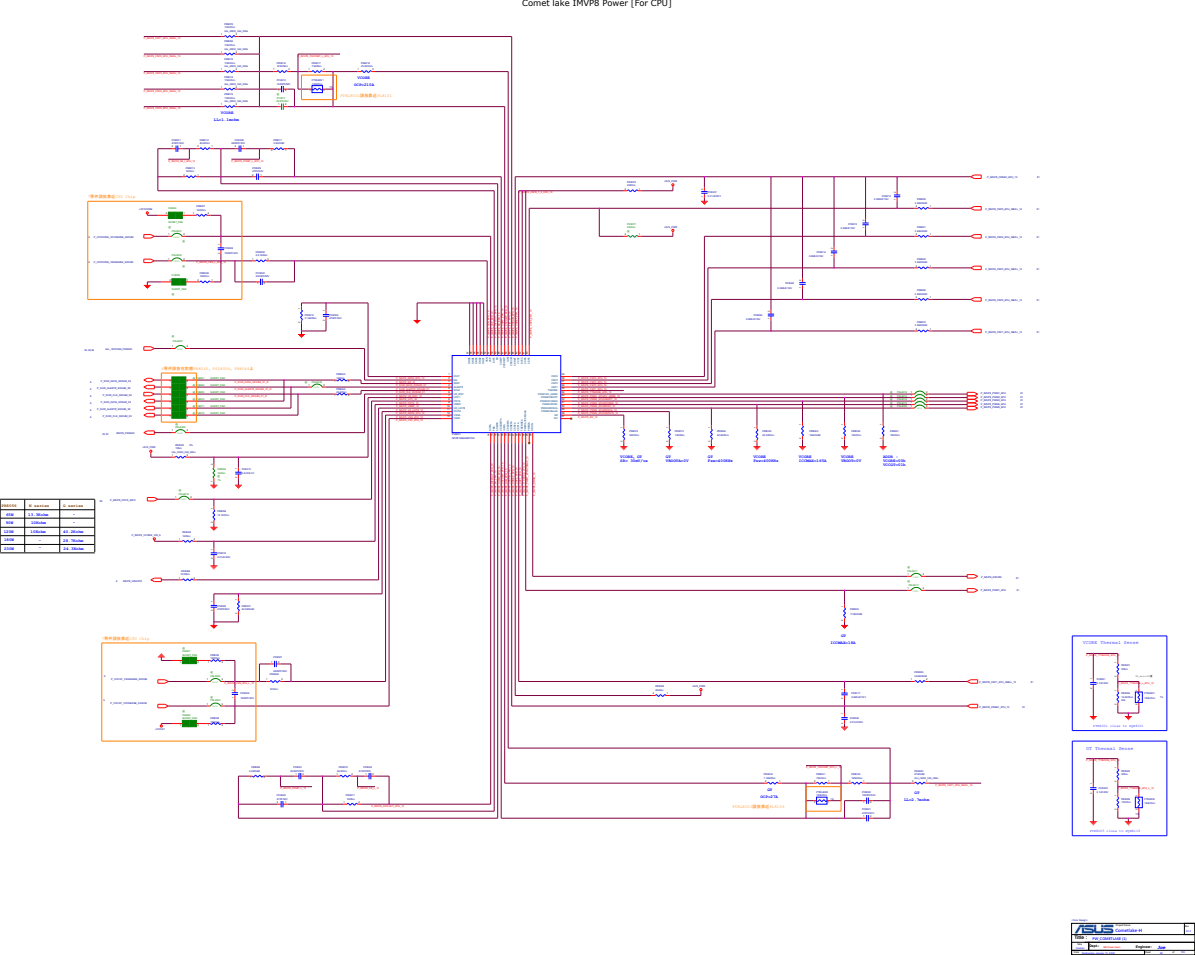
Title : Thunderbolt

Size Custom	**Dept.:** ASUS Power Team	**Engineer:** Joe

Date: Wednesday, January 15, 2020	Sheet	85	of	103

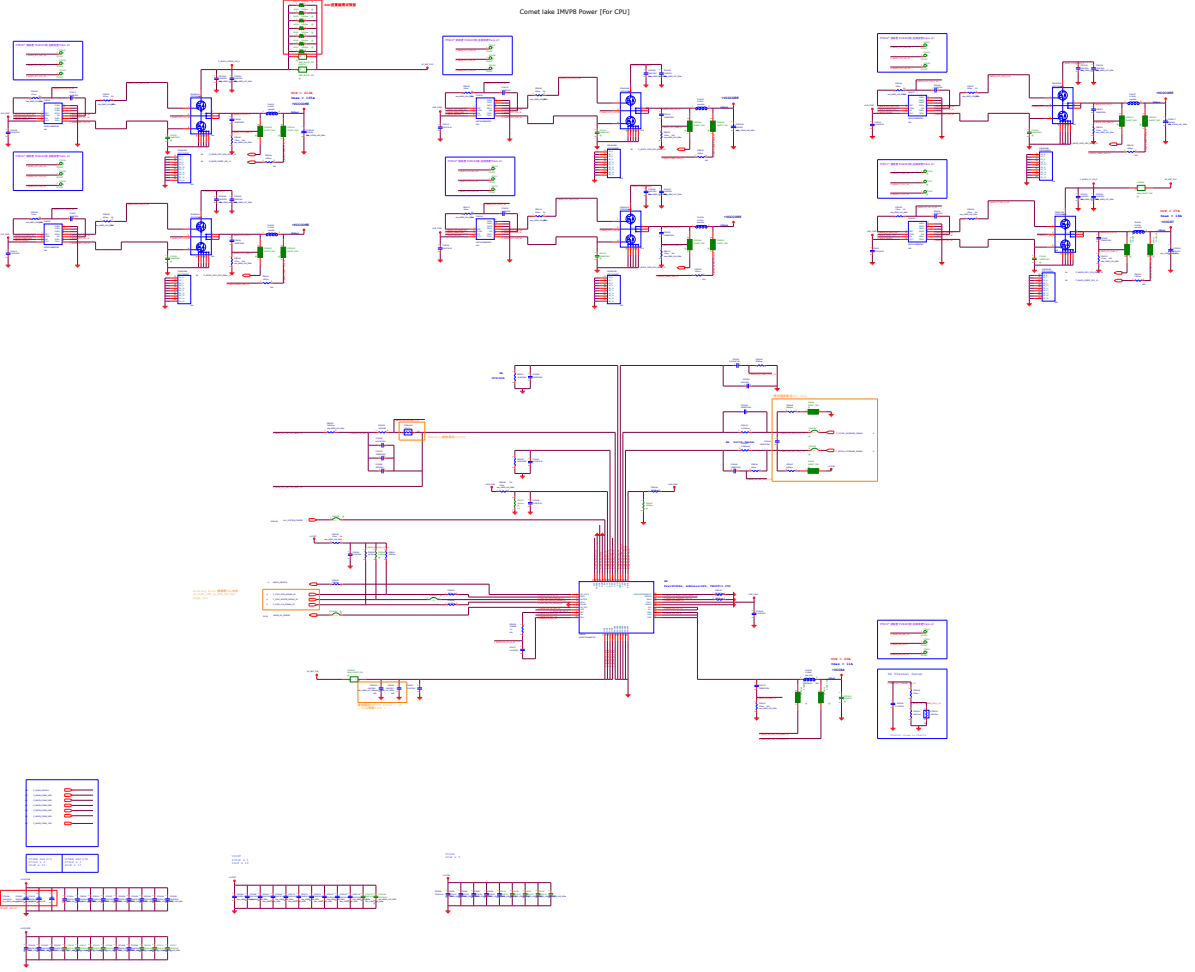


Title:			
Size:	Project:	Version:	Engineer:
Date:	Sheet:	of:	File:

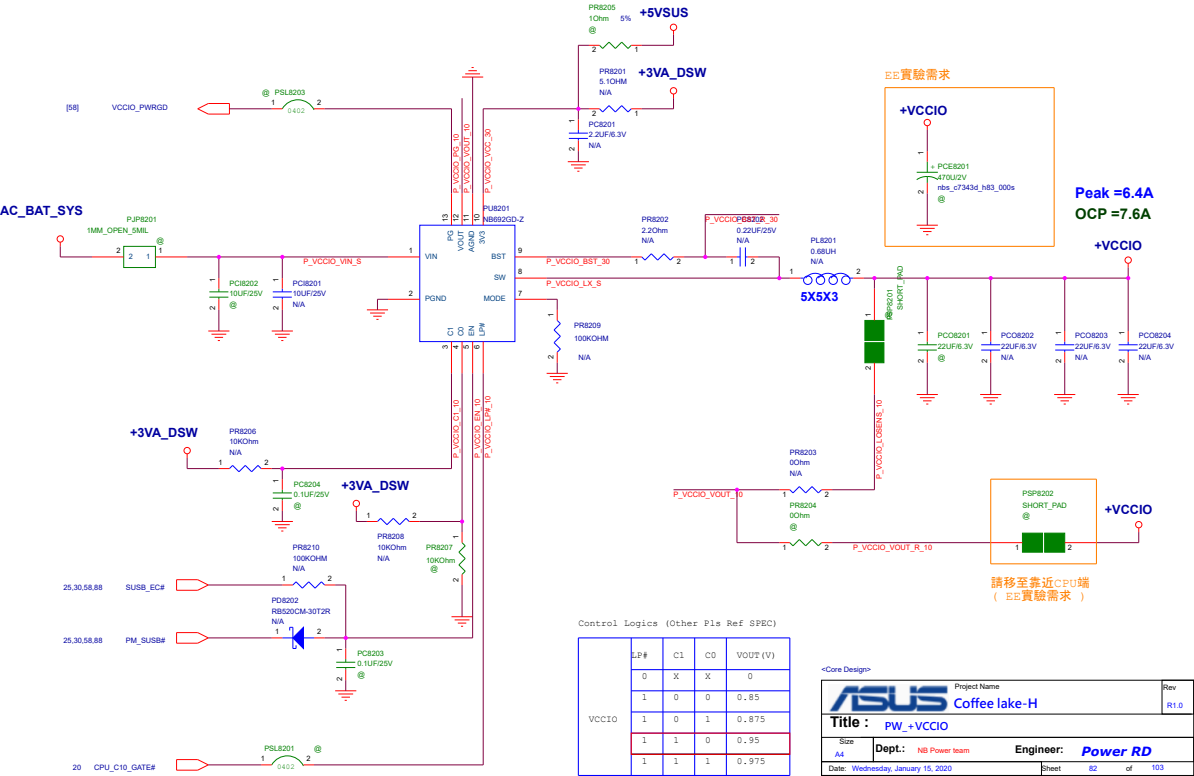


PSID(TS)	R value	C value
00H	1.1 - 30ohm	-
01H	100ohm	-
10H	130ohm	10 - 33nfm
11H	-	33 - 75nfm
21H	-	75 - 150nfm

Title:	File: C1MVP2.SCH		
Size:	Document Number:	Rev:	
Date:	Sheet of		



+VCCIO [For CPU]



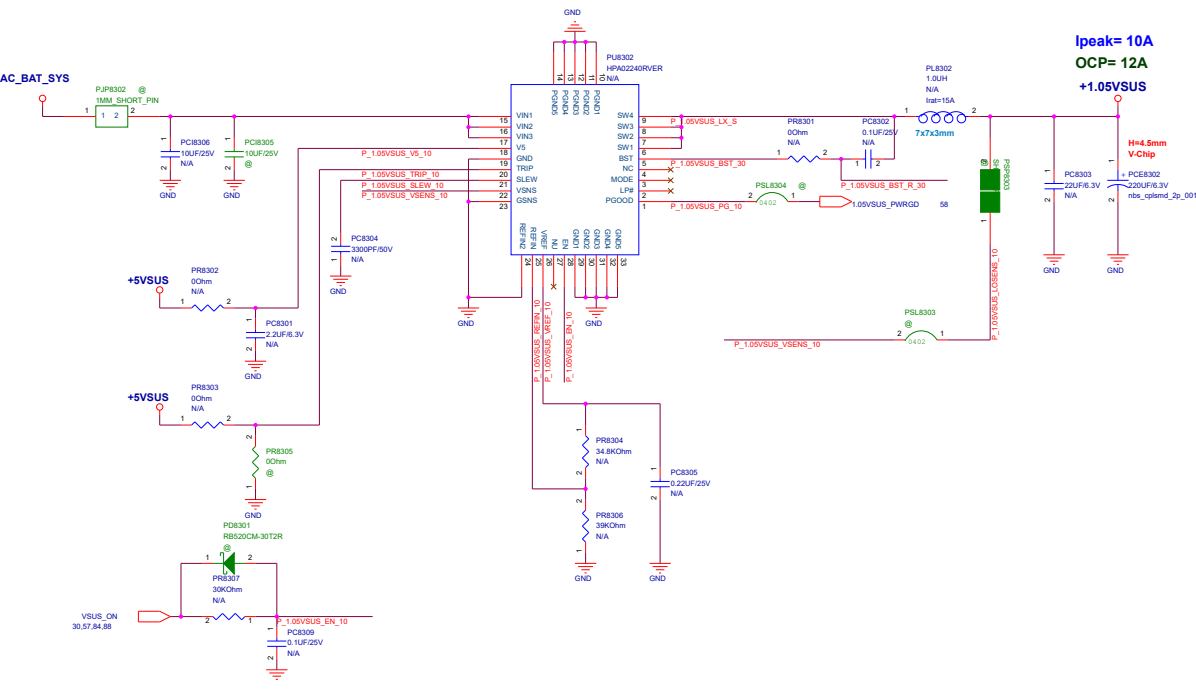
Control Logics (Other Pls Ref SPEC)

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

<Core Design>

Project Name: Coffee lake-H		Rev: R1.0
Title : PW_+VCCIO		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Wednesday, January 15, 2020	Sheet 82 of 103	

+1.05VSUS [For PCH]



PT840* 請放置 PU8401旁;並請放置Trace 上!

PT8301 NB_TPC20T @

P_1.05VSUS_LX_S

Project Name: Coffe Lake-H			Rev: R1.0
Title : PW_+1.0VSUS			
Size: A4	Dept.: NB Power team	Engineer: Power RD	
Date: Wednesday, January 15, 2020	Sheet 83 of 103		

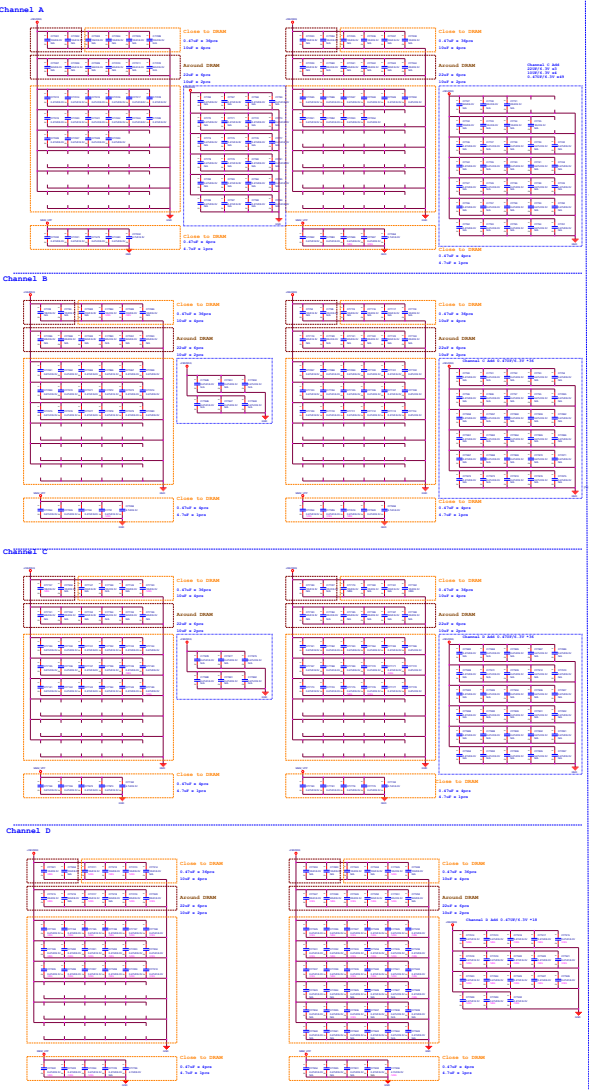
<Variant Name>

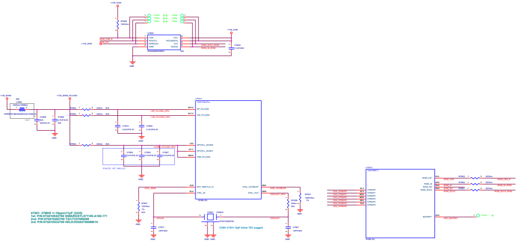
	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

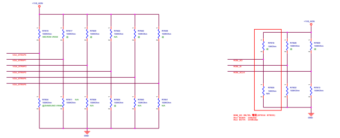
Size Custom	**Dept.:** NB Power Team	**Engineer:** Joe

Date: Wednesday, January 15, 2020	Sheet	93	of	117


Channel A
Close to DRAM
0.47uF x 3pcs
10nF x 4pcs
Around DRAM
20nF x 6pcs
10nF x 2pcs
Channel C Add 0.47UF/6.3V x10
100K/1% 5V x1
0.47UF/1.5V x10
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Channel B
Channel D Add 0.47UF/6.3V *16
Channel C Add 0.47UF/6.3V *16
VRAM PWR_FBVDDQ
Partition A under GPU
Partition B under GPU
Partition C under GPU
Partition D under GPU
Power GPU
0.47uF x 12pcs
10nF x 2pcs
10nF x 7pcs
Power CTRL01
Add for FC
For power sequence measurement
GDDR6 VDD power +1.8V
GDDR6 VPP power +1.8V
CLOCK/CA
CK/CA/DQ(A1)
CK/CA/DQ(B1)
CK/CA/DQ(B2)
CK/CA/DQ(B3)
VRAM PWR
Channel A
Channel B
Channel C
Channel D
0.47UF/6.3V x40
100K/1% 5V x12
220K/1% 5V x11
0.47UF/1.5V x40
100K/1% 5V x10
0.47UF/6.3V x44
0.47UF/1.5V x44
0.75UF/6.3V x40



STRAP PIN



	Physical Configuration	
Level Option	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

Assorted Configuration Straps

1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2C address 0x9E, "1" Dual GPU setting I2C address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0" normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(invalid; do not configure)

Strap 0X1 - GDDR5X B-die

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Memory Configuration	FBVDDQ/2	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Start	Qual Plan	Status
8 Gb	2Gx256Mx16	1.35V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Pass	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x6	14 Gbps	N/A	Pass	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WDK: TBD

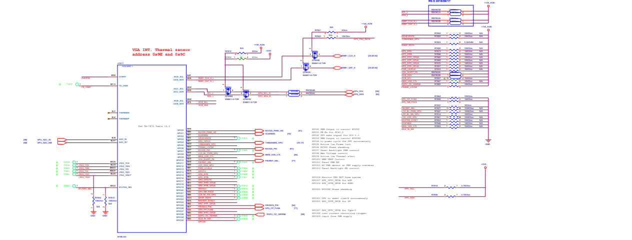
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

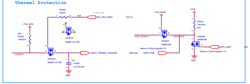
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is eDP Supported on: IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	See This Row of Table 5.4
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	[illegible]
4	3	--	--	yes	[illegible]
3	3	--	--	--	[illegible]
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	[illegible]	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

VGA INT. Thermal sensor address 0x9E and 0x9C

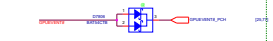


Thermal Protection



VGA EXT. Thermal Sensor

GPU GPIO INPUT

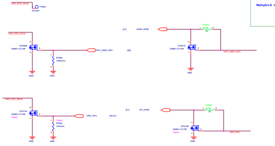


NVIDIA GC6 2.0 follow DG-07290-001_v01
GPU_GPIO 5 --> FRAME_LOCK# (Input, Open Drain)
High -->driver display ,Low Normal

FRAME_LOCK#_C Pull High +3VS_LCD at Panel side

Mshybid not support NVSR panel (frame lock)

HPD Invert



ASUS	Project Name: G711GW			Rev: 2.0
Title :	GPU_CLOCK/STRAP/GPIO			
Size: Custom	Dept.: ASUSTeK COMPUTER		Engineer: Gaming RD	
Date: Wednesday, January 15, 2020		Sheet: 78	of 103	

<Variant Name>

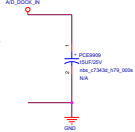
	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

Size	Dept.:	Engineer:
Custom	NB Power Team	Joe

Date: Wednesday, January 15, 2020	Sheet	95	of	117

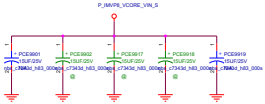
A/D_DOCK_IN



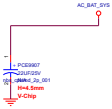
5VSUS

SA

VCORE

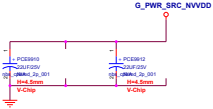


Charger



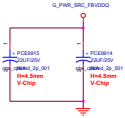
GT

NVVDD (X70)

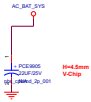


1.05

FBVDDQ



1.2

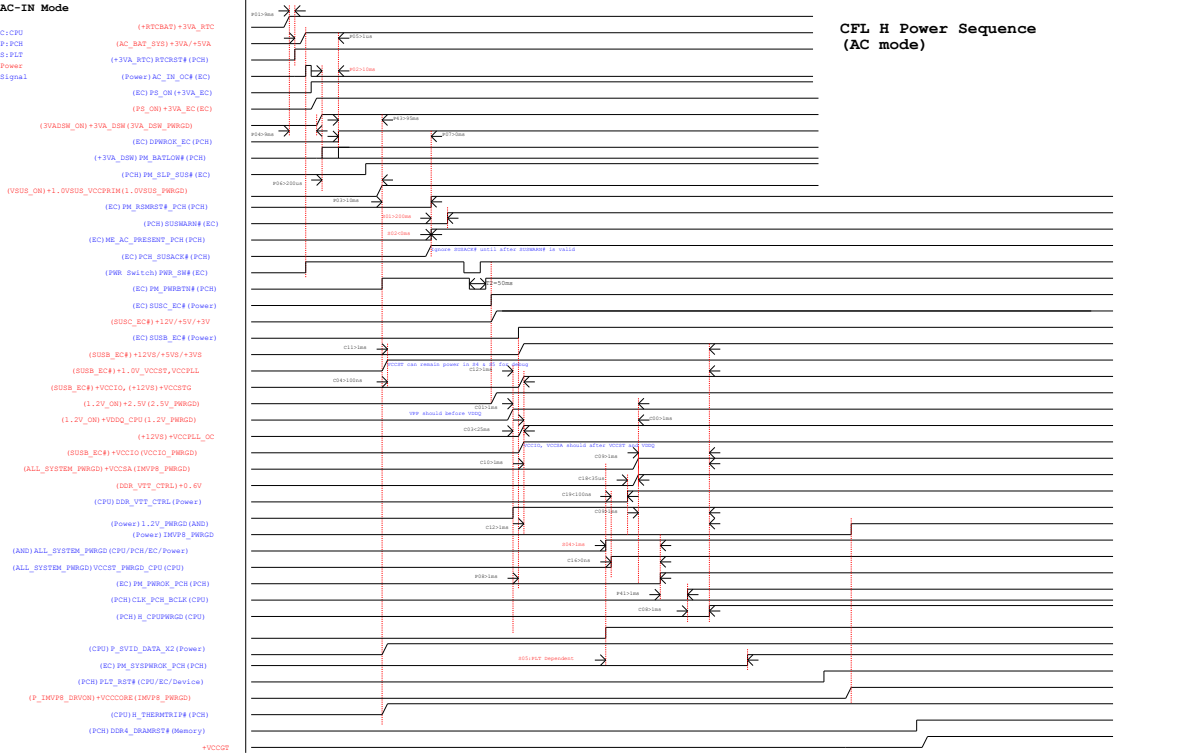


VCCIO

***共12顆**

***請將對應電容放置對應PWR VRM輸入端**

AC-IN Mode



CFL H Power Sequence (AC mode)

ASUS	Project Name: G711GW		Rev: 0.5
Title :	Power On Timing-AC mode		
Size: Custom	Dept.: MB/PM COMPUTER	Engineer:	Gaming RD
Date: Wednesday, January 16, 2019	Sheet	of	

Rev	Date	Description
1.0	2019.04.03	1.Based on G5_GS31GE_REA_MB_0410_R10 change to GM1-M
	2019.04.04	2.Change CPU from GPL to CML
	2019.04.04	3.Change PCH from CPL to CML

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK Computer Inc.

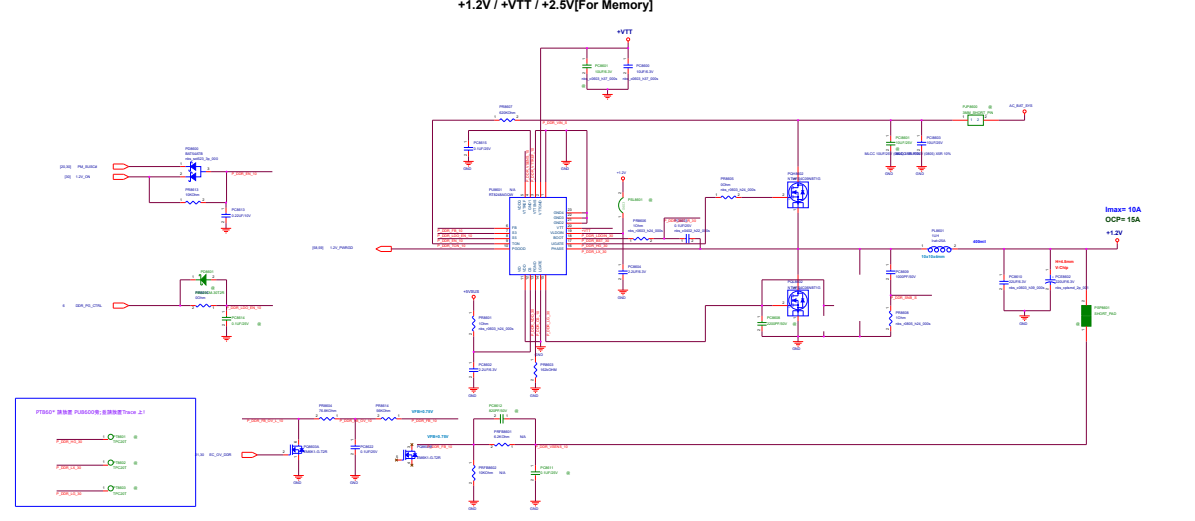
Title : Revision History

Engineer: Sammy Hsi

Size	Document Number	Rev
A4	GPJ10GM	

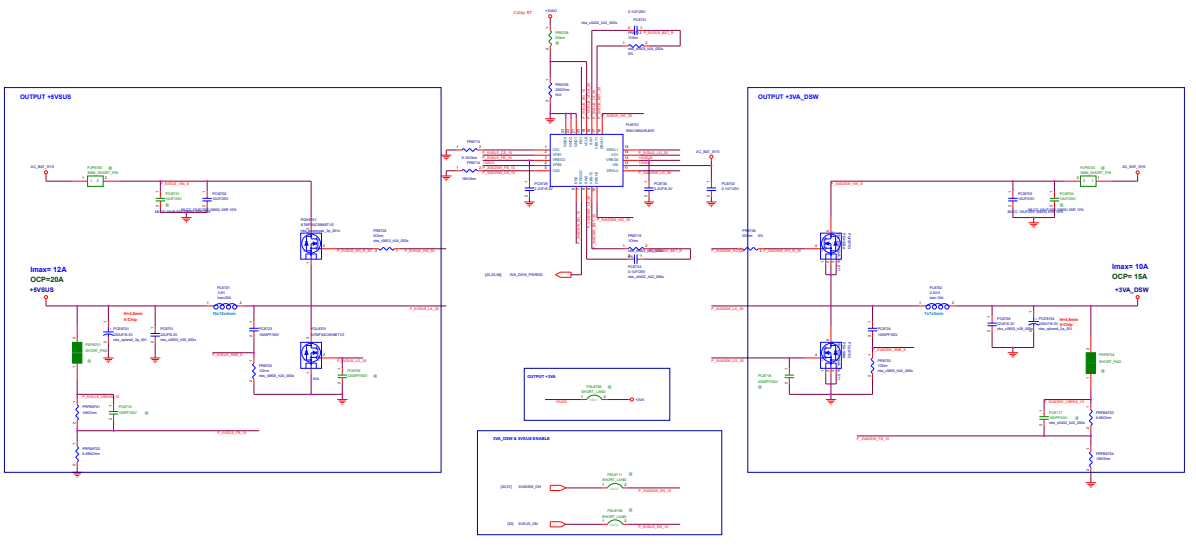
Date: Monday, December 09, 2019 Sheet of

+1.2V / +VTT / +2.5V[For Memory]



Project Name: G711GW			Rev: 0.3
Title: PM_+1.2V/+VTT/+2.5V			
Size: A3	Dept.:	Engineer: Neil	
Date: Wednesday, January 15, 2020	Sheet: 86	of: 100	

+3VA_DSW / +5VSUS [System Power]



Adaptor Mode (MVPS)

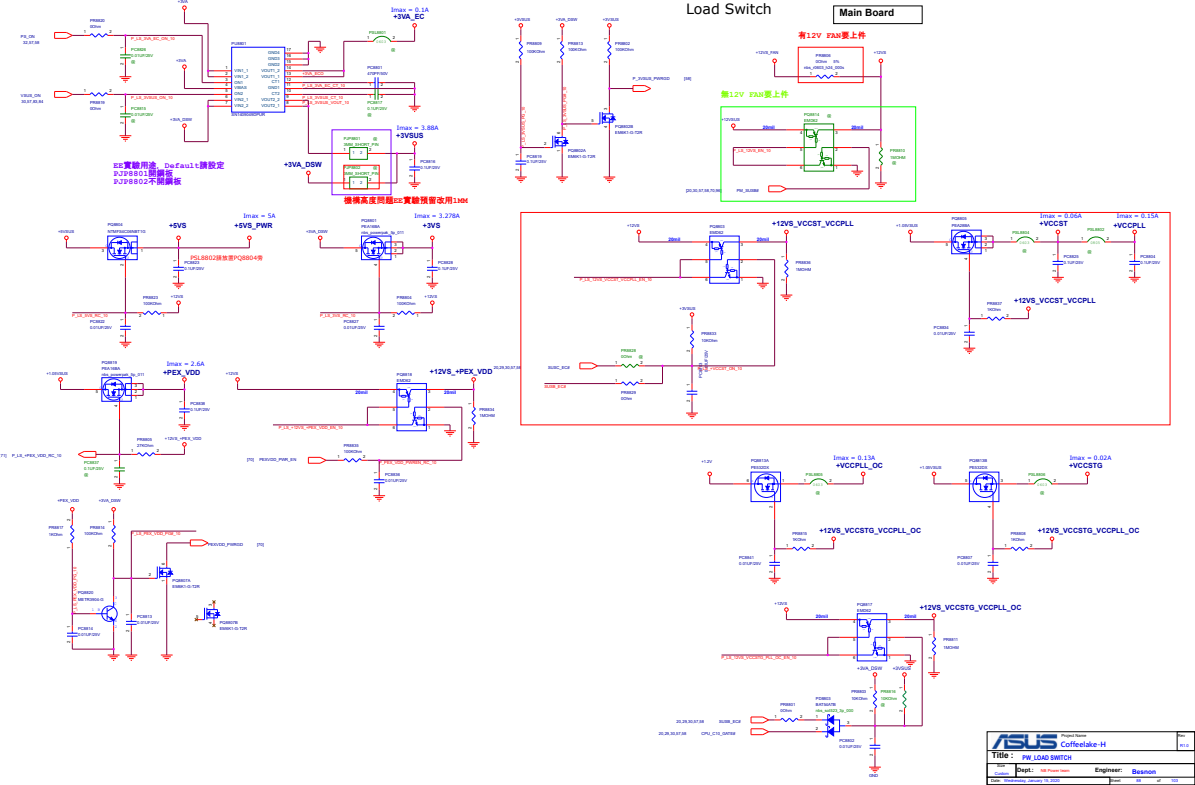
	S0	CS	S1	DS3	S3	S5	S5 with USB Charge=
PS_ON	1	-	1	-	1	-	1
5VALW_ON	1	-	1	-	1	-	1
3VALW_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.05V_ON	1	-	1	-	0	-	0
SUSC_SCB	1	-	1	-	0	-	0
SUSB_SCB	1	-	0	-	0	-	0

Battery Mode (MVPS)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charge=
PS_ON	1	-	1	0	0	0	1
5VALW_ON	1	-	1	1	0	0	0
3VALW_ON	1	-	1	1	0	0	0
5VSUS_ON	1	-	1	1	0	0	1
1.05V_ON	1	-	1	1	0	0	0
SUSC_SCB	1	-	1	1	0	0	0
SUSB_SCB	1	-	1	1	0	0	0

請 check 整個線路 +12VSUS total 並聯對地電阻不得小於10ohm

ASUS	Project Name: G711GW		Rev: REV:0
Title :	PW_+3VA_DSW/+5VSUS		
Size:	Dept.: VS Power Team	Engineer: Neil	
Date: Wednesday, January 15, 2020		Sheet: 60 of: 100	


Load Switch
Main Board
有12V FAN要上件
無12V FAN要上件
Imax = 0.1A
+3VA_EC
Imax = 3.88A
+3VSUS
+3VA_DSW
EE實驗用途 Default換設定
PJP8801開繼板
PJP8802不開繼板
機構高度問題EE實驗預留改用1MM
Imax = 5A
+5VS
+5VS_PWR
PQ8802換裝PQ8804等
Imax = 3.278A
+3VS
Imax = 2.6A
+PEX_VDD
+12VS_+PEX_VDD
+12VS_VCCST_VCCPLL
Imax = 0.06A
+VCCST
Imax = 0.15A
+VCCPLL
+12VS_VCCST_VCCPLL
Imax = 0.13A
+VCCPLL_OC
+12VS_VCCSTG_VCCPLL_OC
Imax = 0.02A
+VCCSTG
+12VS_VCCSTG_VCCPLL_OC
Coffeelake-H
PW_LOAD SWITCH
Bosnon

PR6R901	ADP=135W	ADP=120W	ADP=100W	ADP=135W
	76K	76K	76K	76K
	76K/0.5%/0603/1W	76K/0.5%/0603/1W	76K/0.5%/0603/1W	76K/0.5%/0603/1W

PR6R903	ADP=135W	ADP=120W	ADP=100W	ADP=230W	ADP=240W	ADP=330W
	215K	215K	X	X	X	787K
	215K/0.5%/0603/1W	215K/0.5%/0603/1W	X	X	X	787K/0.5%/0603/1W

AD : 17.9V

AC_BAT_SYS

BAT

盛理高頻音用

TL Limit : Charge 4A
DisCharge 24A

HW_Throttle

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

Plug HW Throttle(Out)

Plug HW Throttle(In)

AD : 17.5V

PCIP window

Adaptor select
total power = 90% ADP

Adaptor select

	H Narrow	V Narrow
	15w	9w
PR6R936		
14K	0.6V	30W
31.6K	0.9V	42W
54K	1.2V	65W
93.1K	1.6V	82W
150K	2.0V	75W
272K	2.4V	90W
562K	2.8V	120W

Address Selection Table

Address	A6	A5	A4	A3	A2	A1	A0	Label
0x90	1	0	0	1	0	0	0	ADDR0
0x92	1	0	0	1	0	0	1	ADDR1

Register Address

Register	Bit	Name	Default	Type	Label
0x00	[7:0]	Chip ID	0x00	R	CHIP_ID
0x01	[7:0]	Chip Revision	0x00	R	CHIP_REV
0x02	[7:0]	Vendor ID	0x00	R	VENDOR_ID

PROTECTION

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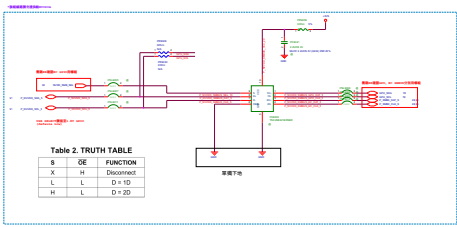
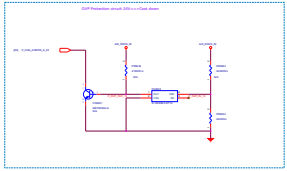
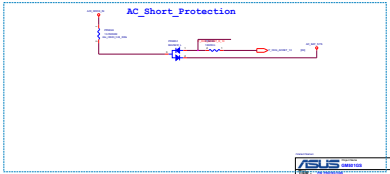
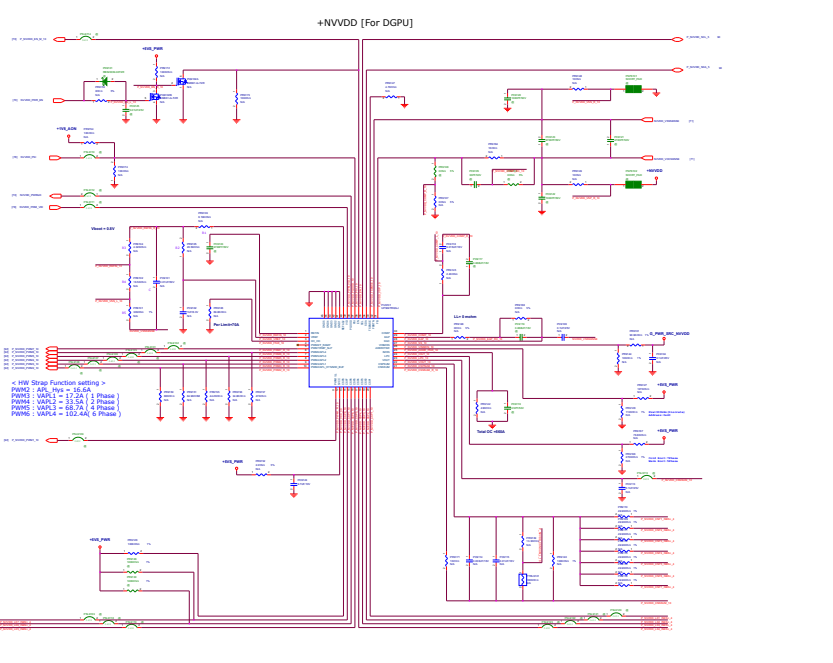
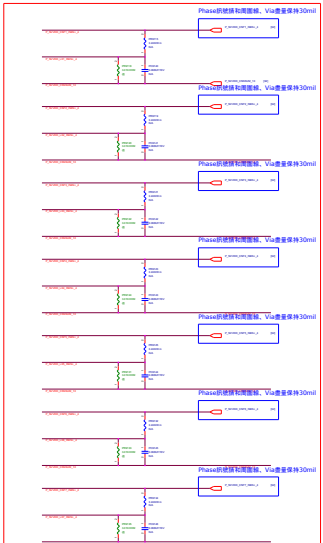






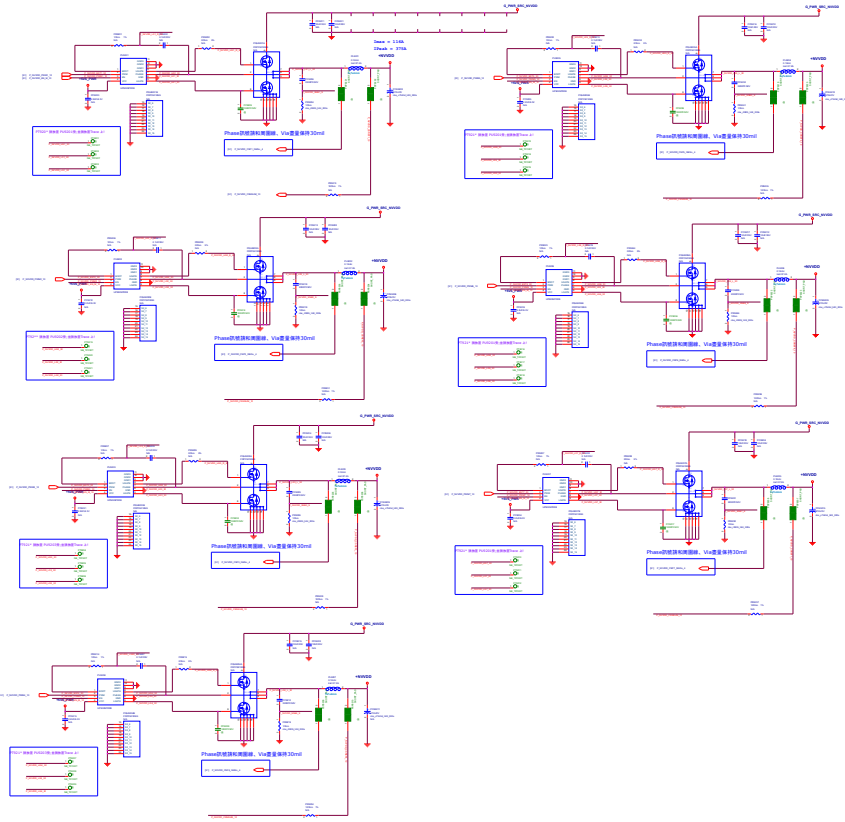


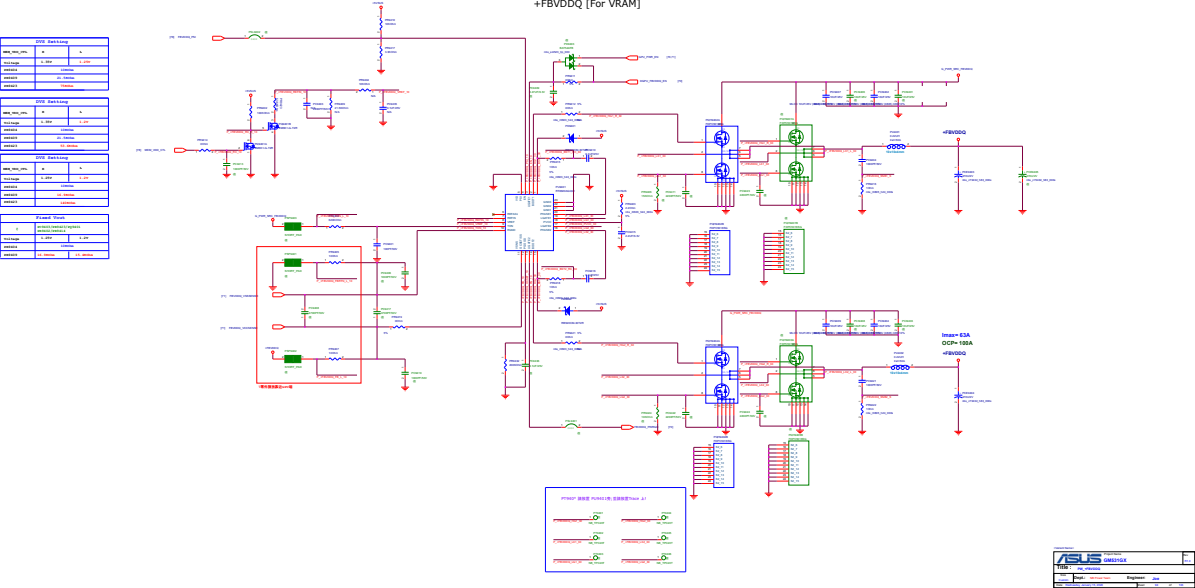
請放靠近PU9101



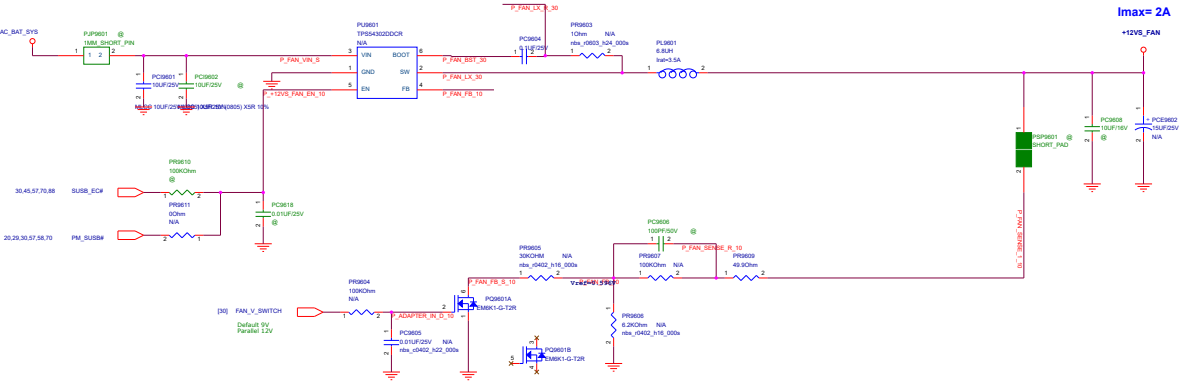
ASUS	Project Name: G710GW		Rev
Title:	Size: A3	Date:	Sheet of
File:	Drawn:	Check:	Engineer:

+NVVDD [For DGPU]




+FBVDDQ [For VRAM]
DYD Switching
MEM_VDD_SEL
H
L
Vid toggle
0.95V
1.25V
0905h10
0905h11
0905h07
1.35Volts
DYD Switching
MEM_VDD_SEL
H
L
Vid toggle
0.95V
1.25V
0905h10
0905h11
0905h03
1.5Volts
DYD Switching
MEM_VDD_SEL
H
L
Vid toggle
0.95V
1.25V
0905h10
0905h11
0905h02
1.8Volts
Vramf Dcap
0
0x10(1),0x04(2),0x20(3),0x08(4),0x01(5)
Vid toggle
0.95V
1.25V
0905h10
0905h11
0905h00
1.0 Volts
1.5 Volts
+FBVDDQ
Imax= 63A
OCP= 100A
+FBVDDQ

+12VS_FAN [For FAN]



<Variant Name>

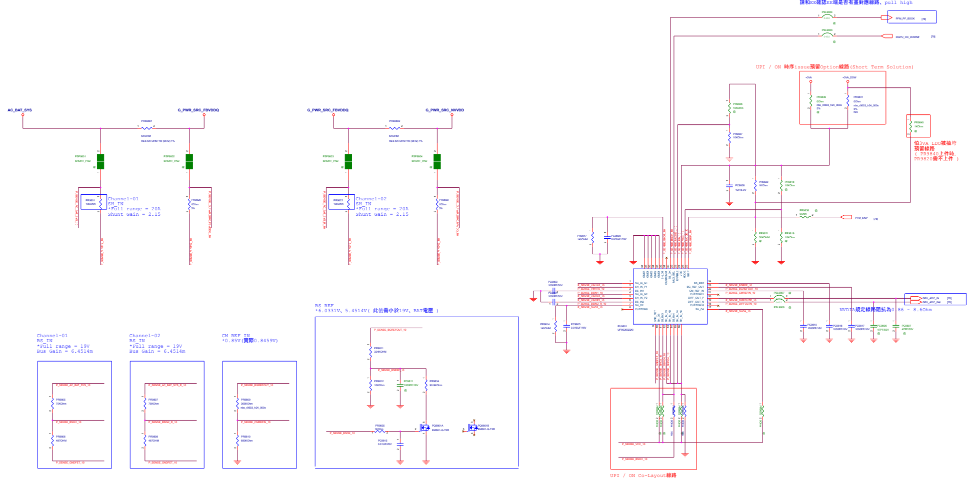
ASUS	Project Name: Coffeelake-H	Rev: R1.0
Title : PW_+12VS_FAN		
Size: B	Dept.: NB Power team	Engineer: Hon
Date: Wednesday, January 15, 2020	Sheet: 96 of 103	

	Project Name GX531GM	Rev R1.0

Title : Type C LDO 3V3

Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Joe

Date: Wednesday, January 15, 2020	Sheet	97	of	103



N18E

N18E-G3/N18E-G3R

	UP9026PQKI(UPI)	
PR9801	100Ω(10G212100014010)	
PR9817	124Ω (10G212124014010)	
PR9822	100Ω(10G212100014010)	
PR9814	124Ω (10G212124014010)	
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

N18E-G2/N18E-G2R
N18E-G1R

	UP9026PQKI(UPI)	
PR9817	140Ω (10G212140014010)	
PR9814	140Ω (10G212140014010)	

N18E-G0
N18E-G1
N18E-G3R MAX-Q
N18E-G2R MAX-Q
N18E-G1R MAX-Q

	UP9026PQKI(UPI)	
PR9817	210Ω (10G212210014010)	
PR9822		
PR9814	210Ω (10G212210014010)	

N18E-G0 MAX-Q

	UP9026PQKI(UPI)	
PR9817	348Ω (10G212348014030)	
PR9822		
PR9814	348Ω (10G212348014030)	

N18P

N18P-G0-MP
N18P-G0-MP MAX-Q
N18P-G0-Q13 MAX-Q
N18P-G62
N18P-G62 MAX-Q
N18P-G61
N18P-G61 MAX-Q

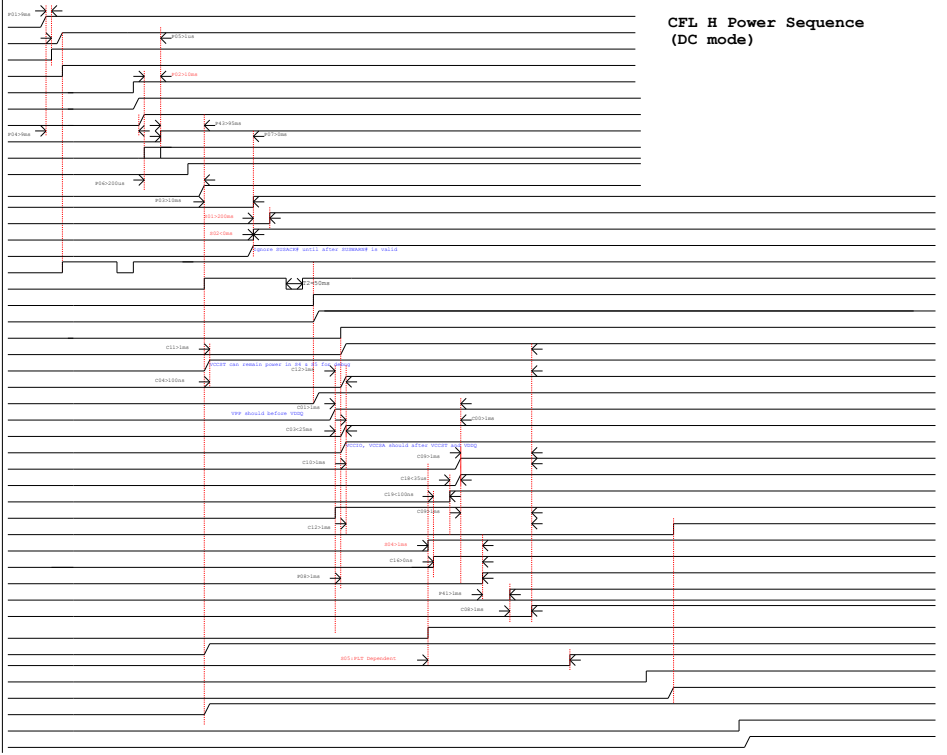
	UP9026PQKI(UPI)	
PR9801	100Ω(10G212100014010)	
PR9817	348Ω (10G212348014030)	
PR9822	100Ω(10G212100014010)	
PR9814	348Ω (10G212348014030)	
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
B:PLT
Power Signal

(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCRST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DSWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST,VCCPLL(VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)
(ALL_SYSTEM_PWRGD)P_IMVP8_EN_10(Power)
(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)
+VCCGT



ASUS	Project Name: G711GW		Rev: 0.5
Title: Power On Timing-DC mode			
Size: Custom	Dept.: MB/PM COMPUTER	Engineer: Gaming RD	
Date: Wednesday, January 16, 2019	Sheet:	of:	

EE PART

G731GX SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R2.0	GX501VSK SKU1	/I7-7700HQ	/230W	8G_Hynix	V8G_Samsung			
60NB0H10-MB2000	R2.0	GX501VSK SKU2	/I5-7300HQ	/230W	8G_Hynix	V8G_Samsung			

1. CPU: INT I7-7700HQ 2.8G/6M SR32Q BGA 01001-01380600
CPU: INT I5-7300HQ 2.5G/6M SR32S BGA 01001-01380500

2. dGPU: nVidia N17E-G2-A1 FCBGA2152 02004-00480500

3.VRAM
GDDR5 256M*32 8.0 1.5V FBGA170, SAMSUNG

4. EC: ITE IT8995VG-128/DX --06037-00050800

5.onboard menory
8G_ Hynix 03012-00030400

<Variant Name>

ASUSTeK COMPUTER

Title : UX302_SKU Table_R1.0

Engineer: Gaming RD

Size	Project Name	Rev
C	G711GW	R2.0

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9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)