Project Name : C14CU

Platform : Ivy Bridge(PROCESSOR)+Panther Poinrt(PCH)

PAGE CONTENT

M/B Schematic Version Change List

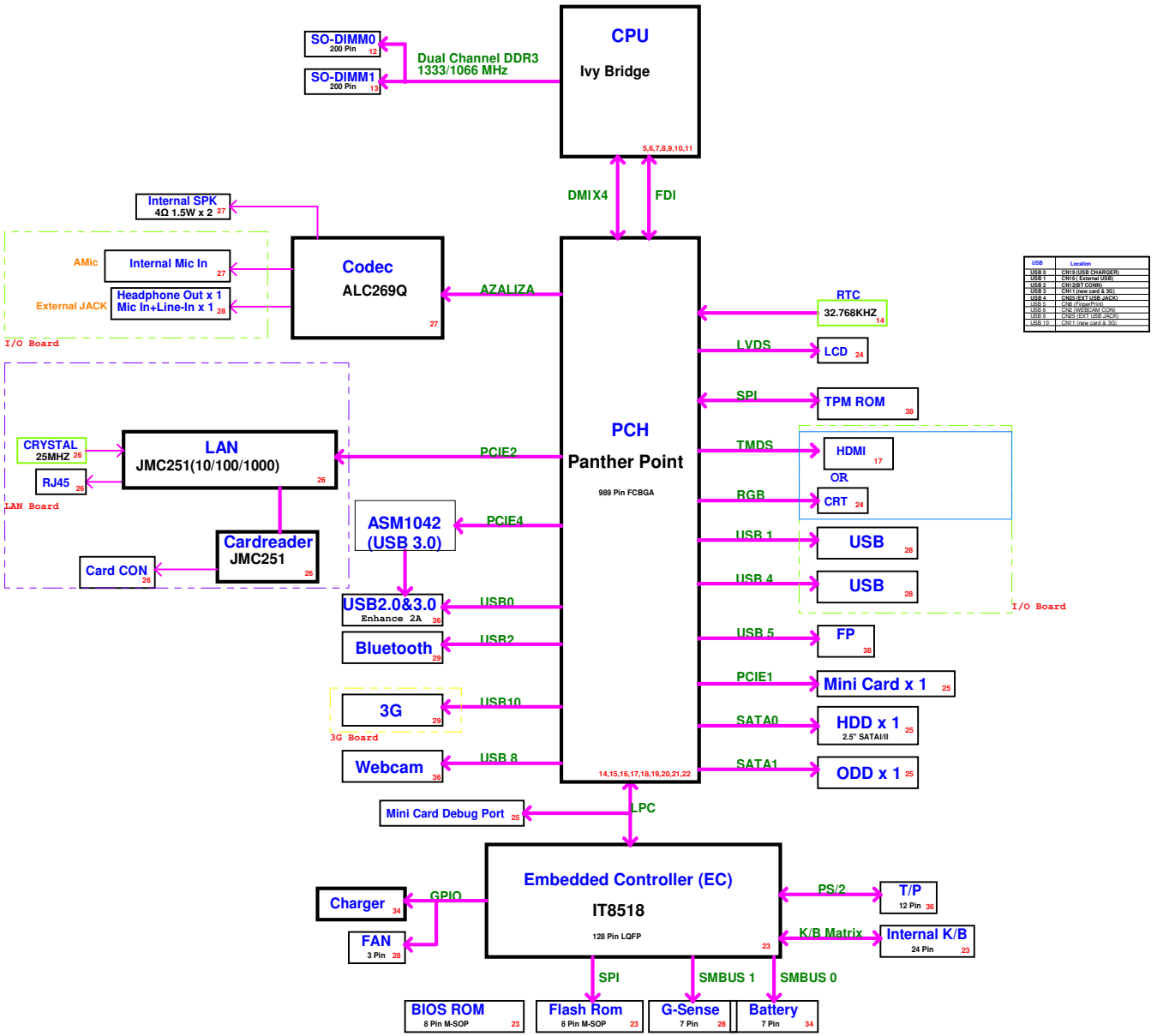
Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note
2012/05/21	A	71R-C14CU6-SU0A			
2012/06/11	B				

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: INDEX		Rev: 1.0
Date: Wednesday, July 18, 2012	Sheet 1 of 41		

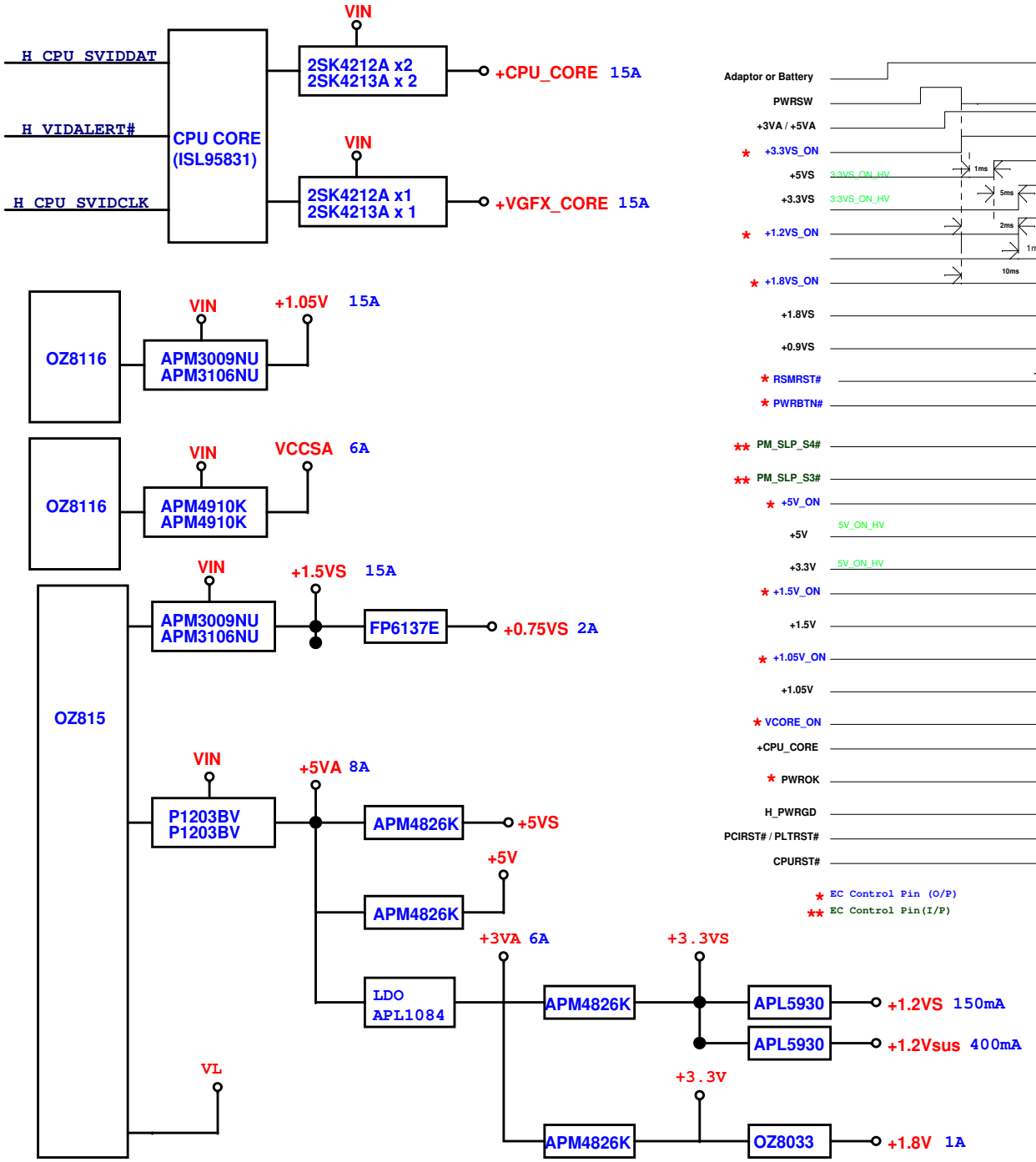
SYSTEM BLOCK DIAGRAM



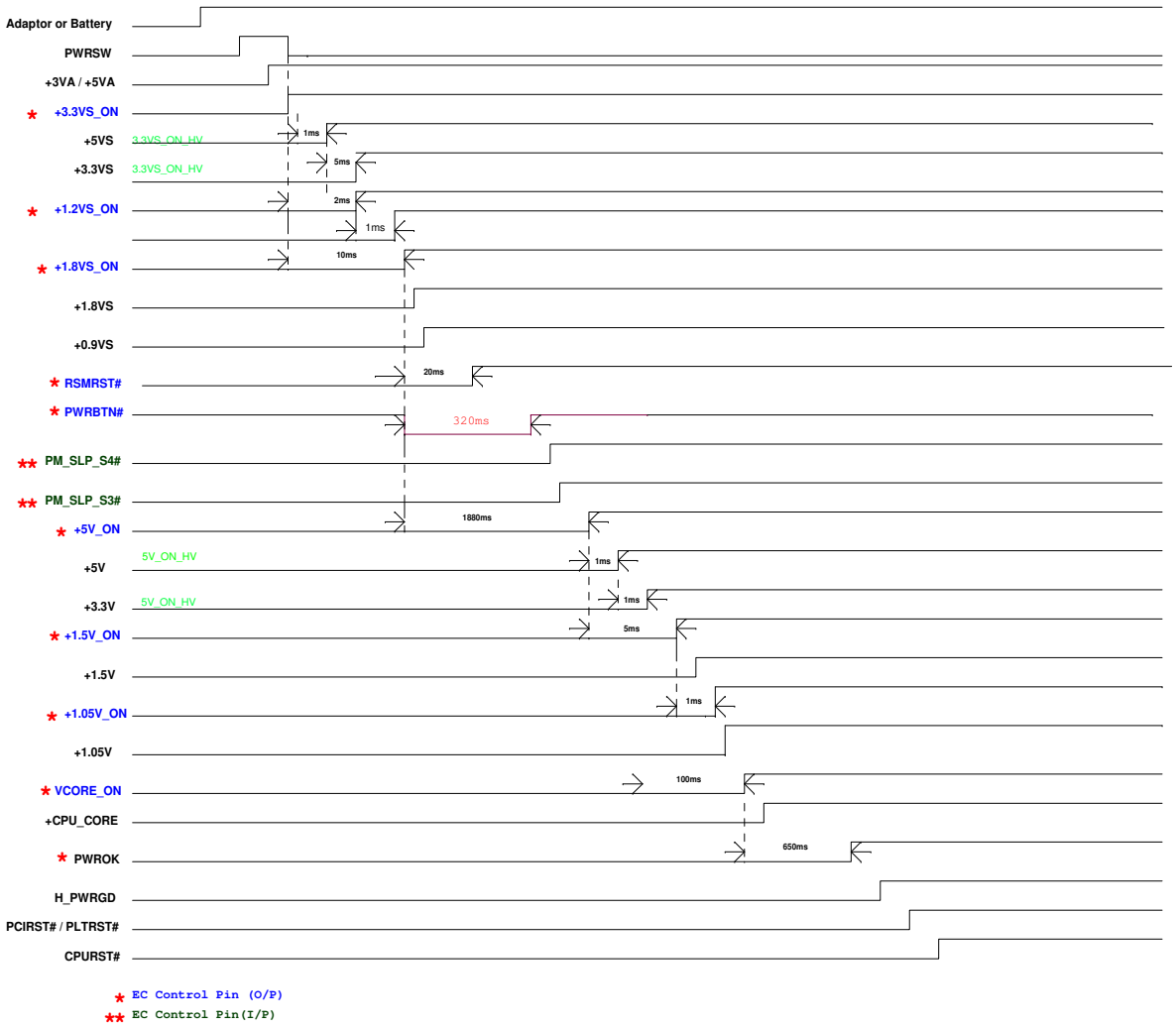
USB	Location
USB 0	CN19 (USB CHARGER)
USB 1	CN16 (External USB)
USB 2	CN12(BT CONN)
USB 3	CN11 (new card & 3G)
USB 4	CN26 (EXT USB JACK)
USB 5	CN8 (Finger Print)
USB 6	CN2 (WEB CAM CON)
USB 9	CN25 (EXT USB JACK)
USB 10	CN11 (new card & 3G)

Shuttle Inc.		
File: C14CU		
Size: Custom	Document Number: SYSTEM BLOCK	Rev: 1.0
Date: Wednesday, July 18, 2012	Sheet 2 of 41	

POWER BLOCK DIAGRAM



System Poewr On Sequence



* EC Control Pin (O/P)
** EC Control Pin(I/P)

Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: POWER DIAGRAM & SEQUENCE	Rev: 1.0
Date: Wednesday, July 18, 2012	Sheet 3 of 41	

Panther Point GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	N.C(TACH3)
GPIO8	N.C
GPIO9	N.C(WOL_EN)
GPIO10	N.C(ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	N.C(GLAN_DOCK#)
GPIO14	N.C(NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	N.C(TACH0)
GPIO18	N.C
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	N.C(SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	N.C(HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8518 GPIO		Default Pull/Mode
GPA0	PID_3_RF_LED_ON#	UP / GPI
GPA1	BATT_VA_OFF#	UP / GPI
GPA2	BTL_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	+1.05V_ON	UP / GPI
GPA5	SENBAT_V	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	3G_PWR#	Dn / GPI
GPB3	SMBCLK	/ GPI
GPB4	SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Func1
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	PID_0_CHG_B_LED	Dn / GPI
GPC4	PWRBTN3#	Dn / GPI
GPC5	PANEL_DETECT 2	Dn / GPI
GPC6	VCCSA_ON	Dn / GPI
GPC7	+1.5VS_ON	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Func1
GPD3	PM_SUS_STAT#	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	Fastcharge_EN	UP / GPI
GPD6	+5V_ON	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	PWR_USB_LED	Dn / GPI
GPE2	ALL_SYS_PGD	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	PCH_BL_EN	UP / GPI
GPF1	+1.8V_ON	UP / GPI
GPF2	BT_ON	UP / GPI
GPF3	N.C	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_PECI	UP / GPI
GPF7	CHG_HI_VOLT#	UP / GPI
GPG0	PWRBTN2#	Dn/GPO/TM
GPG1	+3.3VS_ON	Dn/GPO/ID7
GPG2	EC_PORST	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PID_1_CHG_R_LED	Dn/GPI/ID1
GPH2	PID_2_PWR_LED	Dn/GPI/ID2
GPH3	EC_HSCS0#	Dn/GPI/ID3
GPH4	EC_HSCK	Dn/GPI/ID4
GPH5	EC_HMISO	Dn/GPI/ID5
GPH6	EC_HMOSI	Dn/GPI/ID6

ITE8518 GPIO		Default Pull/Mode
GPI0	CRT_DETECT	/GPI/ADC
GPI1	PANEL_DETECT	/GPI/ADC
GPI2	PLATFORM_ID	/GPI/ADC
GPI3	CPPE#	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PWR_USB#	/GPI/DAC

Ivy Bridge CPU

	CPU CORE(V)	ICC(A)	W	TEMP(℃)
IMVP-7	1.05	44.0	36	

Panther Point

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

Panther Point

VCC	ICC(mA)	mW	TEMP(℃)
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

ITE8518

VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	100	330	70

IDT92HD87B

VCC	ICC(mA)	mW	TEMP(℃)
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

ADM1032

VCC	ICC	mW	TEMP(℃)
+3.3V	170uA	0.56	150

JMC251

VCC	ICC(mA)	mW	TEMP(℃)
+3.3VS	300	990	70
+1.2VS	150	180	

Shuttle Inc

Title: C14CU

Size: Custom | Document Number: GPIO & Power Consumption | Rev: 1.0

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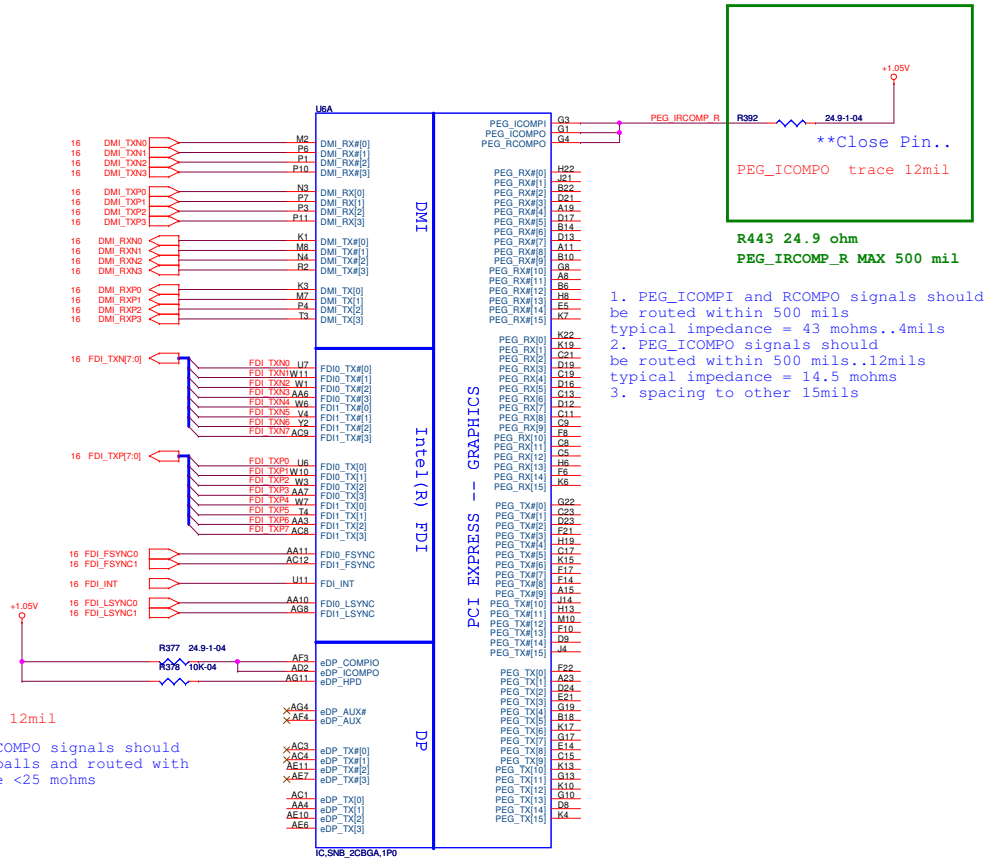
SANDYBRIDGE PROCESSOR(DMI,PEG,FDI)



R443 24.9 ohm

PEG_IRCOMP_R MAX 500 mil

1. PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms..4mils
2. PEG_ICOMPO signals should be routed within 500 mils..12mils typical impedance = 14.5 mohms
3. spacing to other 15mils

DP_ICOMPO trace 12mil

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

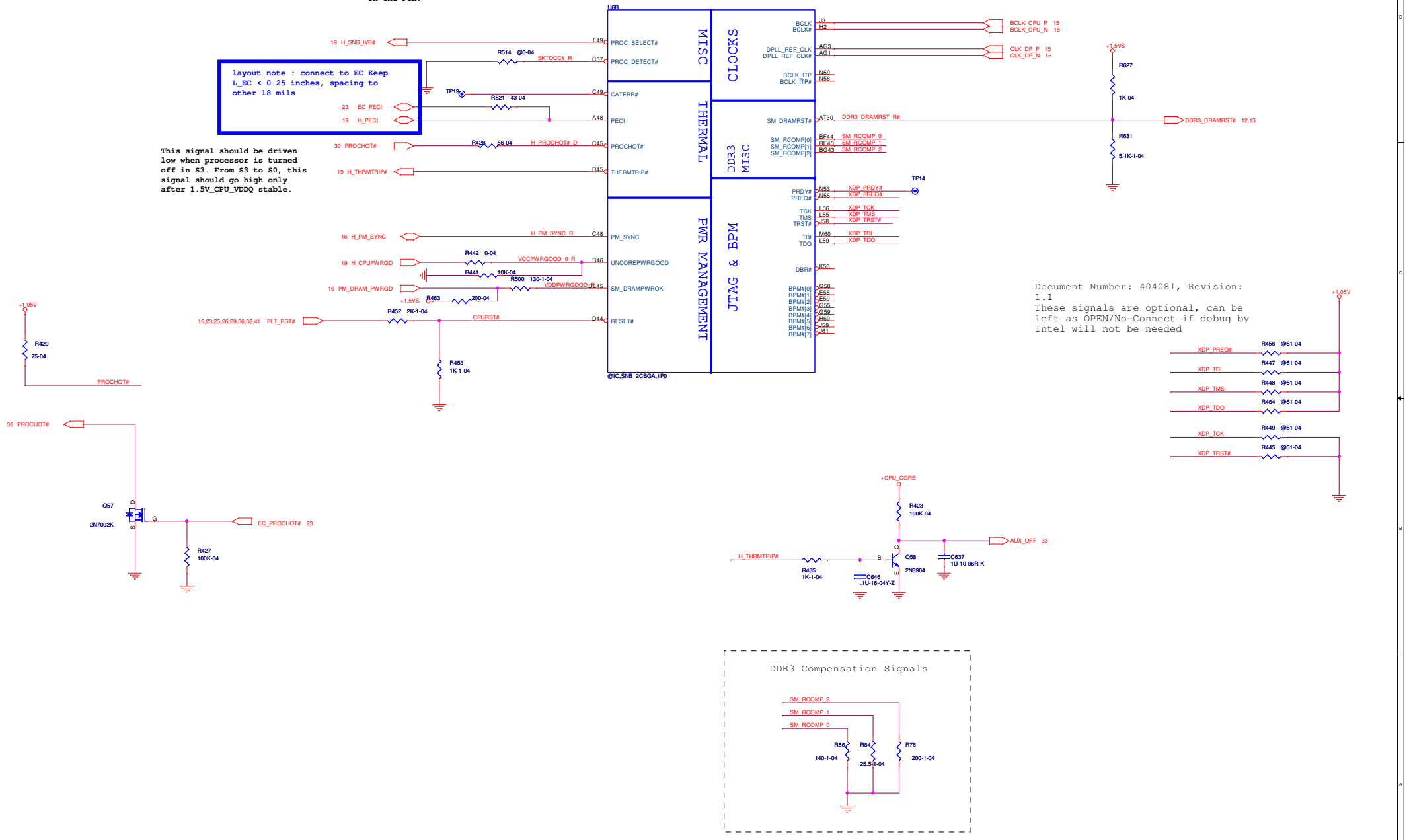
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: CPU_DMI/PEG/FDI (1 of 7)	Rev: 1.0
Date: Wednesday, July 18, 2012	Sheet 5 of 41	

SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)

This pin is for compability with future platforms. A pull up resistor to VCPLL is required if connected to the DF_TVS strap on the PCH.

layout note : connect to EC Keep L_EC < 0.25 inches, spacing to other 18 mils

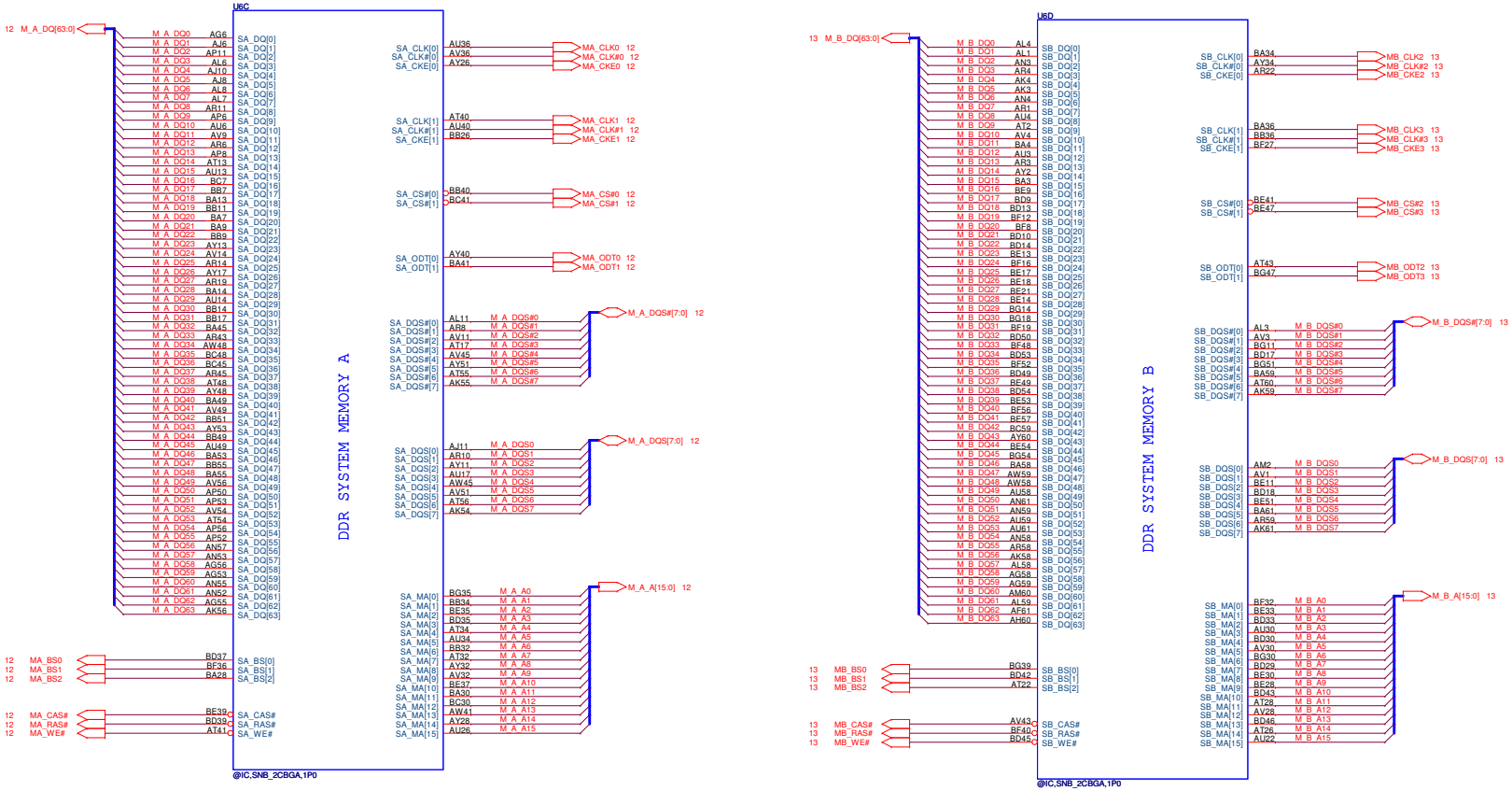
This signal should be driven low when processor is turned off in S3. From S3 to S0, this signal should go high only after 1.5V_CPU_VDDQ stable.



Document Number: 404081, Revision: 1.1
These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed

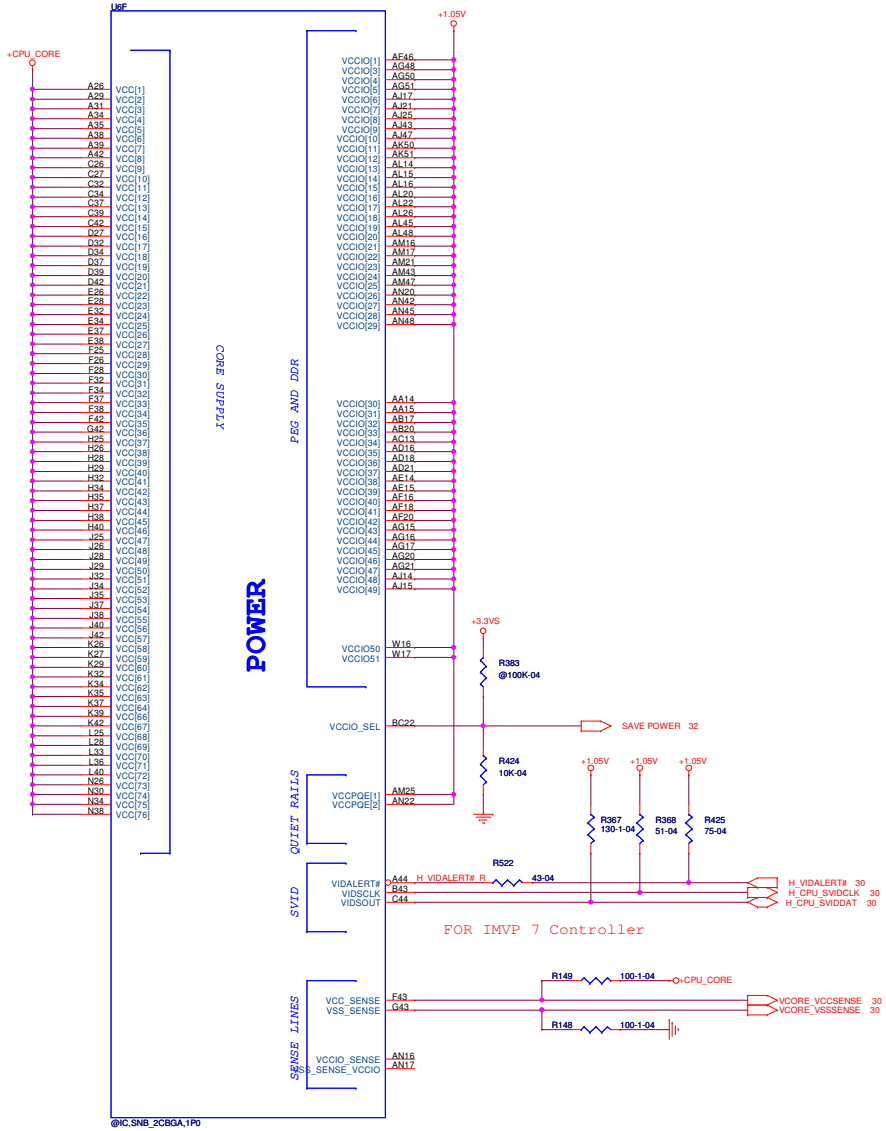
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: CPU_CLK/MISC/JTAG (2 of 7)	Rev: B
Date: Monday, June 11, 2012	Sheet 6 of 41	

SANDYBRIDGE PROCESSOR (DDR3)

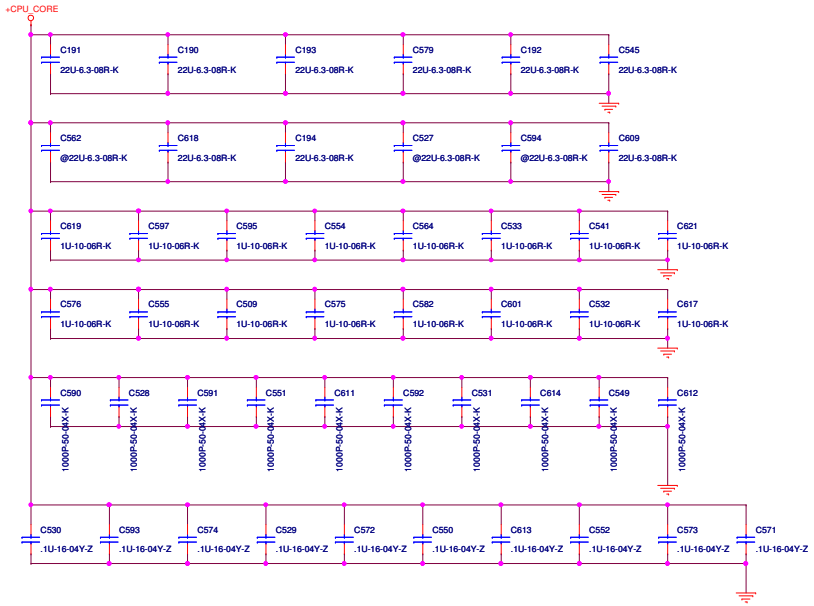


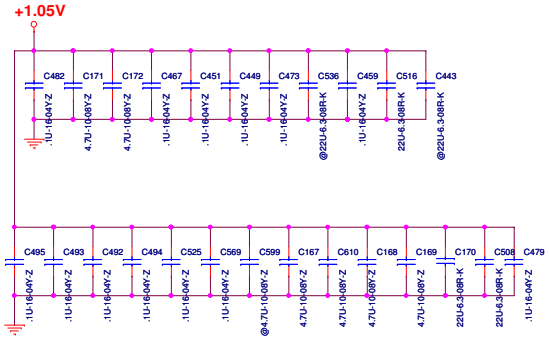
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: CPU_DDR3 BUS (3 of 7)	Rev: B
Date: Monday, June 11, 2012	Sheet 7 of 41	

IVY BRIDGE PROCESSOR (POWER)



+CPU_Core Decoupling





Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: CPU_PWR (4 of 7)	Rev: B
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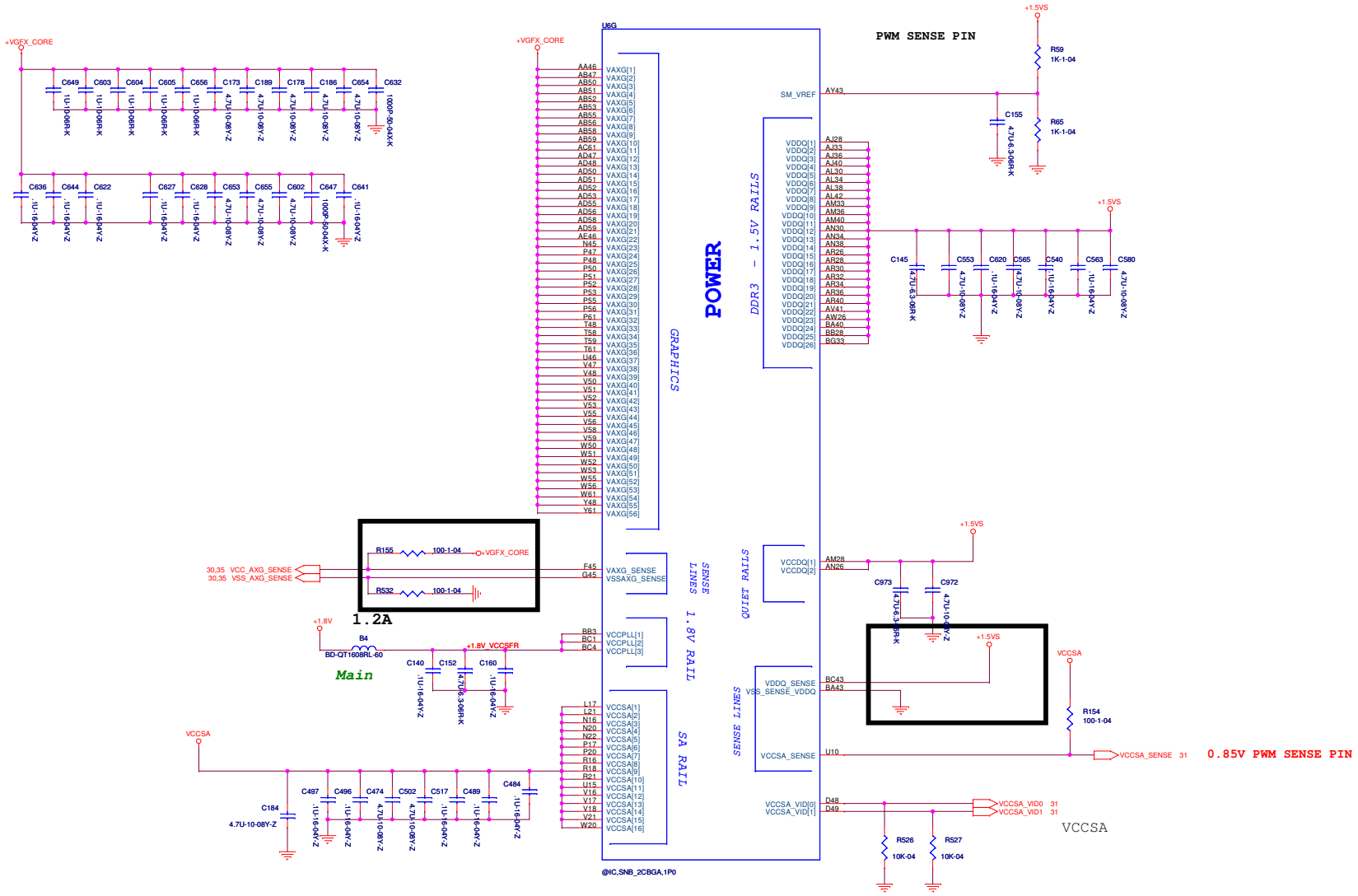
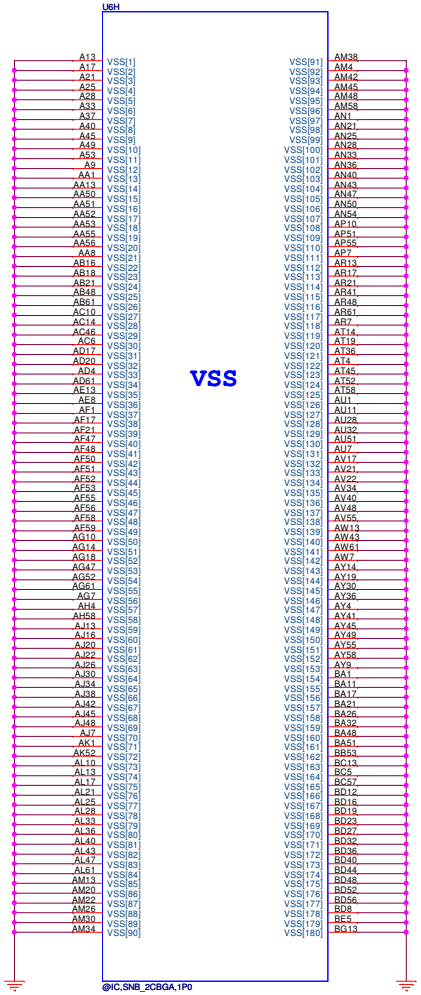
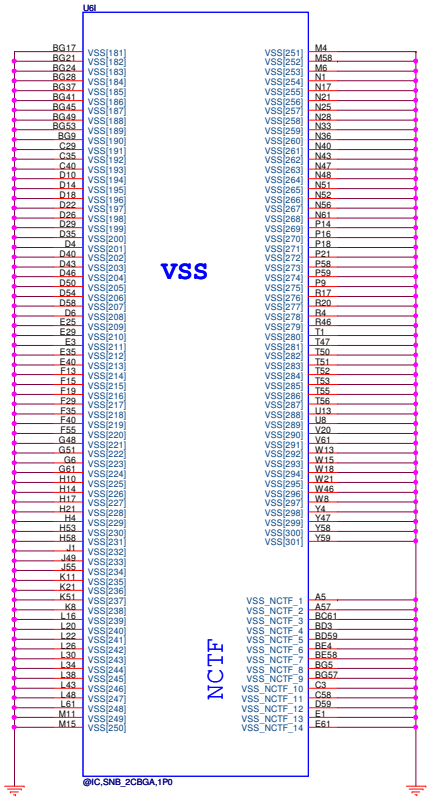
IVY BRIDGE PROCESSOR (POWER)



Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: CPU_GRAPHICS POWER (5 of 7)		Rev: B
Date: Monday, June 11, 2012		Sheet 9 of 41	

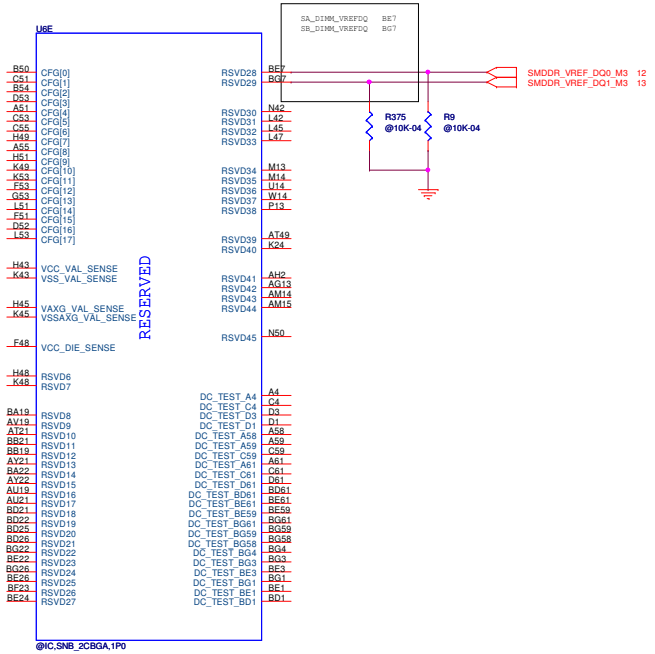
IVY BRIDGE PROCESSOR (VSS)



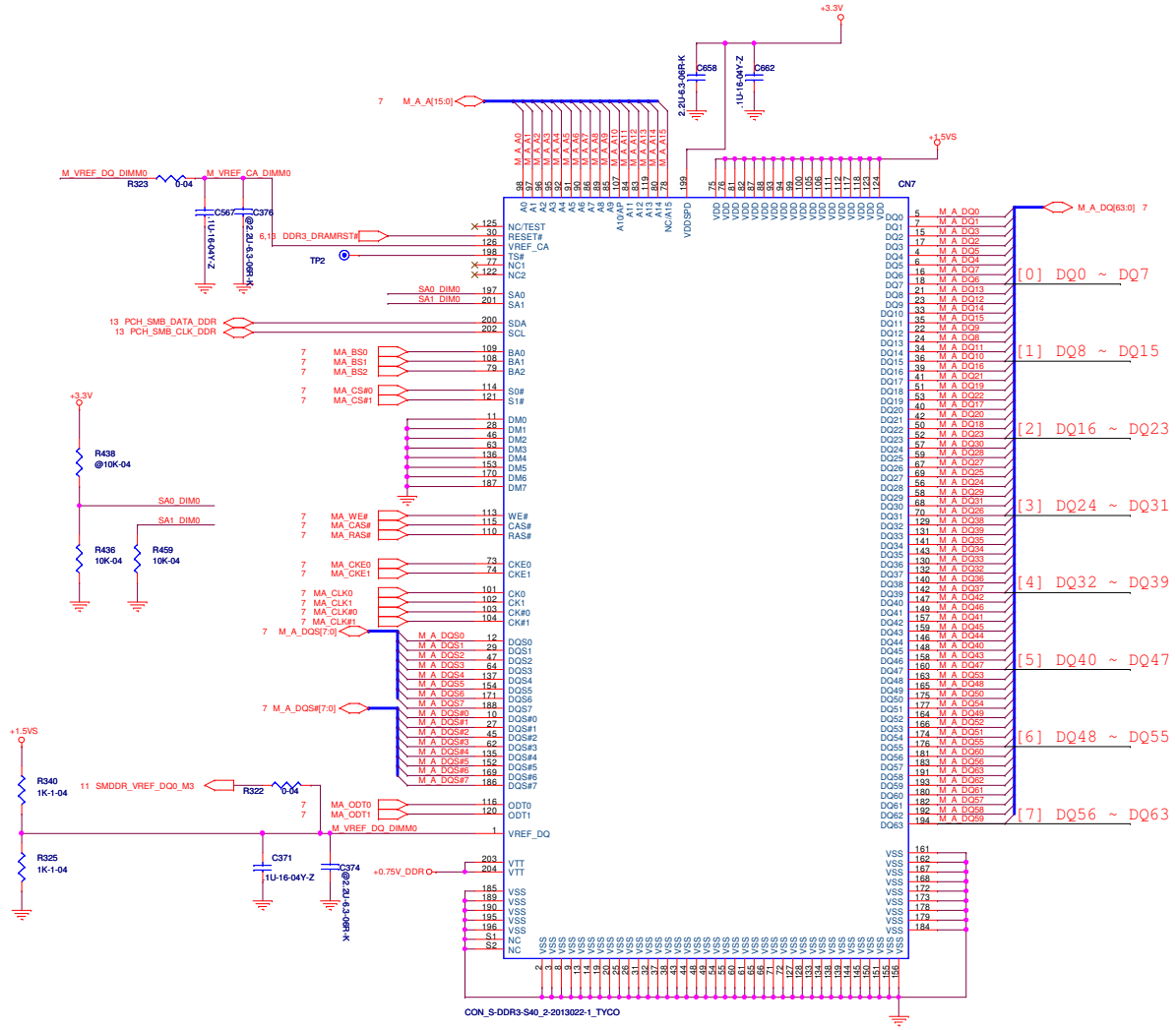


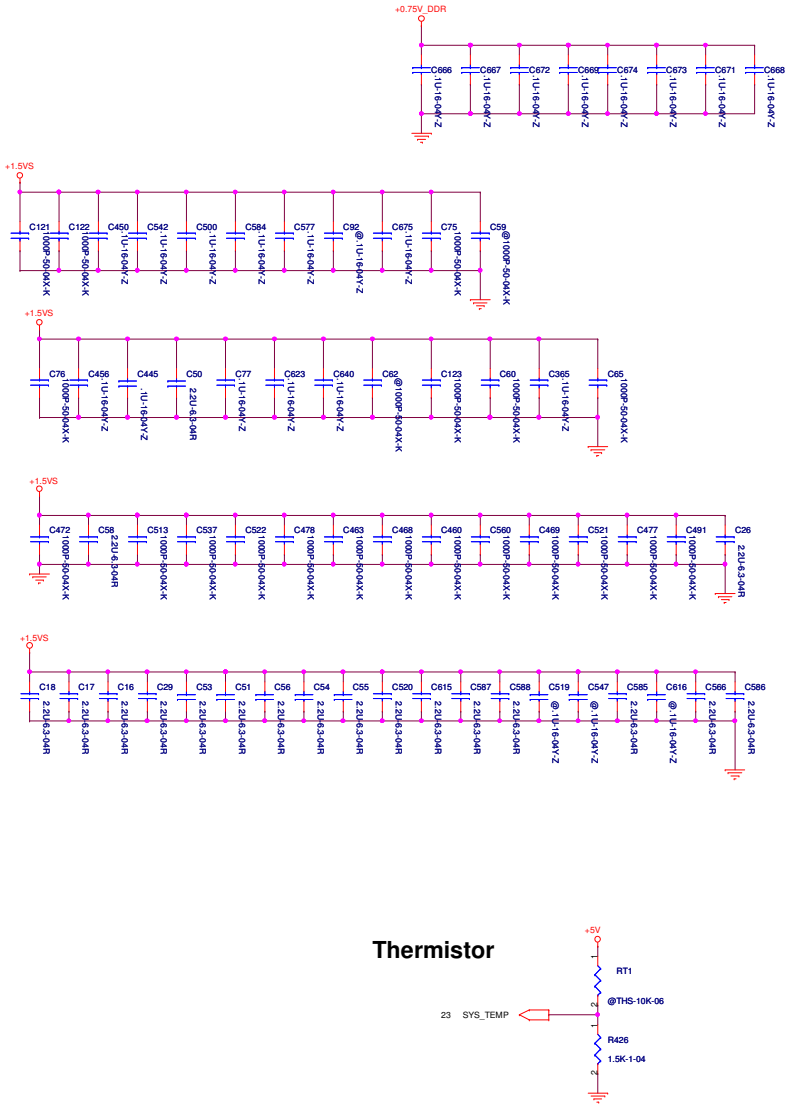
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: CPU_GND (6 of 7)	Rev: B
Date: Monday, June 11, 2012	Sheet 10 of 41	

IVY BRIDGE PROCESSOR (RESERVED)



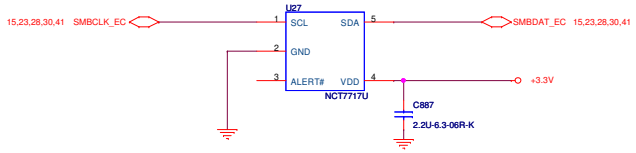
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: CPU_RESERVED (7 of 7)	Rev: B
Date: Monday, June 11, 2012	Sheet 11 of 41	



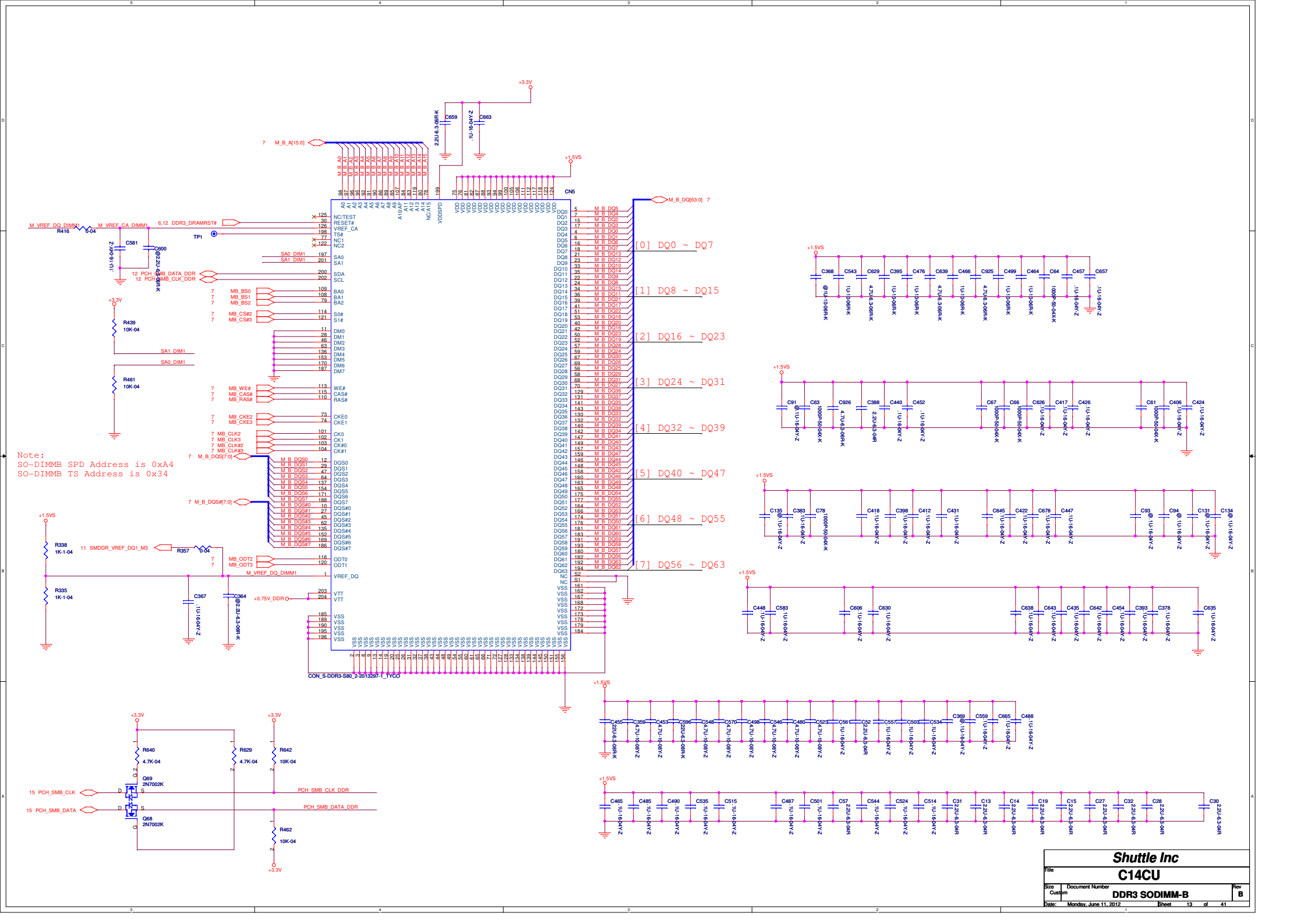


Thermistor

CPU Thermal Sensor

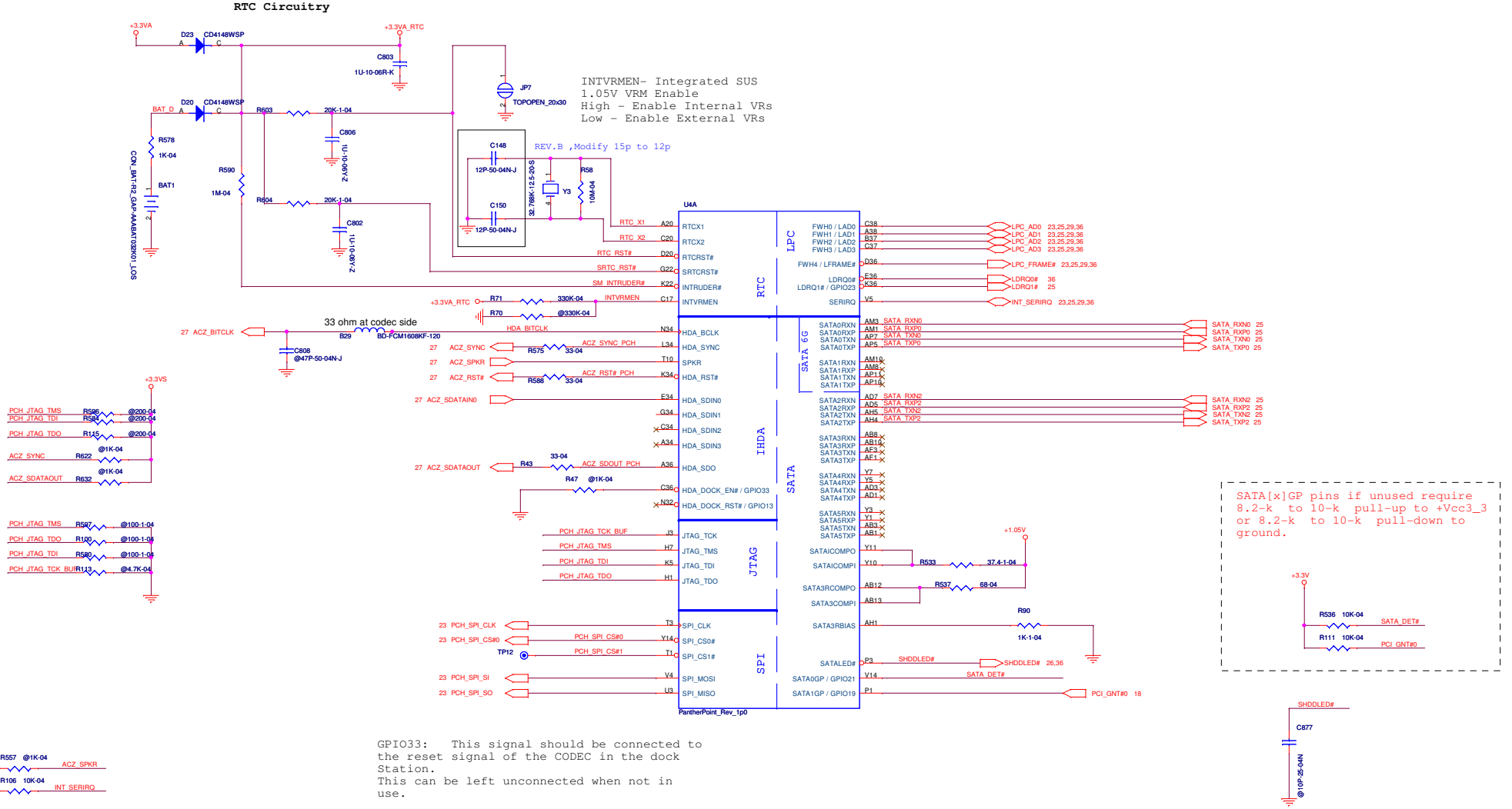


Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: DDR3 SODIMM-A		Rev: B
Date: Monday, June 11, 2012		Sheet 12 of 41	



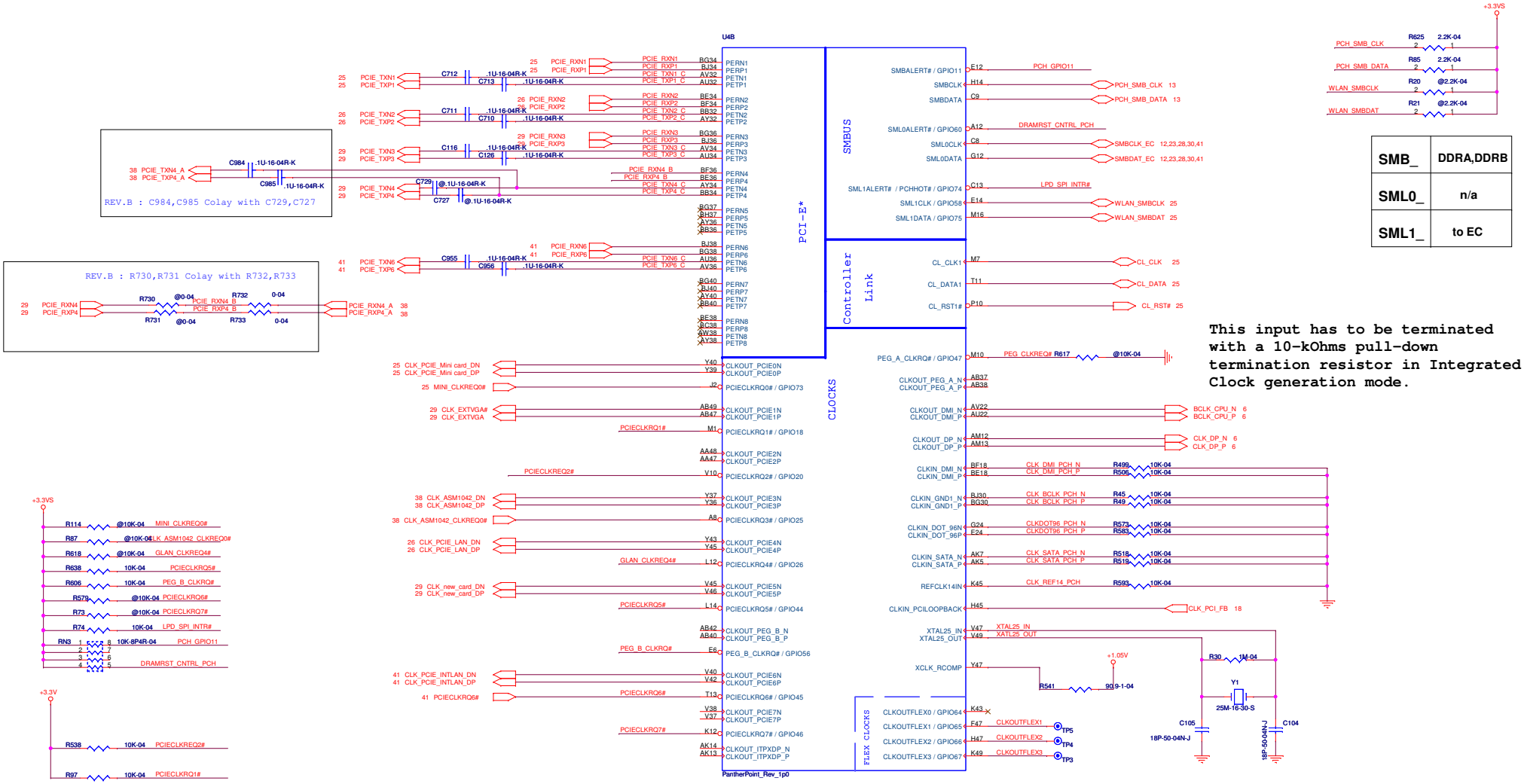
Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: DDR3 SODIMM-B		Rev: B
Date: Monday, June 11, 2012	Sheet 13 of 41		

Panther Point Chipset (RTC,LPC,SATA,HDA,SPI,JTAG)



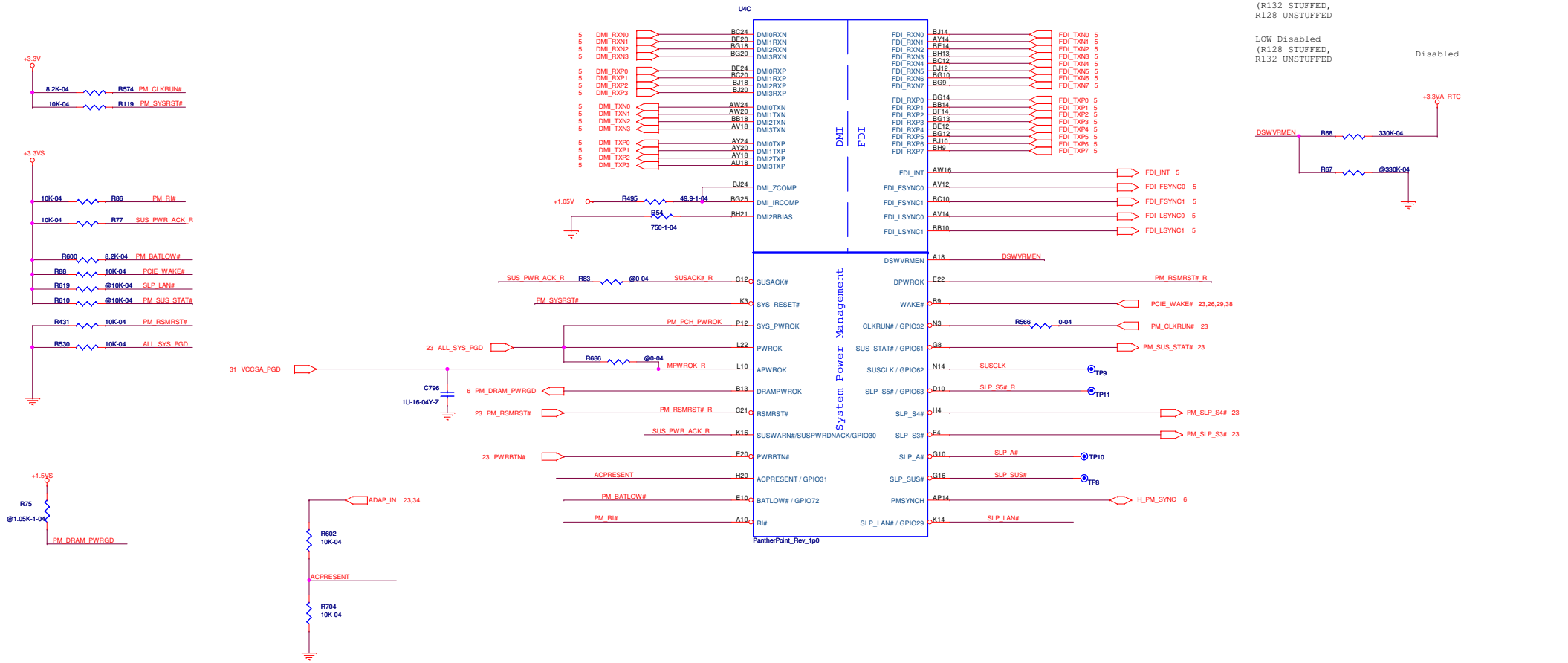
Shuttle Inc	
Title	C14CU
Size: Custom	Document Number: PCH_HDA/JTAG/SATA (1 of 9)
Rev: B	
Date: Monday, June 11, 2012	Sheet 14 of 41

Panther Point Chipset (PCIE,SMBUS,CLOCK)



Shuttle Inc	
Title: C14CU	
Size: Custom	Document Number: PCH_PCIE/CLK/SMBUS (2 of 9)
Rev: B	
Date: Tuesday, June 12, 2012	Sheet 15 of 41

Panther Point Chipset (DMI,FDI)

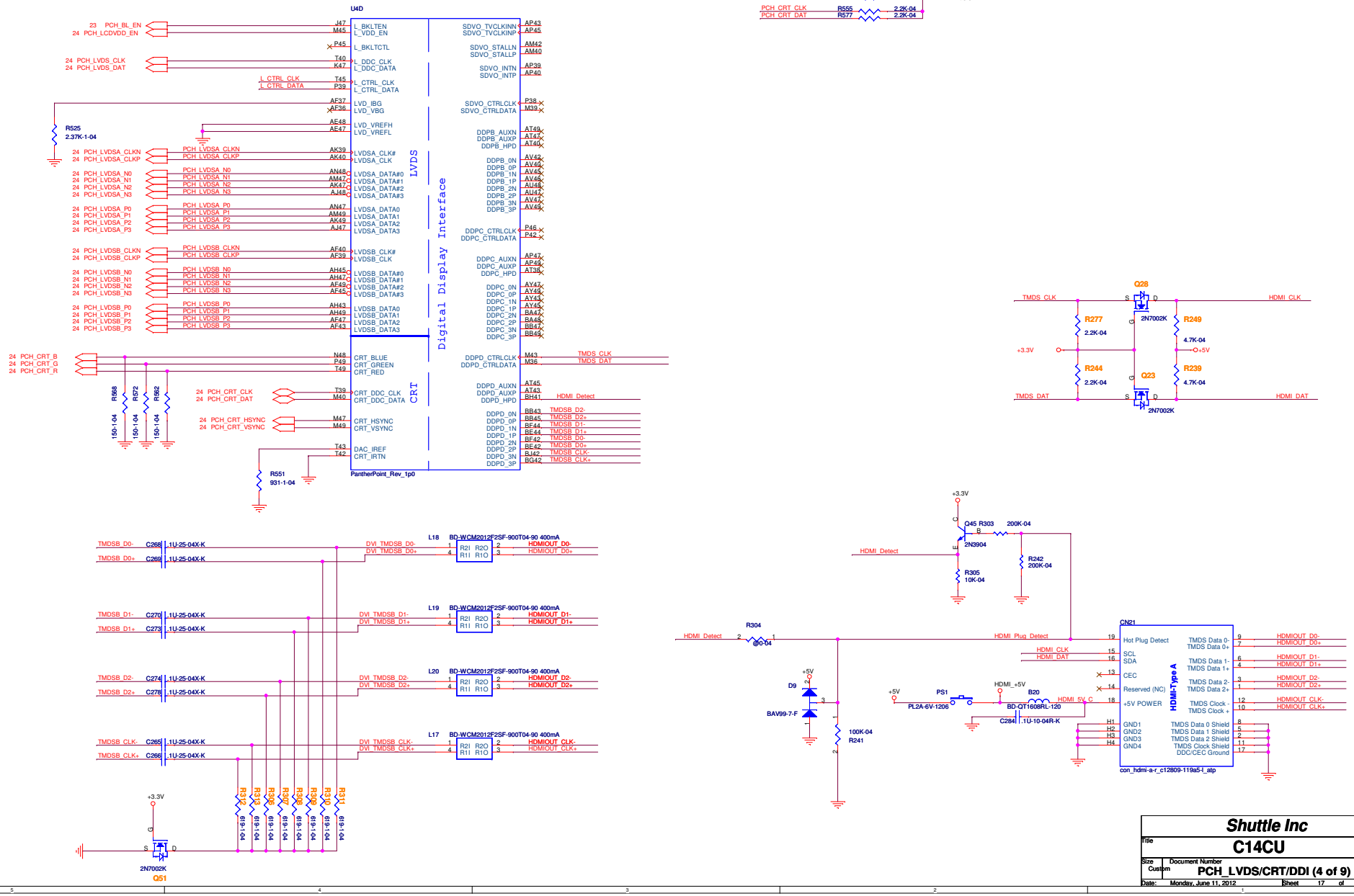


DSWODVREN – On Die DSW VR Enable

HIGH Enabled (DEFAULT) (R132 STUFFED, R128 UNSTUFFED	Enabled (DEFAULT)
LOW Disabled (R128 STUFFED, R132 UNSTUFFED	Disabled

Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: PCH_DMI/FDI/PM (3 of 9)		Rev: B
Date: Monday, June 11, 2012	Sheet 16 of 41		

Panther Point Chipset (LVDS,CRT,Digital Display)



Title	**C14CU**
Size	Custom
Document Number	PCH_LVDS/CRT/DDI (4 of 9)
Rev	B
Date:	Monday, June 11, 2012
Sheet	17 of 41

Shuttle Inc

Default : SPI

No need Pull Hi, checked CRB & Checklist

14 PCI_GNT#0 — PCI_GNT#0 — R117 @1K-04

PCI_GNT#1 — R616 @1K-04

Boot BIOS Strap

PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
1	1	SPI (Default)

+3.3V

RN2 8.2K-8P4R-04
- INT_PIRQA#
- INT_PIRQB#
- INT_PIRQC#
- INT_PIRQD#

RN4 8.2K-8P4R-04
- ASM1042_SMI#
- INT_PIRQF#
- INT_PIRQE#
- INT_PIRQH#

R39 @10K-04 REQ1#

R614 @10K-04 REQ2#

R620 @10K-04 REQ3#

R615 10K-04 PCI_GNT#1

+3.3VS

R611 @8.2K-04 PCI_PME#

R102 0-04

+3.3V

C704 @.1U-10-04V-K

5,23,25,26,29,36,38,41 PLT_RST# — PLT_RST#_R

R657 @100K-04

U5 @74AHC1G08

U4E

RSVD: TP1–TP24, RSVD1–RSVD29

USB3_RX1_N_C — TP25
USB3_RX1_P_C — TP28
USB3_TX1_N_C — TP31
USB3_TX1_P_C — TP34

36,38 USB30_RX_P — R351 @0-04 — USB3_RX1_P_C
36,38 USB30_RX_N — R349 @0-04 — USB3_RX1_N_C

36,38 USB30_TX_P — C929 @.1U-16-04R-K — USB3_TX1_P_C
36,38 USB30_TX_N — C930 @.1U-16-04R-K — USB3_TX1_N_C

PCI: INT_PIRQA#, INT_PIRQB#, INT_PIRQC#, INT_PIRQD#; REQ1#, REQ2#, REQ3#; PCI_GNT#1; INT_PIRQE#, INT_PIRQF#, INT_PIRQH#; PCI_PME#; PLT_RST#_R

38 ASM1042_SMI#

USB: USBP0N/P … USBP13N/P

USB_PN0 R — R166 0-04 — USB_PN0 36,38
USB_PP0 R — R167 0-04 — USB_PP0 36,38

R211 0-04 — USB_PN2 29
R218 0-04 — USB_PP2 29

R209 @0-04 — USB_WN2 25
R210 @0-04 — USB_WP2 25

USB_PN8 36
USB_PP8 36
USB_PN9 28
USB_PP9 28
USB_PN10 28
USB_PP10 28
R316 0-04 — USB_PN11 29
R373 0-04 — USB_PP11 29
USB_PN12 28
USB_PP12 28

R46 22.6-1-04

R201 @0-04 — USB_TN11 28
R206 @0-04 — USB_TP11 28

OC0# / GPIO59 — USB_OC# 0_1
OC1# / GPIO40 — USB_OC# 2_3
OC2# / GPIO41 — USB_OC# 4_5
OC3# / GPIO42 — USB_OC# 6_7
OC4# / GPIO43 — USB_OC# 8_9
OC5# / GPIO9 — USB_OC# 10_11
OC6# / GPIO10 — USB_OC# 12_13
OC7# / GPIO14 — 0C7#/GPIO14

USB	Location
USB 0	CN19 (USB CHARGER)
USB 1	CN25 (20pin External USB BD)
USB 2	CN12 BT CONN
USB 3	CN11 Express card
USB 4	Mini card
USB 5	no use
USB 6	no use
USB 7	no use
USB 8	CN2 (WEBCAM)
USB 9	finger print
USB 10	CN25 (20pin External USB BD)
USB 11	CN11 Express card
USB 12	T/P
USB 13	no use

+3.3VS

RN1 10K-8P4R-04
- USB_OC# 10_11
- USB_OC# 6_7
- 0C7#/GPIO14

RN5 10K-8P4R-04
- USB_OC# 8_9
- USB_OC# 12_13
- USB_OC# 4_5
- USB_OC# 2_3

R624 @10K-04 — USB_OC# 0_1 — R685 10K-04

25 CLK_Debug BD — R38 22-04 — CLK_PCI_SIO_R
15 CLK_PCI_FB — R582 22-04 — CLK_PCI_FB_R
23,29 CLK_EC_LPC — R31 22-04 — CLK_PCI_KBC_R
36 SUPER_IO_CLK — R37 22-04 — CLKOUT_PCI3

CLKOUT_PCI0, CLKOUT_PCI1, CLKOUT_PCI2, CLKOUT_PCI3, CLKOUT_PCI4

C108 @-18P-50V-J

C110 @-18P-50V-J

PantherPoint_Rev_1p0

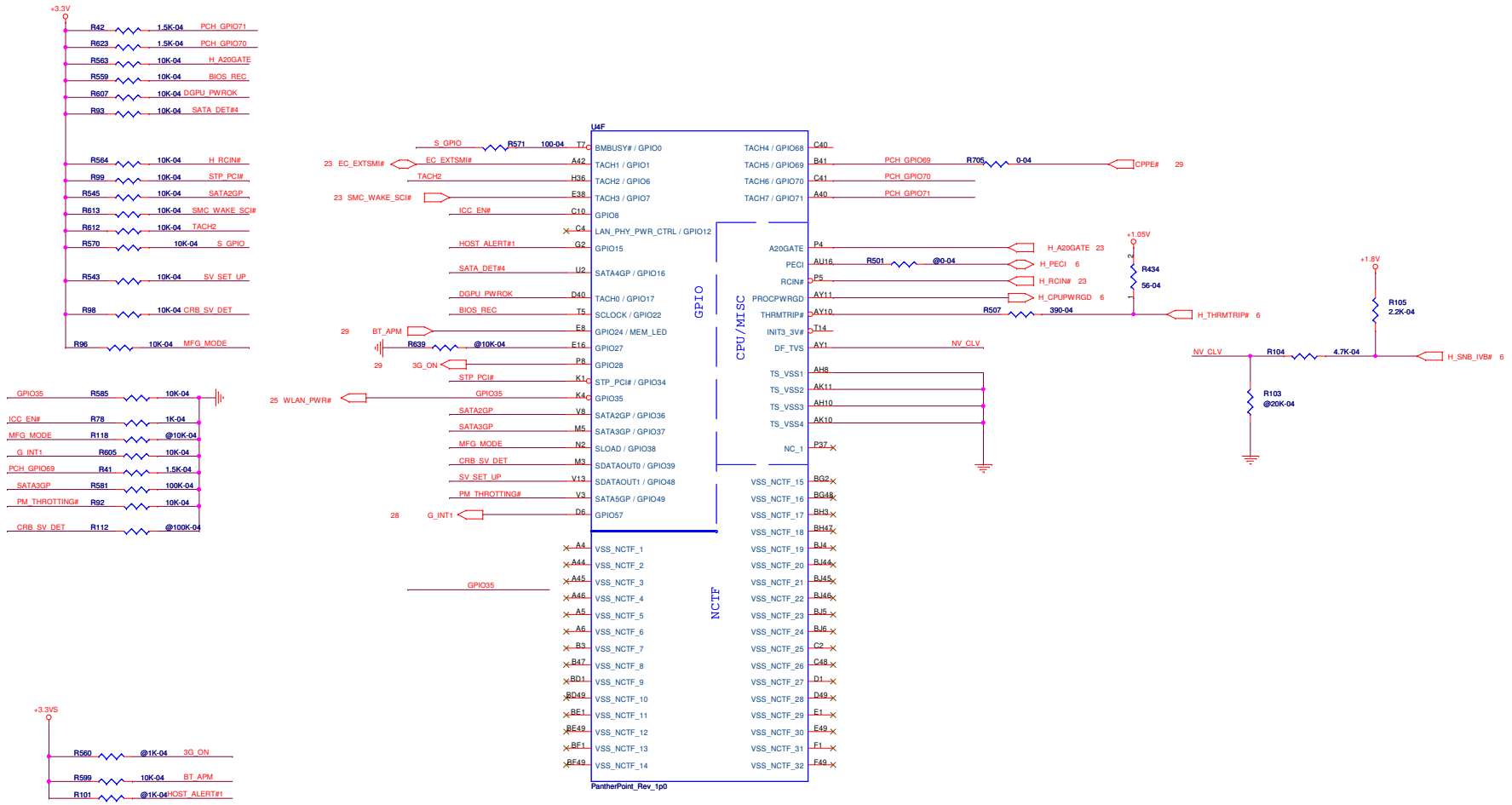
GPIO50,52,54,51,53,55
Desktop: Multiplexed
with REQ2#.
Mobile: Used as GPIO only

Shuttle Inc

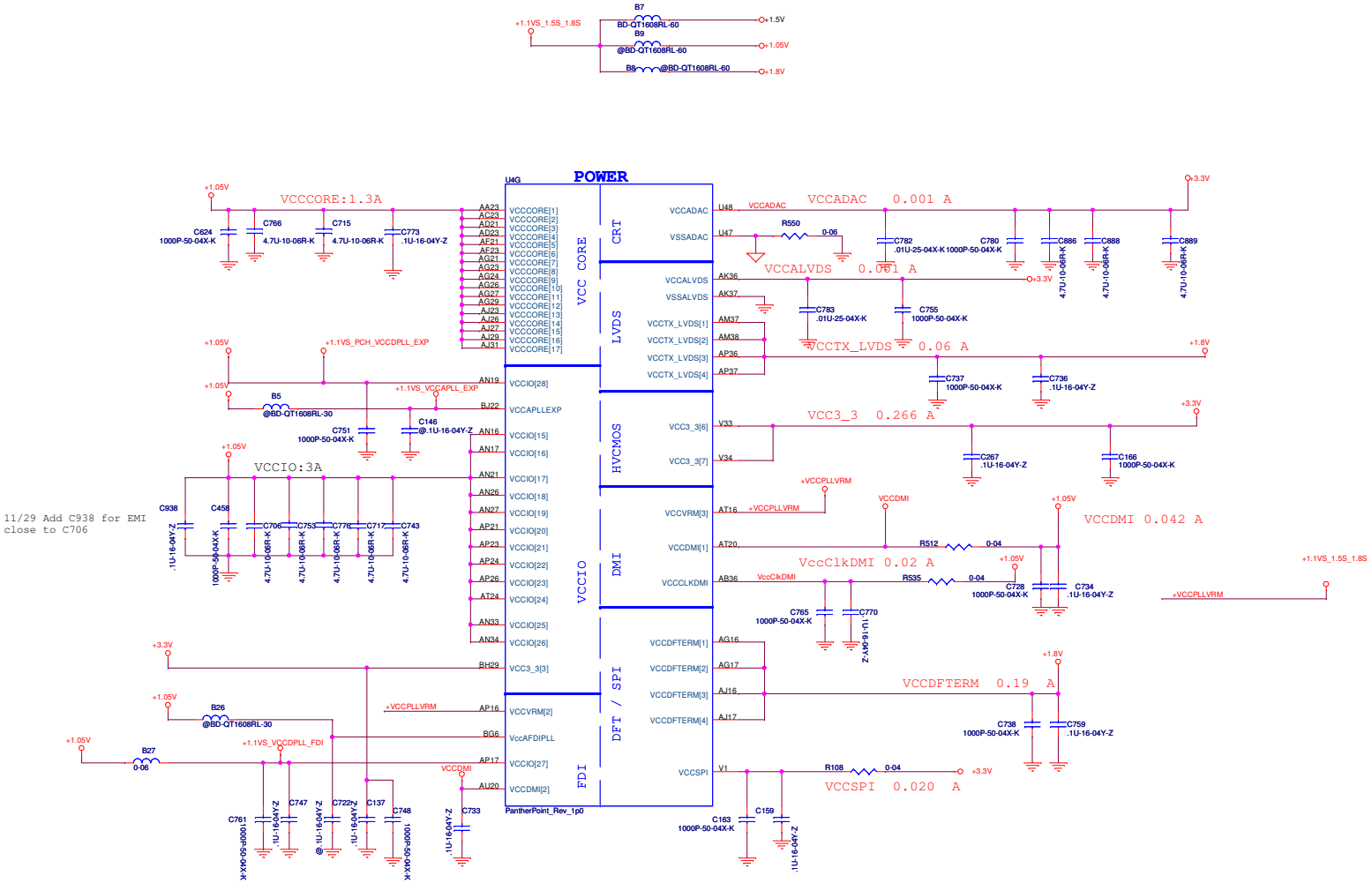
Title: **C14CU**

Size: Custom | Document Number: **PCH_PCI/USB (5 of 9)** | Rev: B

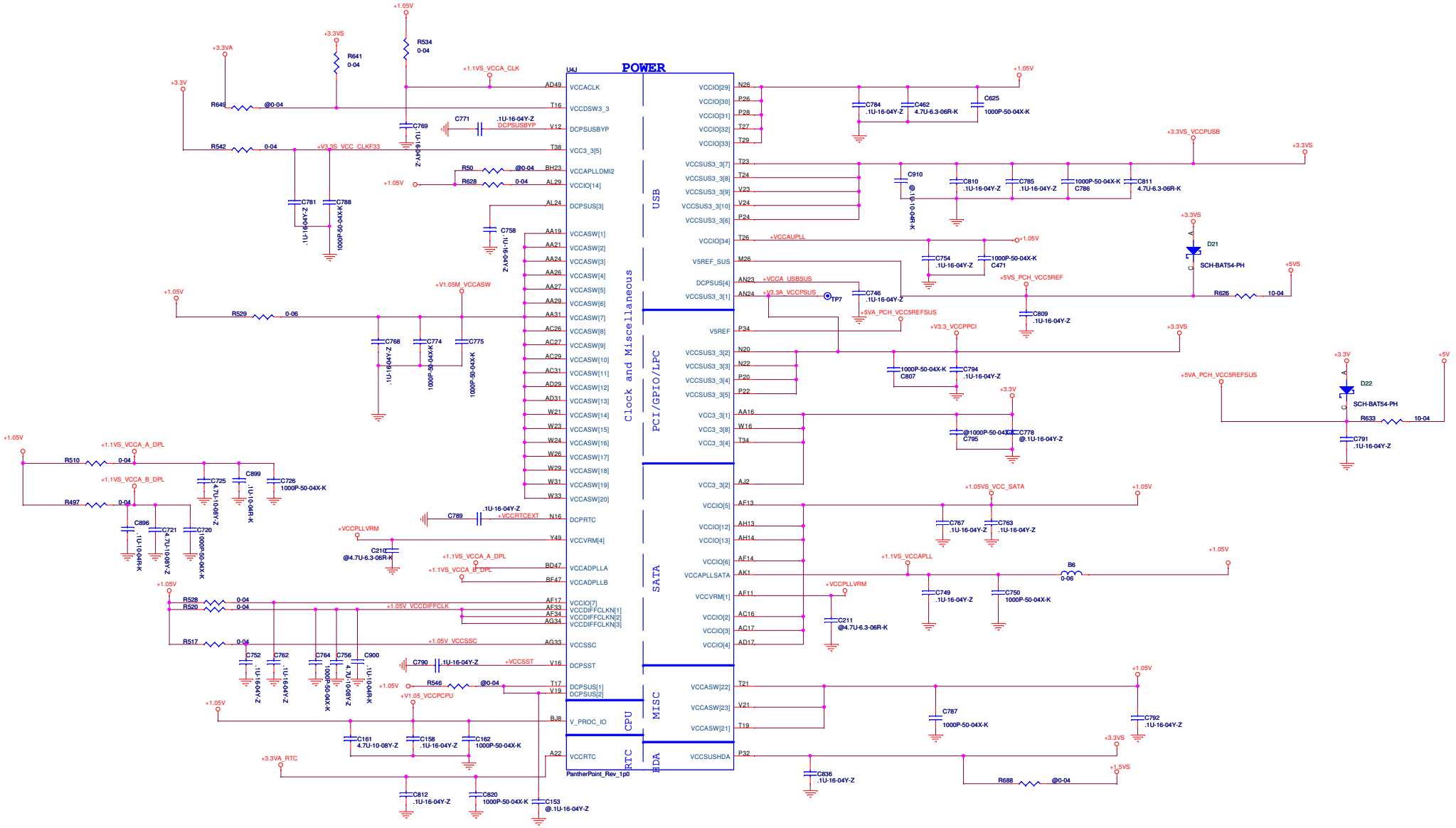
Date: Monday, June 11, 2012 | Sheet 18 of 41



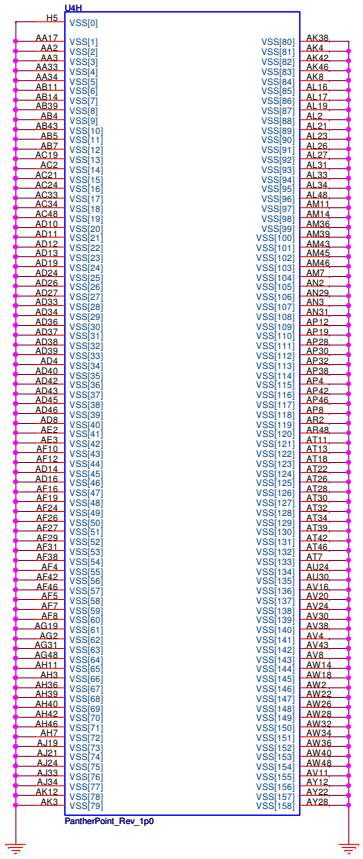
Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: PCH_GPIO/CPU (6 of 9)		Rev: B
Date: Monday, June 11, 2012	Sheet 19 of 41		

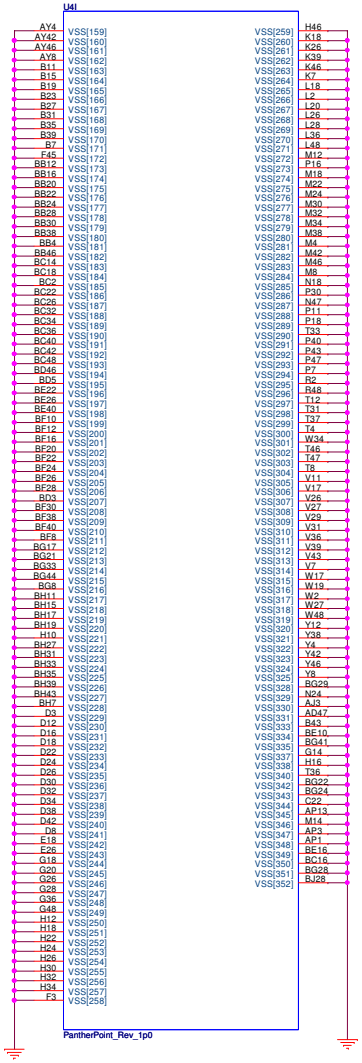


Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: PCH POWER-A (7 of 9)	Rev: B
Date: Monday, June 11, 2012	Sheet 20 of 41	

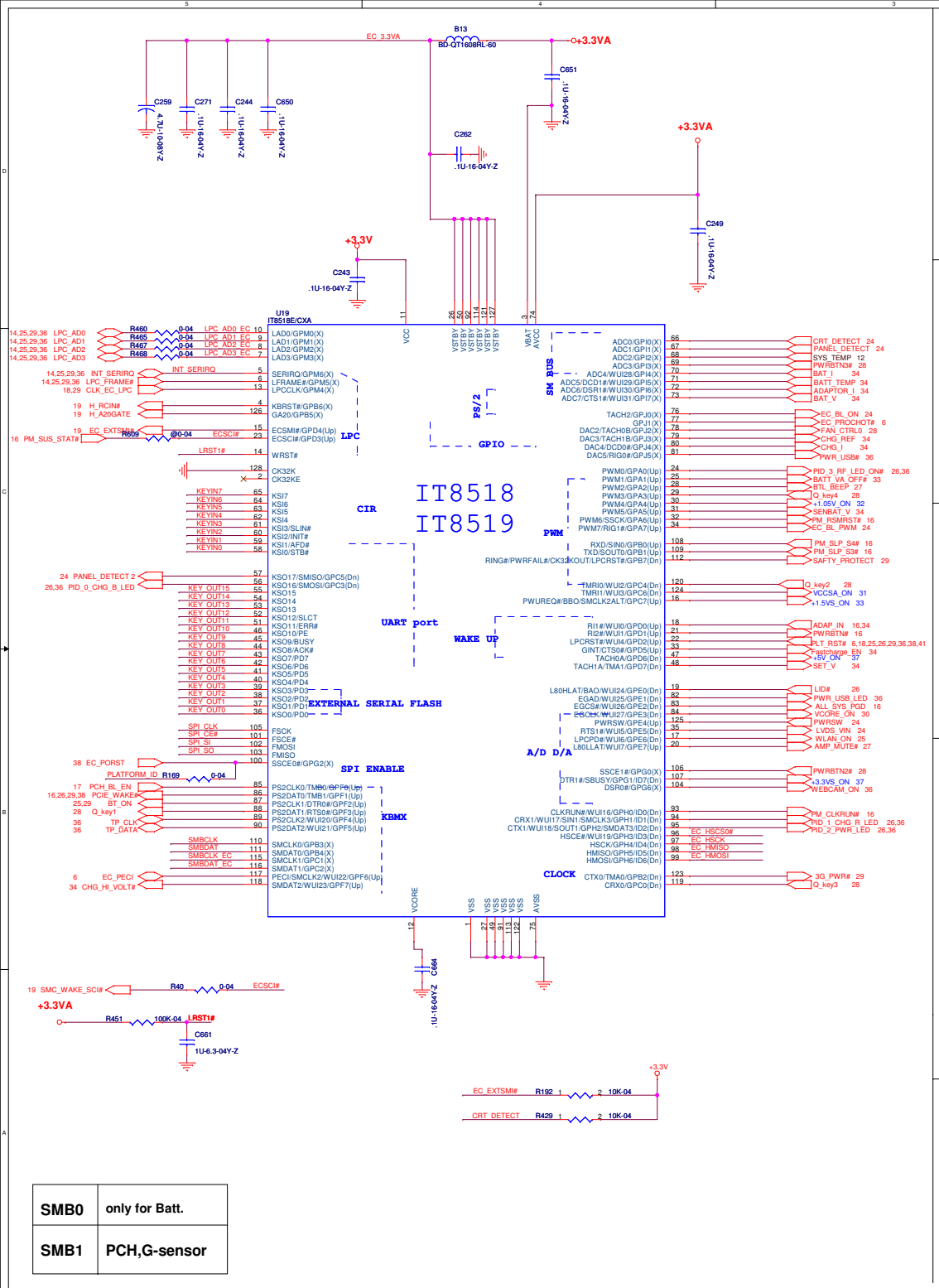


Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: PCH POWER-B (8 of 9)		Rev: B
Date: Monday, June 11, 2012	Sheet 21 of 41		



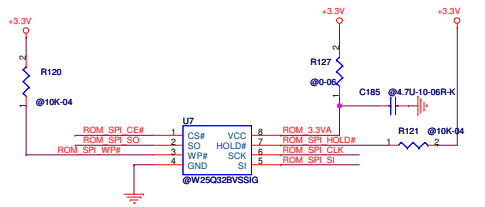


Shuttle Inc		
Title: **C14CU**		
Size: Custom	Document Number: **PCH GND (9 of 9)**	Rev: **B**
Date: Monday, June 11, 2012	Sheet 22 of 41	

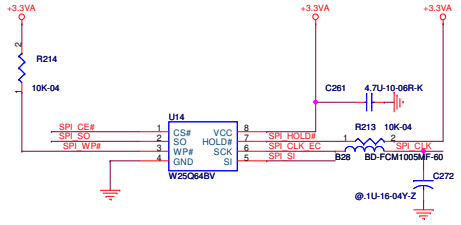


SMB0	only for Batt.
SMB1	PCH,G-sensor

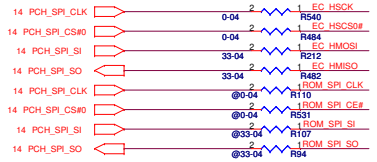
BIOS/ME FLASH ROM(SPI)



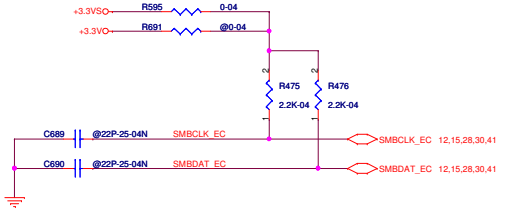
EC FLASH ROM(SPI)



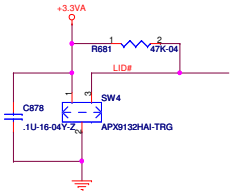
HSPI Select

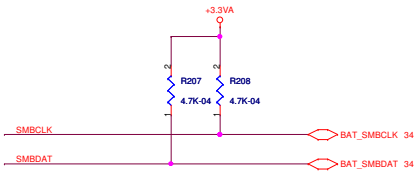


EC SMBUS LEVEL SHIFT

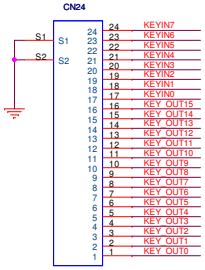


LID SW

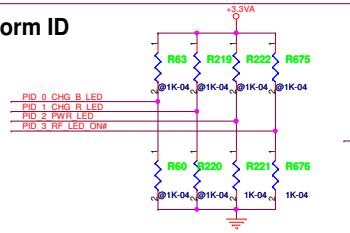


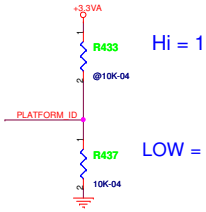


KEYBOARD Conn



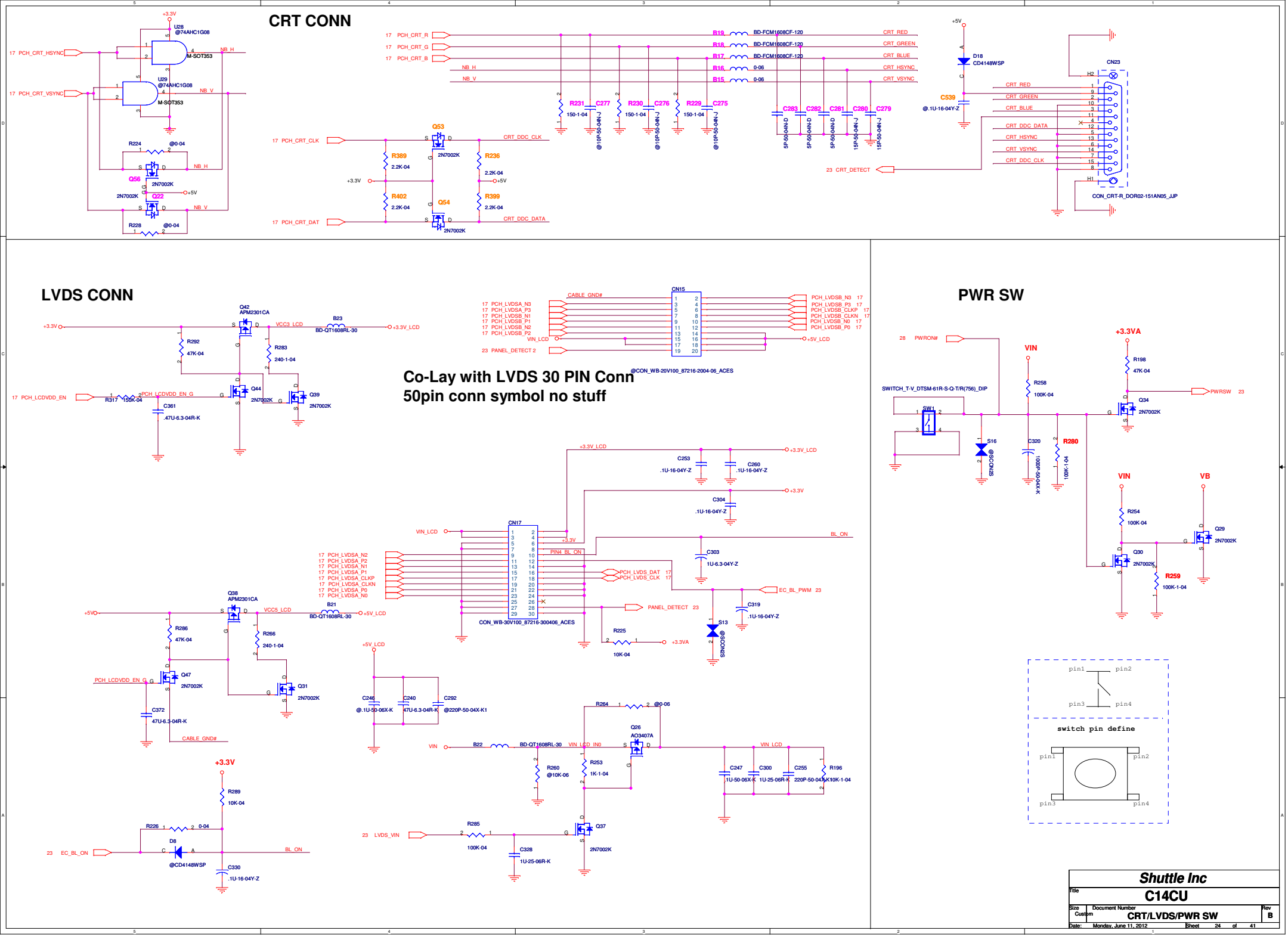
Platform ID



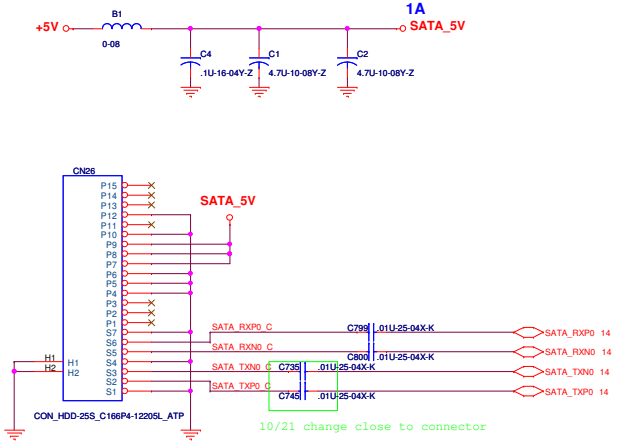


PID_2_PWR_LED: Low ,use 40W Adapter
High, use 65W Adapter

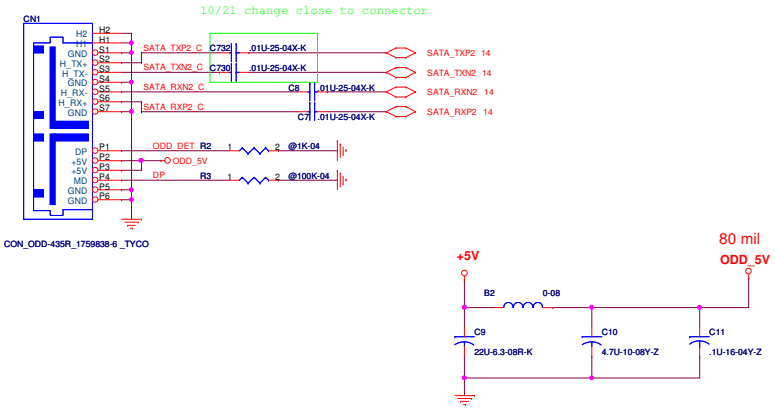
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: EC IT8500BX/BIOS/KB CONN	Rev: B
Date: Wednesday, July 18, 2012	Sheet 23 of 41	


CRT CONN
LVDS CONN
PWR SW
Co-Lay with LVDS 30 PIN Conn
50pin conn symbol no stuff
switch pin define
Shuttle Inc
C14CU
CRT/LVDS/PWR SW
Monday, June 11, 2012

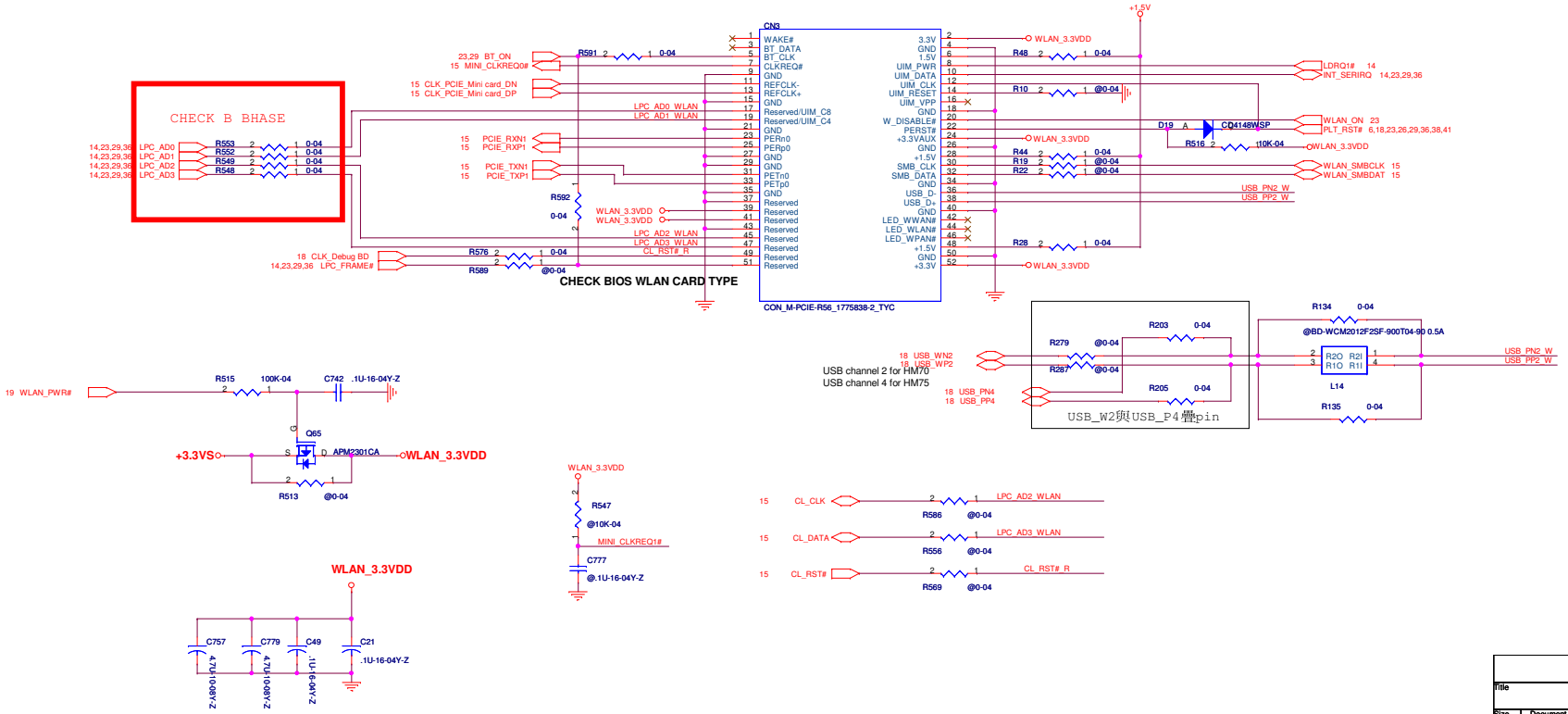
SATA-HDD



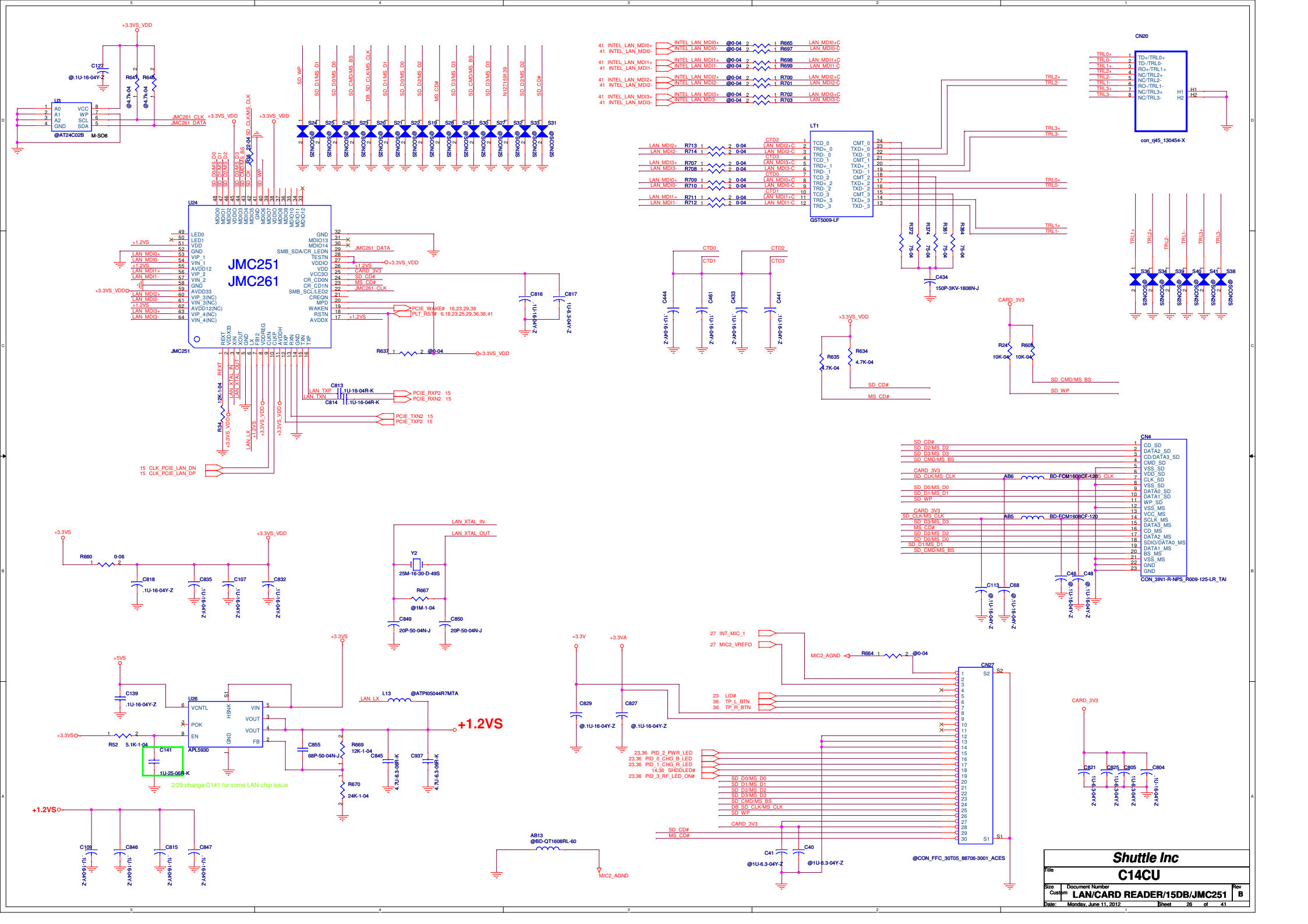
CD-ROM



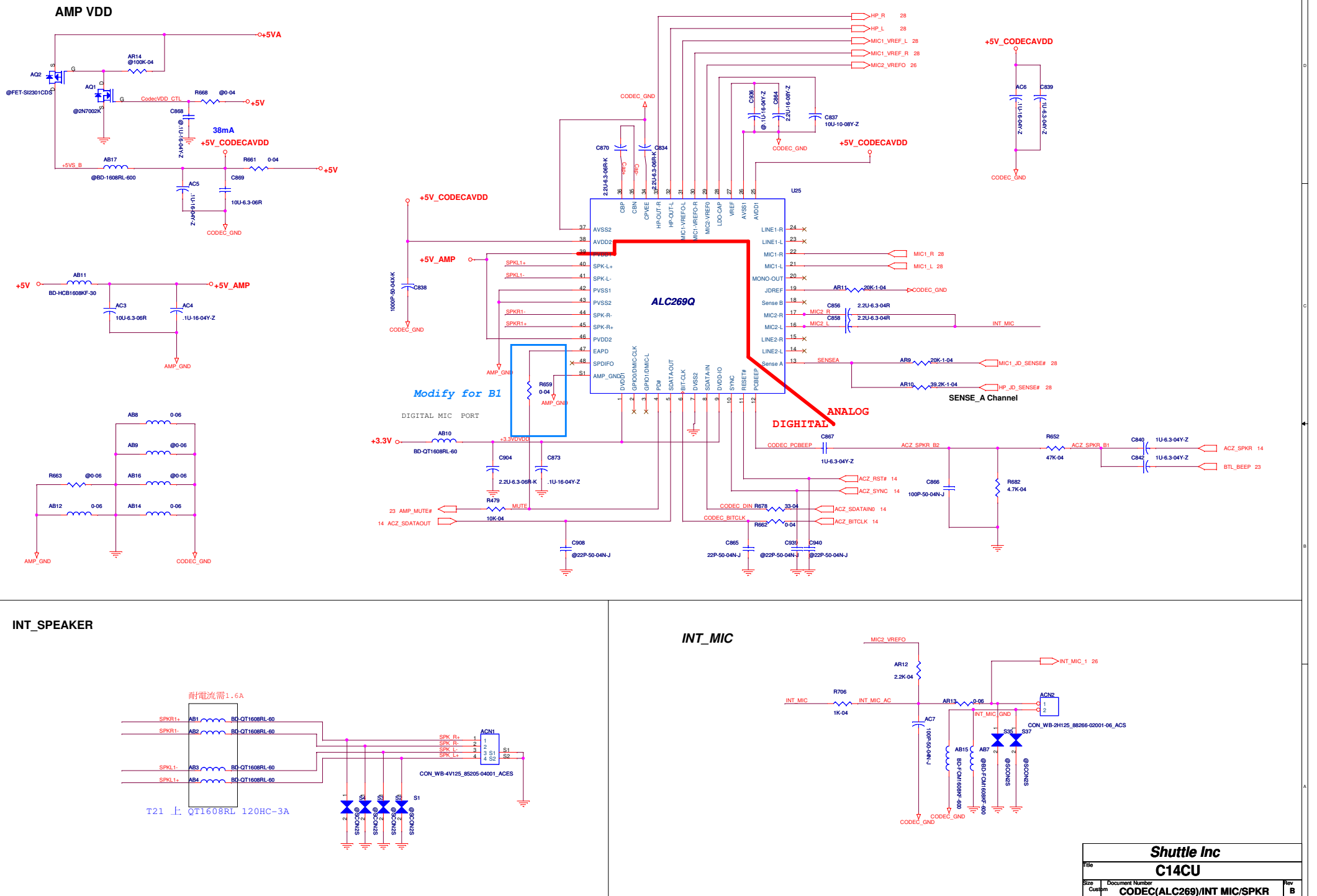
MINI CARD CONN



Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: HDD/ODD /MINI CARD		Rev: B
Date: Monday, June 11, 2012	Sheet 25 of 41		


JMC251
JMC261
APL5930
U24
U26
U3
LT1
CN20
CN4
CN27
GST5009-LF
con_rj45_130454-X
CON_3IN1-R-NPS_R009-125-LR_TAI
@CON_FFC_30T05_88706-3001_ACES
@AT24C02B M-SO8
Shuttle Inc
C14CU
LAN/CARD READER/15DB/JMC251
Monday, June 11, 2012
2/29 change C141 for some LAN chip issue

CODEC ALC269Q

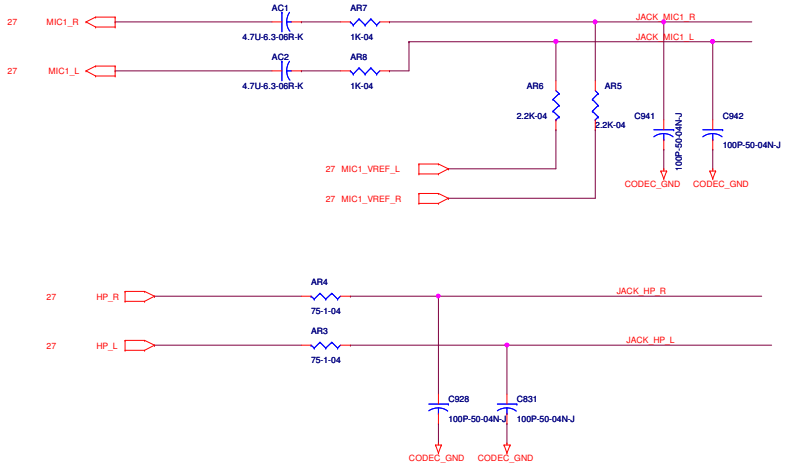


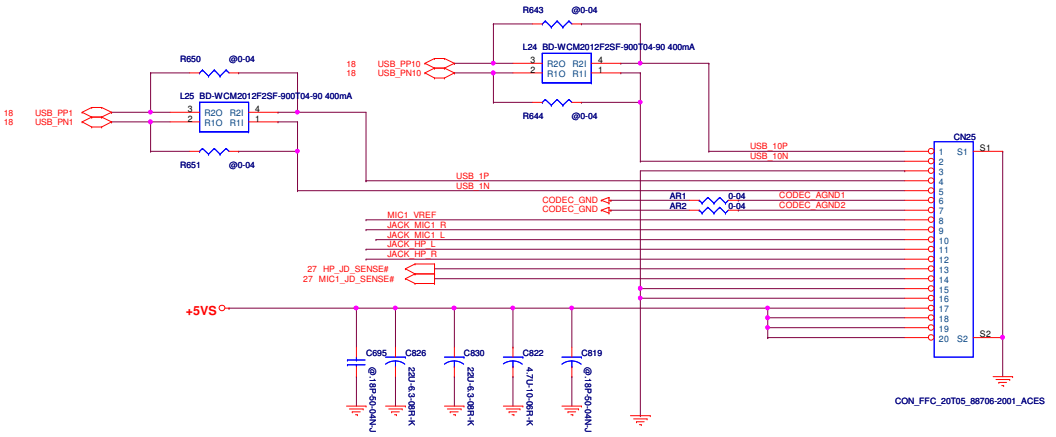
INT_SPEAKER

INT_MIC

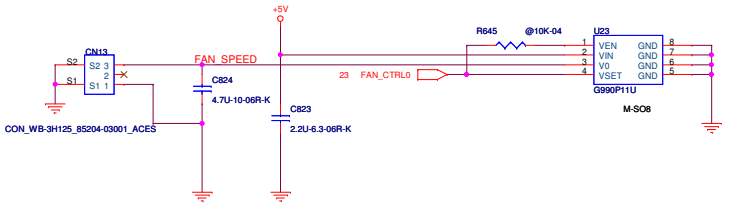
Shuttle Inc		
Title: **C14CU**		
Size: Custom	Document Number: **CODEC(ALC269)/INT MIC/SPKR**	Rev: B
Date: Monday, June 11, 2012	Sheet 27 of 41	

EXT MIC / EXT LINE IN / EXT USB JACK

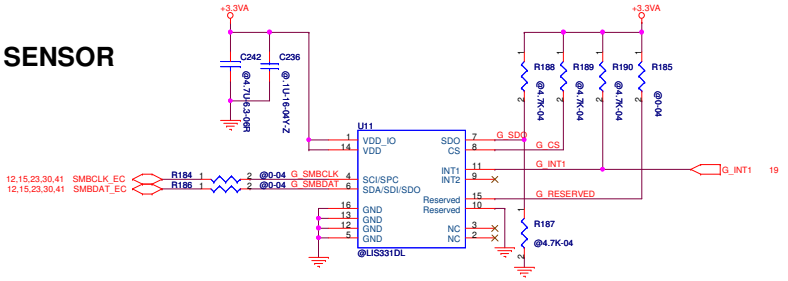




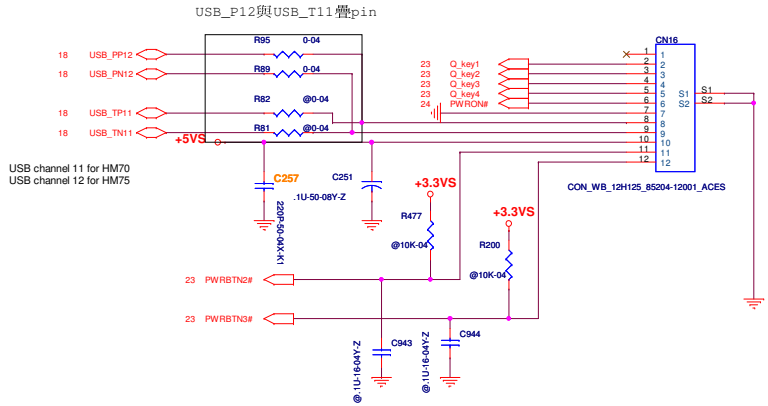
FAN CONTROLLER



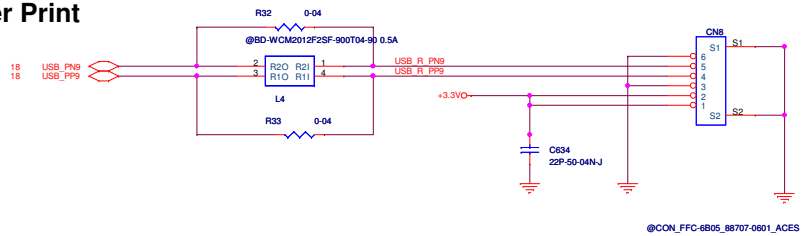
G SENSOR



EXT USB PORT 4 & Q KEY



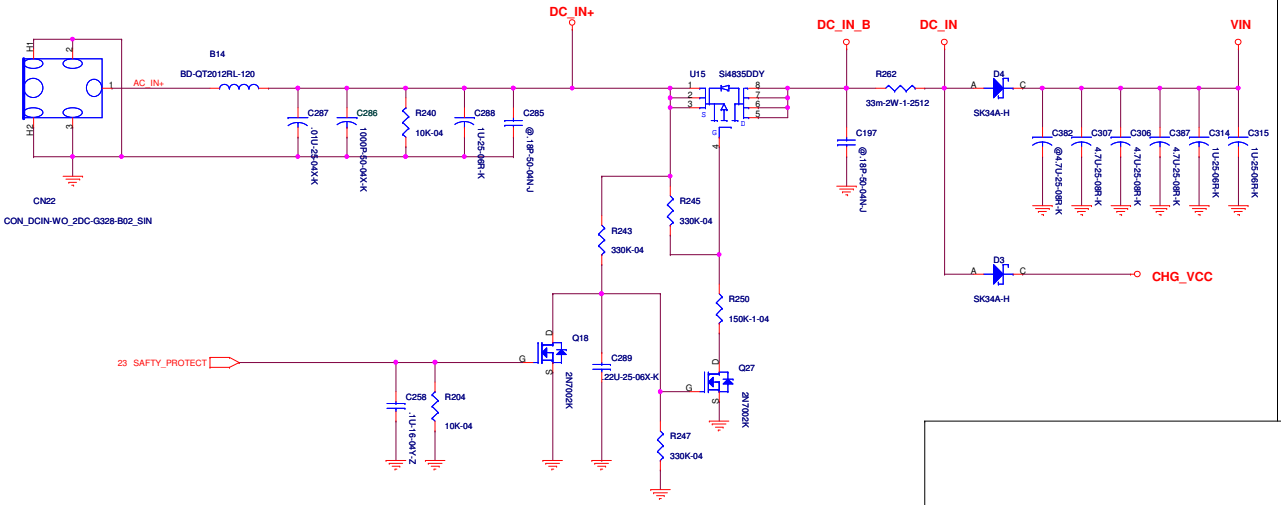
Finger Print



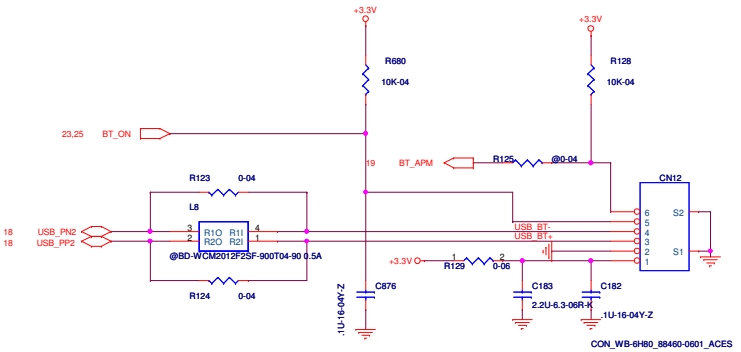
Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: EXT_MIC/H_P/USB/FAN/G-SENSOR/3G	Rev: B
Date: Monday, June 11, 2012	Sheet 28 of 41	

DC IN

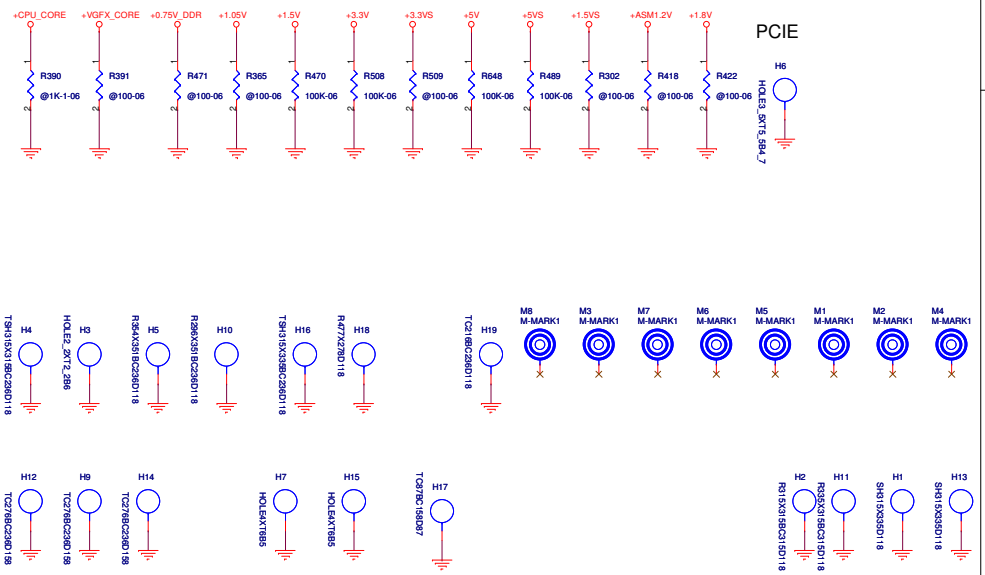
PROJECT	C14CR03			
Adaptor	40W	65W	90W	120W
Rsense	50m Ohm	33m Ohm	25m Ohm	18m Ohm
Stop Charger	?W	60W	80W	110W



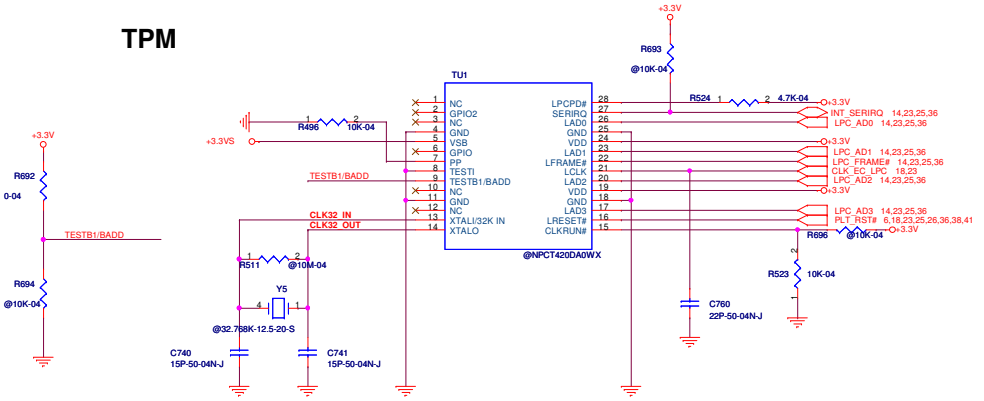
BT CONN

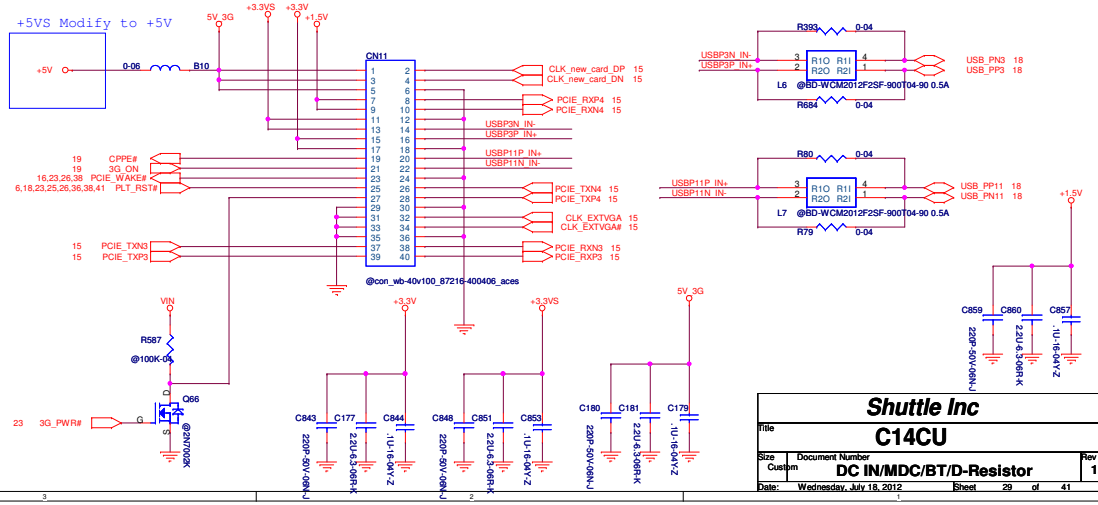


Discharge Resistor



TPM





Shuttle Inc

Title: **C14CU**

Size: Custom | Document Number: **DC IN/MDC/BT/D-Resistor** | Rev: 1.0

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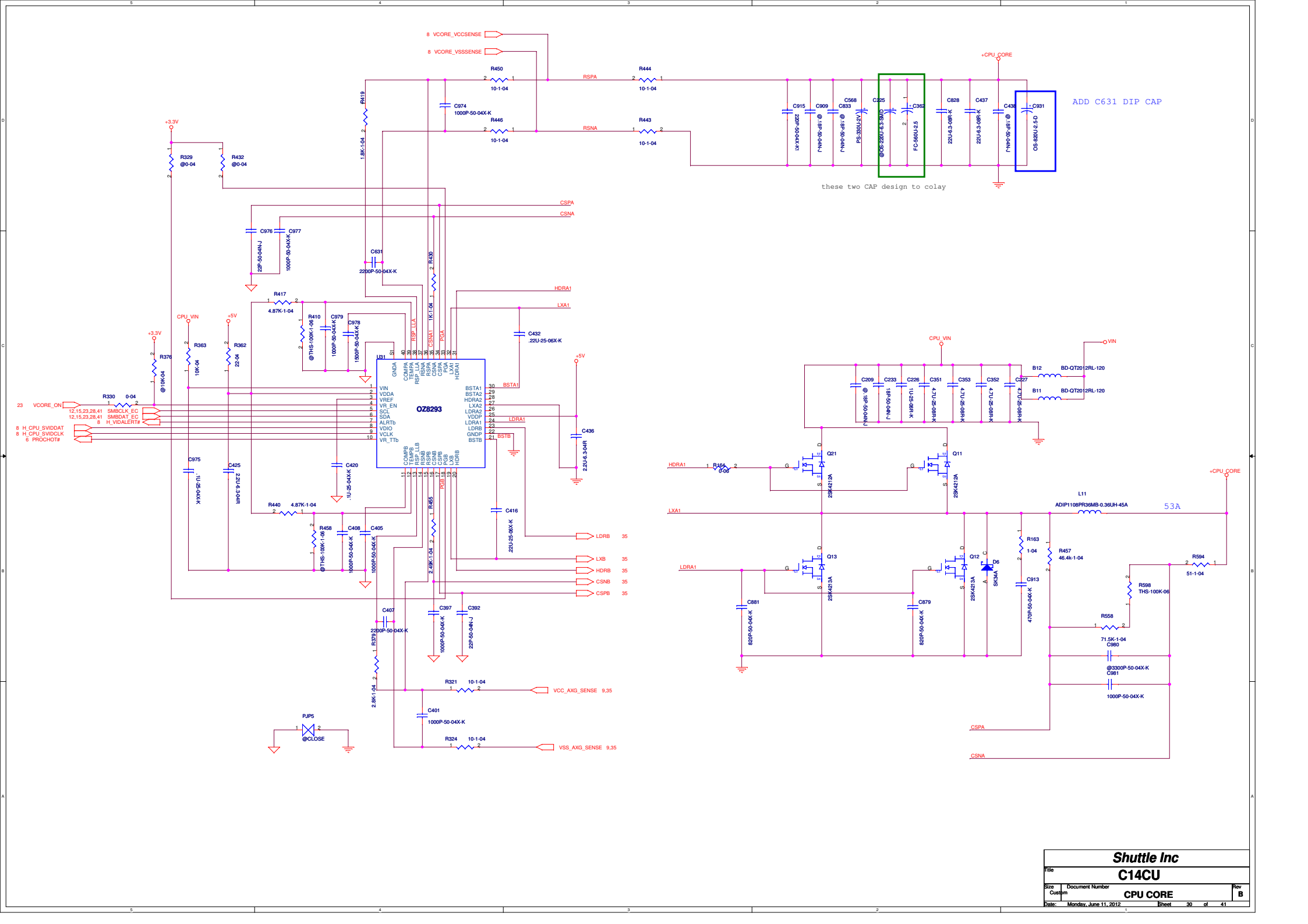
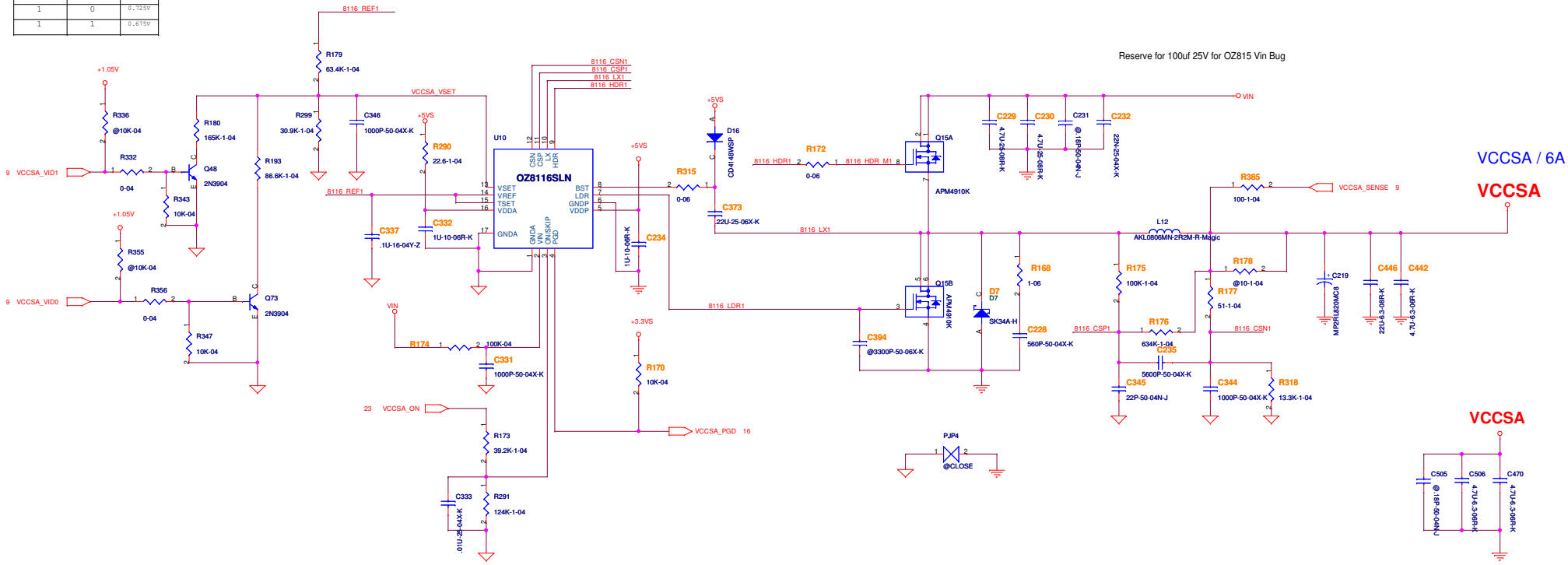
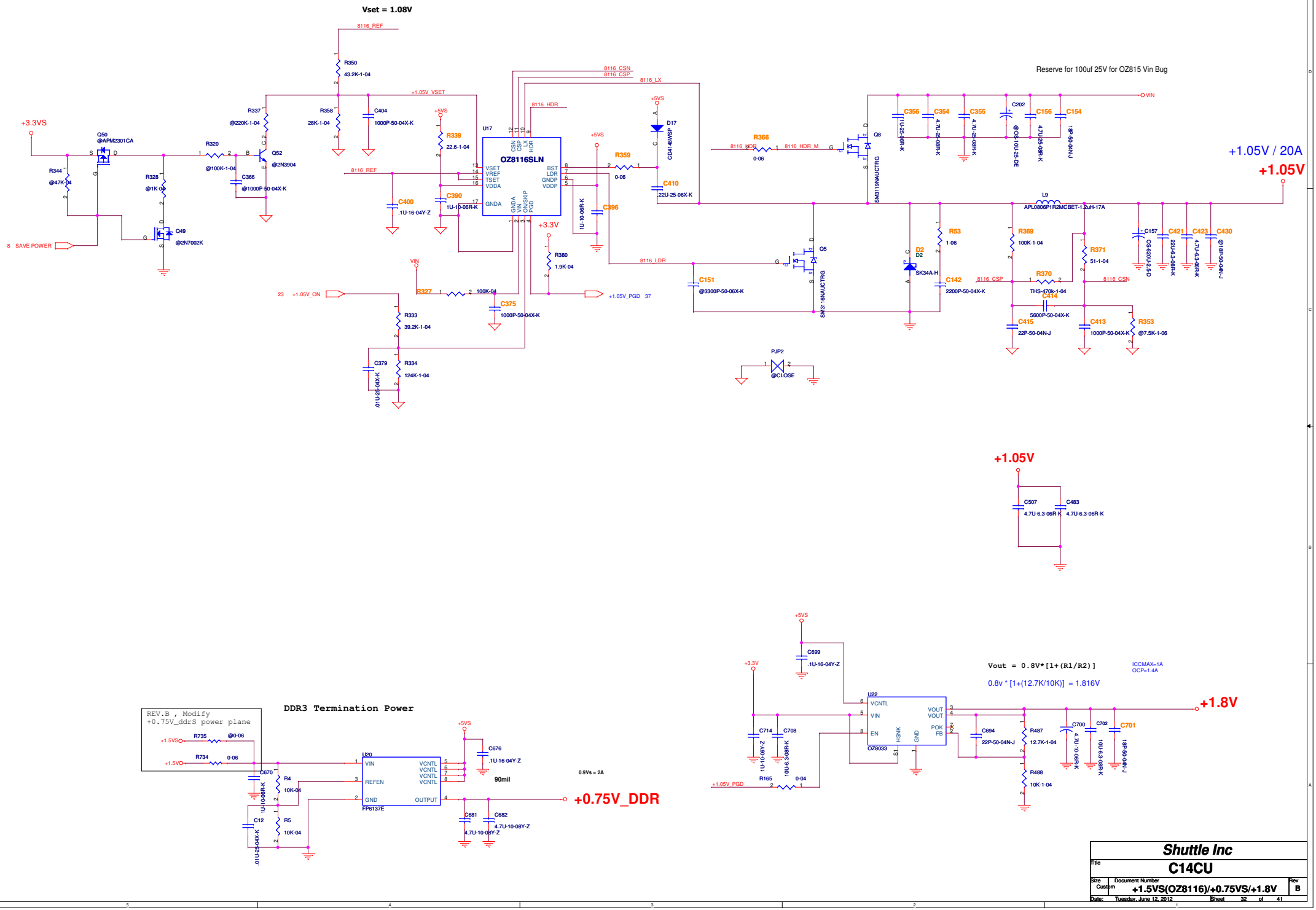


Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: CPU CORE		Rev: B
Date: Monday, June 11, 2012		Sheet 30 of 41	

VCCSA_SEL		
VCCSA_VID0	VCCSA_VID1	V_set
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



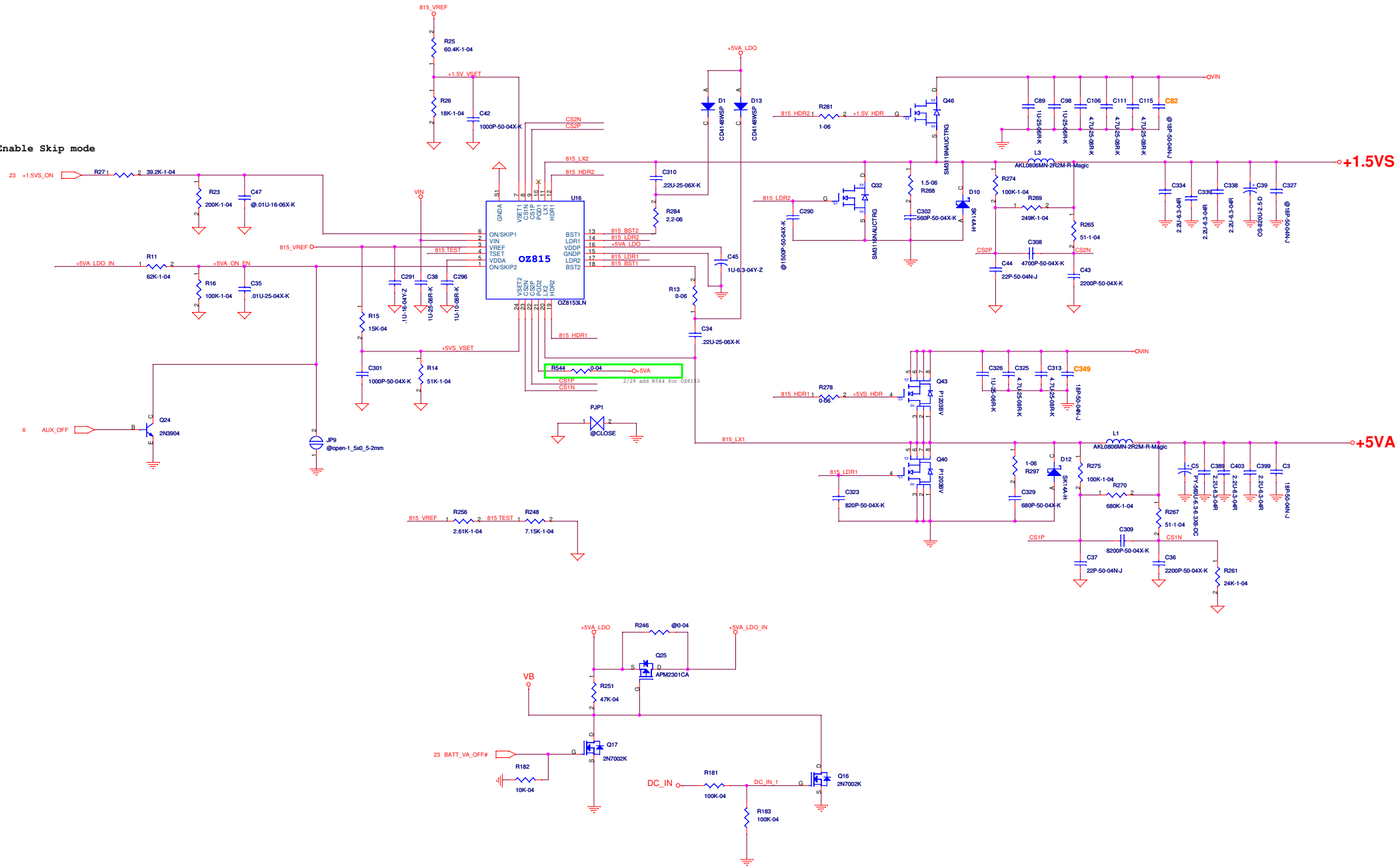
Title	C14CU		
Size: Custom	Document Number: CPU VCCSA		Rev: B
Date: Monday, June 11, 2012	Sheet 31 of 41		


Vset = 1.08V
Reserve for 100uf 25V for OZ815 Vin Bug
+1.05V / 20A
+1.05V
OZ8116SLN
SM3118NAUCTRG
SM3116NAUCTRG
APL0806P1R2MCBET-1.2uH-17A
+3.3VS
+5VS
VIN
8116_REF
8116_CSN
8116_CSP
8116_LX
8116_HDR
8116_LDR
+1.05V_VSET
+1.05V_ON
+1.05V_PGD
SAVE POWER
DDR3 Termination Power
REV.B , Modify
+0.75V_ddrS power plane
FP6137E
+0.75V_DDR
0.9Vs = 2A
90mil
Vout = 0.8V*[1+(R1/R2)]
0.8v * [1+(12.7K/10K)] = 1.816V
ICCMAX=1A
OCP=1.4A
OZ8033
+1.8V
Shuttle Inc
C14CU
+1.5VS(OZ8116)/+0.75VS/+1.8V
Rev B
Tuesday, June 12, 2012
Sheet 32 of 41

+1.8V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

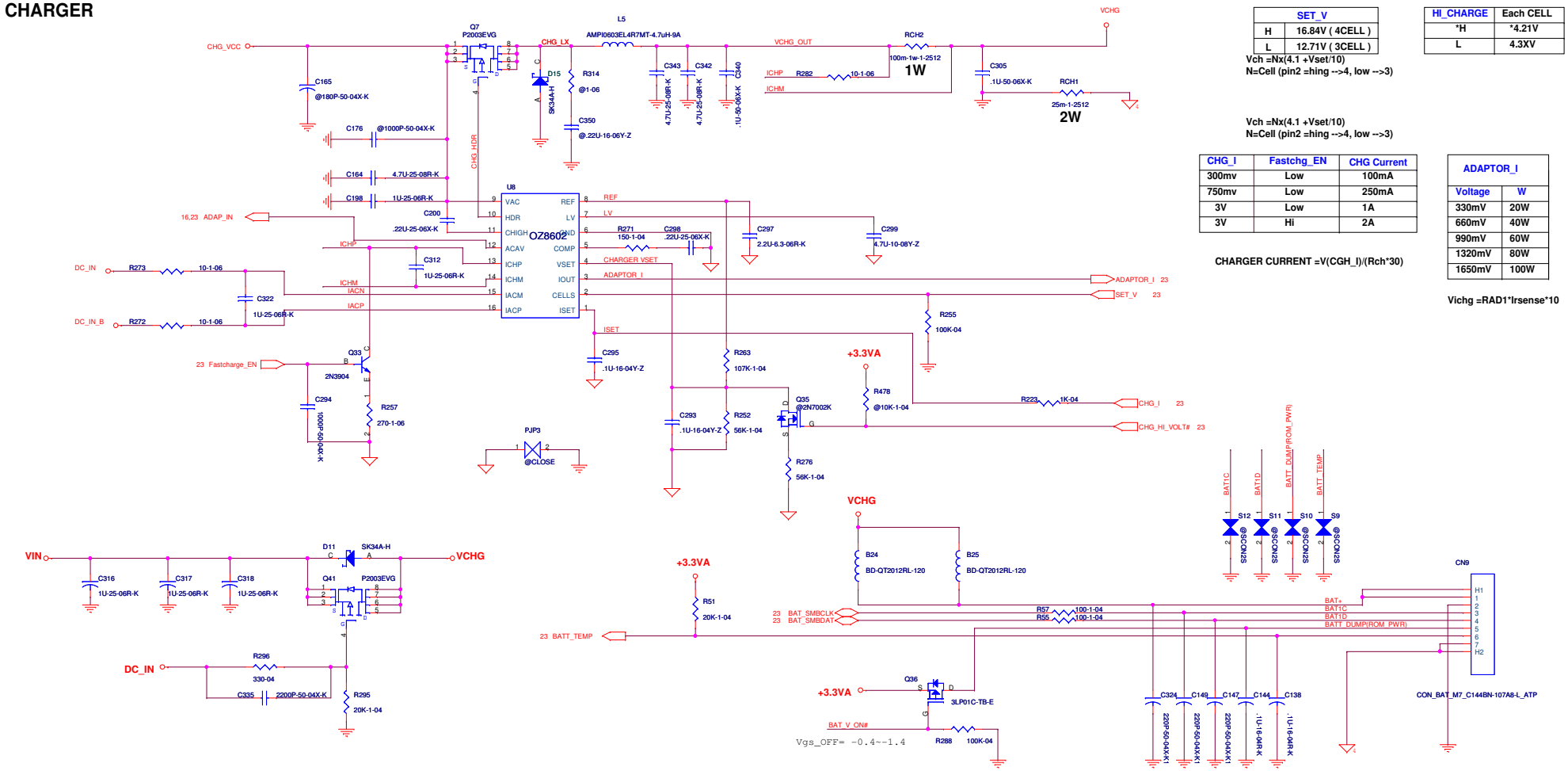
Output Voltage =[Vref x R2/(R1+R2)] x 2

Enable Skip mode



Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: +1.05VS/+5VA (OZ815)		Rev: B
Date: Monday, June 11, 2012		Sheet 33 of 41	

CHARGER



SET_V	
H	16.84V (4CELL)
L	12.71V (3CELL)

Vch =Nx(4.1 +Vset/10)
N=Cell (pin2 =hing -->4, low -->3)

HI_CHARGE	Each CELL
*H	*4.21V
L	4.3XV

Vch =Nx(4.1 +Vset/10)
N=Cell (pin2 =hing -->4, low -->3)

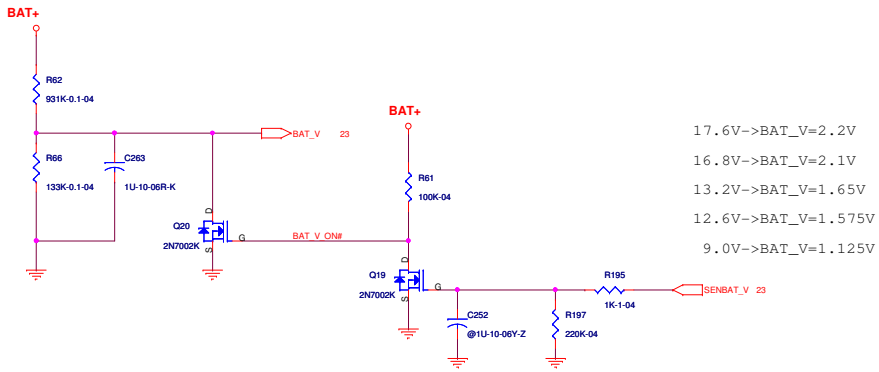
CHG_I	Fastchg_EN	CHG Current
300mv	Low	100mA
750mv	Low	250mA
3V	Low	1A
3V	Hi	2A

CHARGER CURRENT =V(CGH_I)/(Rch*30)

ADAPTOR_I	
Voltage	W
330mV	20W
660mV	40W
990mV	60W
1320mV	80W
1650mV	100W

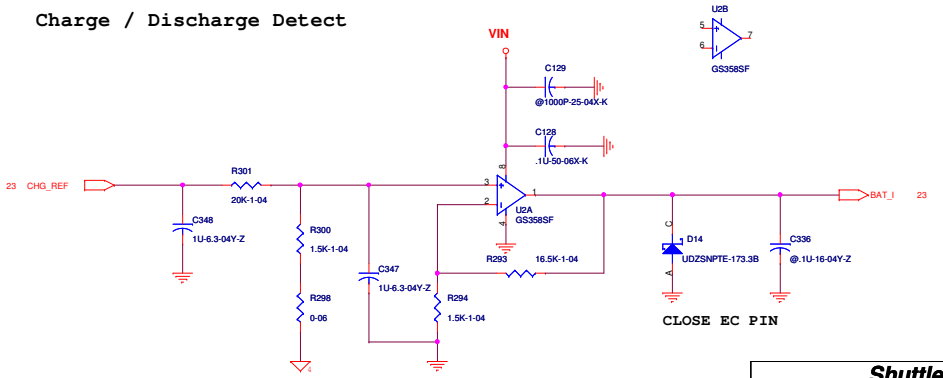
Vichg =RAD1*Irsense*10

Battery Voltage Detect



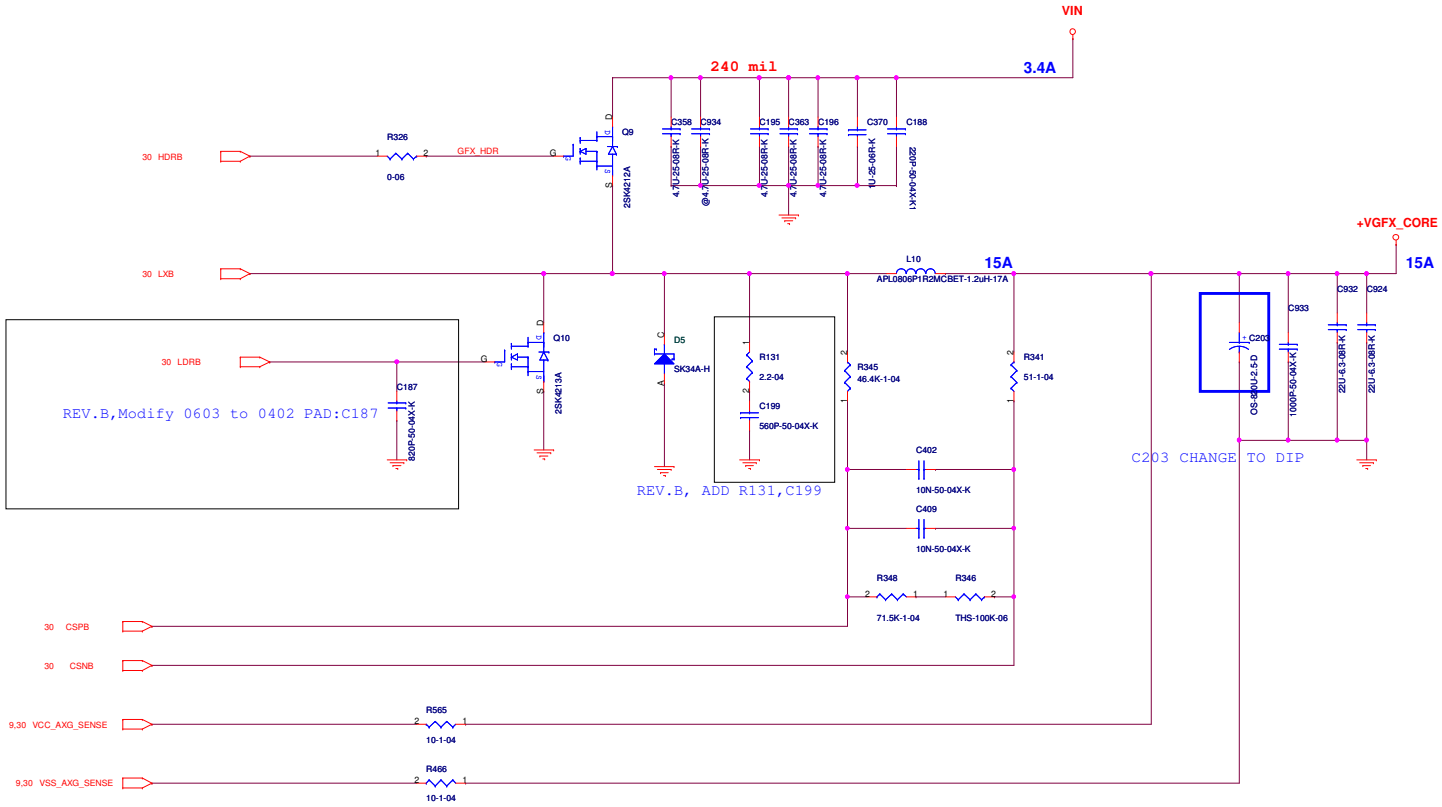
17.6V->BAT_V=2.2V
16.8V->BAT_V=2.1V
13.2V->BAT_V=1.65V
12.6V->BAT_V=1.575V
9.0V->BAT_V=1.125V

Charge / Discharge Detect



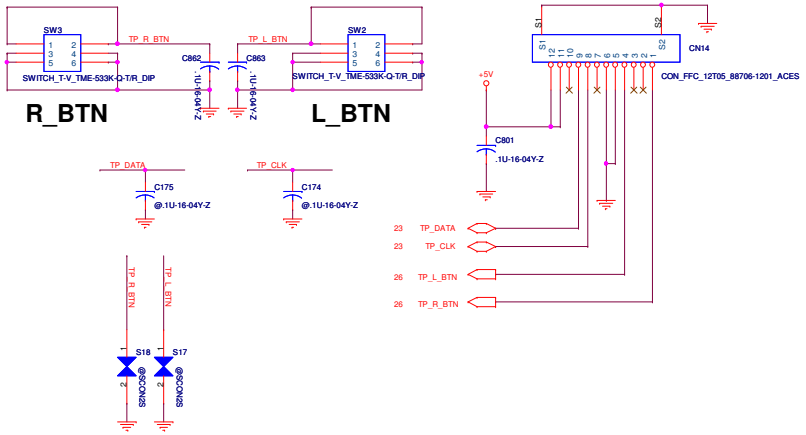
CLOSE EC PIN

Shuttle Inc			
Title: C14CU			
Size: Custom	Document Number: BATT IN/CHARGER(OZ8602)		Rev: B
Date: Monday, June 11, 2012		Sheet 34 of 41	

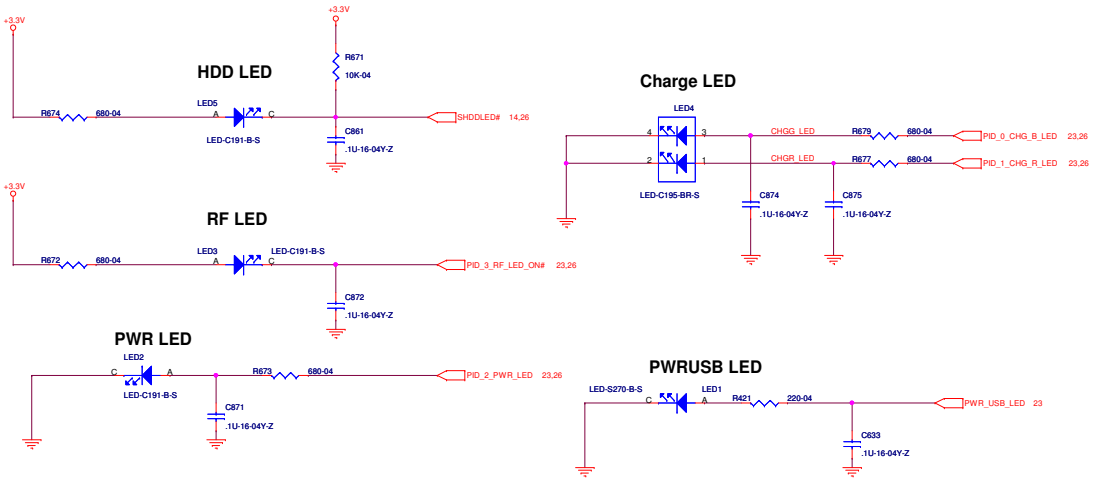


Shuttle Inc		
Title: C14CU		
Size: Custom	Document Number: iGPU_CORE	Rev: B
Date: Monday, June 11, 2012	Sheet 35 of 41	

Touch Pad

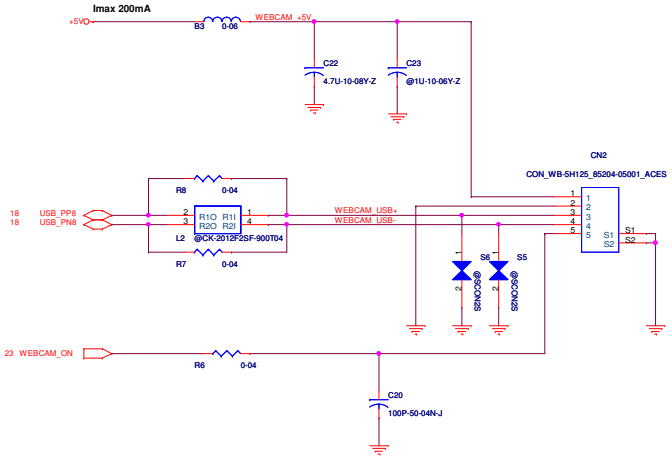


LED

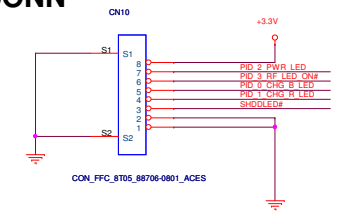


Webcam CONN

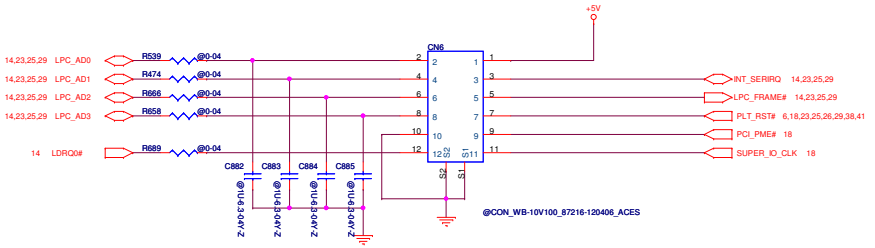
WEBCAM_ON	
1	ON
0	OFF



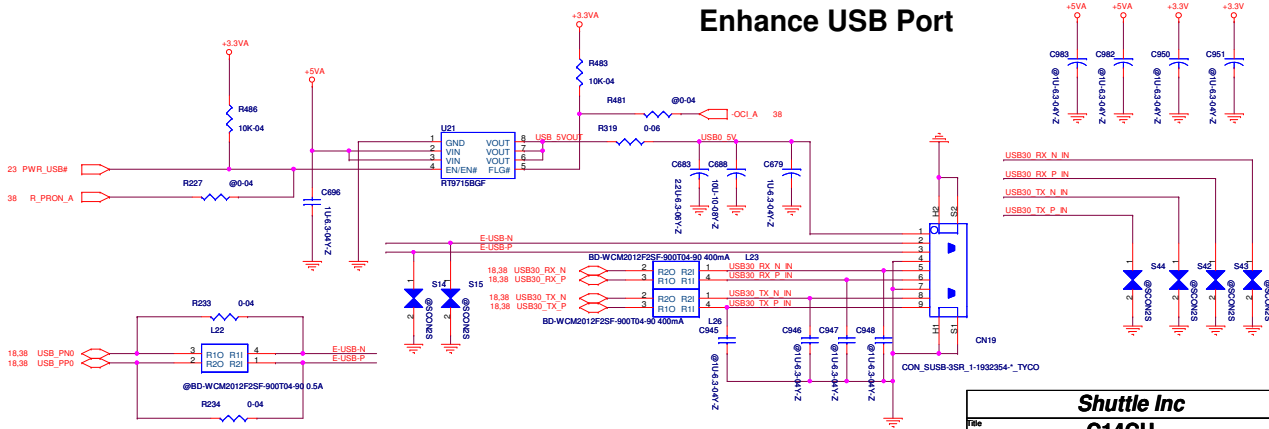
LED CONN



RS232 CONN



Enhance USB Port



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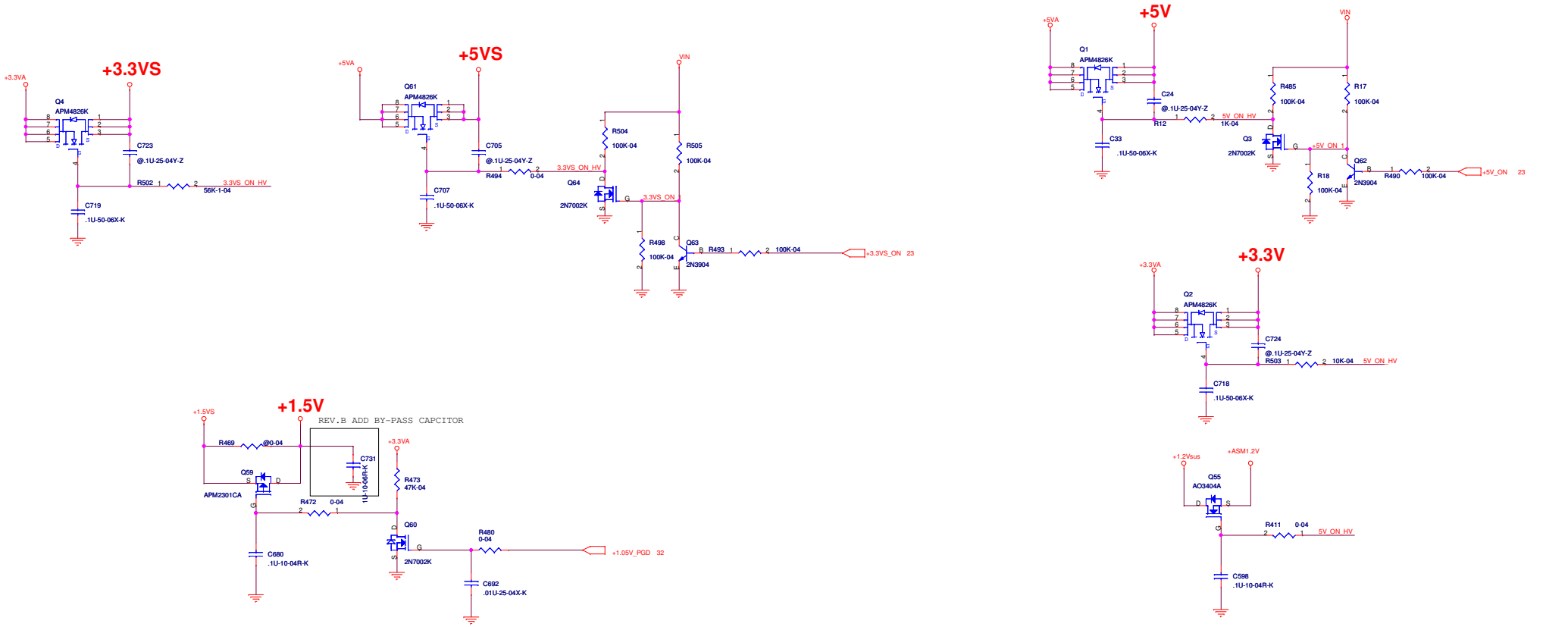
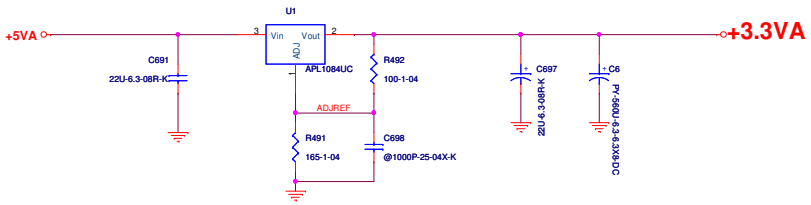
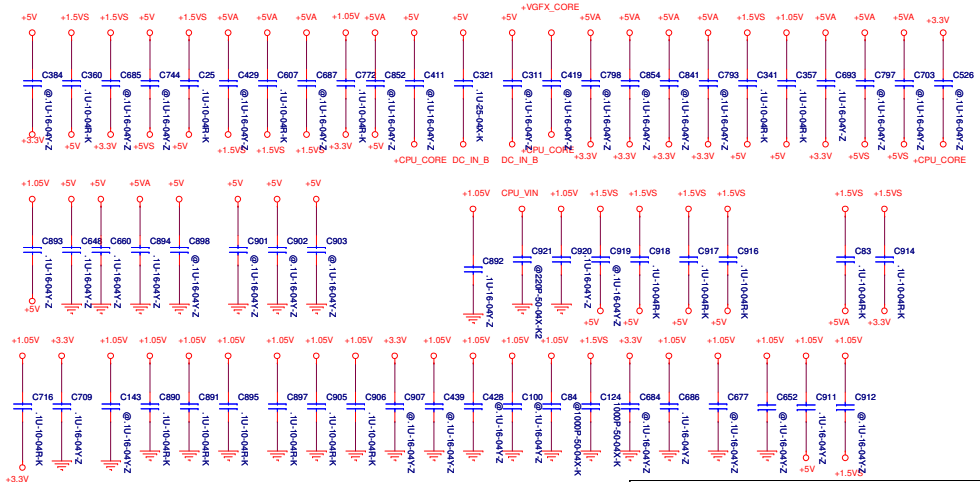
VCCSW



LDO



HIGH-SPEED CAP



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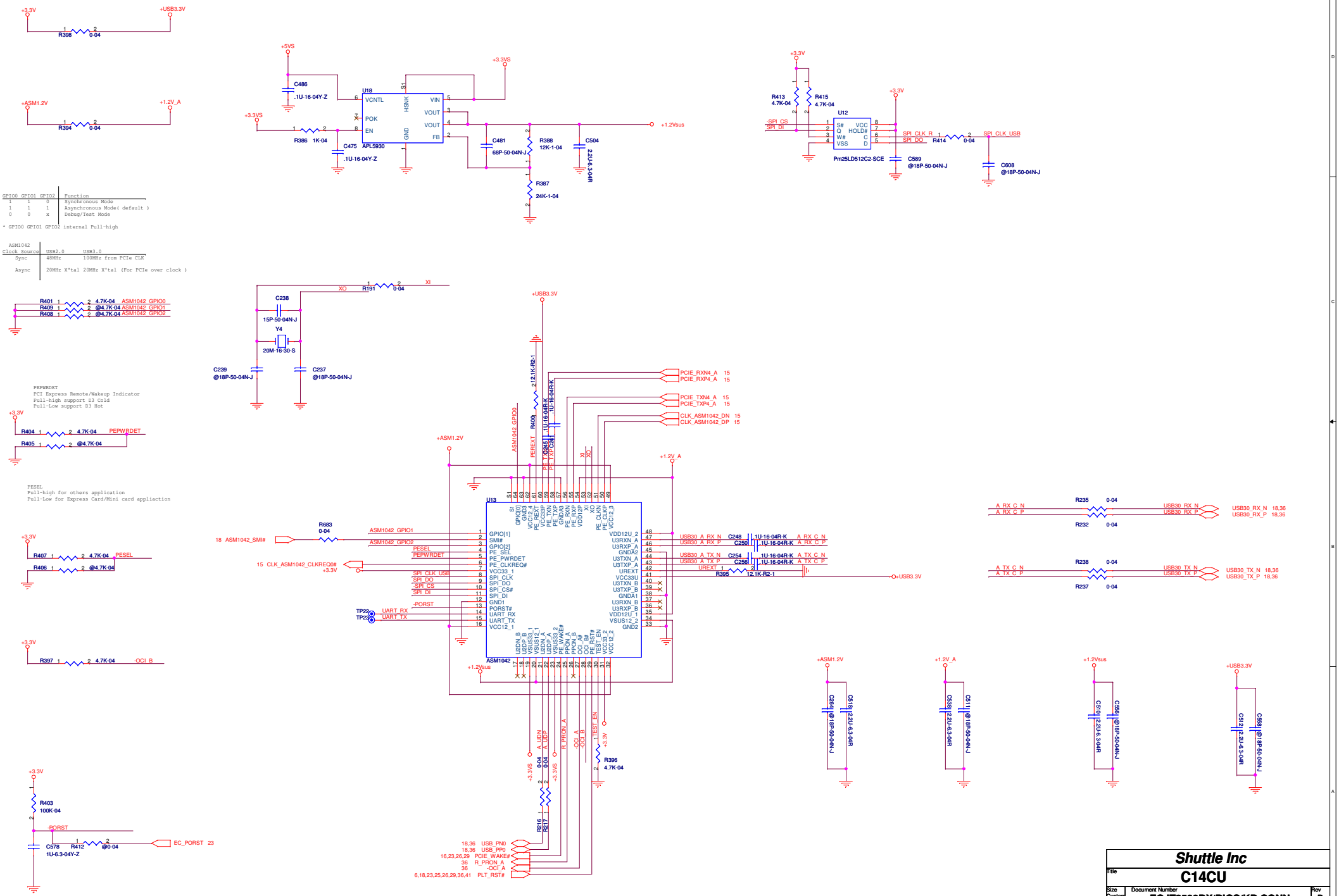
USB 3.0



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MA1:Change net name from PCH_SMB_CLK to PCH_SMB_CLK_DDR
MA2:Change net name from PCH_SMB_DATA to PCH_SMB_DATA_DDR
MA3:DEL CLK_ASM1042_CLKREQ0# path(R87 OP)
MA4:Change ACPRESENT to EC pin 88
MA5:ADD 0R FOR 25MHZ CLK(R534)
MA6:ADD 0R FOR PCH SATA POWER(B6)
MA7:Sharing System BIOS ROM for KB & EC Codes(Del U7)
MA8:ADD EC_HSCK path for sharing ROM(ADD R540)
MA9:ADD EC_HSCS0# path for sharing ROM(ADD R484)
MA10:ADD EC_HMOSI path for sharing ROM(ADD R212)
MA11:ADD EC_HMISO path for sharing ROM(ADD R482)
MA12:ADD 0R FOR AMP_GND(ADD AB12)
MA13:Change CN16 PIN DEFINE
MA14:DEL R147 for PROCHOT issue
MA15:ADD ISEN1 Pull Hi +5V(ADD R356)
MA16:Change C203 SMD CAP TO DIP CAP
MA17:ADD ASM1042_SMI# path(ADD R683)
MA18:Change CN19 PIN DEFINE
MA19:ADD EMI solution(ADD C251,C257,C357,C341,C684,C686,C25,C660,C677   DEL C99,C430)

MB1:Change CPURST# path(OP:R457,Q72,R656,Q71,R659   ADD:R452,R453)
MB2:Change DDR3_DRAMRST_R path(OP:Q67   ADD:R628)
MB3:Change PM_SYSRST# Pull_up power to +3.3V
MB4:Change USB part 1(External USB)to USB part 12 for testingSignal
MB5:Sharing System BIOS ROM for KB & EC Codes(OP:R110,R531,R107,R94)
MB6:ADD SYS_TEMP EC Pin68 for Thermal(ADD RT1,R426)
MB7:ADD CPU Thermal Sensor NTC7717U for Thermal(ADD U27,R693,C887)
MB8:Change SATA3RBIAS external pull-down resistor for testingSignal (R90:1K-1-04)
MB9:ADD RS-232 CONNECT FOR DA18(OP:CN6,,R539,R474,R666,R658,R689,C882,C883,C884,C885)
MB10:Change ASM1042_SMI# path for AMI(GPIO4)

B PHASE

1.Page 35 :C187 Modify 0603 to 0402 SIZE

2.Page 15,Modify PCIE port4 colay,USB3.0 IC use PORT4 ,add C984,C985,ADD R730,R731,R732,R733

3.PAGE 35,REV.B, ADD R131,C199

4. Page14, Modify C148,C150 from 15p to 12p

5. Page32, Modify 0.75v_DDR power plane

6. Page32, REV.B ADD BY-PASS CAPCITOR C731

NPI PHASE

1.Page 23 :Add R221 for 40W Adapter support

2.Page 29 :CN11 "+5VS" Modify to "+5V"

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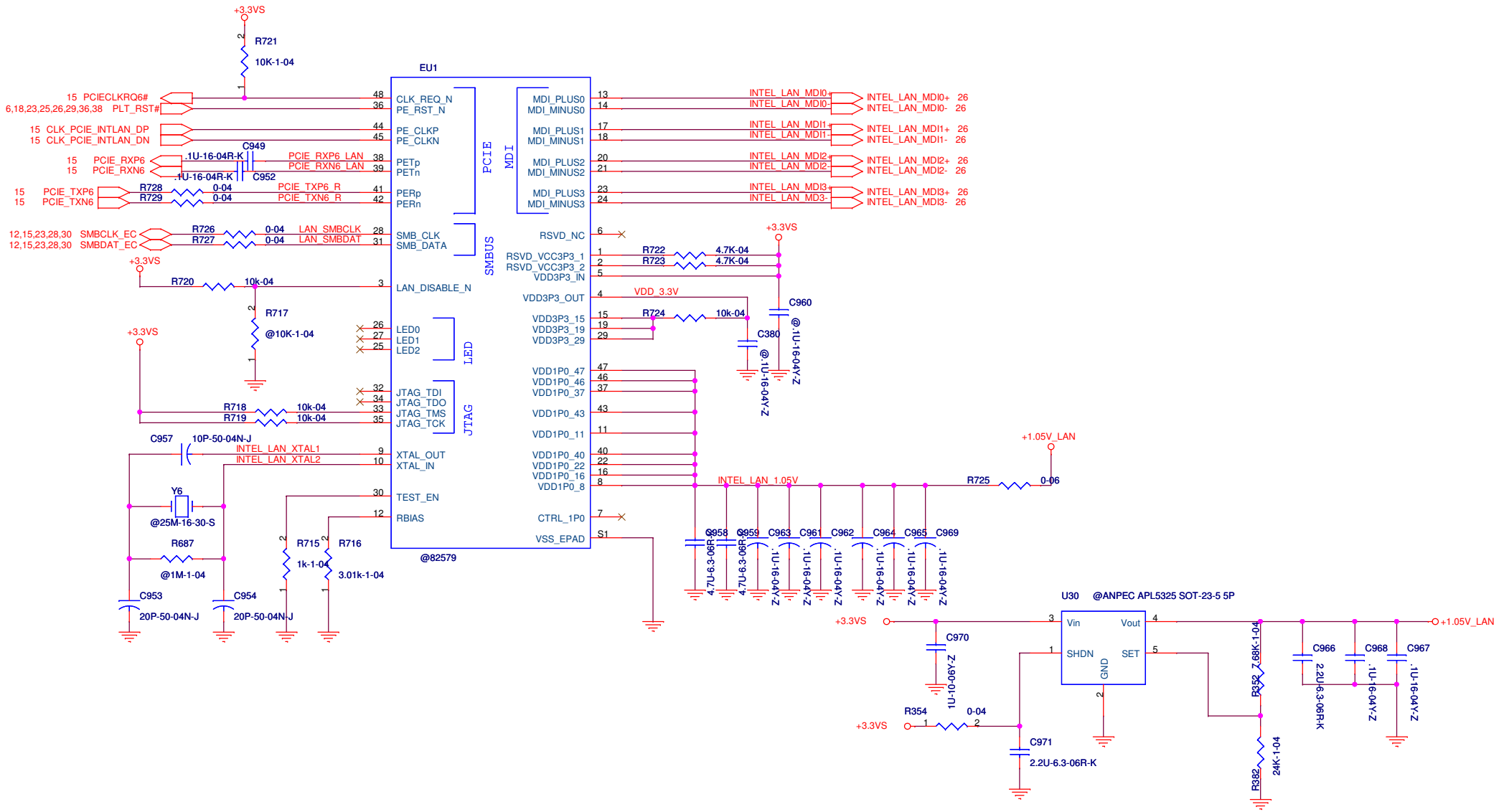

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