Mockingbird-N/V 14/15_ICL & Hellcat 14/15_ICL Schematic

2019-09-17
REV : SA

DY : None Installed
UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

<Core Design>

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Title	*Cover Page*	
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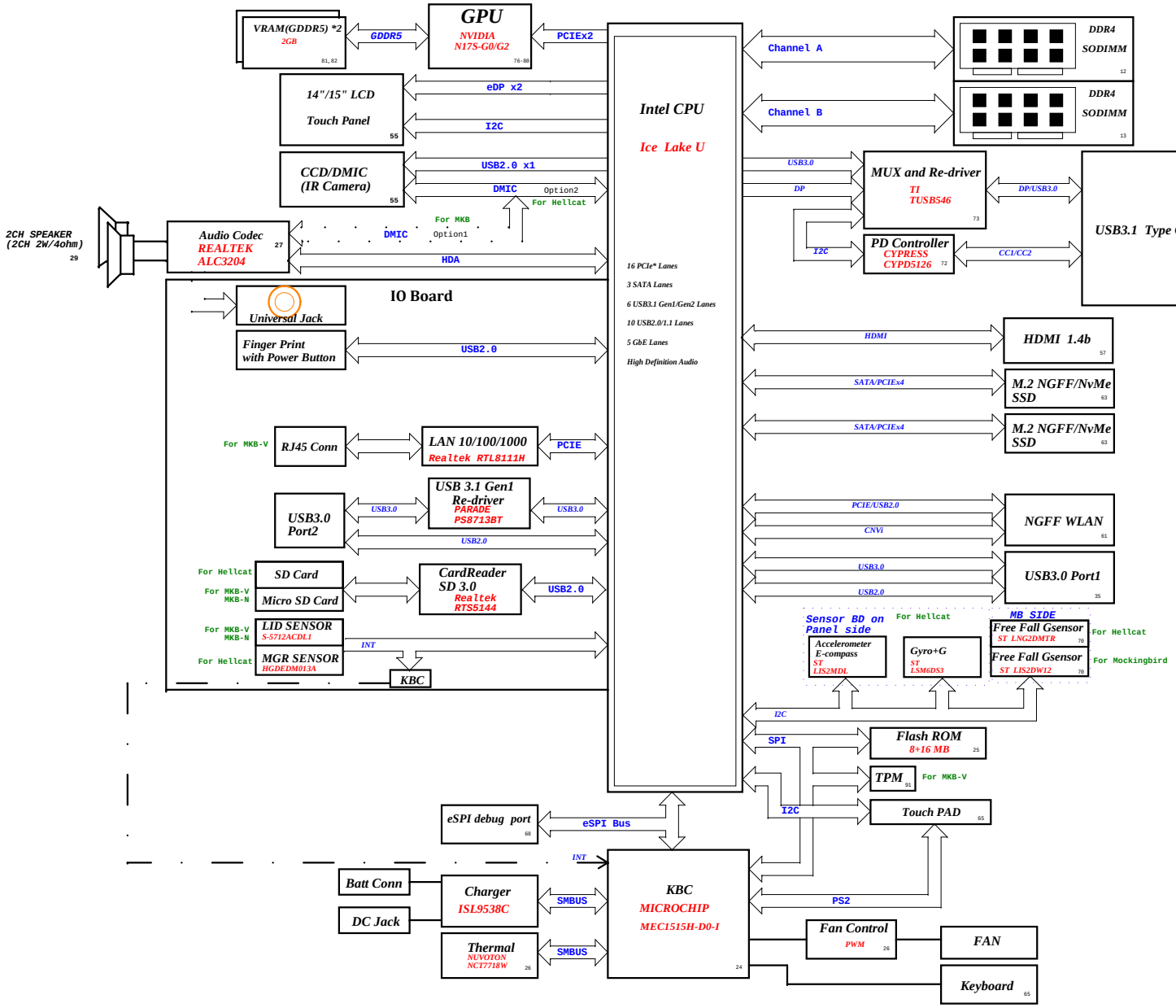
Mockingbird N/V/HellCat CML Block Diagram



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Title: Block Diagram

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Main Func = CPU

[24] PECI_CPU
[22,24,44,46] PROCHOT#_CPU

[99] CPU_JTAG_TCK
[99] CPU_JTAG_TDI
[99] CPU_JTAG_TDO
[99] CPU_JTAG_TMS
[99] CPU_JTAG_TRST#
[99] PCH_JTAG_TCK
[99] CPU_JTAG_PRDY#
[99] CPU_JTAG_PREQ#
[15,99] DBG_PMODE

[15] GPP_E6
[15] GPP_H2

[55] TOUCH_PANEL_PD#
[55] TOUCH_PANEL_DET#

[24,65] TOUCHPAD_INTR#

1D05V_VCCSTG_TERM

R313 51R2J-2-GP — CPU_JTAG_TDO
DY
R311 51R2J-2-GP — CPU_JTAG_PREQ#
R314 51R2J-2-GP
R315 51R2J-2-GP — CPU_JTAG_TDI
CPU_JTAG_TMS

TPAD14-OP-GP
TP301

R312 51R2J-2-GP — CPU_JTAG_TCK
DY
RN304 SRN51J-GP
1 CPU_JTAG_TRST#
2 PCH_JTAG_TCK
R305 49D9R2F-GP — CPU_POPI_RCOMP
R306 49D9R2F-GP — PCH_OPI_RCOMP
DY
RN306 SRN49D9F-GP
1 EDRAM_OPIO_RCOMP
2 CPU_EOPIO_RCOMP

R307 0R2J-2-GP
TOUCHPAD_INTR# — 1TOUCH_PAD_INTR#

CPU1D 4 OF 19

H_CATERR#	J4	CATERR#	
PECI_CPU	CD5	PECI	
PROCHOT#_CPU_R	C3	PROCHOT#	
THERMTRIP#_CPU	E3	THRMTRIP#	
CPU_POPI_RCOMP	CJ41	PROC_POPIRCOMP	
PCH_OPI_RCOMP	DU3	PCH_OPIRCOMP	
EDRAM_OPIO_RCOMP	A14	RSVD_25	
CPU_EOPIO_RCOMP	B14	RSVD_26	
DBG_PMODE	DL15	DBG_PMODE	
GPP_E3	DV11	GPP_E3/CPU_GP0	
TOUCH_PANEL_PD#	DT11	GPP_E7/CPU_GP1	
TOUCH_PAD_INTR#	CR38	GPP_B3/CPU_GP2	
TOUCH_PANEL_DET#	CR39	GPP_B4/CPU_GP3	
GPP_E6	DT12	GPP_E6	
GPP_H2	DJ38	GPP_H2/CNV_BT_I2S_SDO	
	DL38	GPP_H19/TIME_SYNC0	

PROC_TCK	P3	CPU_JTAG_TCK	
PROC_TDI	K5	CPU_JTAG_TDI	
PROC_TDO	K3	CPU_JTAG_TDO	
PROC_TMS	P4	CPU_JTAG_TMS	
PROC_TRST#	N1	CPU_JTAG_TRST#	
PCH_TRST#	N5		
PCH_TCK	R5	PCH_JTAG_TCK	
PCH_TDI	K1		
PCH_TDO	K2		
PCH_TMS	N3		
PCH_JTAGX	N2		
PROC_PRDY#	P6	CPU_JTAG_PRDY#	
PROC_PREQ#	M6	CPU_JTAG_PREQ#	

ICE-LAKE-U-GP-U

1D05V_VCCSTG_TERM
R302 1KR2F-3-GP
PROCHOT#_CPU — R303 499R2F-GP — PROCHOT#_CPU_R

1D05V_VCCST
R304 1KR2F-3-GP — THERMTRIP#_CPU
R309 49D9R2F-GP — H_CATERR#

3D3V_S0
R301 100KR2J-1-GP
TOUCH_PANEL_DET#

1: non touch
0: touch

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Title: CPU (THML/JTAG)

Size	Document Number	Rev
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Main Func = CPU

eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P
[24] L_BKLT_EN
[55] EDP_VDD_EN
[55] L_BKLT_CTRL
[55] eDP_HPD_CPU

HDMI

[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N2
[57] HDMI_DDI_TX_P3
[57] HDMI_DDI_TX_N3
[57] CPU_DISP_HPDB
[57] CPU_DPB_CTRL_CLK
[57] CPU_DPB_CTRL_DATA

DP for Type-C Mux

[73] DP2_DDI_TX_P0
[73] DP2_DDI_TX_N0
[73] DP2_DDI_TX_P1
[73] DP2_DDI_TX_N1
[73] DP2_DDI_TX_P2
[73] DP2_DDI_TX_N2
[73] DP2_DDI_TX_P3
[73] DP2_DDI_TX_N3

DisplayPort AUX

[73] DP2_AUX_CPU_P
[73] DP2_AUX_CPU_N

[76] DGPU_HOLD_RST#

[72,73] DP1_HPD_CPU

[15] GPP_D12
[15] GPP_D10
[65] KB_DET#
[66] USB_OC1#

CPU1A — 1 OF 19

eDP_TX_CPU_N0 Y5 — DDIA_TXN_0
eDP_TX_CPU_P0 Y3 — DDIA_TXP_0
eDP_TX_CPU_N1 Y1 — DDIA_TXN_1
eDP_TX_CPU_P1 Y2 — DDIA_TXP_1
V2 — DDIA_TXN_2
V1 — DDIA_TXP_2
V3 — DDIA_TXN_3
V5 — DDIA_TXP_3

eDP_AUX_CPU_N W4 — DDIA_AUX_N
eDP_AUX_CPU_P W3 — DDIA_AUX_P

HDMI_DDI_TX_N2 AE3 — DDIB_TXN_0
HDMI_DDI_TX_P2 AE5 — DDIB_TXP_0
HDMI_DDI_TX_N1 AE2 — DDIB_TXN_1
HDMI_DDI_TX_P1 AE1 — DDIB_TXP_1
HDMI_DDI_TX_N0 AC5 — DDIB_TXN_2
HDMI_DDI_TX_P0 AC3 — DDIB_TXP_2
HDMI_DDI_TX_N3 AC1 — DDIB_TXN_3
HDMI_DDI_TX_P3 AC2 — DDIB_TXP_3

AD3 — DDIB_AUX_N
AD4 — DDIB_AUX_P

DP15 — GPP_E22/DDPA_CTRLCLK/PCIE_LNK_DOWN
DJ17 — GPP_E23/DDPA_CTRLDATA/BK4/SBK4

CPU_DPB_CTRL_CLK DL40 — GPP_H16/DDPB_CTRLCLK
CPU_DPB_CTRL_DATA DP42 — GPP_H17/DDPB_CTRLDATA

DL17 — GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
DK17 — GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD
[15] TBT_LSX0_RXD

DN17 — GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
DP17 — GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD
[15] TBT_LSX1_RXD

DK34 — GPP_D9/ISH_SPI_CS_N/DDP3_CTRLCLK/GSPI2_CS0_N/TBT_LSX2_TXD
GPP_D10 DL34 — GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK/TBT_LSX2_RXD

DN33 — GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO/TBT_LSX3_TXD
GPP_D12 DL33 — GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI/TBT_LSX3_RXD

eDP_HPD_CPU DW11 — GPP_E14/DPPE_HPDA/DISP_MISCA
CPU_DISP_HPDB CV42 — GPP_A18/DDSP_HPDB/DISP_MISCB
DP1_HPD_CPU_R CV39 — GPP_A19/DDSP_HPD1/DISP_MISC1
CY43 — GPP_A20/DDSP_HPD2/DISP_MISC2
USB_OC1# CR41 — GPP_A14/USB_OC1_N/DDSP_HPD3/DISP_MISC3
USB_OC2# CT41 — GPP_A15/USB_OC2_N/DDSP_HPD4/DISP_MISC4
DGPU_HOLD_RST# DV14 — GPP_E17

EDP_VDD_EN DN21 — EDP_VDDEN
L_BKLT_EN DL19 — EDP_BKLTEN
L_BKLT_CTRL DU19 — EDP_BKLTCTL
J3 — RSVD_1

TPAD14-OP-GP TP409 — DISP_UTILS_DSI_DE_TE1 — D2 — DISP_UTILS
R401 150R2F-1-GP — DISP_RCOMP — R2 — DISP_RCOMP

ICE-LAKE-U-GP-U

TCP0_TX_N0 BB5 — DP2_DDI_TX_N0
TCP0_TX_P0 BB6 — DP2_DDI_TX_P0
TCP0_TX_N1 AV6 — DP2_DDI_TX_N1
TCP0_TX_P1 AV5 — DP2_DDI_TX_P1
TCP0_TXRX_N0 BH2 — DP2_DDI_TX_N2
TCP0_TXRX_P0 BH1 — DP2_DDI_TX_P2
TCP0_TXRX_N1 BF1 — DP2_DDI_TX_N3
TCP0_TXRX_P1 BF2 — DP2_DDI_TX_P3

AY5 — DP2_AUX_CPU_N
TCP0_AUX_N AY6 — DP2_AUX_CPU_P
TCP0_AUX_P

TCP1_TX_N0 AR5
TCP1_TX_P0 AR6
TCP1_TX_N1 AL5
TCP1_TX_P1 AL3
TCP1_TXRX_N0 BD2
TCP1_TXRX_P0 BD1
TCP1_TXRX_N1 BB1
TCP1_TXRX_P1 BB2

TCP1_AUX_N AN3
TCP1_AUX_P AN5

TCP2_TX_N0 BF6
TCP2_TX_P0 BF5
TCP2_TX_N1 BJ5
TCP2_TX_P1 BJ6
TCP2_TXRX_N0 BL1
TCP2_TXRX_P0 BL2
TCP2_TXRX_N1 BM2
TCP2_TXRX_P1 BM1

TCP2_AUX_N BG6
TCP2_AUX_P BG5

TCP3_TX_N0 BP6
TCP3_TX_P0 BP5
TCP3_TX_N1 BV5
TCP3_TX_P1 BV6
TCP3_TXRX_N0 BR1
TCP3_TXRX_P0 BR2
TCP3_TXRX_N1 BT2
TCP3_TXRX_P1 BT1

TCP3_AUX_N BT6
TCP3_AUX_P BT5

R402 150R2F-1-GP
AY1 TCRCOMP_DN
AY2 TCRCOMP_DP
TC_RCOMP_N
TC_RCOMP_P

CT38 GPP_A17
CV43 3.3V_CAM_EN
CV41 KB_DET#
GPP_A17/DISP_MISCC
GPP_A21
GPP_A22

TP403 TPAD14-OP-GP
TP404 TPAD14-OP-GP

NOTE:
"eDP_HPD_CPU"
"eDP_VDDEN_CPU"
PD 100K to LCD side

3D3V_S0 — HDMI
RN402 SRN2K2J-1-GP
CPU_DPB_CTRL_DATA
CPU_DPB_CTRL_CLK

DGPU_HOLD_RST# — R420 10KR2J-3-GP — OPS

3D3V_S0 — R419 10KR2J-3-GP — KB_DET#

DP1_HPD_CPU_R — R403 100KR2J-1-GP

3D3V_S5_PCH
R421 10KR2J-3-GP — USB_OC1#
R422 10KR2J-3-GP — USB_OC2#

Add RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH — R406 10KR2J-3-GP — RTC_RST
3D3V_S5_PCH — R405 10KR2J-3-GP — RTC_RST

Q401
CPU_DP_HPD_P
DP1_HPD_CPU_R
DP1_HPD_CPU
RTC_RST
common part
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

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Title	CPU (DDI/EDP/TBT/TPC/)	
Size A3	Document Number MOCKINGBIRD_ICL	Rev SA
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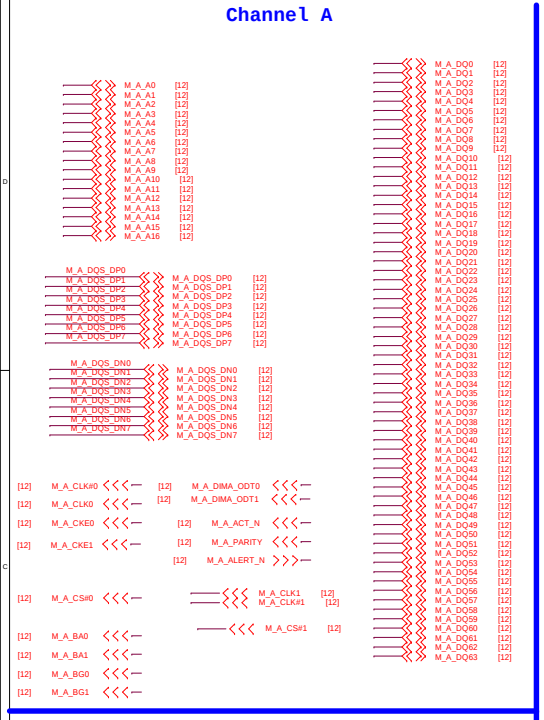
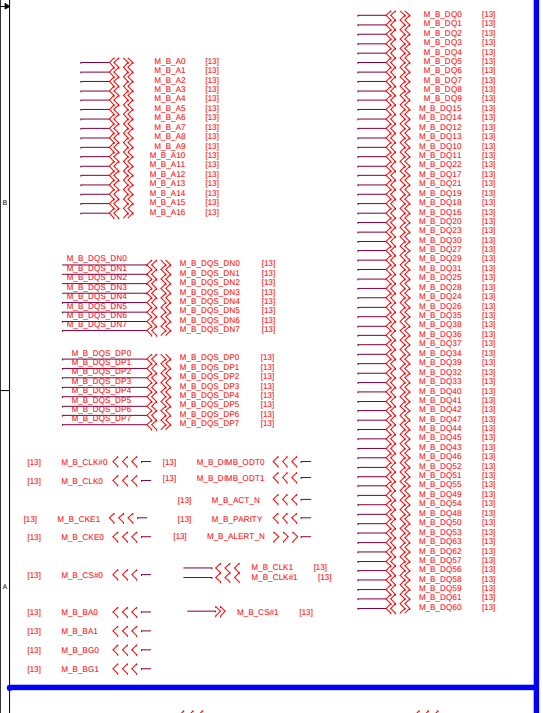
DDR4 ball type: Non-Interleaved Type

Channel A



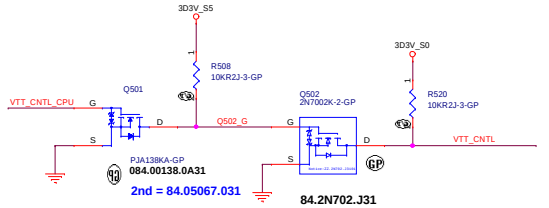
Channel B

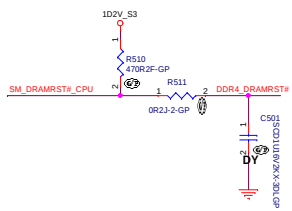


[12] V_SM_VREF_CNTA
[13] V_SM_VREF_CNTB
[51] VTT_CNTL
[12,13] DDR4_DRAMRST#

CPU1B

CPU1C





Title: CPU (DDR)

Size	Document Number	Rev
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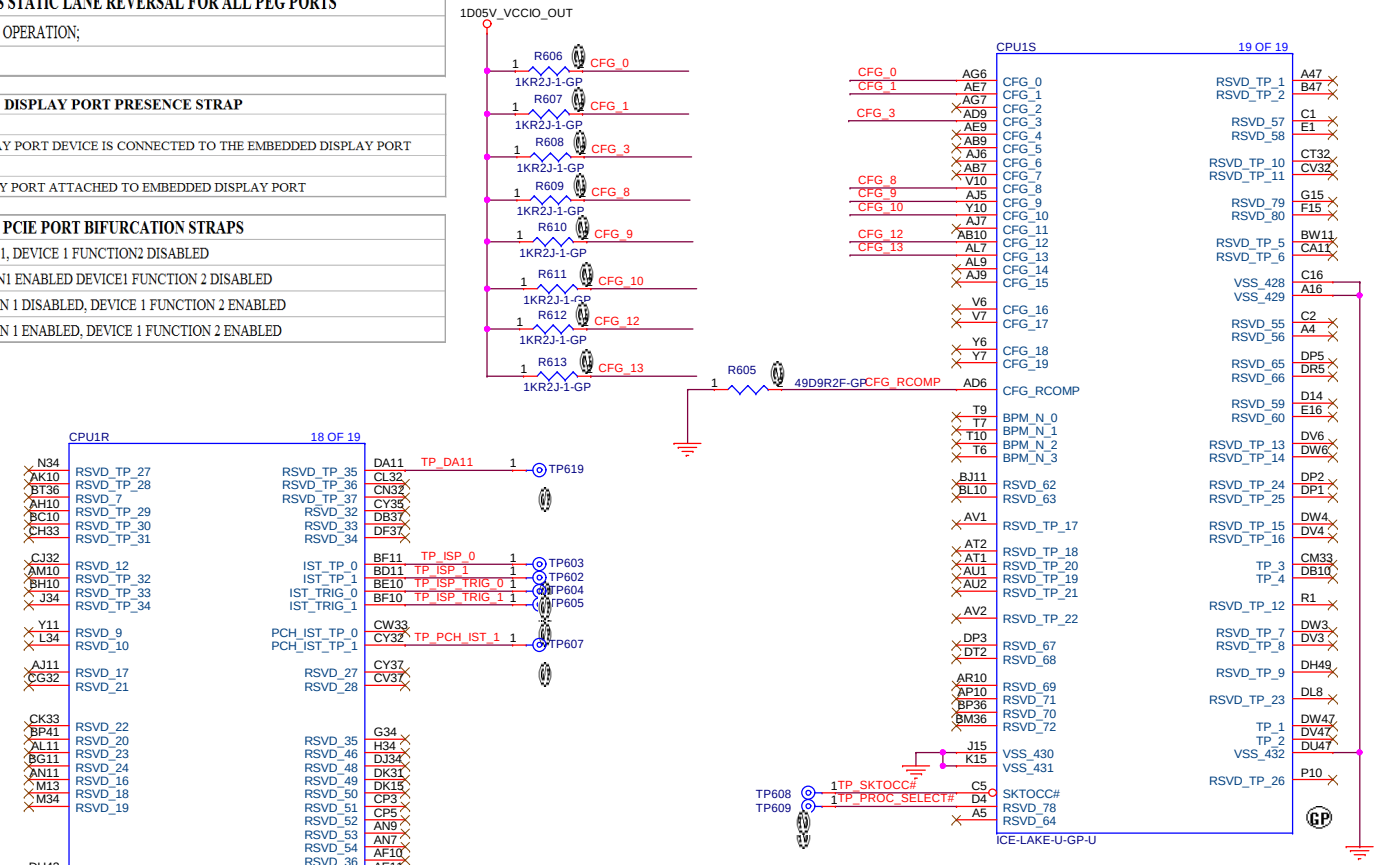
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION;
	0: LANE REVERSAL

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED
	AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1: DISABLED
	NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
	10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
	01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
	00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED



Platform Workaround:

- Pull-up CFG[0, 1, 3, 8, 9, 10, 12, 13] signals to VCCIO_OUT
- Different configuration options:
  1. Add 1K Ohm pull-up resistors to each of the CFG[0, 1, 3, 8, 9, 10, 12, 13] signals
  2. Tie all eight CFG[0, 1, 3, 8, 9, 10, 12, 13] signals together with a single 100 Ohm pull-up resistor; only use this option when CFG signals are not routed to MIPI60 debug connector
  3. Use 270 Ohm resistor to pull up 3 or 4 CFG signals together through a single resistor, and/or 470 Ohm resistor to pull up 2 CFG signals through a single resistor; only use this option when CFG signals are not routed to MIPI60 debug connector

Table 5-76. CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall.	Pull Up	1K Ohm
CFG1,8,9,10,12,13	RSVD	Pull Up	1K Ohm
CFG2,3,5,6,7,11,14,15	RSVD	No termination	N/A
CFG4	CFG[4]: eDP enable: — 1 = Disabled. — 0 = Enabled.	Pull Down	1K Ohm
Note: Refer Chapter 13, "Platform Debug and Test Hooks" for debug connectivity guidelines.			

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Title: CPU (CFG/IST)

Size: A3 | Document Number: MOCKINGBIRD_ICL | Rev: SA

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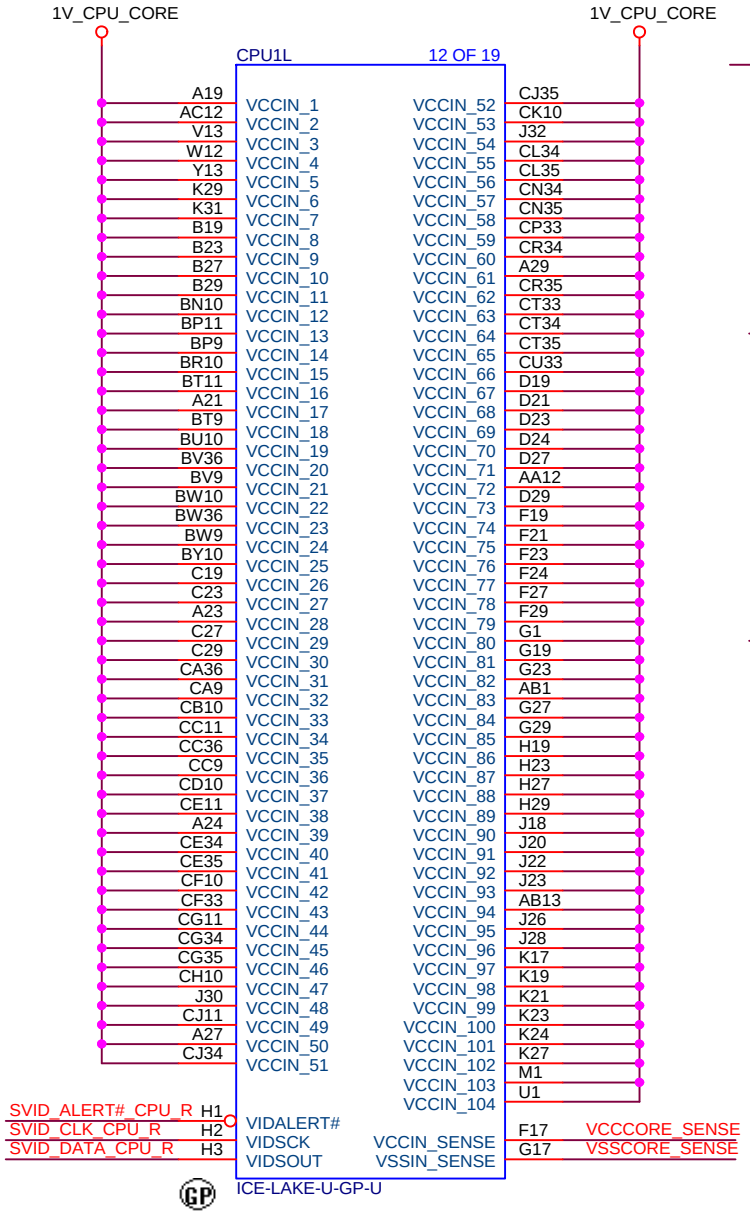
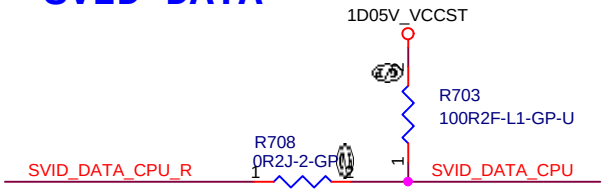
Main Func = CPU

[46] SVID_ALERT#_CPU
[46] SVID_CLK_CPU
[46] SVID_DATA_CPU

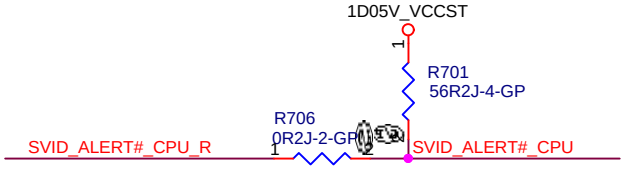
[46] VCCCORE_SENSE
[46] VSSCORE_SENSE



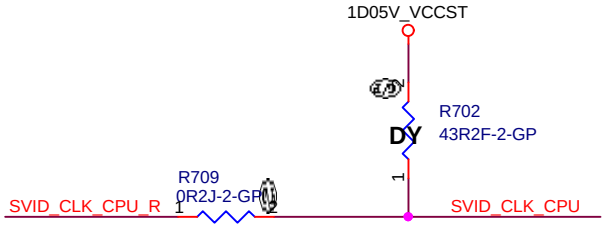
SVID DATA



SVID ALERT

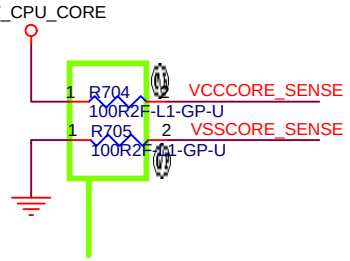


SVID CLOCK



Layout note:

3.Length matchin 25mil, and close SOC in 2inch "



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title: CPU (VCCIN/VID)		
Size: A4	Document Number: MOCKINGBIRD_ICL	Rev: SA
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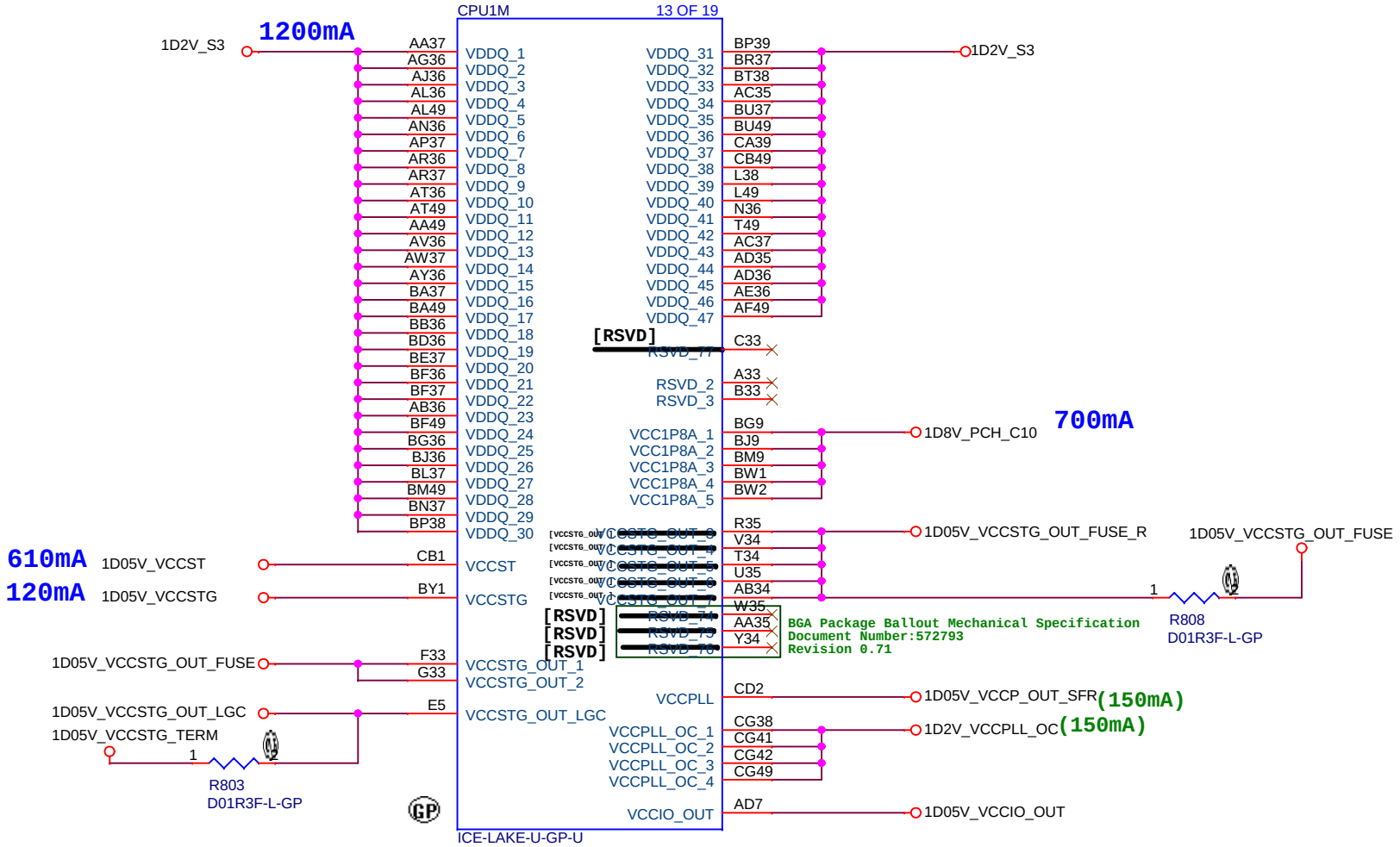
Main Func = CPU



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Title: **CPU (VDDQ/VCC/VCCST/VCCSTG)**

Size	Document Number	Rev
A4	MOCKINGBIRD_ICL	SA

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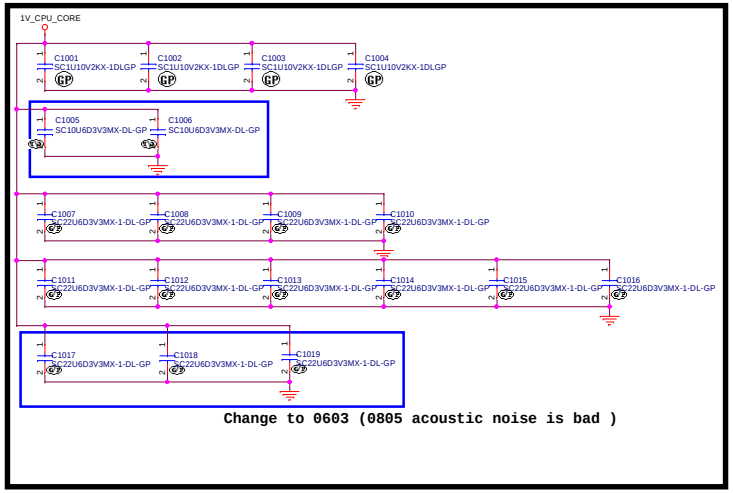
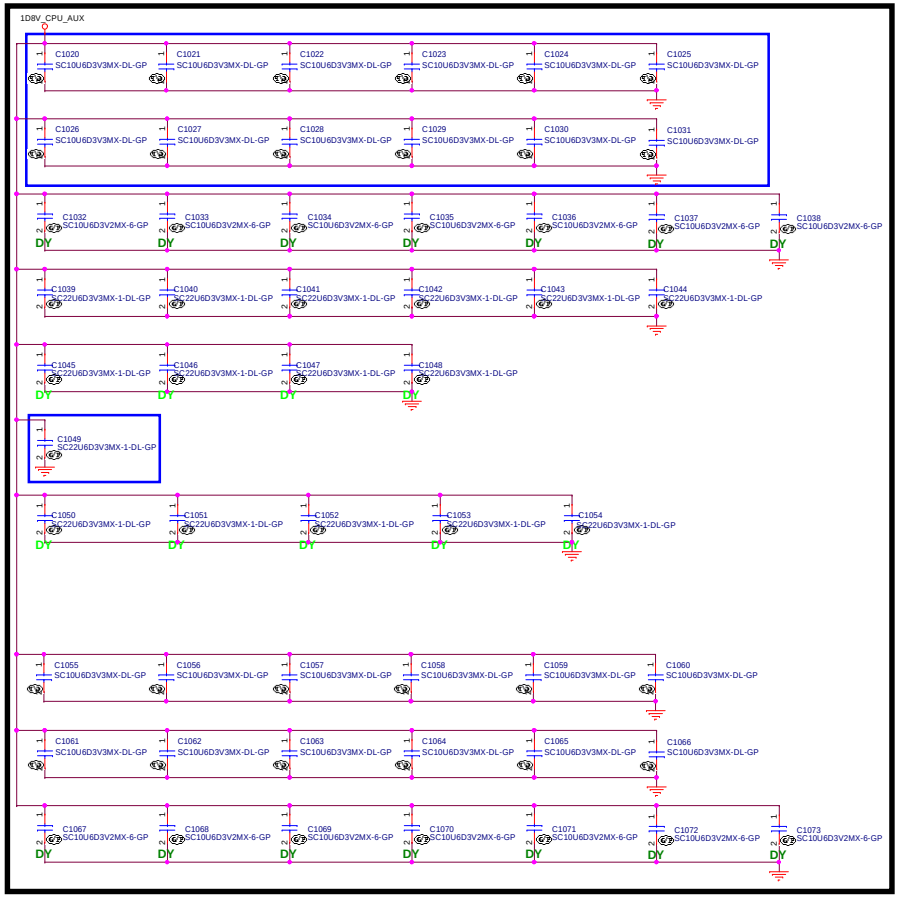
Main Func = CPU



Change to 0603 (0805 acoustic noise is bad)

Decoupling Requirements for Ice Lake U Processor for VCCIN

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCIN	4x 1uF 0402		Place as close as possible to CP33, and CT33.
	2x 1uF 0402		Place closest possible to CA36 *Place for ICL U43e only.*
	1x 1uF 0402		Place as close as possible to BU10 *Place for ICL U43e only.*
		2x 10uF 0402	Place as close as possible to each U1 and AB1.
		4x 22uF 0603	Place closest possible to package near heat sink mounting hole.
		6x 22uF 0603	Place closest possible to package along the plane breakout as in Figure 10-5.
		2x 22uF 0603	Place closest possible to package along the plane breakout as in Figure 10-5. *Place for ICL U43e only.*
		1x 47uF 0805	Place closest possible to package along the plane breakout. *Place for ICL U43e only.*
		3x 47uF 0805	Place closest possible to package near heat sink mounting hole.
		1x 47uF 0805	Place closest possible to package near heat sink mounting hole. *Place for ICL U43e only.*
		2x 330uF 7343	Refer to the placement guideline in Figure 10-5.



Decoupling Requirements for Ice Lake U Processor for VCCIN_AUX

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCIN_AUX	12x 10uF 0402		Place them as directly below the BGAs as possible .
	7x 0402 (placeholder)		
		6x 22uF 0603	Place them close to VR.
		4x 0603 (placeholder)	
		1x 47uF 0805	Place them as close to the VR as possible.
		5x 0805 (placeholder)	
		2x 330uF 7343	Place them close to VR.
		12x 10uF 0402	Place them close to the BGAs on the primary side.
		7x 0402 (placeholder)	

Notes:

1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-6 for decoupling capacitor placements.

<Core Design>

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Title: CPU (CORE Power Cap1)

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

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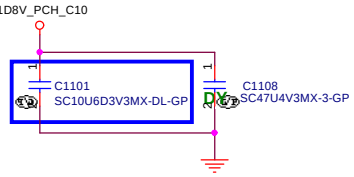
Main Func = CPU

1D8V_PCH_C10

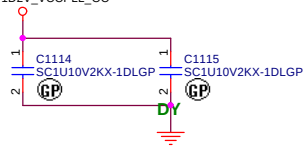


Decoupling Requirements for Ice Lake U Processor for VCC1P8A

Domain	Backside cap	Primary side cap	Placement guideline[2]
VCC1P8A		1x 10uF 0402	Place as close to BGA as possible.
		1x 0603 (placeholder)	Place this post power gate path to BGAs.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-8 for decoupling capacitor placements.

1D2V_VCCPLL_OC

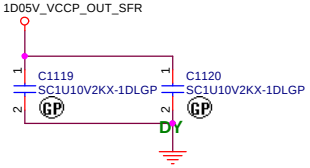


Decoupling Requirements for Ice Lake U Processor for VCCPLL_OC

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCPLL_OC		1x 1uF 0402	Place as close as possible to the package.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-12 for decoupling capacitor placements.

1D05V_VCCP_OUT_SFR

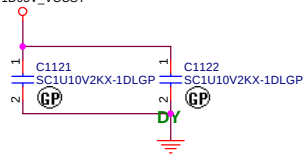


Decoupling Requirements for Ice Lake U Processor for VCCPLL

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCPLL		1x 1uF 0402	Place as close to the package as possible.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-14 for decoupling capacitor placements.

1D05V_VCCST

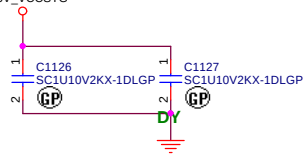


Decoupling Requirements for Ice Lake U Processor for VCCST

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCST		1x 1uF 0402	Place as close to the package as possible.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-16 for decoupling capacitor placements.

1D05V_VCCSTG

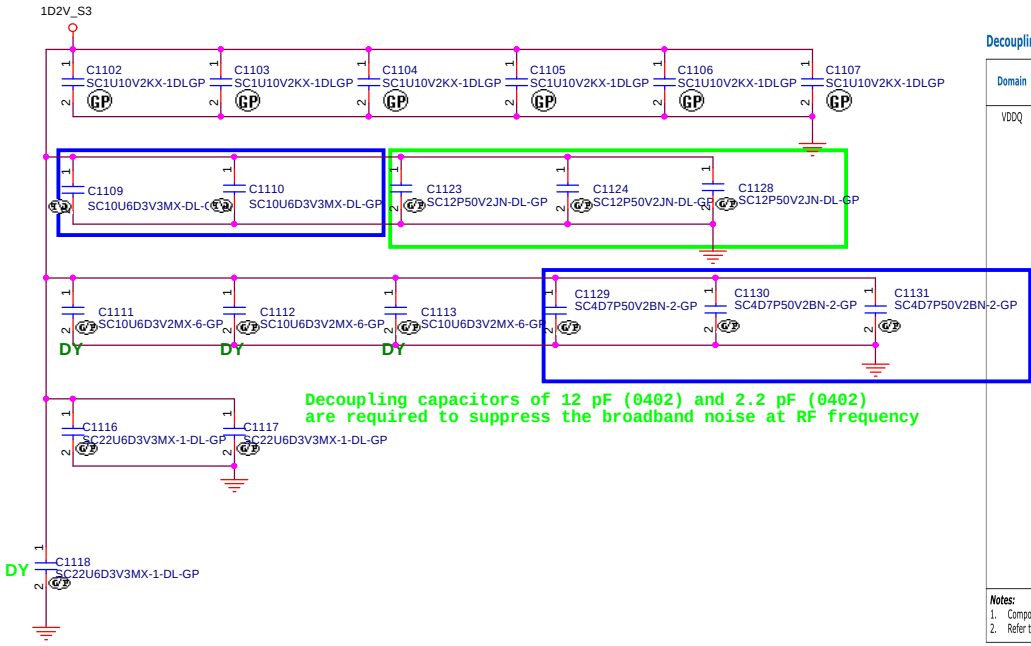


Decoupling Requirements for Ice Lake U Processor for VCCSTG

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCSTG		1x 1uF 0402	Place as close to the package as possible.
		1x 0402 (placeholder)	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-18 for decoupling capacitor placements.

1D2V_S3



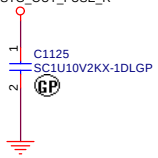
Decoupling capacitors of 12 pF (0402) and 2.2 pF (0402) are required to suppress the broadband noise at RF frequency

Decoupling Requirements for Ice Lake U Processor for VDDQ

Domain	Backside cap	Primary side cap	Placement guideline [3]
VDDQ	6x 1uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 10uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	3x 0402 (placeholder)		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 22uF 0603		Place after the TOP DDR signal breakout. These should not be omitted on SODIMM designs, and can be removed only in Memory Down designs when the following conditions are met: 1) DRAM's are soldered down, so their decoupling is shared with the SoC. 2) DRAM's and SoC VDDQ plane copper is shared between both directly (no shorting resistors, pads or similar in the middle). 3) DRAM's are placed close to the SoC allowing that at least 5x10uF capacitors of the DRAM decoupling is within a 30mm radius from SoC Edge.
	1x 0603 (placeholder)		Place after the TOP DDR signal breakout.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-10 for decoupling capacitor placements.

1D05V_VCCSTG_OUT_FUSE_R



<Core Design>

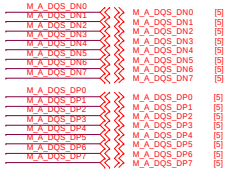
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

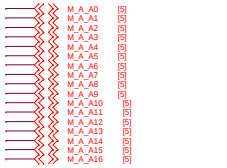
Title: CPU (Power Cap2)

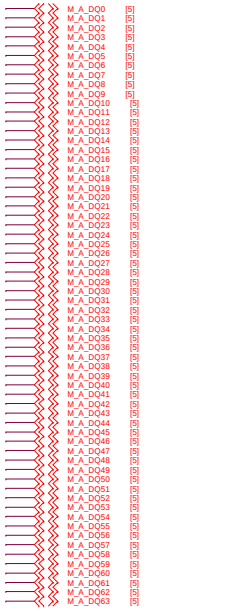
Size: A3 | Document Number: MOCKINGBIRD_ICL | Rev: SA

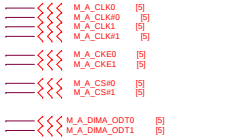
Date: Tuesday, September 17, 2019 | Sheet 11 of 106

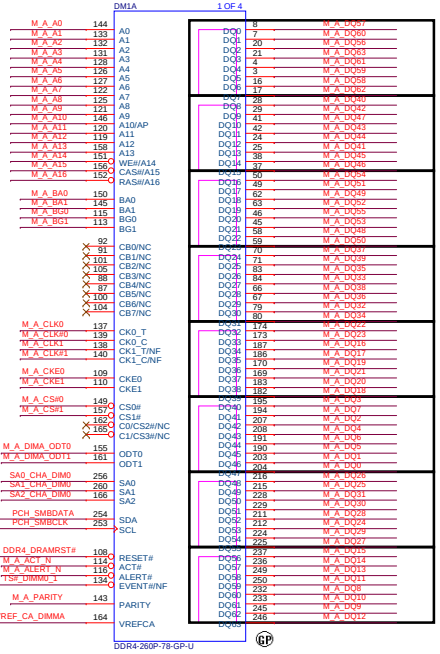
Main Func = MEMORY











M_A_DQ[56:63]

M_A_DQ[40:47]

M_A_DQ[48:55]

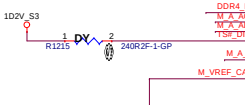
M_A_DQ[32:39]

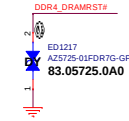
M_A_DQ[16:23]

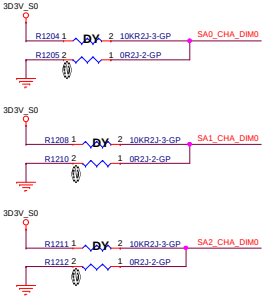
M_A_DQ[0:7]

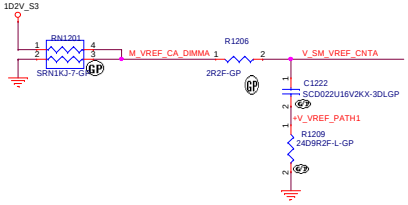
M_A_DQ[24:31]

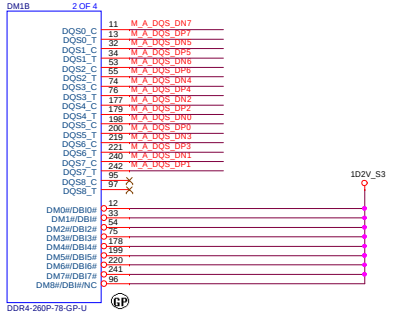
M_A_DQ[8:15]

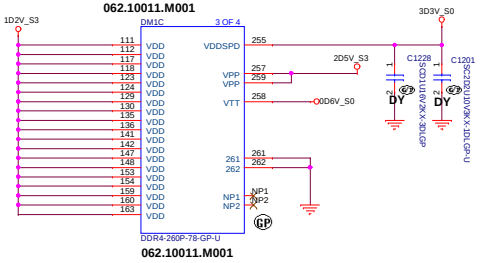


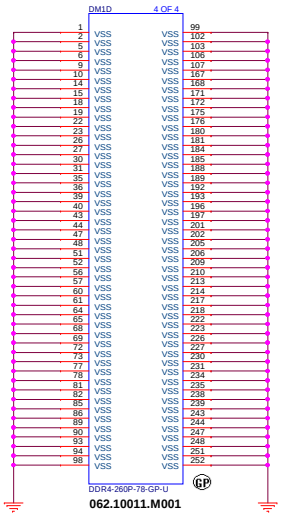


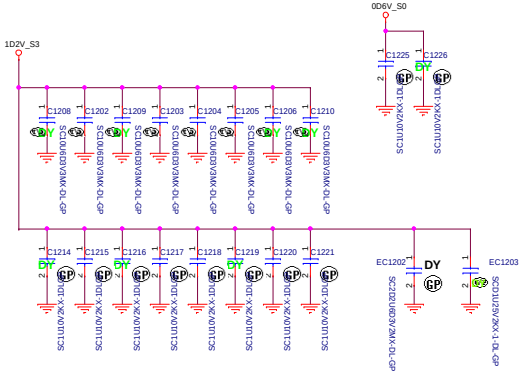


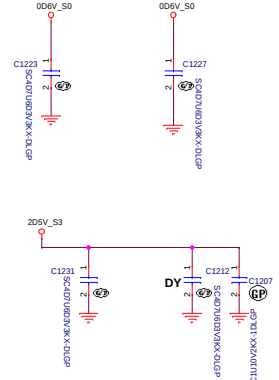




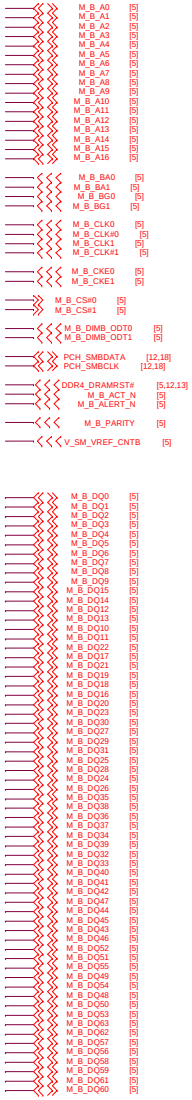


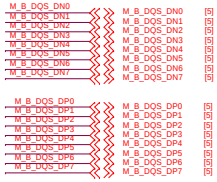


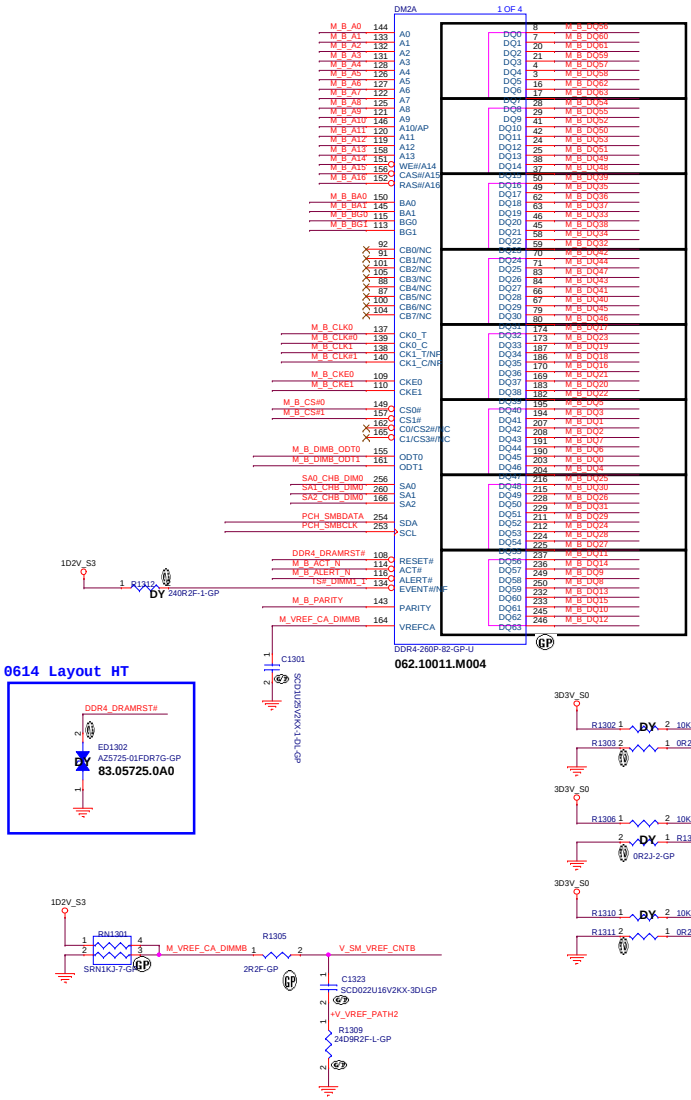


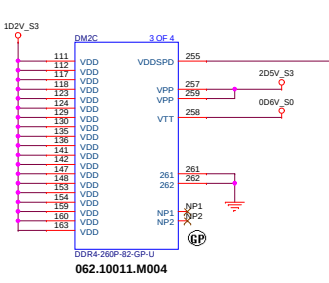


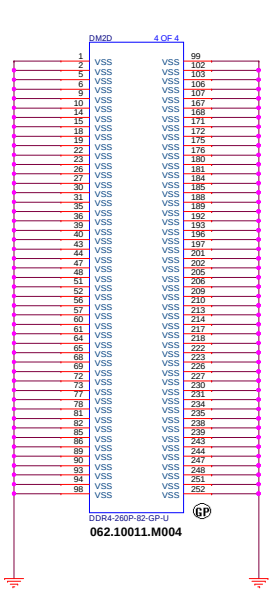
Main Func = MEMORY

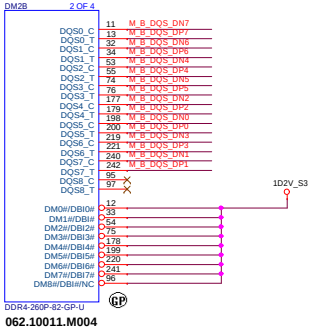


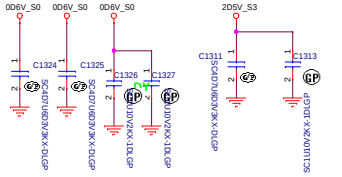


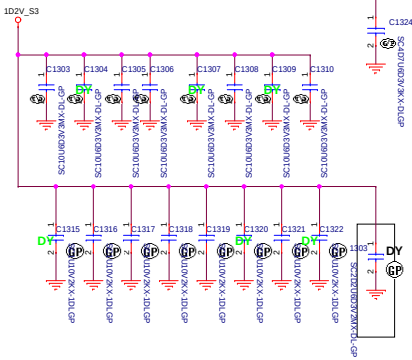












0614 Layout HT

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
A2	MOCKINGBIRD_ICL	SA

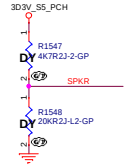
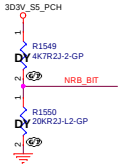
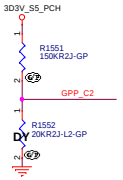
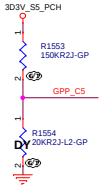
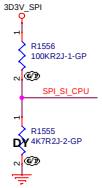
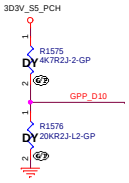
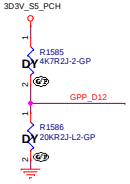
Date: Tuesday, September 17, 2019 Sheet 13 of 106

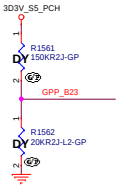
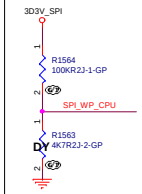
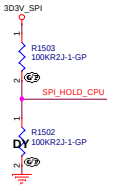
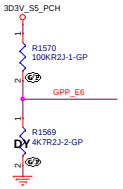
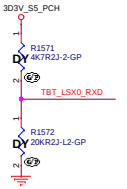
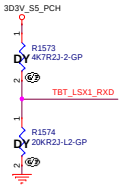
Main Func = PCH

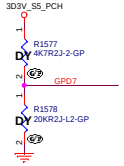
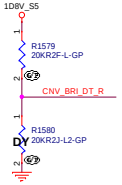
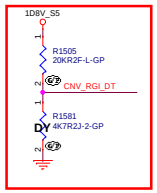
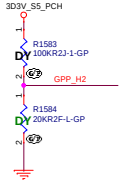
[20,27] SPKR
[20] NRB_BIT
[18] GPP_C2
[18] GPP_C5
[18] SPI_SI_CPU

[20] GPP_B23
[18] SPI_WP_CPU
[18] SPI_HOLD_CPU
[19] HDA_SDO
[3] GPP_E6
[4] TBT_LSX0_RXD
[4] TBT_LSX1_RXD

[17] GPD7
[21,61] CNV_BRI_DT_R
[21,61] CNV_RGI_DT
[3] GPP_H2
[4] GPP_D10
[4] GPP_D12

Description	Top Swap Override	No Reboot	TLS Confi-dentiality	eSPI Disable	Reserved	DDP3 I2C/TBT LSX #2/ BSSB-LS #2 pins VCC configuration	DDP4 I2C/TBT LSX #3/ BSSB-LS #3 pins VCC configuration
GPIO	GPP_B14 / SPKR / TIME_SYNC1 / GSPI0_CS#	GPP_B18	GPP_C2	GPP_C5	SPI0_MOSI	GPP_D10	GPP_D12
							
LOW	Disable (Default)	Disable (Default)	Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)	Enable eSPI. (Default)		DDP3 I2C/TBT LSX #2/BSSB_LS #2 pins at 1.8V	DDP4 I2C/TBT LSX #3/BSSB_LS #3 pins at 1.8V
HIGH	Enable	Enable	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.	Disable eSPI.	This strap should sample HIGH.	DDP3 I2C/TBT LSX #2/BSSB_LS #2 pins at 3.3V	DDP4 I2C/TBT LSX #3/BSSB_LS #3 pins at 3.3V
	20 K± 30% internal pull-down.						

Description	CPUNSSC Clock Frequency	Reserved	Reserved	Flash Descriptor Security Override	Reserved	DDP1 I2C /TBT LSX #0 / BSSB-LS #0 pins VCC configuration	DDP2 I2C/TBT LSX #1/ BSSB-LS #1 pins VCC configuration
GPIO	GPP_B23 / SML1ALERT# / PCHHOT# / GSPI1_CS1#	SPI0_IO2	SPI0_IO3	GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO	GPP_E6	GPP_E19 / DDP1_CTRLDATA / CNV_BT_IF_SELECT / BSSB_LS0_RX	GPP_E21 / DDP2_CTRLDATA / BSSB_LS1_TX
							
LOW	38.4 MHz clock (direct from crystal) (default)			Enable security measures defined in the Flash Descriptor. (Default)		1.8V	1.8V
HIGH	19.2 MHz clock (from internal divider)	This strap should sample HIGH	This strap should sample HIGH	Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.	This strap should sample HIGH.	3.3V	3.3V
	20 K± 30% internal pull-down.			20 K± 30% internal pull-down.			20 K± 30% internal pull-down.

Description	Reserved	Reserved	XTAL Frequency Selection	M.2 CNVi Mode Select	eSPI Flash Sharing Mode	ITP_PMODE
GPIO	ITP_PMODE	GPD7	GPP_F0 / CNV_BRI_DT / UART0_RTS#	GPP_F2 / CNV_RGI_DT / UART0_TXD	GPP_H2 / CNV_BT_I2S_SDI/ MODEM_CLKREQ	
						
LOW		This strap should sample LOW.	38.4 MHz (default)	Integrated CNVi enabled.	Master Attached Flash Sharing (MAFS) is enabled. (Default)	Reserved
HIGH	This strap should sample high.		24MHz	Integrated CNVi disabled.	Slave Attached Flash Sharing (SAFS) is enabled.	Reserved
	20 K± 30% internal pull-up	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.		20 K± 30% internal pull-down.	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

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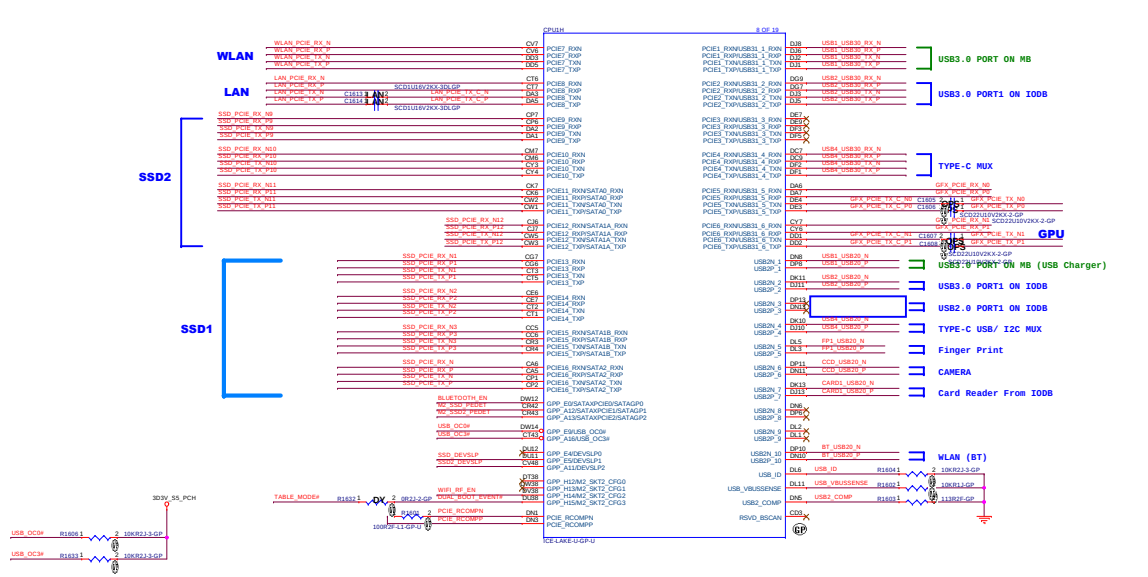

High Speed I/O (HSIO) Lane Multiplexing in Ice Lake U PCH-LP																
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1 / Gen2 #1	USB3.1 Gen1 / Gen2 #2	USB3.1 Gen1 / Gen2 #3	USB3.1 Gen1 / Gen2 #4	USB3.1 Gen1 / Gen2 #5	USB3.1 Gen1 / Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
PCIe*Remap Support	No Support				No Support						Yes				Yes	

CY20 Port Mapping											
Mockingbird N	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	NC	M.2 SSD2	M.2 SSD1		
Mockingbird V	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	LAN	M.2 SSD2	M.2 SSD1		
Hellcat 14	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	NC	NC	M.2 SSD1		
Hellcat 15	MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	dGPU	WLAN	NC	NC	M.2 SSD1		

USB2.0 (10 Ports)										
USB2 #1	USB2 #2	USB2 #3	USB2 #4	USB2 #5	USB2 #6	USB2 #7	USB2 #8	USB2 #9	USB2 #10	
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT	
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT	
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT	
MB USB-A 3.1 Gen1	IO USB-A 3.1 Gen1	NC	USB Type-C	Finger Printer	Camera	Card Reader	NC	NC	BT	

DDI Ports Availability for U-Processor Lines					
DDI A [eDP]	DDI B [DP / HDMI]	TCP0 (DDI C) [DP / HDMI]	TCP1 (DDI D) [DP / HDMI]	TCP2 (DDI E) [DP / HDMI]	TCP3 (DDI F) [DP / HDMI]
eDP	HDMI	Type-C DP	NC	NC	NC
eDP	HDMI	Type-C DP	NC	NC	NC
eDP	HDMI	Type-C DP	NC	NC	NC
eDP	HDMI	Type-C DP	NC	NC	NC

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
Custom	MOCKINGBIRD_ICL	SA

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Main Func = PCH

[40,54,55,81] PM_SLP_S3#
[40,51,66] PM_SLP_S4#
[40] SIO_SLP_S0#
[17,24] SYS_PWROK
[24] SIO_PWRBTN#
[24,26] IMVP_VR_ON
[18,64] PM_RSMRST#
[44] AC_IN#
[40] CPU_C10_GATE#
[53] SIO_SLP_SUS#

[15] GPD7
[15] PCH_DPWROK

[17,24] SYS_PWROK

[61,63,66,76,91] PLT_RST#

[24,40,44,46] VCCST_PWRGD

[44,46] PWR_IMVP_PWRGD

[25,53] 3V_5V_PWRGD

CPU1K
11 OF 19
ICE-LAKE-U-GP-U

SIO_SLP_SUS# DM49
SIO_SLP_S5# DF45
PM_SLP_S4# DC49
PM_SLP_S3# DF47
SIO_SLP_A# DM47
SIO_SLP_S0# CL45
SIO_SLP_WLAN# DE49
SIO_SLP_LAN# DN48
RSMRST# DG49
SYS_RESET# DK19
PCH_PLTRST# CM49
DSW_PWROK DR48
PCH_PWROK DN47
SYS_PWROK DP19
INPUT3VSEL DN49
RTC_INTRUDER# DR47

SLP_SUS#
GPD10/SLP_S5#
GPD5/SLP_S4#
GPD4/SLP_S3#
GPD6/SLP_A#
GPP_B12/SLP_S0#
GPD9/SPL_WLAN#
SLP_LAN#
RSMRST#
SYS_RESET#
GPP_B13/PLTRST#
DSW_PWROK
PCH_PWROK
SYS_PWROK
INPUT3VSEL
SPI_VCCIO_SEL

GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_B11/PMCALERT
GPP_H18/CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF_N/CNV_BT_I2S_SDO
WAKE#
GPD_2/LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON
VCCST_OVERRIDE
VCCST_PWRGD
VCCSTPWRGOOD_TCSS
PROCPWRGD
GPD7

CY42 SIO_PWRBTN#
DE46 AC_PRESENT
DH48 PCH_BATLOW#
CL39
DG45 CPU_C10_GATE#
DG40 TPM_PRSNT#
DL45 PCH_PCIE_WAKE#
DE47 LAN_WAKE#
DF48 PM_LANPHY_ENABLE
CE4
CF2 VCCST_PWRGD_R
CE3 VCCSTPWRGOOD_TCSS
CF1 VCORE_PWRGD
DC47 GPD7

90820-SA_James CL39 Remove net TBT_I2C_INT#

TP1702 TP1703 TP1720 TP1707 TP1719

PM_RSMRST# R1774 0R2J-2-GP
3V_5V_PWRGD R1748 0R2J-2-GP DY
PCH_DPWROK_R
IMVP_VR_ON R1743 0R2J-2-GP
PCH_PWROK
SYS_PWROK

3D3V_S0
R1722 100KR2J-1-GP CPU_C10_GATE#
3D3V_S5_PCH
R1723 100KR2J-1-GP AC_PRESENT
R1724 10KR2J-3-GP LAN_WAKE#
R1726 10KR2J-3-GP SYS_RESET#
3D3V_S5_PCH
R1727 1KR2F-3-GP PCH_PCIE_WAKE#
R1728 100KR2J-1-GP SIO_PWRBTN#
3D3V_S5
R1770 10KR2J-3-GP
VCCSTPWRGOOD_TCSS [40]
RTC_AUX_S5
R1718 330KR2J-L1-GP RTC_INTRUDER#
SPI Voltage Configu-ration

3D3V_S5_PCH
non dTPM
R1733 100KR2J-1-GP TPM_PRSNT#
dTPM
R1738 100KR2J-1-GP

R1717 100KR2J-1-GP SYS_PWROK
R1713 10KR2J-3-GP RSMRST#
R1716 10KR2J-3-GP PCH_PWROK
PCH_DPWROK_R
SYS_RESET#
PCH_PLTRST#
EC1701 EC1702 EC1703 EC1704 SCD1U16V2KX-1DLGP DY

3V SELECT STRAP
LOW → 3.3V +/-5%
HIGH → 3.0V +/-5%

3D3V_S5_PCH
R1729 4K7R2J-2-GP DY
INPUT3VSEL
R1730 100KR2J-1-GP
3D3V_S5_PCH
R1725 10KR2J-3-GP
PCH_BATLOW#
R1732 10KR2J-3-GP DY

20190424(EVT)
Reverse R1705, R1739 by Dell Andy
PWR_IMVP_PWRGD R1705 0R2J-2-GP DY IMVP_VR_ON
VCCST_PWRGD R1739 0R2J-2-GP DY PWR_IMVP_PWRGD

90821-SA_James Remove R1763

3D3V_AUX_S5
R1747 100KR2J-1-GP
R1746 10KR2J-3-GP
Q1701
PJT138KA-GP
075.00138.0A7C
3V_5V_POK#
PM_RSMRST# R1702 1KR2J-1-GP
3V_5V_POK_C R1749 0R2J-2-GP
3V_5V_PWRGD
PCH_RSMRST#_R [24]
R1764 100KR2J-1-GP DY
C1710 SCD47U10V2KX-1-GP DY
EC1712 SCD1U16V2KX-3DLGP DY

90821-SA_James R1750 DY
SYS_PWROK R1750 0R2J-2-GP PCH_PWROK
PCH_PLTRST# R1714 0R2J-2-GP PLT_RST#
R1715 100KR2J-1-GP

3D3V_S5_PCH
R1763 100KR2J-1-GP SIO_SLP_S0#
SIO_SLP_SUS# R1752 100KR2J-1-GP DY
PM_SLP_S4# R1753 100KR2J-1-GP DY
PM_SLP_S3# R1754 100KR2J-1-GP
90821-SA_James Remove net SIO_SLP_WLAN#
90821-SA_James Remove R1765

3D3V_AUX_S5
R1737 100KR2J-1-GP PM_RSMRST#_M
Q1702 2N7002KDW-1-GP
common part
75.27002.F7C
D1701 RB520S30-GP AC_IN#
83.R2003.A8M
2nd = 083.52030.008F
AC_PRESENT
PM_RSMRST#

PCH_DPWROK_R R1765 0R2J-2-GP PCH_DPWROK
R1766 100KR2J-1-GP
C1711 SCD1U16V2KX-3DLGP DY

1D05V_VCCST
R1768 1KR2F-3-GP
3D3V_S0
R1769 100KR2J-1-GP DY
VCCST_PWRGD
R1767 60D4R2F-GP
VCCST_PWRGD_R
R1719 47KR2F-GP
C9214 SCD022U16V2KX-3DLGP

SVID Bus
IMVP9 CPU SVID Rails VCCIN
VR_ON
VR_READY
SVID
SoC
Level Shifter
VCCST_PWRGD
CPUPWRGD
Note: VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
PCH_PWROK
PLTRST#
ALL_SYS_PWRGD
OEM Delay (ms)
SYS_PWROK

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: A2
Document Number: MOCKINGBIRD_ICL
Rev: SA
Date: Tuesday, September 17, 2019
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Main Func = PCH

SPI ROM
[24,25,91] SPI_CLK_ROM
[24,25,91] SPI_SI_ROM
[24,25,91] SPI_SO_ROM
[24,25] SPI_WP_ROM
[24,25] SPI_HOLD_ROM
[24,25] SPI_CS_ROM_N0
[24,25] SPI_CS_ROM_N1
[15] SPI_HOLD_CPU

TPM
[91] SPI_CS_CPU_N2
[91] TPM_SPI_IRQ#

WLAN
[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] WLAN_CLKREQ_CPU_N

ESPI
[24,68] ESPI_IO0
[24,68] ESPI_IO1
[24,68] ESPI_IO2
[24,68] ESPI_IO3
[24,68] ESPI_CS#
[24,68] ESPI_RESET#
[24,68] ESPI_CLK

OTHER
[12,13] PCH_SMBCLK
[12,13] PCH_SMBDATA
[12,13] SML0_SMBCLK
[12,13] SML0_SMBDATA
[15] GPP_C2
[15] GPP_C5
[24,61] SUS_CLK
[66] LAN_CLK_CPU_N
[66] LAN_CLK_CPU_P
[66] LAN_CLKREQ_CPU_N
[64] SATA_LED#
[24,25] RTCRST_ON
[15] SPI_SI_CPU
[15] SPI_WP_CPU

GPU
[76] GFX_CLK_CPU_N
[76] GFX_CLK_CPU_P
[76] CLK_PCIE_PEG_REQ#

SSD
[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] SSD_CLKREQ_CPU_N
[63] SSD2_CLK_CPU_P
[63] SSD2_CLK_CPU_N
[63] SSD2_CLKREQ_CPU_N
[17,64] PM_RSMRST#
[24] EC_PCH_SPI_EN

CPU1E 5 OF 19
SPI0_CLK SPI0_MOSI SPI0_MISO SPI0_IO2 SPI0_IO3 SPI0_CS0# SPI0_CS1# SPI0_CS2#
GPP_E11/SPI1_CLK/BK1/SBK1 GPP_E13/SPI1_MOSI/BK3/SBK3 GPP_E12/SPI1_MISO/BK2/SBK2 GPP_E1/SPI1_IO2 GPP_E2/SPI1_IO3 GPP_E10/SPI1_CS_N/BK0/SBK0 GPP_E8/SATALED#/SPI1_CS1#
CL_CLK CL_DATA CL_RST#
GPP_C0/SMBCLK GPP_C1/SMBDATA GPP_C2/SMBALERT#
GPP_C3/SML0CLK GPP_C4/SML0DATA GPP_C5/SML0ALERT#
GPP_C6/SML1CLK/SUSWARN_N/SUSPWRDNACK GPP_C7/SML1DATA/SUSACK#
GPP_A5/ESPI_CLK GPP_A0/ESPI_IO0 GPP_A1/ESPI_IO1 GPP_A2/ESPI_IO2 GPP_A3/ESPI_IO3 GPP_A4/ESPI_CS# GPP_A6/ESPI_RESET#
ICE-LAKE-U-GP-U

Strap Pin
Strap Pin

3D3V_S5_PCH
CPU_SMB_SCL R1804 2.1KR2J-1-GP
CPU_SMB_SDA R1805 2.1KR2J-1-GP
SML0_SMBCLK R1806 499R2F-2-GP
SML0_SMBDATA R1807 499R2F-2-GP
CPU_SMB_SCL_P1 R1810 2.1KR2J-1-GP
CPU_SMB_SDA_P1 R1811 2.1KR2J-1-GP
SPI_CLK_CPU R1813 100KR2J-1-GP

3D3V_S0 R1808 10KR2J-3-GP SATA_LED#

If support TPM change to 5R

RN1802 SRN1KJ-7-GP Q1802 2N7002KDW-1-GP
CPU_SMB_SDA PCH_SMBDATA
CPU_SMB_SCL PCH_SMBCLK
75.27002.F7C

PCH_ESPI_CLK R1834 33R2F-3-GP ESPI_CLK
PCH_ESPI_IO0 R1835 0R2J-2-GP ESPI_IO0
PCH_ESPI_IO1 R1836 0R2J-2-GP ESPI_IO1
PCH_ESPI_IO2 R1837 0R2J-2-GP ESPI_IO2
PCH_ESPI_IO3 R1838 0R2J-2-GP ESPI_IO3
Intel requst set as PDG .

ESPI_CLK RC1801 DY SC27P50V2JN-2-GP
RF Reserve

XTL_32K_X1_CPU R1847 0R2J-2-GP
XTL_32K_X2_CPU R1849 0R2J-2-GP
XTL_32K_X1_CPU_R R1844 10MR2J-2-GP
XTL_32K_X2_CPU_R X1803 XTAL-32D768KHZ-8G-GP
C1810 SC15P50V2JN-DL-GP
C1809 SC12P50V2JN-DL-GP
082.30003.0191

	C1810(Cg)	C1809(Cd)
EPSON 082.30003.0191	15pF	12pF
SEIKO 082.30003.0301	12pF	15pF
NDK 082.30003.0221	15pF	12pF

3D3V_S0 RN1805 SRN10KJ-6-GP
LAN_CLKREQ_CPU_N WLAN_CLKREQ_CPU_N SSD2_CLKREQ_CPU_N
R1801 10KR2J-3-GP SSD_CLKREQ_CPU_N

CPU1J 10 OF 19
GPU
GFX_CLK_CPU_N CJ3
GFX_CLK_CPU_P CJ5
CLK_PCIE_PEG_REQ# DK33
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_D5/SRCCLKREQ0#

WLAN
WLAN_CLK_CPU_N CL2
WLAN_CLK_CPU_P CL1
WLAN_CLKREQ_CPU_N DN34
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_D6/SRCCLKREQ1#

LAN
LAN_CLK_CPU_N CL3
LAN_CLK_CPU_P CL5
LAN_CLKREQ_CPU_N DP34
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_D7/SRCCLKREQ2#

SSD1
SSD_CLK_CPU_N CJ2
SSD_CLK_CPU_P CJ1
SSD_CLKREQ_CPU_N DN40
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_H10/SRCCLKREQ4#

CK3 CK4 DP36
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_D8/SRCCLKREQ3#

CLKOUT_PCIE_N5 CF5 SSD2_CLK_CPU_N
CLKOUT_PCIE_P5 CF3 SSD2_CLK_CPU_P
GPP_H11/SRCCLKREQ5# DP40 SSD2_CLKREQ_CPU_N
SSD2

RTCX1 DL48 XTL_32K_X1_CPU
RTCX2 DL49 XTL_32K_X2_CPU
RTCRST# DT47 RTC_RST#
SRTCRST# DK46 SRTC_RST#
GPDB/SUSCLK DF49 SUS_CLK
XTAL_IN DW8 XTL_38D4M_X1_CPU
XTAL_OUT DU8 XTL_38D4M_X2_CPU
XCLK_BIASREF DU6 XCLK_BIASREF R1823 60D4R2F-GP
SUS_CLK R1812 DY 100KR2J-1-GP
ICE-LAKE-U-GP-U

XTL_38D4M_X1_CPU R1850 0R2J-2-GP XTL_38D4M_X1_CPU_R
XTL_38D4M_X2_CPU R1851 0R2J-2-GP XTL_38D4M_X2_CPU_R
R1824 200KR2F-L-GP
C1805 SC15P50V2JN-DL-GP
X1802 XTAL-38D4MHZ-18-GP
082.30040.0091
2nd = 082.30040.0161
3rd = 082.30040.0171
C1806 SC15P50V2JN-DL-GP

RTC_AUX_S5
RN1801 SRN20KJ-1-GP
RTCRST_ON EC1804 DY SC1U10V2KX-3DLGP
RTC_RST R1816 100KR2J-3-GP
Q1803 RTC_RST 2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.031
3rd = 84.07002.I31
C1808 SC1U10V2KX-3DLGP
G1801 SJA-OPEN
C1807 SC1U10V2KX-1DLGP
SRTC_RST#
RTC_RST#
(#514849)
Layout: Place at the open door area.

PCH_SPI_EN_Q
SPI_CLK_ROM Q1804 PJE8408-R1-00001-GP SPI_CLK_CPU_R
084.08408.0031

SPI_SI_ROM Q1805 PJE8408-R1-00001-GP SPI_SI_CPU_R
084.08408.0031

SPI_WP_ROM Q1807 PJE8408-R1-00001-GP SPI_WP_CPU_R
084.08408.0031

SPI_CS_ROM_N0 Q1809 PJE8408-R1-00001-GP SPI_CS_CPU_N0
084.08408.0031

SPI_SO_ROM Q1806 PJE8408-R1-00001-GP SPI_SO_CPU_R
084.08408.0031

SPI_HOLD_ROM Q1808 PJE8408-R1-00001-GP SPI_HOLD_CPU_R
084.08408.0031

SPI_CS_ROM_N1 Q1810 PJE8408-R1-00001-GP SPI_CS_CPU_N1
084.08408.0031

PM_RSMRST# R1802 DY 0R1J-GP
EC_PCH_SPI_EN R1803 0R1J-GP PCH_SPI_EN R1814 100KR2J-1-GP

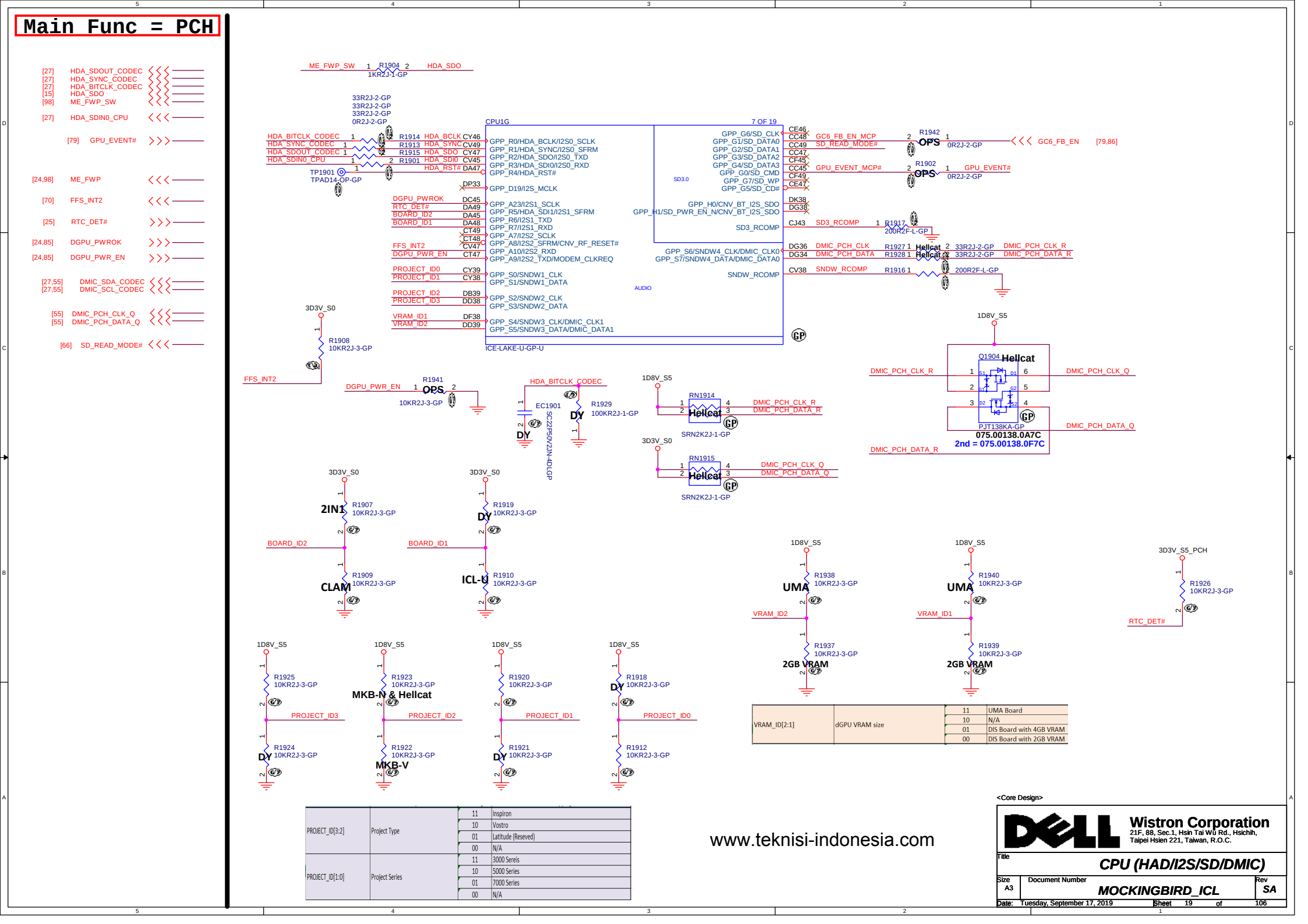
5V_S5 R1817 100KR2J-1-GP
3D3V_S5 R1815 100KR2J-1-GP
Q1811 Q1811_D_G
PCH_SPI_EN
PCH_SPI_EN_Q
2N7002KDW-1-GP
75.27002.F7C

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (SPI/LPC/SMBS/XTAL/CLK)		
Size A2	Document Number MOCKINGBIRD_ICL	Rev SA
Date: Tuesday, September 17, 2019	Sheet 18 of 106	

Main Func = PCH



VRAM_ID[2:1]	dGPU VRAM size		
		11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

PROJECT_ID[3:2]	Project Type		
		11	Inspiron
		10	Vostro
		01	Latitude (Reseved)
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Series
		01	7000 Series
		00	N/A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size: A3 | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 19 of 106

Main Func = PCH

[91] TPM_PIRQ#
[15] GPP_B23

[65,66] CPU_I2C_SDA_P0
[65,66] CPU_I2C_SCL_P0

[55,70] SENSOR_I2C_SDA
[55,70] SENSOR_I2C_SCL

[15] NRB_BIT

[15,27] SPKR

[24,66] LID_CL_SIO#

[55] CPU_I2C_SDA_TS
[55] CPU_I2C_SCL_TS

[65] KB_LED_BL_DET

[70] FFS_INT1

[24,66] LID_CL_SIO_TAB#

[55] DBC_PANEL_EN

[70] GSEN2_INT1_C
[55] GSEN_INT1_C

[15,27] TOUCH_PANEL_INTR#

[24] NB_MODE

[24,64] MASK_SATA_LED#

[64] SATA_LED#_D

[24,64] BATT_WHITE_LED#

[68] UART_2_CRXD_DTXD
[68] UART_2_CTXD_DRXD

[24] TABLE_MODE#

CPU1F — 6 OF 19 — ICE-LAKE-U-GP-U

NRB_BIT	CH48	GPP_B16/GSPI0_CLK	
	CF48	GPP_B18/GSPI0_MOSI	
	CF47	GPP_B17/GSPI0_MISO	
	CH49	GPP_B15/GSPI0_CS0#	
SPKR	CH47	GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#	
TPM_PIRQ#	CL47	GPP_B20/GSPI1_CLK	
	CK47	GPP_B22/GSPI1_MOSI	
	CK46	GPP_B21/GSPI1_MISO	
	CH45	GPP_B19/GSPI1_CS0#	
GPP_B23	CL48	GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1#	
FFS_INT1	DP21	GPP_C8/UART0_RXD	
SBIOS_TX	DK21	GPP_C9/UART0_TXD	
	DL21	GPP_C10/UART0_RTS#	
	DJ22	GPP_C11/UART0_CTS#	
UART_2_CRXD_DTXD	DT22	GPP_C20/UART2_RXD	
UART_2_CTXD_DRXD	DW22	GPP_C21/UART2_TXD	
	DV22	GPP_C22/UART2_RTS#	
TOUCH_PANEL_INTR#	DU22	GPP_C23/UART2_CTS#	
CPU_I2C_SDA_TS	DT24	GPP_C16/I2C0_SDA	
CPU_I2C_SCL_TS	DT23	GPP_C17/I2C0_SCL	
CPU_I2C_SDA_P0	DW23	GPP_C18/I2C1_SDA	
CPU_I2C_SCL_P0	DU23	GPP_C19/I2C1_SCL	
	DU41	GPP_H4/I2C2_SDA	
	DV41	GPP_H5/I2C2_SCL	
	DW41	GPP_H6/I2C3_SDA	
DBC_PANEL_EN	DT41	GPP_H7/I2C3_SCL	
	DT40	GPP_H8/I2C4_SDA/CNV_MFUART2_RXD	
	DW40	GPP_H9/I2C4_SCL/CNV_MFUART2_TXD	
	DV33	GPP_D13/ISH_UART0_RXD	
	DW33	GPP_D14/ISH_UART0_TXD	
	DT33	GPP_D15/ISH_UART0_RTS_N/GSPI2_CS1_N/IMGCLKOUT5	
KB_LED_BL_DET	DU33	GPP_D16/ISH_UART0_CTS_N/CNV_WCEN	
SIO_EXT_WAKE#	DK22	GPP_C12/UART1_RXD/ISH_UART1_RXD	
	DW24	GPP_C13/UART1_TXD/ISH_UART1_TXD	
	DV24	GPP_C14/UART1_RTS#/ISH_UART1_RTS#	
	DU24	GPP_C15/UART1_CTS#/ISH_UART1_CTS#	
	CN43	GPP_B5/ISH_I2C0_SDA	
	CN42	GPP_B6/ISH_I2C0_SCL	
	CN41	GPP_B7/ISH_I2C1_SDA	
	CL43	GPP_B8/ISH_I2C1_SCL	
	CL41	GPP_B9/I2C5_SDA/ISH_I2C2_SDA	
	CJ39	GPP_B10/I2C5_SCL/ISH_I2C2_SCL	
ISH_GP0	DU36	GPP_D0/ISH_GP0	
ISH_GP1	DV36	GPP_D1/ISH_GP1	
ISH_TABLE_MODE#	DW36	GPP_D2/ISH_GP2	
	DT36	GPP_D3/ISH_GP3	
ISH_KB_DISABLE	DU34	GPP_D17/ISH_GP4	
LID_CL_SIO#	DW34	GPP_D18/ISH_GP5	
LID_CL_SIO_TAB#	DT14	GPP_E15/ISH_GP6	
	DU14	GPP_E16/ISH_GP7	

TPAD14-OP-GP TP2026

Touch Screen

Touch Pad

3D3V_S0
RN2005
CPU_I2C_SDA_ISH0
CPU_I2C_SCL_ISH0
SRN1KJ-7-GP

CPU_I2C_SDA_ISH0 — R20511 — 0R2J-2-GP — SENSOR_I2C_SDA — ISH
CPU_I2C_SCL_ISH0 — R20521 — 0R2J-2-GP — SENSOR_I2C_SCL

ISH_GP0 — R20391 — 2IN1 — 0R2J-2-GP — GSEN_INT1_C — For Gyro+G
ISH_GP1 — R20371 — 2IN1 — 0R2J-2-GP — GSEN2_INT1_C
ISH_TABLE_MODE# — R20531 — 2IN1 — 0R2J-2-GP — TABLE_MODE#

ISH_KB_DISABLE — R2056 — 2IN1 — 100KR2J-1-GP

3D3V_S0
R2002 DEBUG 51KR2J-1-GP UART_2_CRXD_DTXD
R2003 DEBUG 51KR2J-1-GP UART_2_CTXD_DRXD

Q2001
ISH_KB_DISABLE — NB_MODE
BATT_WHITE_LED# — MASK_SATA_LED#
SATA_LED#_D
2N7002KDW-1-GP
75.27002.F7C

3D3V_S5_PCH
R2001 — DY — 10KR2J-3-GP — SIO_EXT_WAKE#

3D3V_S5
R2050 — 2IN1 — 10KR2J-3-GP
NB_MODE

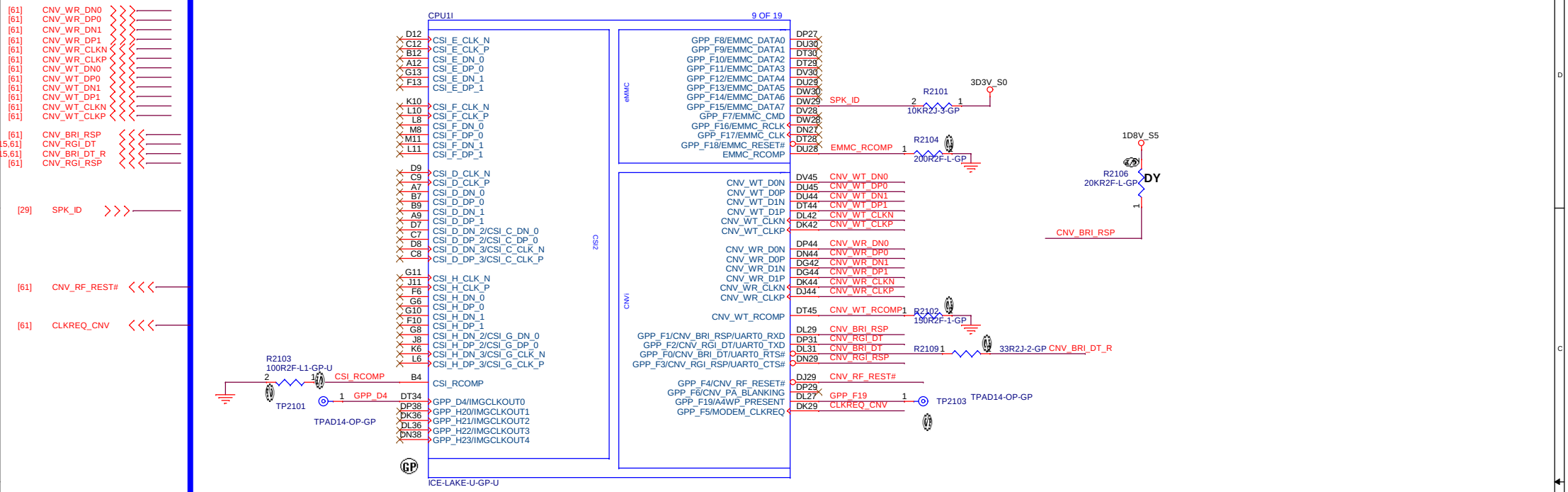
	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB可以動
Tablet Mode	don´t care	0	KB鎖住
Clam Shell Mode	0	1	KB鎖住

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A3 | Document Number: MOCKINGBIRD_ICL | Rev: SA
Date: Tuesday, September 17, 2019 | Sheet 20 of 106

Main Func = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (CSI/EMMC/CNVi)	
Size A3	Document Number MOCKINGBIRD_ICL	Rev SA
Date: Tuesday, September 17, 2019	Sheet 21 of 106	

Main Func = PCH

[50] VCCAUX_SENSE
[50] VSSAUX_SENSE
[40,50] CORE_VID0
[40,50] CORE_VID1

1D8V_CPU_AUX
CPU1N
14 OF 19
VCCIN_AUX_1 … VCCIN_AUX_36
VCCAUX_SENSE
VSSAUX_SENSE
VCCIN_AUX_VCCSENSE
VCCIN_AUX_VSSSENSE

3D3V_S5_VCCPRIM
3D3V_S5_PCH
R2202 0R2J-2-GP
(209mA)
1D8V_S5
(705mA)
VCCPRIM_3P3_2
VCCPRIM_3P3_3
VCCPRIM_3P3_4
VCCPRIM_1P8_2 … VCCPRIM_1P8_9

VCCLDOSTD_0P85 — 0D85V_S5_VCCLDOSTD_OUT
VCCA_CLKLDO_1P8 — 1D8V_S5_CLKLDO (100mA)
VCCDPHY_1P24 — 1D24V_S5_VCCDPHY_OUT
VCCDSW_1P05 — 1D05V_S5_VCCDSW_OUT
VCC1P05_1 / VCC1P05_2 / VCC1P05_3 — 1D05V_S5_OUT (1.5A) Supply to VCCST & VCCSTG
[VCC1P05_OUTPUT_PLL] — CD1 — 1D05V_VCCP_OUT_SFR (Output)
VCCPRIM_1P05_1 / VCCPRIM_1P05_2 / VCCPRIM_1P05_3 / VCCPRIM_1P05_4 — 1D05V_S5_VCCPRIM_OUT
VCCRTC — RTC_AUX_S5
VCCDSW_3P3 — 3D3V_VCCDSW
VCCPGPPR — 3D3V_S5_HDA
GPP_B0/CORE_VID0 — CORE_VID0
GPP_B1/CORE_VID1 — CORE_VID1
GPP_B2/VRALERT# — VRALERT#

1D05V_S5_VCCPRIM_OUT — C2203 SC2U10V2KX-1DLGP
1D05V_S5_OUT — C2208 SC2U10V2KX-1DLGP
3D3V_S5_HDA — C2214 SC2D2U10V3KX-3DLGP
1D05V_S5_BYPASS — R2209 100KR2J-1-GP
1D05V_VNN_BYPASS — R2210 100KR2J-1-GP
1D05V_VCCP_OUT_SFR — C2215 SC1U10V2KX-1DLGP, C2216 SC1U10V2KX-1DLGP

PH/PL 100R at VR side.

1D05V_S5_BYPASS — VCC_V1P05EXT_1P05
1D05V_VNN_BYPASS — VCC_VNNEXT_1P05
3D3V_S5_VCCPRIM_FUSE — VCCPRIM_3P3_1
1D8V_S5 — VCCPRIM_1P8_1
3D3V_SPI — VCCSPI

ICE-LAKE-U-GP-U

3D3V_S5_PCH — R2211 100KR2J-GP — CORE_VID0, CORE_VID1
R2212 100KR2J-1-GP
R2201 100KR2J-1-GP — VRALERT#
R2205 0R2J-2-GP — (3mA)
R2207 0R2J-2-GP
R2213 0R2J-2-GP — 1D8V_S5

3D3V_S5 — R2218 100KR2J-1-GP
VRALERT# — R2217 0R2J-2-GP — VRALERT#_R — D2201 RB520S30-GP — PROCHOT#_CPU [8,24,44,46]
Follow TDK design
83.R2003.A8M
2nd = 83.1R003.N8F
VRALERT#_R [44]

[Q] Follow EVB or need to connect to PD or power page .

Decoupling Requirements for Ice Lake U PCH-LP for VCCPRIM_3P3

Domain	Backside cap	Primary side cap	Placement guideline [2]
VCCPRIM_3P3		1x 0402 (placeholder)	Place the cap as close as possible to package pin DG26.
		1x 0402 (placeholder)	Place the cap as close as possible to package pin DF23.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-22 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U Processor for VCCPRIM_1P8

Domain	Backside cap	Primary side cap	Placement guideline [1]
VCCPRIM_1P8		1x 0402 (placeholder)	Place the cap near to package pin DG20 right after signal breakout.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.

Decoupling Requirements for Ice Lake U PCH-LP for VCCA_CLKLDO_1P8

Domain	Component/ Placement	Value	Placement Guideline [2, 3]
VCCA_CLKLDO_1P8	Decap/Top Side	1x 47uF 0603	Place the component near to package pin DU15 right after signal breakout.
	Resistor/Top Side	1x 100mOhm 0603	
	Inductor/Top Side	1x 600nH XFL4012-601ME	

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-26 for decoupling capacitor/filter placements.
3. By Default: 47uF 0603 is stuffed; Inductor is placeholder; Resistor is stuffed only when Inductor is stuffed.

Must take care this power layout and add shield GND.
Need to apply XFL4012-601ME P/N

Decoupling Requirements for Ice Lake U PCH-LP for VCCDSW_3P3

Domain	Backside cap	Primary side cap	Placement guideline [3]
VCCDSW_3P3		1x 0402 (placeholder)	Place the cap near to package pin DE31 right after signal breakout.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-28 for decoupling capacitor placements.

Decoupling Requirements for Ice Lake U PCH-LP (Sheet 1 of 2)for VCCRTC

Domain	Backside cap	Primary side cap	Placement guideline [1,2]
VCCRTC		1x 0.1uF 0402	Place the cap closest possible to package pin DG33. 0.1uF cap should place before the 1uF cap.
		1x 1uF 0402	Place the cap closest possible to package pin DG33. 1uF cap should place after the 0.1uF cap.

Trace width > 40mil

Decoupling Requirements for Ice Lake U PCH-LP for VCCDSW_1P05

Domain	Backside cap	Primary side cap	Placement guideline
VCCDSW_1P05		1x 1uF 0402	Place the cap closest possible to package pin.

Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-33 for decoupling capacitor placements.

Place cap within 3mm from SOC edge.

Decoupling Requirements for Ice Lake U PCH-LP for VCCDPHY_1P24

Domain	Backside cap	Primary side cap	Placement guideline
VCCDPHY_1P24		1x 4.7uF 0402	Place cap within 3mm from package edge.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-34 for decoupling capacitor placements.

Place cap within 3mm from SOC edge

Decoupling Requirements for Ice Lake U PCH-LP for VCCLDOSTD_0P85

Domain	Backside cap	Primary side cap	Placement guideline
VCCLDOSTD_0P85		1x 2.2uF 0402	Place cap within 3mm from package edge.

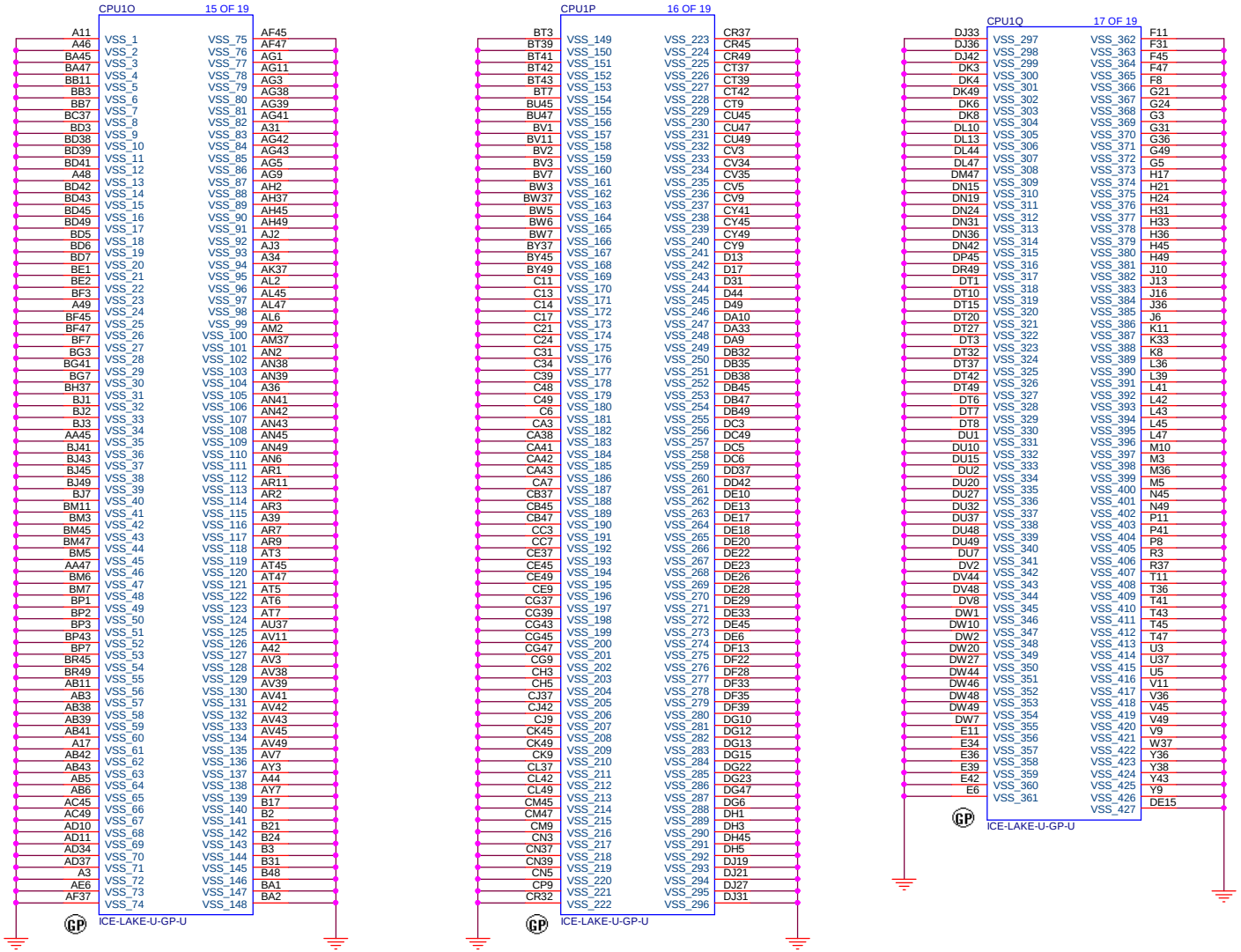
Note:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)
Size: Custom | Document Number: MOCKINGBIRD_ICL | Rev: SA
Date: Tuesday, September 17, 2019 | Sheet 22 of 106

Main Func = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size: A3	Document Number: MOCKINGBIRD_ICL	Rev: SA
Date: Tuesday, September 17, 2019	Sheet 23 of 106	

Main Func = KBC

MODEL ID

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	14" UMA	100.0K	**10.0K**	3
2	15" Upsell UMA	100.0K	**17.8K**	2.801
3	15" M/V/3.5" M/S UMA	100.0K	**27.0K**	2.598
4	17" CS UMA	100.0K	**37.4K**	2.402
5	15" Upsell DIS	100.0K	**49.9K**	2.201
6	17" 2in1 UMA	100.0K	**64.9K**	2.001
7	14"/15" M/S DIS	100.0K	**82.5K**	1.808
8	17" CS DIS	100.0K	**107K**	1.594
9	15" Upsell DIS	100.0K	**154K**	1.299
10	17" 2in1 DIS	100.0K	**200K**	1.1

64.82525.6DL

Mockingbird

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	N5 14"/15" UMA	100.0K	**10.0K**	3
2	V5 14"/15" UMA	100.0K	**17.8K**	2.801
3	L 14"/15" UMA(CML&KBL-R)	100.0K	**27.0K**	2.598
4	N7/V7 UMA	100.0K	**37.4K**	2.402
5	N5 14"/15" DIS	100.0K	**49.9K**	2.201
6	V5 14"/15" DIS	100.0K	**64.9K**	2.001
7	L 14"/15" DIS(CML)	100.0K	**82.5K**	1.808
8	N7/V7 DIS	100.0K	**107K**	1.594

64.49925.6DL
64.64925.6DL
64.82525.6DL

BOARD ID

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	**10.0K**	3
2	X01	100.0K	**17.8K**	2.801
3	X02	100.0K	**27.0K**	2.598
4	X03(Reserve)	100.0K	**37.4K**	2.402
5	A00	100.0K	**49.9K**	2.201
6	A01	100.0K	**64.9K**	2.001
7	A02	100.0K	**82.5K**	1.808
8	A03	100.0K	**107K**	1.594
9	Reserve	100.0K	**154K**	1.299
10	Reserve	100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

For Charge (confirm level shift 1.8V to 3.3V)

For eSPI

GPIO45 (CR_STRAP)

For USB TypeC

JTAG DEBUG CONN

EC G3 Flash Share

For eSPI

GPIO55 (BSS_STRAP)

Already pull low on CPU side

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot Note 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/CT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used as to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.

2.14 MEC1618 / DEC1618 Shared SPI Flash Isolation Requirement

Per latest Intel PCH design, all the SPI lines to the PCH are tied to GND until the prime rails come up. In this case, the MEC1618 must implement the following:

- Isolation on all Shared SPI pins or
- Keep th PCH powered off the time or
- Wait for the Prime Rails to come up by holding the EC in reset by the RESET_INP pin. The example circuitry is shown in the figure below.

Power Switch Logic(PSL)

pull high on CPU side

Main Func = SPI Flash

Socket for 16M

Layout : SKT251 and U2503 co-lay

SKT251 — SKT-G6179HT0321-001-GP — 62.10089.011

U2501 — 8M — W25Q64JVSSIQ-GP — 072.25Q64.0H01 / 2nd = 072.25647.000D / 3rd = 072.25B64.0C01

U2503 — 16M — W25Q128JVSIQ-GP — 072.25128.0B51 / 2nd = 072.25127.0001 / 3rd = 072.25128.0D61

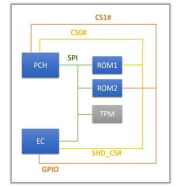
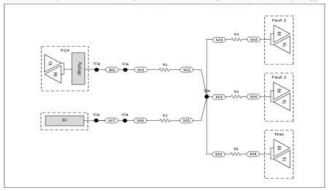


Figure 6-85. SPI0 3-Load(2 Flash and 1 TPM) EC G3 Flash Fharing with Wire-OR Topology



Main Func = RTC

Q2507 — PJA3413-1-GP — 084.03413.0031 / 2nd = 084.02301.0031

D2501 — BAT54C-12-GP — 75.00054.A7D / 2nd = 75.00054.T7D

Q2501 — 2N7002KDW-1-GP — 75.27002.F7C

U2502 — RT9742CGJ5-GP — 074.09742.0A9F / 2nd = 074.00524.0B9F

D2503 — BAT54A-11-GP

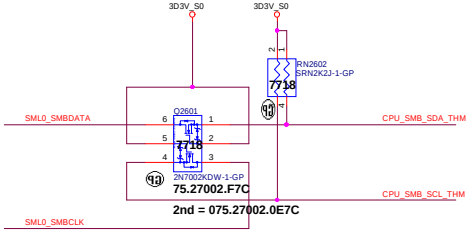
<Core Design>

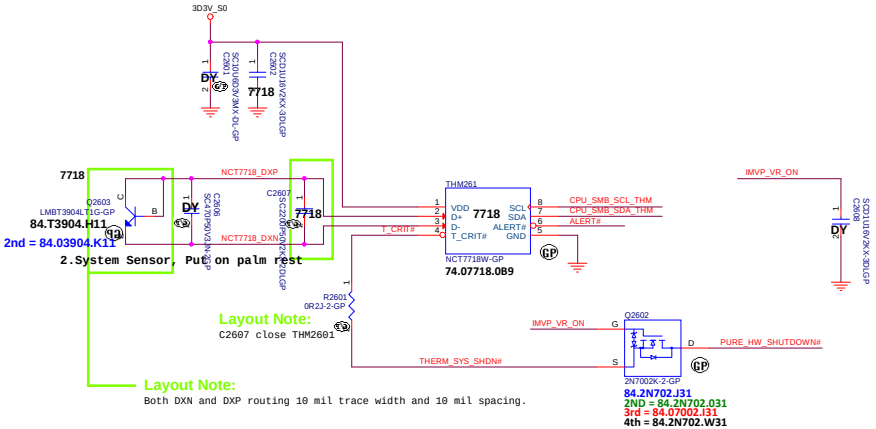
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

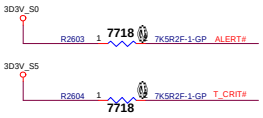
Title	Flash	
Size: A2	Document Number: MOCKINGBIRD_ICL	Rev: SA
Date: Tuesday, September 17, 2019	Sheet 25 of 105	

Main Func = Thermal Sensor

[18,24,79] SML0_SMBDATA
[18,24,79] SML0_SMBCLK
[17,24] IMVP_VR_ON
[40] PURE_HW_SHUTDOWN#
[24] PWM_FAN1
[24] FAN_TACH1



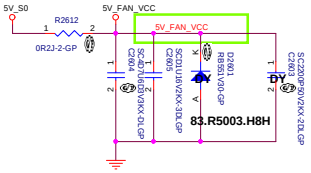


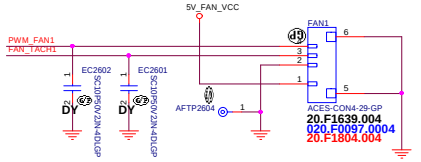


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1

Layout Note:
Signal Routing Guideline:
Trace width = 15mil





<Core Design>

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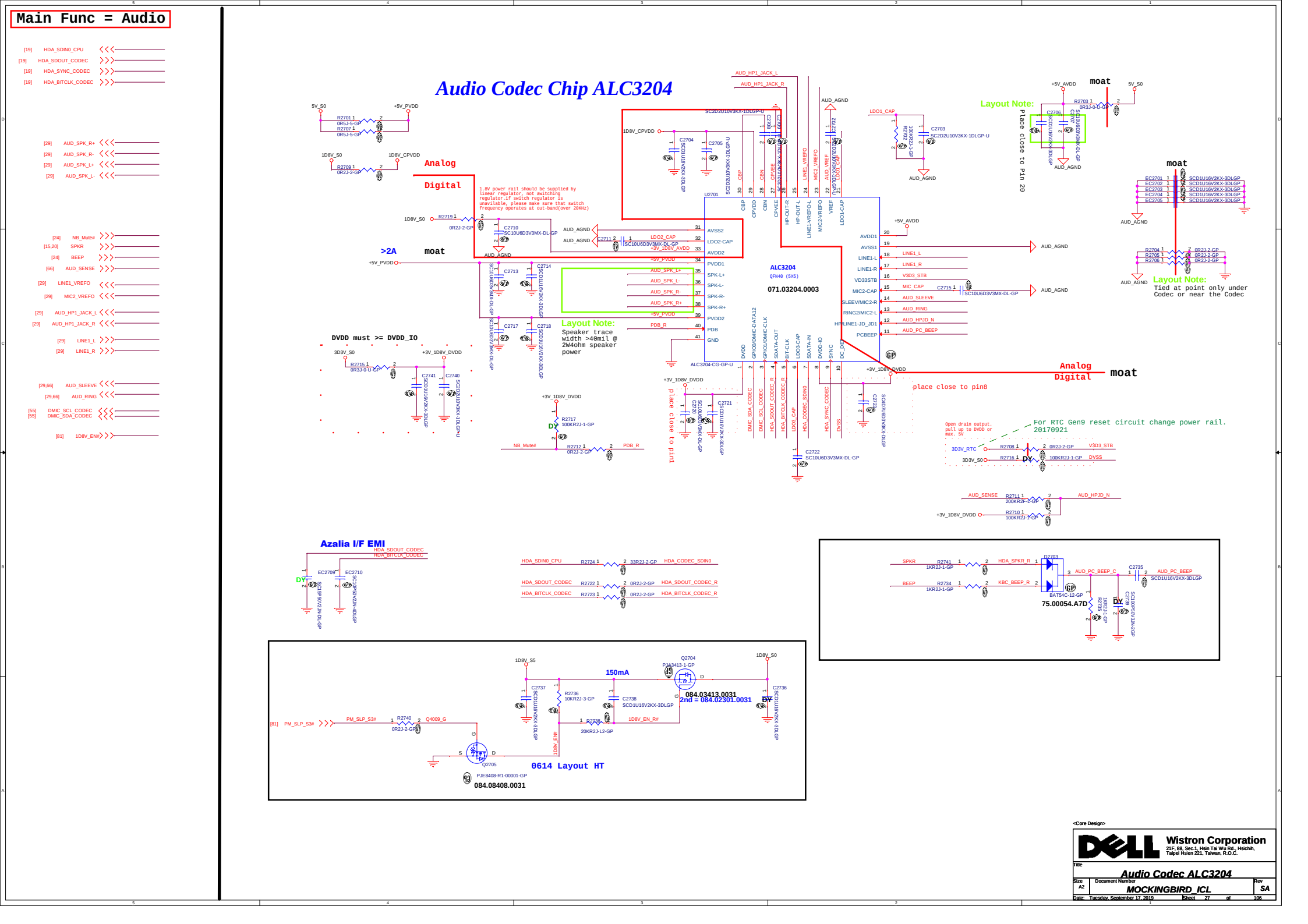
Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: MOCKINGBIRD_ICL
Rev: SA
Date: Tuesday, September 17, 2019
Sheet 26 of 106

Main Func = Audio



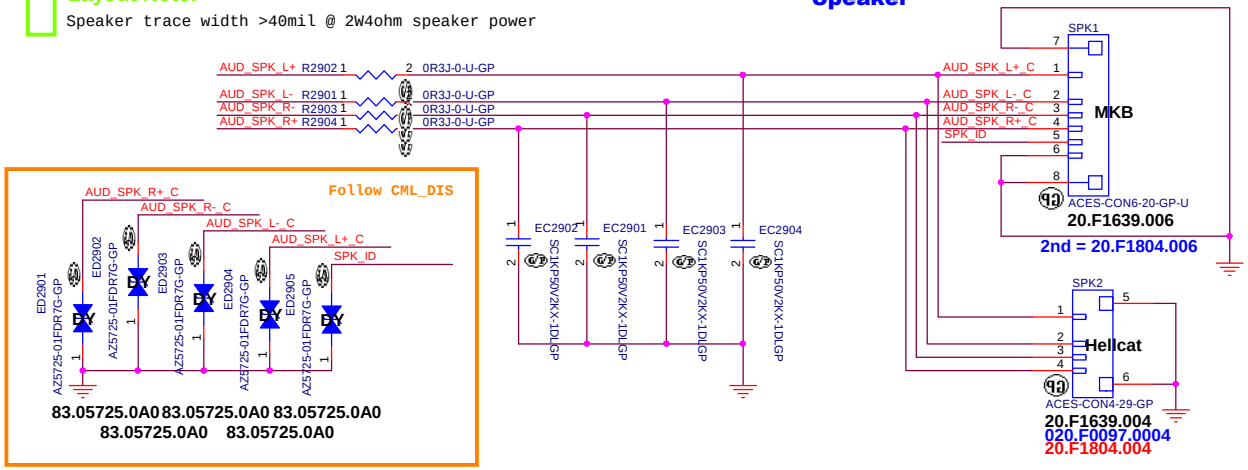
Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[20] SPK_ID

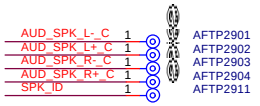
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: FG
0: Veci



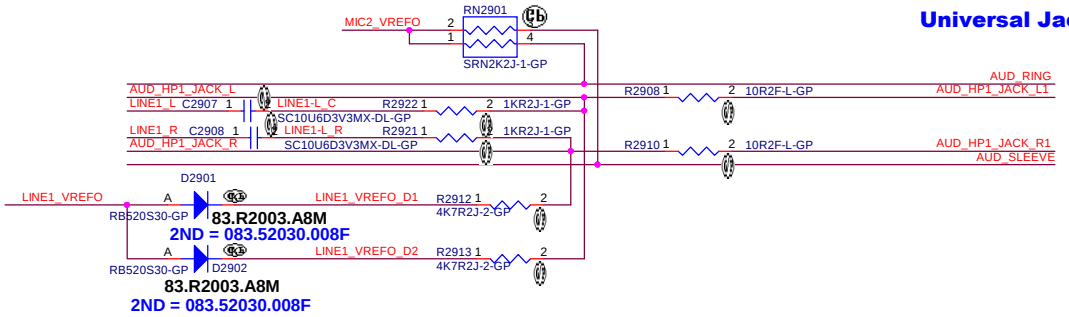
From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

Universal Jack (Moved to I/O Board)



<Core Design>

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Title: Audio IO

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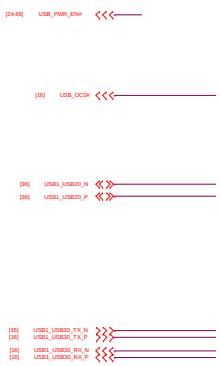
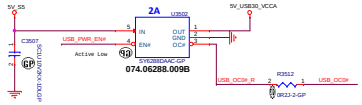
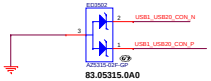
A3	MOCKINGBIRD_ICL	SA

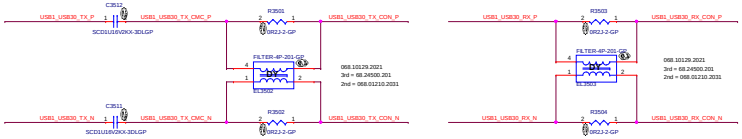
Date: Tuesday, September 17, 2019 Sheet 29 of 106

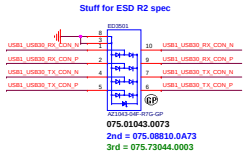
Main Func = USB3.0 Port1

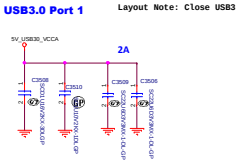


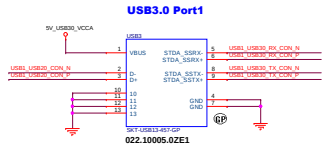












Main Func = USB3.0 Port2

Title: **USB3.0 CONN**

Size	Document Number	Rev
A1	MOCKINGBIRD_ICL	SA

Date: Tuesday, September 17, 2013 Sheet 35 of 105

SSID = Power Plane & Sequence

5V_S0 & 3D3V_S0

[51] 1D2V_VTT_PWRGD
[17,54,55,81] PM_SLP_S3#
[45] 3V_5V_EN
[26] PURE_HW_SHUTDOWN#
[24] ALWON
[17] SIO_SLP_S0#
[17,51,66] PM_SLP_S4#
[22,50] CORE_VID0
[22,50] CORE_VID1
[17] CPU_C10_GATE#
[17,24,44,46] VCCST_PWRGD

ROSA Run Power

5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

83.R2003.A8M
2nd = 083.52030.008F

074.02898.0093

Power Good

All_SYS_PWRGD

1D05V_VCCSTG_EN

73.01G08.EHG

1D05V_VCCST/1D05V_VCCSTG

650mA
074.05027.0B93
2nd = 074.05201.0A93

150mA
074.05027.0B93
2nd = 074.05201.0A93

1D2V_VCCPLL_OC

1D05V_VCCST_EN

75.00054.A7D
75.00054.A7D

If VCCPLL_OC is powered directly from VDDQ with no power gate, then SLP_3# should be replaced with SLP_S4# in the VCCST enable logic.

75.27002.F7C

Note 1: Vpullup voltage may be V1.8VA or V3.3A as set by the OEM for the GPIOs that CORE_VID[1:0] reside on. See the ICL-LP SPI Programming Guide for details.

Note 2: If VCCIN_AUX is on at a non-0V, VCCST must also be powered on.

Note 3: If VCCPLL_OC is powered directly from VDDQ with no power gate, then SLP_3# should be replaced with SLP_S4# in the VCCST enable logic.

See Note2 and Note3

V-tree_VCCIO

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.3	0.64	0.9	V

1D8V_PCH_C10/1D8V_S0

700mA
Premium
Volume
500mA

ICL no VCCIO

084.08408.0031
084.08408.0031

<Core Design>

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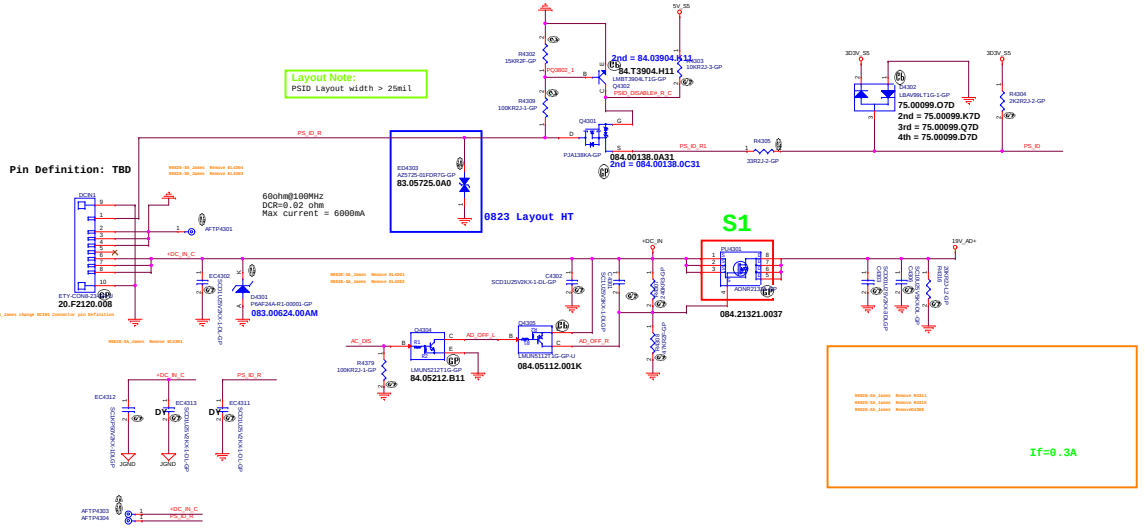
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

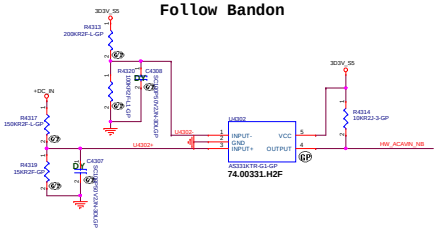
Size: A1 | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Thursday, September 27, 2012 | Sheet 49 of 105

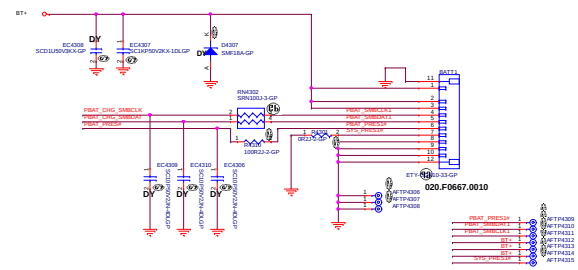
Main Func = ADT Input

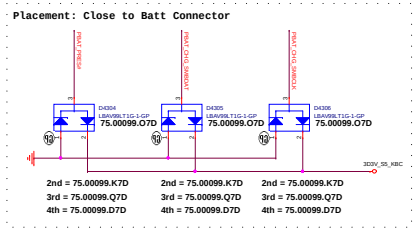


Barrel Adapter Piug-in Detect
Follow Bandon



Main Func = M-BAT Input





Wistron Corporation	DCIN	
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ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

I2C form EC

To EC

ISL9538 AMON/BMON to EC

From NXP ACK

E3

S2

084.21321.0037

084.07380.0037

DCR=8mm~9m Ohm,
Idc=13A, Isat=16A
10.0mm x 11.5mm x 3.0mm

084.21307.0037

ISL9538C4HRTZ-T GP
074.09538.M500

0523

PU 3V3_AON_S0 on GPU side

PU +VCCSTG = 1.0 V on CPU side

TypeC Prochot
Follow custormer circuits.

CHECK EE
follow custormer circuits.

+3D3V_VDD_DCIN

Vcore_OVP

Vout=1.24*(1+(R1/R2))

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIm1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

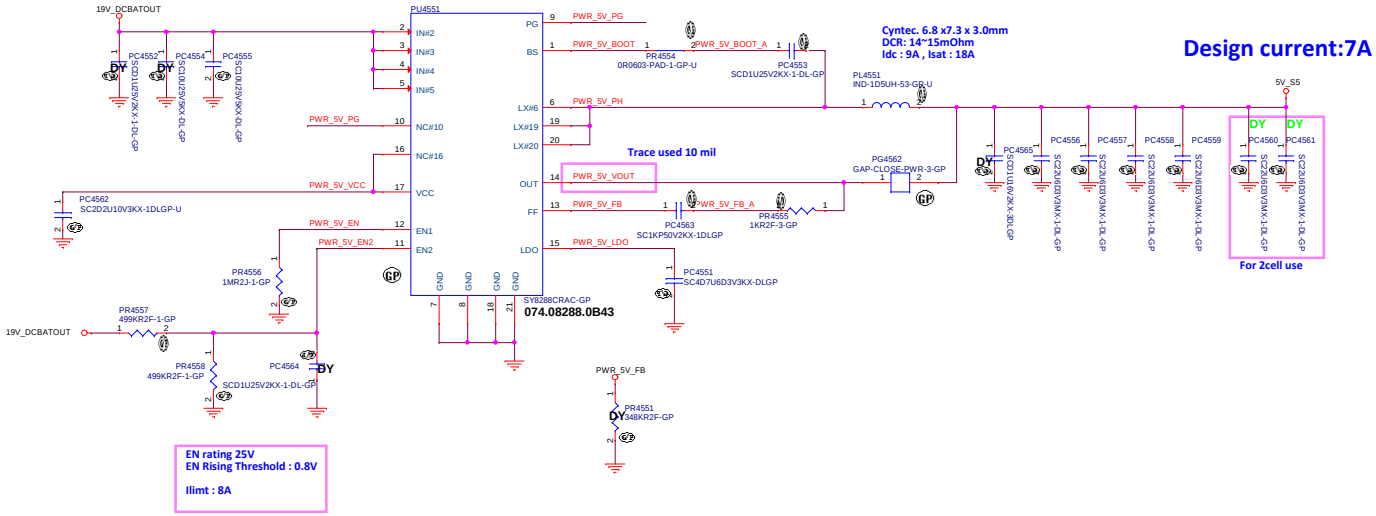
Wistron Corporation
Power (Charger_ISL9538)
MOCKINGBIRD_ICL

SSID = PWR.Plane.Regulator_5V

SY8288C For 5V

OFFPAGE-Signal

OFFPAGE-GAP

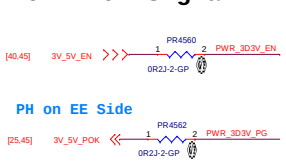


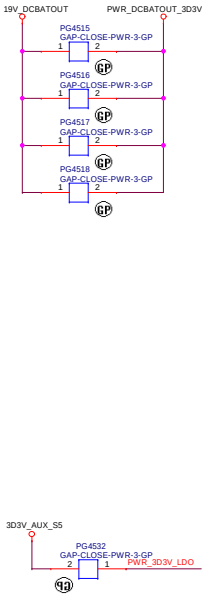
SSID = PWR.Plane.Regulator_3D3V

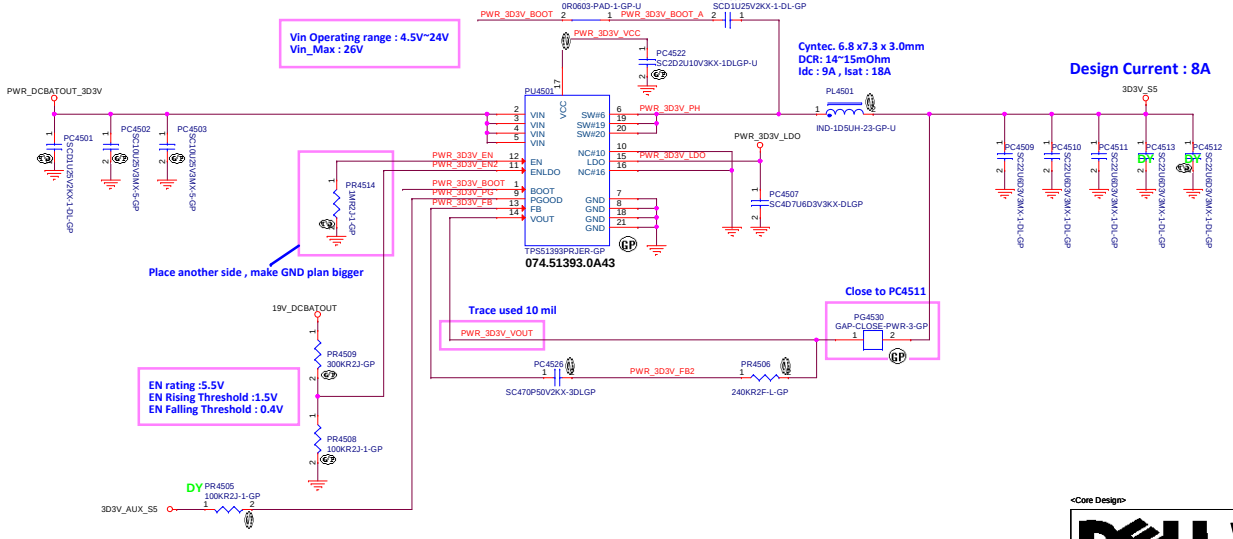
TPS51393 For 3D3V

OFFPAGE-Signal

OFFPAGE-GAP







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

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Main Func = CPU_CORE

OFFPAGE

SVID

- [7] SVID_CLK_CPU — PR4632 0R0402-PAD-1-GP — PWR_VCORE_SCLK_R
- [7] SVID_DATA_CPU — PR4633 0R0402-PAD-1-GP — PWR_VCORE_SDIO_R
- [7] SVID_ALERT#_CPU — PR4634 0R0402-PAD-1-GP — PWR_VCORE_ALERT#_R
- [3,22,24,44] PROCHOT#_CPU — PR4631 0R0402-PAD-1-GP — PWR_VCORE_VRHOT_R
- [44] CHGR_PSYS_IMVP — CHGR_PSYS_IMVP
- [7,44] PWR_IMVP_PWRGD — PR4636 0R0402-PAD-1-GP — PWR_VCORE_VR_READY
- [5,40,44] VCCST_PWRGD — PR4635 0R0402-PAD-1-GP — PWR_VCORE_VR_EN

VCORE SENSE

- [7] VSSCORE_SENSE — VSSCORE_SENSE
- [7] VCCCORE_SENSE — VCCCORE_SENSE

- [47] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
- [47] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
- [47] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1
- [47] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
- [47] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
- [47] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2
- [47] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
- [47] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
- [47] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
- [47] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

1D05V_VCCST — PR4604 PR4605 PR4606 — PR4621 PR4622 PR4623 — 1D05V_VCCSTG_TERM — PR4603 1KR2F-3-GP — PWR_VCORE_SCLK_R — PWR_VCORE_ALERT#_R — PWR_VCORE_SDIO_R — PWR_VCORE_VRHOT_R — PR4607 100R2F-L1-GP-U — 5V_S5 — PR4617 0R2J-2-GP — 3D3V_S0 — PR4609 10K2J-3-GP — PWR_VCORE_VR_READY — PR4601 0R2J-2-GP — 19V_DCBATOUT — PC4601 SCD22U25V2KX-4-GP — PC4613 SC1U10V2KX-1DLGP — PWR_VCORE_VR_EN

PC4612 SC4700P50V2KX-1DLGP — PR4602 12K1R2F-L1-GP — PC4609 SC330P50V2KX-3-DL-GP — PR4608 93K1R2F-L-GP

PU4601 ISL95869HRTZ-T-GP 074.95869.0073

CHGR_PSYS_IMVP — PWR_VCORE_IMON — PWR_VCORE_NTC — PWR_VCORE_COMP — PWR_VCORE_FB — PWR_VCORE_RTN — PWR_VCORE_ISUMN1

PROG1 — PWR_VCORE_PROG1 — PR4619 9K31R2F-GP — PR4620 9K31R2F-GP

PROG2 — PWR_VCORE_PROG2

BOOT1 — PWR_VCORE_BOOT1 — PR4621 0R3F-1-GP-U — PWR_VCORE_BOOT1_N — PC4610 SCD22U25V2KX-4-GP

UGATE1 — PWR_VCORE_UGATE1

PHASE1 — PWR_VCORE_PHASE1

LGATE1 — PWR_VCORE_LGATE1

PWM3 — PWR_VCORE_VDDP — PR4625 0R2J-2-GP — 5V_S5 — PC4625 SC1U10V2KX-1DLGP

PR4616 10KR2F-2-GP — PWR_VCORE_NTC_N — PR4655 27K4R2F-GP — PR4618 69.60012.0001 — B=4500

PR4611 0R3F-1-GP-U — PWR_VCORE_BOOT2_N — PC4611 SCD22U25V2KX-4-GP

5V_S5

PR4615 1K3R2F-1-GP — PC4608 SC82P50V2KX-3-DL-GP — PWR_VCORE_COMP_N

PR4614 2K2R2F-3-GP — PR4613 20K0R2F-L-GP — PR4612 392R2F-GP — PC4607 SC5D01U25V2KX-3DLGP — PC4606 SC330P50V2KX-3-DL-GP — PWR_VCORE_FB1 — PWR_VCORE_FB4 — PWR_VCORE_FB2 — PC4604 SC820P50V2KX-1-DL-GP — PR4665 0R2J-2-GP — PWR_VCORE_FB3

VCCCORE_SENSE — PR4667 0R0402-PAD-1-GP — PR4640 100R2F-L1-GP-U — O1V_CPU_CORE — PC4615 SCD01U25V2KX-3DLGP — PC4605 SC330P50V2KX-3-DL-GP — PC4638 SC330P50V2KX-3-DL-GP — PR4626 100R2F-L1-GP-U

PWR_VCORE_ISEN2 — PWR_VCORE_ISEN1 — PWR_VCORE_ISUMP

PC4623 SC2200P50V2KX-2DLGP — PWR_VCORE_ISUMN_N — PR4628 3K48R2F-GP — PR4627 511R2F-2-GP — PR4666 0R0402-PAD-1-GP — VSSCORE_SENSE

PC4614 SCD22U16V2KX-3DLGP — PC4618 SCD22U16V2KX-3DLGP — PR4629 0R2J-2-GP — PWR_VCORE_ISUMP_N — PC4616 SC5D02U16V2KX-3DLGP — PC4602 SCD01U16V2KX-3DLGP — PR4630 11KR2F-L-GP — PR4653 2K61R2F-1-GP — PWR_VCORE_ISUMNP_2 — PR4650 NTC-10K-29-GP-U 69.60011.201 — B=3370 — PWR_VCORE_ISUMN — PC4603 SCD01U16V2KX-3DLGP

PROG1 VBOOT:1.8V F=750kHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(1/3))

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 46 of 106

Main Func = VCCIN

OFFPAGE

[46] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
[46] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
[46] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

[46] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
[46] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
[46] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

[46] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
[46] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
[46] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
[46] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

19V_DCBATOUT — PWR_DCBATOUT_VCOREA

PL4703 BLM21PG220SN1DGP 68.00084.831
PL4704 BLM21PG220SN1DGP 68.00084.831

PWR_DCBATOUT_VCOREA

PC4702 SC1DU25V3MX-5-GP
PC4703 SC1DU25V3MX-5-GP
PC4704 SC1DU25V3MX-5-GP
PC4705 SC1DU25V3MX-5-GP
PC4706 SC1D1U25V2KX-1DLGP

PWR_VCORE_LGATE1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_DCBATOUT_VCOREA

PU4701 AOE6932-GP 075.06932.0A73

PWR_VCORE_PHASE1

ICL_U42 15W
Performance
TDC=39A
ICCMAX=70A

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

1V_CPU_CORE

PL4701 IND-D1SUH-33-GP 068.R1510.1171

PR4705 2D2R6J-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP

PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP

PT4701 SE330U2D5VDM-2GP 79.3371V.2PL

PWR_VCORE_ISUMP_GA
PWR_VCORE_ISUMN_GA

PWR_VCORE_ISEN1
PR4721 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4708 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2

PR4709 10R2F-L-GP
PR4722 100KR2F-L1-GP

PWR_DCBATOUT_VCOREA

PC4717 SC1DU25V3MX-5-GP
PC4714 SC1DU25V3MX-5-GP
PC4716 SC1DU25V3MX-5-GP
PC4715 SC1DU25V3MX-5-GP
PC4718 SC1D1U25V2KX-1DLGP

PWR_VCORE_LGATE2
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_DCBATOUT_VCOREA

PU4702 AOE6932-GP 075.06932.0A73

PWR_VCORE_PHASE2

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

1V_CPU_CORE

PL4702 IND-D1SUH-33-GP 068.R1510.1171

PR4714 2D2R6J-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP

PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP

PWR_VCORE_ISUMP_GB
PWR_VCORE_ISUMN_GB

PWR_VCORE_ISEN2
PR4723 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4716 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1

PR4715 10R2F-L-GP
PR4724 100KR2F-L1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))
Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA
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Main Func = VCCIN_AUX

OFFPAGE

VID

[22,40] CORE_VID0 — PR5014 0R2J-2-GP — PWR_VCCIN_AUX_VID0

[22,40] CORE_VID1 — PR5015 0R2J-2-GP — PWR_VCCIN_AUX_VID1

VCCIN_AUX SENSE

[22] VCCAUX_SENSE — PR5017 0R2J-2-GP — PWR_VCCIN_AUX_FB_O

[22] VSSAUX_SENSE — PR5018 0R2J-2-GP — PWR_VCCIN_AUX_RGND

[53] 1D8V_S5_PWROK — PR5012 0R2J-2-GP — PWR_VCCIN_AUX_EN_R

[54] 1D8V_CPU_AUX_PG — PR5013 0R2J-2-GP — PWR_VCCIN_AUX_PG

19V_DCBATOUT — PL5003 BLM21PG220SN1DGP 68.00084.831 — PL5004 BLM21PG220SN1DGP 68.00084.831 — PWR_VCCIN_AUX_IN

PWR_VCCIN_AUX_IN — PC5006 PC5007 PC8638 PC8639 22U/6.3V/X6S/0805

PWR_VCCIN_AUX_BOOT — PC5009 SC1U10V2KX-1DLGP

PU5001 RT6543AGQW-GP 074.06543.0073

Pin	Net
1	PWR_VCCIN_AUX_CS
2	PWR_VCCIN_AUX_ISENP
3	PWR_VCCIN_AUX_ISENN
4	PWR_VCCIN_AUX_PG
5	PWR_VCCIN_AUX_COMP
6	PWR_VCCIN_AUX_FB
7	PWR_VCCIN_AUX_RGND
8	1D8V_CPU_AUX
9	PWR_VCCIN_AUX_FSW
10	BOOT
11	PWR_VCCIN_AUX_UG
12	PWR_VCCIN_AUX_LX
13	PWR_VCCIN_AUX_LG
14	PGND
15	PWR_VCCIN_AUX_VCC
16	VCC
17	PWR_VCCIN_AUX_VID1
18	PWR_VCCIN_AUX_VID0
19	PWR_VCCIN_AUX_EN
20	PWR_VCCIN_AUX_IN
21	AGND

PR5002 124KR2F-GP — PR5001 2D2R2J-GP — PR5004 10KR2J-3-GP — PC5008 SC1U10V2KX-1DLGP — PR5005 2D2R2J-GP — PC5010 SC1U10V2KX-1DLGP — PR5003 DY 10KR2J-3-GP

PU5002 PU5003 FDMS3600-02-RJK0215-COLAY-GP 075.07321.0073

ICL_U42 15W Performance TDC=14A ICCMAX=32A

Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A

PL5001 IND-D22UH-37-GP — PR5021 17K8R2F-GP — PR5016 0R2J-2-GP — PR5007 100R2F-L1-GP-U — PT5001 SE330U2D5VDM-2GP 79.3371V.2PL — PC5011 SCD1U25V2KX-1-DL-GP — PR5008 332R2F-1-GP — PR5022 634R2F-1-GP — PWR_VCCIN_AUX_RC — PR5023 NTC-10K-29-GP-U B=3370K

PC5003 SC2200P50V2KX-2DLGP — PWR_VCCIN_AUX_COMP_R — PR5011 10KR2F-2-GP

PC5002 SC470P50V2KX-3DLGP — PWR_VCCIN_AUX_FB_R — PR5009 1K6R2F-GP DY

PC5004 SC22P50V2JN-4DLGP — PR5010 5K62R2F-GP

PR5006 100R2F-L1-GP-U — PR5020 0R2J-2-GP

PWR_VCCIN_AUX_FB_O

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX

Size: A2 | Document Number | Rev: SA

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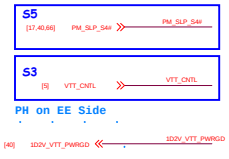
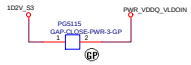
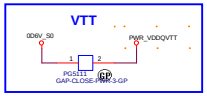
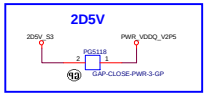
OFFPAGE



OFFPAGE_GAP







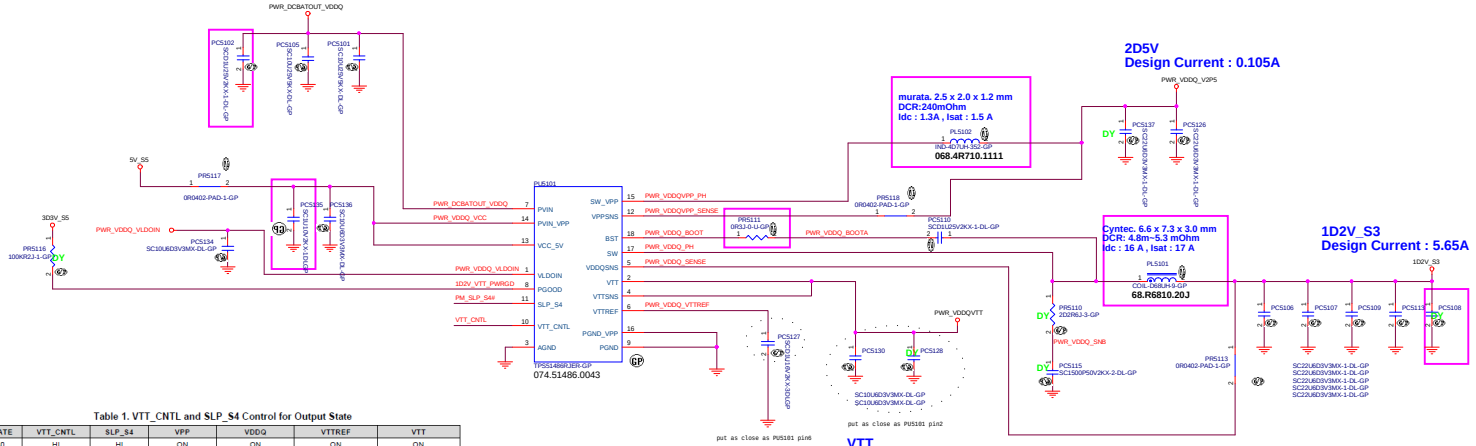


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

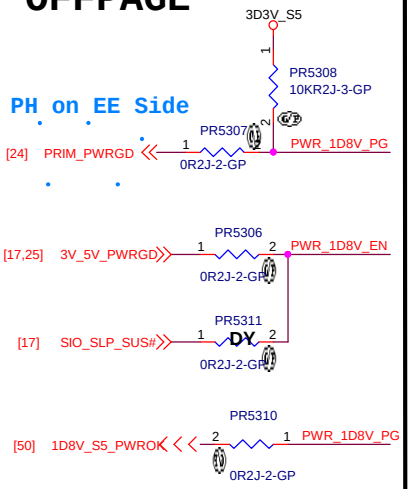
Title: 051_POWER (TPS51486R_VDDQ/VTT)

Size: Custom | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2013 | Sheet 51 of 106

Main Func = 1D8V/1D2V

OFFPAGE



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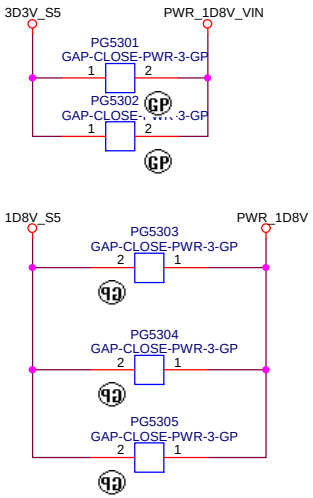
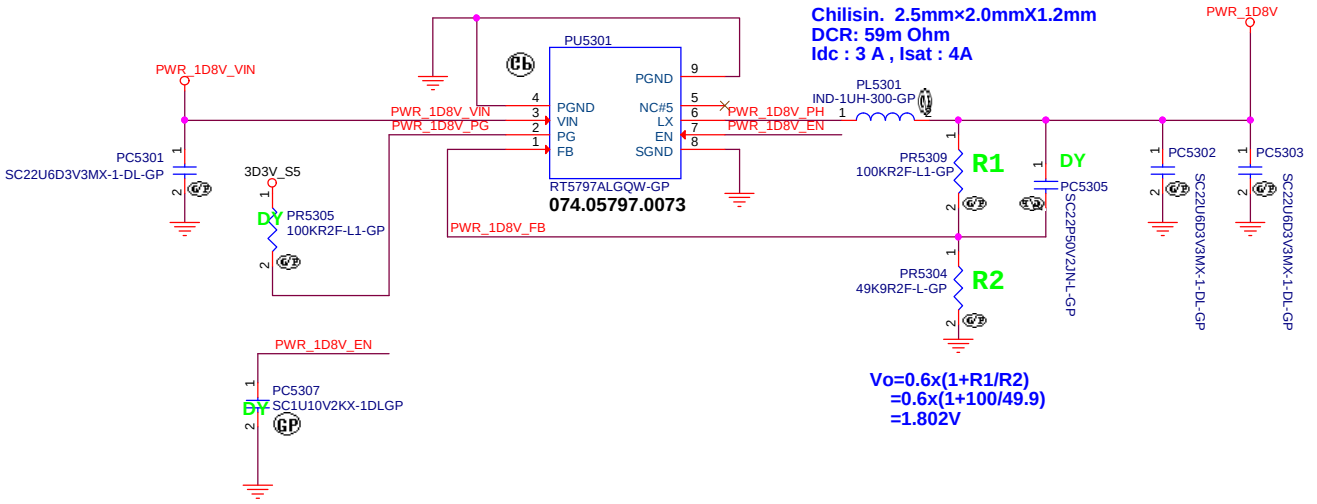


Design Current=1.7A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD&CAM&DMC&Touch	
Size B	Document Number MOCKINGBIRD_ICL	Rev SA
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Main Func = 1D05V

OFFPAGE

[50] 1D8V_CPU_AUX_PG — PR5450 0R2J-2-GP — PWR_VNN_EN

PWR_1D05A_EN — PR5454 0R2J-2-GP — PWR_VNN1D05_POK1

[17,40,55,81] PM_SLP_S3# — PR5452 0R2J-2-GP — PWR_VNN1D05_VID

OFFPAGE-GAP

PWR_VNN — R5499 DY D01R2J-L-GP — 1D05V_VNN_BYPASS

PWR_1D05V — R5498 DY D01R2J-L-GP — 1D05V_S5_BYPASS

3D3V_S5

PR5420 100KR2J-1-GP — PWR_VNN1D05_POK1

PR5421 100KR2J-1-GP — PWR_VNN1D05_POK2

Design Current=0.2A

DFE252012F-1R0M=P2

PWR_VNN — PL5401 IND-1UH-363-GP

PC5411 SC10U6D3V3MX-DL-GP

PC5412 SC10U6D3V3MX-DL-GP

Design Current=0.2A

1239AS-H-100N=P2

PWR_1D05V — PL5402 IND-10UH-271-GP

PR5408 7K5R2F-1-GP

PR5407 10KR2F-2-GP

PC5410 SC10U6D3V3MX-DL-GP

PR5419 0R0402-PAD-1-GP — PWR_VNN

PC5401 SC1U10V2KX-1DLGP

5V_S5 — PR5413 2D2R2J-GP

PC5402 SC10U6D3V3MX-DL-GP

PR5422 0R0402-PAD-1-GP — PWR_VNN1D05_VIN1

5V_S5 — PR5410 0R0402-PAD-1-GP — PWR_VNN1D05_VIN2

PC5403 SC10U6D3V3MX-DL-GP

PWR_VNN1D05_VID

PWR_VNN1D05_BOOT1R — PC5404 SCD1U25V2KX-1-DL-GP — PWR_VNN1D05_BT1

PWR_VNN1D05_BOOT2R — PC5405 SCD1U25V2KX-1-DL-GP — PWR_VNN1D05_BT2

PC5406 DY SCD1U16V2KX-3DLGP — PWR_VNN1D05_POK1

PC5407 DY SCD1U16V2KX-3DLGP — PWR_VNN1D05_POK2

PR5423 0R2J-2-GP — PWR_VNN1D05_LX2

PR5401 0R2J-2-GP — PWR_VNN1D05_LX1

PU5401

VCC	8	EN1	15 PWR_VNN_EN
VIN1	11	EN2	6 PWR_1D05A_EN
VIN2	10	LX1	1 PWR_VNN1D05_LX1
VID	13	LX2	4 PWR_VNN1D05_LX2
BOOT1	2	FB2	5 PWR_VNN1D05_FB2
BOOT2	3	VOUT1	16 PWR_VNN1D05V_VOUT1
POK1	14	AGND	17
POK2	7	PGND	9, 12

APW8738AQBI-TRG-1-GP

074.08738.0073

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER(APW8738A_VNN1D05)***

Size	Document Number	Rev
A3	*MOCKINGBIRD_ICL*	*SA*

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Main Func = LCD

From CPU

[4] eDP_TX_CPU_N0
[4] eDP_TX_CPU_P0
[4] eDP_TX_CPU_N1
[4] eDP_TX_CPU_P1
[4] eDP_AUX_CPU_N
[4] eDP_AUX_CPU_P
[4] eDP_HPD_CPU
[4] EDP_VDD_EN
[4] L_BKLT_CTRL

From EC

[24,55] PANEL_BKEN
[17,40,54,81] PM_SLP_S3#

FOR TESTING

[20] DBC_PANEL_EN
[24] LCD_VCC_TEST_EN
[24] LCD_TST
[24] CABLE2_OCP#
[24] PANEL_MONITOR
[66] 3D3V_LCDVDD_R
[20,70] SENSOR_I2C_SDA
[20,70] SENSOR_I2C_SCL
[20] GSEN_INT1_C
[24,55] PANEL_BKEN

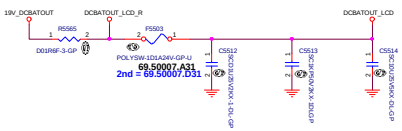
Main Func = Touch panel

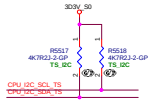
[20] CPU_I2C_SDA_TS
[20] CPU_I2C_SCL_TS
[3] TOUCH_PANEL_INTR#
[24] TOUCH_REPORT_SW
[3] TOUCH_PANEL_DET#
[20] TOUCH_PANEL_PD#

Main Func = CAMERA

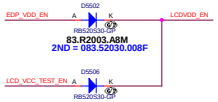
[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SCL_CODEC
[27] DMIC_SDA_CODEC
[19] DMIC_PCH_CLK_Q
[19] DMIC_PCH_DATA_Q

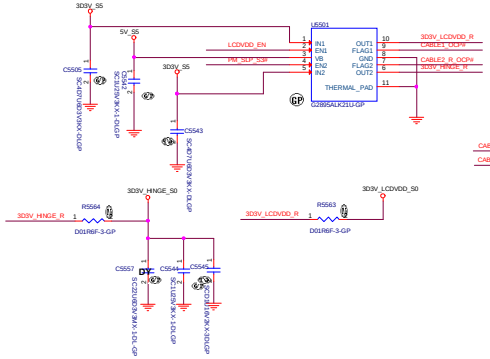
INVERTER POWER



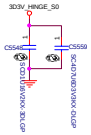


Hinge up cable protection

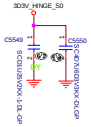




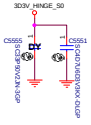
MIC POWER



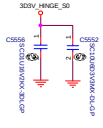
CAMERA POWER

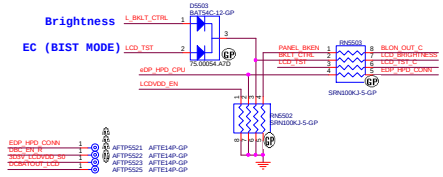


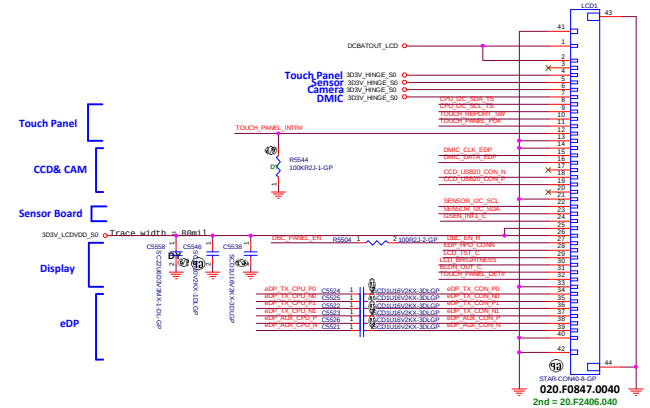
SENSOR POWER



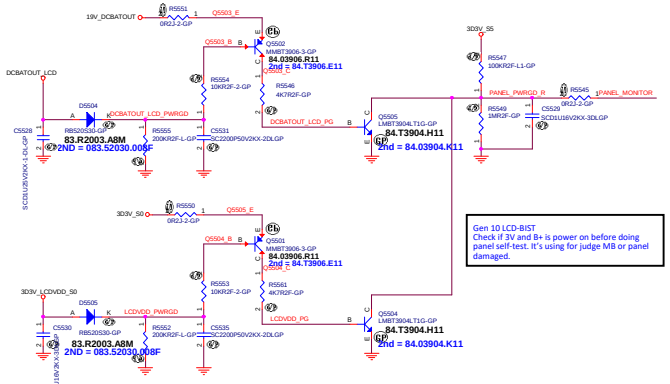
TOUCH PANEL POWER





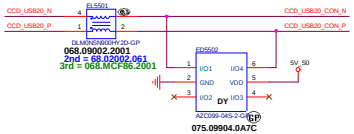


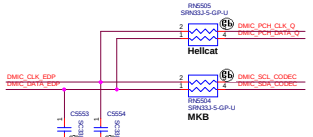
PANEL_PWRGD CIRCUIT



Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.

Main Func = CAMERA





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: Custom
Document Number: MOCKINGBIRD_ICL
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Date: Tuesday, September 17, 2019
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SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0
[4] HDMI_DDI_TX_P0
[4] HDMI_DDI_TX_N1
[4] HDMI_DDI_TX_P1
[4] HDMI_DDI_TX_N2
[4] HDMI_DDI_TX_P2
[4] HDMI_DDI_TX_N3
[4] HDMI_DDI_TX_P3

[4] CPU_DPB_CTRL_CLK
[4] CPU_DPB_CTRL_DATA
[4] CPU_DISP_HPDB

HDMI_DDI_TX_N3 C5701 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_P3 C5704 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_N0 C5705 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_P0 C5703 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_N1 C5707 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_P1 C5706 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_N2 C5708 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_P2 C5709 1 — SCD1U16V2KX-3DLGP — HDMI_DDI_TX_CON_P2

0503

5V_S0
R57051 470R2F-GP
R57591 470R2F-GP
R57731 470R2F-GP
R57741 470R2F-GP
R57751 470R2F-GP
R57761 470R2F-GP
R57771 470R2F-GP
R57781 470R2F-GP
HDMI_PLL_GND
Q5701 PJE8408-R1-00001-GP

D5701 RB520S30-GP
D5702 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
83.R2003.A8M
2ND = 083.52030.008F

0614 Layout HT

HDMI_SCL_R
HDMI_SDA_R
RN5702 SRN2K2J-1-GP
3D3V_S0
Part Reference = Q5702
CPU_DPB_CTRL_CLK
HDMI_SCL_CON
CPU_DPB_CTRL_DATA
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
HDMI_SDA_CON

HDMI_DDI_TX_CON_N0 — ER5701 150R2J-L1-GP-U — HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1 — ER5702 150R2J-L1-GP-U — HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2 — ER5703 150R2J-L1-GP-U — HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N3 — ER5704 150R2J-L1-GP-U — HDMI_DDI_TX_CON_P3

5V_S0 — F5701 POLYSW-1D1A6V-9-GP-U 69.48001.081 — 5V_HDMI
2ND = 69.50011.081
3RD = 69.50013.101

HDMI CONN

5V_HDMI
SCD1U16V2KX-3DLGP C5702
HDMI1
+5V_POWER
SCL
SDA
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
HDMI (A_Type)
GND
SKT-HDMI23-211-GP
022.10025.0421

3D3V_S0
HDMI_HPD_B R57101 2 150KR2F-L-GP HDMI_DET_CON
Q5703 LMBT3904LT1G-GP
84.T3904.H11
CPU_DISP_HPDB R57121 0R2J-2-GP
HDMI_HPD_E
R5709 100KR2J-1-GP
R5711 200KR2F-L-GP

EMI Request:

HDMI_DDI_TX_CON_P0 — ED5704 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_N0 — ED5705 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_P1 — ED5706 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_N1 — ED5707 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_P2 — ED5708 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_N2 — ED5709 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_P3 — ED5710 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DDI_TX_CON_N3 — ED5711 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_DET_CON — ED5712 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_SCL_CON — ED5713 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF
HDMI_SDA_CON — ED5714 PESD5V0H1BSFYL-GP-U1 — 083.5V0H1.00AF

<Core Design>

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21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: Custom
Document Number: MOCKINGBIRD_ICL
Rev: SA
Date: Tuesday, September 17, 2019
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Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] WLAN_CLKREQ_CPU_N

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

Single end

[3] BLUETOOTH_EN
[21] WIFI_RF_EN
[17,63,66,76,91] PLT_RST#
[18,24] SUS_CLK

Debug

Power EN (Madesimo)

[15,21] CNV_BRI_DT_R
[15,21] CNV_RGI_DT
[19] CLKREQ_CNV
[19] CNV_RF_REST#
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_BRI_RSP
[21] CNV_RGI_RSP
[24] JIO3_PCIE_WAKE#

3D3V_S5 — R6140 D01R5F-GP — 3D3V_WLAN

1.1A

C6110 SCD1U16V2KX-3DLGP
C6106 SC10U6D3V3MX-DL-GP
C6109 SCD1U16V2KX-3DLGP

AFTE14P-GP AFTP6101 — 3D3V_WLAN
AFTE14P-GP AFTP6105 — WLAN_CLKREQ_CPU_N
AFTE14P-GP AFTP6106 — WIFI_RF_EN_R
AFTE14P-GP AFTP6107 — BLUETOOTH_EN_R
AFTE14P-GP AFTP6108 — PLT_RST#
AFTE14P-GP AFTP6109 — BT_USB20_CON_N
AFTE14P-GP AFTP6110 — BT_USB20_CON_P
AFTE14P-GP AFTP6111 — JIO3_PCIE_WAKE#

3D3V_WLAN — R6145 10KR2J-3-GP DY — WIFI_RF_EN — R6144 0R2J-2-GP DY — WIFI_RF_EN_R

3D3V_WLAN — R6146 10KR2J-3-GP DY — BLUETOOTH_EN — R6143 0R2J-2-GP DY — BLUETOOTH_EN_R

3D3V_WLAN — WLAN1 — NGFF_KEY_E_75P — SKT-NGFF75P-164-GP

76	76	77	77
74	3_3VAUX	75	GND
72	3_3VAUX	73	RESERVED#73 — CNV_WT_CLKP
70	RESERVED#70	71	RESERVED#71 — CNV_WT_CLKN
68	RESERVED#68	69	GND
66	RESERVED#66	67	RESERVED#67/2ND_LANE_PERN1 — CNV_WT_DP0
64	GPIO0_NFC_RESET#/MGPIO7 — CLKIN_XTAL_LCP_R	65	RESERVED#65/2ND_LANE_PERP1 — CNV_WT_DN0
62	NFC_I2C_IRQ/MGPIO5	63	GND
60	NFC_I2C_SM_CLK	61	RESERVED#61/2ND_LANE_PETN1 — CNV_WT_DP1
58	NFC_I2C_SM_DATA	59	RESERVED#59/2ND_LANE_PETP1 — CNV_WT_DN1
56	W_DISABLE#1 — WIFI_RF_EN_R	57	GND
54	RESERVED#54/W_DISABLE#2 — BLUETOOTH_EN_R	55	PEWAKE0# — JIO3_PCIE_WAKE#
52	PERST0# — PLT_RST#	53	CLKREQ0# — WLAN_CLKREQ_CPU_N
50	SUSCLK_32KHZ — SUSCLK_WLAN	51	GND
48	COEX1	49	REFCLKN0 — WLAN_CLK_CPU_N
46	COEX2	47	REFCLKP0 — WLAN_CLK_CPU_P
44	COEX3	45	GND
42	CLINK_CLK	43	PERN0 — WLAN_PCIE_RX_N
40	CLINK_DATA	41	PERP0 — WLAN_PCIE_RX_P
38	CLINK_RESET	39	GND
36	UART_CTS — CNV_BRI_DT_R	37	PETN0 — WLAN_PCIE_TX_CON_N — C61071 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_N
34	UART_RTS — CNV_RGI_RSP_R	35	PETP0 — WLAN_PCIE_TX_CON_P — C61081 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_P
32	UART_TX — CNV_RGI_DT	33	GND
22	UART_RX — CNV_BRI_RSP_R	23	SDIO_RESET — CNV_WR_CLKP
20	UART_WAKE	21	SDIO_WAKE — CNV_WR_CLKN
18	GND	19	SDIO_DAT3
16	LED#2	17	SDIO_DAT2 — CNV_WR_DP0
14	PCM_OUT — BT_PCMOUT_CLKREQ0_R	15	SDIO_DAT1 — CNV_WR_DN0
12	PCM_IN	13	SDIO_DAT0
10	PCM_SYNC — BT_PCMFRM_CRF_RST_N	11	SDIO_CMD — CNV_WR_DP1
8	PCM_CLK	9	SDIO_CLK — CNV_WR_DN1
6	LED#1	7	GND
4	3_3VAUX	5	USB_D- — BT_USB20_CON_N
2	3_3VAUX	3	USB_D+ — BT_USB20_CON_P
		1	GND
NP2	NP2	NP1	NP1

CNV_RGI_RSP — R6109 22R2J-2-GP — CNV_RGI_DT_R
CNV_BRI_RSP — R6118 22R2J-2-GP — CNV_BRI_RSP_R
CLKREQ_CNV — R6141 33R2J-2-GP
CNV_RF_REST# — R6142 33R2J-2-GP
R6134 75KR2F-GP — R6133 71K5R2F-1-GP — 3D3V_WLAN
SUS_CLK — R6135 33R2J-2-GP — SUSCLK_WLAN
R6106 10KR2J-3-GP — CLKIN_XTAL_LCP_R

062.10003.0B11

BT_USB20_CON_P — R6111 0R2J-2-GP — BT_USB20_P
BT_USB20_CON_N — R6110 0R2J-2-GP — BT_USB20_N

<Core Design>

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Title: NGFF WLAN CONN
Size: A3 | Document Number: MOCKINGBIRD_ICL | Rev: SA
Date: Tuesday, September 17, 2019 | Sheet 61 of 106

Main Func = M.2 SSD

[18] SSD_CLKREQ_CPU_N
[17,61,63,66,76,91] PLT_RST#

[16] SSD_DEVSLP
[18] SSD_CLK_CPU_P
[18] SSD_CLK_CPU_N
[16] SSD_PCIE_TX_P
[16] SSD_PCIE_TX_N
[16] SSD_PCIE_RX_N
[16] SSD_PCIE_RX_P
[16] SSD_PCIE_TX_P3
[16] SSD_PCIE_TX_N3
[16] SSD_PCIE_RX_P3
[16] SSD_PCIE_RX_N3
[16] SSD_PCIE_TX_P2
[16] SSD_PCIE_TX_N2
[16] SSD_PCIE_RX_P2
[16] SSD_PCIE_RX_N2
[16] SSD_PCIE_TX_P1
[16] SSD_PCIE_TX_N1
[16] SSD_PCIE_RX_P1
[16] SSD_PCIE_RX_N1

[16] M2_SSD_PEDET
[64] M2_PCIE_LED#
[24] SSD_SCP#

3D3V_S0
R6355
D01R5F-1-GP
3D3V_SSD1
SC33P50V2JN-3DLGP
C6347
SC82U25V2KX-4-GP
C6341
SC10U6D3V3MX-GP
C6340

SSD M.2 CONN

SSD1
NP2
NP1
SUSCLK_32KHZ
PEDET(OC_PCIE/GND_SATA)
SSD_CLKREQ_CPU_N
PLT_RST#
SSD_DEVSLP
R6352
0R2J-2-GP
MSATA_DEVSLP_R
M2_PCIE_LED#
R6354
SSD_SCP#
R6356
0R2J-2-GP
M2_PCIE_LED#_R
SSD_SCP1#
SKT-NGFF75P-224-GP
NGFF_KEY_M 75P

R6353
100KR2J-1-GP
M2_SSD_PEDET
SSD_CLK_CPU_P
SSD_CLK_CPU_N
SSD_SATA_TX_CON_P
SSD_SATA_TX_CON_N
C6343
C6345
SCD22U10V2KX-2GP
SSD_PCIE_TX_P
SSD_PCIE_TX_N
SSD_PCIE_RX_N
SSD_PCIE_RX_P
SSD_PCIE_TX_CON_P3
SSD_PCIE_TX_CON_N3
C6344
C6346
SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_TX_CON_P2
SSD_PCIE_TX_CON_N2
C6339
C6342
SSD_PCIE_TX_P2
SSD_PCIE_TX_N2
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_TX_CON_P1
SSD_PCIE_TX_CON_N1
C6335
C6337
SSD_PCIE_TX_P1
SSD_PCIE_TX_N1
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1

PCIE:1 SATA:0

062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-12.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 3/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	108 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:
1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled OOBs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled OOBs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled OOBs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General/Differential Signals Design Guidelines" for PCIe* Gen 3 motherboard design requirements for AC coupling capacitors.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen1 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled OOBs / Devices.**

M.2 SSD2

[16] SSD_PCIE_TX_P9
[16] SSD_PCIE_TX_N9
[16] SSD_PCIE_RX_N9
[16] SSD_PCIE_RX_P9

[16] SSD_PCIE_TX_P10
[16] SSD_PCIE_TX_N10
[16] SSD_PCIE_RX_P10
[16] SSD_PCIE_RX_N10

[16] SSD_PCIE_TX_P11
[16] SSD_PCIE_TX_N11
[16] SSD_PCIE_RX_P11
[16] SSD_PCIE_RX_N11

[16] SSD_PCIE_TX_P12
[16] SSD_PCIE_TX_N12
[16] SSD_PCIE_RX_P12
[16] SSD_PCIE_RX_N12

[18] SSD2_CLK_CPU_P
[18] SSD2_CLK_CPU_N
[18] SSD2_CLKREQ_CPU_N

[16] SSD2_DEVSLP
[16] M2_SSD2_PEDET

3D3V_S0
R6351
D01R5F-1-GP
MKB
3D3V_SSD2
SC33P50V2JN-3DLGP
C6320
C6321
SC82U25V2KX-4-GP
C6319
C6322
SC10U6D3V3MX-GP
C6323

SSD M.2 CONN

SSD2
NP2
NP1
SUSCLK_32KHZ
PEDET(OC_PCIE/GND_SATA)
SSD2_CLKREQ_CPU_N
PLT_RST#
SSD2_DEVSLP
R6350
0R2J-2-GP
MSATA_DEVSLP2_R
M2_PCIE_LED#
R6357
SSD_SCP#
SSD_SCP2#
SKT-NGFF75P-224-GP
NGFF_KEY_M 75P

R6349
100KR2J-1-GP
M2_SSD2_PEDET
SSD2_CLK_CPU_P
SSD2_CLK_CPU_N
SSD_SATA_TX_CON_P12
SSD_SATA_TX_CON_N12
C6324 MKB
C6325 MKB
SCD22U10V2KX-2GP
SSD_PCIE_TX_P12
SSD_PCIE_TX_N12
SSD_PCIE_RX_N12
SSD_PCIE_RX_P12
SSD_PCIE_TX_CON_P11
SSD_PCIE_TX_CON_N11
C6326 MKB
C6327 MKB
SSD_PCIE_TX_P11
SSD_PCIE_TX_N11
SSD_PCIE_RX_P11
SSD_PCIE_RX_N11
SSD_PCIE_TX_CON_P10
SSD_PCIE_TX_CON_N10
C6328 MKB
C6329 MKB
SSD_PCIE_TX_P10
SSD_PCIE_TX_N10
SSD_PCIE_RX_P10
SSD_PCIE_RX_N10
SSD_PCIE_TX_CON_P9
SSD_PCIE_TX_CON_N9
C6330 MKB
C6331 MKB
SSD_PCIE_TX_P9
SSD_PCIE_TX_N9
SSD_PCIE_RX_P9
SSD_PCIE_RX_N9

PCIE:1 SATA:0

062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21
MKB

<Core Design>

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2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA
Size: A2
Document Number: Mockingbird_CML
Rev: SA
Date: Tuesday, September 17, 2019
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Main Func = Power BTN

NONE FINGER PRINT 才會上件

Power button

[24] KBC_PWRBTN#

[66] KBC_PWRBTN#_R

Layout note:
G6401 place to buttom
G6402 place to top

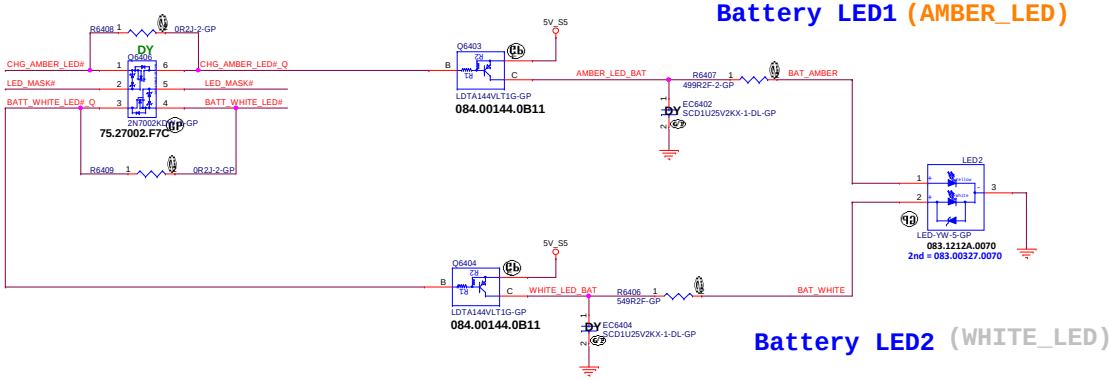
Main Func = Battery LED

Low actived from KBC GPIO

[24] LED_MASK#

[24] CHG_AMBER_LED#

[24] BATT_WHITE_LED#



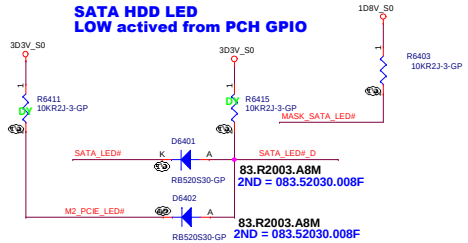
Main Func = HDD LED

[20,24] MASK_SATA_LED#

[18] SATA_LED#

[63] M2_PCIE_LED#

[63] SATA_LED#_D

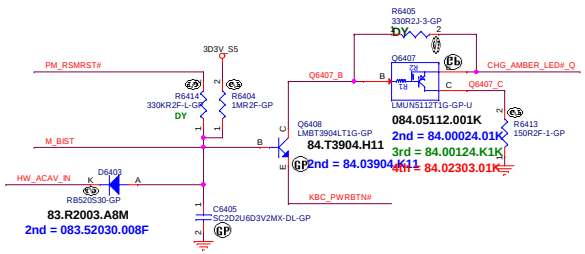


Main Func = M-BIST

[17,18] PM_RSMRST#

[24] M_BIST

[24,44] HW_ACAV_IN



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

<Core Design>

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Title: LED Board&Power Button

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

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Main Func = KB

0513

[24] CAP_LED#_R

[4] KB_DET#

[20] KB_LED_BL_DET

[24] KB_LED_PWM

[24] KSO00 KSO01 KSO02 KSO03 KSO04 KSO05 KSO06 KSO07 KSO08 KSO09 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16

[24] KSI[0..7] KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

Keyboard Backlight (Reserved)

5V_S0 → F6502 KBBL POLYSW-1D1A6V-9-GP-U 69.48001.081

+5V_KB_BL

C6501 SCD1U16V2KX-3DLGP

KB_LED_BL_DET → R6503 KBBL 51KR2J-1-GP

KBBL R6507 100KR2J-1-GP

KB_LED_DET_C

KB_BL_CTRL#

KBBL1 ACES-CON4-90-GP-U 020.K0298.0004

AFTP6565

KB Backlight Power Consumption: 285mA max.

KB_LED_PWM → Q6501 PJA3402-R1-00001-GP 084.03402.0031 KBBL

DY R6505 100KR2J-1-GP

+5V_KB_BL → AFTP6506

KB_LED_DET_C → AFTP6566

KB_BL_CTRL# → AFTP6567

KB_LED_DET_C → EC6501 SCD1U16V2KX-3DLGP DY

KB_BL_CTRL# → EC6503 SCD1U16V2KX-3DLGP DY

CAP LED Control

LOW actived from KBC GPIO

CAP_LED#_R → Q6502 LDTA144VLT1G-GP 084.00144.0B11

5V_S0 → R6506 1KR2J-1-GP → CAP_LED

Internal Keyboard Connector

KB1 ACES-CON30-29-GP 020.K0254.0030

AFTP6532 CAP_LED
AFTP6603 KSO10
AFTP6504 KSO11
AFTP6516 KSO09
AFTP6539 KSO14
AFTP6535 KSO13
AFTP6515 KSO15
AFTP6508 KSO16
AFTP6538 KSO12
AFTP6520 KSO00
AFTP6510 KSO02
AFTP6517 KSO01
AFTP6518 KSO03
AFTP6505 KSO08
AFTP6512 KSO06
AFTP6534 KSO07
AFTP6522 KSO04
AFTP6536 KSO05
AFTP6507 KSI0
AFTP6502 KSI3
AFTP6540 KSI1
AFTP6513 KSI5
AFTP6533 KSI2
AFTP6521 KSI4
AFTP6511 KSI6
AFTP6523 KSI7
AFTP6519 KB_DET#
AFTP6537

Main Func = TPAD

0513

[24] CLK_TP_SIO_I2C_DAT
[24] DAT_TP_SIO_I2C_CLK

[20,66] CPU_I2C_SCL_P0
[20,66] CPU_I2C_SDA_P0

[3,24] TOUCHPAD_INTR#
[24] PTP_DIS#

3D3V_S0 → R6502 0R2J-2-GP → TP_VDD

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

TP_VDD

TP side has pull high

TOUCHPAD_INTR# → R6511 10KR2J-3-GP

Support PTP

PS2: DAT_TP_SIO_I2C_CLK, CLK_TP_SIO_I2C_DAT

I2C: CPU_I2C_SCL_P0, CPU_I2C_SDA_P0

RN6502 SRN0J-6-GP

R6513 0R2J-2-GP → I2C1_SCL_R

R6512 0R2J-2-GP → I2C1_SDA_R

SC139P50V2JN-3GP DY DY

TP_VDD → RN6503 SRN2K2J-1-GP → I2C1_SCL_R, I2C1_SDA_R

Precision Touch Pad Connector

TP_VDD → C6505 SCD1U16V2KX-3DLGP

TP1 PTWO-CON8-16-GP 020.K0255.0008 2nd = 020.K0151.0008

I2C1_SDA_R
I2C1_SCL_R
TOUCHPAD_INTR#
PTP_DIS#

AFTP6531

TP_VDD → AFTP6529

I2C1_SCL_R → AFTP6528
I2C1_SDA_R → AFTP6527
TOUCHPAD_INTR# → AFTP6525
PTP_DIS# → AFTP6526

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 65 of 106

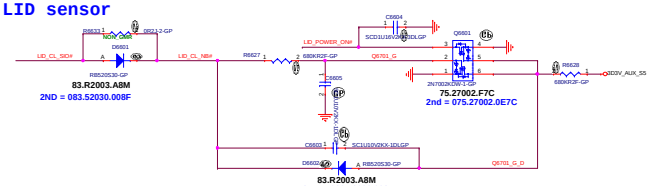
Main Func = IO Connector

USB2.0 Power

Pin define by follow layout routing

074.06288.009B

LID sensor

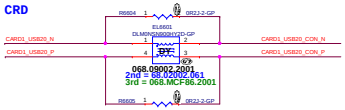


83.R2003.ABM
2ND = 083.52030.008F

75.27002.F7C
2nd = 075.27002.0E7C

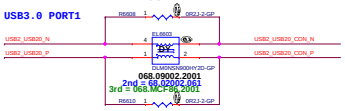
83.R2003.ABM
2ND = 083.52030.008F

CRD



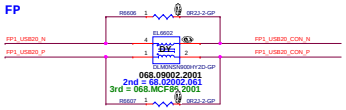
068.09002.2001
2nd = 68.02002.061
3rd = 068.MCF86.2001

USB3.0 PORT1



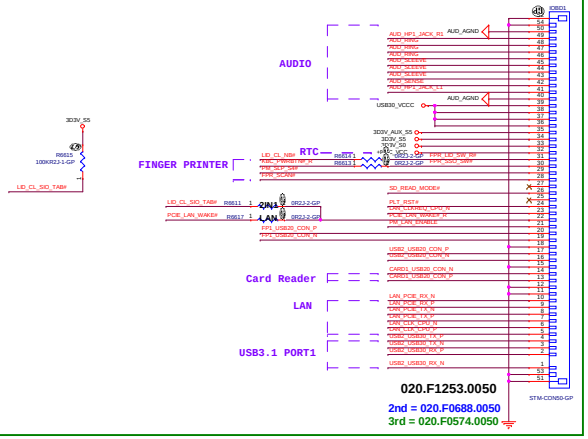
068.09002.2001
2nd = 68.02002.061
3rd = 068.MCF86.2001

FP

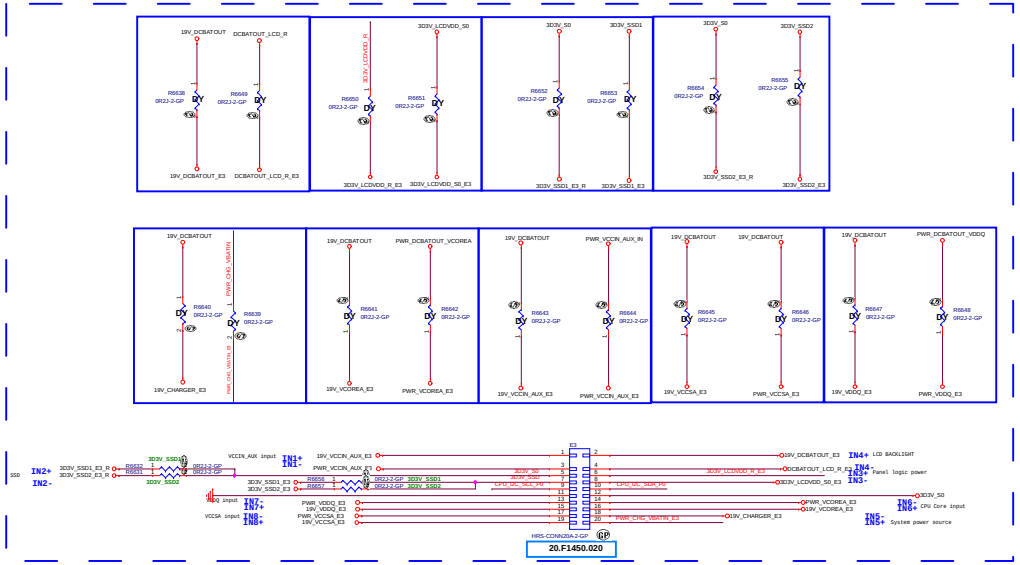


068.09002.2001
2nd = 68.02002.061
3rd = 068.MCF86.2001

I/O Board Connector



020.F1253.0050
2nd = 020.F0688.0050
3rd = 020.F0574.0050



20.F1450.020

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Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A4	MOCKINGBIRD_ICL	SA

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AUDIO

[27,29] AUD_RING
[27,29] AUD_SLEEVE
[29] AUD_HP1_JACK_L1
[29] AUD_HP1_JACK_R1
[27] AUD_SENSE

CRD

[16] CARD1_USB20_N
[16] CARD1_USB20_P
[33] SD_READ_MODE#

USB3.0

PORT1

[16] USB2_USB30_RX_N
[16] USB2_USB30_RX_P
[16] USB2_USB30_TX_N
[16] USB2_USB30_TX_P
[16] USB2_USB20_N
[16] USB2_USB20_P

USB CONTROL

[6] USB_OC1#
[24,35] USB_PWR_ENF

LAN

[18] LAN_PCIE_RX_N
[18] LAN_PCIE_RX_P
[18] LAN_PCIE_TX_N
[18] LAN_PCIE_TX_P
[18] LAN_CLK_CPU_N
[18] LAN_CLK_CPU_P
[18] LAN_CLKREQ_CPU_N
[24] PM_LAN_ENABLE
[24] PCIE_LAN_WAKE#

FP

[16] FP1_USB20_N
[16] FP1_USB20_P
[24] FPR_SCAN#
[64] KBC_PWRBTN#_R
[17,40,51] PM_SLP_S4#

[20,24] LID_CL_SIO#
[24] LID_POWER_ON#
[24] LID_CL_SIO_TABF
[17,61,63,76,91] PLT_RST#
[20,65] CPU_I2C_SCL_P0
[20,65] CPU_I2C_SDA_P0
[44] PWR_CHG_VBATIN
[55] 3D3V_LCDVDD_R

Main Func = Debug

ESPI

[18,24] ESPI_CLK

[18,24] ESPI_RESET#

[18,24] ESPI_CS#

[18,24] ESPI_IO[3..0]

ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0

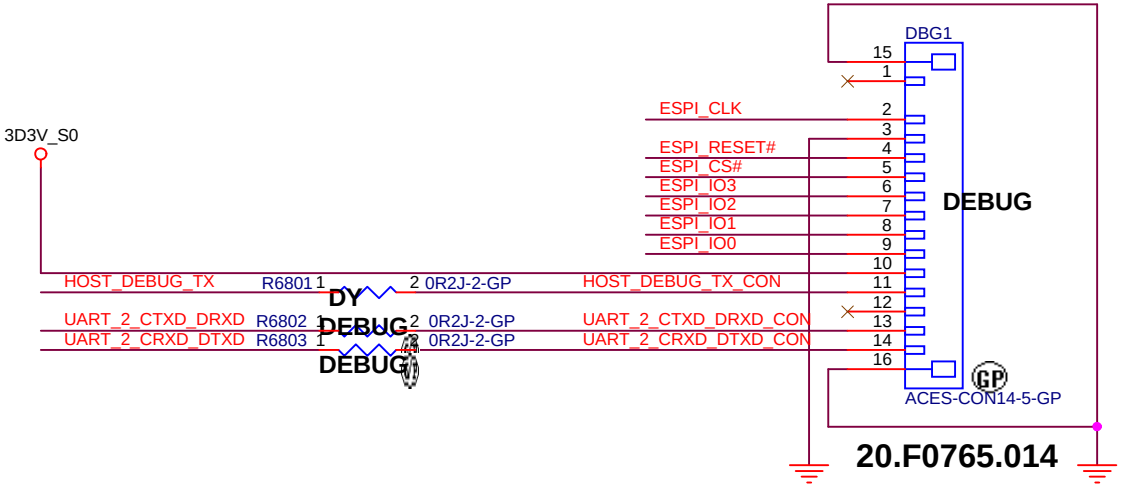
UART

[24] HOST_DEBUG_TX

[20] UART_2_CTXD_DRXD

[20] UART_2_CRXD_DTXD

ESPI Debug Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

Size	Document Number	Rev
A4	*MOCKINGBIRD_ICL*	*SA*

Date: Tuesday, September 17, 2019 Sheet 68 of 106

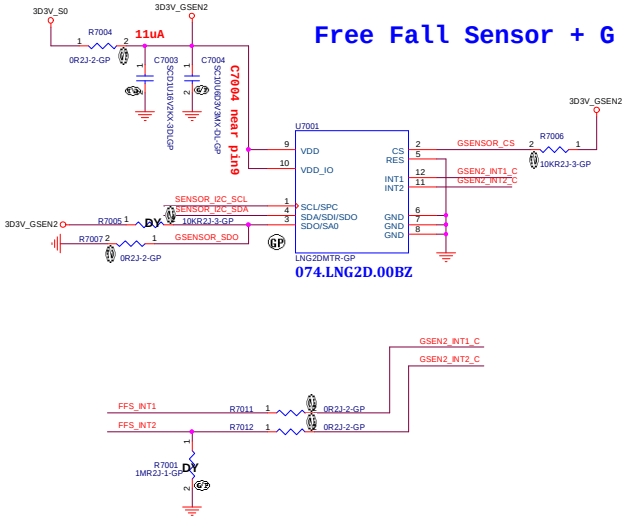
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

[20] GSEN2_INT1_C
[20,55] SENSOR_I2C_SCL
[20,55] SENSOR_I2C_SDA
[20] FFS_INT1
[19] FFS_INT2

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
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Title: Free Fall Sensor

Size	Document Number	Rev
A2	MOCKINGBIRD_ICL	SA

Date: Tuesday, September 17, 2019 Sheet 70 of 106

Main Func =TI

[74] PD_VBUS_C_CTRL1

EC

[24] UPD1_SMBCLK
[24] UPD1_SMBDAT

[74] VBUS_P_CTRL

[24] CCG5C_I2C_INT#

0513

MUX TUSB546

[73] I2C_DATA_PD
[73] I2C_CLK_PD

[4,73] DP1_HPD_CPU

[73] CCG5_SBU1
[73] CCG5_SBU2

[74] NX5P3363_FO

TYPE-C CONNECTOR

[73] USB1_CC1
[73] USB1_CC2
[73] TOP_MUX_P_L
[73] TOP_MUX_N_L
[73] BOT_MUX_P_L
[73] BOT_MUX_N_L
[73] USB1_SBU1
[73] USB1_SBU2

PCH

[16] USB4_USB20_P
[16] USB4_USB20_N

From System

3D3V_S5

VCC3PD_1

D7202 SBA0520Q-R1-00001-GP-U

For debattery

3D3V_S5 — D7203 SBA0520Q-R1-00001-GP-U — VCC3PD — R7211 0R2J-2-GP — VDDD

083.00520.0F8F

2nd = 083.05S40.001F

90829-SA_James add D7203
90829-SA_James add R7211

Power

VDDD

C7203 SCD1U10V2KX-3DLGP
C7204 SCD1U10V2KX-3DLGP
C7207 SCD1U10V2KX-1DLGP

VCC3PD_1

C7210 SCD1U10V2KX-3DLGP
C7212 SCD1U10V2KX-1DLGP

90829-SA_James add R7210

VCC3PD_1

R7217 100KR2J-1-GP
R7223 100KR2J-1-GP

PD_VBUS_C_CTRL1
VBUS_P_CTRL_C

Q7201 2N7002KDW-1-GP

PD_VBUS_C_CTRL1_C
VBUS_P_CTRL

R7218 100KR2J-1-GP
R7222 100KR2J-1-GP

2nd = 075.27002.0E7C
75.27002.F7C

U7201

VDDD
VCC3PD_1
5V_S5
20V_VCCPD_VBUS

SCD1U16V2KX-3DLGP
C7218 PD_VCCD

VDDD 31 32
VDDIO 19
VSYS 33
VCCD 8
V5V 22
VBUS 1 40
CSP
CSN

CCG5C_I2C_INT#
UPD1_SMBCLK
UPD1_SMBDAT
I2C_INT_EC 15
I2C_SCL_SCB1_EC 17
I2C_SDA_SCB1_EC 16

CCG5_MOD_ID2 5
I2C_CLK_PD 4
I2C_DATA_PD 3
I2C_INT_AR
I2C_SCL_SCB2_AR
I2C_SDA_SCB2_AR

CCG5_MOD_ID1 21
UCSS_LIM 20
SCL3/VSEL_1
SDA3/VSEL_2

NX5P3363_FO 13
CCG5_PROCHOT# 14
UV_OCP_TRIP/SCL_4
OVP_TRIP/SDA_4

CCG5_SWD_CLK/CCG5_I2C_CFG_EC 2
CCG5_SWD_IO 6
SWD_CLK/I2C_CFG
SWD_IO/AR_RST

VBUS_P_CTRL 11
VBUS_C_CTRL 12
CC1 9
CC2 7
DPLUS_SYS 23
DMINUS_SYS 24
UART_TX 29
UART_RX 30
DPLUS_TOP 28
DMINUS_TOP 27
DPLUS_BOT 26
DMINUS_BOT 25
SBU1 35
SBU2 34
AUX_P 36
AUX_N 37
LSTX 38
LSRX 39
XRES# 10
HPD 18
GND 41

PD_VBUS_C_CTRL1_C
USB1_CC1
USB1_CC2
USB4_USB20_P
USB4_USB20_N
UPD1_SMBCLK
UPD1_SMBDAT
TOP_MUX_P_L
TOP_MUX_N_L
BOT_MUX_P_L
BOT_MUX_N_L
USB1_SBU1
USB1_SBU2
CCG5_SBU1
CCG5_SBU2
PD_XRES
CPD_DP_HPD_MUX

CYPD5126-40LQXIT-12-GP

071.05126.0P03

C7221 SC330P50V2KX-3-DL-GP
C7220 SC330P50V2KX-3-DL-GP

3D3V_S5

R7225 10KR2J-3-GP DY
R7226 10KR2J-3-GP DY
R7216 10KR2J-3-GP DY
NX5P3363_FO

CCG5_SWD_CLK/CCG5_I2C_CFG_EC
R7224 0R2J-2-GP
CCG5_SWD_IO

VDDD

R7207 10KR2J-3-GP DY
R7208 0R2J-2-GP
DP1_HPD_CPU
R7209 100KR2J-1-GP

PD_XRES
R7221 4K7R2J-2-GP
VDDD

C7219 SCD1U16V2KX-3DLGP DY

VDDD

RN7202 SRN2K2J-1-GP
I2C_CLK_PD
I2C_DATA_PD

3D3V_S5
R7202 100KR2J-1-GP
CCG5C_I2C_INT#

MOD ID Settings

VDDD
R7201 51KR2J-1-GP
CCG5_MOD_ID1
R7213 150KR2J-GP

MOD ID Settings

VDDD
R7212 100KR2J-1-GP DY
CCG5_MOD_ID2
R7214 100KR2J-1-GP

VDDD
R7219 1KR2F-3-GP DY
CCG5_SWD_CLK/CCG5_I2C_CFG_EC
R7220 1KR2F-3-GP DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB PD(CYPD5126)

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 72 of 106

Main Func = TYPEC MUX

DisplayPort Source

[4] DP2_DDI_TX_P0
[4] DP2_DDI_TX_N0
[4] DP2_DDI_TX_P1
[4] DP2_DDI_TX_N1
[4] DP2_DDI_TX_P2
[4] DP2_DDI_TX_N2
[4] DP2_DDI_TX_P3
[4] DP2_DDI_TX_N3

USB HOST

[16] USB4_USB30_RX_P
[16] USB4_USB30_RX_N
[16] USB4_USB30_TX_P
[16] USB4_USB30_TX_N

DisplayPort AUX

[4] DP2_AUX_CPU_P
[4] DP2_AUX_CPU_N

MUX I2C

[72] I2C_CLK_PD
[72] I2C_DATA_PD

DisplayPort HPD

[4,72] DP1_HPD_CPU

I2C/USB MUX

[72] CCG5_SBU1
[72] CCG5_SBU2

TypeC CC

[72] USB1_SBU1
[72] USB1_SBU2
[72] USB1_CC1
[72] USB1_CC2
[72] TOP_MUX_P_L
[72] TOP_MUX_N_L
[72] BOT_MUX_P_L
[72] BOT_MUX_N_L

For displayport function at dead battery condition

3D3V_SS
R73031 0R2J-2-GP
3D3V_MUX
C7312 SCD1U16V2KX-3DLGP
C7313 SCD1U16V2KX-3DLGP
C7309 SCD1U16V2KX-3DLGP
C7308 SCD1U16V2KX-3DLGP
C7314 SCD1U16V2KX-3DLGP
C7307 SCD1U16V2KX-3DLGP
C7311 SCD1U16V2KX-3DLGP
C7310 SCD1U16V2KX-3DLGP
C7305 SCD100U6D3VDM-CLK-GP
C7306 SCD100U6D3VDM-CLK-GP

R7306 10KR2J-3-GP DY
R7307 4K7R2J-2-GP DY
CAD_SNK
HPDIN

Slave address : 0X44

U7301 TUSB546-DCIRNQR-1-GP
071.00546.M001

DisplayPort Source
USB HOST
3D3V_MUX
R7301 100KR2J-1-GP DP2_AUX_C_N
R7302 100KR2J-1-GP DP2_AUX_C_P

R7320 R7318 R7344 R7325 R7341 R7327 R7323
1KR2J-1-GP DY
EQ0 EQ1 I2CEN DPEQ1 DPEQ0_A1 SSEQ1 SSEQ0_A0
R7321 R7319 R7343 R7340 R7342 R7322 R7324

FLIP/ POL	CTL0/ SWAP EN	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

DCI		Note: DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode & Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

20V_VCCPD_VBUS
3A
C7329 C7325 C7326 C7327 C7328 C7330
SCD1U25V2KX-1DLGP SCD22U25V2KX-1DLGP

20V_VCCPD_VBUS
R73471 0R2J-2-GP
ED7308 ED7309 SDR5K3SKXTDG-GP

20V_VCCPD_VBUS_R
USB1 SKT-USB39-1-GP
USB1_SSTX_CON_P1 USB1_SSTX_CON_N1 USB1_CC1 TOP_MUX_P TOP_MUX_N USB1_SBU1 USB1_SSRX_CON_N2 USB1_SSRX_CON_P2
USB1_SSTX_CON_P2 USB1_SSTX_CON_N2 USB1_CC2 BOT_MUX_P BOT_MUX_N USB1_SBU2 USB1_SSRX_CON_N1 USB1_SSRX_CON_P1
R7345 2MR2F-GP
R7346 2MR2F-GP
062.10009.0681

USB1_SSTX_C_P1 C7324 SCD1U16V2KX-3DLGP USB1_SSTX_CMC_P1 R7310 0R2J-2-GP USB1_SSTX_CON_P1
USB1_SSTX_C_N1 C7323 SCD1U16V2KX-3DLGP USB1_SSTX_CMC_N1 R7311 0R2J-2-GP USB1_SSTX_CON_N1
FILTER-4P-201-GP EL7303
068.10129.2021
3rd = 68.24500.201
2nd = 068.01210.2031

ED7302 AZ1043-04F-R7G-GP
USB1_SSTX_CON_N2 USB1_SSTX_CON_P2 USB1_SSRX_CON_N2 USB1_SSRX_CON_P2
USB1_SSTX_CON_N2 USB1_SSTX_CON_P2 USB1_SSRX_CON_N2 USB1_SSRX_CON_P2
075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003

USB1_SSRX_C_P1 C7331 SCD1U16V2KX-3DLGP USB1_SSRX_CMC_P1 R7312 0R2J-2-GP USB1_SSRX_CON_P1
USB1_SSRX_C_N1 C7332 SCD1U16V2KX-3DLGP USB1_SSRX_CMC_N1 R7313 0R2J-2-GP USB1_SSRX_CON_N1
FILTER-4P-201-GP EL7304
068.10129.2021
3rd = 68.24500.201
2nd = 068.01210.2031

ED7301 AZ1043-04F-R7G-GP
USB1_SSRX_CON_P1 USB1_SSRX_CON_N1 USB1_SSTX_CON_P1 USB1_SSTX_CON_N1
USB1_SSRX_CON_P1 USB1_SSRX_CON_N1 USB1_SSTX_CON_P1 USB1_SSTX_CON_N1
075.01043.0073
2nd = 075.08810.0A73
3rd = 075.73044.0003

USB1_SSRX_C_P2 C7333 SCD1U16V2KX-3DLGP USB1_SSRX_CMC_P2 R7314 0R2J-2-GP USB1_SSRX_CON_P2
USB1_SSRX_C_N2 C7334 SCD1U16V2KX-3DLGP USB1_SSRX_CMC_N2 R7315 0R2J-2-GP USB1_SSRX_CON_N2
EL7305 FILTER-4P-201-GP
2nd = 068.01210.2031
3rd = 68.24500.201
068.10129.2021

USB1_SSTX_C_P2 C7321 SCD1U16V2KX-3DLGP USB1_SSTX_CMC_P2 R7316 0R2J-2-GP USB1_SSTX_CON_P2
USB1_SSTX_C_N2 C7322 SCD1U16V2KX-3DLGP USB1_SSTX_CMC_N2 R7317 0R2J-2-GP USB1_SSTX_CON_N2
EL7306 FILTER-4P-201-GP
2nd = 068.01210.2031
3rd = 68.24500.201
068.10129.2021

0614 Layout HT

ED7304 AZ5315-02F-GP
BOT_MUX_P BOT_MUX_N
83.05315.0A0

ED7305 AZ5315-02F-GP
USB1_SBU1 USB1_SBU2
83.05315.0A0

ED7306 AZ5315-02F-GP
TOP_MUX_P TOP_MUX_N
83.05315.0A0

ED7307 AZ5315-02F-GP
USB1_CC1 USB1_CC2
83.05315.0A0

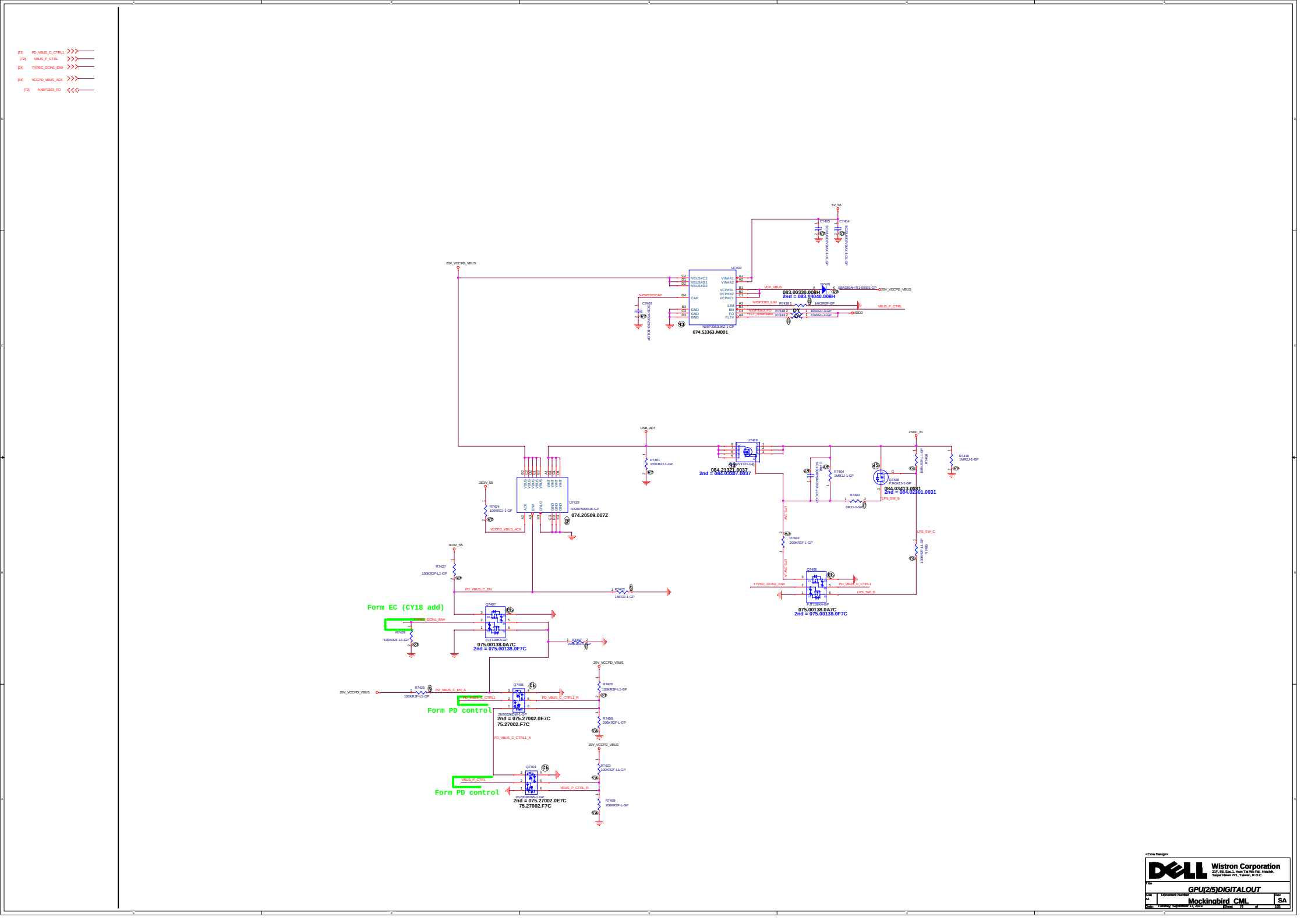
EL7301
TOP_MUX_N_L TOP_MUX_P_L TOP_MUX_N TOP_MUX_P
068.09002.2001
DLM0NSN900HY2D-GP

EL7302
BOT_MUX_P_L BOT_MUX_N_L BOT_MUX_P BOT_MUX_N
DLM0NSN900HY2D-GP
068.09002.2001

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Type-C&MUX(TUSB546)**
Size: Custom | Document Number: **MOCKINGBIRD_ICL** | Rev: **SA**
Date: Tuesday, September 17, 2019 | Sheet 73 of 105



<Core Design>

Wistron Corporation
22F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A1	Mockingbird_CML	SA

Date: Tuesday, September 17, 2013 Sheet 74 of 105

Main Func = dGPU

[18] GFX_CLK_CPU_P
[18] GFX_CLK_CPU_N
[4] DGPU_HOLD_RST#
[17,61,63,66,91] PLT_RST#
[85] VGACORE_VDD_SENSE_1
[85] VGACORE_GND_SENSE_1
[18] CLK_PCIE_PEG_REQ#
[16] GFX_PCIE_RX_P0
[16] GFX_PCIE_RX_N0
[16] GFX_PCIE_TX_P0
[16] GFX_PCIE_TX_N0
[16] GFX_PCIE_RX_P1
[16] GFX_PCIE_RX_N1
[16] GFX_PCIE_TX_P1
[16] GFX_PCIE_TX_N1

0508

dGPU Reset

73.01G08.EHG
2ND = 073.7S208.000G
3RD = 73.01G08.L04

084.08408.0031

071.0N17S.0000

OPS

1.05V +/- 30mV
3.3A

Place close VDD ball
Place close Chip

3.3V +/- 5%
210mA

POWER IC

Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

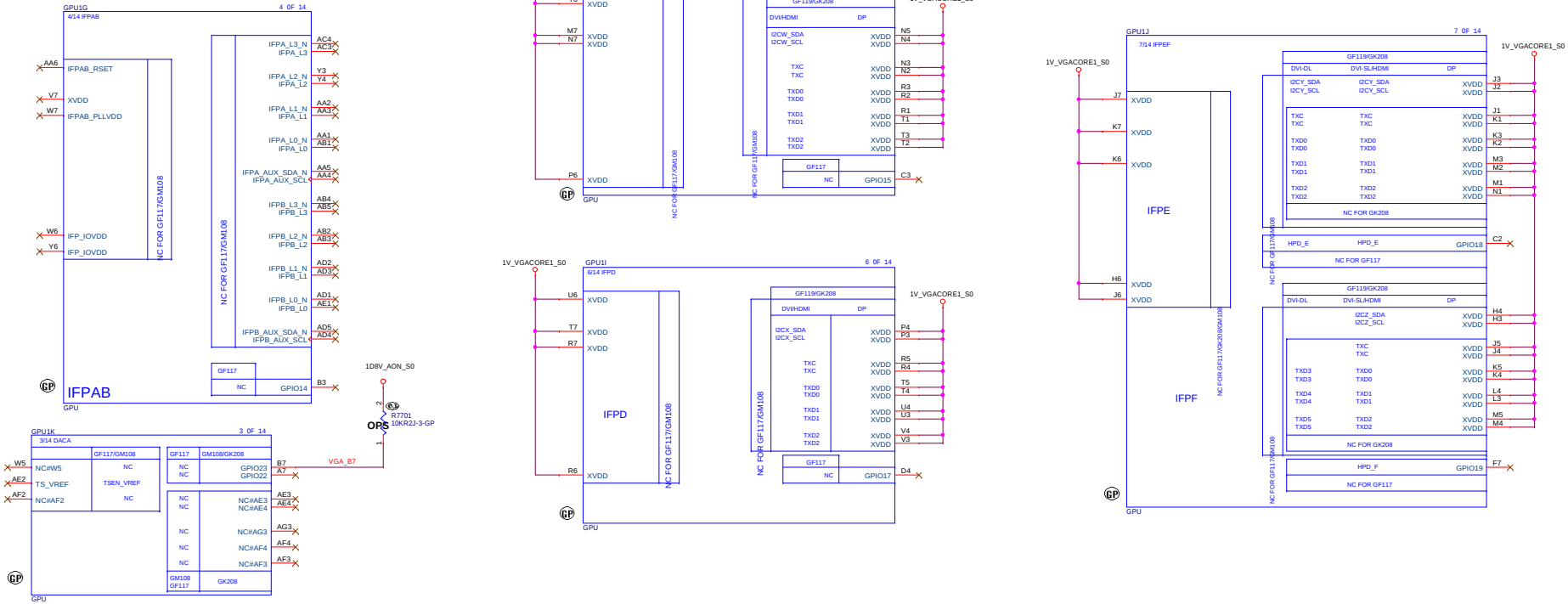
Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU(1/5)PEG
Size: Custom | Document Number: MOCKINGBIRD_ICL | Rev: SA
Date: Tuesday, September 17, 2013 | Sheet 76 of 105

Main Func = dGPU



<Core Design>

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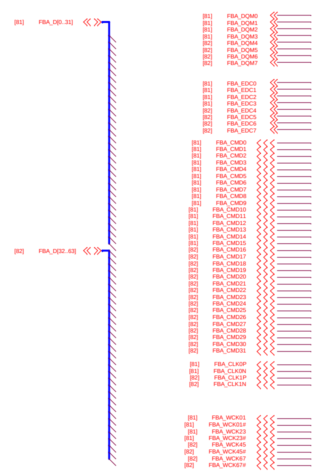
Taipei Hsien 221, Taiwan, R.O.C.

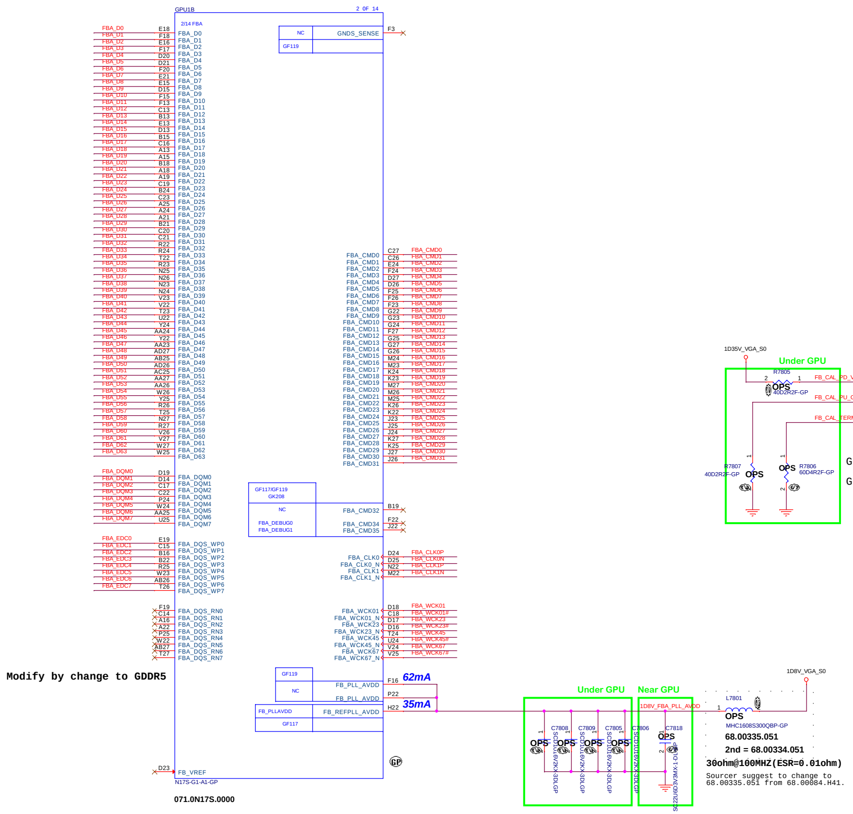
Title: GPU(2/5)DIGITALOUT

Size: A2 | Document Number: MOCKINGBIRD_ICL | Rev: SA

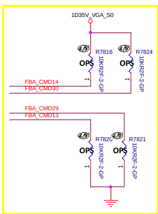
Date: Tuesday, September 17, 2019 | Sheet 77 of 106

Main Func = dGPU





Modify by change to GDDR5



Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

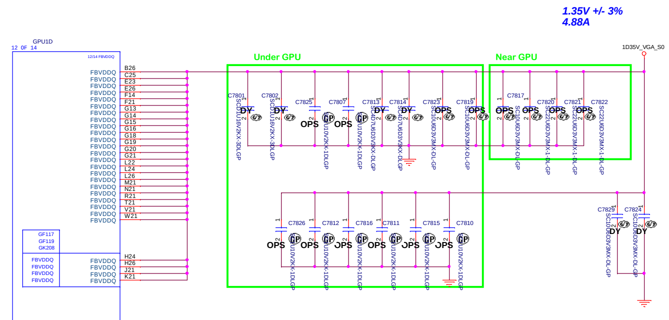


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

<Core Design>

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Title: GPU(3/5)VRAM I/F
Size: A1 | Document Number: MOCKINGBIRD_ICL | Rev: SA
Date: Tuesday, September 17, 2019 | Sheet 78 of 106

Main Func = dGPU

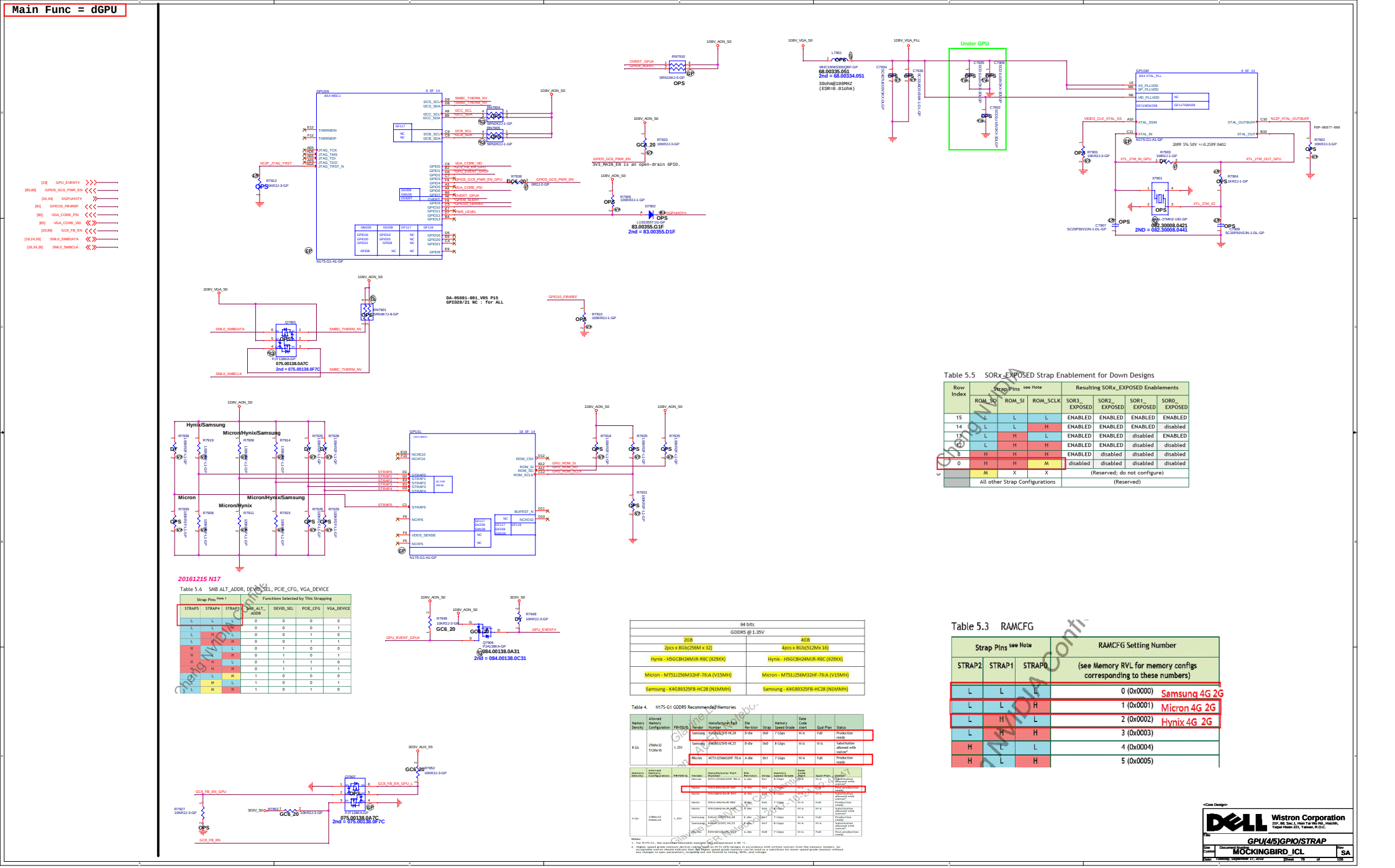

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

20161215 N17

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

64 bits	
GDDR5 @ 1.35V	
2GB	4GB
2pcs x 8Gb(256M x 32)	4pcs x 8Gb(512Mx 16)
Hynix - H5GC8H24MJR-R0C (029XX)	Hynix - H5GC8H24MJR-R0C (029XX)
Micron - MT51J256M32HF-70:A (V15MH)	Micron - MT51J256M32HF-70:A (V15MH)
Samsung - K4G80325FB-HC28 (N1MMH)	Samsung - K4G80325FB-HC28 (N1MMH)

Table 4. N175-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with notice[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000) Samsung 4G 2G
L	L	H	1 (0x0001) Micron 4G 2G
L	H	L	2 (0x0002) Hynix 4G 2G
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)

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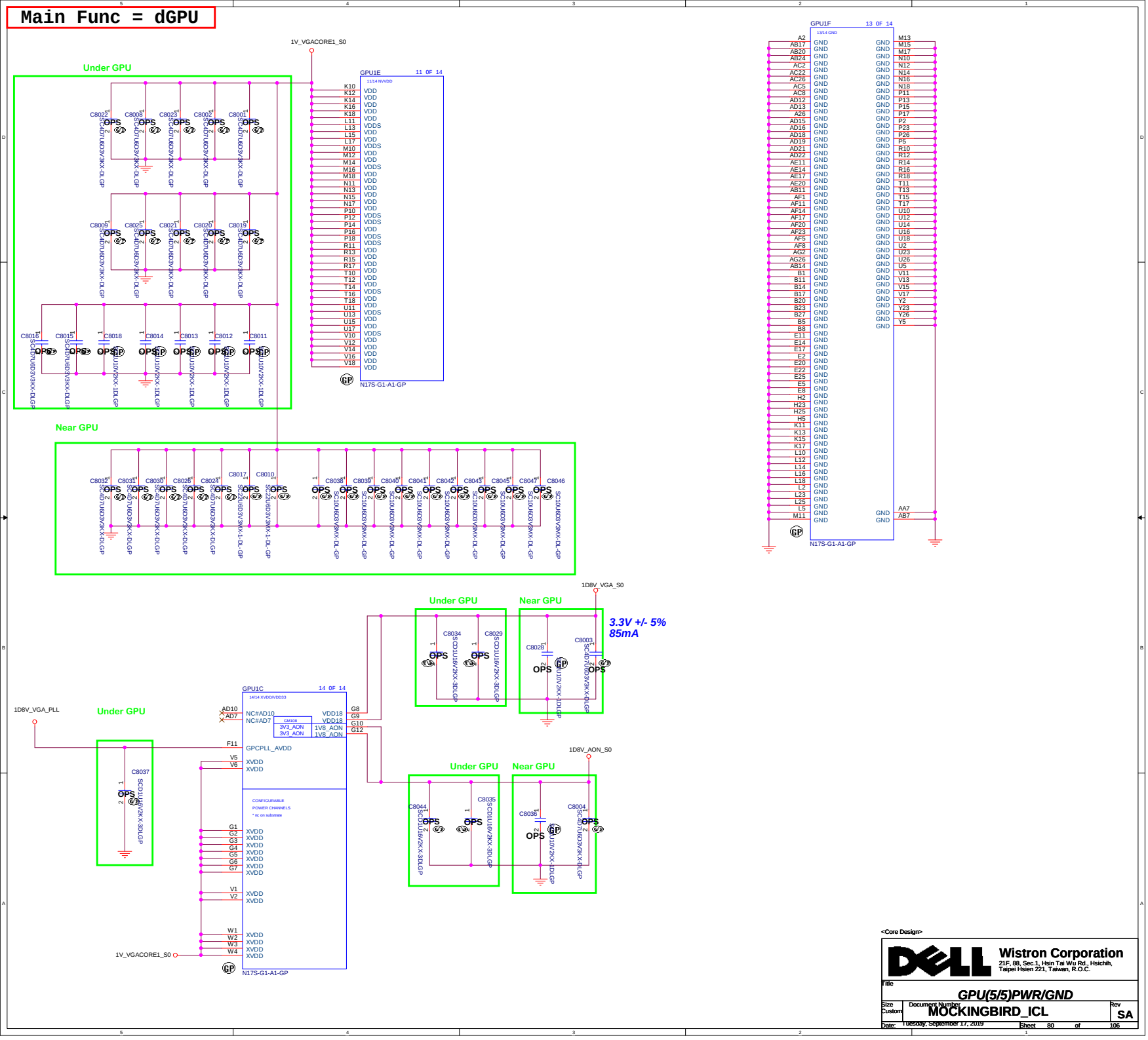
File: GPU(4/5)GPIO/STRAP

Size: C | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 07, 2010 | Sheet 29 of 106

Main Func = dGPU



<Core Design>

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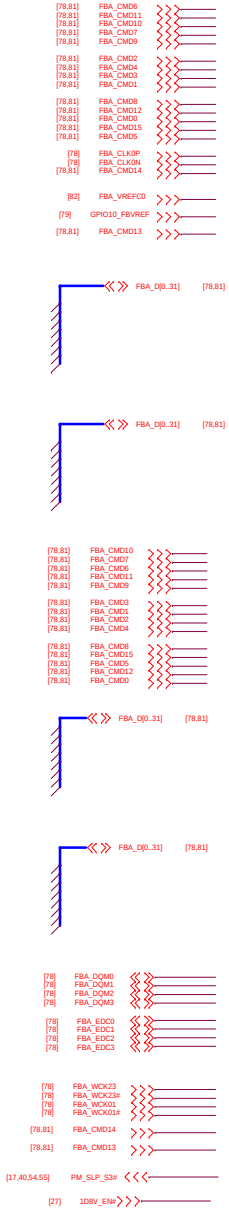
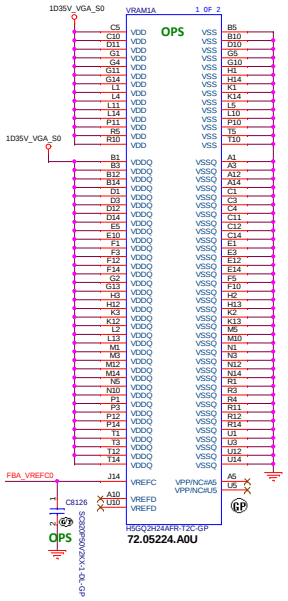
Title: GPU(5/5)PWR/GND

Size: Custom | Document Number: MOCKINGBIRD_ICL | Rev: SA

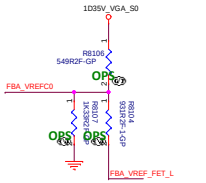
Date: Tuesday, September 17, 2019 | Sheet 80 of 106

SSID = VRAM

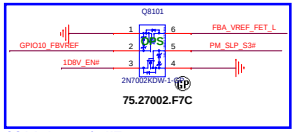




Frame Buffer Patition A-Lower Half



0614 Layout HT

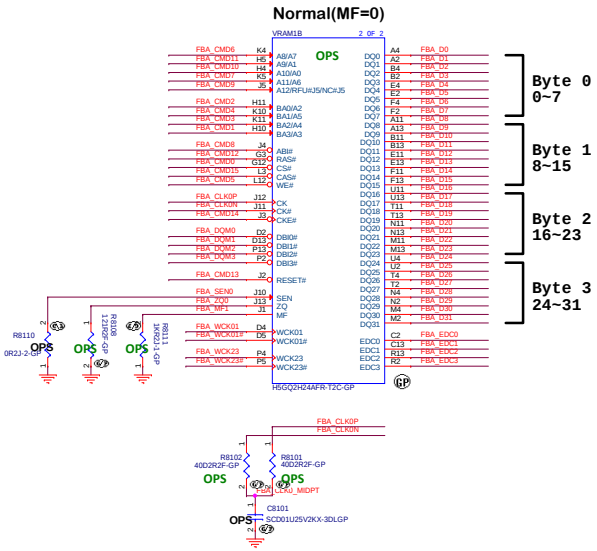


0614 Layout HT

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Normal(MF=0)



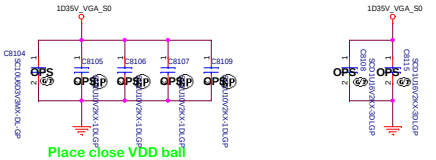
Byte 0 0~7

Byte 1 8~15

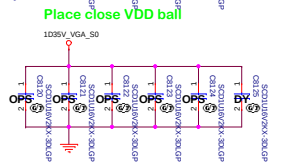
Byte 2 16~23

Byte 3 24~31

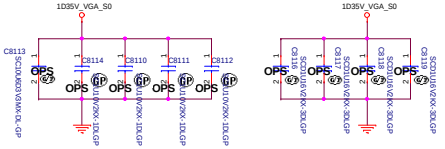
Place close VDD ball



Place close VDD ball



Place close VDDQ ball



<Core Design>

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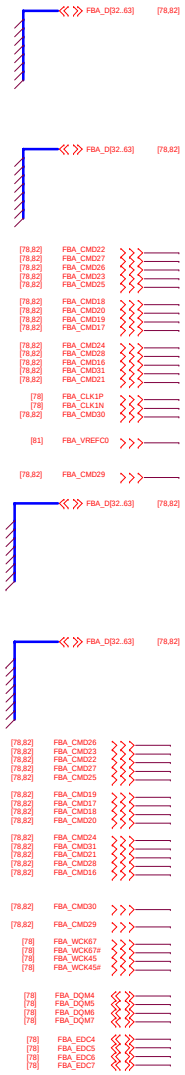
Title: GPU-VRAM1,2 (1/4)

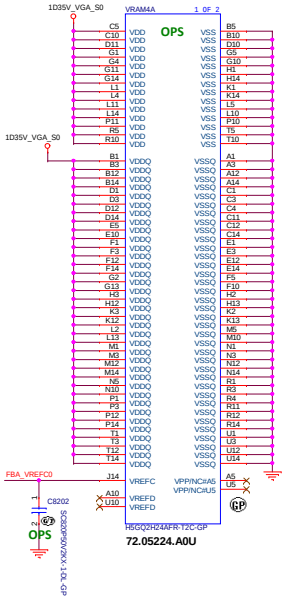
Size	Document Number	Rev
Custom	MOCKINGBIRD_ICL	SA

Date: Tuesday, September 17, 2019 Sheet 81 of 108

SSID = VRAM

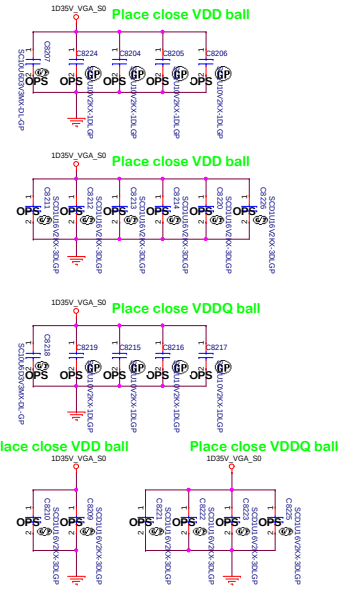


Frame Buffer Patition A-Upper Half

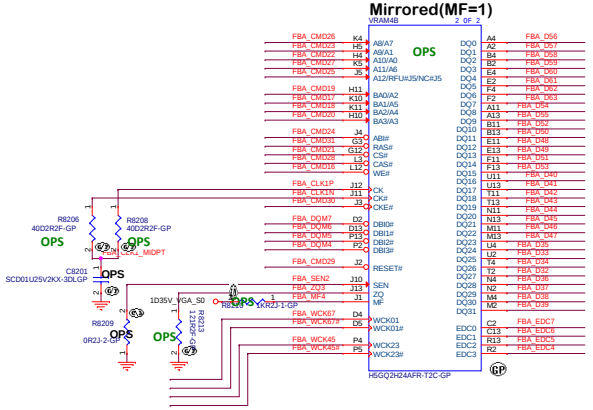


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Mirrored(MF=1)



Byte 7 56~63

Byte 6 48~55

Byte 5 40~47

Byte 4 32~39

<Core Design>

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Title: GPU-VRAM3.4 (2/4)

Size: Custom | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 82 of 105

OFFPAGE-Signal

PH on EE side

1. Check EE side
2. Modify DAT

PH on EE side

EE need check

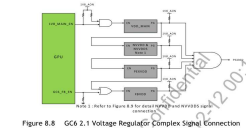
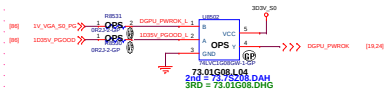
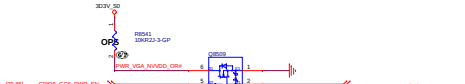
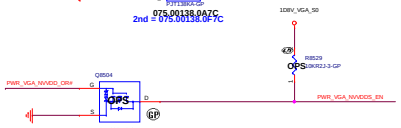


Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

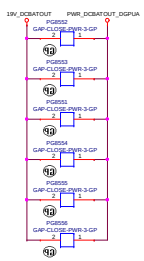


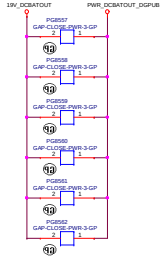
For VGA_CORE sequence
EE need check





OFFPAGE-GAP



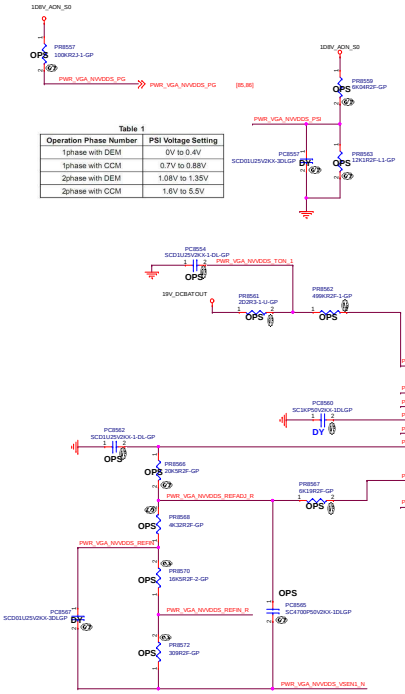


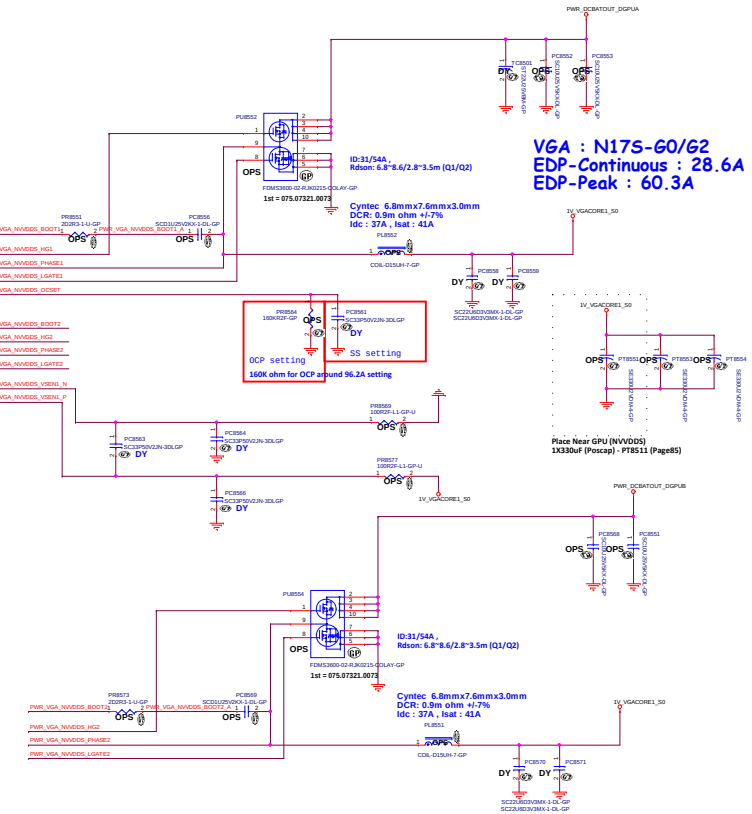
RT8816B For NVVDDS

VGA : N17S-G1
EDP-Continuous : 30A
EDP-Peak : 60.1A

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V





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Title	GPU (RT8816A_VGA)	
Size: A1	Document Number: MOCKINGBIRD_ICL	Rev: SA
Date: Tuesday, September 17, 2019	Sheet 85 of 105	

Main Func = dGPU

Main Func = dGPU

[DG-07158-001 Rev03]Power up sequence:
3.3V ==> MVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> FBVDD/Q (1.35V)

3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0

1D8V_AON_S0 to 1D8V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D35V_VGA_S0

1D8V_AON_S0

1D8V_VGA_S0

RT5797 for 1V_VGA_S0

For tuning VGA_CORE sequence.

1V_VGA_S0

1D35V_VGA_S0

SY8288RAC for 1D35V

OCP setting	
High	16A
Floor	12A
Low	6A

Design Current=3.2A

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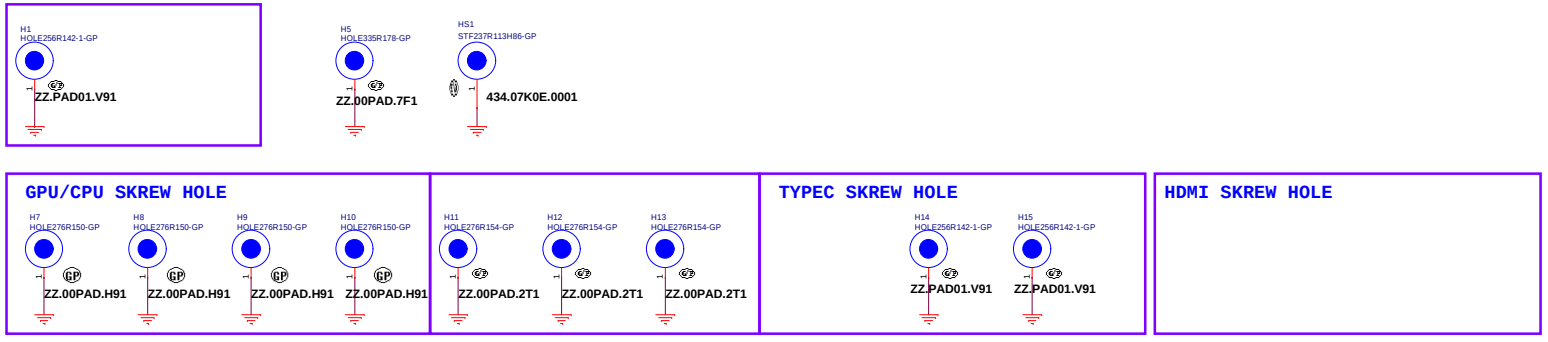
DISCRETE VGA POWER

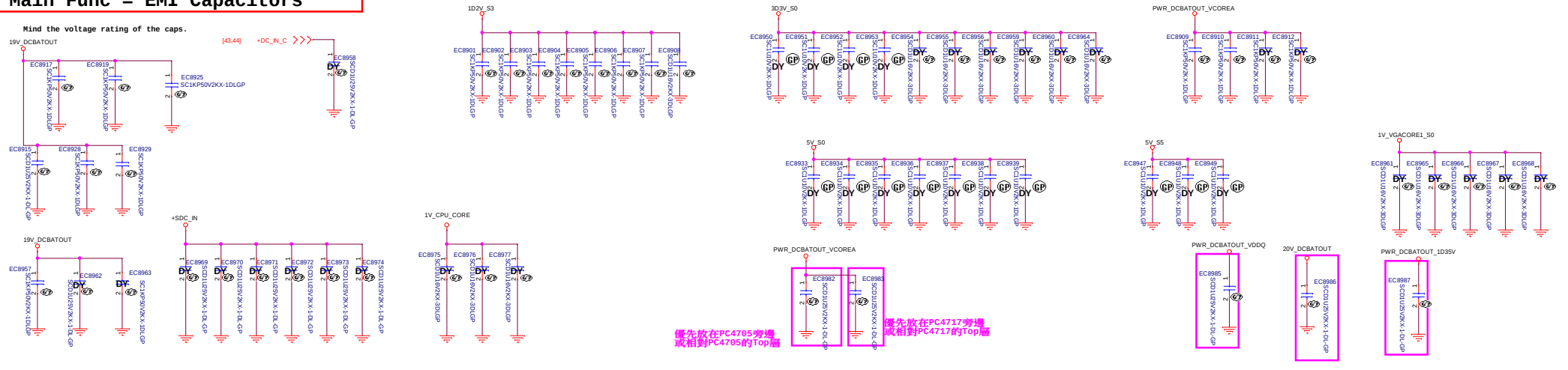
MOCKINGBIRD_ICL

SA

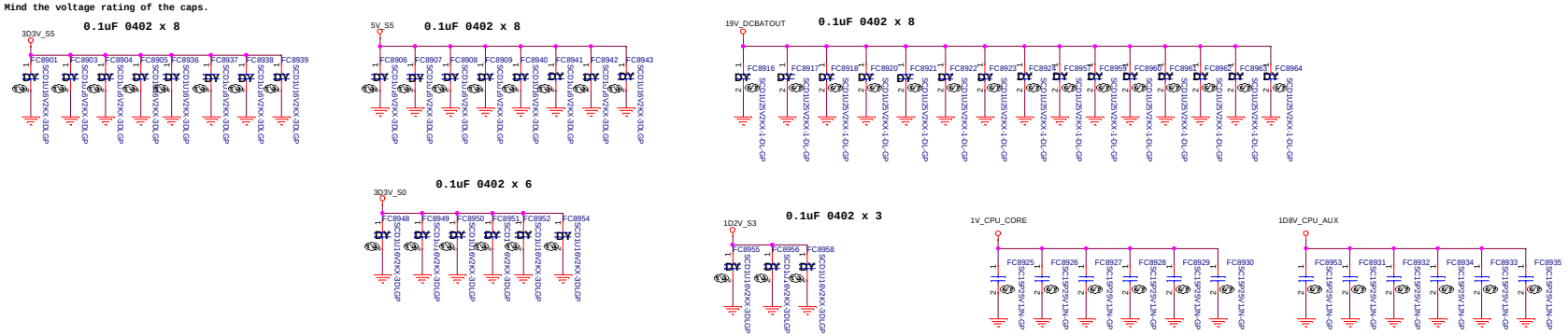
Main Func = UnusedParts



Main Func = EMI Capacitors



Main Func = RF Capacitors



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A2	MOCKINGBIRD_ICL	SA

Date: Tuesday, September 17, 2019 Sheet 89 of 106

Main Func = TPM

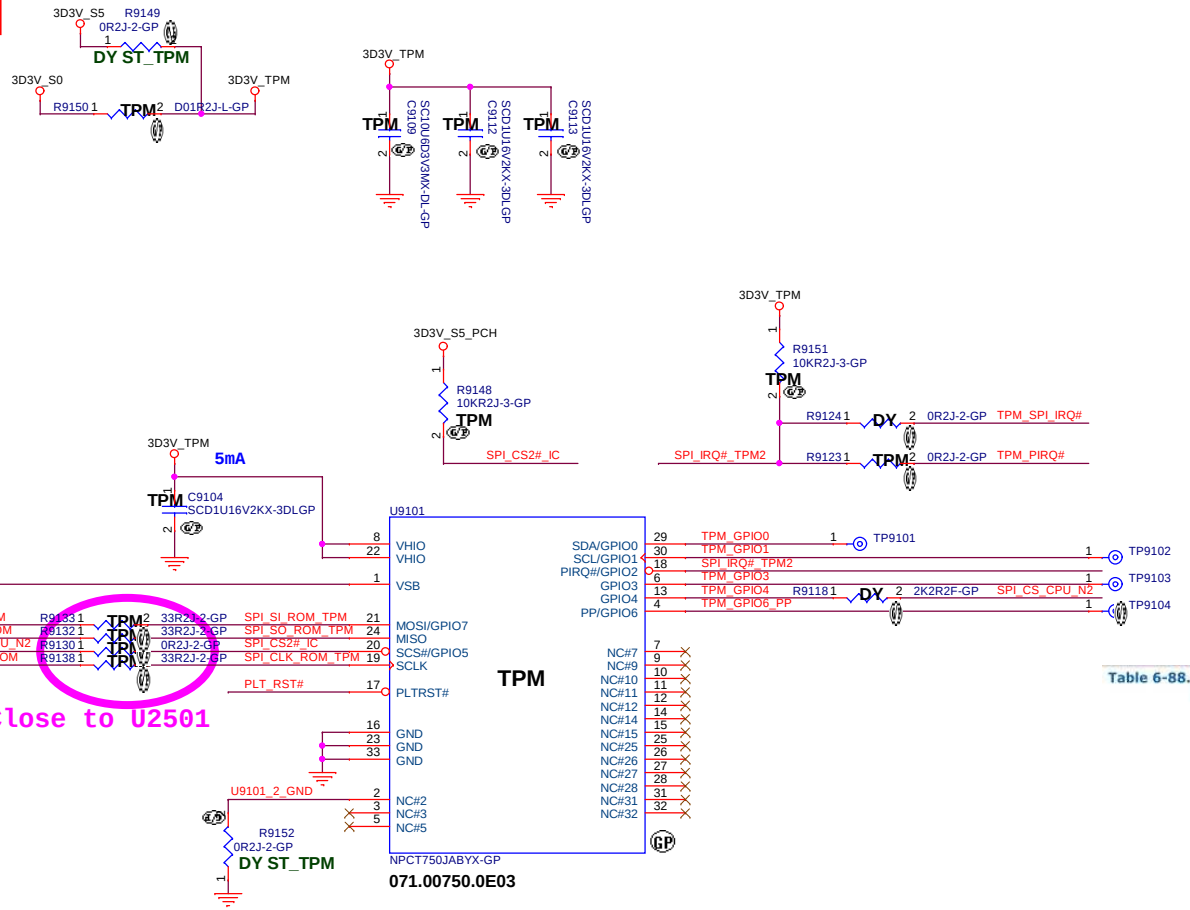
[17,61,63,66,76] PLT_RST#

[18,24,25] SPI_CLK_ROM
[18,24,25] SPI_SI_ROM
[18,24,25] SPI_SO_ROM

[18] TPM_SPI_IRQ#

[20] TPM_PIRQ#

[18] SPI_CS_CPU_N2



SPI0 2-Load(1 Flash and 1 Flash/1 TPM) EC G3 Flash Sharing with Wire-OR Topology

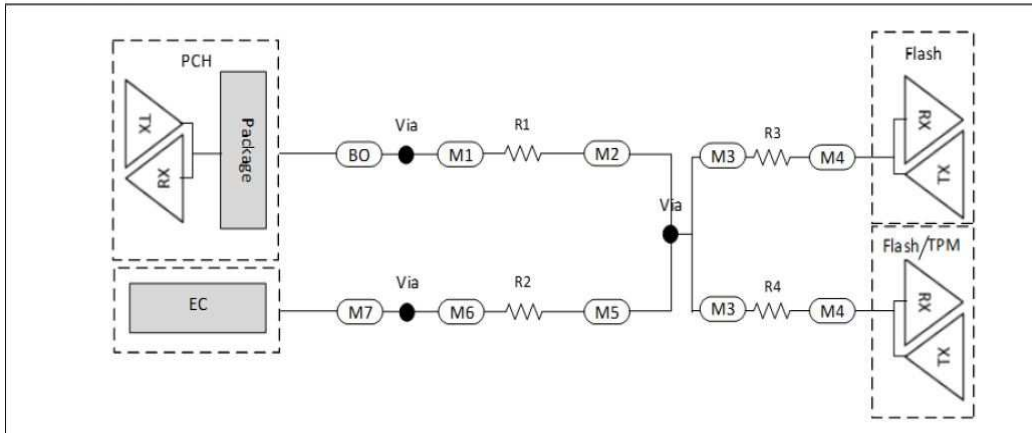


Table 6-88. SPI0 2-Load(1 Flash and 1 TPM) EC G3 Flash Sharing with Wire-OR Topology Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
B0/M7	MS/SL	VSS	1	12.7	152.4
M1/M6	MS/SL/DSL	VSS	1	76.2	
M2/M5	MS	VSS	0	25.4	
M3	MS	VSS	0	12.7	
M4	MS	VSS	0	25.4	

Notes:

1. EC and PCH branch requirement: Delta between M1+M2 and M5+M6 shall not exceed 50.8mm (2inch).
2. R1 resistor should be stuffed with 0 ohm placeholder for 3.3V and 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
3. R2 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If topology uses two flash then R2 for SPI0_IO2 and SPI0_IO3 shall be same as MISO and MOSI recommendation.
4. R2 resistor should be stuffed with 75 ohm for 3.3V and 50 ohm for 1.8V. To be placed on SPI0_IO2 and SPI0_IO3, if topology uses 1 flash and 1 TPM.If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.
5. R3 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If topology uses two flash then R3 for SPI0_IO2 and SPI0_IO3 shall be same as MISO and MOSI recommendation.
6. R3 resistor should be stuffed with 22 ohm for 3.3V and 50 ohm for 1.8V. To be placed on SPI0_IO2 and SPI0_IO3, if topology uses 1 flash and 1 TPM.If TPM use these signals, R3 value shall follow MISO and MOSI recommendation.
7. If topology uses two flash, R4 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3. If TPM use SPI0_IO2 and SPI0_IO3, R4 value shall follow MISO and MOSI recommendation
8. Minimum length for M1, M2, M4, M5 and M6: 12.7mm

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (TPM)

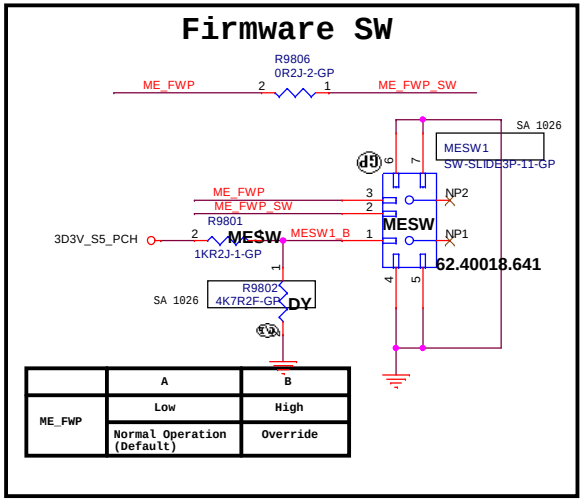
Size: A3 | Document Number: MOCKINGBIRD_ICL | Rev: SA

Date: Tuesday, September 17, 2019 | Sheet 91 of 106

Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

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Title: CRT_Switch

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Title: ***Debug (XDP debug)***

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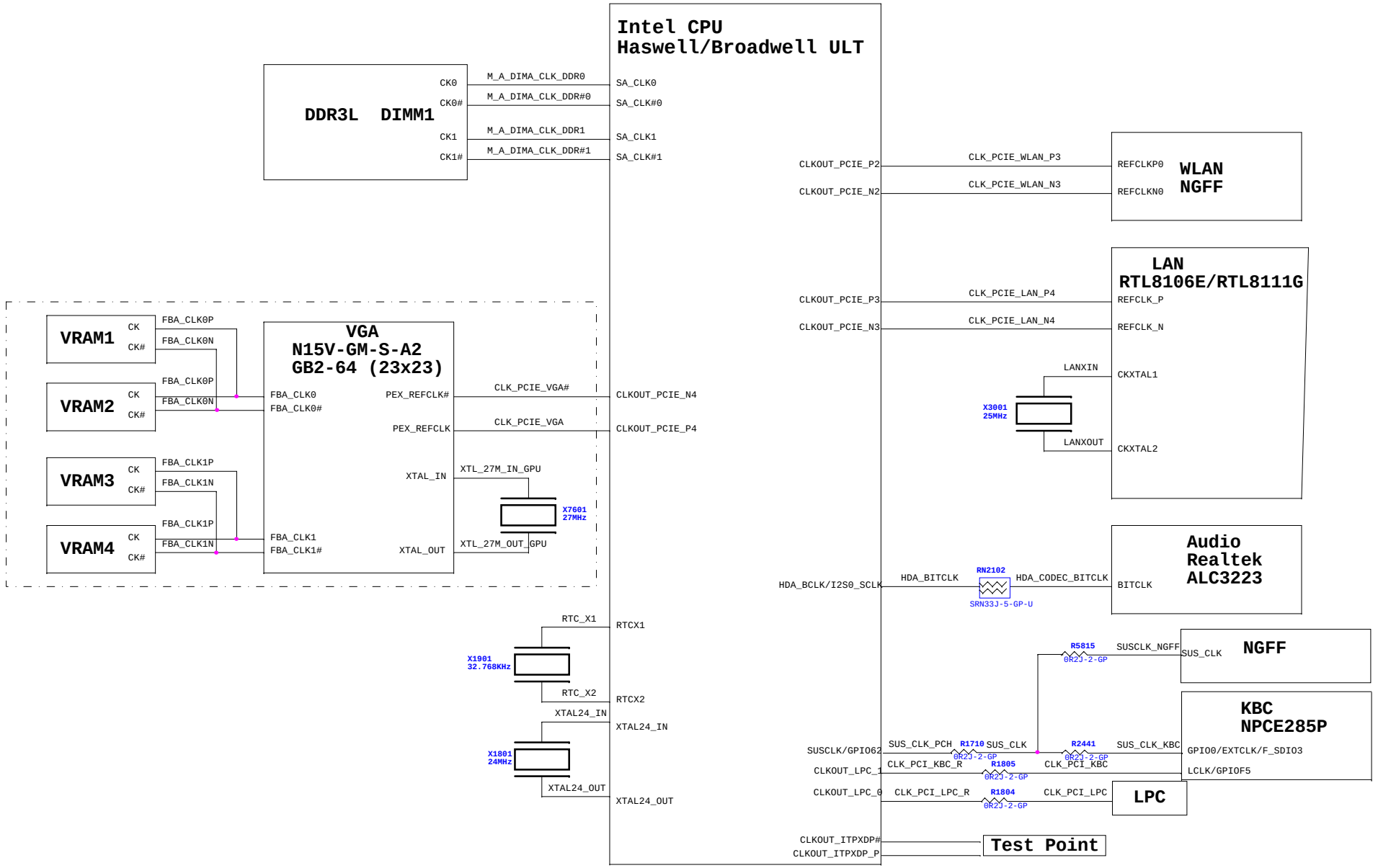
CLK Block Diagram



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Title: CLK Block Diagram

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Change notes -

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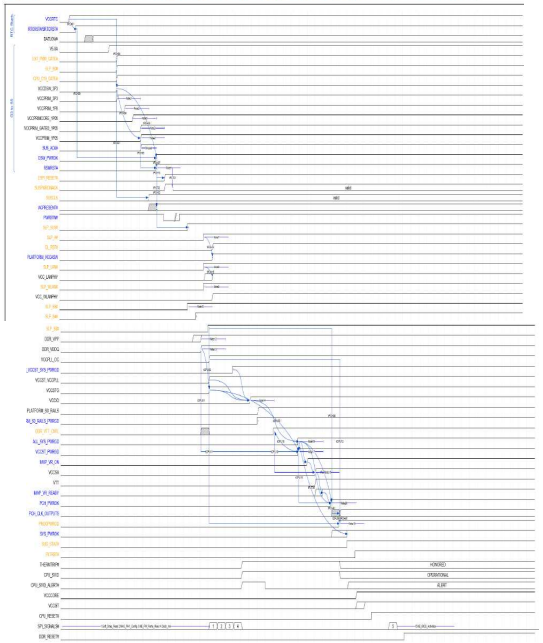
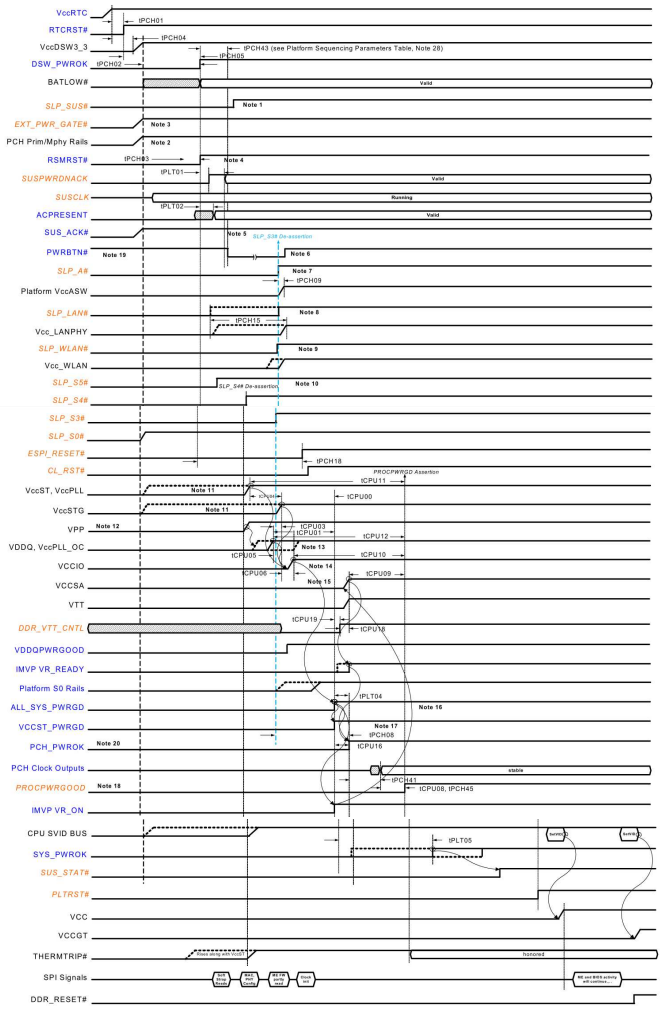
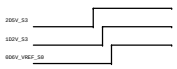
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



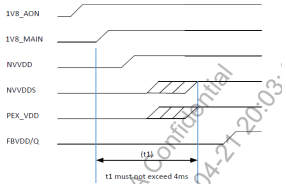
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



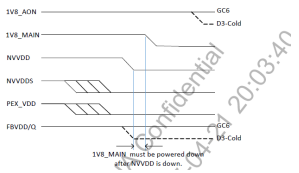
For DDR4 power sequence



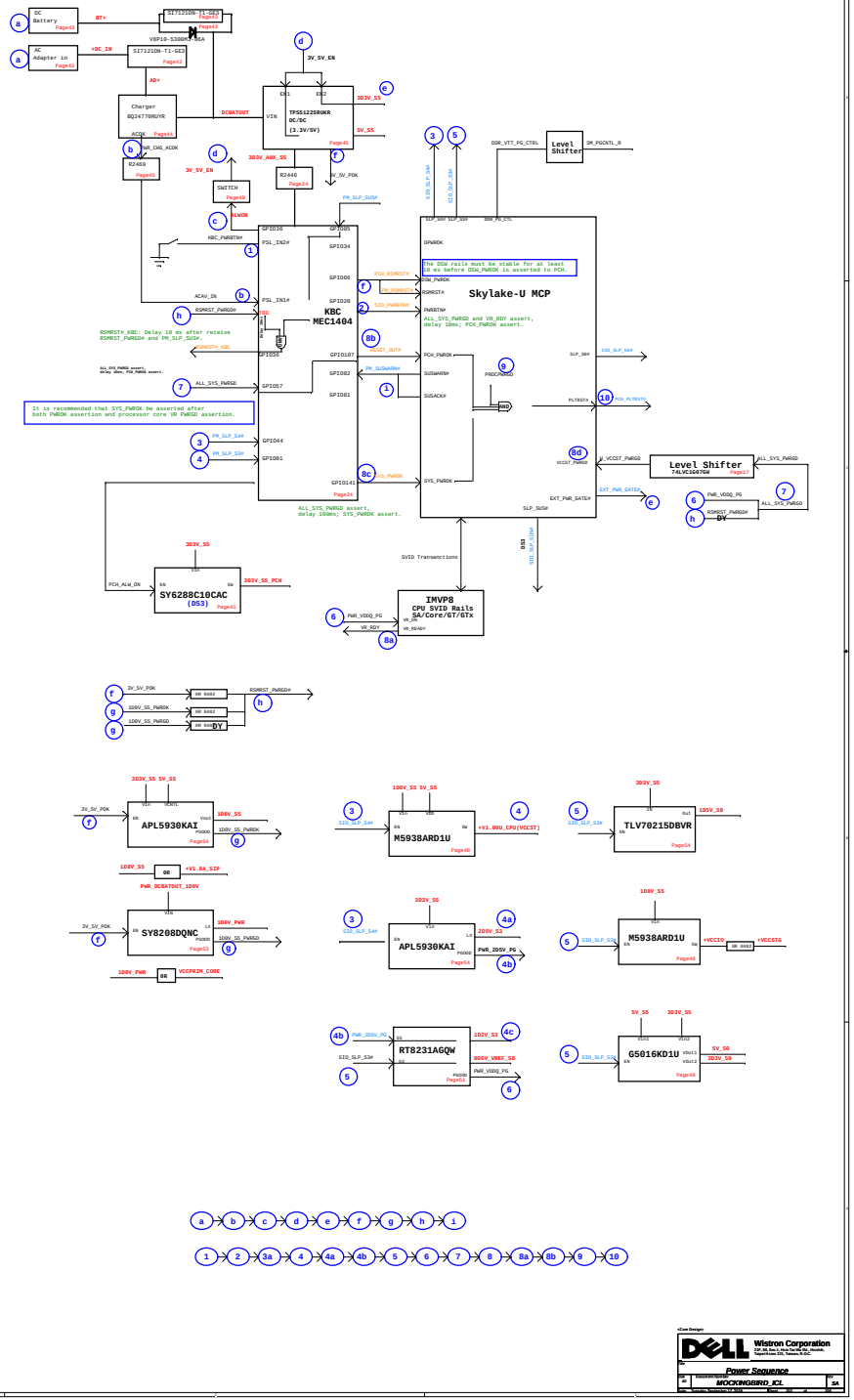
NV N17S GPU Power ON sequence

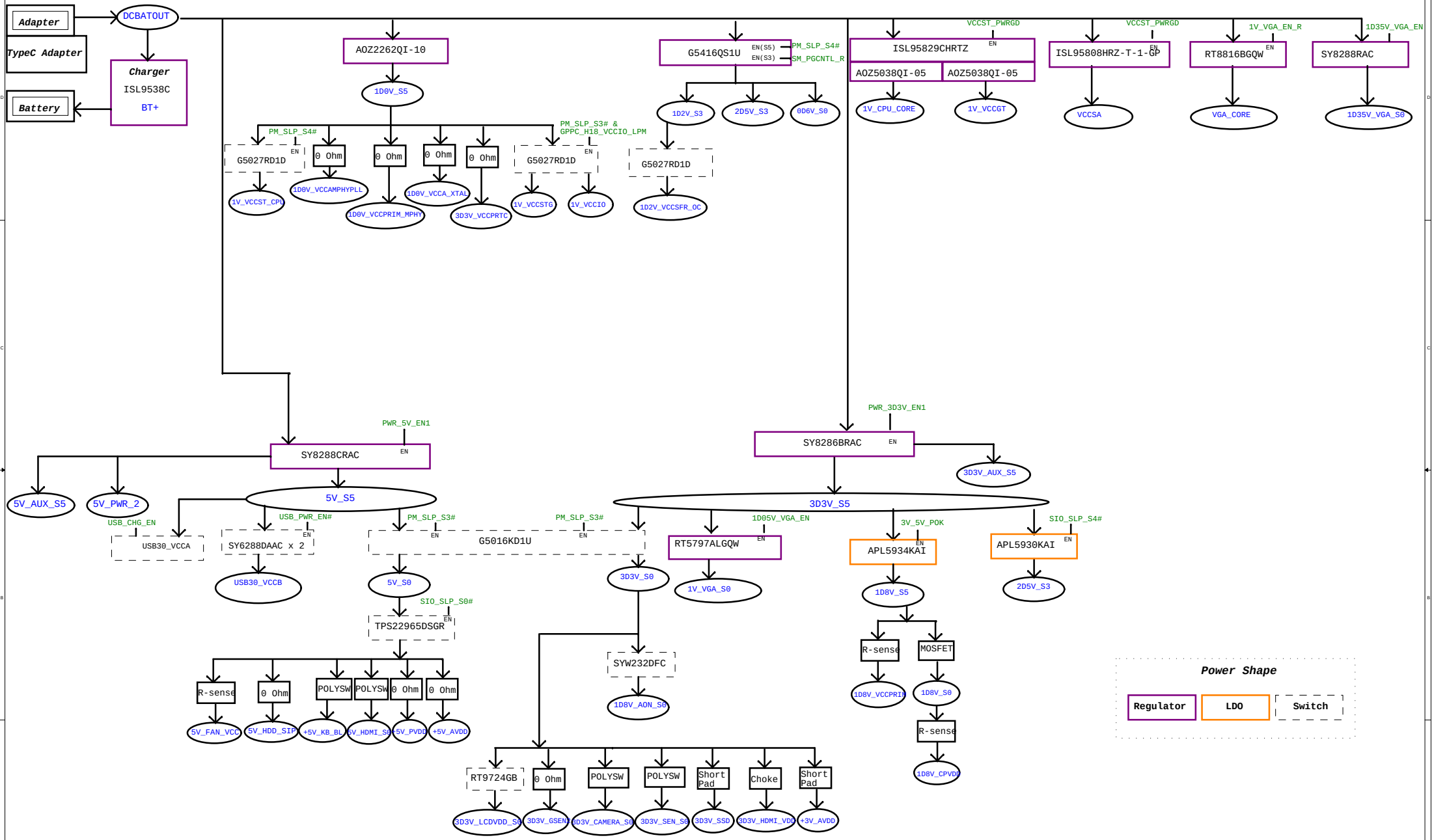


NV N17S GPU Power Down sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)





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Title: Power Block Diagram

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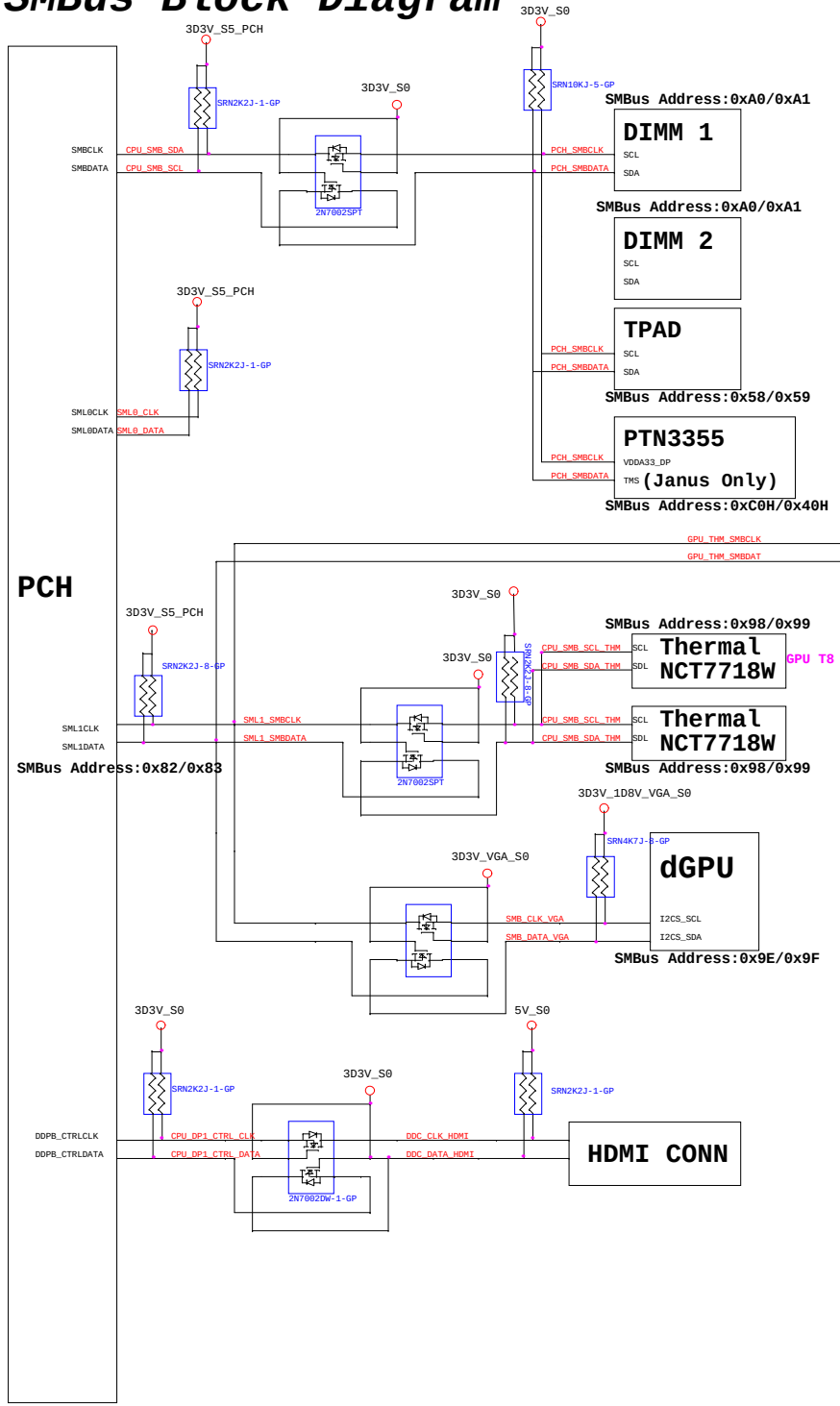
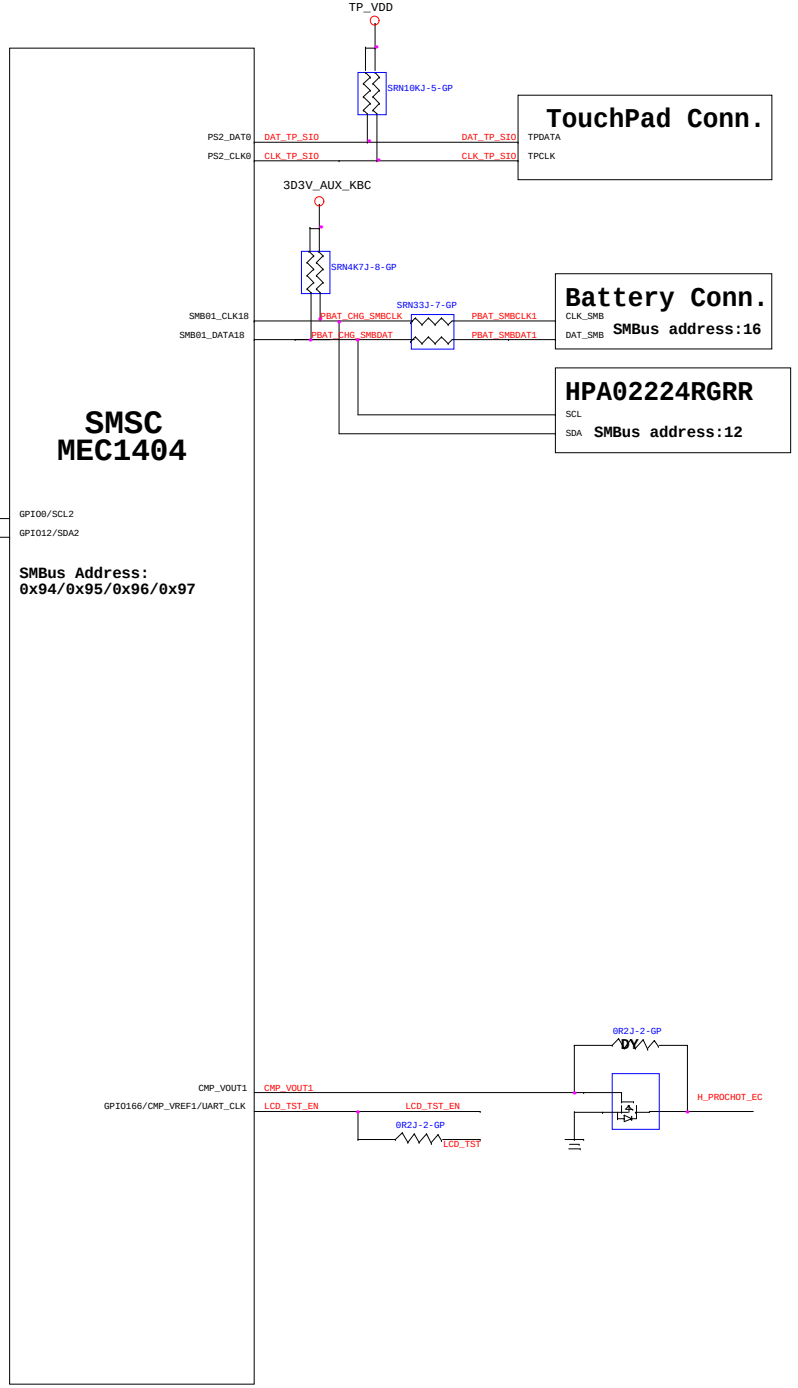
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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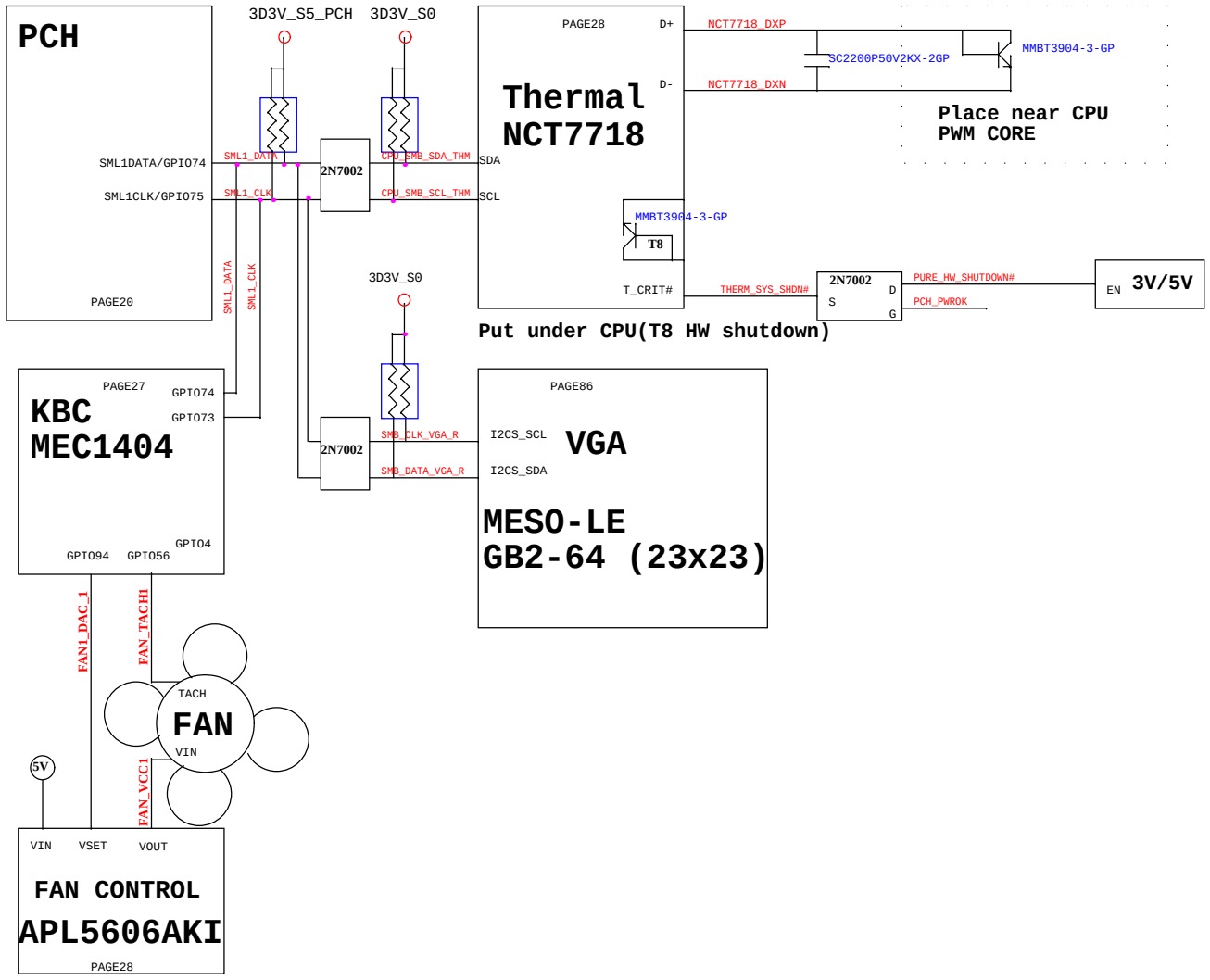
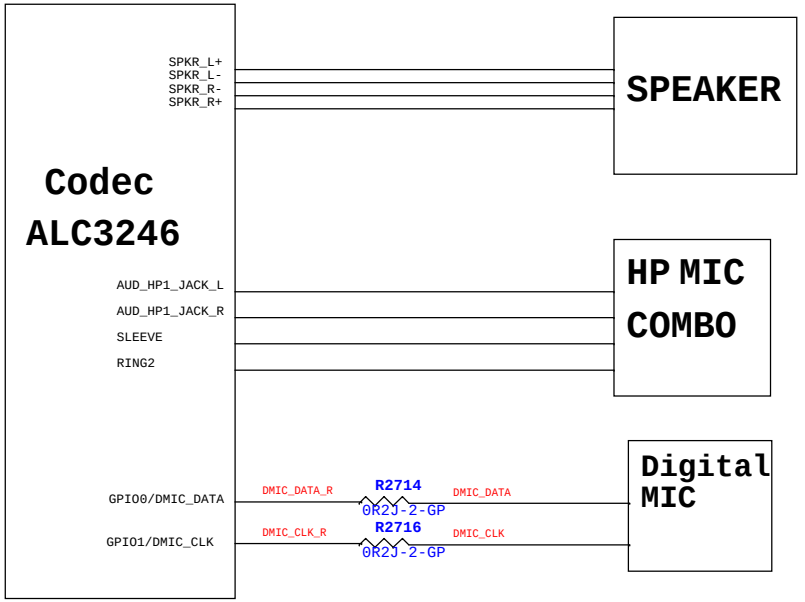
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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