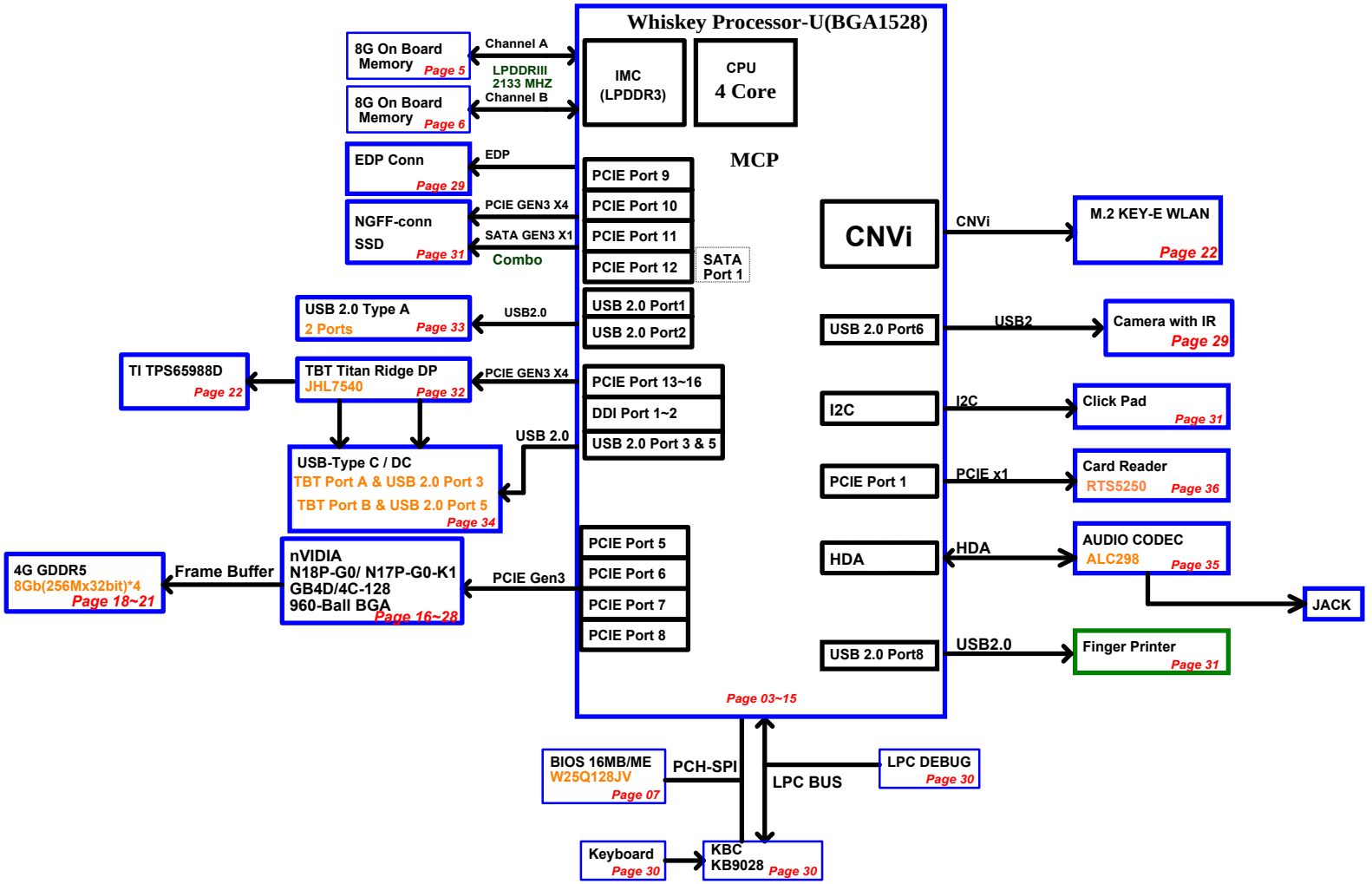
Whiskey Lake Processor-U Platform MS-14C1 VER : A



MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Friday, April 12, 2019 | Sheet 1 of 56

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_05VSUS	1.0V power rail	+1_8VSUSPWROK
+1_8VSUS	1.8V power rail	3V5VPWROK
+1_2VDIMM/+1_8VDIMM	1.2V power rail DDR (off in S4-S5)	S4_DIMM_ON_AND
+VDDQ_CPU	1.2V power rail CPU DRAM (off in S4-S5)	S4_DIMM_ON_AND
+VCCST/+VCCPLL	1.0V power rail CPU (off in S4-S5)	+1_2VDIMM_PWRGD
+VCCSTG	1.0V power rail CPU (off in S3-S5)	RUND
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND
+0_6VRUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND
+VCC_IO	1.0V rail for Processor & PCH (off in S3-S5)	RUND
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON

Net Naming Conventions

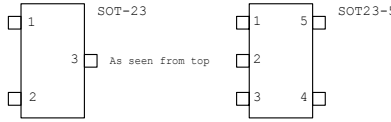
Suffix

\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+3VSUS	+*VSUS	+*VRUN	+VTT_CORE	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	ON	OFF	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF
S3(Suspend to RAM) WOL_EN	LOW	HIGH	HIGH	ON	ON	ON	OFF	OFF	OFF
S4(Suspend to Disk) WOL_EN	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF	OFF
S5 (Soft OFF) WOL_EN	LOW	LOW	LOW	ON	ON	ON	OFF	OFF	OFF

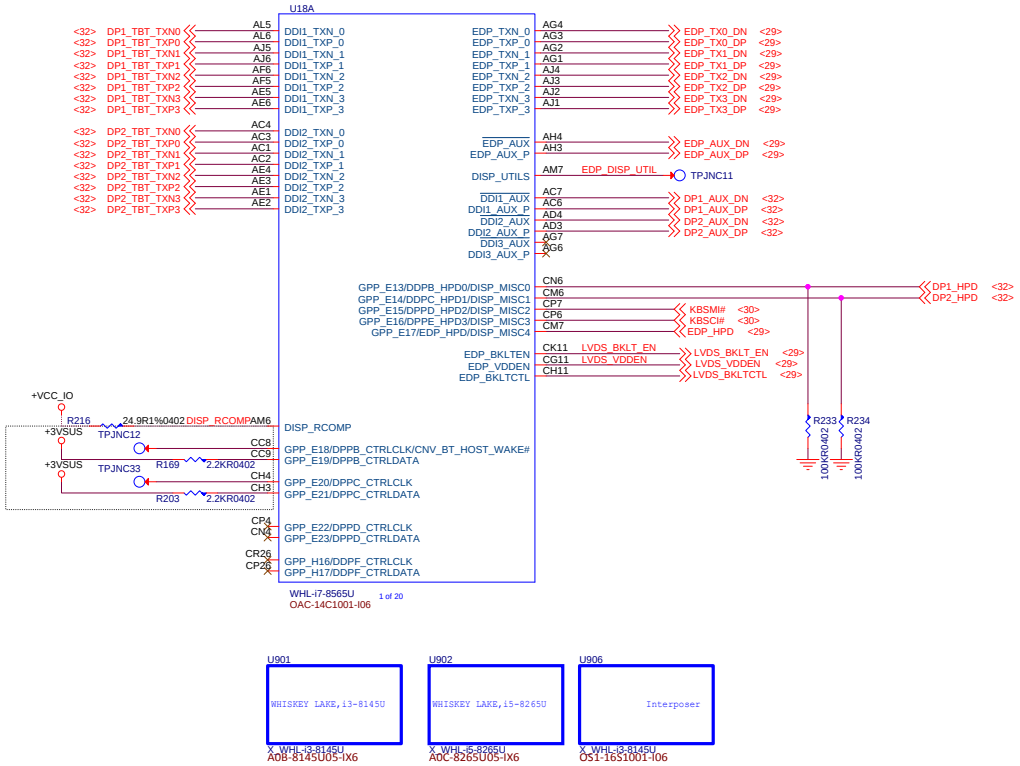
Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Friday, April 12, 2019 | Sheet 2 of 56

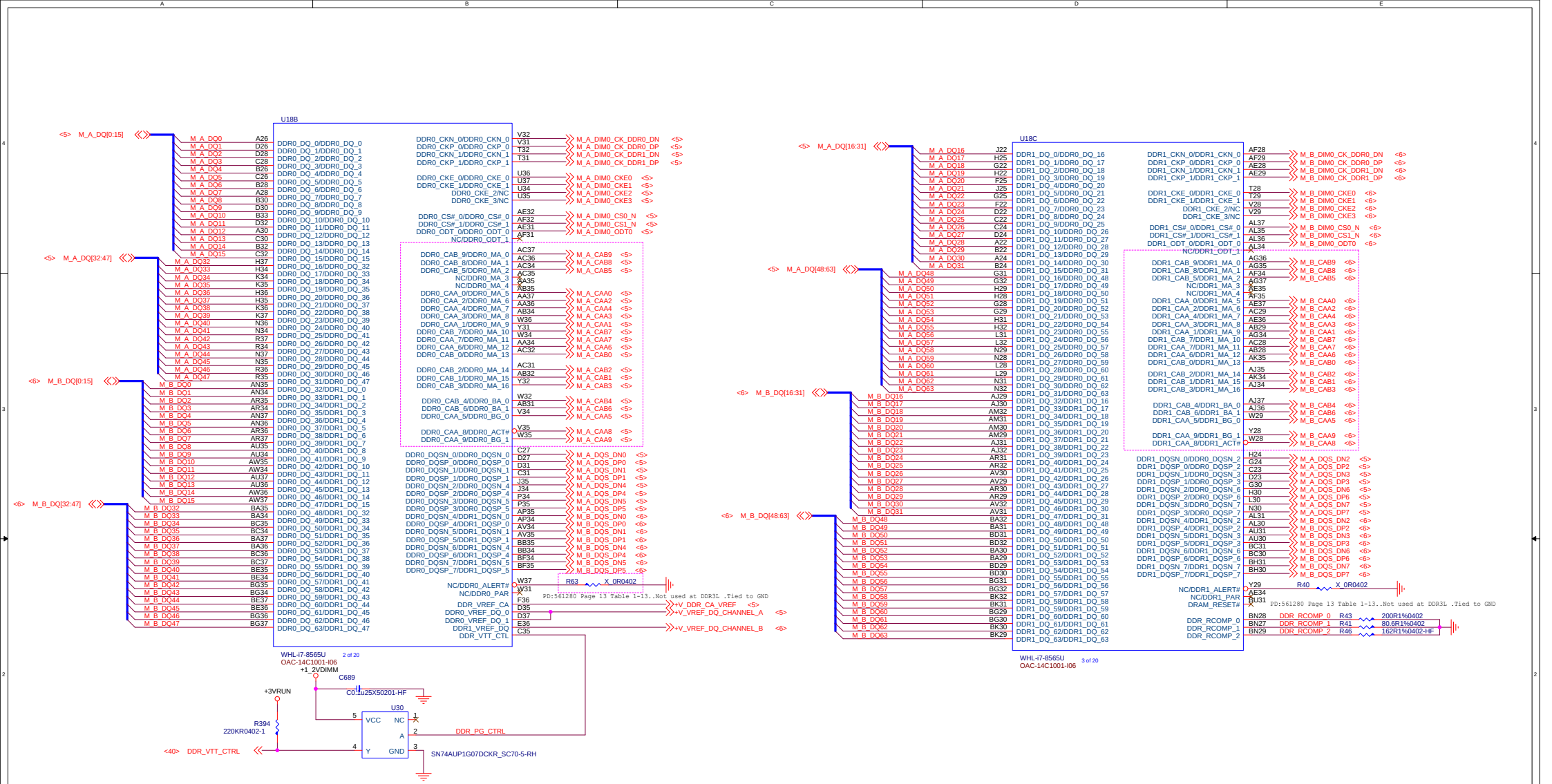


MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake(EDP & HDMI)

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 | Sheet 3 of 56



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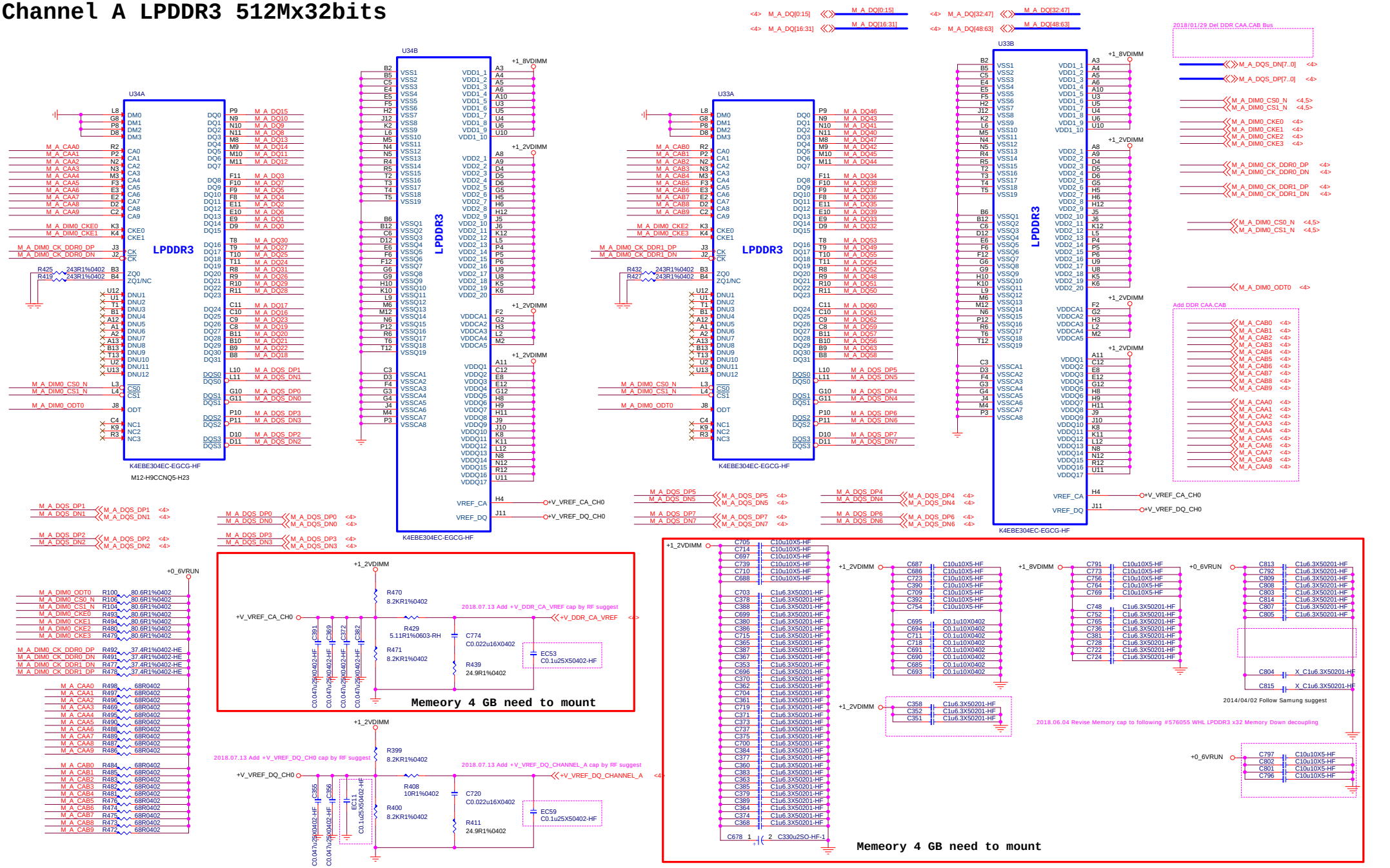
MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Whiskey lake U (LPDDR3 A)		
Size: Custom	Document Number: MS-14C1	Rev: 0A	
Date: Monday, April 22, 2019	Sheet 4 of 56		

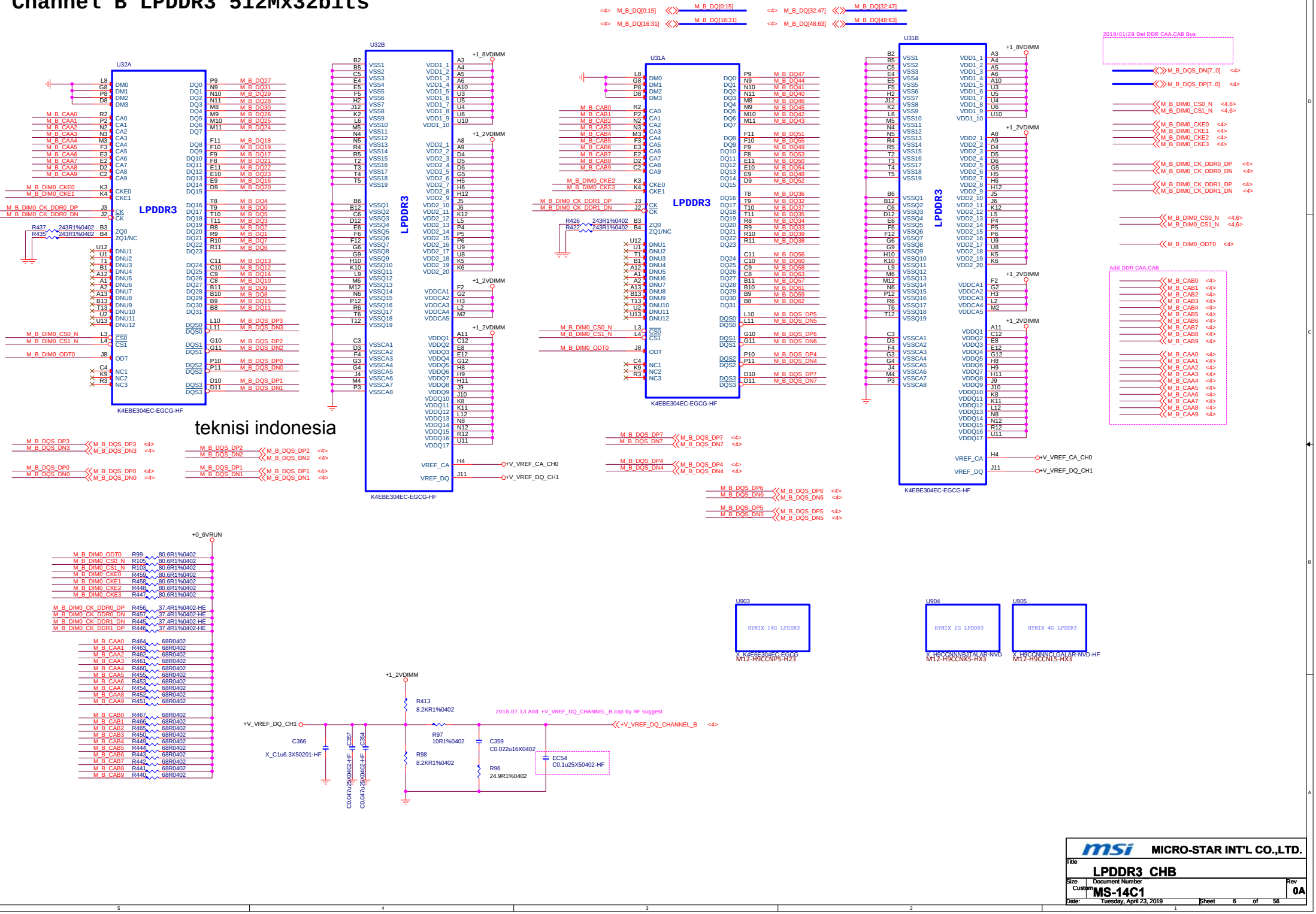
Channel A LPDDR3 512Mx32bits



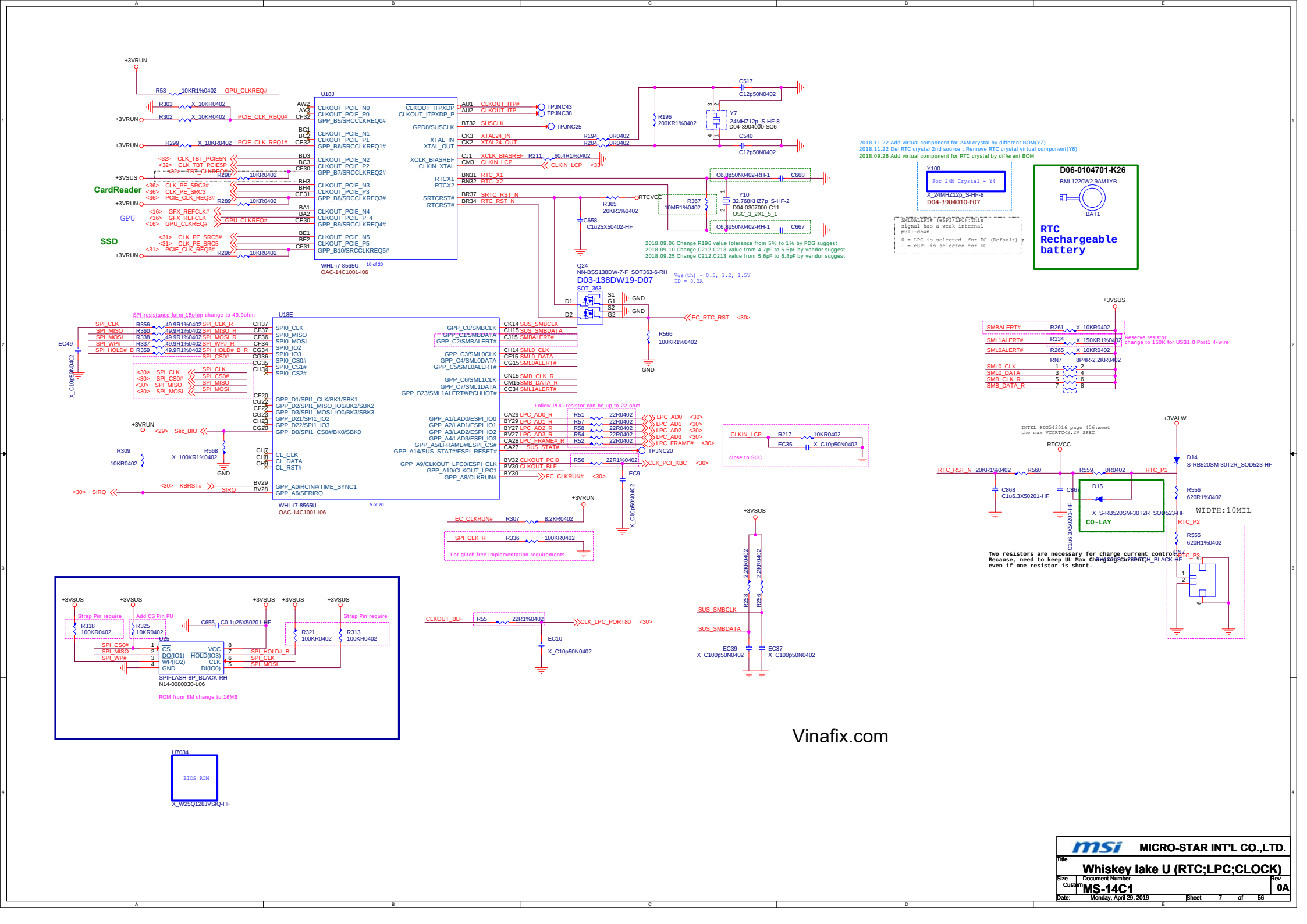
Title	LPDDR3_CHA
Size	Custom
Document Number	MS-14C1
Rev	0A
Date:	Tuesday, April 23, 2019
Sheet	5 of 56

MICRO-STAR INT'L CO.,LTD.

Channel B LPDDR3 512Mx32bits



MICRO-STAR INT'L CO.,LTD.		
Title: LPDDR3_CHB		
Size: Custom	Document Number: MS-14C1	Rev: 0A
Date: Tuesday, April 23, 2019	Sheet 6 of 56	


+3VRUN
R53 10KR1%0402 GPU_CLKREQ#
R303 X_10KR0402
R302 X_10KR0402 PCIE_CLK_REQ0#
R299 X_10KR0402 PCIE_CLK_REQ1#
+3VSUS
CardReader
GPU
SSD
R298 10KR0402
R289 10KR0402
R290 10KR0402
U18J
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4
CLKOUT_PCIE_P_4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL_IN
XTAL_OUT
XCLK_BIASREF
CLKIN_XTAL
RTCX1
RTCX2
SRTCRST#
RTCRST#
CLKOUT_ITP#
CLKOUT_ITP
TPJNC43
TPJNC38
SUSCLK
TPJNC25
XTAL24_IN
XTAL24_OUT
R194 0R0402
R204 0R0402
R196 200KR1%0402
XCLK_BIASREF
CLKIN_LCP
R211 60.4R1%0402
RTC_X1
RTC_X2
SRTC_RST_N
RTC_RST_N
R365 20KR1%0402
C658 C1u25X50402-HF
C517 C12p50N0402
Y7 24MHZ12p_S-HF-8 D04-3904000-SC6
C540 C12p50N0402
C6.8p50N0402-RH-1 C668
Y10 32.768KHZ7p_S-HF-2 D04-0307000-C11 OSC_3_2X1_5_1
R367 10MR1%0402
C6.8p50N0402-RH-1 C667
RTCVCC
WHL-i7-8565U
OAC-14C1001-I06
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2018.09.06 Change R196 value tolerance from 5% to 1% by PDG suggest
2018.09.10 Change C212.C213 value from 4.7pF to 5.6pF by vendor suggest
2018.09.25 Change C212.C213 value from 5.6pF to 6.8pF by vendor suggest
2018.11.22 Add virtual component for 24M crystal by different BOM(Y7)
2018.11.22 Del RTC crystal 2nd source ; Remove RTC crystal virtual component(Y6)
2018.09.26 Add virtual component for RTC crystal by different BOM
Y100
For 24M Crystal - Y4
X_24MHZ12p_S-HF-8
D04-3904010-F07
SML0ALERT# (eSPI/LPC):This signal has a weak internal pull-down.
0 = LPC is selected for EC (Default)
1 = eSPI is selected for EC
D06-0104701-K26
BML1220W2.9AM1YB
BAT1
RTC Rechargeable battery
Q24
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
Vgs(th) = 0.5, 1.2, 1.5V
ID = 0.2A
D1
D2
S1
G1
S2
G2
GND
EC_RTC_RST <30>
R566 100KR1%0402
SPI resistance form 15ohm change to 49.9ohm
U18E
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_WP#
SPI_HOLD#_B
SPI_CS0#
SPI_CS1#
SPI_CS2#
SPI_CLK_R
SPI_MISO_R
SPI_MOSI_R
SPI_WP#_R
SPI_HOLD#_B_R
EC49
X_C10p50N0402
GPP_D1/SPI1_CLK/BK1/SBK1
GPP_D2/SPI1_MISO_IO1/BK2/SBK2
GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS0#/BK0/SBK0
CL_CLK
CL_DATA
CL_RST#
SIRQ
KBRST#
Sec_BIO
R309 10KR0402
R568 X_100KR1%0402
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
SUS_SMBCLK
SUS_SMBDATA
SMBALERT#
SML0_CLK
SML0_DATA
SML1_CLK
SML1_DATA
SMB_CLK_R
SMB_DATA_R
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
LPC_AD0_R
LPC_AD1_R
LPC_AD2_R
LPC_AD3_R
LPC_FRAME#_R
SUS_STAT#
R51 22R0402
R57 22R0402
R58 22R0402
R54 22R0402
R52 22R0402
TPJNC20
Follow PDG resistor can be up to 22 ohm
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
CLKOUT_PCI0
CLKOUT_BLF
R56 22R1%0402
CLK_PCI_KBC <30>
EC_CLKRUN# <30>
EC9
GPP_A0/RCIN#/TIME_SYNC1
GPP_A6/SERIRQ
WHL-i7-8565U
OAC-14C1001-I06
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EC_CLKRUN# R307 8.2KR0402
SPI_CLK_R R336 100KR0402
For glitch free implementation requirements
CLKIN_LCP R217 10KR0402
EC35 X_C10p50N0402
close to SOC
+3VALW
INTEL PDG543016 page 456:meet the max VCCRTC<3.2V SPEC
RTCVCC
RTC_RST_N 20KR1%0402
R560
R559 0R0402
RTC_P1
C868 C1u6.3X50201-HF
C867
D15
X_S-RB520SM-30T2R_SOD523-HF
CO-LAY
D14 S-RB520SM-30T2R_SOD523-HF
R556 620R1%0402
WIDTH:10MIL
RTC_P2
R555 620R1%0402
RTC_P3
CN7 CONN_2_BLACK-HF
Two resistors are necessary for charge current control
Because, need to keep UL Max Charging Current,
even if one resistor is short.
SMBALERT# R261 X_10KR0402
SML1ALERT# R334 X_150KR1%0402
SML0ALERT# R265 X_10KR0402
Reserve resistor change to 150K for USB1.0 Port1 4-wire
RN7 8P4R-2.2KR0402
SML0_CLK
SML0_DATA
SMB_CLK_R
SMB_DATA_R
+3VSUS
2.2KR0402
R258
R256
SUS_SMBCLK
SUS_SMBDATA
EC39 X_C100p50N0402
EC37 X_C100p50N0402
CLKOUT_BLF R55 22R1%0402
CLK_LPC_PORT80 <30>
EC10 X_C10p50N0402
+3VSUS
Strap Pin require
Add CS Pin PU
R318 100KR0402
R325 10KR0402
C655 C0.1u25X50201-HF
R321 100KR0402
R313 100KR0402
U25
SPI_CS0#
SPI_MISO
SPI_WP#
SPI_HOLD#_B
SPI_CLK
SPI_MOSI
SPIFLASH-8P_BLACK-RH
N14-0080030-L06
ROM from 8M change to 16MB
U7034
BIOS ROM
X_W25Q128JVSIQ-HF
Vinafix.com
MICRO-STAR INT'L CO.,LTD.
Title
Whiskey lake U (RTC;LPC;CLOCK)
Size
Custom
Document Number
MS-14C1
Rev
0A
Date: Monday, April 29, 2019
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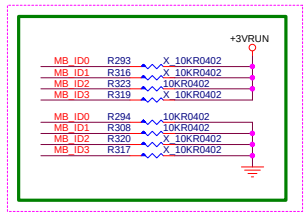

2018.07.05 Revise MB_ID configuration and MB_ID table list

MB_ID	Configuration	Remark
[0]	0 : Samsung LPDDR3 * 1 : Hynix LPDDR3	
[2:1]	00 : 4GB(2 chip) 01 : 8GB(4 chip) 10 : 16GB(4 chip) * 11 : NA	
[3]	Reserve	

2018.06.01 Revise memory configuration table

2018.06.23 Change MB_ID1 of signal from GPP_B18 to GPP_B19 because GPP_B18 is a strap pin

U18F

MB_ID2 CC27 GPP_B15/GSPI0_CS0#
PIRQA# CC32 GPP_A7/PIRQA#/GSPI0_CS1#
MB_ID3 CE28 GPP_B16/GSPI0_CLK
MB_ID0 CE27 GPP_B17/GSPI0_MISO
CE29 GPP_B18/GSPI0_MOSI
MB_ID1 CA31 GPP_B19/GSPI1_CS0#
CA32 GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
CC29 GPP_B20/GSPI1_CLK
CC30 GPP_B21/GSPI1_MISO
CA30 GPP_B22/GSPI1_MOSI

<33> CNVI_BRI_RSP CK20 GPP_F5/CNV_BRI_RSP
<33> CNVI_RGI_DT_R R271 75R0402 CNVI_RGI_DT CG19 GPP_F6/CNV_RGI_DT
<33> CNVI_BRI_DT_R R283 75R0402 CNVI_BRI_DT CJ20 GPP_F4/CNV_BRI_DT
<33> CNVI_RGI_RSP CH19 GPP_F7/CNV_RGI_RSP

CNVi 1.8v level
DT resistance close to SOC
RSP resistance close to module

CR12 GPP_C20/UART2_RXD
CP12 GPP_C21/UART2_TXD
CN12 GPP_C22/UART2_RTS#
CM12 GPP_C23/UART2_CTS#

I2C_DATA_TP CM11 GPP_C16/I2C0_SDA
I2C_CLK_TP CN11 GPP_C17/I2C0_SCL

TP_INT_N_SUS CK12 GPP_C18/I2C1_SDA
<27> GPIO2_GPU_EVENT_PCH CJ12 GPP_C19/I2C1_SCL

<27> GC6_FB_EN CF27 GPP_H4/I2C2_SDA
CF29 GPP_H5/I2C2_SCL

<28,30> DGPU_PWRGD CH27 GPP_H6/I2C3_SDA
CH28 GPP_H7/I2C3_SCL

<27> DGPU_HOLD_RST# CJ30 GPP_H8/I2C4_SDA
<28> DGPU_PWR_EN 3.3V CJ31 GPP_H9/I2C4_SCL

Active HI
GND R45 100KR1%0402

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# CN22
GPP_D10/ISH_SPI_CLK/GSPI2_CLK CR22
GPP_D11/ISH_SPI_MISO/GSPI2_MISO CM22 TBT_WAKE# PDI2C_PCH_IRQ <32>
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI CP22 GPP_D12 TBT_WAKE# <32>

GPP_D5/ISH_I2C0_SDA CK22
GPP_D6/ISH_I2C0_SCL CH20

GPP_D7/ISH_I2C1_SDA CH22
GPP_D8/ISH_I2C1_SCL CJ22

GPP_H10/I2C5_SDA/ISH_I2C2_SDA CJ27 PDI2C_SDA_PCH <32>
GPP_H11/I2C5_SCL/ISH_I2C2_SCL CJ29 PDI2C_SCL_PCH <32>

GPP_D13/ISH_UART0_RXD CM24
GPP_D14/ISH_UART0_TXD CN23
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1# CM23 RTD3_CIO_PWR_EN RTD3_CIO_PWR_EN <32>
GPP_D16/ISH_UART0_CTS#/SML0BALERT# CR24

GPP_C12/UART1_RXD/ISH_UART1_RXD CG12
GPP_C13/UART1_TXD/ISH_UART1_TXD CH12
GPP_C14/UART1_RTS#/ISH_UART1_RTS# CF12 R586 0R0402 0R0402 CG14 R181 PWREN_WKCTRL_N <32>
GPP_C15/UART1_CTS#/ISH_UART1_CTS# TBT_PERST_N <8>

GPP_A18/ISH_GP0 BW35
GPP_A19/ISH_GP1 BW34
GPP_A20/ISH_GP2 CA37
GPP_A21/ISH_GP3 CA36
GPP_A22/ISH_GP4 CA35
GPP_A23/ISH_GP5 CA34
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF# BW37

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WHL-i7-8565U
OAC-14C1001-I06

+3VSUS
Strap Pin require
R275 100KR0402

+1_8VSUS
CNVI_BRI_RSP R277 X_20KR0402-2
CNVI_RGI_RSP R269 X_20KR0402-2
DT resistance close to module
RSP resistance close to SOC

Q25
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
SUS
TP_INT_N_SUS D1 D2 S1 G1 S2 G2
RUN
TP_INT_N TP_INT_N <31>
Vgs(th) = 0.5V,1.2V,1.5V
C1676 C0.1u25X50402-HF GND
+3VRUN

Q19
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
SUS
I2C_CLK_TP D1 D2 S1 G1 S2 G2
RUN
I2C_CLK_TP_Q I2C_CLK_TP_Q <31>
I2C_DATA_TP_Q I2C_DATA_TP_Q <31>
Vgs(th) = 0.5V,1.2V,1.5V
C844 C0.1u25X50402-HF GND
+3VRUN

+3VRUN
I2C_CLK_TP_Q R527 2.2KR0402
I2C_DATA_TP_Q R528 2.2KR0402
TP_INT_N R522 2.2KR0402

+3VSUS
I2C_CLK_TP R579 2.2KR0402
I2C_DATA_TP R580 2.2KR0402
TP_INT_N_SUS R583 2.2KR0402

DSWROK can be tied to RSMRST# for platforms that dose not support the Deep Sx state.
DSW_PWROK R364 0R0402 RSMRST#

2018.06.14 PCIE_WAKE# signal follow CRB Pull up 8.2k ohm
2018.06.14 Del PM_SLP_S0# and EXT_PWR_GATE# pull up resistor
Because function pin is output pin and isn`t be used
For glitch free implementation requirements
PCIE_WAKE# R339 8.2KR0402
AC_PRESENT R363 10KR0402
PM_PWRBTN# R385 X_10KR0402
2018.06.13 Del SUSPWRDNACK pull up resistor for PDG suggest
PIRQA# R324 10KR0402
RSMRST# R342 10KR0402
PCH_PWROK R355 10KR0402
AC_PRESENT R340 X_100KR0402
For glitch free implementation requirements
PM_SLP_S3# R379 100KR0402
PM_SLP_S4# R322 100KR0402

<27> PLT_RST#
PLT_RST#
+3VRUN R251 10KR0402
SYS_RESET# JNCCN10 BJ35
RSMRST# BR36
<30> RSMRST#
PROCPWRGD AR2
TPJNC44 VCCST_PWRGD BJ2
<30> SYS_PWROK R245 0R0402 CR10
<30> PCH_PWROK R335 0R0402 BP31
DSW_PWROK BP30
TPJNC54 SUS_PWR_ACK BV34
GPP_A13/SUSWARN#/SUSPWRDACK BV32
GPP_A15/SUSACK#
<32> PCIE_WAKE# PCIE_WAKE# BU30
R314 61.9KR1%0402-RH BU32
WAKE# BU31
GPD2/LAN_WAKE#
GPD11/LANPHYPC
For glitch free implementation requirements

U18K

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
DSW_PWROK

GPP_B12/SLP_S0# BJ37 PM_SLP_S0# TPJNC53
GPD4/SLP_S3# BU36 PM_SLP_S3# PM_SLP_S3# <30,32>
GPD5/SLP_S4# BU27 PM_SLP_S4# PM_SLP_S4# <30,40>
GPD10/SLP_S5# BT29 PM_SLP_S5# TPJNC22
SLP_SUS# BU29
SLP_LAN# BT31
GPD9/SPL_WLAN# BT30
GPD6/SLP_A# BU37
GPD3/PWRBTN# BU28 PM_PWRBTN# PM_PWRBTN# <30>
GPD1/ACPRESENT BU35 AC_PRESENT AC_PRESENT <30>
GPD0/BATLOW# BV36
INTRUDER# BR35 SM_INTRUDER_N 1MR0402 R380 RTCVCC
GPP_B11/EXT_PWR_GATE# CC37 EXT_PWR_GATE# TPJNC56
GPP_B2/VRALERT# CC36
INPUT3VSEL BT27 INPUT3VSEL

2018/01/30 3V Select Strap
Low ->3.3V +-5%
High -> 3.0V +-5%

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WHL-i7-8565U
OAC-14C1001-I06

+3VSUS
C0.1u25X50201-HF C635
U22
SN74AHC1G08DCKR_SC70-RH
<30,31,36> BUF_PLT_RST#
R297 100KR0402
U12
SN74AHC1G08DCKR_SC70-RH
<32> TBT_RST_N
R168 100KR0402
R589 10KR0402
TBT_PERST_N <8>
R176 X_10KR0402

+3VSUS
R378 X_4.7KR0402
INPUT3VSEL
R354 4.7KR0402

+3VSUS
+VCCST
C480 C0.1u25X50201-HF
R173 1KR0402
U13
74AHC1G07GW_SOT353-RH
<30,41> EC_ALLSYSPG
VCCST_PWRGD_R R180 60.4R1%0402 VCCST_PWRGD
2018.06.13 VCCST_PWRGD of signal add series resistor to follow PDG suggest

MICRO-STAR INT'L CO.,LTD.
Title: Whiskey lake U (LPSS;ISH;I2C)
Size: Custom
Document Number: MS-14C1
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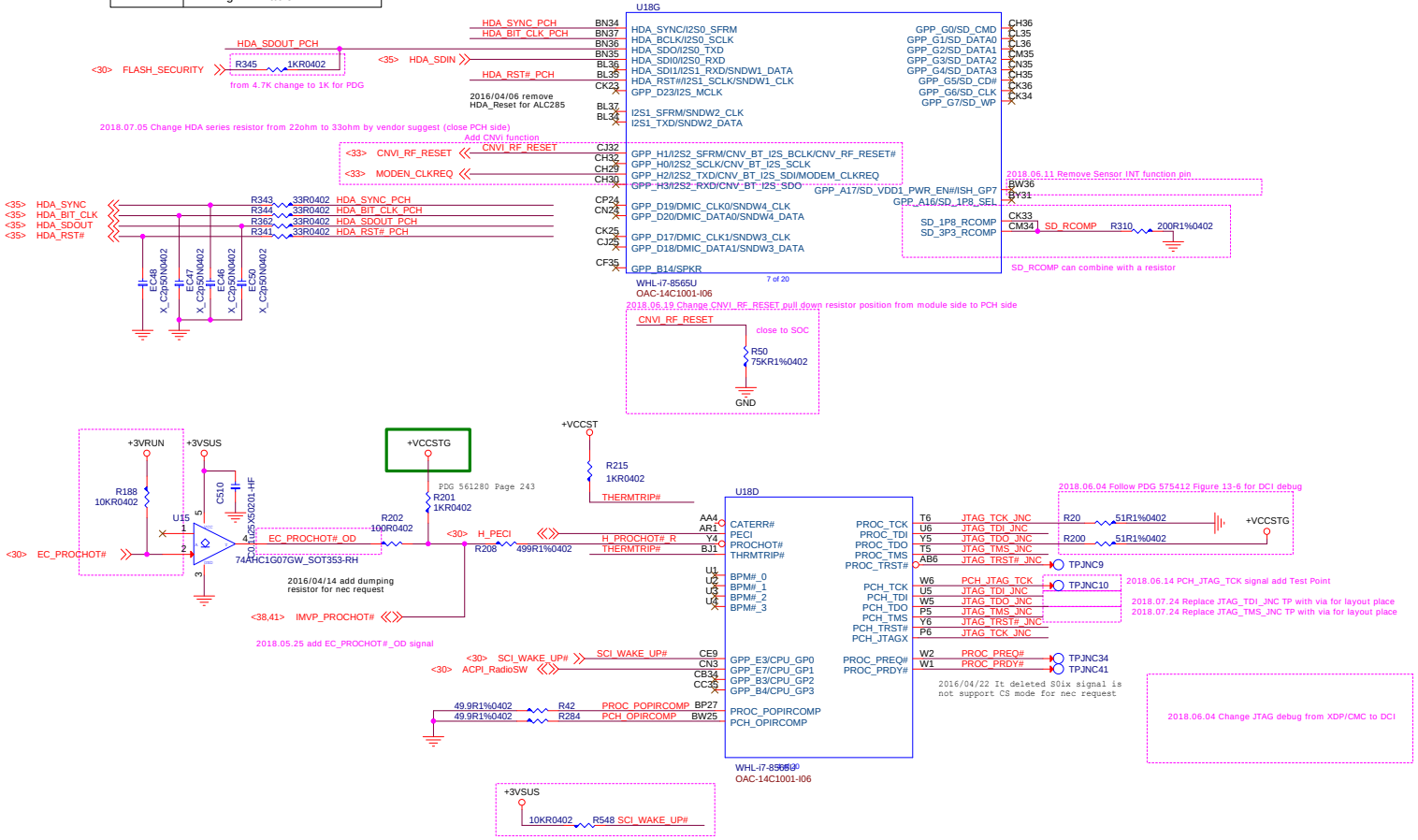
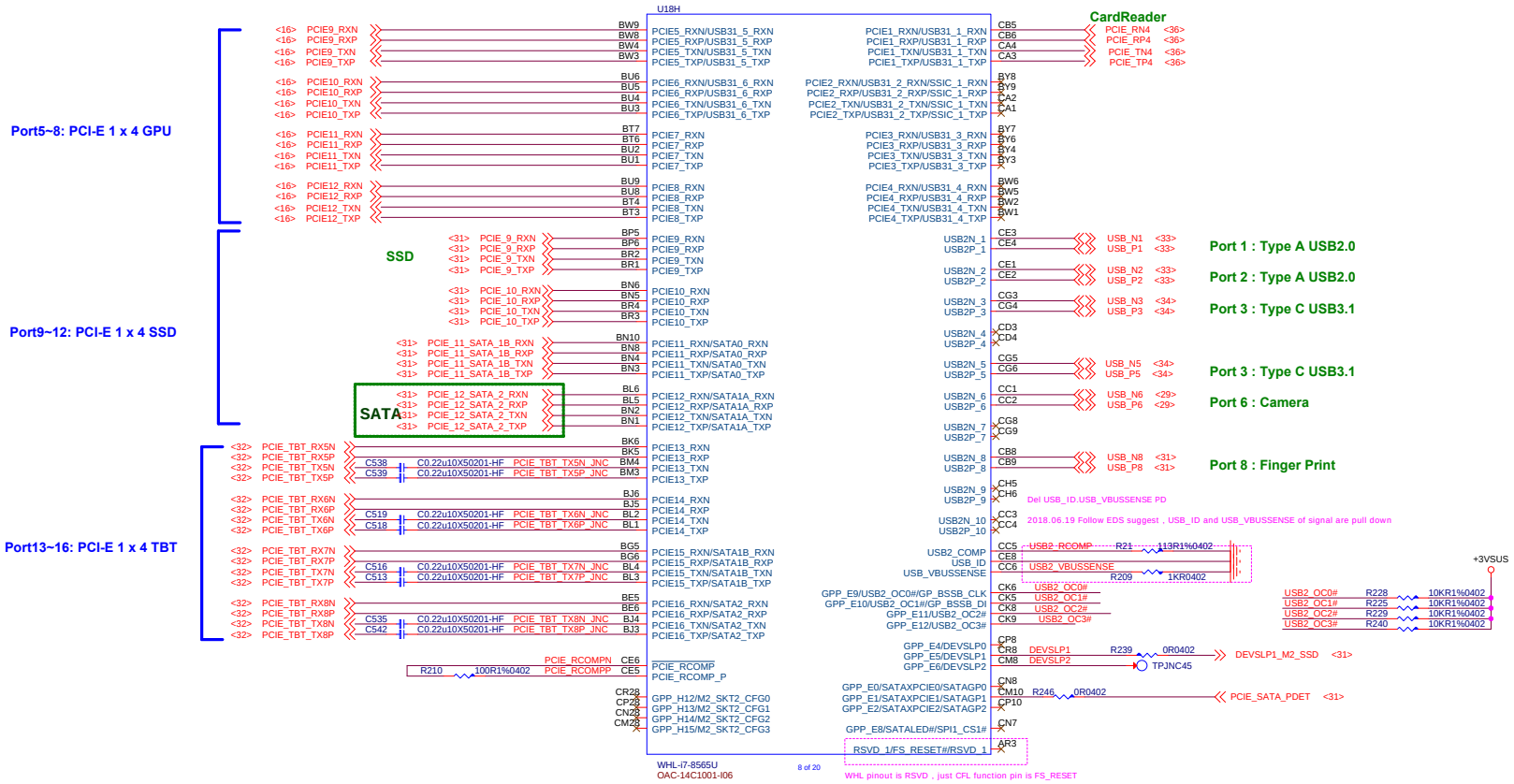
Date: Monday, April 22, 2019
Sheet 8 of 56

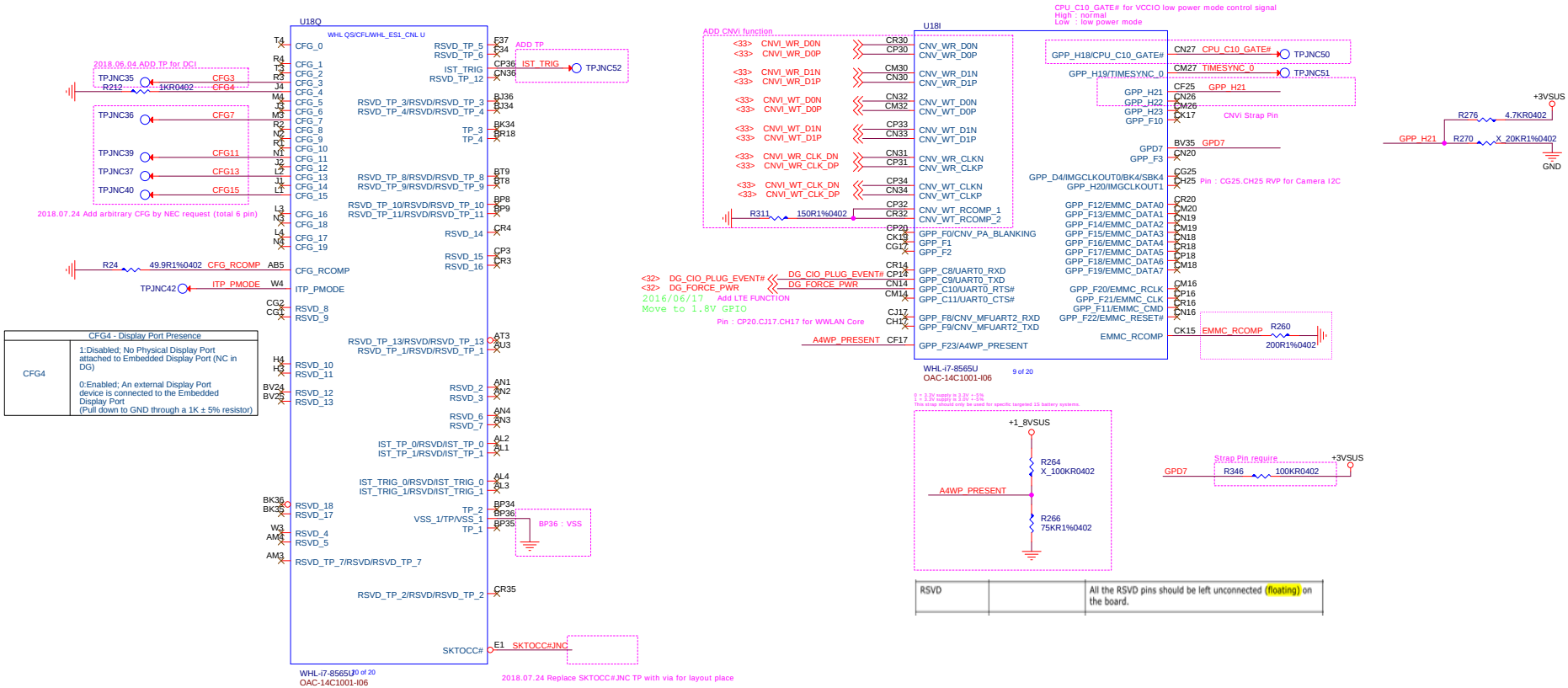
Flash Descriptor Security Override	
HDA_SDO	Low = Disable High = Enable



MICRO-STAR INT'L CO.,LTD.		
Title: Whiskey lake U(HDA;MISC,JTAG)		
Size: Custom	Document Number: MS-14C1	Rev: 0A
Date: Monday, April 22, 2019	Sheet 9 of 56	



MICRO-STAR INT'L CO.,LTD.			
Title: Whiskey lake U(PCIE;USB;SATA)			
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 10 of 56		



Title	Whiskey lake U (CFG;CSI;RSVD)
Size	Custom
Document Number	MS-14C1
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Date:	Monday, April 22, 2019
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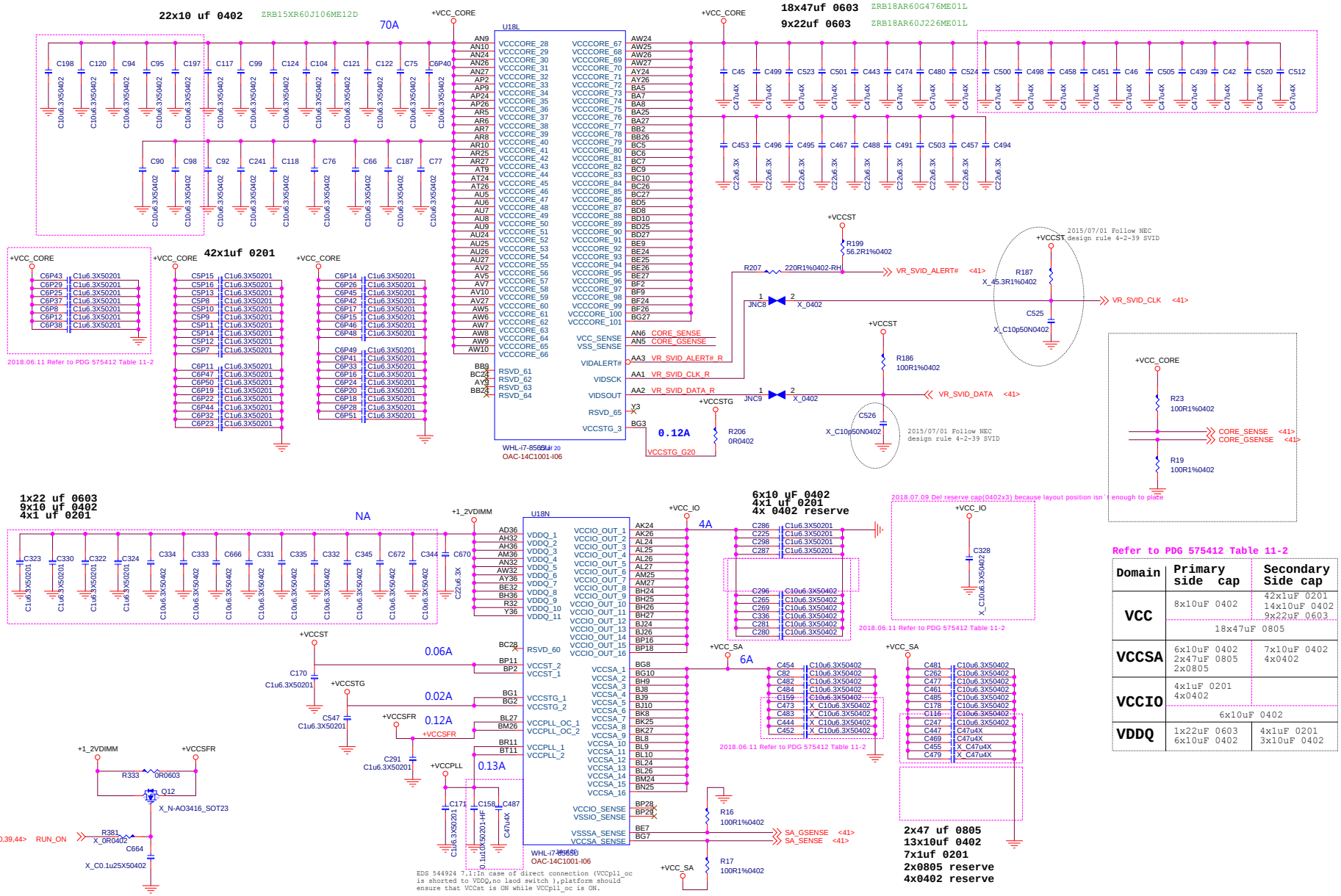
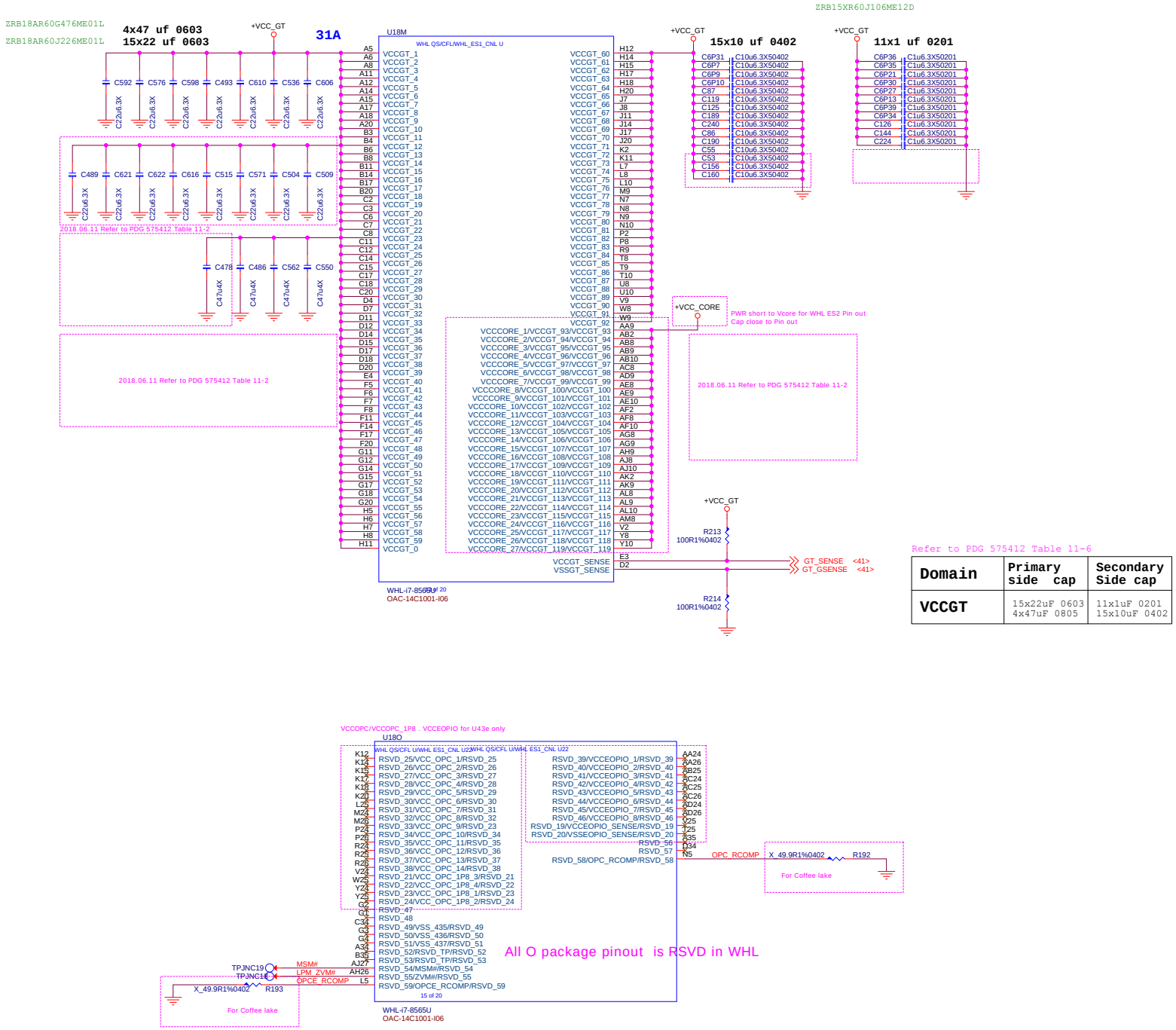
MICRO-STAR INT'L CO.,LTD.



Refer to PDG 575412 Table 11-2

Domain	Primary side cap	Secondary Side cap
VCC	8x10uF 0402	42x1uF 0201 14x10uF 0402 9x22uF 0603
	18x47uF 0805	
VCCSA	6x10uF 0402 2x47uF 0805 2x0805	7x10uF 0402 4x0402
VCCIO	4x1uF 0201 4x0402	
	6x10uF 0402	
VDDQ	1x22uF 0603 6x10uF 0402	4x1uF 0201 3x10uF 0402

MICRO-STAR INT'L CO.,LTD.			
Title: Whiskey lake U (CPU POWER)			
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 12 of 56		



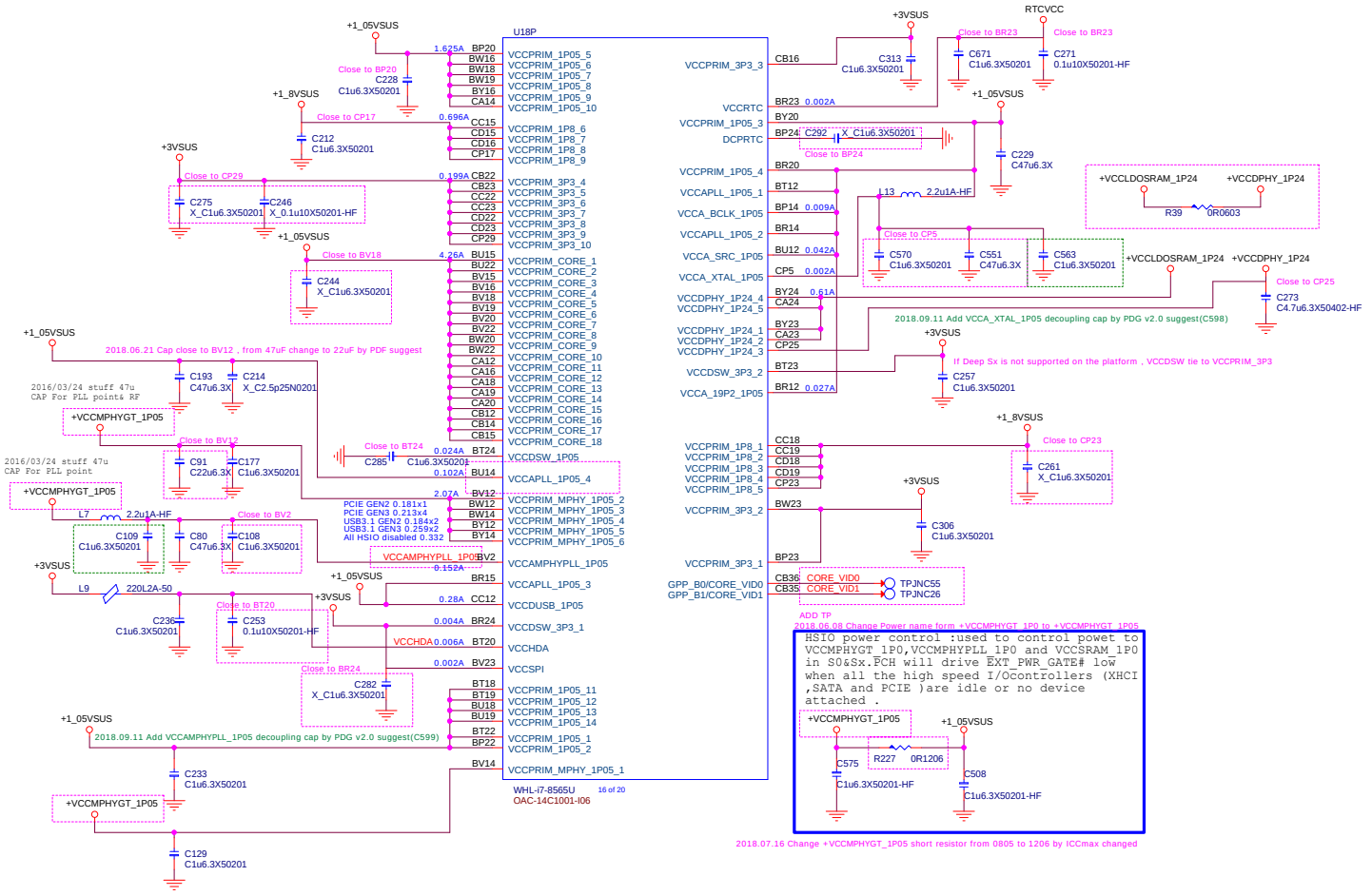
Domain	Primary side cap	Secondary Side cap
VCCGT	15x22uF 0603 4x47uF 0805	11x1uF 0201 15x10uF 0402

MICRO-STAR INT'L CO.,LTD.

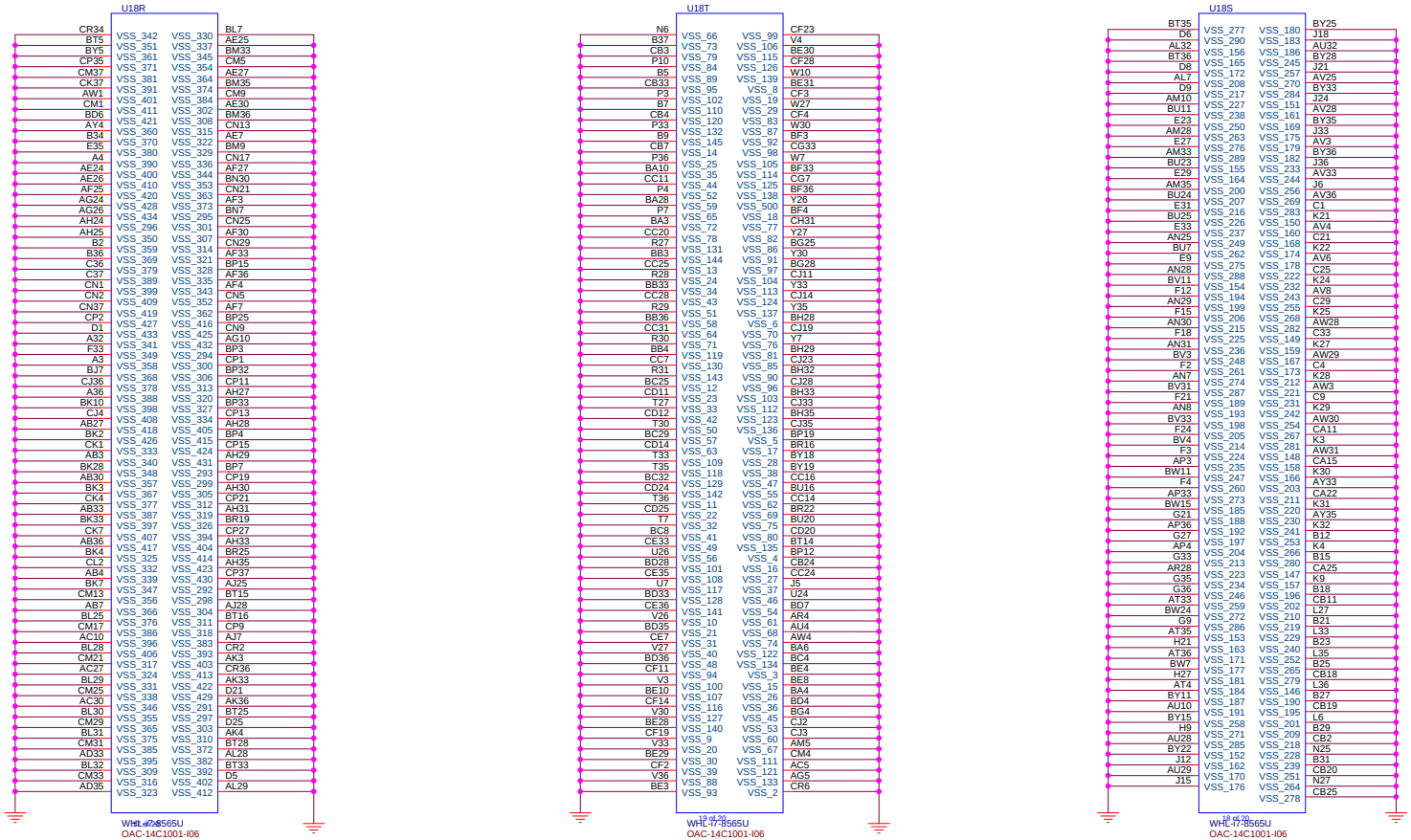
Title: Whiskey lake U (GT POWER)

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 | Sheet 13 of 56



MICRO-STAR INT'L CO.,LTD.			
Title: Whiskey lake U (PCH POWER)			
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 14 of 56		



MICRO-STAR INT'L CO.,LTD.

Title: Whiskey lake U (GND)

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 | Sheet 15 of 56

Reference 14B2

GPU PCI EXPRESS

20181025

G5009 — X_N18E-G2-A1 — OB3-1W1E003-N08

G5008 — X_N18E-G1-KD-A1 — OB3-16P7003-N08

N18:0.47u*15,change 10,4.7u*3,10u*3,22u*2
N17:1u*4,4.7u*2,10u,22u*1

N18 :1u*6

Under GPU: C128 C1u6.3X60201, C147 C1u6.3X60201, C123 C1u6.3X60201, C136 C1u6.3X60201 — 1uF*4 X6S

Near GPU: C44 C4.7u6.3X60402-HF, C410 C4.7u6.3X60402-HF — 4.7uF*3 X6S

PEX_VDD 3A: C426 C22u6.3X0603, C43 C22u6.3X0603 — 22uF*2 X5R

PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N17P	4	2	1	1
N18P	6	3	3	2

PEX_DVDD: AG21, AG22, AG24, AH25, AG19, AH21

C140 C1u6.3X60201, C152 C1u6.3X60201 — 1uF*2X6S

C421 C10u4X60603, C161 C10u4X60603, C418 C10u4X60603, C38 C4.7u6.3X60402-HF — 10uF*3 X6S

N18 :1u*7

Under GPU: C208 C1u6.3X60201, C192 C1u6.3X60201, C201 C1u6.3X60201, C174 C1u6.3X60201 — 1uF*4 X6S

Near GPU: C88 C10u4X60603, C97 C10u4X60603, C555 C10u4X60603 — 10uF*3 X6S; C543 C22u6.3X0603, C544 C22u6.3X0603 — 22uF*2 X5R

1V8_MAIN 0.9A

PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N17P	4	2	2	1
N18P	7	3	3	2

PEX_HVDD: AG13, AG15, AG16, AG18, AG25, AH15, AH18, AH26, AH27, AJ27, AK27, AL27, AM28, AN28

C185 C1u6.3X60201, C259 C1u6.3X60201, C250 C1u6.3X60201 — 1uF*3 X6S

C679 C4.7u6.3X60402-HF, C183 C4.7u6.3X60402-HF, C676 C4.7u6.3X60402-HF — 4.7uF*3 X6S

Under GPU: 1V8_MAIN; PEX_PLL_HVDD AH12; C73 C1u6.3X60201, C545 X_C0.1u25X70402

wake# NC

C1A COMMON — 1/17 PCI_EXPRESS

TP7

<27> GPU_RST# — GC6_GPU_WAKE# AJ11 — PEX_WAKE

R295 100KR0402 — AJ12 — PEX_RST

1V8_AON — R263 10KR0402 — PEX_CLKREQ# AK12 — PEX_CLKREQ

<7> GFX_REFCLK — AL13 — PEX_REFCLK

<7> GFX_REFCLK# — AK13 — PEX_REFCLK

<10> PCIE9_RXP	C230 C0.22u10X50201-HF	PEG_C_TXP1_JNC	AK14	PEX_TX0
<10> PCIE9_RXN	C221 C0.22u10X50201-HF	PEG_C_TXN1_JNC	AJ14	PEX_TX0
<10> PCIE9_TXP	C615 C0.22u10X50201-HF	PEG_C_RXP1_JNC	AN12	PEX_RX0
<10> PCIE9_TXN	C611 C0.22u10X50201-HF	PEG_C_RXN1_JNC	AM12	PEX_RX0
<10> PCIE10_RXP	C186 C0.22u10X50201-HF	PEG_C_TXP2_JNC	AH14	PEX_TX1
<10> PCIE10_RXN	C175 C0.22u10X50201-HF	PEG_C_TXN2_JNC	AG14	PEX_TX1
<10> PCIE10_TXP	C607 C0.22u10X50201-HF	PEG_C_RXP2_JNC	AN14	PEX_RX1
<10> PCIE10_TXN	C608 C0.22u10X50201-HF	PEG_C_RXN2_JNC	AM14	PEX_RX1
<10> PCIE11_RXP	C162 C0.22u10X50201-HF	PEG_C_TXP3_JNC	AK15	PEX_TX2
<10> PCIE11_RXN	C153 C0.22u10X50201-HF	PEG_C_TXN3_JNC	AJ15	PEX_TX2
<10> PCIE11_TXP	C605 C0.22u10X50201-HF	PEG_C_RXP3_JNC	AP14	PEX_RX2
<10> PCIE11_TXN	C602 C0.22u10X50201-HF	PEG_C_RXN3_JNC	AP15	PEX_RX2
<10> PCIE12_RXP	C146 C0.22u10X50201-HF	PEG_C_TXP4_JNC	AL16	PEX_TX3
<10> PCIE12_RXN	C138 C0.22u10X50201-HF	PEG_C_TXN4_JNC	AK16	PEX_TX3
<10> PCIE12_TXP	C596 C0.22u10X50201-HF	PEG_C_RXP4_JNC	AN15	PEX_RX3
<10> PCIE12_TXN	C593 C0.22u10X50201-HF	PEG_C_RXN4_JNC	AM15	PEX_RX3

AK17	AJ17	PEX_TX4 PEX_TX4
AN17	AM17	PEX_RX4 PEX_RX4
AH17	AG17	PEX_TX5 PEX_TX5
AP17	AP18	PEX_RX5 PEX_RX5
AK18	AJ18	PEX_TX6 PEX_TX6
AN18	AM18	PEX_RX6 PEX_RX6
AL19	AK19	PEX_TX7 PEX_TX7
AN20	AM20	PEX_RX7 PEX_RX7
AK20	AJ20	PEX_TX8 PEX_TX8
AP20	AP21	PEX_RX8 PEX_RX8
AH20	AG20	PEX_TX9 PEX_TX9
AN21	AM21	PEX_RX9 PEX_RX9
AK21	AJ21	PEX_TX10 PEX_TX10
AN23	AM23	PEX_RX10 PEX_RX10
AL22	AK22	PEX_TX11 PEX_TX11
AP23	AP24	PEX_RX11 PEX_RX11
AK23	AJ23	PEX_TX12 PEX_TX12
AN24	AM24	PEX_RX12 PEX_RX12
AH23	AG23	PEX_TX13 PEX_TX13
AN26	AM26	PEX_RX13 PEX_RX13
AK24	AJ24	PEX_TX14 PEX_TX14
AP26	AP27	PEX_RX14 PEX_RX14
AL25	AK25	PEX_TX15 PEX_TX15
AN27	AM27	PEX_RX15 PEX_RX15

PEX_TERMP AP29 — PEX_TERMP — R170 2.49KR1%0402 — GND

GPU CLK REQ#

1V8_MAIN — PEX_CLKREQ# — Q10 N-AO3414_SOT23-3 — GPU_CLKREQ# <7>

Vgs=1.8V

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_PCI-E Host

Size: Custom — Document Number: MS-14C1 — Rev: 10

Date: Monday, April 22, 2019 — Sheet 16 of 56

Reference 14B2

GPU Frame Buffer Partition A/B

51B COMMON — 2/17 FBA

51C COMMON — 3/17 FBB

GDDR5 Mode F Mapping By GB4C-128

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

FB_REFPLL_AVDD — K27 — FB_PLLAVDD — C573 C4.7u6.3X6S0402 — GND

FBVDDQ — R145 10KR1%0402 — R147 10KR1%0402 — FBA_CMD<14> FBA_CMD<30> — R150 10KR1%0402 — R148 10KR1%0402 — FBA_CMD<13> FBA_CMD<29> — GND

FBVDDQ — R238 10KR1%0402 — R223 10KR1%0402 — FBB_CMD<14> FBB_CMD<30> — R224 10KR1%0402 — R237 10KR1%0402 — FBB_CMD<13> FBB_CMD<29> — GND

1V8_MAIN — LB8 30L5A-0603-0.01R — 1.5A

Under GPU: C79 C1u6.3X60201, C85 C1u6.3X60201, C572 C22u6.3X0603 — GND

LB1 30ohm 0.01ohm wond 10/08

Under GPU: FB_PLLAVDD — C168 C1u6.3X0402 — GND

FB_VREF — R12 1KR1%0402 — C67 X_C3.9p50N0402 — GND

FB_VREF	
N17P	NC
N18P	1K ohm pull-down

N18:4.7u*2, 22u*1,0.47*3
N17:0.1U*3,22U*1,

PBA_PLL_AVDD	0.1uF X7R	1uF X6S
N17P	3 2	0
N18P	0	2

PBx_PLL_AVDD	4.7uF X6S	22uF X6S
N17P	1	1
N18P	2 1	1

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MSI MICRO-STAR INT'L CO.,LTD.

Title: DGPU_MEM IF A/B

Size: Custom | Document Number: MS-14C1 | Rev: 10

Date: Monday, April 22, 2019 | Sheet 17 of 56

Reference 14B2

DGPU_GDDR5 FrameBuffer A0

M7D INS159544858 — NORMAL — MT51J256M32HF-80

M7A INS159544638 — NORMAL — MT51J256M32HF-80

M7B INS159544733 — MT51J256M32HF-80

M7C INS159544367 — Normal — MT51J256M32HF-80

FBVDDQ

Near DRAM 22µF x 5

Near DRAM 10µF x 2

Under DRAM 10µF x 4

Under DRAM 1µF x 18

GND

MICRO-STAR INT'L CO.,LTD.

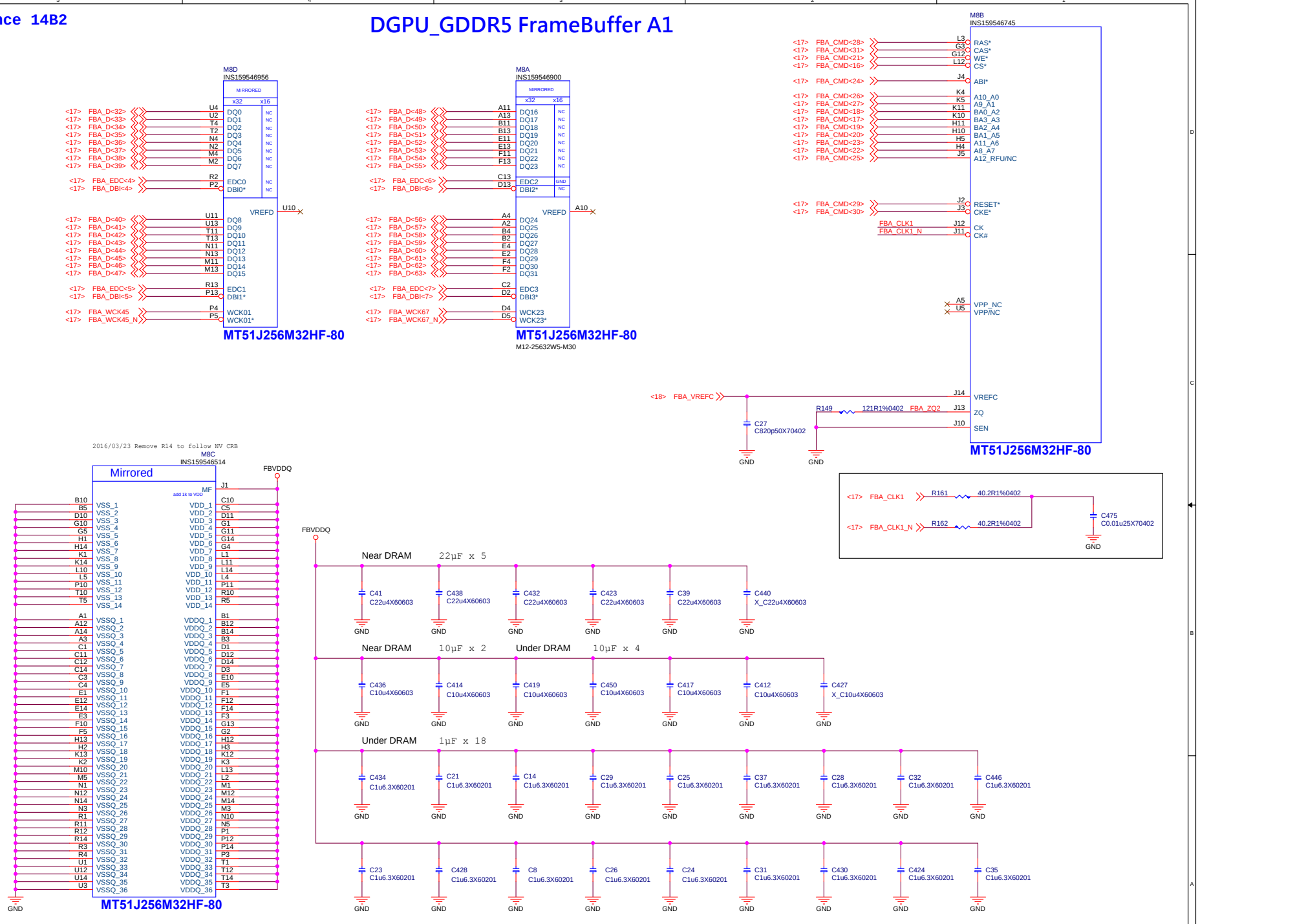
Title: DGPU_GDDR5 FrameBuffer A0

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 | Sheet 18 of 56

Reference 14B2

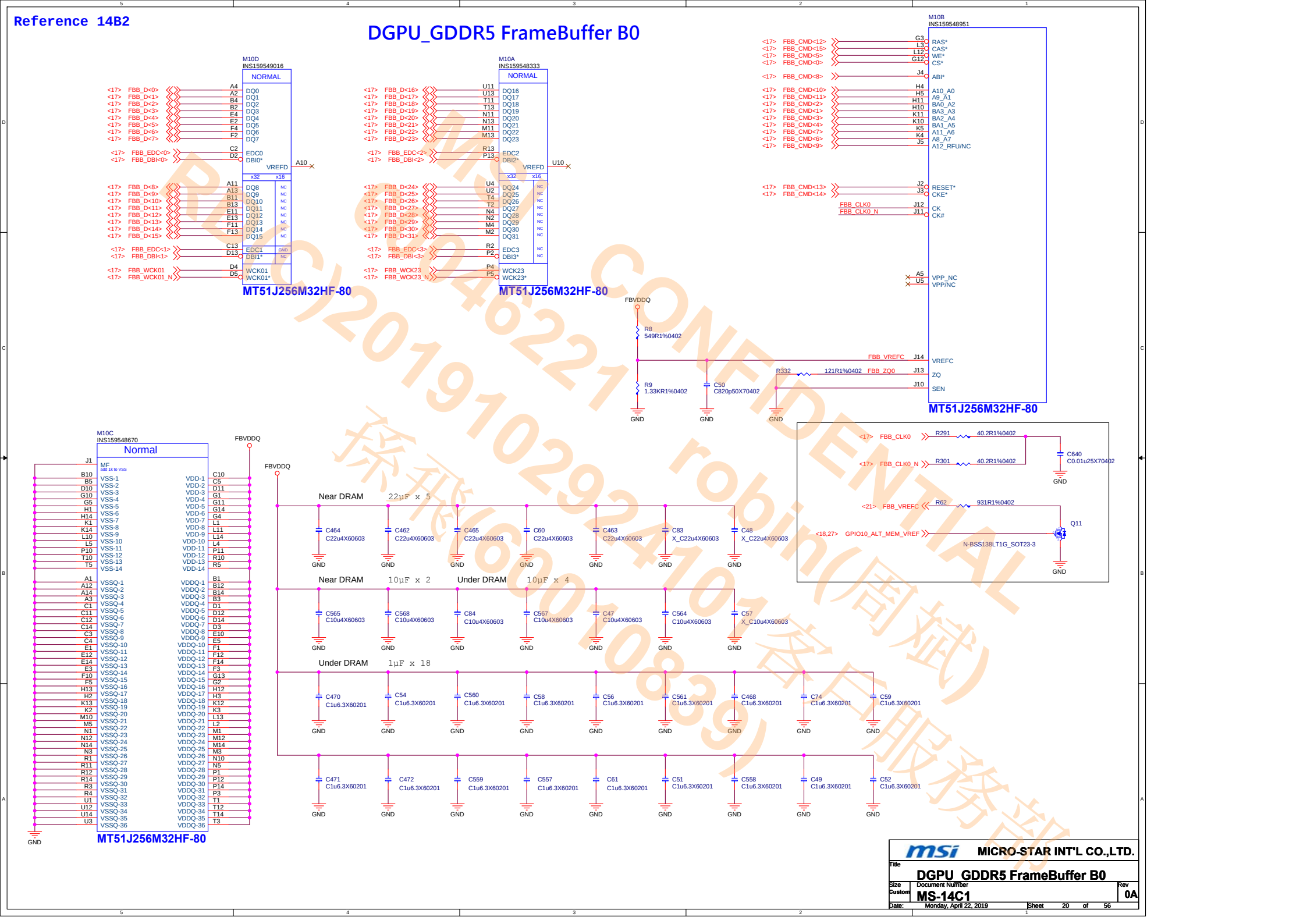
DGPU_GDDR5 FrameBuffer A1



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GDDR5 FrameBuffer A1			
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 19 of 56		

Reference 14B2

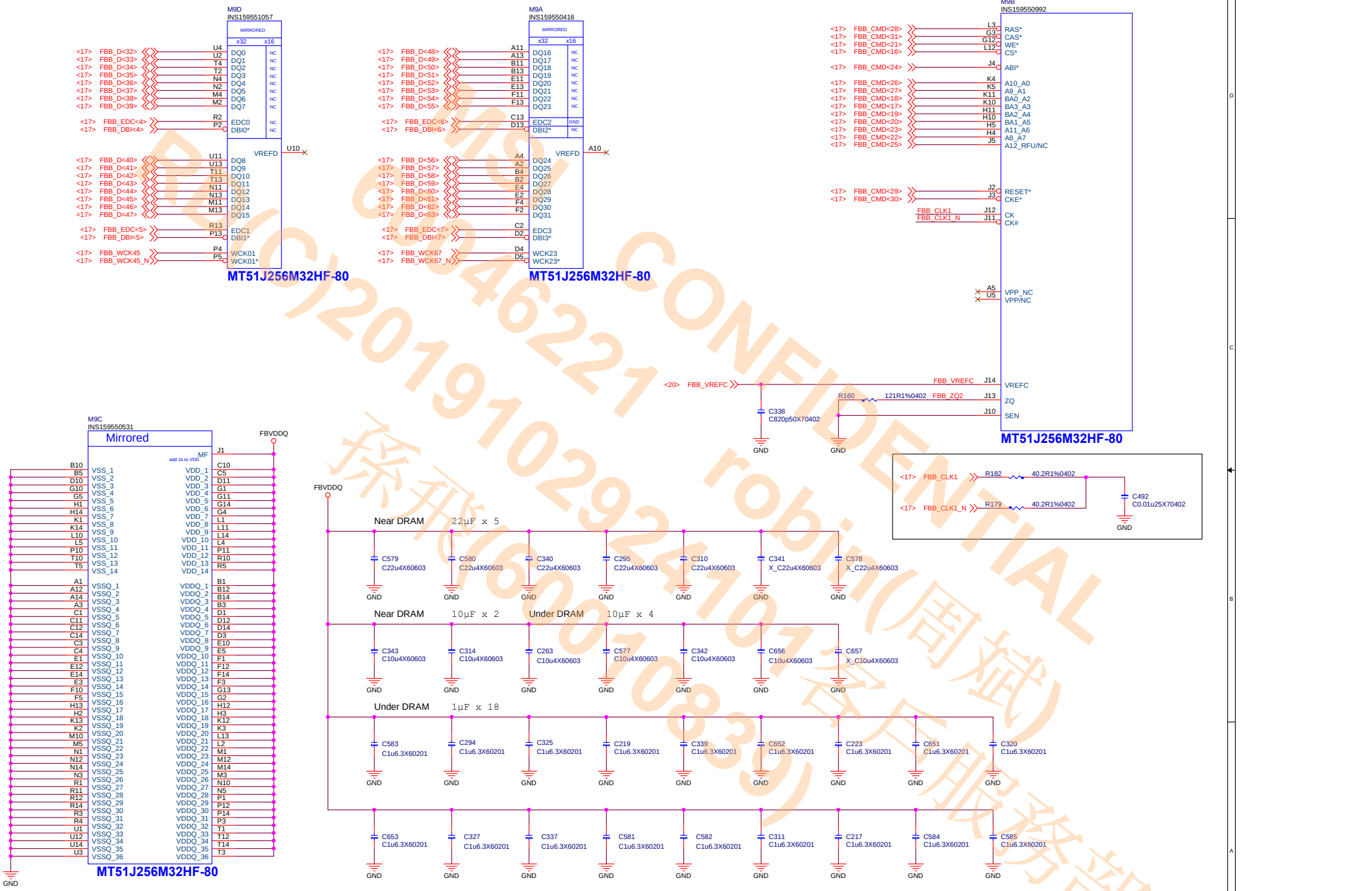
DGPU_GDDR5 FrameBuffer B0



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GDDR5 FrameBuffer B0			
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 20 of 56		

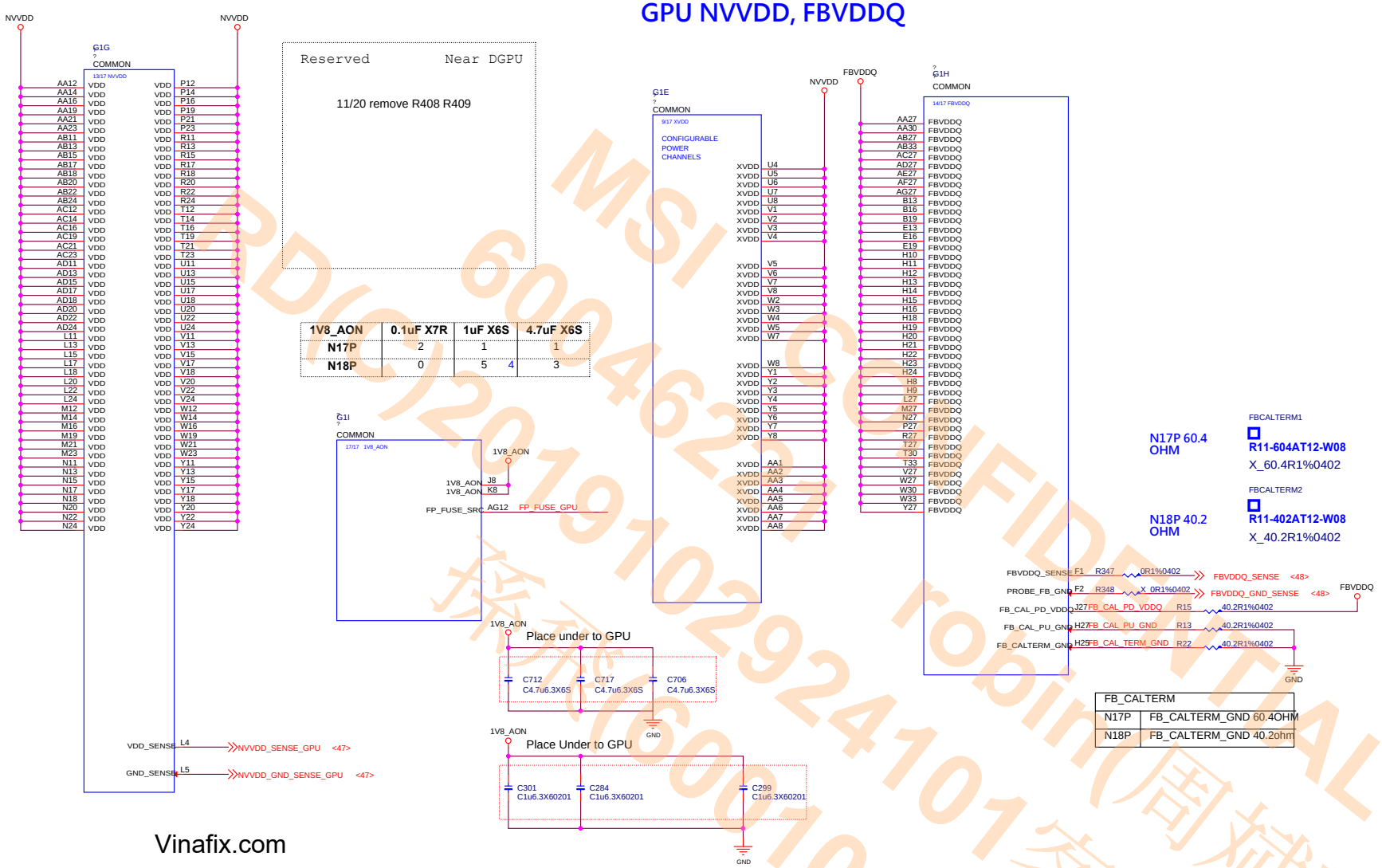
Reference 14B2

DGPU_GDDR5 FrameBuffer B1



MSI	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_GDDR5 FrameBuffer B1
Size: Custom	Document Number: MS-14C1
Rev	0A
Date: Monday, April 22, 2019	Sheet 21 of 56

GPU NVVDD, FBVDDQ



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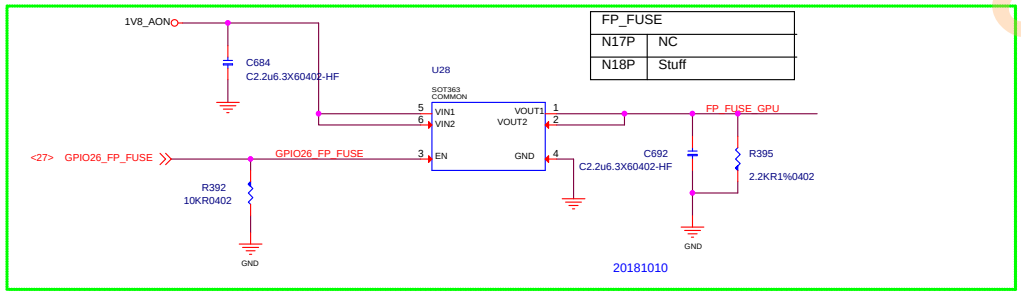
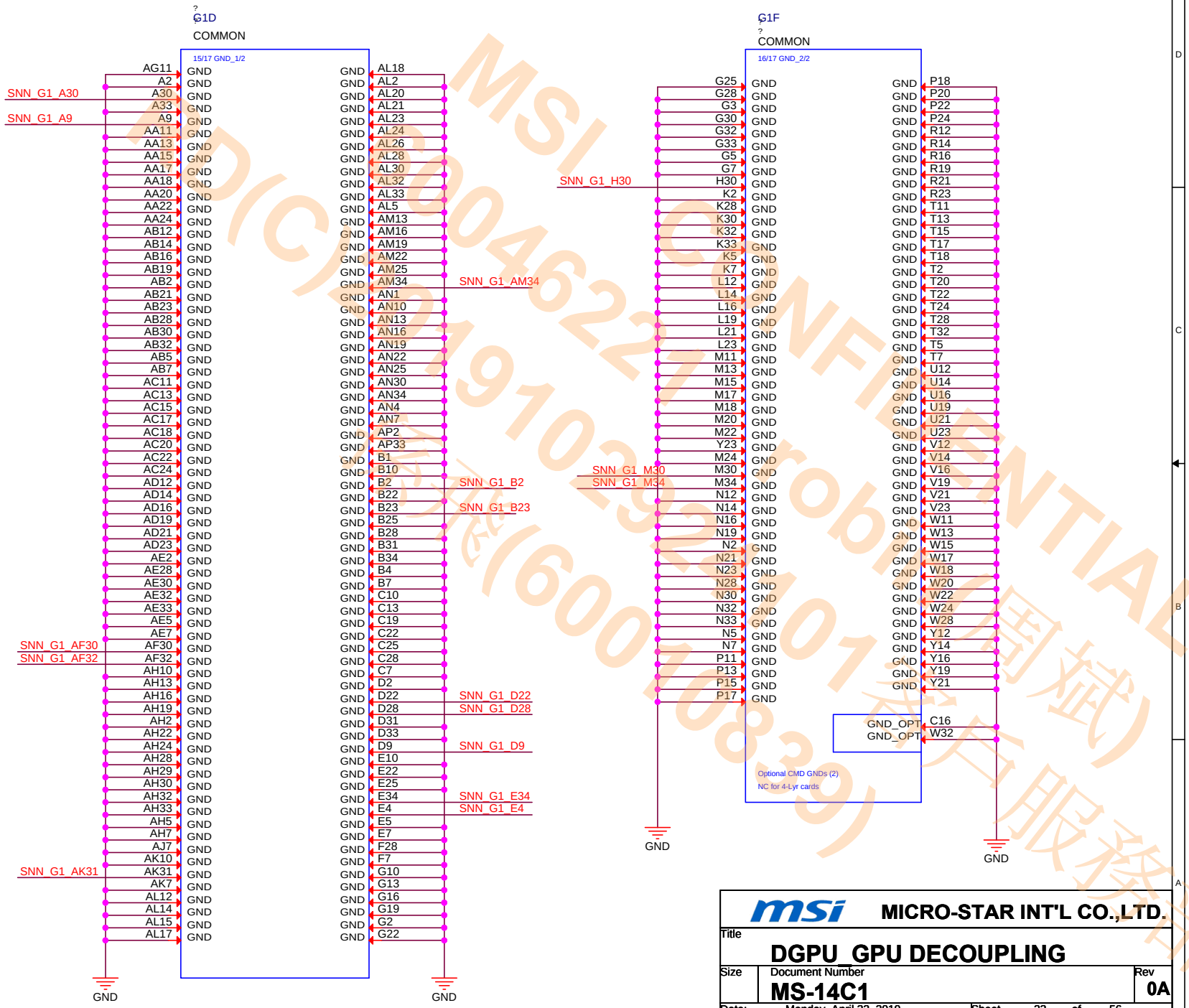


MSI	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_POWER
Size / Custom	Document Number: MS-14C1
Rev	0A
Date:	Monday, April 22, 2019
Sheet	22 of 56

DGPU GND



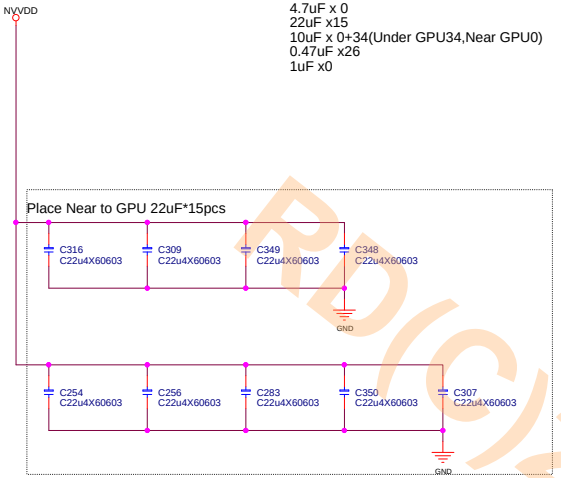
msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_GPU DECOUPLING	
Size	Document Number MS-14C1	Rev 0A
Date: Monday, April 22, 2019	Sheet 23 of 56	

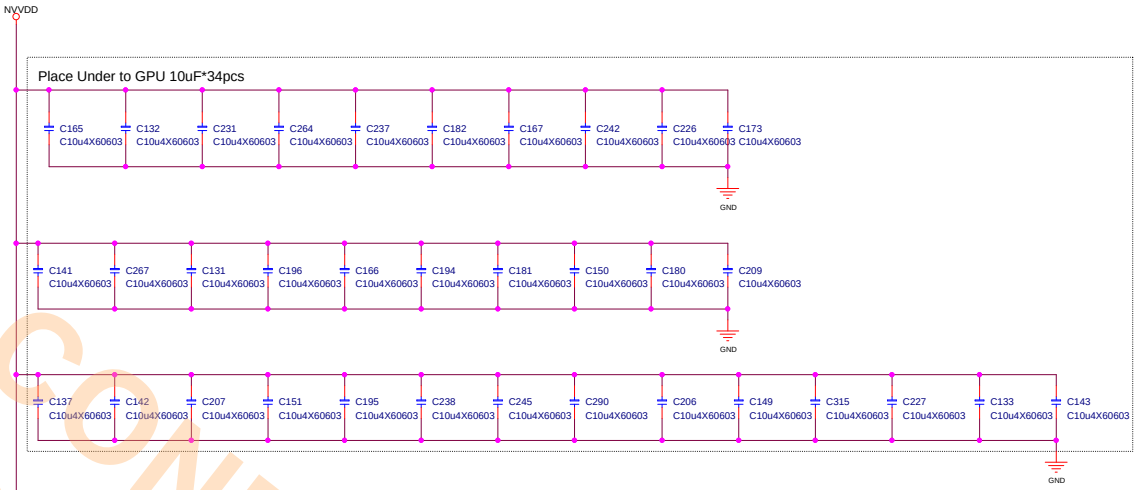
GPU DECOUPLING

NVVDD

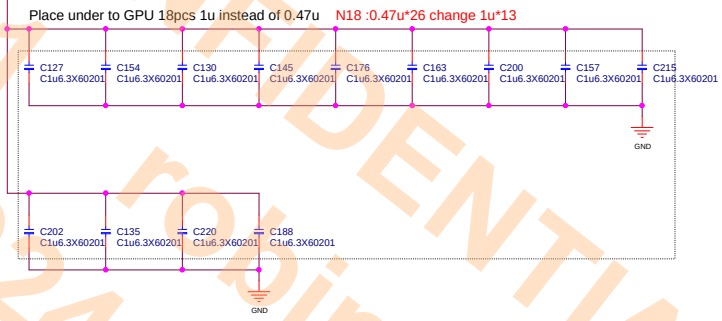
N18P
330uF x0
4.7uF x 0
22uF x15
10uF x 0+34(Under GPU34,Near GPU0)
0.47uF x26
1uF x0

N17P
330uF x1
4.7uF x 2
22uF x10
10uF x 11+21(Under GPU21,Near GPU11)
0.47uF x0
1uF x 13





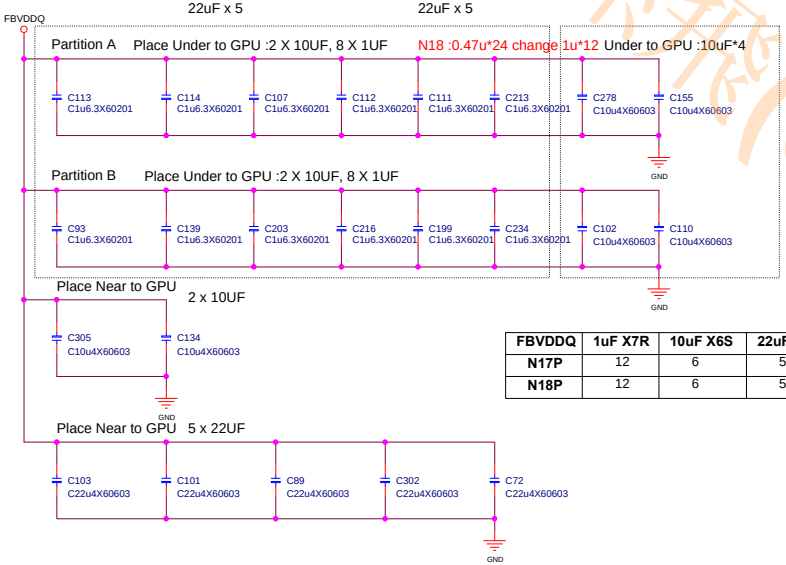
NVVDD	1uF X7R	4.7uF X6S	10uF X6S	22uF X6S
N17P	13	2	31	10
N18P	13	0	34	15 9



FBVDDQ

1uF x 16 N18P
10uF x 6
22uF x 5

1uF x 12 N17P
10uF x 6
22uF x 5



FBVDDQ	1uF X7R	10uF X6S	22uF X6S
N17P	12	6	5
N18P	12	6	5

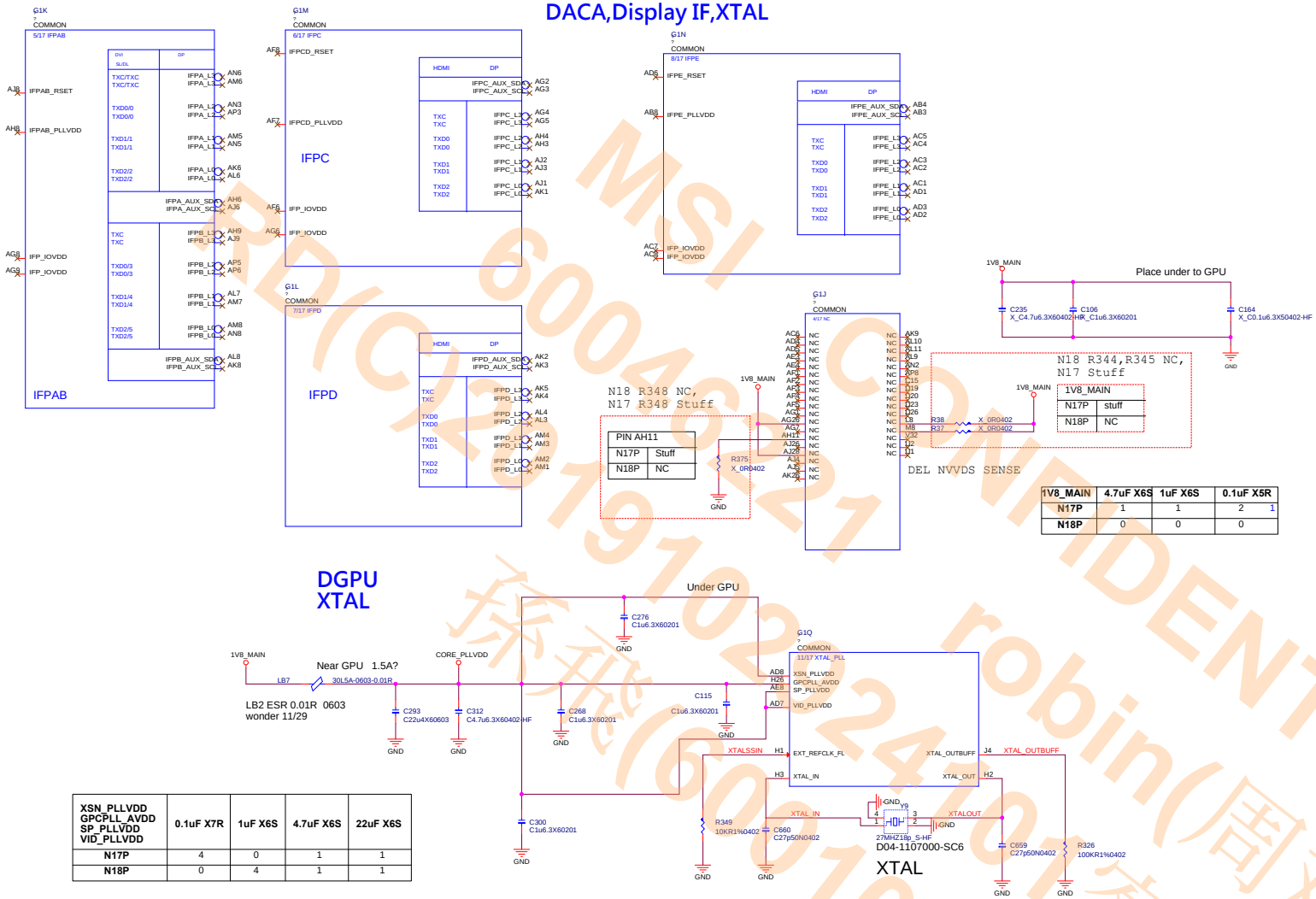
MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING

Size: | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 Sheet 24 of 56

DACA,Display IF,XTAL



1V8_MAIN	4.7uF X6S	1uF X6S	0.1uF X5R	
N17P	1	1	2	1
N18P	0	0	0	

DGPU XTAL

XSN_PLLVDD GPCPLL_AVDD SP_PLLVDD VID_PLLVDD	0.1uF X7R	1uF X6S	4.7uF X6S	22uF X6S
N17P	4	0	1	1
N18P	0	4	1	1

MICRO-STAR INT'L CO.,LTD.

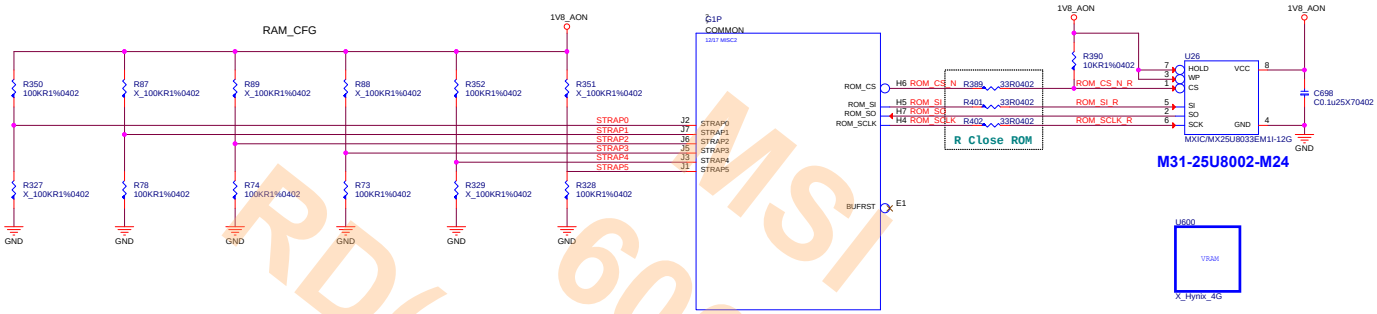
Title: DACA,Display IF,XTAL

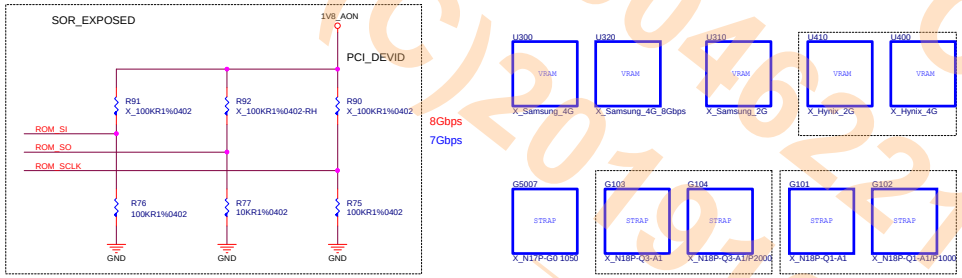
Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 | Sheet 25 of 56

Reference 14B2

ROM, MULTI-LEVEL STRAPS





ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE	
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE	
L	L	H	1110		
L	H	L	1101		
L	H	H	1100		
H	L	L	1011		
H	L	H	1010		
H	H	L	1001		
H	H	H	1000		
L	L	M	0111		
L	M	L	0110		
L	M	H	0101		
L	H	M	0100		
H	L	M	0011		
H	M	L	0010		
H	M	H	0001		
H	H	M	0000	V	

GPU	ROM_SO
N17P	100k
N18P	10k

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE	
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE FS_OVERT	N18P
H	H	M	0000	V	N17P

	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		STRAP Set
N17P	L	L	L	**0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28**	4GB	R116 R120 R388
	L	L	H	0x1 Micron: MT51J256M32HF-70:A		R116 R120 R398
	L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	4GB	R116 R127 R388
	L	H	H			
	H	L	L			
	H	L	H			
	H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	2GB	R129 R127 R388
	H	H	H	**0x7 Samsung: M12-41325A5-S02/K4G41325FE-HC28**	2GB	R129 R127 R398
	L	L	M	0x8 Micron: EDW032BABG-70-F:A		R116 R120 R398/R388
	L	M	L			

	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		STRAP Set
N18P	L	L	L	**0x0 Samsung: K4G80325FC-HC25 :C**	4GB	R116 R120 R388
	L	L	H	0x1 Micron: MT51J256M32HF-80:B	4GB	R116 R120 R398
	L	H	L	**0x2 Hynix: H5GC8H24AJR-R2C :A**	4GB	R116 R127 R388

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	N18P
L	L	L	0	0	0	0	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

MICRO-STAR INT'L CO.,LTD.

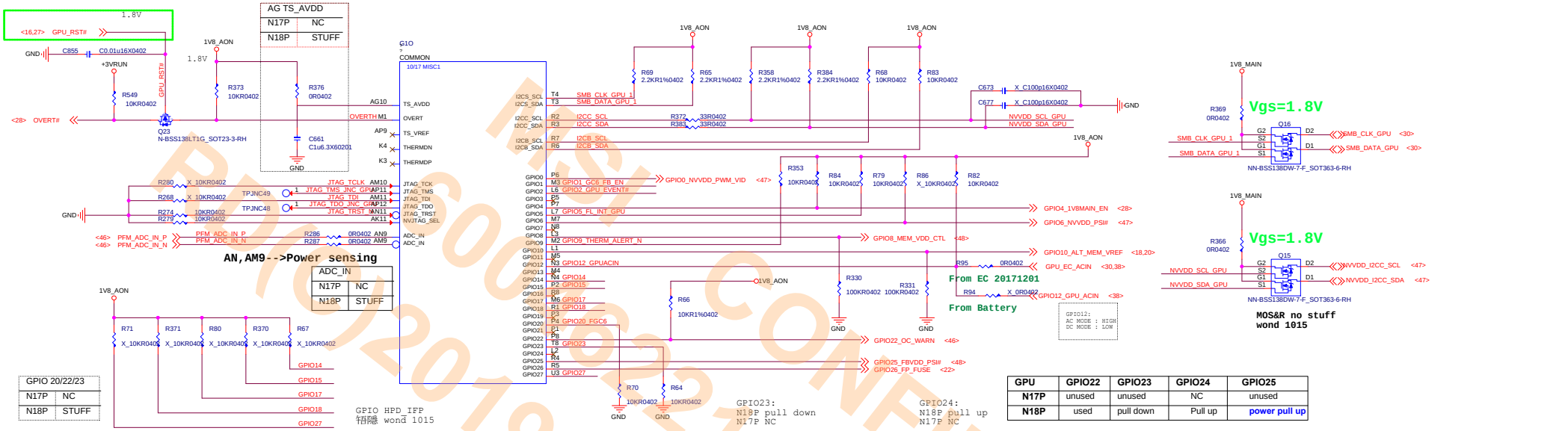
Title: ROM/HW Straps/XTAL

Size: Custom | Document Number: MS-14C1 | Rev: 0A

Date: Monday, April 22, 2019 | Sheet 26 of 56

Reference 14B2

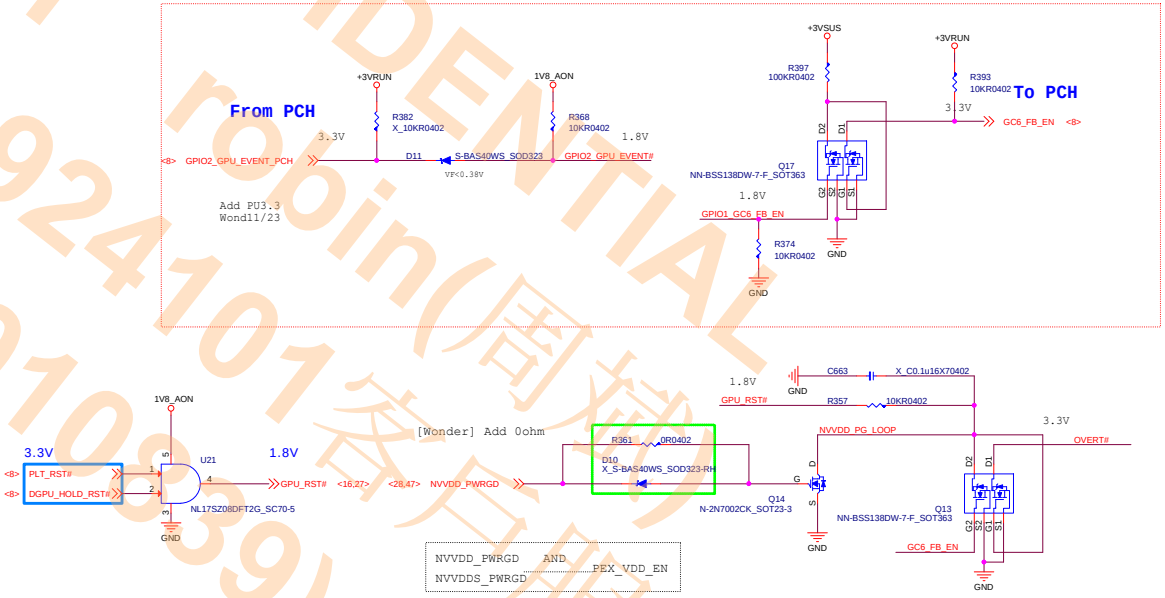
DGPU GPIO, I2C



GPU	GPIO22	GPIO23	GPIO24	GPIO25
N17P	unused	unused	NC	unused
N18P	used	pull down	Pull up	power pull up

teknisi indonesia

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brighteness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDDQ power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	



msi	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_GPIO/I2C
Size / Custom	Document Number: MS-14C1
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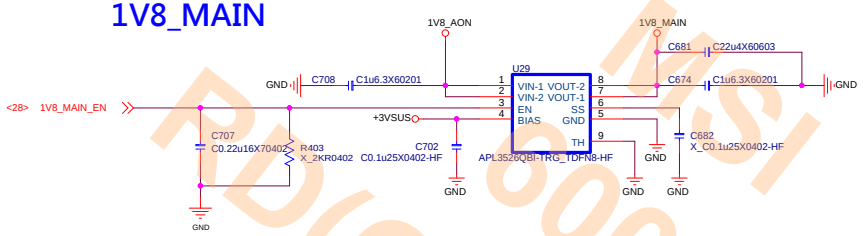
Reference 14B2

NVIDIA Power Sequence Control

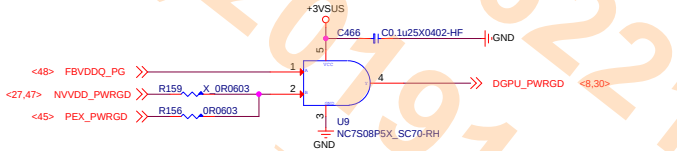
Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV/NVVDD -> NVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power down = NVDDS -> PEX_VDD -> NVVDD/FBVDDQ -> 3V3_NV -> 1V8_MAIN -> 1V8_AON

1V8_MAIN

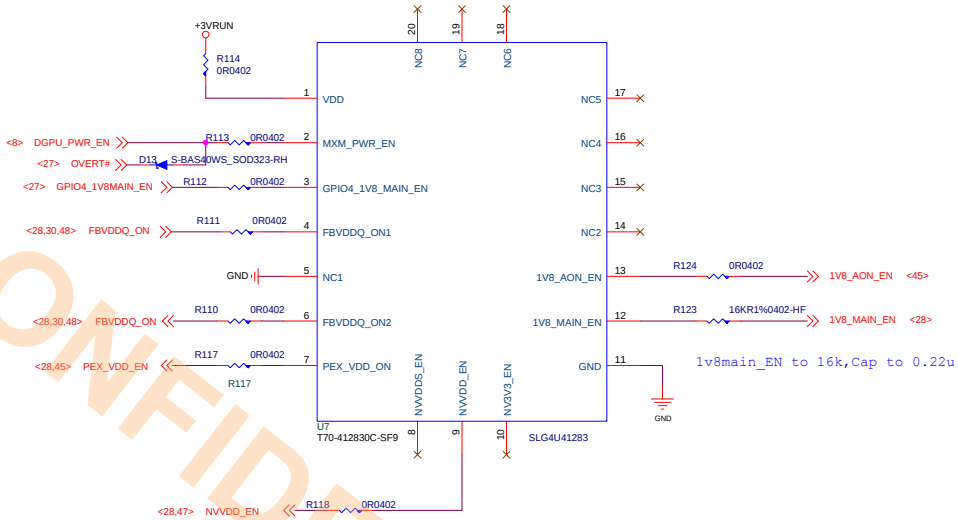


DGPU POWER GOOD

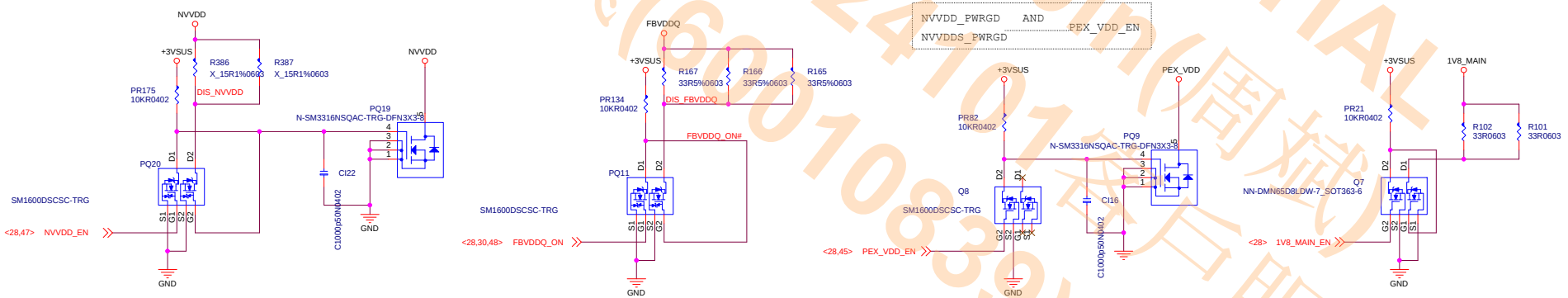


11/05 remove GPU_ON

SLG4U41283 power sequence control IC



Discharge



VGS(th): MIN:1.0 Max:2.0

msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_Power Control	
Size: Custom	Document Number: MS-14C1	Rev: 0A
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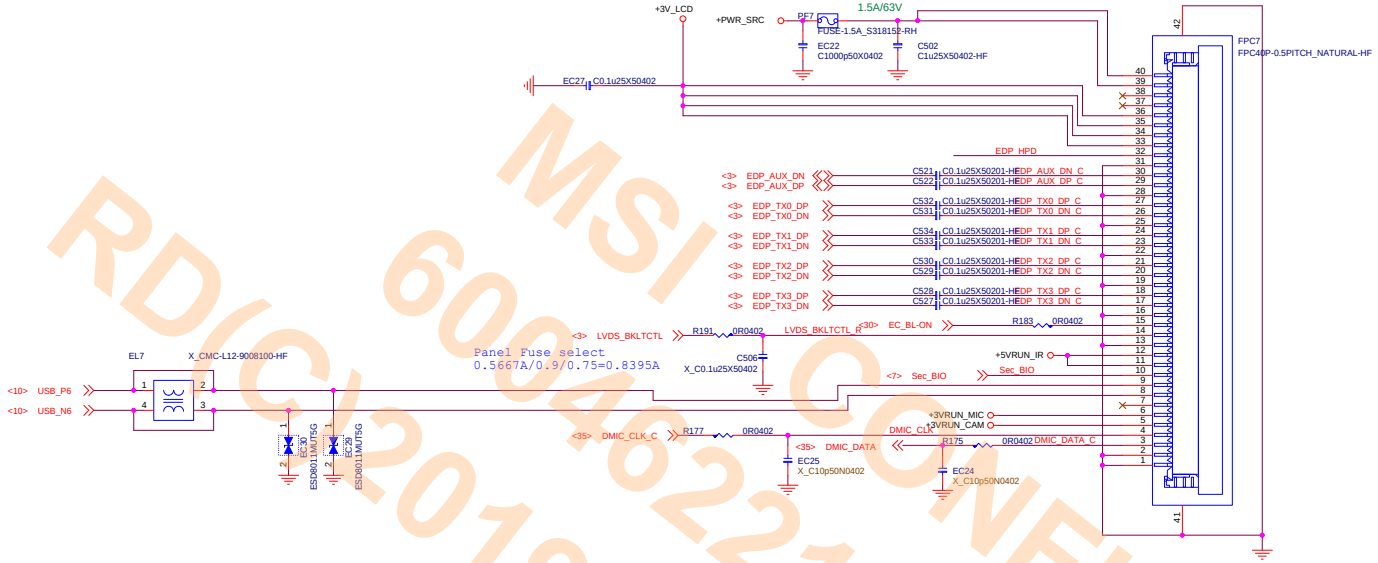
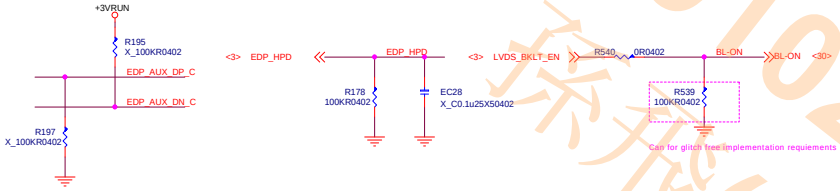
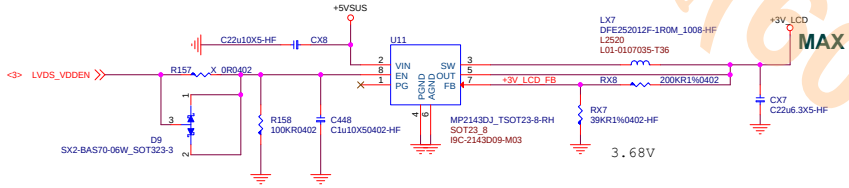
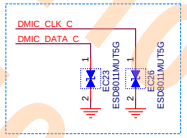
WEBCAM/Internal MIC

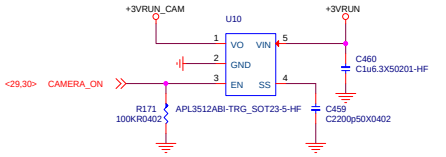
Pannel

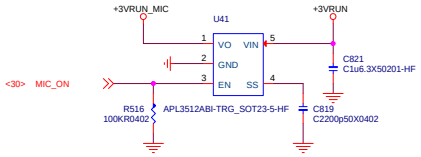


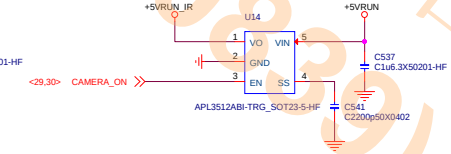




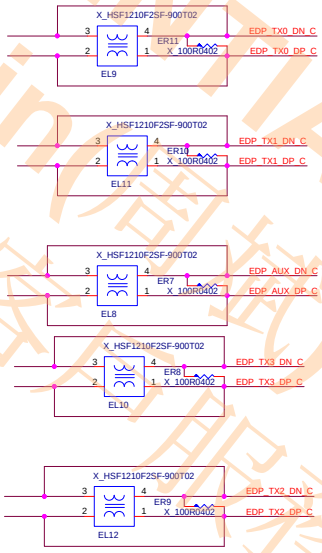








EMI
CLOSE TO CON5



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	EDP Pannel/Camera/TP	
Size: Custom	Document Number: MS-14C1	Rev: 0A
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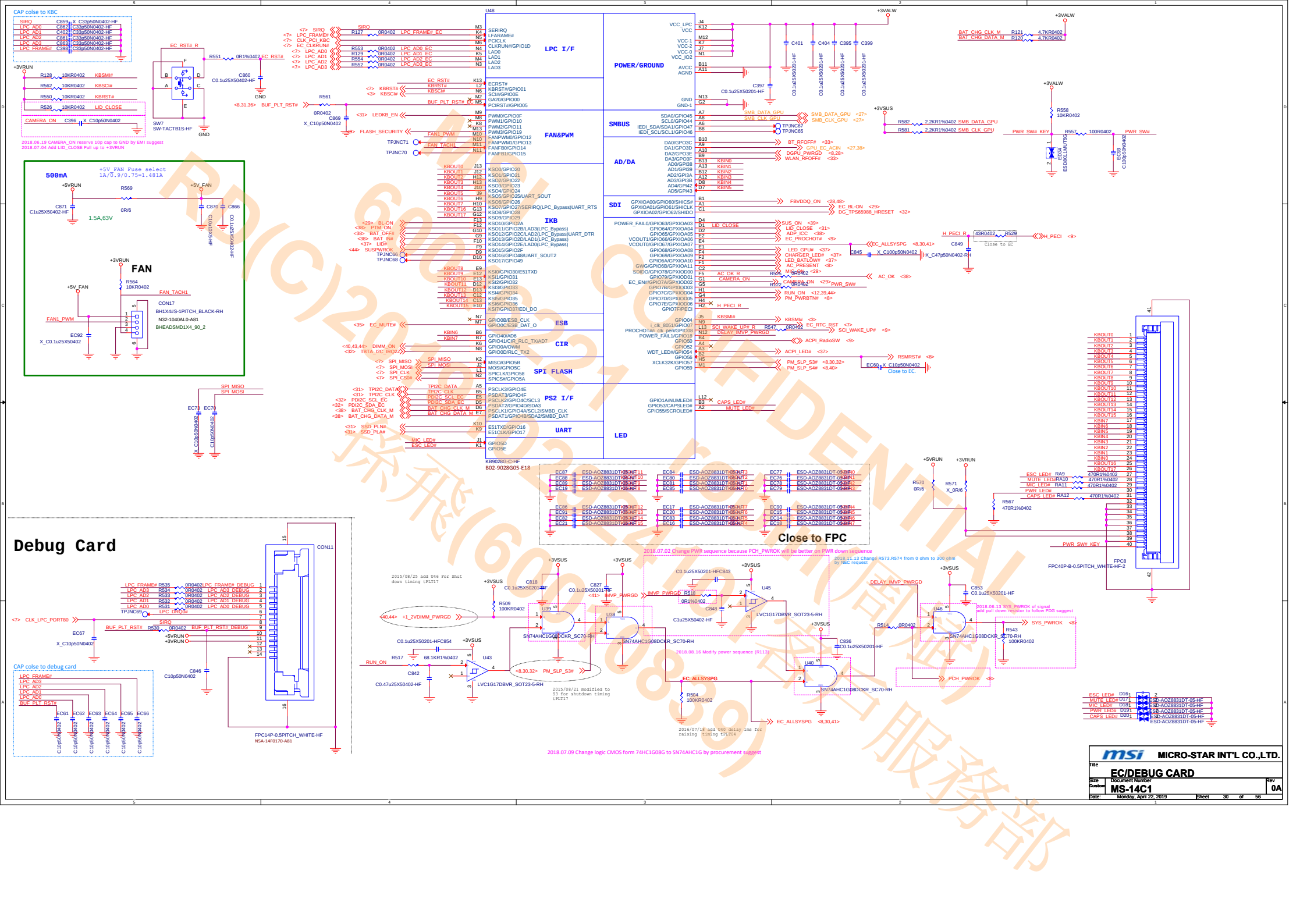
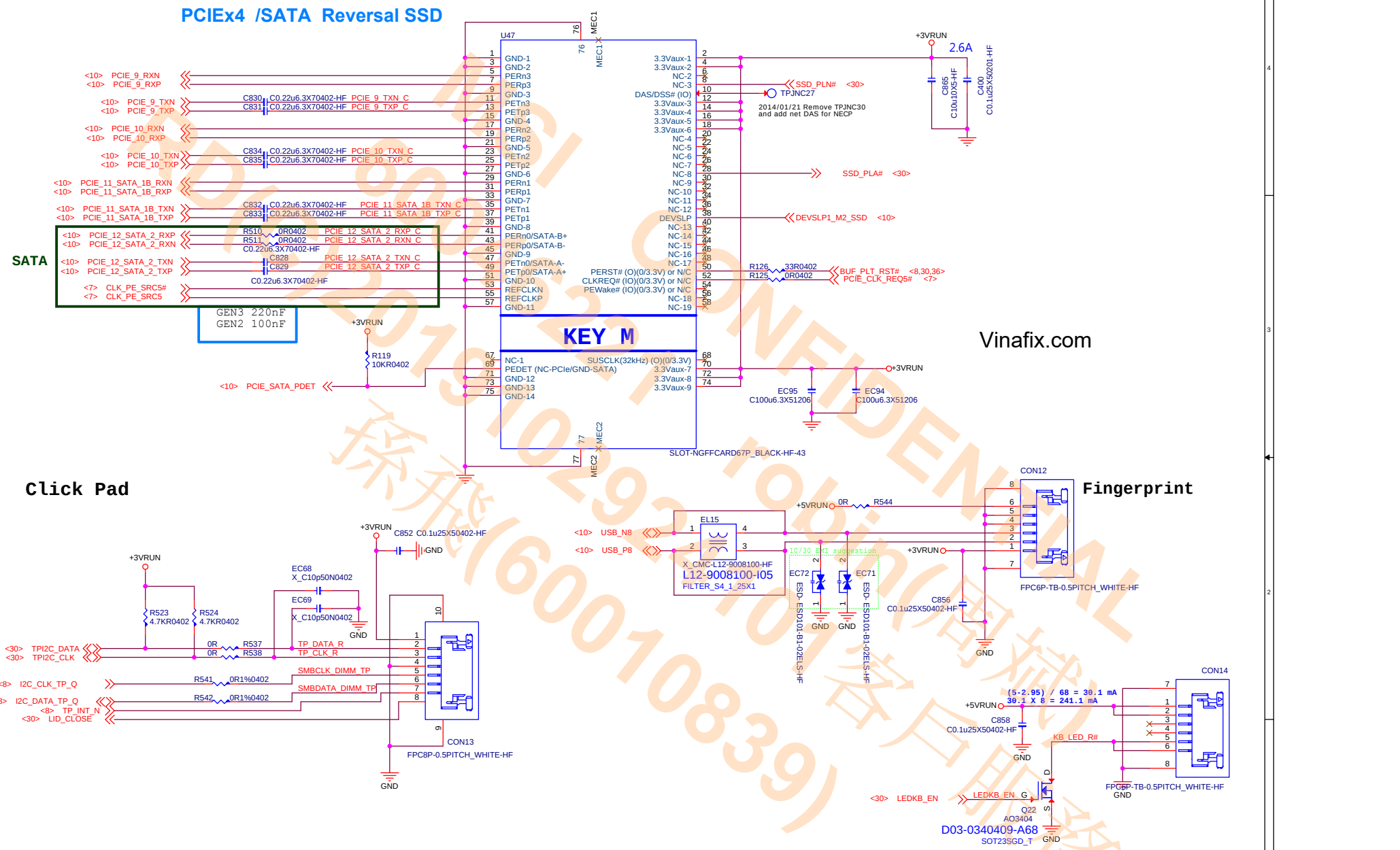
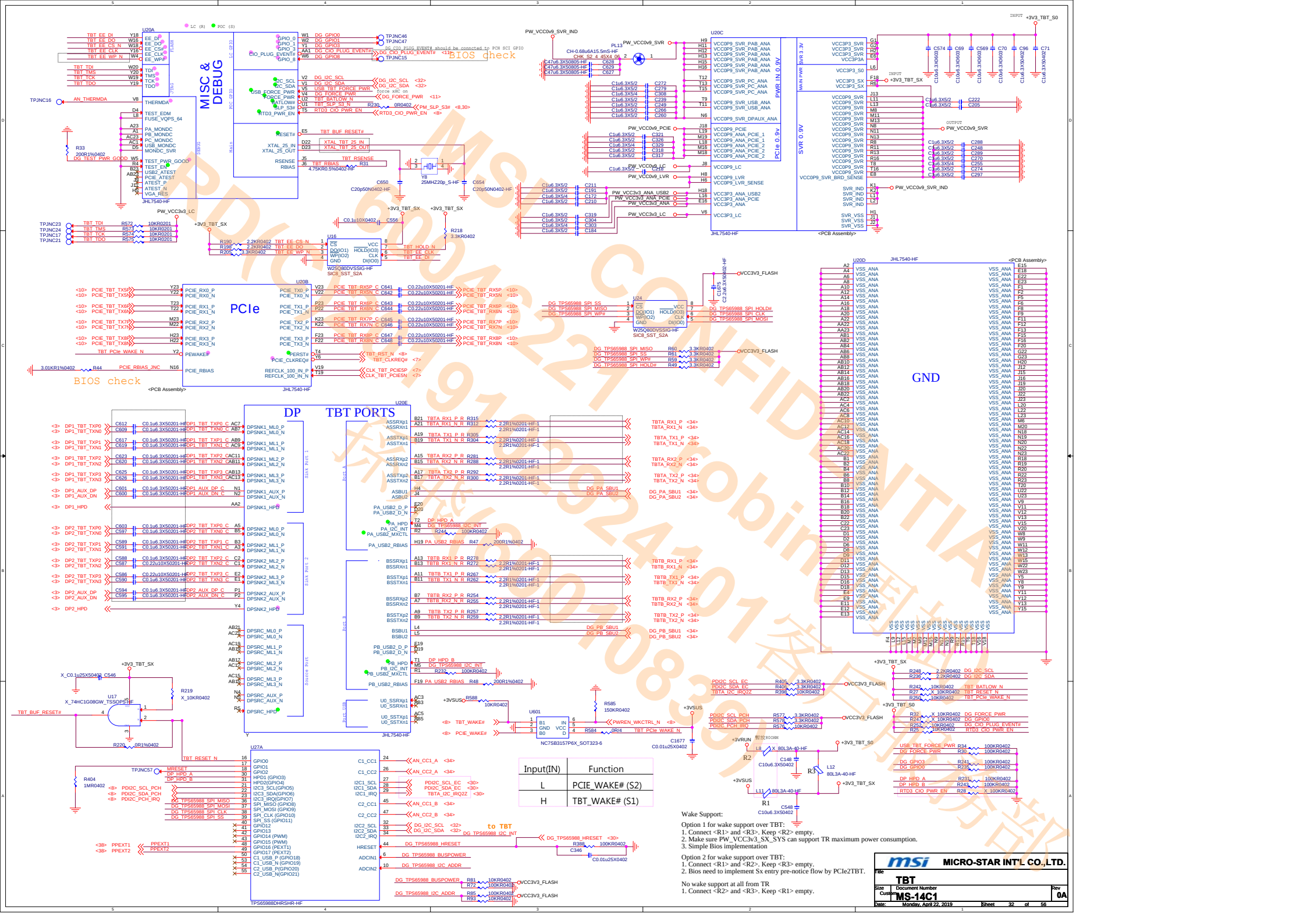

CAP colse to KBC
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
FAN
500mA
Debug Card
CAP colse to debug card
Close to FPC
MICRO-STAR INT'L CO.,LTD.
EC/DEBUG CARD
MS-14C1
Monday, April 22, 2019


PCIEx4 /SATA Reversal SSD
U47
MEC1
SATA
GEN3 220nF
GEN2 100nF
KEY M
SLOT-NGFFCARD67P_BLACK-HF-43
Vinafix.com
Click Pad
Fingerprint
CON12
FPC6P-TB-0.5PITCH_WHITE-HF
CON13
FPC8P-0.5PITCH_WHITE-HF
CON14
FPC6P-TB-0.5PITCH_WHITE-HF
D03-0340409-A68
SOT23SGD_T
MICRO-STAR INT'L CO.,LTD.
EDP Pannel/Camera/TP
MS-14C1
Monday, April 22, 2019


MISC & DEBUG
BIOS check
PCIe
DP TBT PORTS
GND
JHL7540-HF
<PCB Assembly>
to TBT
Input(IN) | Function
L | PCIE_WAKE# (S2)
H | TBT_WAKE# (S1)
Wake Support:
Option 1 for wake support over TBT:
1. Connect <R1> and <R3>. Keep <R2> empty.
2. Make sure PW_VCC3v3_SX_SYS can support TR maximum power consumption.
3. Simple Bios implementation
Option 2 for wake support over TBT:
1. Connect <R1> and <R2>, Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.
No wake support at all from TR
1. Connect <R2> and <R3>. Keep <R1> empty.
MICRO-STAR INT'L CO.,LTD.
Title: TBT
Size: Custom
Document Number: MS-14C1
Rev: 0A
Date: Monday, April 22, 2019
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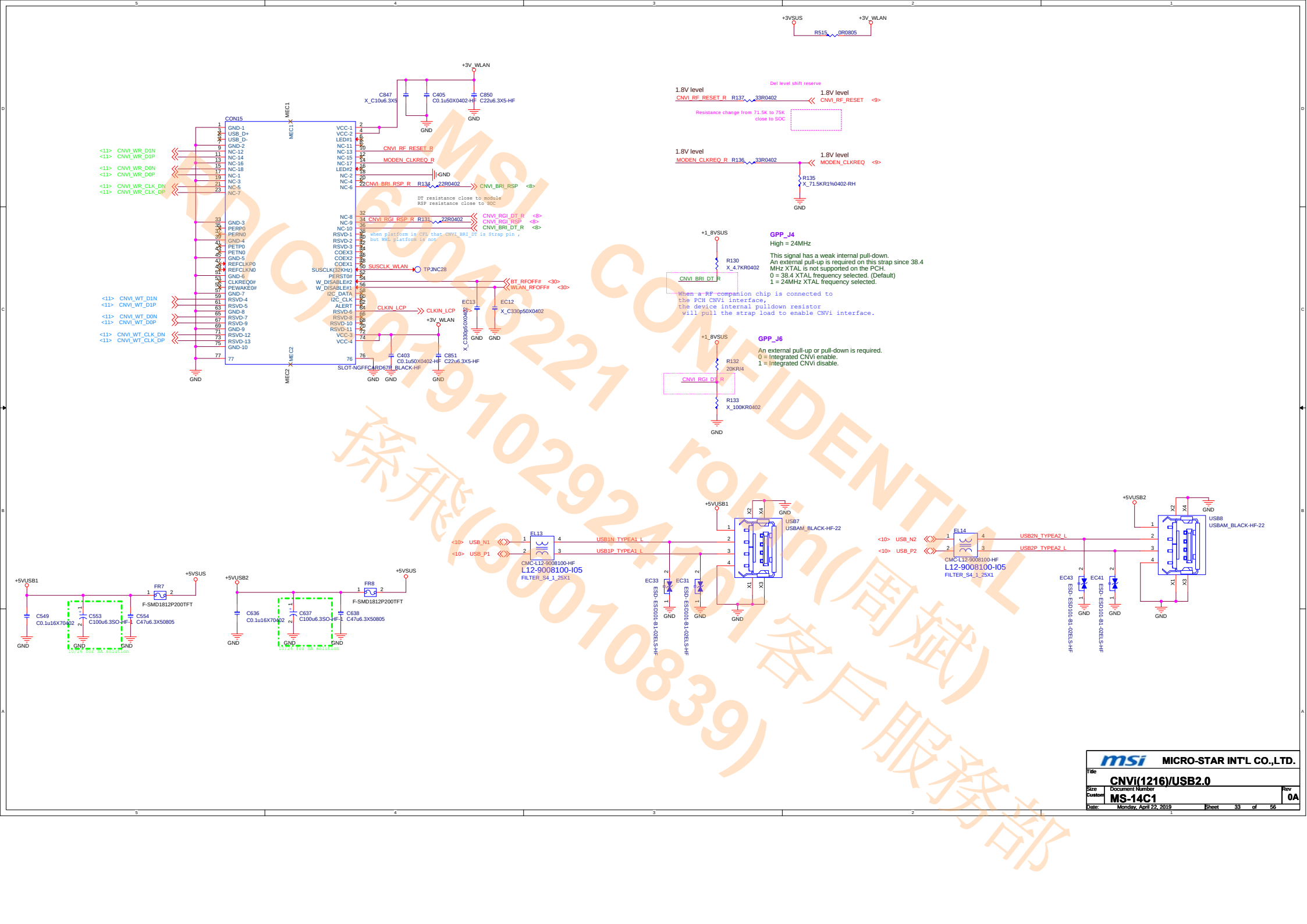
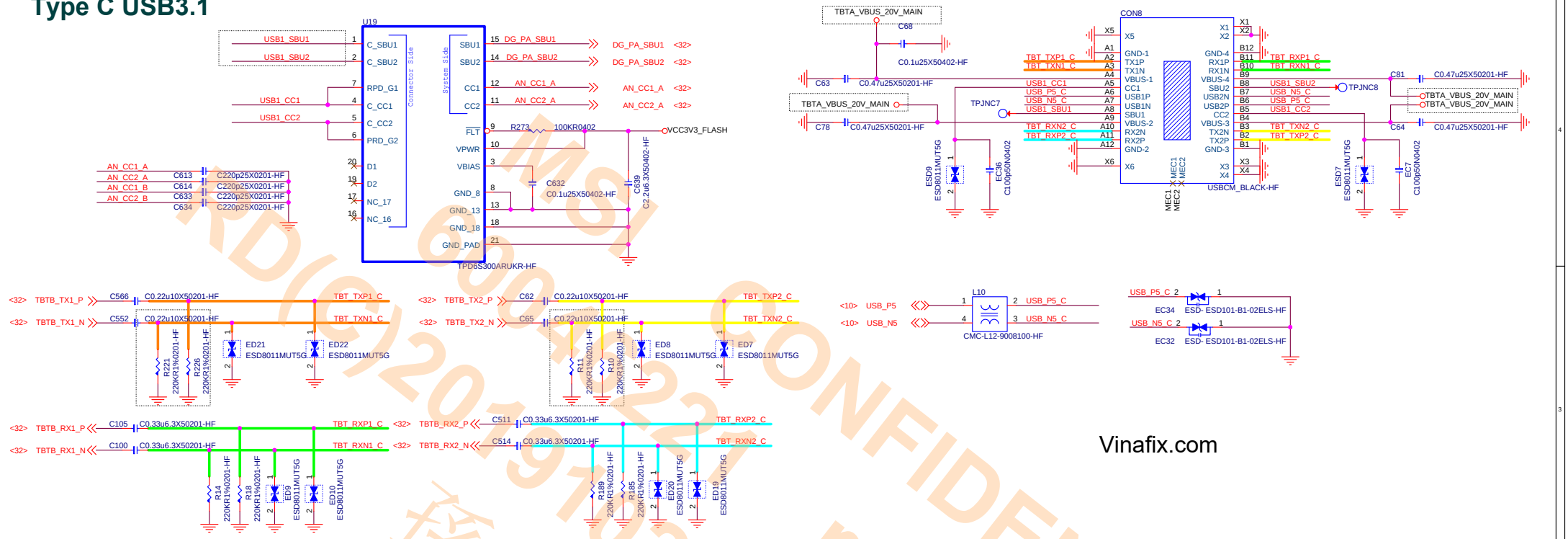


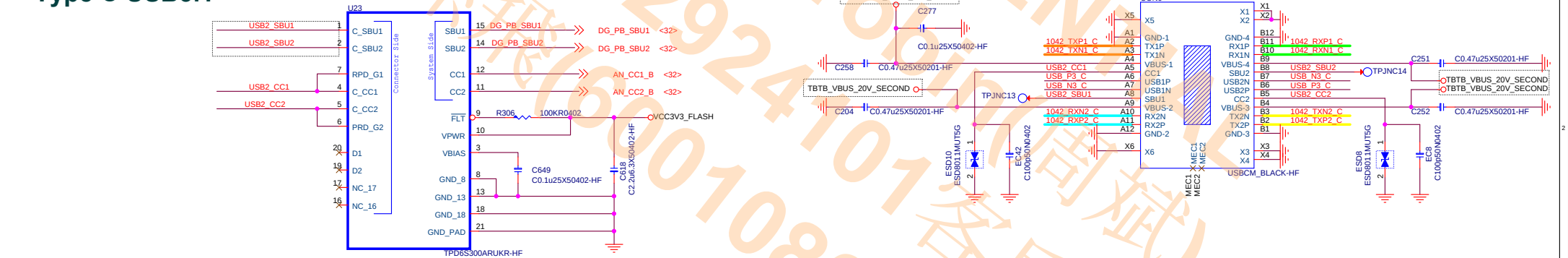
msi	MICRO-STAR INT'L CO.,LTD.	
Title	CNVi(1216)/USB2.0	
Size: Custom	Document Number: MS-14C1	Rev: 0A
Date: Monday, April 22, 2019	Sheet 33 of 56	

Type C USB3.1



Vinafix.com

Type C USB3.1



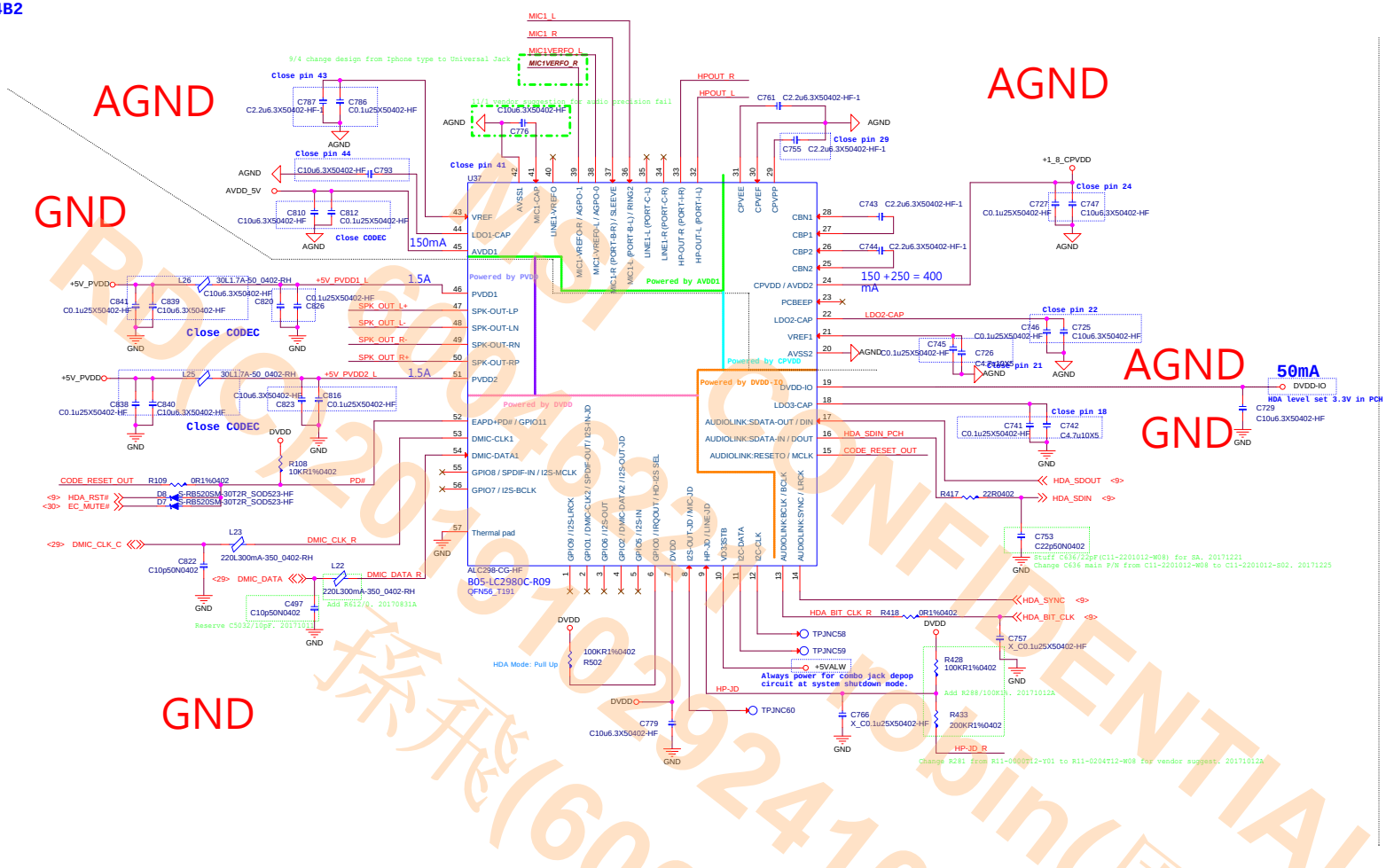
MICRO-STAR INT'L CO.,LTD.

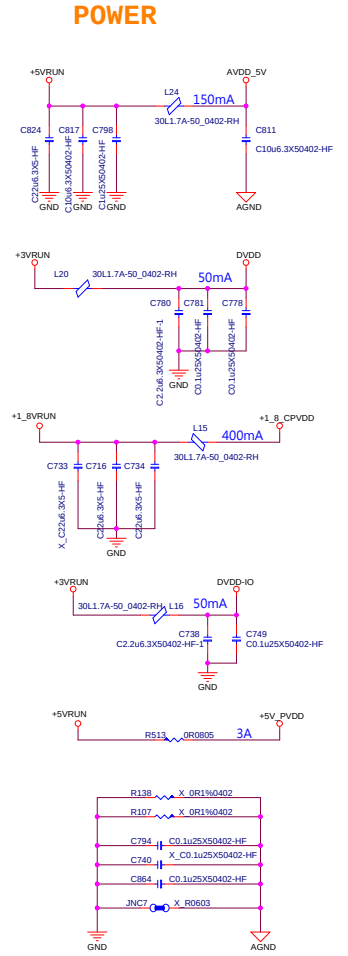
Title: USB3.1 GEN2

Size: Custom | Document Number: MS-14C1 | Rev: 0A

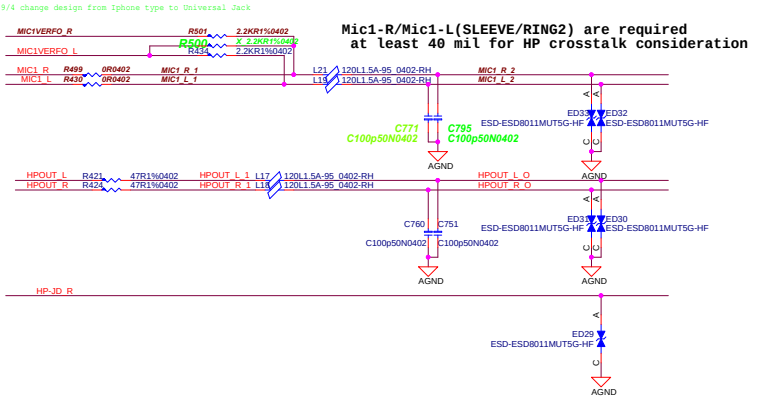
Date: Monday, April 22, 2019 | Sheet 34 of 56

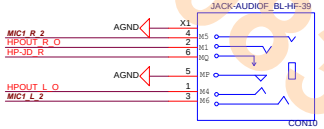
Reference 14B2

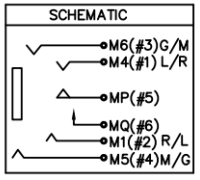




Universal Jack

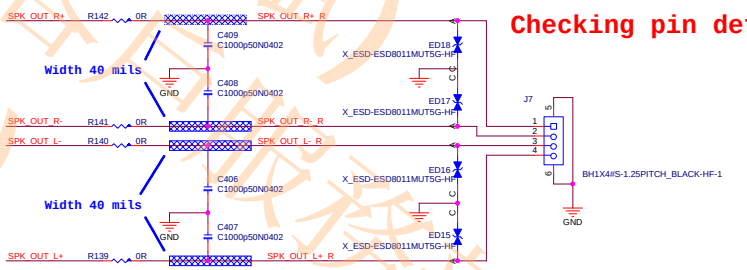






SPEAKER

1.SPK L+ L- R+ R- trace width: Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
2.If you mount the LC filter((L1~L4;C4/C11;C2/C7/C10/C13),Please let them together and close to codec.
3.Please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
4.If L1,L2,L3,L4 are replaced by 0 ohm/1.6A resistetor(please don't use general bead, because it may influence the THD+N quality),and C4,C11 should be NC



Checking pin define

MICRO-STAR INT'L CO.,LTD.		
Title: Audio (ALC298-CG), JACK		
Size: Custom	Document Number: MS-14C1	Rev: 0A
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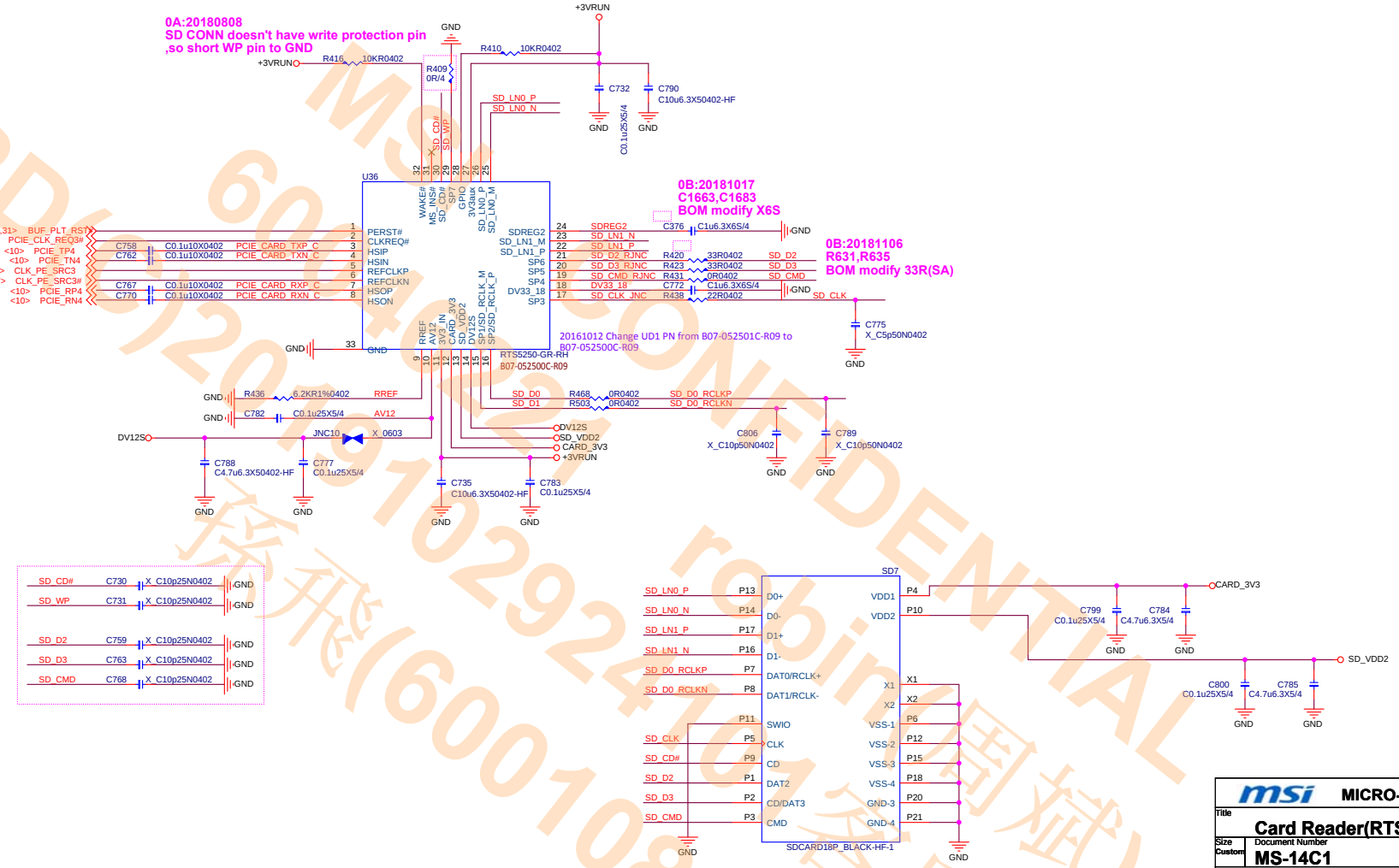
CardReader (RTS5250)



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Card Reader(RTS5250)		
Size: Custom	Document Number: MS-14C1		Rev: 0A
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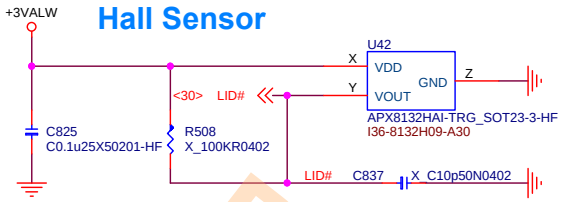
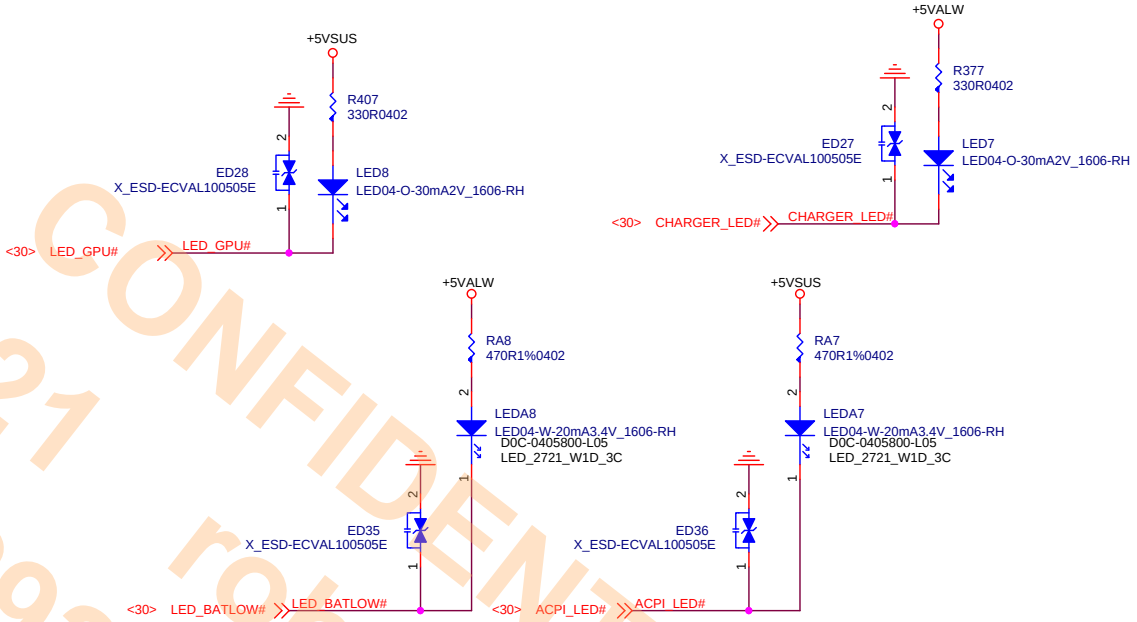
2018.06.20 Change hall sensor IC from AH1887 (2 output) to AH1810 (1 output)
2018.06.15 Add Hall sensor function on board (AH1887)

Hall Sensor

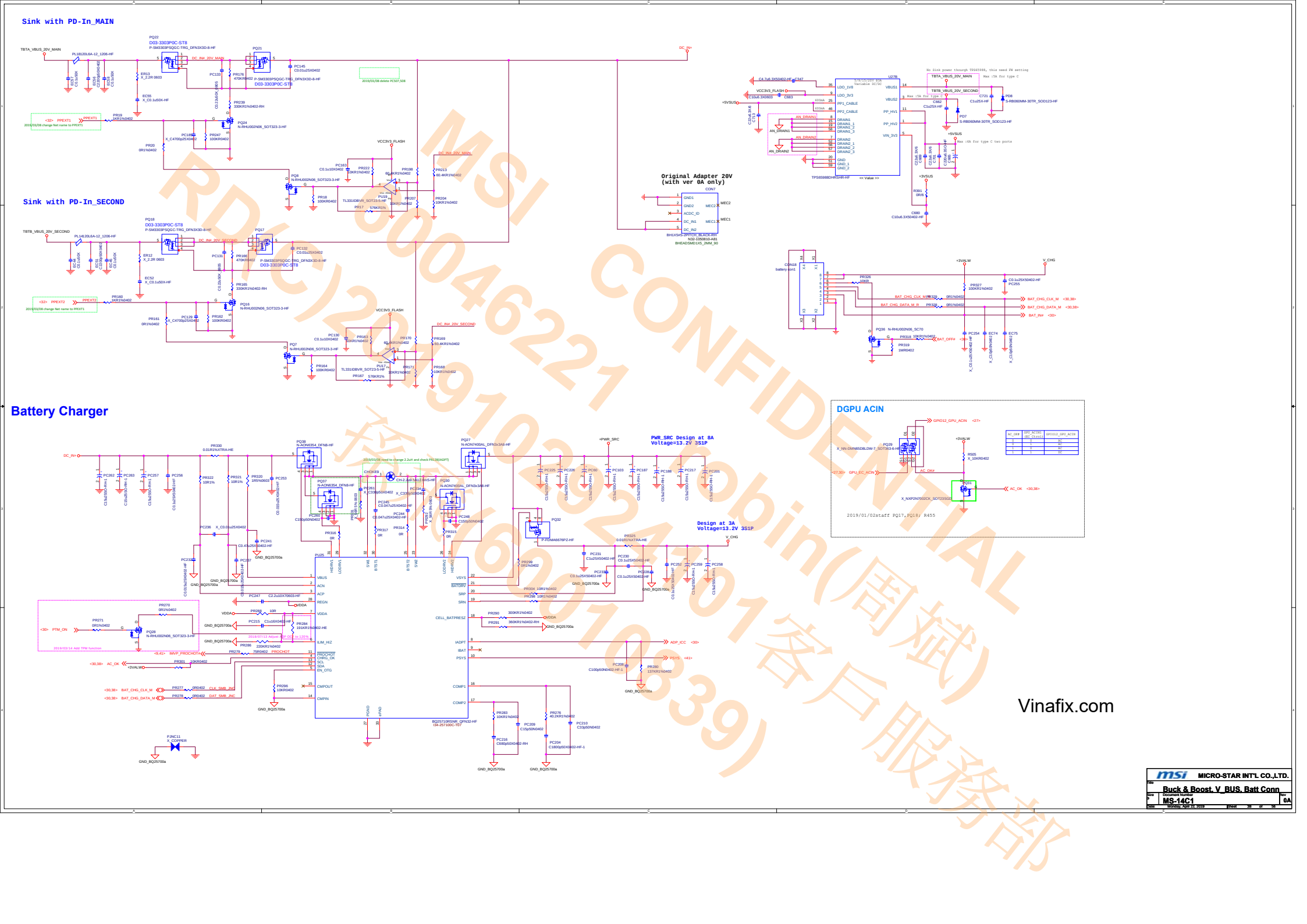


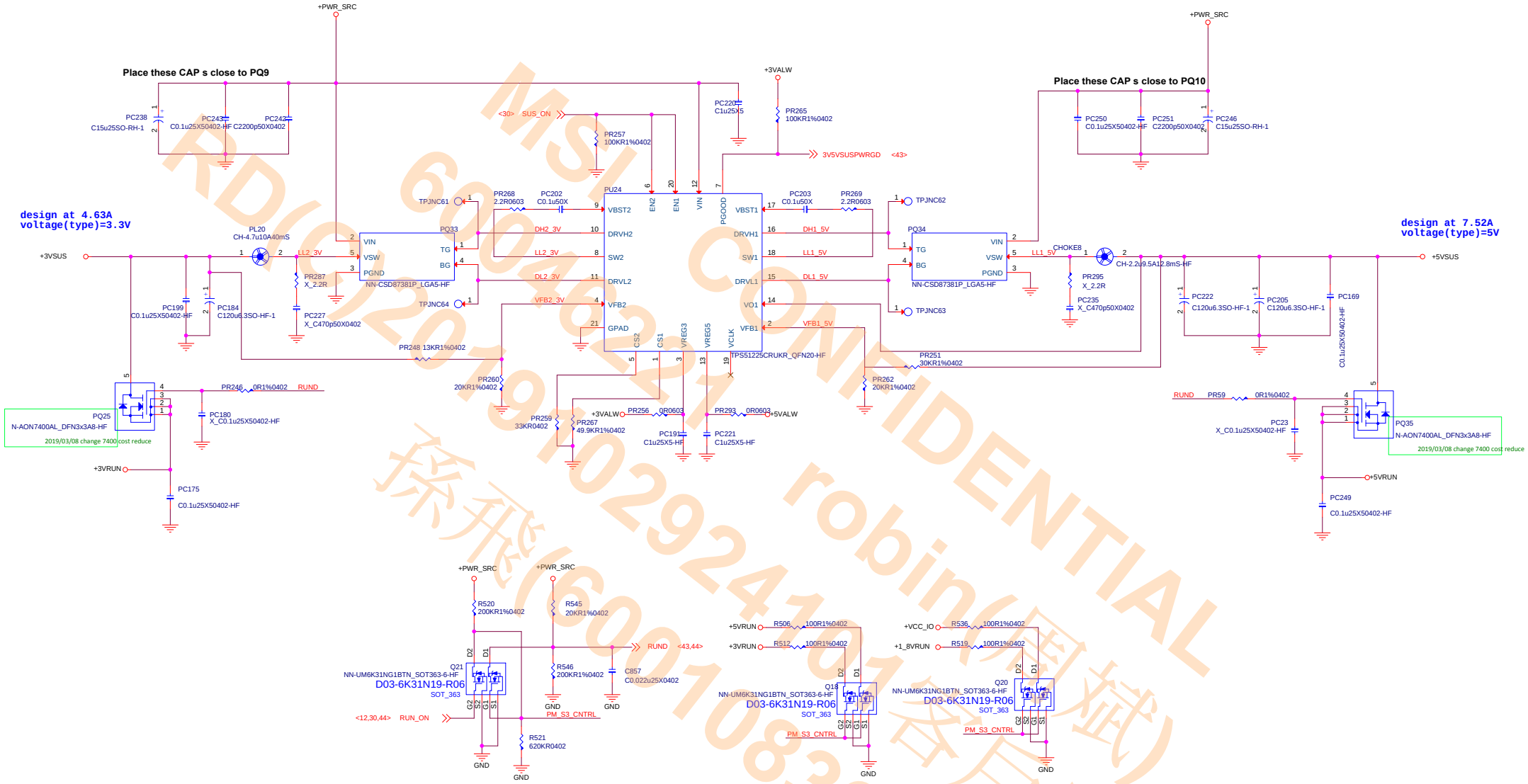
2018.06.26 Change hall sensor IC from AH1810 to APX8132 by ME suggest

LED

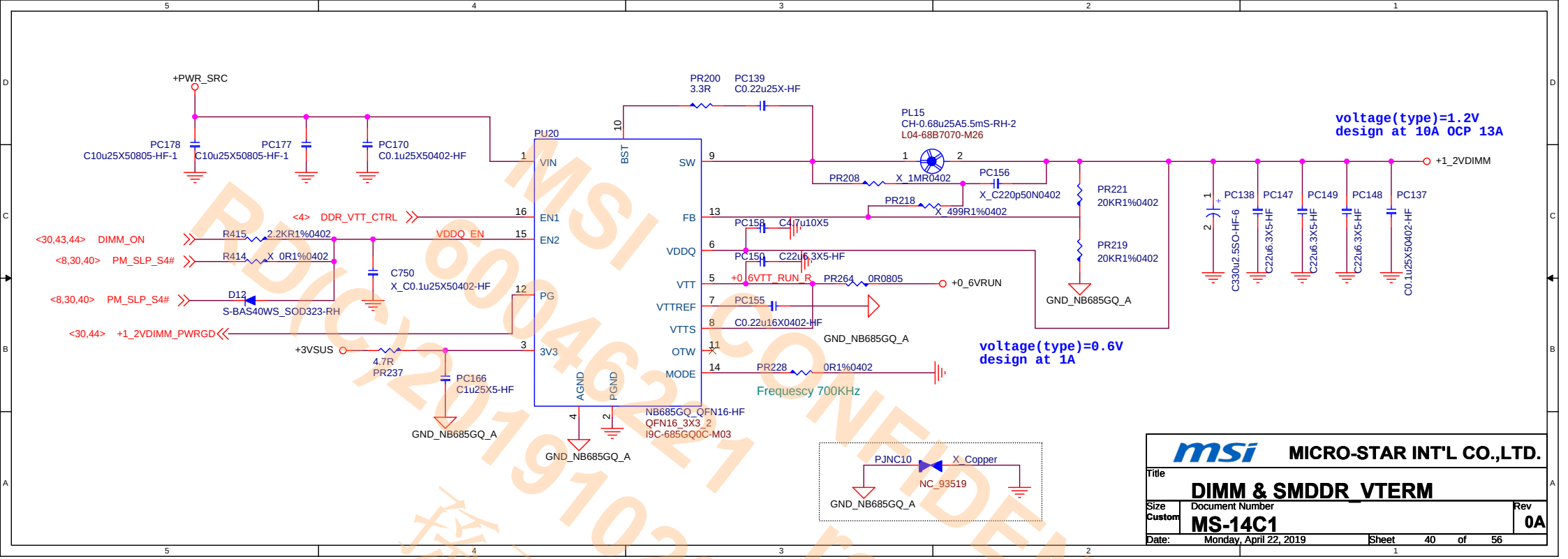


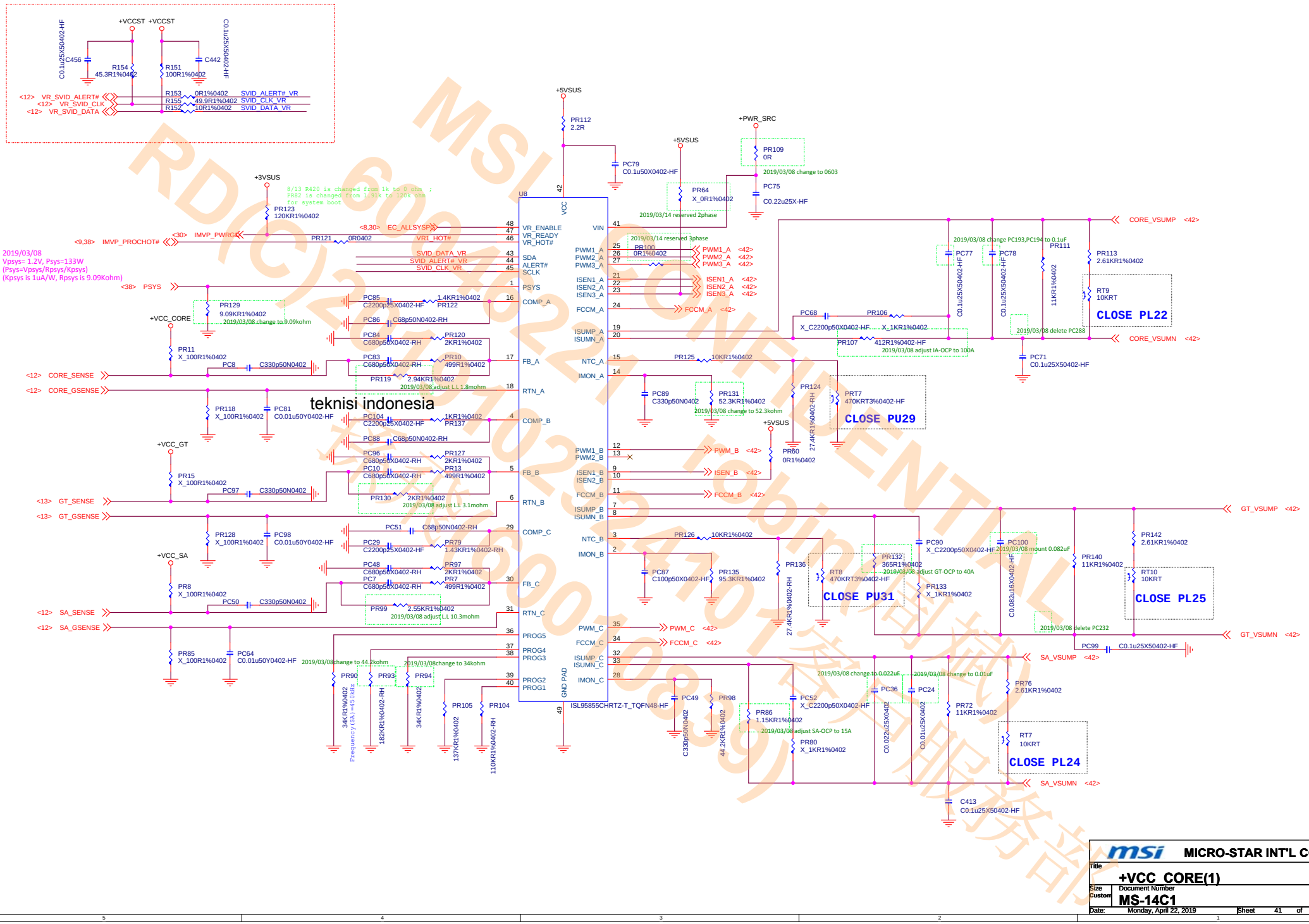
MICRO-STAR INT'L CO.,LTD.		
Title: PWR SW/FP/LED/LID		
Size: Custom	Document Number: MS-14C1	Rev: 0A
Date: Monday, April 22, 2019	Sheet 37 of 56	





MICRO-STAR INT'L CO.,LTD.			
Title: System Power			
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 39 of 56		





msi MICRO-STAR INT'L CO.,LTD.			
Title: +VCC_CORE(1)			
Size: Custom	Document Number: MS-14C1		Rev: 0A
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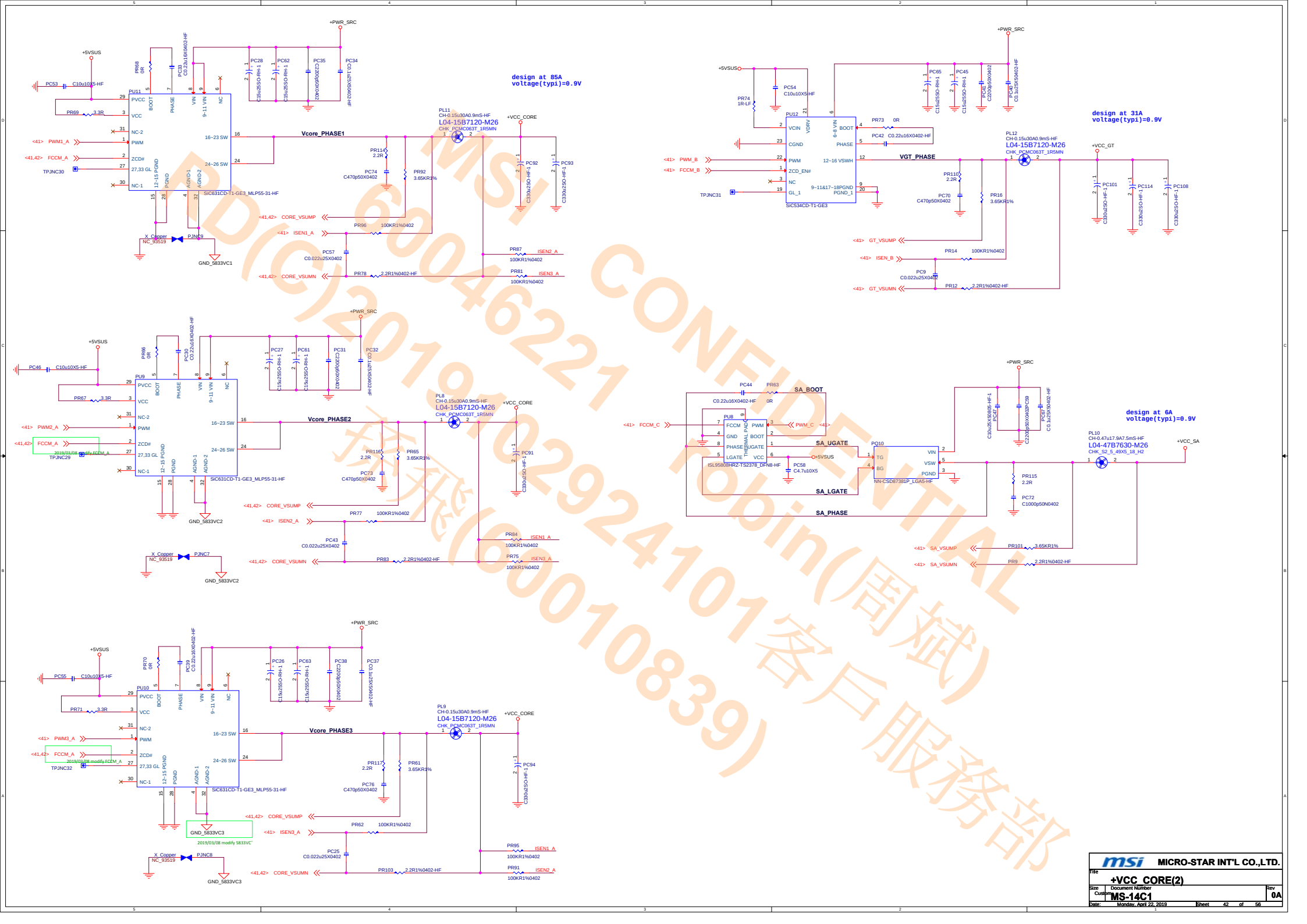

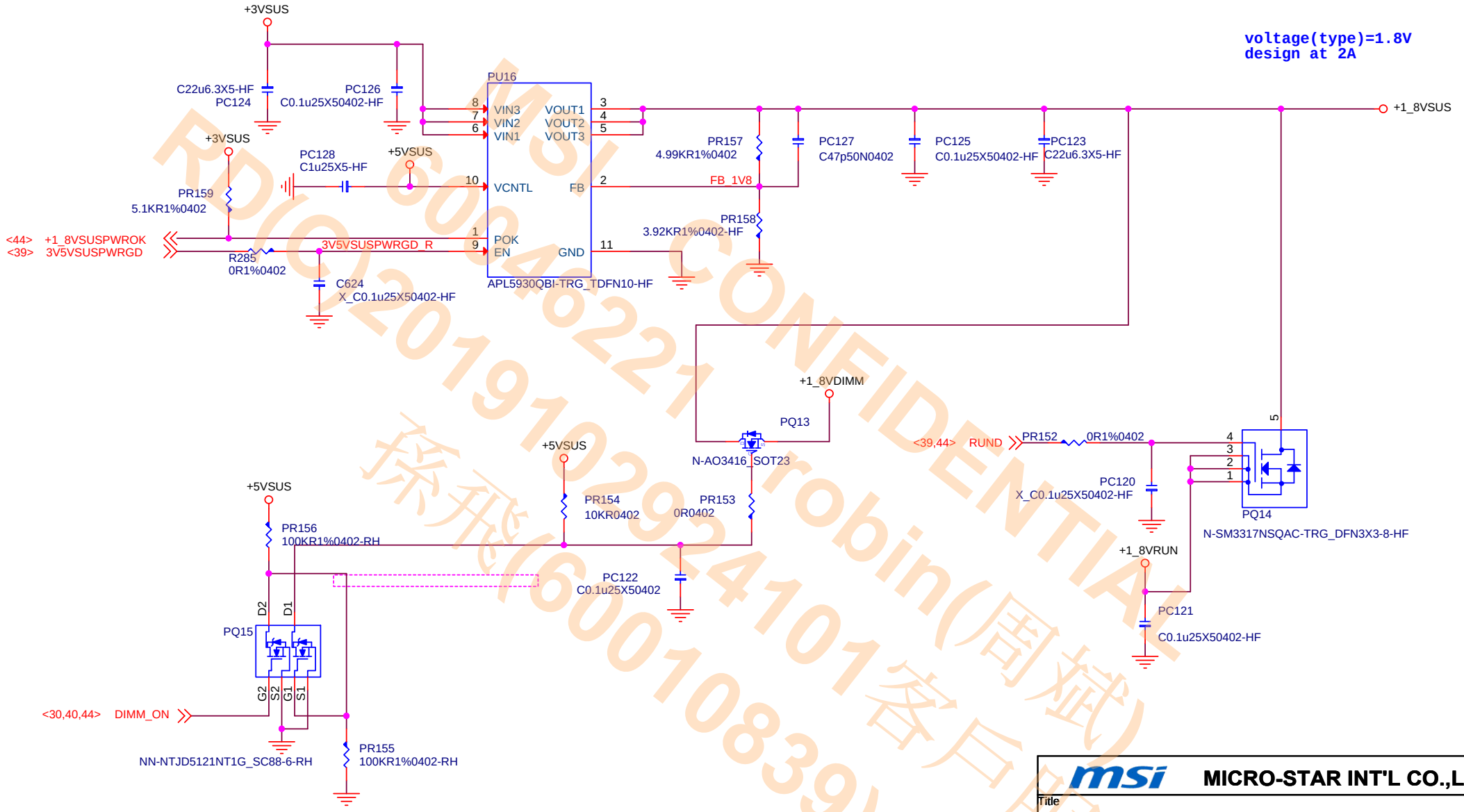

MICRO-STAR INT'L CO.,LTD.

Title: 2V5 & 1.8VSUS

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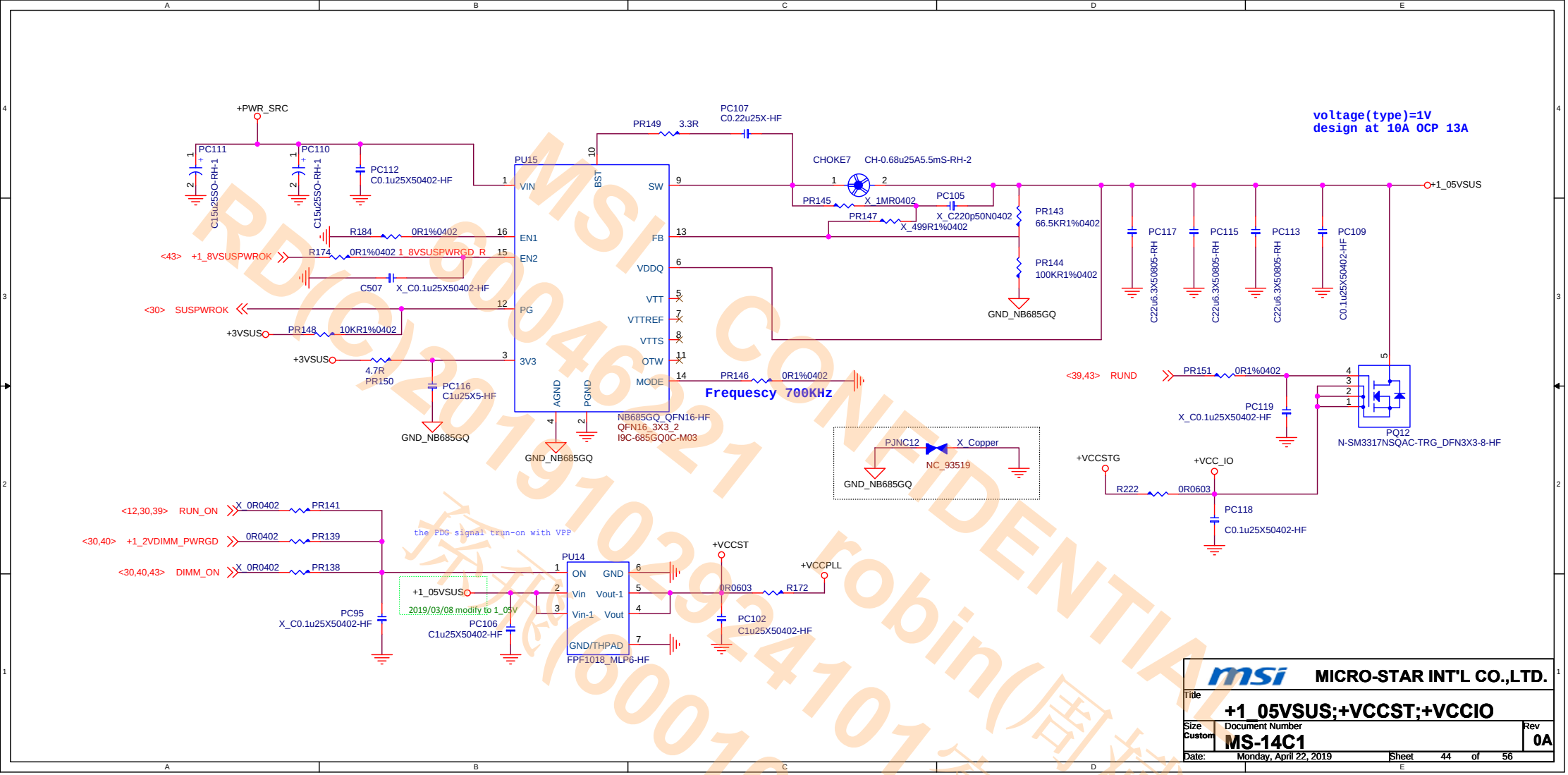
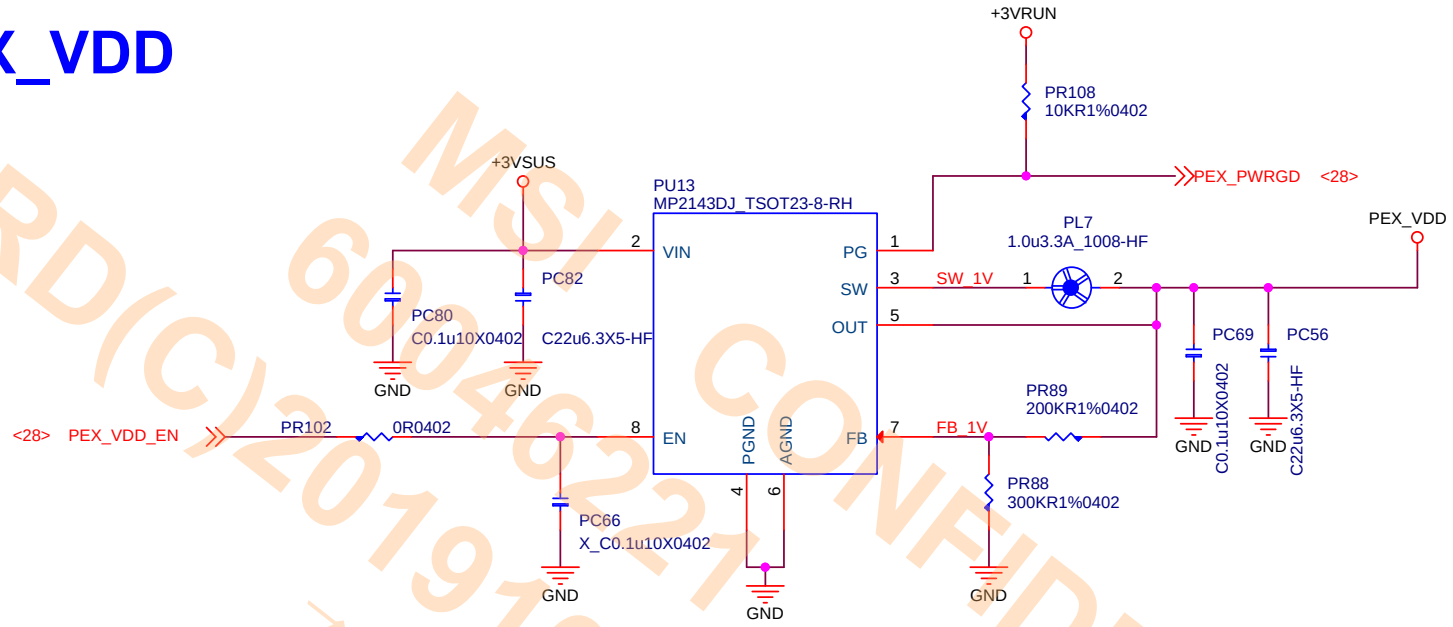
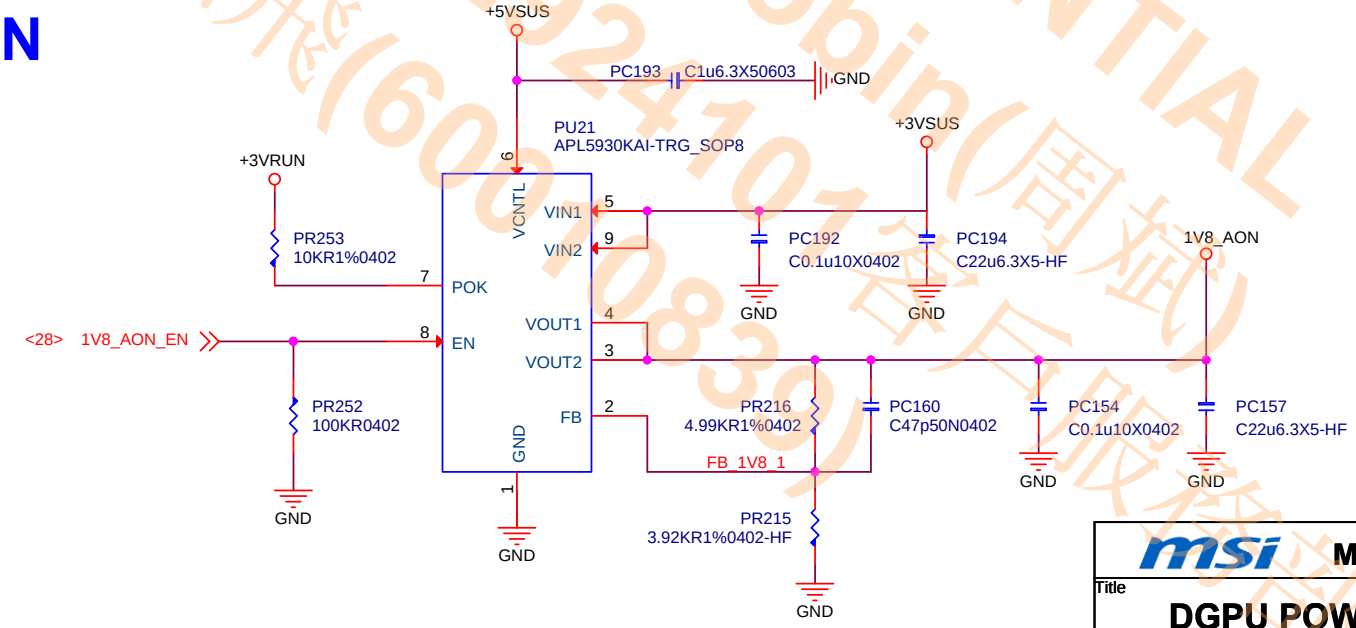


PEX_VDD



PEX_VDD
Voltage = 1.0V
Current = 1.6A
OCP(typi) = 4.8A

1V8_AON



1V8_AON
Voltage = 1.8V
Current = 2.3A

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Title: DGPU POWER PEX_VDD/1V8_AON

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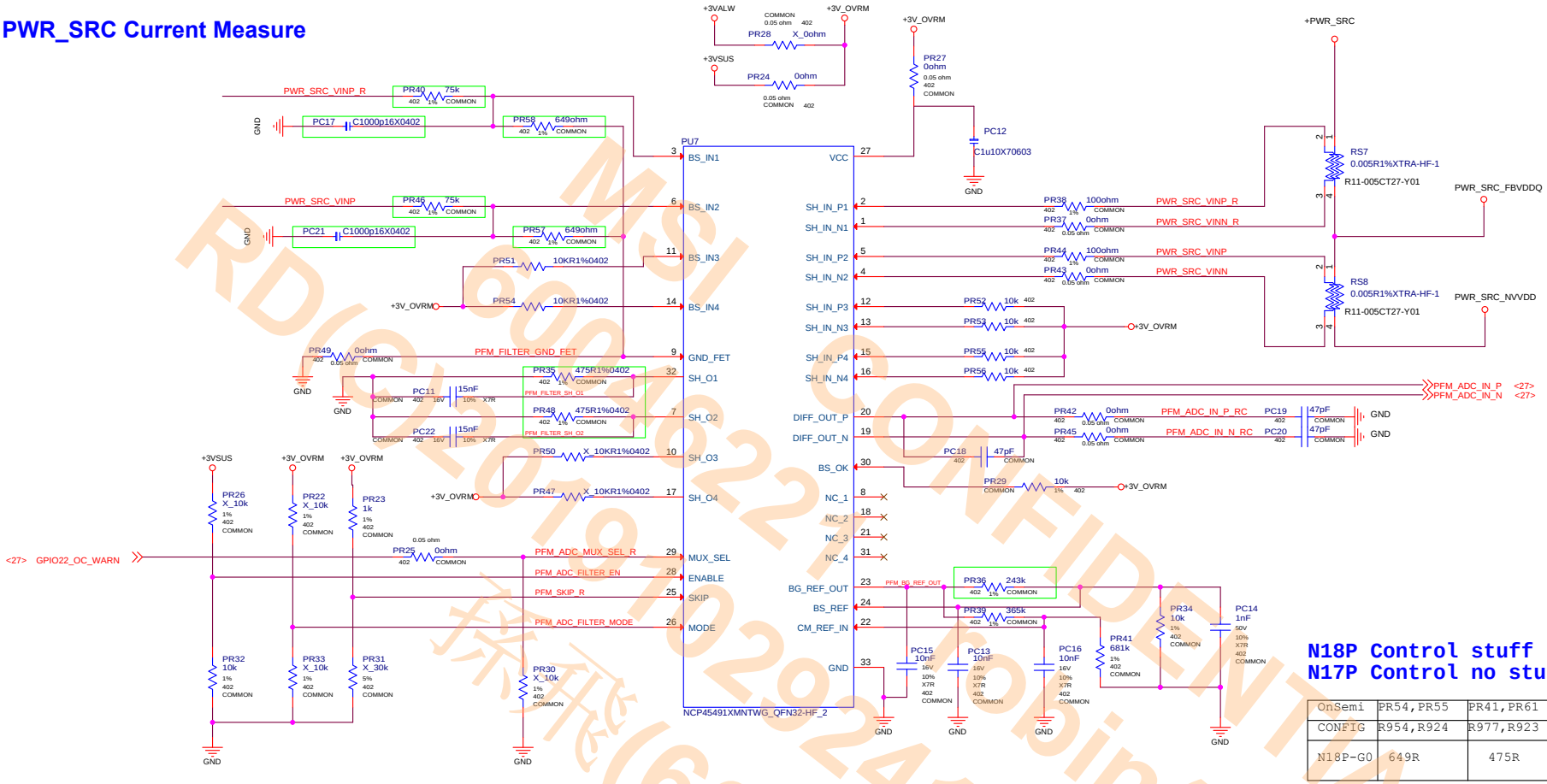
PWR_SRC Current Measure



N18P Control stuff
N17P Control no stuff **RS3,RS4**

OnSemi	PR54,PR55	PR41,PR61	PR43	PR45,PR51	PC21,PC26
CONFIG	R954,R924	R977,R923	R950	R953,R952	C841,C836
N18P-G0	649R	475R	243K	75K	1.0nF

	MICRO-STAR INT'L CO.,LTD.
Title	DGPU POWER MONITORING
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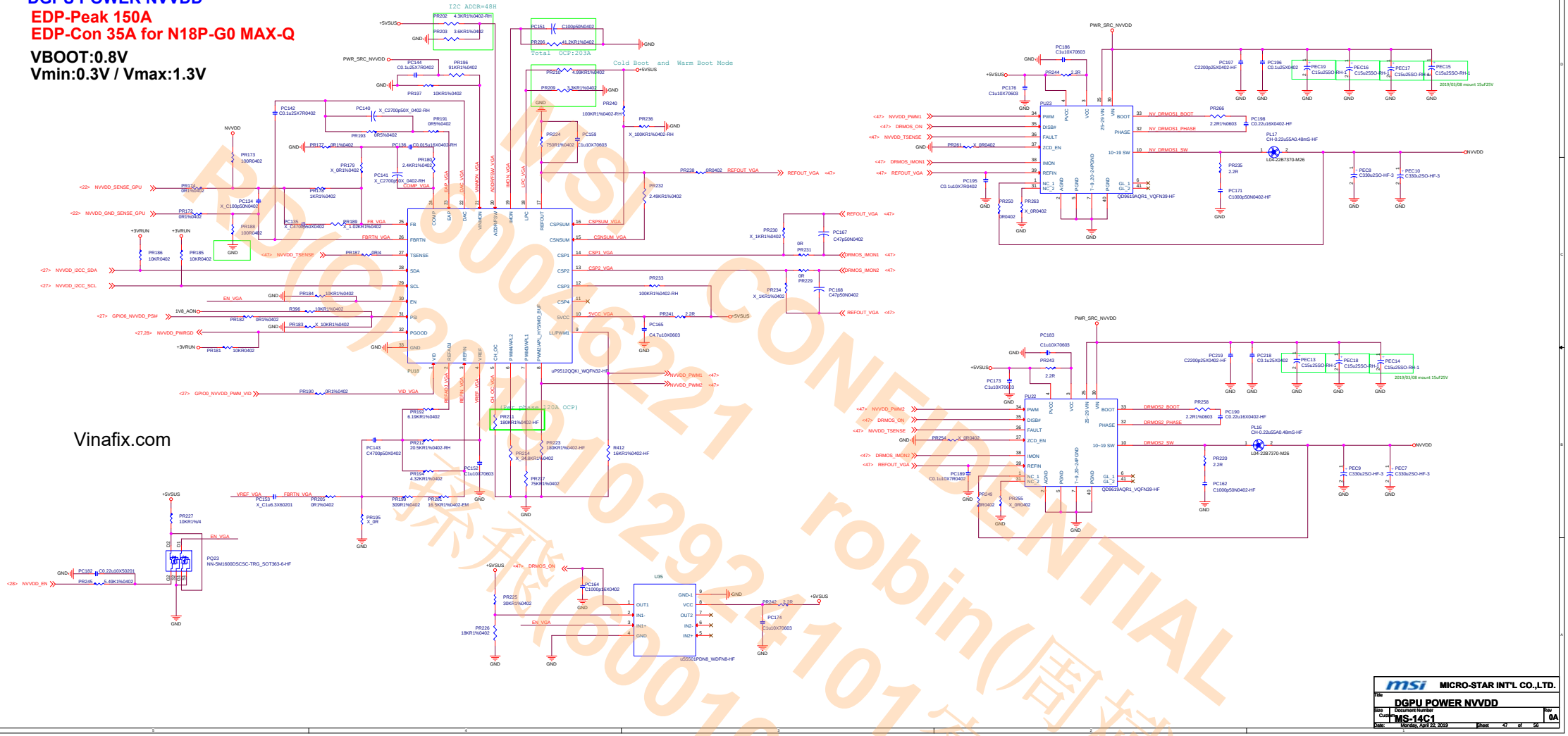
DGPU POWER NVVDD

EDP-Peak 150A
EDP-Con 35A for N18P-G0 MAX-Q

VBOOT:0.8V
Vmin:0.3V / Vmax:1.3V

Vinafix.com



msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU POWER NVVDD		
Size	Document Number		Rev
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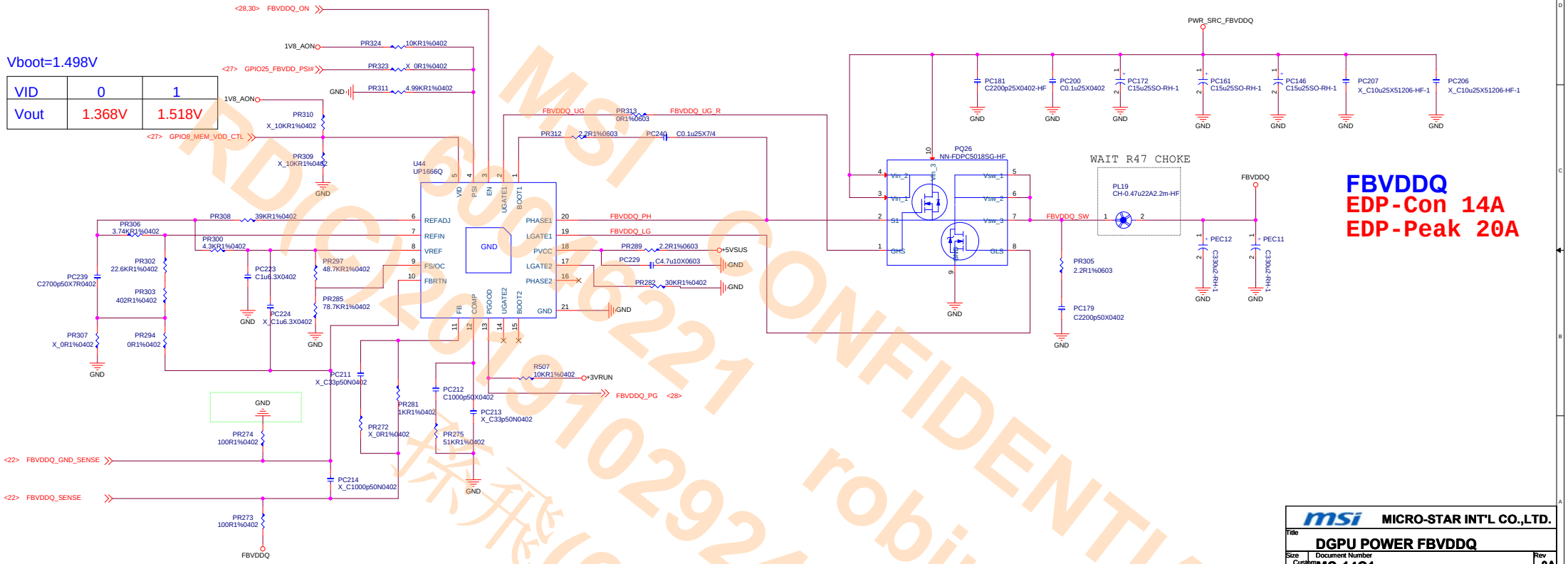
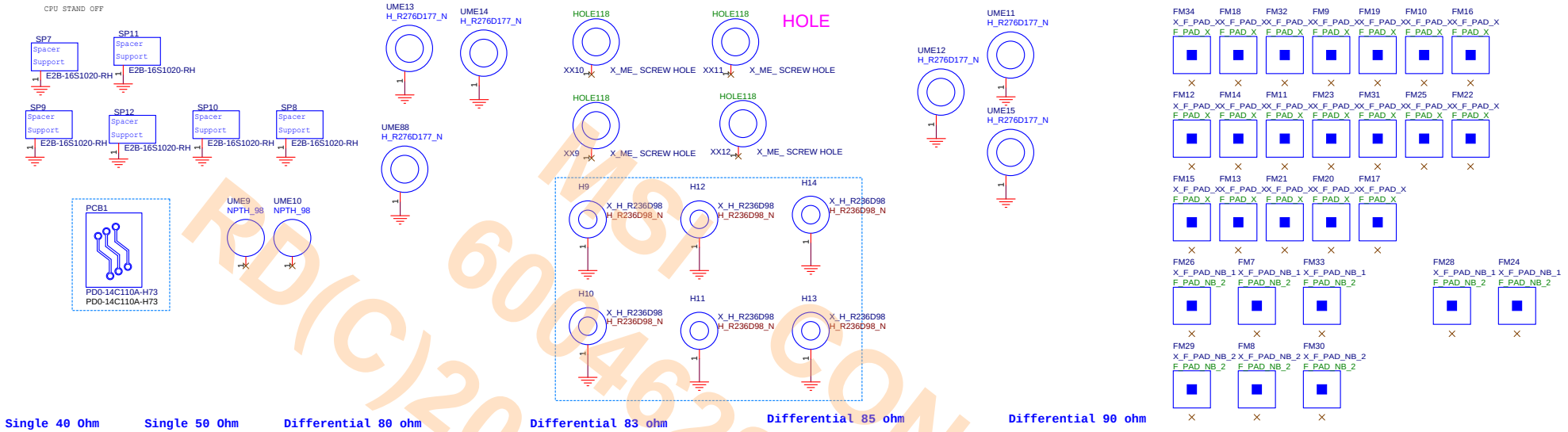
FBVDDQ

Vboot=1.498V

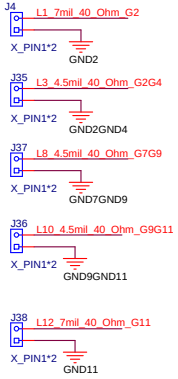
VID	0	1
Vout	1.368V	1.518V



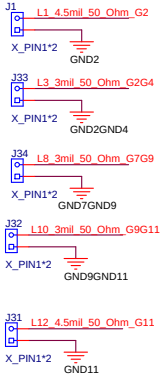
msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU POWER FBVDDQ		
Size: Custom	Document Number: MS-14C1		Rev: 0A
Date: Monday, April 22, 2019	Sheet 48 of 56		



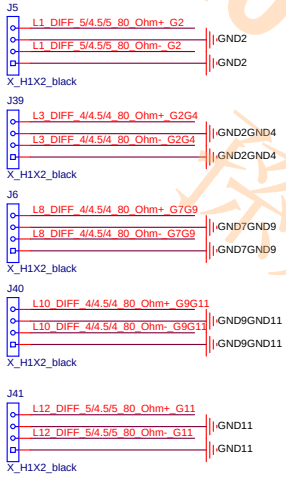
Single 40 Ohm



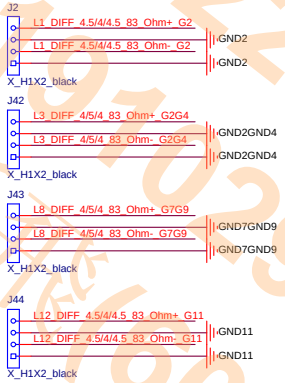
Single 50 Ohm



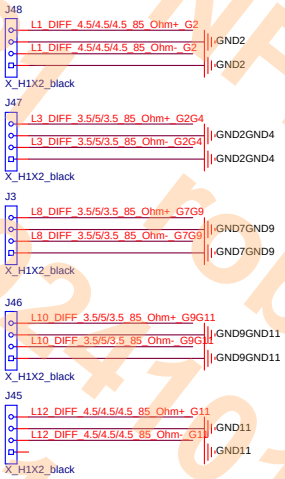
Differential 80 ohm



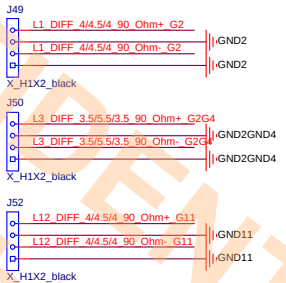
Differential 83 ohm



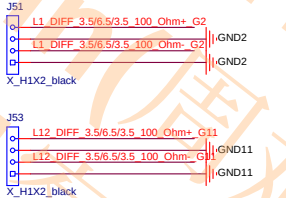
Differential 85 ohm



Differential 90 ohm



Differential 100 ohm



MICRO-STAR INT'L CO.,LTD.		
Title: ME		
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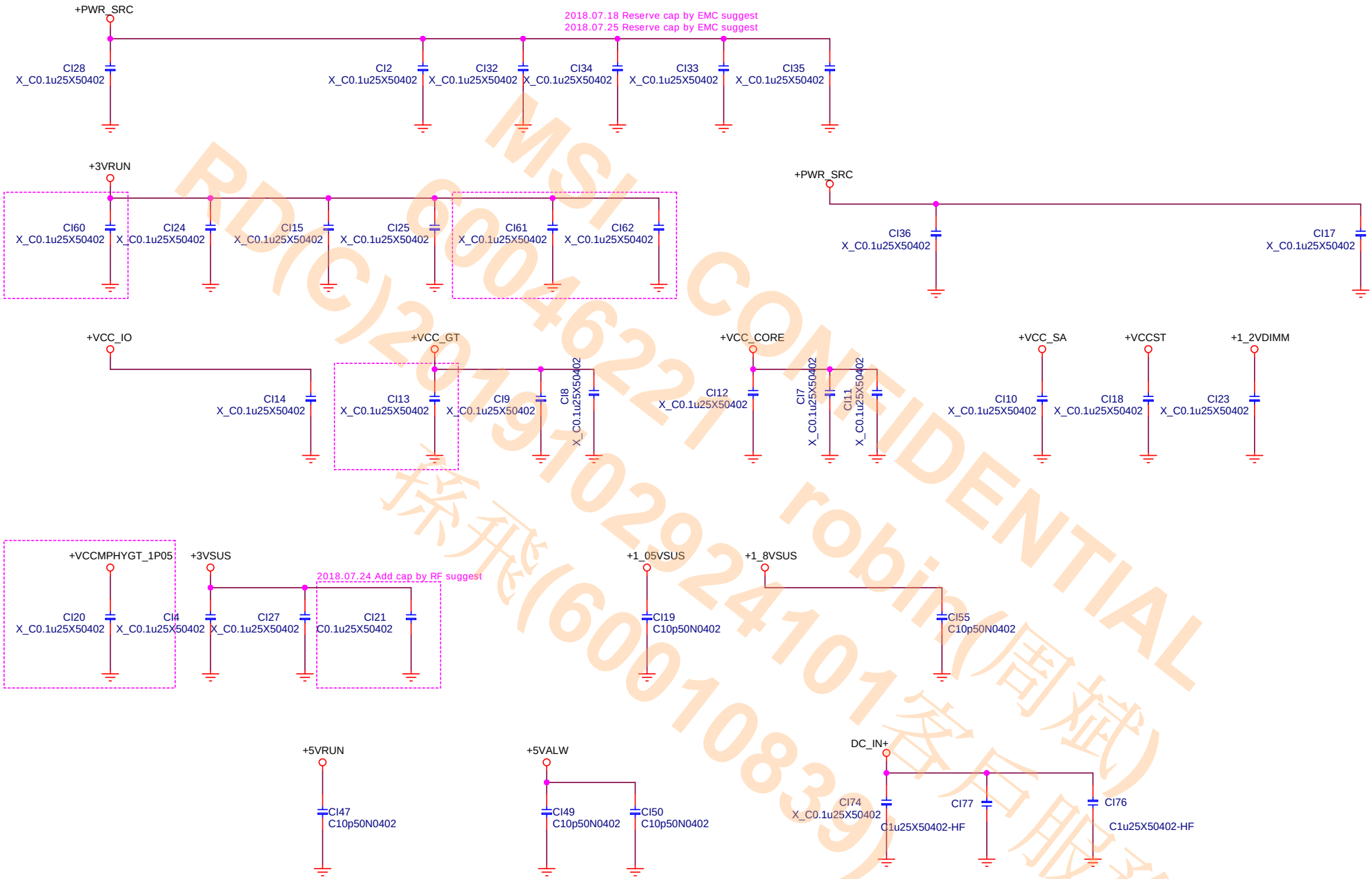

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Title: EMI List

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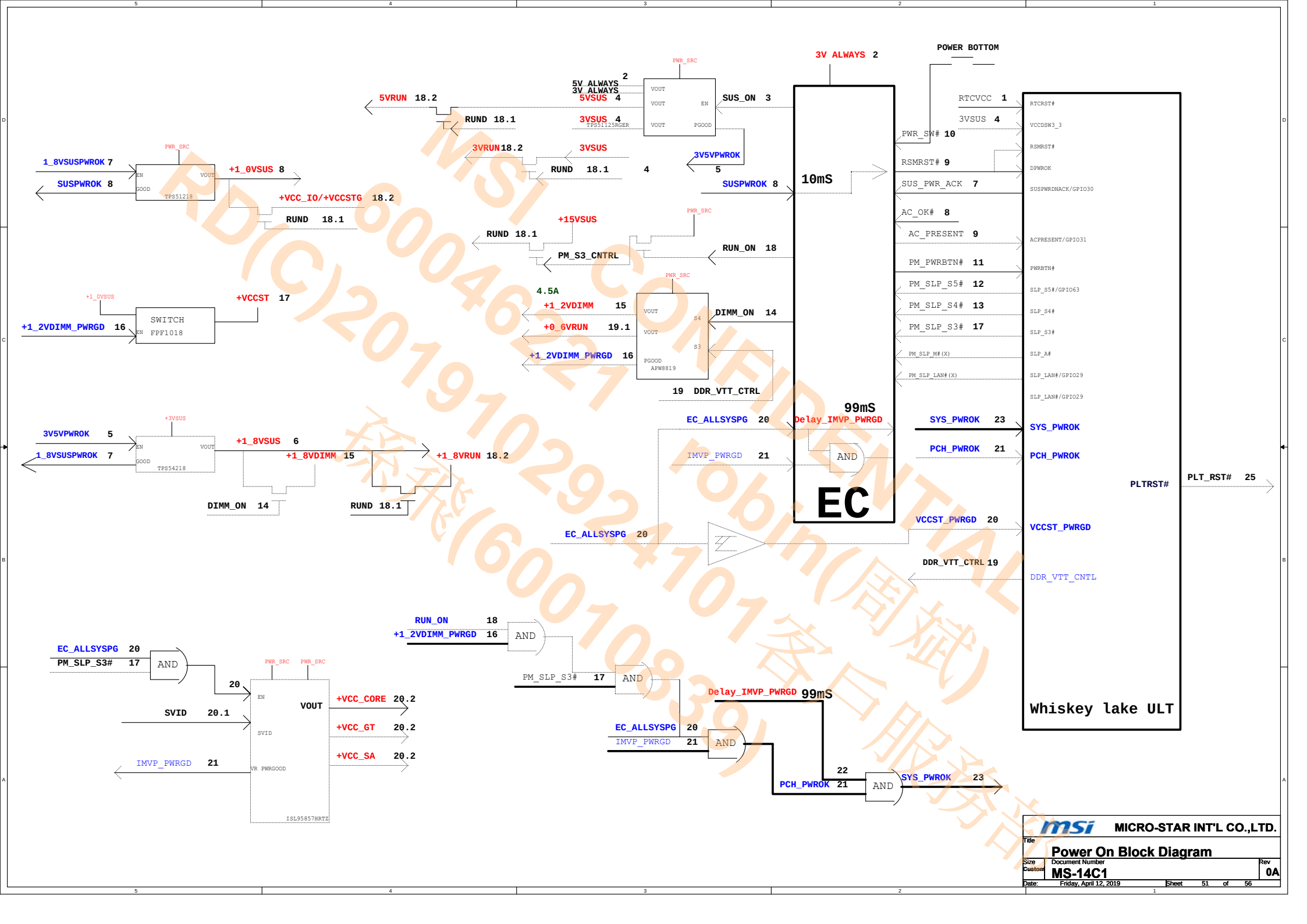

MICRO-STAR INT'L CO.,LTD.

Title: Power On Block Diagram

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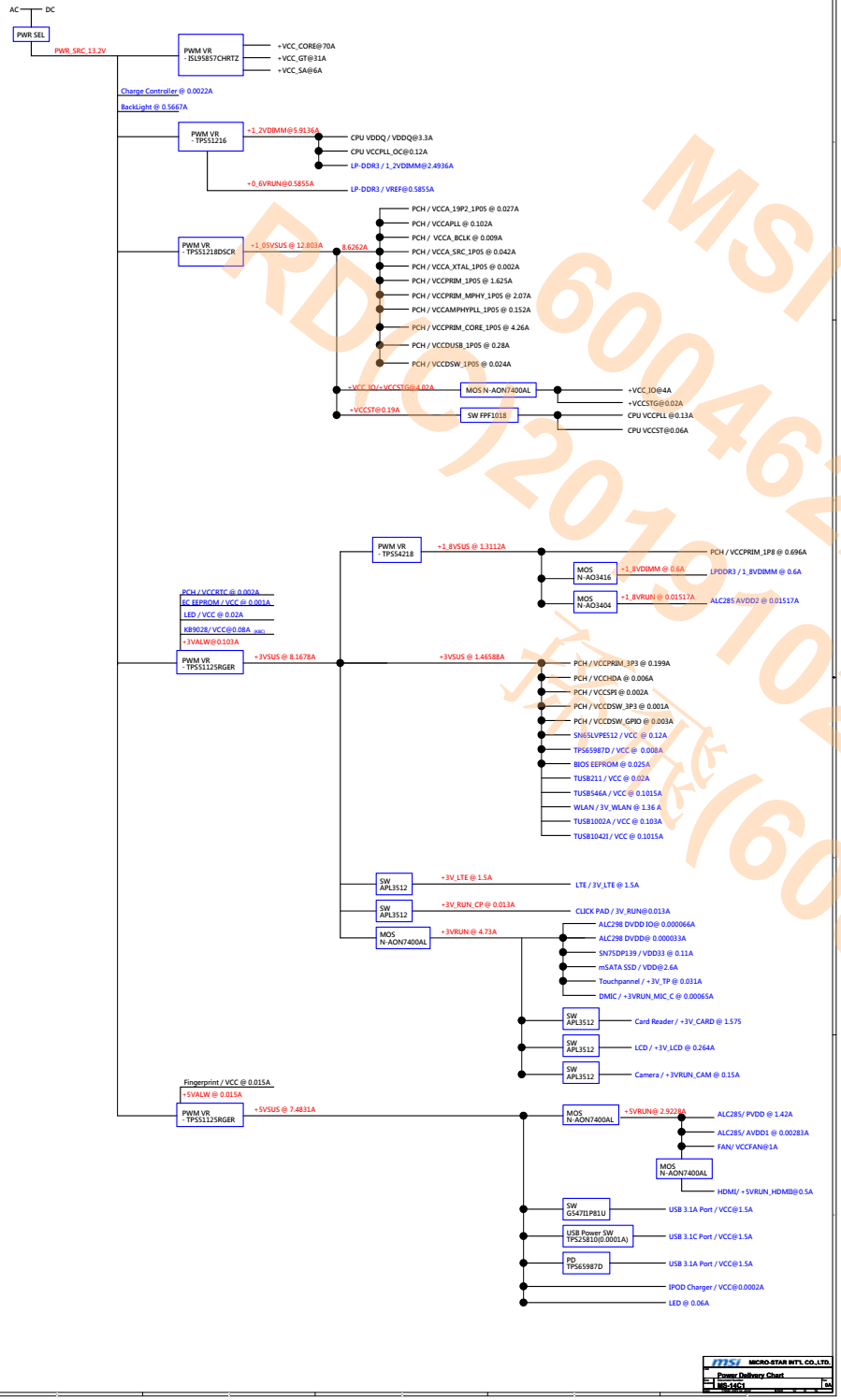
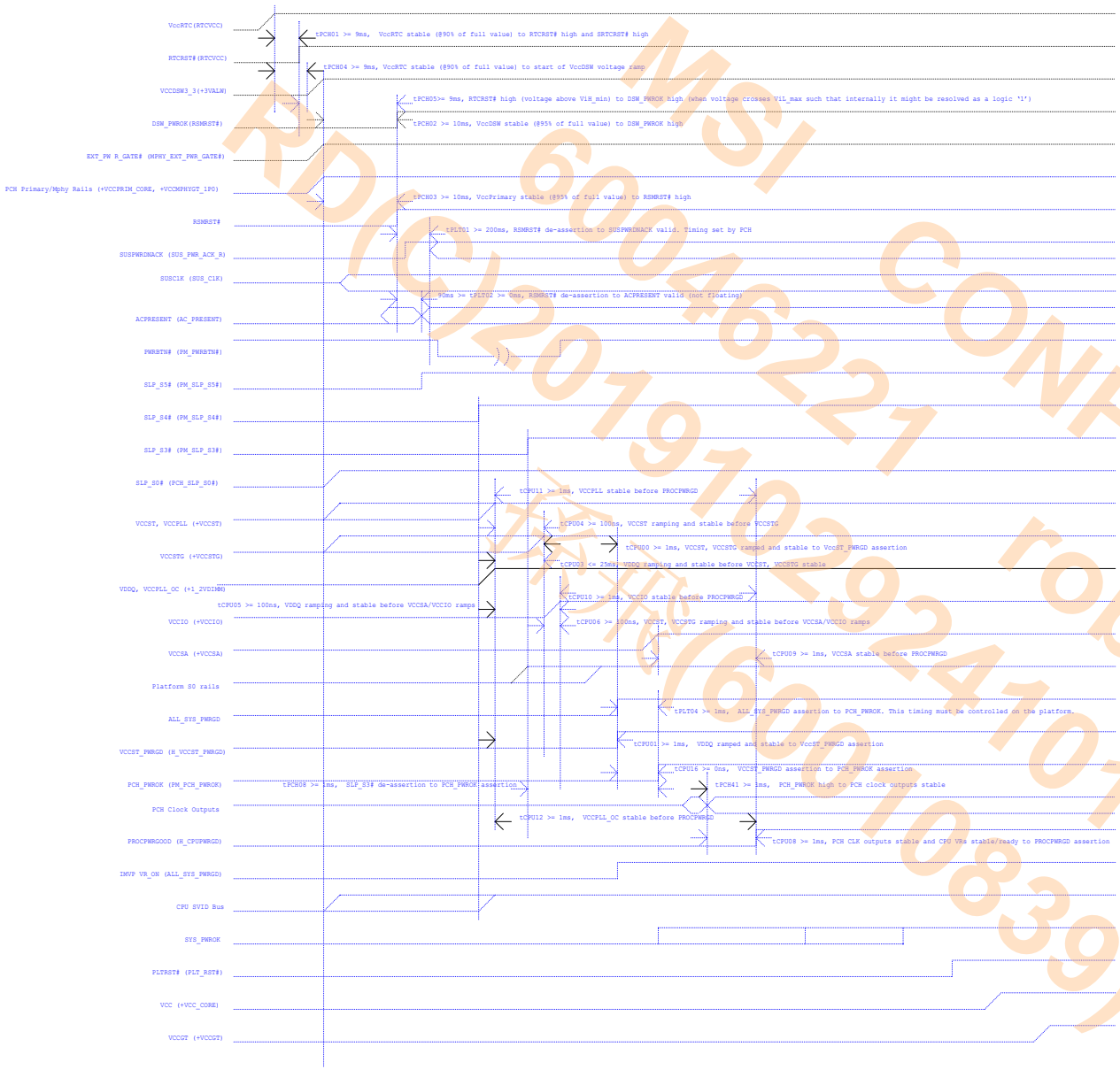
13H1 Power Delivery Chart



G3 to S0



MICRO-STAR INT'L CO.,LTD.

Title: Power sequence G3 -> S0

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S0 to G3

msi MICRO-STAR INT'L CO.,LTD.		
Title: Power sequence S0 -> G3		
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Ver: A

N/A

Ver: B

Ver: C

497. 2018/11/02 Page19 Add R585 for TPS25810 overcurrent heat issue
498. 2018/11/02 Page19 Add Type-C_OC# of signal for TPS25810 overcurrent heat issue (Del TP:INC172)
499. 2018/11/02 Page11 Change signal from USBC_OC# to Type-C_OC# for TPS25810 overcurrent heat issue

500. 2018/11/06 Page38 Update PCB shielding symbol by manufactory suggest
501. 2018/11/06 Page15 Un-stuff R215 because EC control pin is push-pull by NEC suggest

502. 2018/11/13 Page19 Change C591 from 220pF to 470pF for SA report
503. 2018/11/13 Page19 Change R573,R574 from 0 ohm to 300 ohm by NEC request

504. 2018/11/16 Page22 Change ESD11.ESD12 from AOZ8902 to AOZ8906 for USB2.0 bus leak by NEC require
505. 2018/11/16 Page29 Del ESD14.ESD16 and add ED109.ED110.ED111.ED112 ; From ESD85046 to ESD8011M for PD component shift by NEC require
506. 2018/11/16 Page26 Change R433 from 510 ohm to 620 ohm by NEC require
507. 2018/11/16 Page26 Change R402 from 243 ohm to 390 ohm by NEC require

508. 2018/11/19 Page20 Remove UME63 by ME require
509. 2018/11/19 Page24 Change R37 value from 2.2Kohm to 1Kohm for Mic cannot be detected

510. 2018/11/22 Page08 Del RTC crystal 2nd source ; Remove RTC crystal virtual component(Y6)
511. 2018/11/22 Page08 Add virtual component for 24M crystal by different BOM(Y7)
512. 2018/11/22 Page17 Stuff EC15.EC18.EC58.EC59 by EMI suggest

513. 2018/11/27 Page27 Change C498 from 100uF to 220uF for voltage drop of +3V_LTE

514. 2018/11/29 Page38 Change MB mylar(UME68) main source from E2P-3H11911-G40 to E2P-3H11911-Y42 by ME require
515. 2018/11/29 Page23 Change TUSB1002A setting by vendor suggest(CH2_EQ1.CH2_EQ2 from 1,0 to R,R)
Un-stuff R522 , stuff R525 ; change R523 from 1K ohm to 20K ohm
516. 2018/11/29 Page38 Add WiFi Module Mylar by ME require (UME69)
517. 2018/11/29 Page38 Add Pipe Acetate Tape -1 by ME require (UME70)
518. 2018/11/29 Page38 Add Pipe Acetate Tape -2 by ME require (UME71)
519. 2018/11/29 Page38 Add Rubber (Square) by ME require
(UME72.UME73.UME74.UME75.UME76.UME77.UME78.UME79.UME80.UME81)
520. 2018/11/29 Page38 Add Rubber (Circle) by ME require
(UME82.UME83.UME84.UME85)
521. 2018/11/29 Page38 Add SIM Connector Mylar by ME require (UME86)

522. 2018/12/06 Page38 Change PCB P/N from PDD-13H110B-H73 to PD0-13H110C-H73 (PCB1)

523. 2018/12/13 Page23 Un-stuff R515 for Type-C USB3.1 GEN2 compliance test by NEC request

524. 2018/12/14 Page23 Change R525.R523 from 20K ohm to 1K ohm for Type-A compliance test by NEC request
525. 2018/12/14 Page23 Un-stuff R528.R530 for Type-A compliance test by NEC request

526. 2018/12/17 Page38 UME70 and UME71 change to unstuff by ME require
527. 2018/12/17 Page38 Add Thermal DDR Sponge for 16GB by ME require (UME87)

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Title: Modified List

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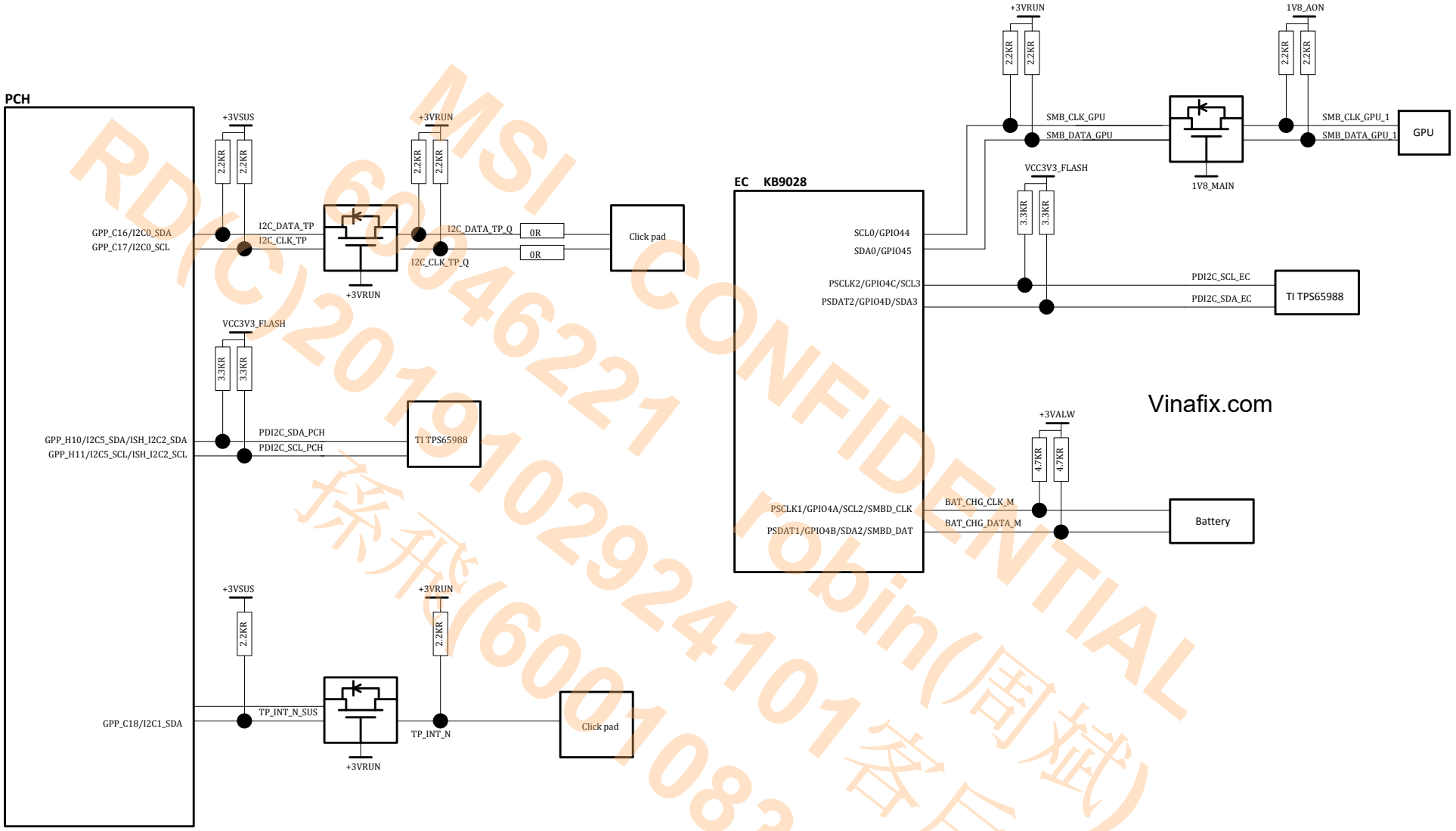

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Title: SMB_I2C Map

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