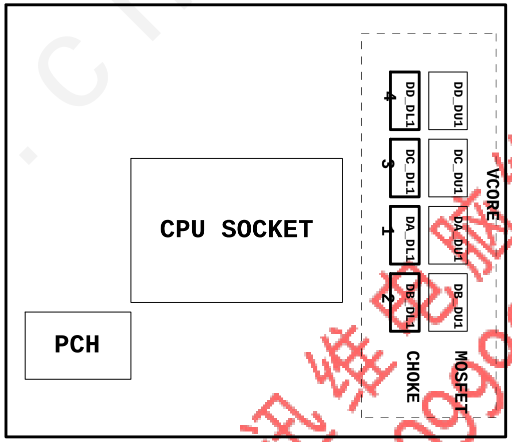
Model Name: GA-H110M-S2PV

Rev 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B-DDR4
06	CPU_LGA1151-C
07	CPU_LGA1151-D
08	DDR 4 CHANNEL A
09	DDR 4 CHANNEL B
10	PCH CLOCK BUFFER
11	PCH DMI,USB,PCIE
12	PCH MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH_PWR,GND
15	Dual BIOS
16	I/O ITE8628
17	HWM
18	FAN CTRL-SIO
19	PCIEX16 SLOT
20	PCIEX1*2 SLOT
21	SATA
22	IT8892E/FX
23	PCI SLOT
24	ISL95858_856 PWM
25	ISL95858_856 MOS_VCORE
26	ISL95858_856 MOS_VCCGT
27	VCCSA_VCCIO_VCCPLL
28	RT8237_DDR_BEAD
29	RT8068A_VPP_TRON
30	RT8237_PCH-BEAD
31	DISCRETE POWER
32	ATX POWER , -PROCHOT
33	KB_MS_USB
34	DVI

SHEET	TITLE
35	RTD2168 - DP to VGA - IC
36	RTD2168 - DP to VGA - Conn
37	R_USB30
38	Realtek 8111G
39	USB30_LAN CONNECTOR-8111HS
40	ALC887-VD2 CODEC
41	REAR AUDIO JACK
42	F_USB30
43	F_USB20
44	COM , LPT
45	F_PANEL
46	USB20 HUB , ESD
47	POWER MAP
48	POWER 零件使用表
49	TABLE LIST



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Title
Cover Sheet

Size
Custom
Document Number
GA-H110M-S2PV
Rev
1.0

Date: Thursday, October 08, 2015
Sheet 1 of 49

H110M-S2PV

Component value change history

2015/08/14

Data	Change Item	Reason
2014/10/13		
2015/01/23	R01A BOM	
2015/03/12	CPU Power Choke Change to IRON CHOKE	
2015/04/15	Update net	
	SATA EXPRESS新增Power for USB3.1小卡, 每個CONNECT都要留一顆0603 0 OHM (Page 22)	
	DDRVTT改用NCT3103S (Page 30)	
	PCI 線路GBRN1 改為R8P4R-0402-SHORT-MASK (Page 25)	
2015/05/26	R01 E-BOM release. PCB:0.1	Modify From B150M-HD3 DDR3 R01
2015/07/28	R10A D-BOM release. PCB:1.0	1. PWM BOM DAR44-->680/4/1 DAR52-->91K/4/1 DAR41-->4.87K/4/1 DAR126-->3.01K/4/1 2. DDR POWER MA_DC15.MA_DR19不上件 MA_R9.MAR10.MAR11.MAQ5.MAQ6.MAC9.MA_DR45上件.MA_DR92.2/6 MA_DR13 to 2K/4/1 , MA_DR12 to 2.15K/4/1 3. PCH POWER NPR12 to 280k/4/1. NPR21 to 471k/4/1. add NPC10 4. ADD DFR4(8.2K/4),DFC3 (22u) 5. NC7 22P change to 27P 6. DDR OV CHOOSE GPIO PIN (GP95/GP93/GP67) G_PLED CHOOSE TO GP37 7. REMOVE FPD2 (-HDLED) 8. EMIC2 change to VDDQ (for EMI , but 不上件) 9. MOS 用料 10. PCI Bridge 0ohm change to short-pad 11. DVFB1/DVFB2/DVFB3 change to "30/4/4A/S" DVC4/DVC5/DVC6 上件
2015/08/14	R10B P-BOM release. PCB:1.01	1. DDR POWER CHANGE TO 1H1L(mask MA_DQ3) 2. MA_DR15 95.3K/4/1 change to 182K/4/1 3. Remove M_BIOS SOCKET 4. OR84 N/A 5. LGA1151 H110統一使用G/F用料(10SC1-F01151-21R/22R) 8/17
2015/08/21	R10C P-BOM release. PCB:1.01	1. DANTC2 remove (NOTE 71)
2015/09/02	R01 E-BOM release. PCB:0.1	1. Modify from H110M-S2PV DDR3 to H110M-S2PV 2. DDR3 change to DDR4 (包含超壓值修改) 3. Remove PWR SEQ(P.26 for VPP_25V use RT8120 SCH) 4. Rev0.1 BIOS SOCKET 上件 5. NR286 remove (LAN 端已Pull Hi) 6. remove NR44 (重複Pull Hi) 7. remove NR17 (N_GPP_B10 已 shortpad pulll down) 8. remove NRN1 , change to NR20 / NR21 N_GPP_B5 change to NRN10 pin1 9. remove WR47 / WR46
2015/08/21	R10A P-BOM release. PCB:1.0	1. Modify from H110M-S2PV Rev01 to Rev10 2. remover BIOS SOCKET 3. DAR67 change to 16.2K

Circuit or PCB layout change

DATE	Change Item	Reason
2014/10/15 PCB:0.1	PCB first release	

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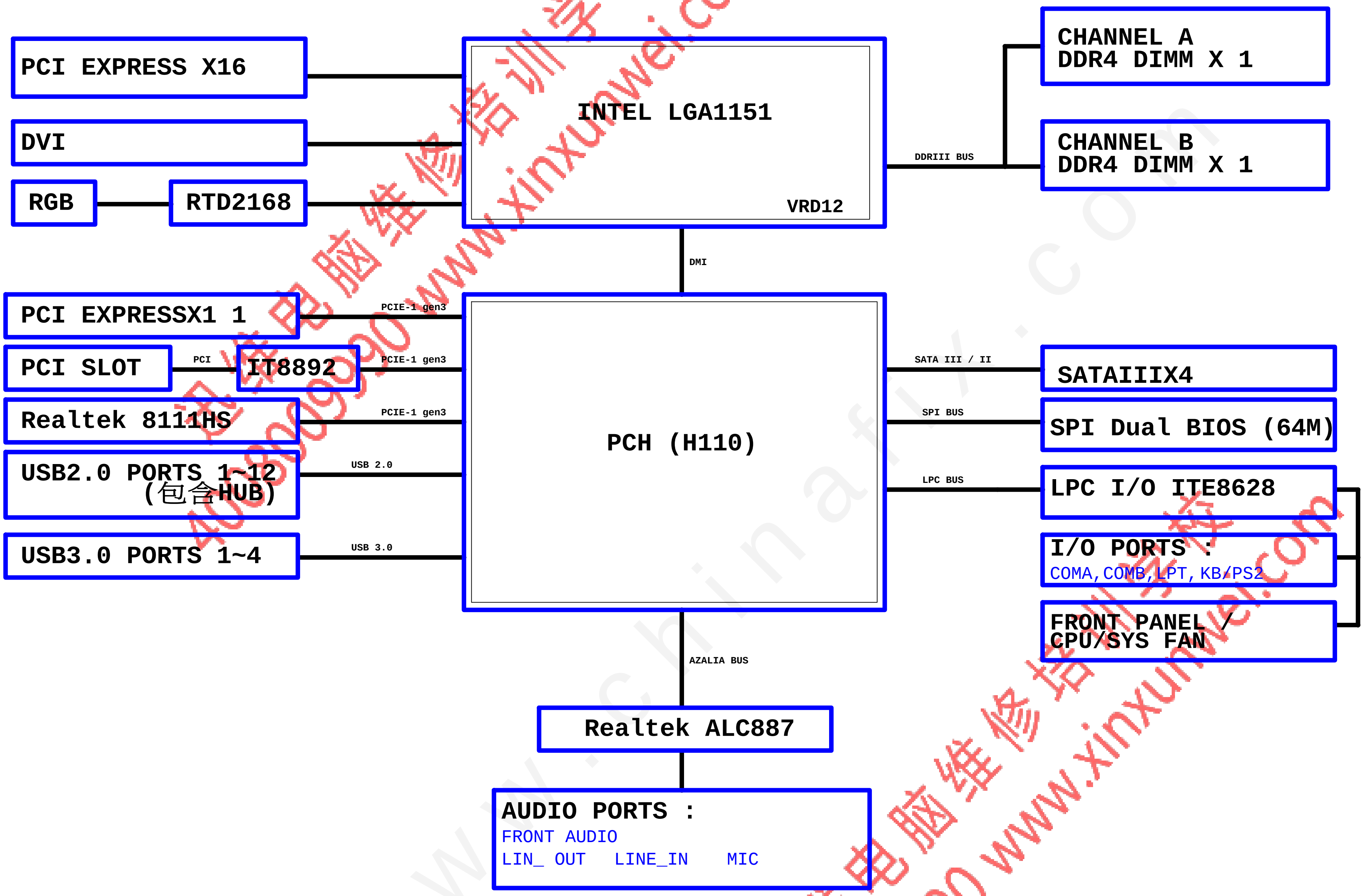
Title
BOM & PCB MODIFY HISTORY

Size	Document Number	Rev
Custom	GA-H110M-S2PV	1.0

Date: Thursday, October 08, 2015 Sheet 2 of 49

BLOCK DIAGRAM



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Title
BLOCK DIAGRAM

Size C | Document Number | GA-H110M-S2PV | Rev 1.0

Date: Thursday, October 08, 2015 | Sheet 3 of 49

*** Rev0.2B**

```
-----------------------------------------
4 layer PEG/DMI=====4/4/4//15
6 layer PEG/DMI=====4/5.5/4//15
-----------------------------------------
Impedance=85 +- 15%
```

W=12 mil out of CPU
S=15 mil out of CPU

```
G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R
```

```
-----------------------------------------
4 layer HDMI/DP/eDP/=====4/4/4//15
6 layer HDMI/DP/eDP/=====4/5.5/4//15
-----------------------------------------
Impedance=85 +- 15%
```

Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0

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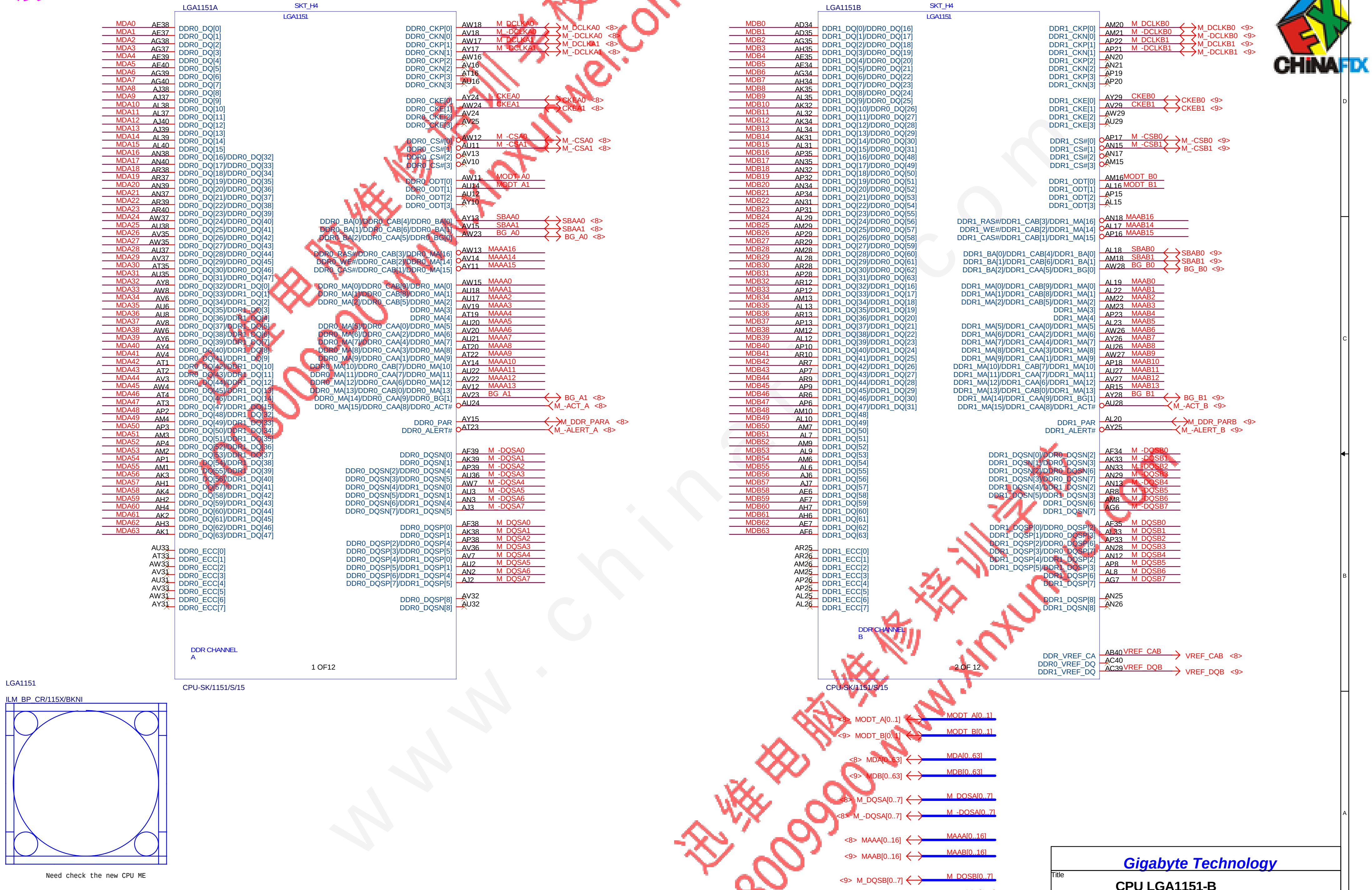
Title
CPU LGA1151-A

Size: Custom
Document Number: GA-H110M-S2PV
Rev: 1.0

Date: Thursday, October 08, 2015
Sheet 4 of 49

* 改DDR4 net



Need check the new CPU ME

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Title
CPU LGA1151-B
Size Custom
Document Number
GA-H110M-S2PV
Rev 1.0
Date: Thursday, October 08, 2015
Sheet 5 of 49