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Arrowhead

BTX **(Version: A03)**

CPU: **Intel Conroe, Wolfdale processors in LGA775 Package.**

Notice that Apart from PRD Requirement CPU will support Yorkfield as well.

System Chipset:

North Bridge ... Eaglelake-Q45
South Bridge ... ICH10DO

Main Memory:

Dual Channel / DDR-III * 4 (Maximum to 8GB)

On Board Device:

Clock Generator ... IDTCV184-2BPAG
Super I/O ... SMSC5524/5514E
LAN ... Boazman 82567-B0
HDA Codec ... AD1984A-04
BIOS ... SPI Flash ROM-64Mbit

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 1
PCI SLOT * 2

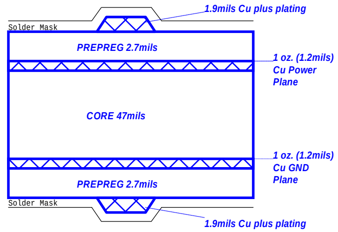
PWM Controller:

Controller ... ADP3293 (3Phase)
Driver ... ADP3120AJRZ

POP1	Proto Build	XDP, LPC HDR, SPI Debug
POP3	SIO SMSC 5524C	
POP4	SIO SMSC 5514E	
POP5	TPM STMicro(4.4mm)	
POP6	TPM Z(6.1mm)	
POP7	TPM J(6.1mm)	
POP8	TPM Winbond(4.4mm)	
POP9	QFN	

Board Stack-up

(1080 Prepreg Considerations)



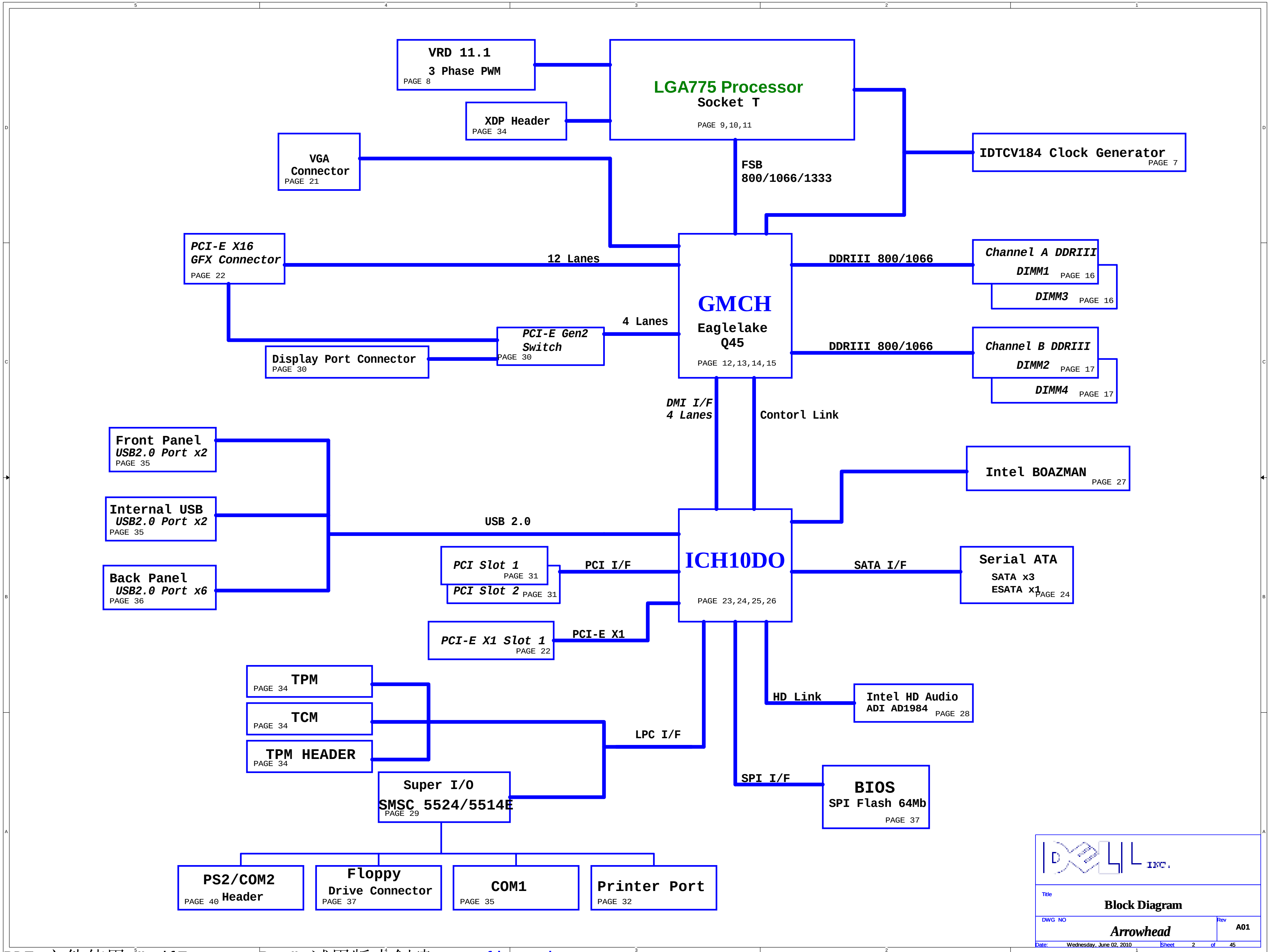
Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIE - 85ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15
LAN - 95ohm : 15/4/8/4/15

DELL INC.

Title: Cover Sheet

DWG NO: Arrowhead | Rev: A01

Date: Thursday, November 25, 2010 | Sheet 1 of 45


VRD 11.1
3 Phase PWM
PAGE 8
LGA775 Processor
Socket T
PAGE 9,10,11
XDP Header
PAGE 34
VGA
Connector
PAGE 21
FSB
800/1066/1333
IDTCV184 Clock Generator
PAGE 7
PCI-E X16
GFX Connector
PAGE 22
12 Lanes
GMCH
Eaglelake
Q45
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DDRIII 800/1066
Channel A DDRIII
DIMM1 PAGE 16
DIMM3 PAGE 16
4 Lanes
PCI-E Gen2
Switch
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Display Port Connector
PAGE 30
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DIMM2 PAGE 17
DIMM4 PAGE 17
DMI I/F
4 Lanes
Contorl Link
Front Panel
USB2.0 Port x2
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Internal USB
USB2.0 Port x2
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USB 2.0
ICH10DO
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PCI Slot 1
PAGE 31
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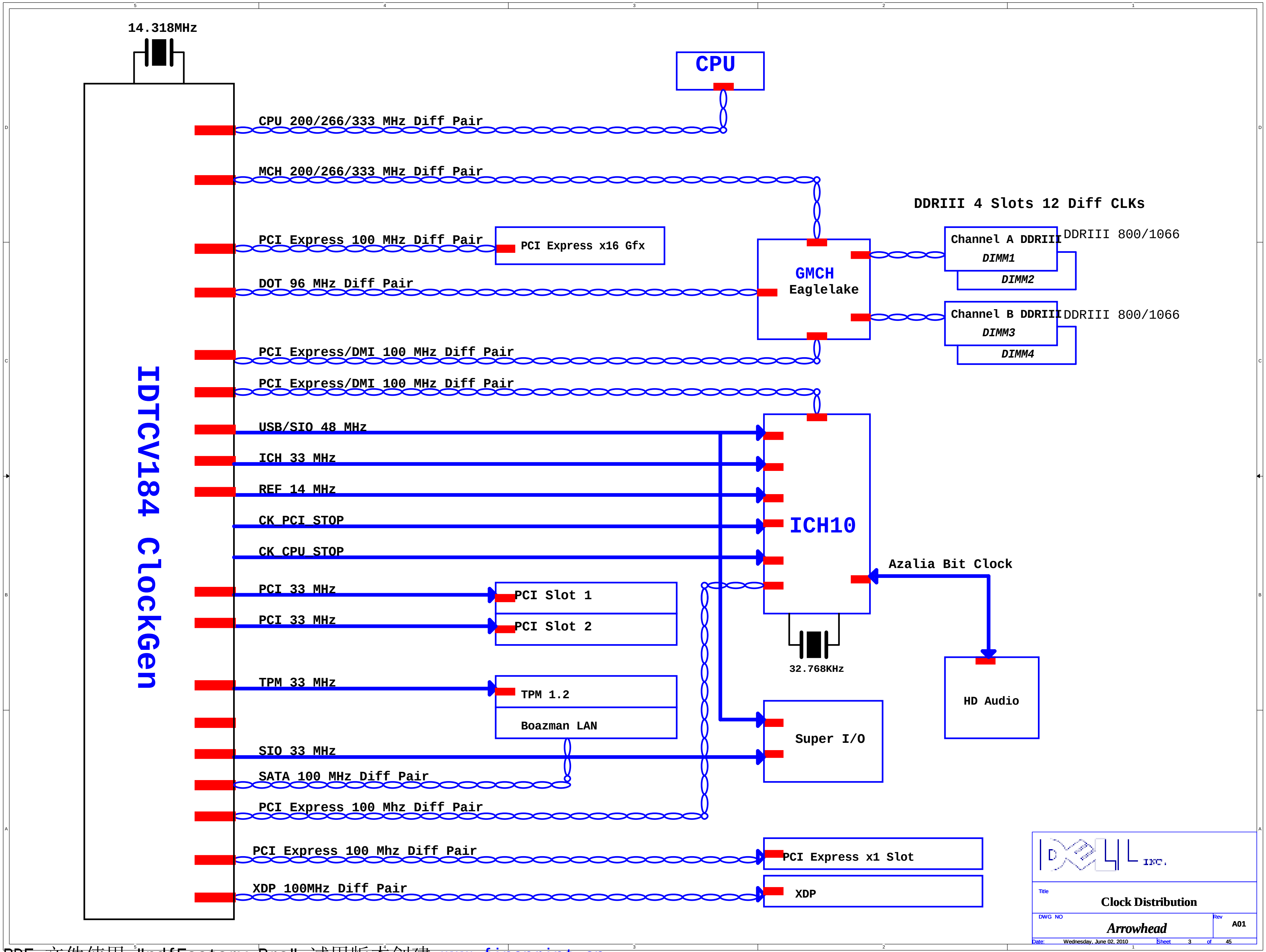
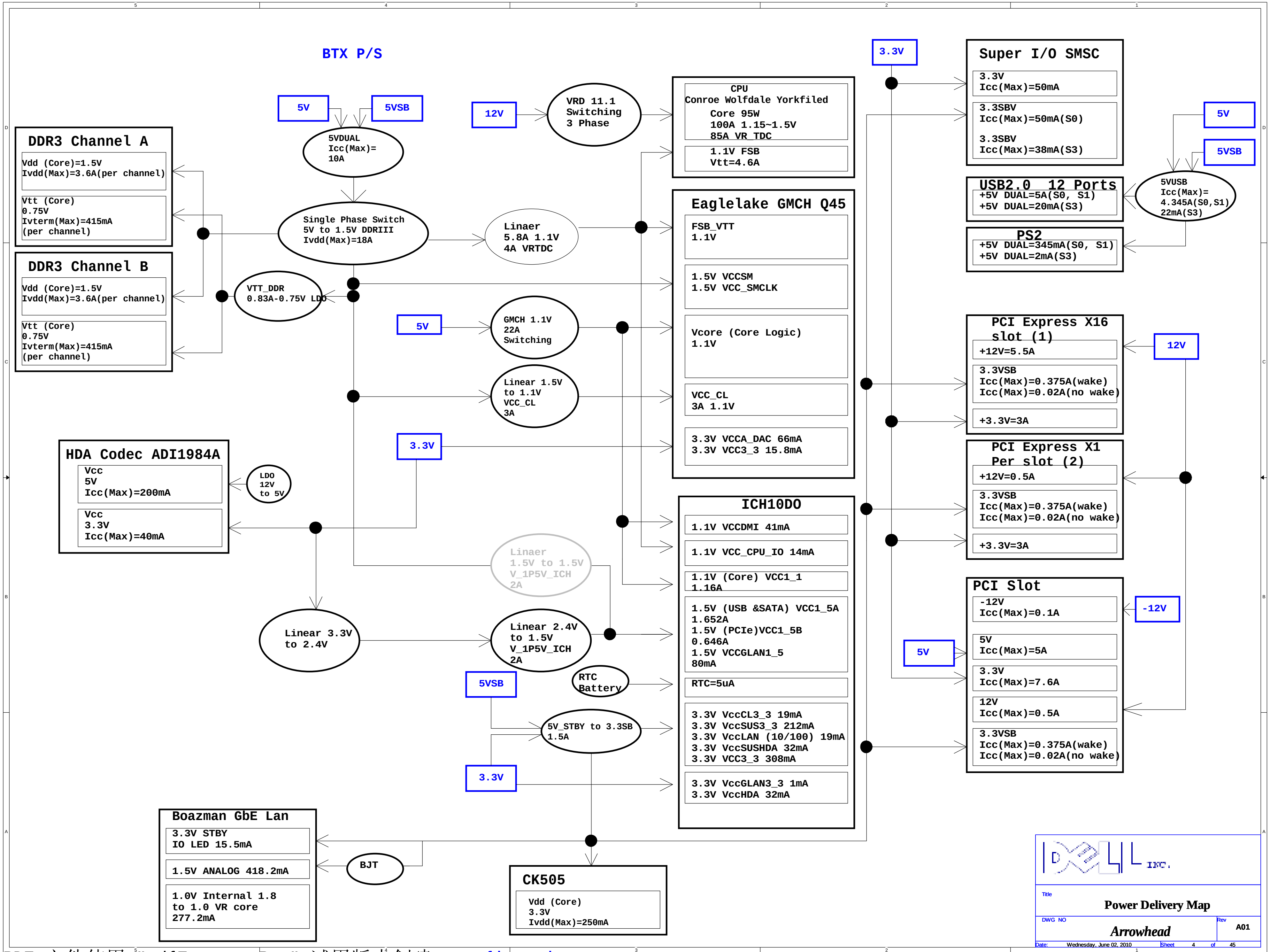
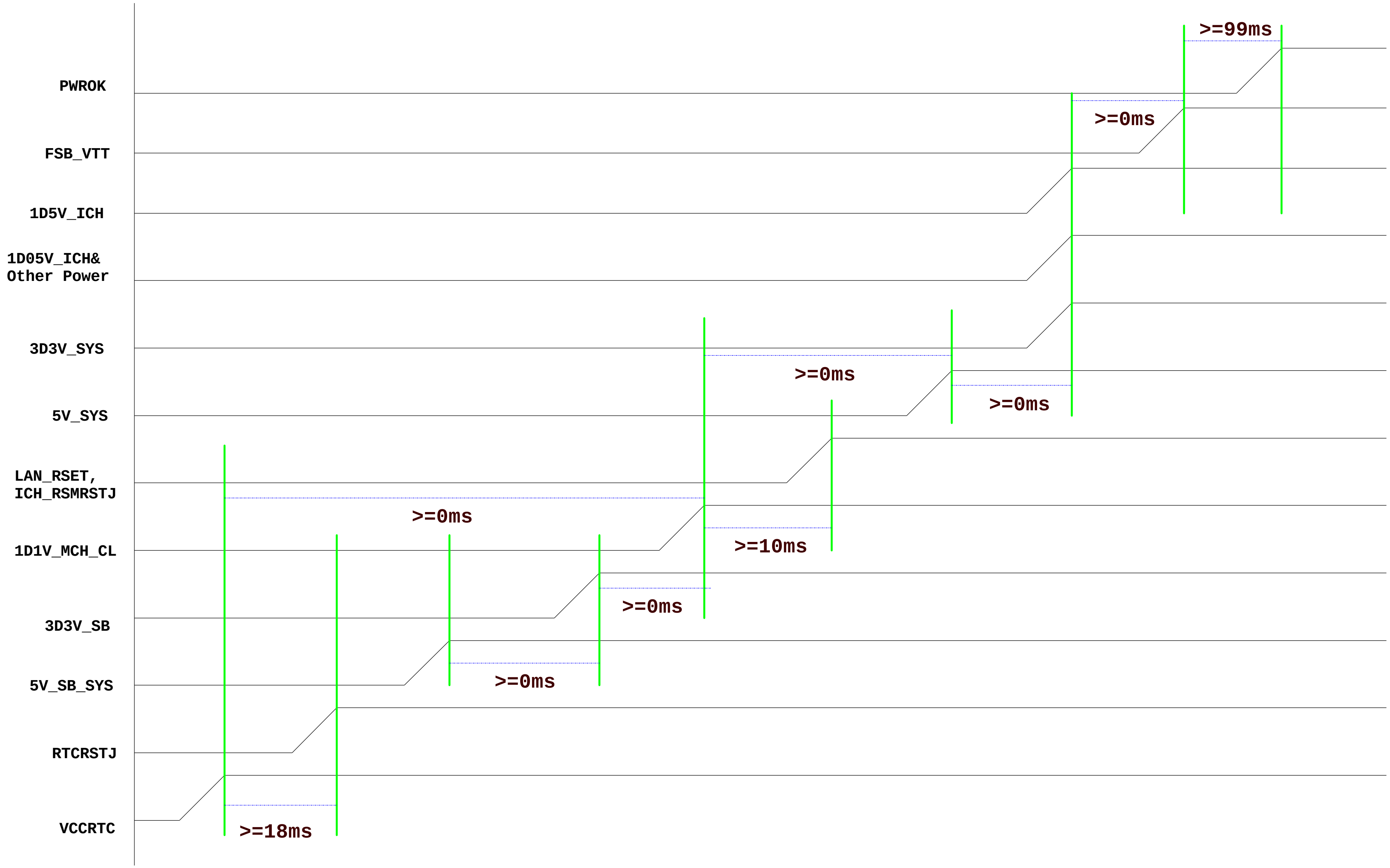
PCI I/F
SATA I/F
Serial ATA
SATA x3
ESATA x1
PAGE 24
Back Panel
USB2.0 Port x6
PAGE 36
PCI-E X1 Slot 1
PAGE 22
PCI-E X1
TPM
PAGE 34
TCM
PAGE 34
TPM HEADER
PAGE 34
HD Link
Intel HD Audio
ADI AD1984
PAGE 28
LPC I/F
SPI I/F
Super I/O
SMSC 5524/5514E
PAGE 29
BIOS
SPI Flash 64Mb
PAGE 37
PS2/COM2
Header
PAGE 40
Floppy
Drive Connector
PAGE 37
COM1
PAGE 35
Printer Port
PAGE 32
DELL INC.
Title
Block Diagram
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, June 02, 2010
Sheet 2 of 45


14.318MHz
IDTCV184 ClockGen
CPU
CPU 200/266/333 MHz Diff Pair
MCH 200/266/333 MHz Diff Pair
PCI Express 100 MHz Diff Pair
PCI Express x16 Gfx
DOT 96 MHz Diff Pair
GMCH
Eaglelake
DDRIII 4 Slots 12 Diff CLKs
Channel A DDRIII
DIMM1
DIMM2
DDRIII 800/1066
Channel B DDRIII
DIMM3
DIMM4
DDRIII 800/1066
PCI Express/DMI 100 MHz Diff Pair
PCI Express/DMI 100 MHz Diff Pair
USB/SIO 48 MHz
ICH 33 MHz
REF 14 MHz
CK_PCI_STOP
CK_CPU_STOP
ICH10
Azalia Bit Clock
PCI 33 MHz
PCI Slot 1
PCI 33 MHz
PCI Slot 2
32.768KHz
HD Audio
TPM 33 MHz
TPM 1.2
Boazman LAN
Super I/O
SIO 33 MHz
SATA 100 MHz Diff Pair
PCI Express 100 Mhz Diff Pair
PCI Express 100 Mhz Diff Pair
PCI Express x1 Slot
XDP 100MHz Diff Pair
XDP
INC.
Title
Clock Distribution
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, June 02, 2010
Sheet 3 of 45


BTX P/S
5V
5VSB
5VDUAL
Icc(Max)=
10A
12V
VRD 11.1
Switching
3 Phase
CPU
Conroe Wolfdale Yorkfiled
Core 95W
100A 1.15~1.5V
85A VR_TDC
1.1V FSB
Vtt=4.6A
3.3V
Super I/O SMSC
3.3V
Icc(Max)=50mA
3.3SBV
Icc(Max)=50mA(S0)
3.3SBV
Icc(Max)=38mA(S3)
5V
5VSB
5VUSB
Icc(Max)=
4.345A(S0,S1)
22mA(S3)
USB2.0 12 Ports
+5V DUAL=5A(S0, S1)
+5V DUAL=20mA(S3)
PS2
+5V DUAL=345mA(S0, S1)
+5V DUAL=2mA(S3)
DDR3 Channel A
Vdd (Core)=1.5V
Ivdd(Max)=3.6A(per channel)
Vtt (Core)
0.75V
Ivterm(Max)=415mA
(per channel)
DDR3 Channel B
Vdd (Core)=1.5V
Ivdd(Max)=3.6A(per channel)
Vtt (Core)
0.75V
Ivterm(Max)=415mA
(per channel)
Single Phase Switch
5V to 1.5V DDRIII
Ivdd(Max)=18A
Linaer
5.8A 1.1V
4A VRTDC
VTT_DDR
0.83A-0.75V LDO
Eaglelake GMCH Q45
FSB_VTT
1.1V
1.5V VCCSM
1.5V VCC_SMCLK
Vcore (Core Logic)
1.1V
VCC_CL
3A 1.1V
3.3V VCCA_DAC 66mA
3.3V VCC3_3 15.8mA
5V
GMCH 1.1V
22A
Switching
Linear 1.5V
to 1.1V
VCC_CL
3A
PCI Express X16
slot (1)
+12V=5.5A
3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)
+3.3V=3A
12V
PCI Express X1
Per slot (2)
+12V=0.5A
3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)
+3.3V=3A
3.3V
HDA Codec ADI1984A
Vcc
5V
Icc(Max)=200mA
Vcc
3.3V
Icc(Max)=40mA
LDO
12V
to 5V
ICH10DO
1.1V VCCDMI 41mA
1.1V VCC_CPU_IO 14mA
1.1V (Core) VCC1_1
1.16A
1.5V (USB &SATA) VCC1_5A
1.652A
1.5V (PCIe)VCC1_5B
0.646A
1.5V VCCGLAN1_5
80mA
RTC=5uA
3.3V VccCL3_3 19mA
3.3V VccSUS3_3 212mA
3.3V VccLAN (10/100) 19mA
3.3V VccSUSHDA 32mA
3.3V VCC3_3 308mA
3.3V VccGLAN3_3 1mA
3.3V VccHDA 32mA
Linaer
1.5V to 1.5V
V_1P5V_ICH
2A
Linear 3.3V
to 2.4V
Linear 2.4V
to 1.5V
V_1P5V_ICH
2A
RTC
Battery
5VSB
5V_STBY to 3.3SB
1.5A
3.3V
PCI Slot
-12V
Icc(Max)=0.1A
-12V
5V
5V
Icc(Max)=5A
3.3V
Icc(Max)=7.6A
12V
Icc(Max)=0.5A
3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)
Boazman GbE Lan
3.3V STBY
IO LED 15.5mA
1.5V ANALOG 418.2mA
1.0V Internal 1.8
to 1.0 VR core
277.2mA
BJT
CK505
Vdd (Core)
3.3V
Ivdd(Max)=250mA
INC.
Title
Power Delivery Map
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, June 02, 2010
Sheet 4 of 45



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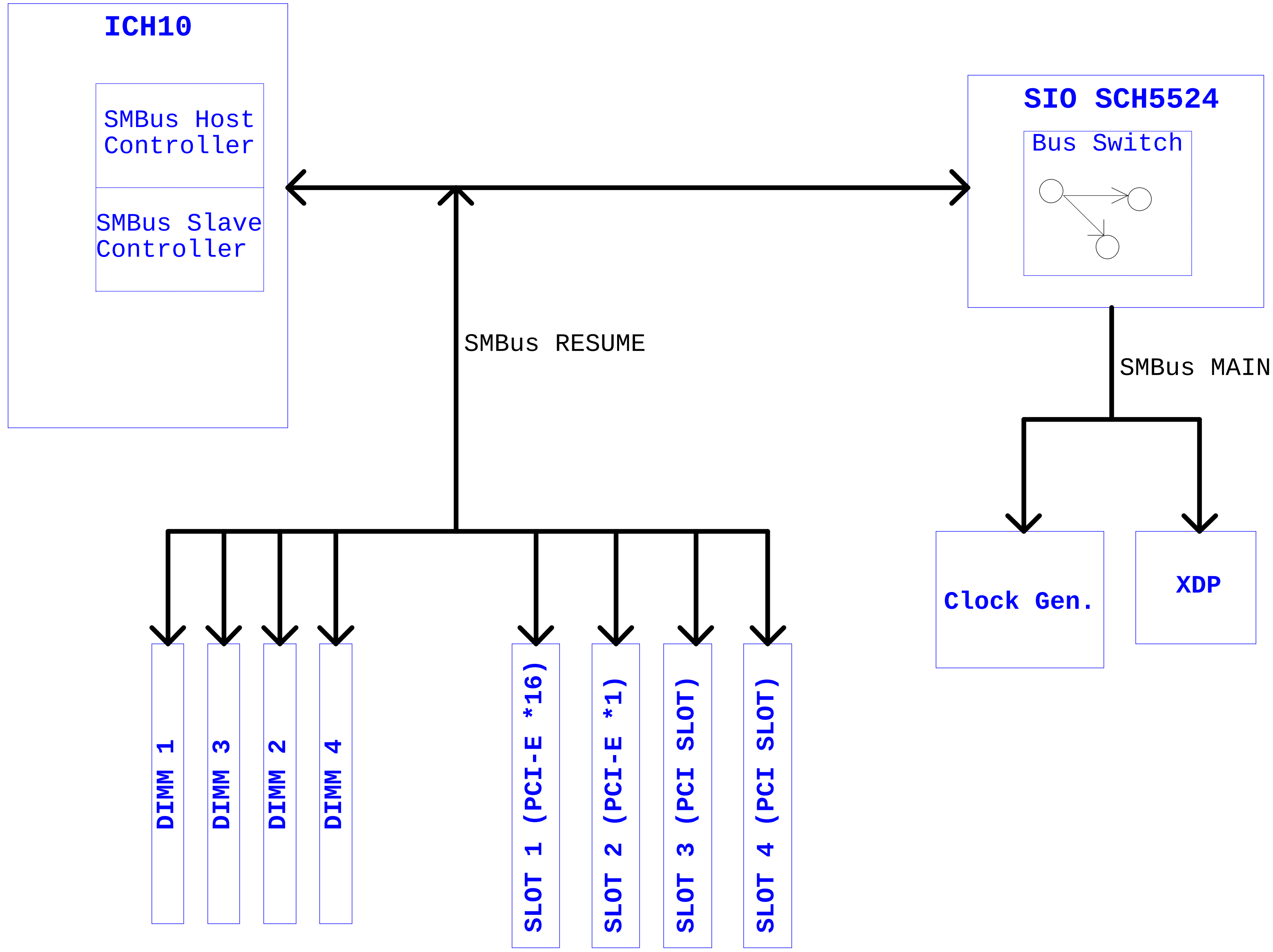
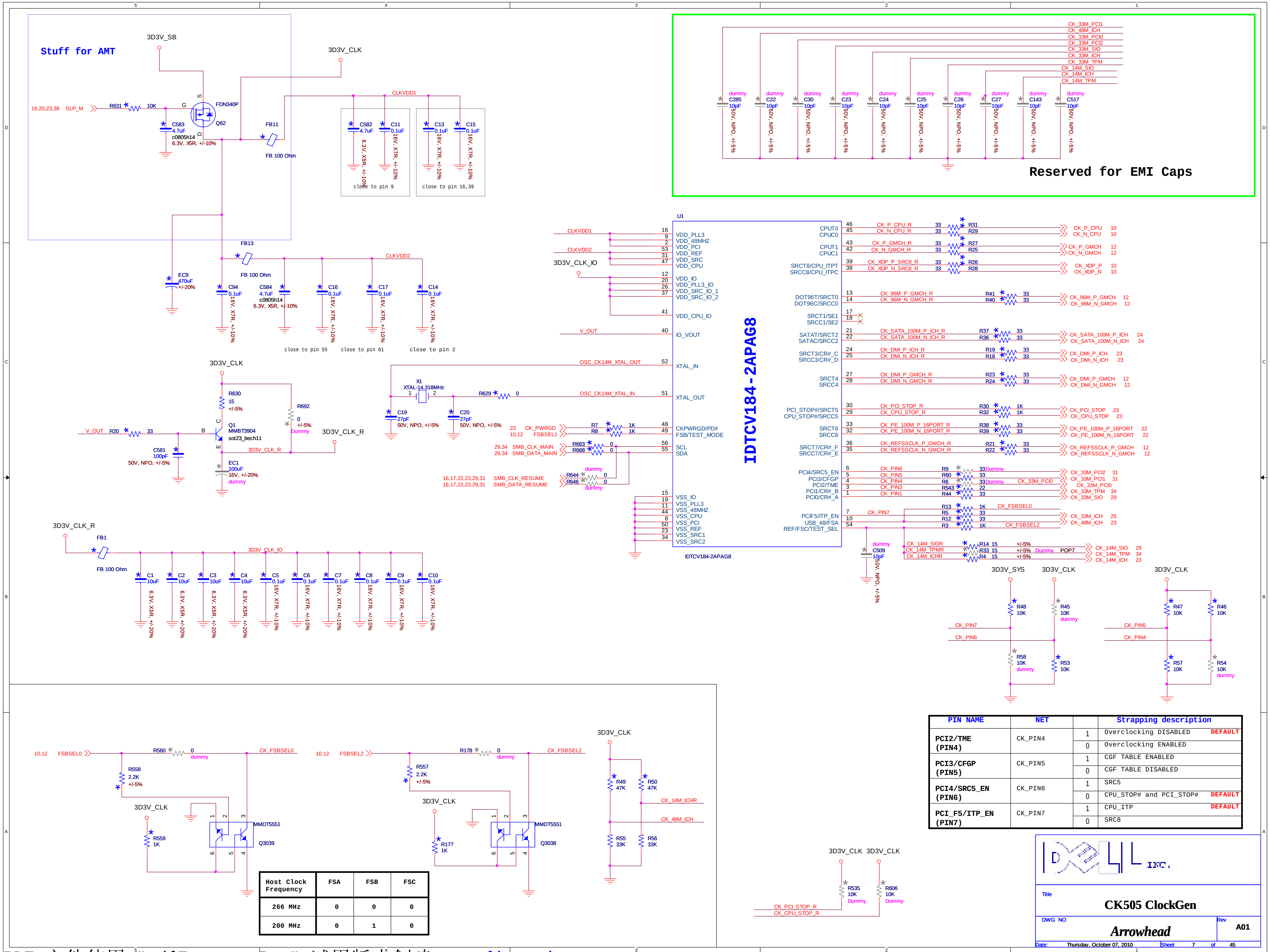
Title
Platform Sequence

DWG NO	Rev
Arrowhead	A01

Date: Wednesday, June 02, 2010 Sheet 5 of 45



Title	SM BUS
DWG NO	Arrowhead
Rev	A01
Date: Wednesday, June 02, 2010	Sheet 6 of 45



Host Clock Frequency	FSA	FSB	FSC
266 MHz	0	0	0
200 MHz	0	1	0

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CFGP (PIN5)	CK_PIN5	1	CGF TABLE ENABLED
		0	CGF TABLE DISABLED
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5
		0	CPU_STOP# and PCI_STOP# DEFAULT
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP DEFAULT
		0	SRC8

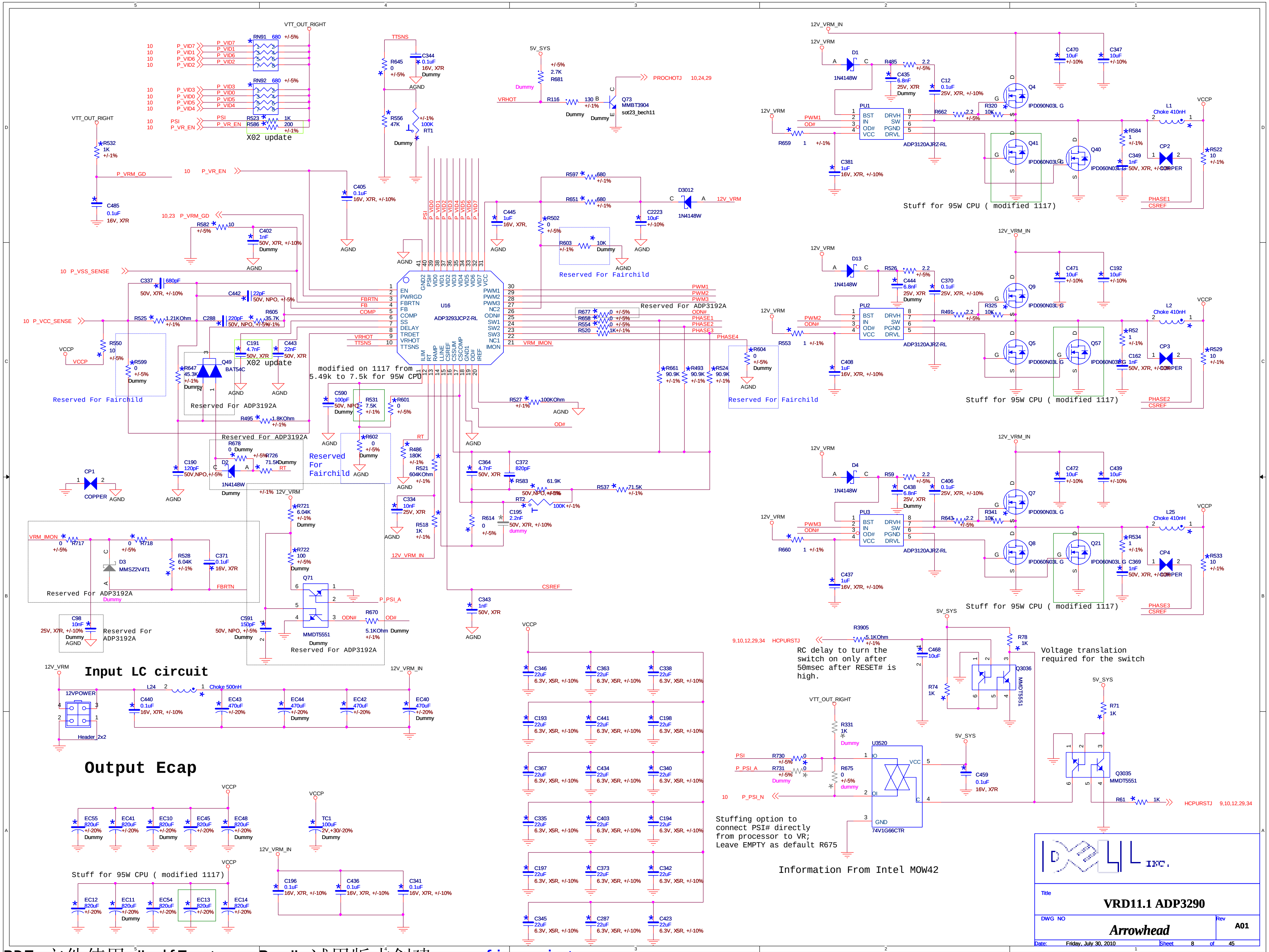
INC.

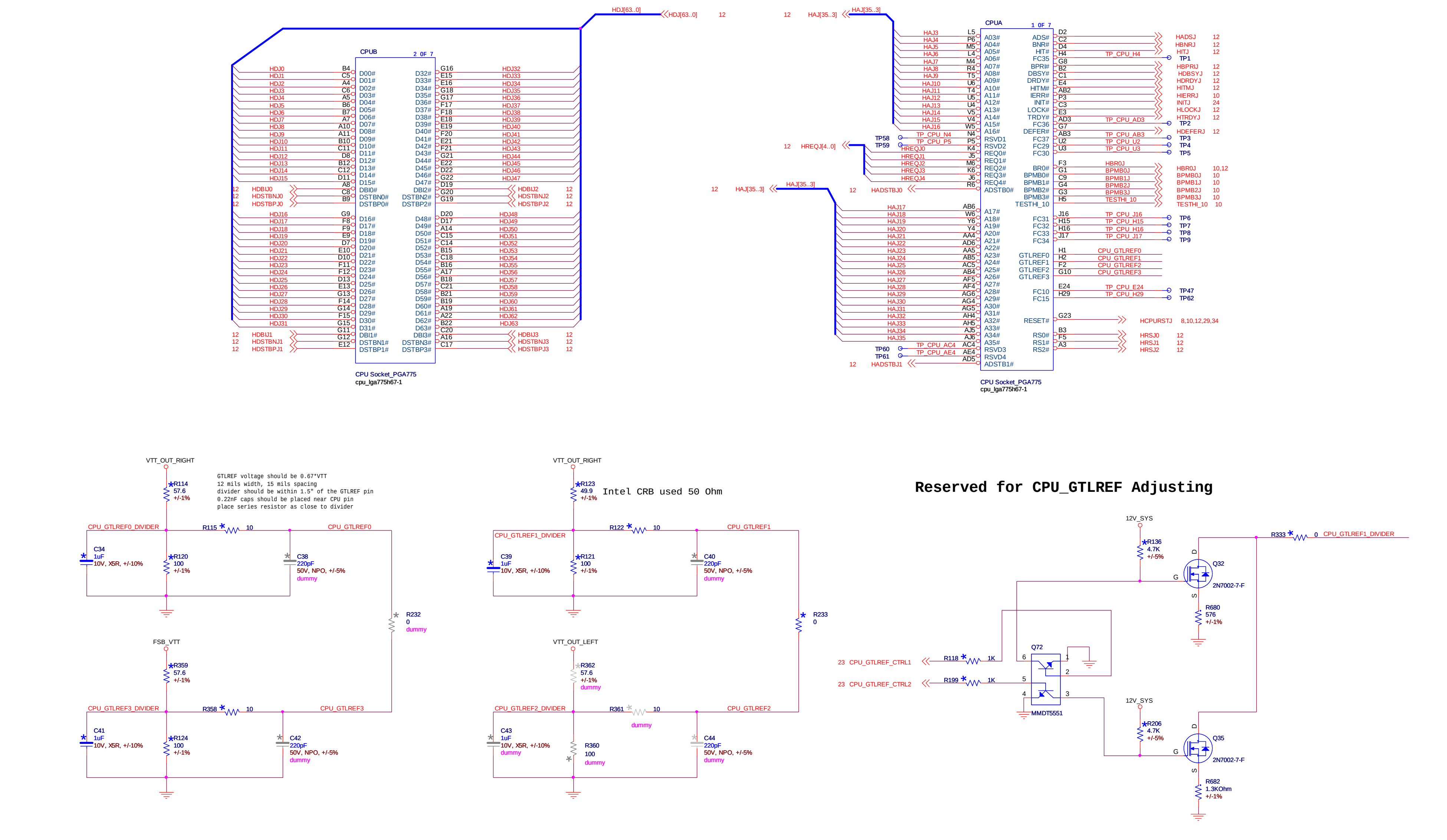
Title
CK505 ClockGen

DWG NO
Arrowhead

Rev
A01

Date: Thursday, October 07, 2010 Sheet 7 of 45


VTT_OUT_RIGHT
X02 update
U16
ADP3293JCPZ-RL
modified on 1117 from 5.49k to 7.5k for 95W CPU
Reserved For ADP3192A
Reserved For Fairchild
Reserved For ADP3192A
MMDT5551
PU1
ADP3120AJRZ-RL
Stuff for 95W CPU (modified 1117)
PU2
ADP3120AJRZ-RL
Stuff for 95W CPU (modified 1117)
PU3
ADP3120AJRZ-RL
Stuff for 95W CPU (modified 1117)
Input LC circuit
Output Ecap
Stuff for 95W CPU (modified 1117)
RC delay to turn the switch on only after 50msec after RESET# is high.
Voltage translation required for the switch
Stuffing option to connect PSI# directly from processor to VR; Leave EMPTY as default R675
Information From Intel MOW42
U3520
74V1G66CTR
Title
VRD11.1 ADP3290
DWG NO
Arrowhead
Rev
A01
Date: Friday, July 30, 2010
Sheet 8 of 45



Reserved for CPU_GTLREF Adjusting

CPU_GTLREF_CTRL1 GP60	CPU_GTLREF_CTRL2 GP18 / 20	GTLREF	
0	0	0.615 x Vtt	
0	1	0.63 x Vtt	Default Value
1	0	0.65 x Vtt	
1	1	0.67 x Vtt	

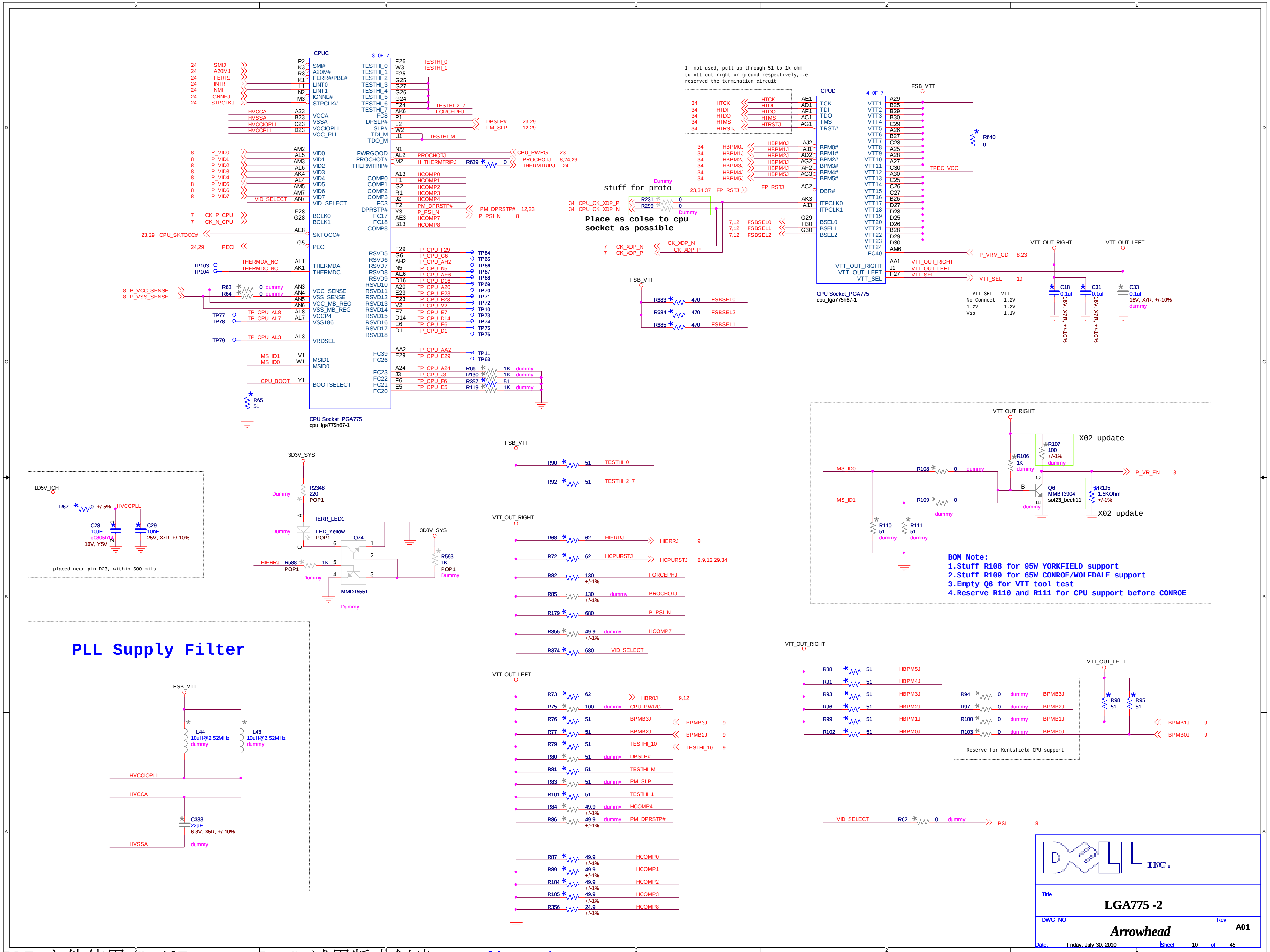
DELL INC.

Title: LGA775 -1

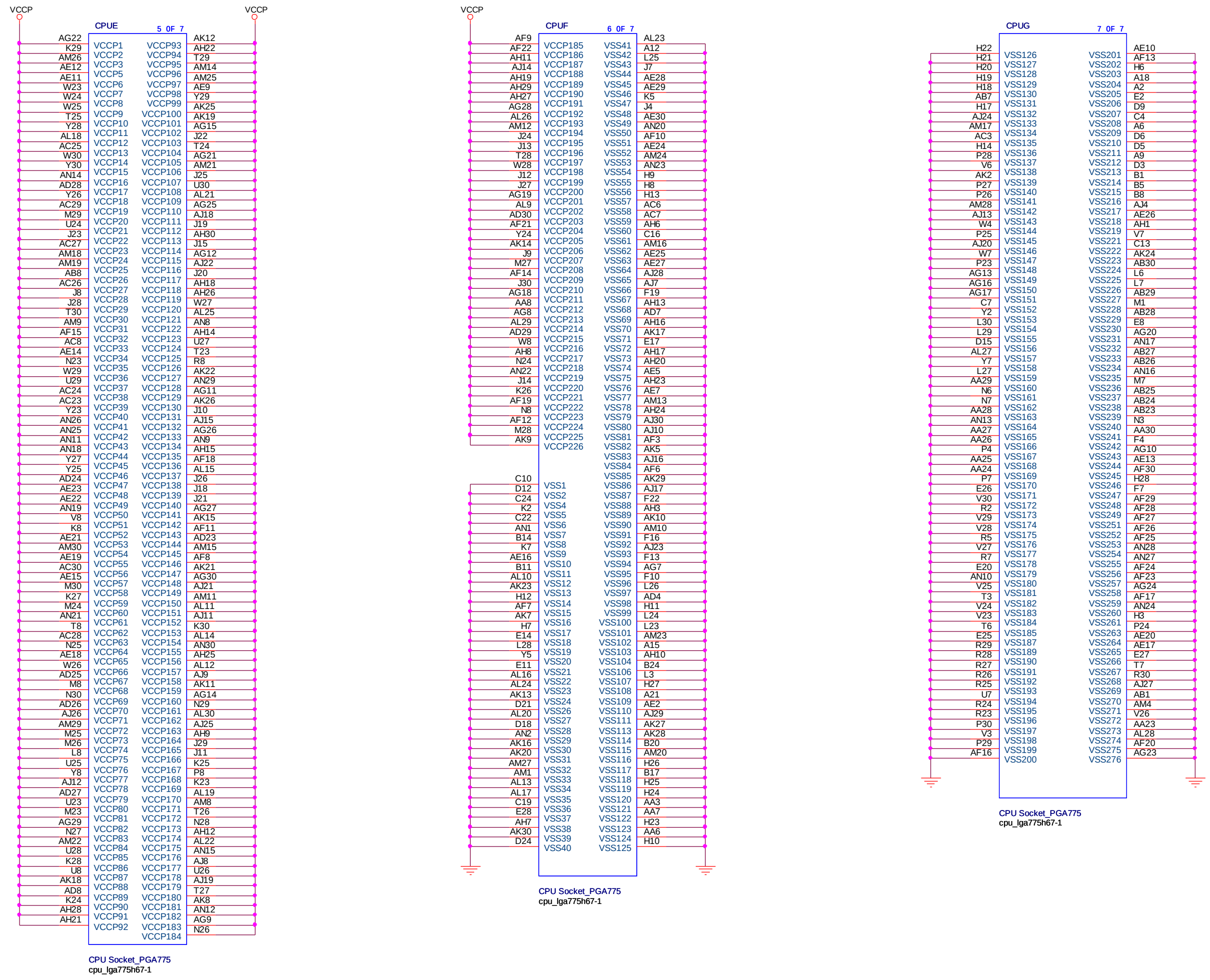
DWG NO: Arrowhead

Rev: A01

Date: Friday, July 30, 2010 Sheet 9 of 45



CPUC
CPU Socket_PGA775
cpu_lga775h67-1
If not used, pull up through 51 to 1k ohm
to vtt_out_right or ground respectively,i.e
reserved the termination circuit
CPUD
stuff for proto
Place as colse to cpu
socket as possible
VTT_SEL VTT
No Connect 1.2V
1.2V 1.2V
Vss 1.1V
placed near pin D23, within 500 mils
PLL Supply Filter
X02 update
BOM Note:
1.Stuff R108 for 95W YORKFIELD support
2.Stuff R109 for 65W CONROE/WOLFDALE support
3.Empty Q6 for VTT tool test
4.Reserve R110 and R111 for CPU support before CONROE
Reserve for Kentsfield CPU support
Title
LGA775 -2
DWG NO
Arrowhead
Rev
A01
Date: Friday, July 30, 2010
Sheet 10 of 45



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Title

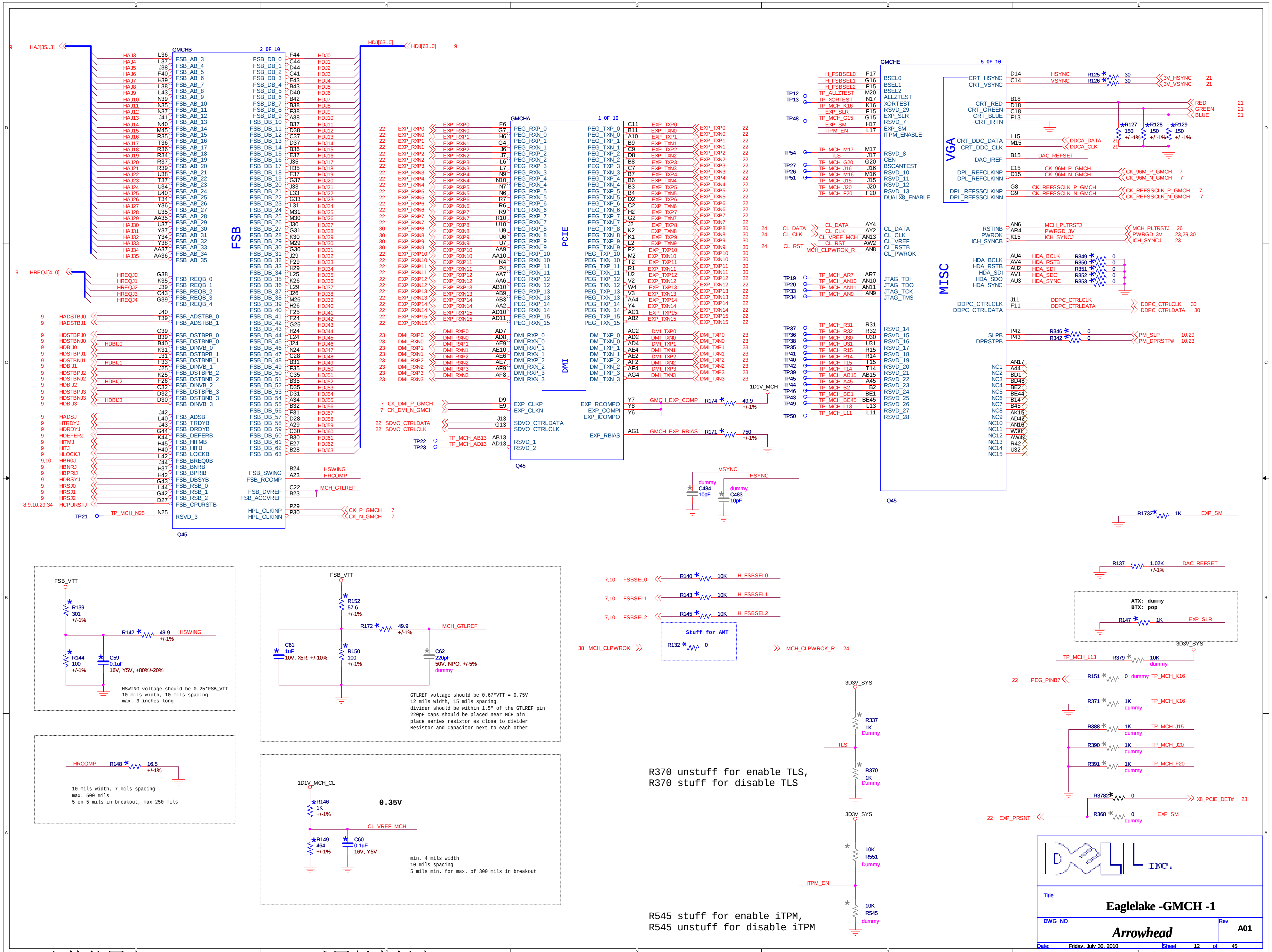
LGA775 -3

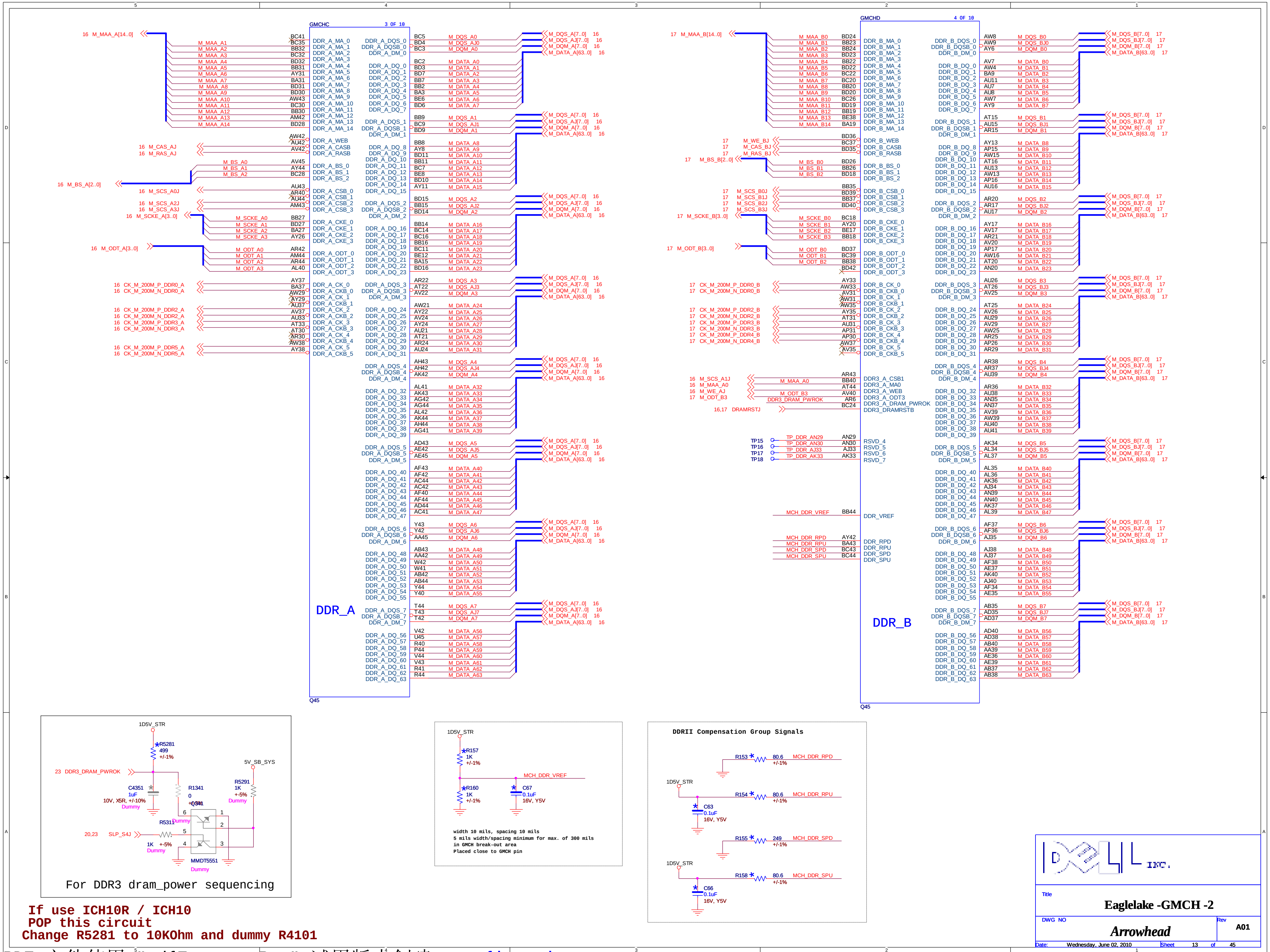
DWG NO

Arrowhead

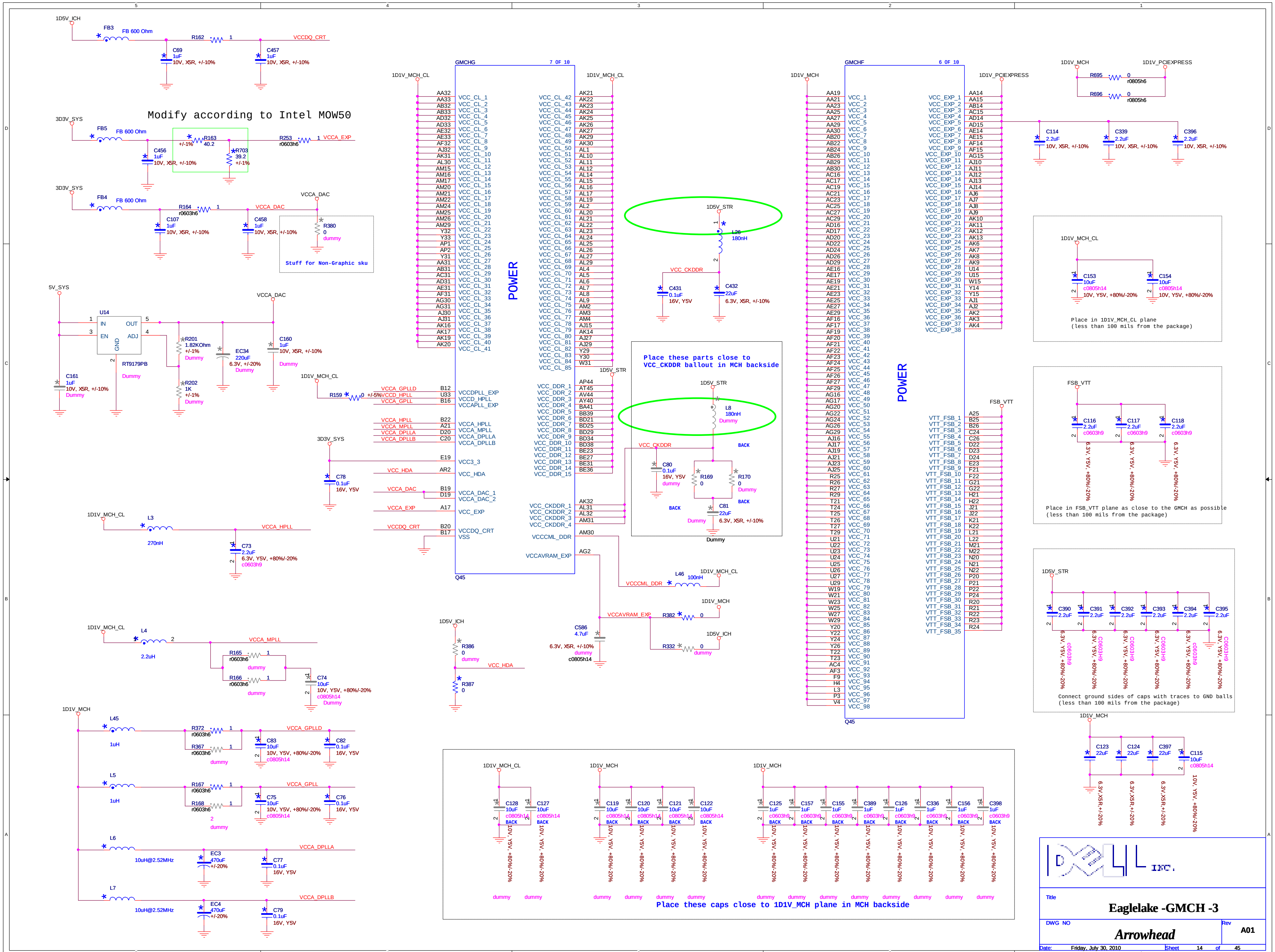
Rev A01

Date: Wednesday, June 02, 2010 Sheet 11 of 45

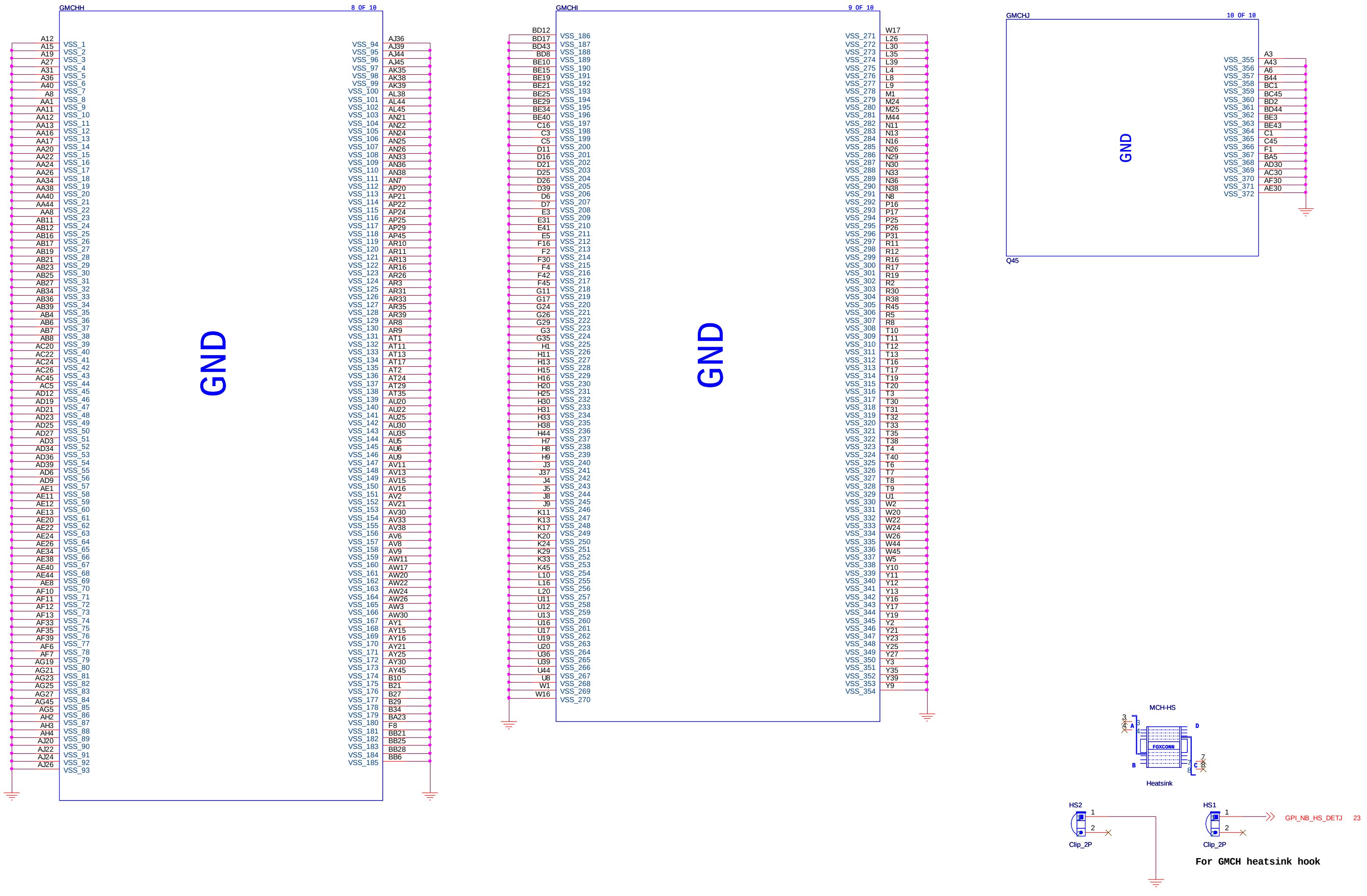

GMCHB 2 OF 10
FSB
Q45
GMCHA 1 OF 10
PCIE
DMI
Q45
GMCHE 5 OF 10
VGA
MISC
Q45
HSWING voltage should be 0.25*FSB_VTT
10 mils width, 10 mils spacing
max. 3 inches long
GTLREF voltage should be 0.67*VTT = 0.75V
12 mils width, 15 mils spacing
divider should be within 1.5" of the GTLREF pin
220pF caps should be placed near MCH pin
place series resistor as close to divider
Resistor and Capacitor next to each other
10 mils width, 7 mils spacing
max. 500 mils
5 on 5 mils in breakout, max 250 mils
0.35V
min. 4 mils width
10 mils spacing
5 mils min. for max. of 300 mils in breakout
Stuff for AMT
ATX: dummy
BTX: pop
R370 unstuff for enable TLS,
R370 stuff for disable TLS
R545 stuff for enable iTPM,
R545 unstuff for disable iTPM
DELL INC.
Title
Eaglelake -GMCH -1
DWG NO
Arrowhead
Rev
A01
Date: Friday, July 30, 2010
Sheet 12 of 45



If use ICH10R / ICH10
POP this circuit
Change R5281 to 10KOhm and dummy R4101



Modify according to Intel MOW50
GMCHG 7 OF 10
POWER
GMCHF 6 OF 10
POWER
Stuff for Non-Graphic sku
Place these parts close to VCC_CKDDR ballout in MCH backside
Place in 1D1V_MCH_CL plane (less than 100 mils from the package)
Place in FSB_VTT plane as close to the GMCH as possible (less than 100 mils from the package)
Connect ground sides of caps with traces to GND balls (less than 100 mils from the package)
Place these caps close to 1D1V_MCH plane in MCH backside
Title
Eaglelake -GMCH -3
DWG NO
Arrowhead
Rev
A01
Date: Friday, July 30, 2010
Sheet 14 of 45



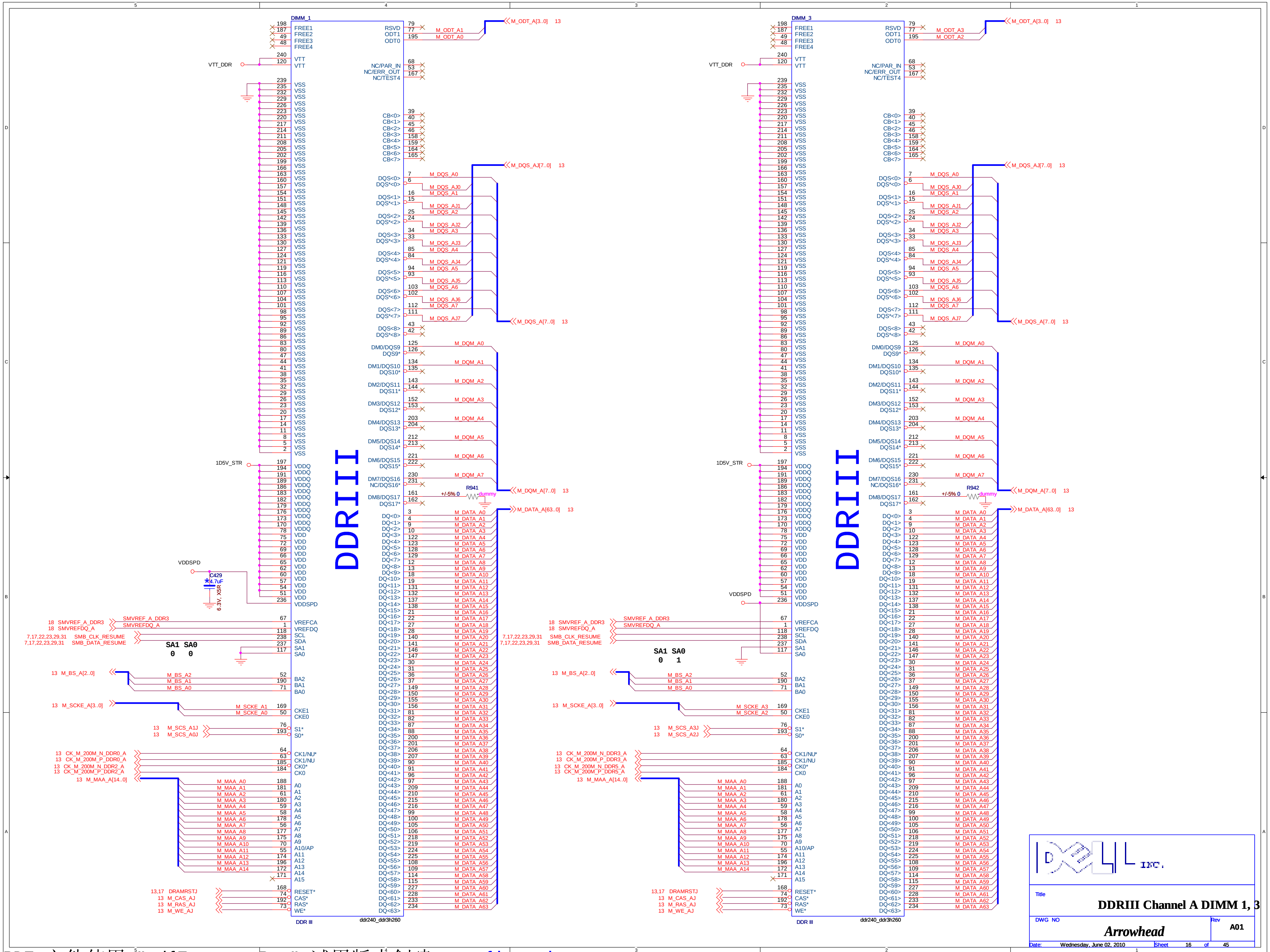
INC.

Title: **Eaglelake -GMCH -4**

DWG NO: *Arrowhead*

Rev: A01

Date: Wednesday, June 02, 2010 | Sheet 15 of 45


DIMM_1
DIMM_3
DDRIII
DDR III
ddr240_ddr3h260
VTT_DDR
1D5V_STR
VDDSPD
C429
4.7uF
6.3V, X5R
R941
R942
+/-5% 0
dummy
M_ODT_A[3..0] 13
M_DQS_AJ[7..0] 13
M_DQS_A[7..0] 13
M_DQM_A[7..0] 13
M_DATA_A[63..0] 13
18 SMVREF_A_DDR3
18 SMVREFDQ_A
7,17,22,23,29,31 SMB_CLK_RESUME
7,17,22,23,29,31 SMB_DATA_RESUME
SA1 SA0
0 0
0 1
13 M_BS_A[2..0]
13 M_SCKE_A[3..0]
13 M_SCS_A1J
13 M_SCS_A0J
13 M_SCS_A3J
13 M_SCS_A2J
13 CK_M_200M_N_DDR0_A
13 CK_M_200M_P_DDR0_A
13 CK_M_200M_N_DDR2_A
13 CK_M_200M_P_DDR2_A
13 CK_M_200M_N_DDR3_A
13 CK_M_200M_P_DDR3_A
13 CK_M_200M_N_DDR5_A
13 CK_M_200M_P_DDR5_A
13 M_MAA_A[14..0]
13,17 DRAMRSTJ
13 M_CAS_AJ
13 M_RAS_AJ
13 M_WE_AJ
DELL INC.
Title
DDRIII Channel A DIMM 1, 3
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, June 02, 2010
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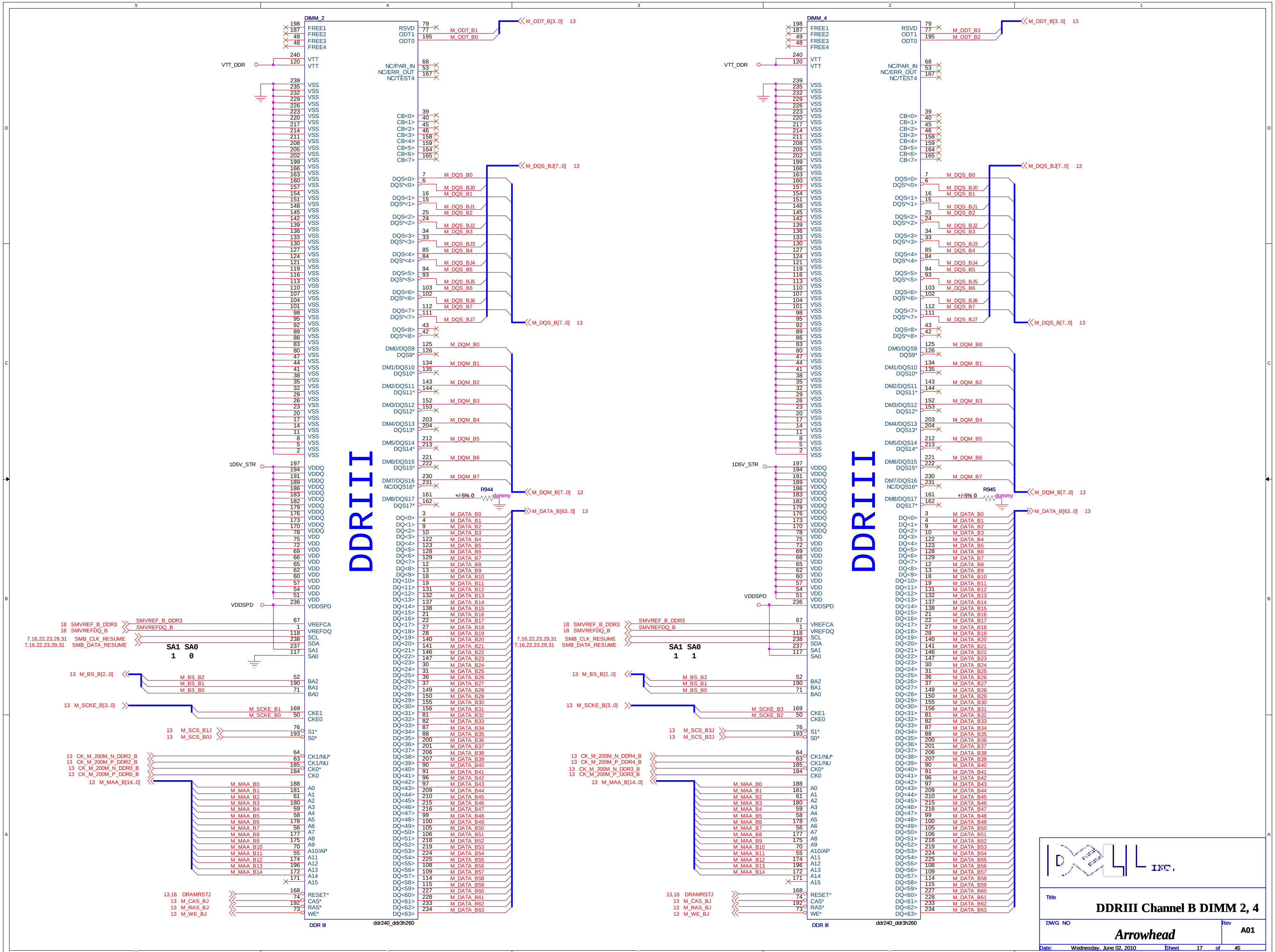
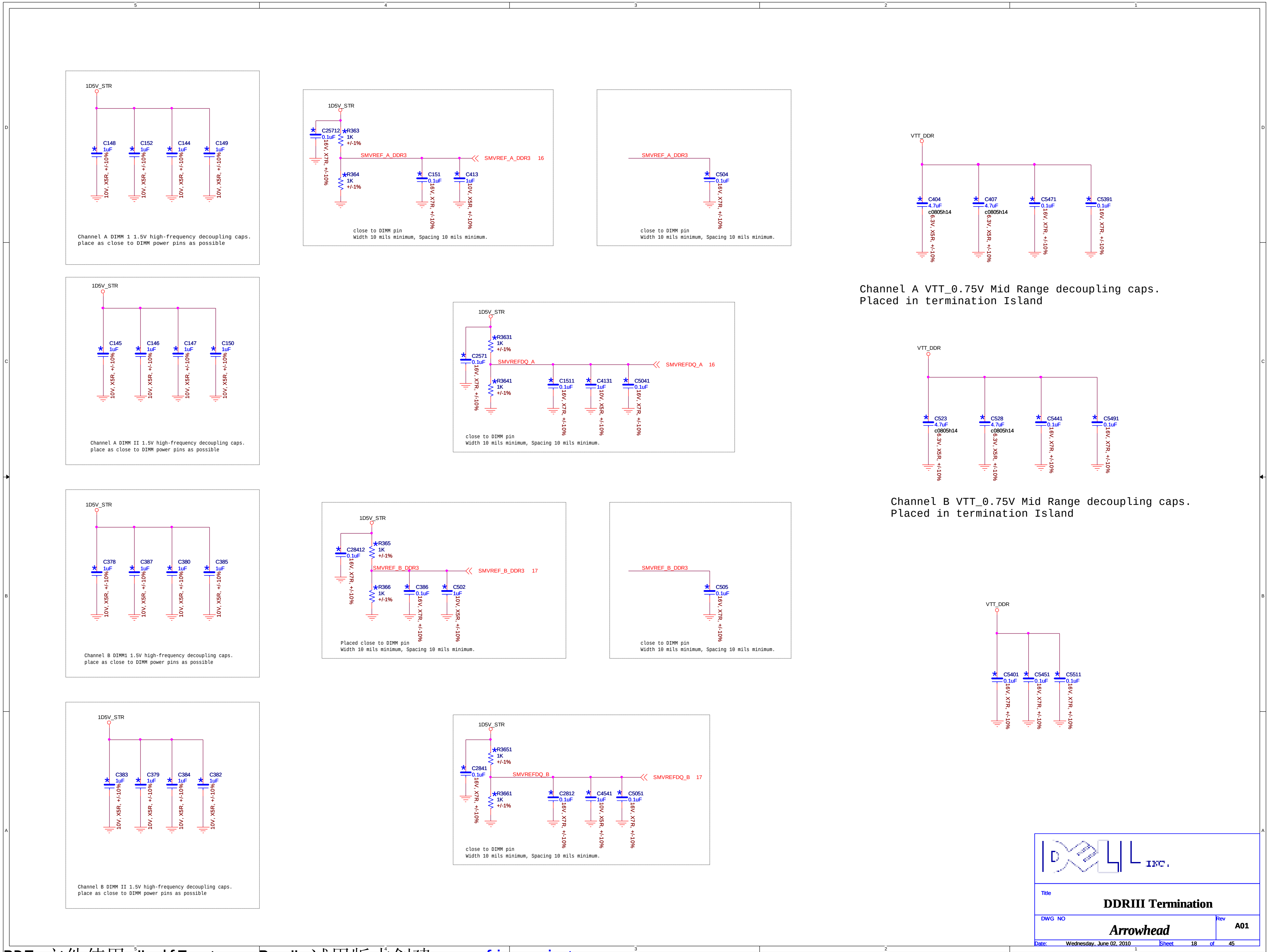

DIMM_2
DIMM_4
DDRIII
DDRIII
DDR III
ddr240_ddr3h260
VTT_DDR
1D5V_STR
VDDSPD
M_ODT_B[3..0]
M_DQS_BJ[7..0]
M_DQS_B[7..0]
M_DQM_B[7..0]
M_DATA_B[63..0]
SMVREF_B_DDR3
SMVREFDQ_B
SMB_CLK_RESUME
SMB_DATA_RESUME
SA1 SA0
1 0
1 1
M_BS_B[2..0]
M_SCKE_B[3..0]
M_SCS_B1J
M_SCS_B0J
M_SCS_B3J
M_SCS_B2J
CK_M_200M_N_DDR2_B
CK_M_200M_P_DDR2_B
CK_M_200M_N_DDR0_B
CK_M_200M_P_DDR0_B
CK_M_200M_N_DDR4_B
CK_M_200M_P_DDR4_B
CK_M_200M_N_DDR3_B
CK_M_200M_P_DDR3_B
M_MAA_B[14..0]
DRAMRSTJ
M_CAS_BJ
M_RAS_BJ
M_WE_BJ
R944
R945
+/-5% 0
dummy
DELL INC.
Title
DDRIII Channel B DIMM 2, 4
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, June 02, 2010
Sheet 17 of 45


1D5V_STR
Channel A DIMM 1 1.5V high-frequency decoupling caps.
place as close to DIMM power pins as possible
Channel A DIMM II 1.5V high-frequency decoupling caps.
place as close to DIMM power pins as possible
Channel B DIMM1 1.5V high-frequency decoupling caps.
place as close to DIMM power pins as possible
Channel B DIMM II 1.5V high-frequency decoupling caps.
place as close to DIMM power pins as possible
SMVREF_A_DDR3
SMVREF_B_DDR3
SMVREFDQ_A
SMVREFDQ_B
close to DIMM pin
Width 10 mils minimum, Spacing 10 mils minimum.
Placed close to DIMM pin
VTT_DDR
Channel A VTT_0.75V Mid Range decoupling caps.
Placed in termination Island
Channel B VTT_0.75V Mid Range decoupling caps.
Placed in termination Island
Title
DDRIII Termination
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, June 02, 2010
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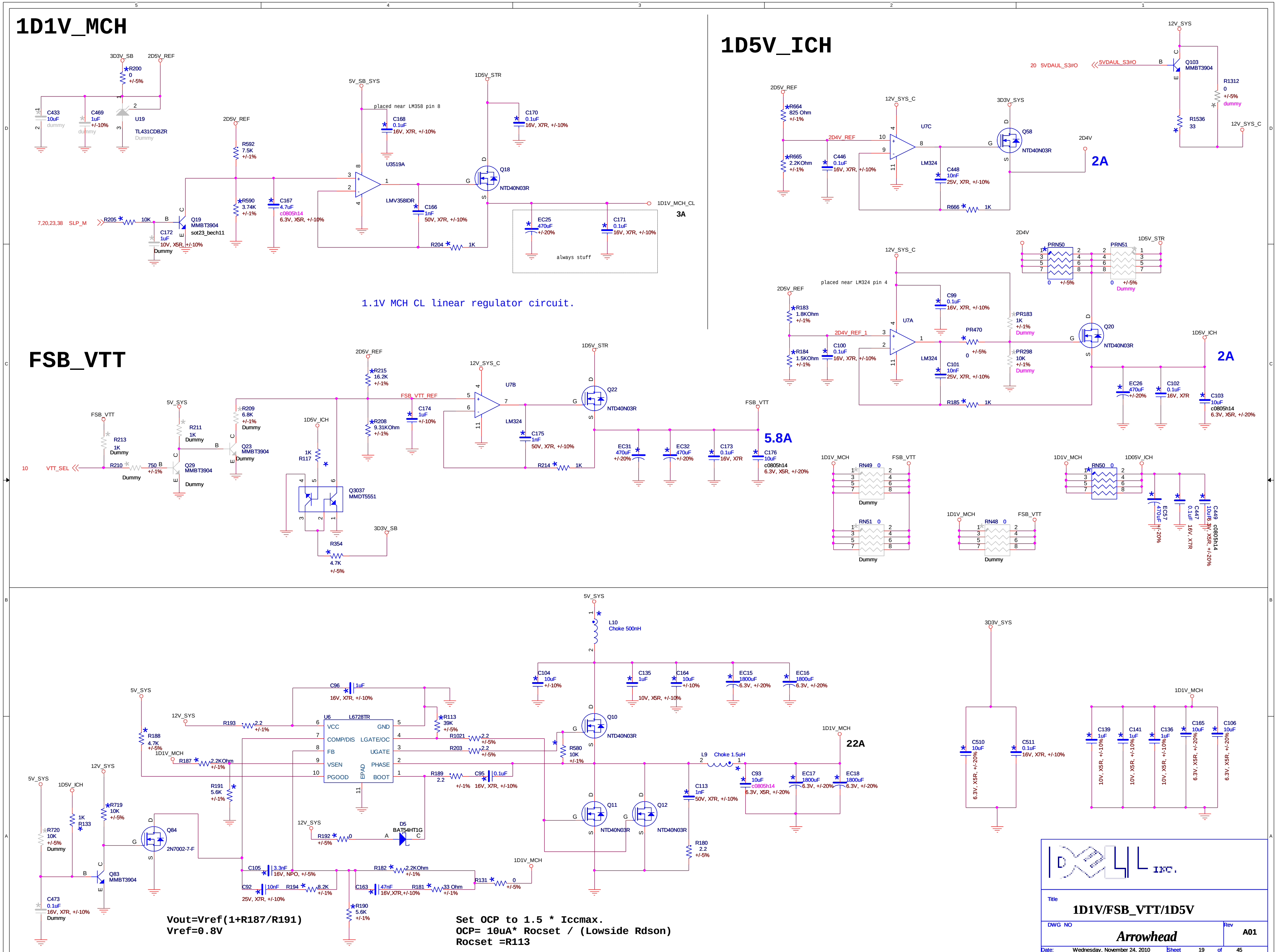

1D1V_MCH
1.1V MCH CL linear regulator circuit.
placed near LM358 pin 8
always stuff
3A
1D5V_ICH
2A
placed near LM324 pin 4
2A
FSB_VTT
5.8A
22A
Vout=Vref(1+R187/R191)
Vref=0.8V
Set OCP to 1.5 * Iccmax.
OCP= 10uA* Rocset / (Lowside Rdson)
Rocset =R113
Title
1D1V/FSB_VTT/1D5V
DWG NO
Arrowhead
Rev
A01
Date: Wednesday, November 24, 2010
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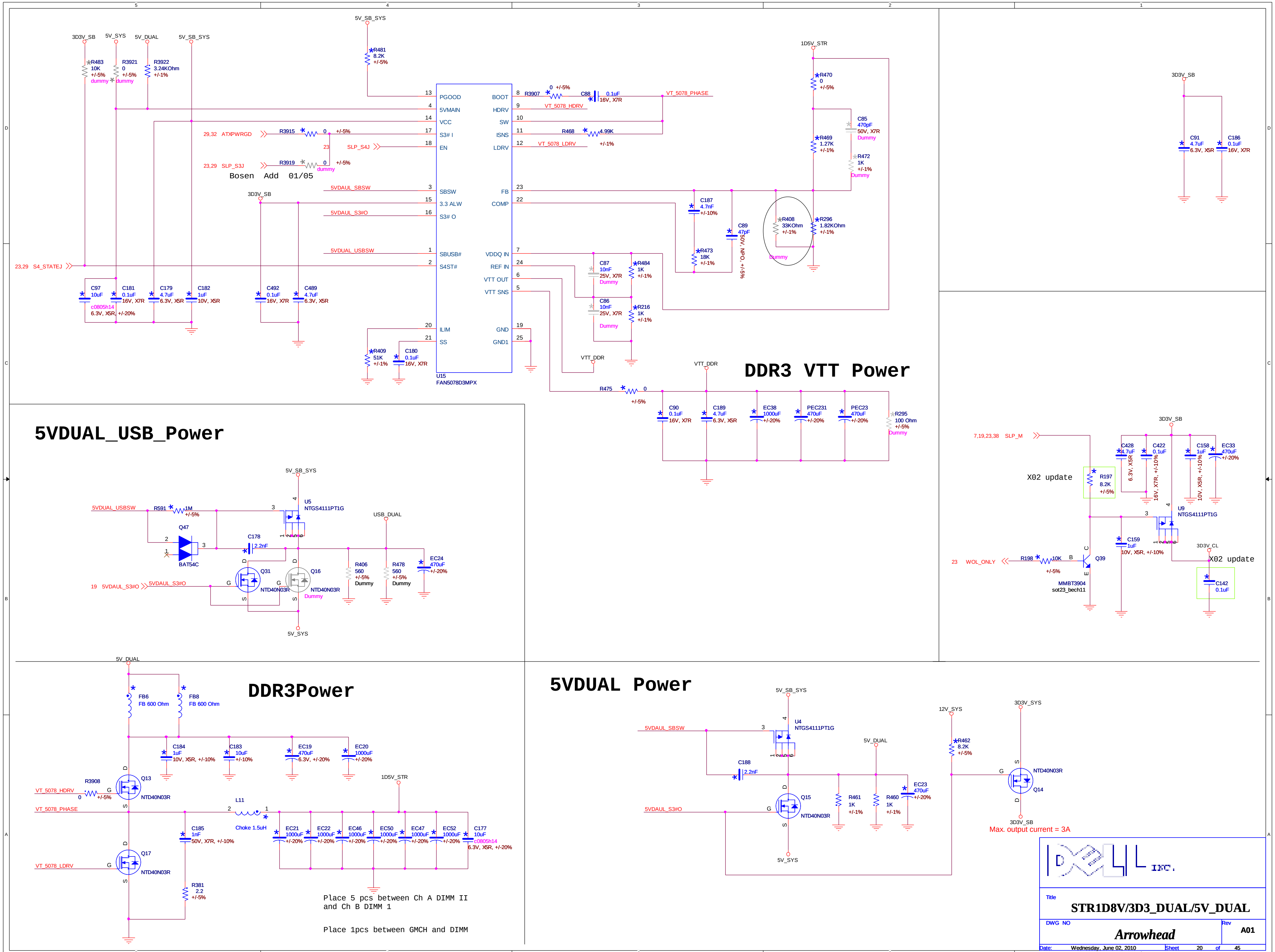
DDR3 VTT Power
5VDUAL_USB_Power
DDR3Power
5VDUAL Power
Bosen Add 01/05
X02 update
X02 update
U15
FAN5078D3MPX
PGOOD
5VMAIN
VCC
S3# I
EN
SBSW
3.3 ALW
S3# O
SBUSB#
S4ST#
ILIM
SS
BOOT
HDRV
SW
ISNS
LDRV
FB
COMP
VDDQ IN
REF IN
VTT OUT
VTT SNS
GND
GND1
VT_5078_PHASE
VT_5078_HDRV
VT_5078_LDRV
5VDUAL_SBSW
5VDUAL_S3#O
5VDUAL_USBSW
ATXPWRGD
SLP_S4J
SLP_S3J
S4_STATEJ
SLP_M
WOL_ONLY
NTGS4111PT1G
NTD40N03R
BAT54C
MMBT3904
Place 5 pcs between Ch A DIMM II
and Ch B DIMM 1
Place 1pcs between GMCH and DIMM
Max. output current = 3A
Title
STR1D8V/3D3_DUAL/5V_DUAL
DWG NO
Arrowhead
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A01
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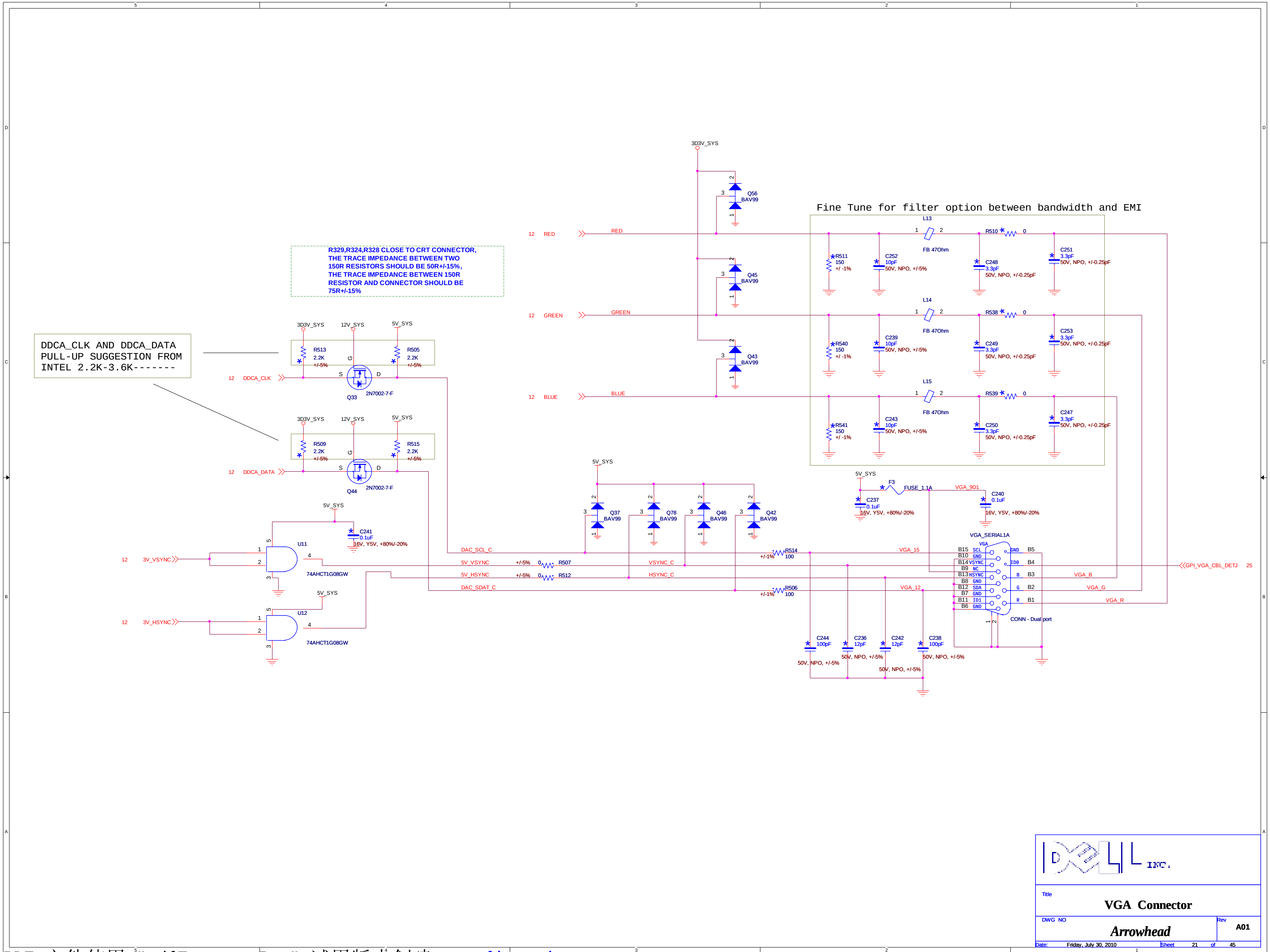
Fine Tune for filter option between bandwidth and EMI
R329,R324,R328 CLOSE TO CRT CONNECTOR,
THE TRACE IMPEDANCE BETWEEN TWO
150R RESISTORS SHOULD BE 50R+/-15%,
THE TRACE IMPEDANCE BETWEEN 150R
RESISTOR AND CONNECTOR SHOULD BE
75R+/-15%
DDCA_CLK AND DDCA_DATA
PULL-UP SUGGESTION FROM
INTEL 2.2K-3.6K-------
3D3V_SYS
12V_SYS
5V_SYS
RED
GREEN
BLUE
DDCA_CLK
DDCA_DATA
3V_VSYNC
3V_HSYNC
Q56 BAV99
Q45 BAV99
Q43 BAV99
Q37 BAV99
Q78 BAV99
Q46 BAV99
Q42 BAV99
Q33 2N7002-7-F
Q44 2N7002-7-F
R513 2.2K +/-5%
R505 2.2K +/-5%
R509 2.2K +/-5%
R515 2.2K +/-5%
U11 74AHCT1G08GW
U12 74AHCT1G08GW
C241 0.1uF 16V, Y5V, +80%/-20%
L13 FB 47Ohm
L14 FB 47Ohm
L15 FB 47Ohm
R510 0
R538 0
R539 0
R511 150 +/-1%
R540 150 +/-1%
R541 150 +/-1%
C252 10pF 50V, NPO, +/-5%
C239 10pF 50V, NPO, +/-5%
C243 10pF 50V, NPO, +/-5%
C248 3.3pF 50V, NPO, +/-0.25pF
C249 3.3pF 50V, NPO, +/-0.25pF
C250 3.3pF 50V, NPO, +/-0.25pF
C251 3.3pF 50V, NPO, +/-0.25pF
C253 3.3pF 50V, NPO, +/-0.25pF
C247 3.3pF 50V, NPO, +/-0.25pF
F3 FUSE_1.1A
VGA_9D1
C237 0.1uF 16V, Y5V, +80%/-20%
C240 0.1uF 16V, Y5V, +80%/-20%
VGA_SERIAL1A
CONN - Dual port
DAC_SCL_C
5V_VSYNC
5V_HSYNC
DAC_SDAT_C
R507 0 +/-5%
R512 0 +/-5%
VSYNC_C
HSYNC_C
R514 100 +/-1%
R506 100 +/-1%
VGA_15
VGA_12
VGA_B
VGA_G
VGA_R
GPI_VGA_CBL_DETJ 25
C244 100pF 50V, NPO, +/-5%
C236 12pF 50V, NPO, +/-5%
C242 12pF 50V, NPO, +/-5%
C238 100pF 50V, NPO, +/-5%
Title
VGA Connector
DWG NO
Arrowhead
Rev
A01
Date: Friday, July 30, 2010
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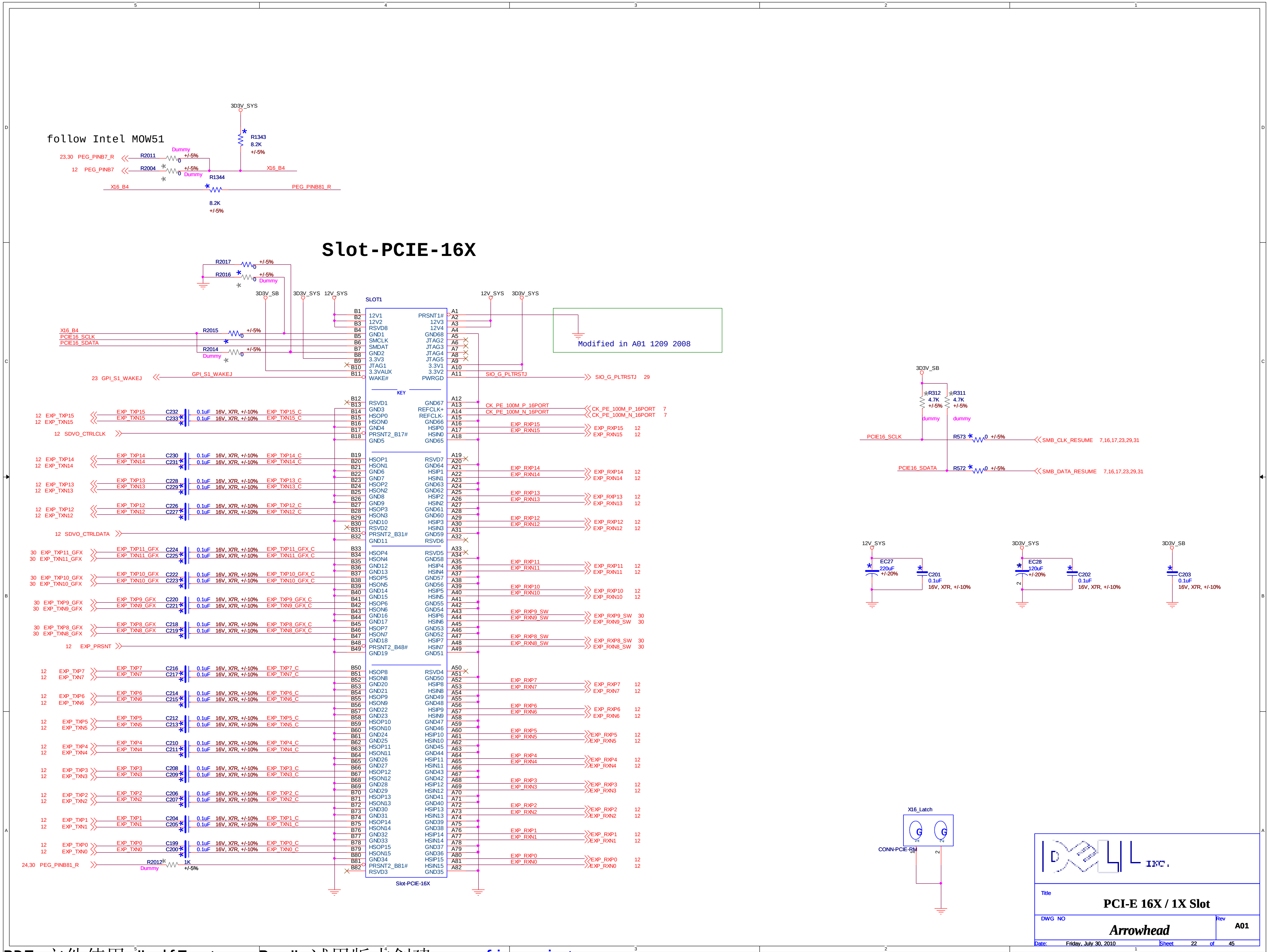
follow Intel MOW51
Slot-PCIE-16X
SLOT1
Modified in A01 1209 2008
Slot-PCIE-16X
X16_Latch
CONN-PCIE-RM
Title
PCI-E 16X / 1X Slot
DWG NO
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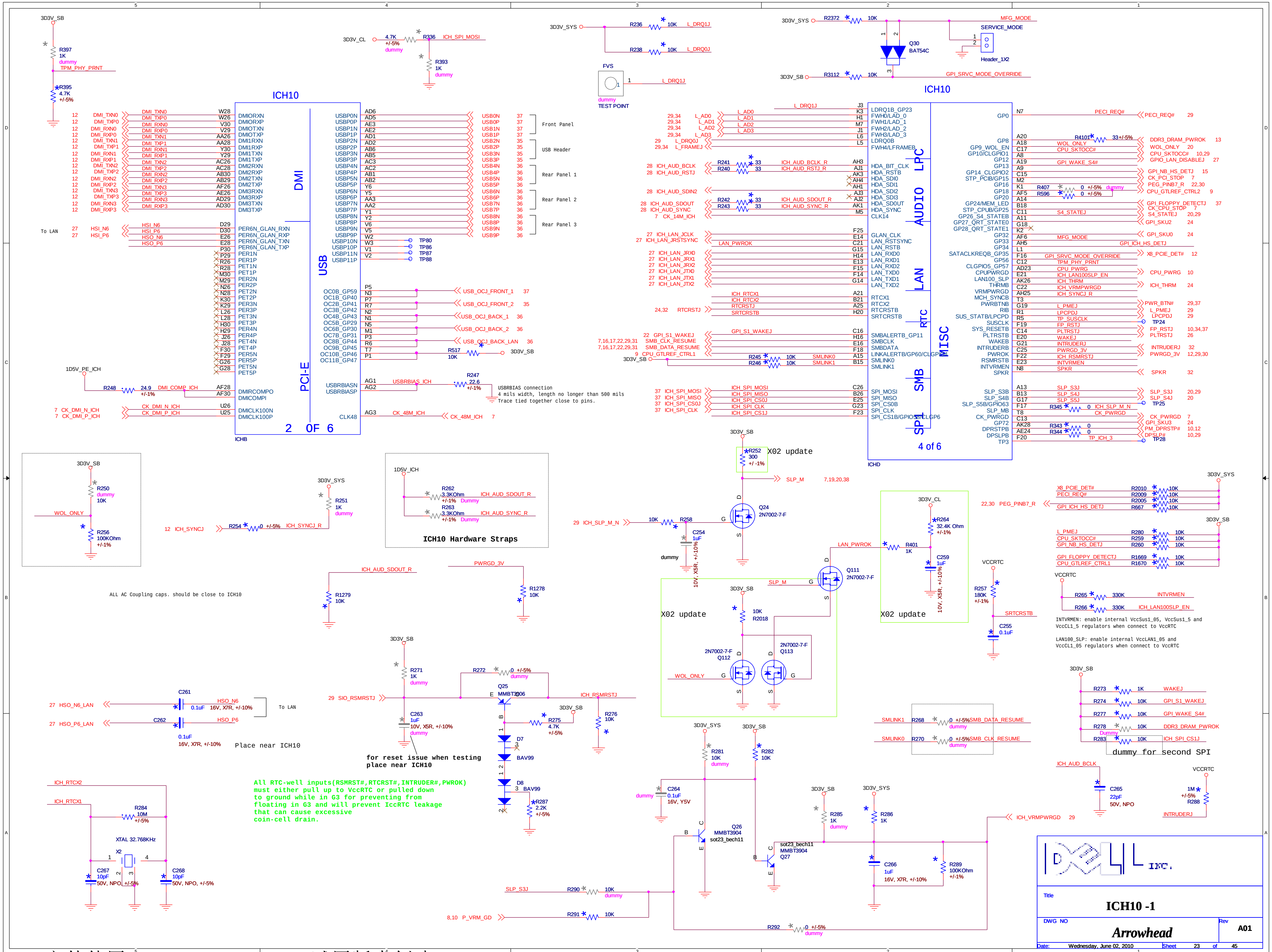

ICH10
DMI
USB
PCI-E
2 OF 6
LPC
AUDIO
LAN
RTC
MISC
SMB
SPI
4 of 6
Front Panel
USB Header
Rear Panel 1
Rear Panel 2
Rear Panel 3
To LAN
USBRBIAS connection
4 mils width, 22.6 no longer than 500 mils
Trace tied together close to pins.
ICH10 Hardware Straps
X02 update
ALL AC Coupling caps. should be close to ICH10
Place near ICH10
for reset issue when testing
place near ICH10
All RTC-well inputs(RSMRST#,RTCRST#,INTRUDER#,PWROK)
must either pull up to VccRTC or pulled down
to ground while in G3 for preventing from
floating in G3 and will prevent IccRTC leakage
that can cause excessive
coin-cell drain.
INTVRMEN: enable internal VccSus1_05, VccSus1_5 and
VccCL1_5 regulators when connect to VccRTC
LAN100_SLP: enable internal VccLAN1_05 and
VccCL1_05 regulators when connect to VccRTC
dummy for second SPI
SERVICE_MODE
Header_1X2
FVS
TEST POINT
XTAL 32.768KHz
Title
ICH10 -1
DWG NO
Arrowhead
Rev
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Date: Wednesday, June 02, 2010
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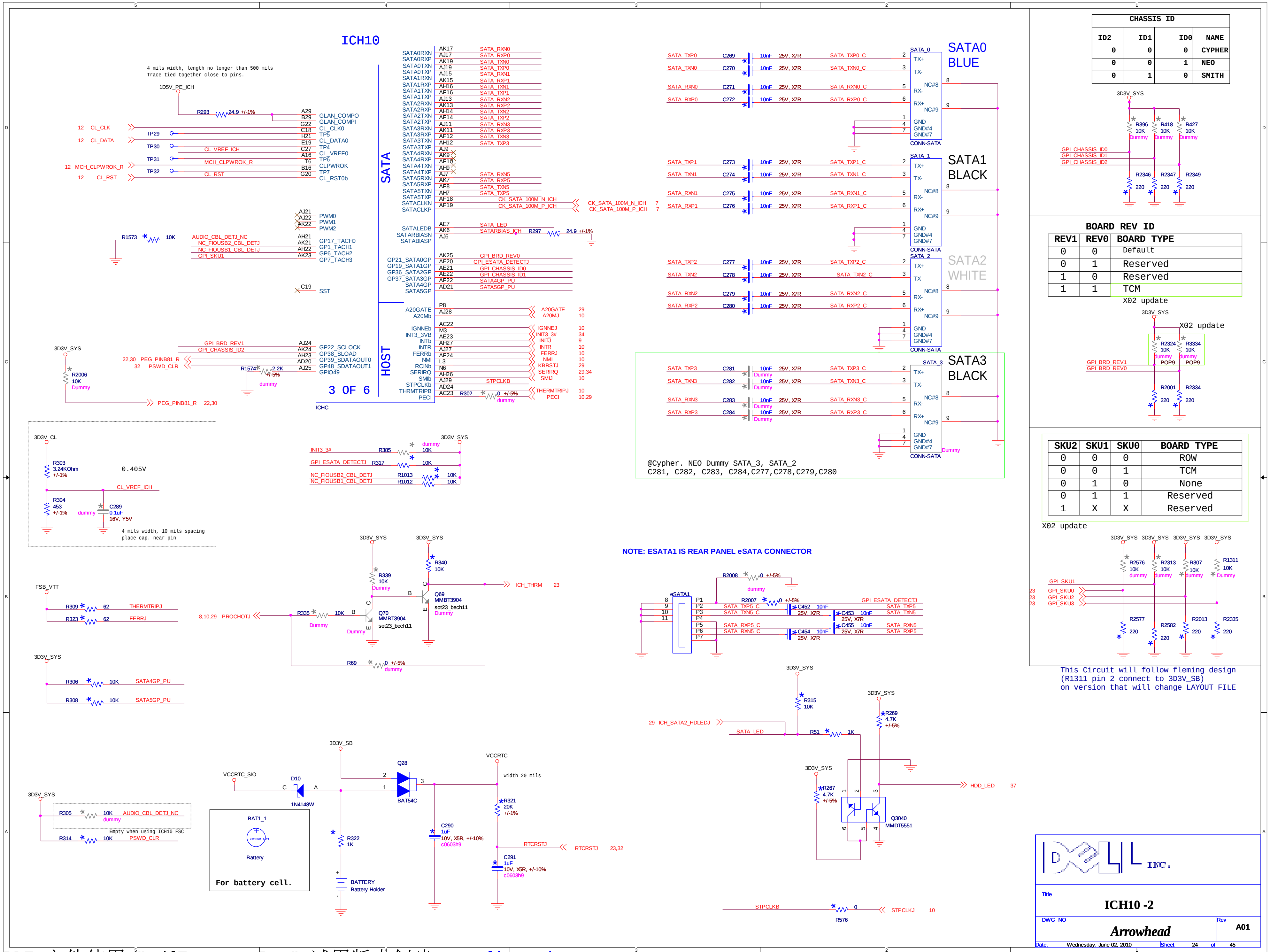

CHASSIS ID

ID2	ID1	ID0	NAME
0	0	0	CYPHER
0	0	1	NEO
0	1	0	SMITH

BOARD REV ID

REV1	REV0	BOARD TYPE
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	TCM

X02 update

SKU2	SKU1	SKU0	BOARD TYPE
0	0	0	ROW
0	0	1	TCM
0	1	0	None
0	1	1	Reserved
1	X	X	Reserved

X02 update

NOTE: ESATA1 IS REAR PANEL eSATA CONNECTOR

@Cypher. NEO Dummy SATA_3, SATA_2
C281, C282, C283, C284,C277,C278,C279,C280

This Circuit will follow fleming design
(R1311 pin 2 connect to 3D3V_SB)
on version that will change LAYOUT FILE

Title: ICH10 -2

DWG NO: Arrowhead   Rev: A01

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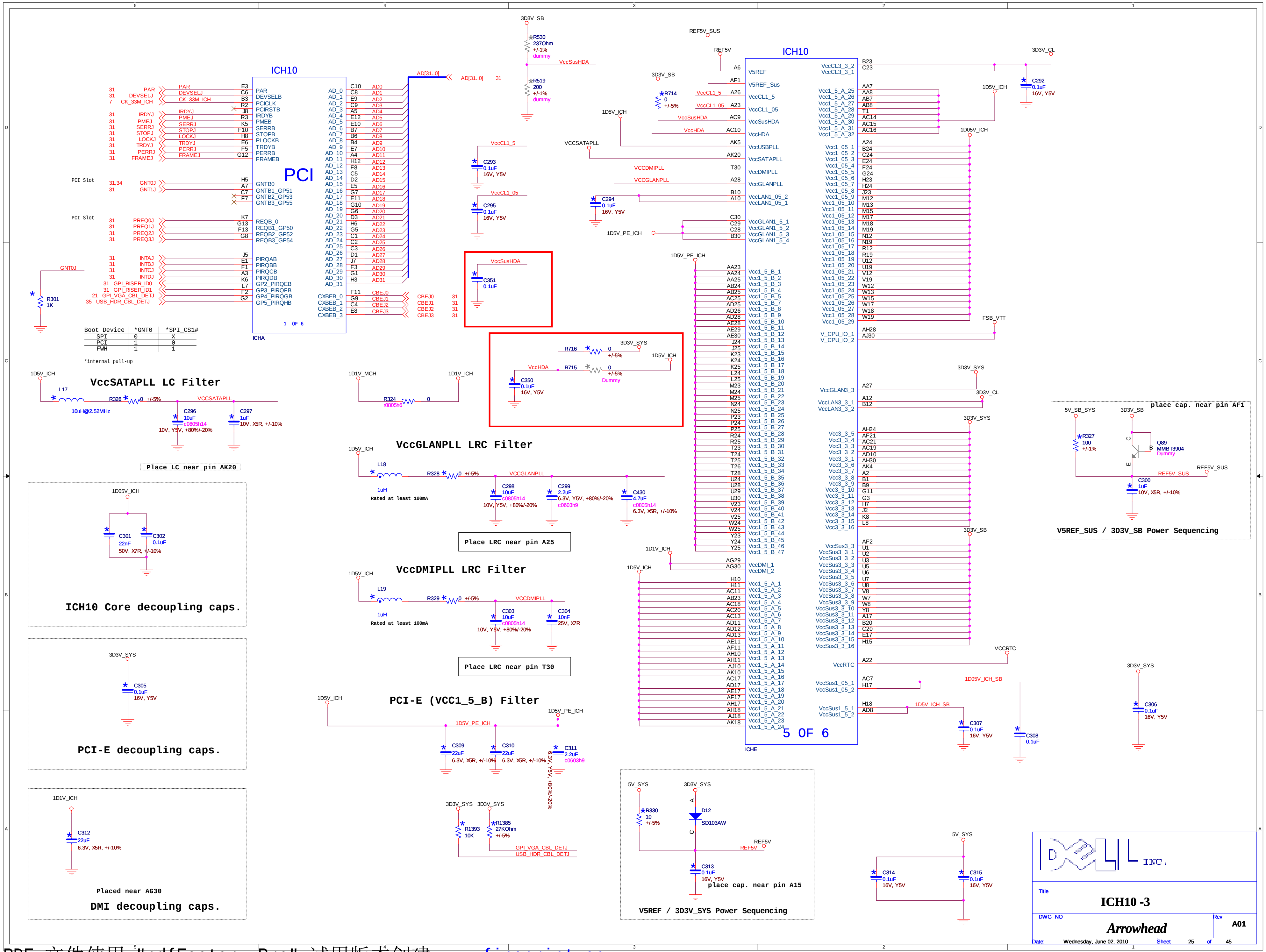
ICH10
PCI
1 OF 6
ICHA
Boot Device *GNT0 *SPI_CS1#
SPI 0 X
PCI 1 0
FWH 1 1
*internal pull-up
VccSATAPLL LC Filter
Place LC near pin AK20
ICH10 Core decoupling caps.
PCI-E decoupling caps.
Placed near AG30
DMI decoupling caps.
VccGLANPLL LRC Filter
Place LRC near pin A25
VccDMIPLL LRC Filter
Place LRC near pin T30
PCI-E (VCC1_5_B) Filter
Rated at least 100mA
ICH10
5 OF 6
ICHE
place cap. near pin AF1
V5REF_SUS / 3D3V_SB Power Sequencing
place cap. near pin A15
V5REF / 3D3V_SYS Power Sequencing
Title
ICH10 -3
DWG NO
Arrowhead
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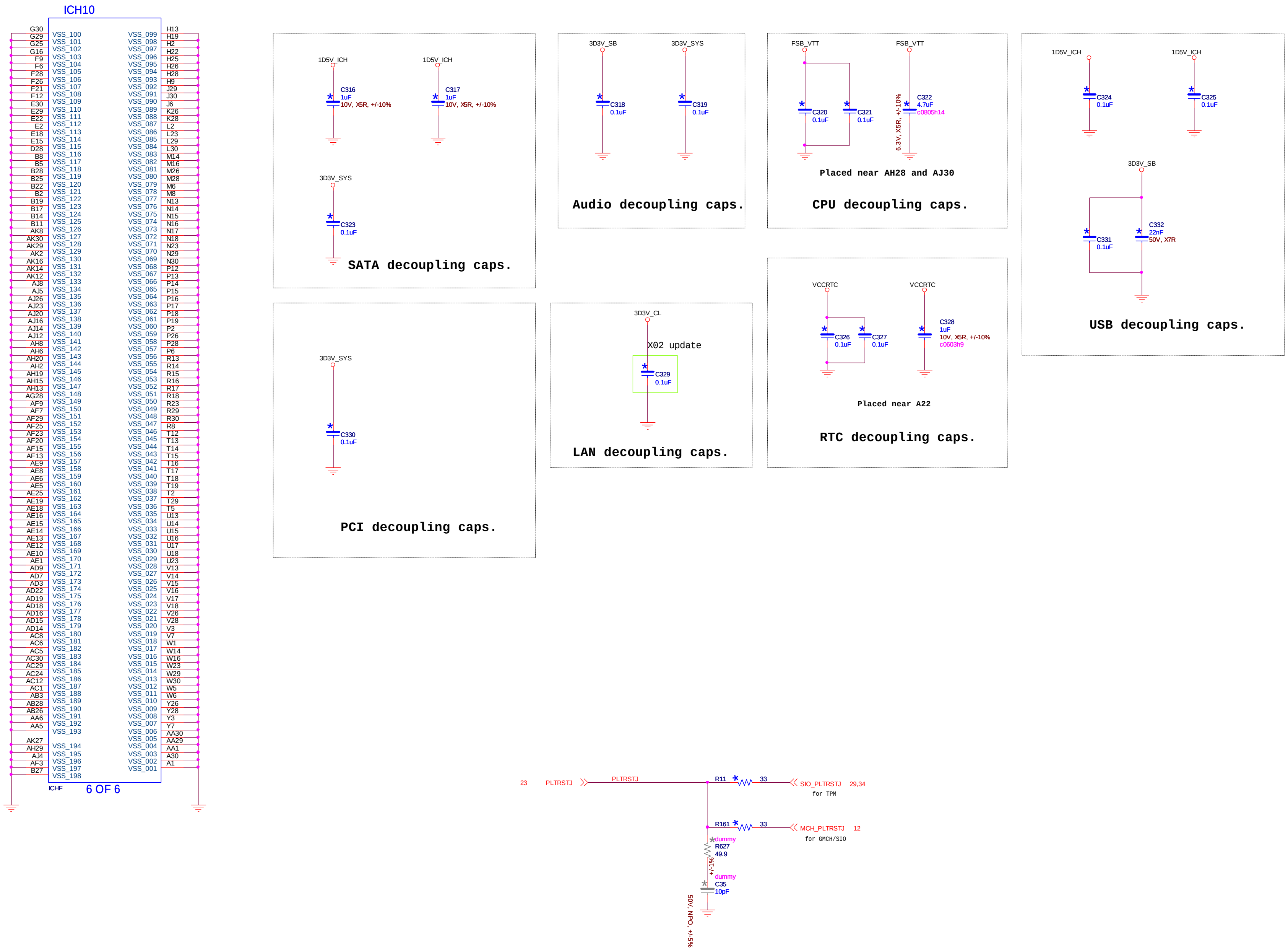

Title: ICH10 -4

DWG NO: Arrowhead

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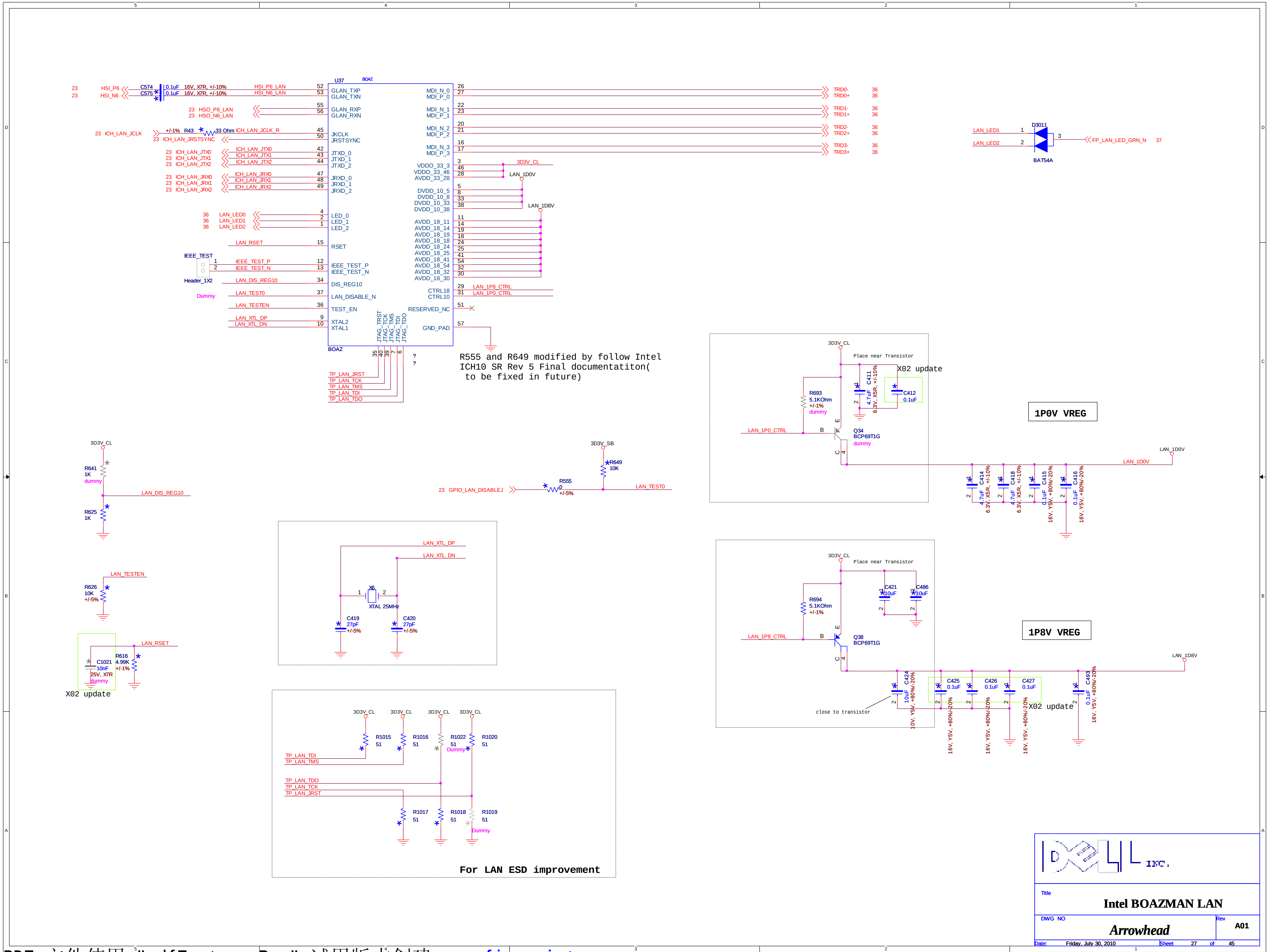

U37
BOAZ
GLAN_TXP
GLAN_TXN
GLAN_RXP
GLAN_RXN
JKCLK
JRSTSYNC
MDI_N_0
MDI_P_0
TRD0-
TRD0+
TRD1-
TRD1+
TRD2-
TRD2+
TRD3-
TRD3+
3D3V_CL
LAN_1D0V
LAN_1D8V
RSET
IEEE_TEST
Header_1X2
DIS_REG10
LAN_DISABLE_N
TEST_EN
XTAL2
XTAL1
GND_PAD
RESERVED_NC
CTRL18
CTRL10
D3011
BAT54A
FP_LAN_LED_GRN_N
R555 and R649 modified by follow Intel ICH10 SR Rev 5 Final documentatiton(to be fixed in future)
Place near Transistor
X02 update
1P0V VREG
1P8V VREG
Q34
BCP69T1G
Q38
BCP69T1G
close to transistor
XTAL 25MHz
For LAN ESD improvement
Title
Intel BOAZMAN LAN
DWG NO
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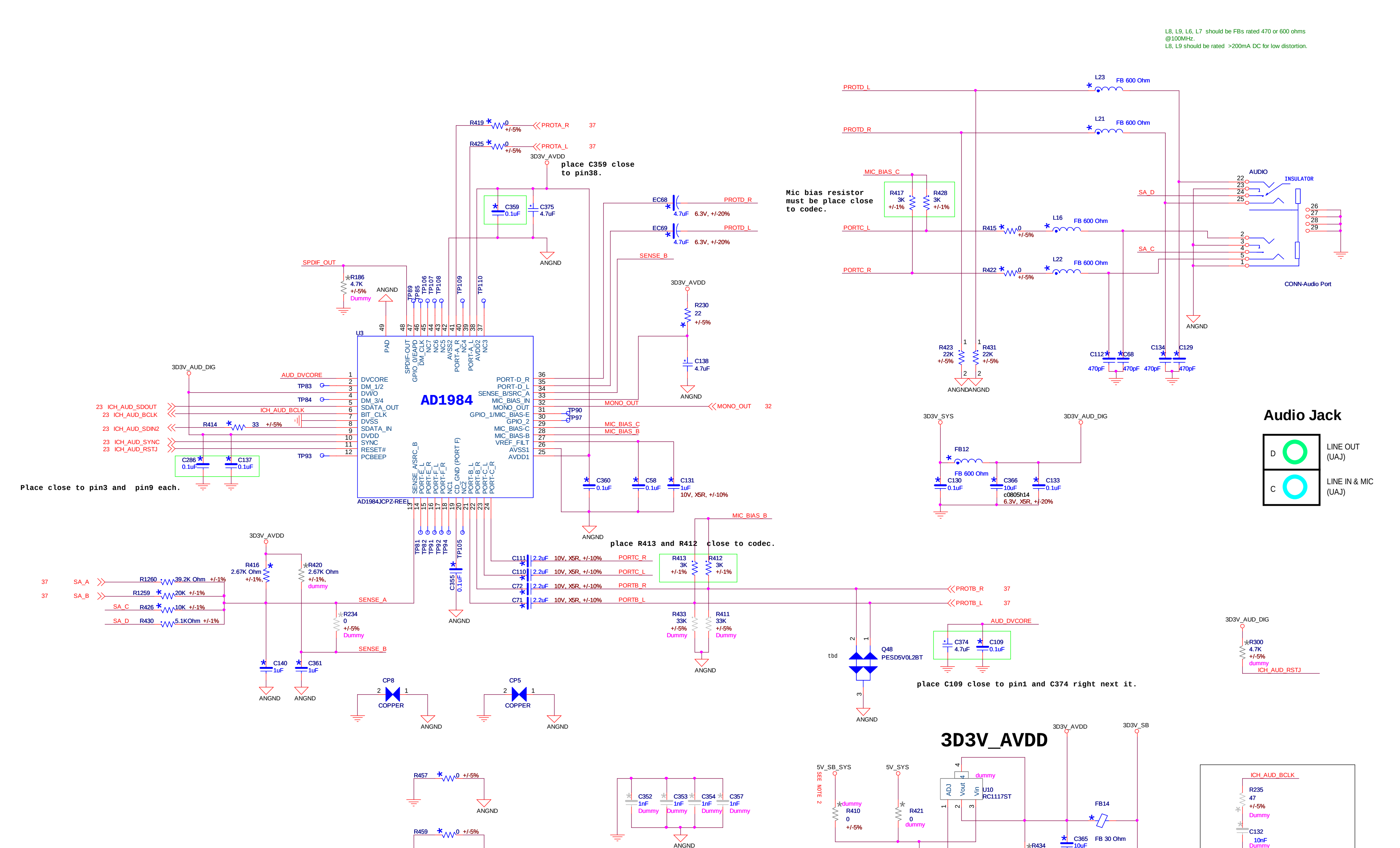

NOTE 1.
AVDD must be +3.3V +/- 5%.
For best audio performance and low noise, use a linear voltage regulator such as LM1117 or AME8800A.
NOTE 2.
The regulator can be powered from +12V or +5V (if using LDO type like LM1117 or AME8800A).
For reduced power ON/OFF pop, suggest installing option to power LDO type regulator from +5V_STBY.
NOTE 3.
R19 option is for higher MIC bias voltage compliance (normally not required).
and is exclusive of R5.
NOTE 4.
L1 and L2 should be rated 300mA or higher (for low THD+N).
NOTE 5
Systems with 2 rear jacks must only implement J1A and J1-B jacks.
In this configuration MIC jack is retaskable as LINE_IN.
Also change R10 and R19 to 150 ohms.
NOTE 6.
Systems with 3 rear jacks must implement J1-A, J1-B and also J1-C as the LINE_IN jack.
In this configuration J1-B functions as MIC input only.

Layout Note

1. Use double via close to pin 7 and directly to DGND plane.
2. place C18 close to pin1 and C38 right next it.
3. place c19 close to pin3.
4. place C21 close to pin9.
5. Place a couple of stitch caps(C30,C31,C32,C33) very close to audio jacks.
6. C4 close to pin38.

Title: HDA Codec AD1984

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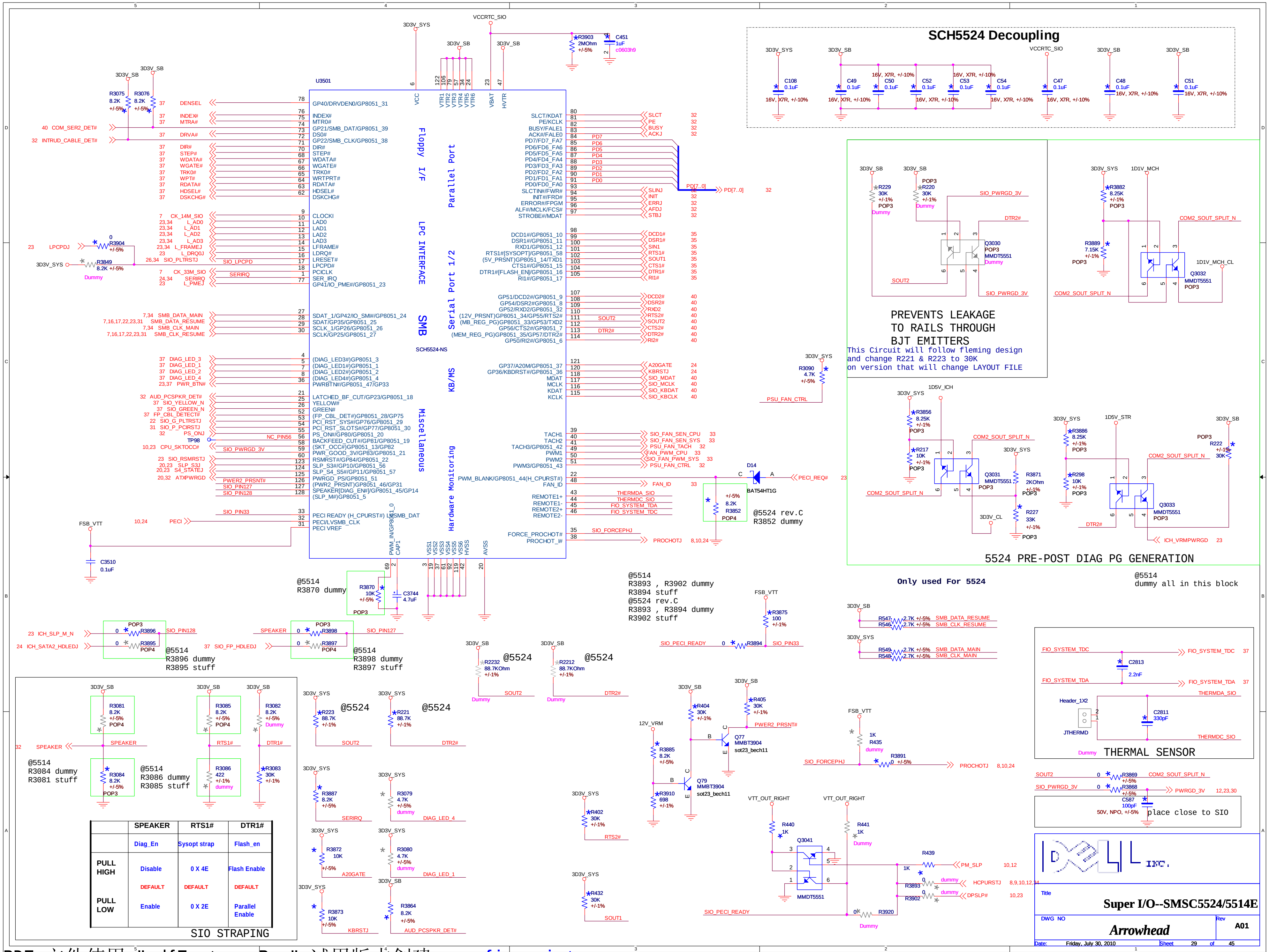
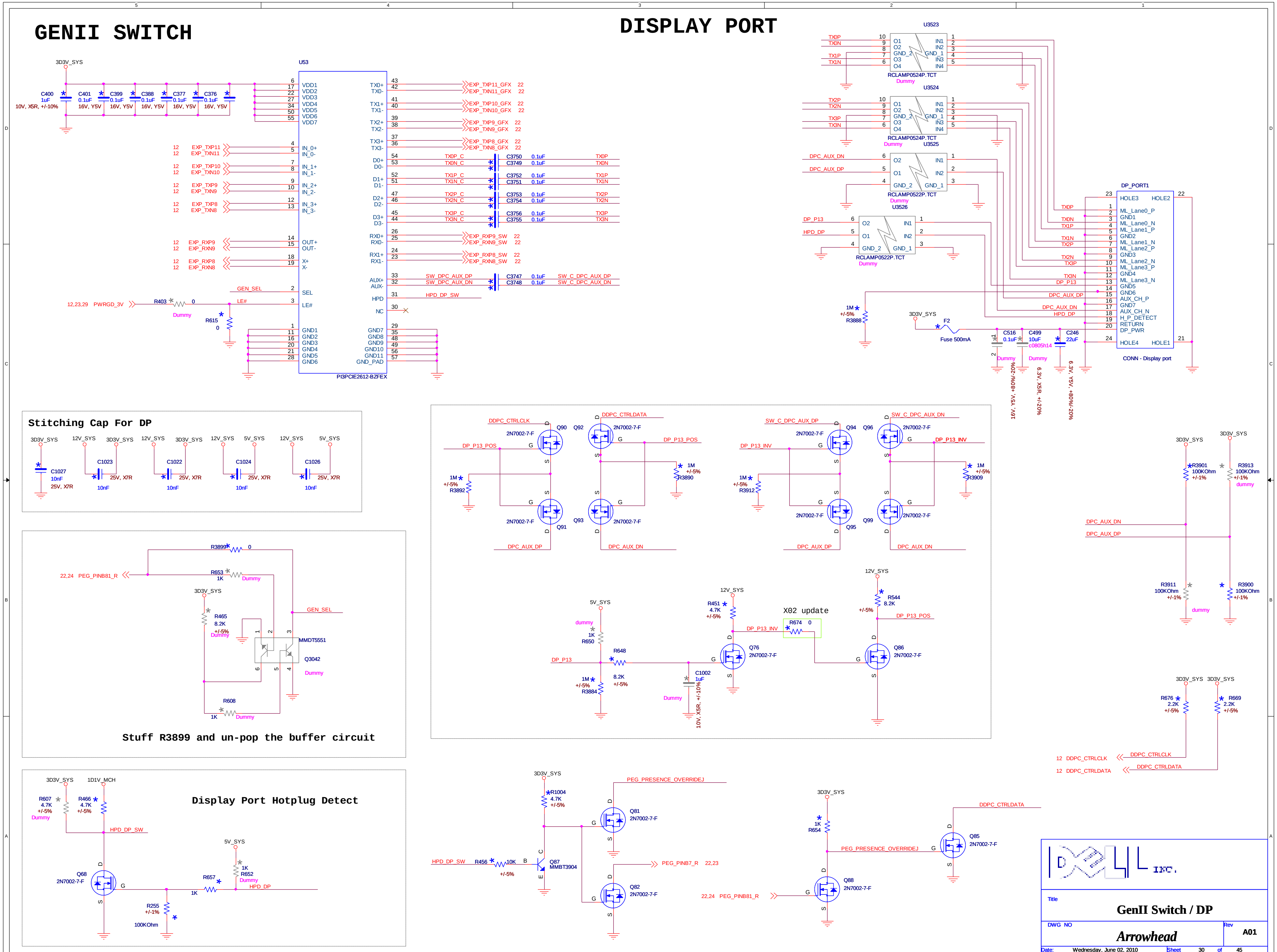


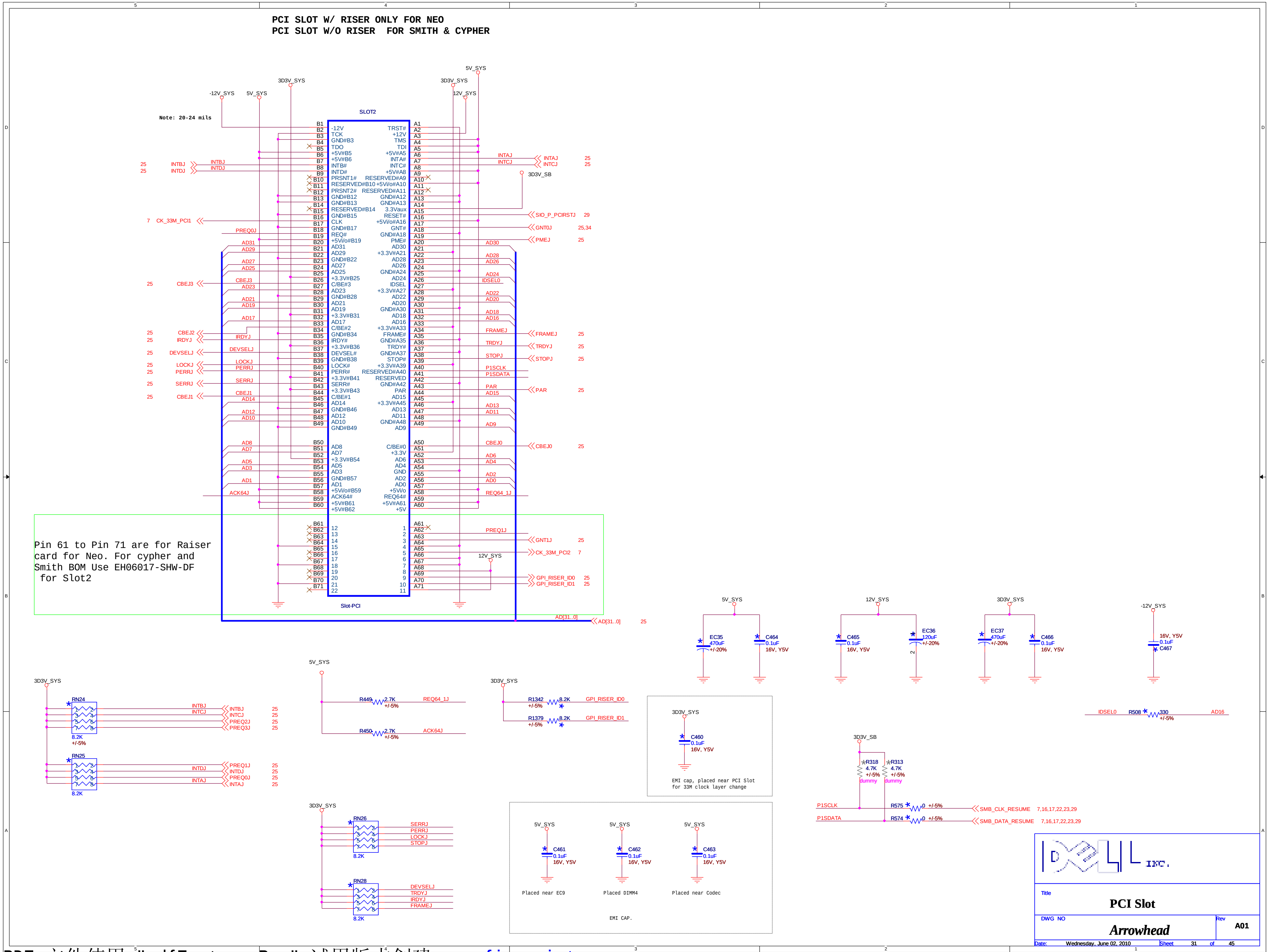
SIO STRAPING

	SPEAKER	RTS1#	DTR1#
	Diag_En	Sysopt strap	Flash_en
PULL HIGH	Disable DEFAULT	0 X 4E DEFAULT	Flash Enable DEFAULT
PULL LOW	Enable	0 X 2E	Parallel Enable

GENII SWITCH

DISPLAY PORT




PCI SLOT W/ RISER ONLY FOR NEO
PCI SLOT W/O RISER FOR SMITH & CYPHER
Note: 20-24 mils
SLOT2
Slot-PCI
Pin 61 to Pin 71 are for Raiser card for Neo. For cypher and Smith BOM Use EH06017-SHW-DF for Slot2
EMI cap, placed near PCI Slot for 33M clock layer change
Placed near EC9
Placed DIMM4
Placed near Codec
EMI CAP.
Title
PCI Slot
DWG NO
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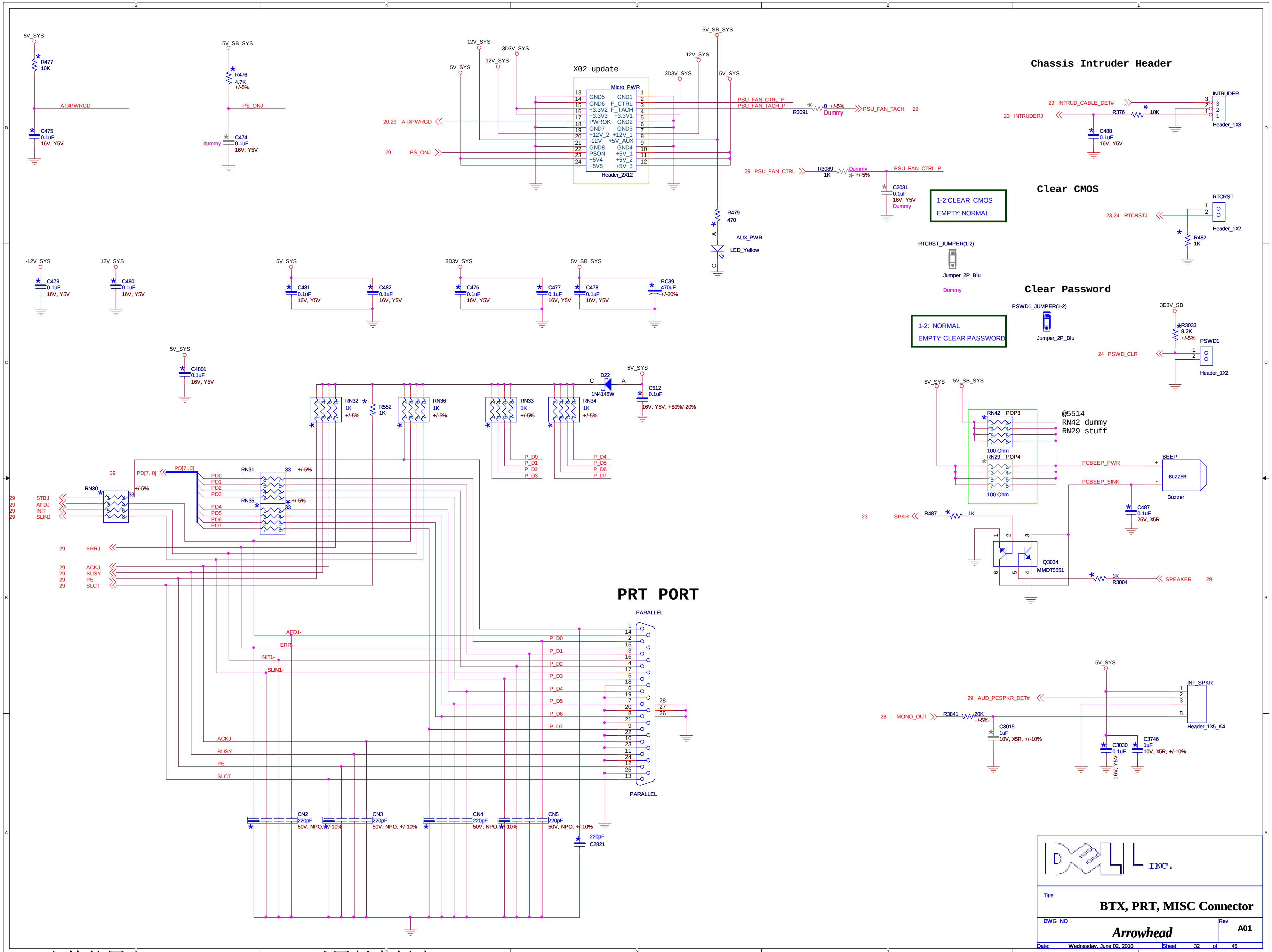

Title
BTX, PRT, MISC Connector

DWG NO
Arrowhead
Rev A01

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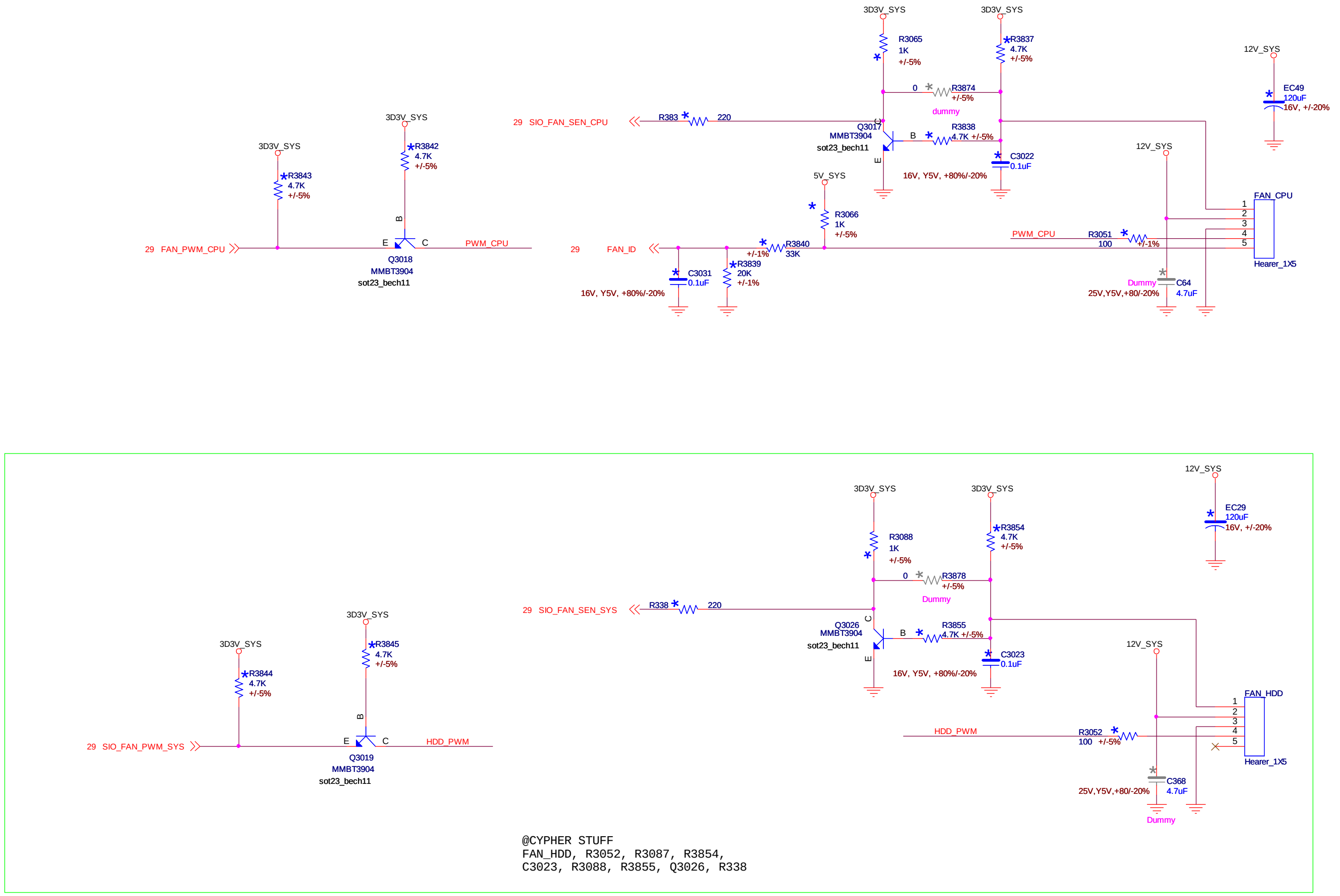

DELL INC.

Title

CPU / System Fan

DWG NO	Rev
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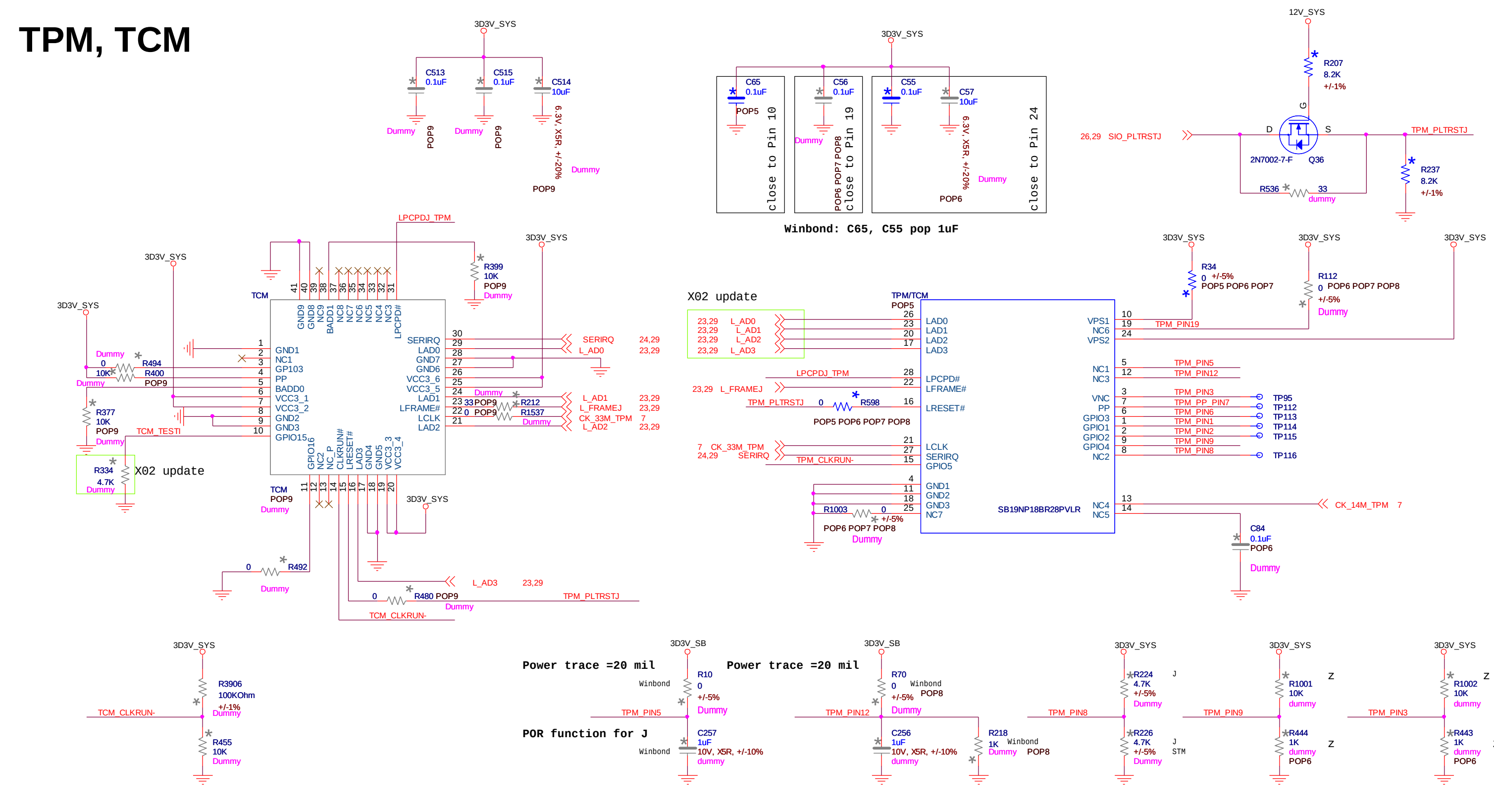
TPM, TCM



Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default set EE/EF as Amy recommended,
Pin 3 and Pin 9 have internal PU in Z.

J

STATUS	TESTEN PIN8	RUNMODES PIN9
NORMAL MODE	0	X
JTAG MODE	1	0
NORMAL MODE	1	1

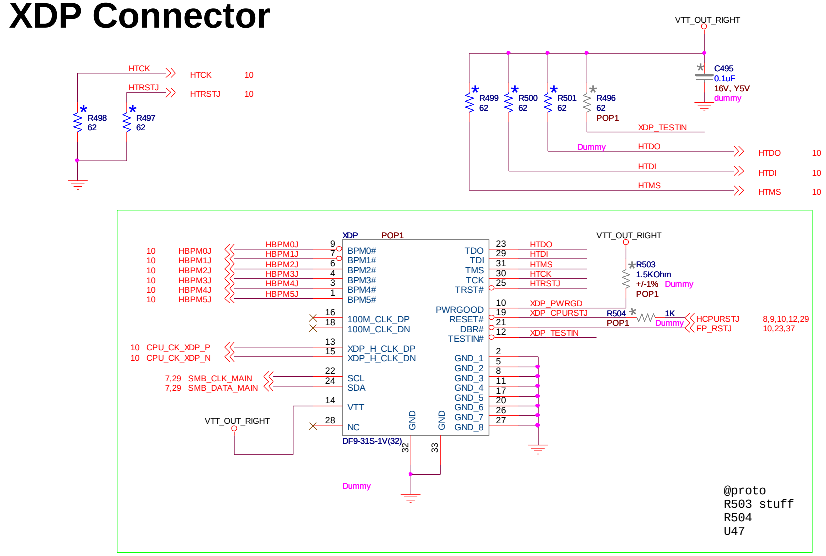
J has internal PD with PIN8,
internal PU with PIN9

J

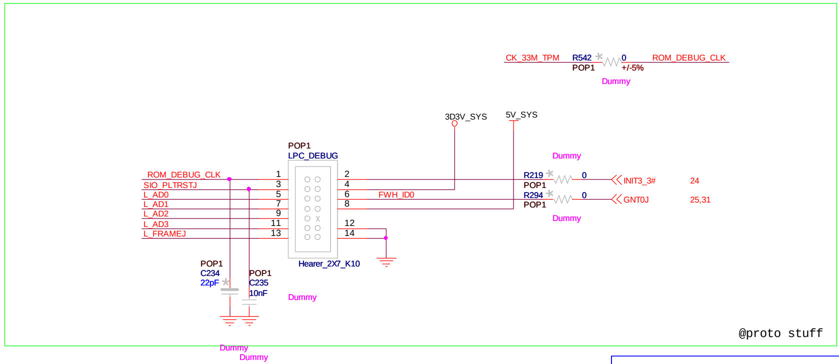
	1(default)	0
BSEL PIN12	FLASH	SRAM

J has internal PU with PIN12

XDP Connector



LPC DEBUG



Title: KB/MS, TPM, XDP,LPC CONN.

DWG NO: Arrowhead

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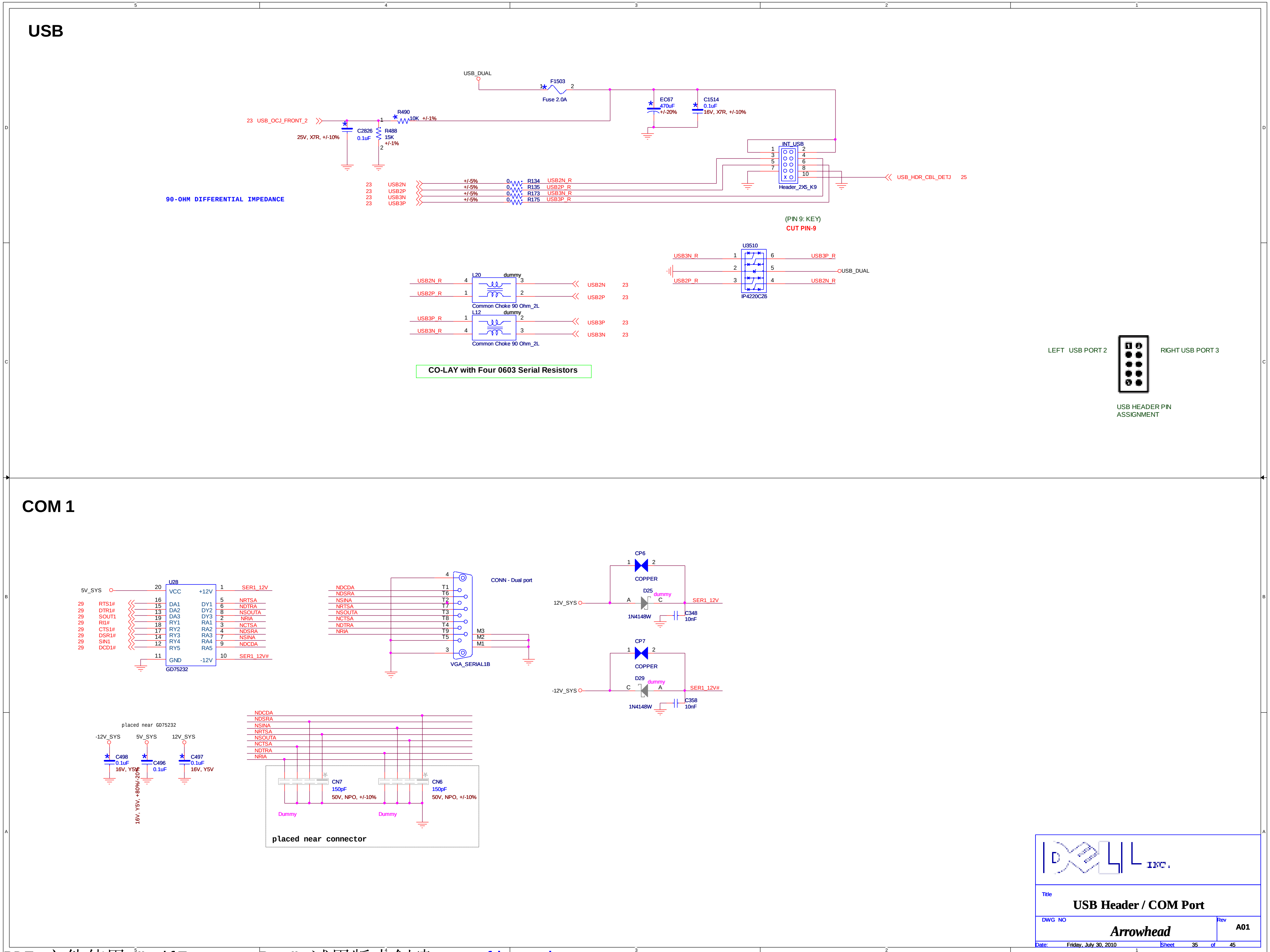

Title

USB Header / COM Port

DWG NO

Arrowhead

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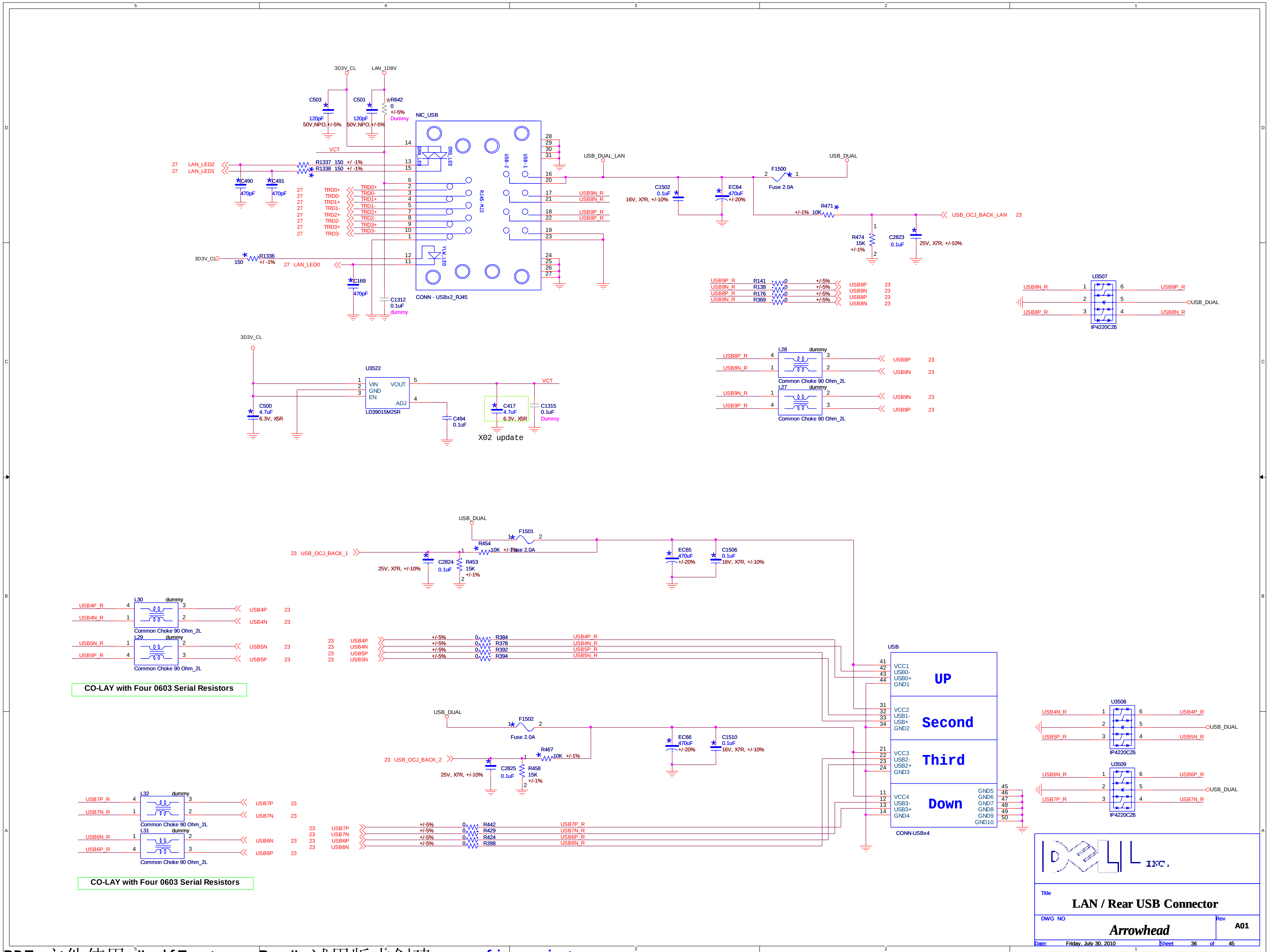
NIC_USB
CONN - USBx2_RJ45
RJ45-M12
USB-1
USB-2
GRN_LED
ORG_LED
YLW_LED
3D3V_CL
LAN_1D8V
VCT
LAN_LED2
LAN_LED1
LAN_LED0
TRD0+
TRD0-
TRD1+
TRD1-
TRD2+
TRD2-
TRD3+
TRD3-
USB_DUAL_LAN
USB_DUAL
F1500
Fuse 2.0A
USB_OCJ_BACK_LAN
USB9N_R
USB8N_R
USB9P_R
USB8P_R
U3507
IP4220CZ6
U3522
LD39015M25R
VIN
GND
EN
VOUT
ADJ
X02 update
L28
L27
dummy
Common Choke 90 Ohm_2L
USB_OCJ_BACK_1
USB_OCJ_BACK_2
F1501
F1502
L30
L29
L32
L31
CO-LAY with Four 0603 Serial Resistors
USB
UP
Second
Third
Down
CONN-USBx4
U3508
U3509
Title
LAN / Rear USB Connector
DWG NO
Arrowhead
Rev
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Date: Friday, July 30, 2010
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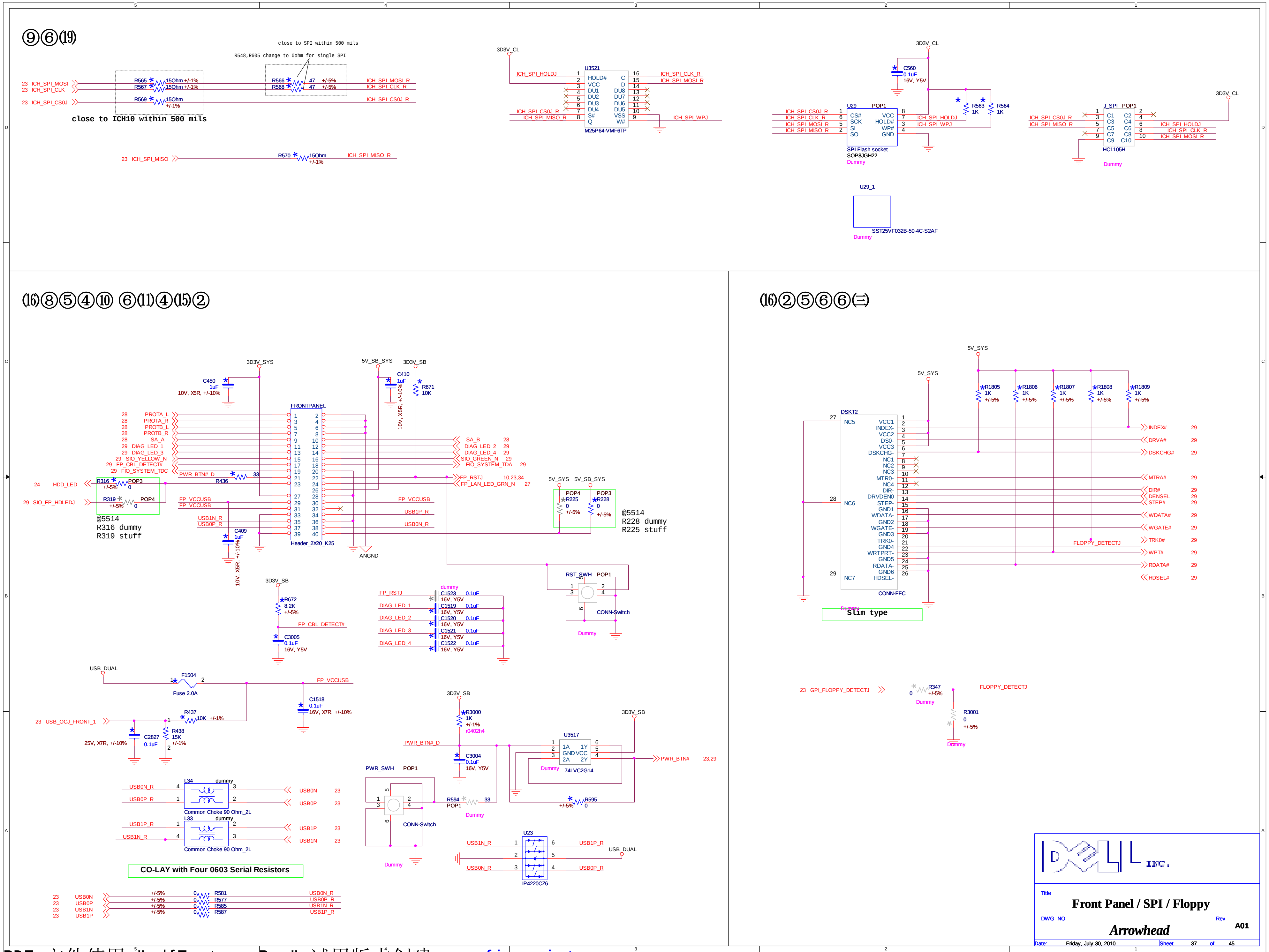
close to SPI within 500 mils
R548,R605 change to 0ohm for single SPI
close to ICH10 within 500 mils
ICH_SPI_MOSI
ICH_SPI_CLK
ICH_SPI_CS0J
ICH_SPI_MISO
U3521
M25P64-VMF6TP
U29
SPI Flash socket
SOP8JGH22
Dummy
J_SPI
HC1105H
U29_1
SST25VF032B-50-4C-S2AF
FRONTPANEL
Header_2X20_K25
@5514
R316 dummy
R319 stuff
@5514
R228 dummy
R225 stuff
RST_SWH
CONN-Switch
PWR_SWH
74LVC2G14
IP4220CZ6
Common Choke 90 Ohm_2L
CO-LAY with Four 0603 Serial Resistors
DSKT2
CONN-FFC
Slim type
FLOPPY_DETECTJ
Title
Front Panel / SPI / Floppy
DWG NO
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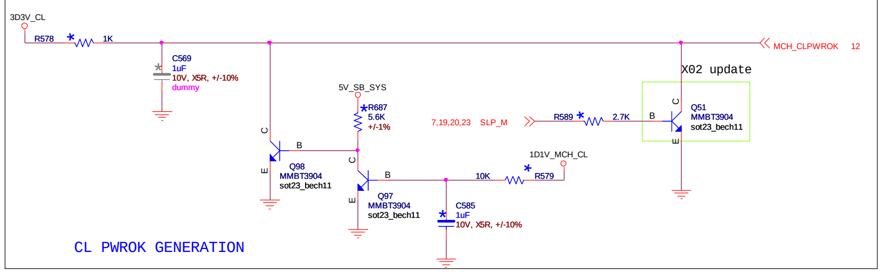
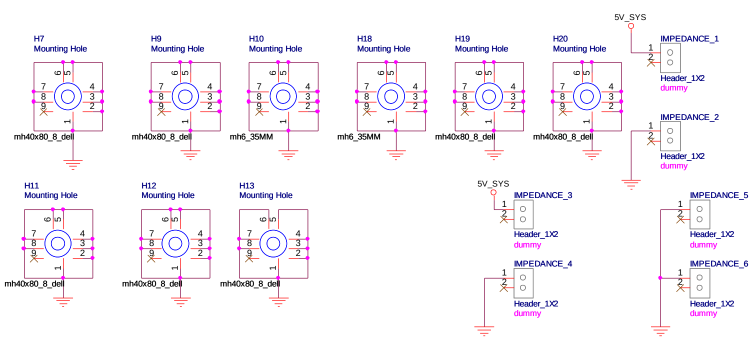
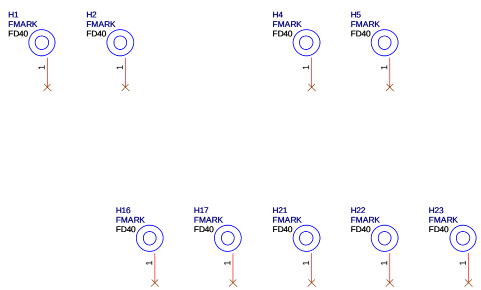
Stuff for AMT







DELL INC.

Title: Reserved-1

DWG NO: Arrowhead

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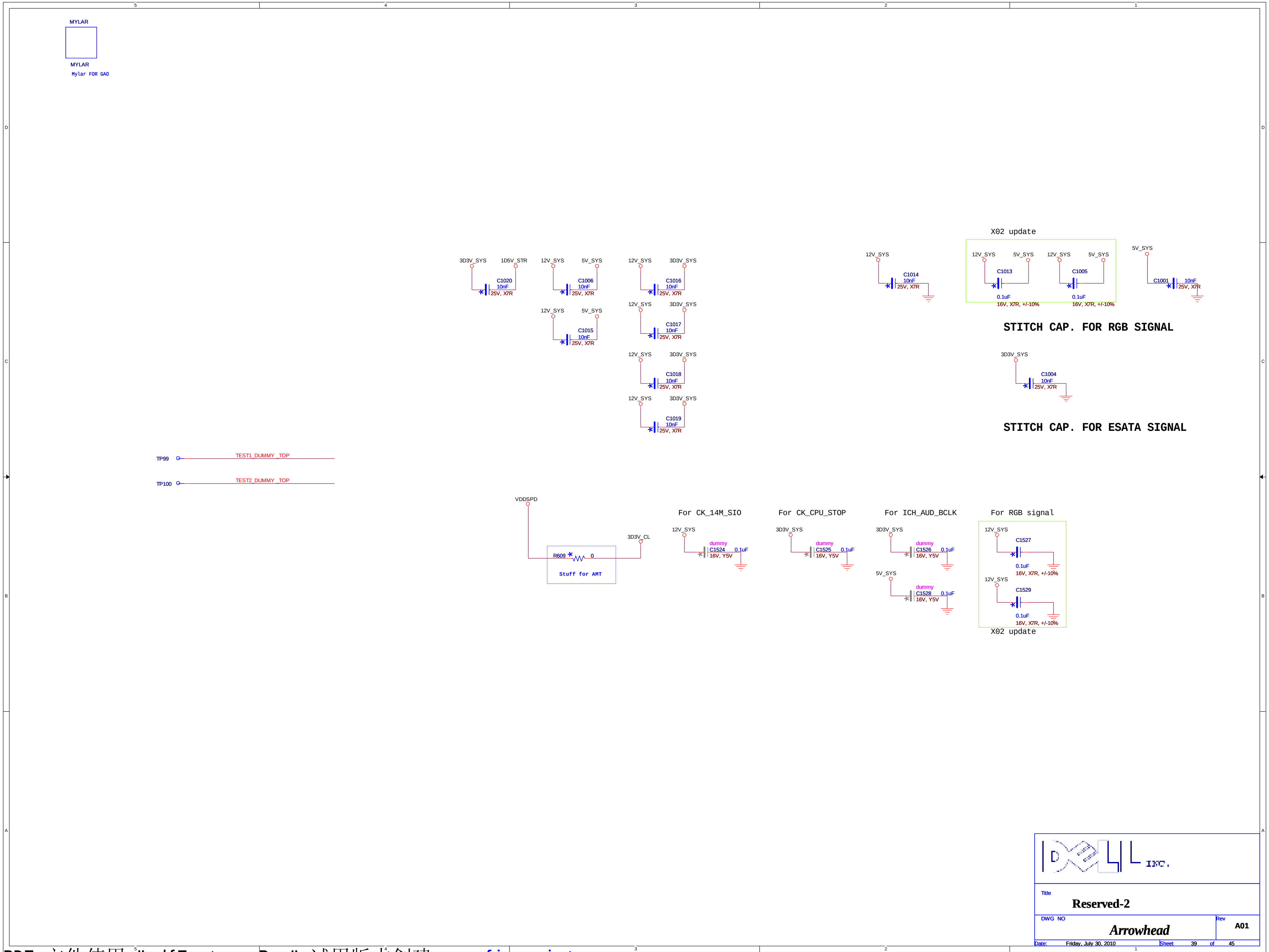
MYLAR
MYLAR
Mylar FOR GAO
X02 update
STITCH CAP. FOR RGB SIGNAL
STITCH CAP. FOR ESATA SIGNAL
3D3V_SYS
1D5V_STR
C1020
10nF
25V, X7R
12V_SYS
5V_SYS
C1006
C1015
C1016
C1017
C1018
C1019
C1014
C1013
C1005
C1001
C1004
0.1uF
16V, X7R, +/-10%
TP99
TEST1_DUMMY_TOP
TP100
TEST2_DUMMY_TOP
VDDSPD
3D3V_CL
R609
0
Stuff for AMT
For CK_14M_SIO
For CK_CPU_STOP
For ICH_AUD_BCLK
For RGB signal
dummy
C1524
C1525
C1526
C1528
C1527
C1529
16V, Y5V
Title
Reserved-2
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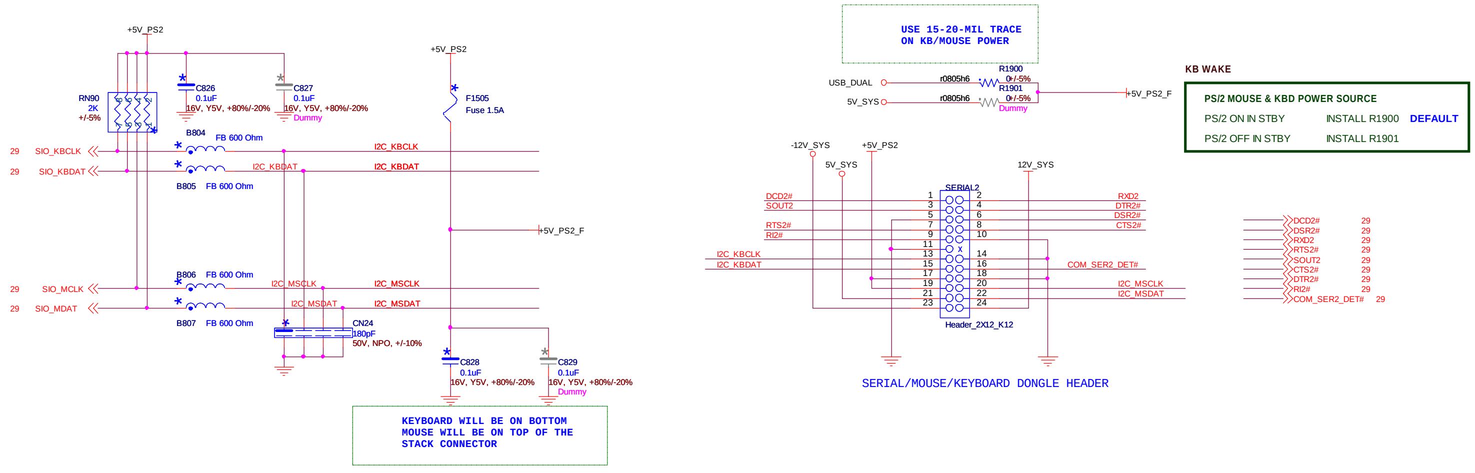
KB / MS + COM2 Connector



Title	KB/MS/COM2
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PCI Routing Summary

	PCI0	PCI1				
INTAJ	A	C				
INTBJ	B	D				
INTCJ	C	A				
INTDJ	D	B				
INTEJ						
INTFJ						
INTGJ						
INTHJ						

DELL INC.

Title
IRQ Map

DWG NO
Arrowhead

Rev
A01

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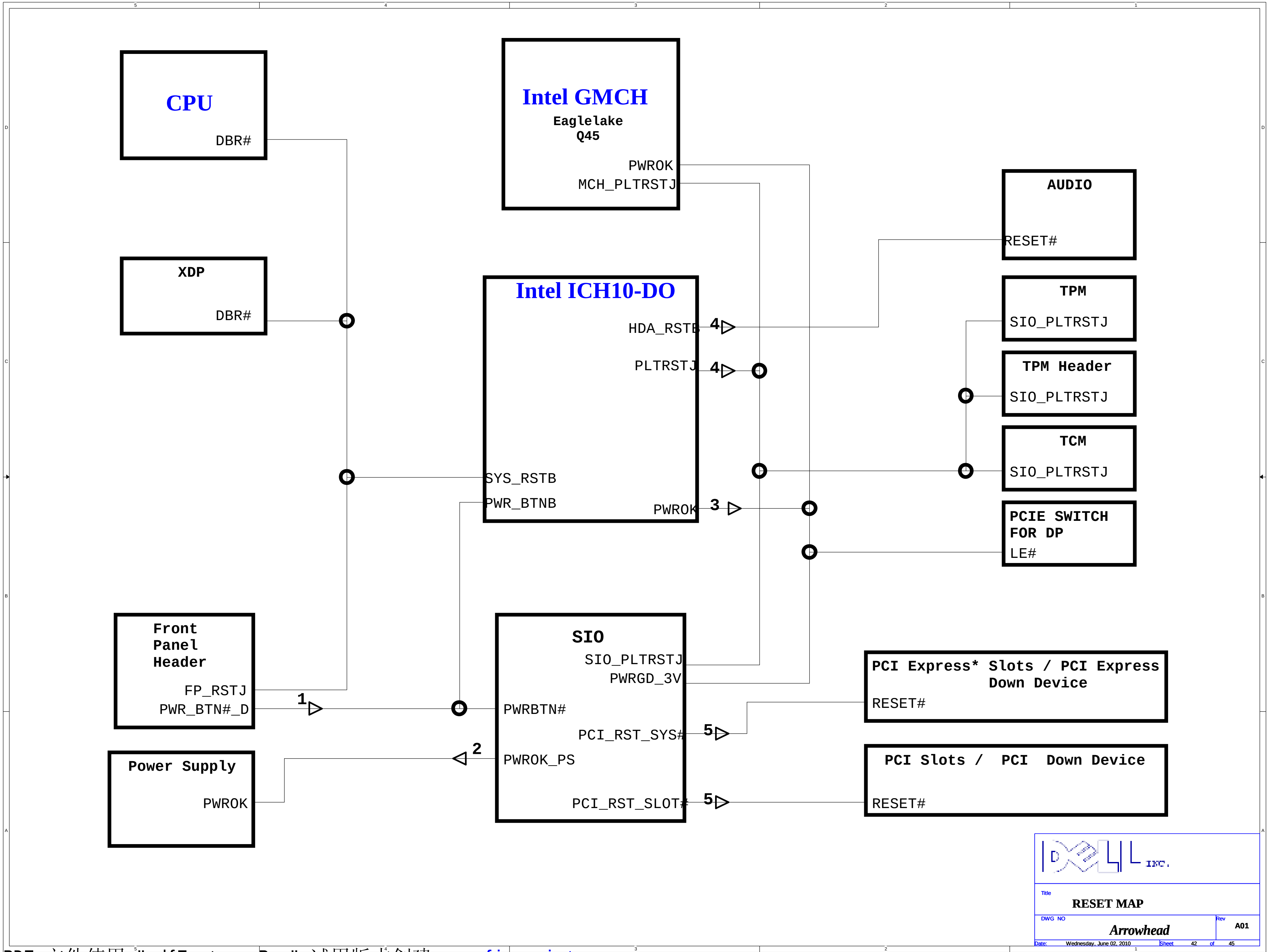
CPU
DBR#
Intel GMCH
Eaglelake
Q45
PWROK
MCH_PLTRSTJ
AUDIO
RESET#
XDP
DBR#
Intel ICH10-DO
HDA_RSTB
PLTRSTJ
SYS_RSTB
PWR_BTNB
PWROK
4
4
3
TPM
SIO_PLTRSTJ
TPM Header
SIO_PLTRSTJ
TCM
SIO_PLTRSTJ
PCIE SWITCH
FOR DP
LE#
Front
Panel
Header
FP_RSTJ
PWR_BTN#_D
1
SIO
SIO_PLTRSTJ
PWRGD_3V
PWRBTN#
PCI_RST_SYS#
PWROK_PS
PCI_RST_SLOT#
2
5
5
PCI Express* Slots / PCI Express
Down Device
RESET#
PCI Slots / PCI Down Device
RESET#
Power Supply
PWROK
DELL INC.
Title
RESET MAP
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Arrowhead
Rev
A01
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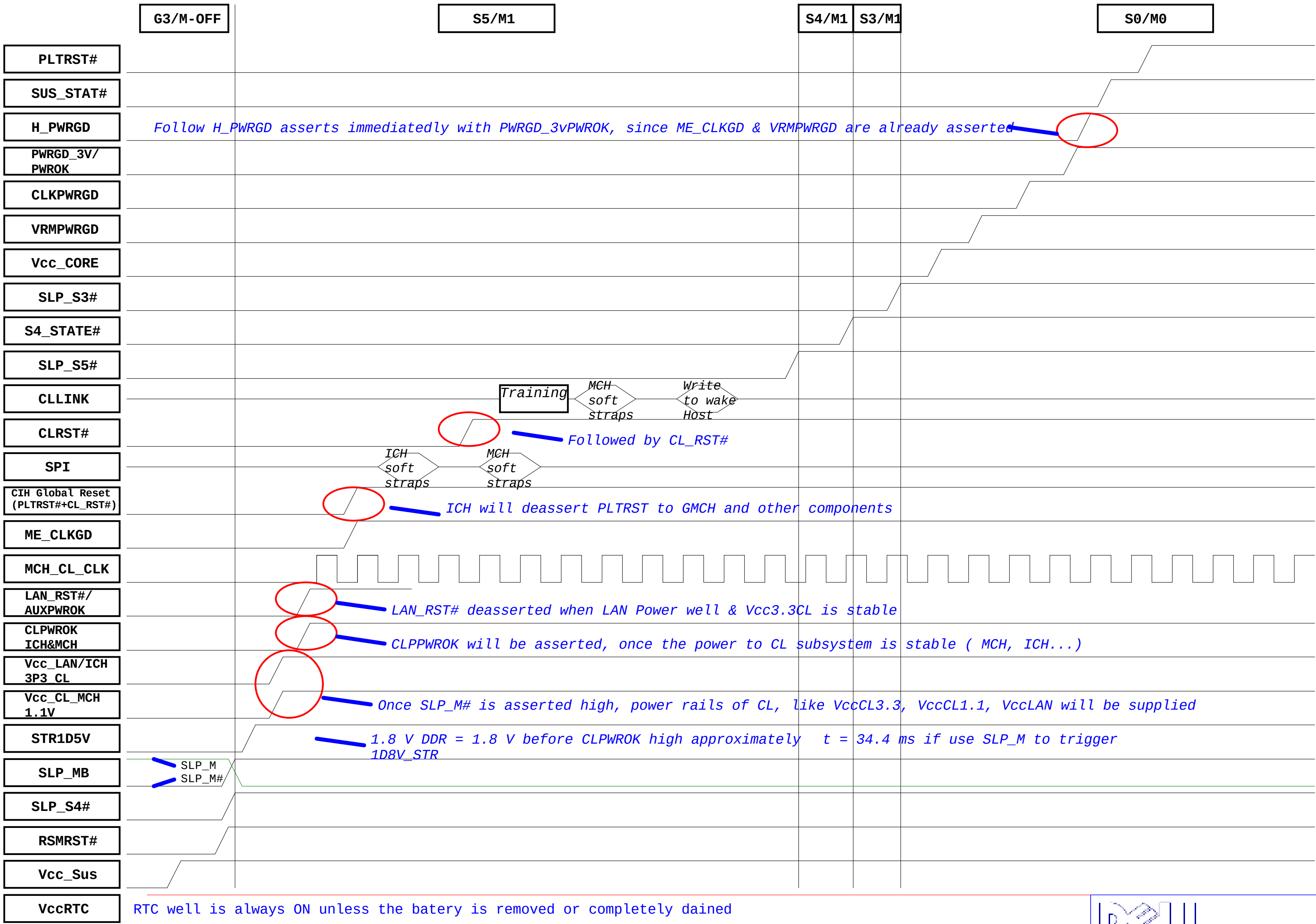

Reference to 367652_Eaglelake_platform_Design_Guide_Rev1_2 Figure 26-8. ME Platform Sequencing Diagram

DELL INC.

Title: AMT TIMING

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Clock Gen IDTCV184 Functional Straps

PIN NAME	NET		Strapping description	
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED	DEFAULT
		0	Overclocking ENABLED	
PCI3/CFGP (PIN5)	CK_PIN5	1	CGF TABLE ENABLED	
		0	CGF TABLE DISABLED	DEFAULT
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5	
		0	CPU_STOP# and PCI_STOP#	DEFAULT
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP	DEFAULT
		0	SRC8	

SIO SMSC5524 Functional Straps

PIN NAME	NET		Strapping description	
SPEAKER[DIAG_EN#] /GP8051_45/GP14 (PIN127)	SPEAKER	1	Diag_En Disable	
		0	Diag_En Enable	DEFAULT
RTS1#[SYSOPT] /GP8051_58 (PIN101)	RTS1#	1	Sysopt strap 0 X 4E	
		0	Sysopt strap 0 X 2E	
DTR1#[FLASH_EN] /GP8051_16 (PIN104)	DTR1#	1	Flash Enable	
		0	Parallel Enable	DEFAULT

Intel ICH10 Functional Straps

PIN NAME	NET		Strapping description	
TP3	TP68	1	Danbury Technology Enable	Internal Pull-up
		0	XOR Chain Entrance	
SPKR	SPKR	1	NoReboot mode	Internal Pull-up
		0	Reboot mode	
GPIO33 / HDA_DOCK_EN#	MFG_MODE	1	MEenable	DEFAULT
		0	ME disable	
SPI_MOSI	ICH_SPI_MOSI	1	MCH TPM Enable	
		0	MCH TPM disable	DEFAULT

Intel MCH Eaglelake Q45 Functional Straps

PIN NAME	NET		Strapping description
cen	TLS	1	TLS Enable
		0	TLS disable
iTPMb	ITPM_EN	1	iTPM Enable
		0	iTPM disable
DDPC_CTRLDATA	DDPC_CTRLDATA	1	SELECT Display Port
		0	SELECT PCIEX16
DDPC_CTRLCLK	DDPC_CTRLCLK	1	SELECT Display Port
		0	SELECT PCIEX16

Chassis	SKU	TPM	TCM	R643	TPM SKU ID					Board ID		
					SKU3	SKU2	SKU1	SKU0	Pop option	REV1	REV0	Pop option
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	2	[illegible]	[illegible]	[illegible]	0	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	1	[illegible]		[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]

Chassis	Chassis ID			
	ID2	ID1	ID0	Pop option
[illegible]	[illegible]	1	[illegible]	[illegible]
[illegible]	[illegible]	1	[illegible]	[illegible]
[illegible]	[illegible]	1	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	0	[illegible]	[illegible]

DELL INC.

Title: **Strap Pin & ID POP Table**

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B00-X00

```
050809/1115:stuff  r1311,change connection from 3D3V_SYS to 3D3V_SB;
050809/1555:Delete PQ54
050809/1712:Change q13 from NTD4910NT4G to NTD40N03R;change q17 from NTD4906NT4G to NTD40N03R;delete PC100,stuff EC20;change EC20 from 470uf to 1000uf;
051109/1040:Change c187 from 4.7nF to 6.8nF,c89 from 47pF to 56pF.
051109/1547:Change R664 from 200 to 100,R665 from 1.5k to 2.2k,and then 2.2v changed to 2.4v for thermal balence;
           change back of 051109/1040

051209/08:31:Add prn50,prn51 for 1.5v_str to 1.5v_ich
             remove ec57 to 1d05v_ich


051209/10:13:Dummy R184,R664,R665,R666,C446,C448,Q58 for 1.5v_str converted 1.5v_ich
051209/10:13:Dummy R184,R664,R665,R666,C446,C448,Q58 for 1.5v_str converted 1.5v_ich
051209/16:00:dummy r229,r220,q3030;
             change r223,r221's source from 3.3v_sb to 3.3v_sys
051309/11:07:Add pr470,PR183,PR298 for 1.5v_ich
             Dummy R183,c100,c101,r185,pr470
051309/1115:change  r1311 connection from 3D3V_SB to 3D3V_SYS;
051809/0829:modify the power dilivery in page 4
051809/1404:Add impedance_5,impedance_6 in page 38
051809/1413:Change r227 from 5% to 1%
051809/1900:delete tp101,tp102;change the footprint of c391,c392,c393,c395 from c0603h9_ddr to c0603h9.
051909/1131:change the power dilivery in page 4
051909/1619:add pc1014,pc1015 for emc in page39
052009/1619:dummy r1311
052009/1620:change r227 from 33 to 33k
052209/0839:change the silkname from SATA0,SATA1,SATA2,SATA3,LPC_DEBUG1 to SATA_0,SATA_1,SATA_2,SATA_3,LPC_DEBUG.
052209/1110:change symbol of DIMM
052209/1600:Dummy U29,U29_1;Stuff U3521
052309/1118:update 32Mb to 64Mb in page1&2
052609/0904:change c178&188 from 0.22uF to 2.2nF.
           change Q20 to AOD452
052609/1134:add PEC23,PREC23 for VTT_DDR
060109/1359:change R5281 from 475 to 499
           change PREC23 to PEC231
060209/1506:add c25712,c28412,c504,c5041,c505,c5051
060309/1545:change H6,H7,H8,H9,H11,H12,H13,H14,H19's footprint
060409/1259:add r1341
060509/0836:dummy r1341
060509/0836:add r664,r665,c446,c448,r666,q58,r183,r184,c100,pr470,c101,r185,prn50.
             dumm pr183,pr298,prn51
060509/1524:add two dummy res r2232,r2212
060809/1008:add C4801 for EMI
061609:change C448,C101 to 10nf;change R252 from 150 to 300.change R589 from 1k to 2.7k.
           change all the Y5V materials to X7R.
```

X00-A00

```
073109:change R149 from 475 to 464.
       Dummy all the debug components.
080509:Dummy DSKT2,R347
```

DELL INC.			
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