TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
SO_DDRIII DIMMA1&SO_DDRIII DIMMB1	7,8
PPT-PCI/E/DMI/CLK/USB20/USB30	9
PPT-SATA/HOST/GPIO/VGA/CCMOS	10
PPT-SMB/LPC/AUDIO/RTC/SPI	11
PPT-POWER,GND/NVRAM /CP STRAPS	12,13,14
PCIE Slot	15,16
PCIE To PCI Bri	17
PCI Slot	18
SIO-Fintek F71869AD	19
AUDIO 892/887	20
LAN - RTL8111E/8105	21
DVI/HDMI/VGA/SATA Connector	22,23,24,25
USB2.0/3.0 Connector	26,27
FAN	28
VRM12 - UT501	29
UP6282 3-Phase+MOS CPU	30
UP6282 1-Phase+MOS GPU	31
UP1504 - VTT POWER	32
OP+MOS - SA POWER	33
UP1504 - DDR POWER	34
UP1504 - PCH POWER	35
ATX F_Panel/EMI/TPM	36
ACPI Controller UPI	37
XDP / Manual Parts	38
EMI CAP	39

MS-7758

ATX

Ver: 2.1(304.8x243.84)

H/W:Jia Wu

PM:Guangmei Zhao

Intel -MahoBay plamform B75

CPU:

IVY bridge LGA1155

System Chipset:

Panther Point B75

Onboard Chip:

HD Audio Codec:ALC892 colay 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 128 MB

Main Memory:

*DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12 -UT501 3+1 Phase

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

*PCI Express (X4) Slot * 1*

*PCI Slot * 3*

Other:

SATA3.0 x1+SATA2.0 x5 (PCH)

*USB2.0 *8*

*REAL USB3.0 *2*

*FRONT USB3.0 *2*

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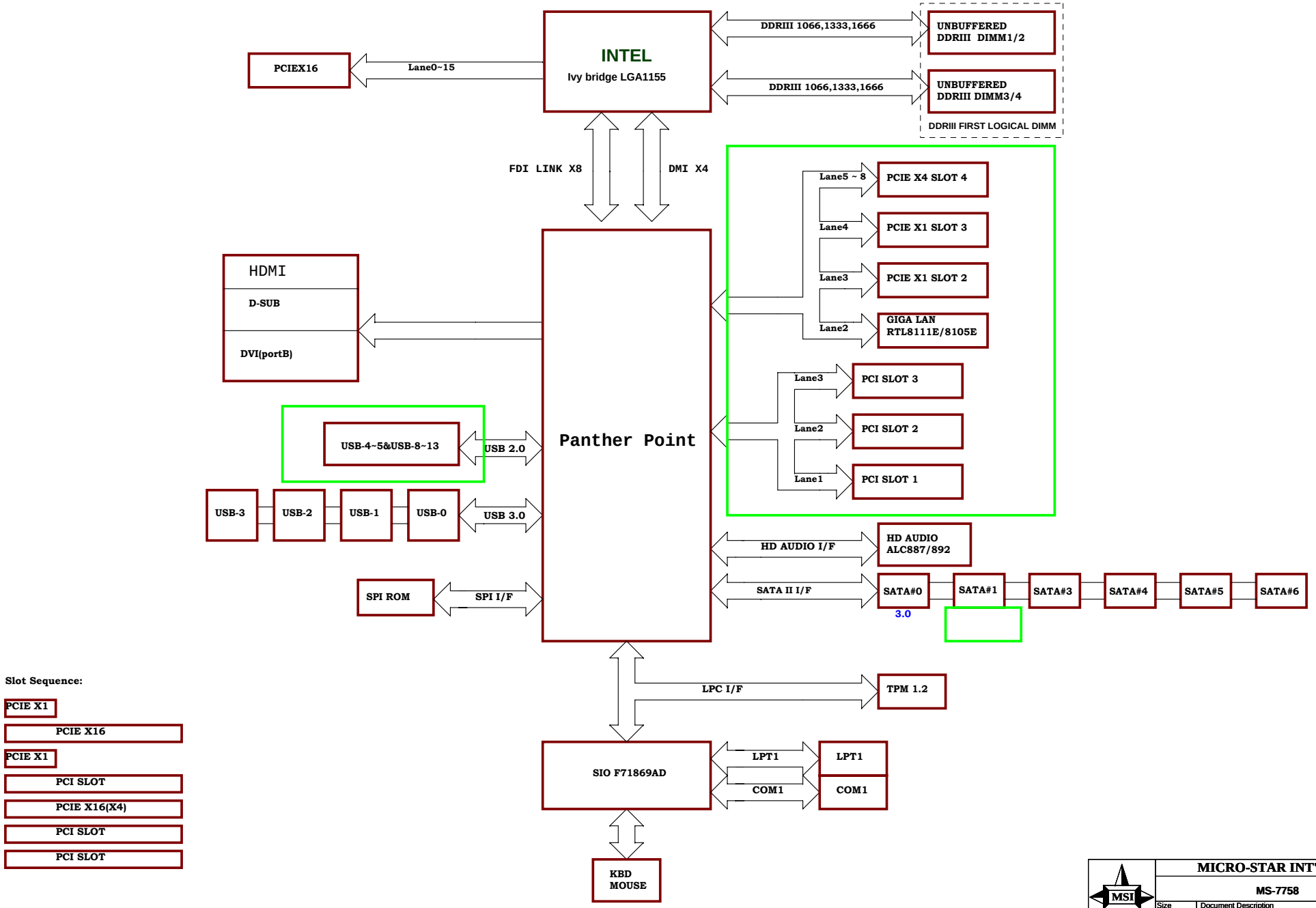
MS-7758

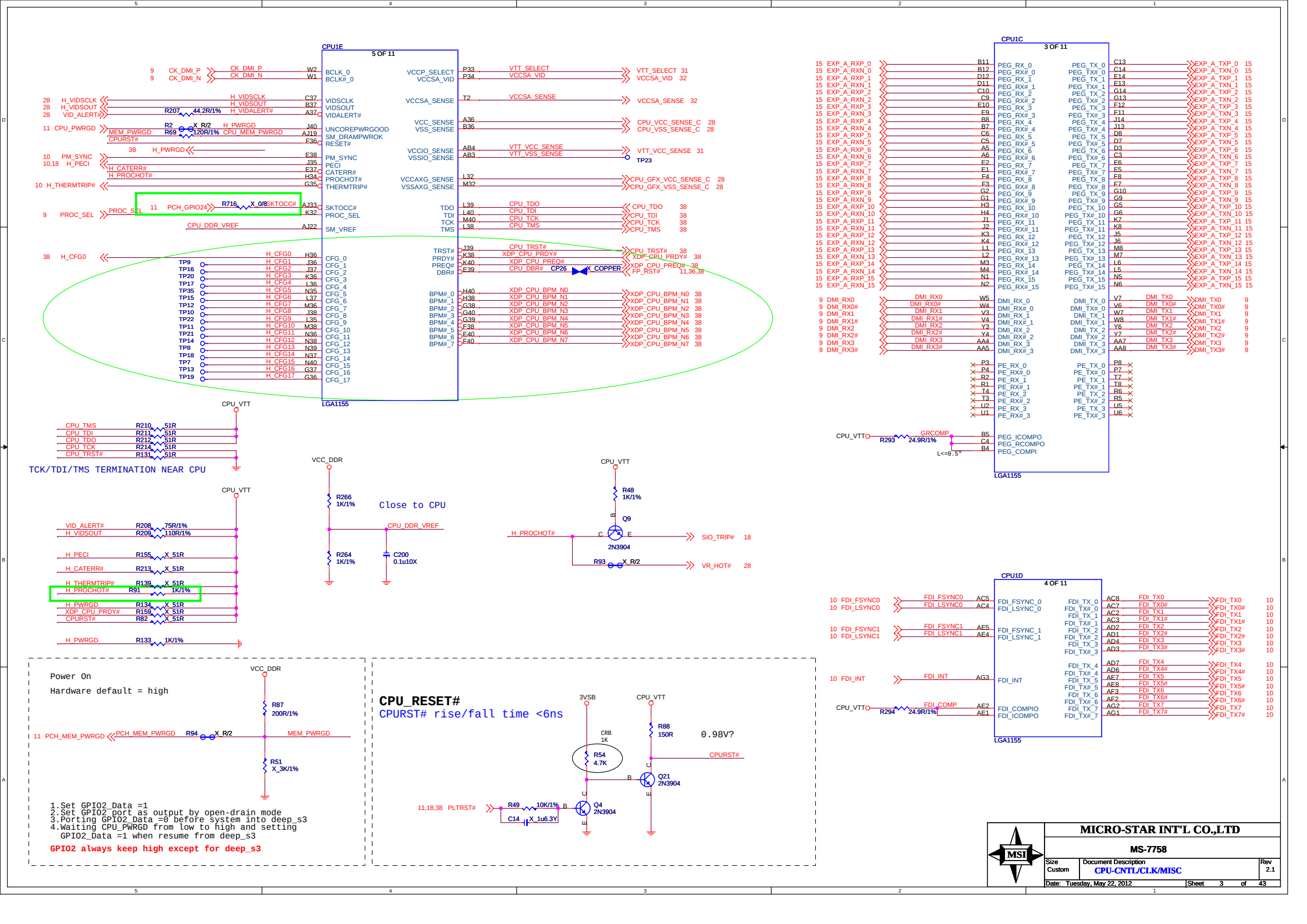
Size: Custom | Document Description: Cover Sheet | Rev: 2.1

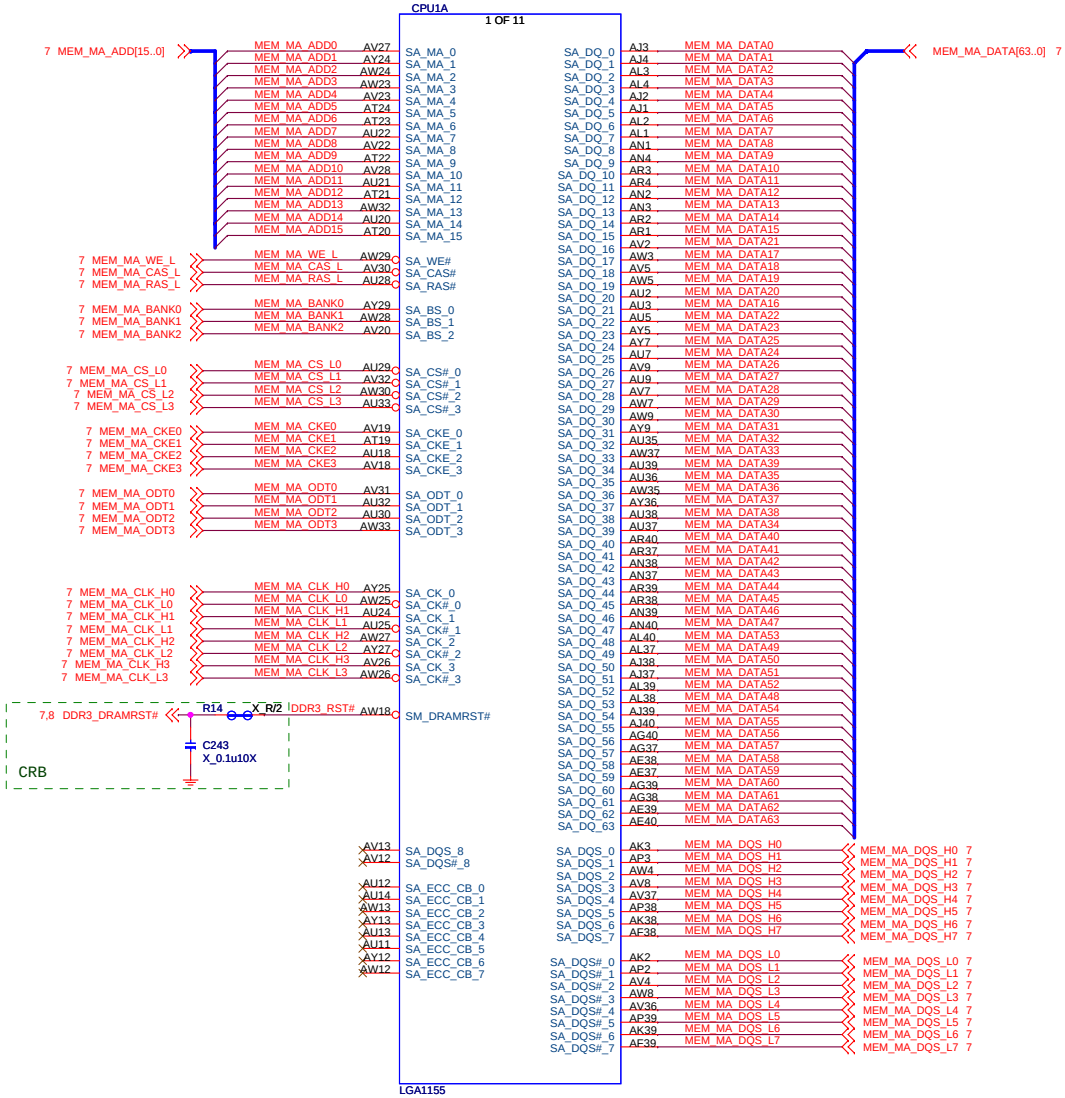
Date: Friday, May 18, 2012 | Sheet 1 of 43

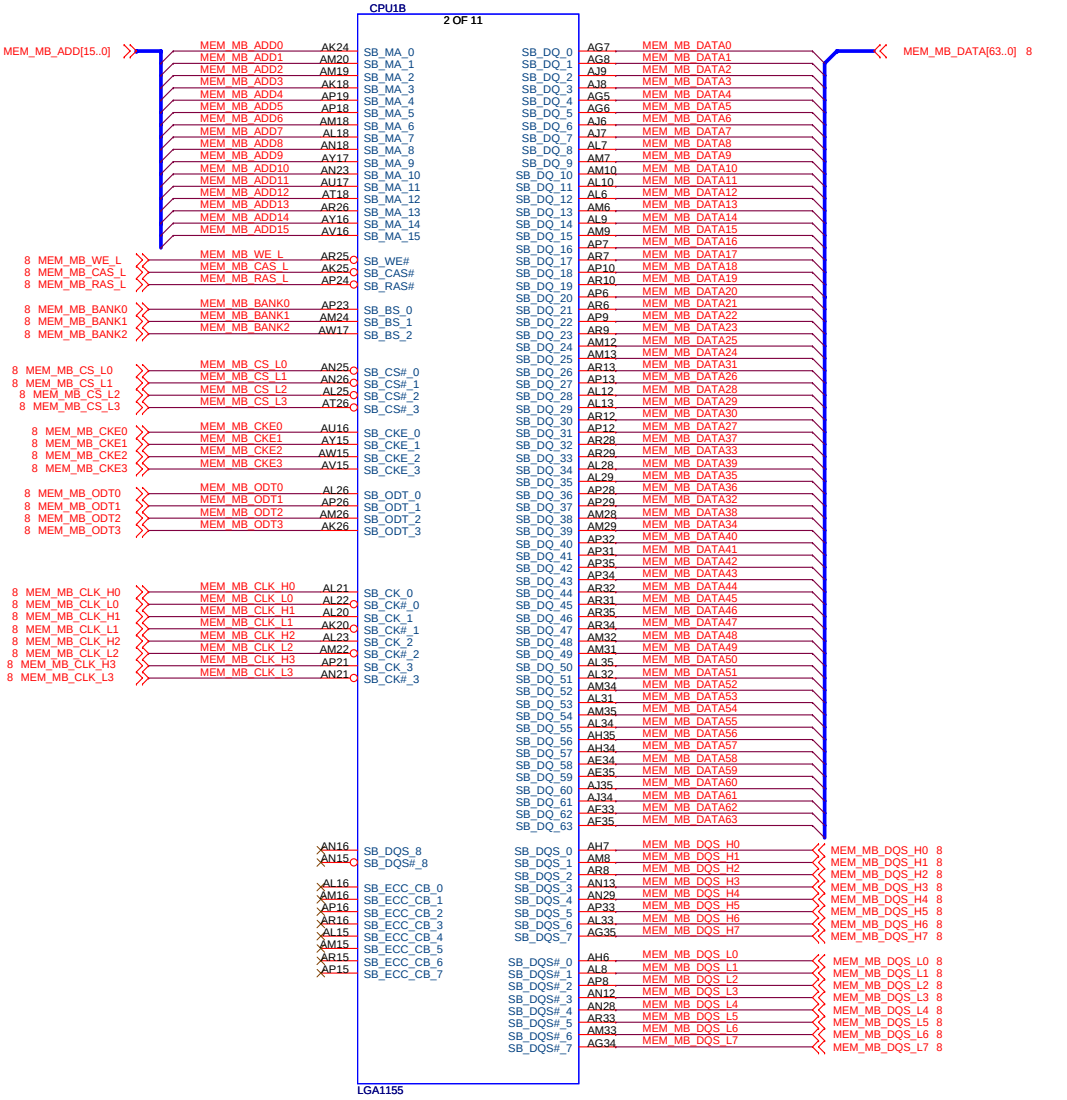
MS-7758 Block Diagram



MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: Block Diagram	Rev: 2.1
Date: Friday, May 18, 2012	Sheet 2 of 43	


CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
TCK/TDI/TMS TERMINATION NEAR CPU
Close to CPU
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2_port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting
GPIO2_Data =1 when resume from deep_s3
GPIO2 always keep high except for deep_s3
CPU_RESET#
CPURST# rise/fall time <6ns
0.98V?
MICRO-STAR INT'L CO.,LTD
MS-7758
CPU-CNTL/CLK/MISC
Rev 2.1
Tuesday, May 22, 2012
Sheet 3 of 43





MICRO-STAR INT'L CO.,LTD

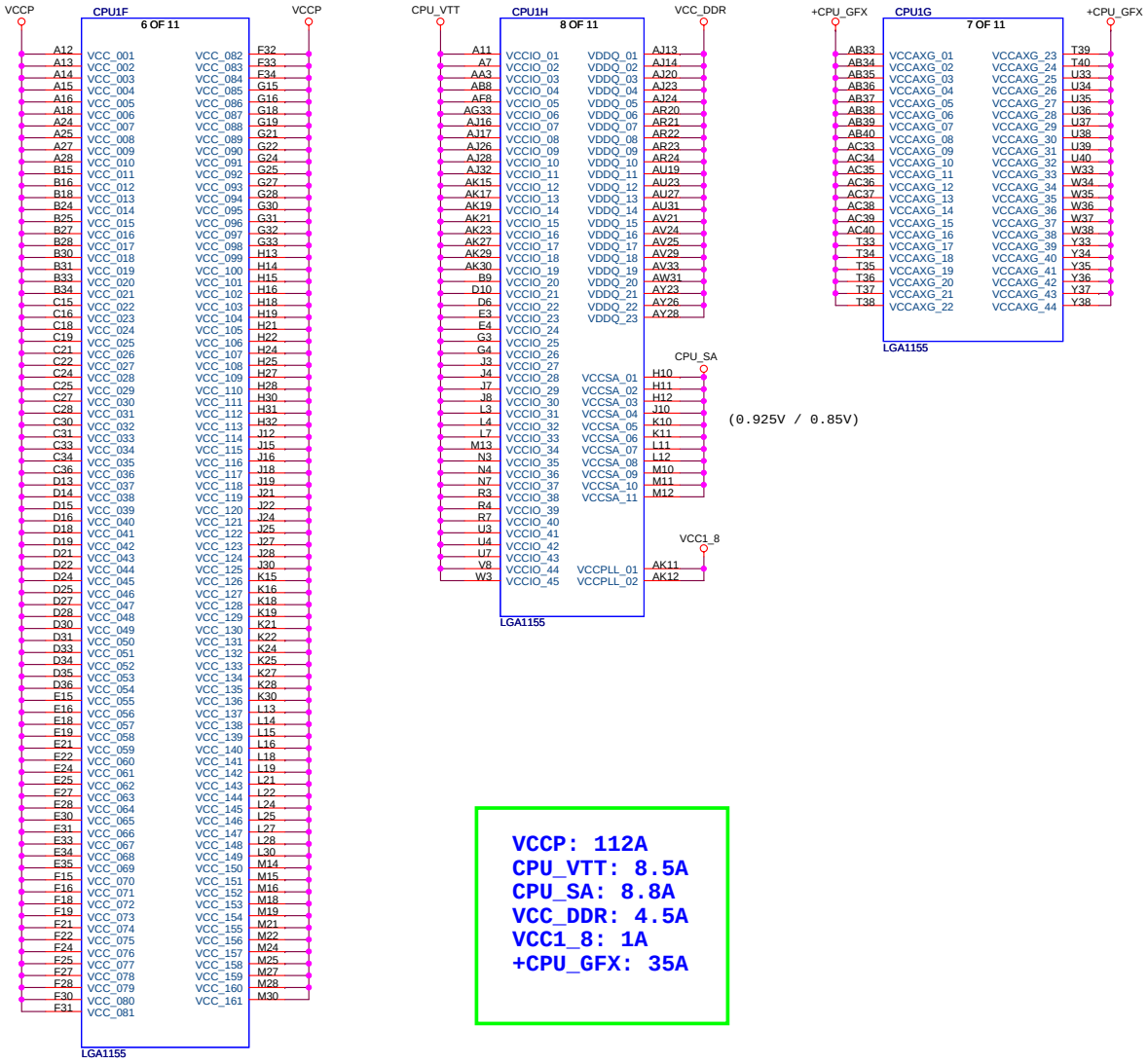
MS-7758

Size	Document Description	Rev
Custom	CPU-Memory	2.1

Date: Tuesday, May 22, 2012 Sheet 4 of 43

(1.05V / 1.00V)

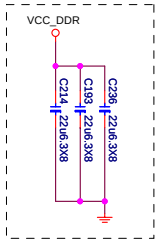
(0.925V / 0.85V)



VCCP: 112A
CPU_VTT: 8.5A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1A
+CPU_GFX: 35A

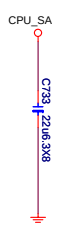
+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



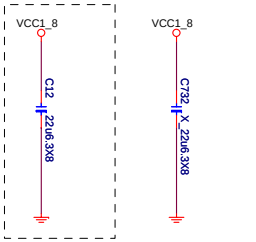
+CPU_SA Decoupling

Backside



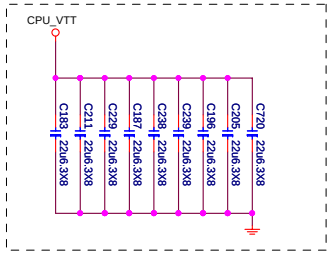
+VCC1_8 Decoupling

Backside

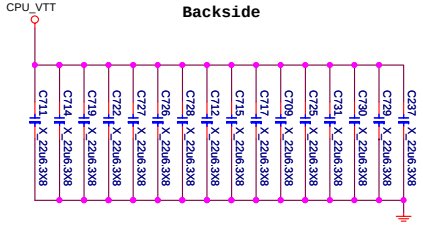


+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

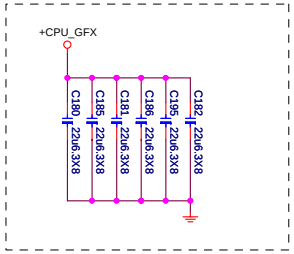


Backside

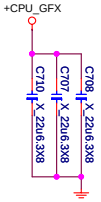


+CPU_GFX Decoupling

CPU SOCKET CAVITY CAPS

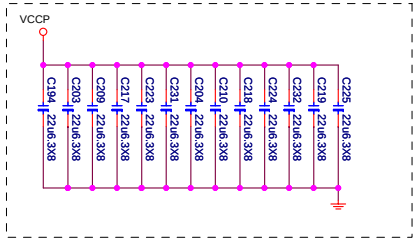


Backside

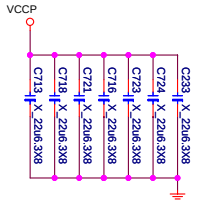


+CPU_VCCP-Decoupling

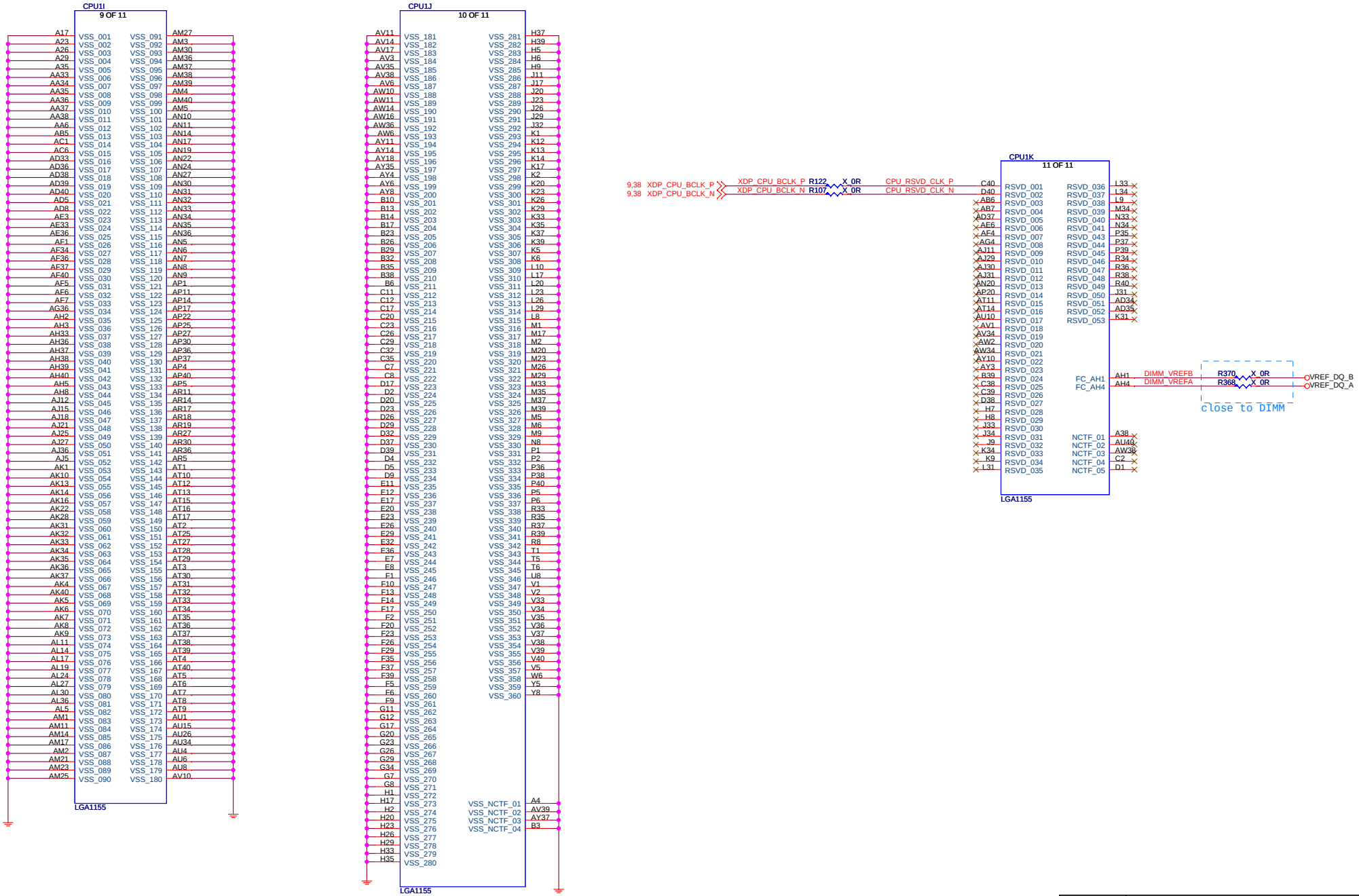
CPU SOCKET CAVITY CAPS



Backside



MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: CPU-Power	Rev: 2.1
Date: Friday, May 18, 2012	Sheet 5 of 43	



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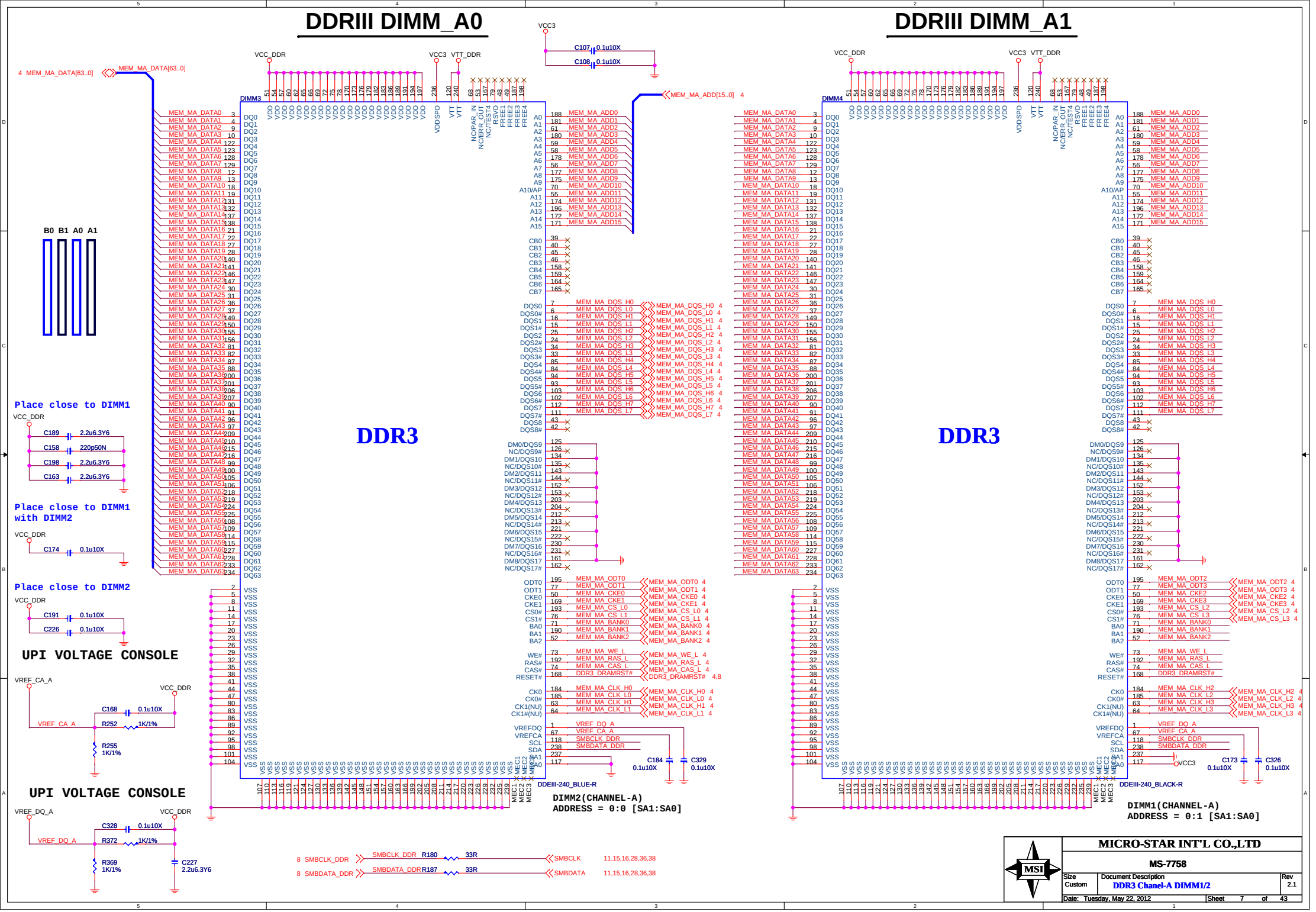
MS-7758		
Size: Custom	Document Description: CPU-GND	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 6 of 43	

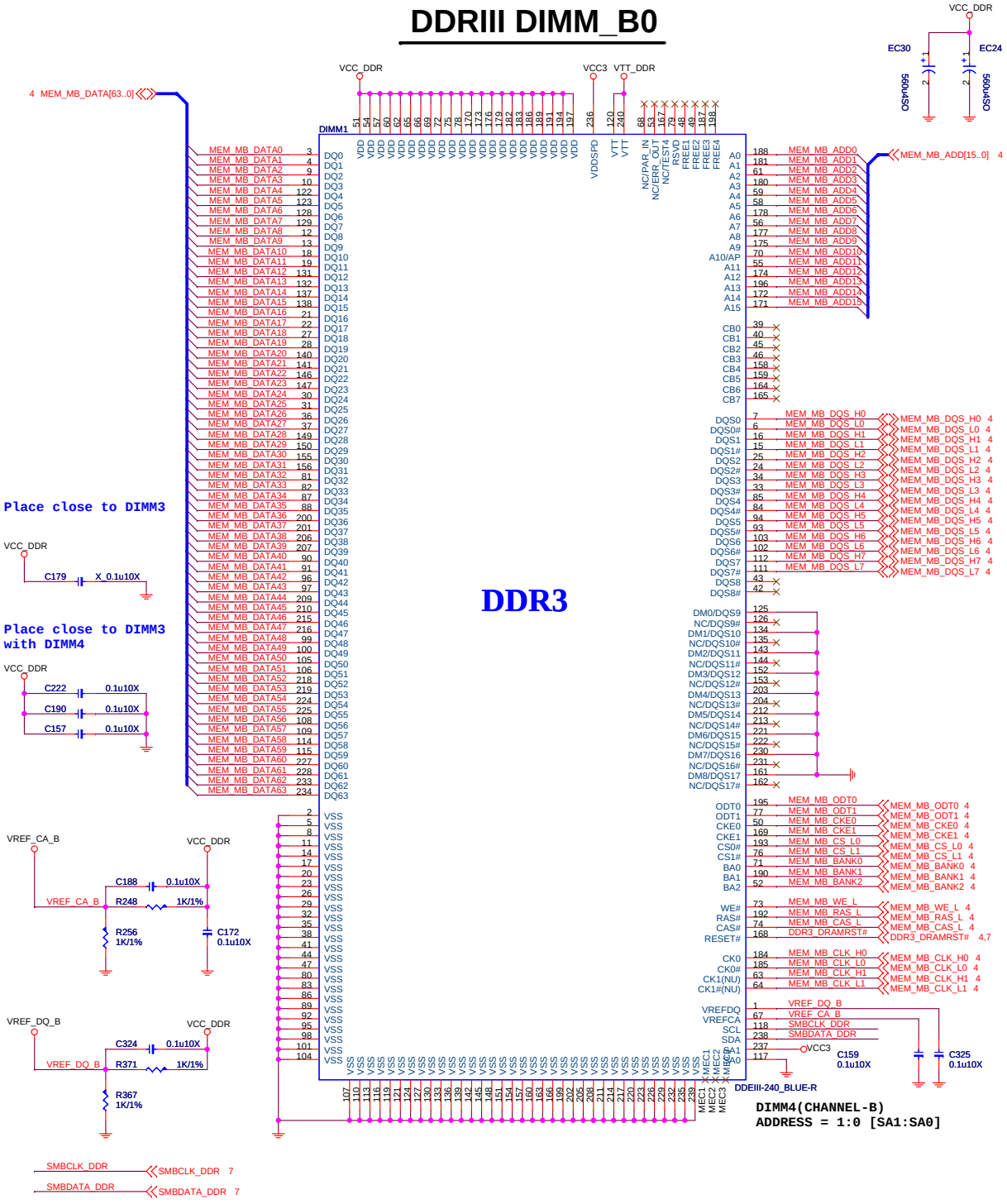
DDRIII DIMM_A0

DDRIII DIMM_A1

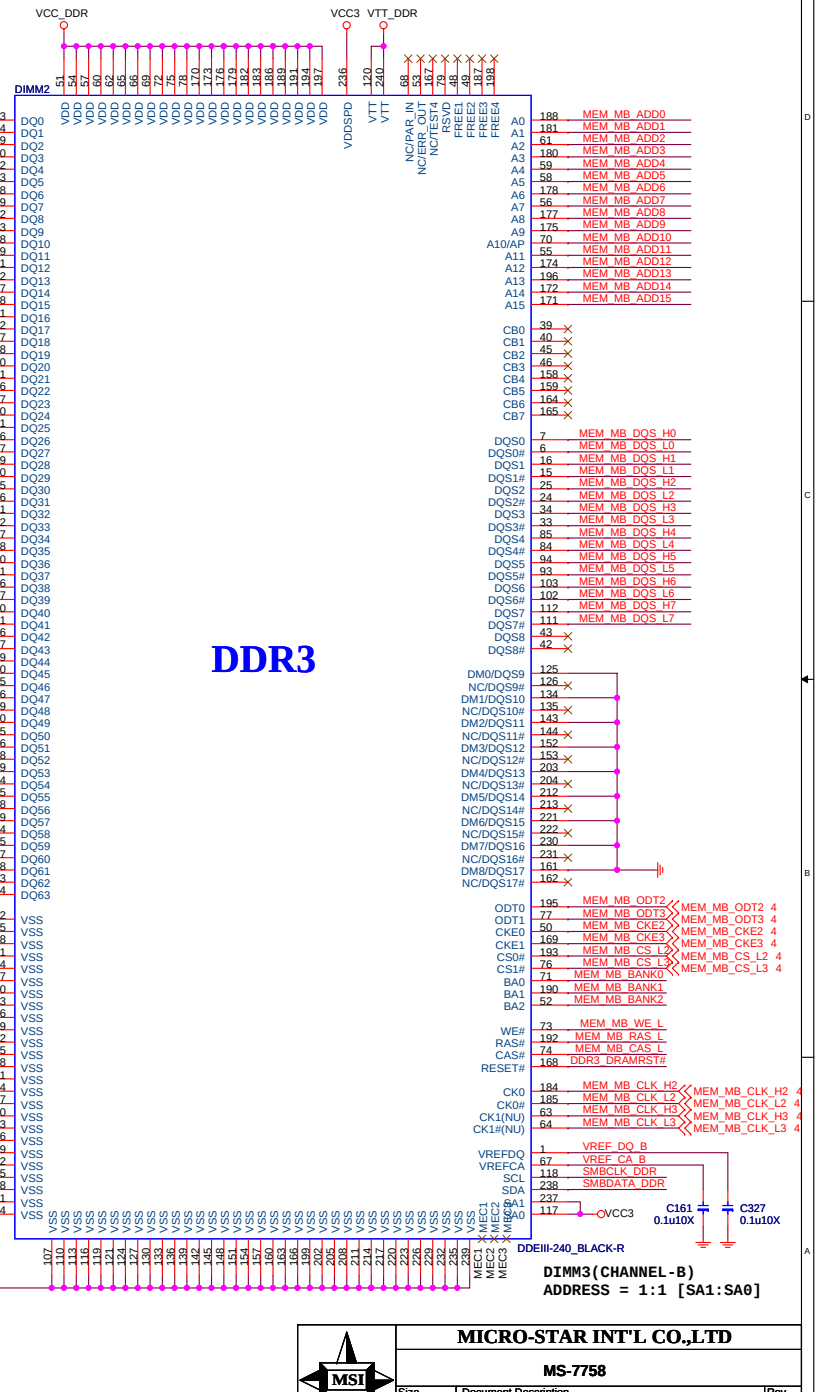


MICRO-STAR INT'L CO.,LTD	
MS-7758	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
Rev: 2.1	
Date: Tuesday, May 22, 2012	Sheet 7 of 43

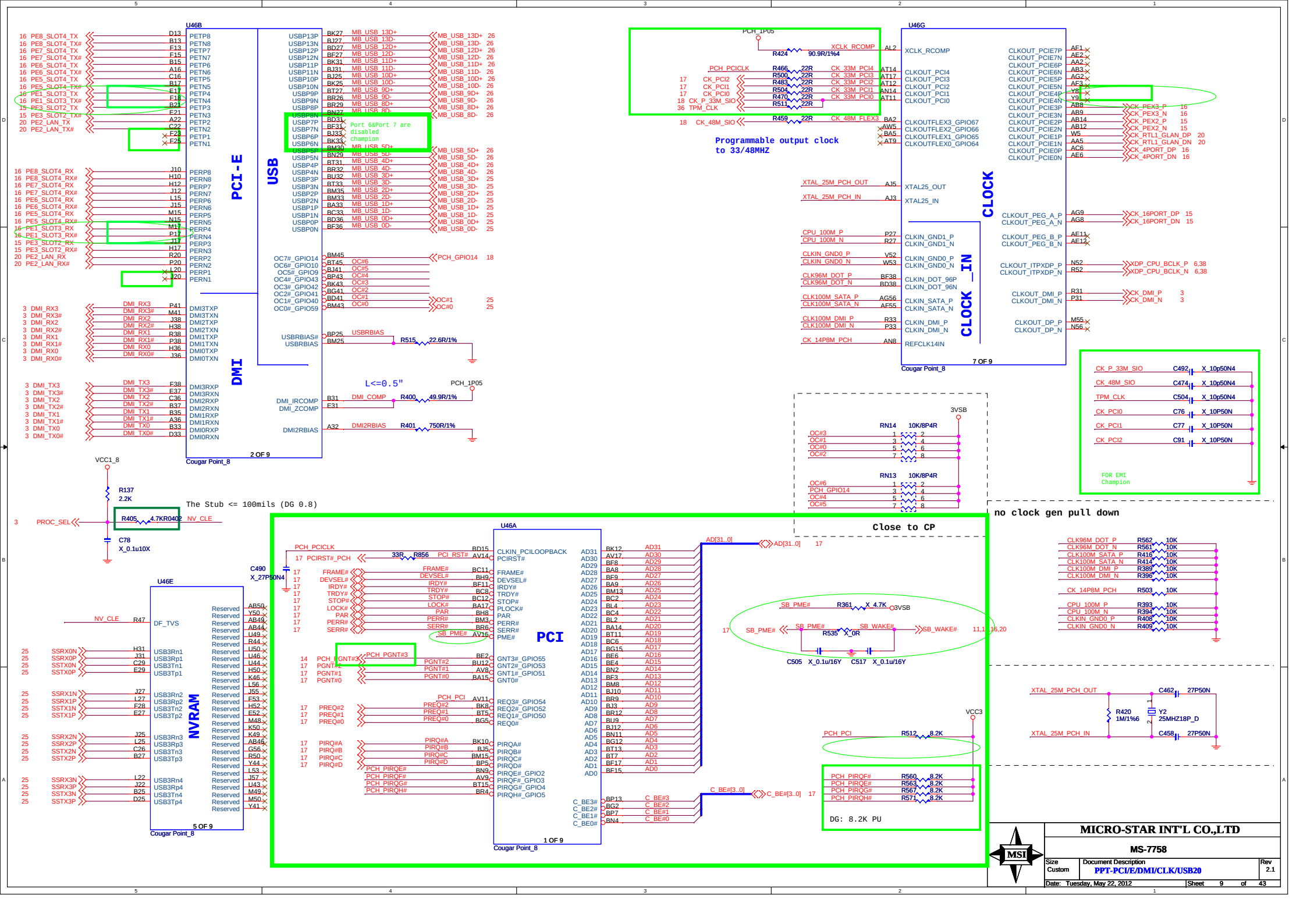
DDRIII DIMM_B0

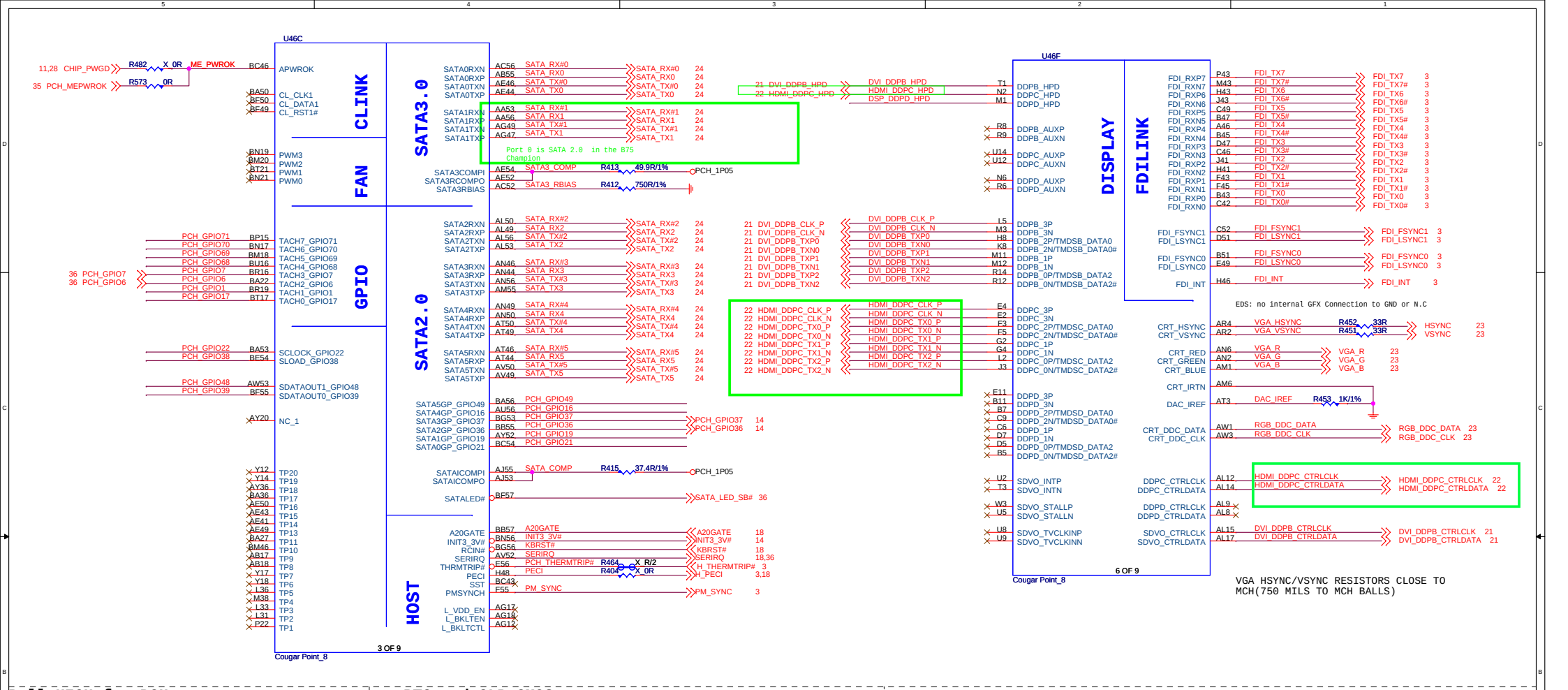


DDRIII DIMM_B1

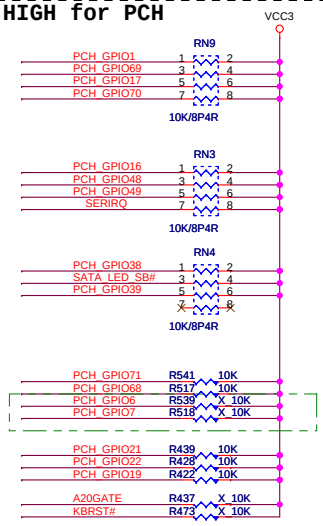


MICRO-STAR INT'L CO.,LTD	
MS-7758	
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4
Rev: 2.1	
Date: Tuesday, May 22, 2012	Sheet 8 of 43


U46B
PCI-E
USB
DMI
2 OF 9
Cougar Point_8
Port 6&Port 7 are disabled champion
L<=0.5"
PCH_1P05
R515 22.6R/1%
R400 49.9R/1%
R401 750R/1%
The Stub <= 100mils (DG 0.8)
VCC1_8
R137 2.2K
R405 4.7KR0402
PROC_SEL
NV_CLE
C78 X_0.1u10X
U46E
NVRAM
5 OF 9
U46A
PCI
1 OF 9
C490 X_27P50N4
R856 33R
PCI_RST#
Close to CP
U46G
CLOCK
CLOCK_IN
7 OF 9
R424 90.9R/1%4
Programmable output clock to 33/48MHZ
XTAL_25M_PCH_OUT
XTAL_25M_PCH_IN
R420 1M/1%6
Y2 25MHZ18P_D
C462 27P50N
C458 27P50N
3VSB
RN14 10K/8P4R
RN13 10K/8P4R
no clock gen pull down
R361 X_4.7K
R535 X_0R
C505 X_0.1u/16Y
C517 X_0.1u/16Y
VCC3
R512 8.2K
R560 8.2K
R563 8.2K
R567 8.2K
R571 8.2K
DG: 8.2K PU
FOR EMI Champion
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description PPT-PCI/E/DMI/CLK/USB20
Rev 2.1
Date: Tuesday, May 22, 2012
Sheet 9 of 43



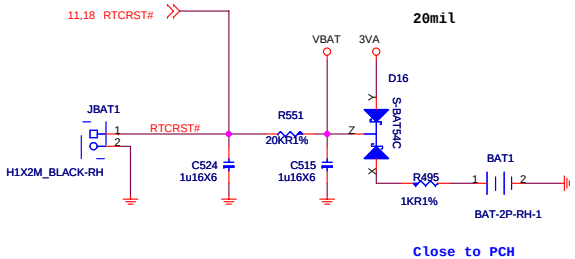
Pull HIGH for PCH



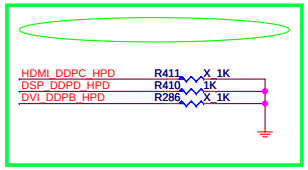
RTC and CLR_CMOS

Clear CMOS

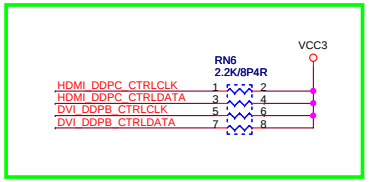
CMOS CLEAR JUMPER	
JBAT1 Clear CMOS	
1 - 2	Clear CMOS



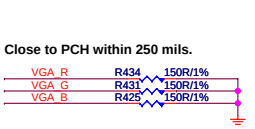
No Display port(pull down)



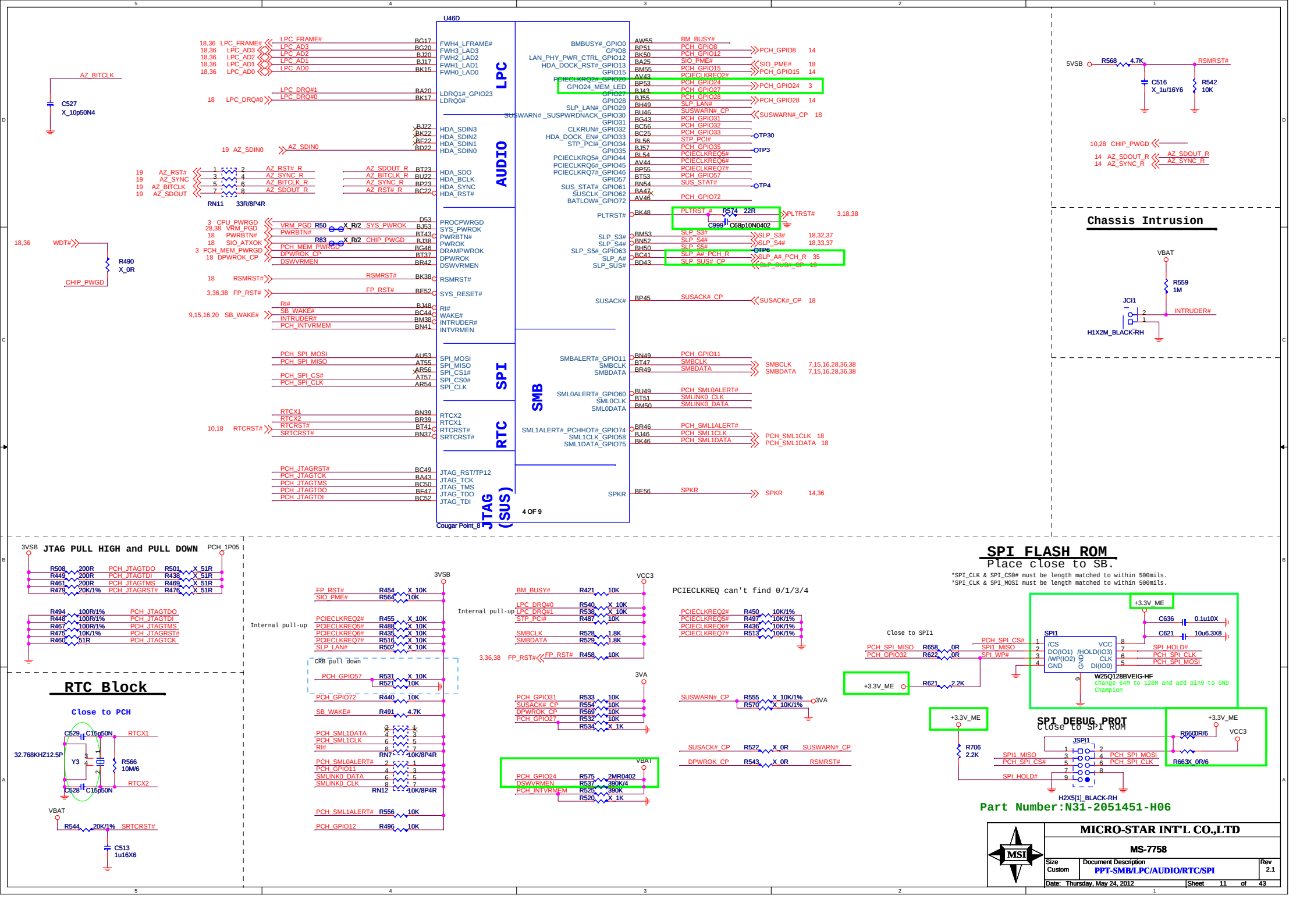
Enable VGA(CTRLCLK/DATA Pull High)

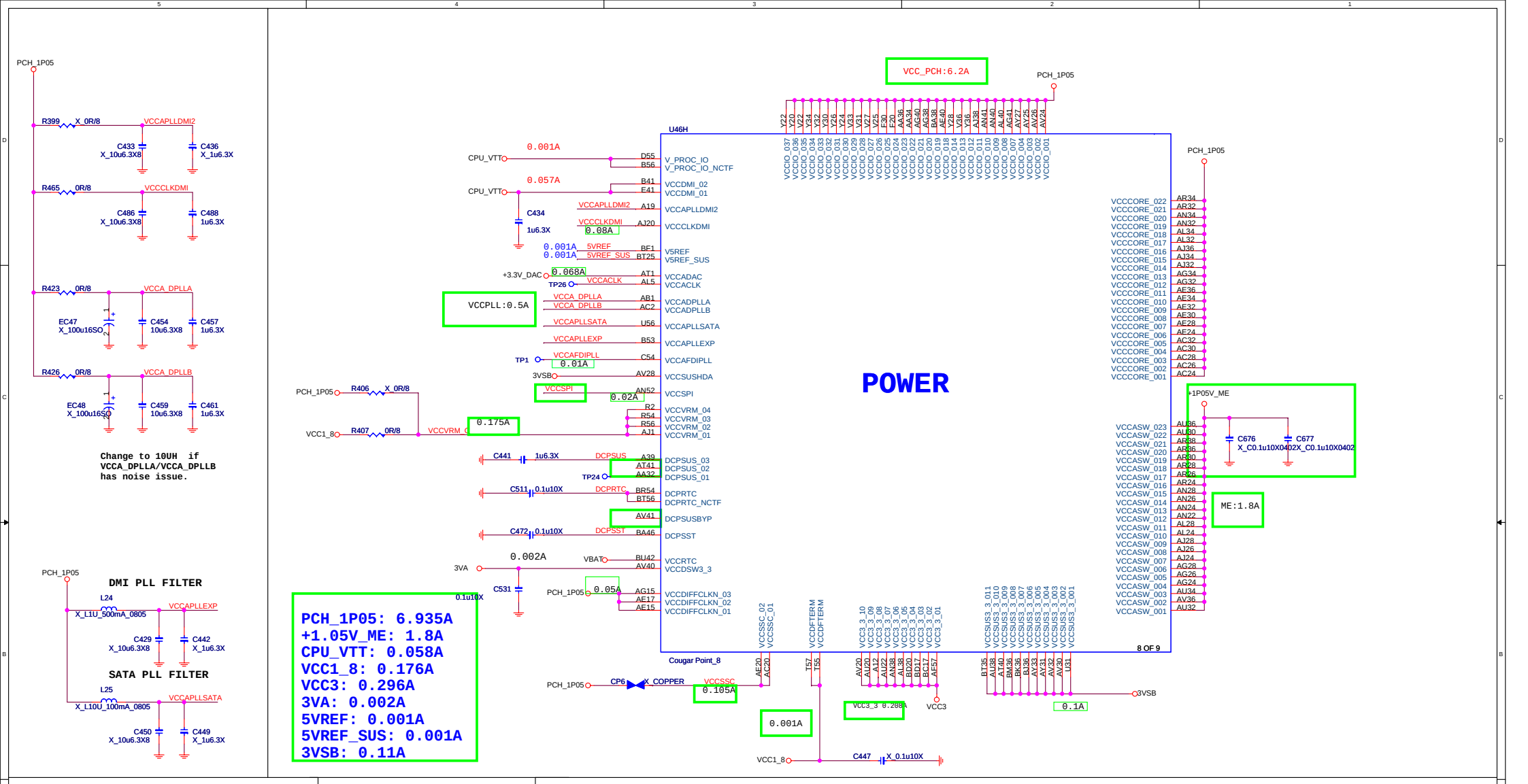


Close to PCH within 250 mils.

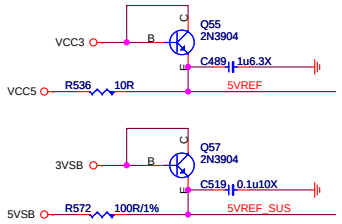


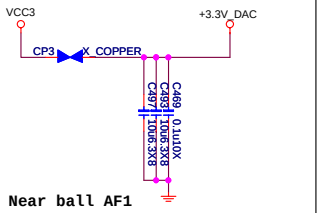
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PPT-SATA/HOST/GPIO/VGA/CCMOS	Rev: 2.1
Date: Friday, May 25, 2012	Sheet 10 of 43	

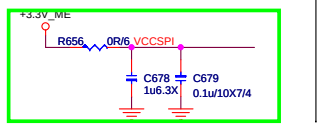

U46D
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
4 OF 9
Cougar Point_8
Chassis Intrusion
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
SPI FLASH ROM
Place close to SB.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
PCIECLKREQ can't find 0/1/3/4
Internal pull-up
CRB pull down
Close to SPI1
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
MICRO-STAR INT'L CO.,LTD
MS-7758
PPT-SMB/LPC/AUDIO/RTC/SPI
Rev 2.1
Date: Thursday, May 24, 2012
Sheet 11 of 43



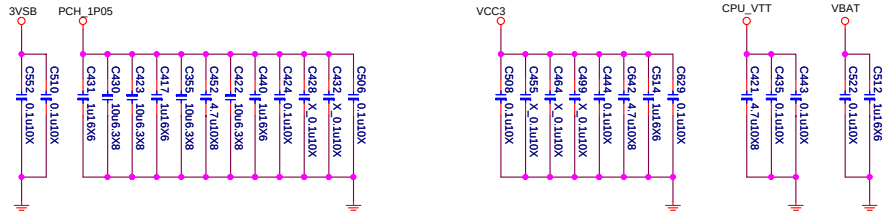
5VREF & 5VREF_SUS Sequencing Circuit



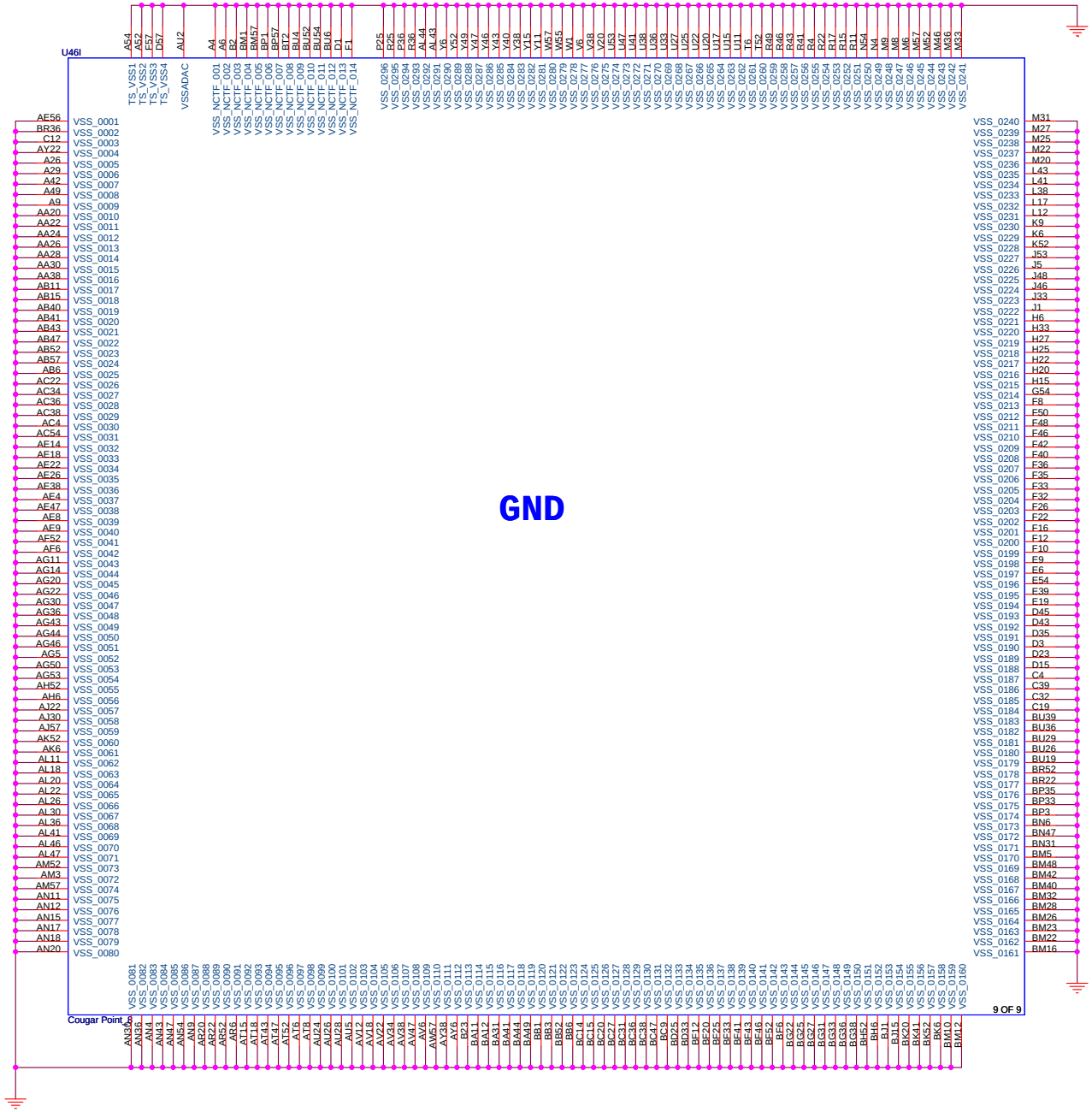




PCH decoupling cap



MICRO-STAR INT'L CO.,LTD	
MS-7758	
Size: Custom	Document Description: PPT-POWER
Rev: 2.1	
Date: Monday, May 21, 2012	Sheet 12 of 43



MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7758		
Size: Custom	Document Description: PPT-GND/NVRAM/USB30		Rev: 2.1
Date: Friday, May 18, 2012		Sheet 13 of 43	

PCH Straps

SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:

Do not pull low.

HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

Internal weak pull down. Do not pull up.

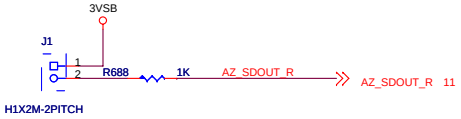
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) – Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP – Use 8.2K-10K pull-down to ground.

The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. If the signal is sampled low, this indicates that the system is strapped to the ※topblock swap§ mode (PCH inverts A16 for all cycles targeting BIOS space).
The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.

Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) – Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP – Use 8.2K-10K pull-down to ground.

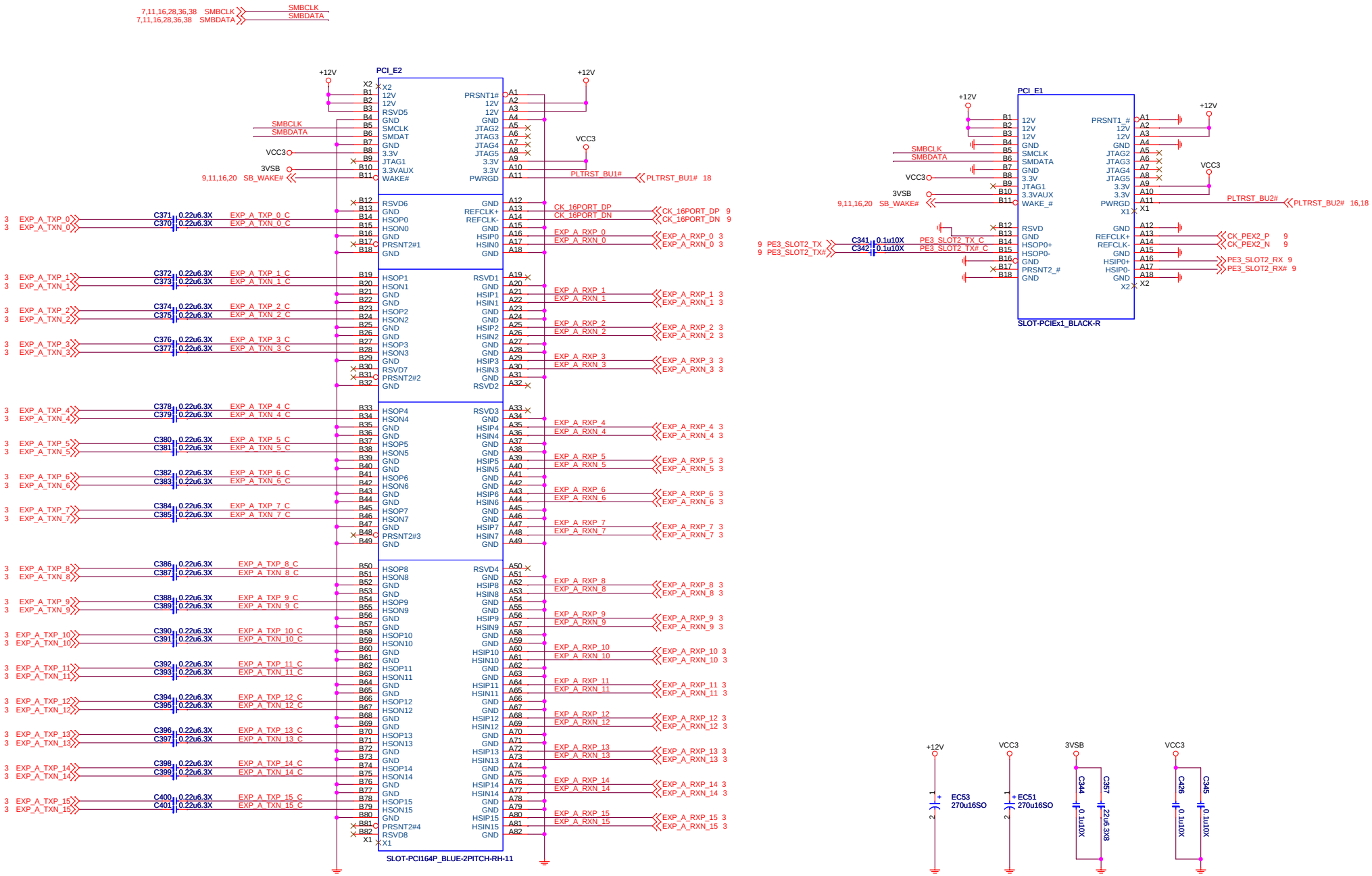
BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by softstrap through ME.



Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

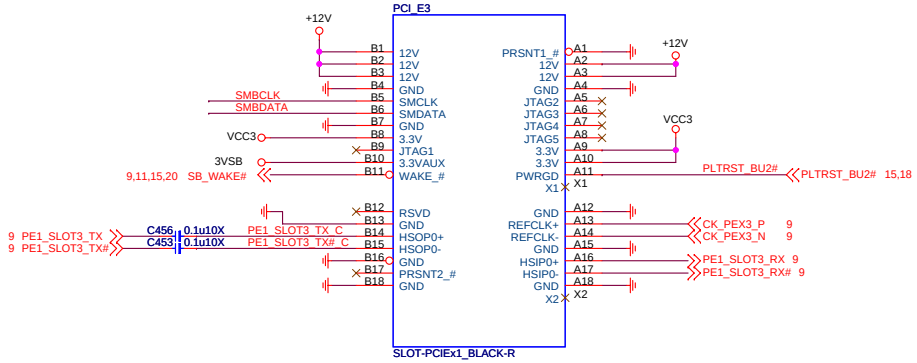
Internal weak pull up. Do not pull low.
On die PLL voltage regulator

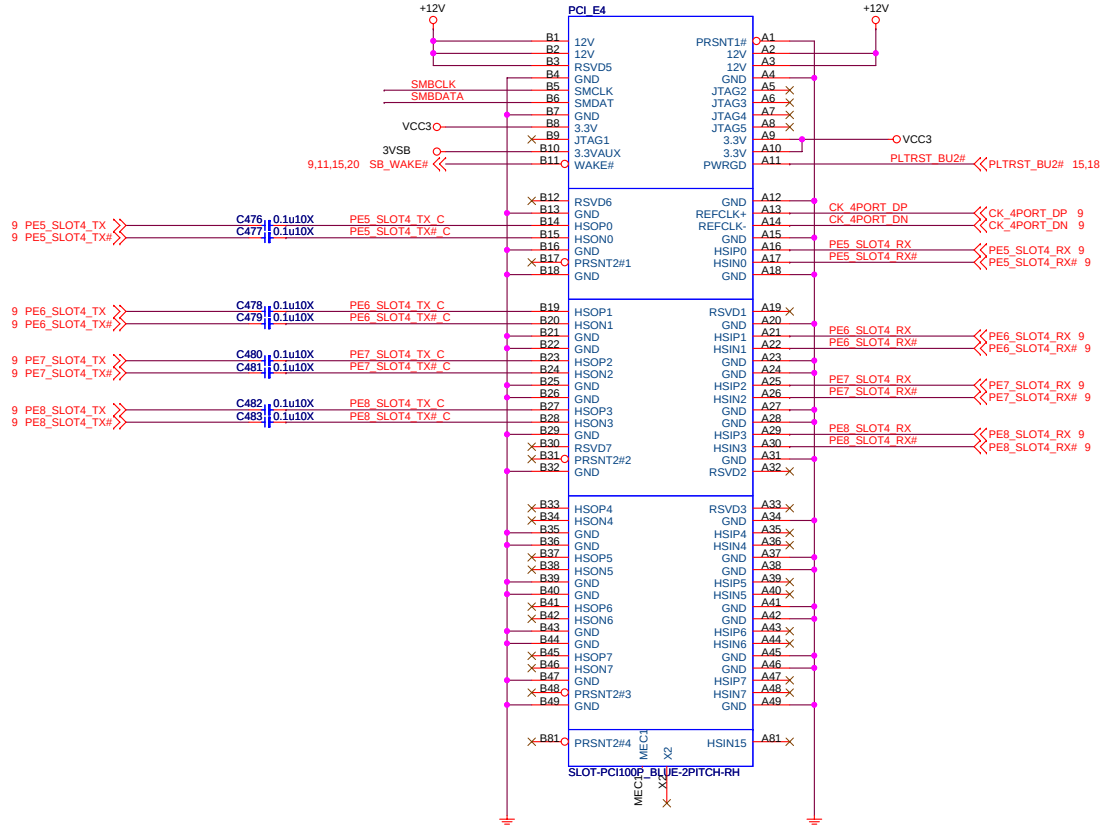
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PPT Strap	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 14 of 43	

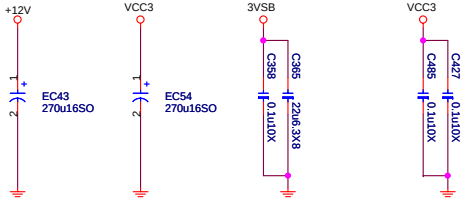


MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PCIE1(X1) & PCIE2(X16) Slots	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 15 of 43	

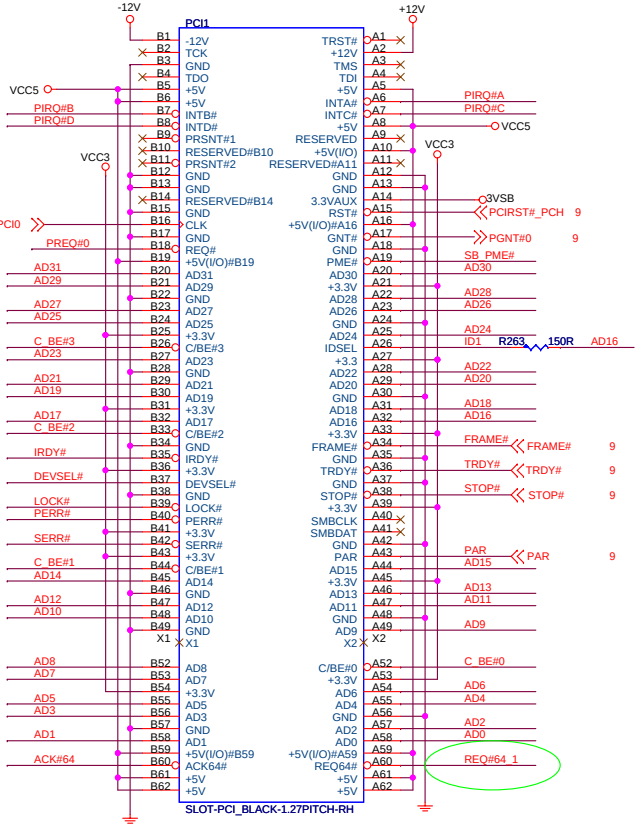
PCI_Express X4 Slot



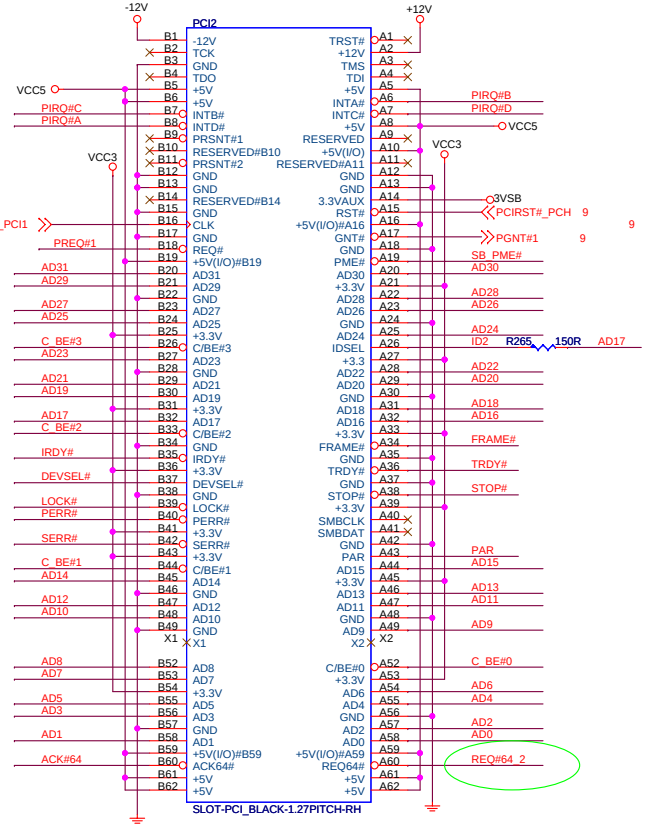




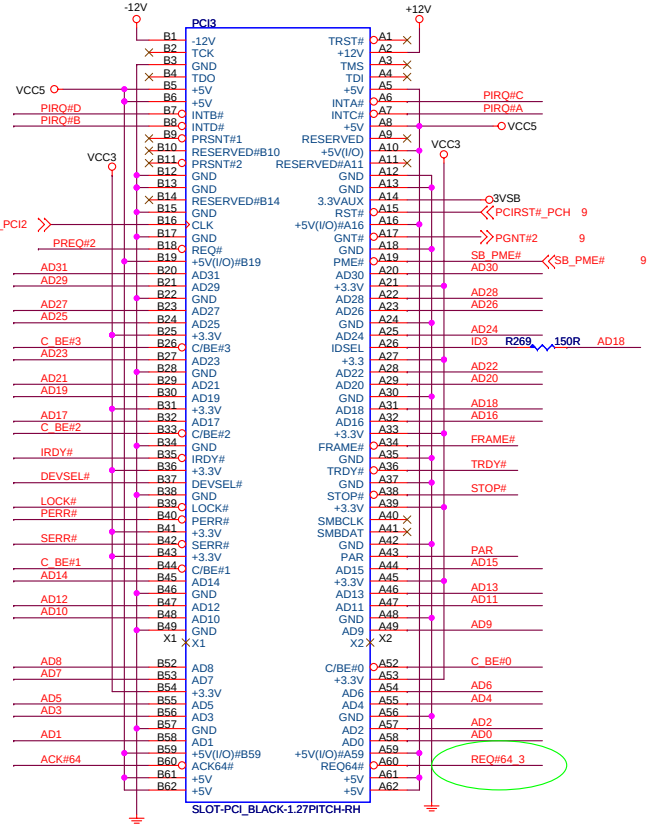
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PCIE3(X1) & PCIE4(X4.) Slots	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 16 of 43	



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



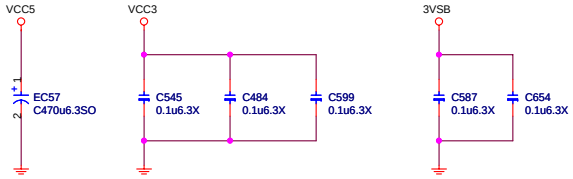
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B



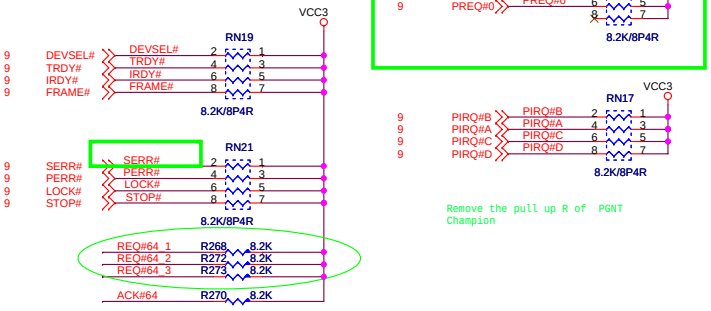
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

AD[31..0] — AD[31..0] 9

C_BE#[3..0] — C_BE#[3..0] 9

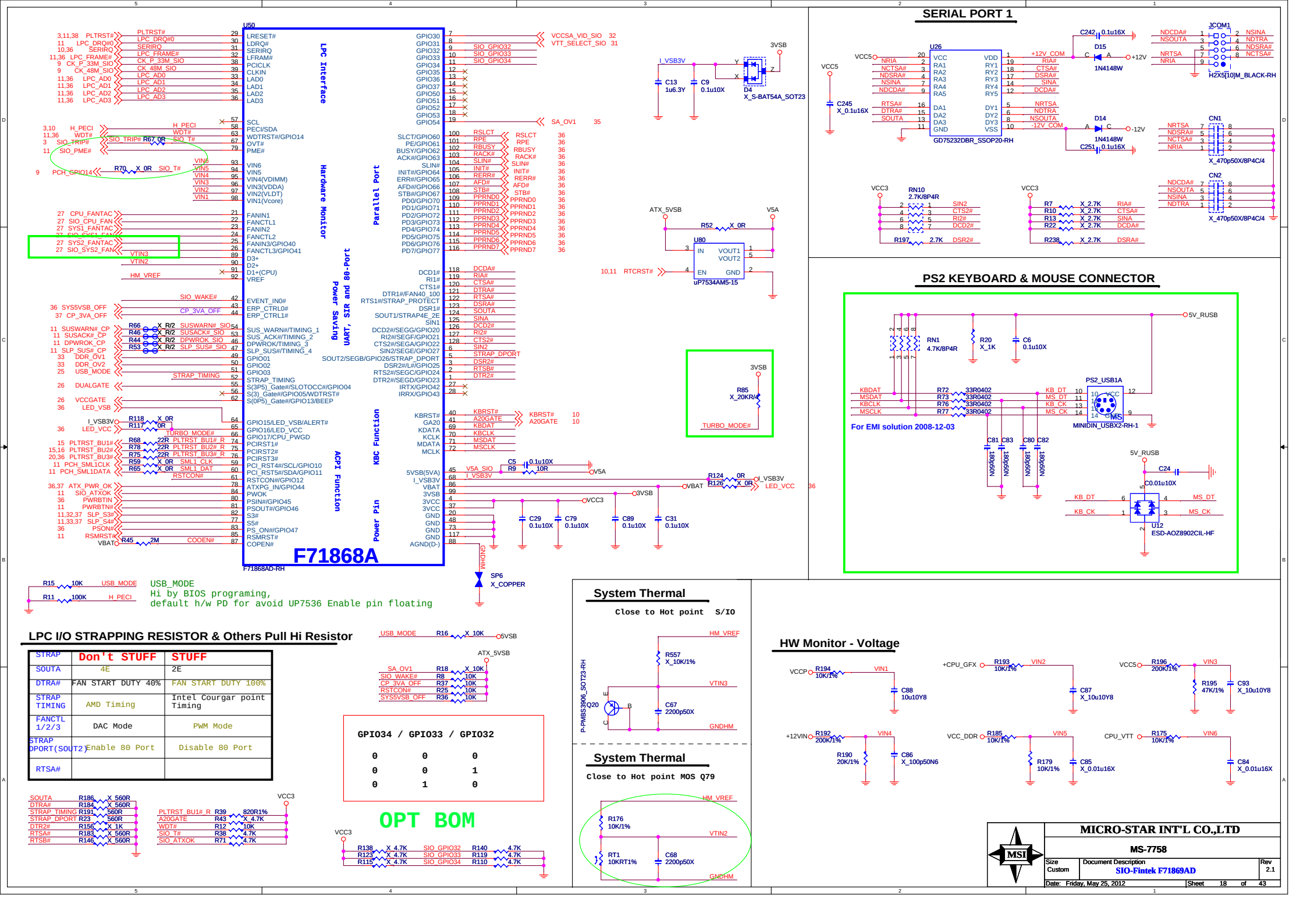


PCI PULL-UP / DOWN RESISTORS

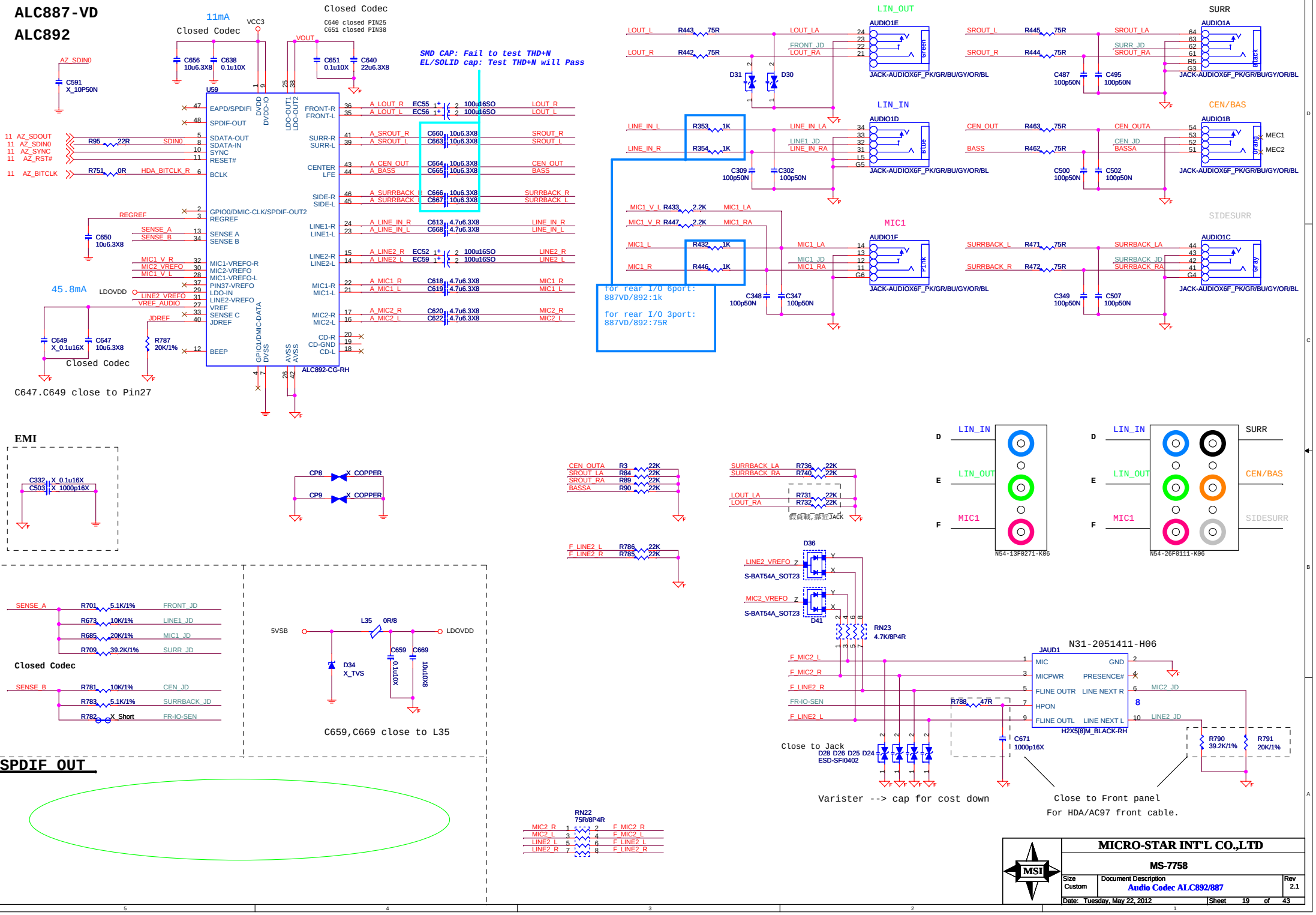


PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A

MICRO-STAR INT'L CO.,LTD	
MS-7758	
Size: Custom	Document Description: PCIx1 Slots — Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 17 of 43


U50
F71868A
F71868AD-RH
LPC Interface
Hardware Monitor
Parallel Port
Power Saving
UART, SIR and 80-Port
KBC Function
ACPI Function
Power Pin
SERIAL PORT 1
PS2 KEYBOARD & MOUSE CONNECTOR
For EMI solution 2008-12-03
USB_MODE
Hi by BIOS programing,
default h/w PD for avoid UP7536 Enable pin floating
LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor
STRAP | Don't STUFF | STUFF
SOUTA | 4E | 2E
DTRA# | FAN START DUTY 40% | FAN START DUTY 100%
STRAP TIMING | AMD Timing | Intel Cougar point Timing
FANCTL 1/2/3 | DAC Mode | PWM Mode
STRAP DPORT(SOUT2) | Enable 80 Port | Disable 80 Port
RTSA#
GPIO34 / GPIO33 / GPIO32
0 0 0
0 0 1
0 1 0
OPT BOM
System Thermal
Close to Hot point S/IO
System Thermal
Close to Hot point MOS Q79
HW Monitor - Voltage
MICRO-STAR INT'L CO.,LTD
MS-7758
SIO-Fintek F71869AD
Rev 2.1
Date: Friday, May 25, 2012
Sheet 18 of 43

ALC887-VD
ALC892



EMI

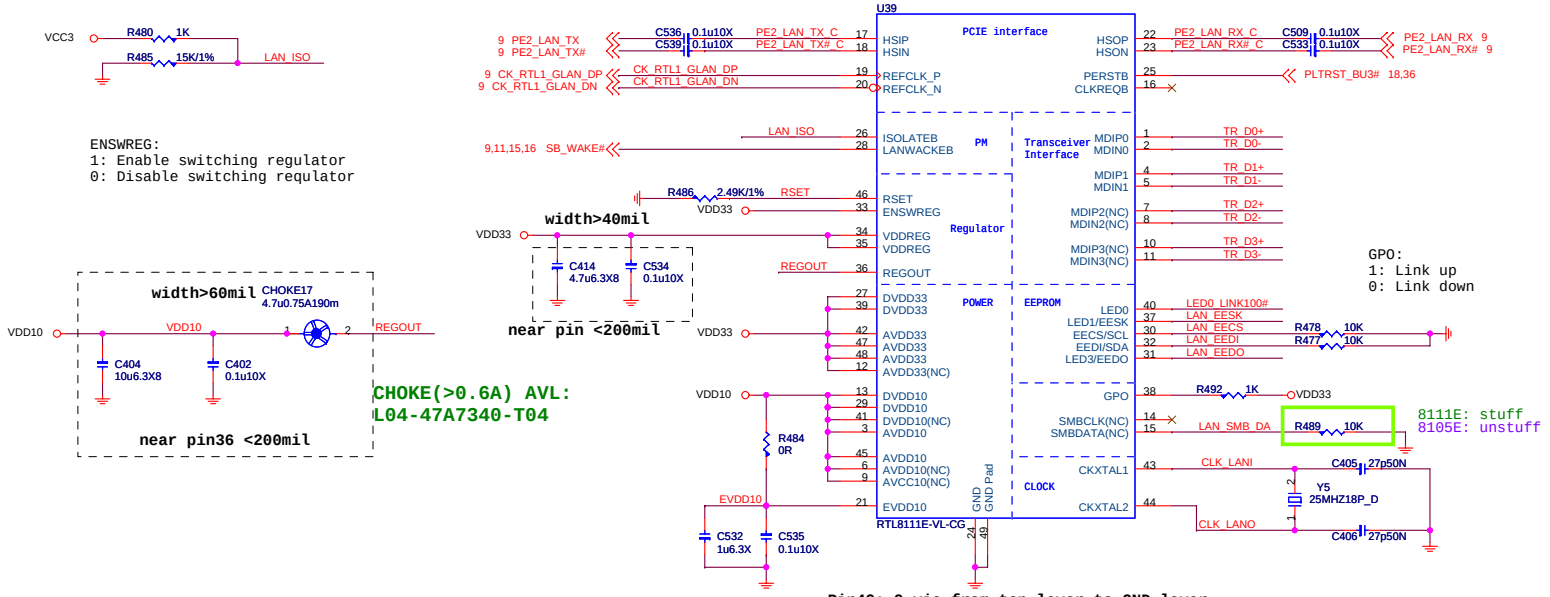
C659,C669 close to L35

SPDIF_OUT

MICRO-STAR INT'L CO.,LTD	
MS-7758	
Size: Custom	Document Description: Audio Codec ALC892/887
Rev: 2.1	
Date: Tuesday, May 22, 2012	Sheet 19 of 43

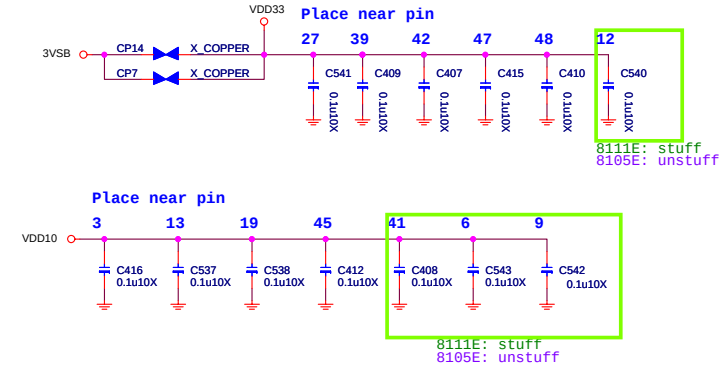
RTL8111E Giga LAN

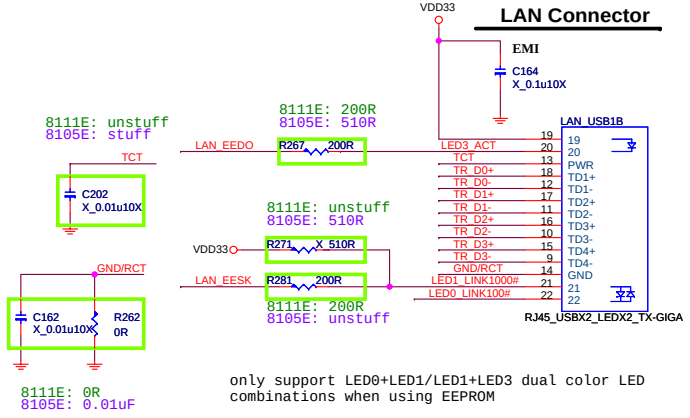
RTL8105E 10/100M LAN



3.3v Power on rise time : 1~100ms.

MAX: 218mA





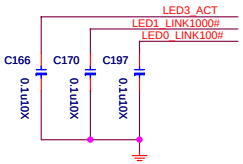
Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19, 20, 250R, Yellow 21, 22, 250R, Orange, Green	19, 20, Yellow 21, 22, Green

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11



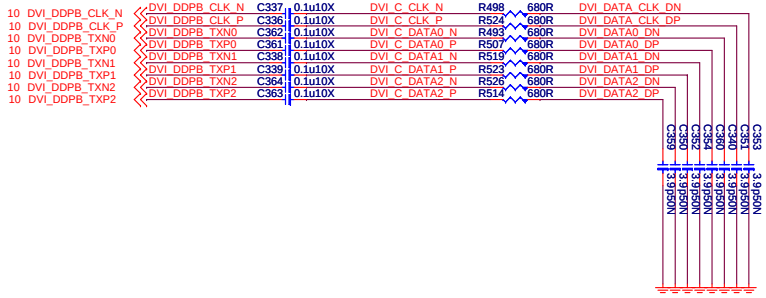
MICRO-STAR INT'L CO.,LTD

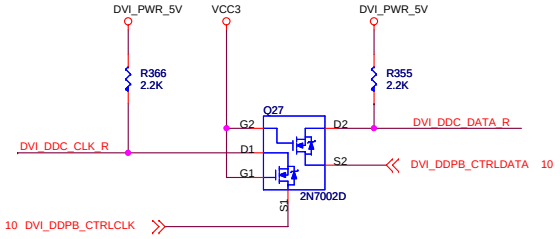
MS-7758

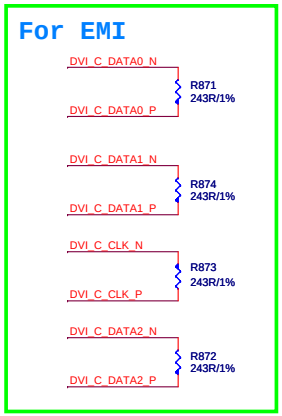
Size	Document Description	Rev
Custom	LAN-RTL8111E/8105E	2.1

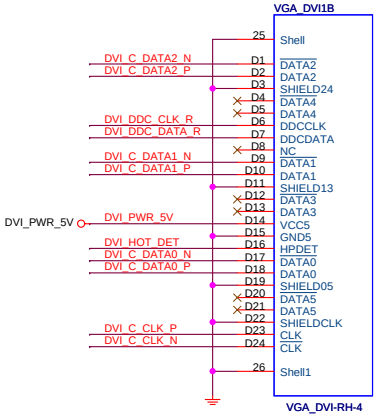
Date: Tuesday, May 22, 2012 Sheet 20 of 43

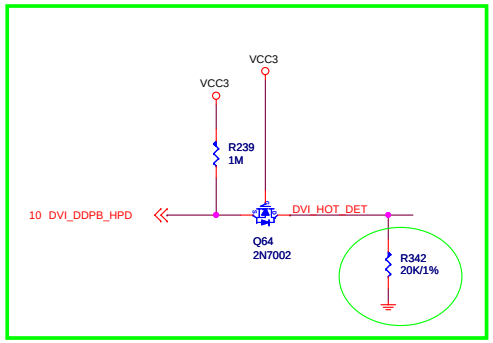
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

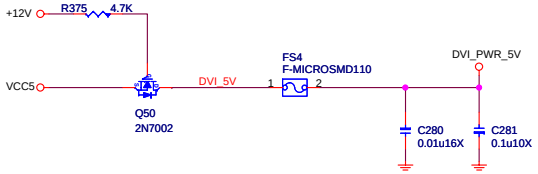


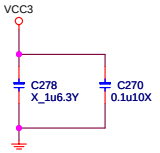


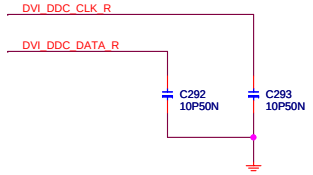












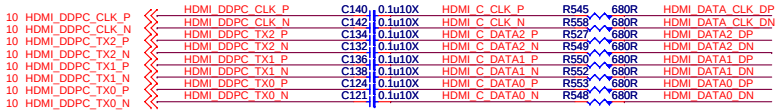
MICRO-STAR INT'L CO.,LTD

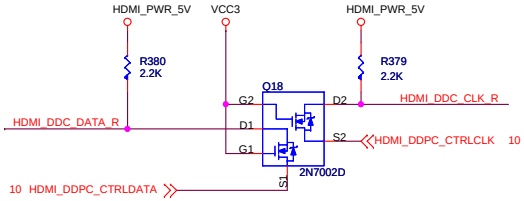
MS-7758

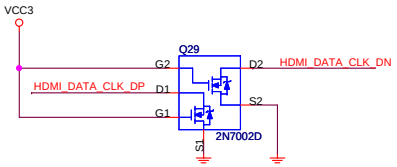
Size	Document Description	Rev
Custom	DVI Connector	2.1

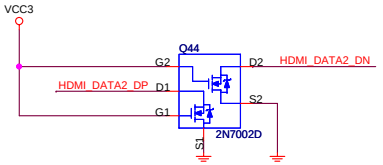
Date: Tuesday, May 22, 2012 Sheet 21 of 43

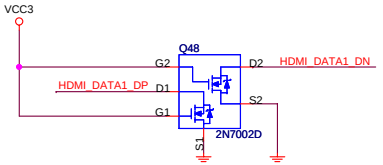
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

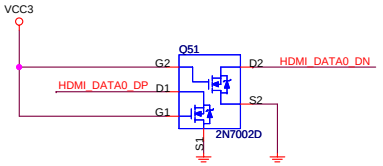


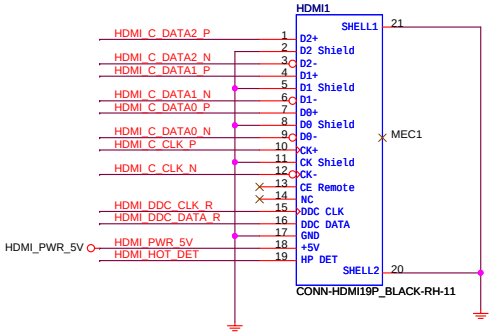


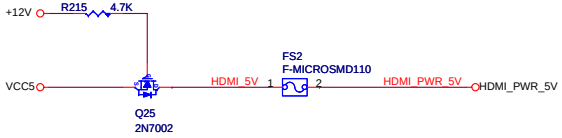


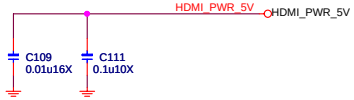


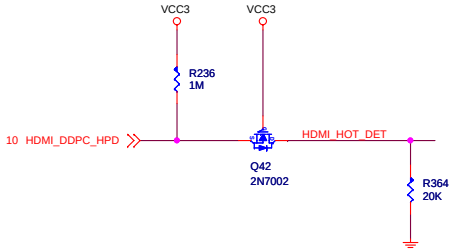


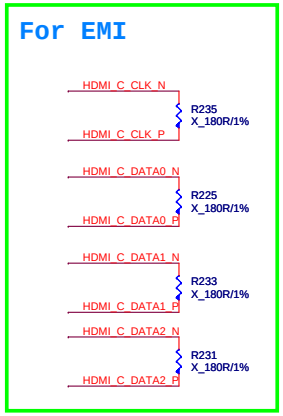


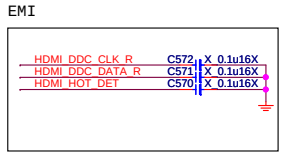










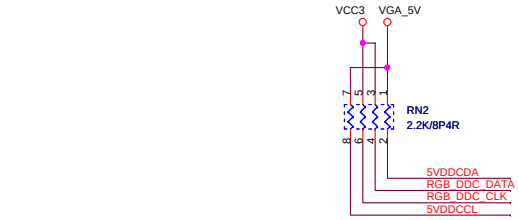


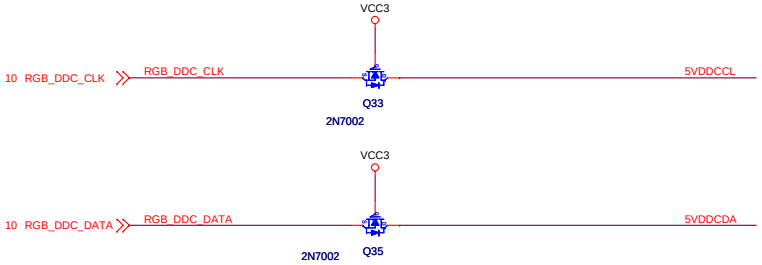
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: HDMI Connector	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 22 of 43	

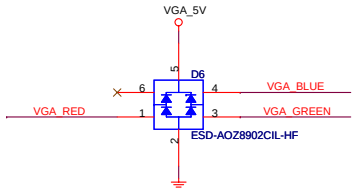
D-Sub

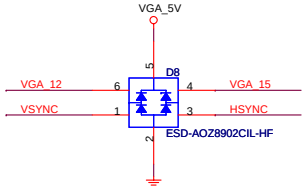
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

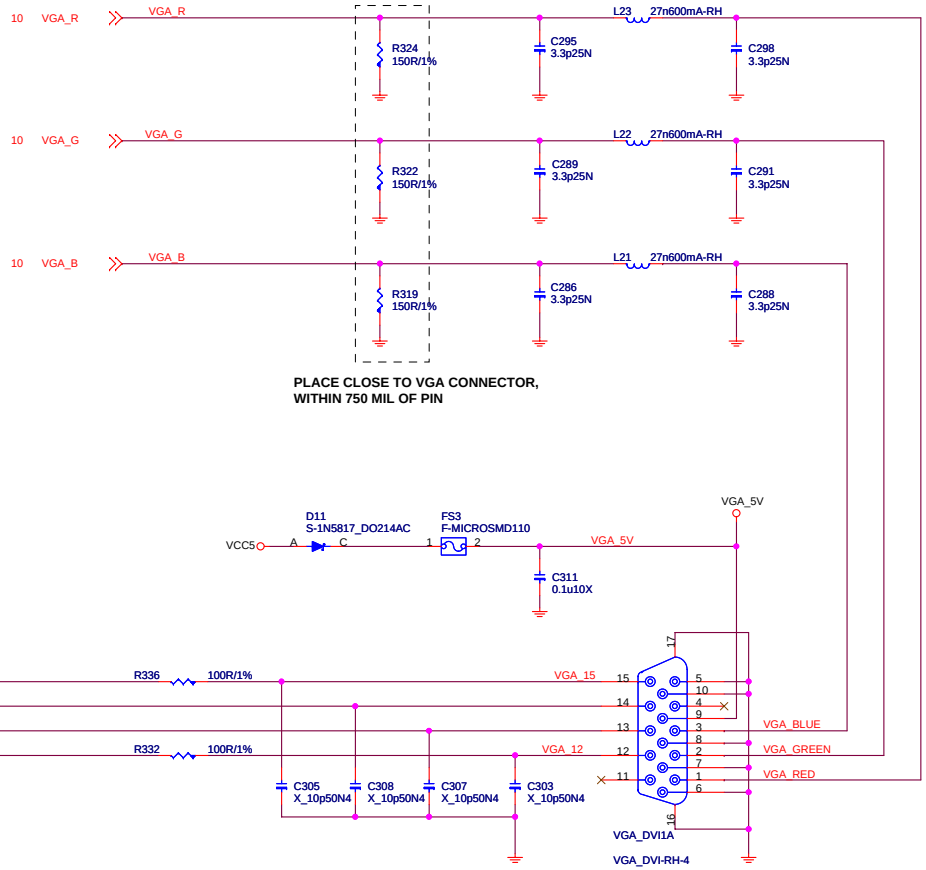
Level shift











MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: VGA Connector	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 23 of 43	

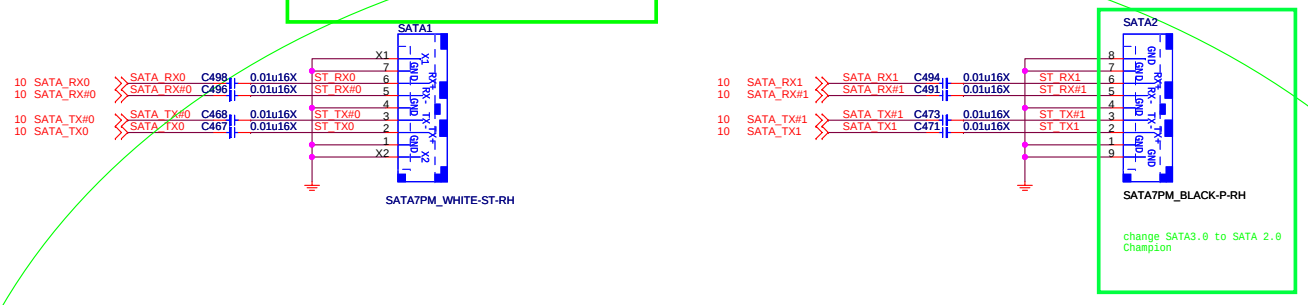
change SATA6G PORT0,1 to SATA PORT 0

SATA 6G PORT 0

3.0 white

add SATA 3G PORT 1
Champion

SATA 3G PORT 1

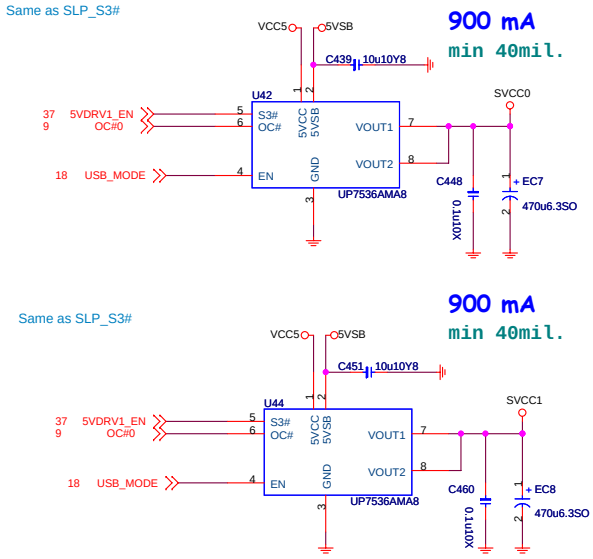


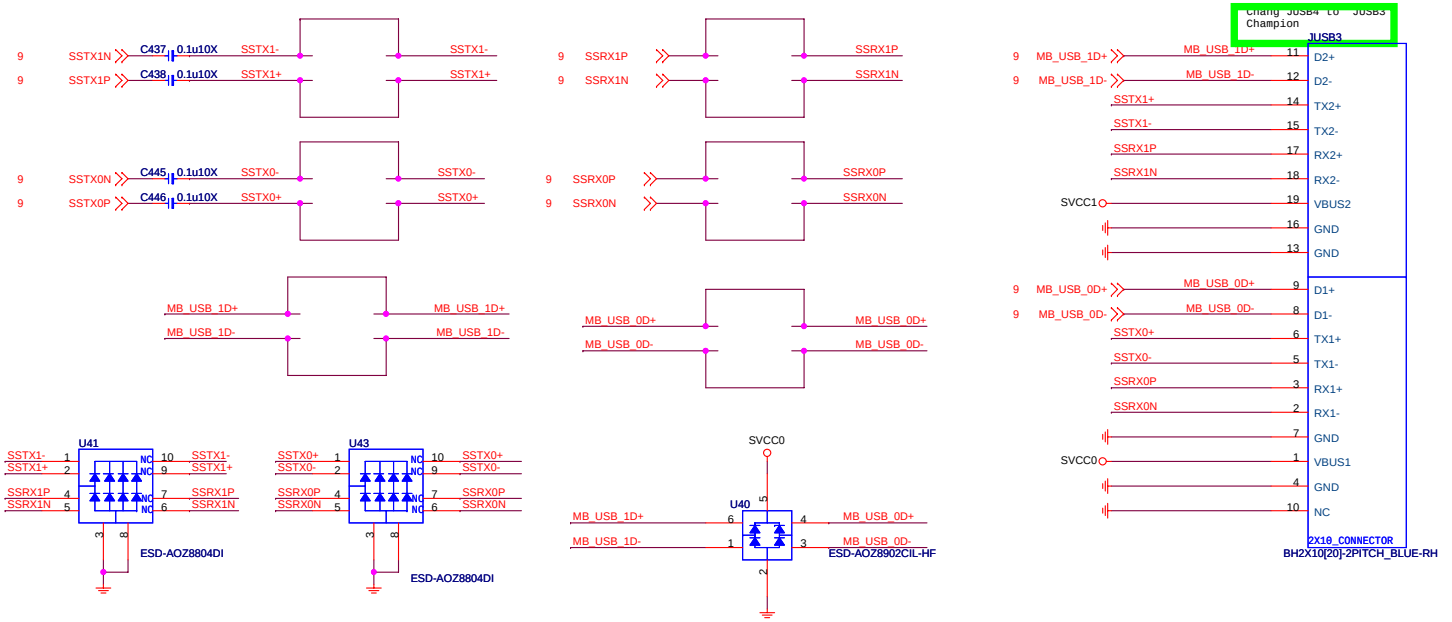
SATA 3G PORT 2,3

SATA 3G PORT 4,5

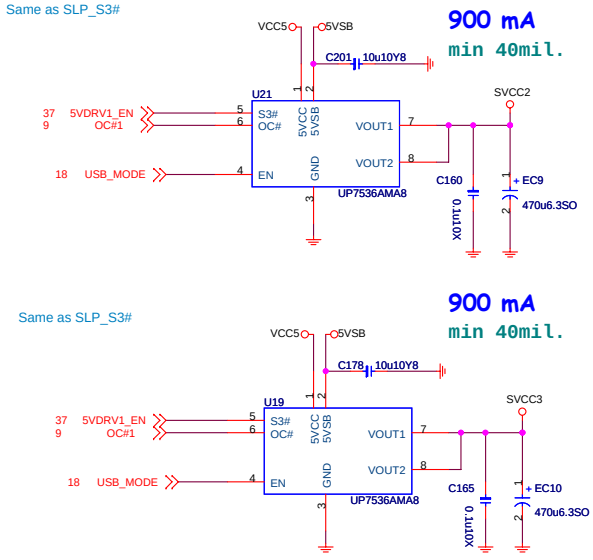
MICRO-STAR INT'L CO.,LTD	
MS-7758	
Size: Custom	Document Description: SATA Connector
Rev: 2.1	
Date: Tuesday, May 22, 2012	Sheet 24 of 43

FRONT USB30 PORT 0,1





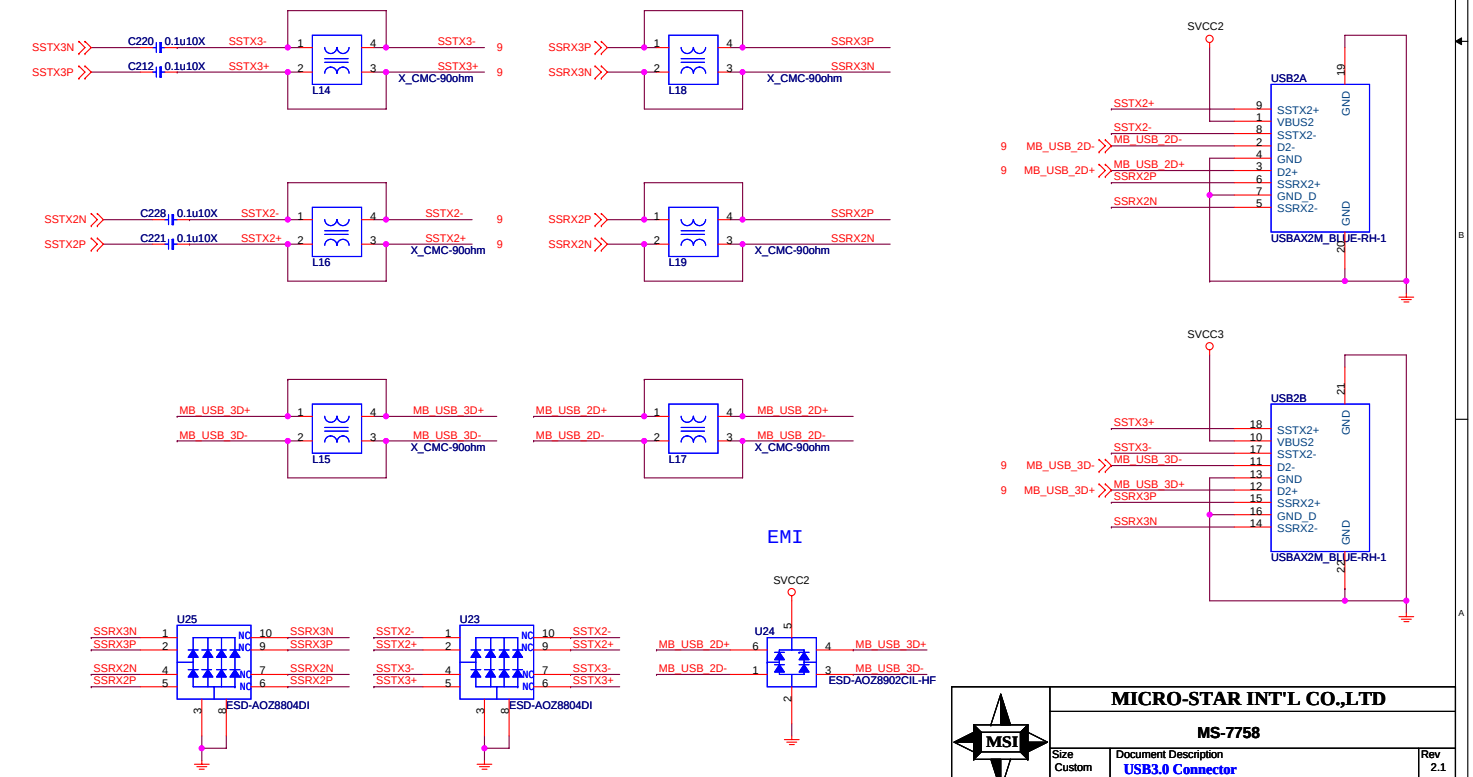
REAR USB30 PORT 2,3



USB_MODE
Hi by BIOS programing,
default h/w PD for avoid UP7536 Enable pin floating

USB_MODE States

MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: USB3.0 Connector	Rev: 2.1
Date: Thursday, May 24, 2012	Sheet 25 of 43	

USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

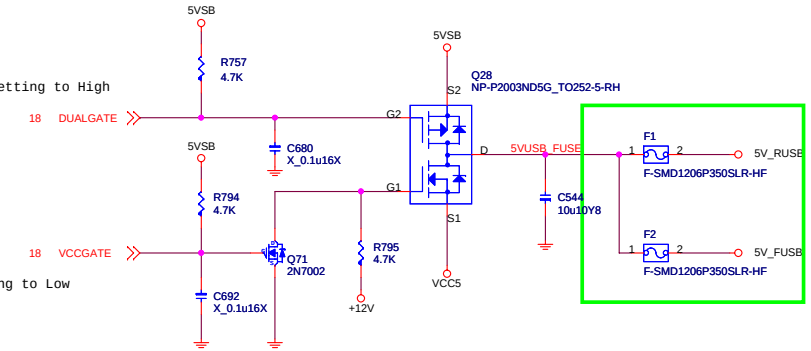
When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

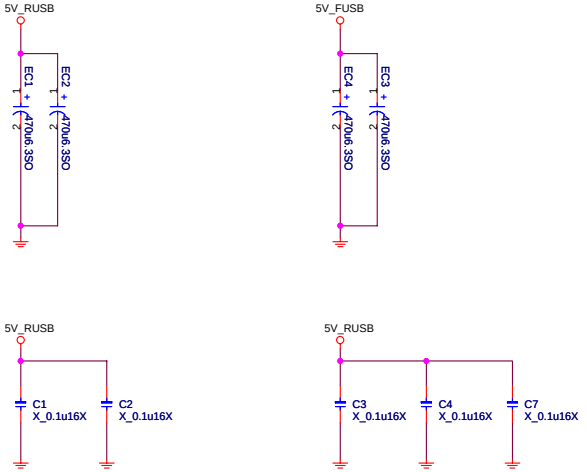
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

When PS2 in S5 support wake , S3P5_Gate# in S5 must setting to Low

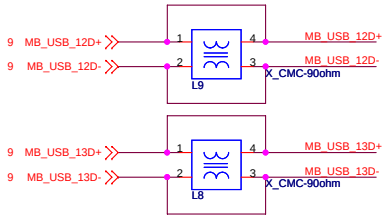
*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

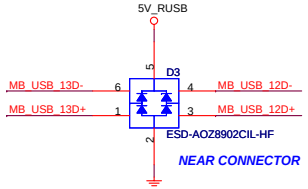
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue

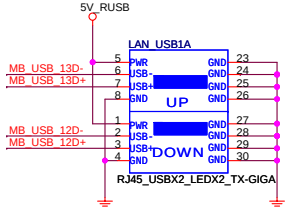




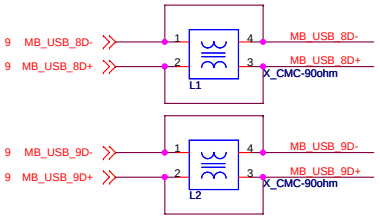
REAR USB PORT 8,9 (With LAN)

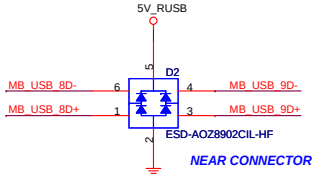


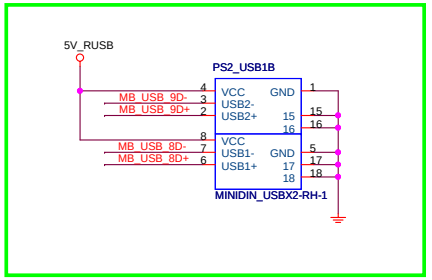




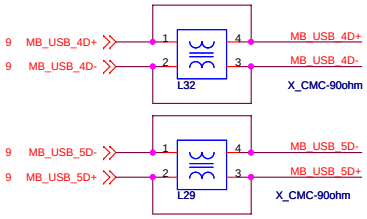
REAR USB PORT 8,9 (With PS2)

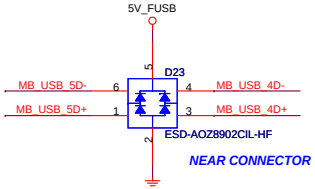


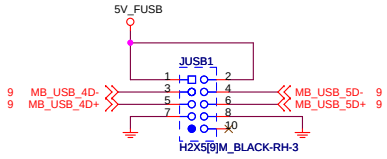




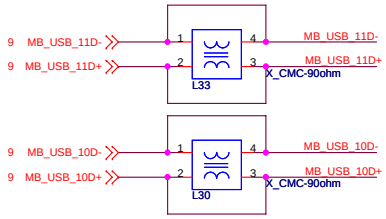
FRONT USB PORT 0,1

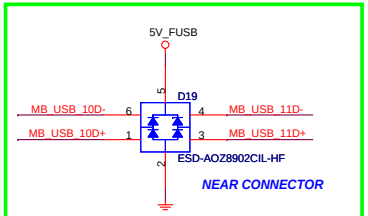


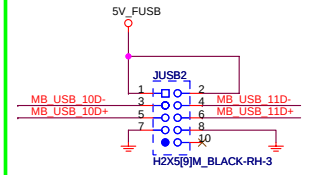




FRONT USB PORT 8,9







Remove USB2.0 PORT 10,11
USB6&USB7
Champion

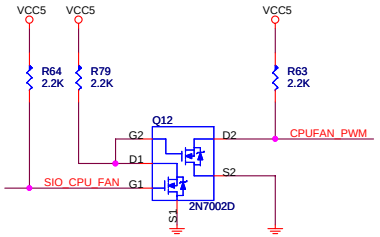
MICRO-STAR INT'L CO.,LTD

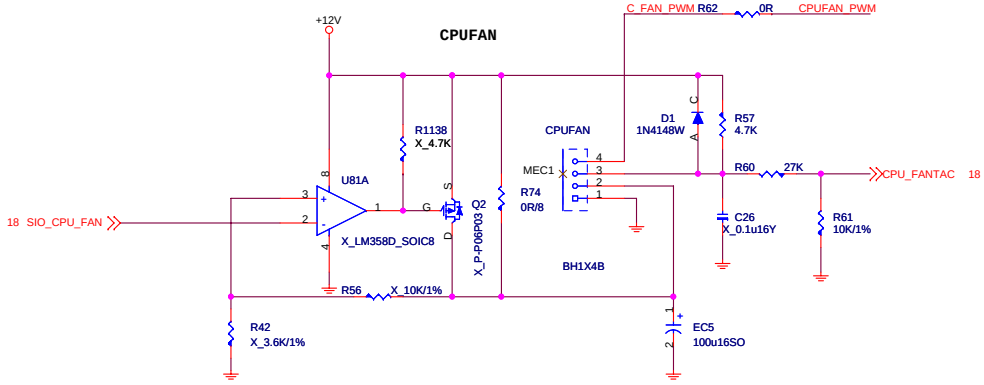
MS-7758

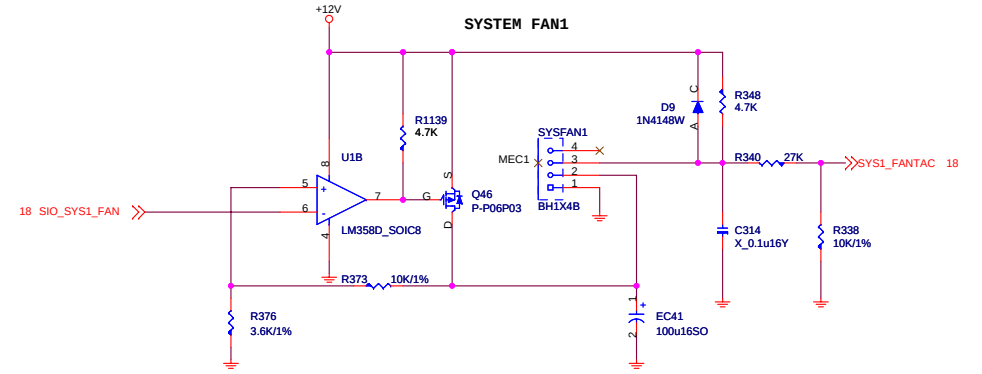
Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	2.1

Date: Thursday, May 24, 2012 Sheet 26 of 43

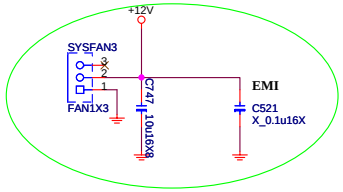
FAN-COUNTROL CIRCUIT



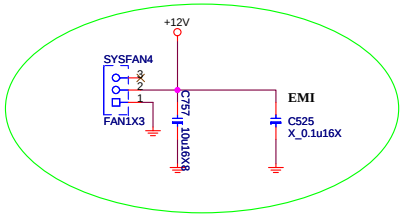


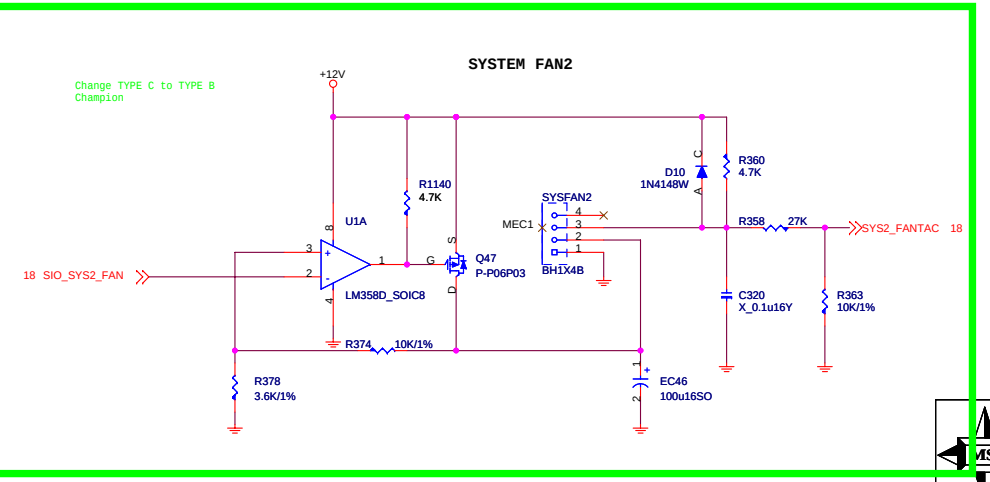


SYSTEM FAN3



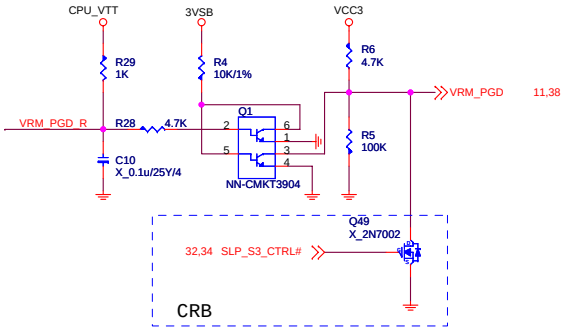
SYSTEM FAN4

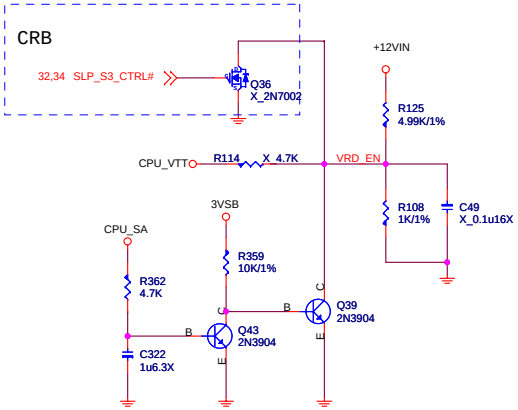


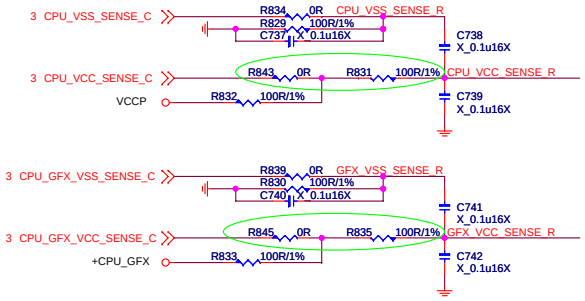


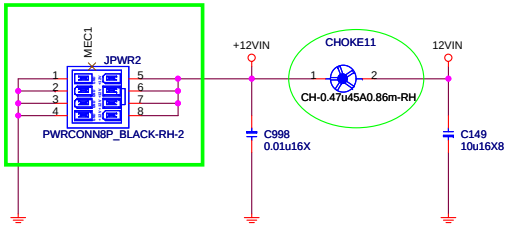
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: FAN Control	Rev: 2.1
Date: Friday, May 25, 2012	Sheet 27 of 43	

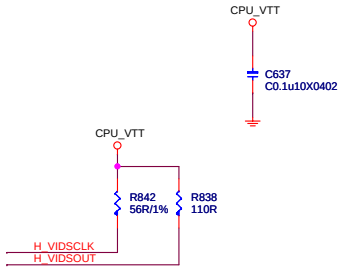
VRMPWRGD LEVEL SHIFT



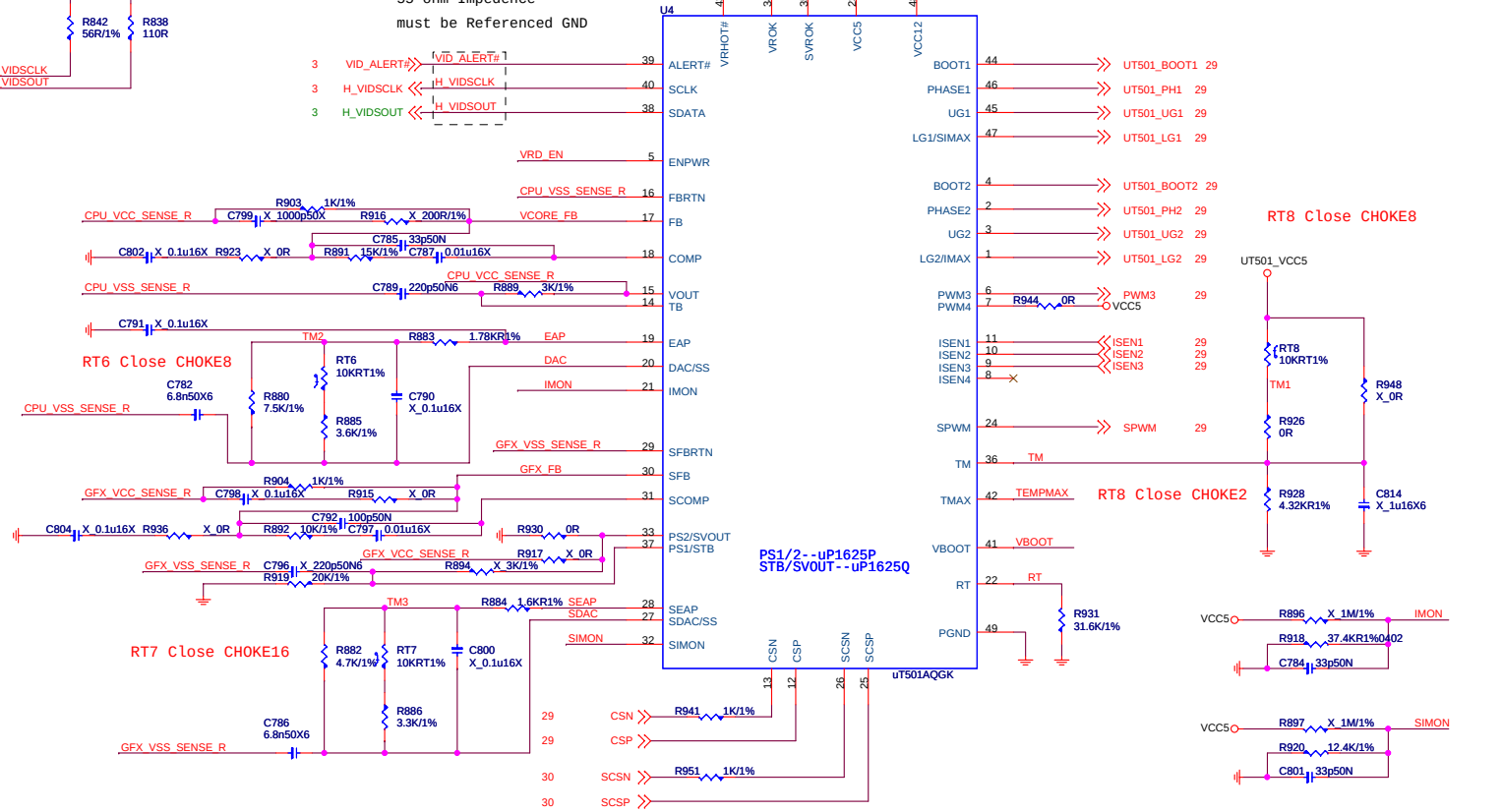








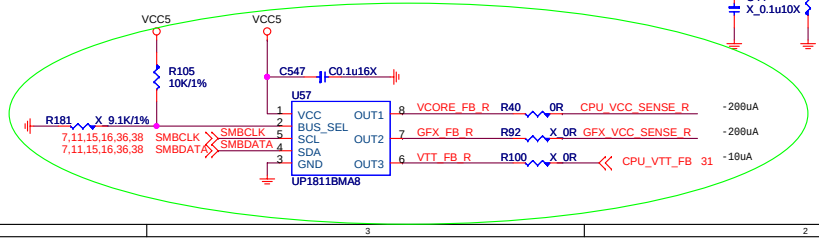
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND

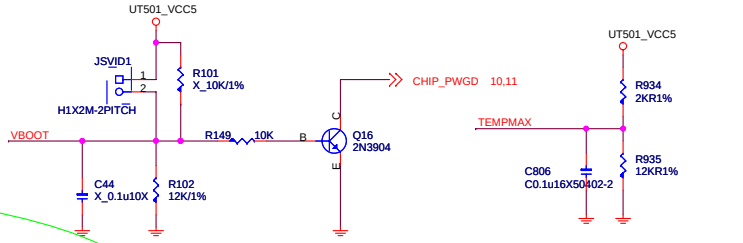


UPI VOLTAGE CONSOLE

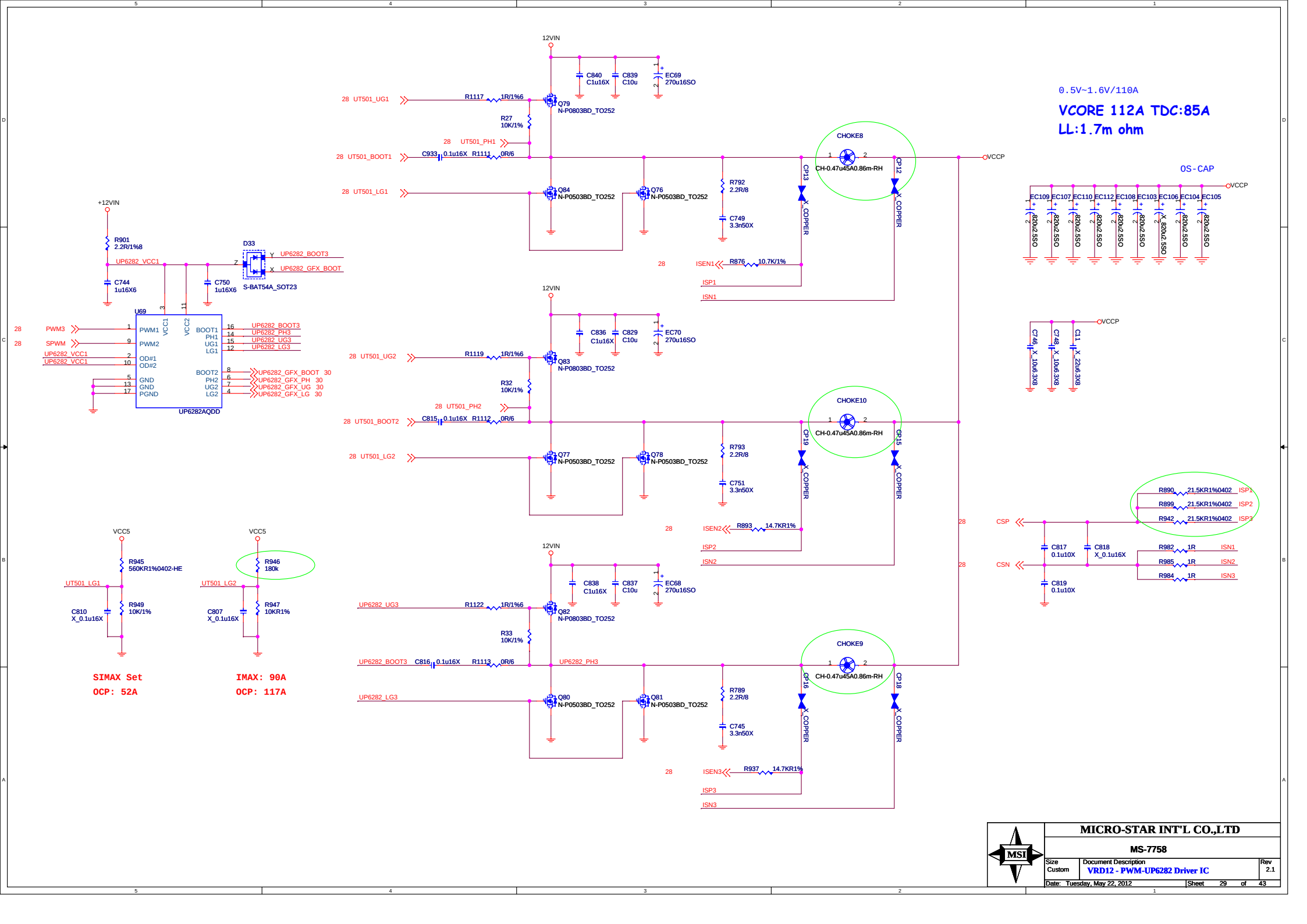
0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



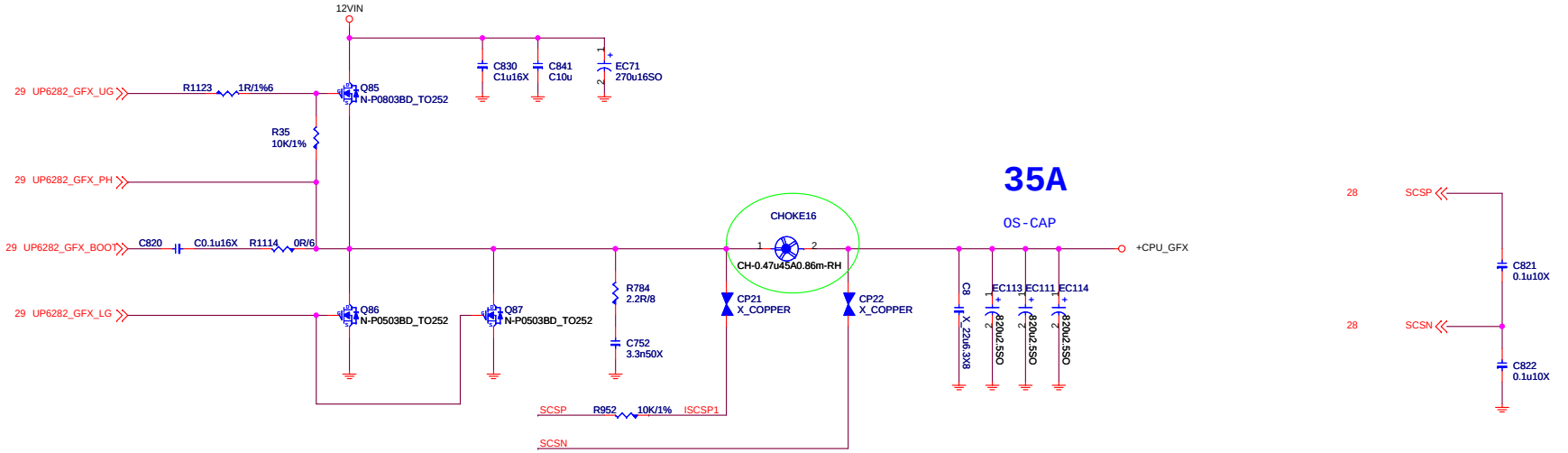


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7758	
Size: Custom	Document Description: VRD12 - PWM-UT501	Rev: 2.1
Date: Friday, May 25, 2012	Sheet 28 of 43	


0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm
OS-CAP
12VIN
+12VIN
VCCP
VCC5
U69
UP6282AQDD
PWM3
SPWM
UP6282_VCC1
UP6282_BOOT3
UP6282_PH3
UP6282_UG3
UP6282_LG3
UP6282_GFX_BOOT 30
UP6282_GFX_PH 30
UP6282_GFX_UG 30
UP6282_GFX_LG 30
D33
S-BAT54A_SOT23
R901 2.2R/1%8
C744 1u16X6
C750 1u16X6
UT501_UG1
UT501_LG1
UT501_PH1
UT501_BOOT1
UT501_UG2
UT501_LG2
UT501_PH2
UT501_BOOT2
UP6282_UG3
UP6282_BOOT3
UP6282_PH3
UP6282_LG3
CHOKE8
CHOKE10
CHOKE9
CH-0.47u45A0.86m-RH
Q79 N-P0803BD_TO252
Q84 N-P0503BD_TO252
Q76 N-P0503BD_TO252
Q83 N-P0803BD_TO252
Q77 N-P0503BD_TO252
Q78 N-P0503BD_TO252
Q82 N-P0803BD_TO252
Q80 N-P0503BD_TO252
Q81 N-P0503BD_TO252
R1117 1R/1%6
R1119 1R/1%6
R1122 1R/1%6
R27 10K/1%
R32 10K/1%
R33 10K/1%
R1111 0R/6
R1112 0R/6
R1113 0R/6
C933 0.1u16X
C815 0.1u16X
C816 0.1u16X
R792 2.2R/8
R793 2.2R/8
R789 2.2R/8
C749 3.3n50X
C751 3.3n50X
C745 3.3n50X
R876 10.7K/1%
R893 14.7KR1%
R937 14.7KR1%
ISEN1
ISEN2
ISEN3
ISP1
ISP2
ISP3
ISN1
ISN2
ISN3
CP13 X_COPPER
CP12 X_COPPER
CP19 X_COPPER
CP15 X_COPPER
CP16 X_COPPER
CP18 X_COPPER
C840 C1u16X
C839 C10u
EC69 270u16SO
C836 C1u16X
C829 C10u
EC70 270u16SO
C838 C1u16X
C837 C10u
EC68 270u16SO
EC109 EC107 EC110 EC112 EC108 EC103 EC106 EC104 EC105
820u2.5SO
C746 X_10u6.3X8
C748 X_10u6.3X8
C11 X_22u6.3X8
R890 21.5KR1%0402
R899 21.5KR1%0402
R942 21.5KR1%0402
CSP
CSN
C817 0.1u10X
C818 X_0.1u16X
C819 0.1u10X
R982 1R
R985 1R
R984 1R
R945 560KR1%0402-HE
R949 10K/1%
C810 X_0.1u16X
R946 180k
R947 10KR1%
C807 X_0.1u16X
SIMAX Set
OCP: 52A
IMAX: 90A
OCP: 117A
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description
VRD12 - PWM-UP6282 Driver IC
Rev 2.1
Date: Tuesday, May 22, 2012
Sheet 29 of 43

CPU_GFX:0.25-1.52

35A FOR CPU



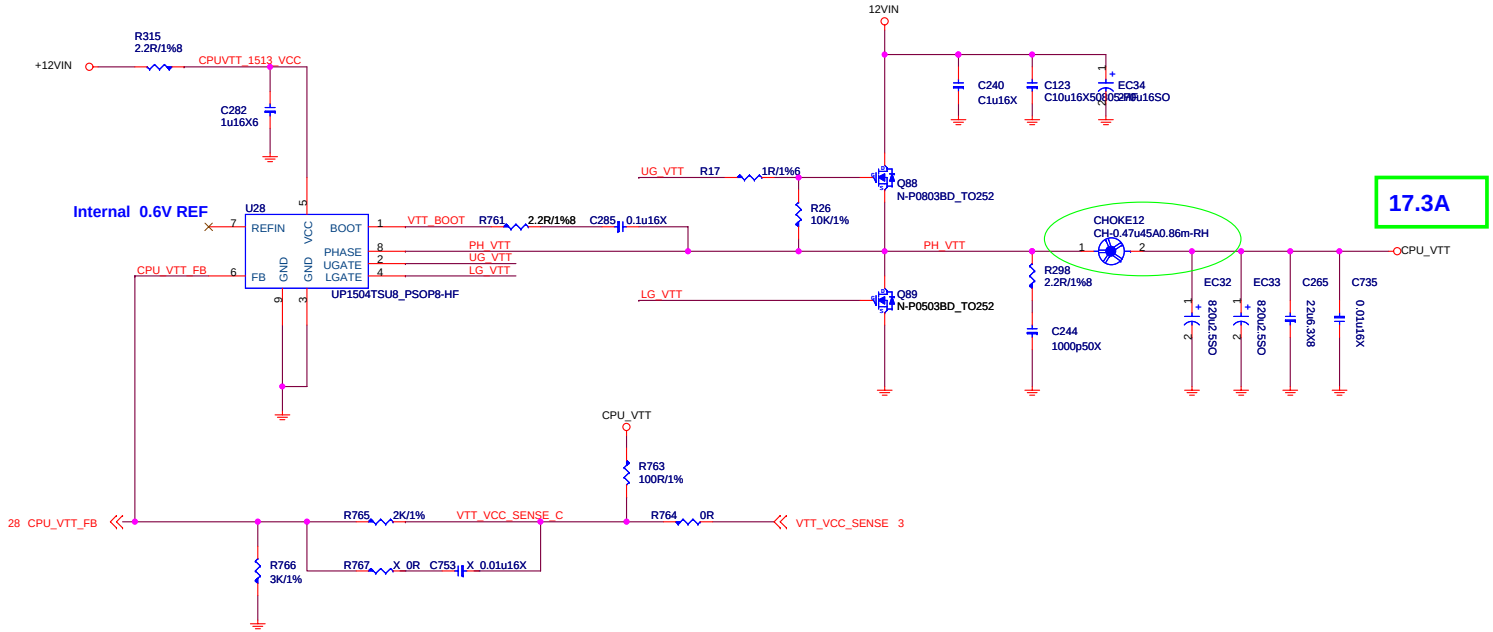
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: VRD12 -GPU 1-Phase MOS	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 30 of 43	

CPU_VTT:1.05/1.00 MAX 17.3A

CPU VTT 8.5A SA Core =8.8A

8.5A FOR CPU

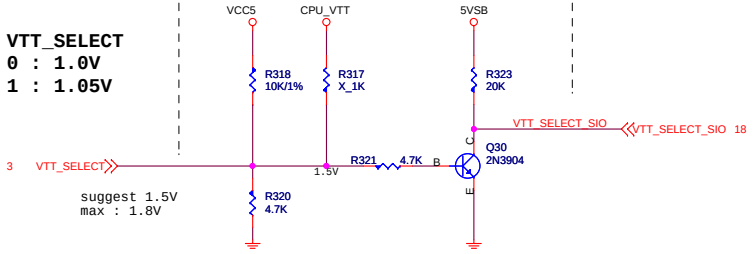
Iripple=1.92(vtt)+1.88(sa)
5*1=5A>3.8A

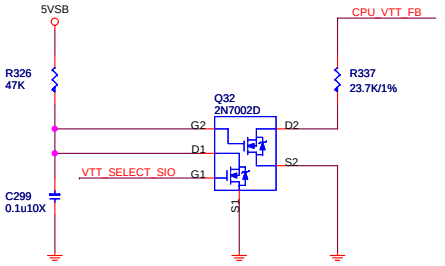


VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

VTT_SELECT
0 : 1.0V
1 : 1.05V

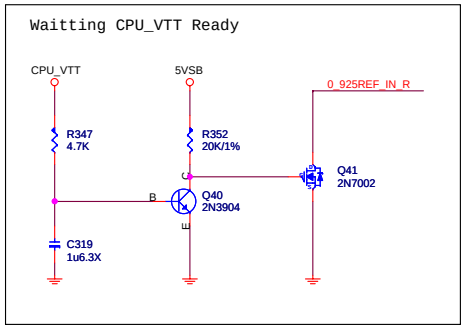


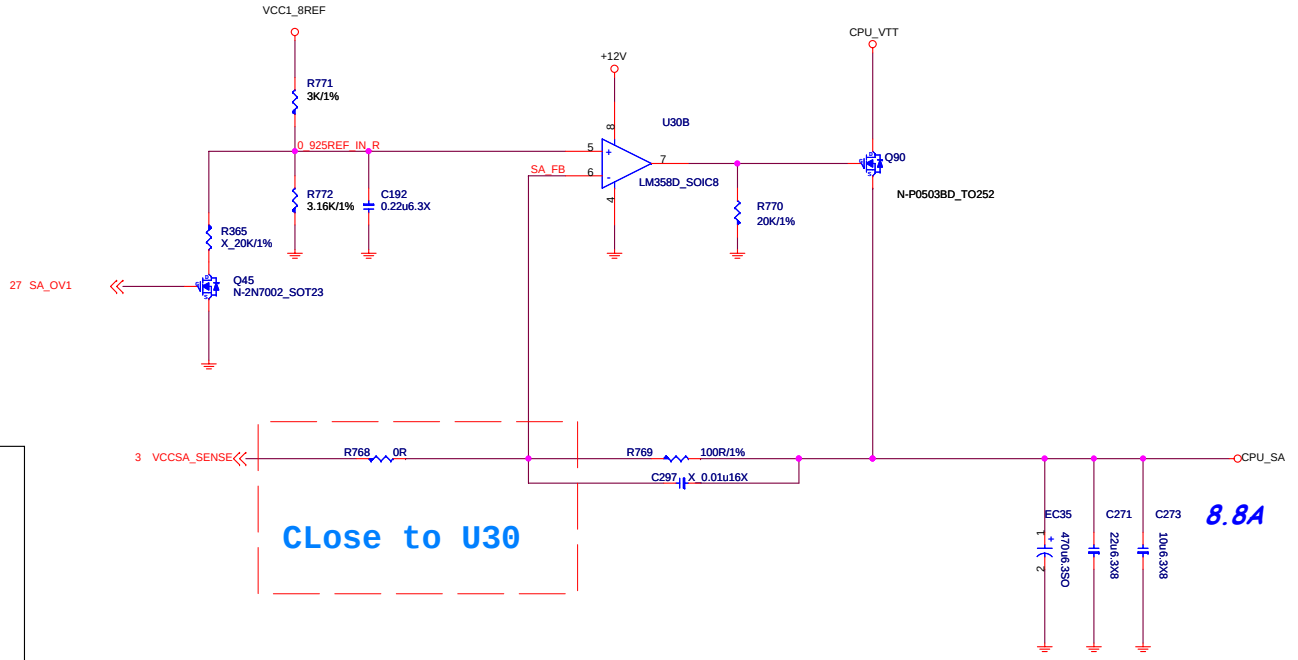


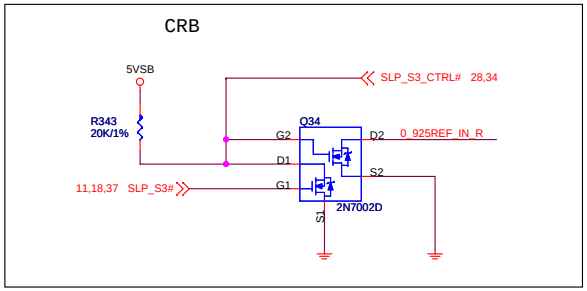
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7758	
Size: Custom	Document Description: VTT POWER- uP1513- 1Phase MOS	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 31 of 43	

CPU_SA:0.925/0.85

SA Core =8.8A

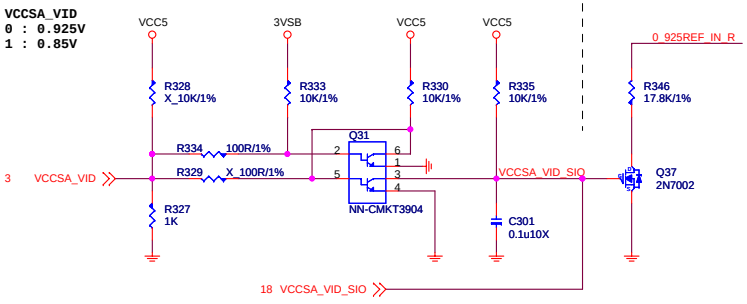






VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	CPU_SA OP+MOS 1-Phase	2.1

Date: Friday, May 25, 2012 Sheet 32 of 43

DDR Power:1.5V

DDR3_1.5V 4.75A+11A+1A=16.75A

4.75A FOR CPU
11A FOR 4DIMM
1A FOR DDR VTT

Iripple=8A
4.7*2*1=9.4A>8A

(OS-CON CAP)

5VDIMM_IN — C99 10u10Y8 — C113 0.1u10X — EC16 470u6.3SO — EC19 470u6.3SO — CHOKE1 CH-1.2u15A1.7m-RH — 5VDIMM — C106 C0.1u25X

D5 S-BAT54C_SOT23 (+12V → 5VDIMM)

R224 2.2R/8 DDR_1513_VCC — C126 1u16X6

DDR OV

5VSB — R339 1K — Q19 2N7002D — R341 X_1K — DDR3_FB — R58 4.02K/1%

18 DDR_OV2 — G2 — D2

DDR3_FB — R55 7.87K1% — D1

18 DDR_OV1 — G1 — S2

R357 X_10KR1%0402 — C59 X_0.1u16X — S1

18 DDR_OV2 — R345 10KR1%0402

*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)

Internal 0.6

VCC_DDR — DDR_0_6_REF_R — R221 2K/1% — DDR3_FB — R223 X_0R — C125 X_0.01u16X — R226 1.58K/1%

U16 UP1504TSU8_PSOP8-HF: REFIN, FB, GND, GND, VCC, BOOT, PHASE, UGATE, LGATE

1513_DDR_BOOT1 — R249 2.2R/8 — C139 0.1u16X

1513_DDR_PH1
1513_DDR_UG1
1513_DDR_LG1

((R221/R226)+1)*0.6=1.5V

DDR3_1.5V

(OS-CON CAP)

CHOKE13 CH-1.1u32A1.4m-RH — VCC_DDR

R261 2.2R/8 — C156 3300p50X

EC28 820u2.5SO — EC31 820u2.5SO — C235 1u6.3Y — C117 22u6.3X8 — C216 10u6.3X6 — C215 10u6.3X6

5VDIMM_IN

1513_DDR_UG1 — Q91 N-P0803BD_TO252

1513_DDR_PH1

1513_DDR_LG1 — Q92 N-P0503BD_TO252 — Q96 N-P0503BD_TO252

ATX_5VSB — R41 10K — DDR3_ENB — Q6 2N7002 — DDR_0_6_REF_R

C18 X_0.1u10X

11,18,37 SLP_S4# — R104 4.7K — Q7 2N3904

37 SLP_S5_LCH# — R112 X_20KR

P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A

VCC5 — C695 0.1u16X

VCC5 — U14 UP0109PSW8_PSOP8-HF: NC3, NC2, VCNTL, NC1, VIN, GND, REFIN, VOUT, GND — 1.25V/2.9A

VCC_DDR — VCC_DDR — R204 10K/1% — DDRVTT_VREF

VTT_DDR — R200 10K/1% — C54 1u10VX8 — C55 22u6.3X8 — C56 22u6.3X8 — EC6 X_820u2.5SO

MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	DDR Power -UP1513 1-Phase MOS	2.1

Date: Thursday, May 24, 2012 — Sheet 33 of 43

PCH Power:1.05V

PCH Core 6.2A+1.8A+0.105A+0.5A+0.08A=8.735A

6.2A FOR PCH

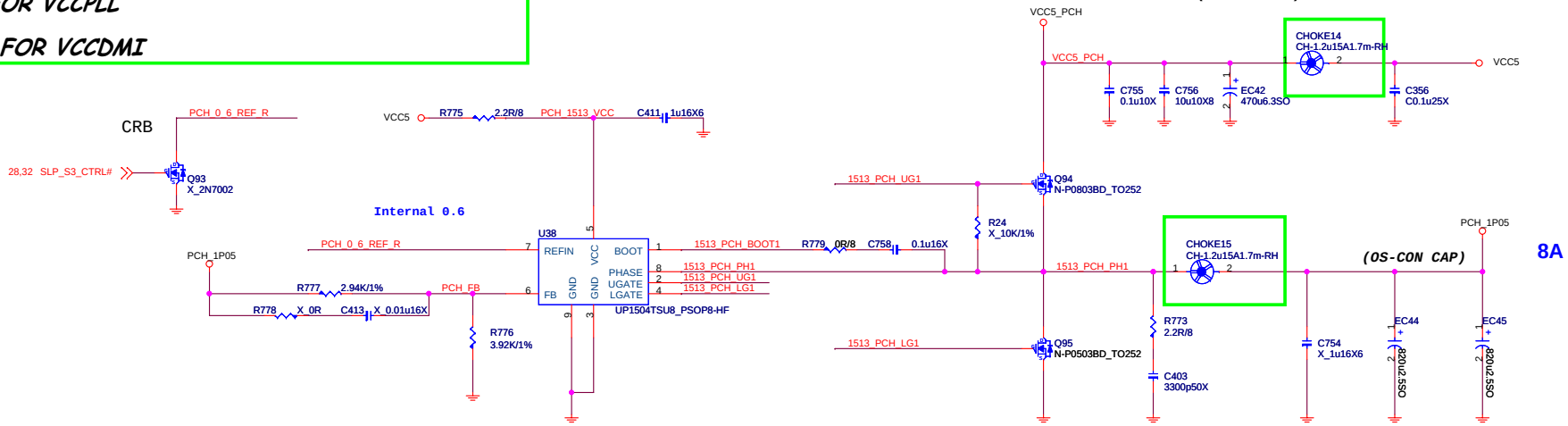
1.8A FOR ME CORE

0.105A FOR VCCSSC

0.5A FOR VCCPLL

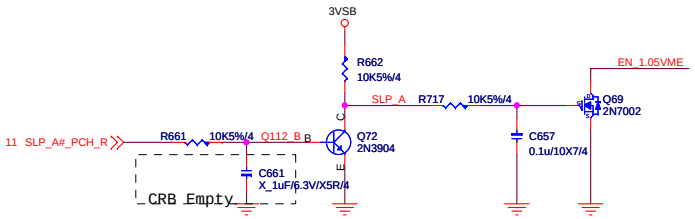
0.08A FOR VCCDMI

Iripple=1.80A
5.08*1=5.08A>1.80A
(OS-CON CAP)



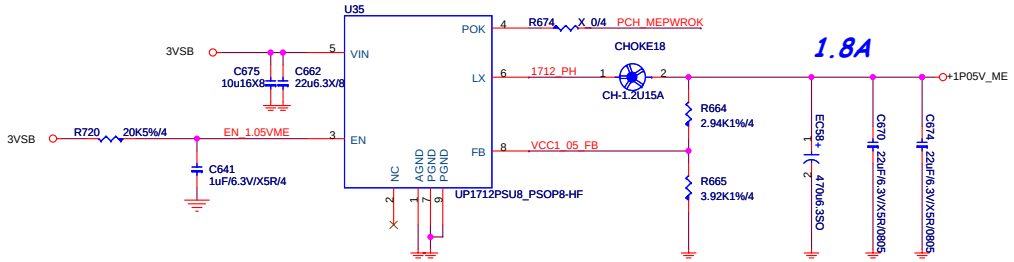
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PCH Power - uP1513 1-Phase MOS	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 34 of 43	

SLP_A

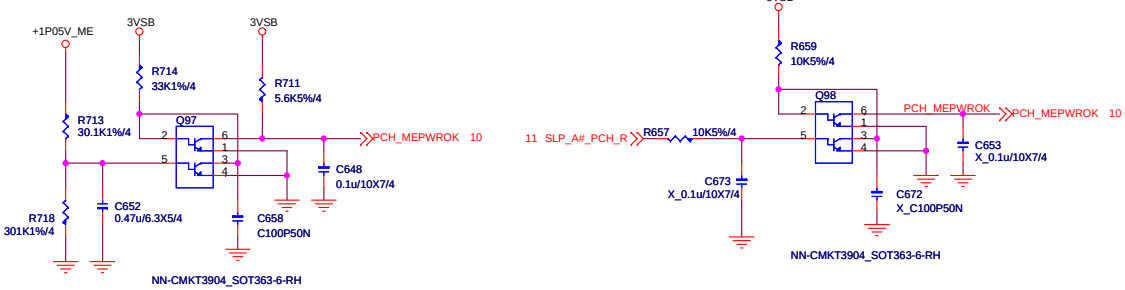


ME Power Control

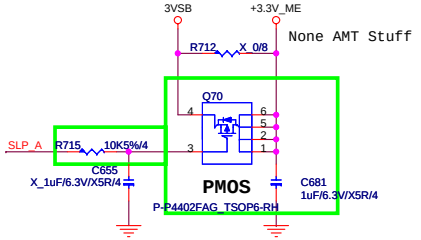
+1.05V_ME(VCCIO_ME)



PCH_MEPWROK



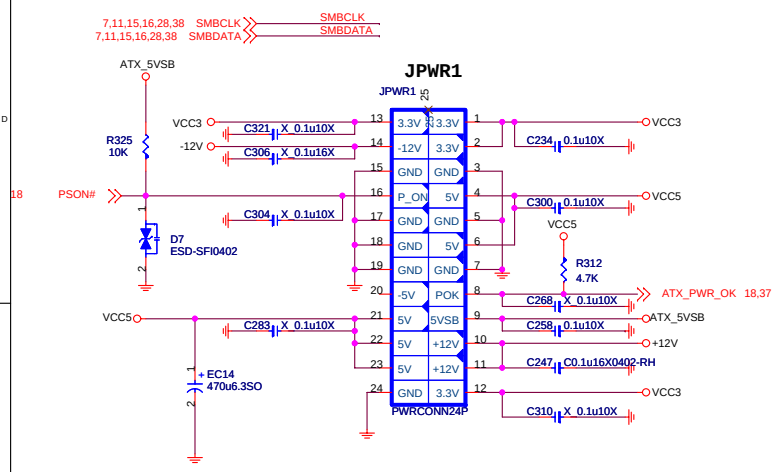
+3.3V_ME



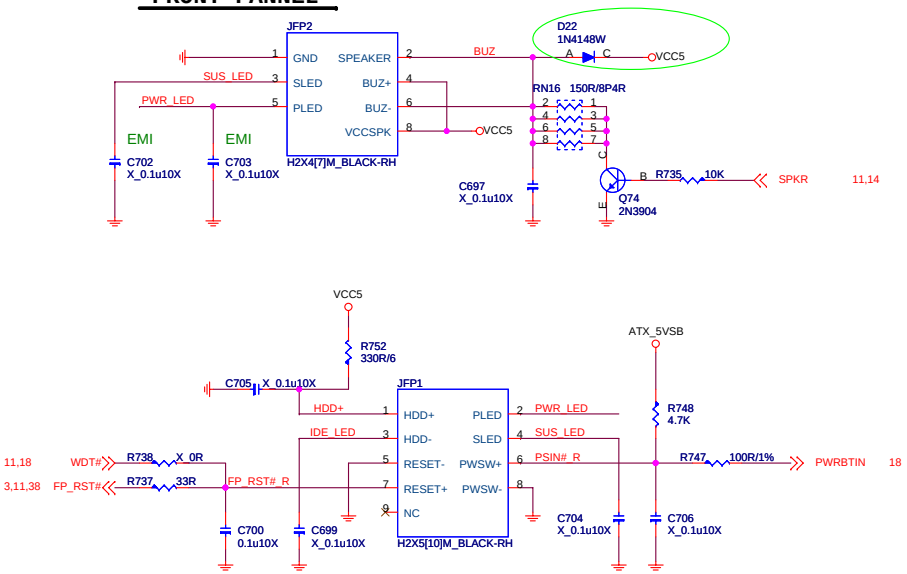
0.09(LAN_1P05)+0.332(+3.3_LAN)+
0.025(SPI ROM MAX)+0.02(SB VCCSPI)=0.467A

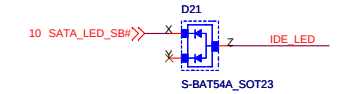
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: ME Power - UP1712	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 35 of 43	

ATX POWER CONNECTOR

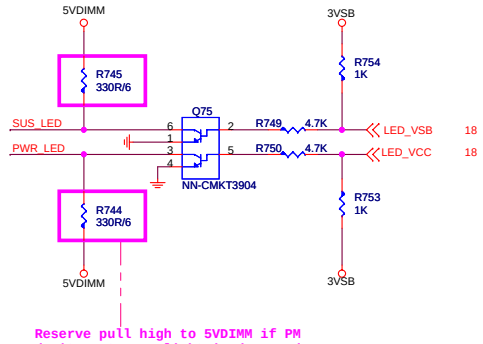


FRONT PANNEL

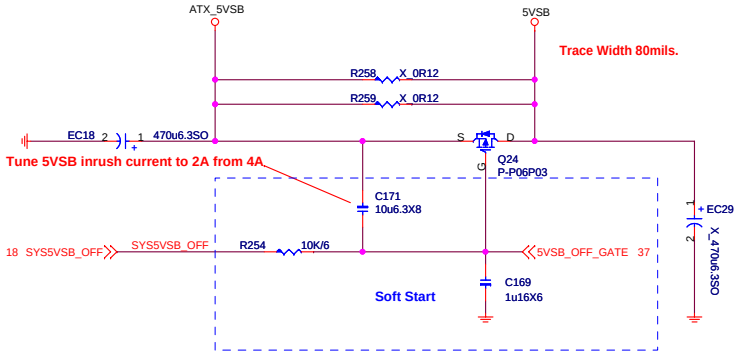




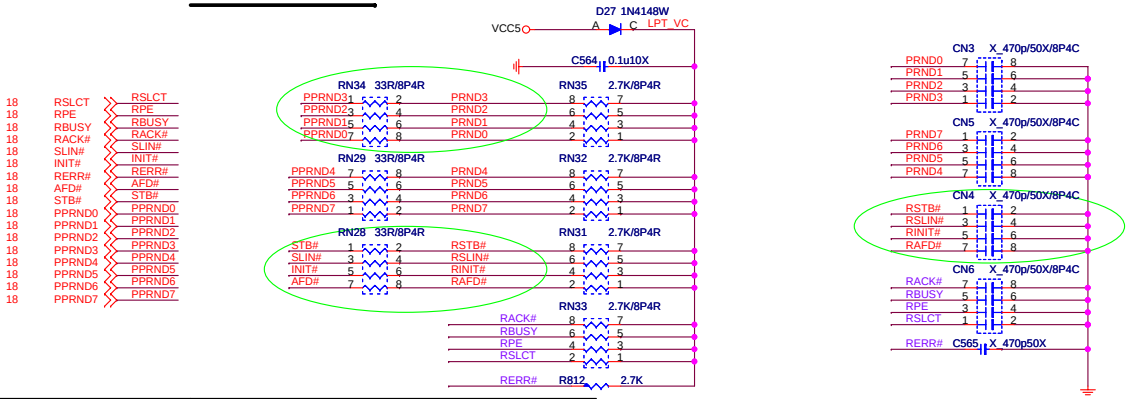
LED (for Fintek 71869)

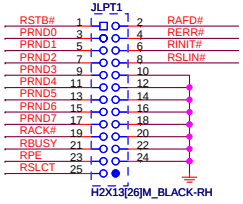


5VSB Power Switch

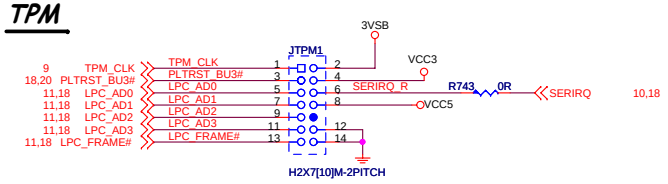


PARALLAL PORT

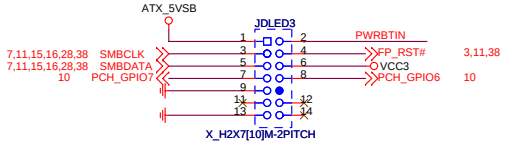




TPM



JDLED3



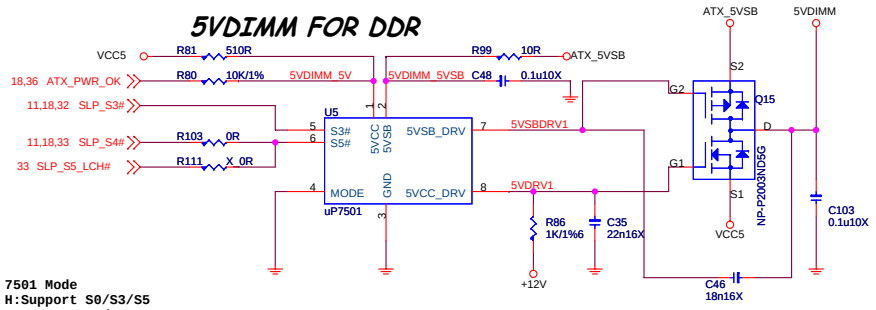
REMOVE Turbo Button

N31-2131151-H06 : 2.0mm

N31-2131131-H06 : 2.54mm

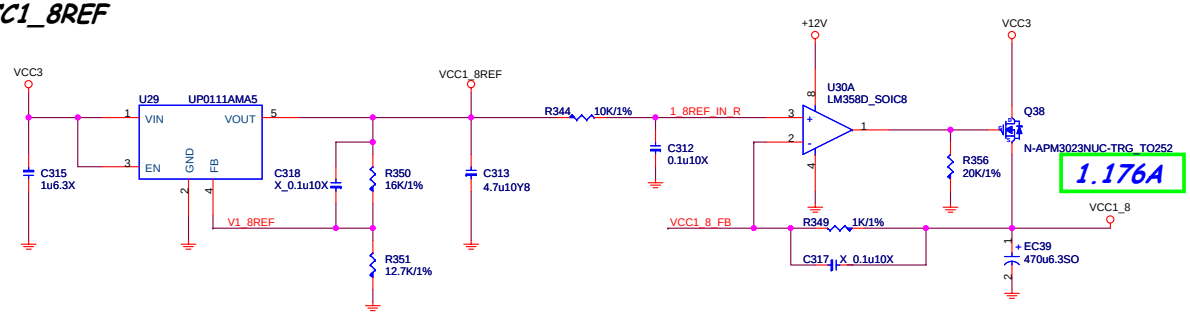
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: ATX F_Panel/EMI/TPM	Rev: 2.1
Date: Monday, May 28, 2012	Sheet 36 of 43	

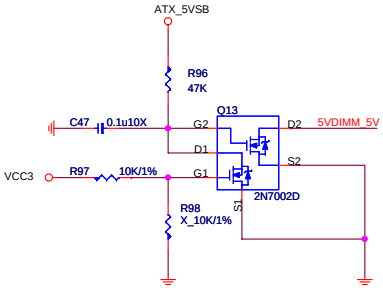
5VDIMM FOR DDR



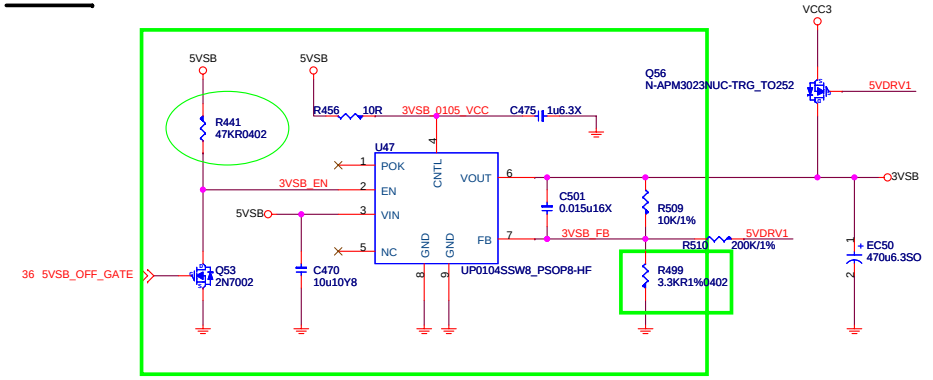
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

VCC1_8REF

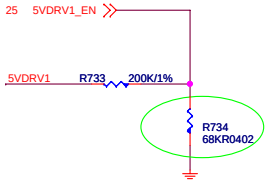




3VSB

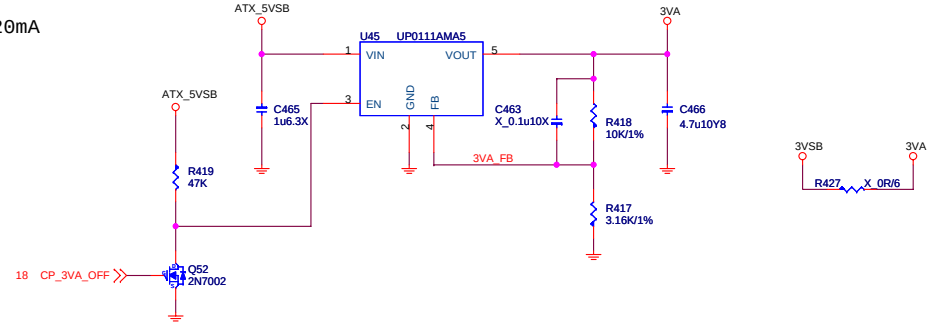


USB MODE



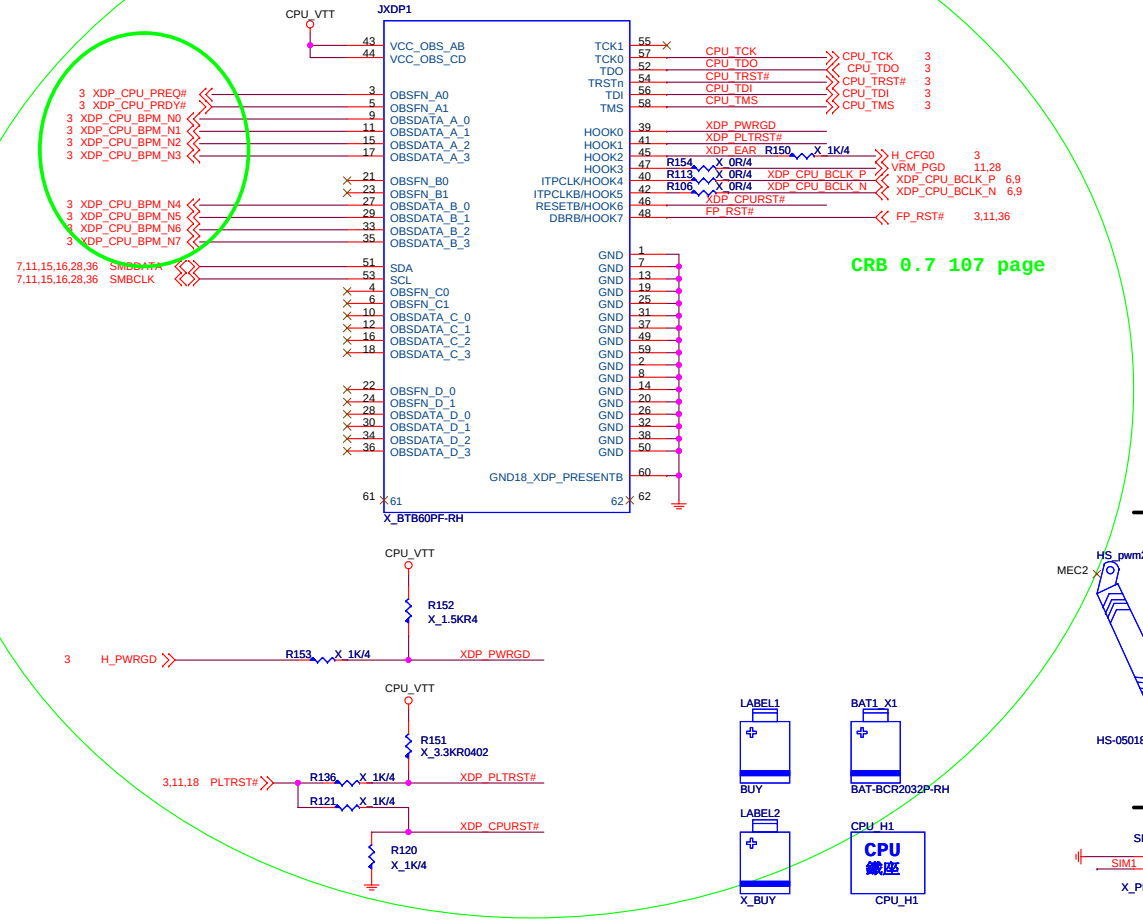
3VA

20mA

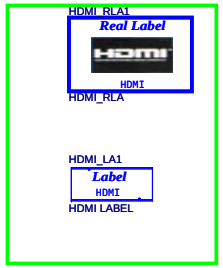


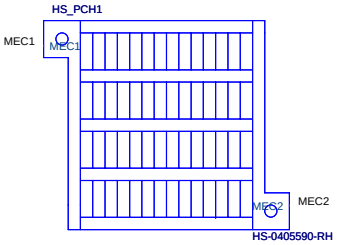
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: ACPI controller UPI	Rev: 2.1
Date: Tuesday, May 22, 2012	Sheet 37 of 43	

Reserve debug port 5020

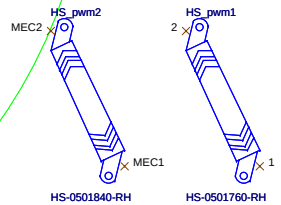


CRB 0.7 107 page

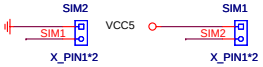




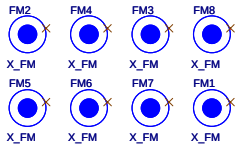
HEATSINK



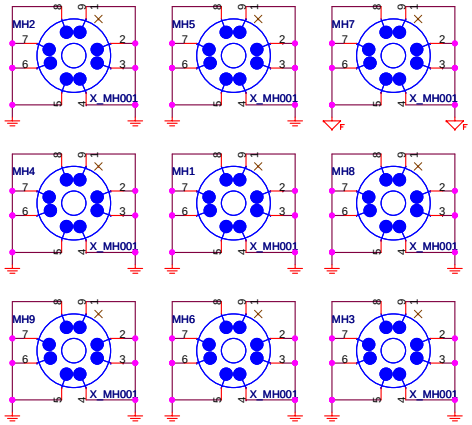
Simulation

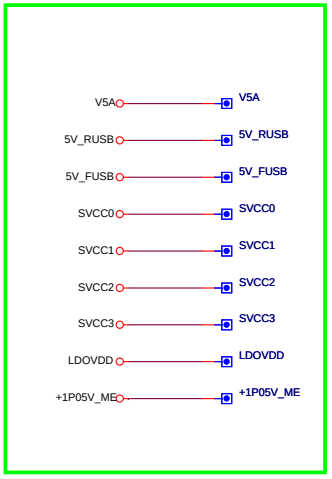


Optical Fiducial Marks-120

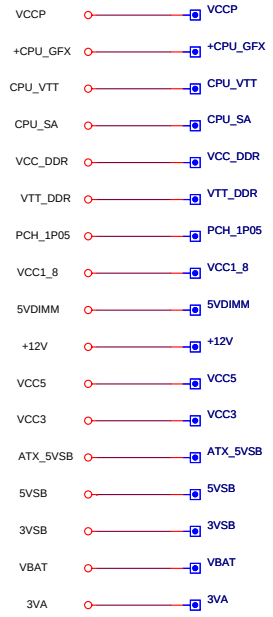


Mounting Holes



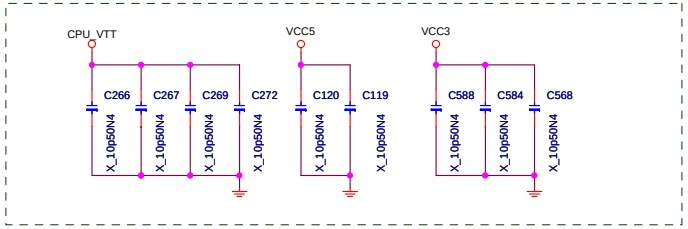


Voltage test point

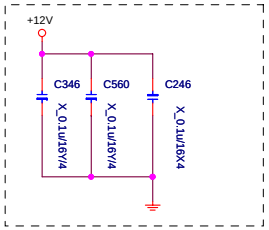


MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: XDP / Manual Parts	Rev: 2.1
Date: Friday, May 25, 2012	Sheet 38 of 43	

EMI:cap. for signal return path



EMI



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7758	
Size: Custom	Document Description: EMI CAP	Rev: 2.1
Date: Friday, May 18, 2012	Sheet 39 of 43	