MS-7758

ATX
Ver: 4.0(304.8x202)

Intel -MahoBay plamform B75

CPU:

IVY bridge LGA1155

System Chipset:

Panther Point B75

Onboard Chip:

HD Audio Codec:ALC892 colay 887
LAN-RTL8111E colay8105E
SIO:Fintek F71868AD
B75 Flash ROM: SPI 128 MB

Main Memory:

*DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12 -UT501 3+1 Phase

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2*
*PCI Slot * 3*

Other:

SATA3.0 x1+SATA2.0 x5 (B75)
*USB2.0 *10*
*REAL USB3.0 *2*
*FRONT USB3.0 *2*

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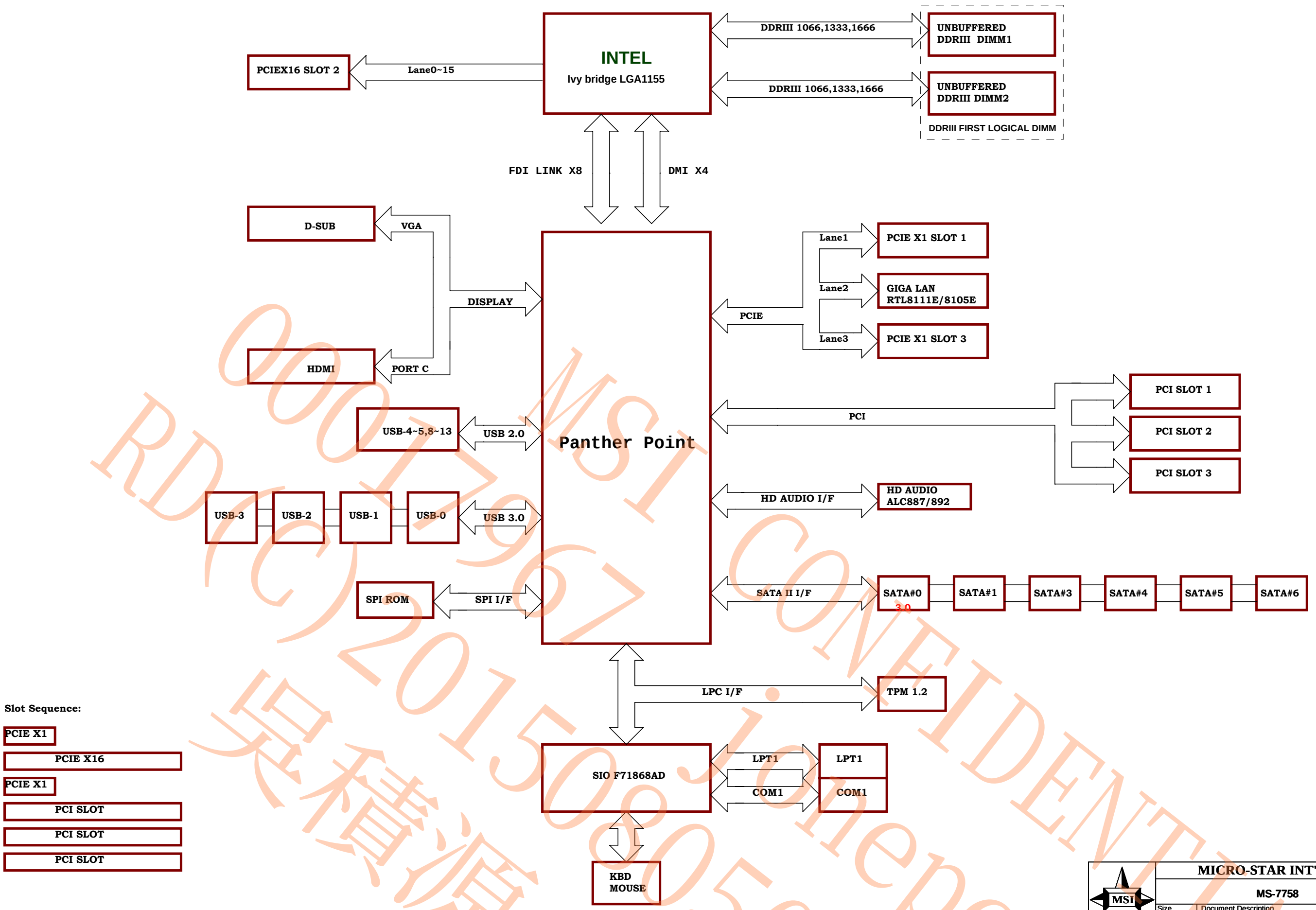
MS-7758		
Size: Custom	Document Description: Cover Sheet	Rev: 4.0
Date: Monday, June 25, 2012	Sheet 1 of 44	

MS-7758-4.0 Block Diagram

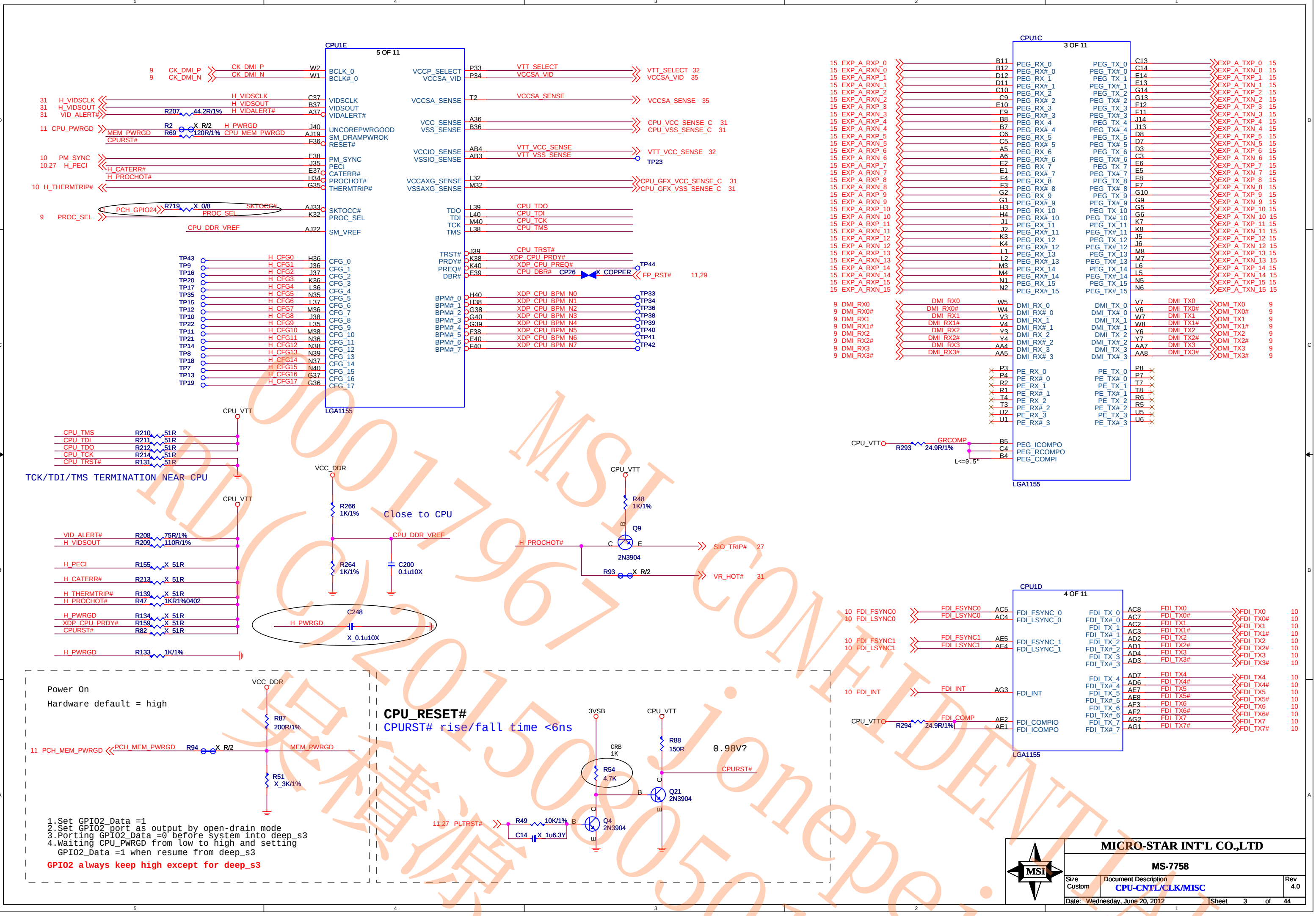


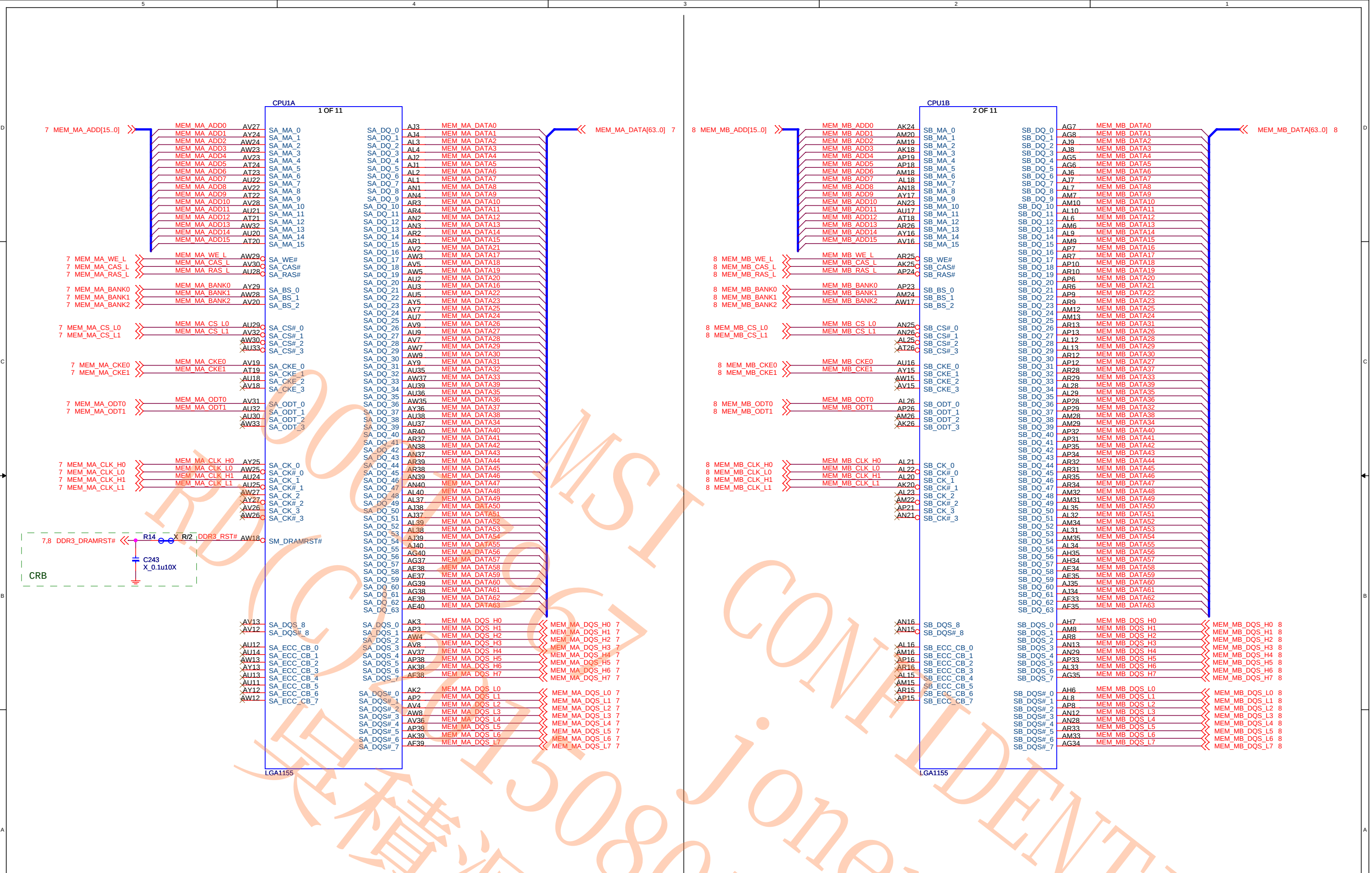
MICRO-STAR INT'L CO.,LTD

MS-7758

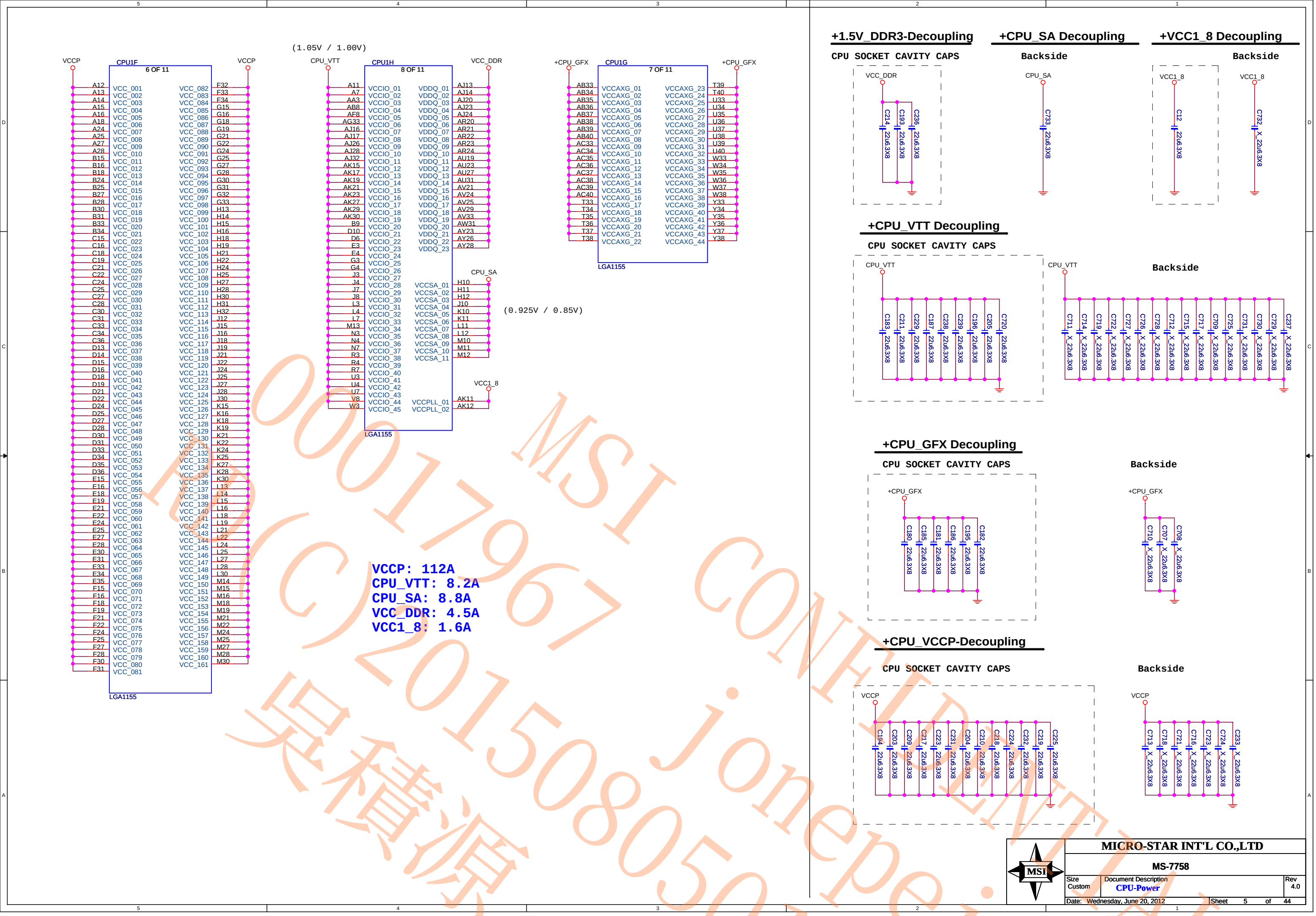
Size	Document Description	Rev
Custom	Block Diagram	4.0

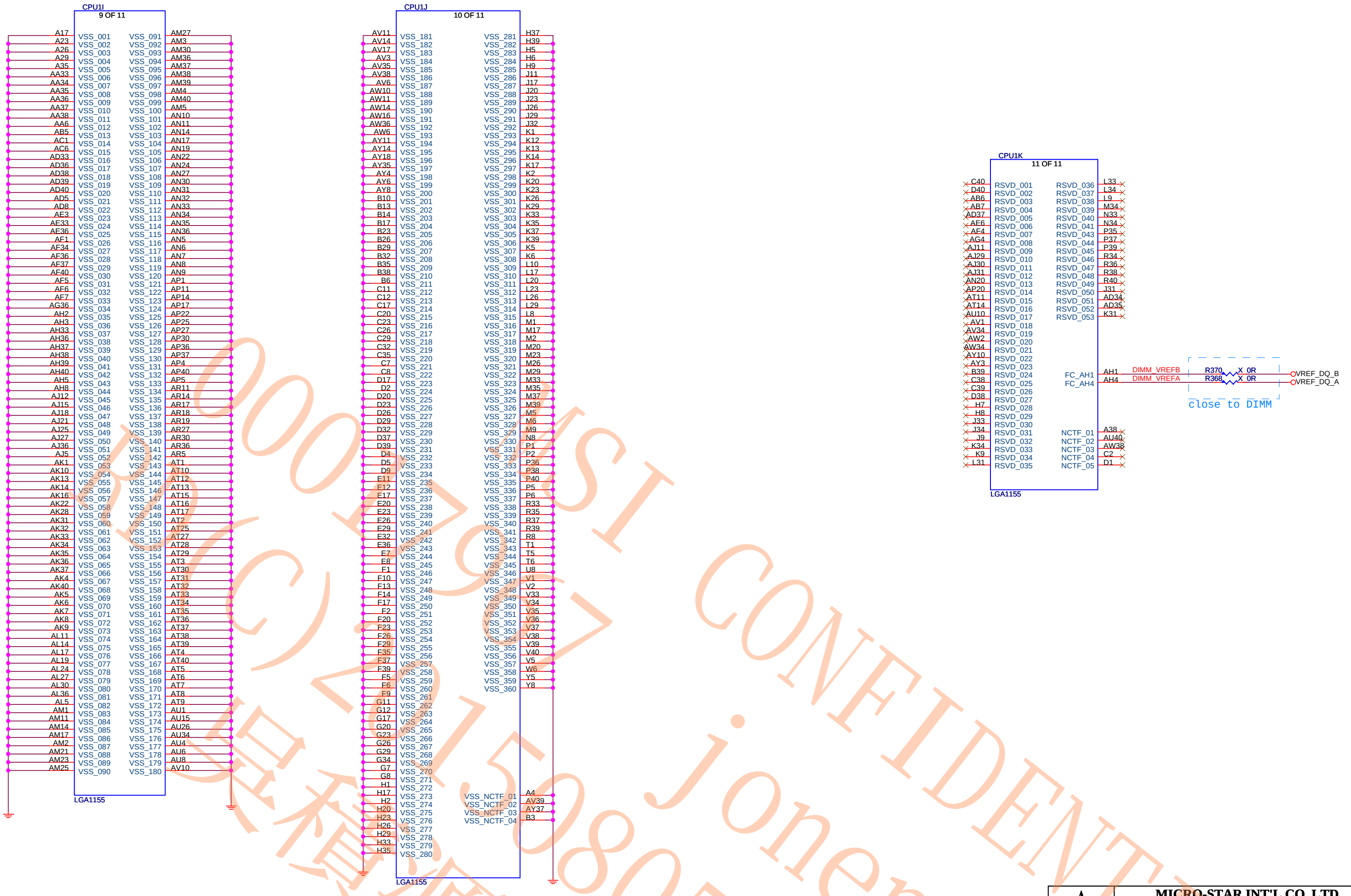
Date: Saturday, June 09, 2012 Sheet 2 of 44





MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: **CPU-Memory**	Rev: 4.0
Date: Wednesday, June 20, 2012	Sheet 4 of 44	


(1.05V / 1.00V)
(0.925V / 0.85V)
CPU1F 6 OF 11 LGA1155
CPU1H 8 OF 11 LGA1155
CPU1G 7 OF 11 LGA1155
VCCP
CPU_VTT
VCC_DDR
CPU_SA
VCC1_8
+CPU_GFX
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A
+1.5V_DDR3-Decoupling
CPU SOCKET CAVITY CAPS
+CPU_SA Decoupling
Backside
+VCC1_8 Decoupling
Backside
+CPU_VTT Decoupling
CPU SOCKET CAVITY CAPS
Backside
+CPU_GFX Decoupling
CPU SOCKET CAVITY CAPS
Backside
+CPU_VCCP-Decoupling
CPU SOCKET CAVITY CAPS
Backside
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description CPU-Power
Rev 4.0
Date: Wednesday, June 20, 2012
Sheet 5 of 44

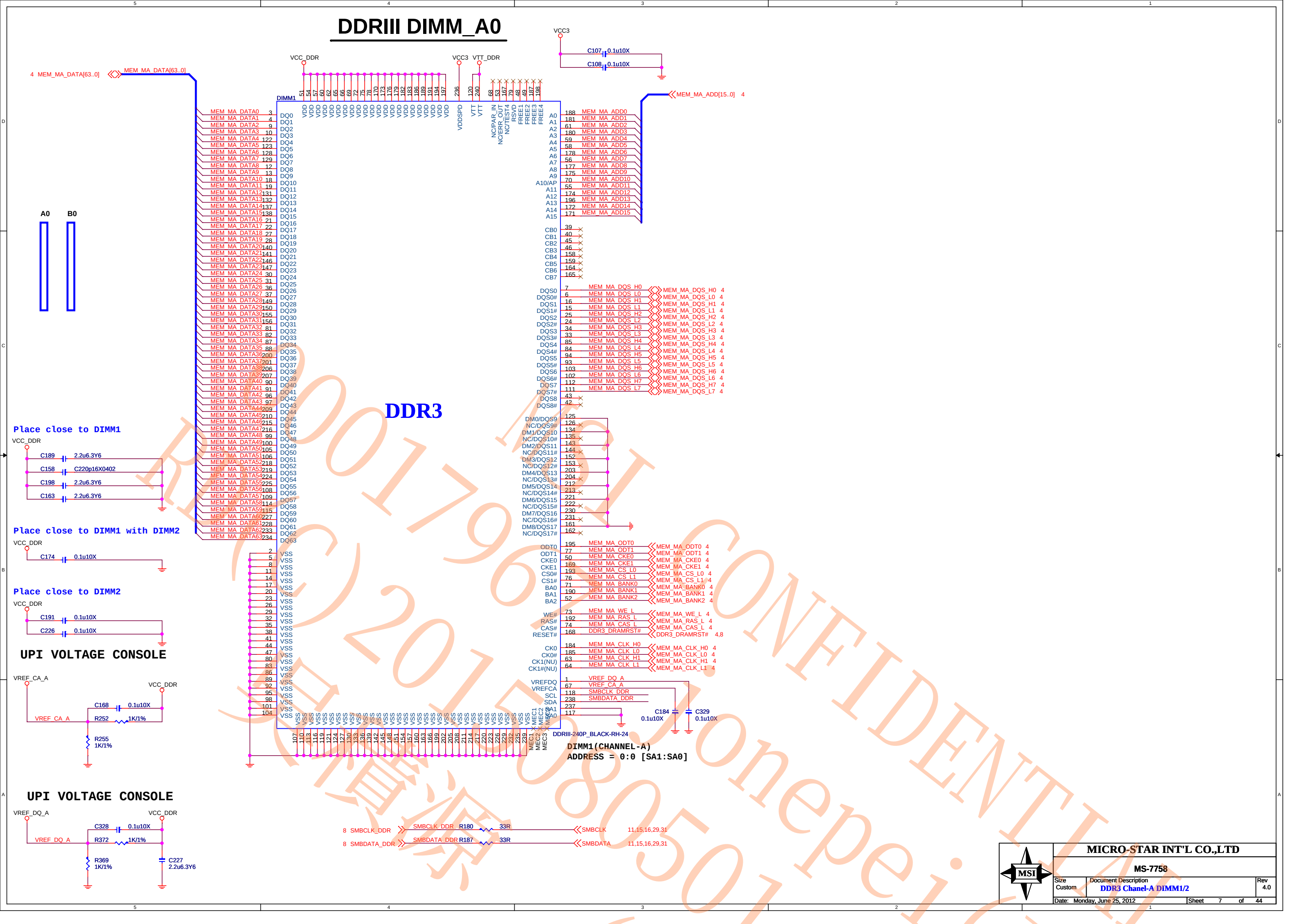


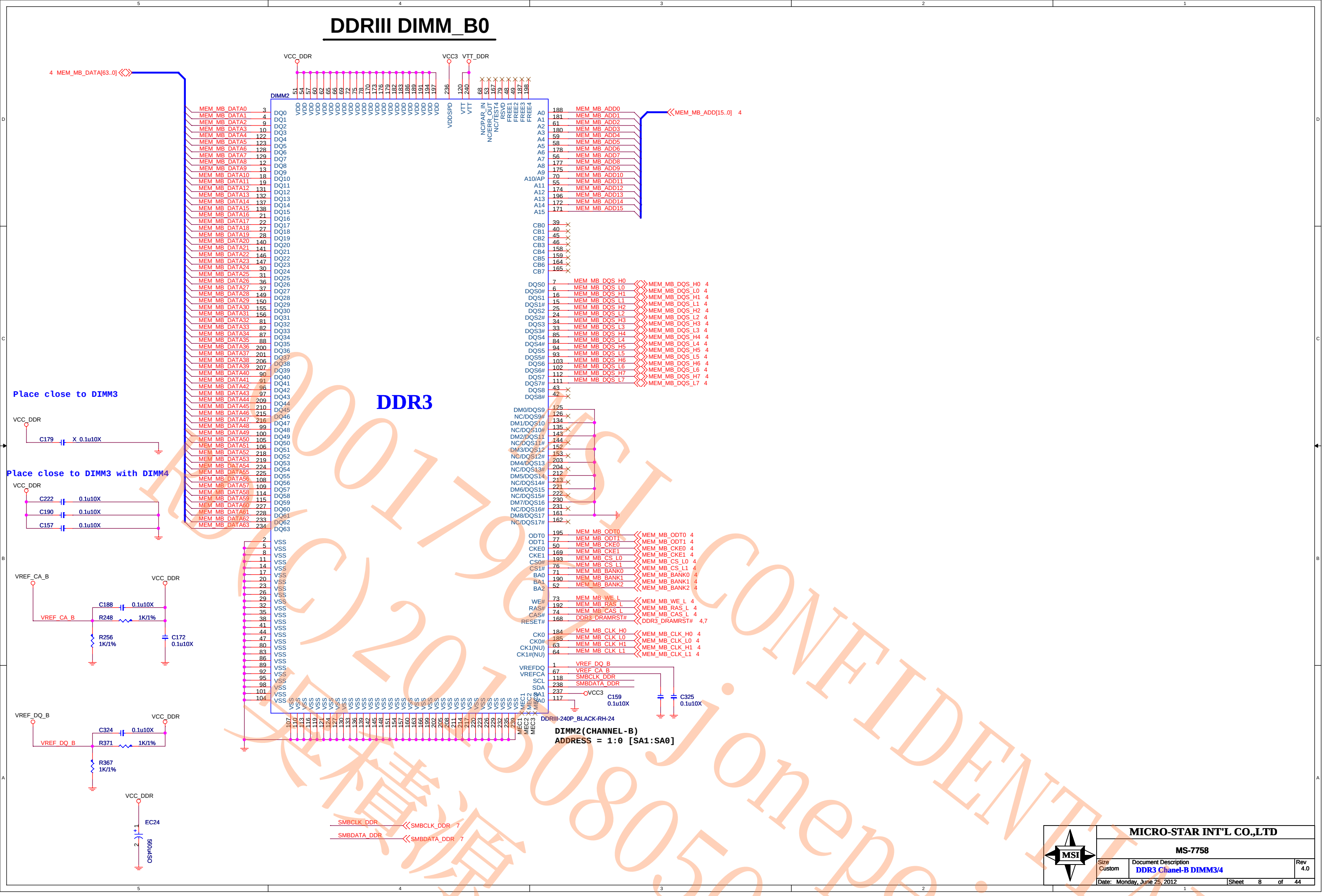
MICRO-STAR INT'L CO.,LTD

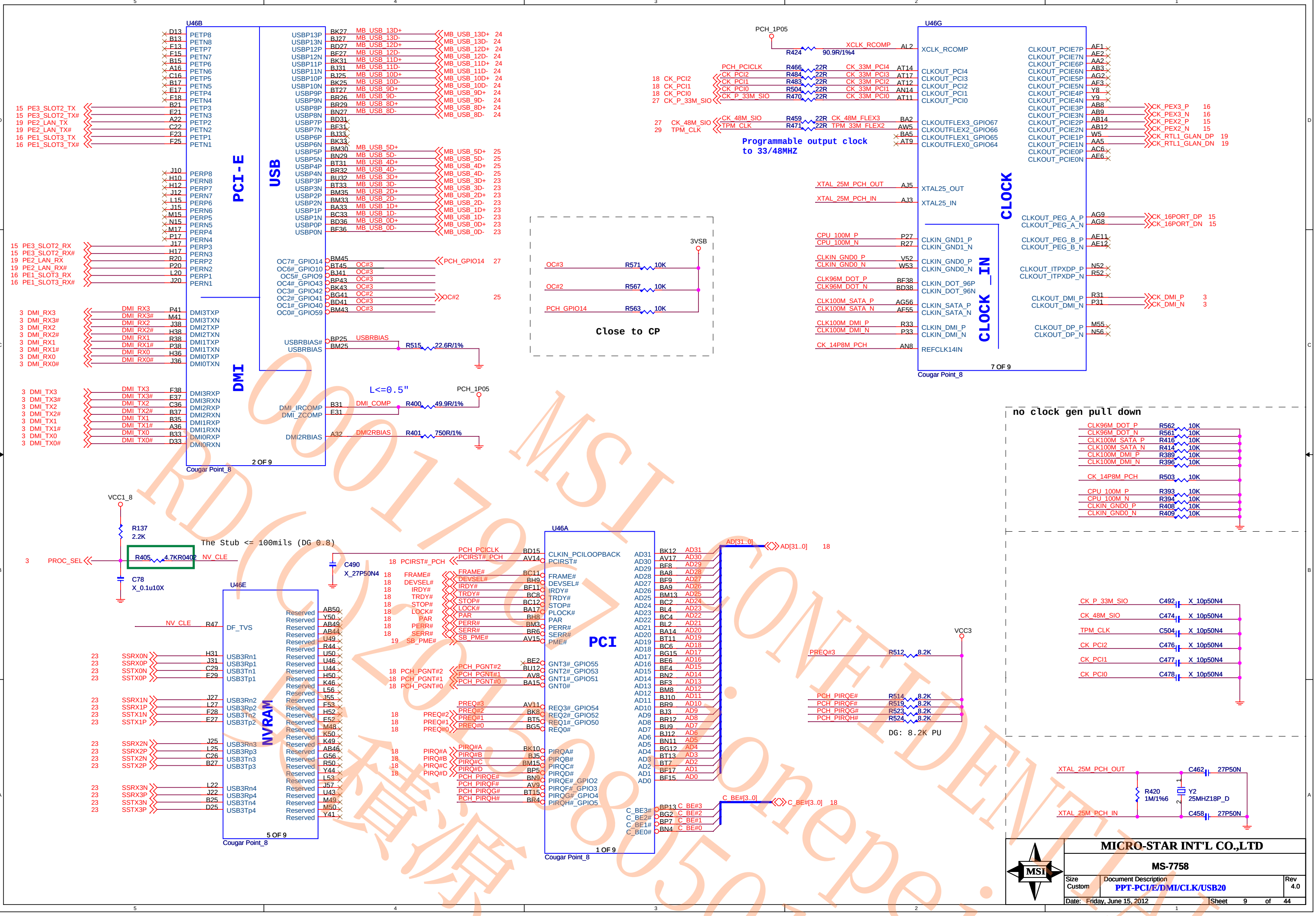
MS-7758

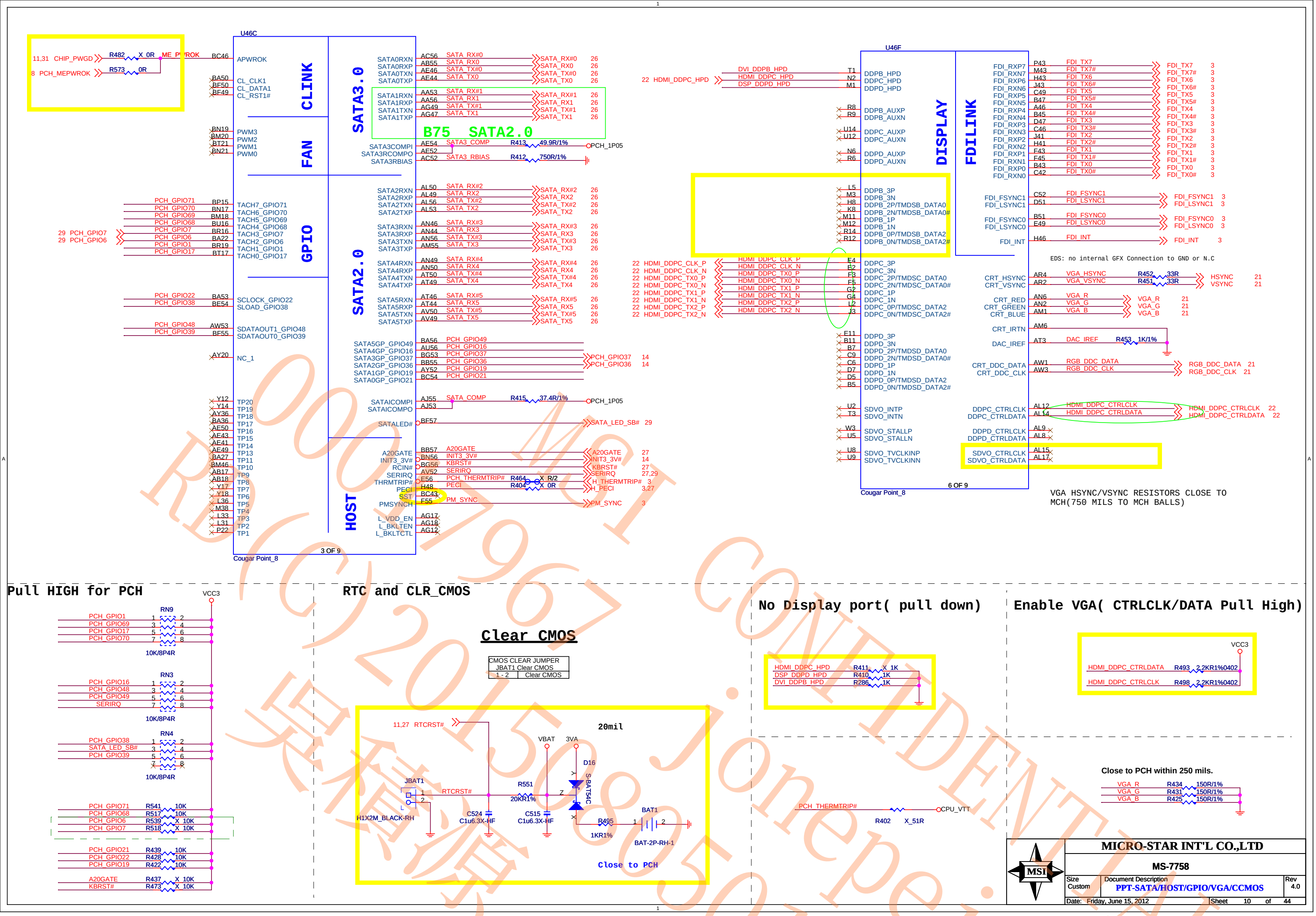
Size	Document Description	Rev
Custom	CPU-GND	4.0

Date: Wednesday, June 20, 2012 Sheet 6 of 44

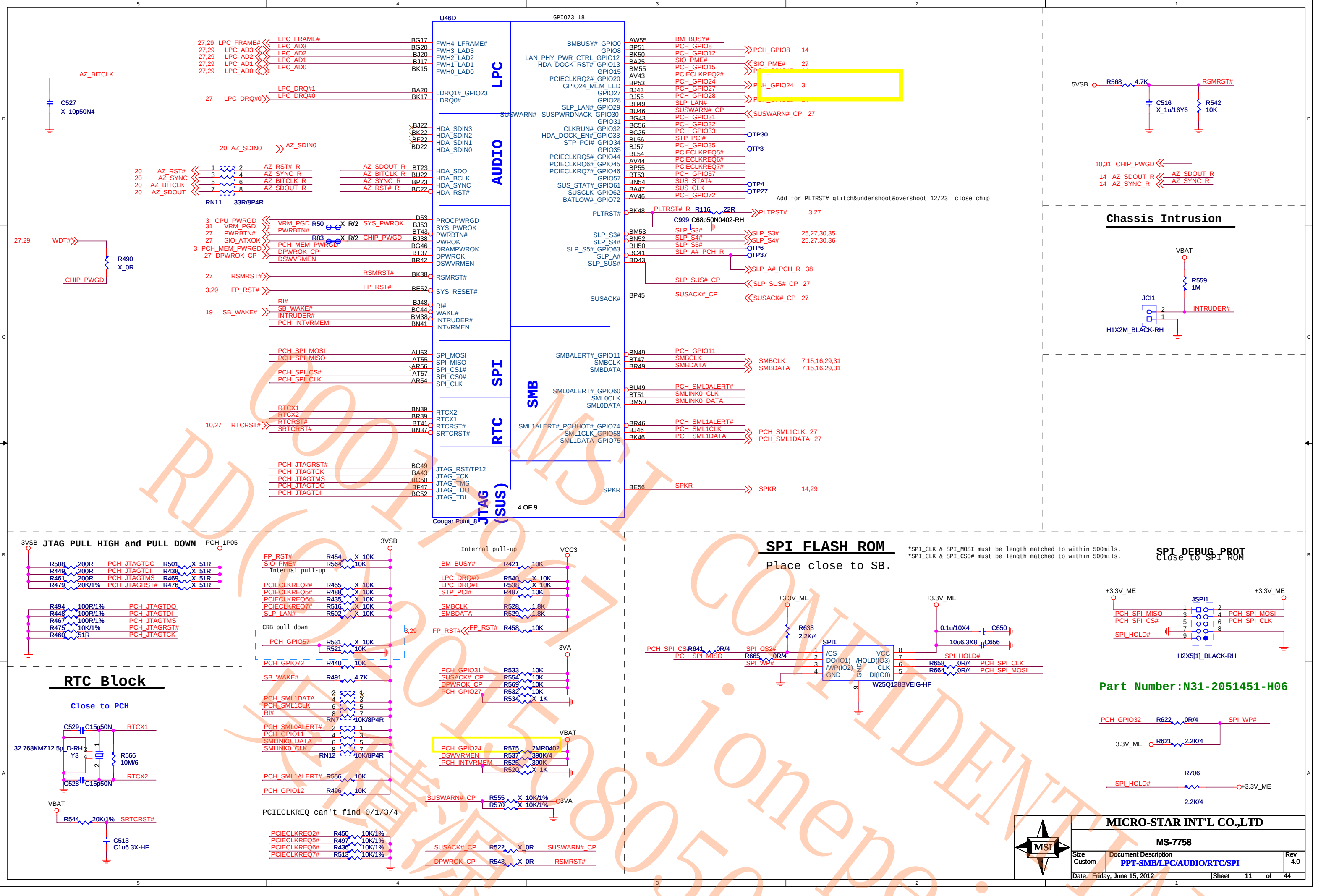


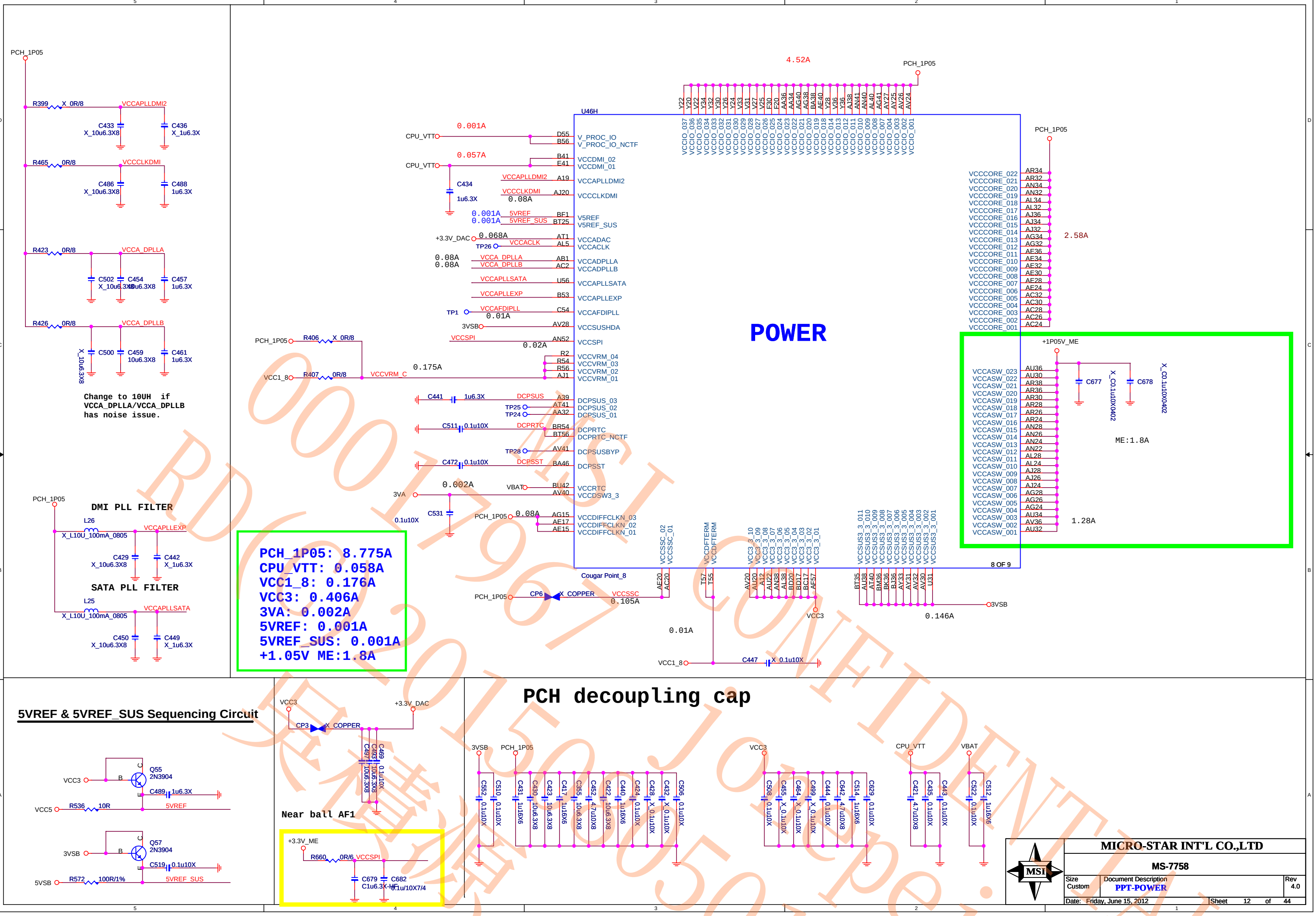

DDRIII DIMM_B0
DDR3
DIMM2
DDRIII-240P_BLACK-RH-24
DIMM2(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
Place close to DIMM3
Place close to DIMM3 with DIMM4
VCC_DDR
VCC3
VTT_DDR
MEM_MB_DATA[63..0]
MEM_MB_ADD[15..0]
VREF_CA_B
VREF_DQ_B
SMBCLK_DDR
SMBDATA_DDR
DDR3_DRAMRST#
C179 X_0.1u10X
C222 0.1u10X
C190 0.1u10X
C157 0.1u10X
C188 0.1u10X
R248 1K/1%
R256 1K/1%
C172 0.1u10X
C324 0.1u10X
R371 1K/1%
R367 1K/1%
EC24
C159 0.1u10X
C325 0.1u10X
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description
DDR3 Chanel-B DIMM3/4
Rev 4.0
Date: Monday, June 25, 2012
Sheet 8 of 44

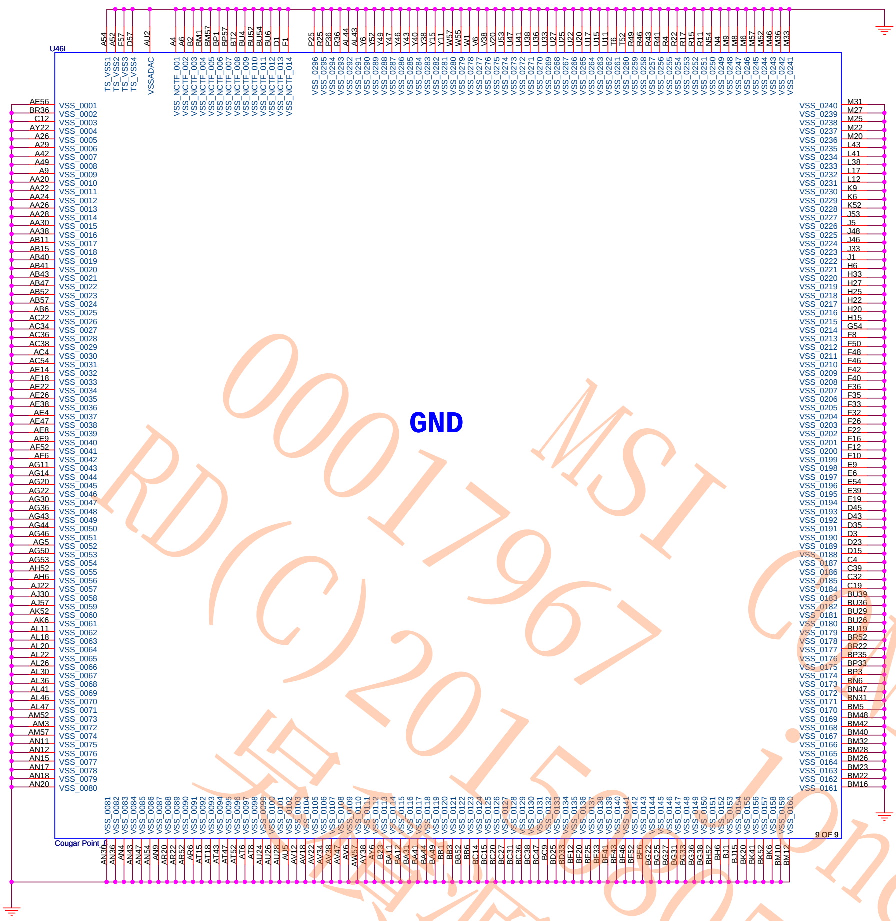



U46C
CLINK
FAN
GPIO
SATA3.0
SATA2.0
HOST
B75 SATA2.0
3 OF 9
Cougar Point_8
U46F
DISPLAY
FDILINK
6 OF 9
Cougar Point_8
EDS: no internal GFX Connection to GND or N.C
VGA HSYNC/VSYNC RESISTORS CLOSE TO MCH(750 MILS TO MCH BALLS)
Pull HIGH for PCH
RTC and CLR_CMOS
Clear CMOS
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Clear CMOS
20mil
Close to PCH
No Display port(pull down)
Enable VGA(CTRLCLK/DATA Pull High)
Close to PCH within 250 mils.
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description
PPT-SATA/HOST/GPIO/VGA/CCMOS
Rev 4.0
Date: Friday, June 15, 2012
Sheet 10 of 44

PCH_GPIO1




POWER
4.52A
2.58A
PCH_1P05
CPU_VTT
U46H
Cougar Point_8
8 OF 9
DMI PLL FILTER
SATA PLL FILTER
Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.
PCH_1P05: 8.775A
CPU_VTT: 0.058A
VCC1_8: 0.176A
VCC3: 0.406A
3VA: 0.002A
5VREF: 0.001A
5VREF_SUS: 0.001A
+1.05V ME:1.8A
ME:1.8A
1.28A
+1P05V_ME
0.001A
0.057A
0.08A
0.068A
0.01A
0.02A
0.175A
0.002A
0.105A
0.01A
0.146A
5VREF & 5VREF_SUS Sequencing Circuit
Near ball AF1
PCH decoupling cap
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description PPT-POWER
Rev 4.0
Date: Friday, June 15, 2012
Sheet 12 of 44



MICRO-STAR INT'L CO.,LTD

MS-7758

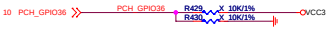
Size	Document Description	Rev
Custom	PPT-GND/NVRAM/USB30	4.0

Date: Friday, June 15, 2012 Sheet 13 of 44

PCH Straps

SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:

Do not pull low.



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

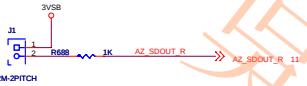
HDA_SYNC
OD PLL_VR_SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

Internal weak pull down. Do not pull up.

Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

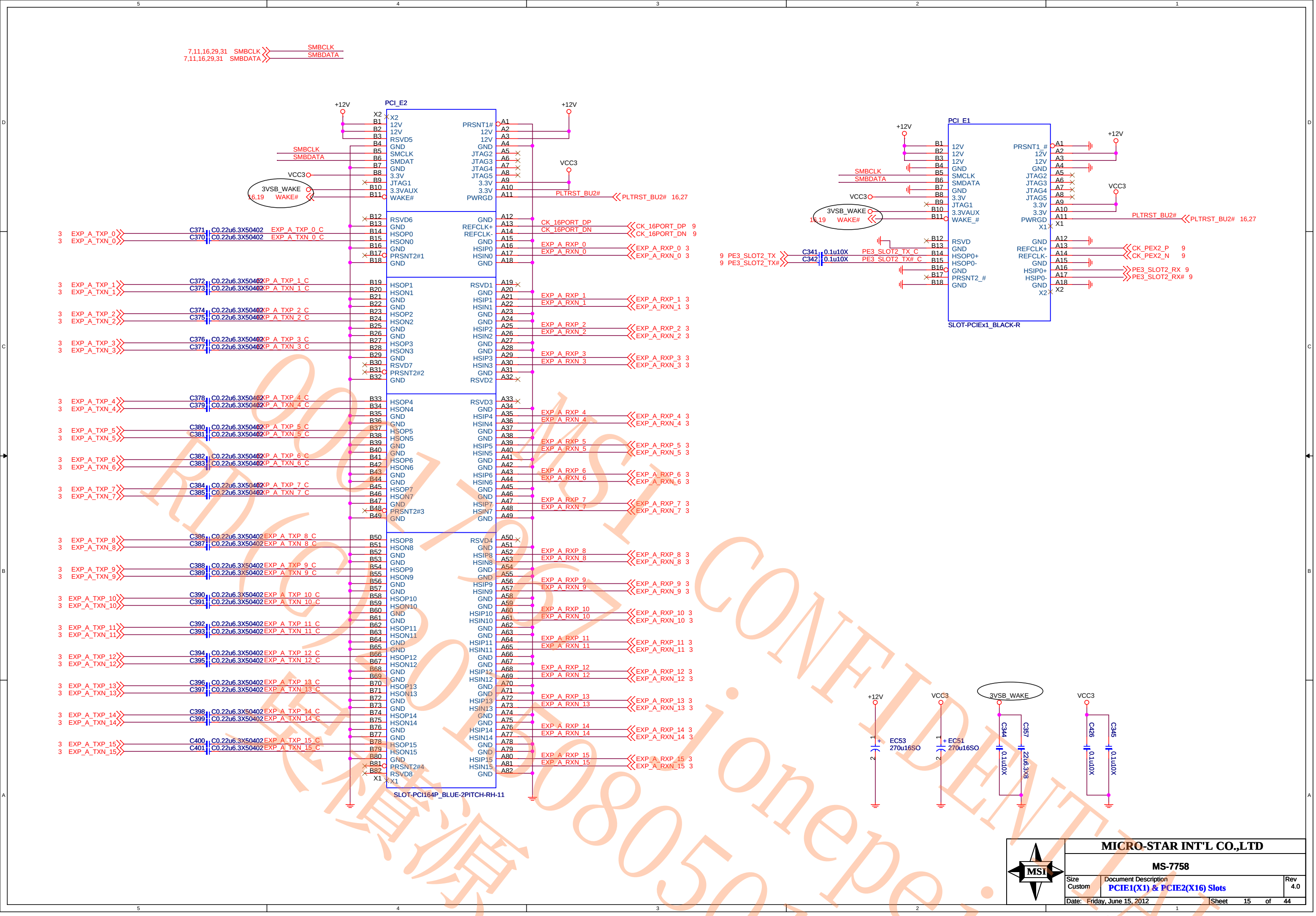
BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by softstrap through ME.

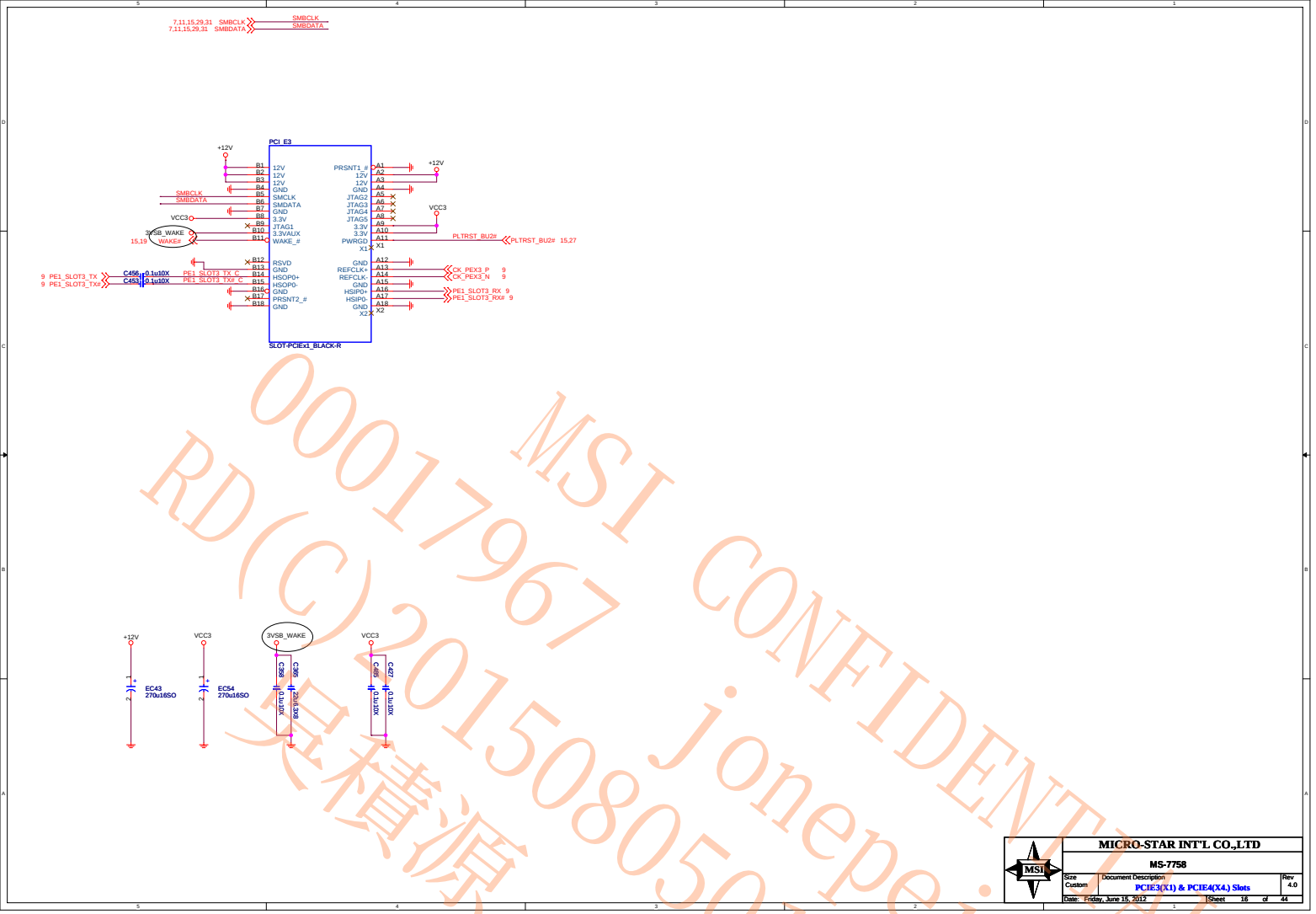


Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

Internal weak pull up. Do not pull low.
On die PLL voltage regulator

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7758	
Size: Custom	Document Description: PPT Strap	Rev: 4.0
Date: Friday, June 15, 2012	Sheet 14 of 44	





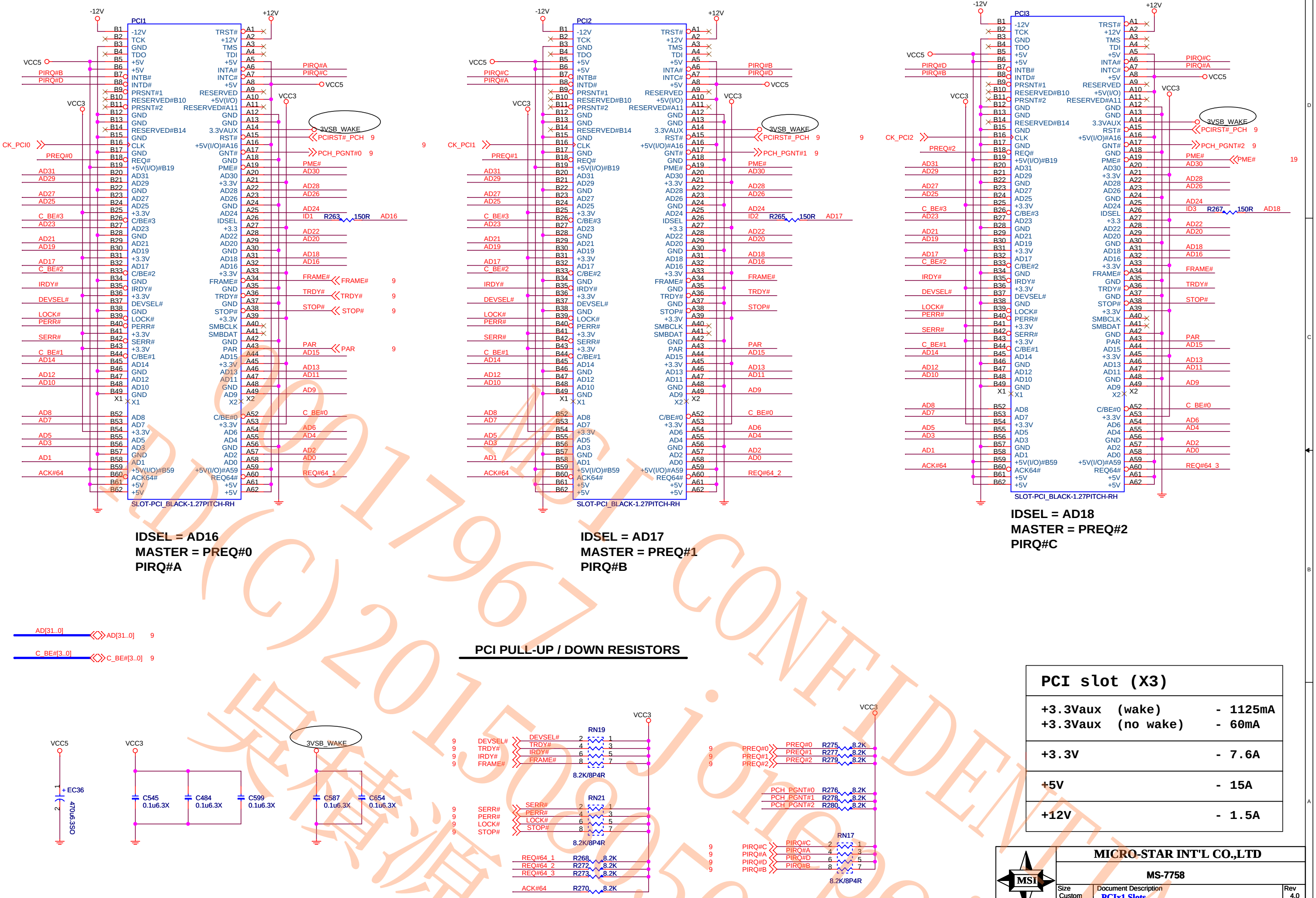
MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PCIE3(X1) & PCIE4(X4.) Slots	Rev: 4.0
Date: Friday, June 15, 2012	Sheet 16 of 44	

MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	ASM1083 PCI Bri.	4.0

Date: Friday, June 08, 2012 Sheet 17 of 44



PCI slot (X3)		
+3.3Vaux (wake)	-	1125mA
+3.3Vaux (no wake)	-	60mA
+3.3V	-	7.6A
+5V	-	15A
+12V	-	1.5A

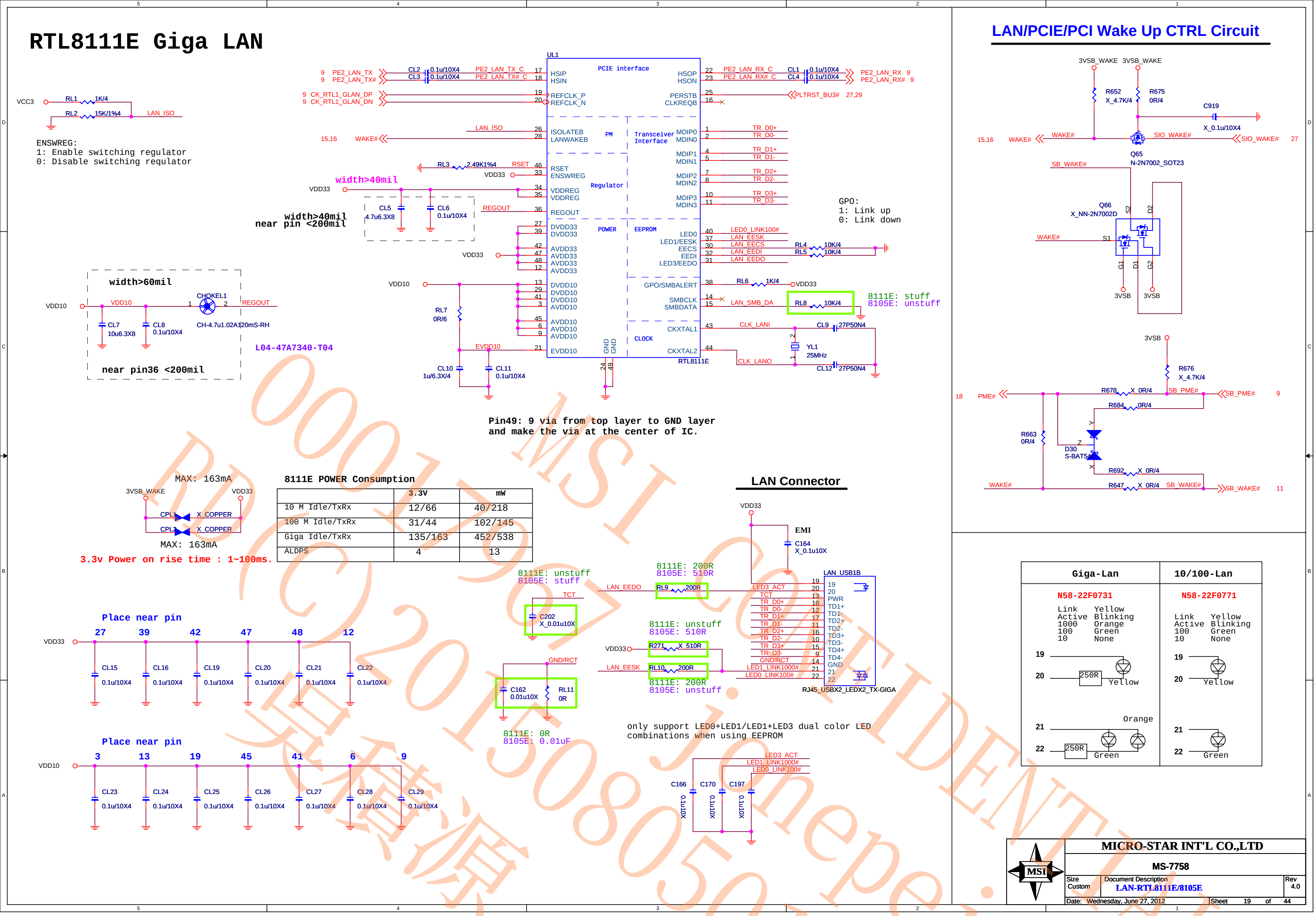
MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	PCIx1 Slots	4.0

Date: Tuesday, June 19, 2012 Sheet 18 of 44

RTL8111E Giga LAN



ENSWREG:
1: Enable switching regulator
0: Disable switching regulator
width>40mil
width>40mil
near pin <200mil
width>60mil
near pin36 <200mil
L04-47A7340-T04
GPO:
1: Link up
0: Link down
8111E: stuff
8105E: unstuff
Pin49: 9 via from top layer to GND layer and make the via at the center of IC.
MAX: 163mA
MAX: 163mA
3.3v Power on rise time : 1~100ms.
LAN Connector
EMI
8111E: unstuff
8105E: stuff
8111E: 200R
8105E: 510R
8111E: unstuff
8105E: 510R
8111E: 200R
8105E: unstuff
8111E: 0R
8105E: 0.01uF
only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM
Place near pin
27 39 42 47 48 12
Place near pin
3 13 19 45 41 6 9
RTL8111E
PCIE interface
Transceiver Interface
Regulator
POWER
EEPROM
CLOCK
RJ45_USBX2_LEDX2_TX-GIGA
LAN/PCIE/PCI Wake Up CTRL Circuit
Giga-Lan
N58-22F0731
Link Yellow
Active Blinking
1000 Orange
100 Green
10 None
10/100-Lan
N58-22F0771
Link Yellow
Active Blinking
100 Green
10 None

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

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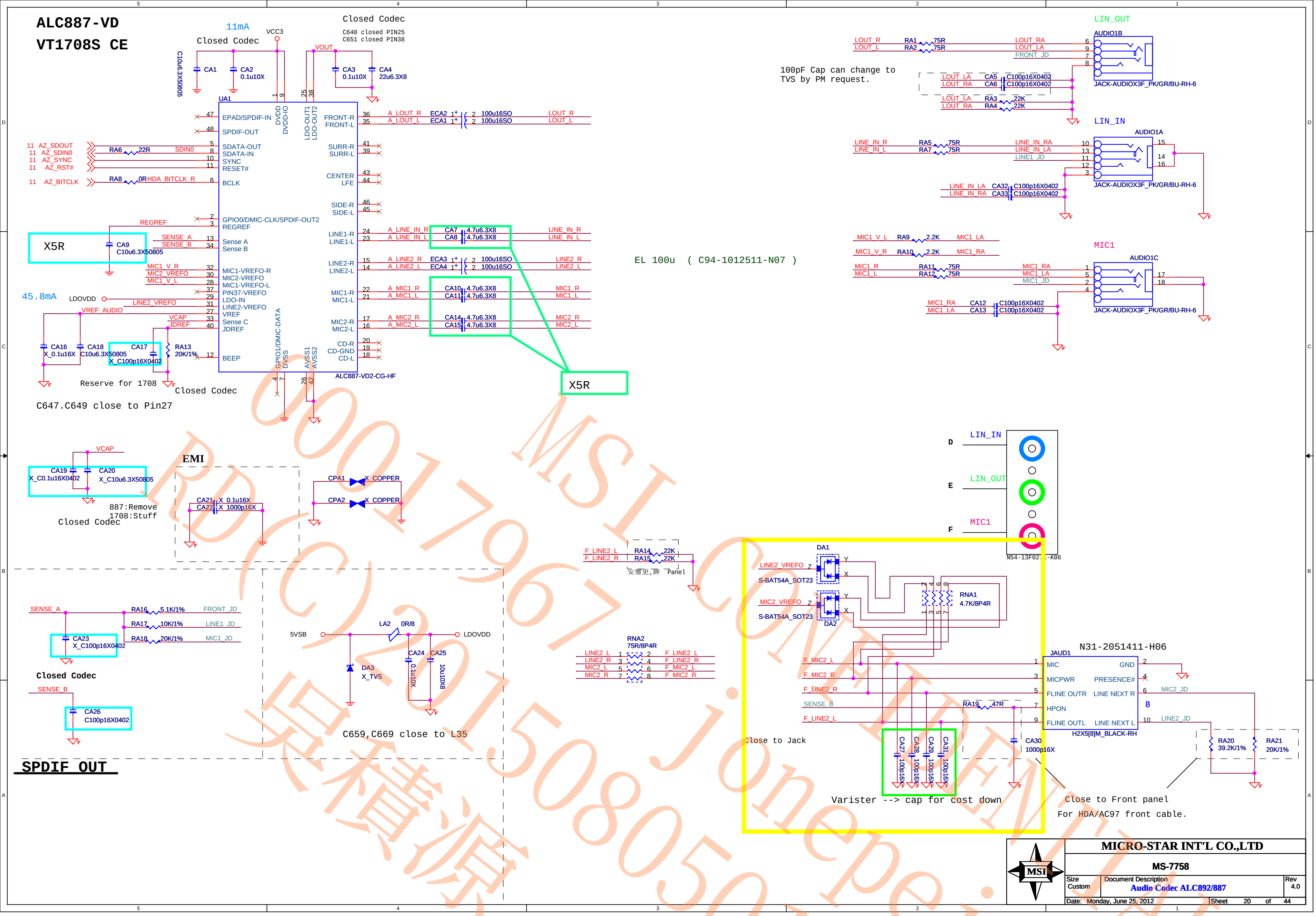
MS-7758

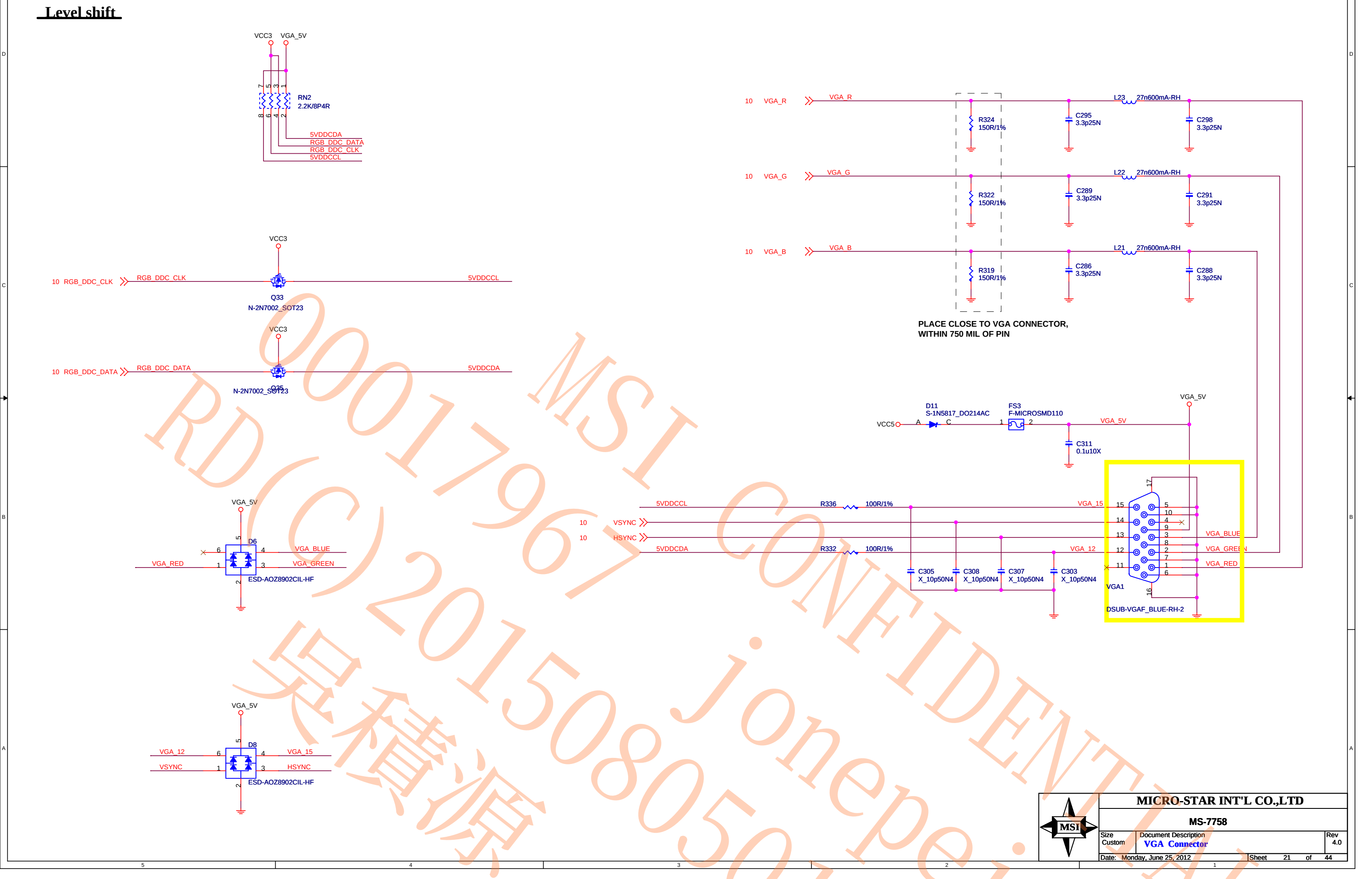
Size: Custom | Document Description: LAN-RTL8111E/8105E | Rev 4.0

Date: Wednesday, June 27, 2012 | Sheet 19 of 44



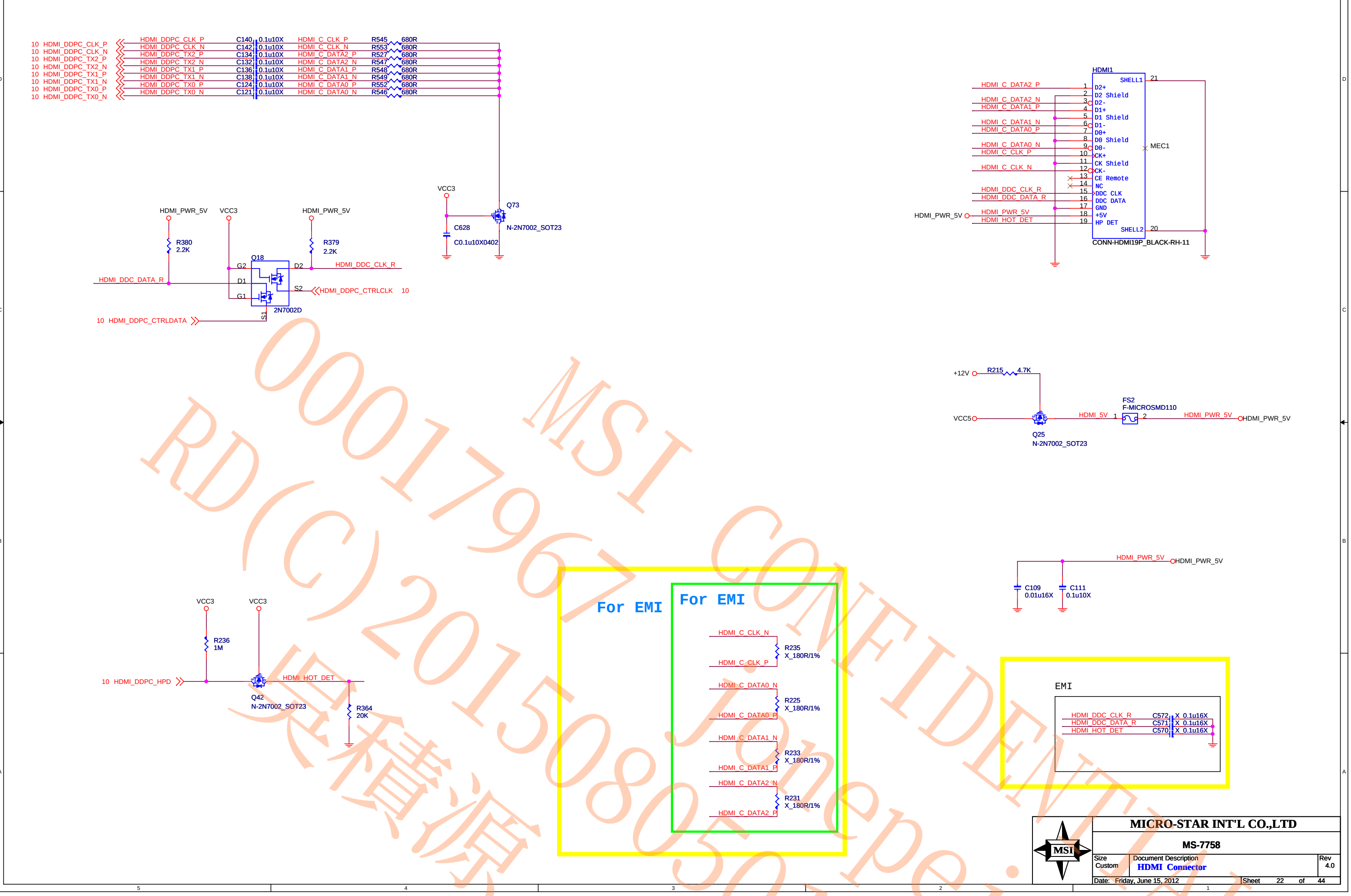
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



Level shift
VCC3
VGA_5V
RN2
2.2K/8P4R
5VDDCDA
RGB_DDC_DATA
RGB_DDC_CLK
5VDDCCL
10 RGB_DDC_CLK
Q33
N-2N7002_SOT23
10 RGB_DDC_DATA
Q35
N-2N7002_SOT23
D6
ESD-AOZ8902CIL-HF
VGA_RED
VGA_BLUE
VGA_GREEN
D8
VGA_12
VSYNC
VGA_15
HSYNC
10 VGA_R
10 VGA_G
10 VGA_B
R324 150R/1%
R322 150R/1%
R319 150R/1%
C295 3.3p25N
C289 3.3p25N
C286 3.3p25N
L23 27n600mA-RH
L22 27n600mA-RH
L21 27n600mA-RH
C298 3.3p25N
C291 3.3p25N
C288 3.3p25N
PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN
D11 S-1N5817_DO214AC
FS3 F-MICROSMD110
VCC5
C311 0.1u10X
R336 100R/1%
R332 100R/1%
10 VSYNC
10 HSYNC
C305 X_10p50N4
C308 X_10p50N4
C307 X_10p50N4
C303 X_10p50N4
VGA1
DSUB-VGAF_BLUE-RH-2
MICRO-STAR INT'L CO.,LTD
MS-7758
Size Custom
Document Description VGA Connector
Rev 4.0
Date: Monday, June 25, 2012
Sheet 21 of 44

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

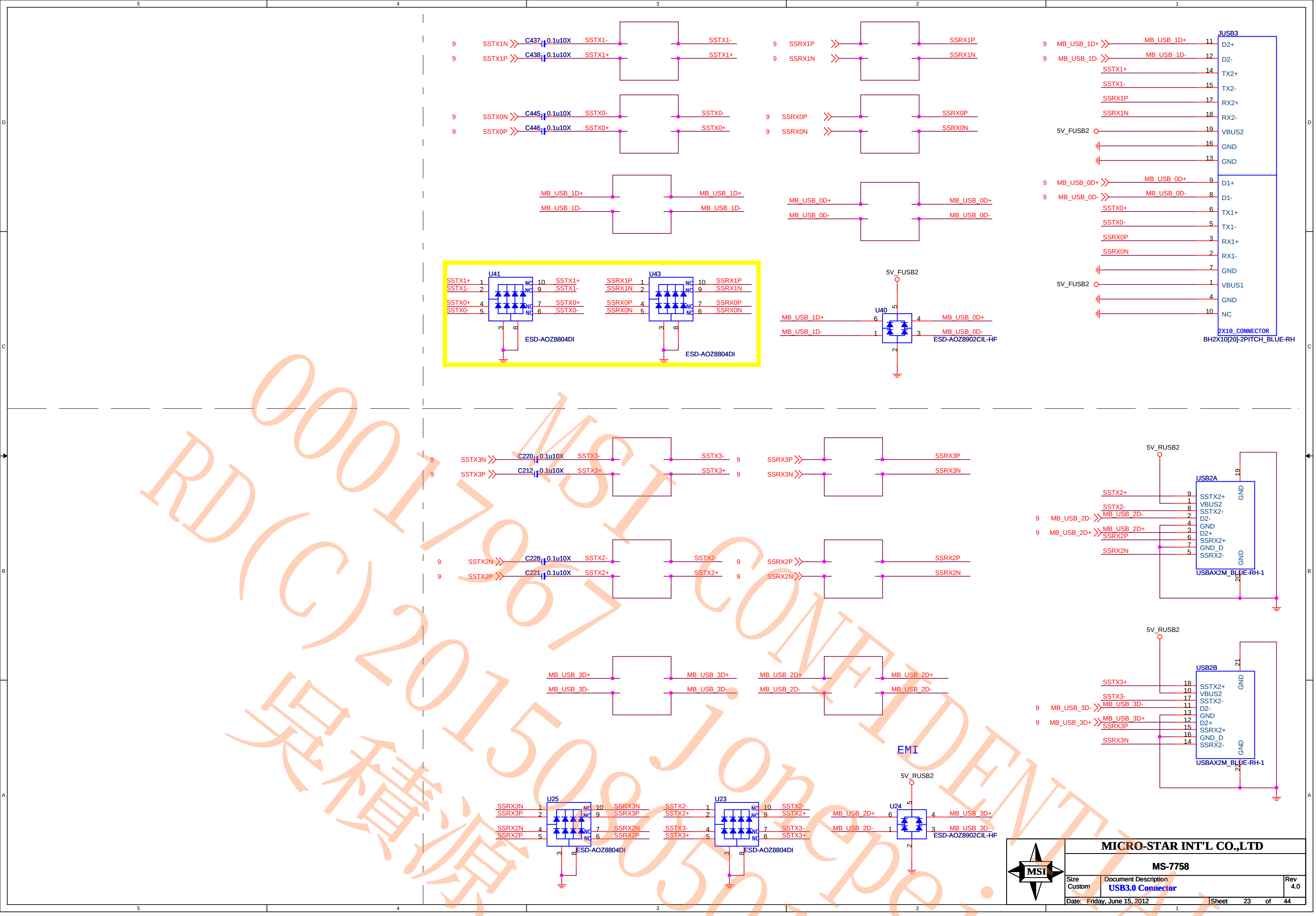


MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	HDMI Connector	4.0

Date: Friday, June 15, 2012 Sheet 22 of 44



USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

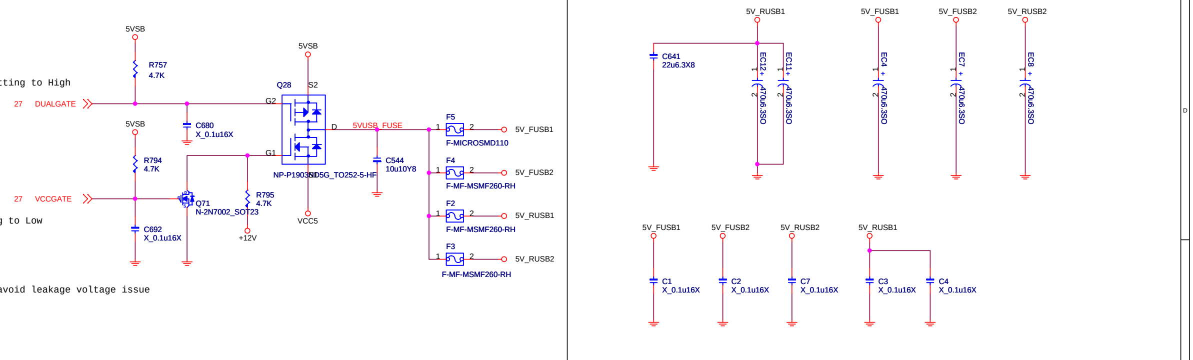
When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

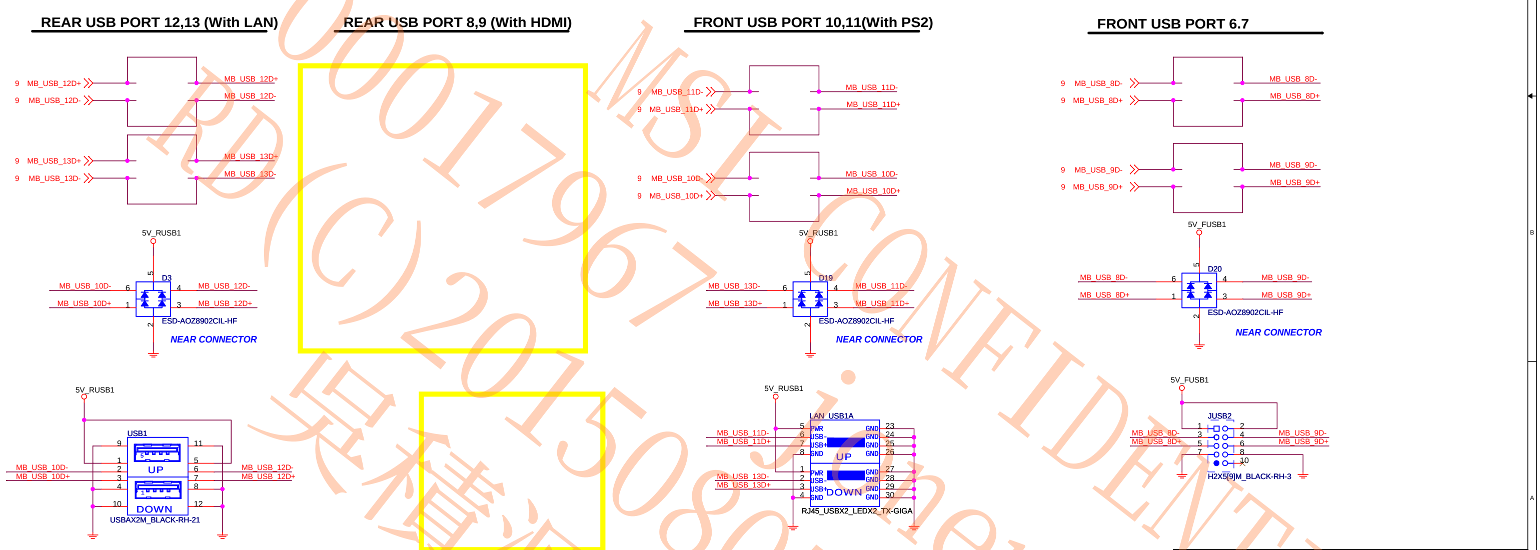
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

When PS2 in S5 support wake , S3P5_Gate# in S5 must setting to Low

*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

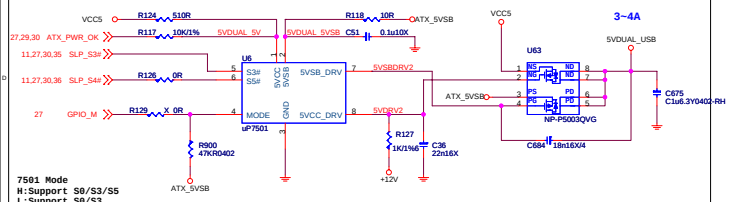
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue





MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: Rear I/O & USB2.0 Connector	Rev: 4.0
Date: Saturday, July 07, 2012	Sheet 24 of 44	

5VDUAL_USB



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

SIO GPIO03 Pin51 (I_VSB3V)

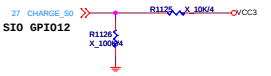
USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

Power plug in , H/W default support USB charge.

Pin power I_3VSB or VBAT
Register power I_3VSB or VBAT
Register reset I_3VSB or VBAT

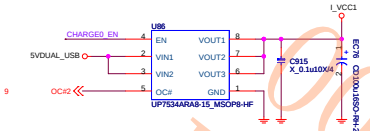
Pin power I_3VSB
Register power I_3VSB
Register reset I_3VSB

Update~2010.9.15

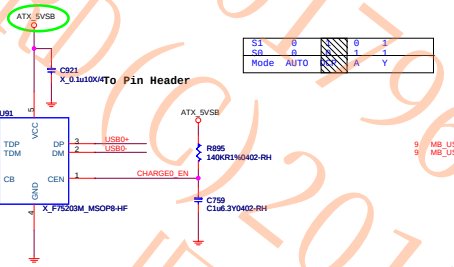


USB POWER PORT 0 For USB Charging

MAX 1.7A

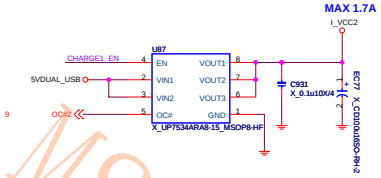


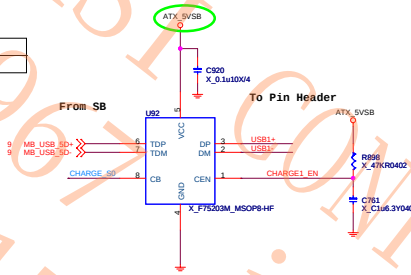
** If your spec will not need bom option, please don't co-lay blue labels.



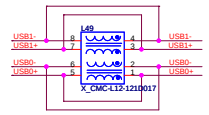
USB POWER PORT 1 For USB Charging

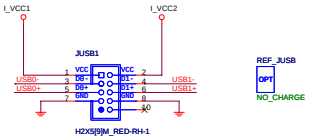
MAX 1.7A





FRONT USB PORT 0,1



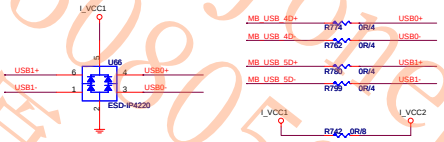


Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

PI5USB14550 has internal EDS diode.

A type
2.70V< D+ <3.1 V
1.85V< D- < 2.1V
For i-Pad / i-Phone 4G charges current up to 1.6A.

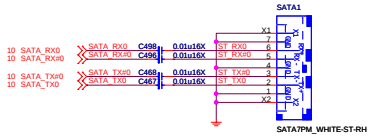
COLAY remove USB charger ic



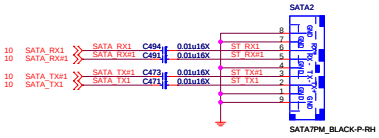
Title	USB FULL CHARGE		
Size	Document Number		Rev
Custom	MS-7758		4.0
Date:	Tuesday, June 26, 2012	Sheet 25 of 44	

SATA 6G PORT 0

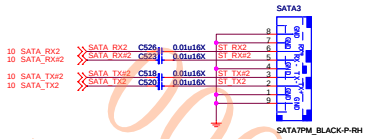
3.0 white

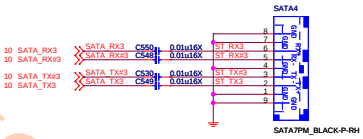


SATA 3G PORT 2

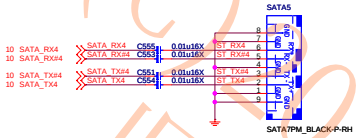


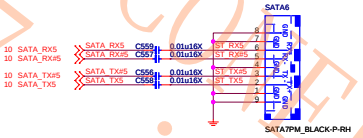
SATA 3G PORT 3,4





SATA 3G PORT 5,6





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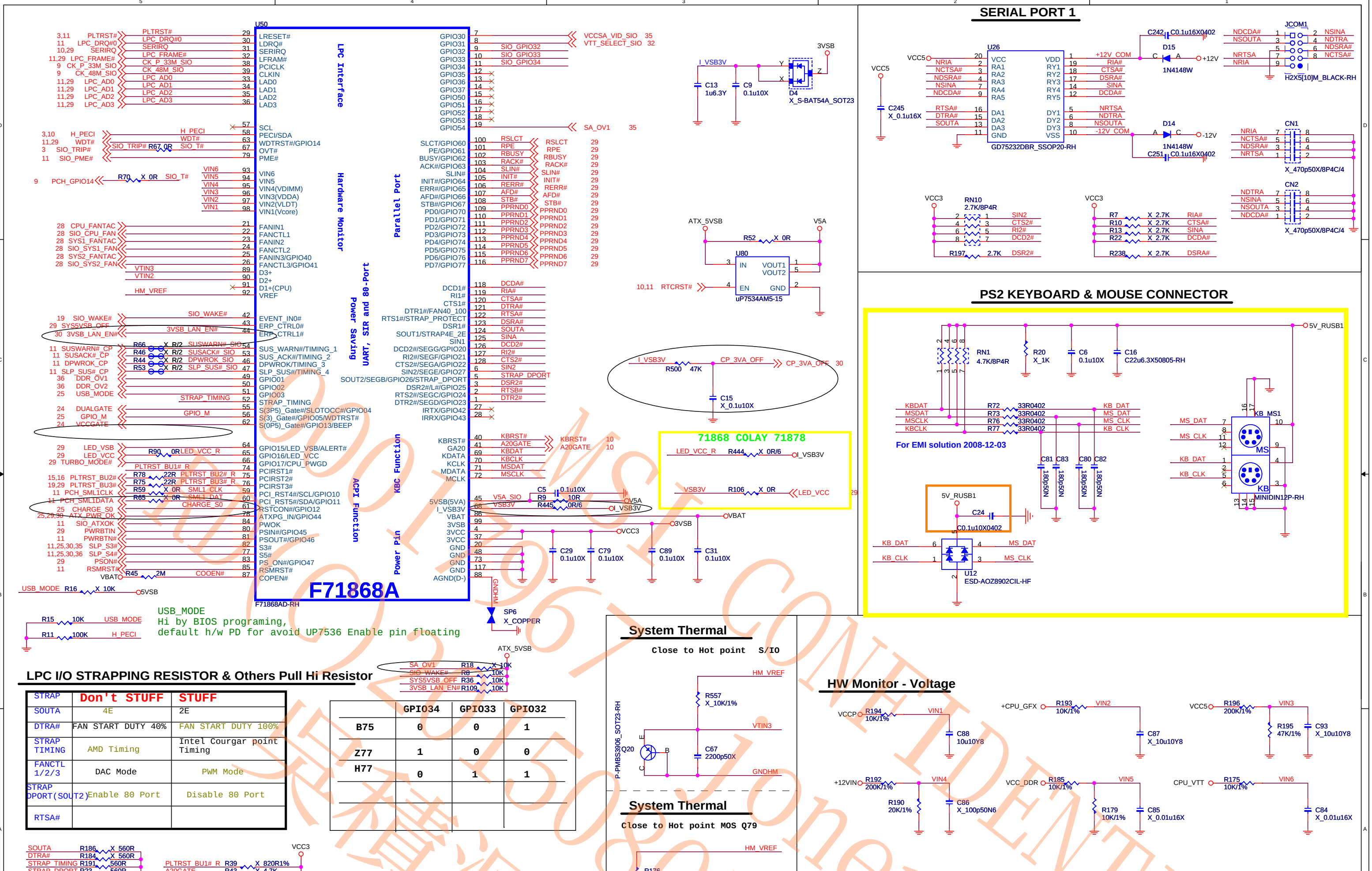
MS-7758		
Size: Custom	Document Description: SATA Connector	Rev: 4.0
Date: Monday, June 25, 2012	Sheet 26 of 44	



LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		

	GPIO34	GPIO33	GPIO32
B75	0	0	1
Z77	1	0	0
H77	0	1	1

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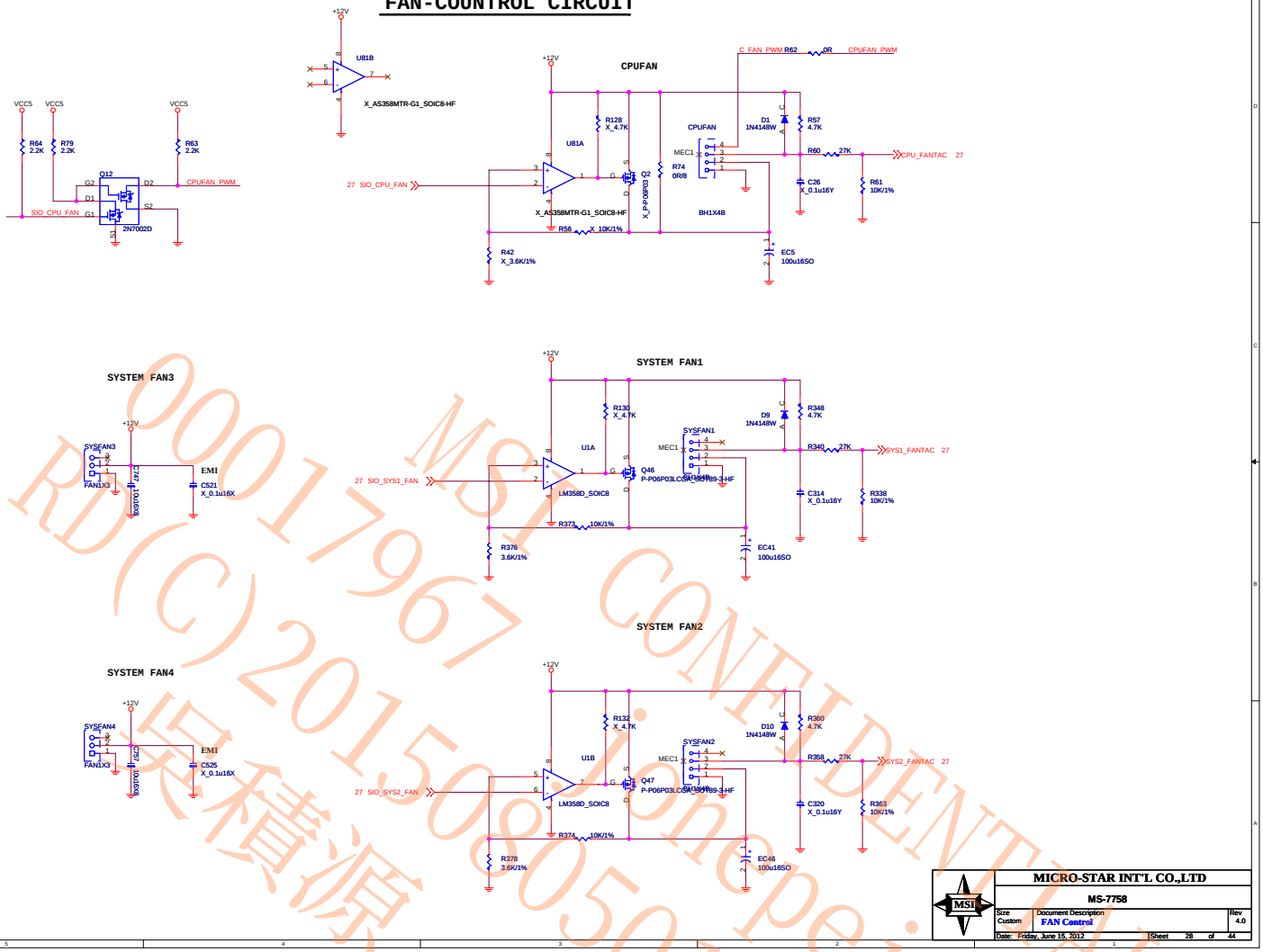
MS-7758

Size: Custom | Document Description: SIO-Fintek F71869AD | Rev: 4.0

Date: Monday, June 25, 2012 | Sheet 27 of 44

FAN-COUNTROL CIRCUIT



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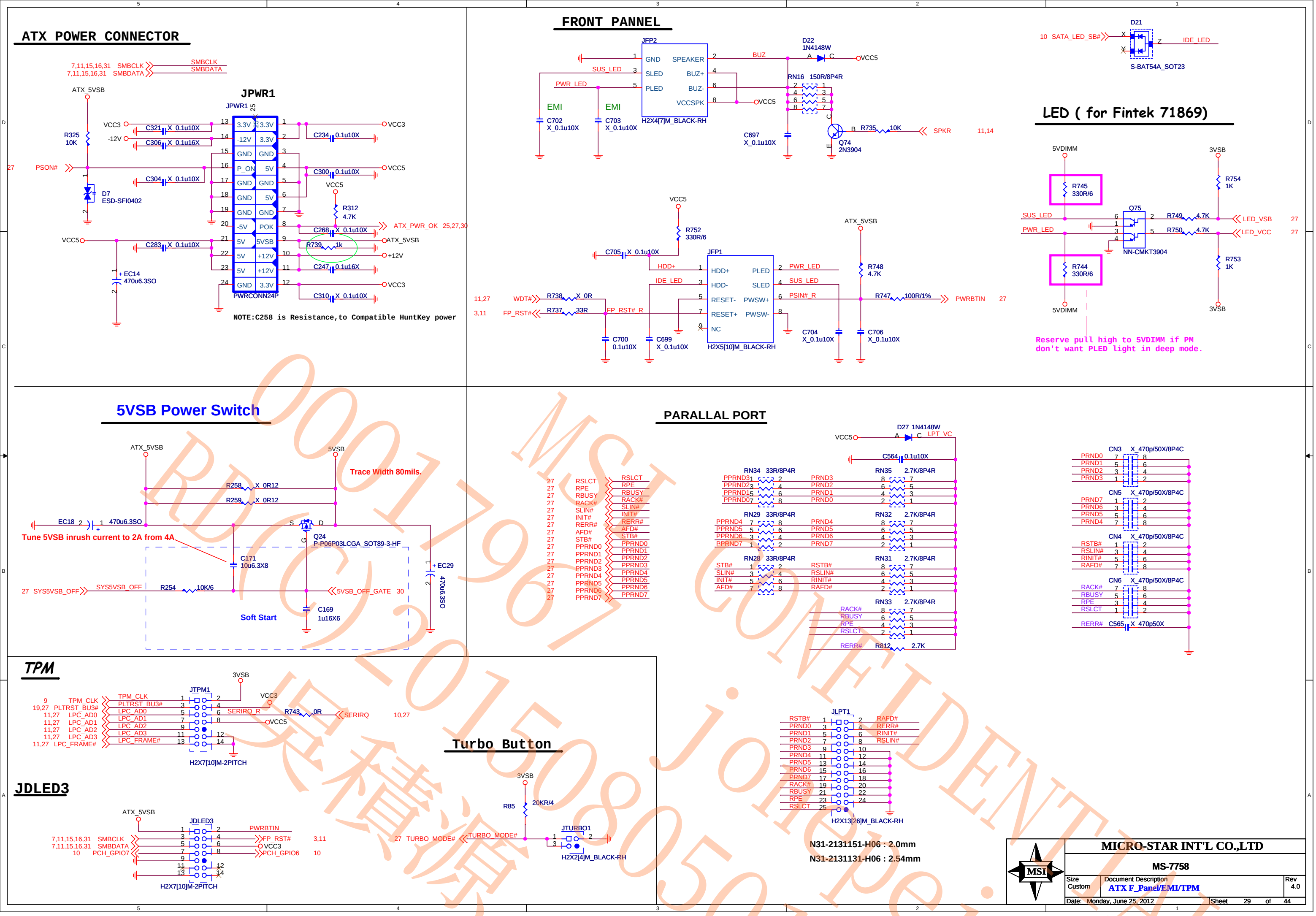
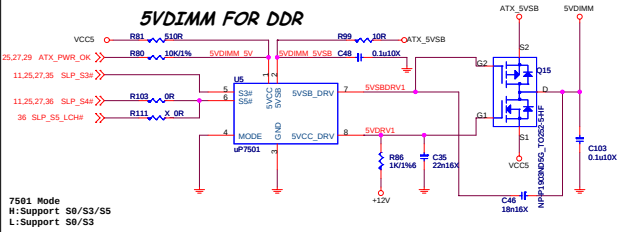
MS-7758		
Size: Custom	Document Description: FAN Control	Rev: 4.0
Date: Friday, June 15, 2012	Sheet 28 of 44	

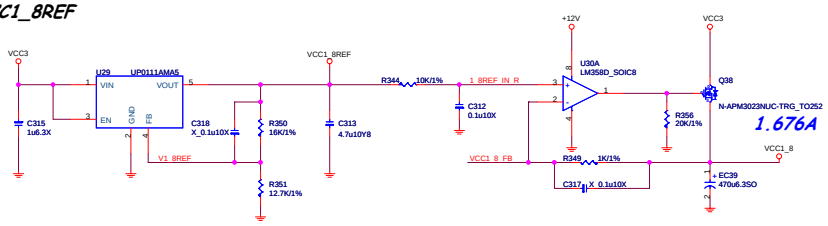


5VDIMM FOR DDR

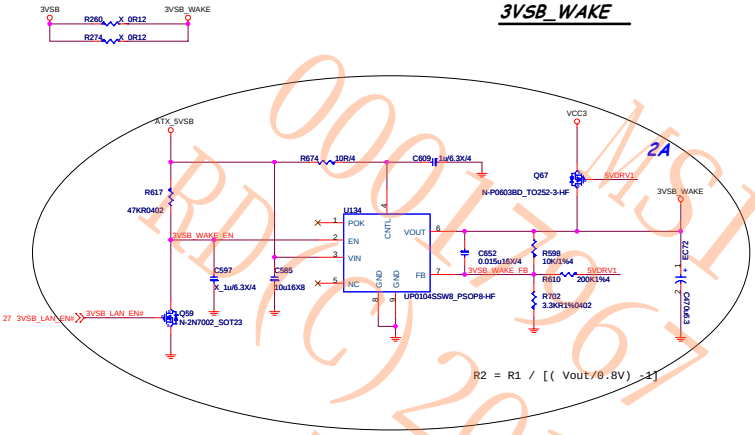


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

VCC1_8REF

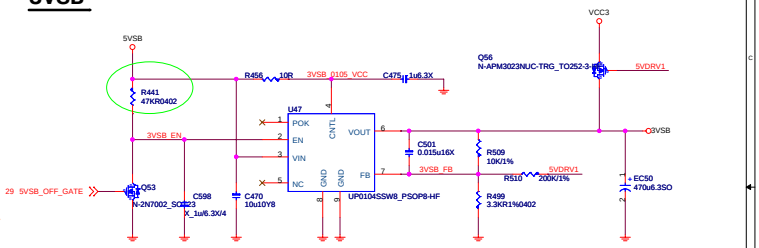


3VSB_WAKE



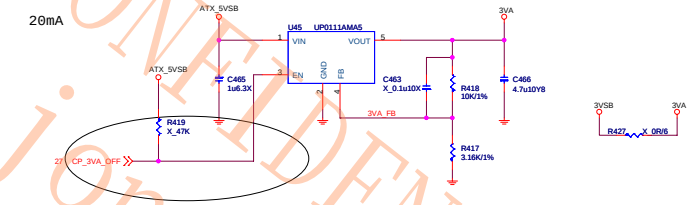
R2 = R1 / [(Vout/0.8V) -1]

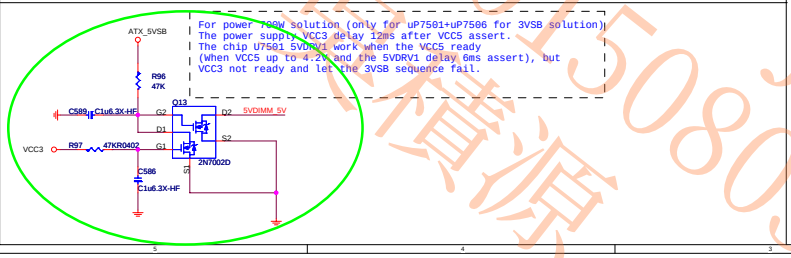
3VSB



3VA

20mA





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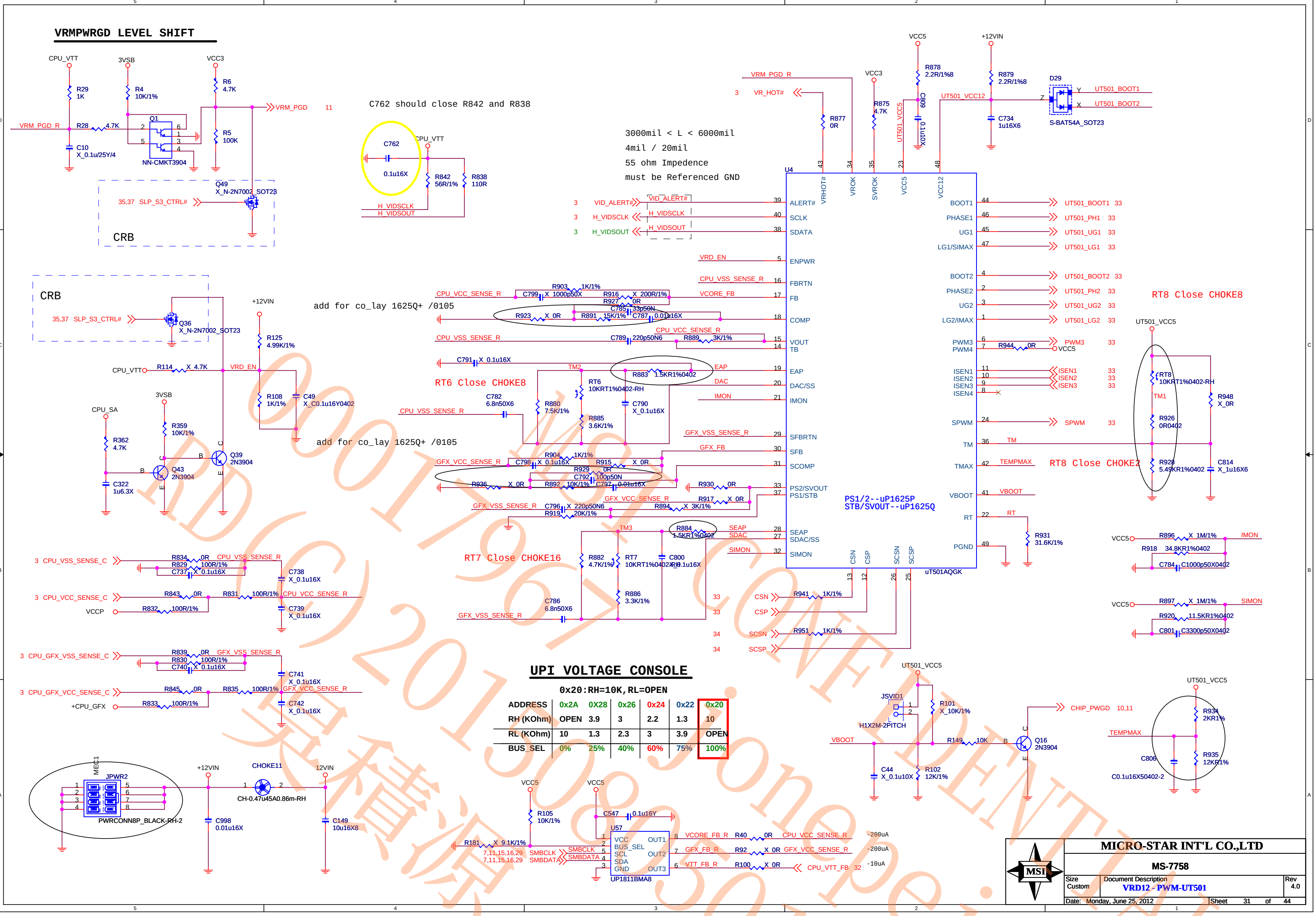
MS-7758		
Size: Custom	Document Description: ACPI controller UPI	Rev: 4.0
Date: Monday, June 25, 2012	Sheet 30 of 44	



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	VRD12 - PWM-UT501	4.0

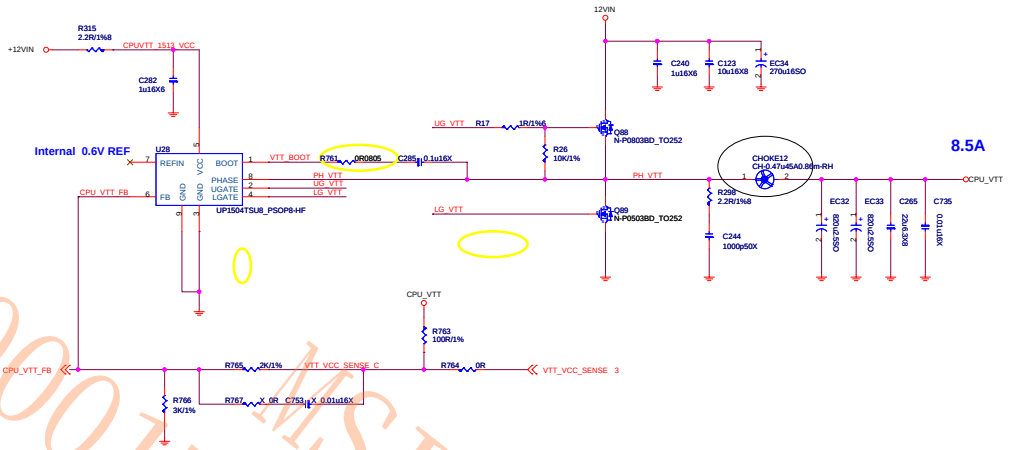
Date: Monday, June 25, 2012 Sheet 31 of 44

CPU_VTT:1.05/1.00 *MAX 17.3A*

CPU VTT 8.5A SA Core =8.8A

8.5A FOR CPU

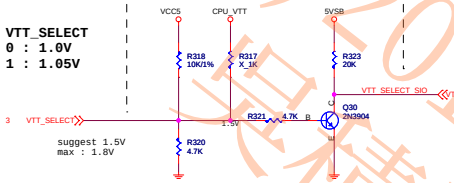
Iripple=1.92(vtt)+1.88(sa)
5*1=5A>3.8A

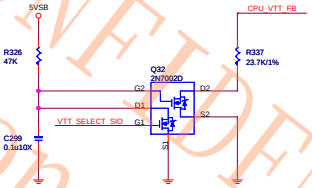


VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

VTT_SELECT
0 : 1.0V
1 : 1.05V





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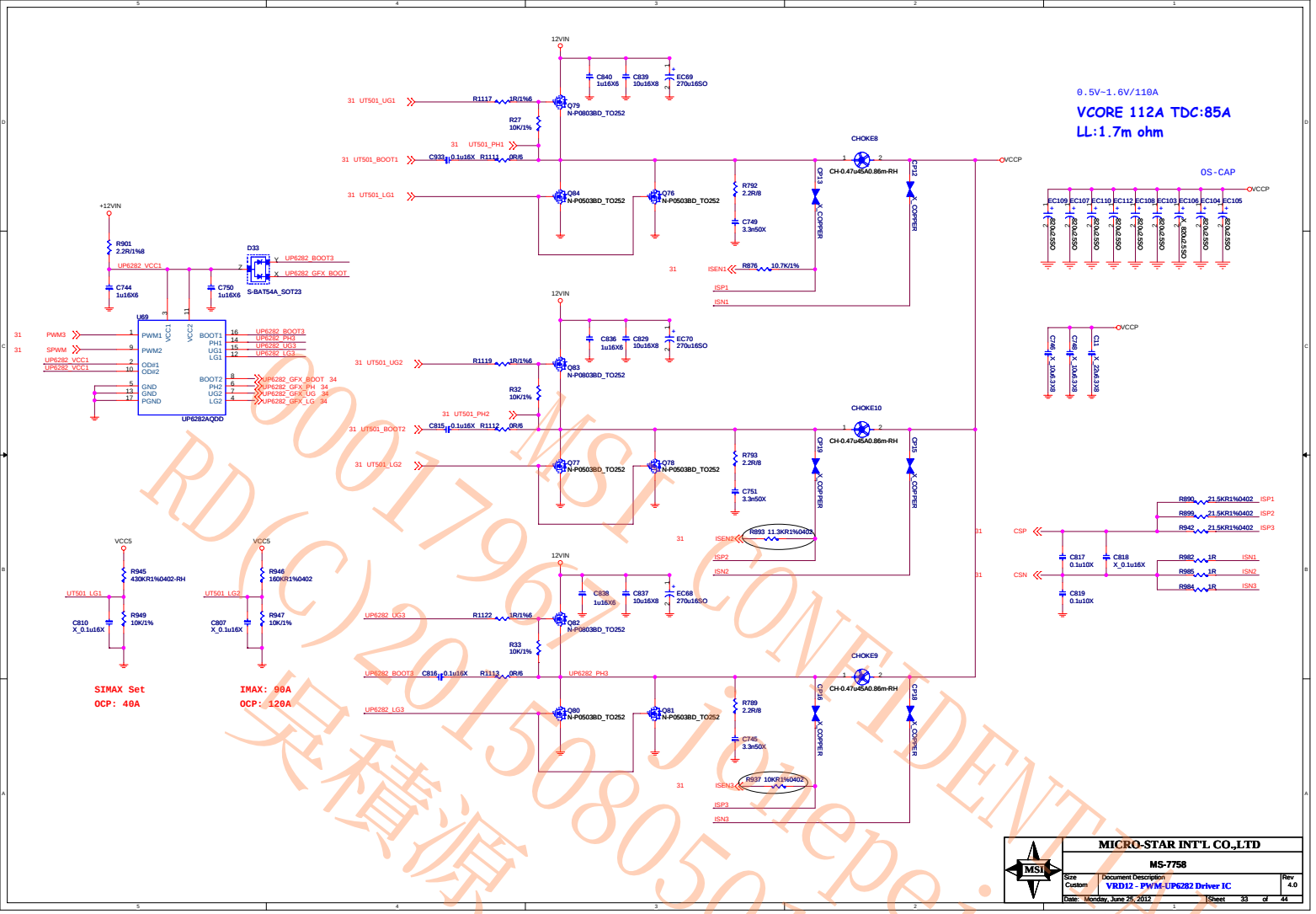
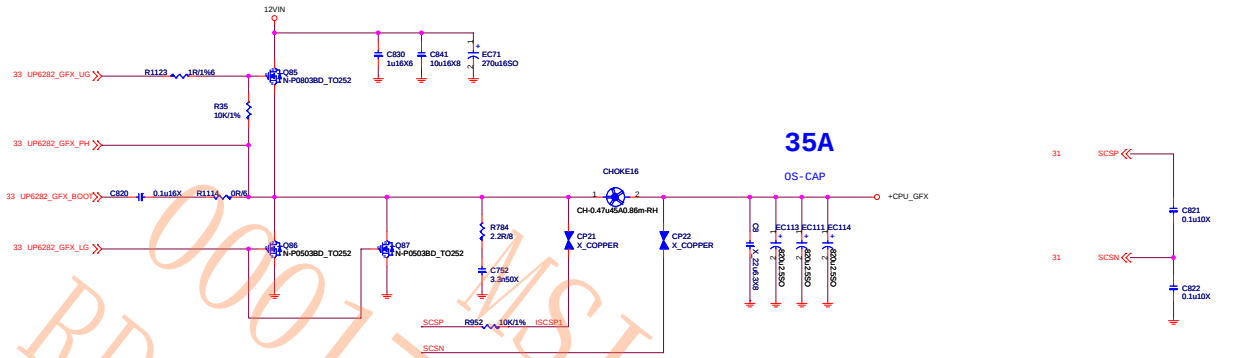
MS-7758		
Size: Custom	Document Description: VTT POWER- uP1513- 1Phase MOS	Rev: 4.0
Date: Monday, June 25, 2012	Sheet 32 of 44	



CPU_GFX:0.25-1.52

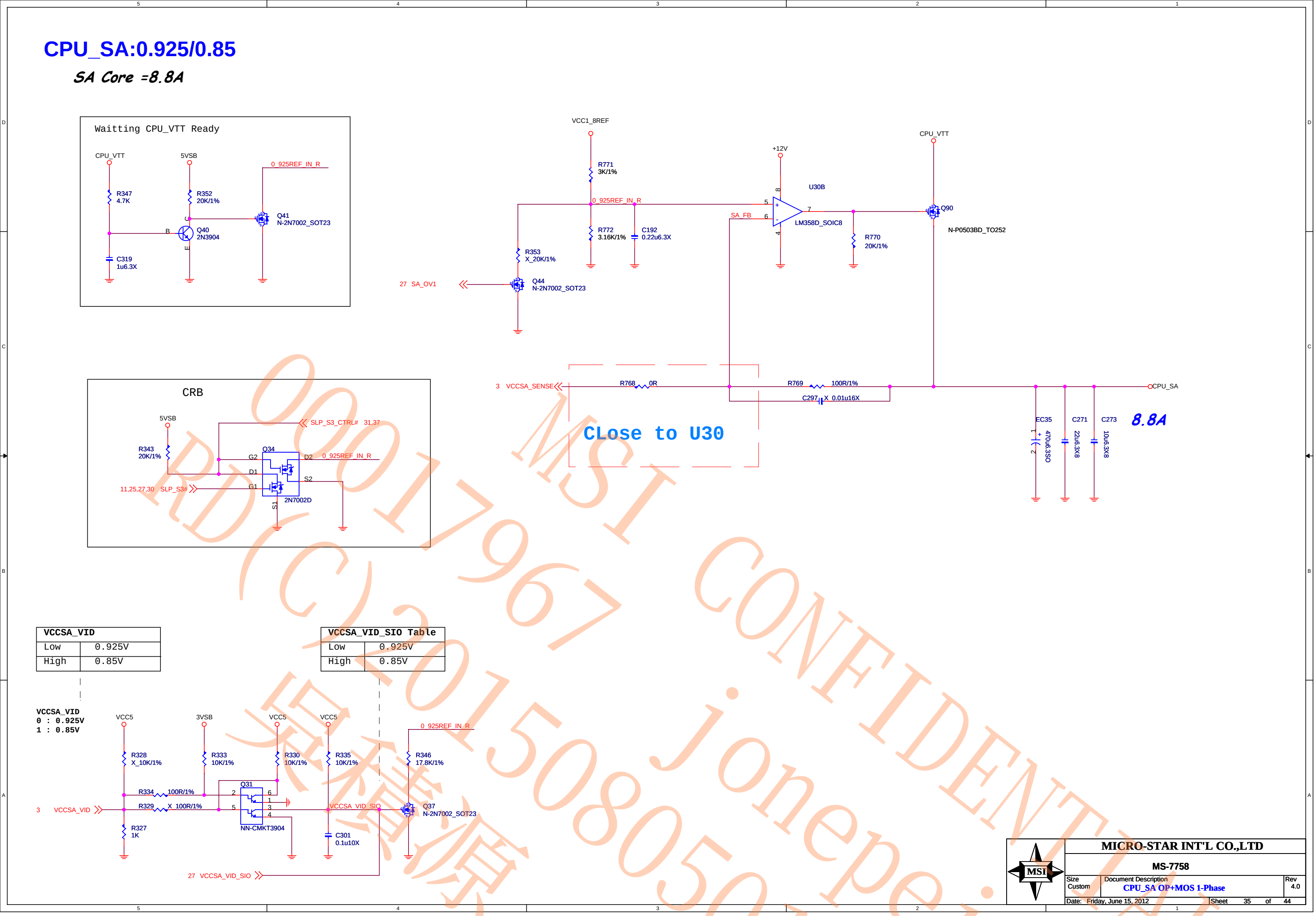
35A FOR CPU



MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: VRD12 -GPU 1-Phase MOS	Rev: 4.0
Date: Friday, June 15, 2012	Sheet 34 of 44	

CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

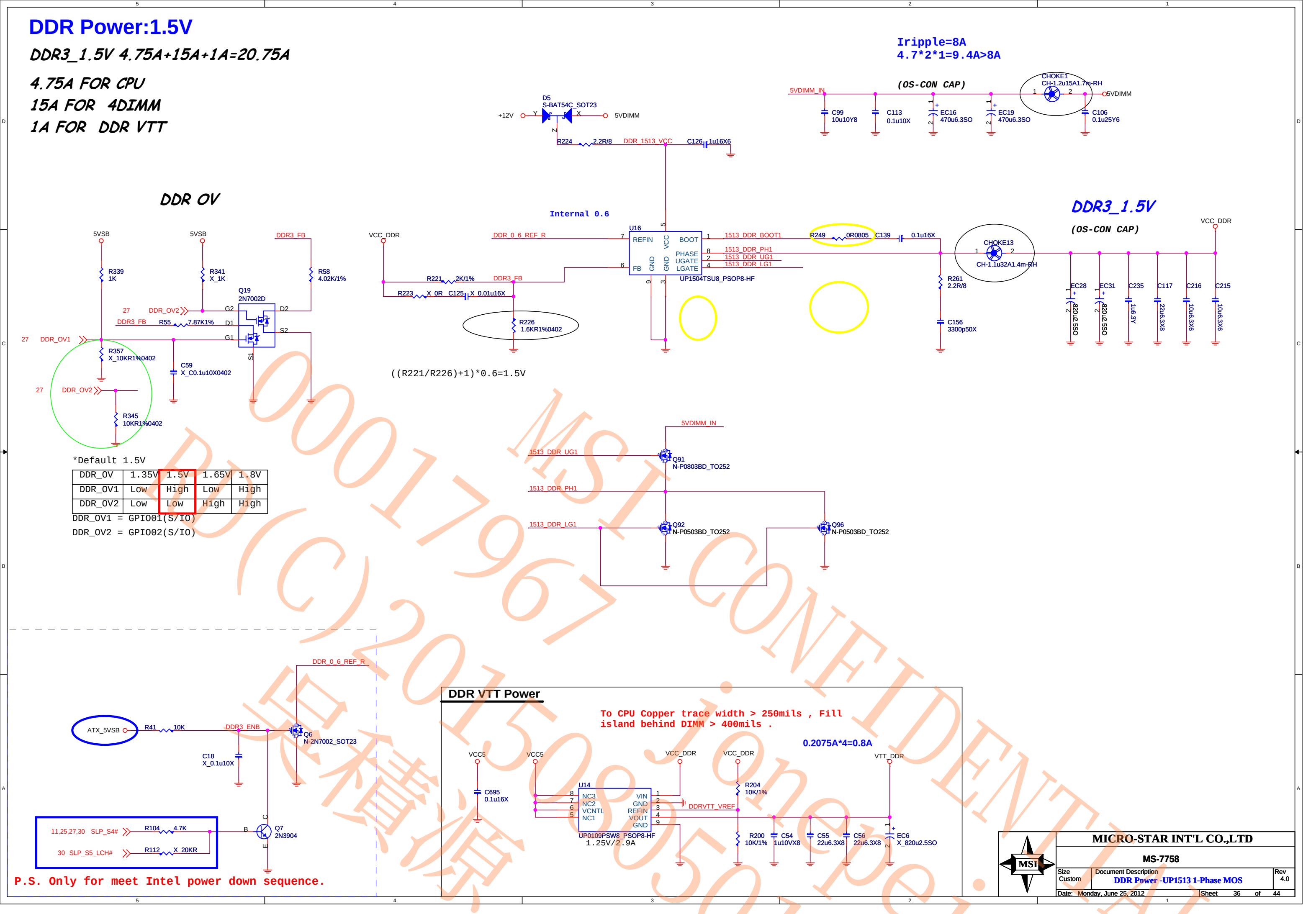
VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

MICRO-STAR INT'L CO.,LTD

MS-7758

Size: Custom | Document Description: CPU_SA OP+MOS 1-Phase | Rev 4.0

Date: Friday, June 15, 2012 | Sheet 35 of 44



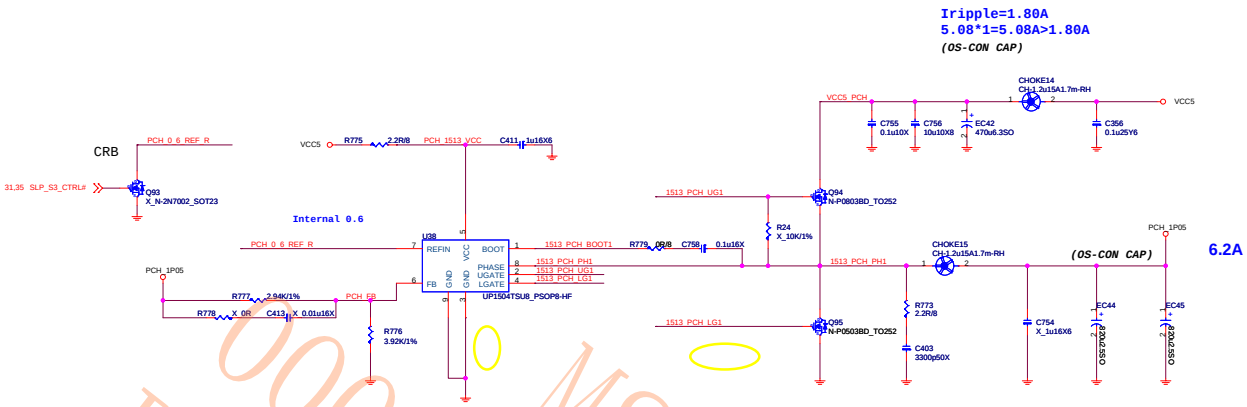
*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)

PCH Power:1.05V

PCH Core 6.2A

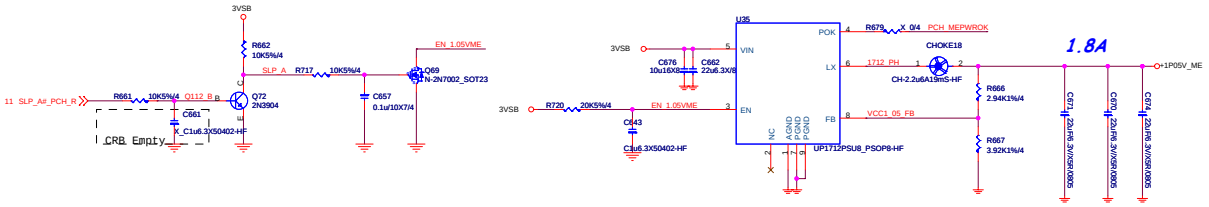


MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: PCH Power - uP1513 1-Phase MOS	Rev: 4.0
Date: Friday, June 15, 2012	Sheet 37 of 44	

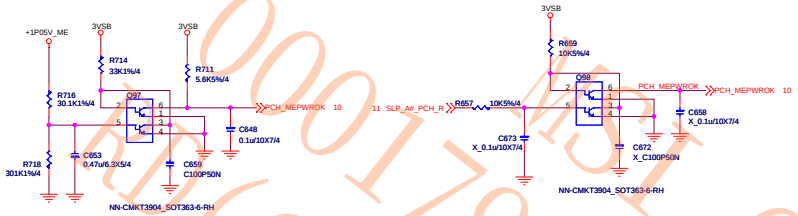
SLP_A

ME Power Control

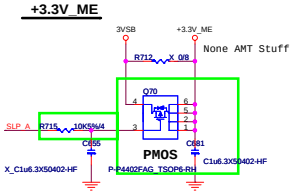
+1.05V_ME(VCCIO_ME)



PCH_MEPWROK



+3.3V_ME



0.09(LAN_1P05)+0.332(+3.3_LAN)+
0.025(SPI ROM MAX)+0.02(SB VCCSPI)=0.467A

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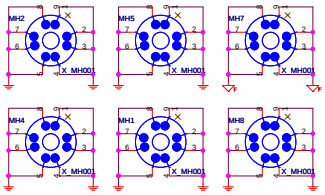
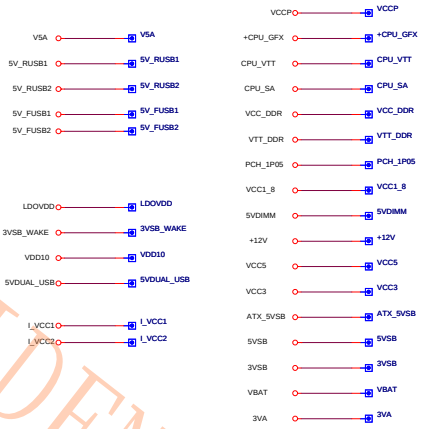
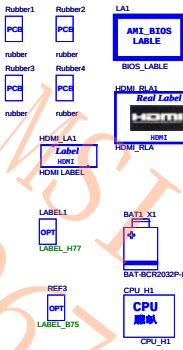
MS-7758		
Size: Custom	Document Description: ME Power - UP1712	Rev: 4.0
Date: Monday, June 25, 2012	Sheet 38 of 44	

Mounting Holes

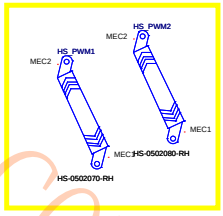


Voltage test point



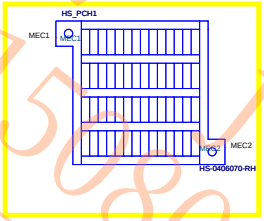


HEATSINK



Simulation

Optical Fiducial Marks-120



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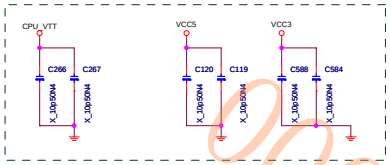
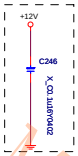
MS-7758		
Size: Custom	Document Description: XDP / Manual Parts	Rev: 4.0
Date: Wednesday, June 27, 2012	Sheet 39 of 44	

EMI:cap. for signal return path



EMI



MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size: Custom	Document Description: EMI CAP	Rev: 4.0
Date: Friday, June 15, 2012	Sheet 40 of 44	