MS-7758

ATX

Ver: 10(304.8x243.84)

Intel -MahoBay plamform H77

CPU:

IVY bridge LGA1155

System Chipset:

Panther Point H77(CO-LAY Z77)

Onboard Chip:

HD Audio Codec:ALC892 colay 887
LAN-RTL8111E colay8105E
SIO:Fintek F71868AD
Flash ROM: SPI 64 MB

Main Memory:

*DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12 -UT501 3+1 Phase

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2*
*PCI Express (X4) Slot * 1*
*PCI Slot * 3*

Other:

SATA3.0 x2+SATA2.0 x4 (PCH)
*USB2.0 *10*
*REAL USB3.0 *2*
*FRONT USB3.0 *2*

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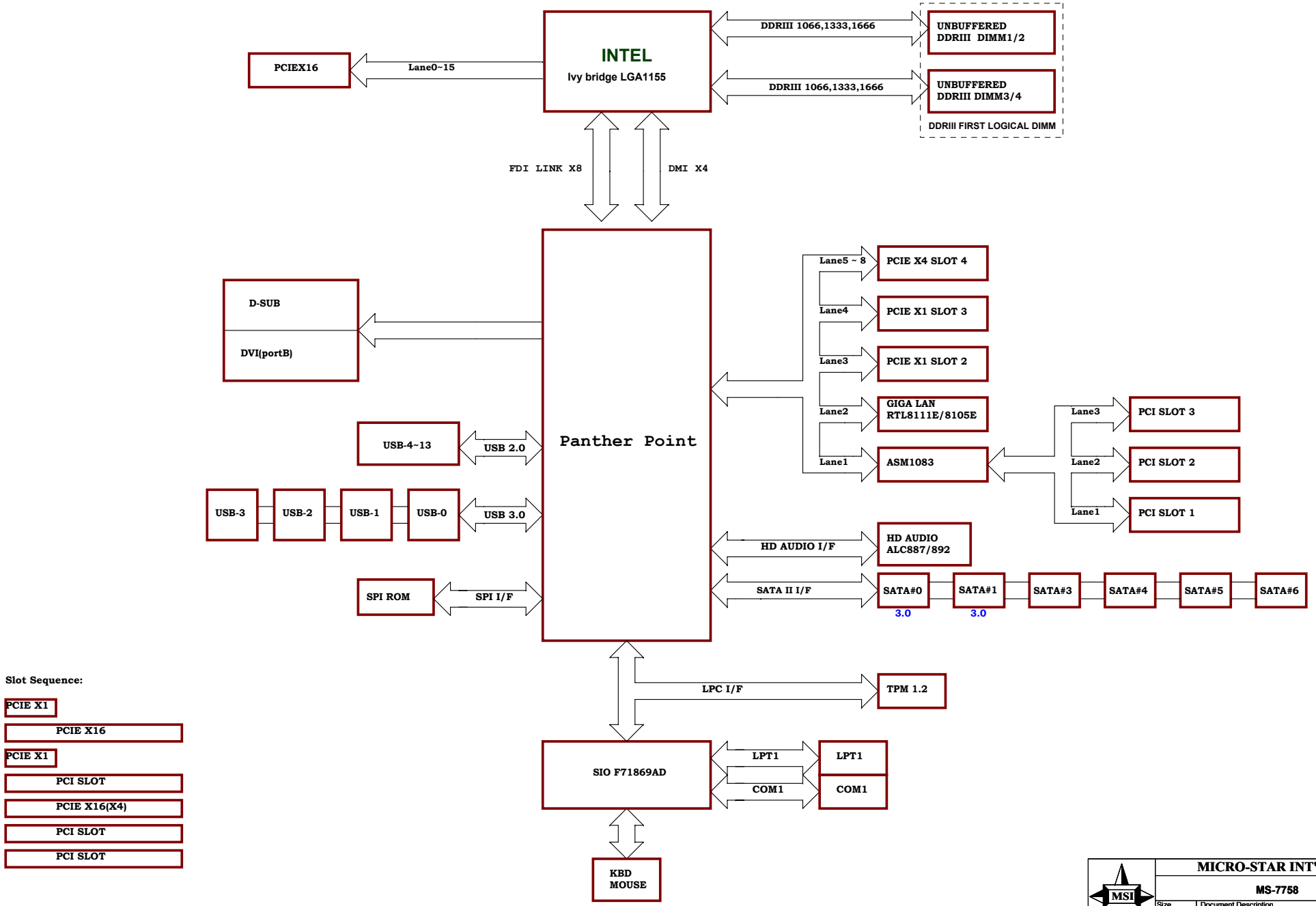
MS-7758 Block Diagram



Slot Sequence:

- PCIE X1
- PCIE X16
- PCIE X1
- PCI SLOT
- PCIE X16(X4)
- PCI SLOT
- PCI SLOT

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7758	
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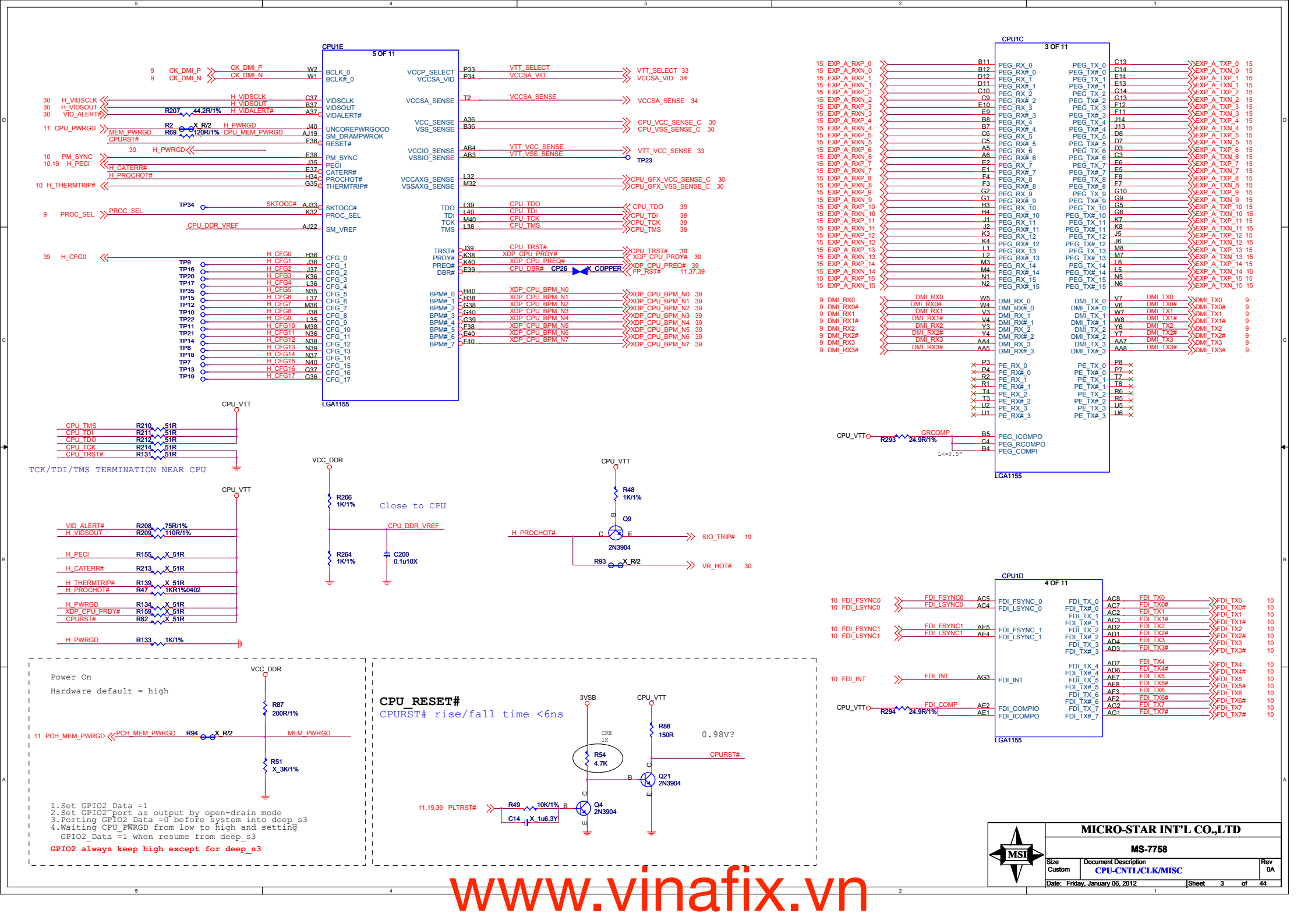

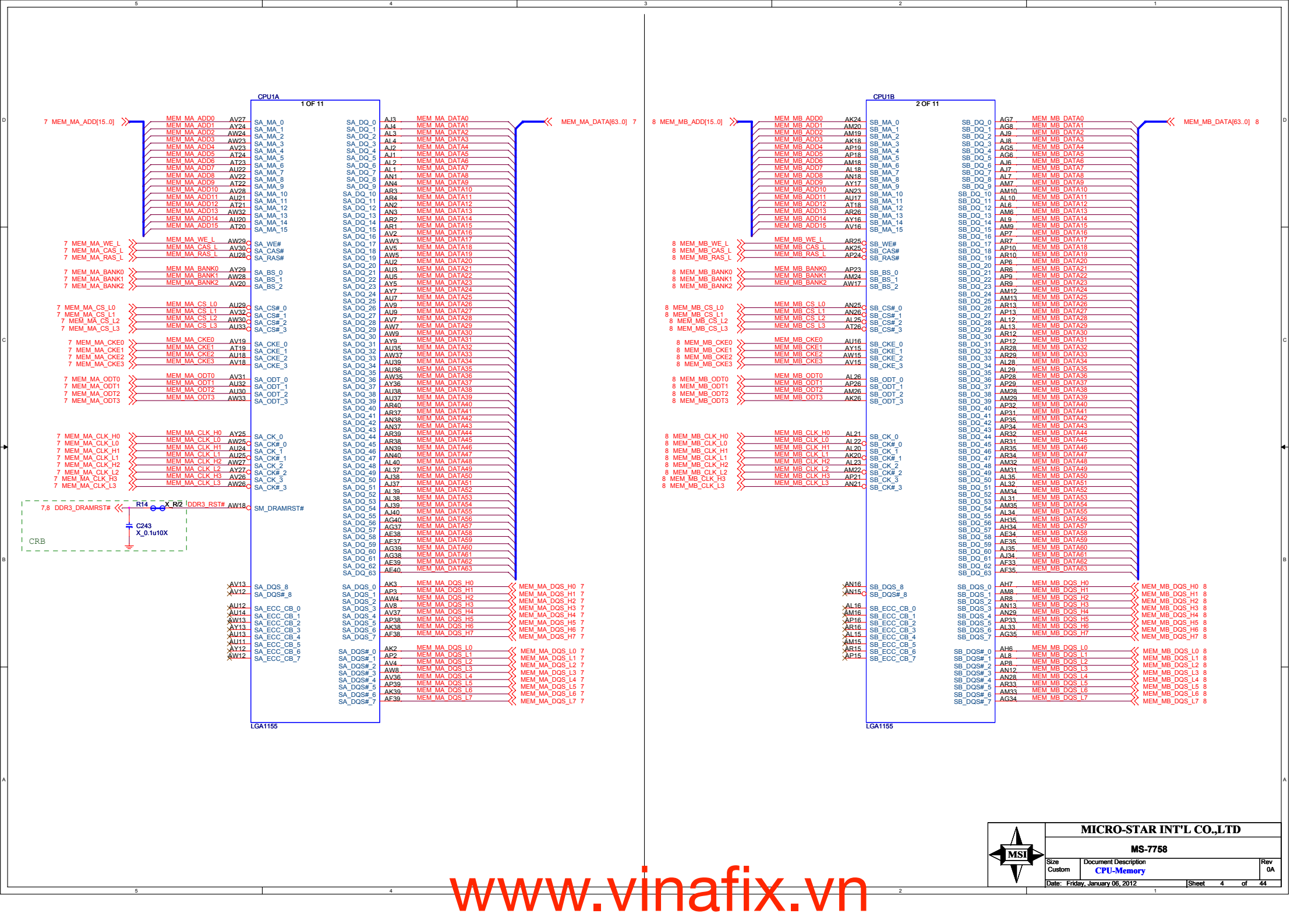

(1.05V / 1.00V)

VCCP

CPU1F
6 OF 11

A12	VCC_001	VCC_082	F32
A13	VCC_002	VCC_083	F33
A14	VCC_003	VCC_084	F34
A15	VCC_004	VCC_085	G15
A16	VCC_005	VCC_086	G16
A18	VCC_006	VCC_087	G18
A24	VCC_007	VCC_088	G19
A25	VCC_008	VCC_089	G21
A27	VCC_009	VCC_090	G22
A28	VCC_010	VCC_091	G24
B15	VCC_011	VCC_092	G25
B16	VCC_012	VCC_093	G27
B18	VCC_013	VCC_094	G28
B24	VCC_014	VCC_095	G30
B25	VCC_015	VCC_096	G31
B27	VCC_016	VCC_097	G32
B28	VCC_017	VCC_098	G33
B30	VCC_018	VCC_099	H13
B31	VCC_019	VCC_100	H14
B33	VCC_020	VCC_101	H15
B34	VCC_021	VCC_102	H16
C15	VCC_022	VCC_103	H18
C16	VCC_023	VCC_104	H19
C18	VCC_024	VCC_105	H21
C19	VCC_025	VCC_106	H22
C21	VCC_026	VCC_107	H24
C22	VCC_027	VCC_108	H25
C24	VCC_028	VCC_109	H27
C25	VCC_029	VCC_110	H28
C27	VCC_030	VCC_111	H30
C28	VCC_031	VCC_112	H31
C30	VCC_032	VCC_113	H32
C31	VCC_033	VCC_114	J12
C33	VCC_034	VCC_115	J15
C34	VCC_035	VCC_116	J16
C36	VCC_036	VCC_117	J18
D13	VCC_037	VCC_118	J19
D14	VCC_038	VCC_119	J21
D15	VCC_039	VCC_120	J22
D16	VCC_040	VCC_121	J24
D18	VCC_041	VCC_122	J25
D19	VCC_042	VCC_123	J27
D21	VCC_043	VCC_124	J28
D22	VCC_044	VCC_125	J30
D24	VCC_045	VCC_126	K15
D25	VCC_046	VCC_127	K16
D27	VCC_047	VCC_128	K18
D28	VCC_048	VCC_129	K19
D30	VCC_049	VCC_130	K21
D31	VCC_050	VCC_131	K22
D33	VCC_051	VCC_132	K24
D34	VCC_052	VCC_133	K25
D35	VCC_053	VCC_134	K27
D36	VCC_054	VCC_135	K28
E15	VCC_055	VCC_136	K30
E16	VCC_056	VCC_137	L13
E18	VCC_057	VCC_138	L14
E19	VCC_058	VCC_139	L15
E21	VCC_059	VCC_140	L16
E22	VCC_060	VCC_141	L18
E24	VCC_061	VCC_142	L19
E25	VCC_062	VCC_143	L21
E27	VCC_063	VCC_144	L22
E28	VCC_064	VCC_145	L24
E30	VCC_065	VCC_146	L25
E31	VCC_066	VCC_147	L27
E33	VCC_067	VCC_148	L28
E34	VCC_068	VCC_149	L30
E35	VCC_069	VCC_150	M14
F15	VCC_070	VCC_151	M15
F16	VCC_071	VCC_152	M16
F18	VCC_072	VCC_153	M18
F19	VCC_073	VCC_154	M19
F21	VCC_074	VCC_155	M21
F22	VCC_075	VCC_156	M22
F24	VCC_076	VCC_157	M24
F25	VCC_077	VCC_158	M25
F27	VCC_078	VCC_159	M27
F28	VCC_079	VCC_160	M28
F30	VCC_080	VCC_161	M30
F31	VCC_081		

LGA1155

VCCP

CPU_VTT

CPU1H
8 OF 11

A11	VCCIO_01	VDDQ_01	AJ13
A7	VCCIO_02	VDDQ_02	AJ14
AA3	VCCIO_03	VDDQ_03	AJ20
AB8	VCCIO_04	VDDQ_04	AJ23
AF8	VCCIO_05	VDDQ_05	AJ24
AG33	VCCIO_06	VDDQ_06	AR20
AJ16	VCCIO_07	VDDQ_07	AR21
AJ17	VCCIO_08	VDDQ_08	AR22
AJ26	VCCIO_09	VDDQ_09	AR23
AJ28	VCCIO_10	VDDQ_10	AR24
AJ32	VCCIO_11	VDDQ_11	AU19
AK15	VCCIO_12	VDDQ_12	AU23
AK17	VCCIO_13	VDDQ_13	AU27
AK19	VCCIO_14	VDDQ_14	AU31
AK21	VCCIO_15	VDDQ_15	AV21
AK23	VCCIO_16	VDDQ_16	AV24
AK27	VCCIO_17	VDDQ_17	AV25
AK29	VCCIO_18	VDDQ_18	AV29
AK30	VCCIO_19	VDDQ_19	AV33
B9	VCCIO_20	VDDQ_20	AW31
D10	VCCIO_21	VDDQ_21	AY23
D6	VCCIO_22	VDDQ_22	AY26
E3	VCCIO_23	VDDQ_23	AY28
E4	VCCIO_24		
G3	VCCIO_25		
G4	VCCIO_26		
J3	VCCIO_27		
J4	VCCIO_28	VCCSA_01	H10
J7	VCCIO_29	VCCSA_02	H11
J8	VCCIO_30	VCCSA_03	H12
L3	VCCIO_31	VCCSA_04	J10
L4	VCCIO_32	VCCSA_05	K10
L7	VCCIO_33	VCCSA_06	K11
M13	VCCIO_34	VCCSA_07	L11
N3	VCCIO_35	VCCSA_08	L12
N4	VCCIO_36	VCCSA_09	M10
N7	VCCIO_37	VCCSA_10	M11
R3	VCCIO_38	VCCSA_11	M12
R4	VCCIO_39		
R7	VCCIO_40		
U3	VCCIO_41		
U4	VCCIO_42		
U7	VCCIO_43		
V8	VCCIO_44	VCCPLL_01	AK11
W3	VCCIO_45	VCCPLL_02	AK12

LGA1155

VCC_DDR

CPU_SA

VCC1_8

(0.925V / 0.85V)

+CPU_GFX

CPU1G
7 OF 11

AB33	VCCAXG_01	VCCAXG_23	T39
AB34	VCCAXG_02	VCCAXG_24	T40
AB35	VCCAXG_03	VCCAXG_25	U33
AB36	VCCAXG_04	VCCAXG_26	U34
AB37	VCCAXG_05	VCCAXG_27	U35
AB38	VCCAXG_06	VCCAXG_28	U36
AB39	VCCAXG_07	VCCAXG_29	U37
AB40	VCCAXG_08	VCCAXG_30	U38
AC33	VCCAXG_09	VCCAXG_31	U39
AC34	VCCAXG_10	VCCAXG_32	U40
AC35	VCCAXG_11	VCCAXG_33	W33
AC36	VCCAXG_12	VCCAXG_34	W34
AC37	VCCAXG_13	VCCAXG_35	W35
AC38	VCCAXG_14	VCCAXG_36	W36
AC39	VCCAXG_15	VCCAXG_37	W37
AC40	VCCAXG_16	VCCAXG_38	W38
T33	VCCAXG_17	VCCAXG_39	Y33
T34	VCCAXG_18	VCCAXG_40	Y34
T35	VCCAXG_19	VCCAXG_41	Y35
T36	VCCAXG_20	VCCAXG_42	Y36
T37	VCCAXG_21	VCCAXG_43	Y37
T38	VCCAXG_22	VCCAXG_44	Y38

LGA1155

VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A

+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS

VCC_DDR
C214 22u6.3X8
C193 22u6.3X8
C226 22u6.3X8

+CPU_SA Decoupling

Backside

CPU_SA
C733 22u6.3X8

+VCC1_8 Decoupling

Backside

VCC1_8
C12 22u6.3X8
VCC1_8
C732 X_22u6.3X8

+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

CPU_VTT
C183 22u6.3X8
C211 22u6.3X8
C229 22u6.3X8
C187 22u6.3X8
C238 22u6.3X8
C239 22u6.3X8
C196 22u6.3X8
C205 22u6.3X8
C720 22u6.3X8

Backside

CPU_VTT
C711 X_22u6.3X8
C714 X_22u6.3X8
C719 X_22u6.3X8
C722 X_22u6.3X8
C727 X_22u6.3X8
C726 X_22u6.3X8
C728 X_22u6.3X8
C712 X_22u6.3X8
C715 X_22u6.3X8
C717 X_22u6.3X8
C709 X_22u6.3X8
C725 X_22u6.3X8
C731 X_22u6.3X8
C730 X_22u6.3X8
C729 X_22u6.3X8
C237 X_22u6.3X8

+CPU_GFX Decoupling

CPU SOCKET CAVITY CAPS

+CPU_GFX
C180 22u6.3X8
C185 22u6.3X8
C181 22u6.3X8
C186 22u6.3X8
C195 22u6.3X8
C182 22u6.3X8

Backside

+CPU_GFX
C710 X_22u6.3X8
C707 X_22u6.3X8
C709 X_22u6.3X8

+CPU_VCCP-Decoupling

CPU SOCKET CAVITY CAPS

VCCP
C194 22u6.3X8
C203 22u6.3X8
C209 22u6.3X8
C217 22u6.3X8
C223 22u6.3X8
C231 22u6.3X8
C204 22u6.3X8
C210 22u6.3X8
C218 22u6.3X8
C224 22u6.3X8
C232 22u6.3X8
C219 22u6.3X8
C225 22u6.3X8

Backside

VCCP
C713 X_22u6.3X8
C718 X_22u6.3X8
C721 X_22u6.3X8
C716 X_22u6.3X8
C723 X_22u6.3X8
C724 X_22u6.3X8
C233 X_22u6.3X8

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Custom	CPU-Power	0A

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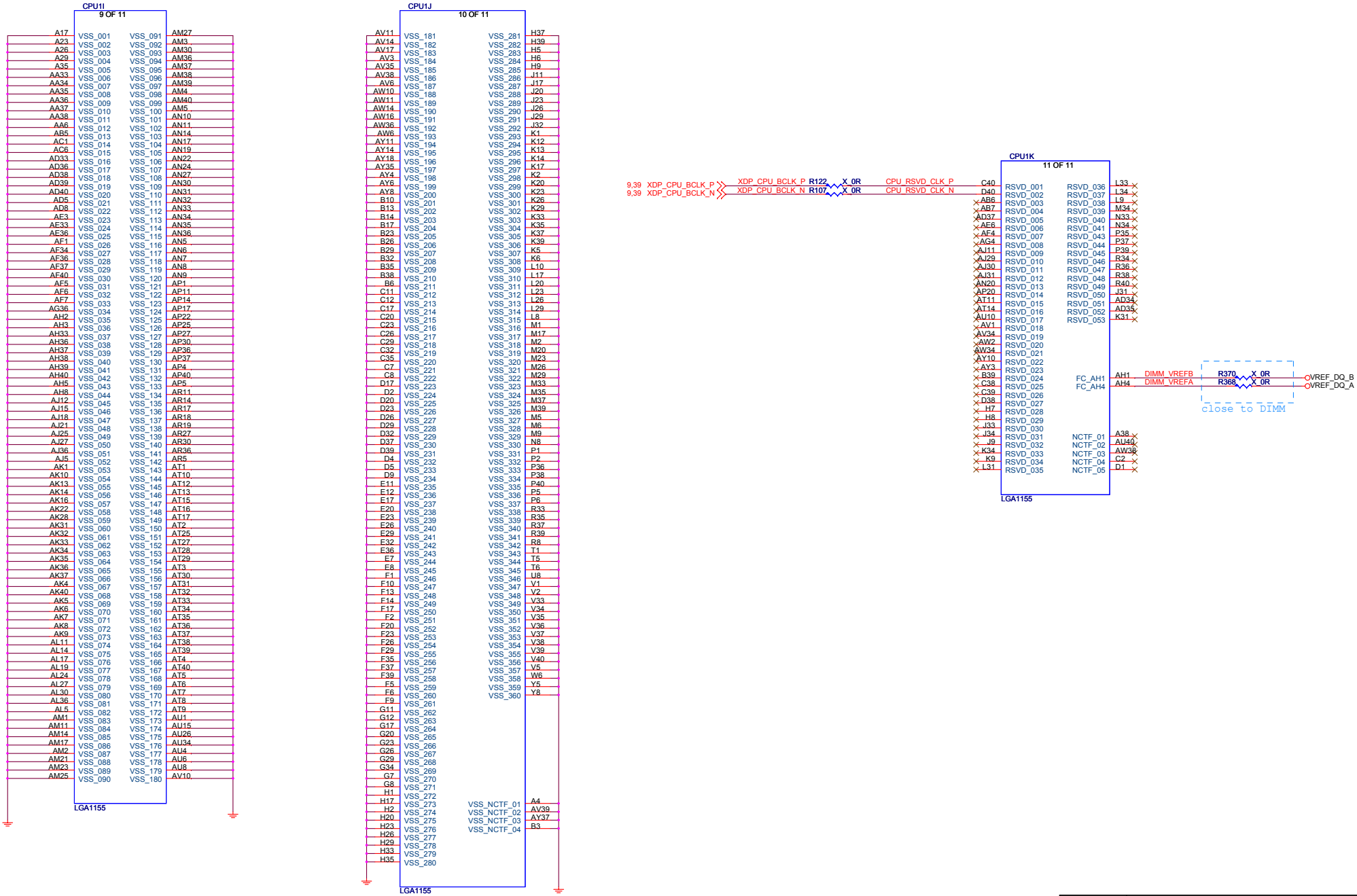

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Size: Custom	Document Description: CPU-GND
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DDRIII DIMM_A0

DDRIII DIMM_A1

DDR3

DDR3

DIMM2 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

Place close to DIMM1

Place close to DIMM1 with DIMM2

Place close to DIMM2

UPI VOLTAGE CONSOLE

UPI VOLTAGE CONSOLE

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
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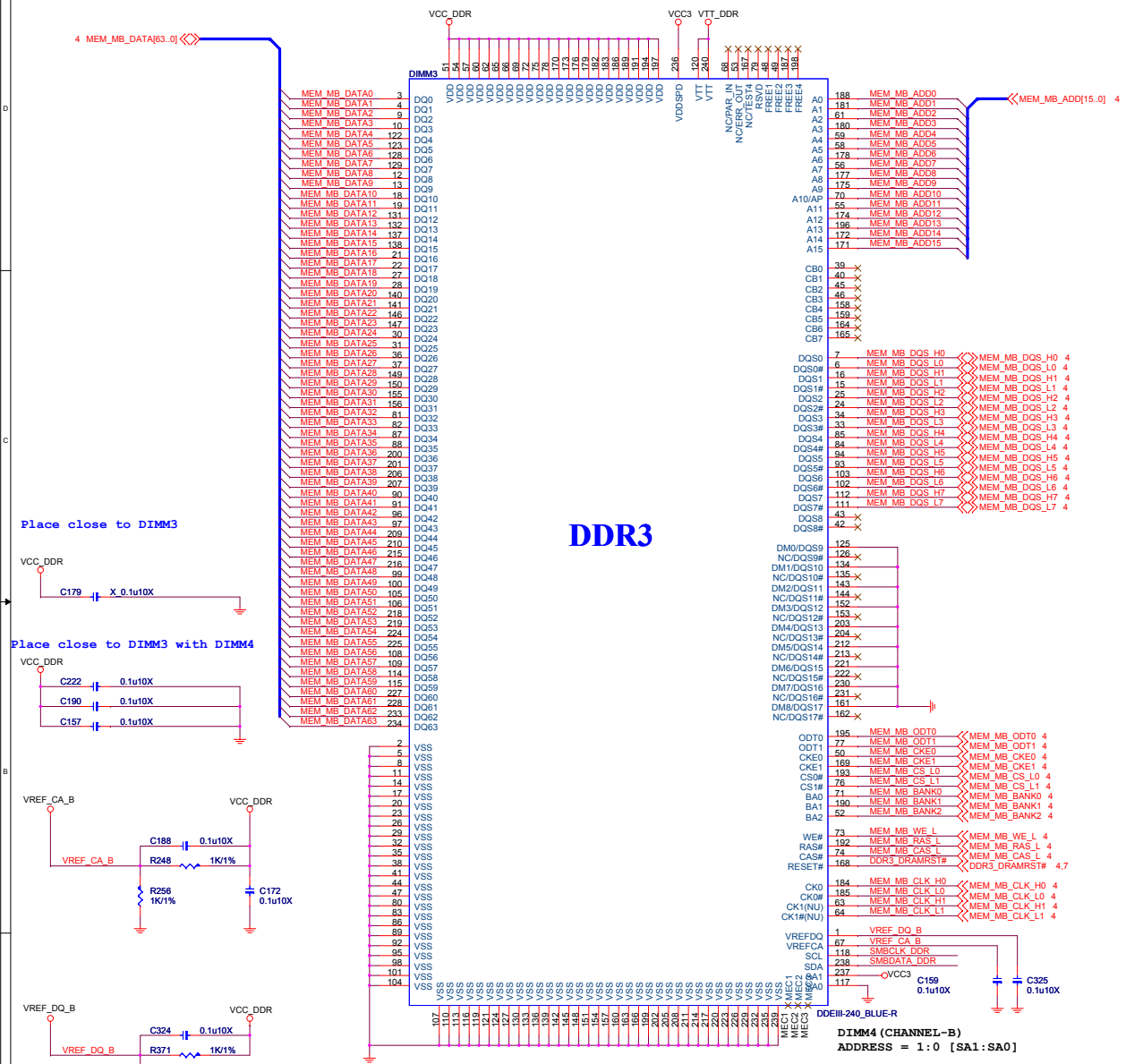
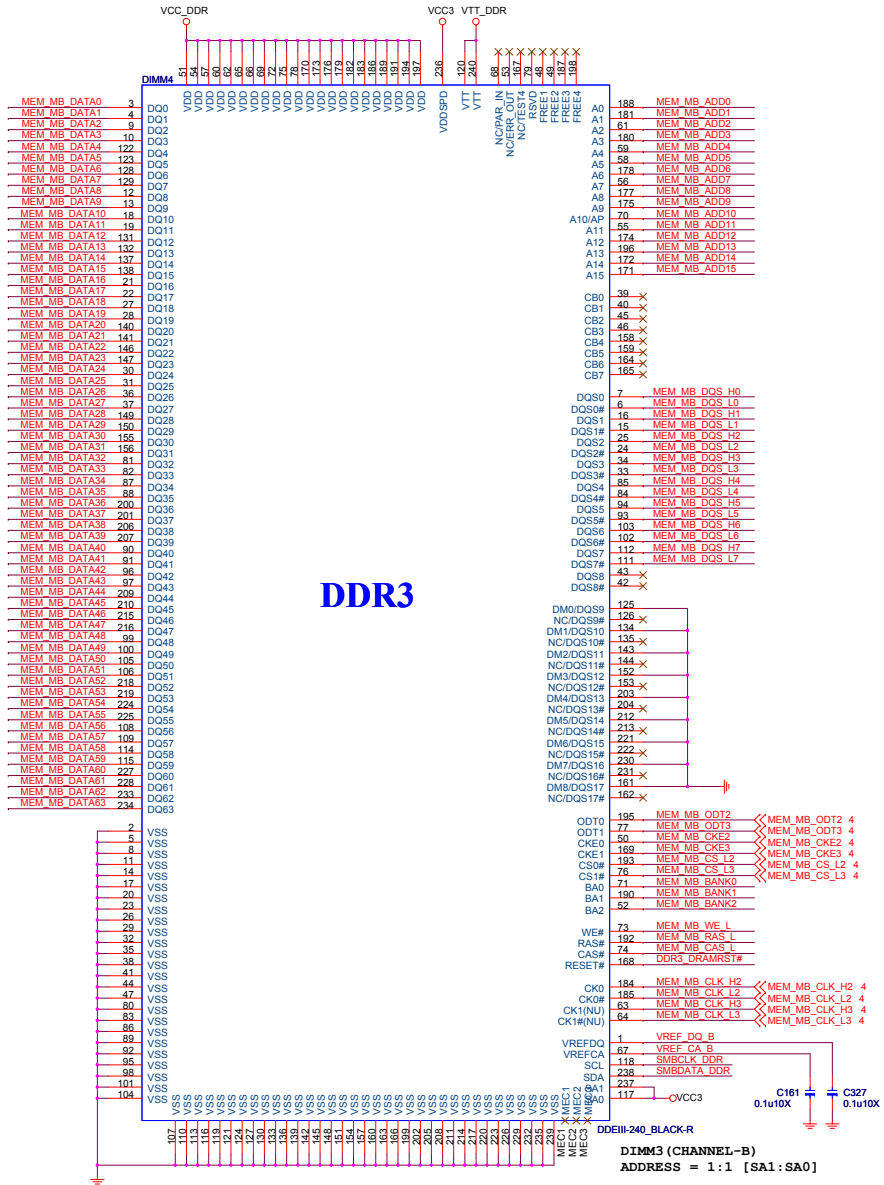
DDRIII DIMM_B0



DDRIII DIMM_B1



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MS-7758	
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4 — Rev: 0A
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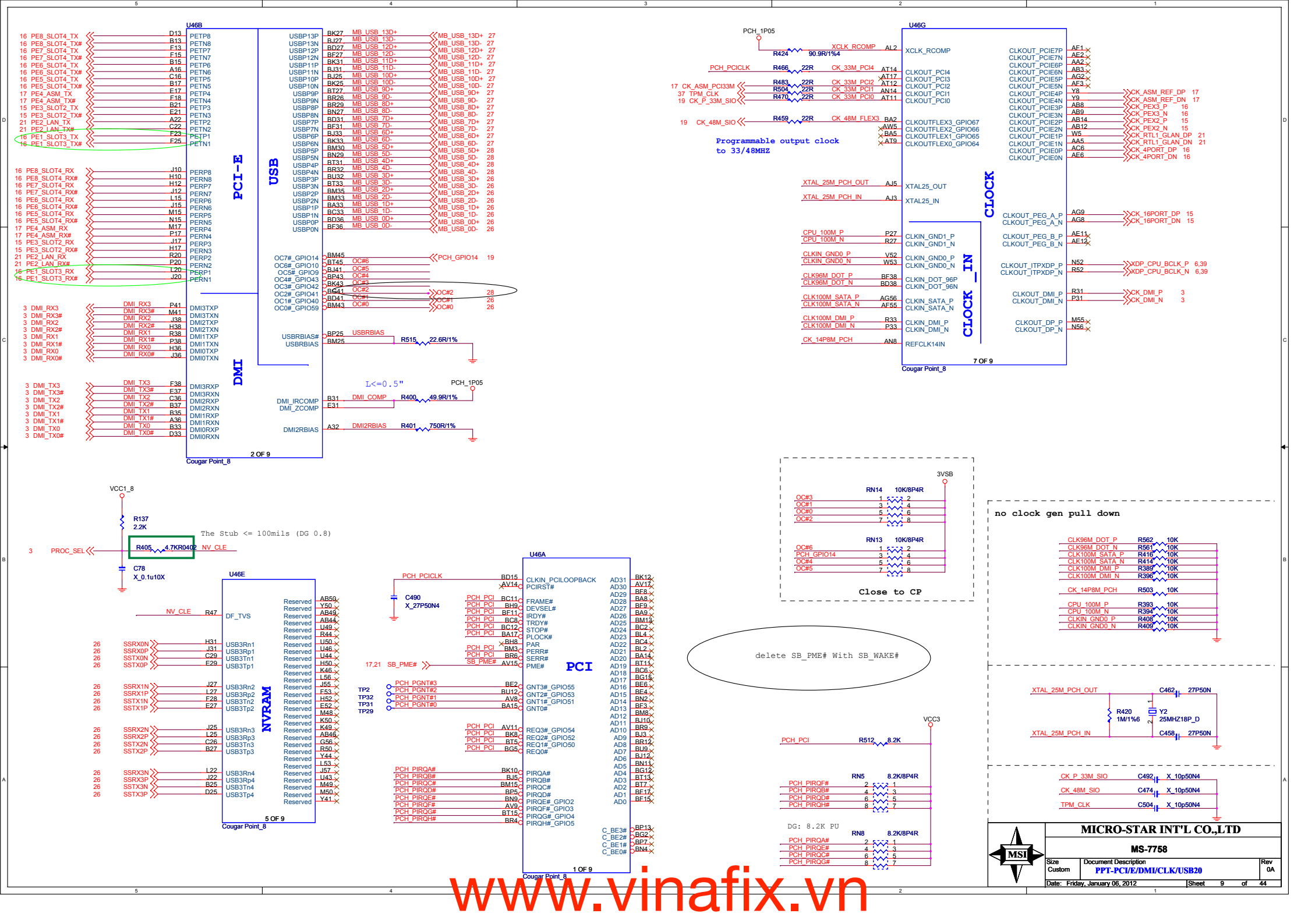
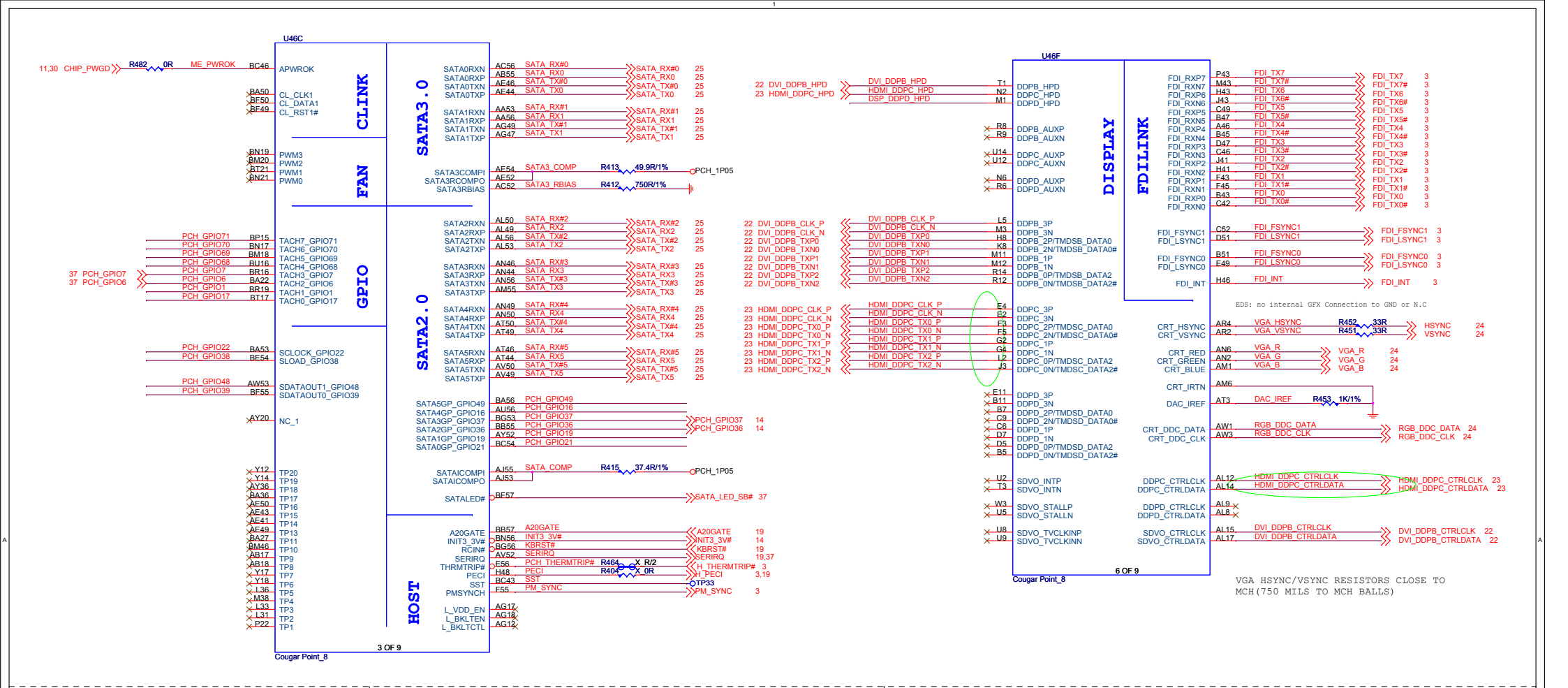
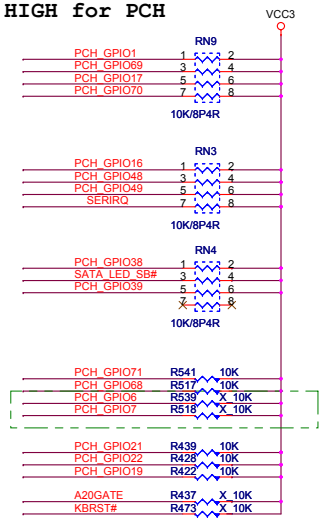




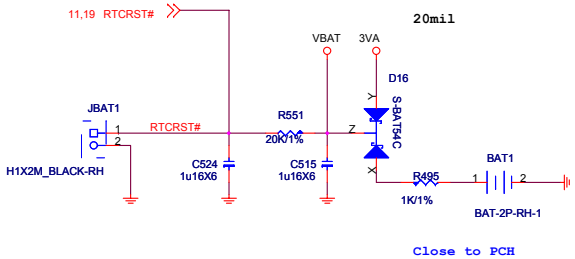
Pull HIGH for PCH



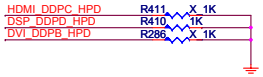
RTC and CLR_CMOS

Clear CMOS

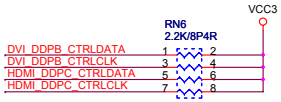
CMOS CLEAR JUMPER JBAT1 Clear CMOS	
1 - 2	Clear CMOS



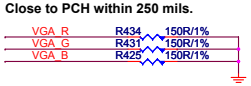
No Display port(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



Close to PCH within 250 mils.



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Size: Custom	Document Description: PPT-SATA/HOST/GPIO/VGA/CCMOS	Rev: 0A
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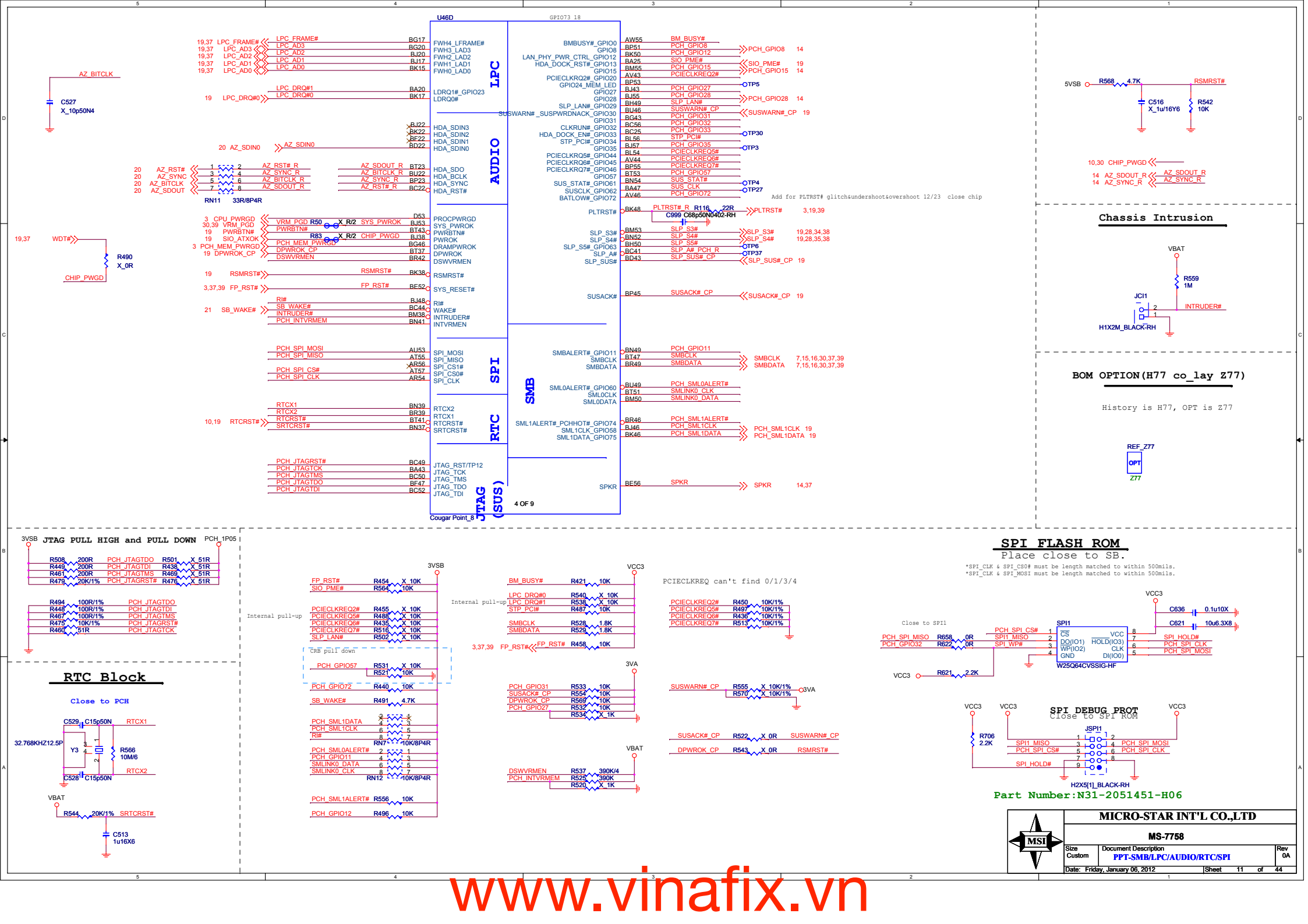

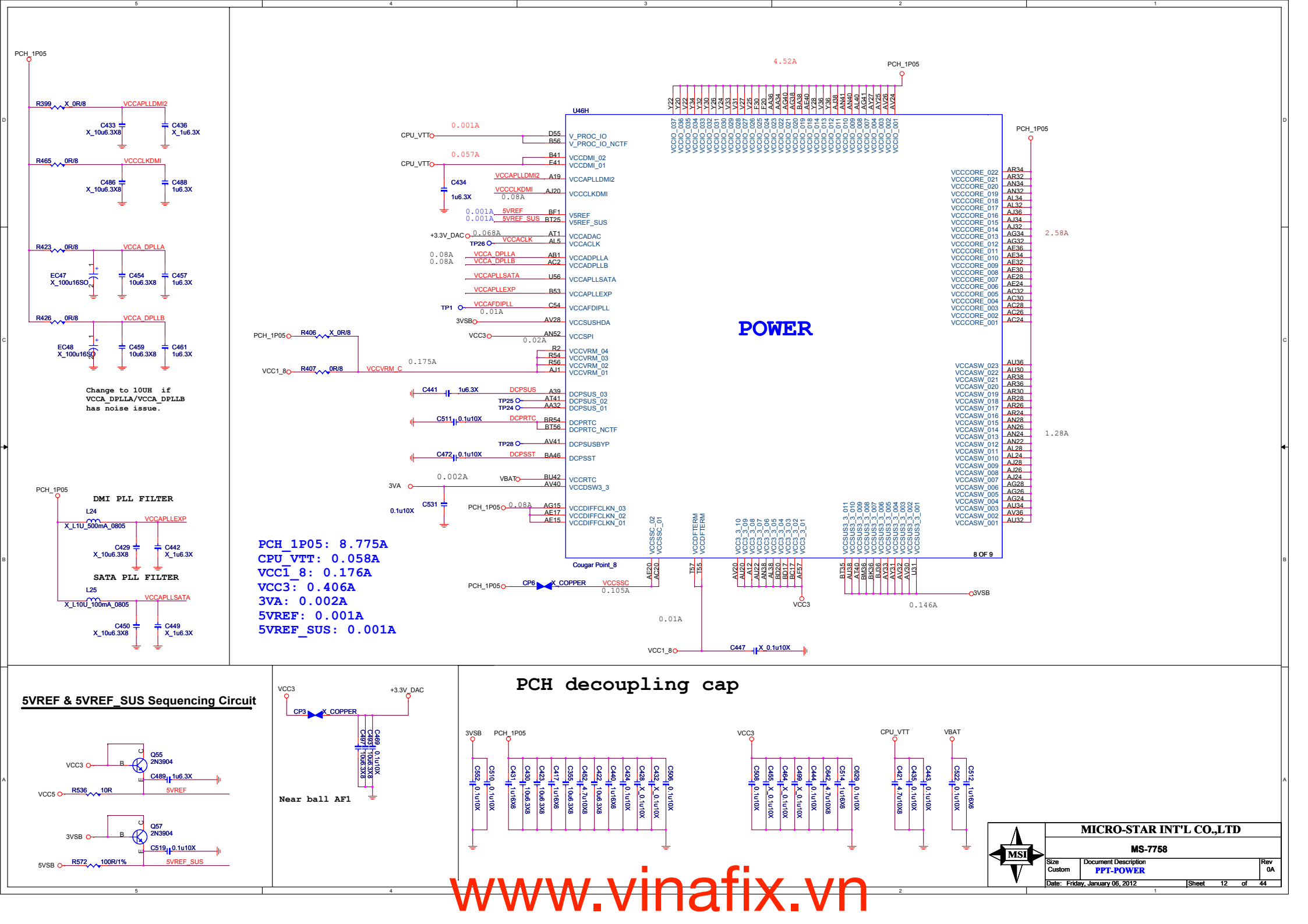

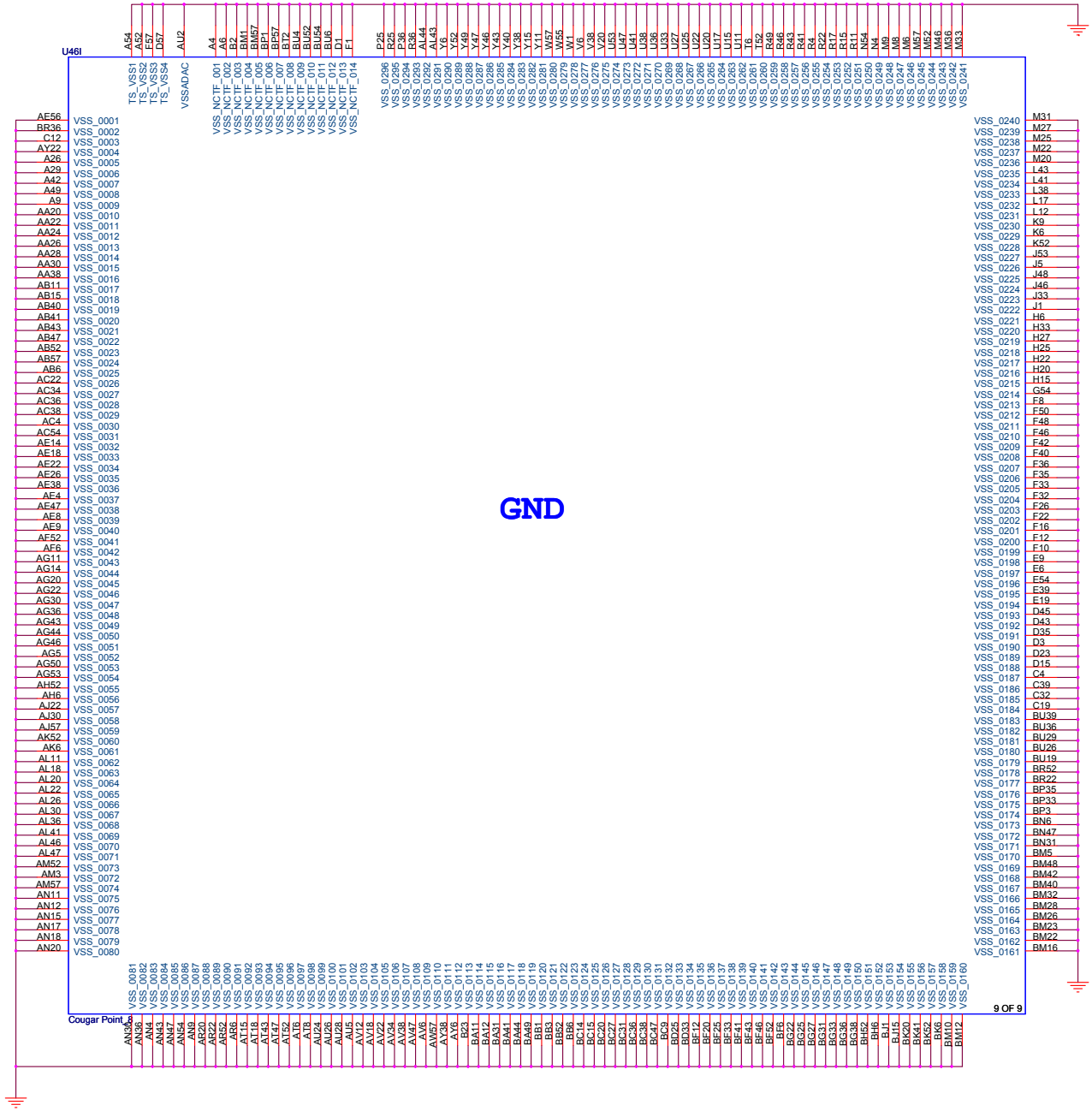

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PCH Straps

SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:

Do not pull low.

HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

Internal weak pull down. Do not pull up.

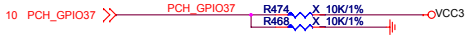
Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by
softstrap through ME.

Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up
resistor through a jumper.

Internal weak pull up. Do not pull low.
On die PLL voltage regulator

Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

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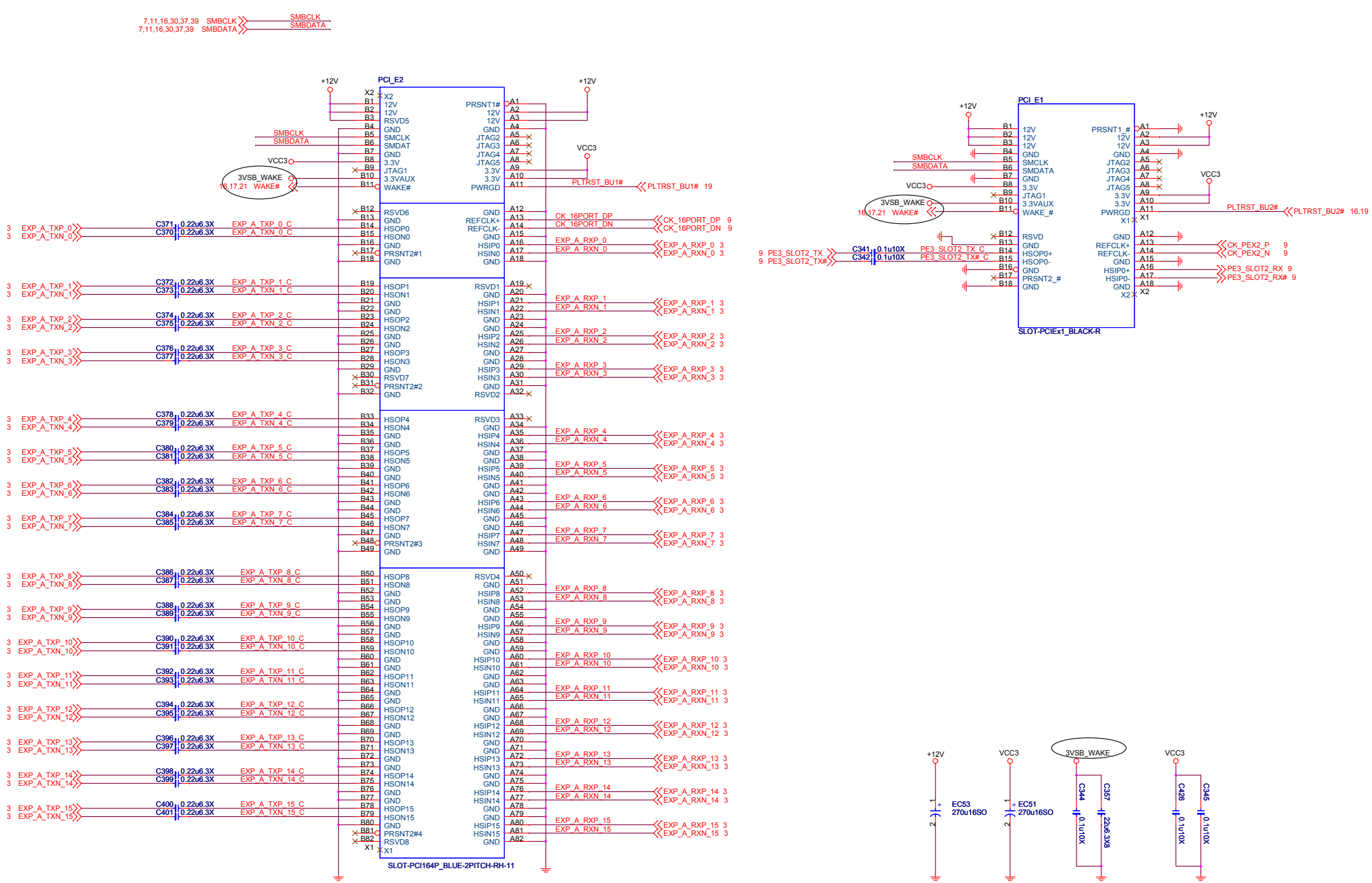
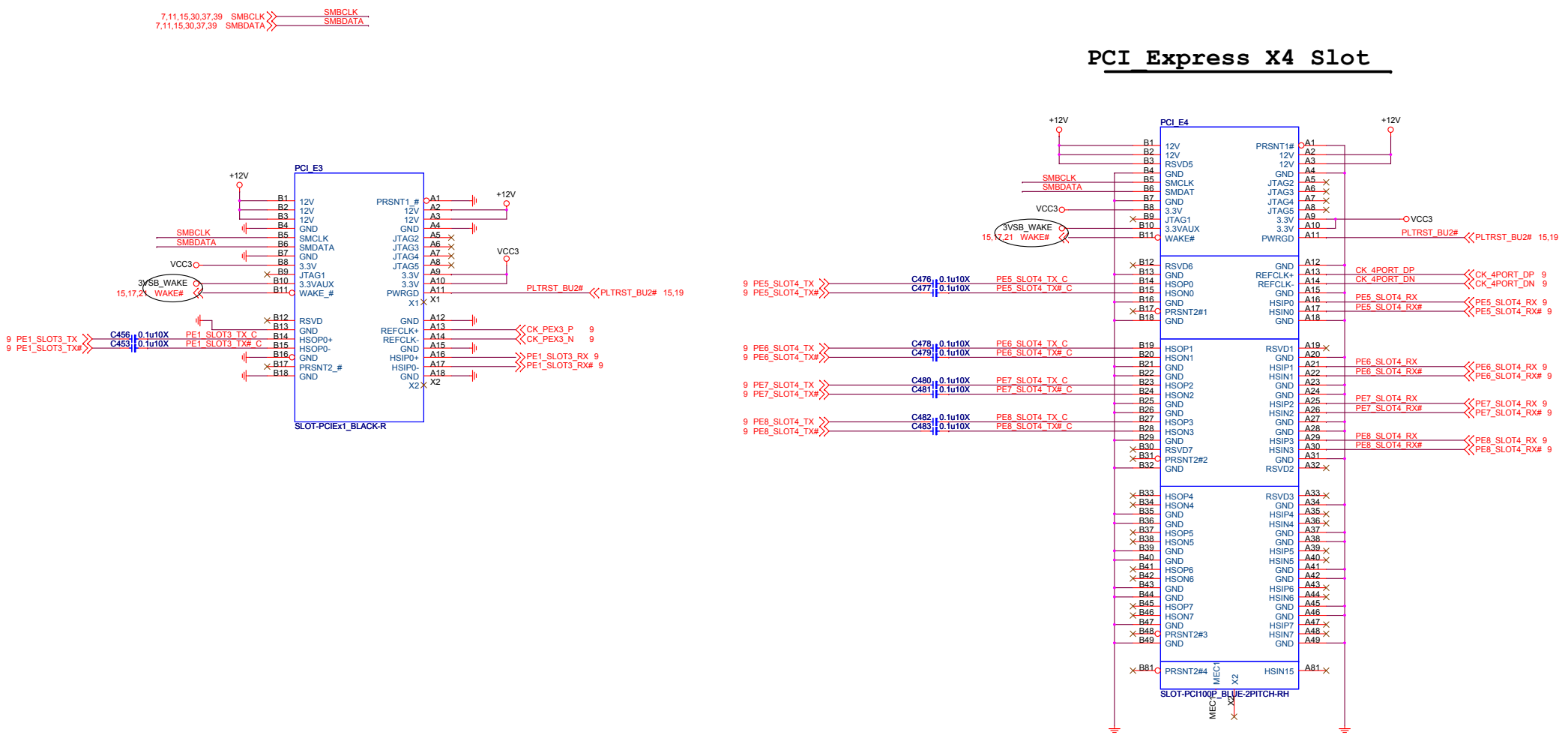
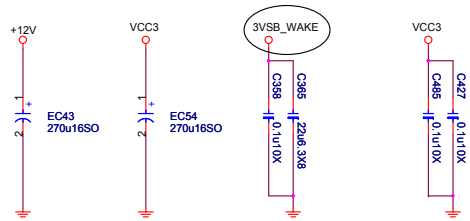


PCI Express X4 Slot





MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCIE3(X1) & PCIE4(X4.) Slots	Rev: 0A
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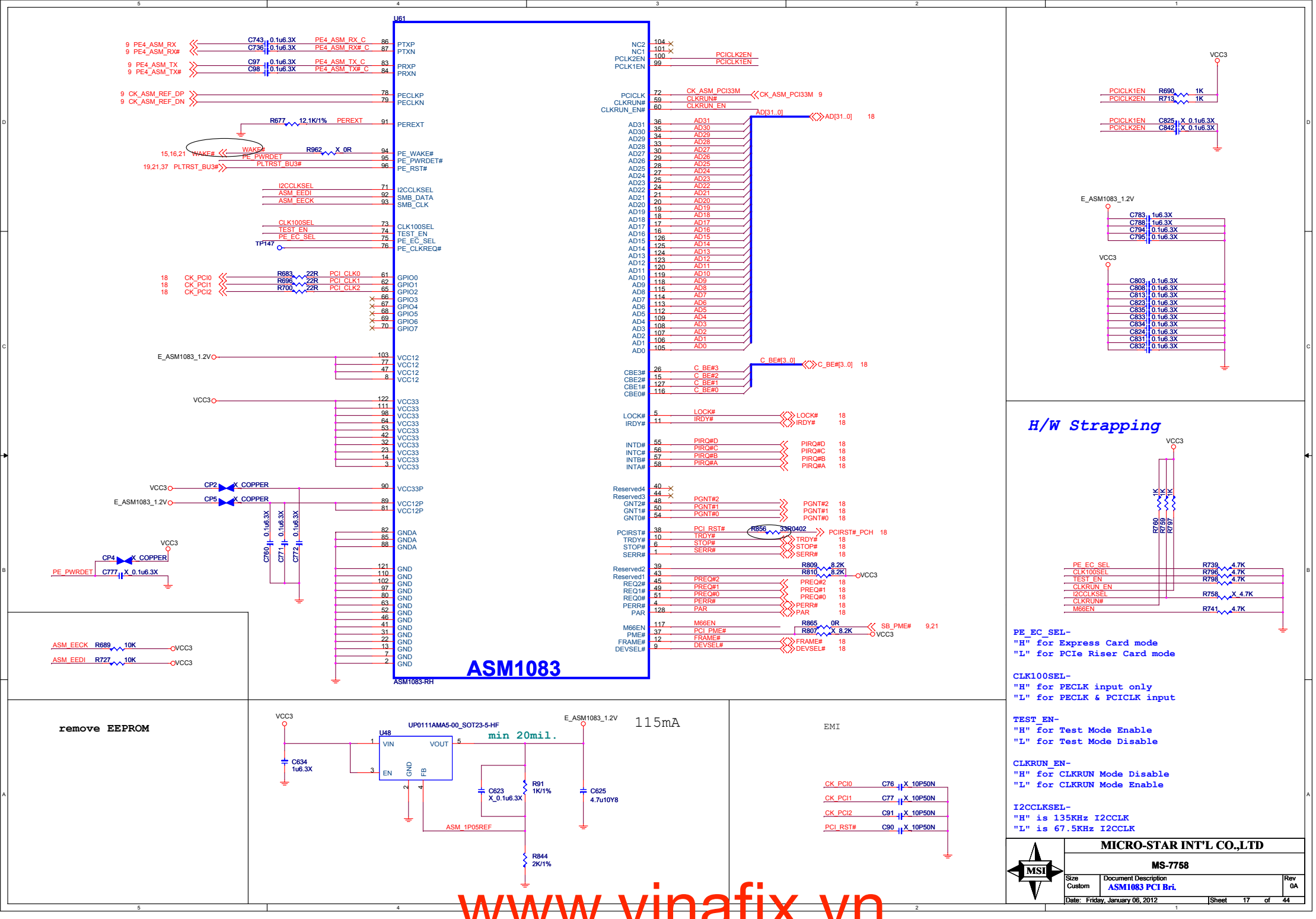

remove EEPROM

EMI

H/W Strapping

PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK

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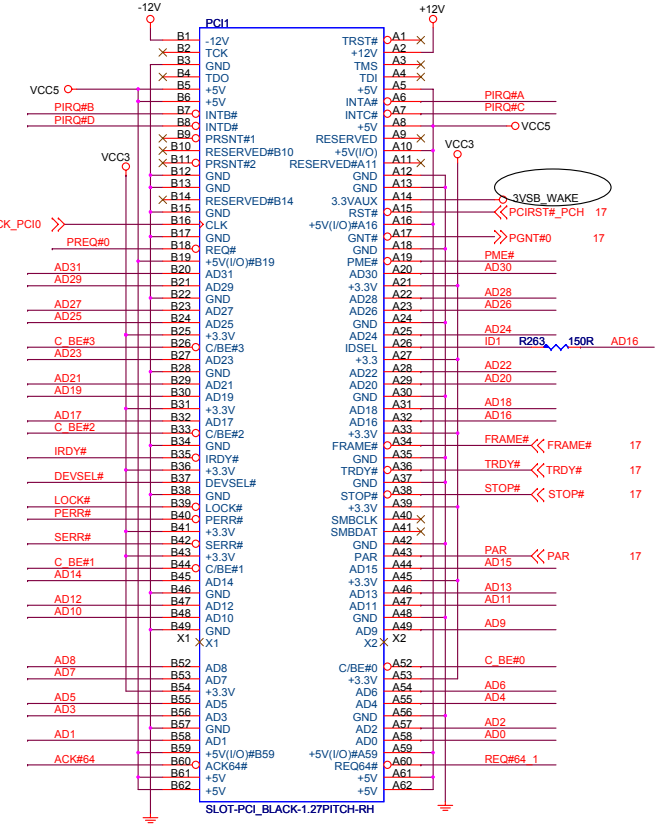
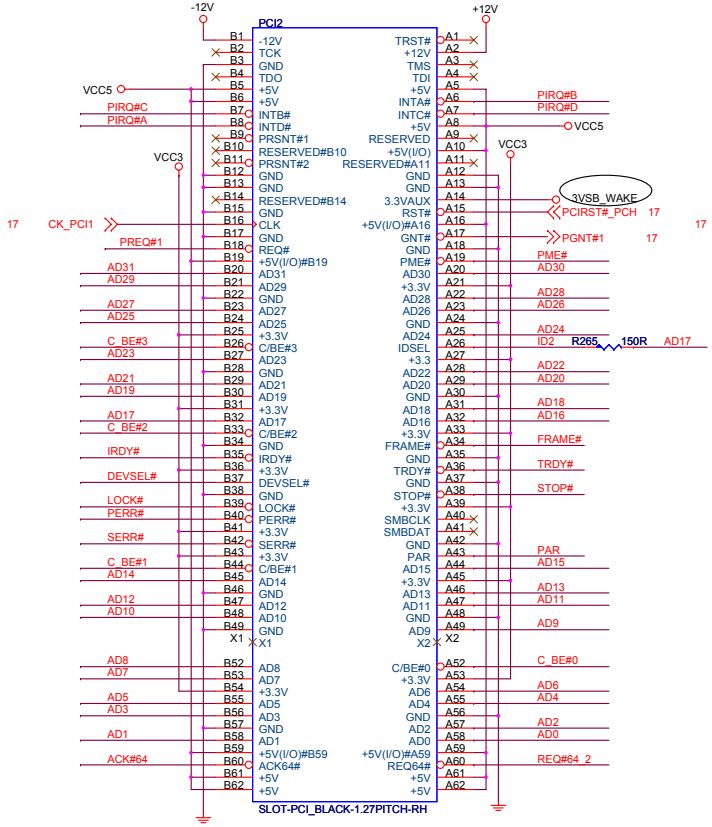
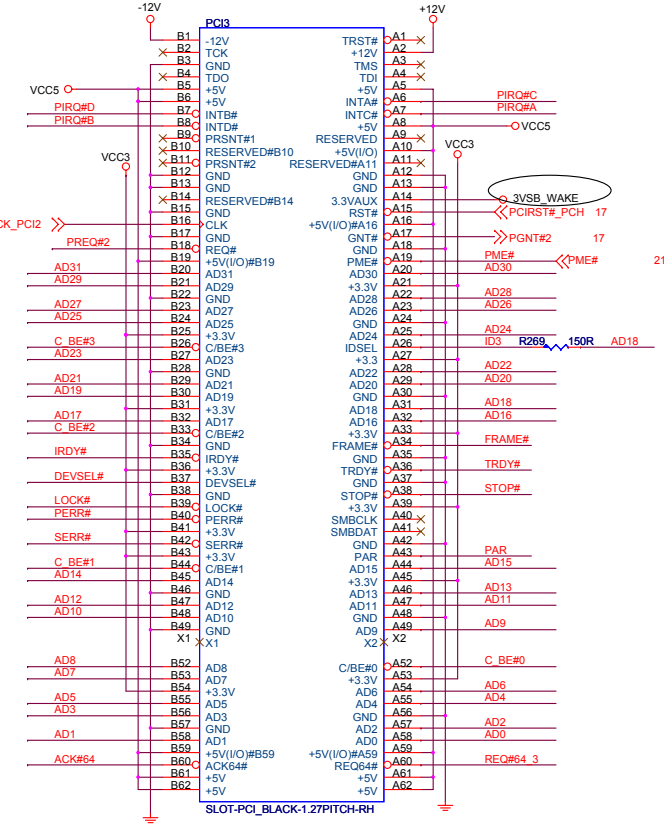


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



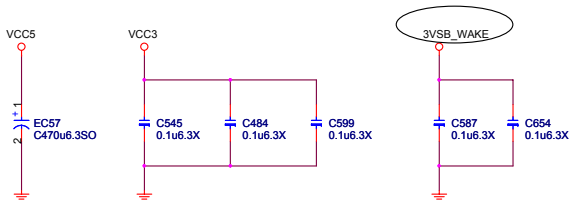
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B



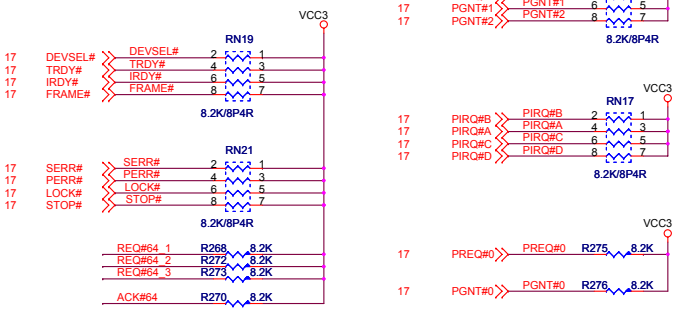
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

AD[31..0]

C_BE#[3..0]



PCI PULL-UP / DOWN RESISTORS



PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A

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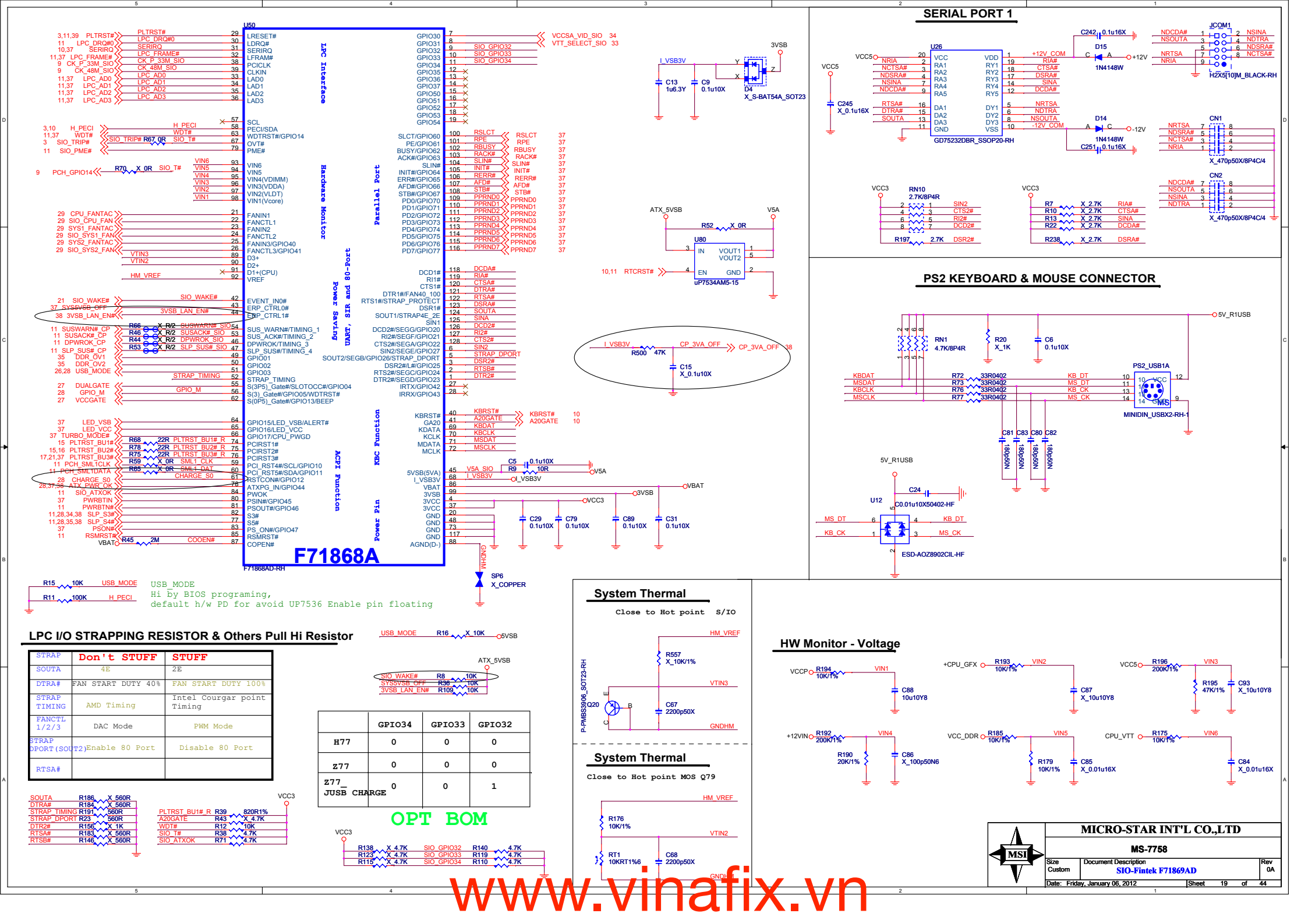
SERIAL PORT 1
PS2 KEYBOARD & MOUSE CONNECTOR
F71868A
F71868AD-RH
LPC Interface
Hardware Monitor
Parallel Port
Power Savings
UART, SIR and 80-Port
KBC Function
ACPI Function
Power Pin
LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor
STRAP | Don't STUFF | STUFF
SOUTA | 4E | 2E
DTRA# | FAN START DUTY 40% | FAN START DUTY 100%
STRAP TIMING | AMD Timing | Intel Cougar point Timing
FANCTL 1/2/3 | DAC Mode | PWM Mode
STRAP DPORT(SOUT2) | Enable 80 Port | Disable 80 Port
RTSA#
GPIO34 GPIO33 GPIO32
H77 0 0 0
Z77 0 0 0
Z77_ JUSB CHARGE 0 0 1
OPT BOM
USB_MODE
Hi by BIOS programing,
default h/w PD for avoid UP7536 Enable pin floating
System Thermal
Close to Hot point S/IO
System Thermal
Close to Hot point MOS Q79
HW Monitor - Voltage
MICRO-STAR INT'L CO.,LTD
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SIO-Fintek F71869AD
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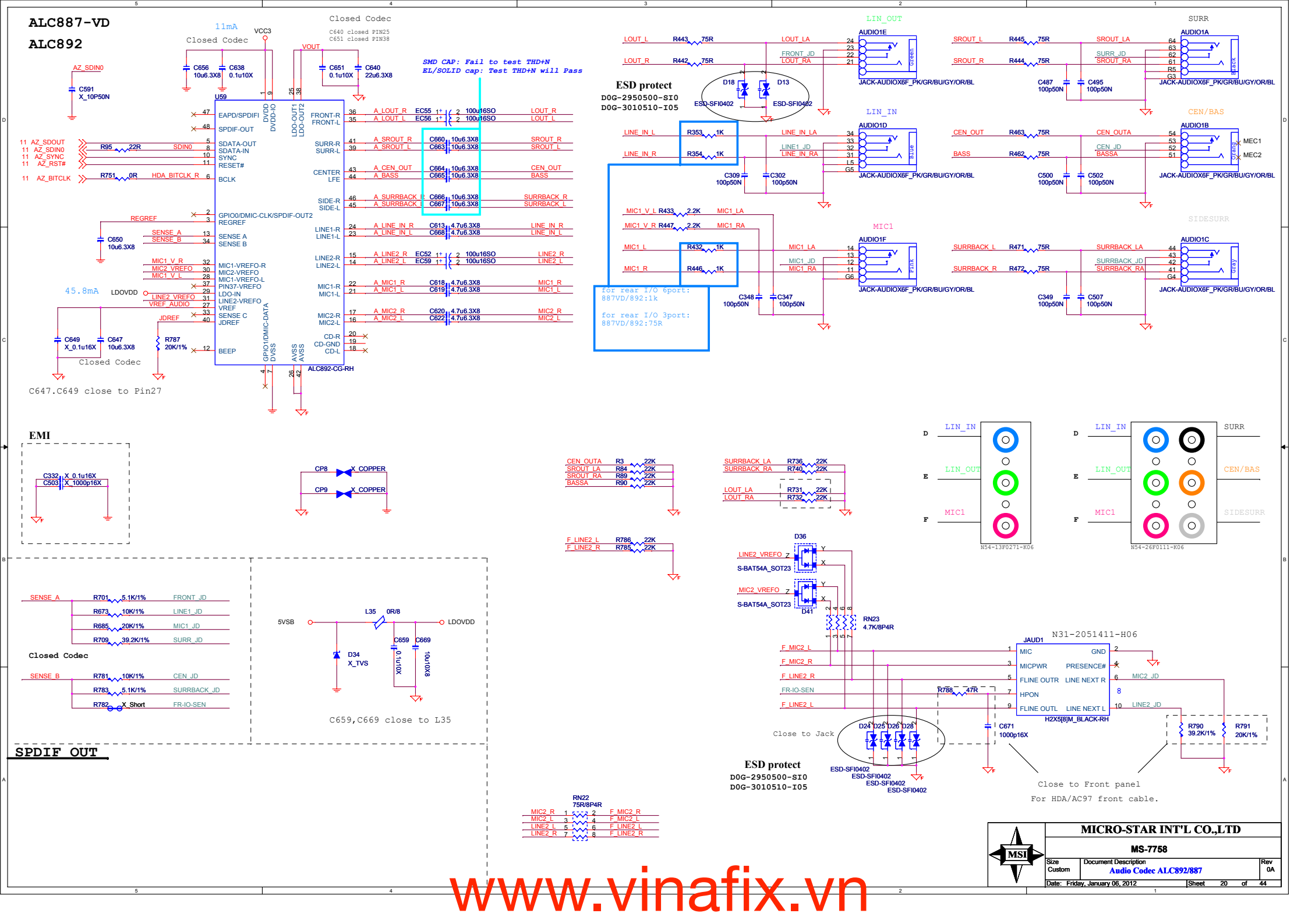
www.vinafix.vn

ALC887-VD
ALC892



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Size: Custom	Document Description: Audio Codec ALC892/887
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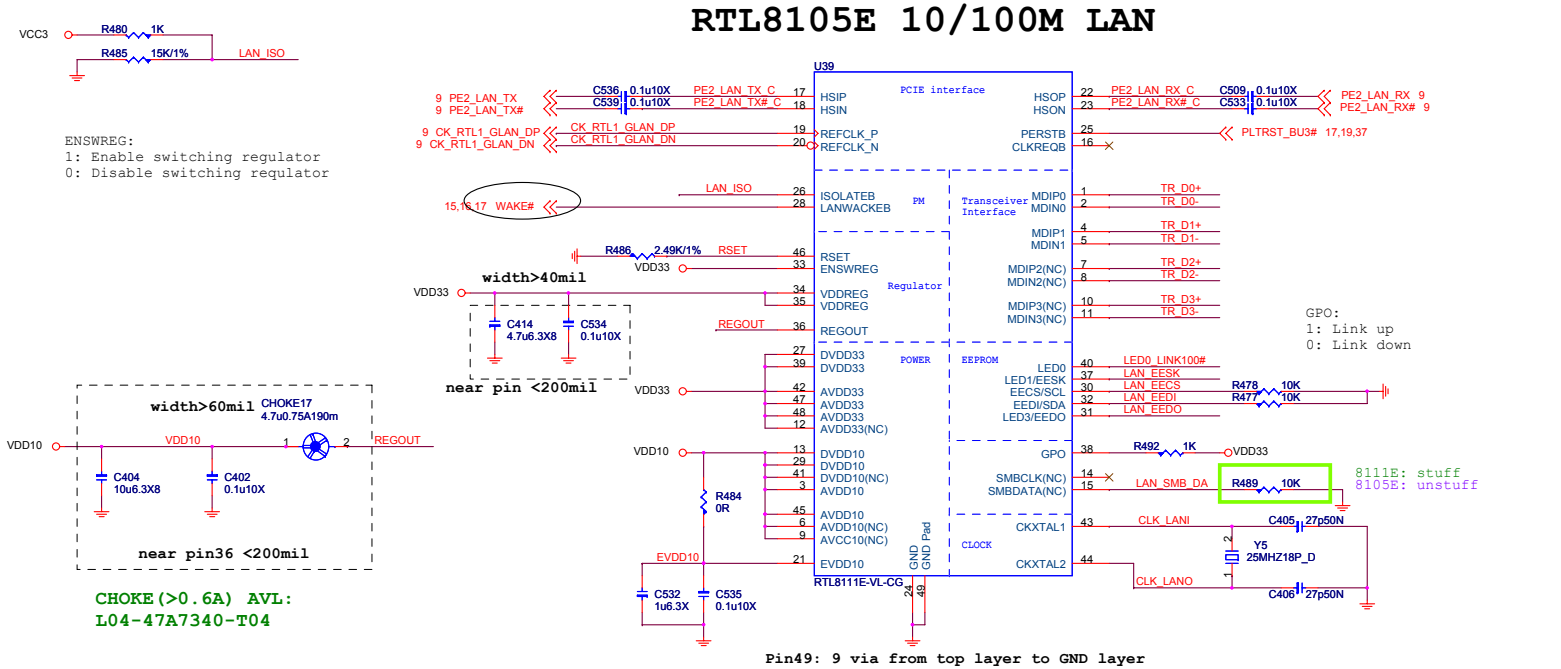
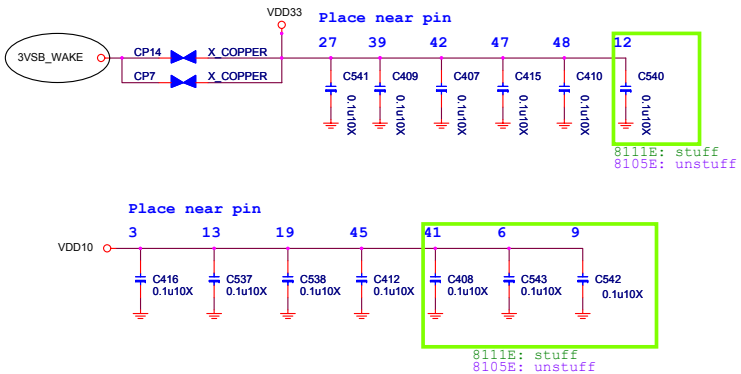
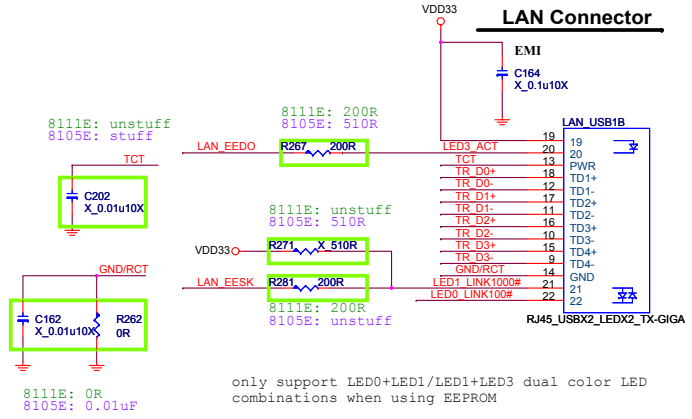
RTL8111E Giga LAN

RTL8105E 10/100M LAN

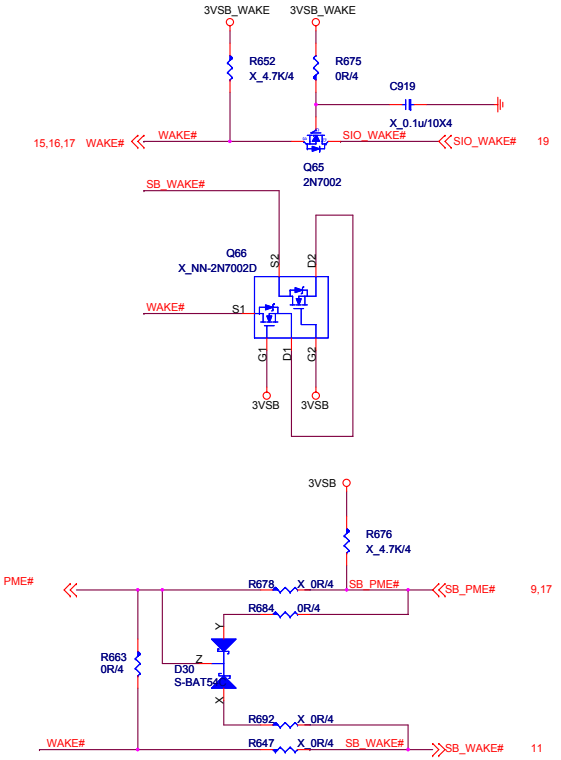


3.3v Power on rise time : 1~100ms. MAX: 163mA





LAN/PCIE/PCI Wake Up CTRL Circuit



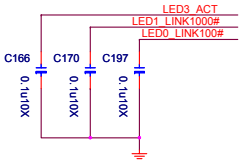
Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Active 1000 100 10 / Yellow Blinking Orange Green None	Link Active 100 10 / Yellow Blinking Green None
19 20 250R Yellow	19 20 Yellow
21 22 250R Orange Green	21 22 Green

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11



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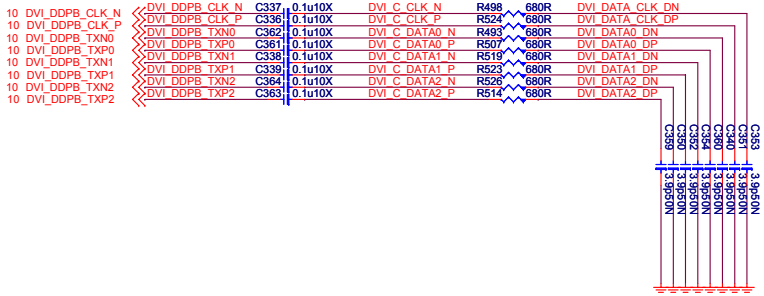
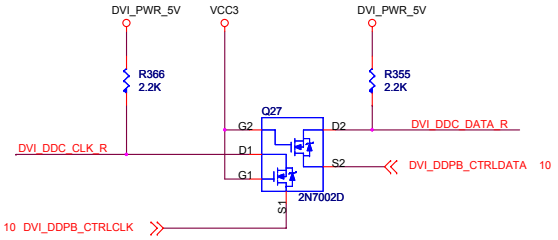
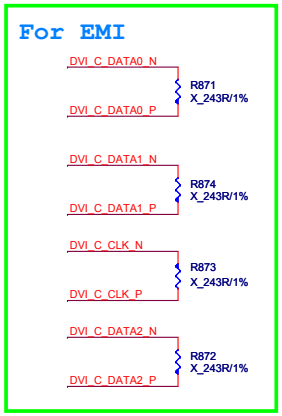
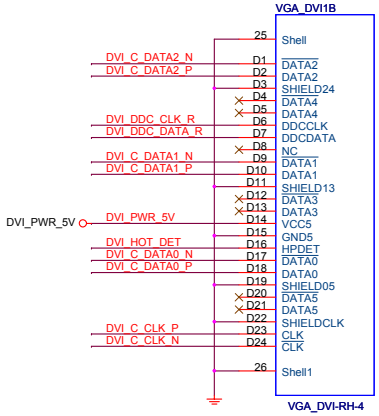
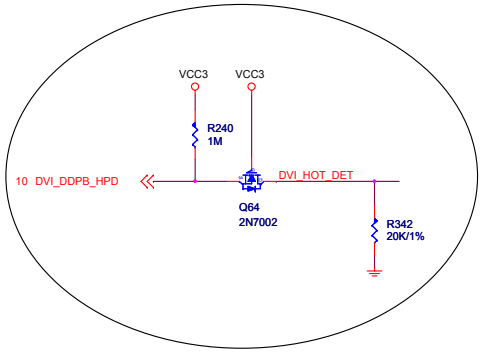
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

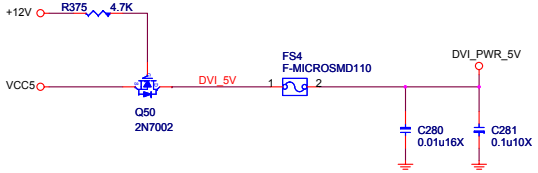


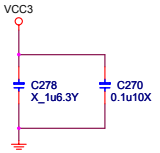


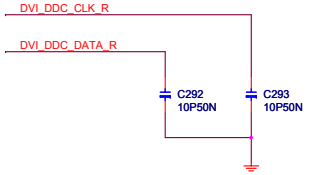












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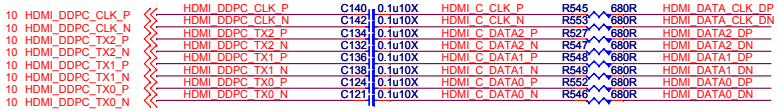
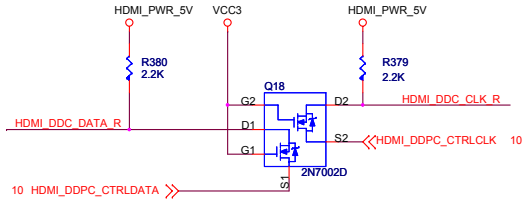
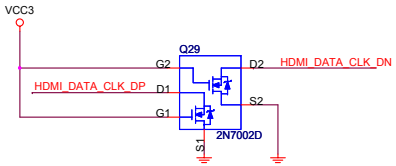
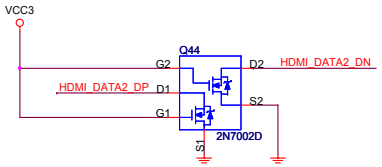
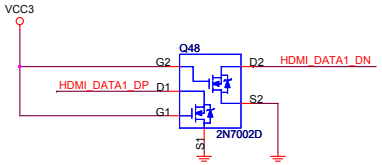
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

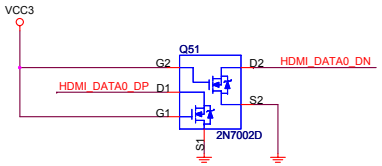


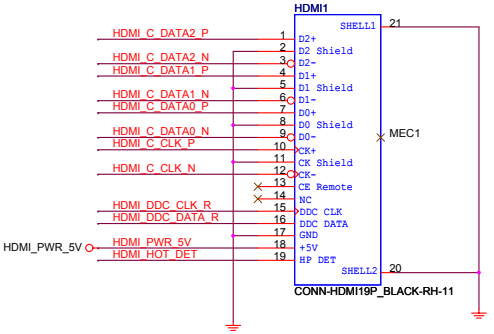


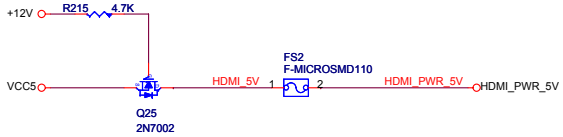


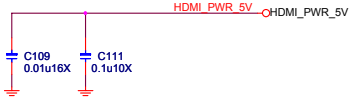


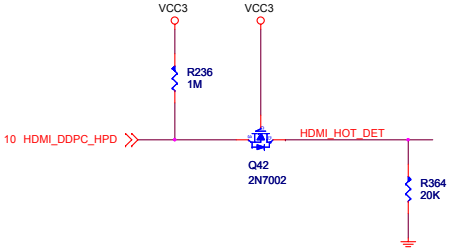


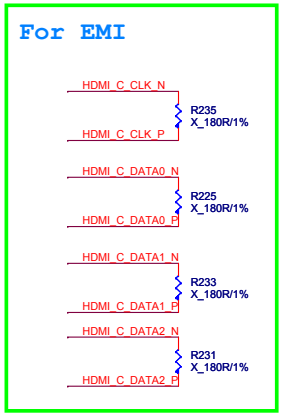


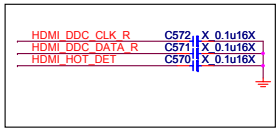












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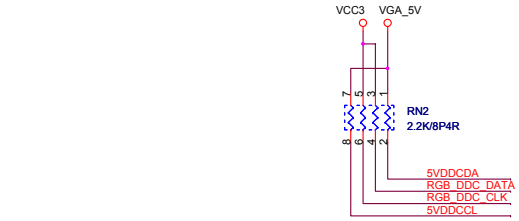
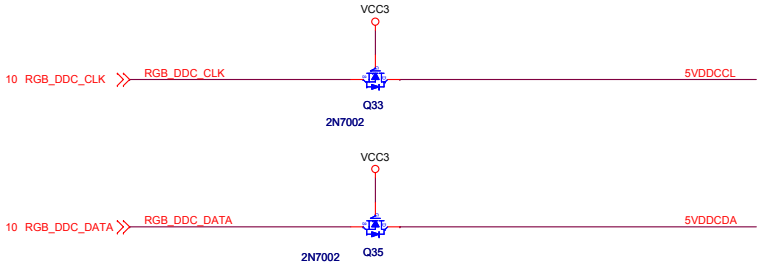
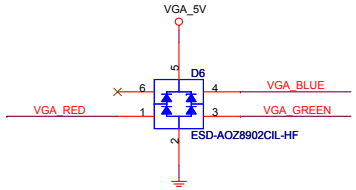
D-Sub

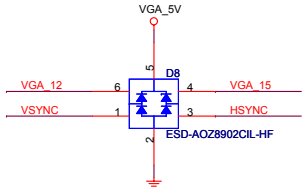
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

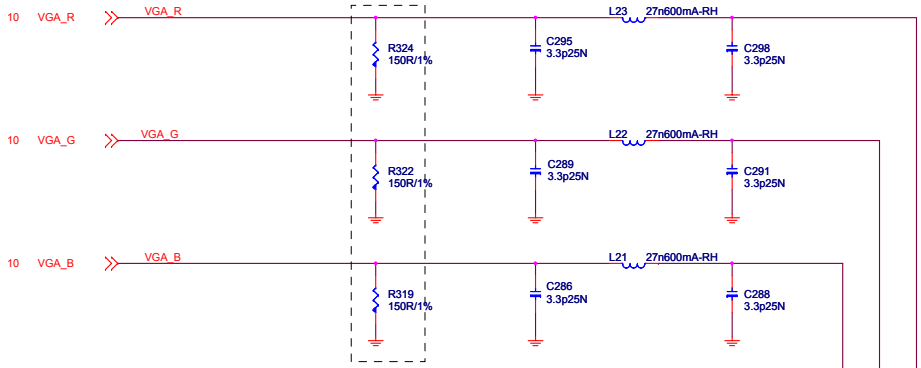
Level shift



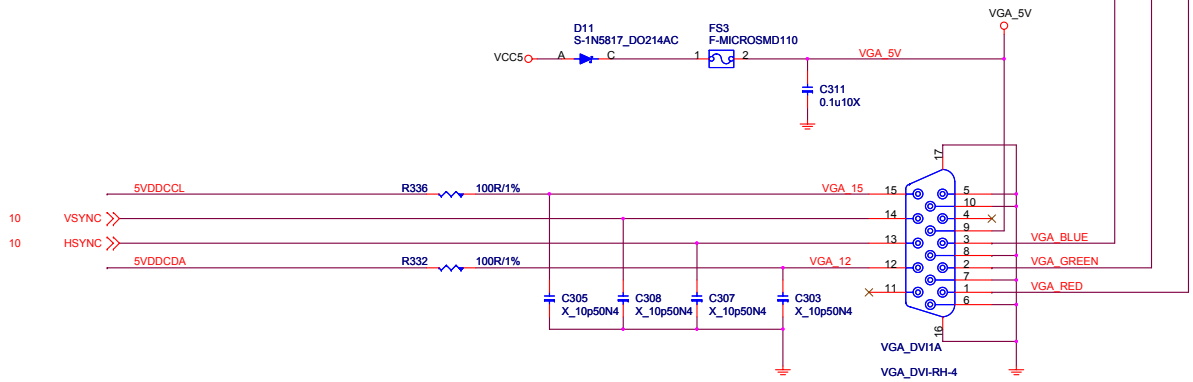








PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



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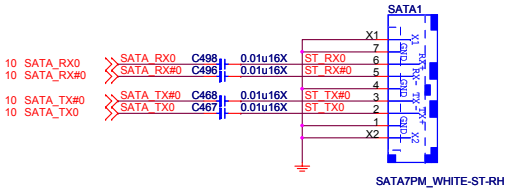
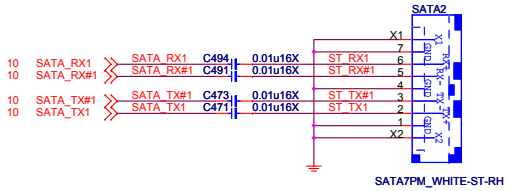
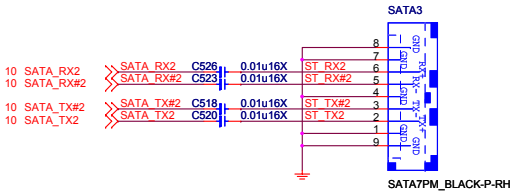
SATA 6G PORT 0,1

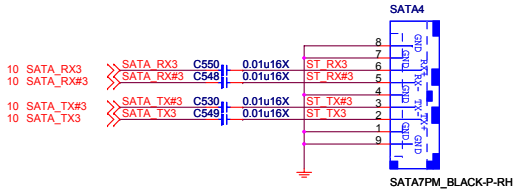
3.0 white



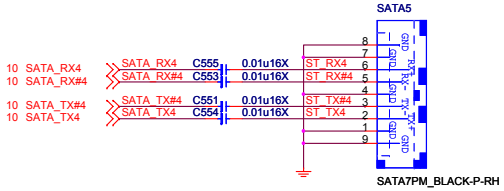


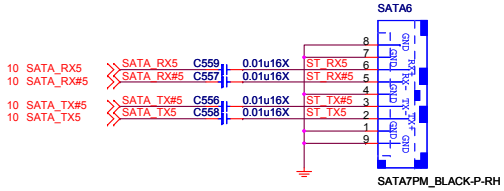
SATA 3G PORT 2,3





SATA 3G PORT 4,5





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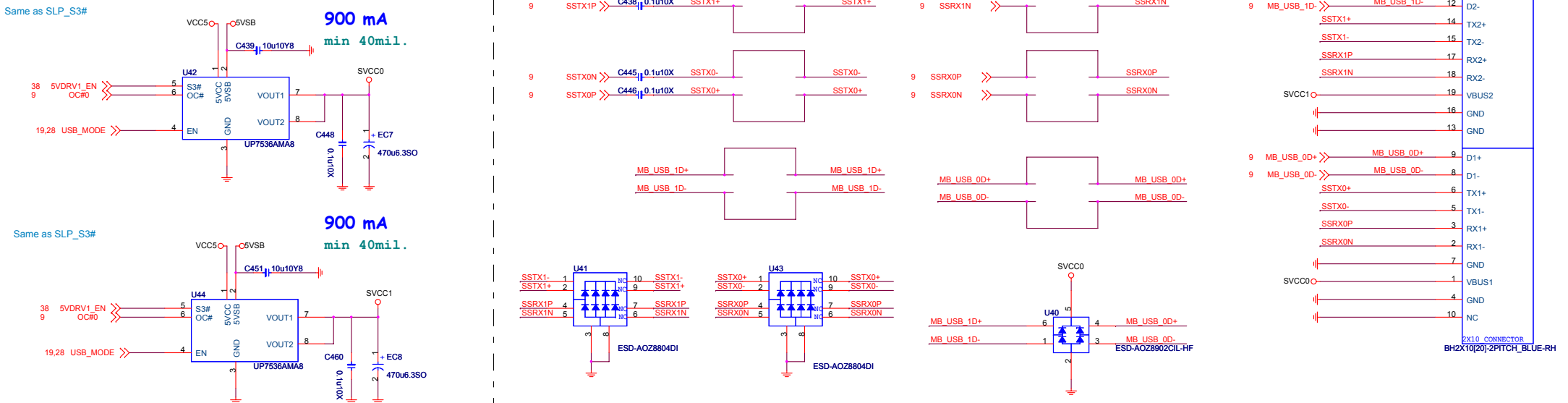
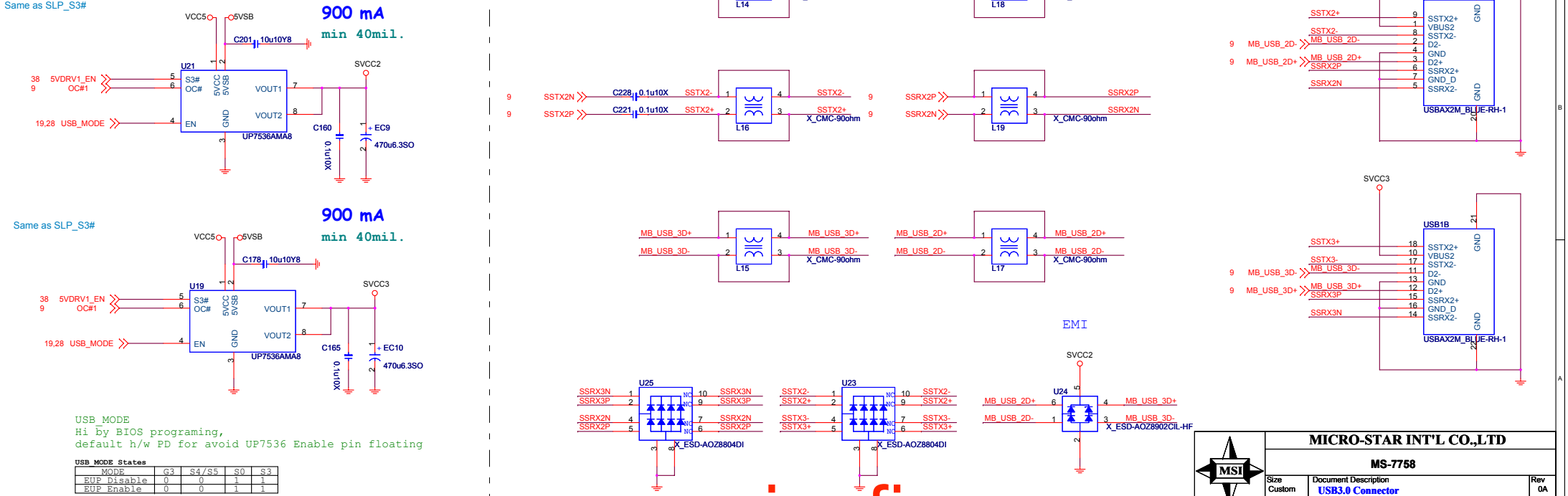
FRONT USB30 PORT 0,1



REAR USB30 PORT 2,3



USB_MODE
Hi by BIOS programing,
default h/w PD for avoid UP7536 Enable pin floating

USB_MODE States

MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1

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Size: Custom | Document Description: USB3.0 Connector | Rev: 0A

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USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

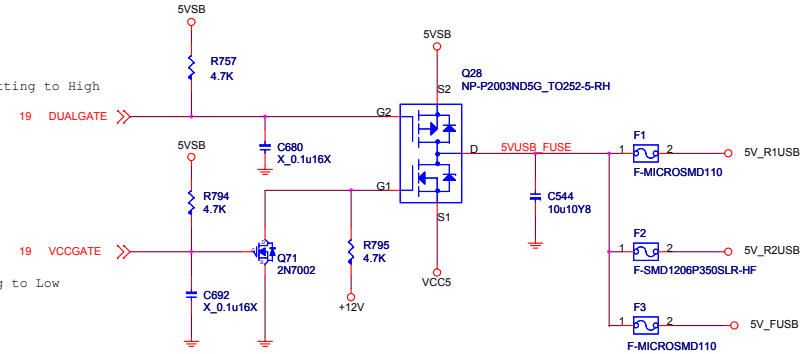
When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

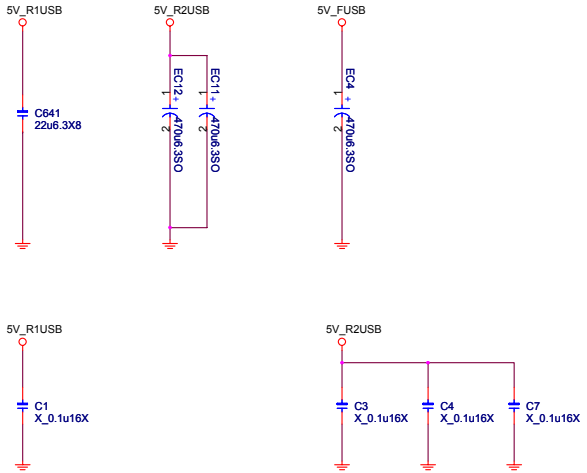
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

When PS2 in S5 support wake , S3P5_Gate# in S5 must setting to Low

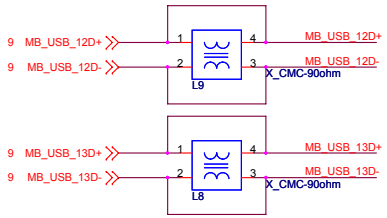
*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

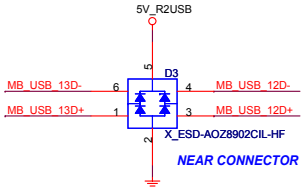
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue

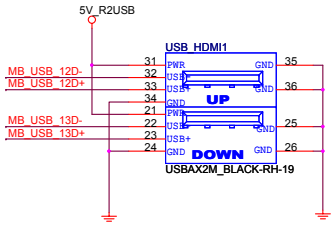




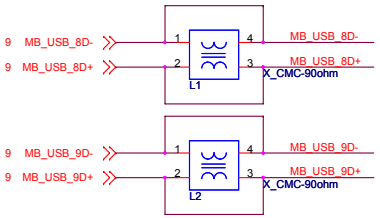
REAR USB PORT 12,13 (With LAN)

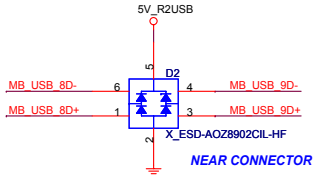


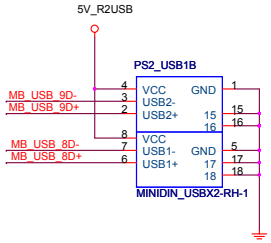




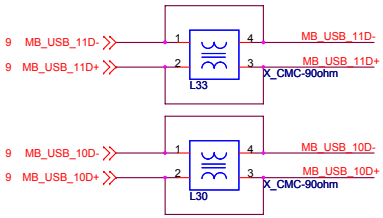
REAR USB PORT 8,9 (With HDMI)

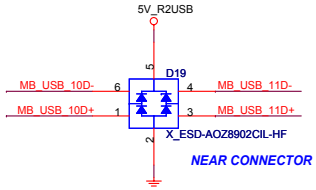


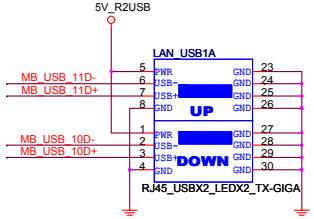




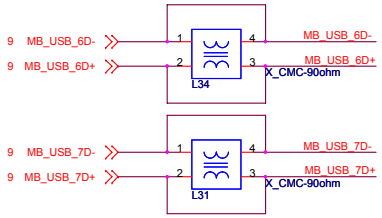
FRONT USB PORT 10,11(With PS2)

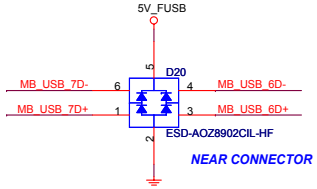


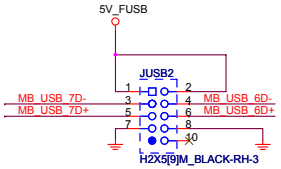




FRONT USB PORT 6.7







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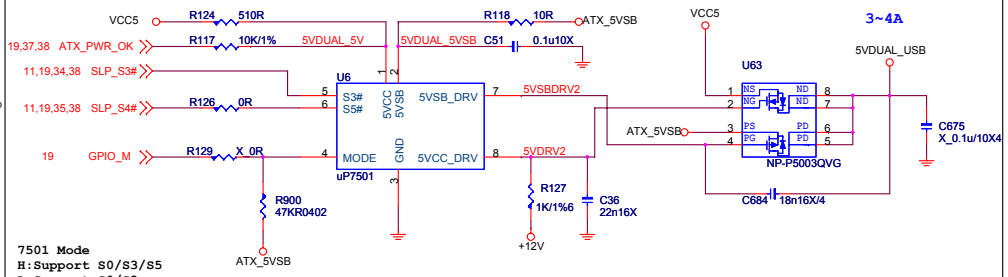
5VDUAL_USB



SIO GPIO40 Pin7 (I_VSB3V)

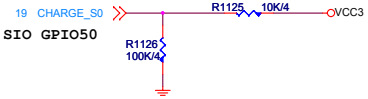
USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

Power plug in , H/W default support USB charge.

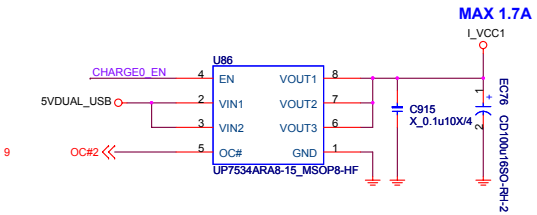
Pin power I_3VSB or VBAT
Register power I_3VSB or VBAT
Register reset I_3VSB or VBAT

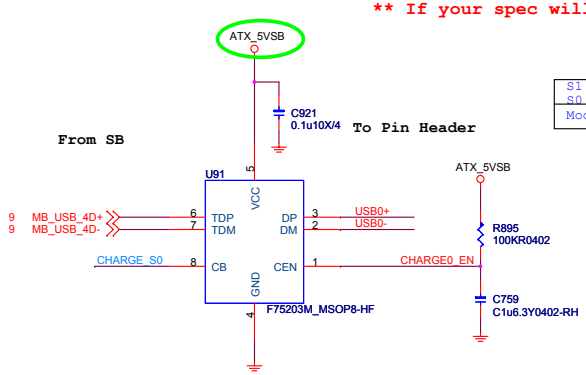
Pin power I_3VSB
Register power I_3VSB
Register reset I_3VSB

Update~2010.9.15



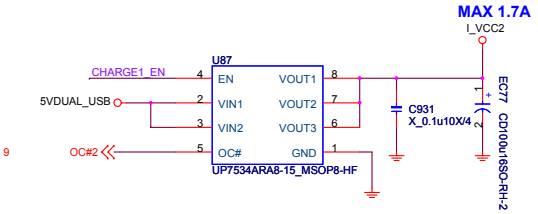
USB POWER PORT 0 For USB Charging

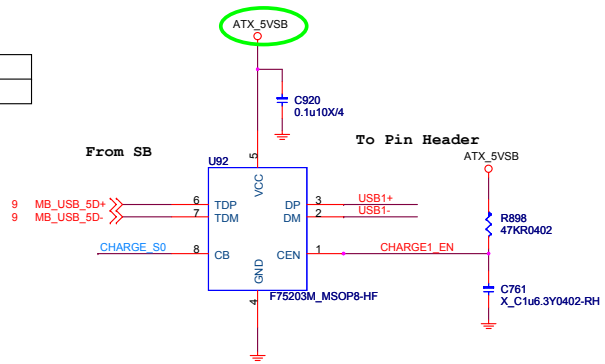




S1	0		0	1
S0	0		1	1
Mode	AUTO		A	Y

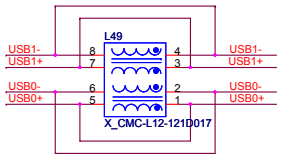
USB POWER PORT 1 For USB Charging

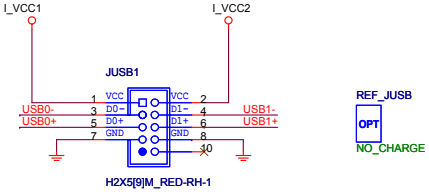




** If your spec will not need bom option, please don't co-lay blue labels.

FRONT USB PORT 0,1



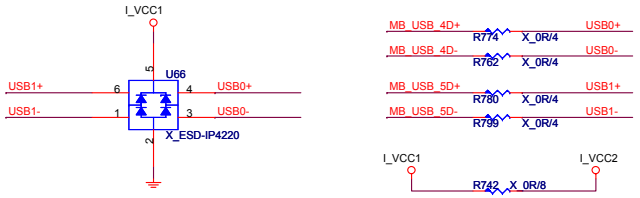


Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

PI5USB14550 has internal EDS diode.

A type
2.70V< D+ <3.1 V
1.85V< D- < 2.1V
For i-Pad / i-Phone 4G charges current up to 1.6A.

COLAY remove USB charger ic



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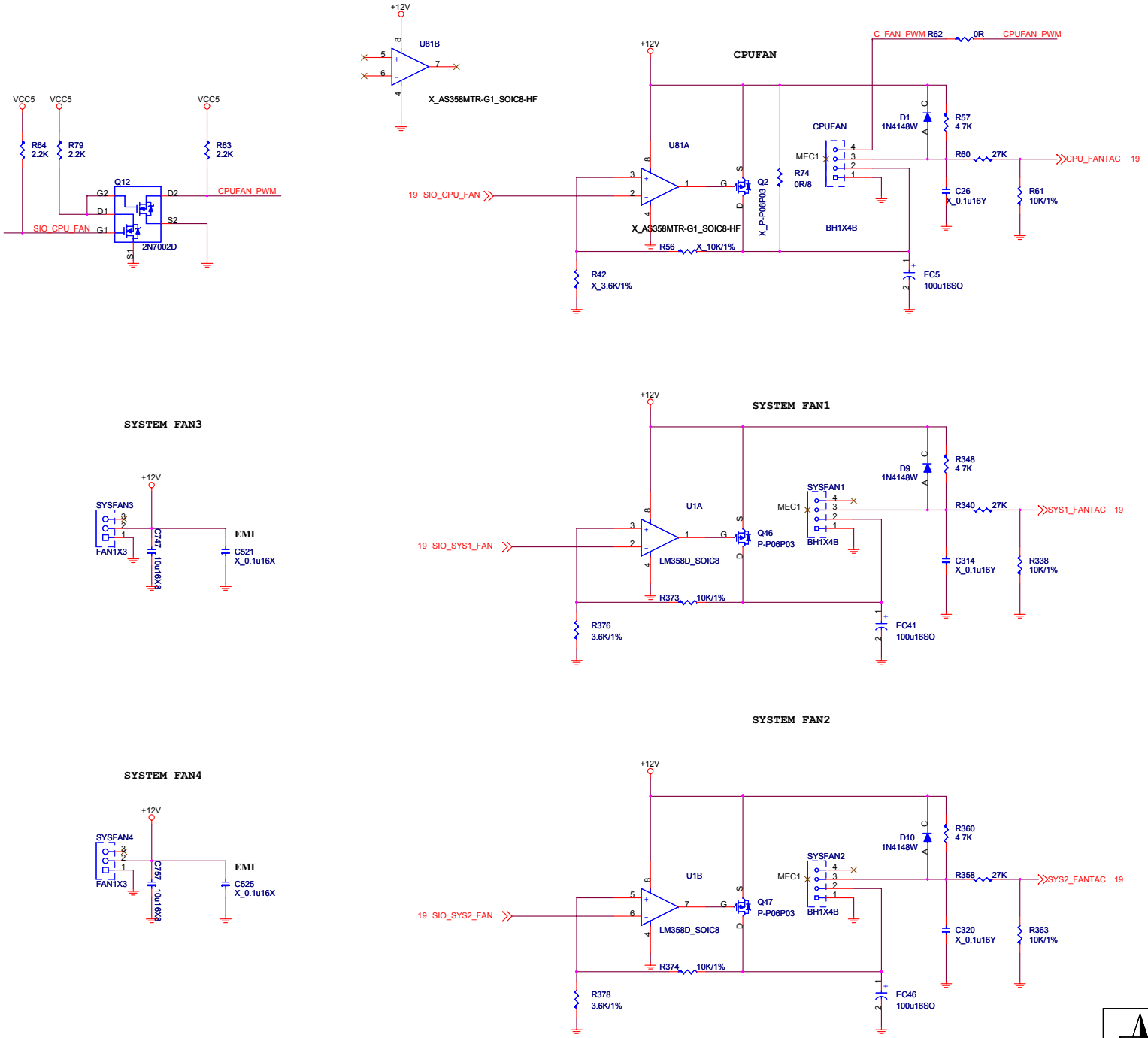
FAN-COUNTROL CIRCUIT



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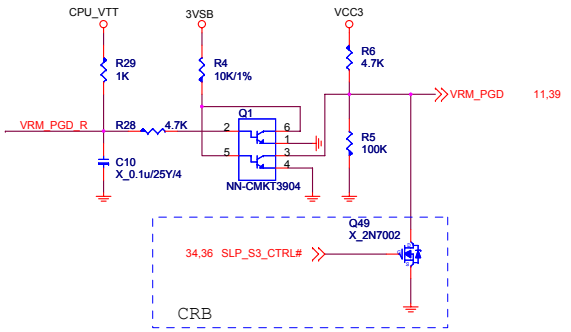
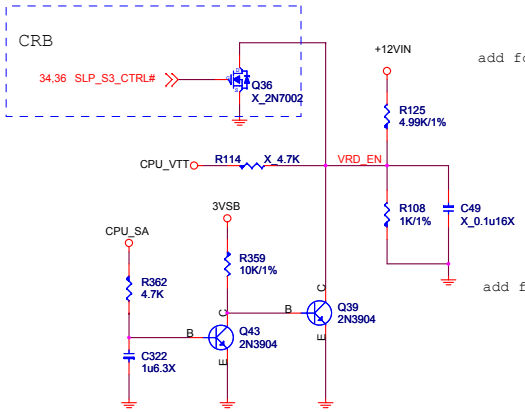
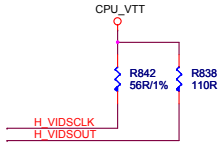
VRMPWRGD LEVEL SHIFT



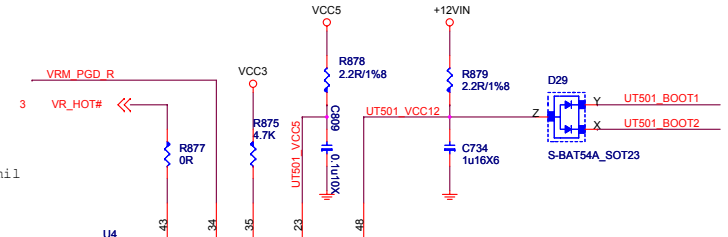


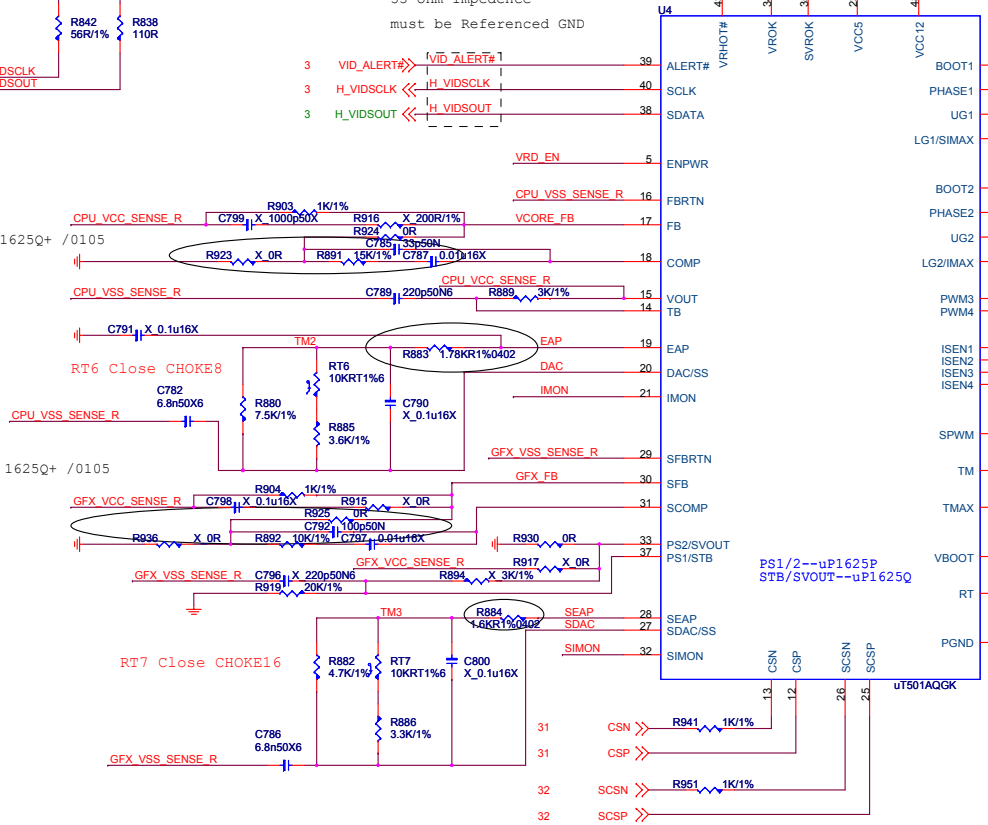
add for co_lay 1625Q+ /0105

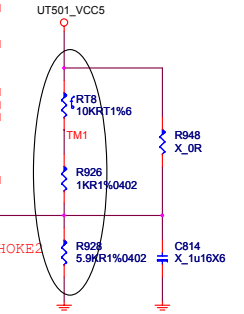
add for co_lay 1625Q+ /0105

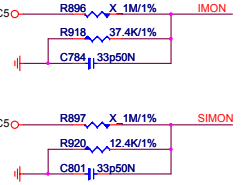


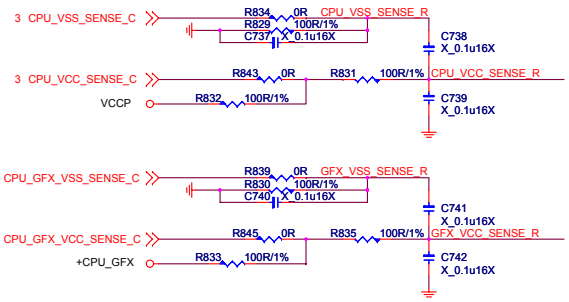
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND







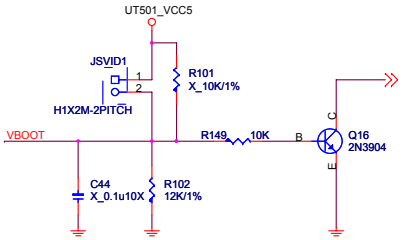


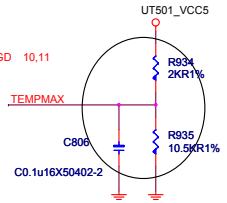


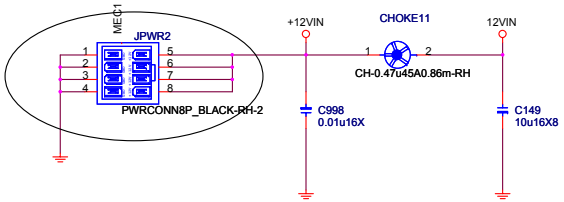
UPI VOLTAGE CONSOLE

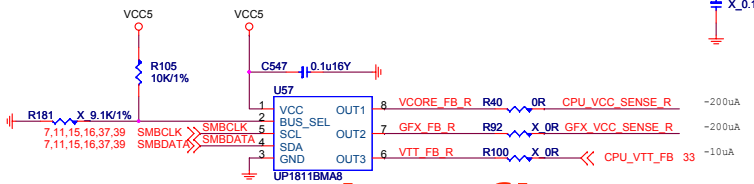
0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%









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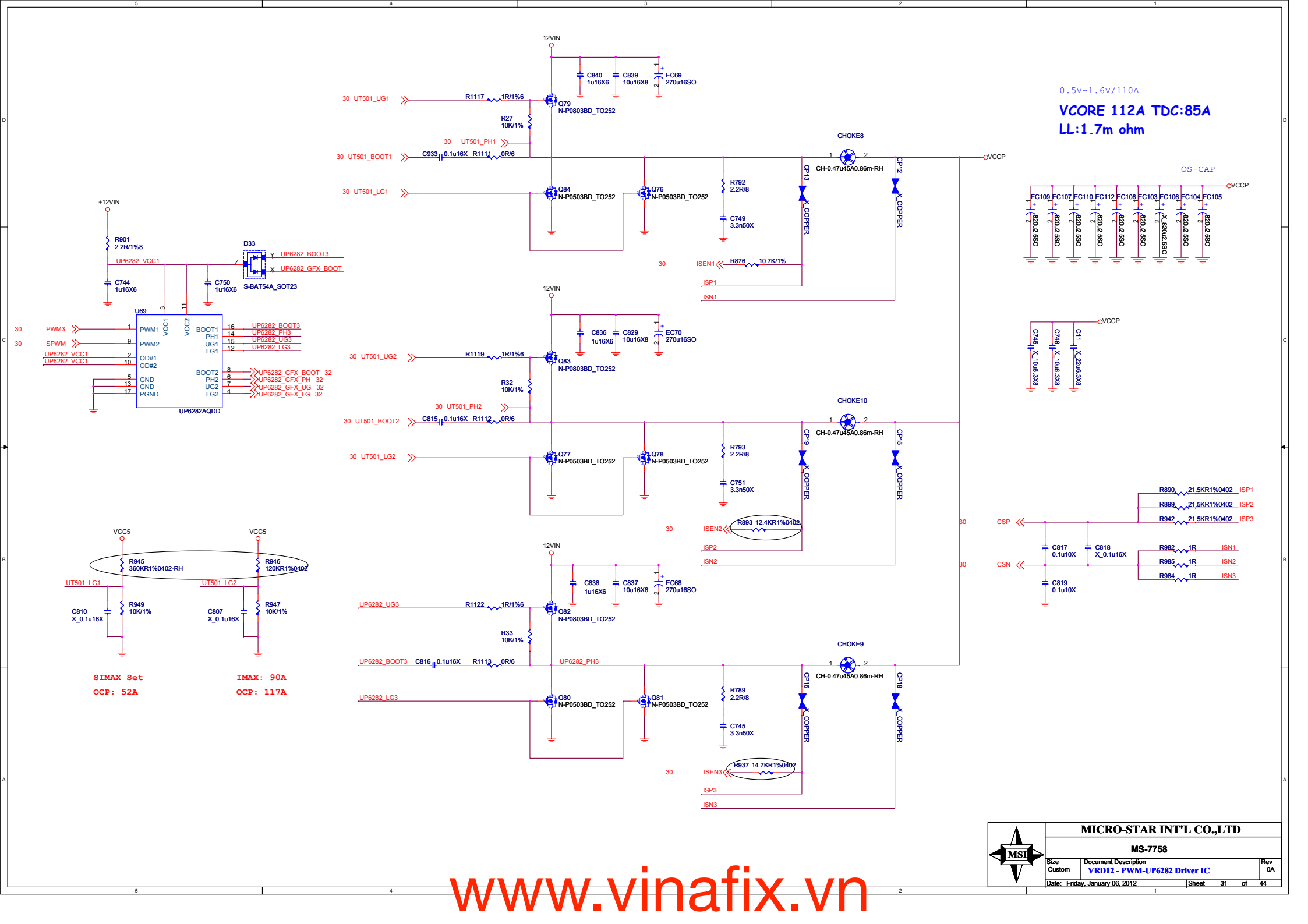
0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm
OS-CAP
12VIN
VCCP
CHOKE8
CHOKE10
CHOKE9
CH-0.47u45A0.86m-RH
UP6282AQDD
S-BAT54A_SOT23
SIMAX Set
OCP: 52A
IMAX: 90A
OCP: 117A
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VRD12 - PWM-UP6282 Driver IC
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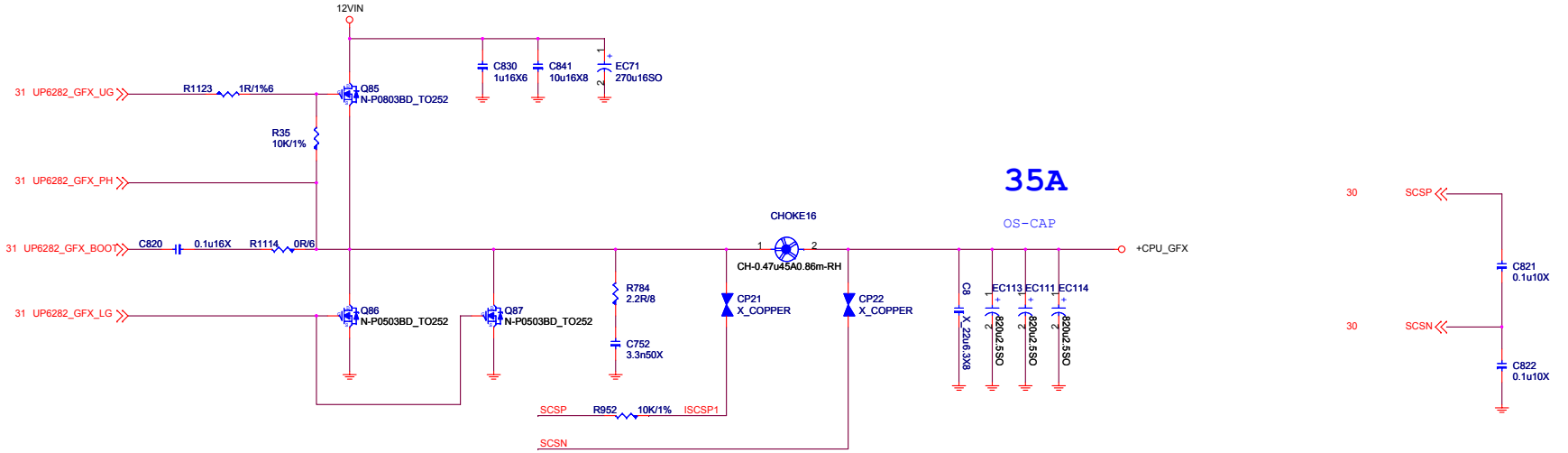
www.vinafix.vn

CPU_GFX:0.25-1.52

35A FOR CPU



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Size: Custom	Document Description: VRD12 -GPU 1-Phase MOS	Rev: 0A
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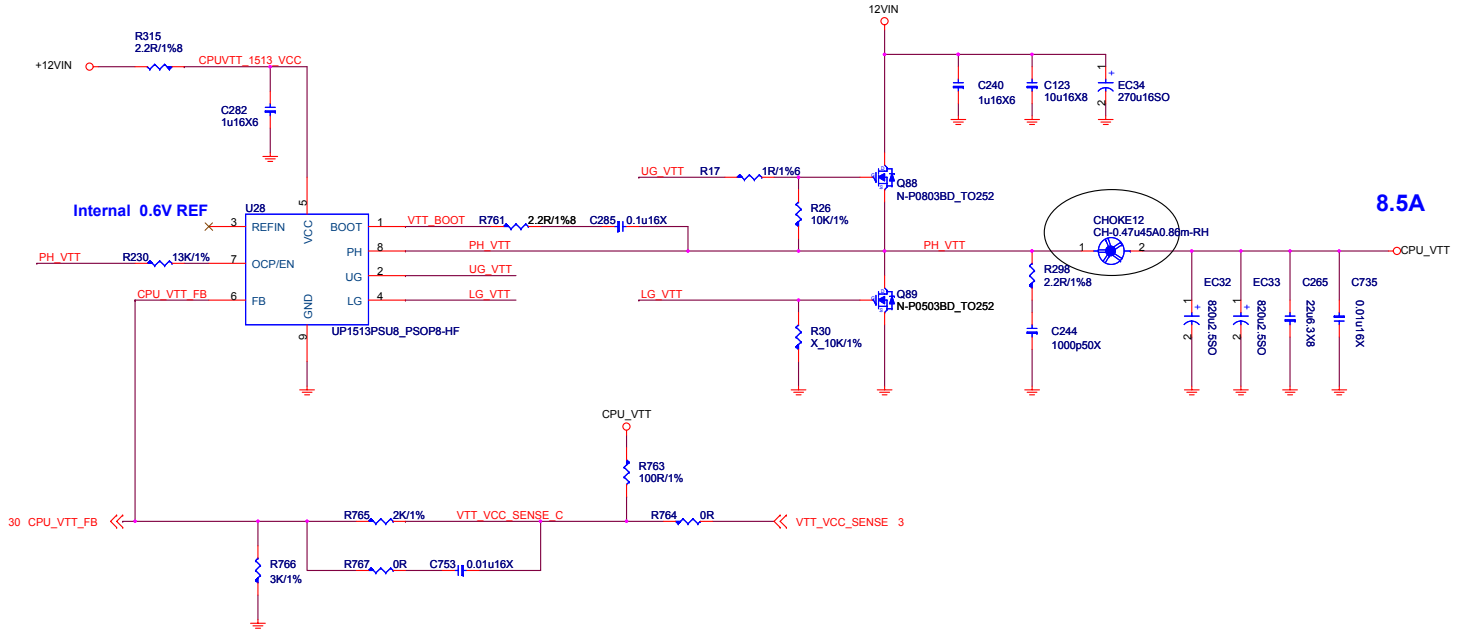
CPU_VTT:1.05/1.00 *MAX 17.3A*

CPU VTT 8.5A SA Core =8.8A

8.5A FOR CPU

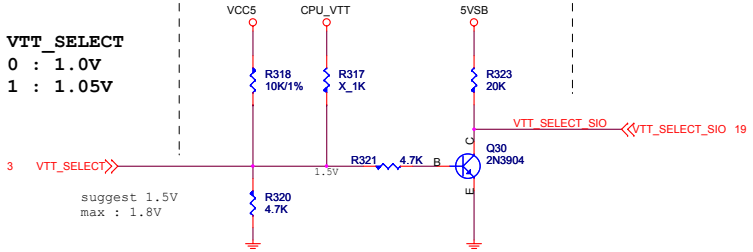
Iripple=1.92(vtt)+1.88(sa)
5*1=5A>3.8A

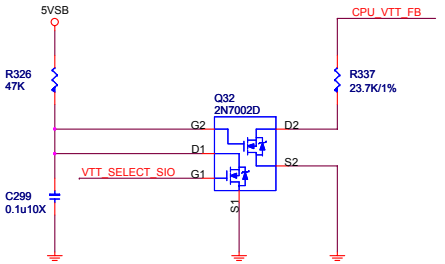


VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

VTT_SELECT
0 : 1.0V
1 : 1.05V





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Custom	VTT POWER- uP1513- 1Phase MOS	0A

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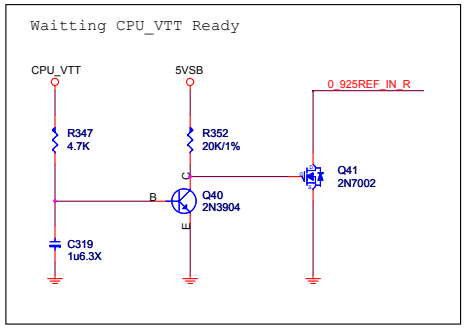
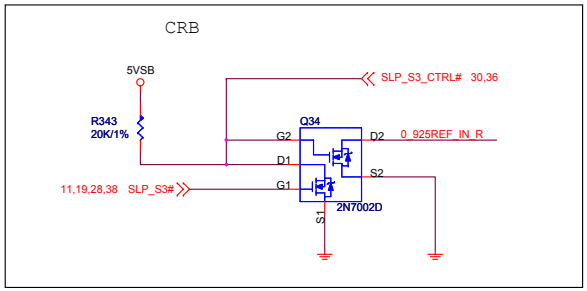
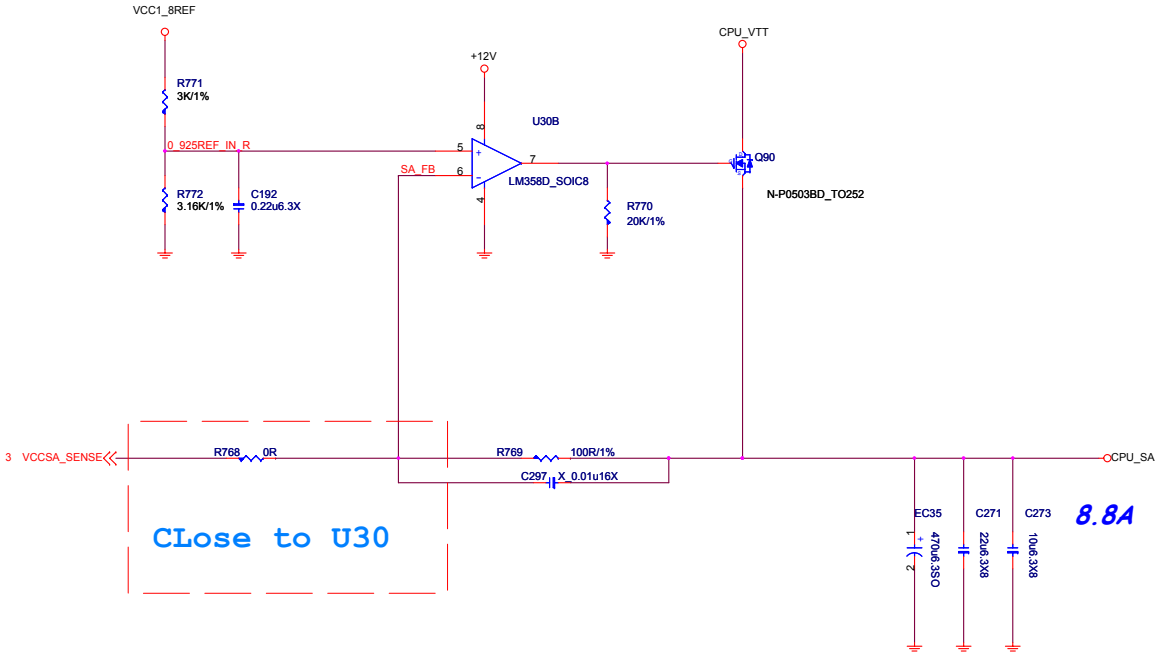
CPU_SA:0.925/0.85

SA Core =8.8A

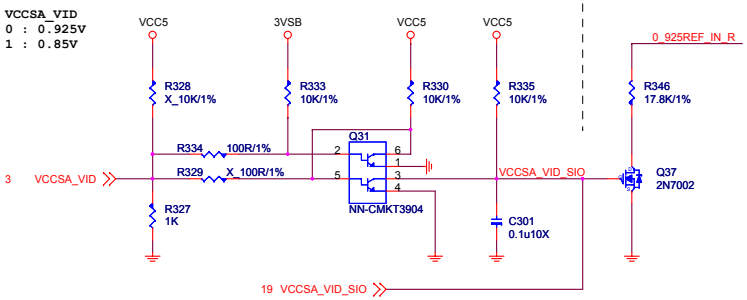






VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



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Size: Custom	Document Description: CPU_SA OP+MOS 1-Phase	Rev: 0A
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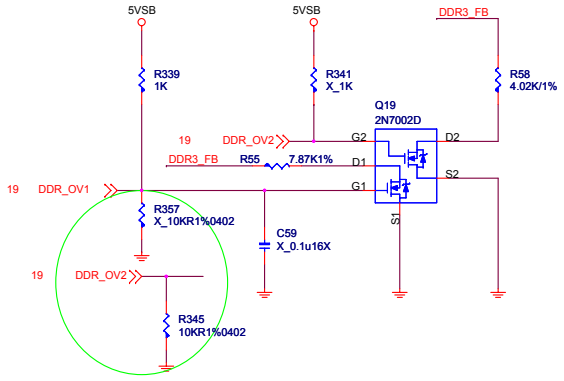
DDR Power:1.5V

DDR3_1.5V 4.75A+15A+1A=20.75A

4.75A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

Iripple=8A
4.7*2*1=9.4A>8A

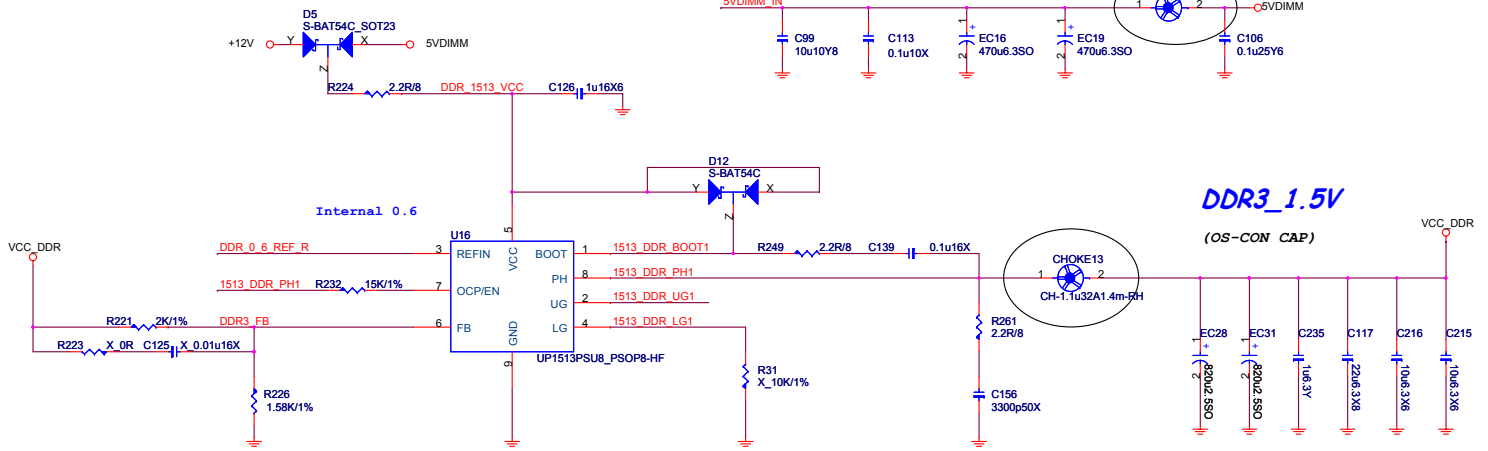
DDR OV



*Default 1.5V

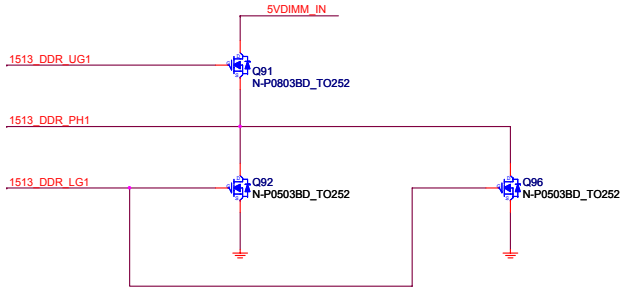
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

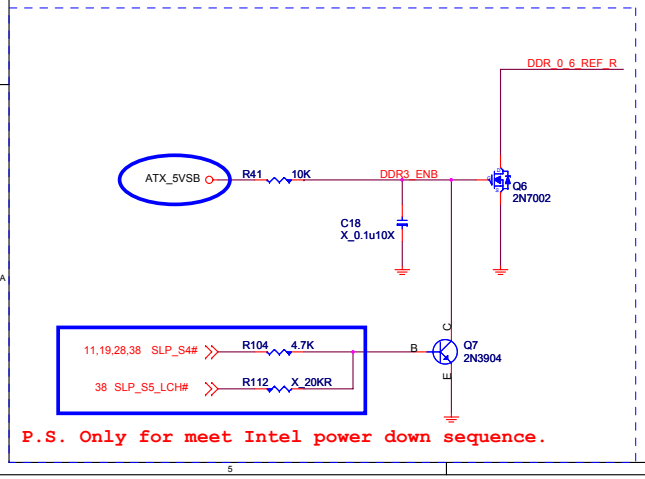
DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)



((R221/R226)+1)*0.6=1.5V

DDR3_1.5V



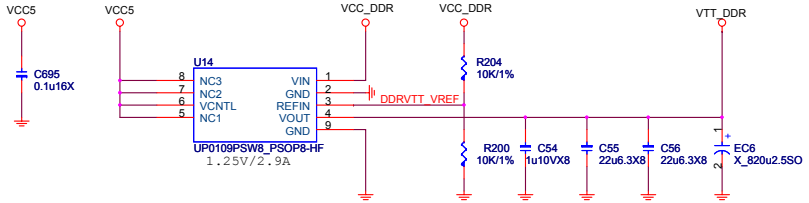


P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A



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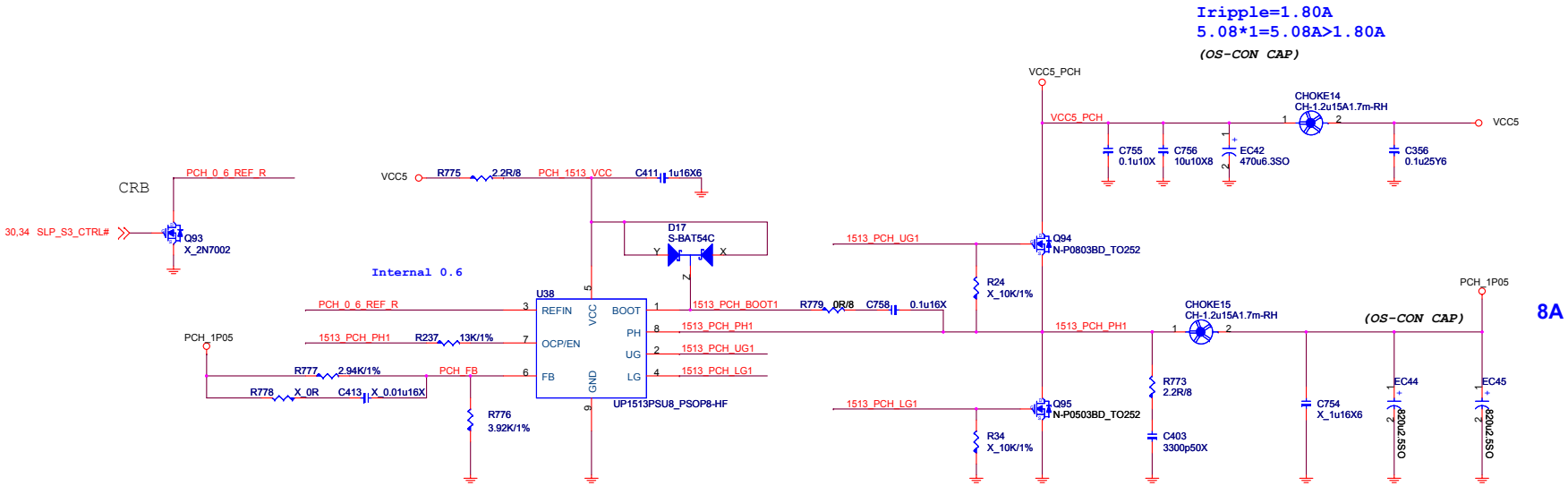
PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE



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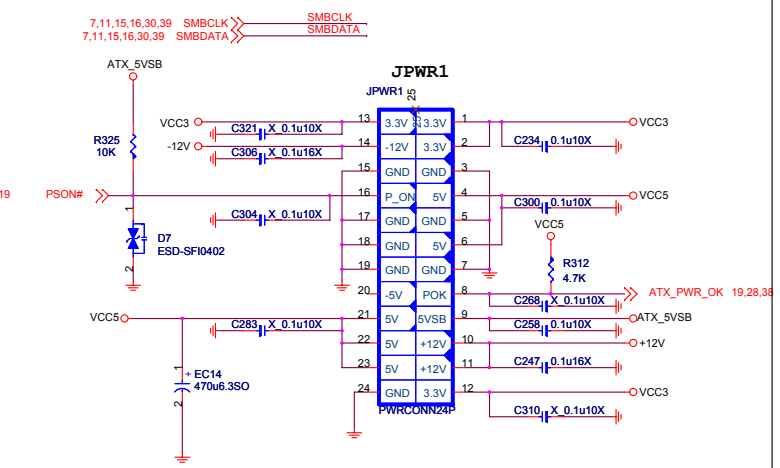
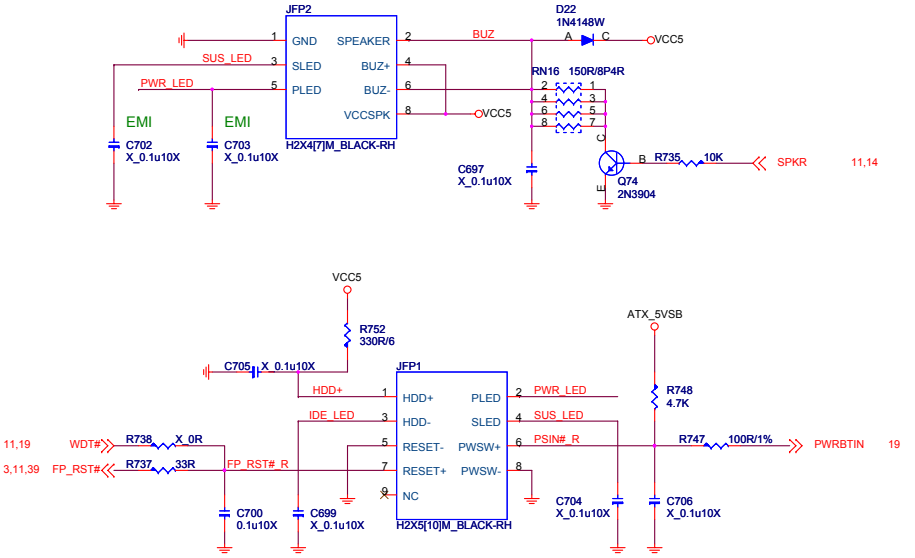
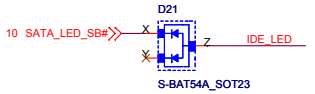
ATX POWER CONNECTOR

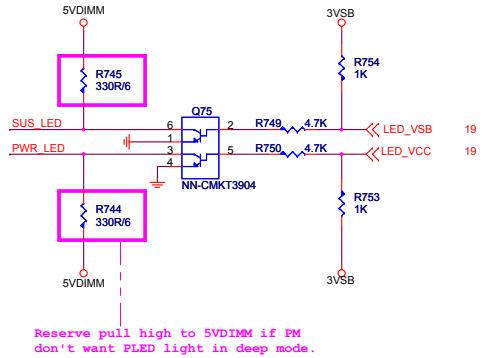


FRONT PANNEL

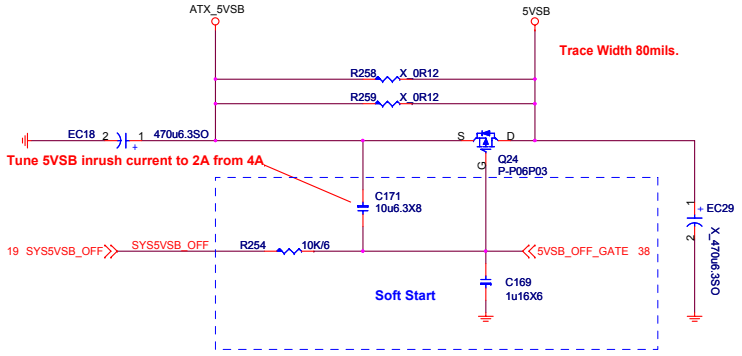




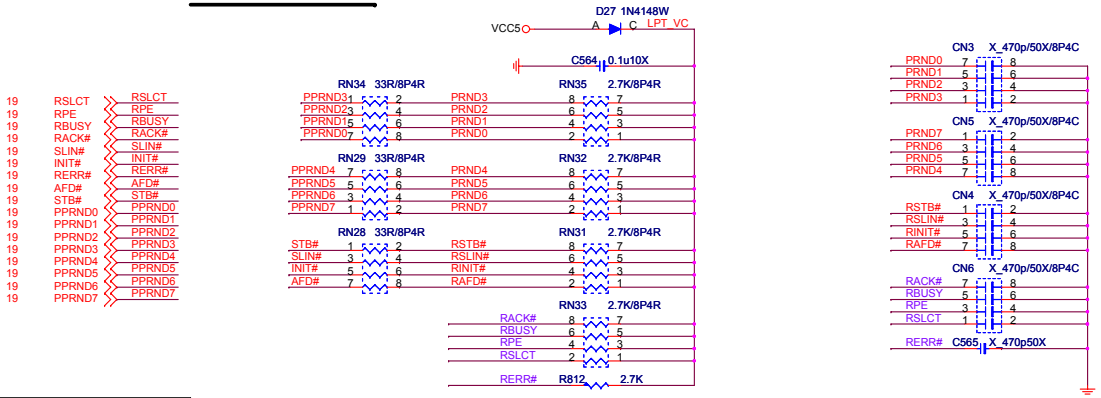
LED (for Fintek 71869)



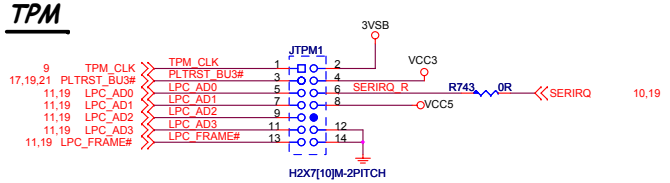
5VSB Power Switch



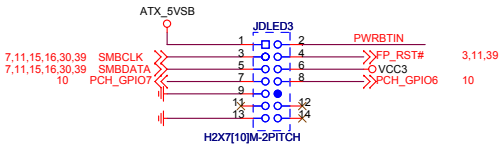
PARALLAL PORT



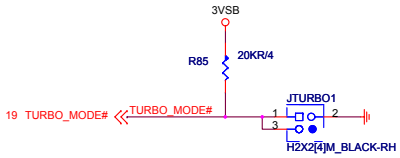
TPM

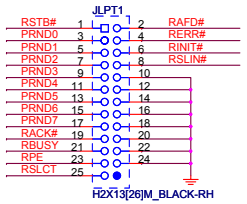


JDLED3



Turbo Button





N31-2131151-H06 : 2.0mm

N31-2131131-H06 : 2.54mm

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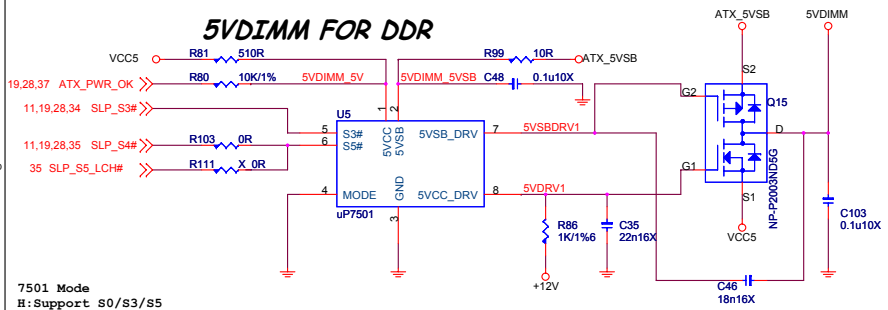
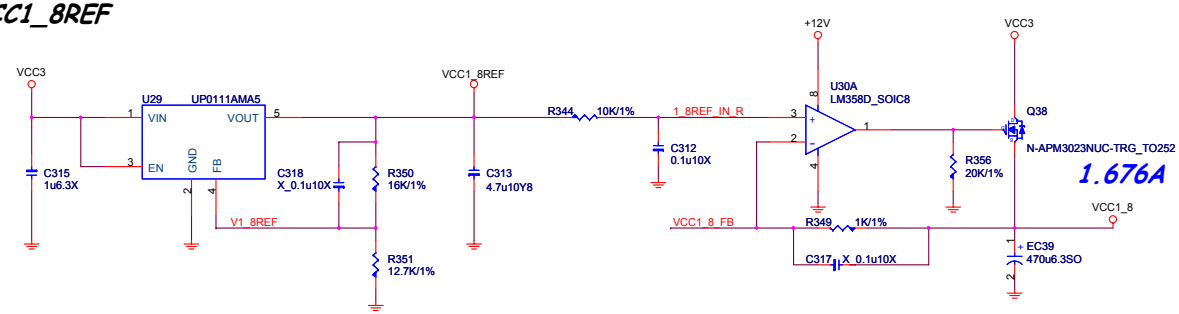
5VDIMM FOR DDR

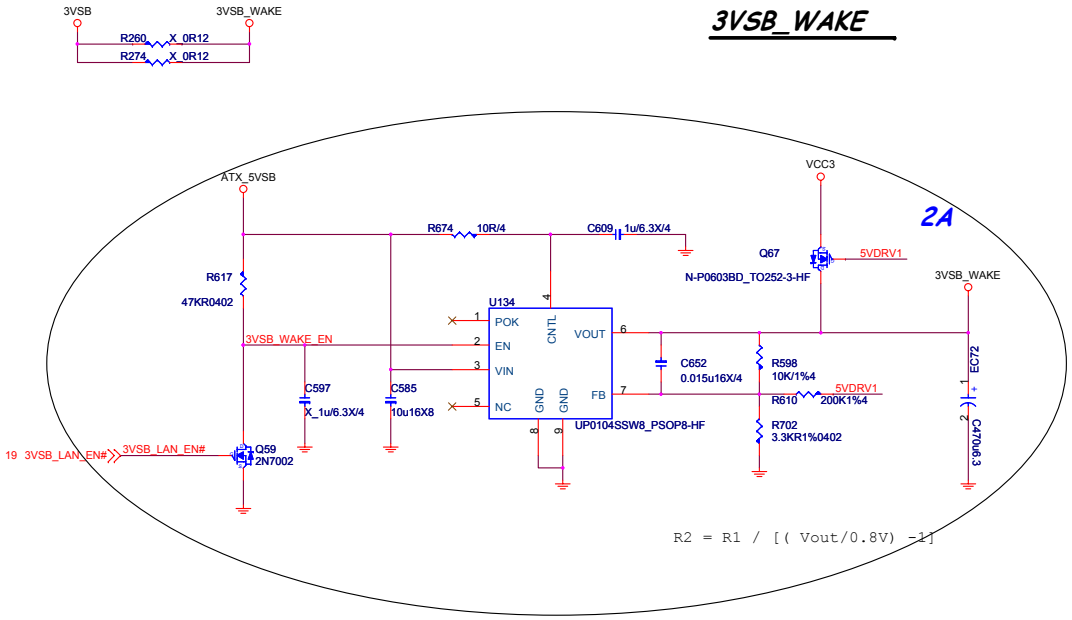


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

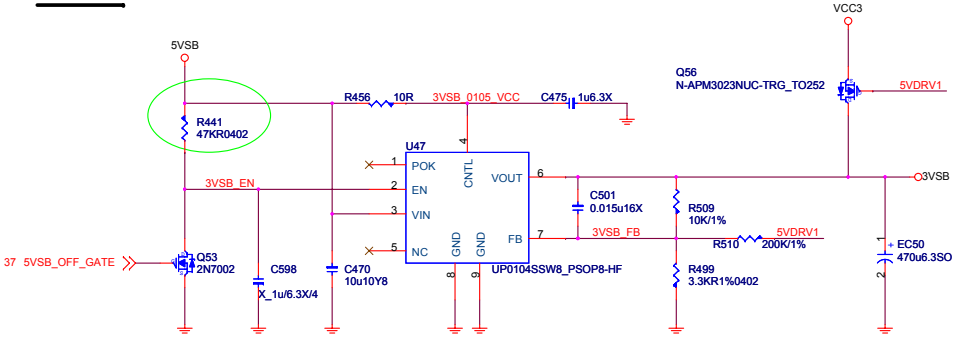
VCC1_8REF



3VSB_WAKE

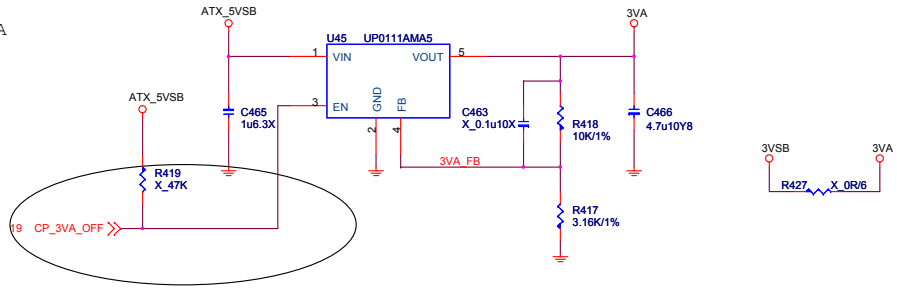


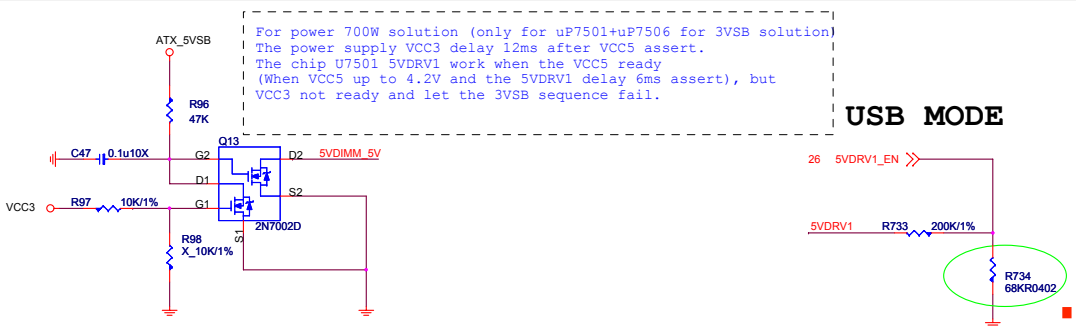
3VSB



3VA

20mA





USB MODE

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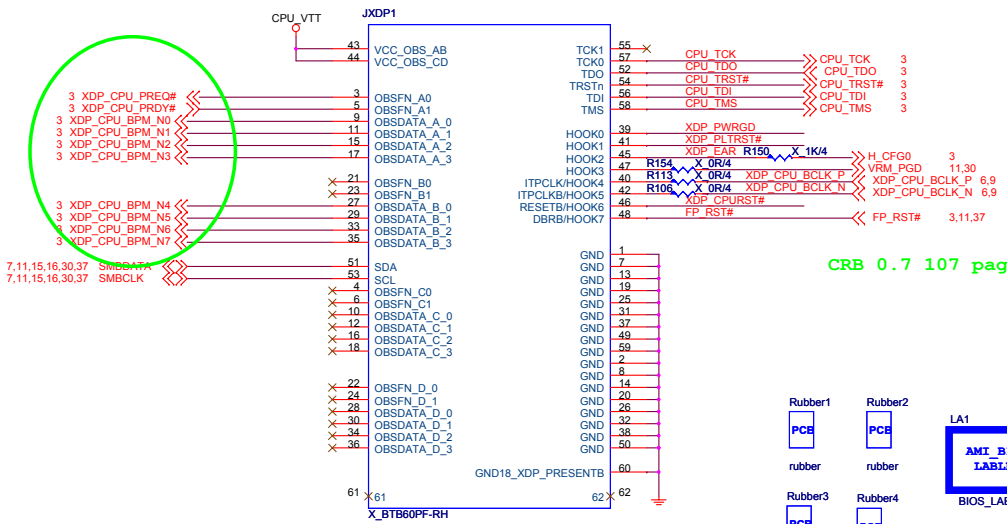
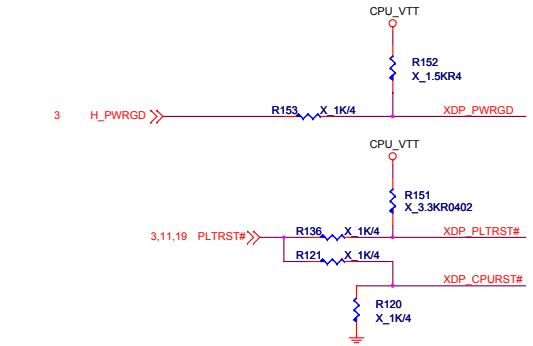
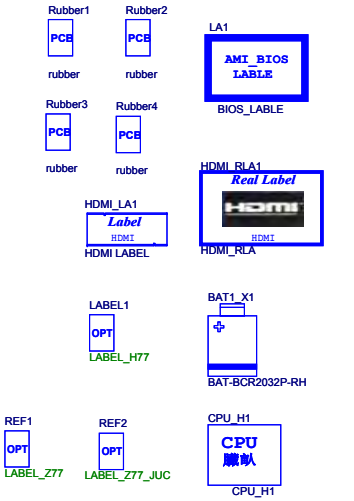
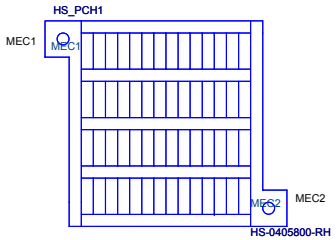
Reserve debug port 5020

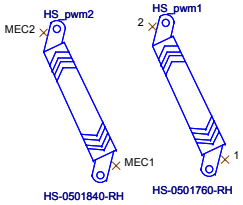




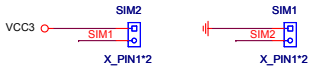




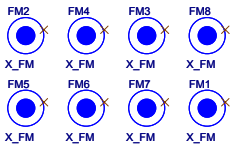
HEATSINK



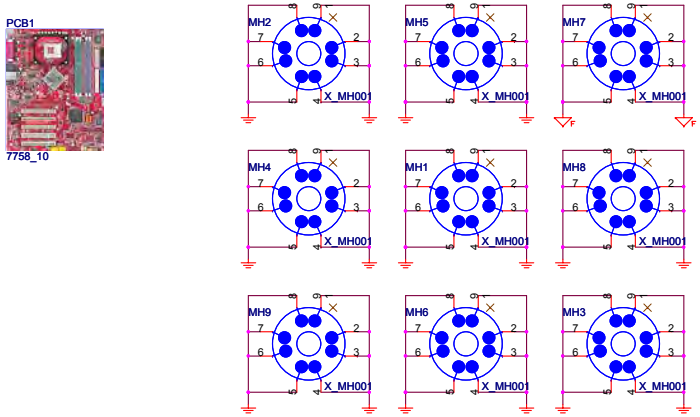
Simulation



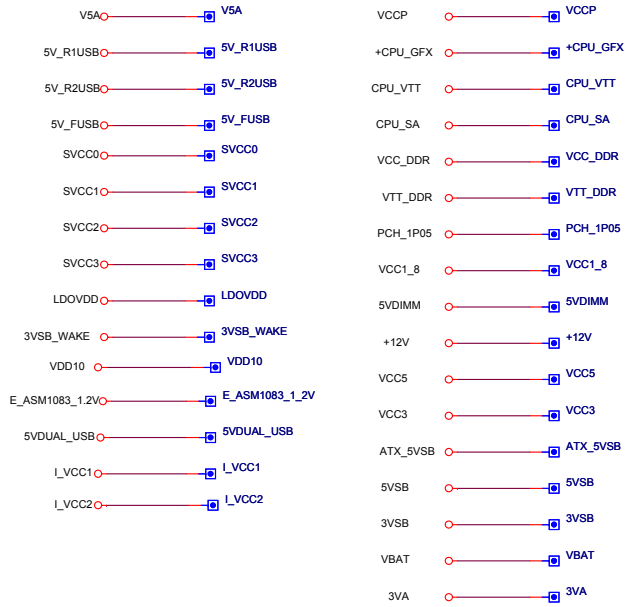
Optical Fiducial Marks-120



Mounting Holes



Voltage test point



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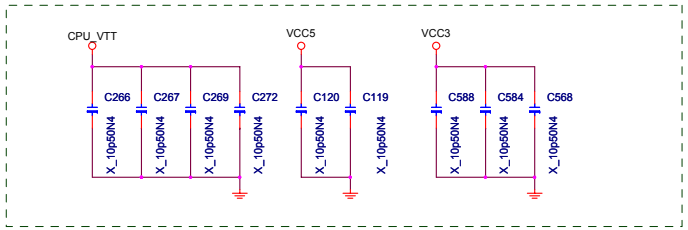
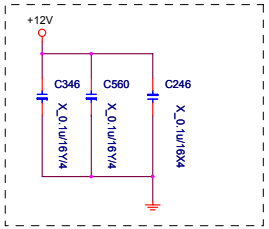
EMI:cap. for signal return path



EMI



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