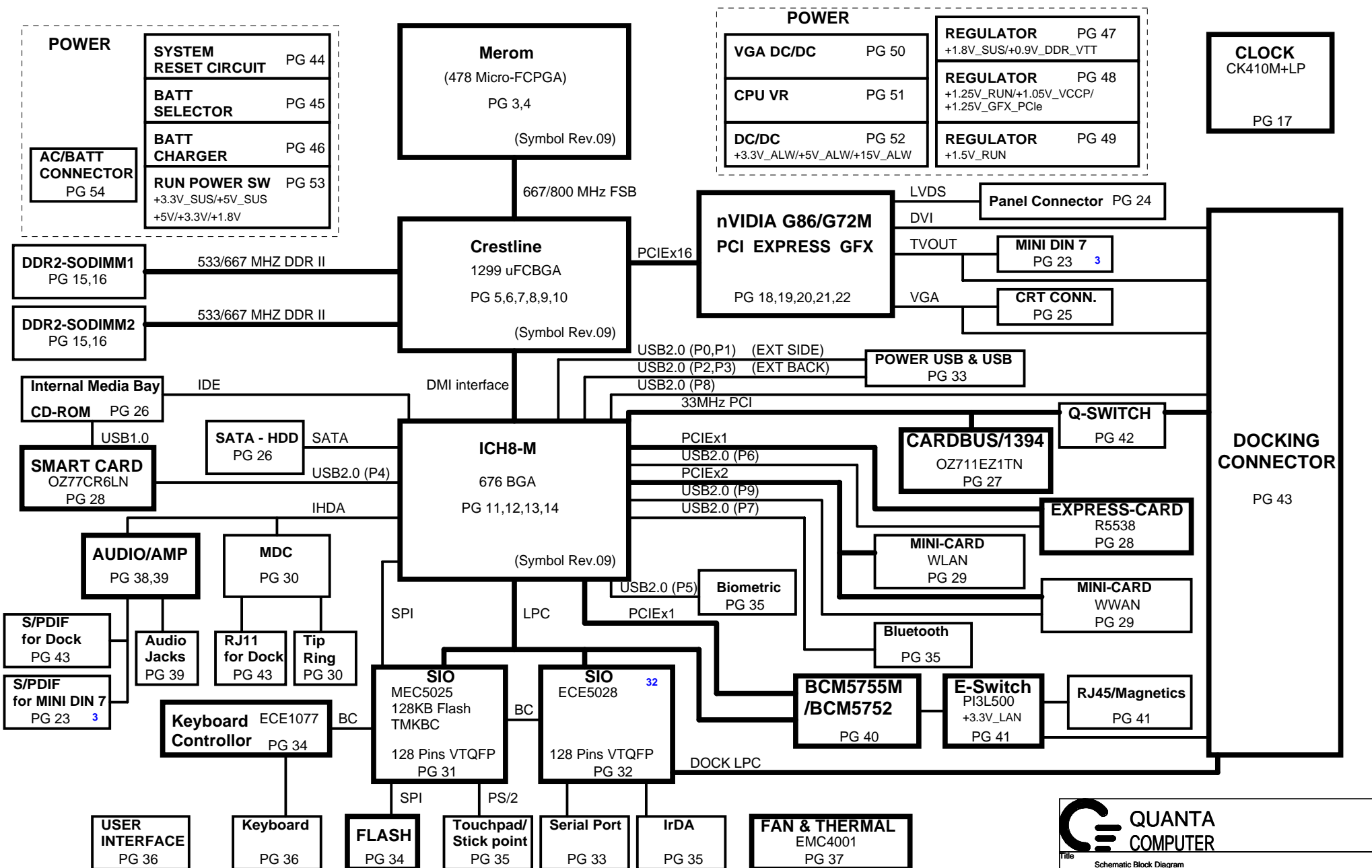


JM7B-DISCRETE

PWA FP384, PWB UW445,
SCHEM KU954. (256MB)
VER : 2A




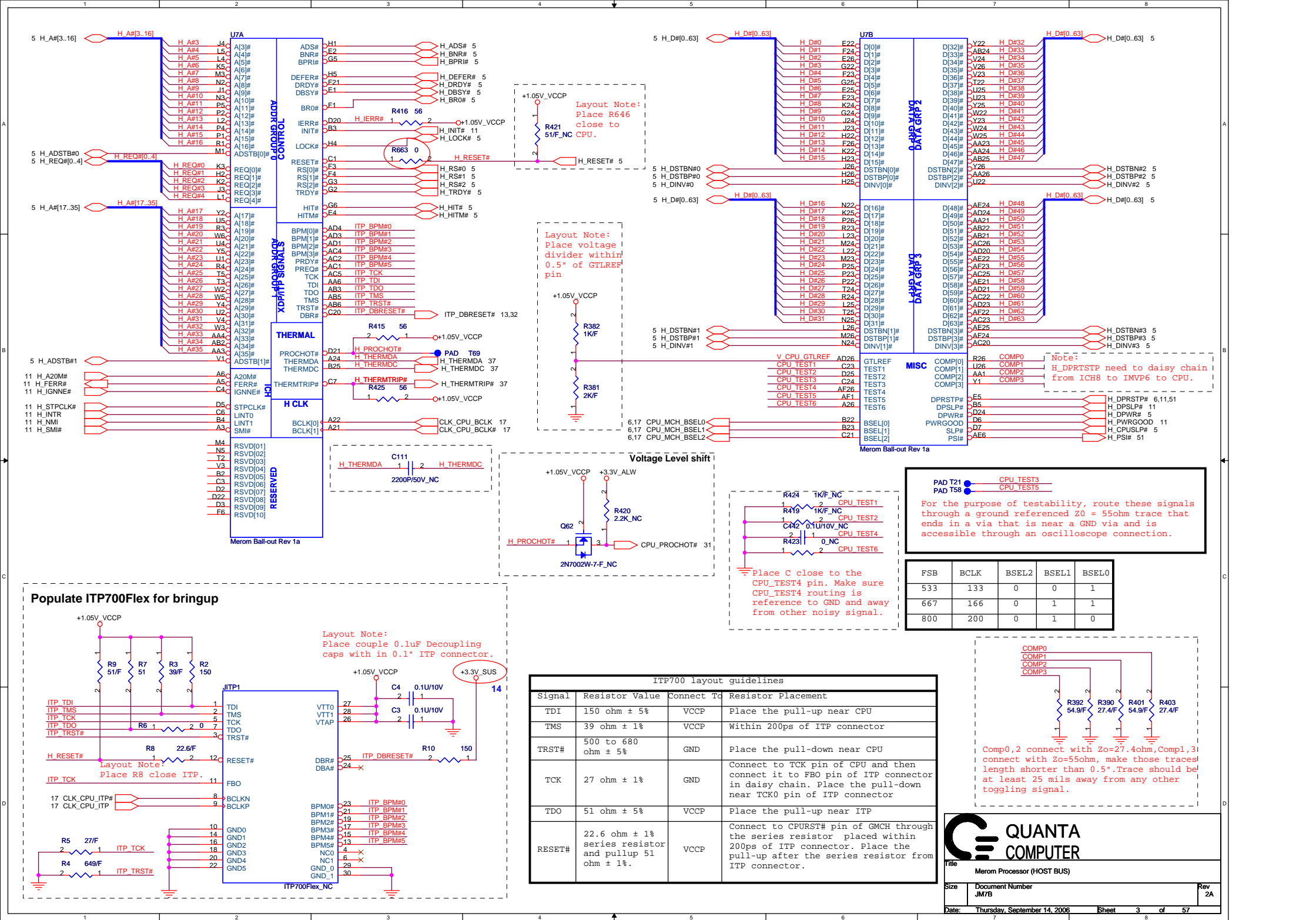
INDEX

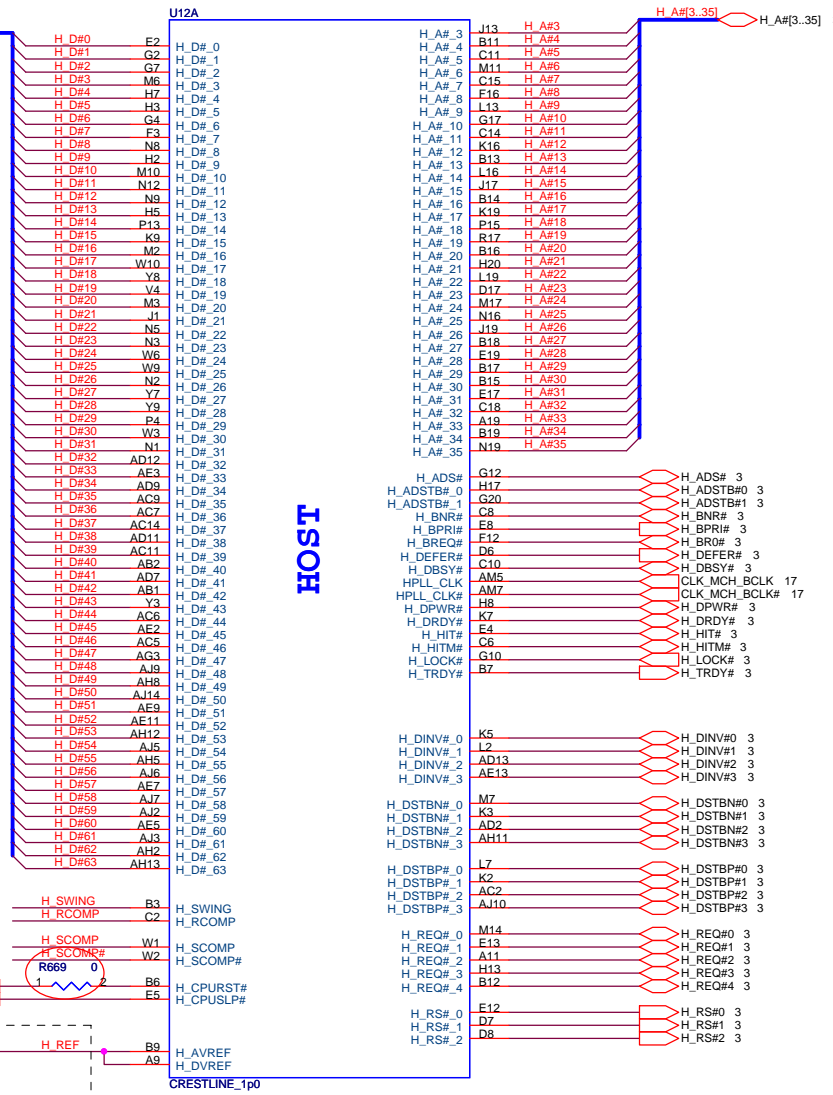
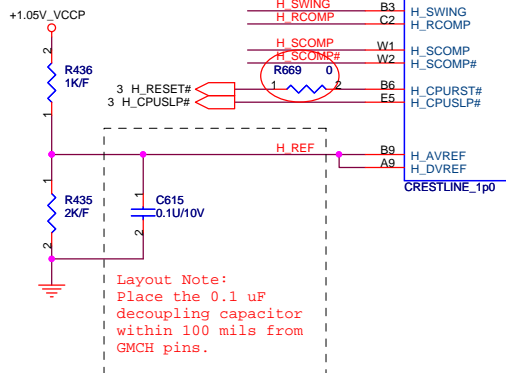
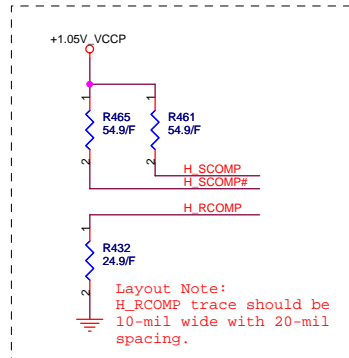
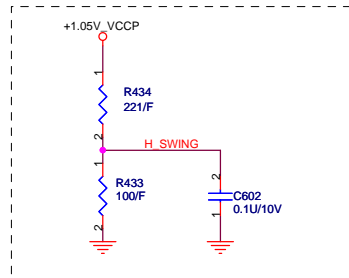
| Pg# | Description |
|-------|----------------------------------|
| 1 | Schematic Block Diagram |
| 2 | Front Page |
| 3-4 | Merom |
| 5-10 | Crestline |
| 11-14 | ICH8M |
| 15-16 | DDRII SO-DIMM(200P) |
| 17 | Clock Generator |
| 18-23 | VGA |
| 24 | LCD Conn. & SSP |
| 25 | CRT Conn |
| 26 | SATA & IDE Conn |
| 27 | PCCARD/Conn & 1394 |
| 28 | Express Card & Smart Card |
| 29 | Mini Card |
| 30 | MDC Conn. |
| 31 | SIO (MEC5025) |
| 32 | SIO (MEC5018) |
| 33 | SERIAL PORT & USB |
| 34 | Flash ROM, RTC & ECE1077 |
| 35 | TP,BT & FIR |
| 36 | Switch,Keyboard & LED |
| 37 | FAN & Thermal |
| 38-39 | Audio CODEC(STAC9205)/Phone Jack |
| 40-41 | LOM (Nineveh)/Switch |
| 42-43 | Docking Conn/Q-Switch |
| 44 | System Reset Circuit |
| 45-46 | Battery Selector & Charger |
| 47 | DDR2_1.8VSUS, 0.9V |
| 48 | 1.5VSUS,1.05V(VTT) |
| 49 | VGA DC/DC,1.25V,1.05V |
| 50 | CPU_MAX8786(3phase) |
| 51 | D/D Power |
| 52 | RUN Power Switch |
| 53 | DCIN,Batt |
| 54 | PAD& SCREW |
| 55 | EMI CAP |
| 56 | SMBUS BLOCK |

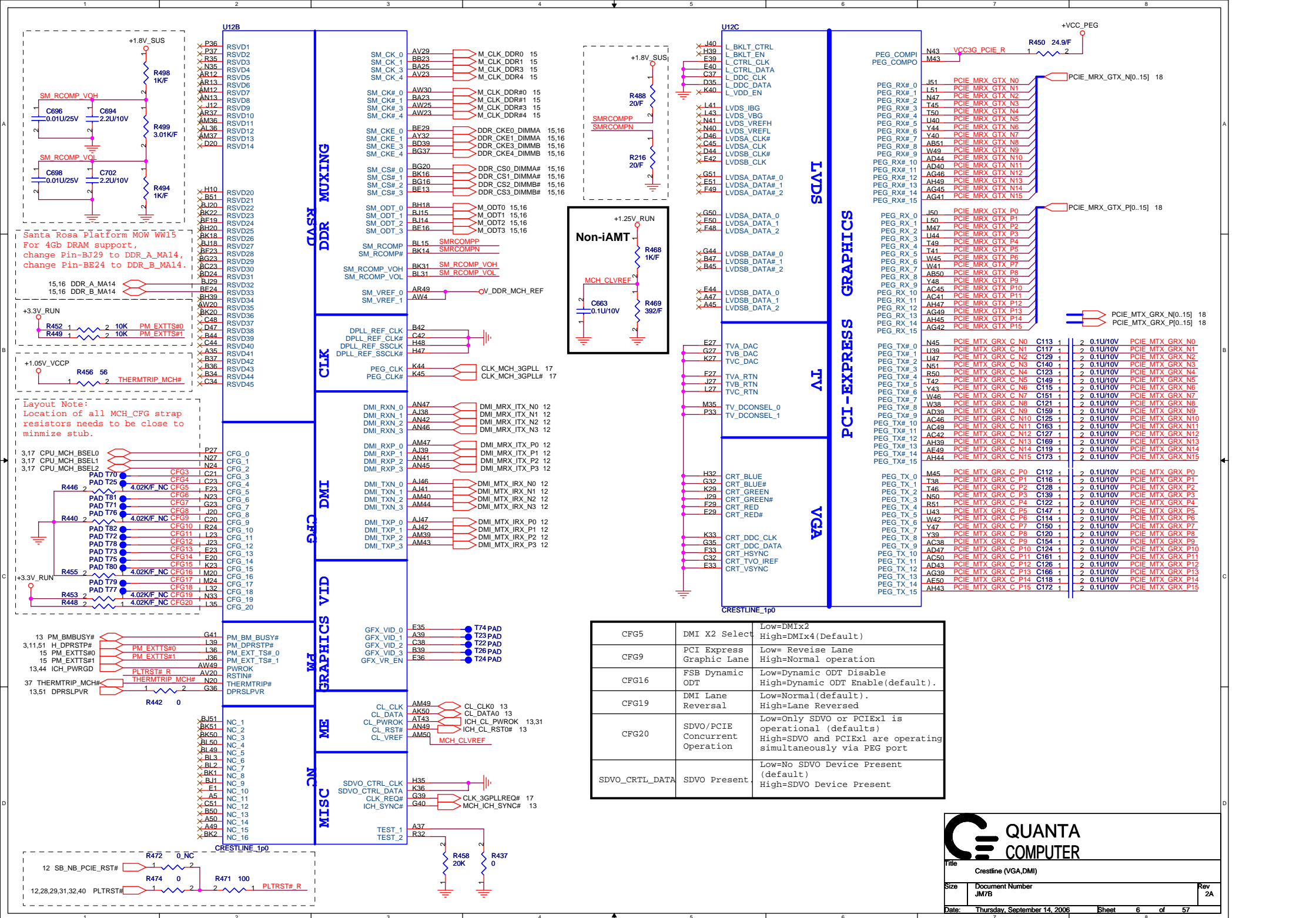
Power States

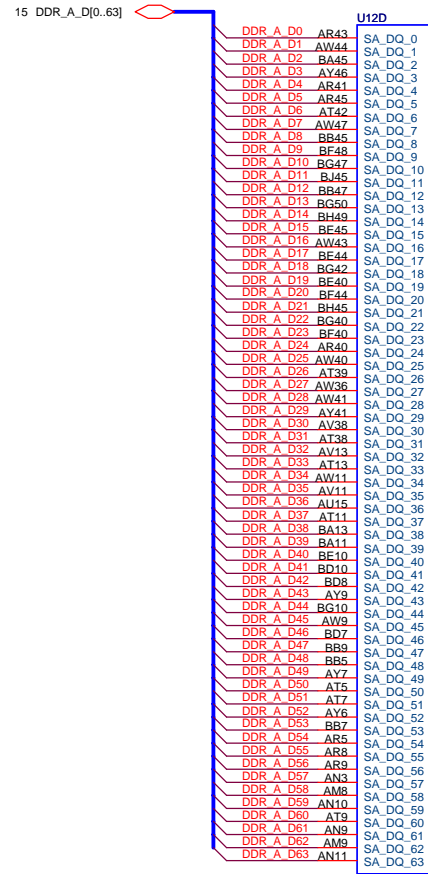
| Power Rail | Control Signal | S0/M0 | S3/M1 | S3/M1 | S4/M1 | S3/M-off | S4/M-off | S5/M-off |
|-----------------|----------------|-------|-------|-------|-------|----------|----------|----------|
| +3.3V_ALW | | | | | | | | |
| +5V_ALW | | | | | | | | |
| +3.3V_LAN | | | | | | | | |
| +1.25V_SRC_M | | | | | | | | |
| +1.05V_M | | | | | | | | |
| +1.8V_SUS | | | | | | | | |
| +0.9V_DDR_VTT | | | | | | | | |
| +5V_SUS | | | | | | | | |
| +3.3V_SUS | | | | | | | | |
| +5V_RUN | | | | | | | | |
| +3.3V_RUN | | | | | | | | |
| +1.8V_RUN | | | | | | | | |
| +1.25V_RUN | | | | | | | | |
| +1.5V_RUN | | | | | | | | |
| +1.05V_VCCP | | | | | | | | |
| VCC_VCRE | | | | | | | | |
| +LCDVCC | | | | | | | | |
| +5V_MOD | | | | | | | | |
| +VCC_GFX_CORE | | | | | | | | |
| +1.25V_GFX_PCle | | | | | | | | |
| +2.5V_RUN | | | | | | | | |

| | | |
|--|----------------------|--------|
|  QUANTA COMPUTER | | |
| Title Index & Power Status | | |
| Size | Document Number JM7B | Rev 2A |
| Date: Thursday, September 14, 2006 | Sheet 2 | of 57 |

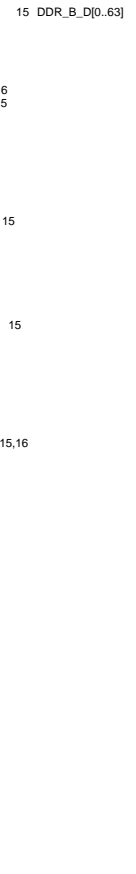
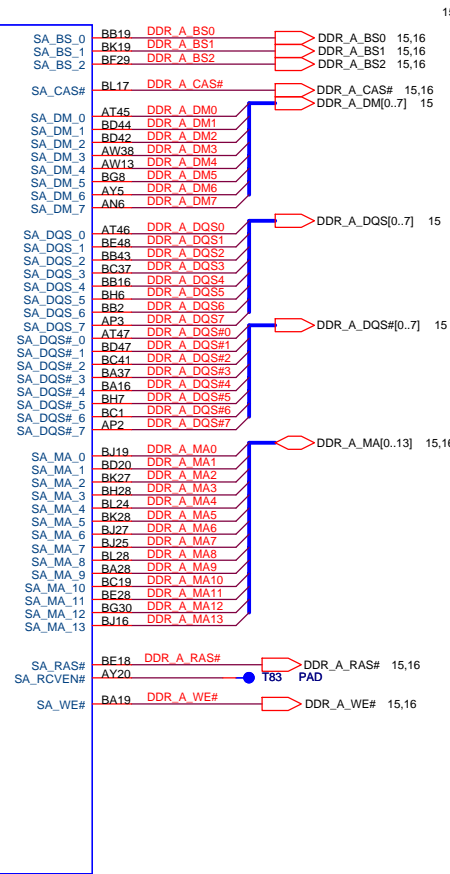




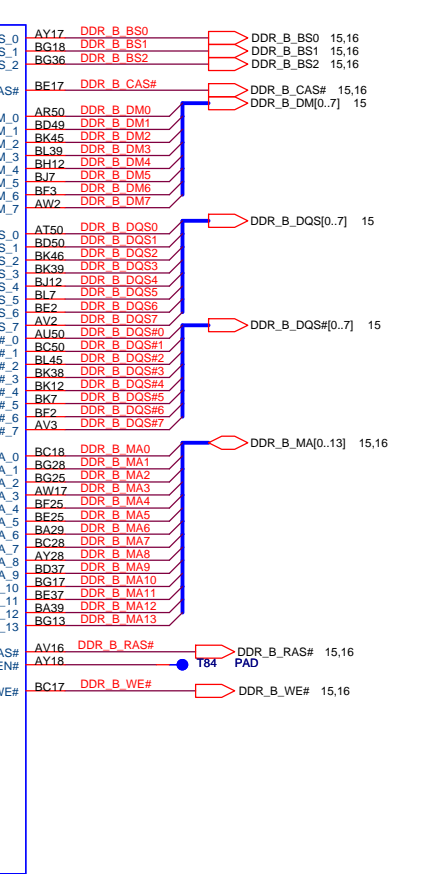
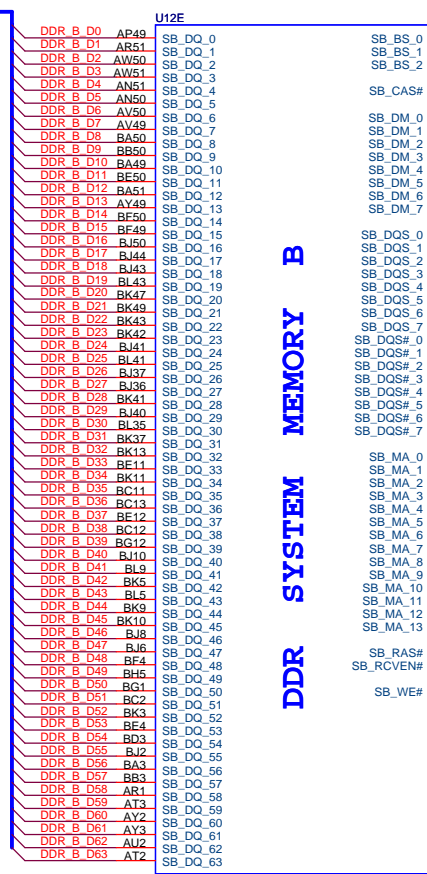


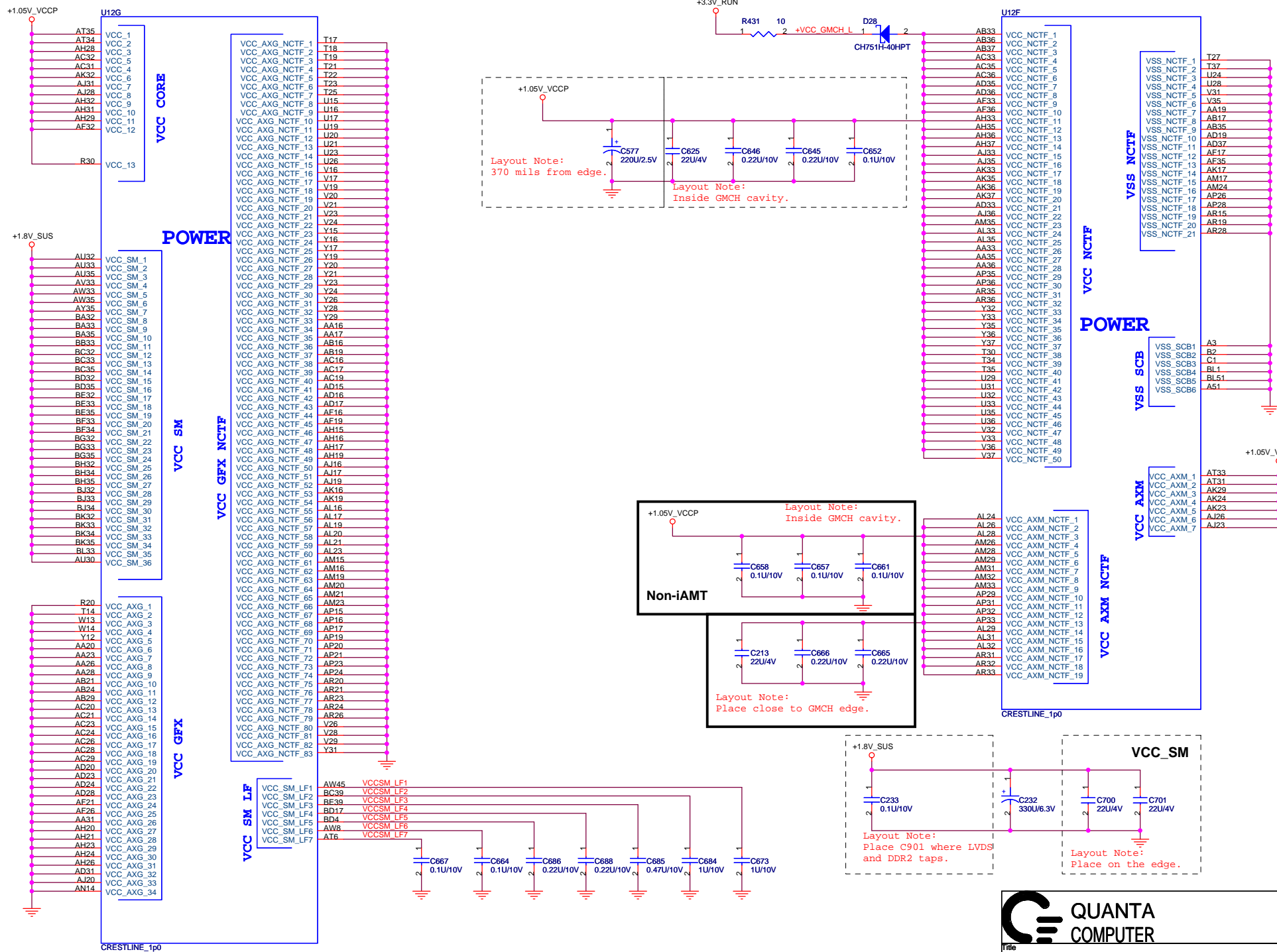


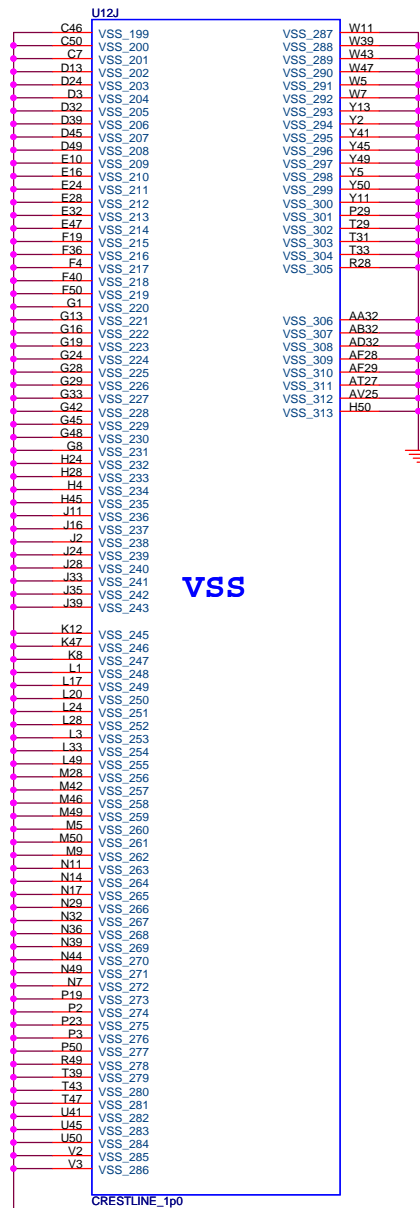
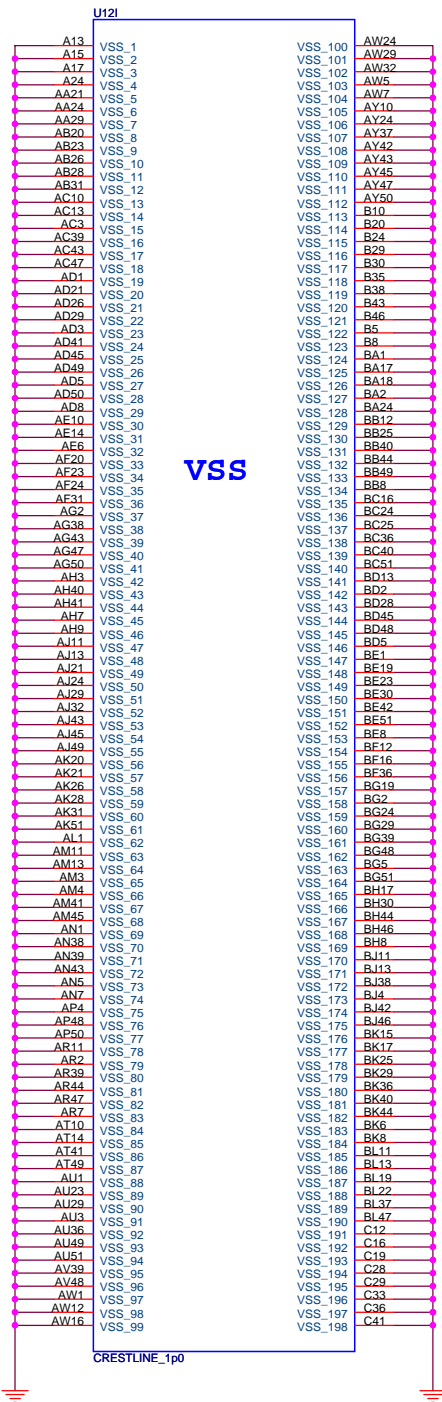
DDR SYSTEM MEMORY A




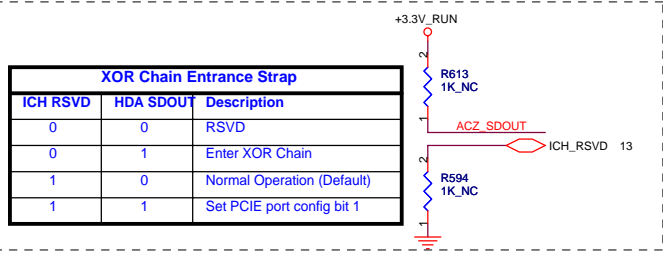
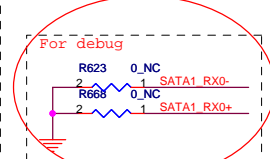
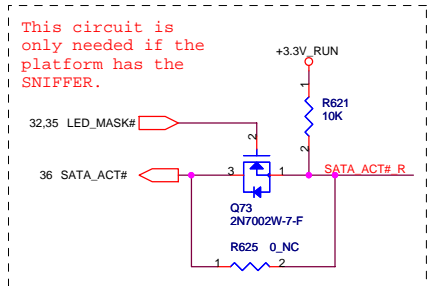
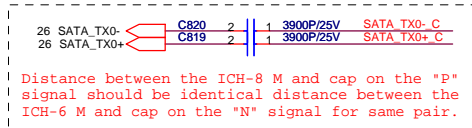
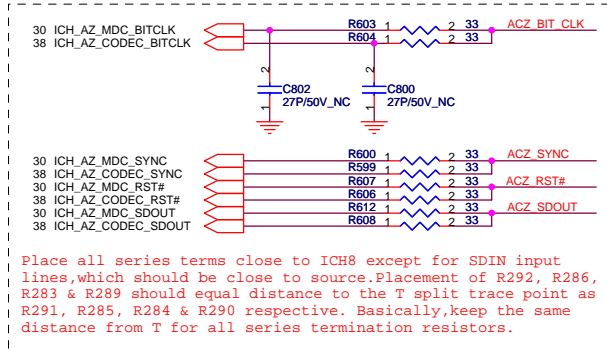
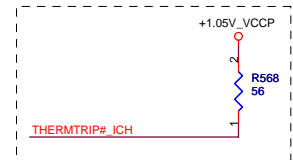
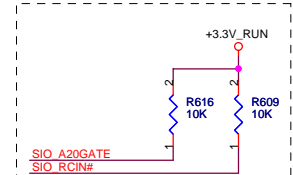
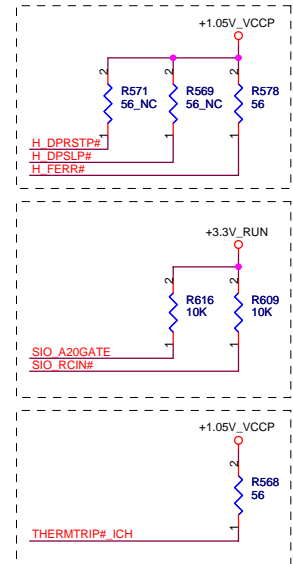
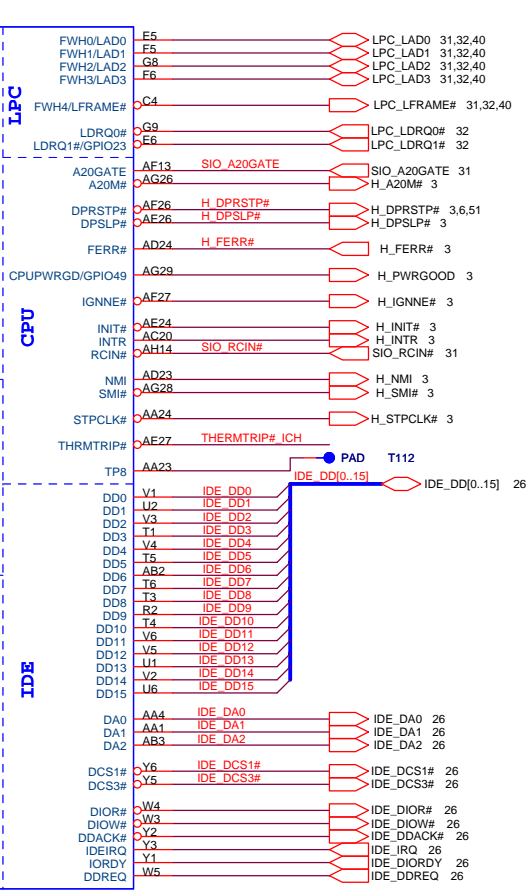
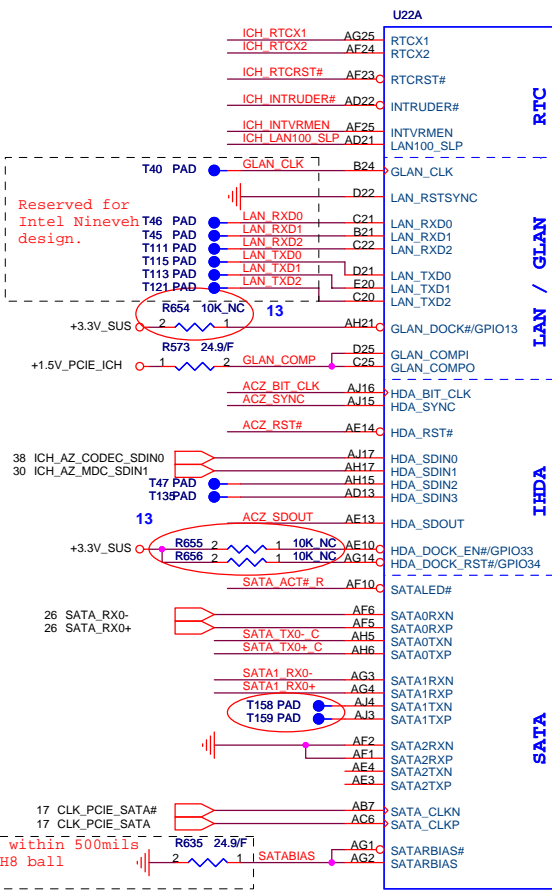
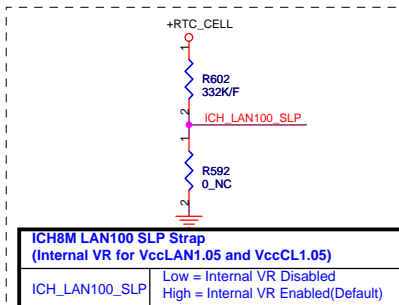
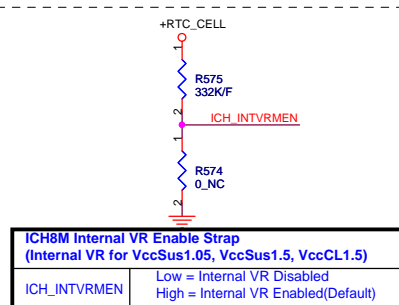
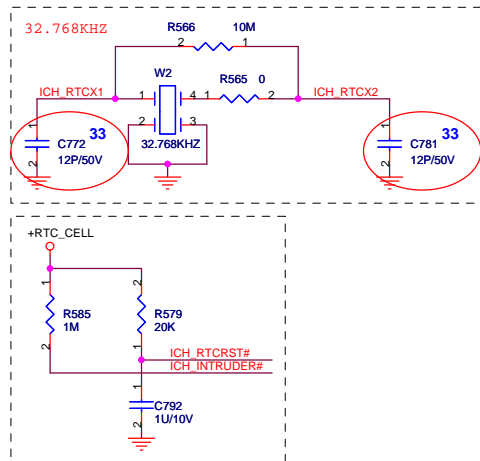
DDR SYSTEM MEMORY B



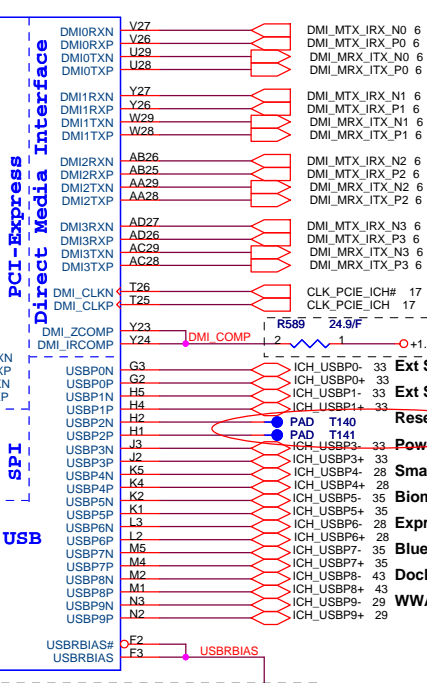
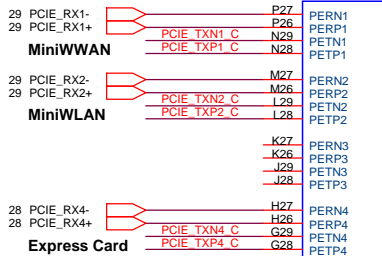
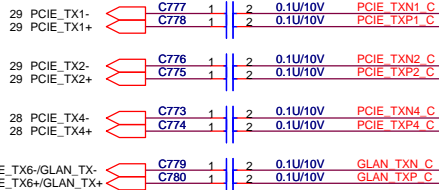


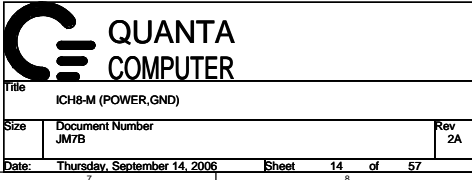


| | | |
|--|------------------------------|----------------|
|  QUANTA COMPUTER | | |
| Title Crestline (VSS) | | |
| Size | Document Number JM7B | Rev 2A |
| Date: | Thursday, September 14, 2006 | Sheet 10 of 57 |

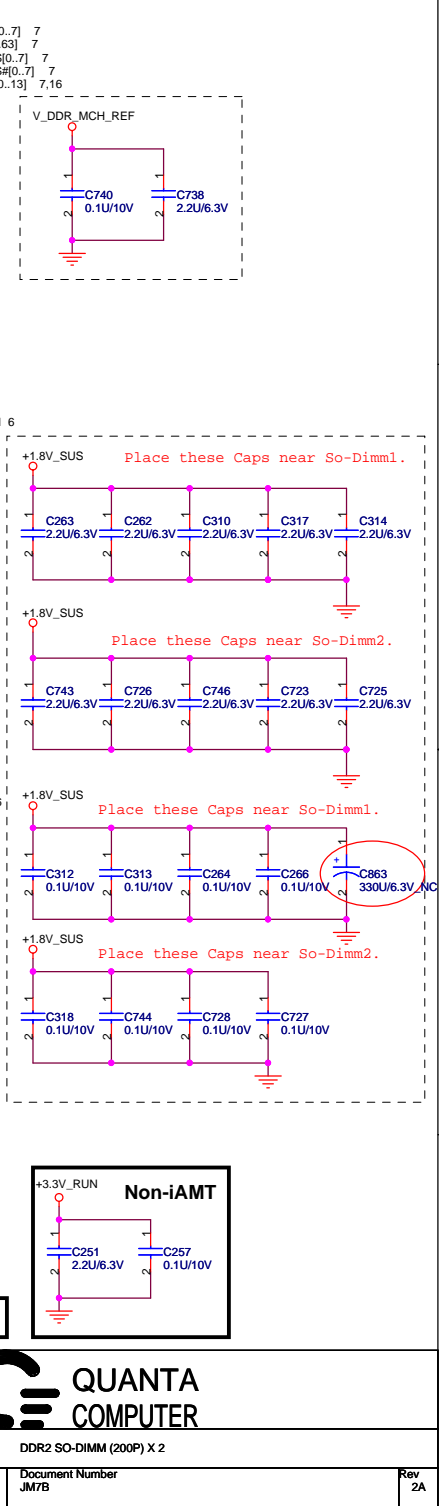
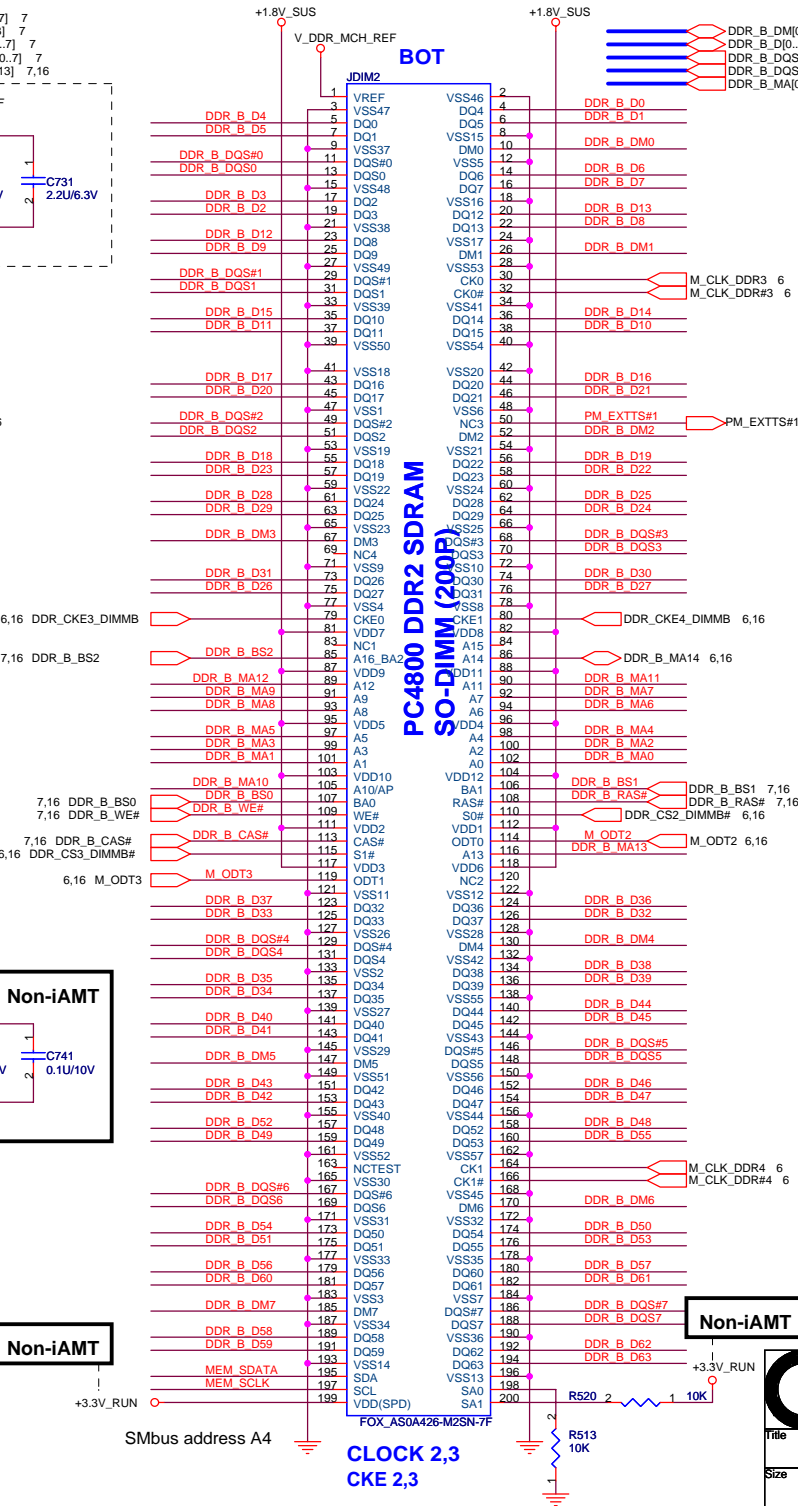
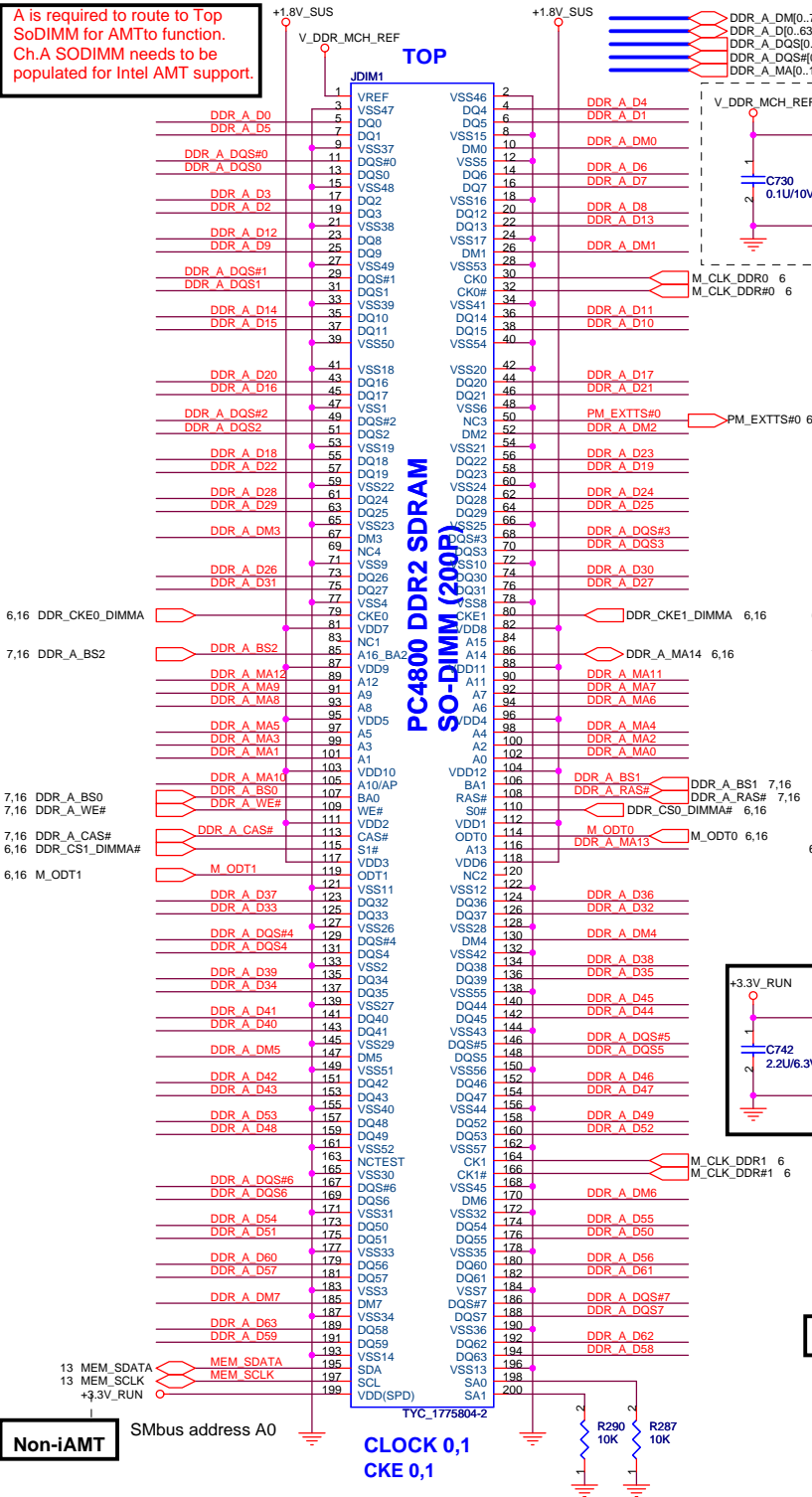


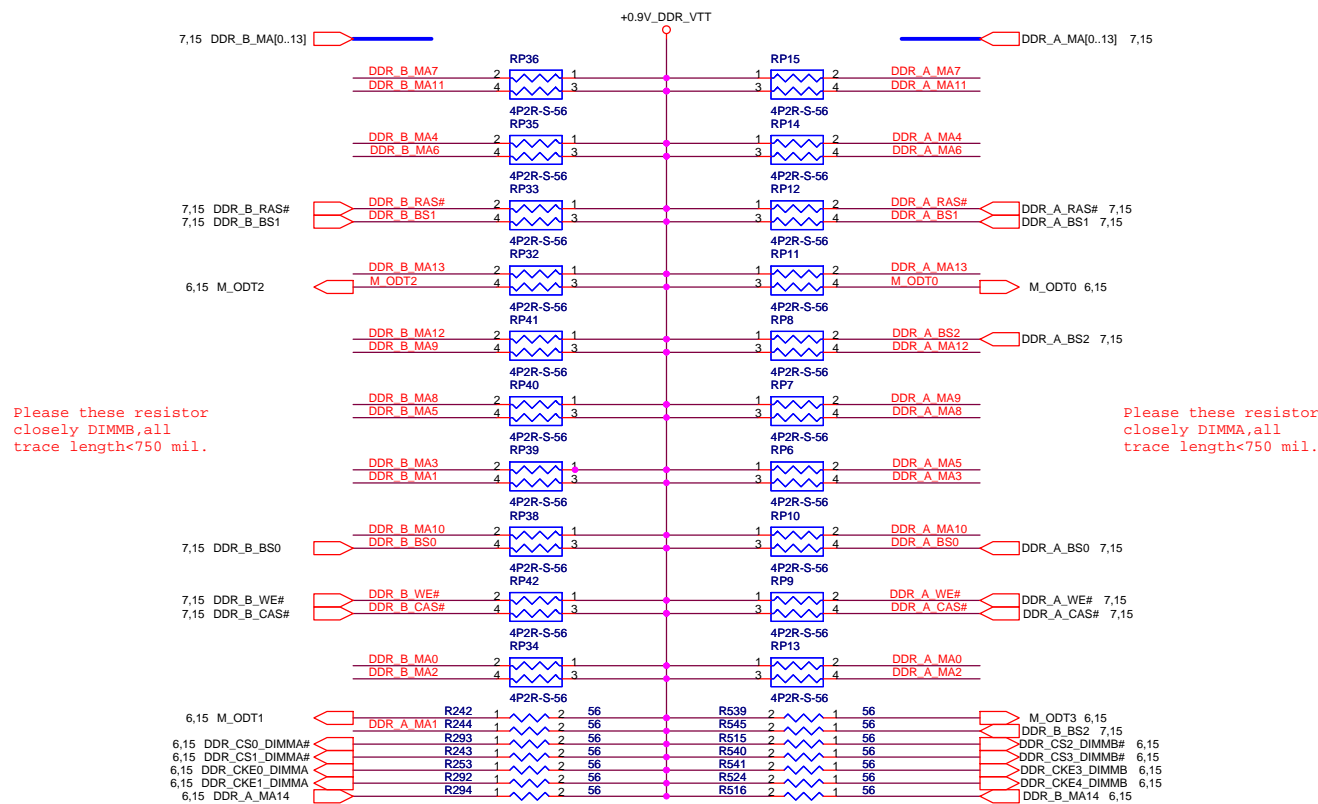
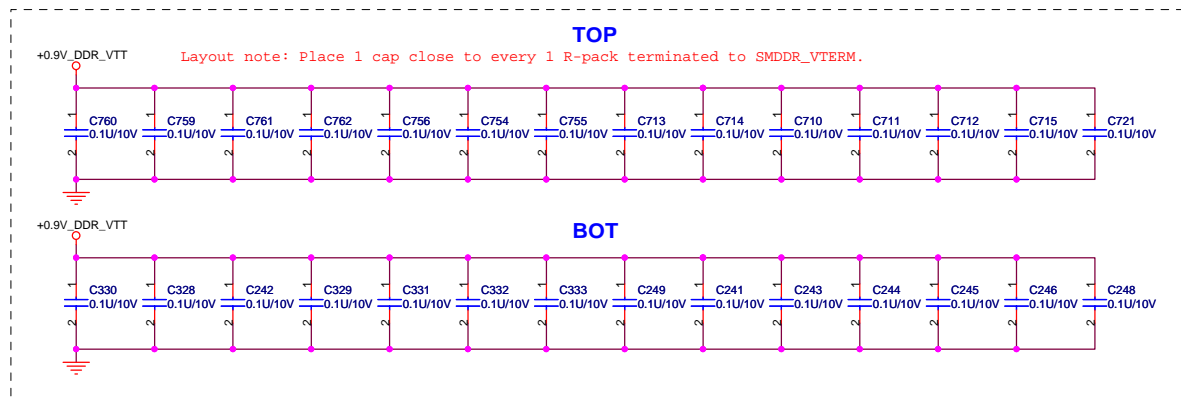
Place TX DC blocking caps close ICH8.

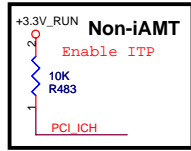
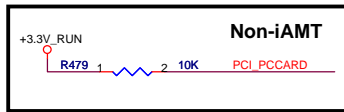
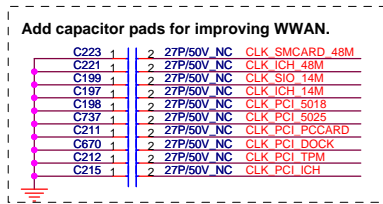
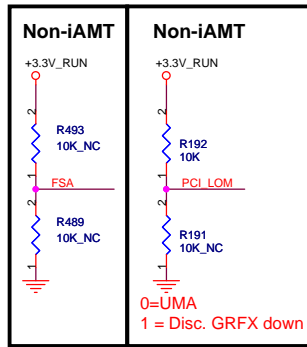




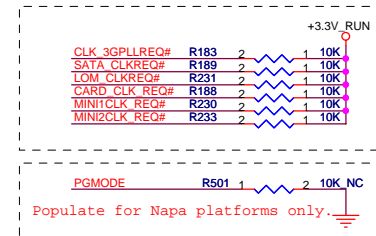
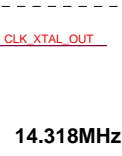
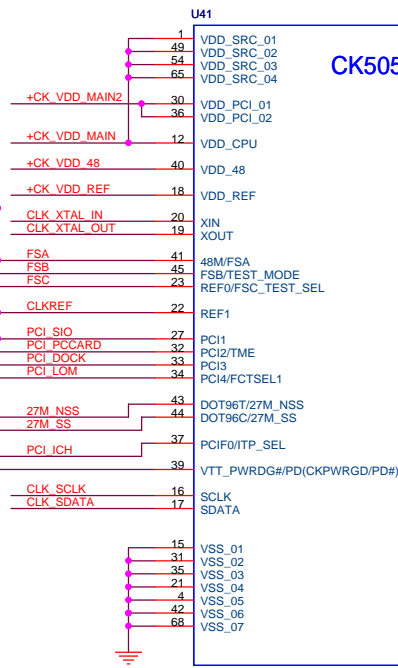
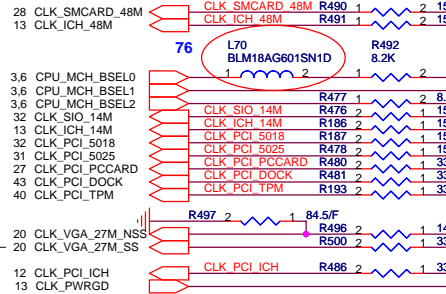
A is required to route to Top SoDIMM for AMT to function. Ch.A SODIMM needs to be populated for Intel AMT support.







Change R764 to i47
ohm TBD and pop R763
84.5 ohm TBD pull
down on R764 pin2.
CLK_VGA_27M_NSS is
max 1.2V.

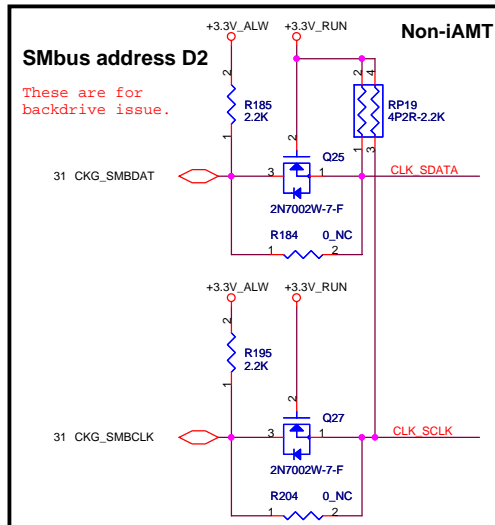
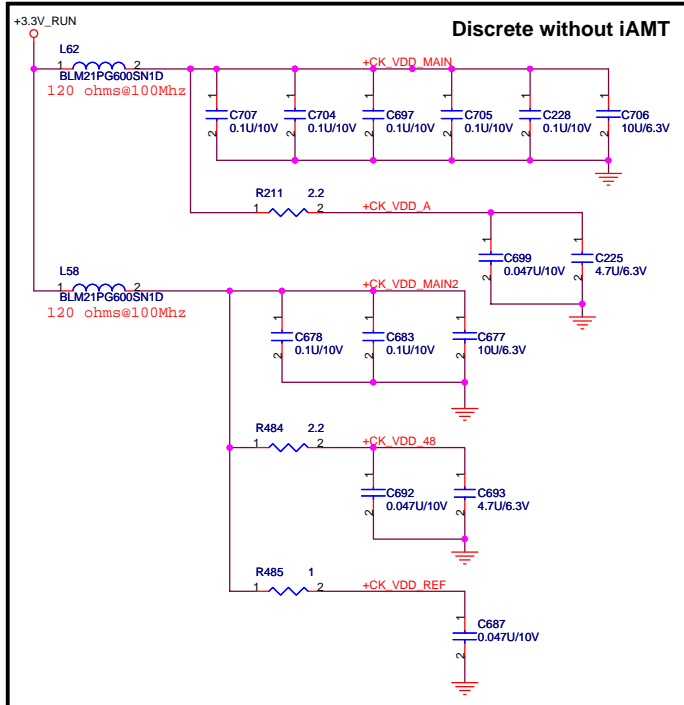


CK505

Non-iAMT

Discrete

Broadcom

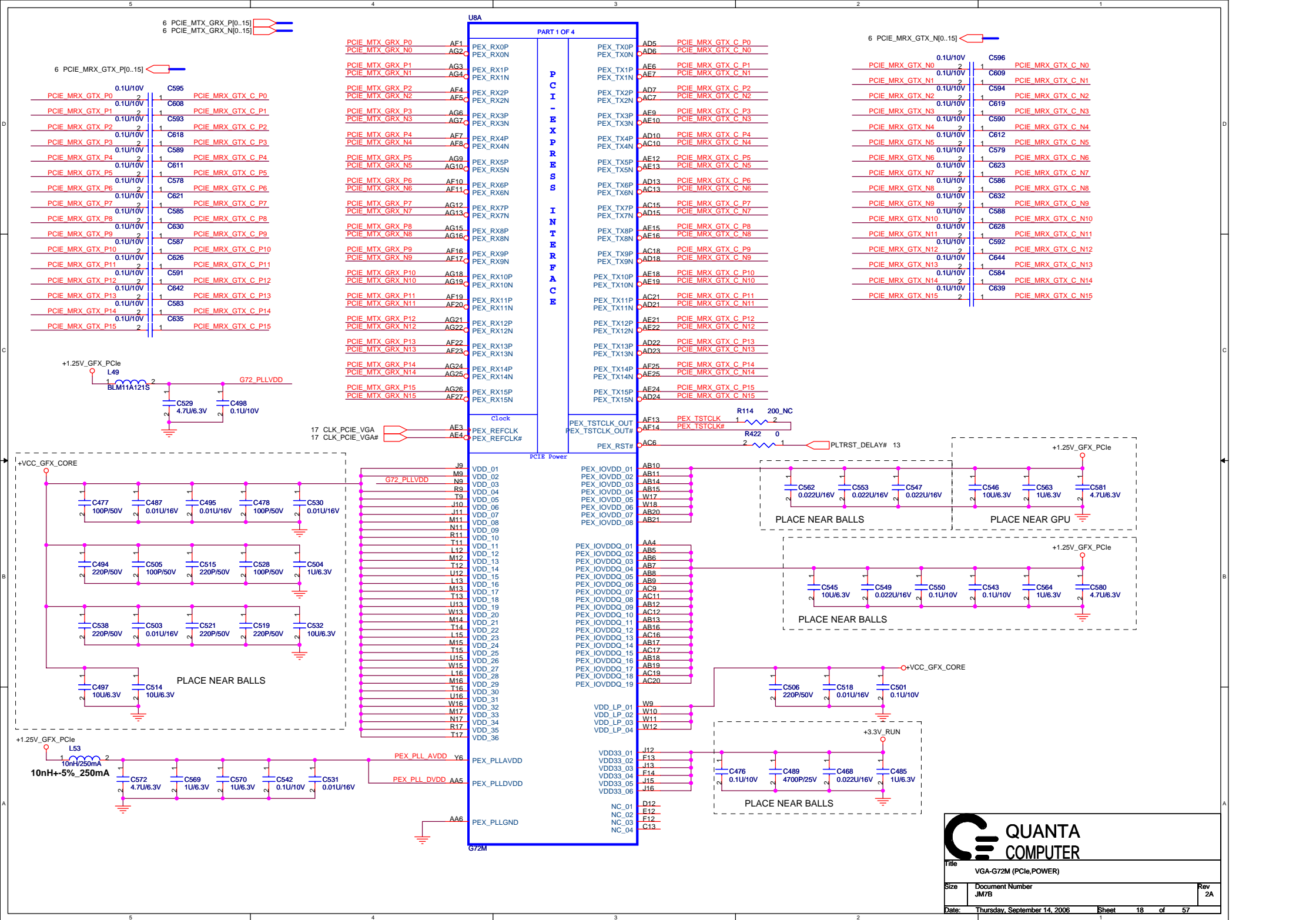


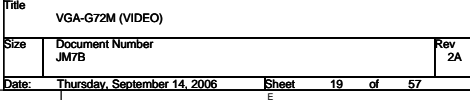
| FSC | FSB | FSA | CPU | SRC | PCI |
|-----|-----|-----|------|-----|-----|
| 1 | 0 | 1 | 100 | 100 | 33 |
| 0 | 0 | 1 | 133 | 100 | 33 |
| 0 | 1 | 1 | 166 | 100 | 33 |
| 0 | 1 | 0 | 200 | 100 | 33 |
| 0 | 0 | 0 | 266 | 100 | 33 |
| 1 | 0 | 0 | 333 | 100 | 33 |
| 1 | 1 | 0 | 400 | 100 | 33 |
| 1 | 1 | 1 | RSVD | 100 | 33 |

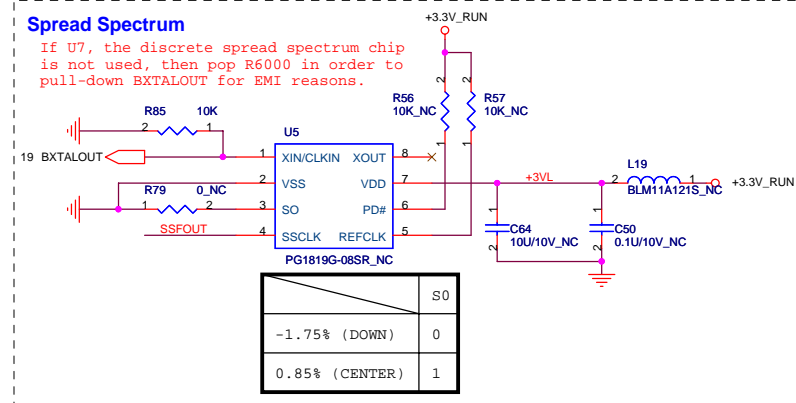
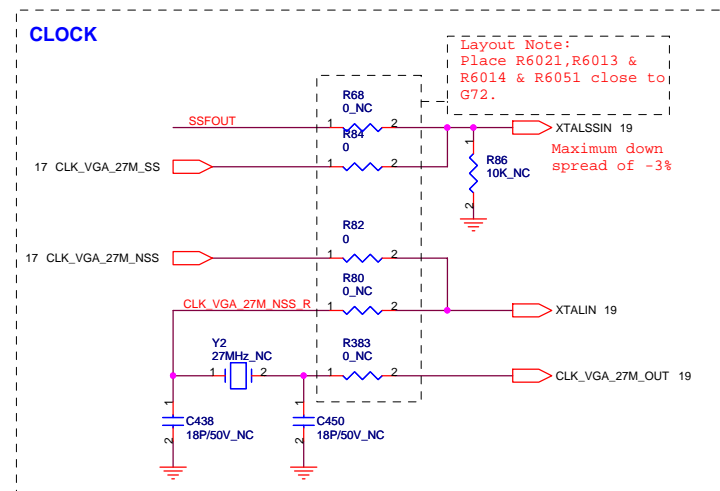
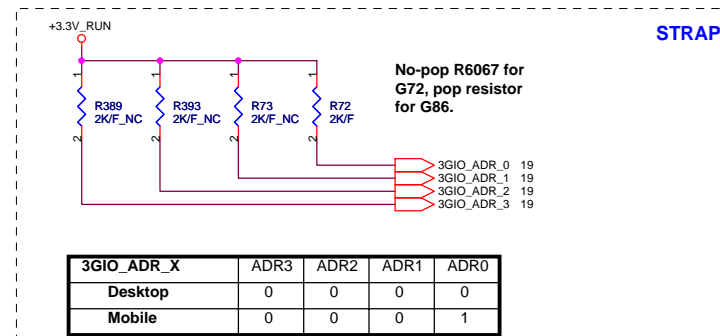
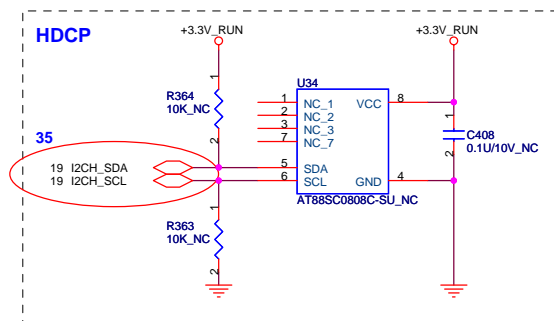
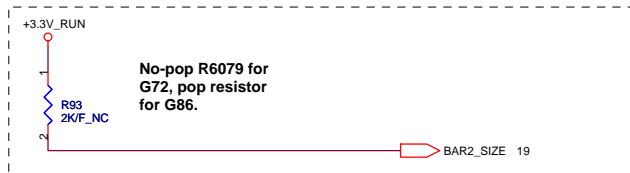
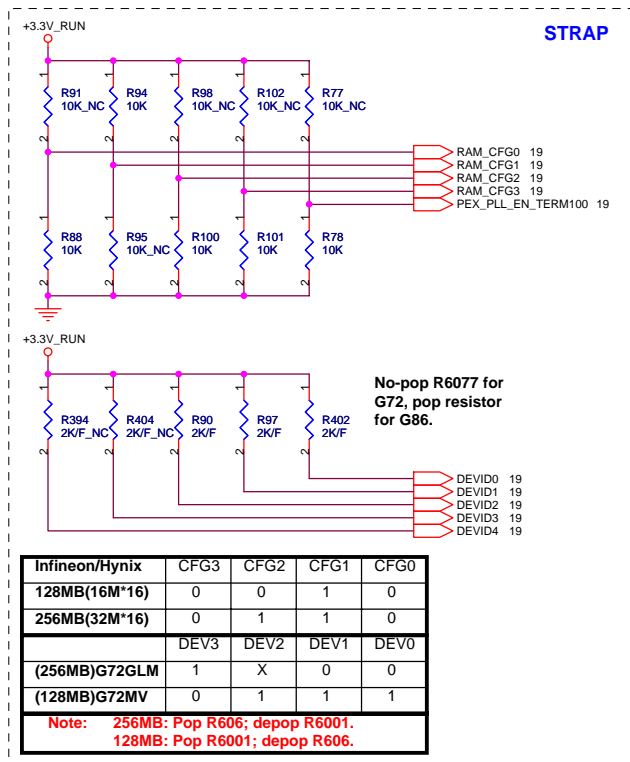
PCI_LOM = FCTSEL1

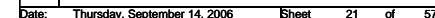
| FCTSEL1 (PIN34) | PIN43 | PIN44 | PIN47 | PIN48 |
|---------------------|--------|----------|-----------|-----------|
| 0=UMA | DOT96T | DOT96C | 96/100M_T | 96/100M_C |
| 1 = Disc. GRFX down | 27Mout | 27MSSout | SRCT0 | SRCC0 |



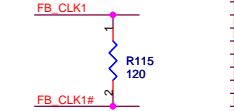
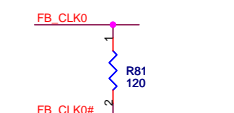
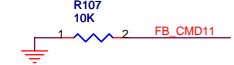
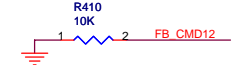




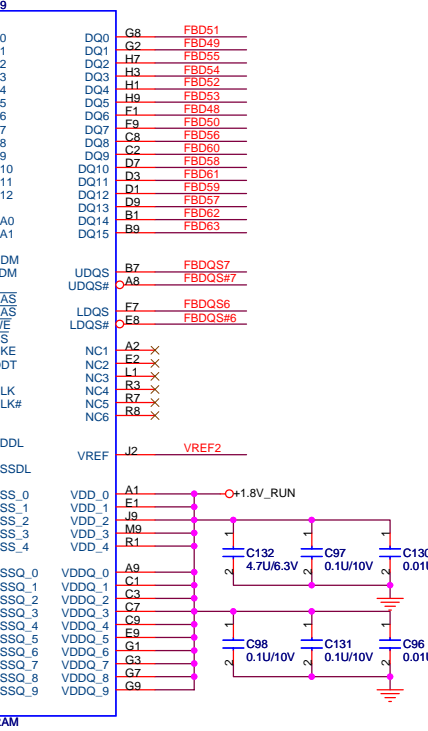
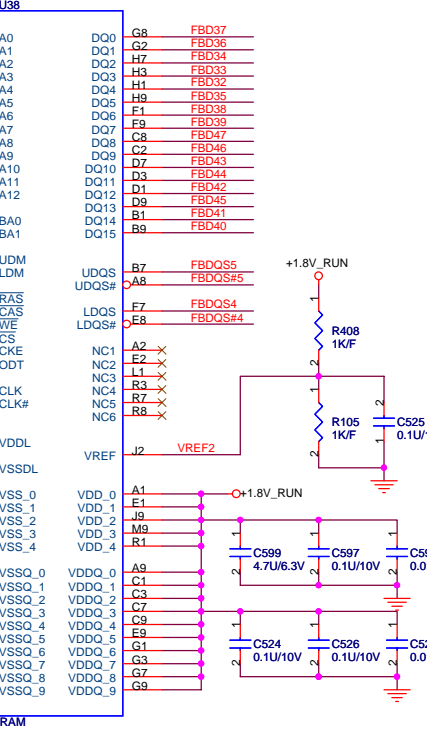
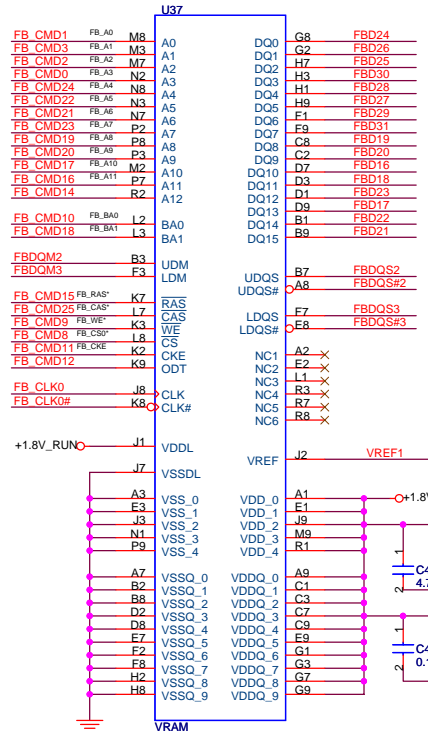
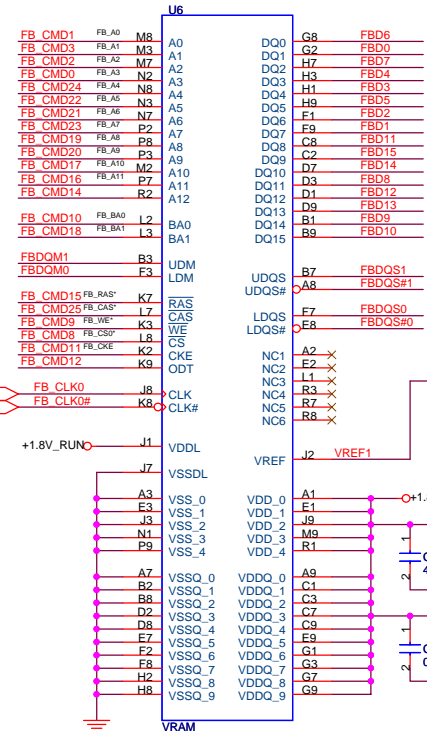
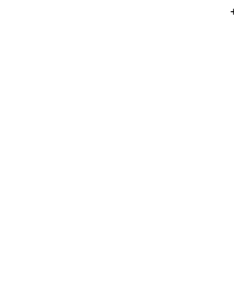


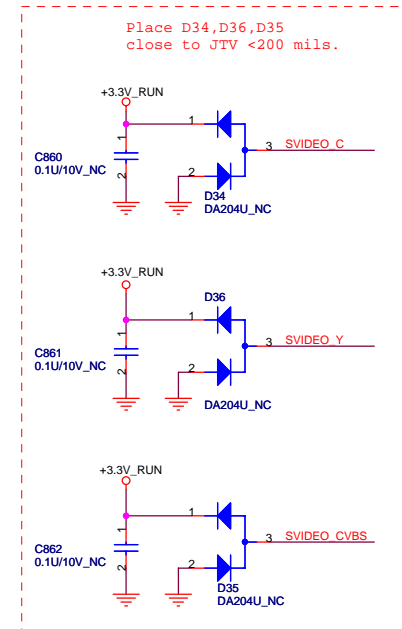
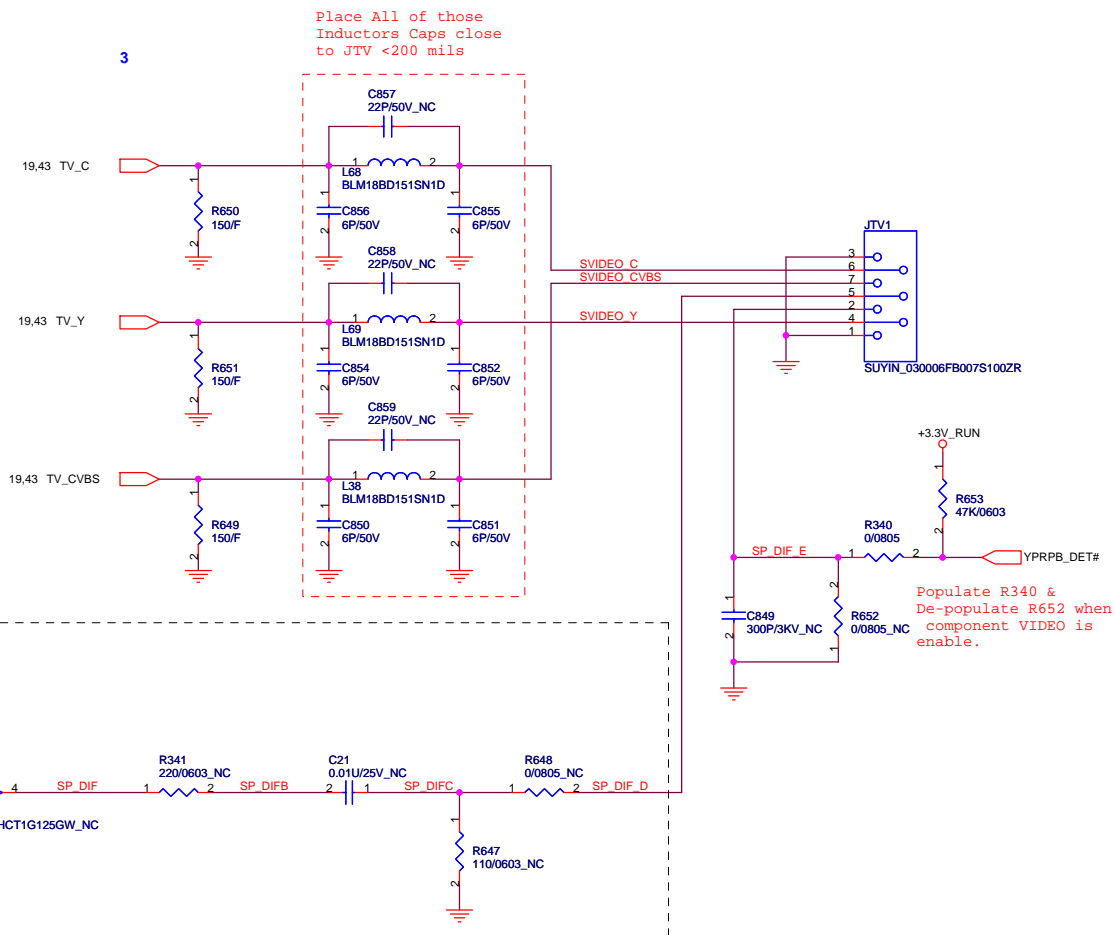


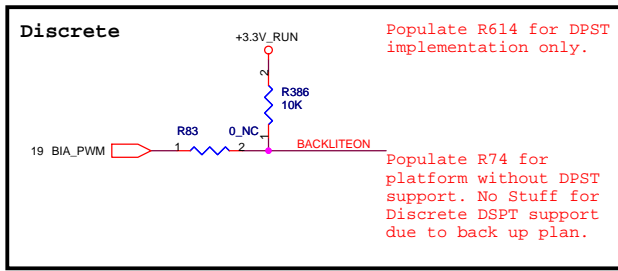
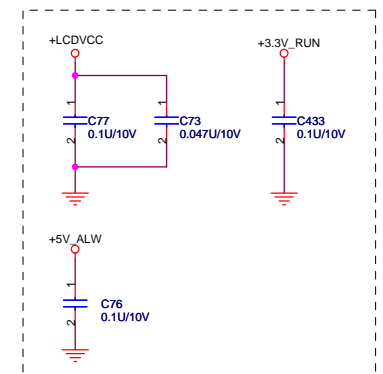
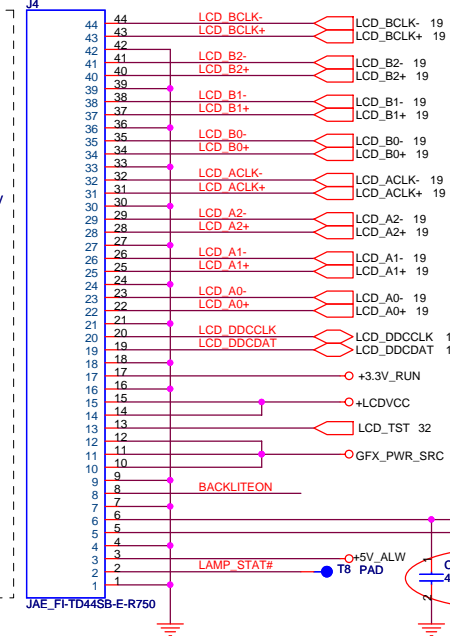
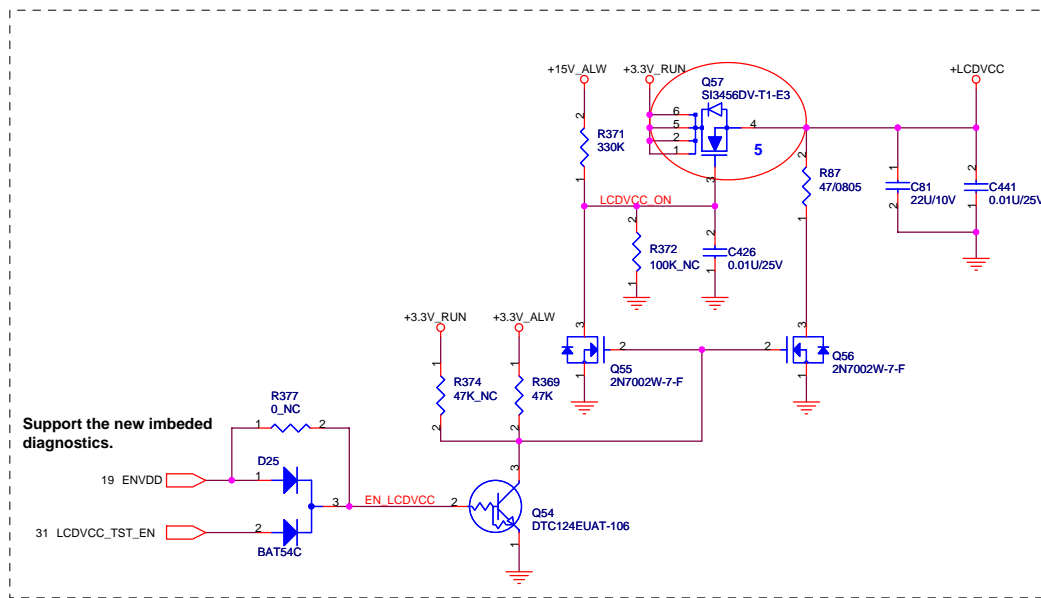
FB_CMD[0..26] 21
FBD[0..63] 21
FBDQM[0..7] 21
FBDQS[0..7] 21



21 FB_CLK1
21 FB_CLK1#

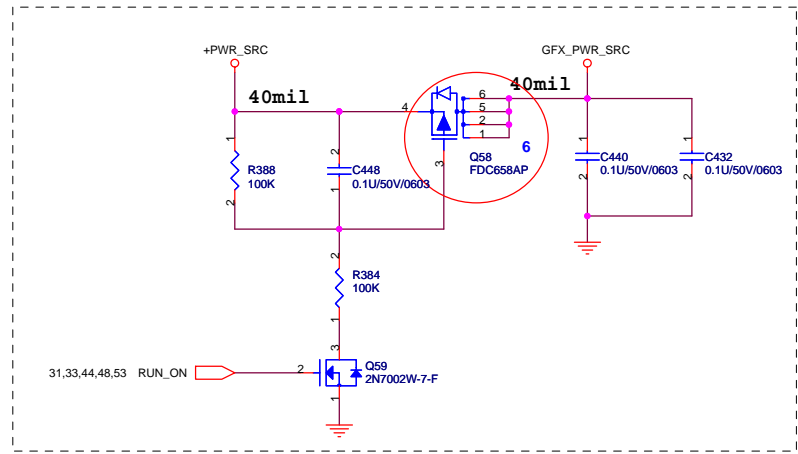






Shunt capacitors on LVDS for improving WWAN.

| | | | | | |
|-----------|------|---|---|-------------|-----------|
| LCD_B0- | C430 | 1 | 2 | 3.3P/50V_NC | LCD_B0+ |
| LCD_B1- | C434 | 1 | 2 | 3.3P/50V_NC | LCD_B1+ |
| LCD_B2- | C425 | 1 | 2 | 3.3P/50V_NC | LCD_B2+ |
| LCD_BCLK- | C63 | 1 | 2 | 3.3P/50V_NC | LCD_BCLK+ |
| LCD_A0- | C80 | 1 | 2 | 3.3P/50V_NC | LCD_A0+ |
| LCD_A1- | C71 | 1 | 2 | 3.3P/50V_NC | LCD_A1+ |
| LCD_A2- | C72 | 1 | 2 | 3.3P/50V_NC | LCD_A2+ |
| LCD_ACLK- | C57 | 1 | 2 | 3.3P/50V_NC | LCD_ACLK+ |



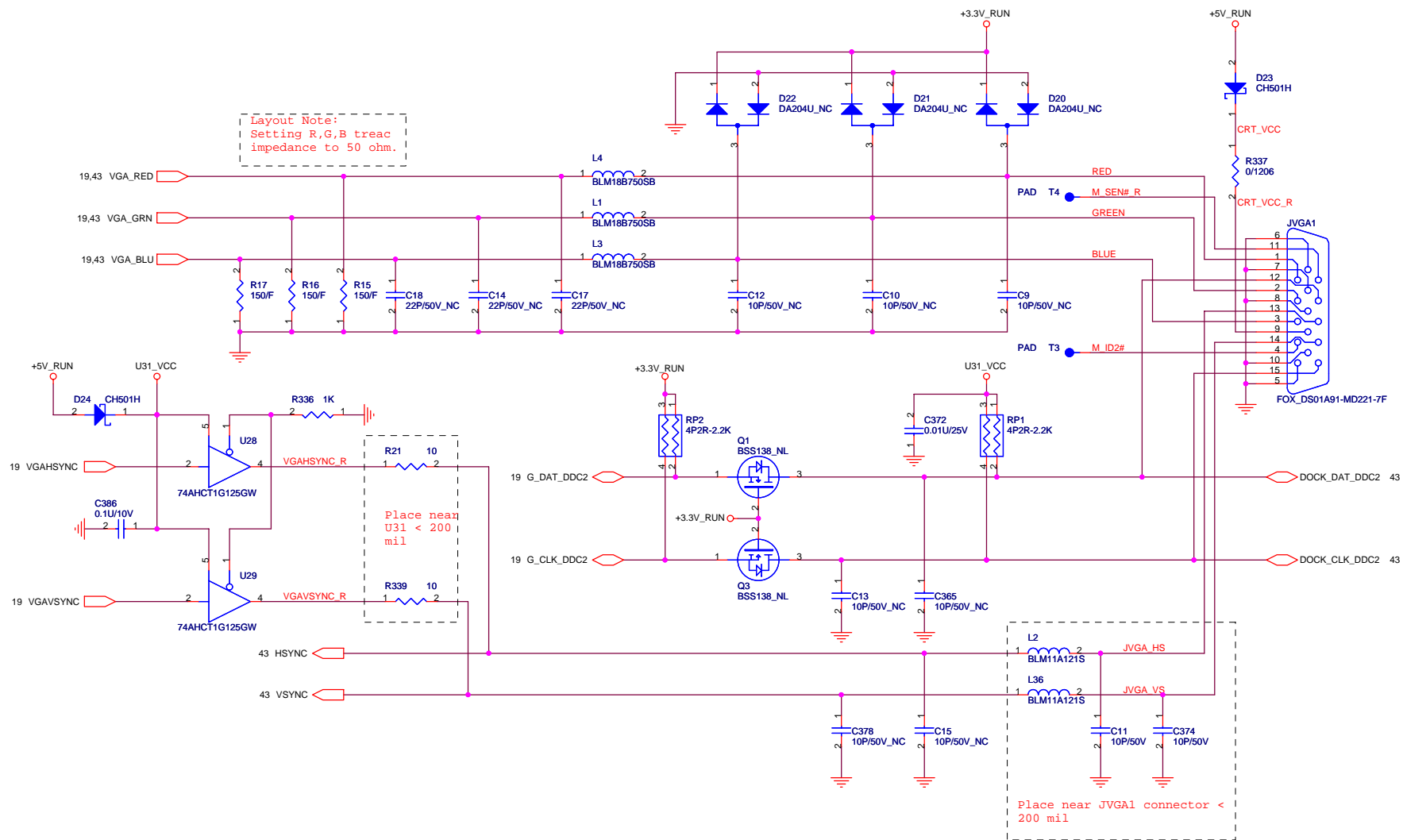


Diagram illustrating the SATA connector wiring for the MLX 67492-1821 component.

Component Labels:

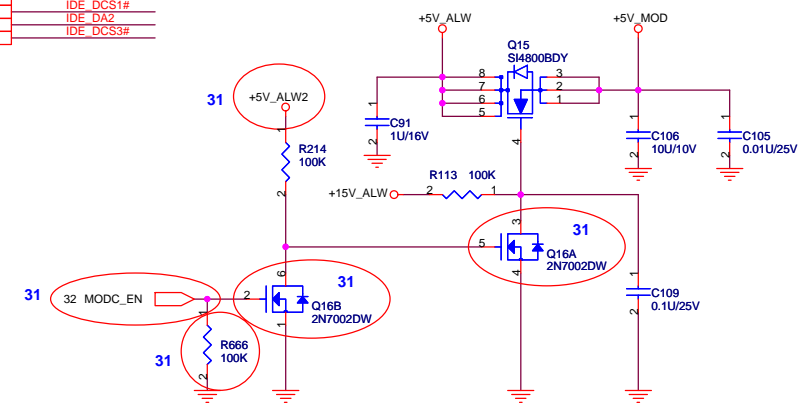
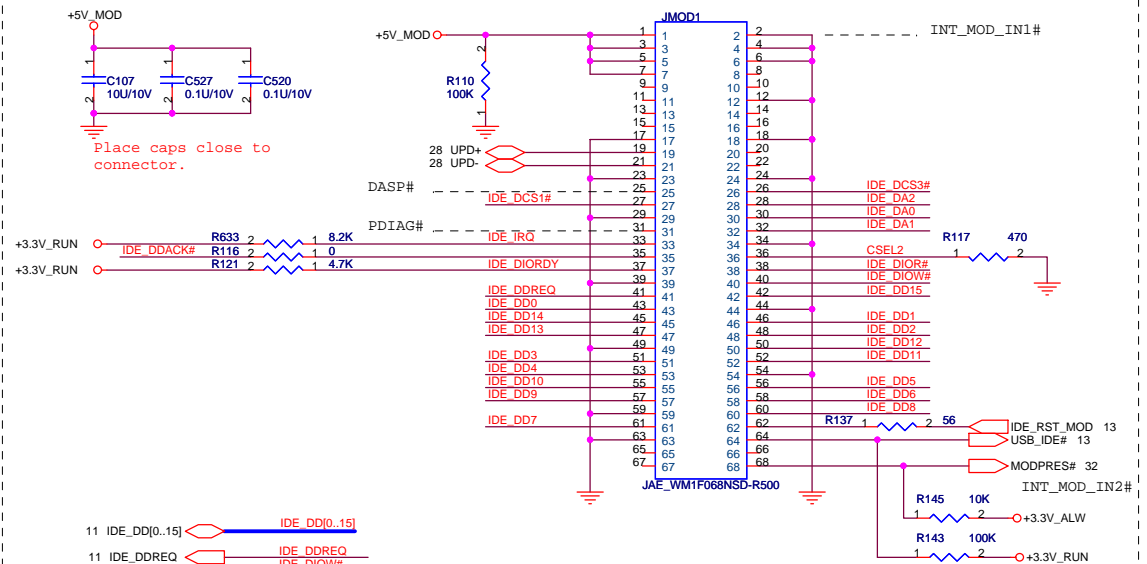
- SATA Pins:** GND1, RXP, RXN, GND2, TXN, TXP, GND3, 3.3V_0, 3.3V_1, 3.3V_2, GND4, GND5, GND6, 5V_0, 5V_1, 5V_2, GND7, RSVD, GND8, 12V_0, 12V_1, 12V_2.
- MLX 67492-1821 Pins:** 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22.

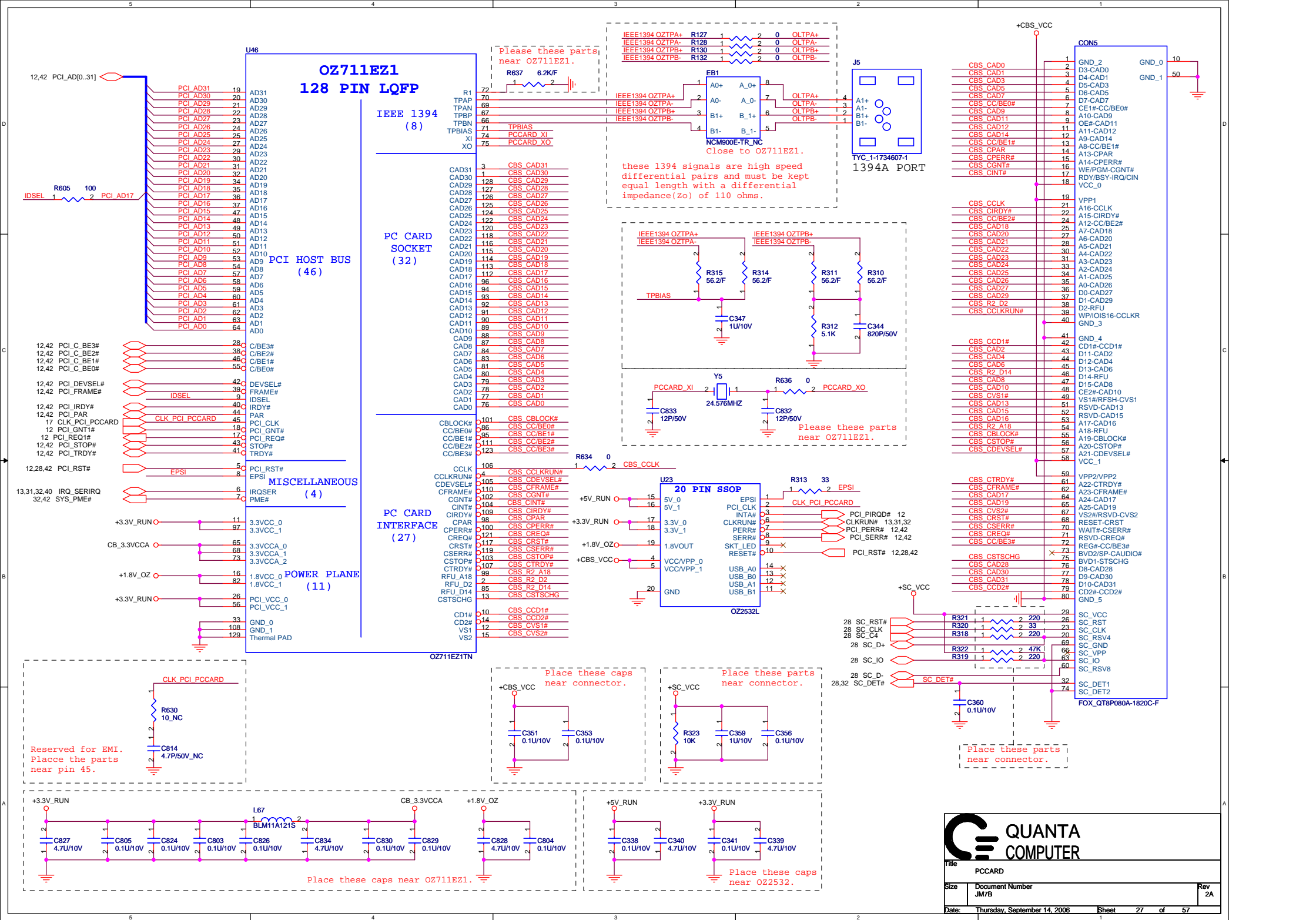
Connections:

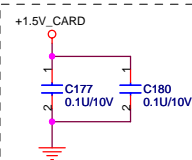
- SATA_TX0+ (Pin 1) connects to MLX pin 1.
- SATA_TX0- (Pin 11) connects to MLX pin 11.
- SATA_RXN0_C (Pin 2) connects to MLX pin 2.
- SATA_RXP0_C (Pin 6) connects to MLX pin 6.
- 3.3V_RUN (Pin 8) connects to MLX pin 8.
- 5V_HDD (Pin 14) connects to MLX pin 14.
- MLX pin 18 connects to MLX pin 19.

Additional Notes:

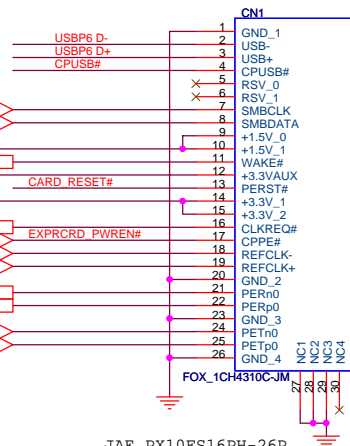
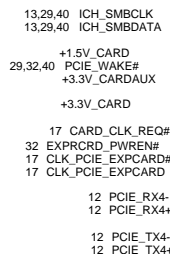
- Place caps close to connector.
- Capacitors: C357 (0.1u/10V_NC), C358 (1000P/50V_NC).
- Resistors: 3900P/25V (connected to MLX pins 2 and 6).







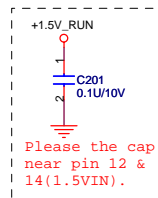
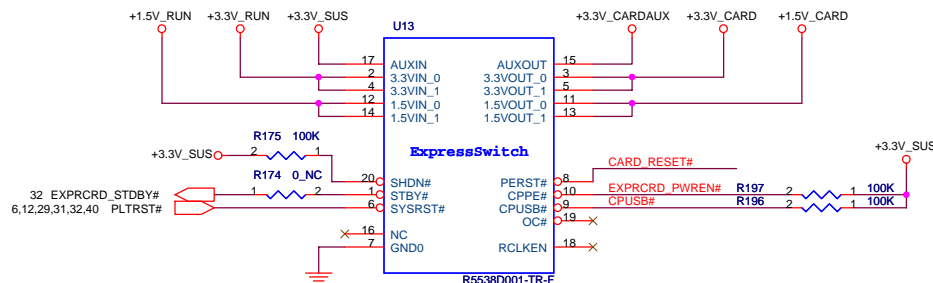
Please the cap
near connector.



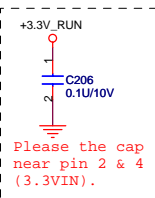
JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector.

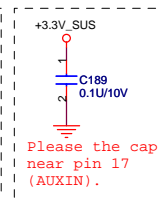
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



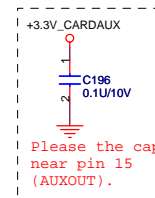
Please the cap
near pin 12 &
14(1.5VIN).



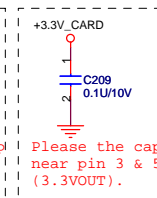
Please the cap near pin 2 & 4 ($3.3V_{IN}$).



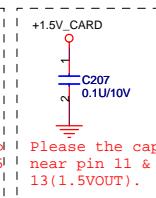
Please the cap
near pin 17
(AUXIN).



Please the cap
near pin 15
(AUXOUT).

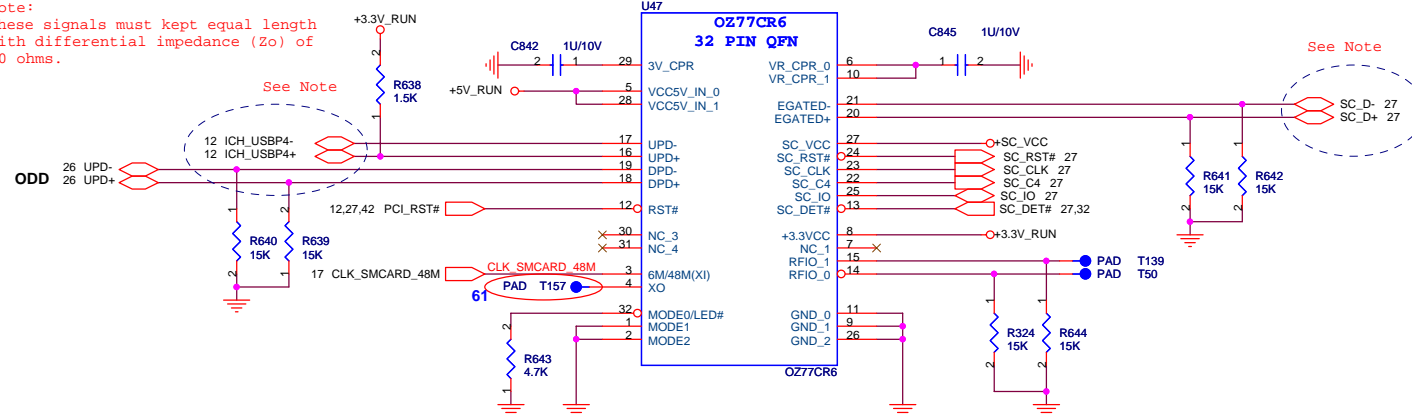


Please the cap near pin 3 & 5 (3.3VOUT).

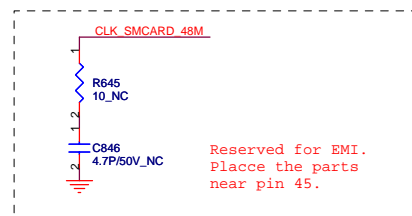


Please the cap near pin 11 & 13(1.5VOUT).

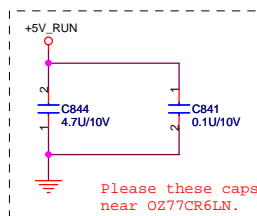
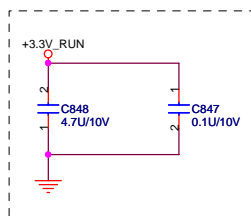
Note:
These signals must kept equal length
with differential impedance (Z_0) of
90 ohms.



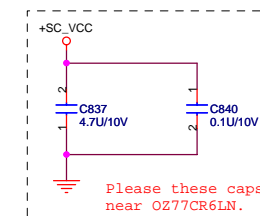
See Note



Reserved for EMI.
Place the parts
near pin 45.



Please these ca
near OZ77CR6LN.



Please these ca
near OZ77CR6LN.



Title ExpressCard/SmartCard

| Size | Docum |
|------|-------|
|------|-------|

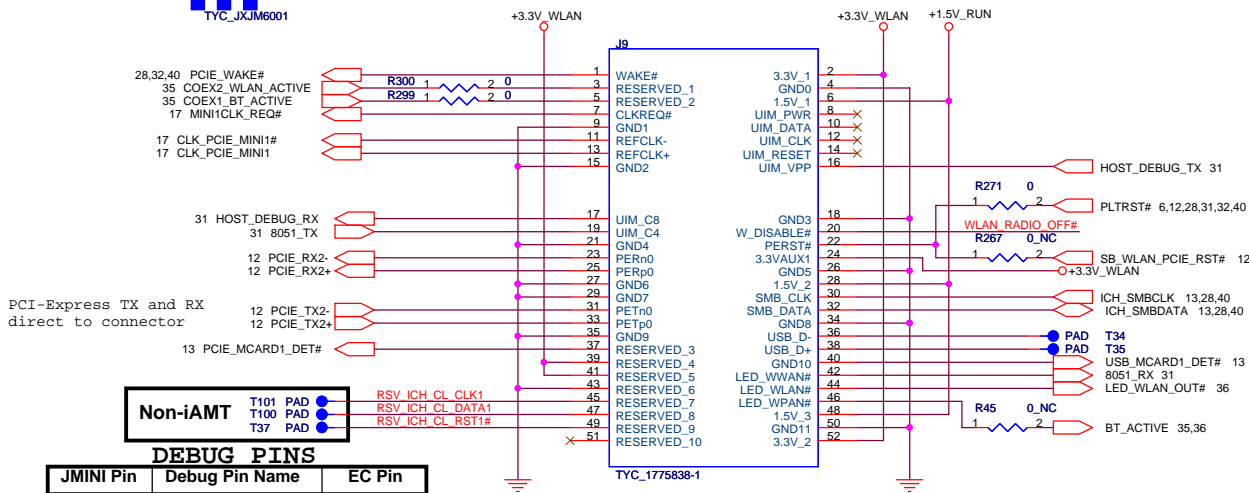
ment Number

Rev

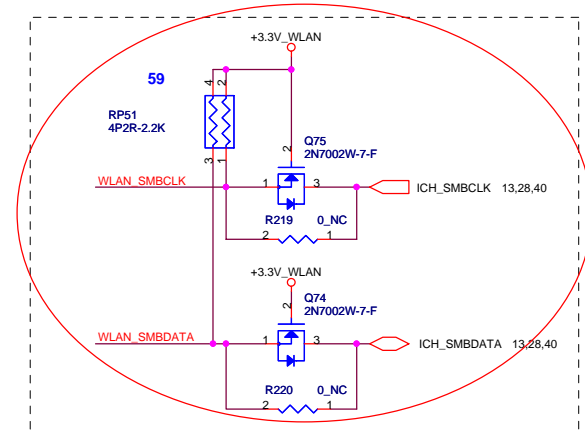
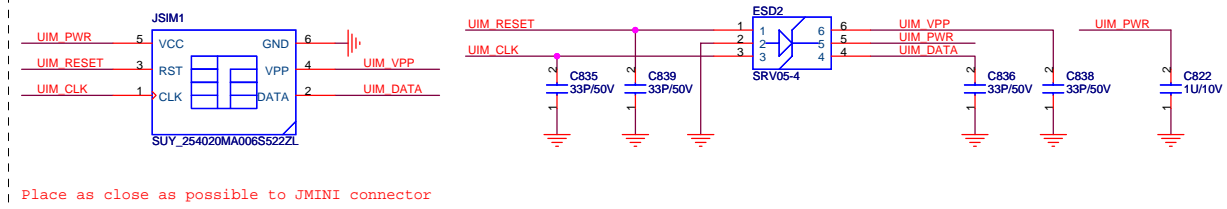
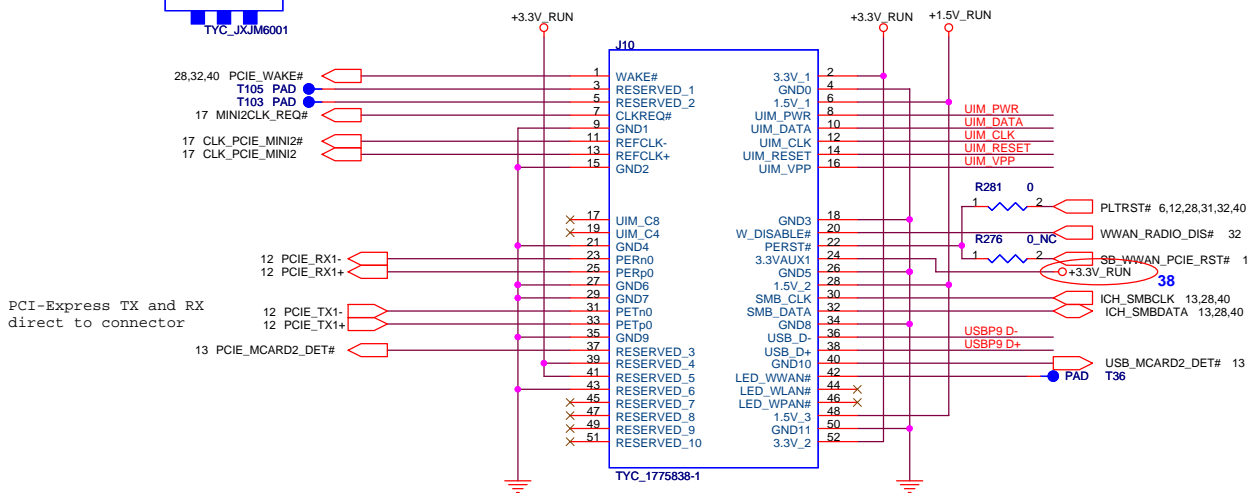
Date: Thursday, September 14, 2006

Sheet 28 of 57

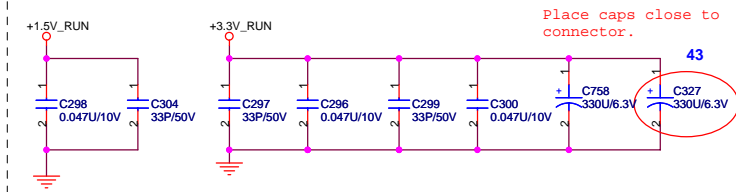
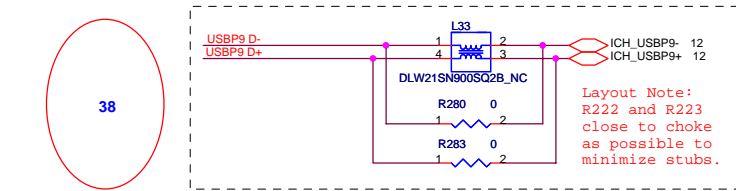
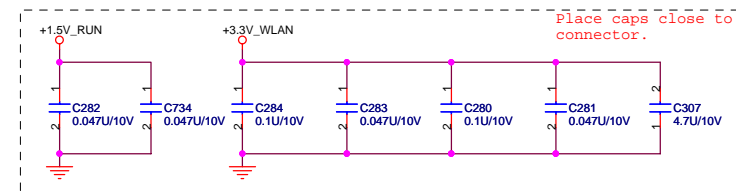
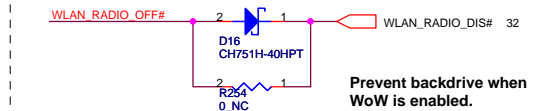
MiniCard WLAN connector

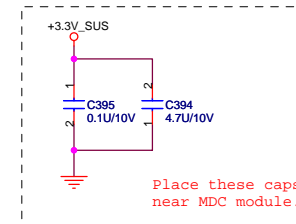
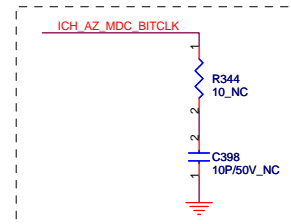
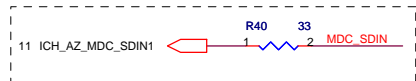
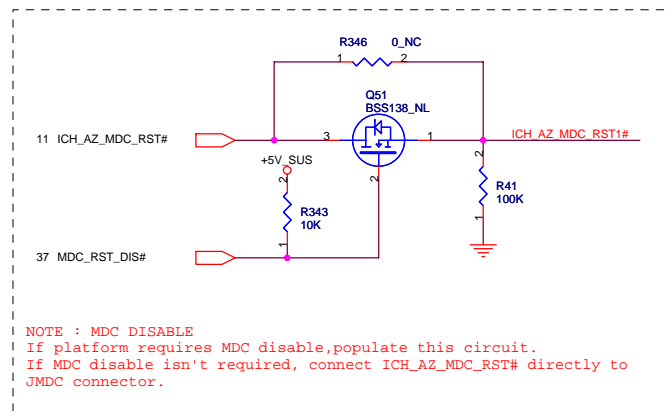
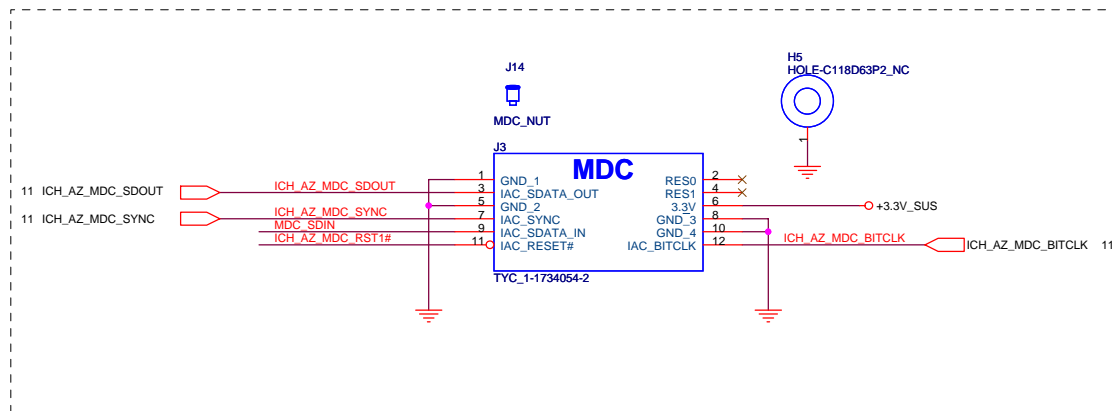
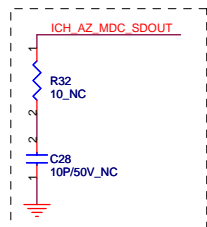
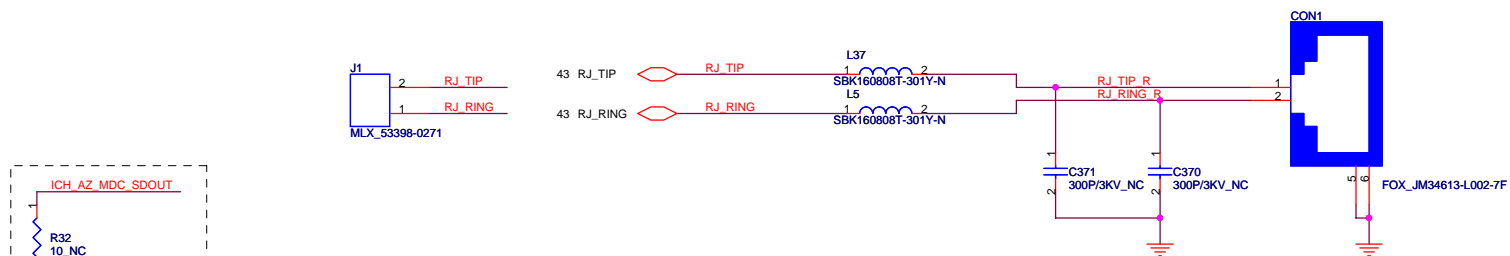


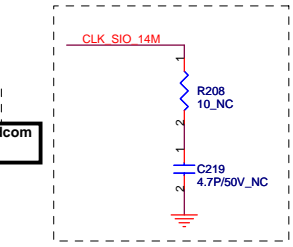
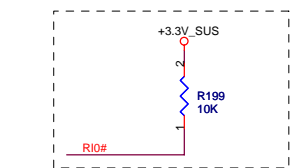
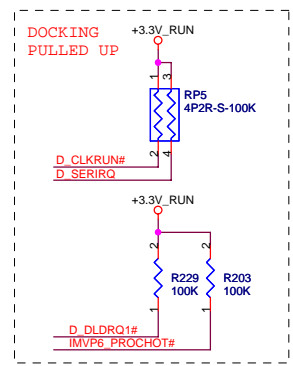
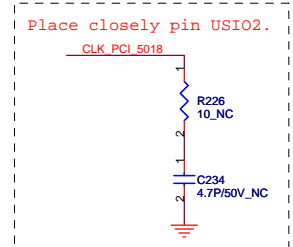
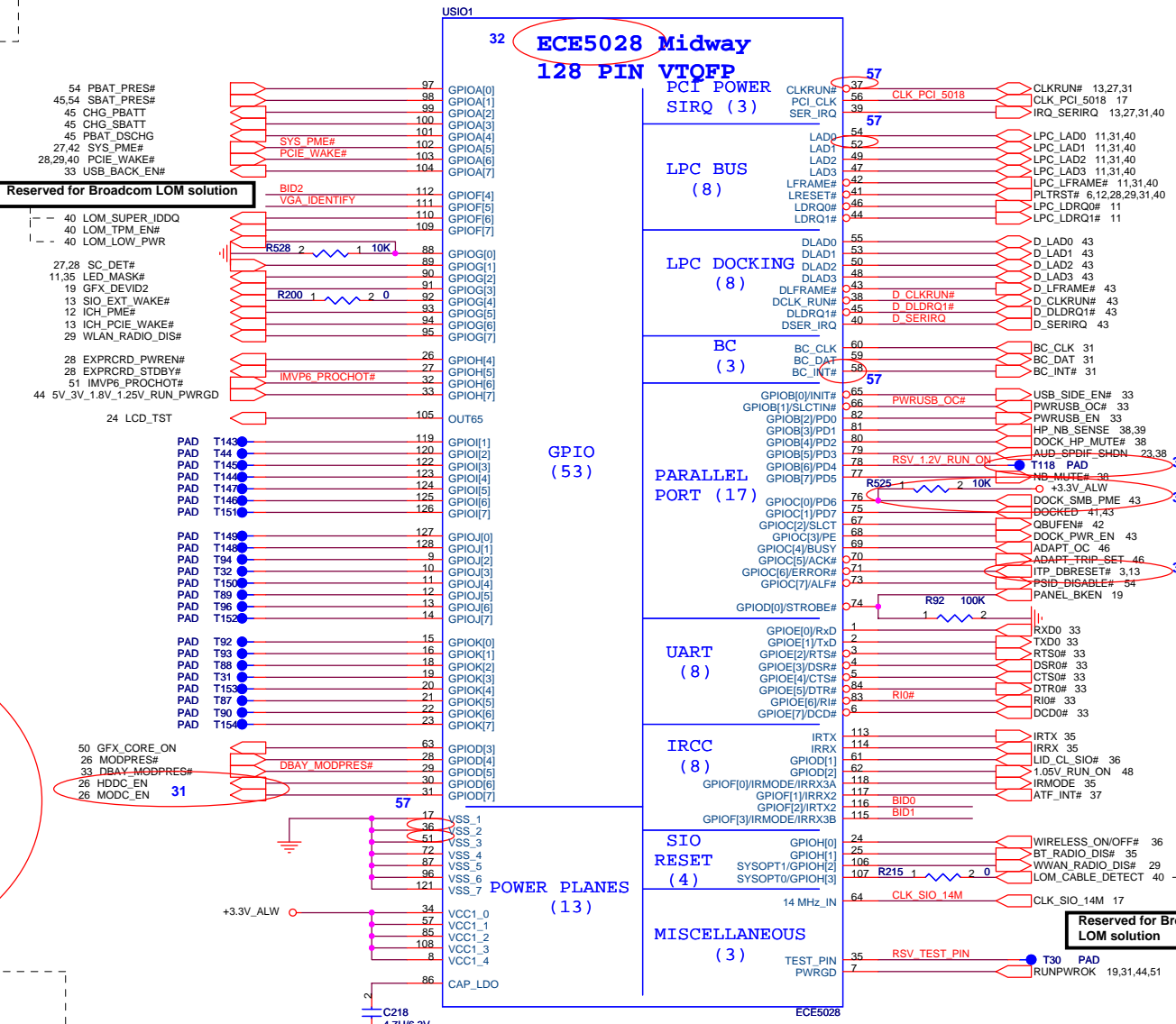
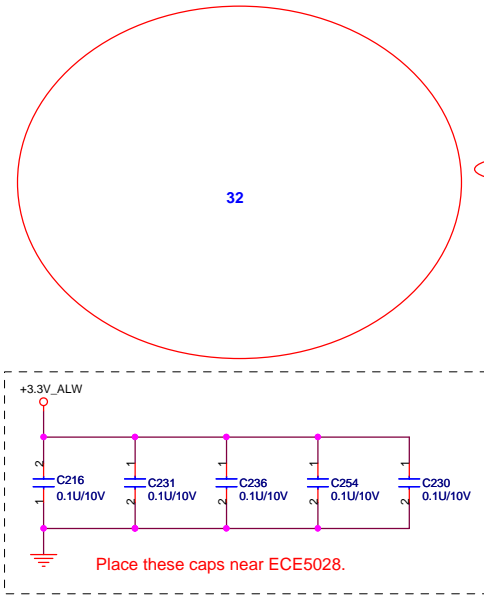
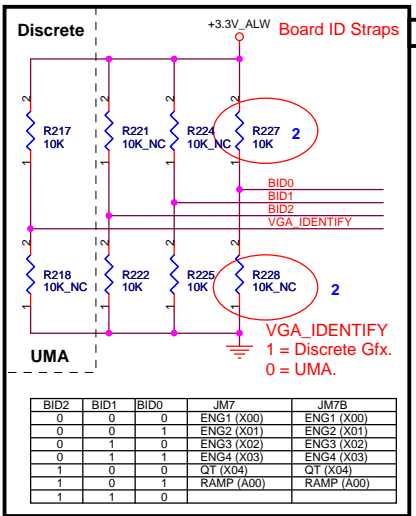
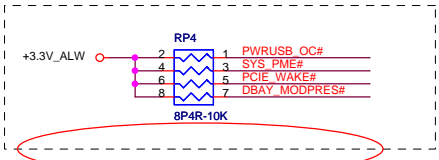
MiniCard WWAN connector



Support for WoW







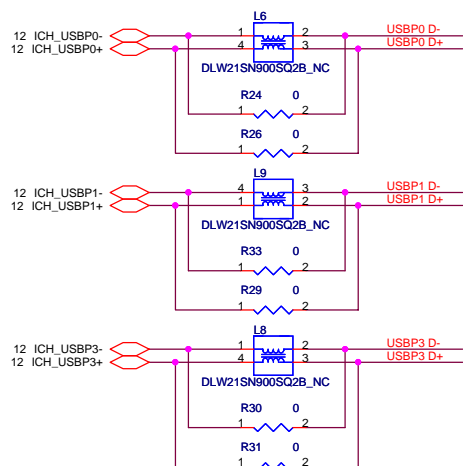
QUANTA COMPUTER

Title: Ultra I/O Controller ECE5028

Size: Document Number JM7B Rev 2A

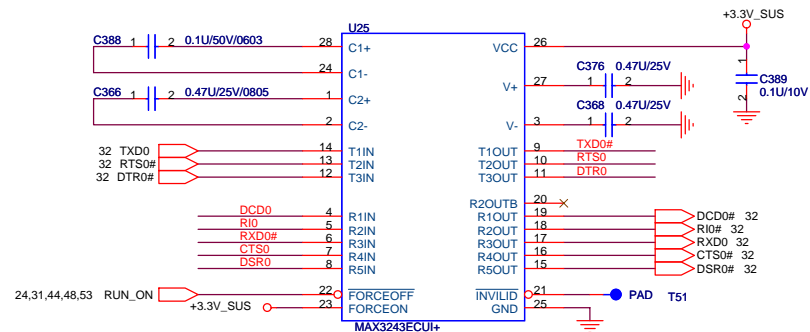
Date: Thursday, September 14, 2006 Sheet 32 of 57

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

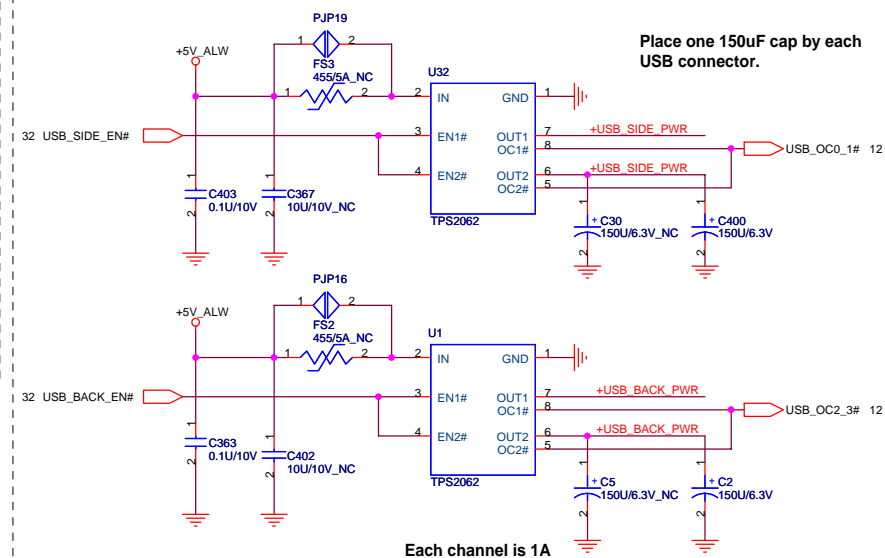
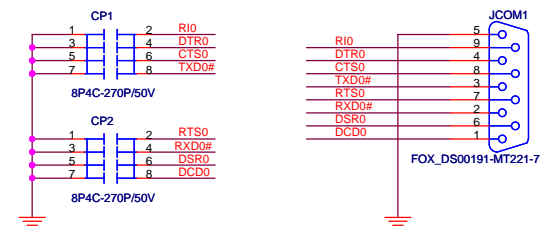


3

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

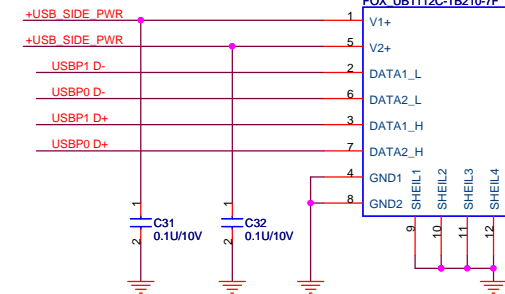


Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



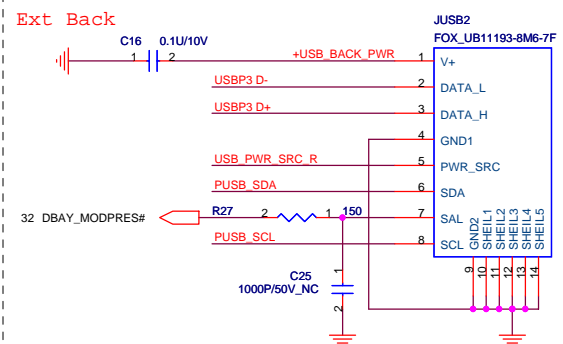
Each channel is 1A

Ext Side

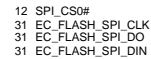


3

Ext Back



Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the
MEC5025.

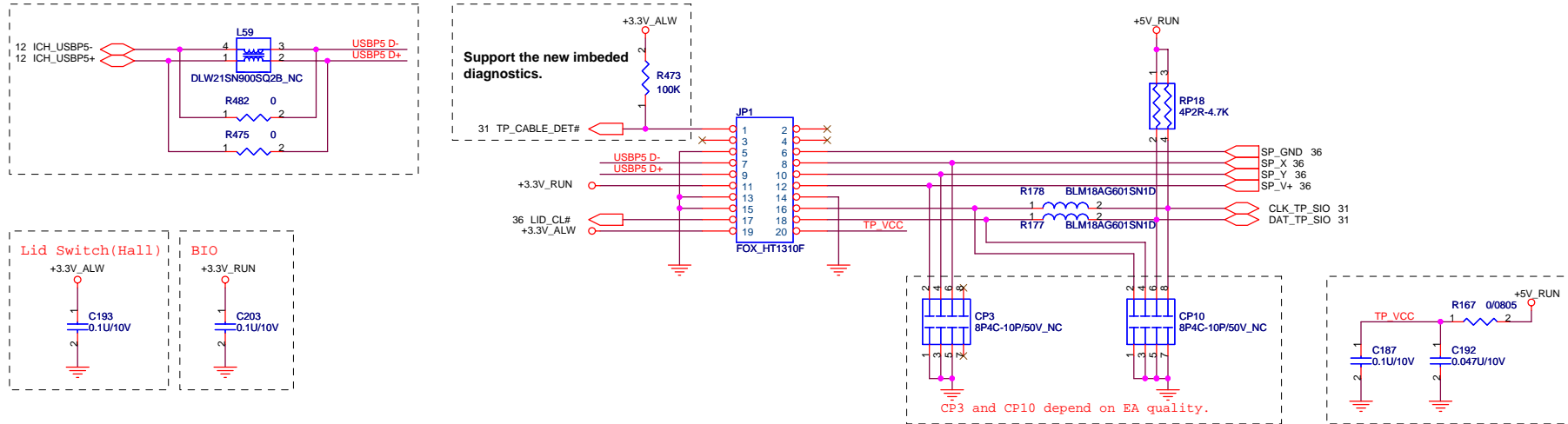
[illegible]

Document Number
JM7B

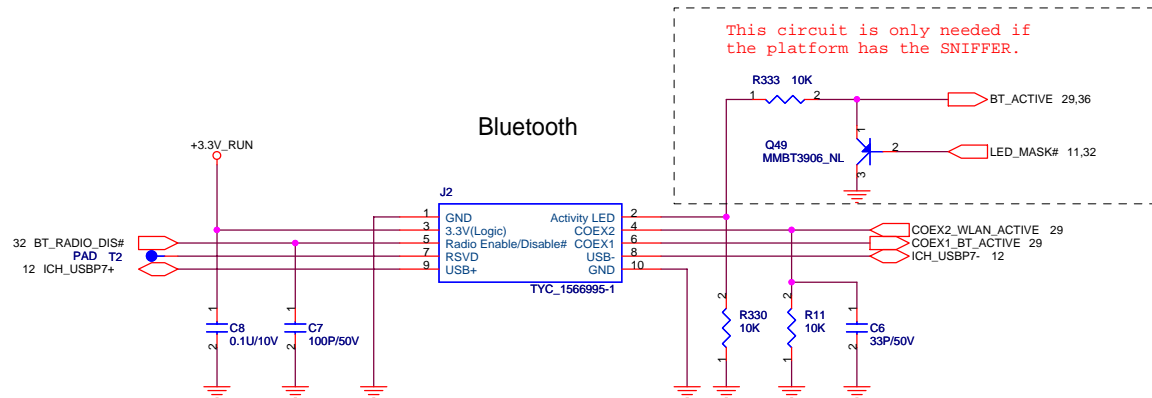
Sheet 34 of 57

Rev
2A

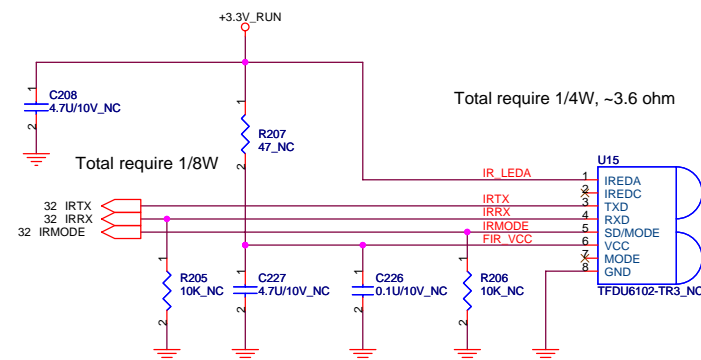
Touch Pad



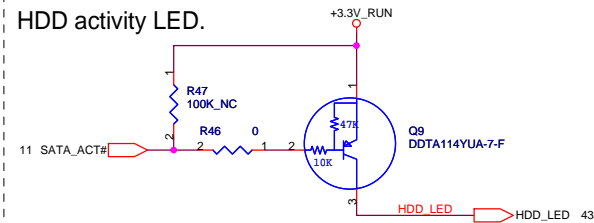
Bluetooth



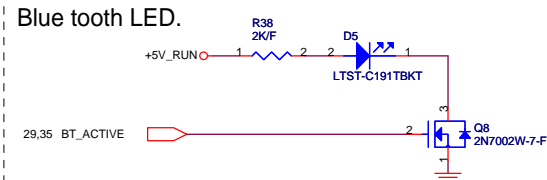
FIR



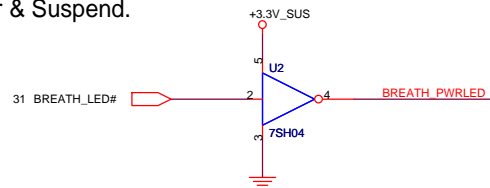
HDD activity LED.



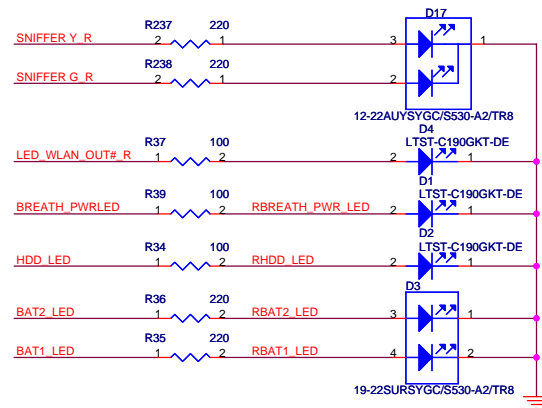
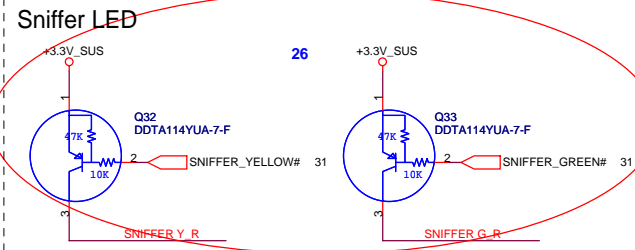
Blue tooth LED.



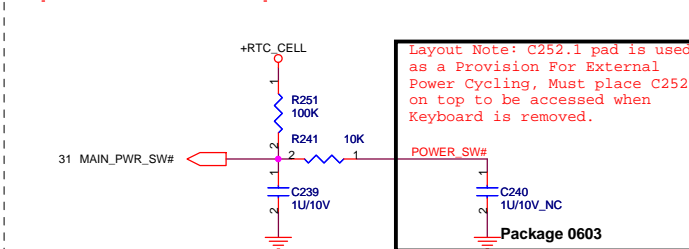
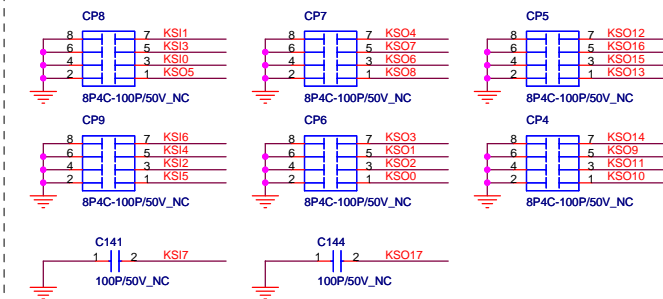
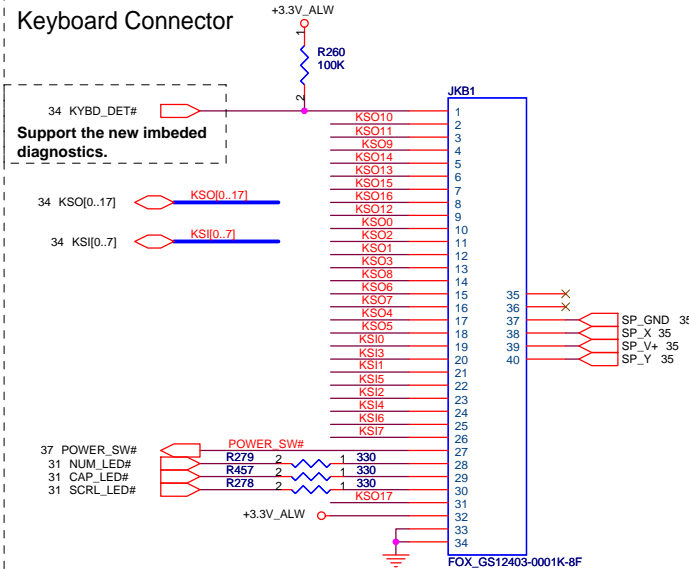
Power & Suspend.



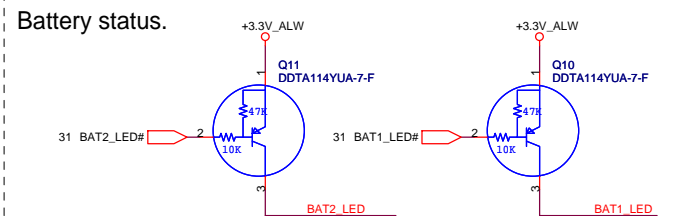
Sniffer LED



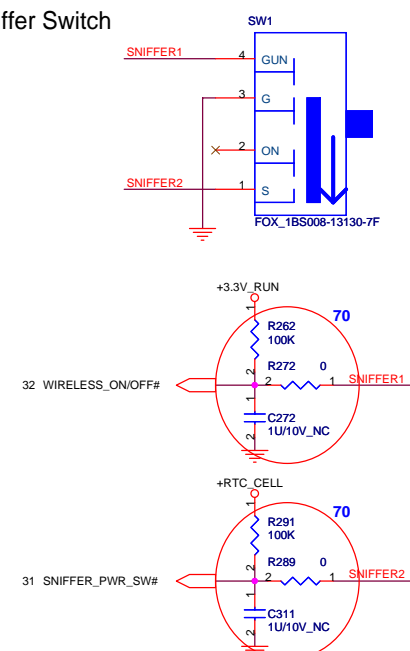
Keyboard Connector



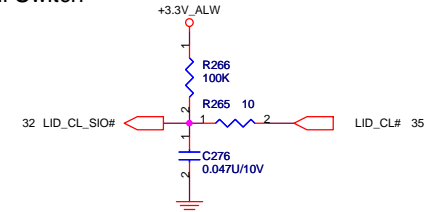
Battery status.



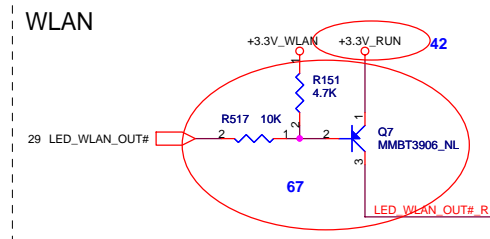
Sniffer Switch



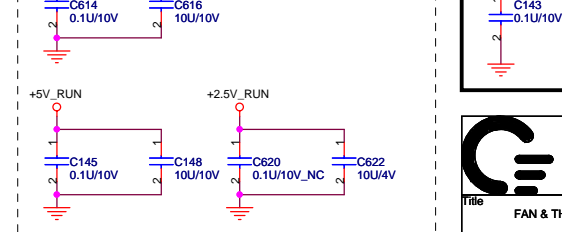
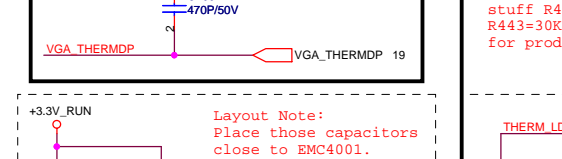
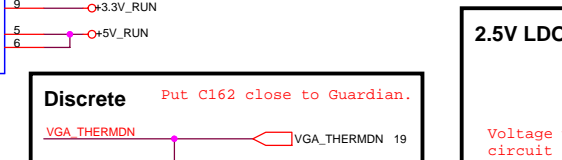
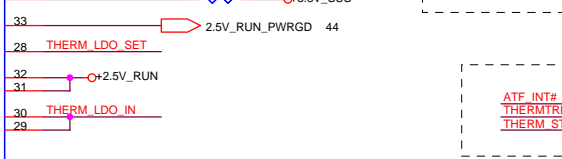
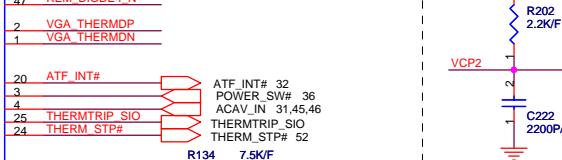
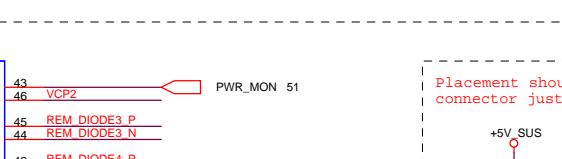
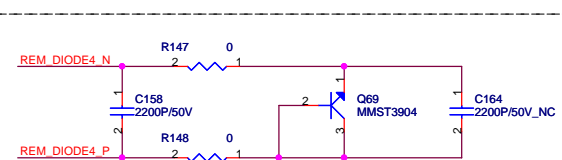
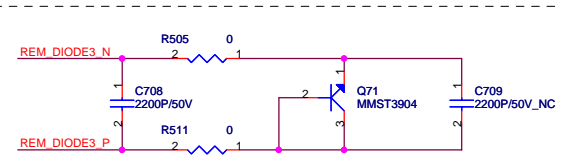
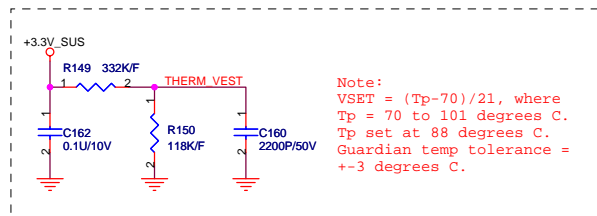
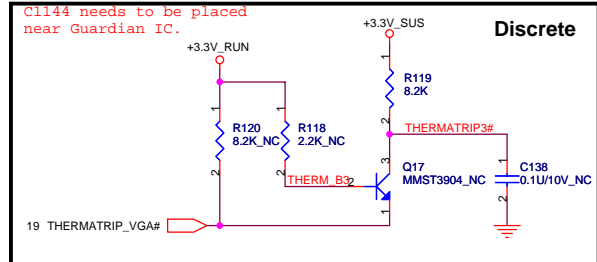
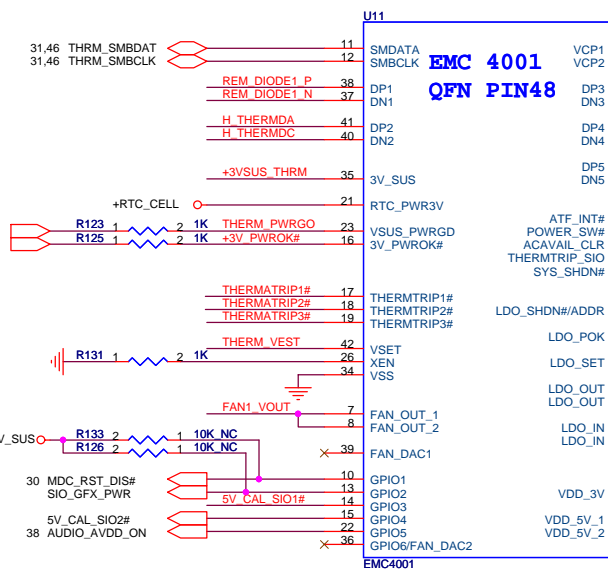
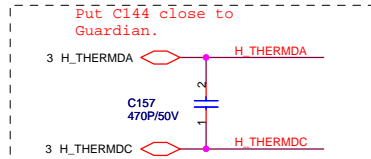
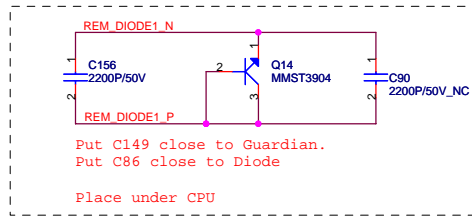
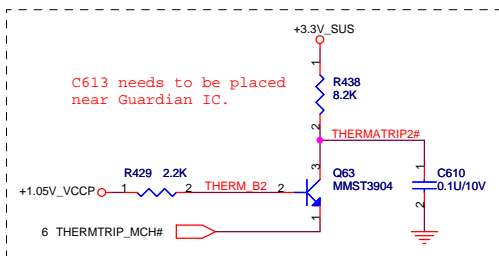
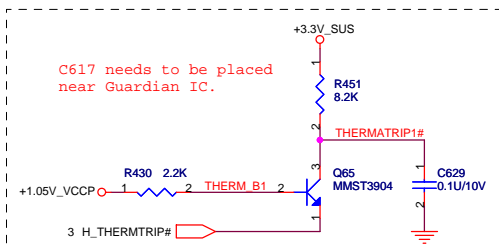
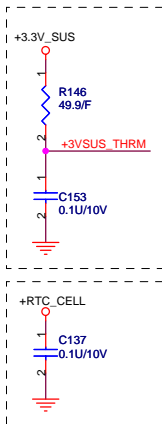
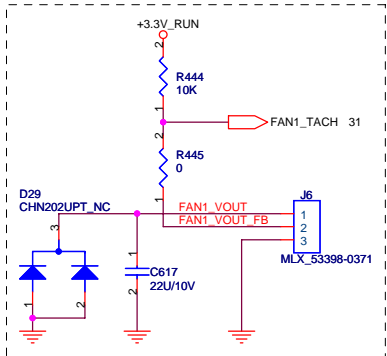
Hall Switch



WLAN



| | | | |
|-------|------------------------------|-------|------------------------|
| Title | | | SWITCH, KEYBOARD & LED |
| Size | Document Number | Rev | |
| | JM7B | 2A | |
| Date: | Thursday, September 14, 2006 | Sheet | 36 of 57 |



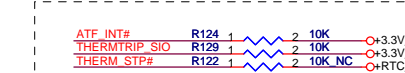
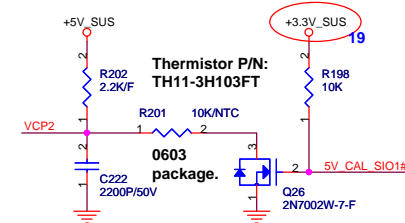
Put C162,R580 & R581 as close as possible to Guardian.
Put C690 close to Diode.

Place near the bottom SODIMM

Put C172,R582 & R583 as close as possible to Guardian.
Put C714 close to Diode.

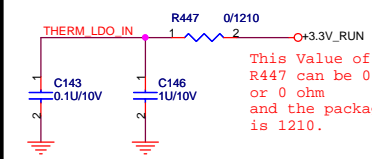
Placement should be on bottom side of MB, located within triangle of CPU/MCH/DRAM

Placement should be near the WWAN minicard connector just under the inserted minicard.



2.5V LDO

Voltage margining circuit for LDO output. For Vmargin stuff R441 and R443=30K. R443=1K for production.



INTERNAL SPEAKER AMP

Package 1206 For THD+N performance and Vista Logo requirements.

X7R

AUD LINE OUT L C334 1 2 0.033U/200V
AUD LINE OUT R C291 1 2 0.033U/200V
AUD HP OUT L C768 2 1 2.2U/25V
AUD HP OUT R C751 2 1 2.2U/25V

21

C753

47P/50V_NC

C764

47P/50V_NC

C288

47P/50V_NC

C323

47P/50V_NC

C308

1U/10V

T106 PAD

C309

10U/10V_NC

C303

1U/10V

C255

1U/16V

C256

1U/16V

C257

1U/16V

C258

1U/16V

C259

1U/16V

C260

1U/16V

C261

10U/10V_NC

C262

10U/10V_NC

C263

10U/10V_NC

C264

10U/10V_NC

C265

10U/10V_NC

C266

10U/10V_NC

C267

10U/10V_NC

C268

10U/10V_NC

C269

10U/10V_NC

C270

10U/10V_NC

C271

10U/10V_NC

C272

10U/10V_NC

C273

10U/10V_NC

C274

10U/10V_NC

C275

10U/10V_NC

C276

10U/10V_NC

C277

10U/10V_NC

C278

10U/10V_NC

C279

10U/10V_NC

C280

10U/10V_NC

C281

10U/10V_NC

C282

10U/10V_NC

C283

10U/10V_NC

C284

10U/10V_NC

C285

10U/10V_NC

C286

10U/10V_NC

C287

10U/10V_NC

C288

10U/10V_NC

C289

10U/10V_NC

C290

10U/10V_NC

C291

10U/10V_NC

C292

10U/10V_NC

C293

10U/10V_NC

C294

10U/10V_NC

C295

10U/10V_NC

C296

10U/10V_NC

C297

10U/10V_NC

C298

10U/10V_NC

C299

10U/10V_NC

C300

10U/10V_NC

C301

10U/10V_NC

C302

10U/10V_NC

C303

10U/10V_NC

C304

10U/10V_NC

C305

10U/10V_NC

C306

10U/10V_NC

C307

10U/10V_NC

C308

10U/10V_NC

C309

10U/10V_NC

C310

10U/10V_NC

C311

10U/10V_NC

C312

10U/10V_NC

C313

10U/10V_NC

C314

10U/10V_NC

C315

10U/10V_NC

C316

10U/10V_NC

C317

10U/10V_NC

C318

10U/10V_NC

C319

10U/10V_NC

C320

10U/10V_NC

C321

10U/10V_NC

C322

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C323

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C324

10U/10V_NC

C325

10U/10V_NC

C326

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C327

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C328

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C329

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C330

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C331

10U/10V_NC

C332

10U/10V_NC

C333

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C334

10U/10V_NC

C335

10U/10V_NC

C336

10U/10V_NC

C337

10U/10V_NC

C338

10U/10V_NC

C339

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C340

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C351

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C353

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C354

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C355

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C356

10U/10V_NC

C357

10U/10V_NC

C358

10U/10V_NC

C359

10U/10V_NC

C360

10U/10V_NC

C361

10U/10V_NC

C362

10U/10V_NC

C363

10U/10V_NC

C364

10U/10V_NC

C365

10U/10V_NC

C366

10U/10V_NC

C367

10U/10V_NC

C368

10U/10V_NC

C369

10U/10V_NC

C370

10U/10V_NC

C371

10U/10V_NC

C372

10U/10V_NC

C373

10U/10V_NC

C374

10U/10V_NC

C375

10U/10V_NC

C376

10U/10V_NC

C377

10U/10V_NC

C378

10U/10V_NC

C379

10U/10V_NC

C380

10U/10V_NC

C381

10U/10V_NC

C382

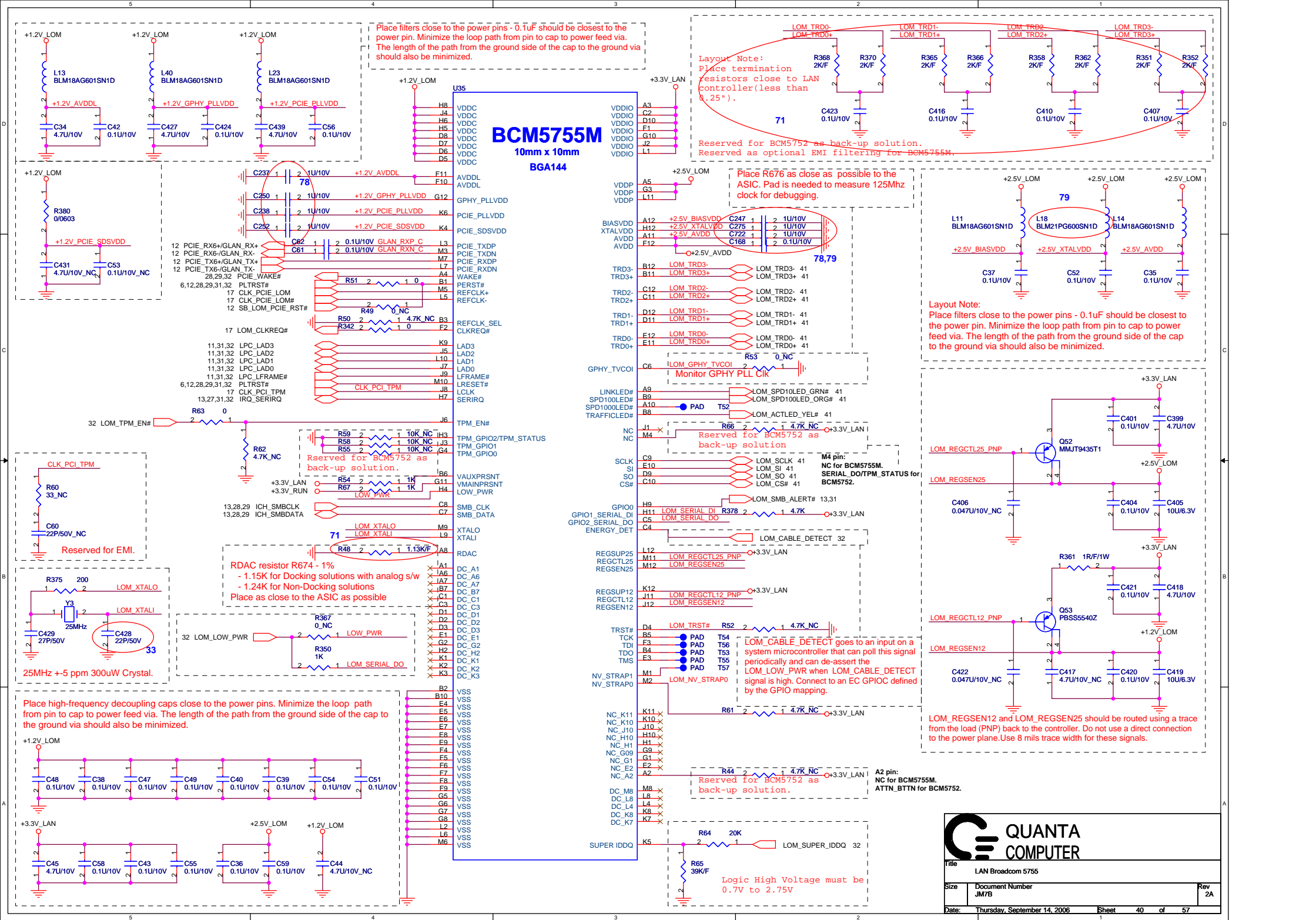
10U/10V_NC

C383

10U/10V_NC

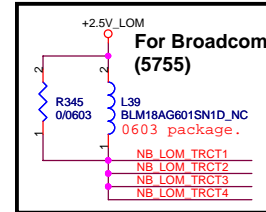
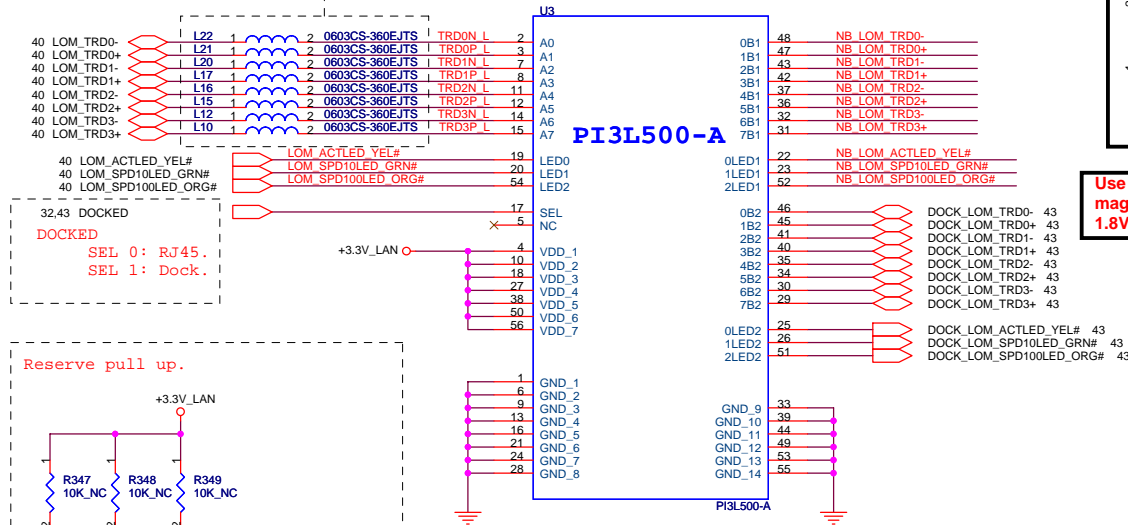
C384

10U/10V_NC

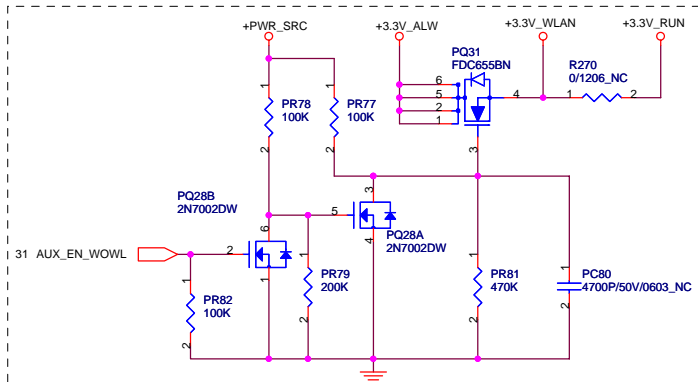
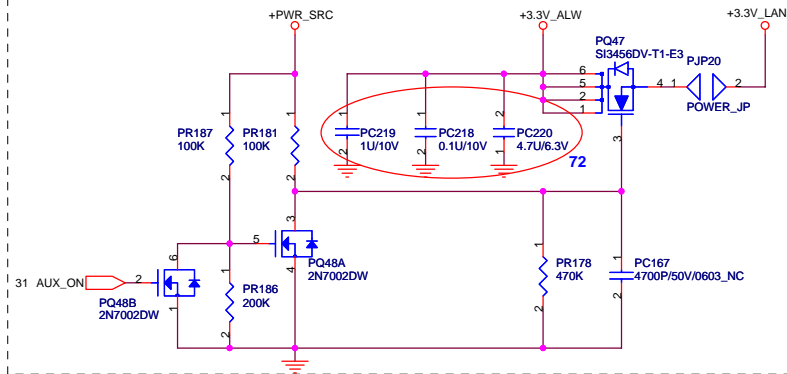
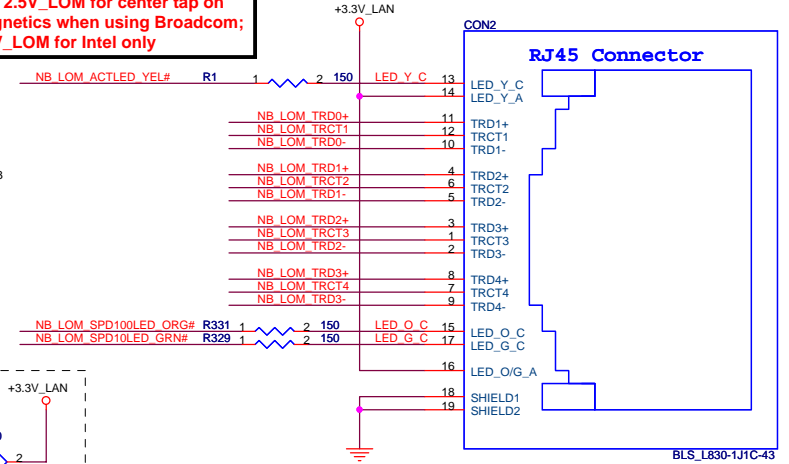
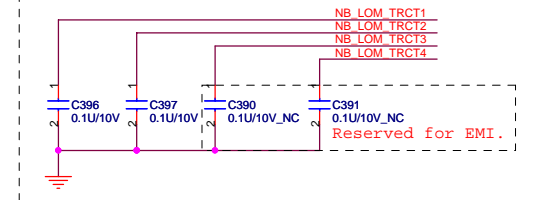


TRANSFORM+RJ45

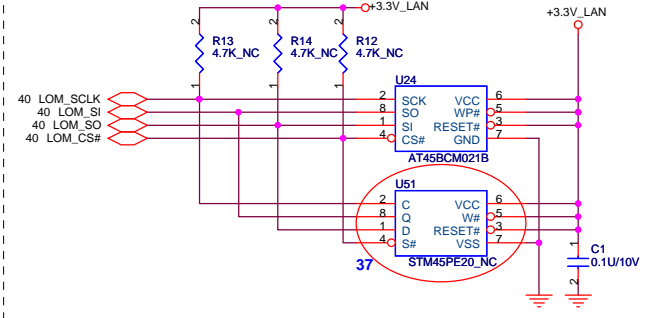
36nH is a suggested value.
Actual value will be system dependent.
Must use 0603 package for lower DC resistance.

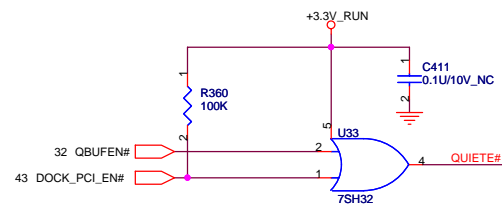
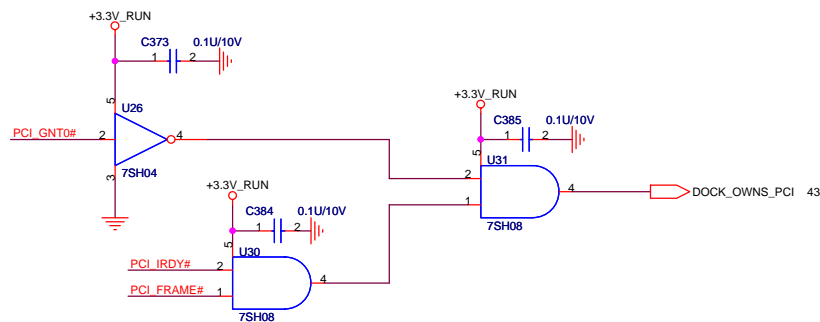
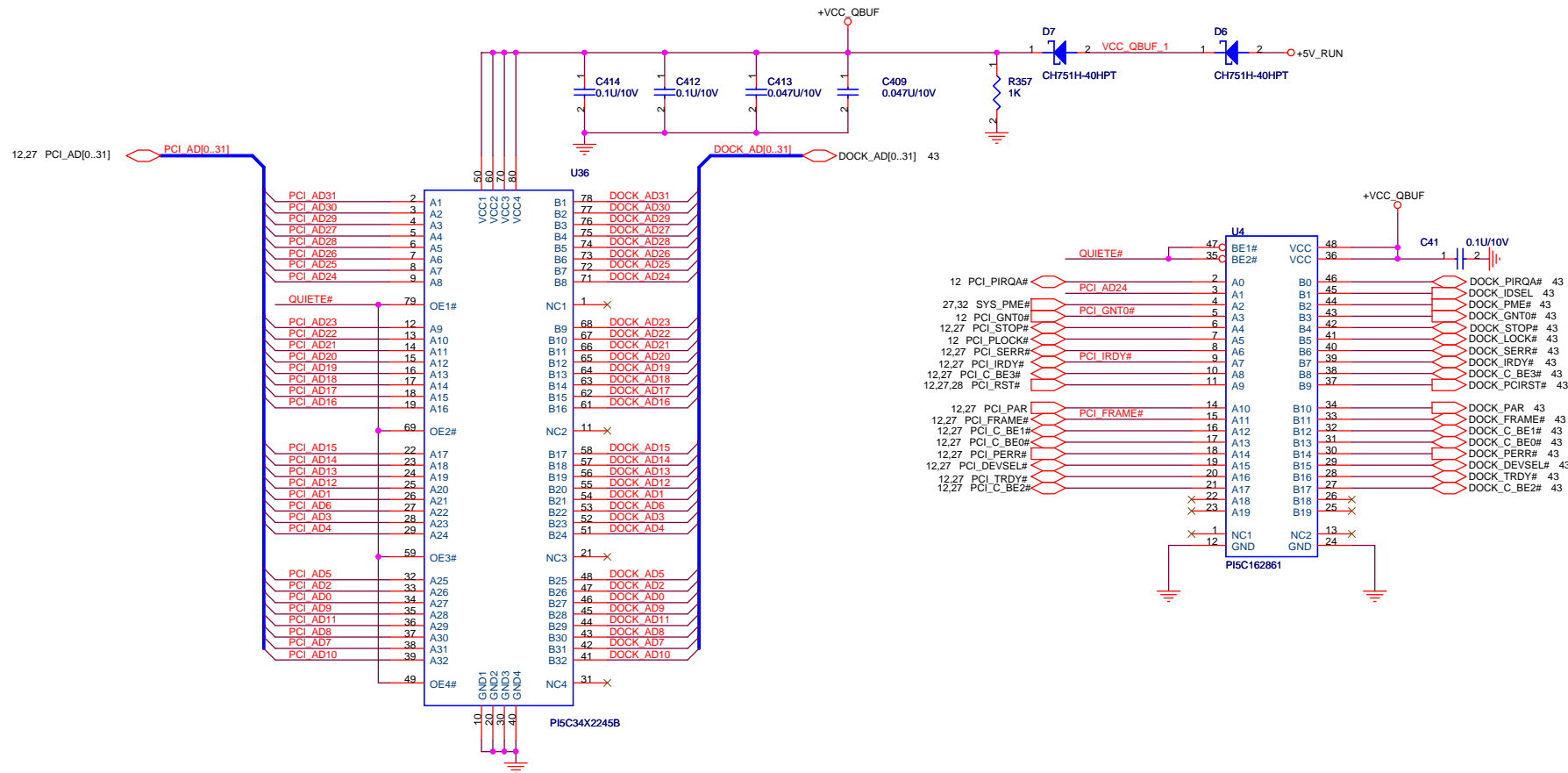


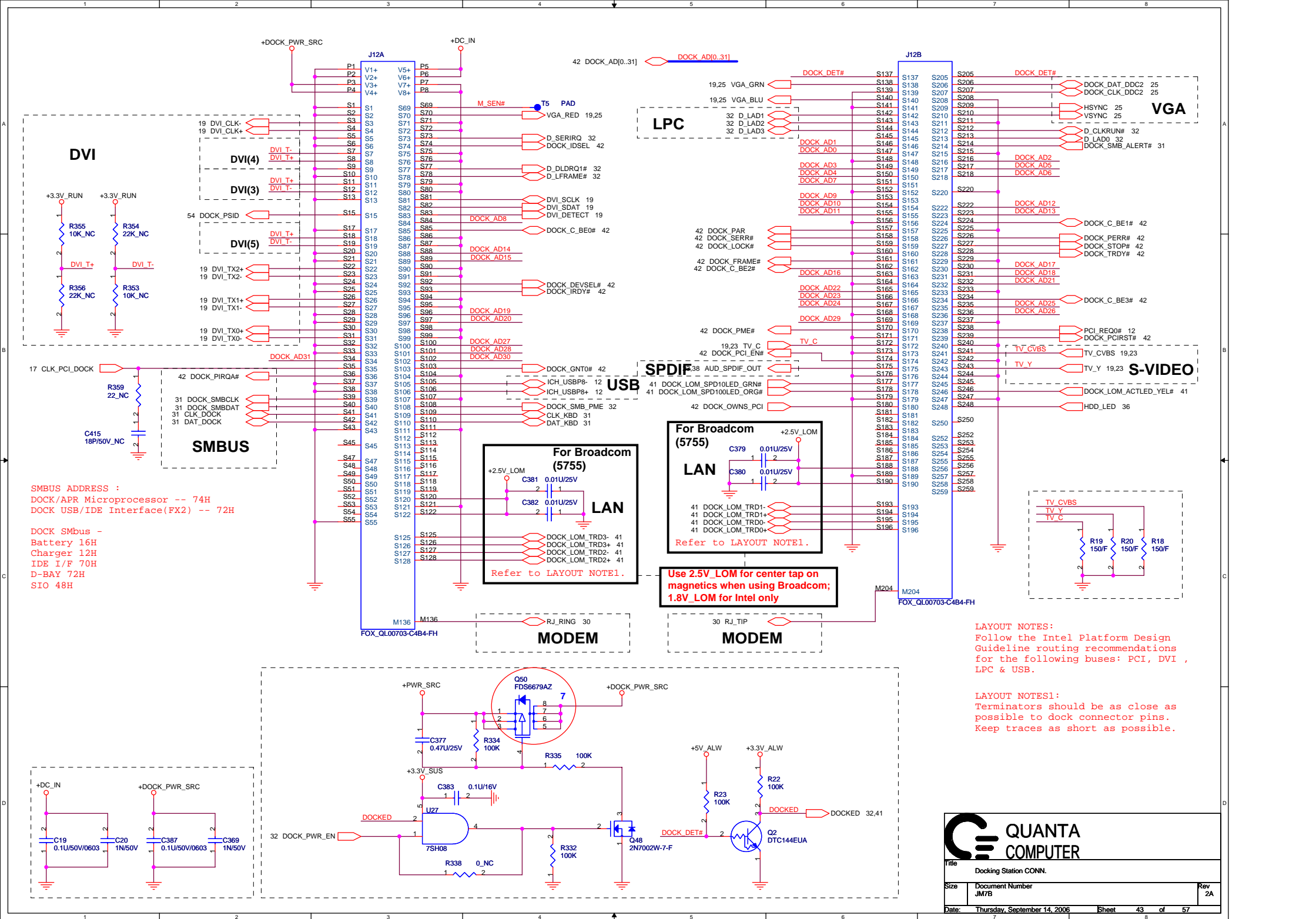
Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only



| | NV_STRAP1 | NV_STRAP0 | S0 | SI | CS# | SCLK |
|-------------------|-----------|-----------|----|----|-----|------|
| Auto-Sense Mode | 0 | 0 | 0 | 0 | 0 | 0 |
| ST M45PE20 | 0 | 1 | 1 | 0 | 0 | 1 |
| Atmel AT45BCM021B | 0 | 0 | 1 | 0 | 1 | 1 |

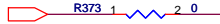






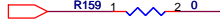
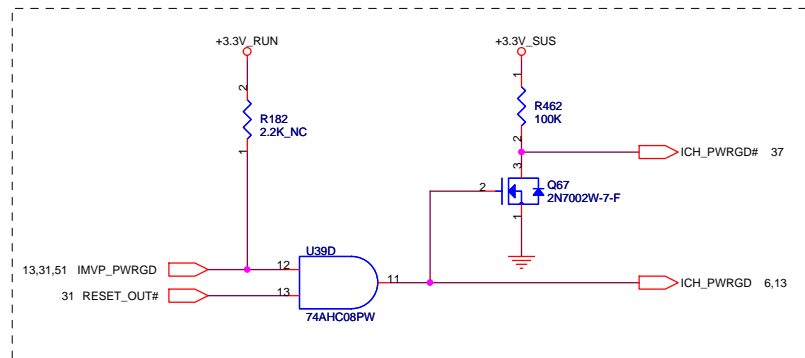
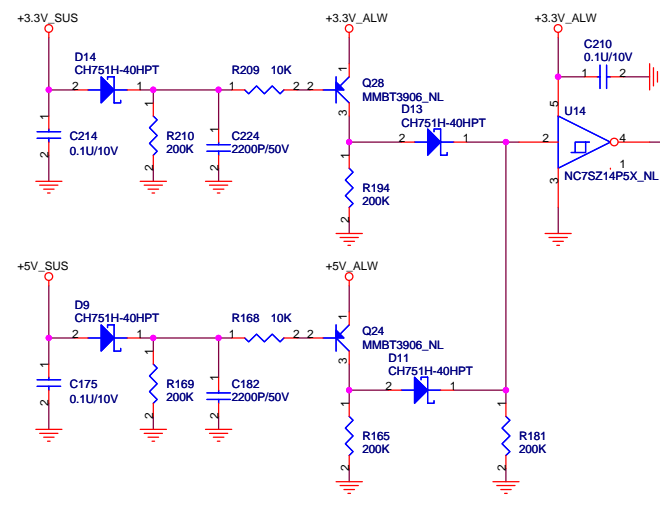
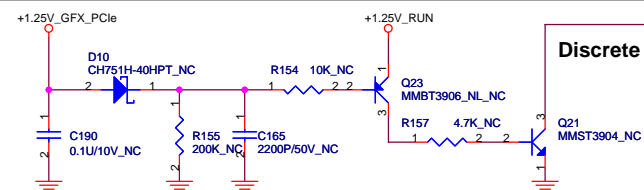
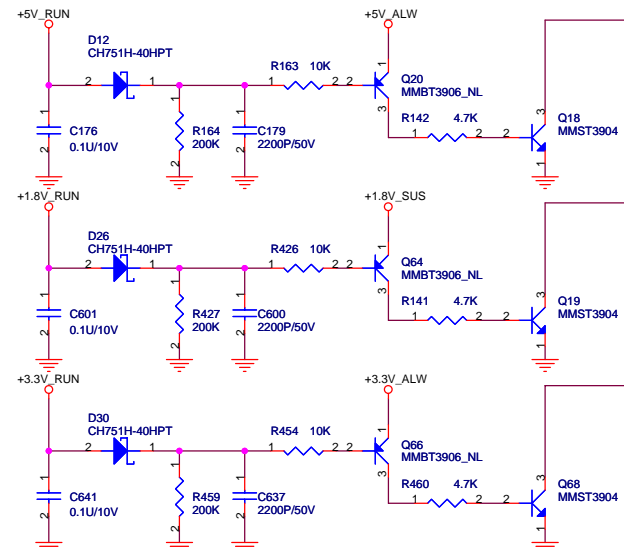
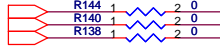
Non-iAMT

48 1.25V_RUN_PWRGD

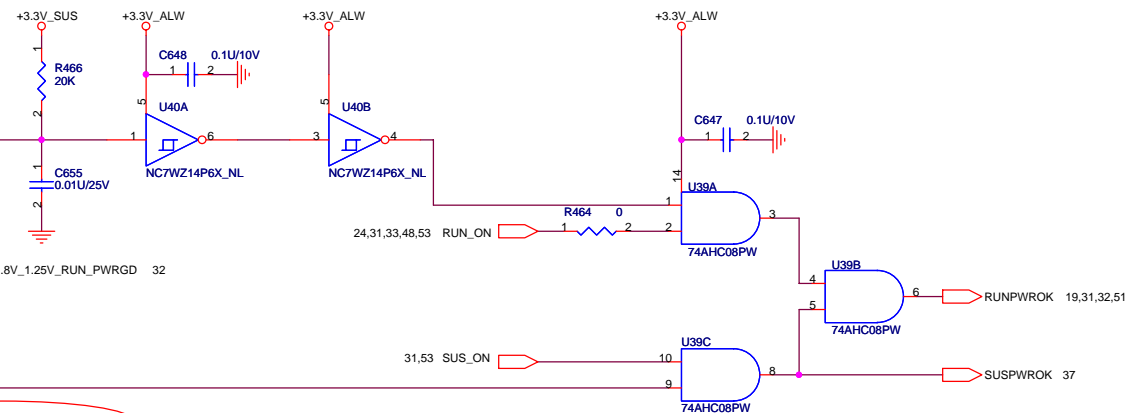


Discrete

50 GFX_CORE_PWRGD

49 1.5V_RUN_PWRGD
48 1.05V_RUN_PWRGD
37 2.5V_RUN_PWRGD

Keep Away from high speed buses



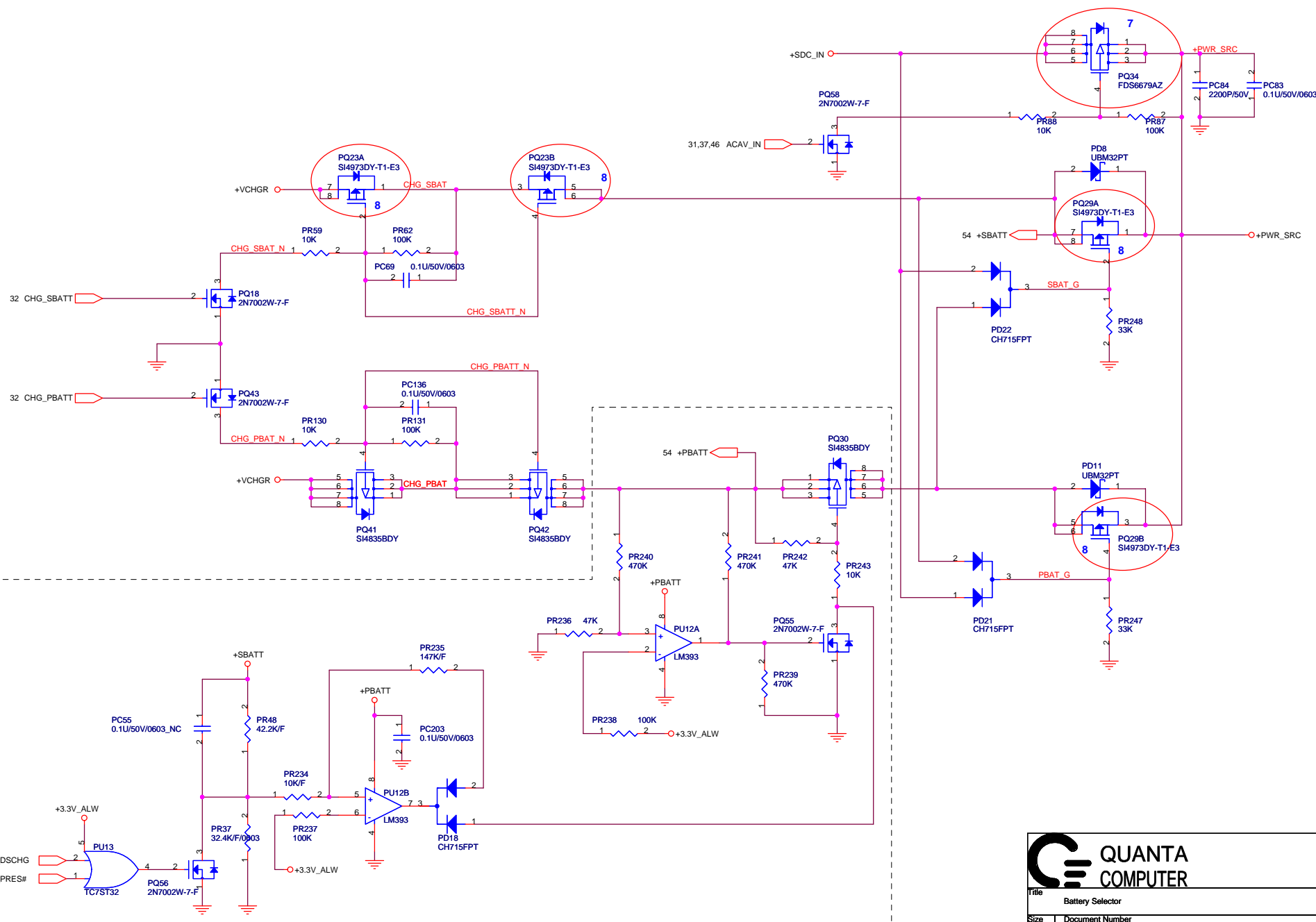
39

60

Title
System Reset CircuitSize
Document Number
JM7BRev
2A

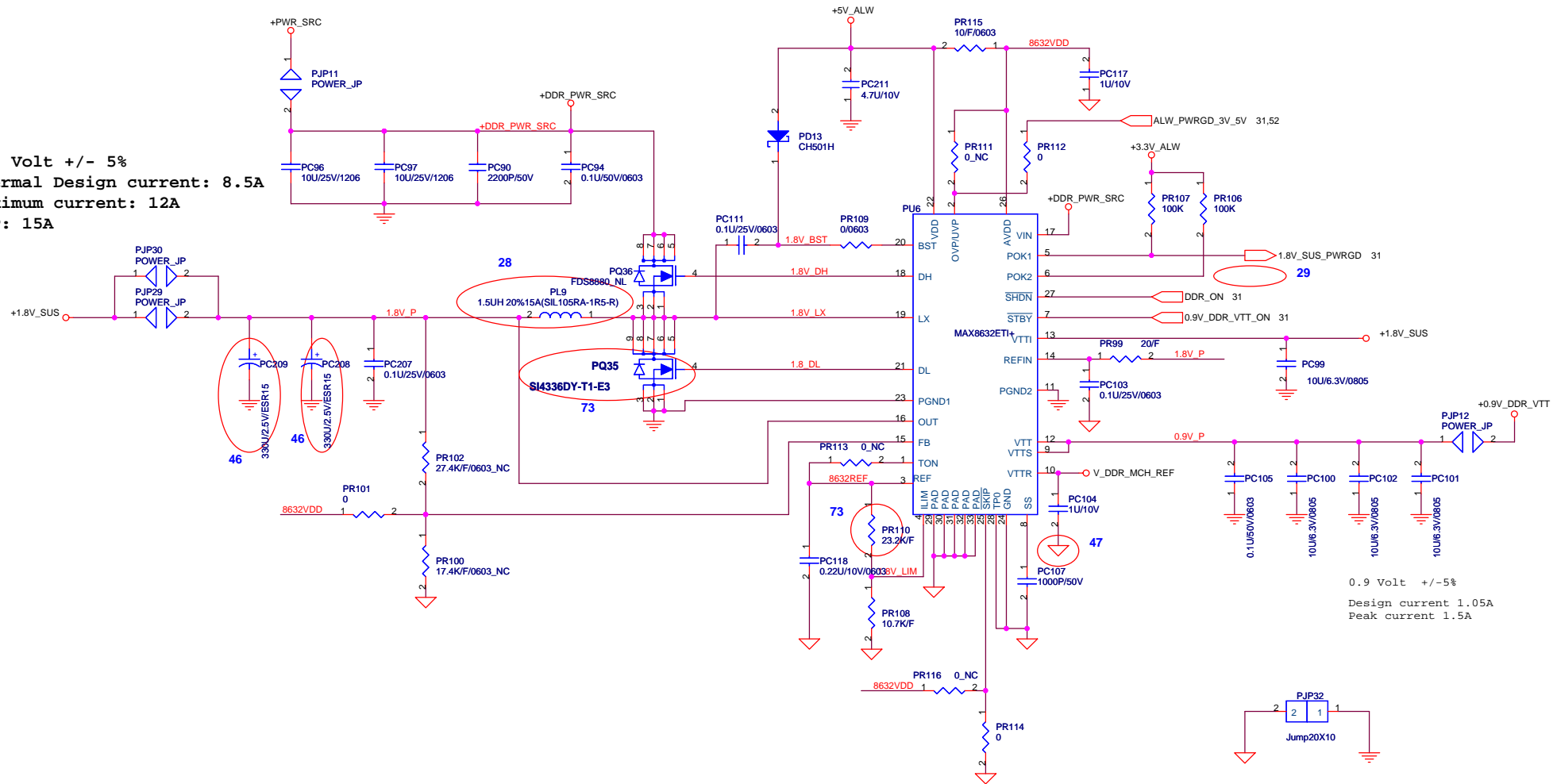
Date: Thursday, September 14, 2006

Sheet 44 of 57



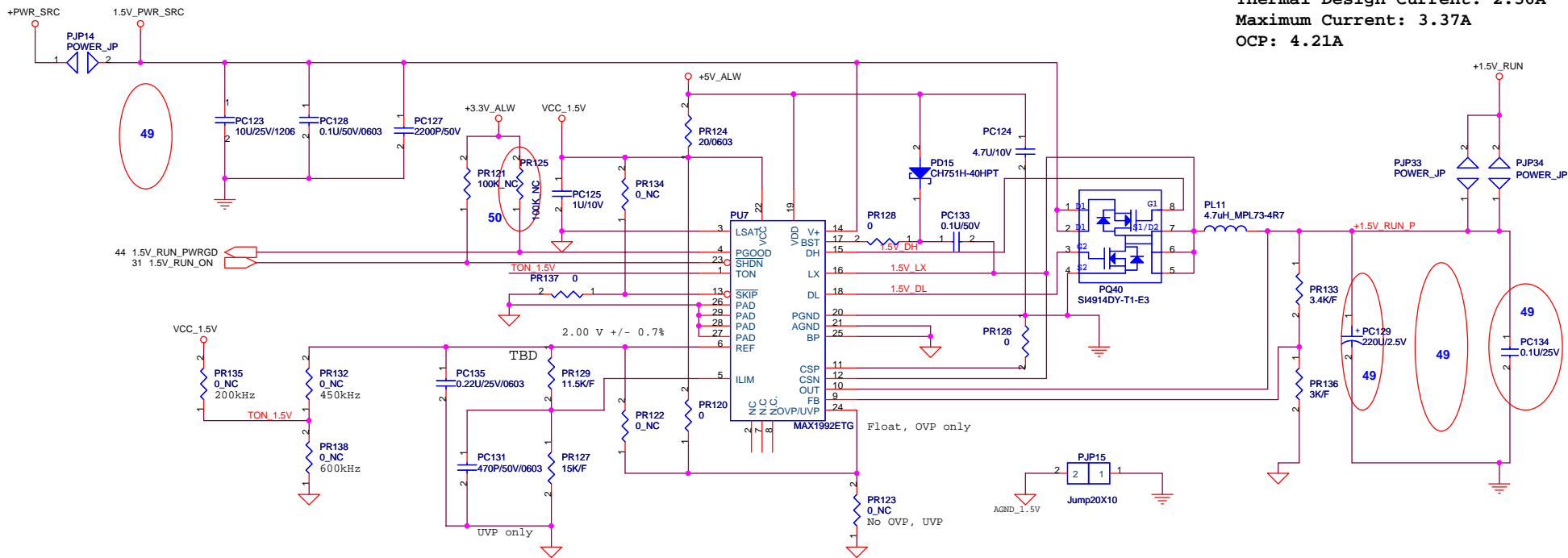
| | | |
|---------------------------------------|-----------------|-----------|
| Title Battery Selector | | |
| Size JM7B | Document Number | Rev 2A |
| Date: Thursday, September 14, 2006 | Sheet 45 | of 57 |

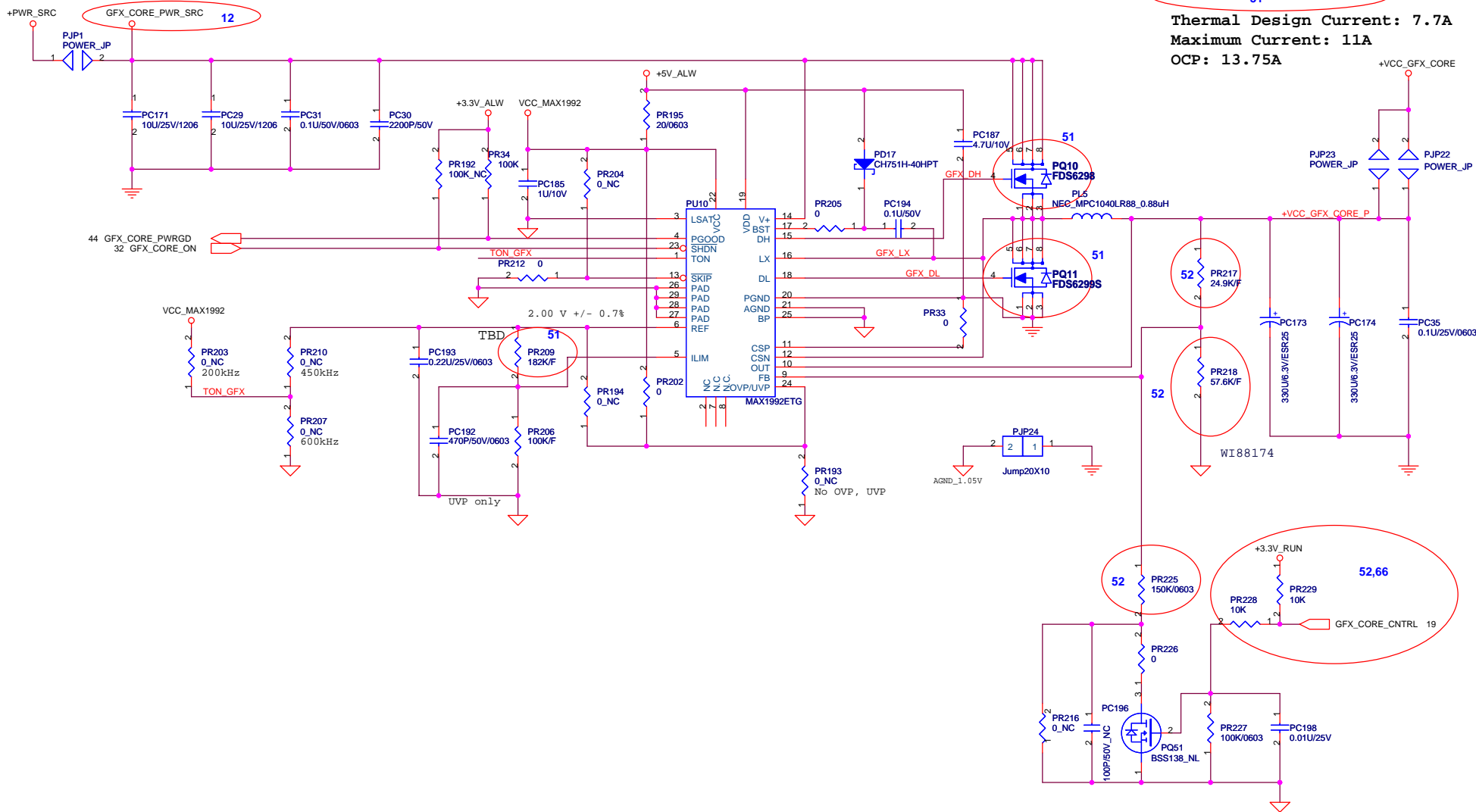
1.8 Volt +/- 5%
 Thermal Design current: 8.5A
 Maximum current: 12A
 OCP: 15A



0.9 Volt +/-5%
 Design current 1.05A
 Peak current 1.5A

1.5V +/- 5%
 Thermal Design Current: 2.36A
 Maximum Current: 3.37A
 OCP: 4.21A





Thermal Design Current: 7.7A
Maximum Current: 11A
OCP: 13.75A

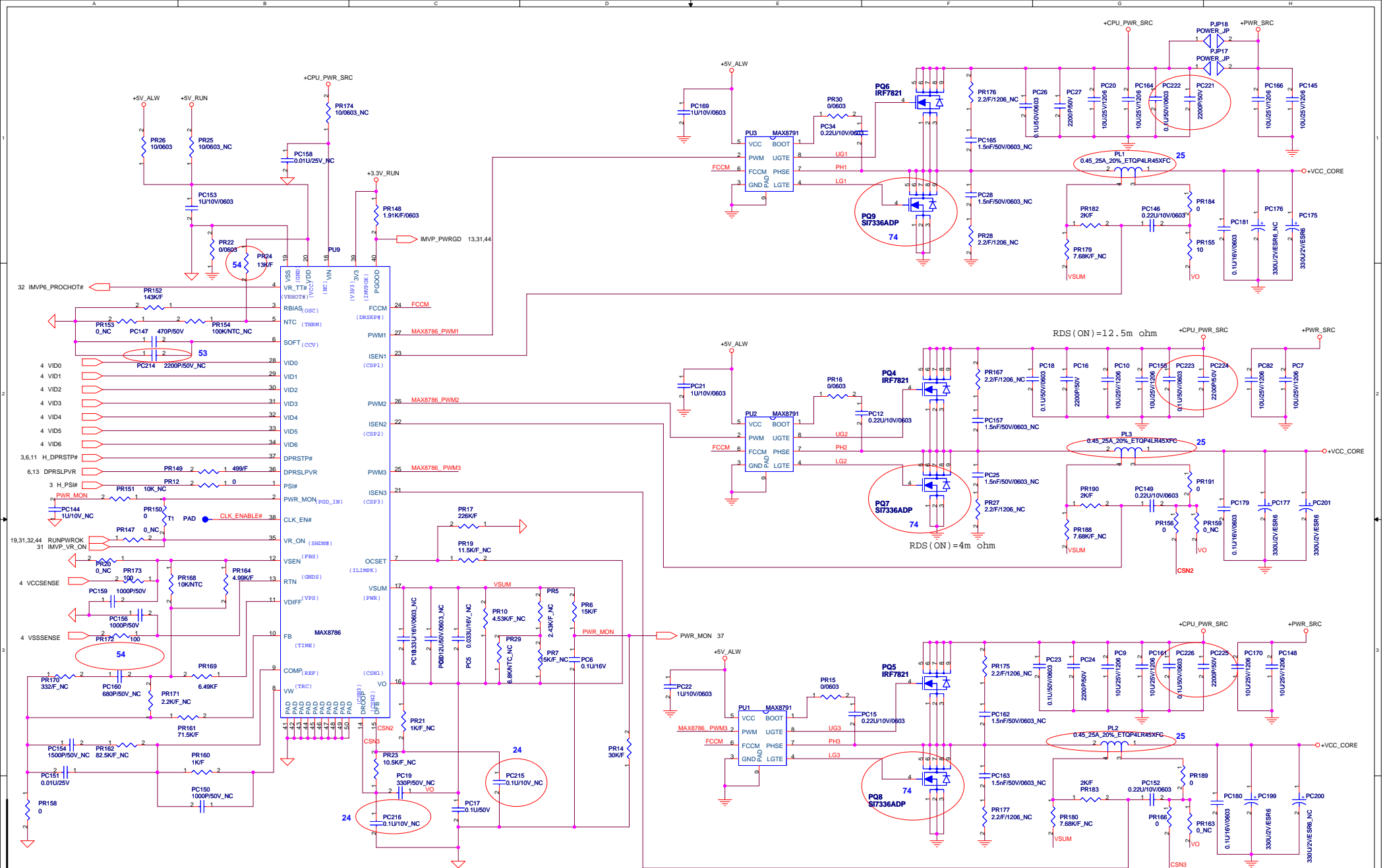
NOTE III: Output voltage control logic

When GFX_CORE_CNTRL High: +VCC_GFX_CORE at High.
 When GFX_CORE_CNTRL Low: +VCC_GFX_CORE at Low.

one more transistor stage should be added when using reverse control logic.



| | | |
|---------------|------------------------------|----------------|
| Title | | |
| VGA (MAX1992) | | |
| Size | Document Number | Rev |
| JM7B | | 2A |
| Date: | Thursday, September 14, 2006 | Sheet 50 of 57 |



If use ISL6260C:PR34 and PR38 are 0 ohm , PR37 and PR41 no stuff.

If use MAX8786:PR34,PR38,PR326 and PR327 no stuff , PR37 and PR41 are 0 ohm.

PHASE 3 populate



| | | | |
|-----------|------------------------------|-----------------|----------|
| File | | | |
| CPU Power | | | |
| Size | | Document Number | Rev |
| | | JMTB | 2A |
| Date: | Thursday, September 14, 2006 | Sheet | 51 of 57 |


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

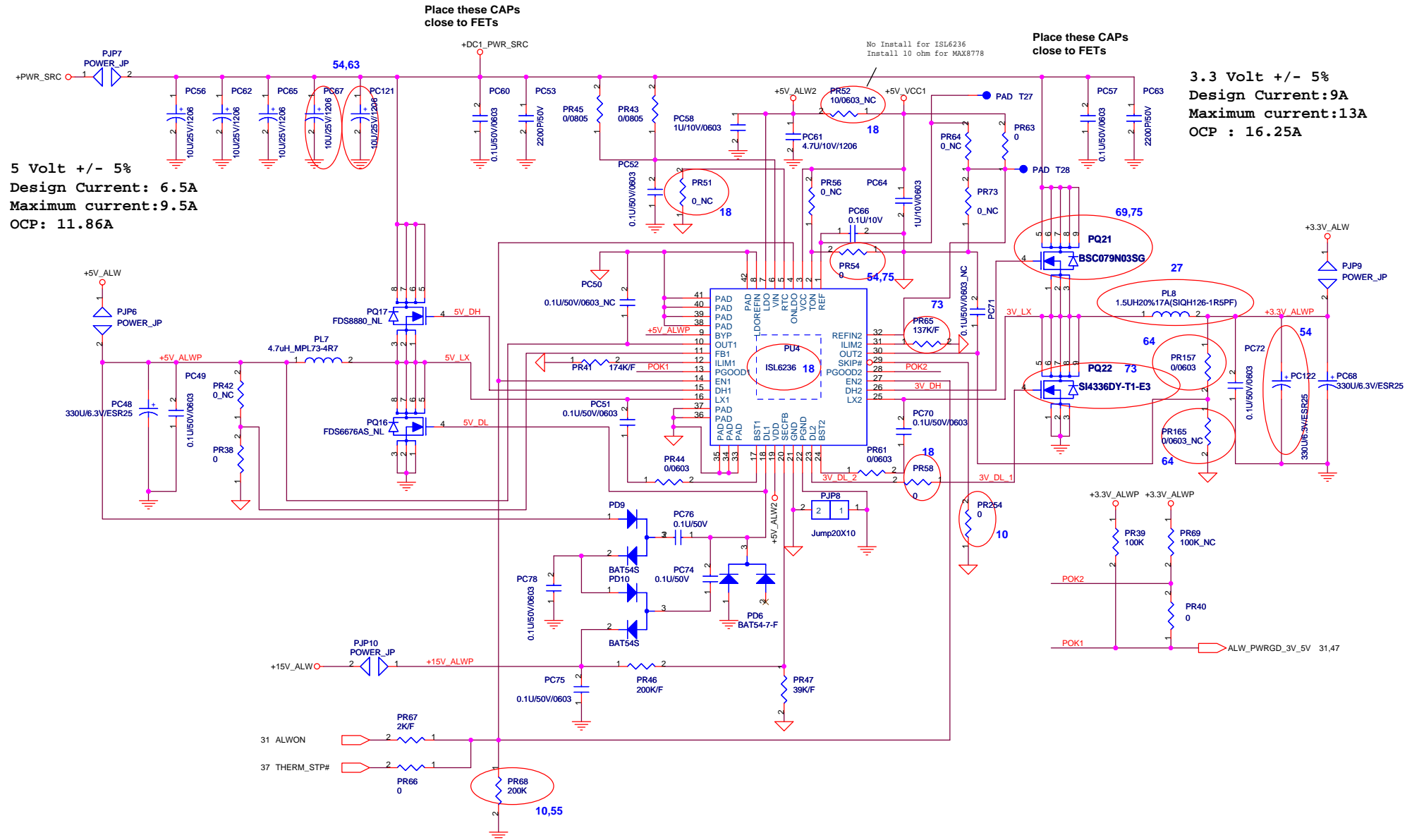
**Place these CAPs
close to FETs**

No Install for ISL6236
Install 10 ohm for MAX8778

**Place these CAPs
close to FETs**

3.3 Volt +/- 5%
Design Current:9A
Maximum current:13A
OCP : 16.25A

5 Volt +/- 5% 
Design Current: 6.5A
Maximum current: 9.5A
OCP: 11.86A



| | |
|-------|-----------------------|
| Title | 3VALW,5V,3V, Power On |
|-------|-----------------------|

| | |
|------|---------------|
| Size | Docum JM7B |
|------|---------------|

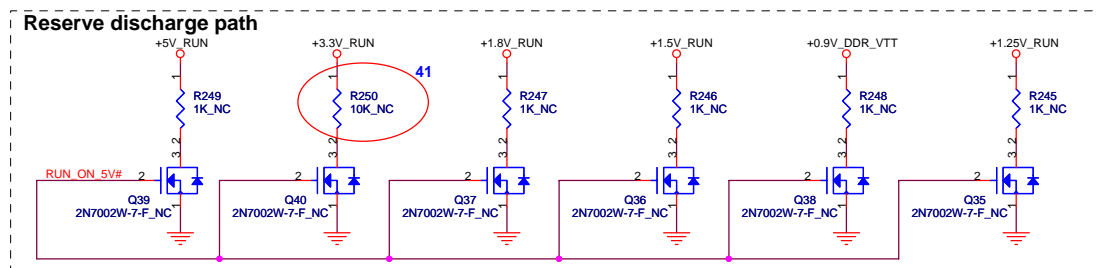
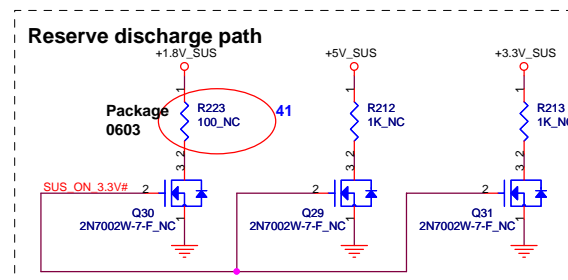
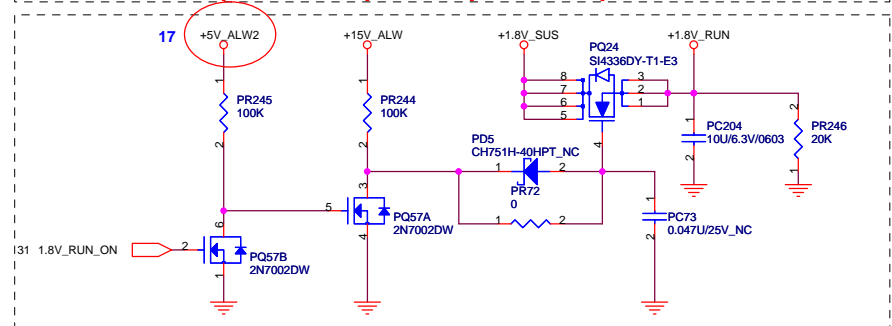
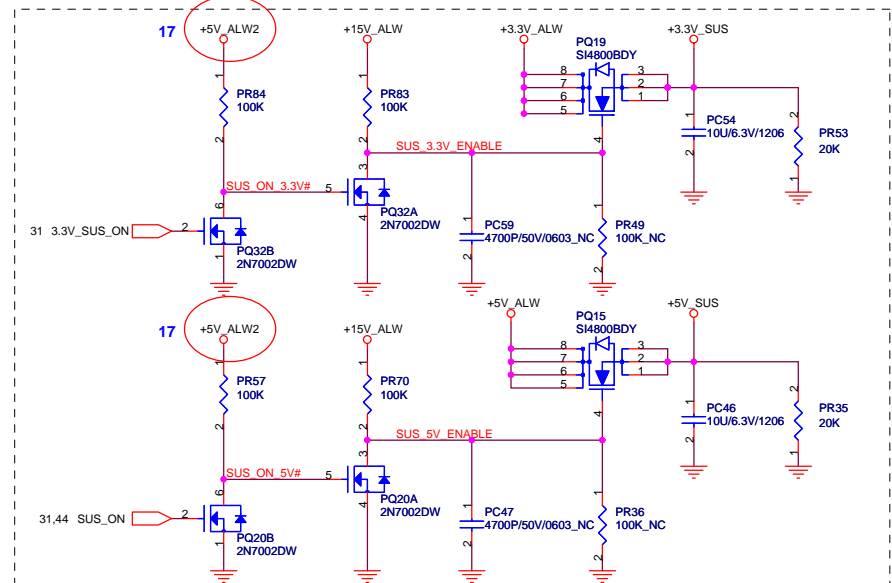
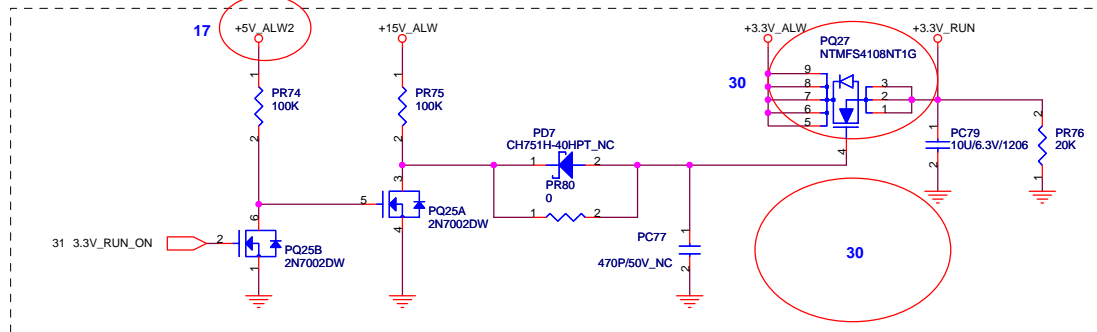
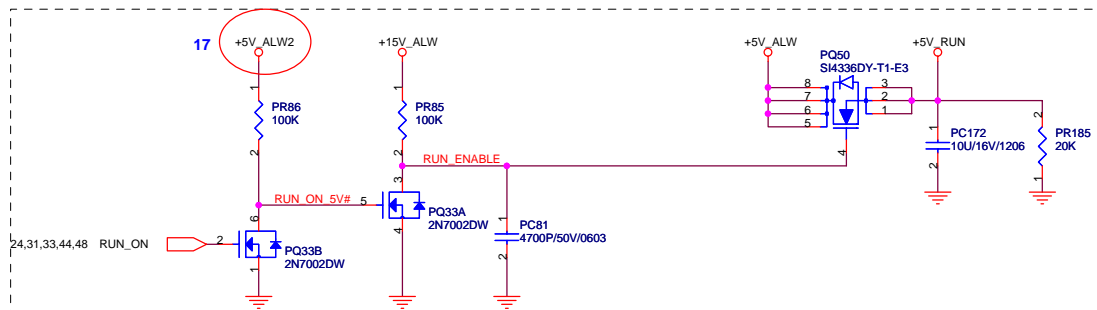
ment Number

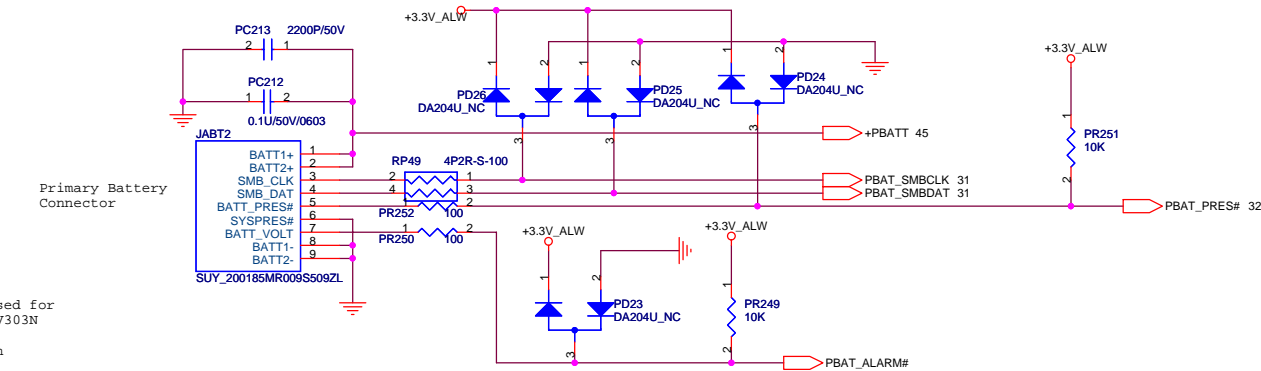
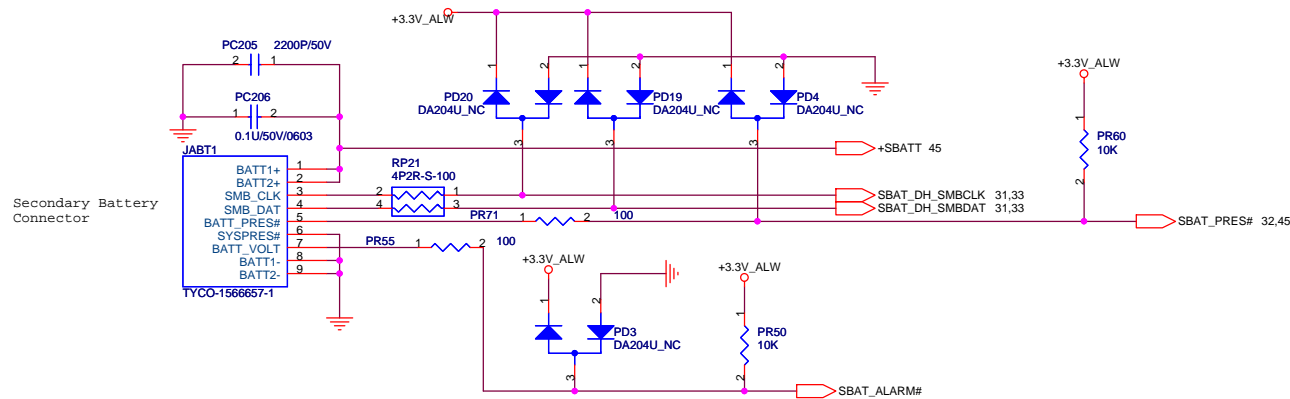
Rev

Date: Thursday, September 14, 2006

Sheet 52 of 57

| | |
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| | |
| | |



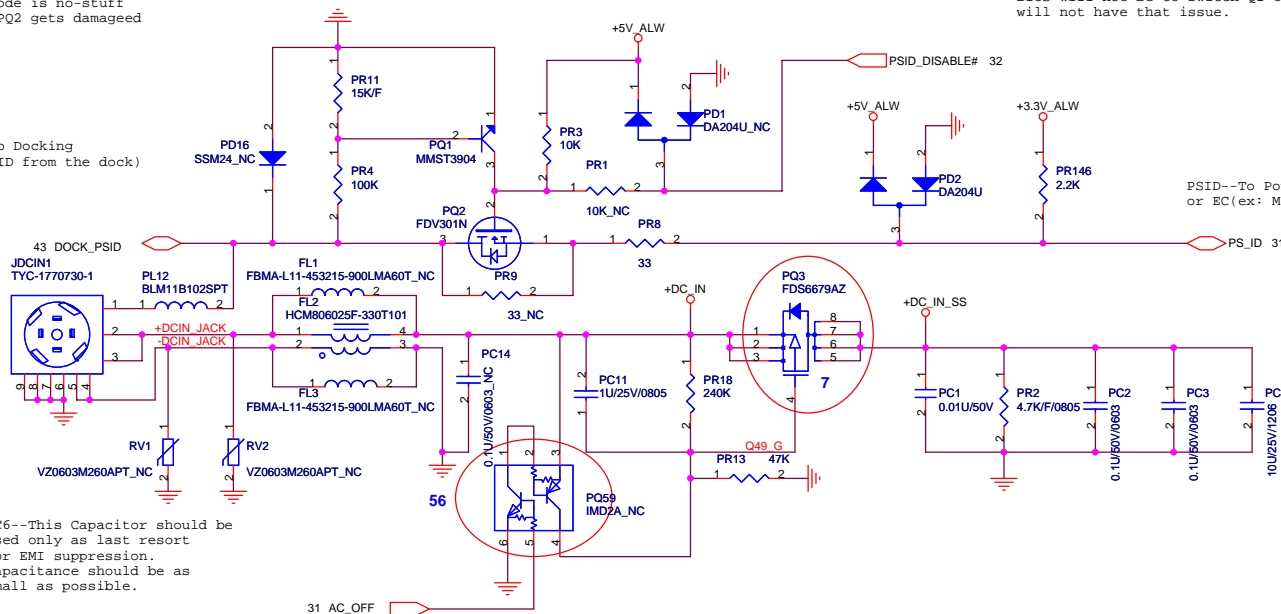


PQ2--Three transistor can be used for PQ2(pin compatible):FDV301N/FDV303N has low Vgs_on w/built-in ESD protection.MMBT100 BJT works in reverse conduction mode.

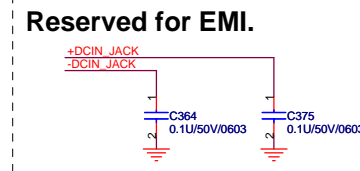
D12--This diode is no-stuff populate if PQ2 gets damaged by ESD.

DOCK_PSID--To Docking connector(PSID from the dock)

PR1--This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, BIOS will not be to switch Q1 off. MMBT100 will not have that issue.

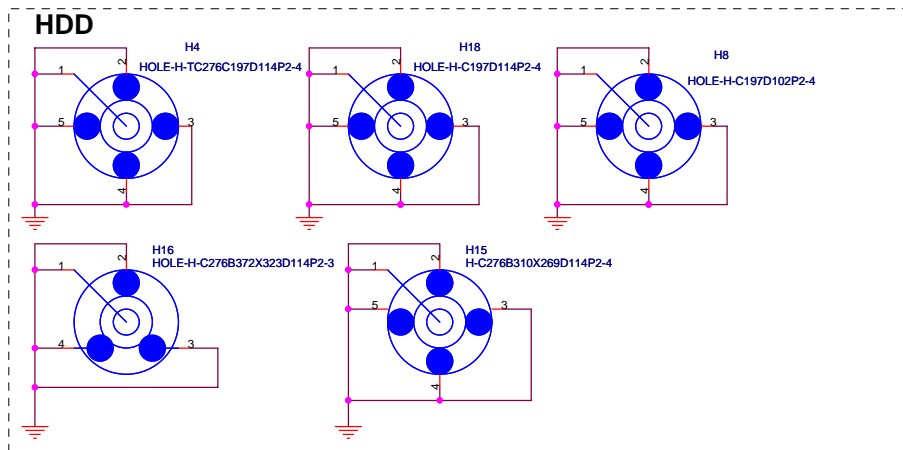
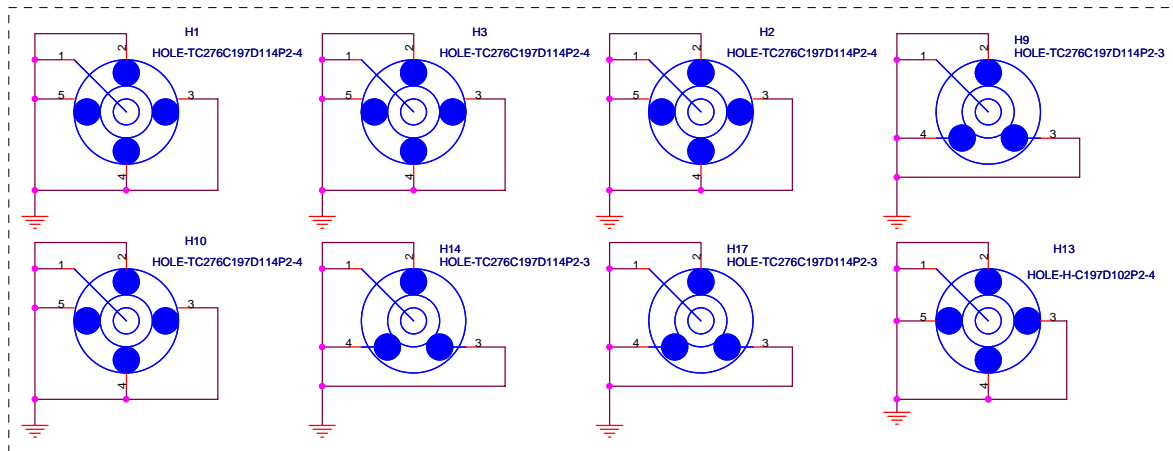
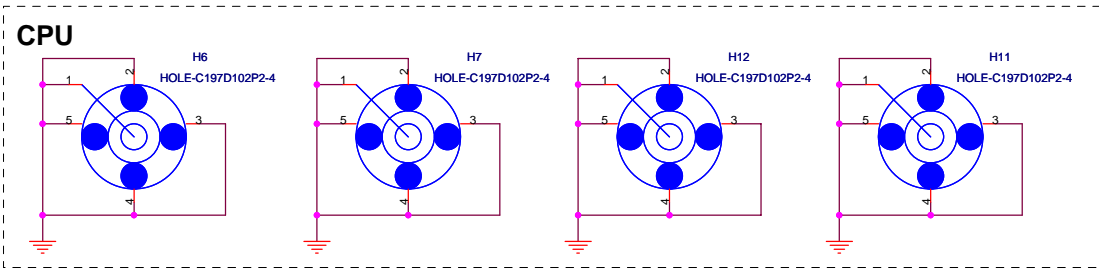
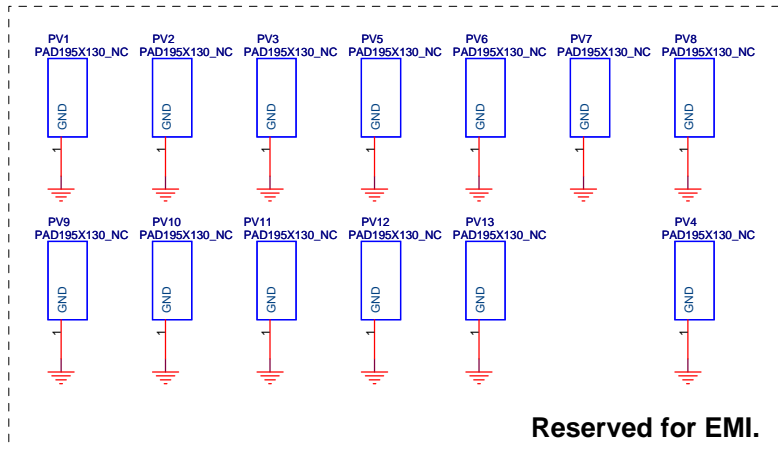


PC6--This Capacitor should be used only as last resort for EMI suppression. Capacitance should be as small as possible.



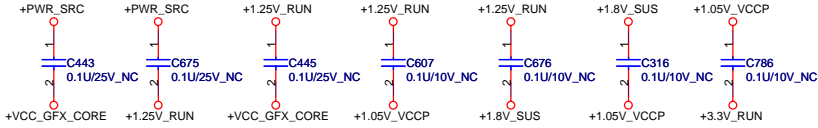
QUANTA COMPUTER

| | | | |
|-------|------------------------------|-------|-----------------|
| Title | | | DCIN,BATT CONN. |
| Size | Document Number | Rev | |
| | JM7B | 2A | |
| Date: | Thursday, September 14, 2006 | Sheet | 54 of 57 |

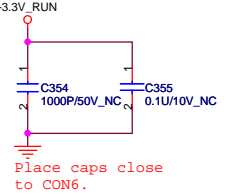


Reserved for EMI.

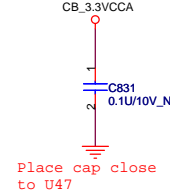
Stitching caps



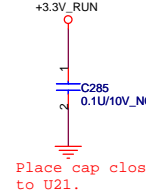
Page 26
SATA (HDD&CD_ROM)



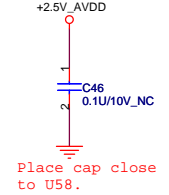
Page 27
PCCARD /CONN



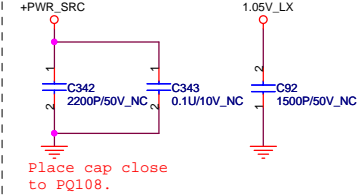
Page 38
Azelia CODEC



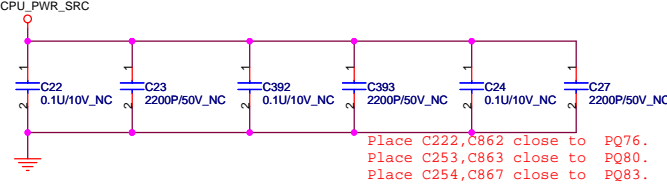
Page 40
LAN(BCM5755M)



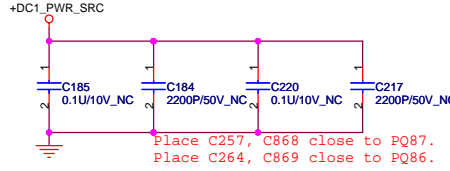
Page 48
1.25V & 1.05V(MAX8778)



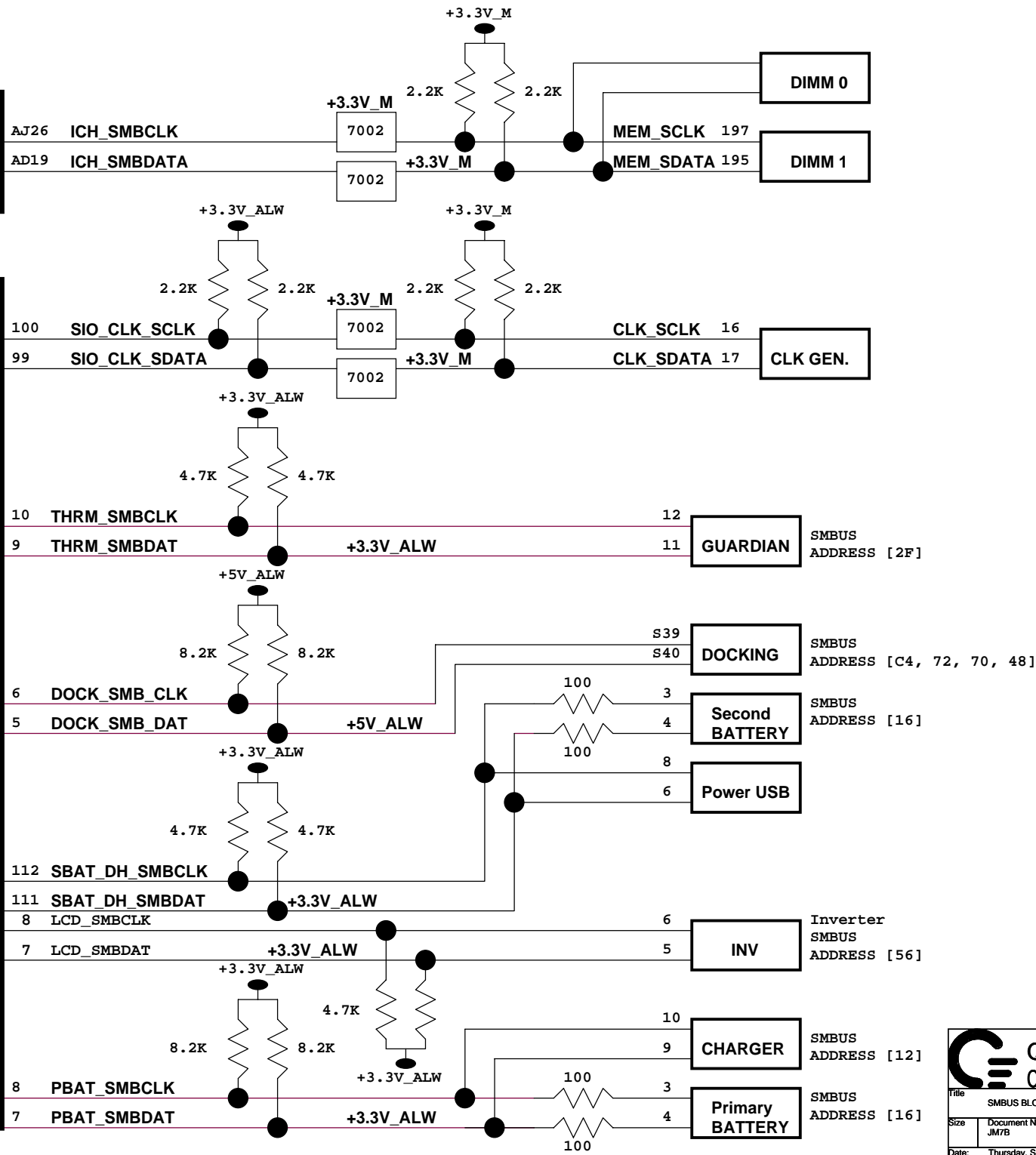
Page 51
CPU_MAX8786(3phase)





Page 52
D/D Power



| | | | |
|-------|------------------------------|-------|----------|
| Title | | | EMI CAP |
| Size | Document Number | Rev | |
| | JM7B | 2A | |
| Date: | Thursday, September 14, 2006 | Sheet | 56 of 57 |




| Model | Item | Page | Date | ECN Number | Item Id | Rev. | Issue Description | Solution Description |
|-------|-------|-----------|-----------|------------|---------|---|--|---|
| JM7B | 1 | 13 | 7/28/2006 | | WI82177 | 2A | SIO_EXT_SMI# Pull-up to Wrong Voltage Rail. SIO_EXT_SMI# pull-up is on 3.3V_ALW. This pull-up should be connected to 3.3V_SUS. This should prevent potential back-drive. | Done. |
| | 2 | 32 | 8/1/2006 | | WI83371 | 2A | Sch X00 - Change Board ID Straps for X01. | Populate R227 and depopulate R228 for Discrete. |
| | 3 | 12,23,33 | 8/3/2006 | | WI83995 | 2A | Add S-Video in place of single USB port. | Remove single USB port on page 33 and related USB trace on page 12. Add S-Video schematic on page 23. |
| | | 1,23 | 8/4/2006 | | | | Disenable SPDIF function for S-Video. Add S-Video block to page 1. | Done. |
| | 4 | 24 | 8/4/2006 | | WI83867 | 2A | X00 SM Bus EA issue | LCD_SMBCLK and LCD_SMBDAT rise time over spec. 1us.We need to remove C74, C75 for Discrete to meet SM Bus rise time Spec. |
| | 5 | 24 | 7/28/2006 | | N/A | 2A | Change MOSFET Q57 due to EOL. | Because Fairchild will change production material we change Q57 from FDC653N_NL to SI3456DV-T1-E3. SI3456DV-T1-E3 have been used by Brewster for second source. |
| | 6 | 24,33 | 7/28/2006 | | N/A | 2A | Change MOSFET Q12,Q58 due to EOL. | Because Fairchild will change production material we change Q12,Q58 from FDC658P_NL to FDC658AP. |
| | 7 | 43,45,54 | 7/28/2006 | | N/A | 2A | Change MOSFET PQ3,PQ34,Q50 due to EOL. | Because Fairchild will change production material we change PQ3,PQ34,Q50 from FDS6679 to FDS6679AZ. |
| | 8 | 45 | 8/4/2006 | | N/A | 2A | Change MOSFET PQ23,PQ29 due to EOL. | Because Fairchild will change production material we change PQ23,PQ29 from FDS4935 to SI4973DY-T1-E3.SI4973DY-T1-E3 have been used by Brewster for second source. |
| | 9 | 48 | 8/8/2006 | | WI84718 | 2A | 1.25V high side fet and low side fet should be overturn.For FDS6982S, the Q1 of the package is optimized for the high-side, and the Q2 is optimized for the low-side. | Modify PQ49 on Discrete. |
| | 10 | 52 | 8/8/2006 | | WI84734 | 2A | For the ALWON issue ,PR68 on Dis should be change to 0.47uF cap. PC214 instead of PR68. | Done. |
| | 11 | 48 | 8/8/2006 | | WI84737 | 2A | Pin 29 of MAX8778 should add a resister to GND since MAX8778 has 5V OVP issue on skip mode.Please refer to attachment from MAXIM.If add a 0 ohm resister on pin29 of MAX8778 ,then we can change to ultrasonic mode. | Add PR253 and PR254 on Dis. |
| | 12 | 50 | 8/8/2006 | | WI84745 | 2A | Since "GFX_PWR_SRC" net name on page 50 the same as page24. Change "GFX_PWR_SRC" net name to "GFX_CORE_PWR_SRC" on page50. | Done. |
| | 13 | 11,13 | 8/9/2006 | | WI81395 | 2A | All unused GPIs on the ICH8 need to be terminated by a pull-up. Feedback from Intel advises that all unused GPIs on the ICH8 need to be terminated with a 8.2k - 10k ohm resistor pulled up to their corresponding volatage rails. | Add 10K termination resistors R654,R655,R656 to GPIO13,GPIO33,GPIO34 and pull up to +3.3V_SUS on page 11. Add 10K termination resistors R658 for GPIO12;R657 for GPIO27;R660 for GPIO26 ;R661 for GPIO24;R659 for GPIO10 and pull up to +3.3V_SUS on page 13. |
| | | 11,13 | 8/16/2006 | | | | Add 10k termination resistor to GPIO9 pulled up to +3.3V_SUS on page 13 / Depop R654, R655, R656, R657, R660, R661 since default state of these pins are GPO. | Done. |
| | 14 | 3 | 8/10/2006 | | WI82350 | 2A | Dawson 3VSUS back drive under S4, S5. After check Dawson (UMA and Discrete) 3VSUS back drive under S4, S5. There are two signal (ITP_DBRESET and SIO_EXT_SMI) need change pull up from 3V_ALW to 3VSUS.These changes need implement into UMA and Discrete both. | Change the power rail of ITP_DBRESET# to +3.3V_SUS for back-drive.SIO_EXT_SMI have been corrected with power rail by WI82177. |
| | 15 | 31,34 | 8/10/2006 | | WI82765 | 2A | Per SMSC, need to have pull-ups for BC Bus Data lines. 1. Add a 100k ohm pullup to +3.3V_ALW on the BC Bus Data line for the high speed BC Bus (pin 86) of the MEC5025. This is needed if the BC Bus is ever operated slower than the 12MHz that we currently operate at. 2. Add a No Stuffed 100k ohm pullup to +3.3V_ALW on the low speed BC Bus Data line for the low speed BC Bus (pin 39) of the MEC5025. There is an internal pullup in the MEC, but since this BC Bus is mulitplexed with the KBC pins, a pad for this resistor is recommended. | Add pullup R662 on BC_DAT to +3.3V_ALW. Change R526 from 10K to 100K and no stuff. |
| | 16 | 34 | 8/16/2006 | | WI85788 | 2A | SCH X01 - Dawson/Fila PT build needs to use 2MB flash part. Due to increase in number of payloads the BIOS is carrying, we need to move to a 2MB SPI flash part for the PT builds. | Change U43 from SST25LF080A to SST25VF016B. |
| | 17 | 48,53 | 8/16/2006 | | WI85909 | 2A | Due to the +15V_ALW rail going high before the +5V_ALW rail, the enable circuit for multiple switched fets needs to change, to prevent unwanted glitches from occurring. | Change pullup rail from +5V_ALW to +5V_ALW2 for the following resistors - PR86, PR74, PR84,PR57,PR245 and PR231. |
| 18 | 48,52 | 8/21/2006 | | WI85916 | 2A | Change from MAX8778 to ISL6236. | Change PU11 from MAX8778 to ISL6236, PR211 to 0 ohm on sheet 48. Change PU4 from MAX8778 to ISL6236, PR58 to 0 ohm ;depop PR51;depop PR52 on page 52. | |
| 19 | 37 | 8/21/2006 | | WI86681 | 2A | Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V. | Pullup is at reference designator R198. | |
| | | | | | | | | <div>QUANTA COMPUTER</div> <div>Title Change list</div> <div>Size JM7B</div> <div>Document Number JM7B</div> <div>Rev 2A</div> <div>Date: Thursday, September 14, 2006</div> <div>Sheet 1 of 5</div> |

| Model | Item | Page | Date | ECN Number | Item Id | Rev. | Issue Description | Solution Description |
|---|------|-----------|-----------|------------|--------------------|---|--|---|
| JM7B | 20 | 39 | 8/21/2006 | | WI86348 | 2A | Change L25 and L26 to BLM18BD601SN1D for Vista audio performance. | Done. |
| | | 39 | 8/25/2006 | | | | | Change L25,L26 from BLM18BD331SN1D to BLM18BD601SN1D. |
| | 21 | 38 | 8/21/2006 | | WI86347 | 2A | Recent audio performance tests show that the original 1.0uF has marginal passing results. 2.2uF needed to ensure audio performance requirements are met. | Change C751 and C768 to 2.2uF for Vista performance requirements. |
| | 22 | 38 | 8/21/2006 | | WI86342 | 2A | Depop C309. This may not be needed in light of C253 and C320. | Done. |
| | 23 | 38 | 8/21/2006 | | WI86335 | 2A | Change codec package to QFN; U19 needs to change to QFN package. STAC9205X5NBEB1XR. | Done. |
| | 24 | 51 | 8/23/2006 | | WI87472 | 2A | V_CORE controller should add two caps at "CSN2" and "CSN3" pin. | For MAXIM suggestion and follow MAX8786 spec, add PC215 and PC216. |
| | 25 | 51 | 8/23/2006 | | WI87480 | 2A | Change v_core choke from "MPC1040LR45" to "ETQP4LR45XFC" since Panasonic(ETQP4LR45XFC) cheaper than NEC-TOKIN(MPC1040LR45). | Change PL1 , PL2 and PL3 to "ETQP4LR45XFC". |
| | 26 | 31,36 | 8/25/2006 | | WI87892 | 2A | In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low. | Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R479 and R480. |
| | 27 | 52 | 8/25/2006 | | WI85389 | 2A | With a max current of 13A, and calculated ripple of 2.12A, the peak current on PL8 will be 14.06A. The current rating for MPO73-2R2 is marginal at best. Need to choose an inductor with a higher current rating. | Change to 1.5UH20%17A(SIQH126-1R5PF) |
| | 28 | 47 | 8/25/2006 | | WI86712 | 2A | For a maximum current rating of 12A, the peak inductor current for PL9 will be 13.7A. The MPO104-1R5 part is rated for 20A. Finding an inductor with a lower current rating could possibly lead to a physically smaller and cheaper inductor. | Change to 1.5UH 20%15A(SIL105RA-1R5-R) |
| | 29 | 31,47 | 8/25/2006 | | WI87919 | 2A | Sch X01: Remove 0.9V_DDR_VTT_PWRGD circuit. The 0.9V_DDR_VTT_PWRGD circuit is not currently being used, and can be removed. | Leave pin 73 of MEC5025 as no connect . |
| | 30 | 53 | 8/25/2006 | | WI88291 | 2A | Reduce Fets PQ26 and PQ27 into only one Fet. It will be more cheaper. Change PQ27 from "SI4336DY" to "NTMFS4108N". Remove PQ26. | Done. |
| | 31 | 26,32 | 8/26/2006 | | WI88236 | 2A | Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment. | To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design. |
| | 32 | 32 | 8/26/2006 | | WI88528 WI88427 | 2A | SCH X01 - Change ECE5018 to ECE5028. For X01 pilot run, USIO1 needs to change to ECE5028. | Remove R259,R258,C271,C270,C237,C238,C252,R240,R239,Y1,C250,C247,L32,C259,C269,C275. and related stubs for Discrete |
| | 33 | 11,40 | 8/28/2006 | | WI88592 | 2A | Tune crystal frequency tolerance for 25MHz in LAN and 32.768KHz in ICH. | Change C428 from 27P to 22P for Y2. Change C772,C781 from 15P to 12P for W2. |
| | 34 | 19 | 8/28/2006 | | WI88358 | 2A | Need to connect thermatrip_vga# to GPIO8 instead of GPIO9.G8x has a new GPIO for our thermal trip output from our internal thermal sensor compared with G7x. So, please connect thermatrip_vga# to GPIO8 instead of GPIO9. It's open collector so it needs a pullup. | Done. |
| | 35 | 19,20 | 8/28/2006 | | WI88367 | 2A | The HDCP rom needs to be connected to the I2CH_SCL(C7) and I2CH_SDA(B7) and the pullups RP16 need to be removed. Currently these hdcp pins are connected to I2CA. | Connect pin5,6 of U34 from I2CA bus to I2CH bus and remove RP16. |
| | 36 | 31 | 8/28/2006 | | WI88584 | 2A | Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k 3. Add 2.7k pull-down to AUX_ON | Change R521,R522 to 2.7K; add pull-up R532 for AUX_ON. |
| 37 | 41 | 8/28/2006 | | WI88588 | 2A | U20 (UMA) & U24 (DIS) footprint should be changed to accommodate both wide-body Atmel AT45BCM021B & narrow-body ST-Micro M45PE20. | Add U37 for ST-Micro M45PE20. | |
| 38 | 29 | 8/29/2006 | | WI88810 | 2A | The 0.1 uF caps can be removed on WLAN (C748) and WWAN (C306). Pin 24 for WWAN should be connected to +3.3V_Run. | Done. | |
| <div><div>QUANTA COMPUTER</div><div><div>Title</div><div>Change list</div><div><div>Size</div><div>Document Number</div><div>Rev</div></div><div><div>JM7B</div><div>2A</div></div><div><div>Date:</div><div>Thursday, September 14, 2006</div><div>Sheet</div><div>2</div><div>of</div><div>5</div></div></div></div> | | | | | | | | |

| Model | Item | Page | Date | ECN Number | Item Id | Rev. | Issue Description | Solution Description |
|-------|------|-----------------------|-----------------------|--|---------|--------------------------------|--|---|
| JM7B | 39 | 12,13 31,32, 44 | 8/29/2006 | | WI88589 | 2A | Sch X01: Update GPIOs | 1. Swap PS_ID (ECE5018, pin 71) with ITP_DBRESET# (MEC5025, pin 55) 2. Move SB_WLAN_PCIE_RST# from ICH pin F18 to pin G11 3. Move SB_NB_PCIE_RST# from ICH pin C10 to pin F12 4. Move PLTRST_DELAY# MEC5025 pin 69 to ICH pin AF9 5. Move BEEP from ECE5018 pin 78 to MEC5025 pin 69 6. Move SIO_EXT_SC# from ICH pin AG22 to ICH pin AC19 7. Connect ICH pin AG22 to LOM_SMBALERT#, add a 0-ohm series resistor and depopulate, name the net LOM_ICH_SMBALERT# 8. Disconnect 3.3V_5V_SUS_PWRGD from MEC5025 pin 29 9. Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29 10. Swap DOCK_SMB_PME# (MEC5025 pin 3) with DOCK_SMB_ALERT# (ECE5018 pin 76) |
| | | 31,32 | 8/30/2006 | DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW | | | | |
| | 40 | 38 | 8/29/2006 | | WI88586 | 2A | Update GAIN settings / table to reflect MAX9789A production parts.Please update the GAIN settings table on page 38 of the schematics to reflect what is described in the MAX9789A specification. The table that is currently in the schematic is for sample parts, not mass production. In addition, please populate the parts for 15.6dB. | Update GAIN table and populate R296,R549; depopulate R550,R297. |
| | 41 | 53 | 8/30/2006 | | WI88965 | 2A | Dawson/Fila X00 Gerber board shows that resistor R250 on 3.3V reserved discharge path violates Dell derating guideline (9E154 A03). The resistance has to be increased to appropriate value to meet the 70% power derating. | Change R250 from 10 ohm to 10K ohm. |
| | | | 9/1/2006 | R223 should be changed to 100 ohm as you did on UMA version and It has to be 0603. | | | Change R223 from 33 ohm to 100 ohm package 0603. | |
| | 42 | 36 | 8/29/2006 | | WI88815 | 2A | BJT Q7 should be pulled up to +3.3V_RUN as opposed to +3.3V_WLAN in order to mimic LED behavior on M'07 systems. | Change power rail with Q7 pin1 from +3.3V_WLAN to +3.3V_RUN. |
| | 43 | 29 | 8/29/2006 | | WI88799 | 2A | Add 2nd 330uF bulk cap for WWAN connected to 3.3V_RUN. This is to help provide enough power for the pulse loads during GPRS operation (max current up to 3A for ~1 ms). Also would help in UMTS modes (more common) where average draw is ~1 A. | Populate 330uF/6.3V to C327. |
| | 44 | 46 | 8/29/2006 | | WI88815 | 2A | Change PR96 value in charger ckt.Per Maxim's recommendation, change the value of PR108 from 4.7k to 10k. | Change PR96 to 10K ohm. |
| | 45 | 48 | 8/29/2006 | | WI88444 | 2A | Cnange value of PC163 on sheet 48.Per Intersil's recommendation, change the value of PC163 from 1uF to 0.1uF. | Change PC163 to 0.1uF/25V. |
| | 46 | 47 | 8/29/2006 | | WI82882 | 2A | PC209,PC208 to be populated in order to meet output ripple requirements. | Done. |
| | 47 | 47 | 8/29/2006 | | WI86924 | 2A | PC104 should connect to analog ground. | On sheet 47 of Dawson Discrete, PC104 should connect to analog ground, not power ground. |
| | 48 | 48 | 8/29/2006 9/1/2006 | | WI88468 | 2A | 6 Changes to 1.25V_RUN regulator on sheet 48. | 1) Only one 10uF input cap is needed, delete PC184 2) Only one 220uF output cap is needed, delete PC32, and change PC178 from 330uF to 220uF. 3) Change PC33 from 10uF to 0.1uF. 4) Change PC189 from 1uF to 0.1uF. 5) Depop PR208. 6) Add a 0.1uF cap to analog ground from pin 9, BYP. |
| | 49 | 49 | 8/29/2006 | | WI88476 | 2A | 4 Changes to 1.5V_RUN regulator. | 1) Only one input cap is needed, delete PC122. 2) PC121 can be deleted 3) PC129 can be changed from 330uF to 220uF 4) Change PC134 from 10uF to 0.1uF. |
| | 50 | 49 | 8/29/2006 | | WI88182 | 2A | There are two 1.5V_RUN_PWRGD pulled up to 3.3V_ALW on sheet 49 AND to 3.3V_SUS on sheet 44. | Done. PR125 no stuff. |
| | 51 | 50 | 8/29/2006 9/8/2006 | | WI88477 | 2A | Changes to VCC_GFX_CORE regulator. | 1) Delete "1.5V +/- 5%" note at top of page 50. Incorrect. 2) Better FETs will probably need to be chosen. Junction temperatures will reach too high for FDS8880 and FDS6676AS. |
| | 52 | 50 | 8/29/2006 | | WI88174 | 2A | Proper setting for voltage dividers at +VCC_GFX_CORE.Regulated voltage at +VCC_GFX_CORE should be 1.0 and 1.1V, depending on the state of GFX_CORE_CNTRL. The current values of PR217 (2k), PR218 (3.4k), and PR225 (75k) give calculated output values of 1.11 and 1.13V. | Done. Delete PQ52 ,PR229 and PR230. Chang PR217 to 24.9K , PR218 to 57.6K and PR225 to 150K. |
| | 53 | 51 | 8/29/2006 9/1/2006 | | WI88154 | 2A | Changes to Vcore circuit. | On sheet 51, Vcore regulator, change PR26 from NC to install (13K). Add a cap, 2.2nF/0402_NC, in parallel with PC127, depopped. Delete PR145. |
| 54 | 52 | 8/29/2006 | | WI88472 | 2A | Changes to 3.3V_ALW regulator. | 1) Depop PR54 to change switching frequency from 500kHz to 300kHz. 2) 3.3V regulator needs another 10uF input cap to go along with PC65 and PC67. 3) One 330uF output cap will have its ripple rating exceeded, and ESR is too high for 2% output ripple. Add another 330uF in parallel with PC68. | |
| | | | | | | | | <div><div><div><div><div></div><div>QUANTA</div><div>COMPUTER</div></div><div><div>Title</div><div>Change list</div></div><div><div>Size</div><div>Document Number</div><div>Rev</div></div><div>JM7B</div><div>2A</div><div><div>Date:</div><div>Thursday, September 14, 2006</div><div>Sheet</div><div>3</div><div>of</div><div>5</div></div></div></div></div> |

| Model | Item | Page | Date | ECN Number | Item Id | Rev. | Issue Description | Solution Description | |
|-------|------|-------|------------------------|------------|---------|------|---|--|---|
| JM7B | 55 | 52 | 8/29/2006 | | WI88163 | 2A | 3V/5V regulator, change enable divider. | On sheet 52, change PC214 back to a 200k resistor. That was the original value. It was changed to a cap to fix a MAX8778 problem, which is no longer used on Dawson/Fila. | |
| | 56 | 54 | 8/29/2006 | | WI86725 | 2A | Change PQ45 and PQ46 in DCIN ckt. | On sheet 54, replace PQ45 and PQ46 with the IMD2A BJT package. The Vgs rating of the Si2301BDS is too low. | |
| | 57 | 32 | 9/1/2006 | | WI89654 | 2A | Update ECE5028 pinout.Per the SMCSC ECE5028 v02 spec, the pins 36, 37, 51, and 52 do not change definition from the ECE5018. Please swap pins 36 and 37. In addition, swap pins 51 and 52. | Swap pin36,37 and pin 51,52 and rename pin 58 from BC_INT to BC_INT#. | |
| | 58 | 13 | 9/1/2006 9/2/2006 | | WI88948 | 2A | Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update. | Change R588 from 10K to 8.2K and no stuff. Depop R593 and Pop R588. | |
| | 59 | 29 | 9/1/2006 | | WI88803 | 2A | Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN. | Done. | |
| | 60 | 31,44 | 9/4/2006 9/5/2006 | | WI89814 | 2A | Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel. | Remove 3.3V_LAN_PWRGD circuit from page 44 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND. | |
| | 61 | 28 | 9/4/2006 | | WI89602 | 2A | No Connect pin 4 OZ77CR6.Recommendation from O2 Micro is to leave pin 4 of the OZ77CR6 as no connect. | Done. | |
| | 62 | 31 | 9/4/2006 | | WI75516 | 2A | External Work Around Circuit for MEC5025 can be removed.The need for the external work around circuit for the MEC5025 does not exist. Please remove this circuit. | Done. | |
| | 63 | 52 | 9/4/2006 | | WI89781 | 2A | Populate PC67 and PC121 in the 3.3V_ALW regulator. These two caps need to be populated for 3.3V and 5V input ripple requirements. | Done. | |
| | 64 | 52 | 9/4/2006 | | WI88782 | 2A | On sheet 52, add a feedback voltage divider on +3.3V_ALWP.In the current schematic, we are unable to margin test 3.3V. It can only be set to 0-2V and 3.3V. | Add a voltage divider like R26 and R27 in the attached file (connects to +3.3V_ALWP, analog ground, and pin 30). The two resistors should be no-connect. | |
| | 65 | 31 | 9/6/2006 | | WI90153 | 2A | Integrate 0-ohm pull-down resistor on ATI_Intel net. Please integrate a 0-ohm pull-down resistor on ATI_Intel net. This is to have as a place holder to account for any possible issues with the default state of this pin. | Add R502 to GND for ATI_Intel. | |
| | 66 | 50 | 9/6/2006 | | WI90252 | 2A | SCH X01- GFX_CORE_CNTRL requires a pullup. On sheet 50, GFX_CORE_CNTRL requires a 10k pullup to +3V_RUN | Add Pullup PR229 for GFX_CORE_CNTRL. | |
| | 67 | 36 | 9/7/2006 | | WI90472 | 2A | Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5. | Please change the WLAN LED implementation to advice from Dell. | |
| | 68 | 31 | 9/7/2006 | | WI90541 | 2A | Per Broadcom, GPIO0 signal on BCM5755M is an open-drain signal. Hence, needs a stronger pull-up. | Change pull-up on LOM_SMB_ALERT# signal to 4.7K | |
| | 69 | 52 | 9/8/2006 | | WI90729 | 2A | Change switching freq and hi-side FET for +3.3V_ALWP.Change PQ21 to BSC079N03.This FET package will require a layout change. | Change PQ21 to FDS8880_NL. | |
| | 70 | 36 | 9/9/2006 | | WI90456 | 2A | Need to remove RC on WLAN Sniffer circuit.Need to remove R272, R289, C272, and C311 on the sniffer circuit. This RC on those lines is not part of the reference schematic and would just slow those lines down. | Change R272, R289 from 10K to 0 ohm, depopulate C272,C311. | |
| | 71 | 40 | 9/9/2006 | | WI90542 | 2A | Change LOM RDAC & Termination component values to improve IEEE results.some of the test results in the IEEE test suite are marignally passing. Results show variation from system to system (due to component variation, board-to-board impedance variation, etc). Hence, need to make sure of sufficient margins to account for these variations. | Change R48 to 1.13K, 1%. This will allow us to increase amplitude in the 100M & 1G template tests, and to compensate for some of the amplitude loss due to the next change. Change R351, R352, R358, R362, R65, R366, R468, R370 to 2K-ohm, 1% and change C407, C410, C416, C423 to 0.1uF. Populate all for X01. This helps in improving the return loss at the lower frequencies | |
| | 72 | 41 | 9/11/2006 | | WI91075 | 2A | WWAN Noise - LOM Improvement - Additional decoupling on +3.3V_ALW.There's no decoupling on the +3.3V_ALW that sources the +3.3V_LAN and other LOM Voltage rails. The +3.3V_ALW traces across the board (near the edges) and is noisy. Add 4.7uF (0805 pkg), 1uF (0603 pkg) and 0.1uF (0402 pkg) near PQ41 (on UMA) or PQ47 (on DIS) to provide some decoupling on this voltage rail near the LOM. | Add PC218,PC219,PC220 on +3.3V_ALW. | |
| | 73 | 47,52 | 9/11/2006 9/12/2006 | | WI91174 | 2A | FDS7066 will be EOL.Because FDS7066ASN3 will be EOL. | Change PQ35 and PQ22 from FDS7066ASN3 to SI4336DY-T1-E3 and PR110 to 23.2K and PR65 to 137K for setting OCP. | |
| | 74 | 48,51 | 9/11/2006 9/12/2006 | | WI91176 | 2A | FDS7088 will be EOL.Because FDS7088SN3 will be EOL. | Change PQ7,PQ8,PQ9 and PQ13 from FDS7088SN3 to SI7336ADP and change PR221 to 162K for setting OCP. | |
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| | | | | | | | | | <div><div><div><div><div></div><div>QUANTA</div><div>COMPUTER</div></div><div><div>Title</div><div>Change list</div></div><div><div>Size</div><div>Document Number</div><div>Rev</div></div><div><div>JM7B</div><div></div><div>2A</div></div><div><div>Date:</div><div>Thursday, September 14, 2006</div><div>Sheet</div><div>4</div><div>of</div><div>5</div></div></div></div></div> |

| Model | Item | Page | Date | ECN Number | Item Id | Rev. | Issue Description | Solution Description |
|---|------|-------|------------------------|------------|---------|------|---|---|
| JM7B | 75 | 52 | 9/11/2006 9/12/2006 | | WI90729 | 2A | Change switching freq and hi-side FET for +3.3V_ALWP.Intersil has discovered an errata in the controller that produces a problem when using 300kHz at 3.3V. They are still digging into the details, but feel confident they can remove this problem with a silicon change. They have assured us we will not have any problem switching at 500kHz at 3.3V. We will, however, need to provide a better FET package that will perform well at this frequency. | Populate PR54 with zero Ohms to change switching frequency from 300kHz to 500kHz on +3.3V_ALWP. Change PQ21 to BSC079N03. This FET package will require a layout change. |
| | 76 | 17 | 9/12/2006 | | WI90831 | 2A | LAY X01- WWAN Noise- Clock. Add ferrite bead in series with R492. | Add L64 in series with R441. |
| | 77 | 12,14 | 9/12/2006 | | WI90828 | 2A | LAY X01- WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add 4 .1uF caps in parallel to C661(UMA)/C813(Disc) close to the ICH pins. Add 4 .1uF caps in parallel to C674(UMA)/C825(Disc) close to the ICH pins. | Add C871~C876 for USB OC. Add C867~C870 in parallel to C813. Add C748,C864~C866 in parallel to C825. |
| | 78 | 40 | 9/12/2006 | | WI90824 | 2A | WWAN Noise - LOM continued. Try to add one more cap (1 uF) on each analog voltage input to 5755 (1.2V_AVDDL, 1.2V_GPHY_PLLVDD, 1.2V_PCIE_PLLVDD, 1.2V_PCIE_SDSVDD, 2.5V_BIASVDD, 2.5V_XTALVDD, 2.5V_AVDD) | Done. |
| | 79 | 40 | 9/12/2006 | | WI90823 | 2A | LAY X01- WWAN Noise - LOM improvement. 1) +2.5V_XTALVDD: Change L18 to 0805 package (larger variety of values available in this package size). 2) +2.5V_AVDD: Add one more 0402 capacitor near L14 and U30.F12 | 1).Change the package of L18 from 0603 to 0805 and use BLM21PG600SN1D instead of BLM18AG601SN1D. 2). Add C168 near L14 and U30.F12 |
| <div><div><div>QUANTA COMPUTER</div></div><div><div>Title</div><div>Change list</div></div><div><div>Size</div><div>Document Number</div><div>Rev</div></div><div><div>JM7B</div><div></div><div>2A</div></div><div><div>Date:</div><div>Thursday, September 14, 2006</div><div>Sheet</div><div>5</div><div>of</div><div>5</div></div></div> | | | | | | | | |