Kyloren 15" Schematics
KabyLake - U/R

2017-6-20

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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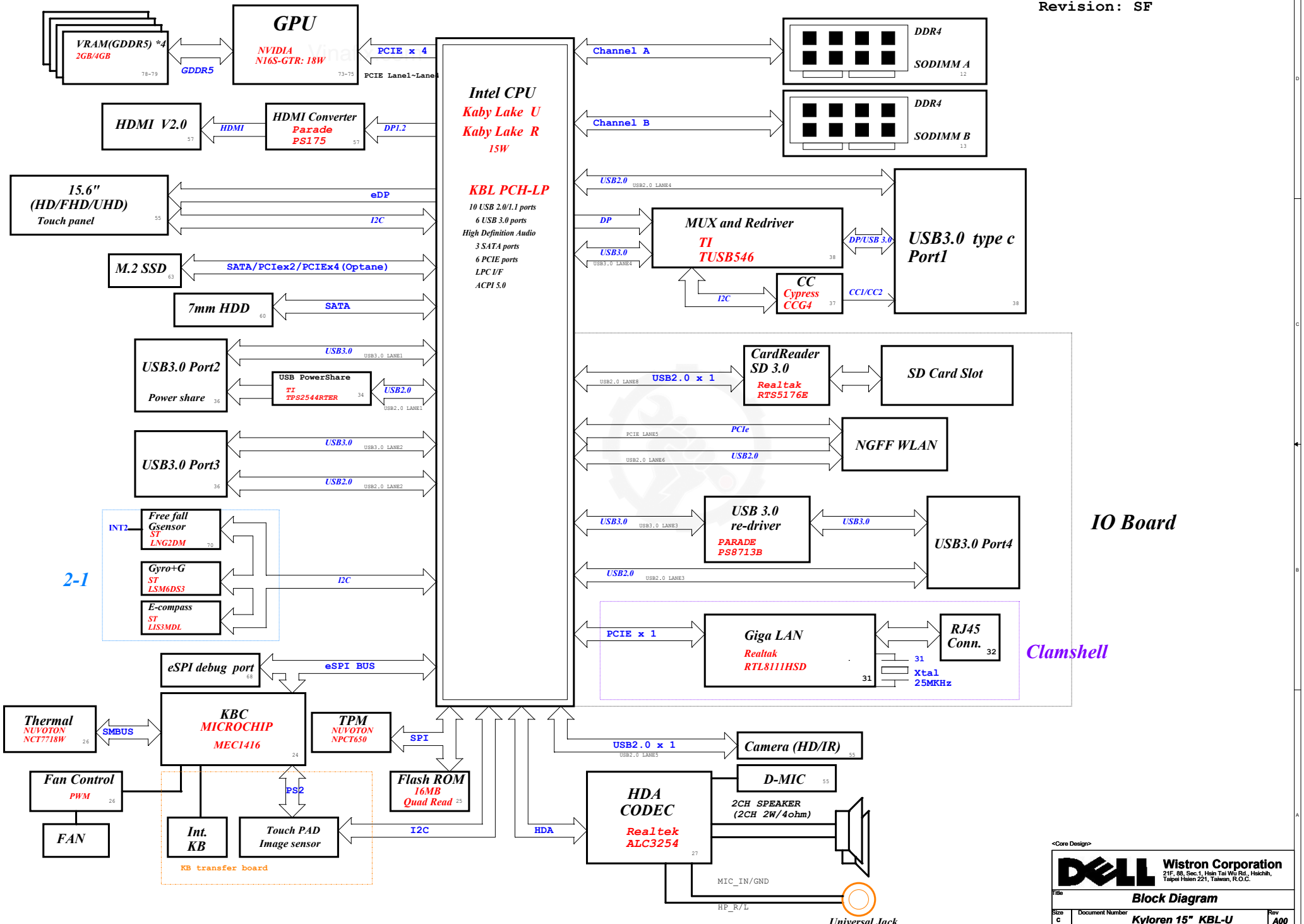
Title: *Cover Page*		
Size: A3	Document Number: Kyloren 15" KBL-U	Rev: A00
Date: Tuesday, June 20, 2017	Sheet 1 of 106	

Kylo Ren 15" CPU 15W + GPU 18W Block Diagram

Project code: 4PD0CL010001
PCB P/N: 16841
Revision: SF



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Title	Block Diagram	
Size: C	Document Number: Kyloren 15" KBL-U	Rev: A00
Date: Tuesday, June 20, 2017	Sheet 2 of 106	

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Title: *(Reserved)*

Size	Document Number	Rev
C	*Kyloren 15" KBL-U*	*A00*

Date: Tuesday, June 20, 2017 Sheet 3 of 106

Main Func = CPU

#544669 CRB Rev0.52

+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

<24> H_PECI_CPU
<24,44,46> H_PROCHOT#

R401 1KR2J-1-GP
499R2F-2-GP R403
TPAD14-OP-GP

TP401 TPAD14-OP-GP
TP402
TP405 TPAD14-OP-GP
TP406 TPAD14-OP-GP

H_CATERR#
H_PROCHOT# R
PCH_THERMTRIP#
1SKTOCC#
XDP_BPM0
XDP_BPM1

+VCCST_CPU
R419 1KR2J-1-GP
PCH_THERMTRIP#
EC401 AZ5725-01FDR7G-GP DY
EMI DVT1 0210

CPU1D 4 OF 20
SKYLAKE_ULT

CATERR# D63
PECI A54
PROCHOT# C65
THERMTRIP# C63
SKTOCC# A65

CPU MISC
BPM#[0] C55
BPM#[1] D55
BPM#[2] B54
BPM#[3] C56

JTAG
PROC_TCK B61 XDP_TCLK
PROC_TDI D60 XDP_TDI
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS
PROC_TRST# B59 XDP_TRST#

<55> TOUCH_PANEL_INTR#
TOUCH_PAD_INTR# BA5
<55> TOUCH_PANEL_PD# AY5

GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

PCH_JTAG_TCK B56 PCH_JTAG_TCK
PCH_JTAG_TDI D59 PCH_JTAG_TDI
PCH_JTAG_TDO A56 PCH_JTAG_TDO
PCH_JTAG_TMS C59 PCH_JTAG_TMS
PCH_TRST# C61 XDP_TRST#
JTAGX A59 XDP_TCK_JTAGX

3D3V_S5_PCH
R404 1 DY 2 100KR2J-1-GP

49D9R2F-GP R412 1 CPU_POPIRCOMP AT16
49D9R2F-GP R413 1 PCH_POPIRCOMP AU16
49D9R2F-GP R414 1 EDRAM_OPIO_RCOMP H66
49D9R2F-GP R415 1 EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

SKYLAKE-U-GP

071.SKYLA.000U

<24,65> TP_WAKE_KBC#
R410 1 2 0R0402-PAD

X02 20170316 change

+VCCSTG = 1.0 V

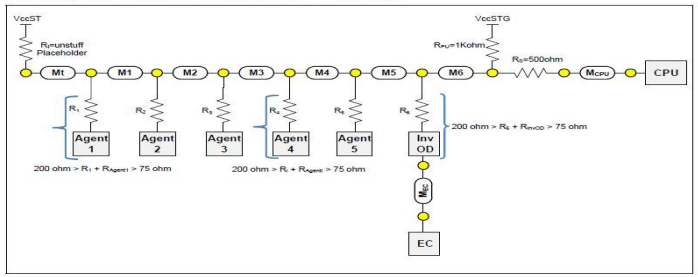
XDP_TMS 1 DY 2 R421 51R2J-2-GP
XDP_TDI 51R2J-2-GP1 DY 2 R422 51R2J-2-GP
XDP_TDO_CPU 1 DY 2 R423 51R2J-2-GP
PH in P.99

PCH_JTAG_TDI 1 R408 51R2J-2-GP
PCH_JTAG_TDO 1 R409 51R2J-2-GP
PCH_JTAG_TMS 1 R416 51R2J-2-GP
XDP_TCK_JTAGX 1 DY 2 R417 1KR2J-1-GP

XDP_TRST# R402 1 DY 2 51R2J-2-GP
XDP_TCLK R406 1 DY 51R2J-2-GP
PCH_JTAG_TCK R407 1 DY 51R2J-2-GP

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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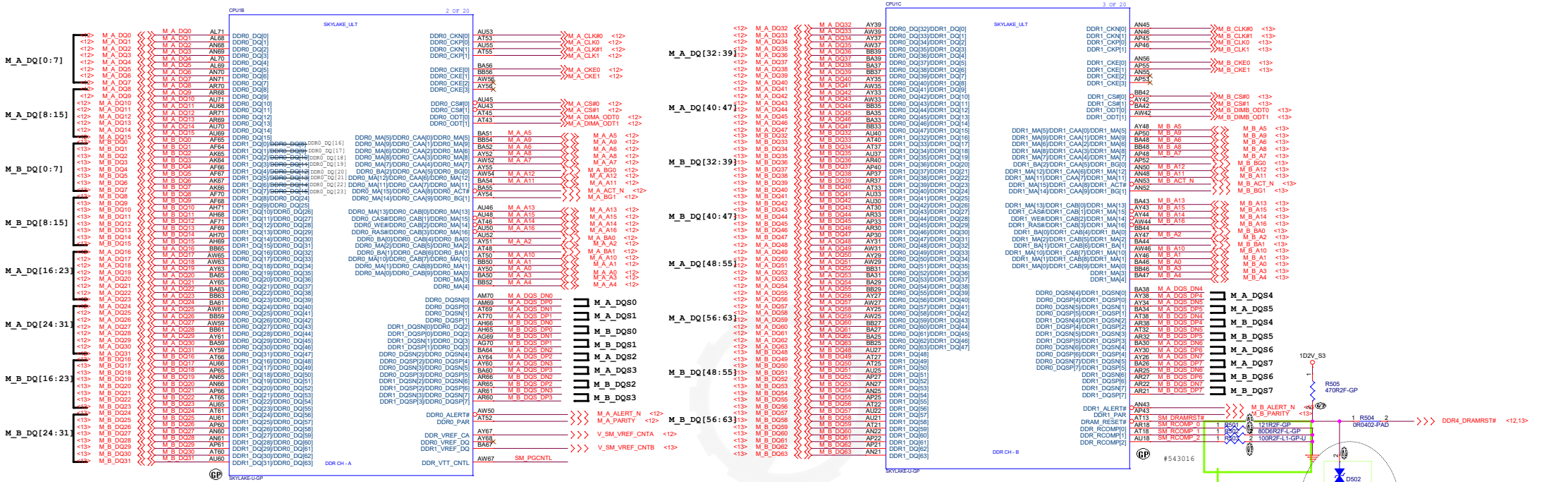
Title: CPU_(JTAG/CPU SIDE BAND)

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 4 of 106

Main Func = CPU

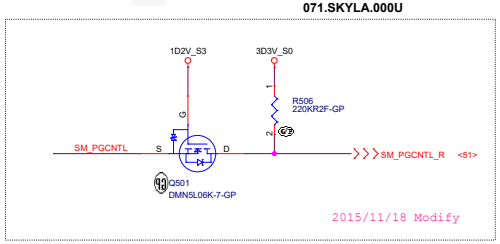
DDR4 ball type: Interleaved Type



071.SKYLA.000U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

071.SKYLA.000U



Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

Layout Note:

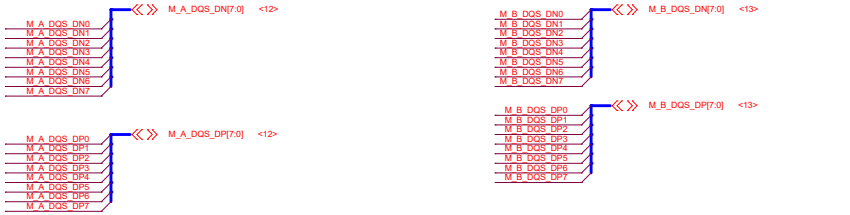
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT . Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks. when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z)
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.



<Core Design>

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Title: CPU_(DDR)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

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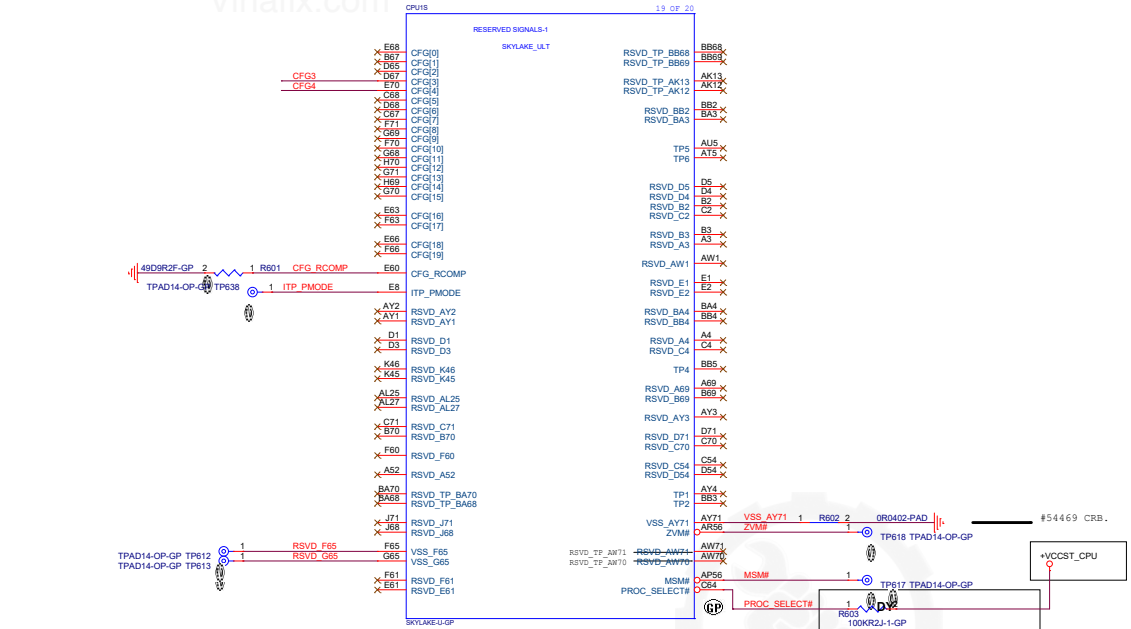
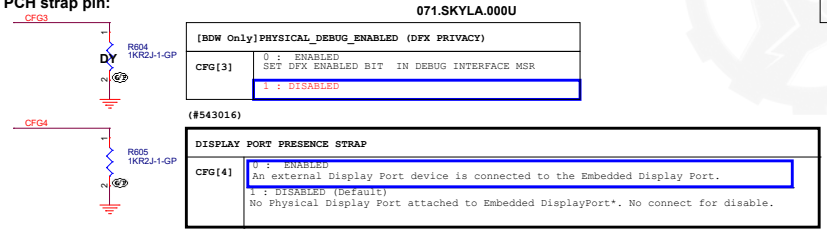
Main Func = CPU



PCH strap pin:



071.SKYLA.000U

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

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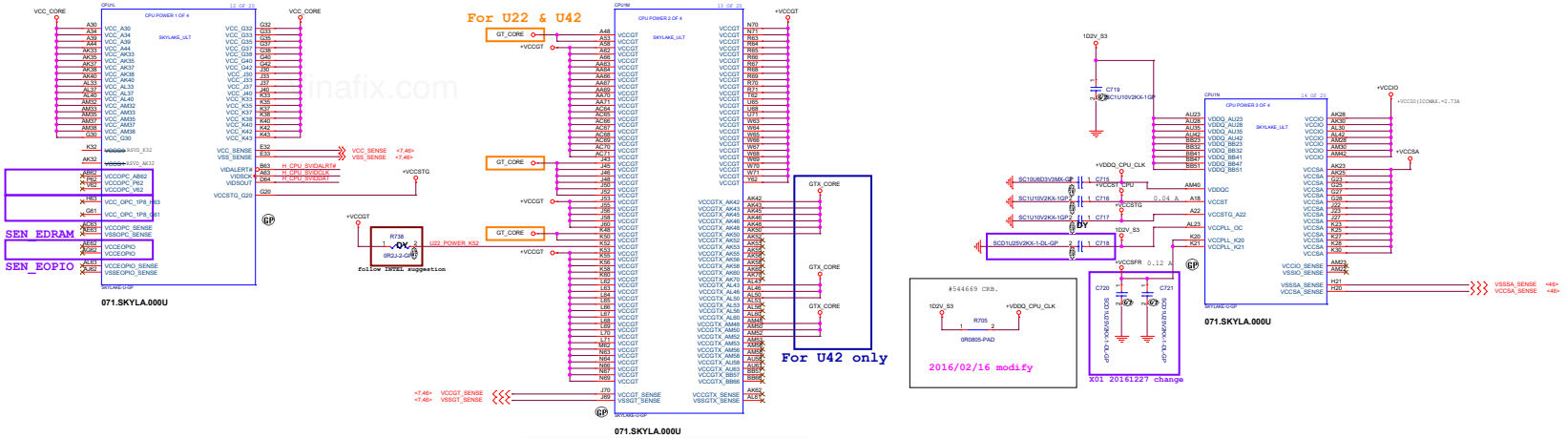
Title: CPU_(RESERVED)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 6 of 106

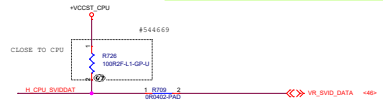
Main Func = CPU



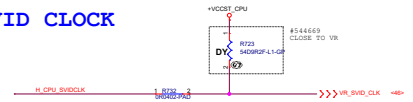
SVID_543016:

SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK



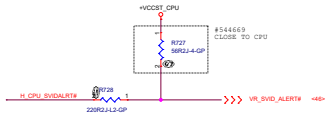


Figure 10-7. Routing Illustration for SVID Topology

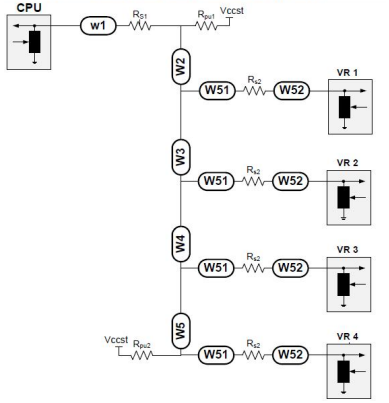


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU0} [Ω]	R_{PU1} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCCpr [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

<Core Design>

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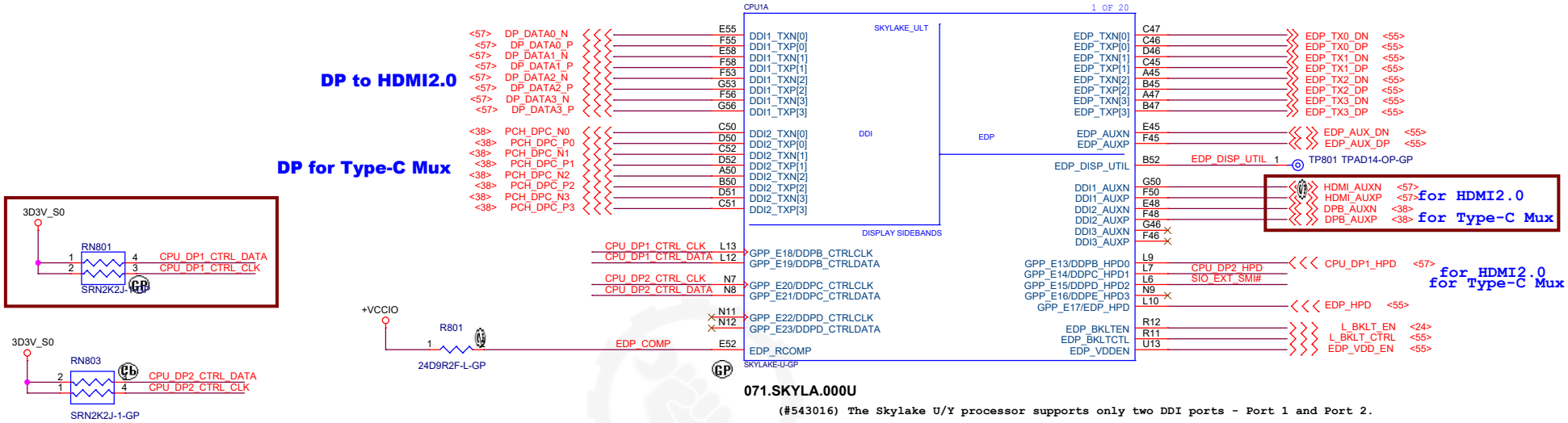
Title: CPU(VCC_CORE)

Size: A1 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 7 of 100

Main Func = CPU



071.SKYLA.000U

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

X02 20170316 change

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title	CPU_(DISPLAY)	
Size: A3	Document Number: Kyloren 15" KBL-U	Rev: A00
Date: Tuesday, June 20, 2017	Sheet 8 of 106	

Main Func = CPU

(Blanking)

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Title: (Reserved)

Size: A3 | Document Number: Kyloren 15" KBL-U | Rev: A00

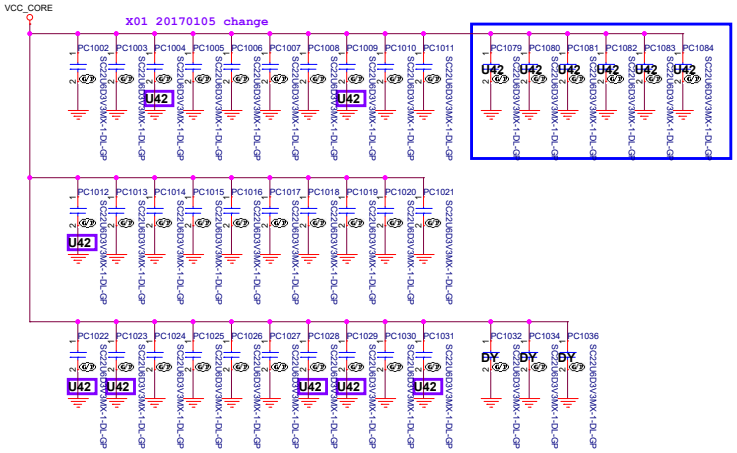
Date: Tuesday, June 20, 2017 | Sheet 9 of 106

Main Func = CPU

VCC_CORE

U-line 22 15W
IccMax current-10ms max = 31 A

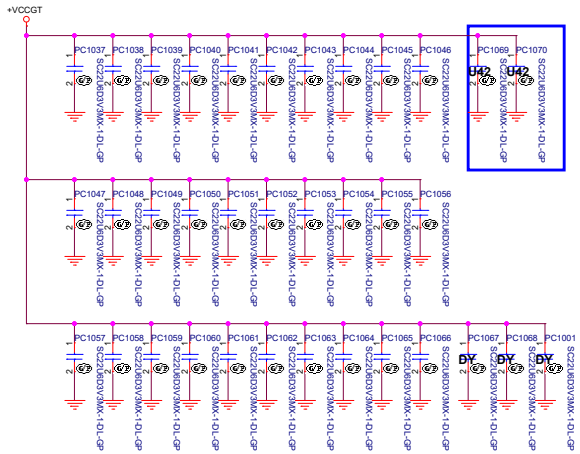
22U 0603 x 30 (3DY)



VCCGT

U-line 22 15W
IccMax current-10ms max[A] = 64 A

22U 0603 x 30 (3 DY)



VCCSA

22U 0603 x 8 (3DY)

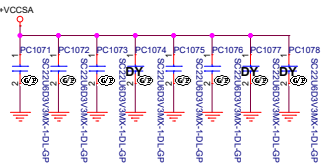


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

<Core Design>

Wistron Corporation
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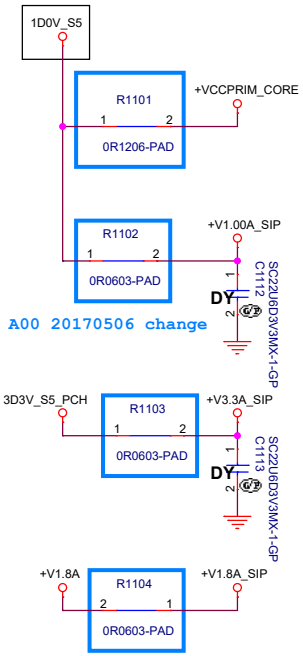
Title: CPU_(Power CAP1)

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

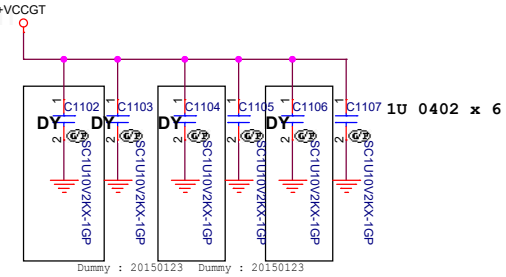
Date: Tuesday, June 20, 2017 | Sheet 10 of 106

Main Func = CPU

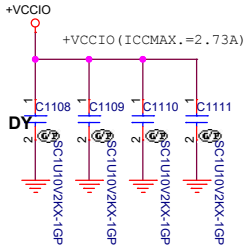
PCH DERIVED RAILS

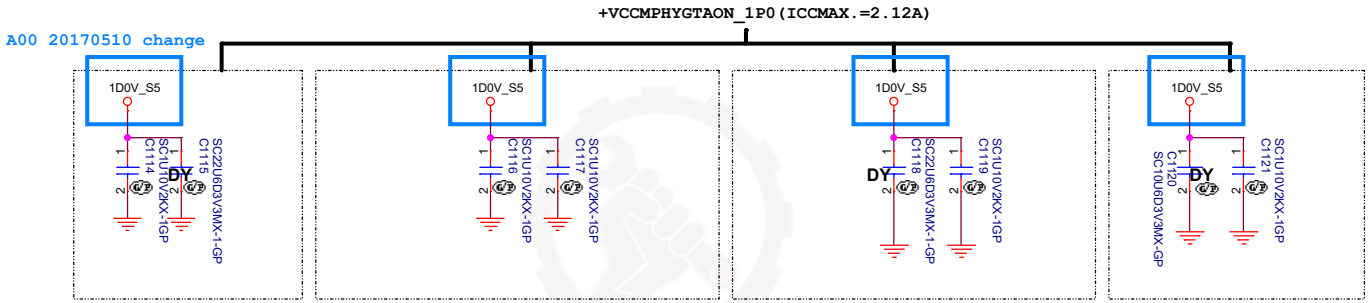


UNSLICED GT



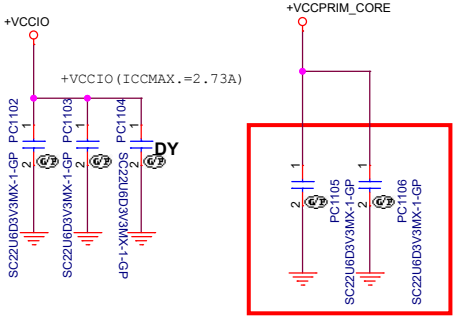
VCCIO



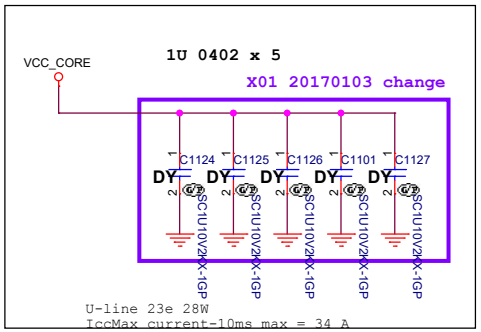


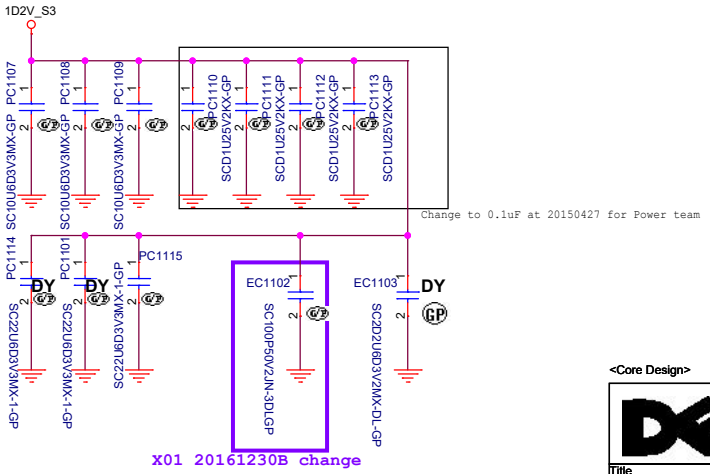
Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15



Size:0805 change to 0603
20141117





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 11 of 106

Main Func = MEMORY

DM1A 1 OF 4

DDR4-260P-65-GP

062.10011.01C1

DM1B 2 OF 4

DDR4-260P-65-GP

DM1C 3 OF 4

DDR4-260P-65-GP

DM1D 4 OF 4

DDR4-260P-65-GP

Layout note: closed to Dimm

X01 20161227 change

跟sw確認

X01 20170109 change

RF request 2016/01/12 modify

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 12 of 106

Main Func
= MEMORY

By layou modify 20150916

By layou modify 20150916

DM2A 1 OF 4

DM2B 2 OF 4

DM2C 3 OF 4

DM2D 4 OF 4

DDR4-260P-64-GP

062.10011.01B1

Layout note: closed to Dimm

A00 20170508 change

X01 20161227 change

X01 20170109 change

跟sw確認

RF request 2016/01/12 modify

RF request 2016/01/12 modify

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 13 of 106

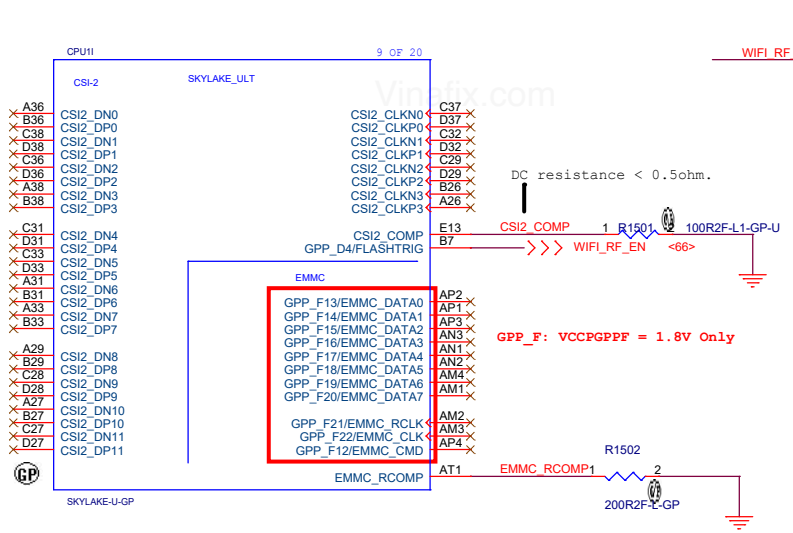
(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)_SODIMM _SODIMM4*		
Size: A4	Document Number: *Kyloren 15" KBL-U*	Rev: *A00*
Date: Tuesday, June 20, 2017	Sheet 14 of 106	

Main Func = PCH



071.SKYLA.000U

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

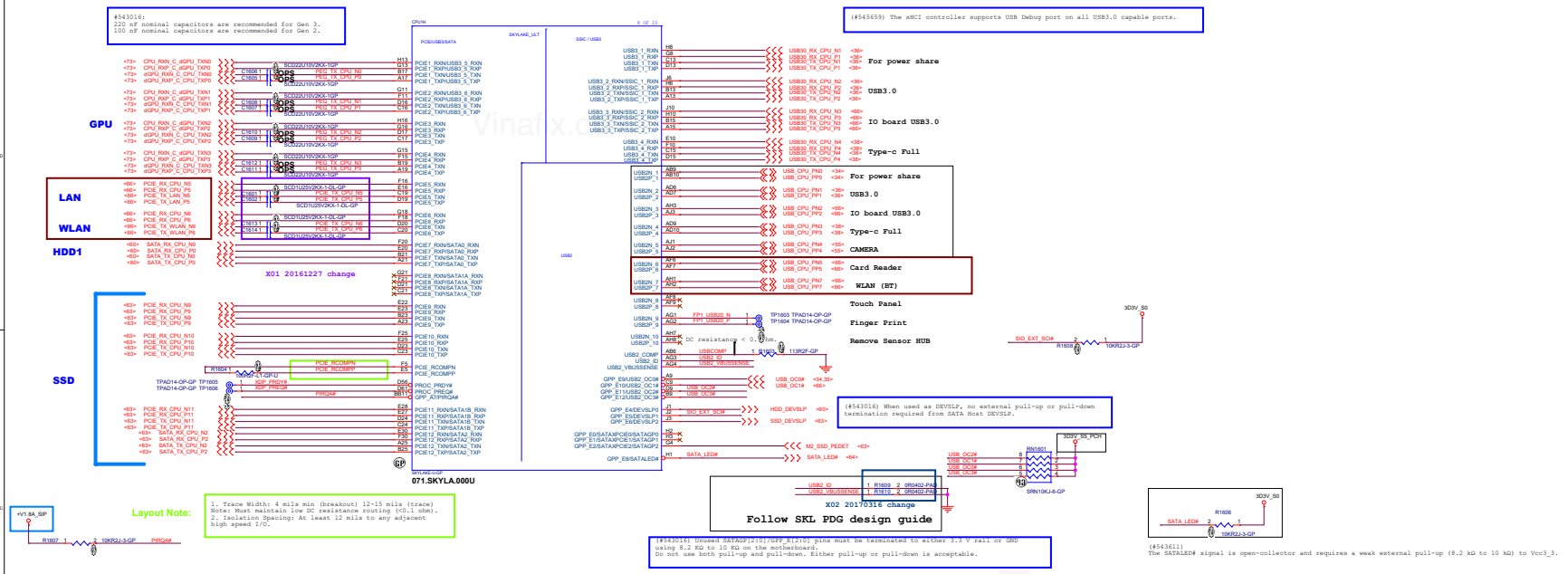
GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)
Size: A3 | Document Number: Kyloren 15" KBL-U | Rev: A00
Date: Tuesday, June 20, 2017 | Sheet 15 of 106



#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

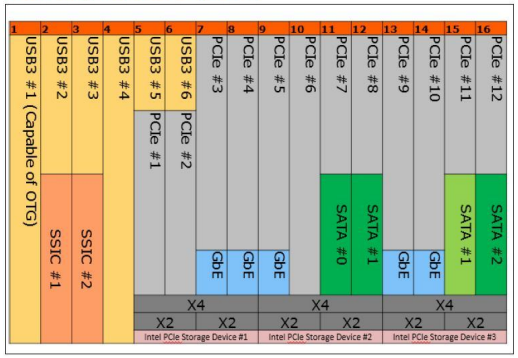


Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Main Func = PCH

R1709,R1723,R1703,R1724 merge to RN1704

RN1704 — AC_PRESENT, PCIE_WAKE# CPU, PCH_BATLOW#, GPD11/LANPHYPC — SRN10KJ-6-GP

2PD11 pull high by Intel PDG1.3 request

3D3V_S5 — R1711 0R0603-PAD — +VCCPDSW_3P3

Layout note: 3 PAD SHARING

RTC_AUX_S5 — R1730 330KR2J-L1-GP — SM_INTRUDER#

#544669 (CRB): 330k.

[#543016 Rev0.7] EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

+V3.3A_SIP — R1731 20KR2J-L2-GP — EXT_PWR_GATE#

#544669 Rev0.52 CRB: No PL resistor on THERMTRIP#.

H_CPUPWRGD — R1714 10KR2J-3-GP DY — EC1701 AZ5725-01FDR7G-GP DY

X01 20170103 change

RN1703 — PM_RSMRST#, PM_PCH_PWROK — SRN10KJ-5-GP

R1717 DY — 10KR2J-3-GP — SYS_PWROK

+V1.8A_SIP — R1738 DY — 10KR2J-3-GP — ME_SUS_PWR_ACK_R

ME_SUS_PWR_ACK_R — R1708 0R0402-PAD — SUSACK#_R

X02 20170316 change

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

+V3.3A_SIP — R1701 10KR2J-3-GP

TP1709 TPAD14-OP-GP — PCH_PLTRST# — XDP_DBRESET# — PM_RSMRST#

TP1705 TPAD14-OP-GP — H_CPUPWRGD — H_VCCST_PWRGD

X02 20170316 change

<24> SYS_PWROK, <24,26> RESET_OUT# — R1706 0R0402-PAD — PM_RSMRST# — R1704 0R0402-PAD

SYS_PWROK — PM_PCH_PWROK — PCH_DPWROK — DSW_PWROK

<24> LAN_WAKE# — R1707 10KR2J-3-GP — +VCCPDSW_3P3

PCIE_WAKE# CPU — LAN_WAKE# — GPD11/LANPHYPC

X01 20170109 change

ME_SUS_PWR_ACK_R — SUSACK#_R

(PDG#543016) WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

CPU1K — 11 OF 20 — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT — SKYLAKE-U-GP

071.SKYLA.000U

GPP_B12/SLP_S0# — SIO_SLP_S0# <24,40,91>
GPD4/SLP_S3# — SIO_SLP_S3# <24,27,40,51>
GPD5/SLP_S4# — SIO_SLP_S4# <40,54>
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
AUX_EN_WOWL <24,66>
GPD3/PWRBTN# — SIO_PWRBTN# <24>
GPD1/ACPRESENT — AC_PRESENT
GPD0/BATLOW# — PCH_BATLOW#
GPP_A11/PME# — SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# — EXT_PWR_GATE#
GPP_B2/VRALERT# — VRALERT# — TP1708 TPAD14-OP-GP

BATLOW#: Pull-up required even if not implemented.

AC_PRESENT — EC1707 DY — SCD1U16V2KX-3GP

+VCCMPHYGTAON_1P0

SKL: 1.0V

+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

1D0V_S5 — EC1710 DY — C1704 SC10U6D3V3MX-GP

A00 20170510 delete

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

<24,40> RUNPWROK — R1716 100KR2F-L1-GP — R1719 47KR2F-GP

H_VCCST_PWRGD — C1711 SCD011U50V2KX-1GP DY — EC1708 AZ5725-01FDR7G-GP DY

EC1709 AZ5725-01FDR7G-GP DY

EMI DVT1 0210

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

<26,63,66,73,91> PLT_RST# — R1715 100KR2J-1-GP DY — C1701 SC220P50V2KX-3GP DY — R1713 0R0402-PAD — PCH_PLTRST#

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

XDP_DBRESET#, SYS_PWROK, PLT_RST#, RESET_OUT#, 3V_5V_POK

EC1706 DY — EC1702 EC1703 EC1704 EC1705 AZ5725-01FDR7G-GP DY

SCKP50V2KX-1GP

EMI DVT1 0210

4th = 84.DMN66.03F
3rd = 75.00601.07C
2nd = 84.2N702.E3F
84.2N702.A3F

3D3V_AUX_S5 — R1737 NON DS3 100KR2J-1-GP — PM_RSMRST#_M

D1701 RB751V-40H-GP — ACOK_IN_M <43,44>

Q1702 2N7002KDW-GP NON DS3 — PM_RSMRST#_R — R1720 0R0402-PAD — PM_RSMRST#

83.R2004.G8F

AC_PRESENT

X02 20170316 change

Reserve by NON DS3 function 20150413

3D3V_AUX_S5 — R1727 100KR2J-1-GP NON DS3 — R1726 10KR2J-3-GP

Q1701 PJT138KA-GP — vth=1.1V

3V_5V_POK# — PM_RSMRST# 1 — R1702 1KR2J-1-GP — 3V_5V_POK_C — R1728 0R0402-PAD — 3V_5V_POK <40,45,52,56>

PCH_RSMRST# <24>

X02 20170316 change

075.00138.0A7C

X02 20170314 change

C1710 SCD47U10V2KX-GP DY — EC1712 SCD1U16V2KX-3GP DY

Dummy C1710 by it's useless

EC1711 modify to 100k and 0.01uF at DVT1 20150203

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 17 of 106

Main Func = PCH

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH Prim

R1835 and R1834 merge to RN1802
2015/10/06 modify

R1806,R1807,R1808,R1809 merge to RN1803
2015/10/06 modify

X01 20170109 change

A00 20170508 add

For eSPI

RCIN#:
Frequency to Avoid: 33 MHz

071.SKYLA.000U

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6: 0 = SPI (Default); 1 = LPC. Notes: 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC. Notes: 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

X01 20170103 change
X02 20170302 change
X01 20170110 change
X02 20170314 change
A00 20170425 change
X01 20161223 add
X01 20170109 change

Layout: Place at the open door area.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPC/SPI/SMBUS/CL/CLK)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 18 of 106

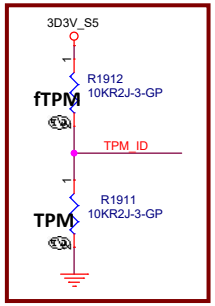
Main Func = PCH

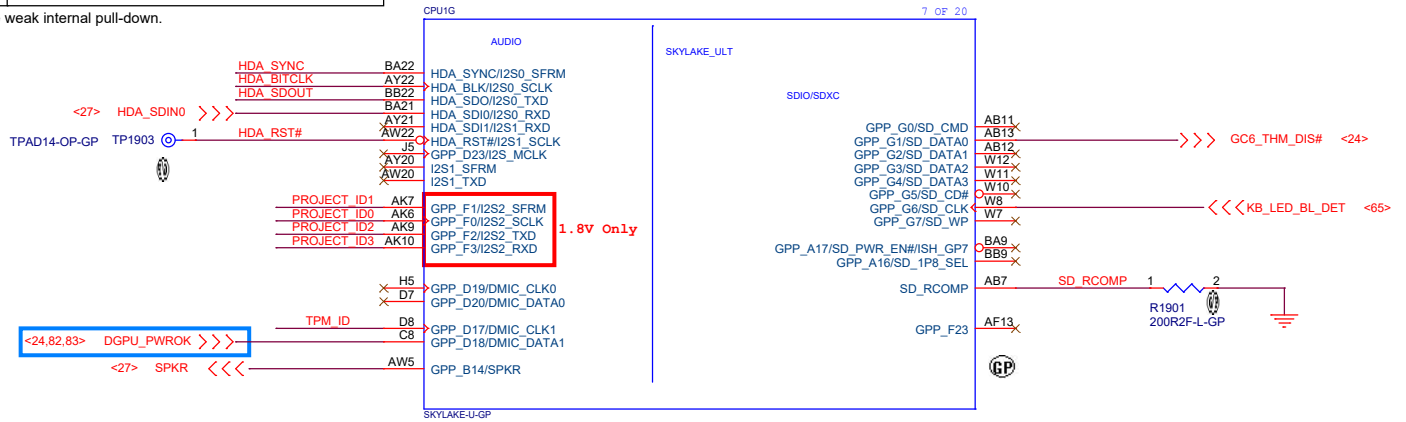
Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

dTPM support: 0
non-dTPM: 1





PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

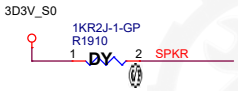
The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

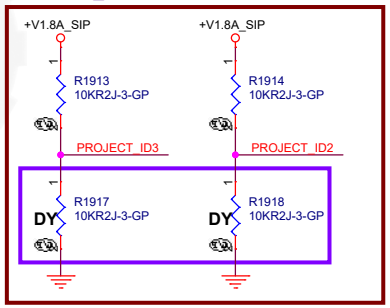
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

071.SKYLA.000U

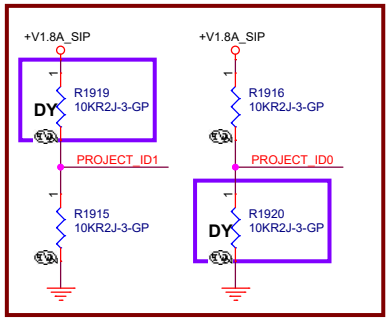


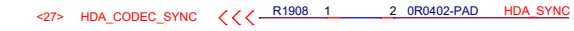
PROJECT_ID[3:2] 11: Inspiron

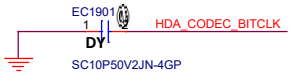


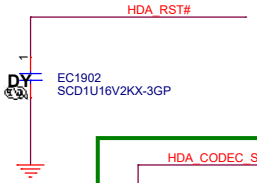
X01 20170109 add

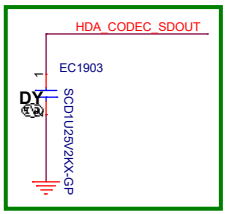
PROJECT_ID[1:0] 01: 7000 Series

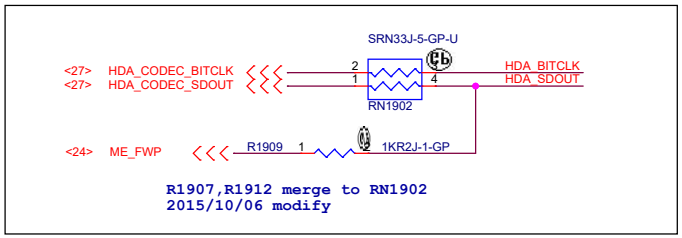












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 19 of 106

Main Func = PCH

X01 20170103 change

EC2002 DY 1K/P50V2KX-1DLGP

DGPU_HOLD_RST# <73>

X01 20170110 change

RN2009 OPS SRN10KJ-5-GP

DGPU_HOLD_RST#

DGPU_PWR_EN#

X02 20170316 change

R2003 0R0402-PAD

R2004 0R0402-PAD

GPU_EVENT_MCP#

GC6_FB_EN_MCP

VRAM_ID1

NRB_BIT

<76> GPU_EVENT#

<75,76,83> GC6_FB_EN

CPU1F

6 OF 20

LPSS

SKYLAKE_ULT

ISH

GPP_B15/GSPI0_CS#

GPP_B16/GSPI0_CLK

GPP_B17/GSPI0_MISO

GPP_B18/GSPI0_MOSI

Strap

<55> DBC_PANEL_EN

GPP_B19/GSPI1_CS#

GPP_B20/GSPI1_CLK

GPP_B21/GSPI1_MISO

GPP_B22/GSPI1_MOSI

GPP_D0/ISH_SPI_CS#

GPP_D1/ISH_SPI_CLK

GPP_D11/ISH_SPI_MISO

GPP_D12/ISH_SPI_MOSI

GPP_D5/ISH_I2C0_SDA

GPP_D6/ISH_I2C0_SCL

GPP_D7/ISH_I2C1_SDA

GPP_D8/ISH_I2C1_SCL

GPP_F10/I2C5_SDA/ISH_I2C2_SDA

GPP_F11/I2C5_SCL/ISH_I2C2_SCL

1.8V Only

GPP_D13/ISH_UART0_RXD/SML0BDATA

GPP_D14/ISH_UART0_TXD/SML0BCLK

GPP_D15/ISH_UART0_RTS#

GPP_D16/ISH_UART0_CTS#/SML0BALERT#

GPP_C12/UART1_RXD/ISH_UART1_RXD

GPP_C13/UART1_TXD/ISH_UART1_TXD

GPP_C14/UART1_RTS#/ISH_UART1_RTS#

GPP_C15/UART1_CTS#/ISH_UART1_CTS#

GPP_A18/ISH_GP0

GPP_A19/ISH_GP1

GPP_A20/ISH_GP2

GPP_A21/ISH_GP3

GPP_A22/ISH_GP4

GPP_A23/ISH_GP5

GPP_A12/BM_BUSY#/ISH_GP6

SKYLAKE-U-GP

071.SKYLA.000U

DGPU_HOLD_RST#

IR_CAM_DET# <55>

RTC_DET# <25>

ISH_I2C0_SDA R2021 0R0402-PAD

ISH_I2C0_SCL R2020 0R0402-PAD

SENSOR_I2C_SDA <55,70>

SENSOR_I2C_SCL <55,70>

X02 20170316 change

I2C1_SDA

I2C1_SCL

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

VRAM_ID2

DGPU_PWR_EN# <83>

X01 20170110 change

BOARD_ID1

FFS_INT2 <70>

A00 20170506 change

ISH_KB_DISABLE

GSEN_INT1 <55>

GSEN_INT2 <55>

GSEN2_INT1_C <70>

GSEN2_INT2_C <70>

GYRO_INT_C <70>

GYRO_DRDY <55>

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

X02 20170314 change

3D3V_S0

RN2007 SRN1KJ-7-GP

ISH_I2C0_SCL

ISH_I2C0_SDA

RN2008 SRN2KJ-1-GP

I2C1_SCL

I2C1_SDA

3D3V_S0

DEBUG

51KR2J-1-GP R2048 UART_2_CRXD_DTXD

51KR2J-1-GP R2049 UART_2_CTXD_DRXD

DEBUG

10KR2J-3-GP R2042 BLUETOOTH_EN

10KR2J-3-GP R2043 DBC_PANEL_EN

10KR2J-3-GP R2044 FFS_INT2

10KR2J-3-GP R2045 KB_DET#

10KR2J-3-GP R2046 IR_CAM_DET#

10KR2J-3-GP R2047 SPK_ID

SPK_ID 1: YG

0: FG

R2039 0R2J-2-GP

<55> TOUCH_DETECT

X01 20170103 add

<29> SPK_ID

<66> BLUETOOTH_EN

LCD_CBL_DET#

BOARD_ID2

X01 20170109 change

<68> UART_2_CRXD_DTXD

<68> UART_2_CTXD_DRXD

UART_2_CRXD_DTXD

UART_2_CTXD_DRXD

<24> SIO_EXT_WAKE#

<65> KB_DET#

PTP

<65> I2C0_SDA_TCH_PAD

<65> I2C0_SCL_TCH_PAD

Touch panel

<55> I2C0_SDA_TCH_PNL

<55> I2C0_SCL_TCH_PNL

+V1.8A_SIP

MEM_CONFIG [1..4]

1.8V Only

PCH Prim

3D3V_S5_PCH

R2007 1KR2J-1-GP

NRB_BIT

R2019 1KR2J-1-GP

R2031 10KR2J-3-GP GSEN_INT1_ISH

R2032 10KR2J-3-GP GSEN_INT2_ISH

R2033 10KR2J-3-GP GSEN2_INT1_ISH

R2034 10KR2J-3-GP GSEN2_INT2_ISH

R2035 10KR2J-3-GP GYRO_INT_ISH

R2036 10KR2J-3-GP GYRO_DRDY_ISH

3D3V_S0

R2053 10KR2J-3-GP

GYRO_DRDY_ISH

X02 20170316 add

3D3V_S5

R2001 10KR2F-2-GP

2IN1

KB_DISABLE_CPU_R

Vth(max)=1.1V

Q2001 2IN1

ISH_KB_DISABLE

NB_MODE# <24>

PJT138KA-GP

075.00138.0A7C

3D3V_S5

R2050 10KR2J-3-GP

2IN1

NB_MODE#

R2002 10KR2J-3-GP

CLAM

3D3V_S5_PCH

R2040 1 2 10KR2J-3-GP RTC_DET#

R2041 1 2 10KR2J-3-GP SIO_EXT_WAKE#

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

3D3V_S0

UMA R2038 10KR2J-3-GP

VRAM_ID2

OPS R2037 10KR2J-3-GP

VRAM_ID R2029 10KR2J-3-GP

VRAM_ID1

VRAM_ID R2030 10KR2J-3-GP

VRAM_ID[2:1] 11: UMA

01: DIS+4G VRAM

00: DIS+2G VRAM

2IN1 R2052 10KR2J-3-GP

BOARD_ID2

CLAM R2051 10KR2J-3-GP

X01 20170109 add

U22 R2010 10KR2J-3-GP

BOARD_ID1

U42 R2009 10KR2J-3-GP

BOARD_ID2 1: 2 in 1

0: clamshell

BOARD_ID1 1: KBL-U

0: KBL-R

MEM_CONFIG4 (GPP_F8) connected to +V1.8A_SIP

MEM_CONFIG3 (GPP_F7) connected to +V1.8A_SIP

MEM_CONFIG[4:3] 11: DIMM Design

MEM_CONFIG2 (GPP_F6) connected to +V1.8A_SIP

MEM_CONFIG1 (GPP_F5) connected to +V1.8A_SIP

MEM_CONFIG[2:1] 11: N/A (memory size)

<Core Design>

Wistron Corporation

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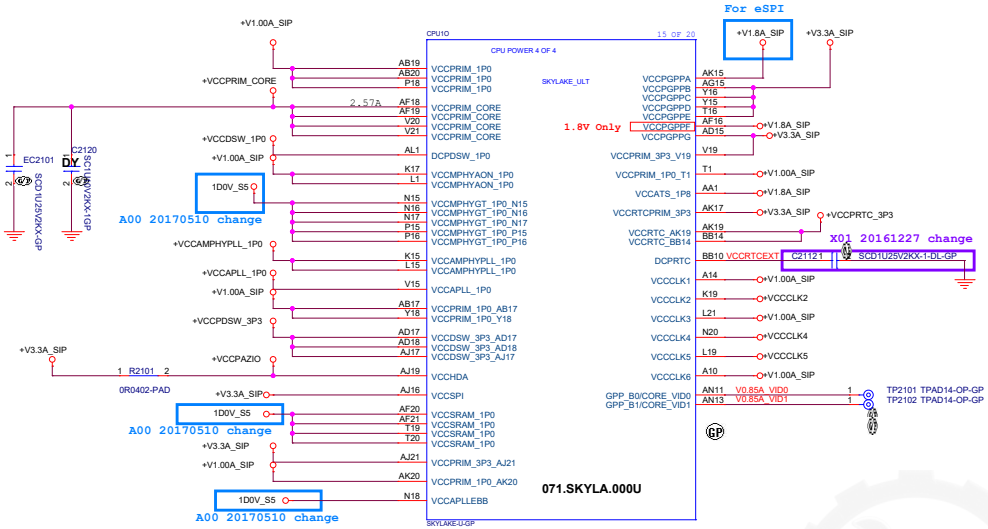
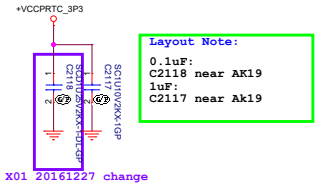
Title: CPU_(LPSS/ISH)

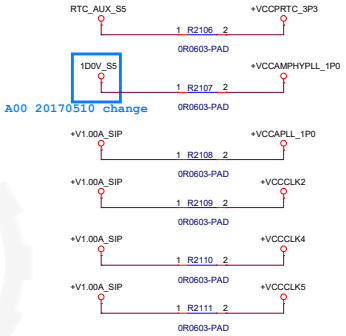
Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

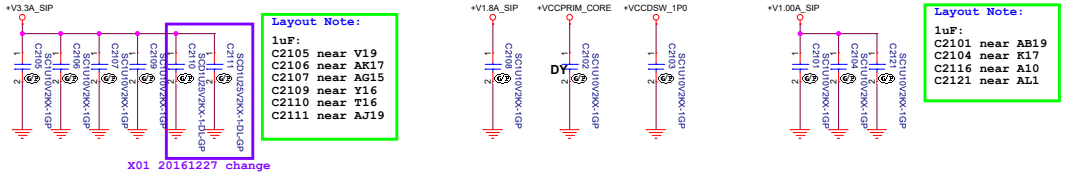
Date: Tuesday, June 20, 2017 | Sheet 20 of 106

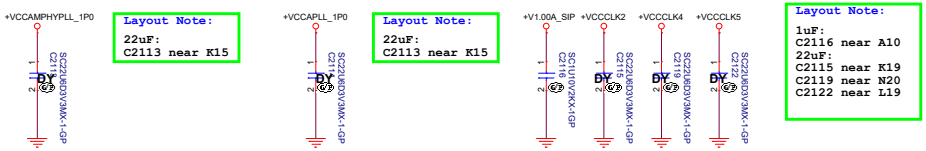
Main Func = PCH











<Core Design>

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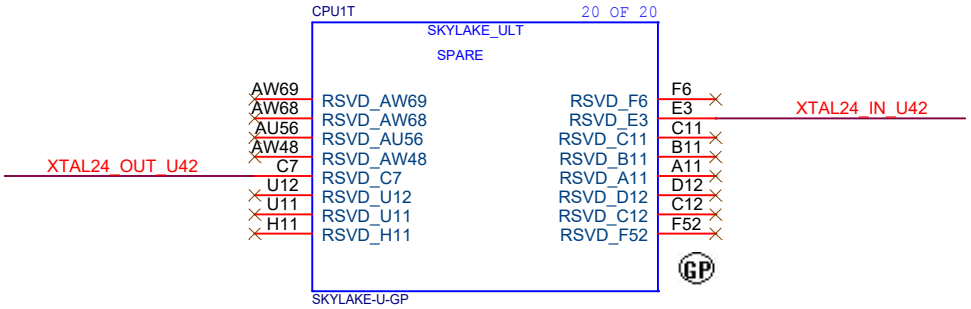
Title: CPU_(POWER1)

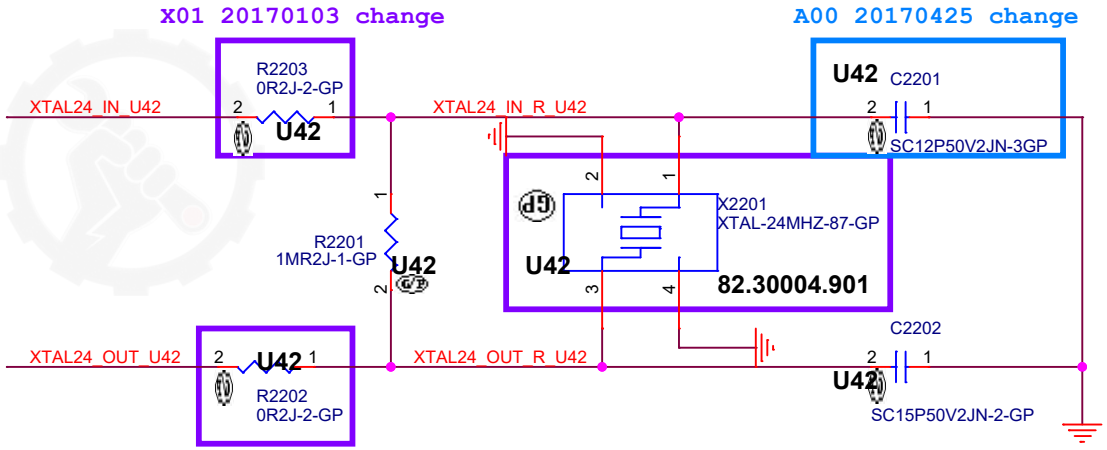
Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 21 of 106

Main Func = PCH



071.SKYLA.000U



<Core Design>

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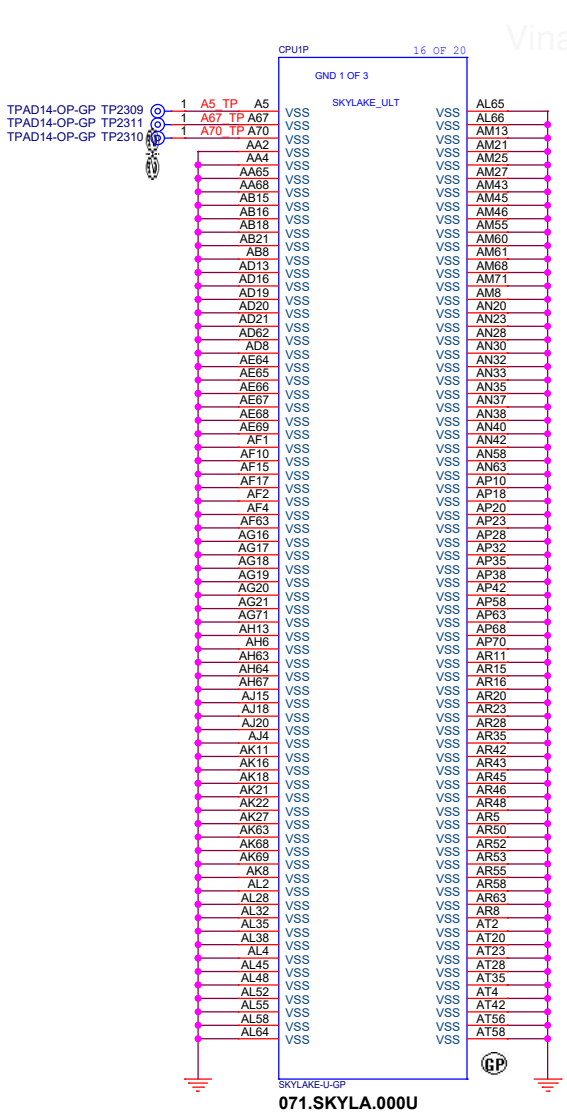
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_(RSVD)*

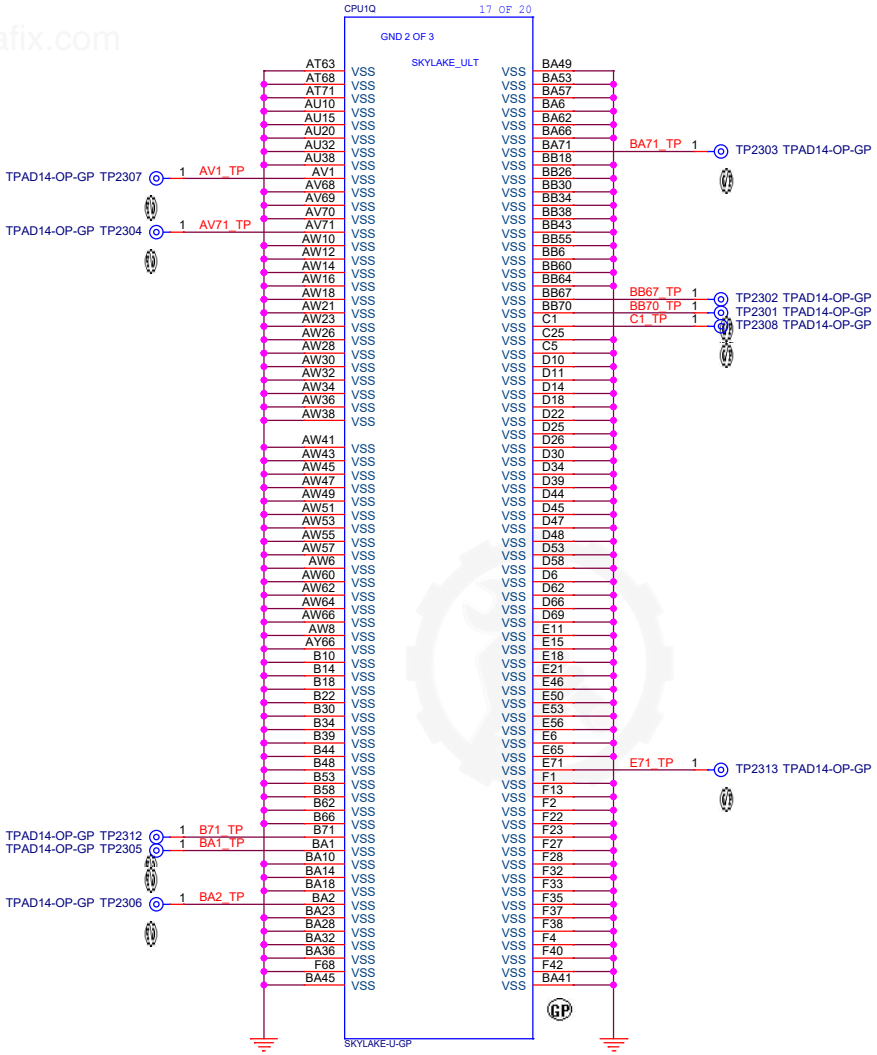
Size	Document Number	Rev
A4	*Kyloren 15" KBL-U*	*A00*

Date: Tuesday, June 20, 2017 Sheet 22 of 106

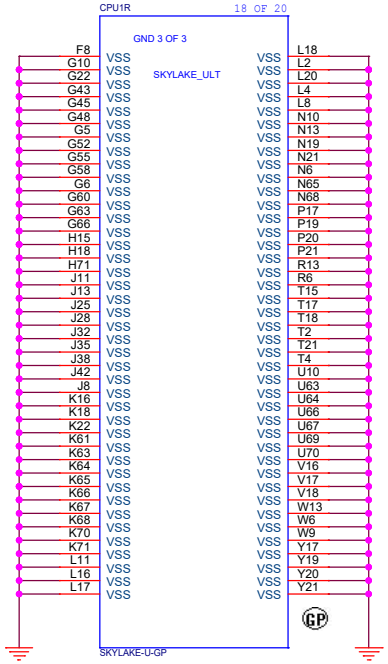
Main Func = PCH



071.SKYLA.000U



071.SKYLA.000U



071.SKYLA.000U

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

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Title: CPU_(VSS)

Size: A3 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 23 of 106

Main Func = KBC

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

MODEL ID

MODEL_ID_DET(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
	100.0K	10.0K	3.000
KyloRen 13" UMA Clamshell	100.0K	17.8K	2.801
KyloRen 13" UMA 2in1	100.0K	27.0K	2.598
	100.0K	37.4K	2.402
KyloRen 15" UMA Clamshell	100.0K	49.9K	2.201
KyloRen 15" UMA 2in1	100.0K	64.9K	2.001
	100.0K	82.5K	1.808
KyloRen 15" DIS Clamshell	100.0K	107K	1.594
KyloRen 15" DIS 2in1	100.0K	154K	1.299
	100.0K	200K	1.100

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

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KBC Nuvoton NPCE285PA0DX

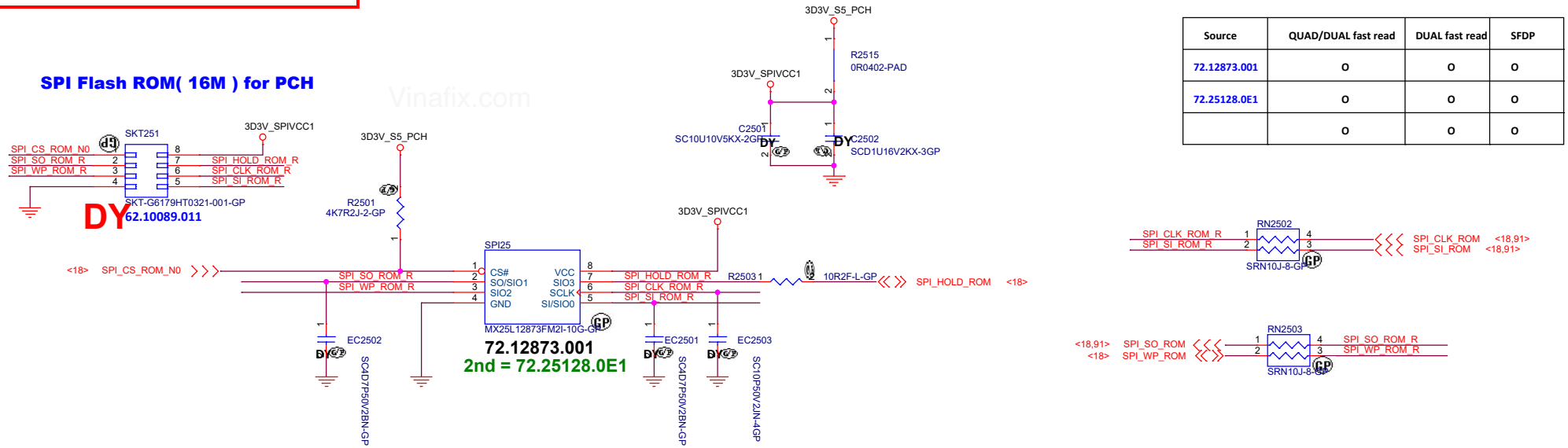
Size: A3 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 24 of 100

Main Func = SPI Flash

SPI Flash ROM(16M) for PCH

Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.12873.001	O	O	O
72.25128.0E1	O	O	O
	O	O	O

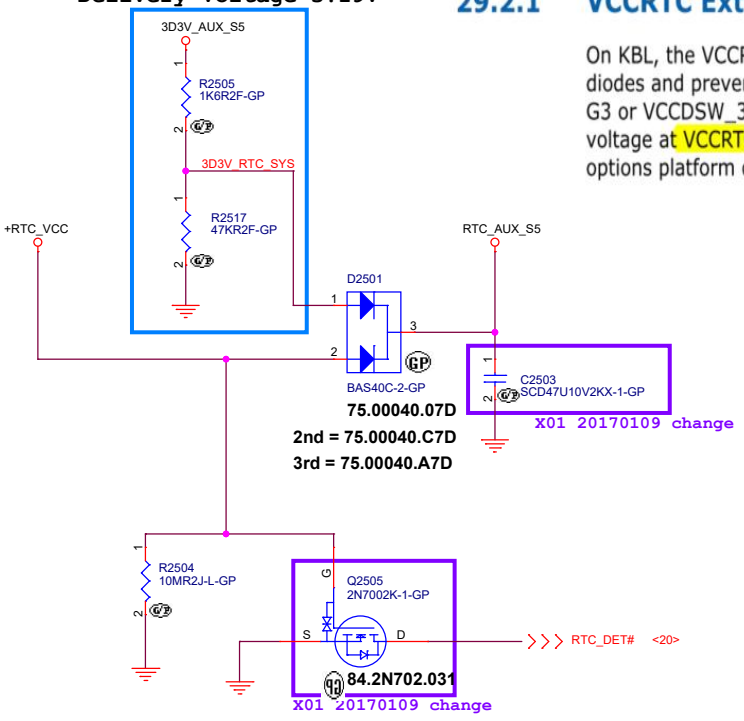


Main Func = RTC

Delivery Voltage 3.19V

29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



<Core Design>

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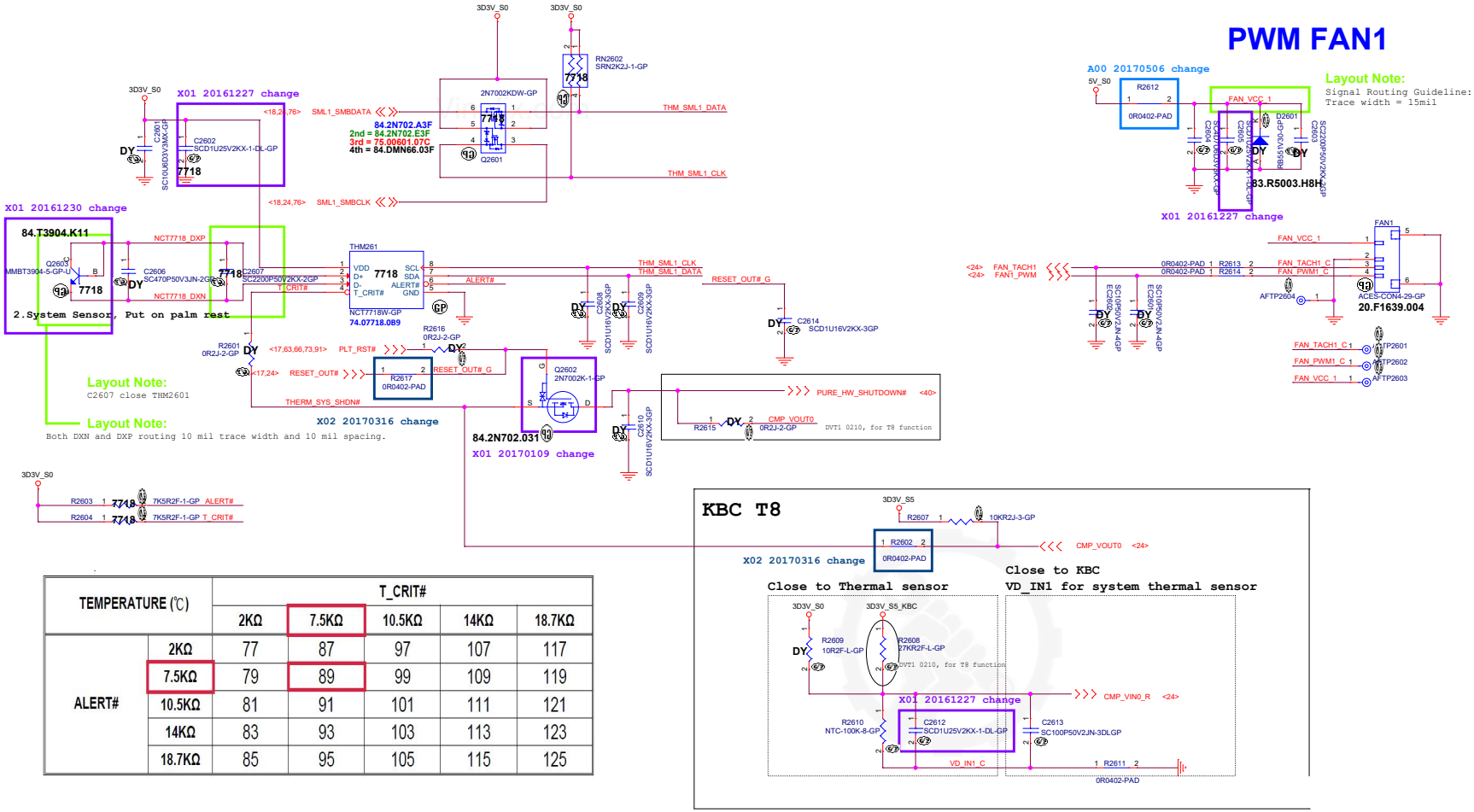
Title	Flash/RTC	
Size A3	Document Number Kyloren 15" KBL-U	Rev A00
Date: Tuesday, June 20, 2017	Sheet 25 of 106	

Main Func = Thermal Sensor



PWM FAN1

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8

<Core Design>
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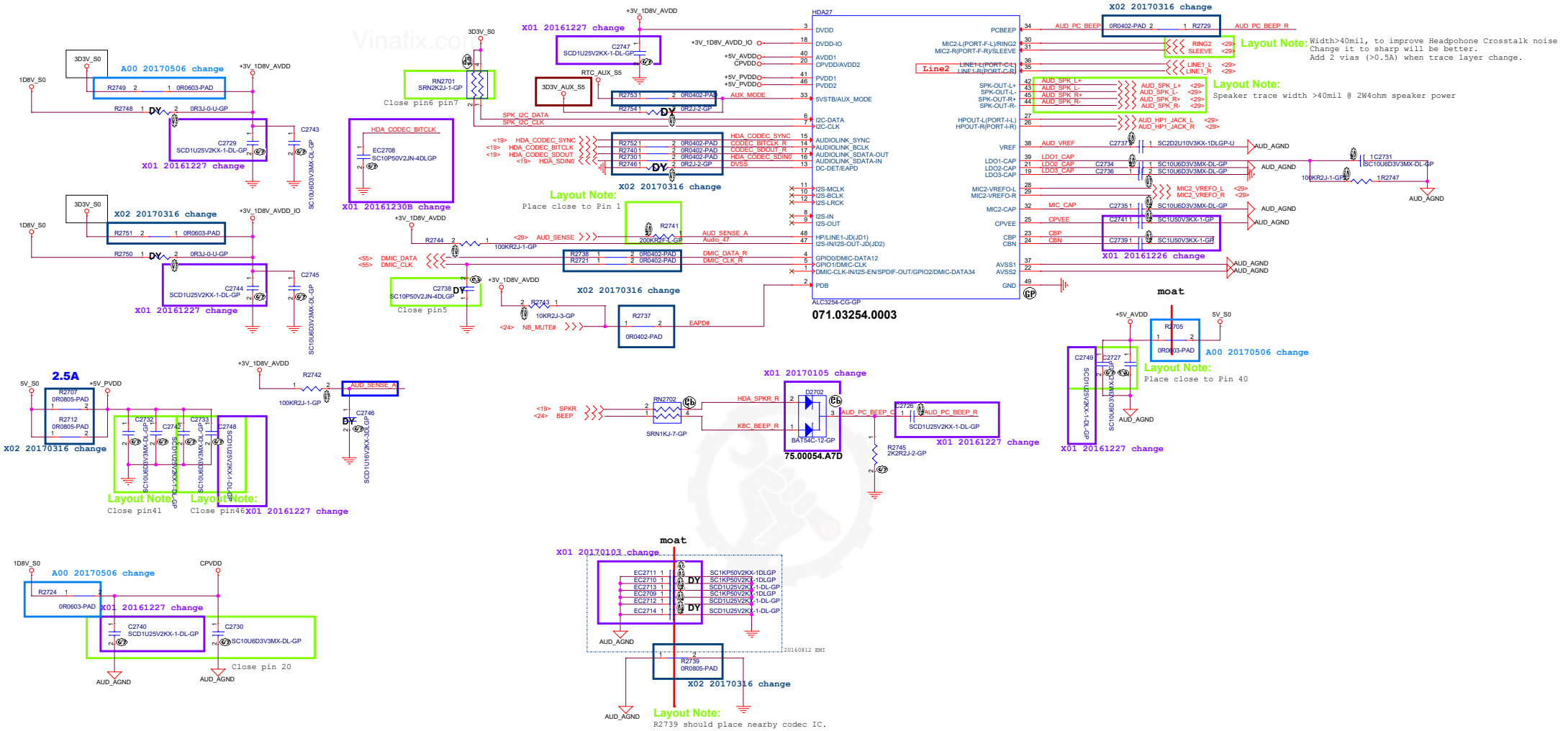
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 26 of 106

Main Func = Audio



<Core Design>

Wistron Corporation
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Title: (Reserved)

Size	Document Number	Rev
A1	Kyloren 15" KBL-U	A00

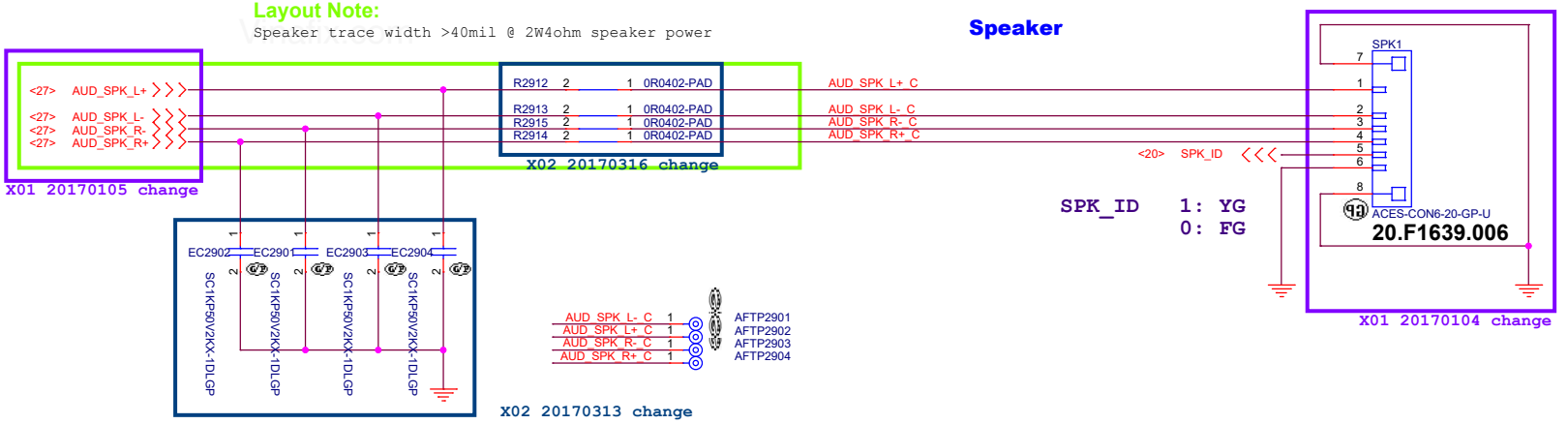
Date: Tuesday, June 20, 2017 Sheet 28 of 106

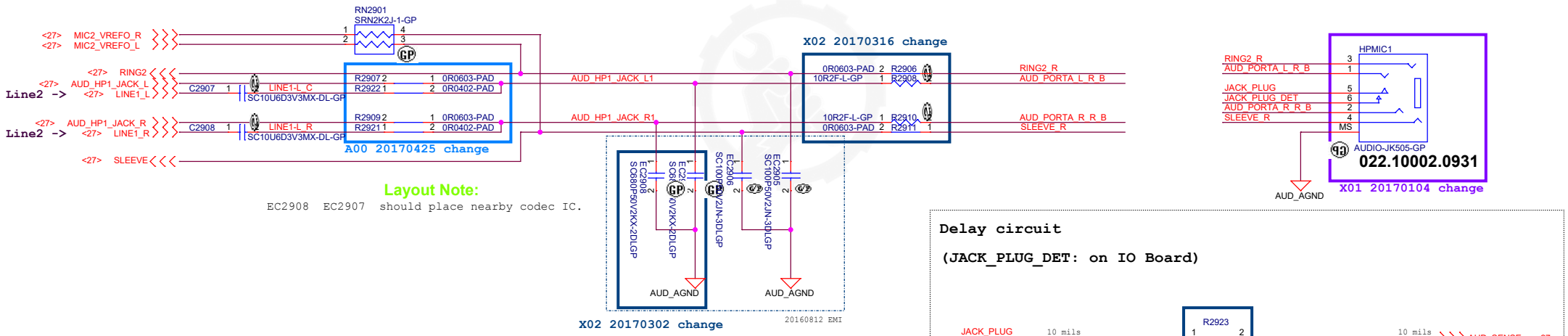
Main Func = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND





<Core Design>

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Title: Audio IO
Size: A3
Document Number: Kyloren 15" KBL-U
Rev: A00
Date: Tuesday, June 20, 2017
Sheet 29 of 106

Main Func = Audio

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 30 of 106

Main Func = LAN

(Blanking)

<Core Design>

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Title: LAN RTL8106

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 31 of 106

Main Func = LAN

(Blanking)

<Core Design>

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Title: XFOM&RJ45

Size: A3 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 32 of 106

Main Func = Card Reader

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

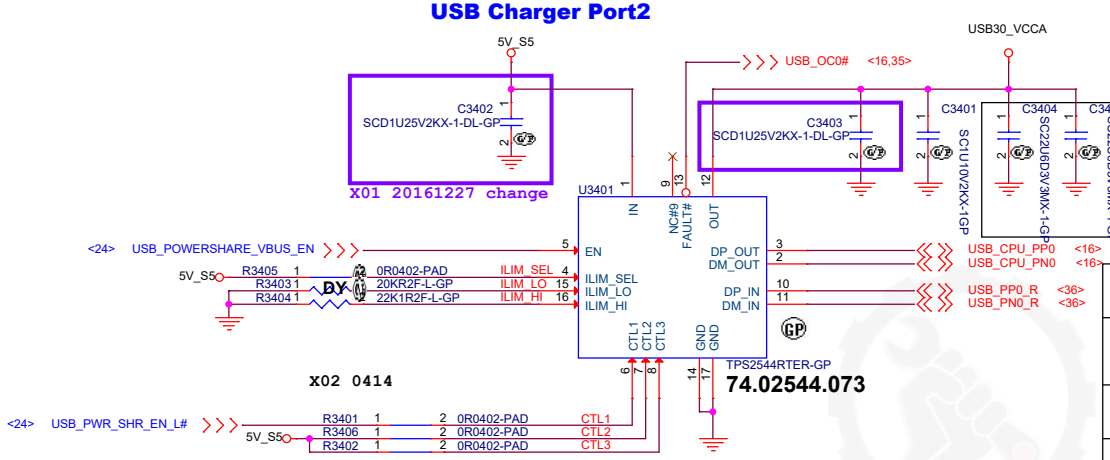
Title: Card Reader-RTS5170

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 33 of 106

Main Func = USB3.0 Port2

USB Charger Port2



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

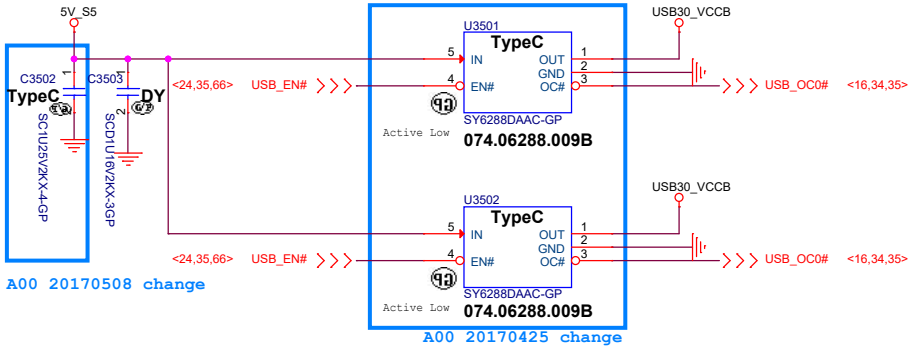
Title: (Reserved)

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 34 of 106

Main Func = USB3.0 Power Switch

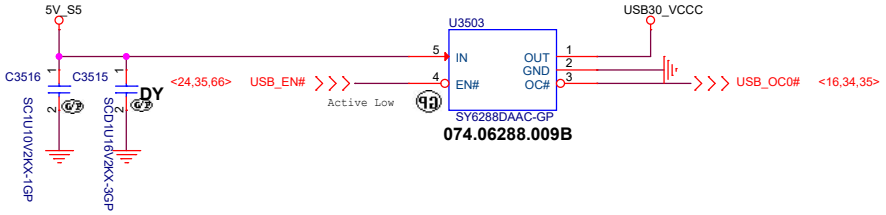
USB Port1 Type-C

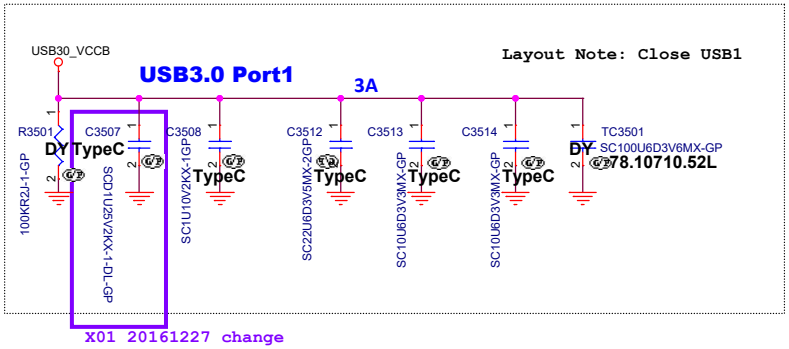


A00 20170508 change

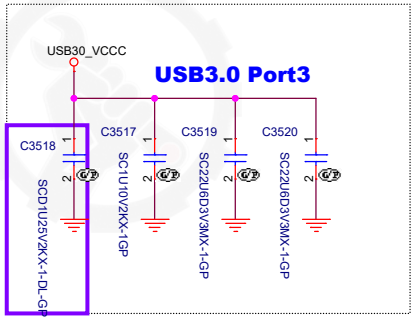
A00 20170425 change

USB 3.0 Port3





X01 20161227 change



X01 20161227 change

<Core Design>

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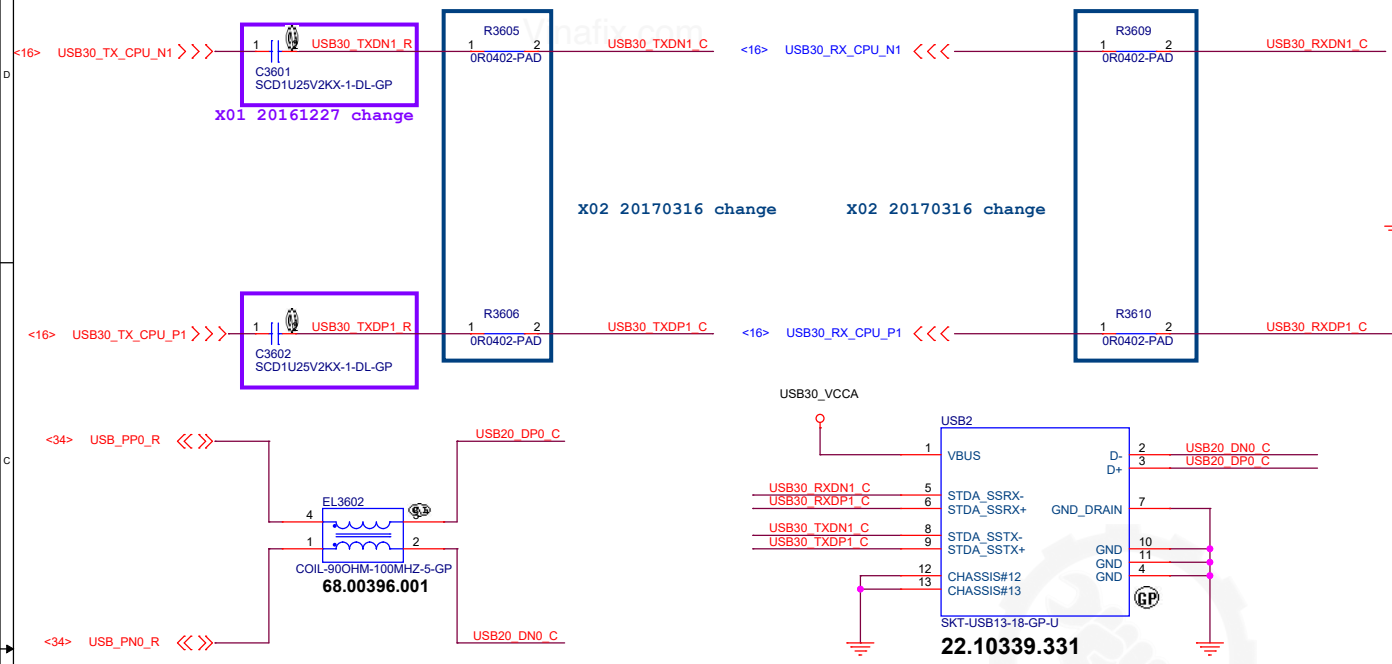
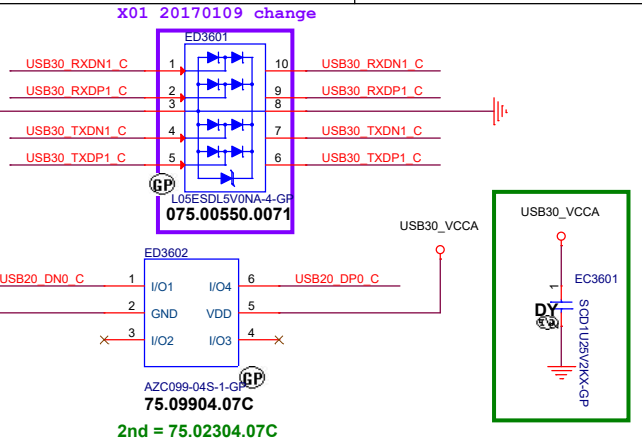
Title		
USB switch		
Size	Document Number	Rev
	Kyloren 15" KBL-U	A00
Date: Tuesday, June 20, 2017	Sheet 35 of 106	

Main Func = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

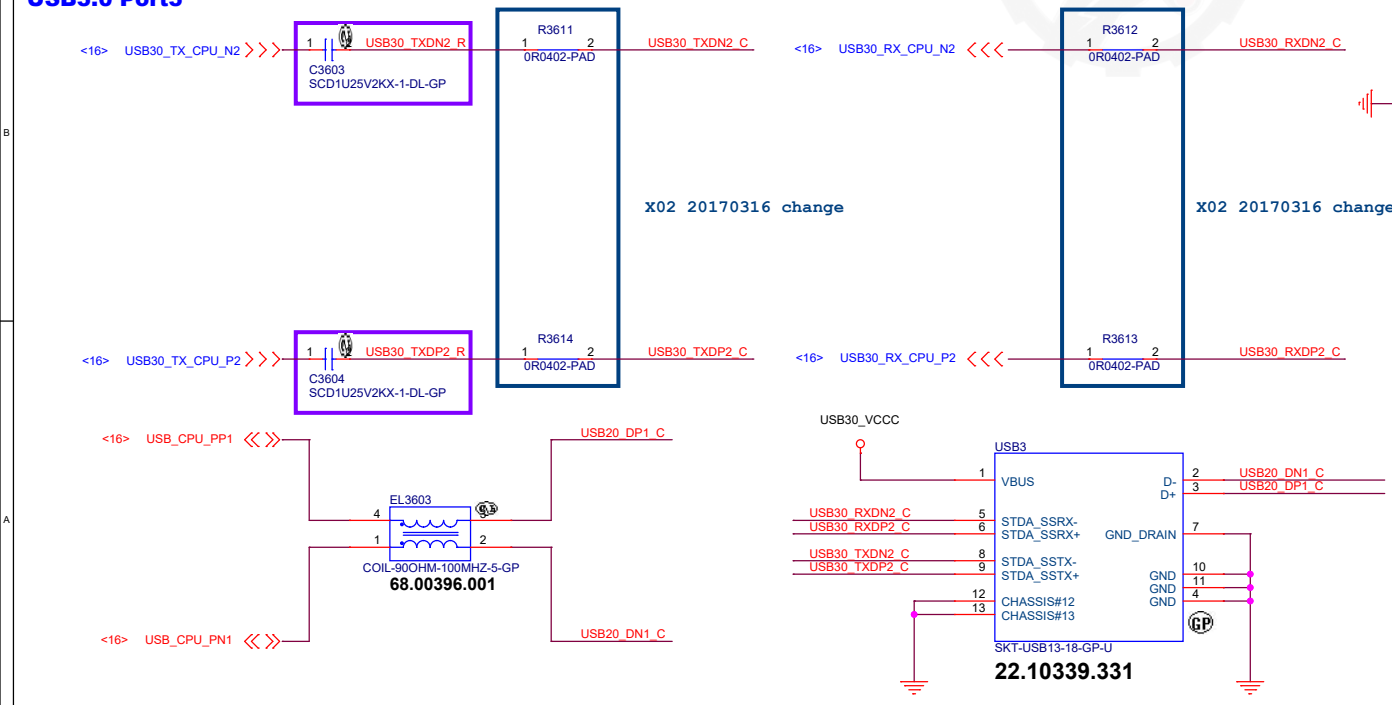
USB3.0 Port2

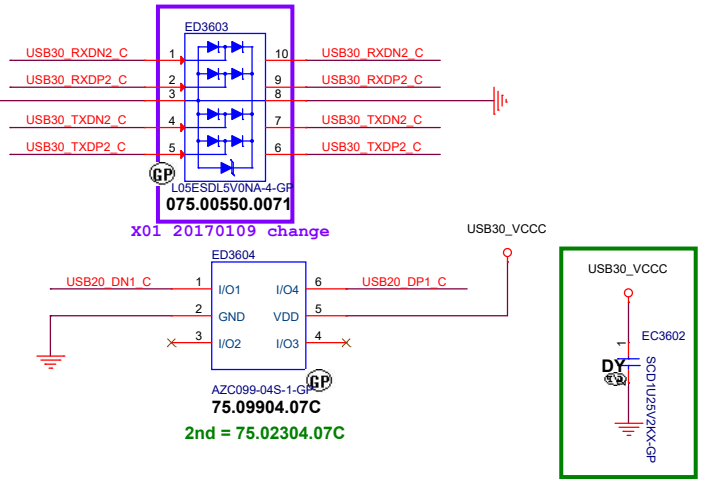




USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port3





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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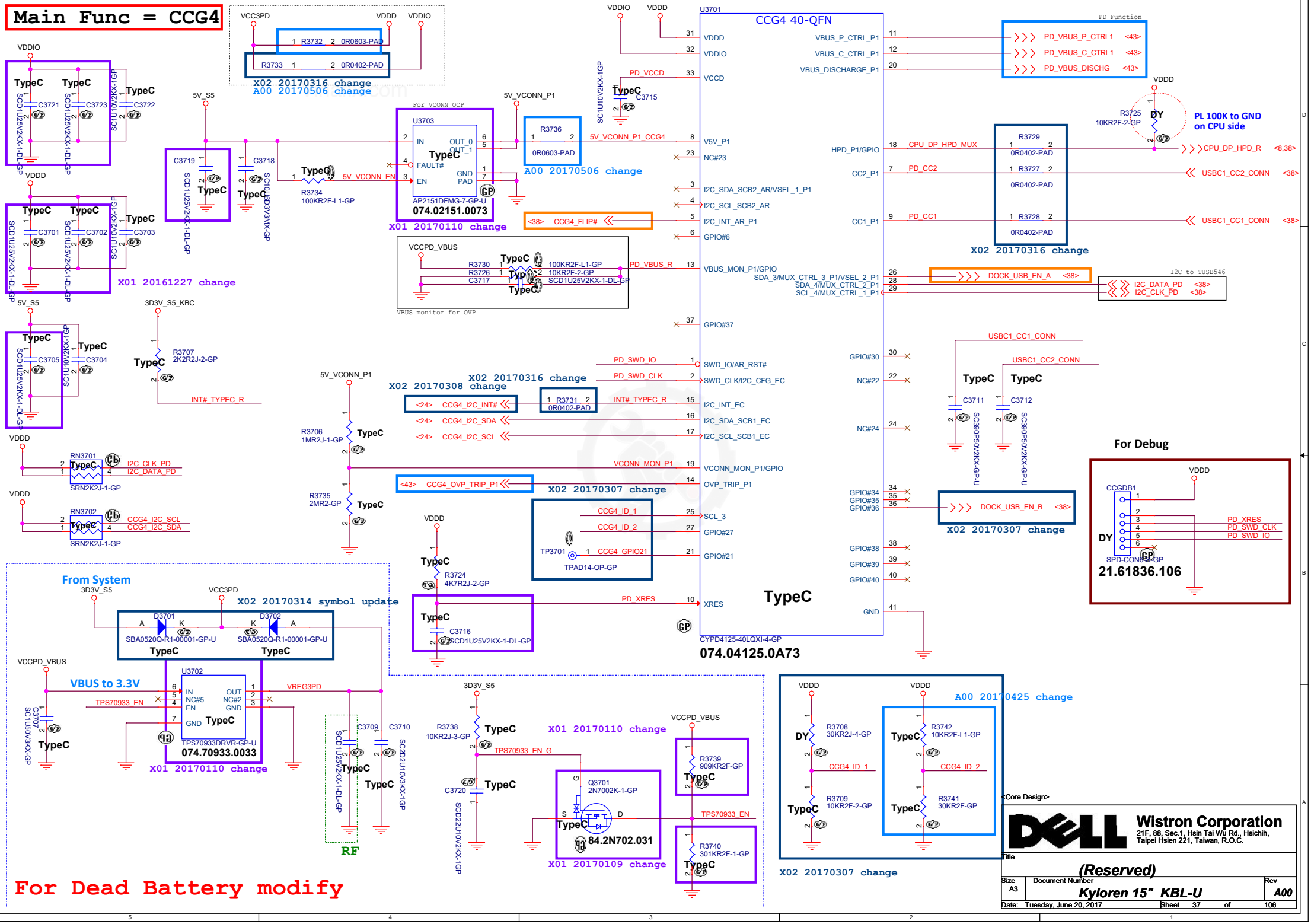
Title: **USB30**

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 36 of 106

Main Func = CCG4



Main Func = TYPEC MUX

DisplayPort Source

USB HOST

U3801 TUSB546-DCIRNQR-GP 071.00546.0003

U3802 TS3DS10224RUKR-GP 071.10224.0003

X01 20161228 change

X02 20170316 change

X01 20170109 change

A00 20170425 change

A00 20170506 delete

A00 20170506 change

A00 20170517 change

X02 20170314 symbol update

For displayport function at dead battery condition

FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI mode	
23 CTL1/HPDIN	DP_ENABLE in GPIO mode HPD in I2C mode	DP_Enable in GPIO mode Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

Main Func = USB3.0 Port1

<Core Design>

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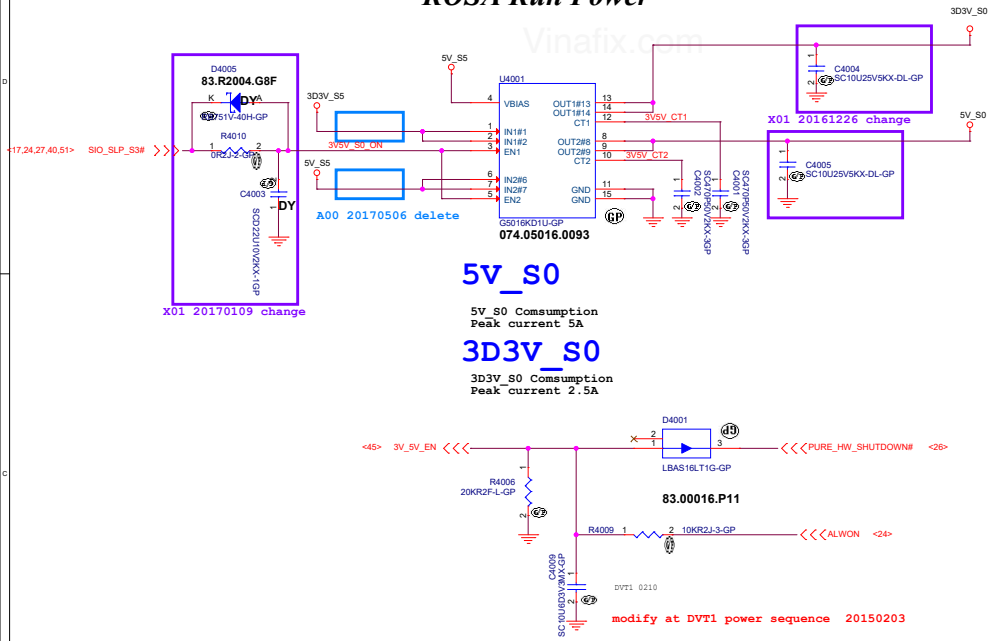
Title: (Reserved)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 39 of 106

Main Func = Power Plane & Sequence

ROSA Run Power



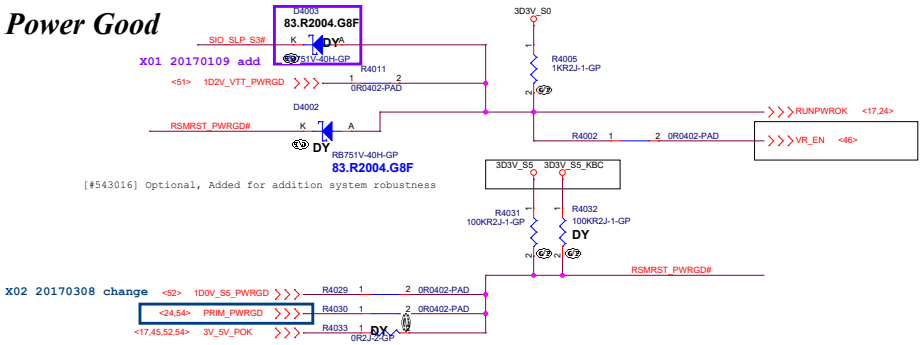
5V_S0

5V_S0 Comsumption
Peak current 5A

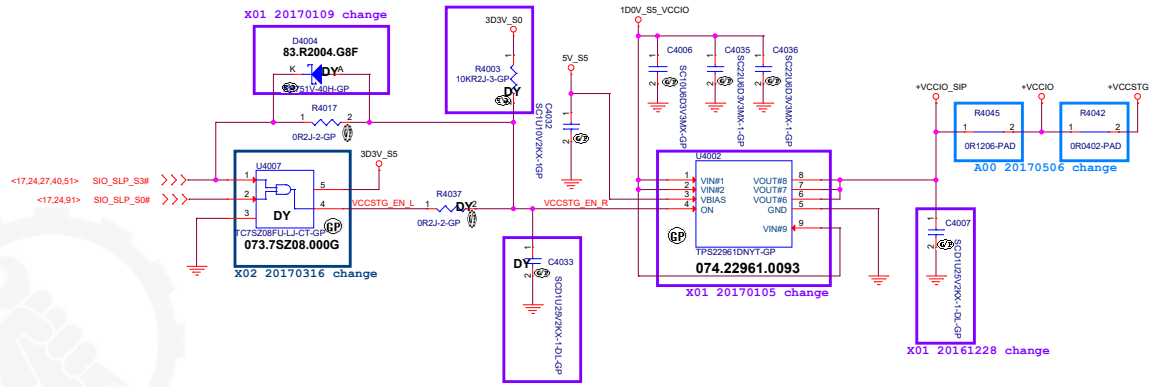
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

Power Good



VCCIO and VCCSTG



EOPIO and EDRAM

+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

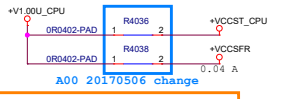
Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

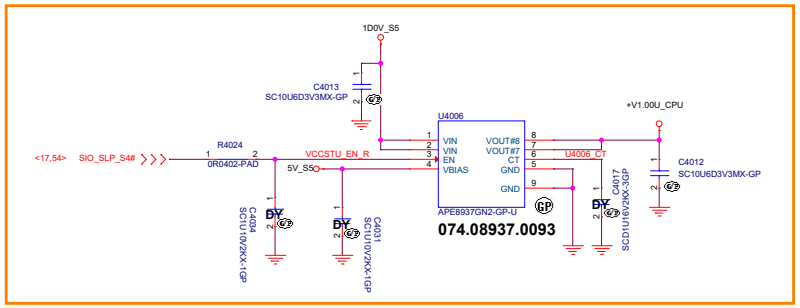
+V1.8S_EDRAM

MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST_CPU





<Core Design>

Wistron Corporation
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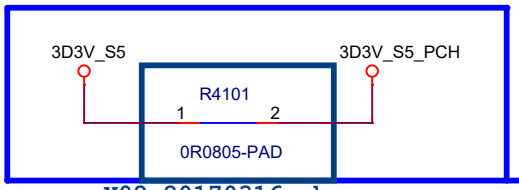
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 40 of 106

Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413

X02 20170316 change

DS3

<Core Design>

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Title: *Connected_Standby(1/2)+DS3*		
Size: A4	Document Number: *Kyloren 15" KBL-U*	Rev: *A00*
Date: Tuesday, June 20, 2017	Sheet 41 of 106	

Main Func = DIMM1

Main Func = DIMM2

<Core Design>

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 42 of 106

Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

Pin Definition: TBD

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

X02 20170316 change
X02 20170316 add
X02 20170314 add
X01 20161230B change
X01 20161230 change
X01 20170109 change
R-A00 20170620 change
R-A00 20170617 change
R-A00 20170612 change
A00 20170425 change
A00 20170512 change

84.T3904.K11
84.05067.031
84.00024.01K
84.05212.B11
84.2N702.031
73.01G04.01V
83.P6SMB.JAG
20.F1295.008
074.01004.00BF
020.F0867.0010
84.07403.037
84.2N702.A3F

75.00099.O7D
2nd = 75.00099.K7D
3rd = 75.00099.Q7D
4th = 75.00099.D7D

If=0.3A
Id=115mA

VBUS_C_CTRL = 1 (Consumer Path ON)
VBUS_C_CTRL = 0/Z (Consumer Path OFF)

VBUS overvoltage output indicator (active LOW)

PD_VBUS_DISCHG = 1 (VBUS Discharging)
PD_VBUS_DISCHG = 0/Z (VBUS not discharging)

PD_VBUS_P_CTRL1 = 1 (Provider Path ON)
PD_VBUS_P_CTRL1 = 0/Z (Provider Path OFF)

Batt Connecter

Placement: Close to Batt Connector

Main Func = M-BAT Input

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Title: DCIN
Size: A2
Document Number: Kyloren 15" KBL-U
Rev: A00
Date: Tuesday, June 20, 2017
Sheet 43 of 106

Main Func = Charger

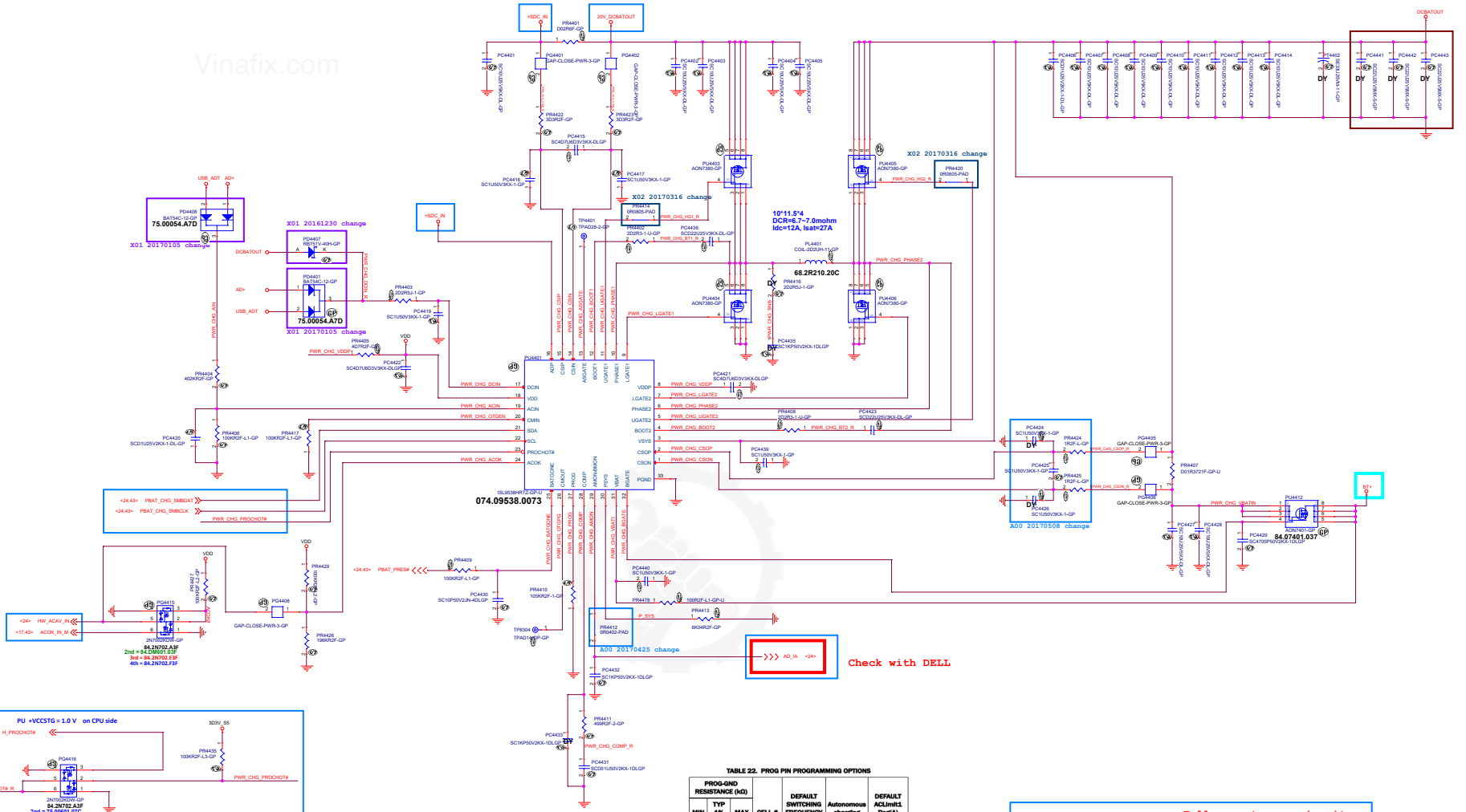
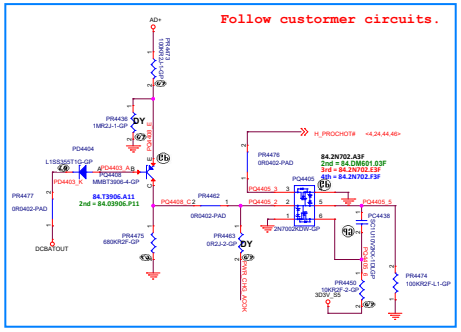


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)				DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP 1%	MAX	CELL #			
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476



<Core Design>

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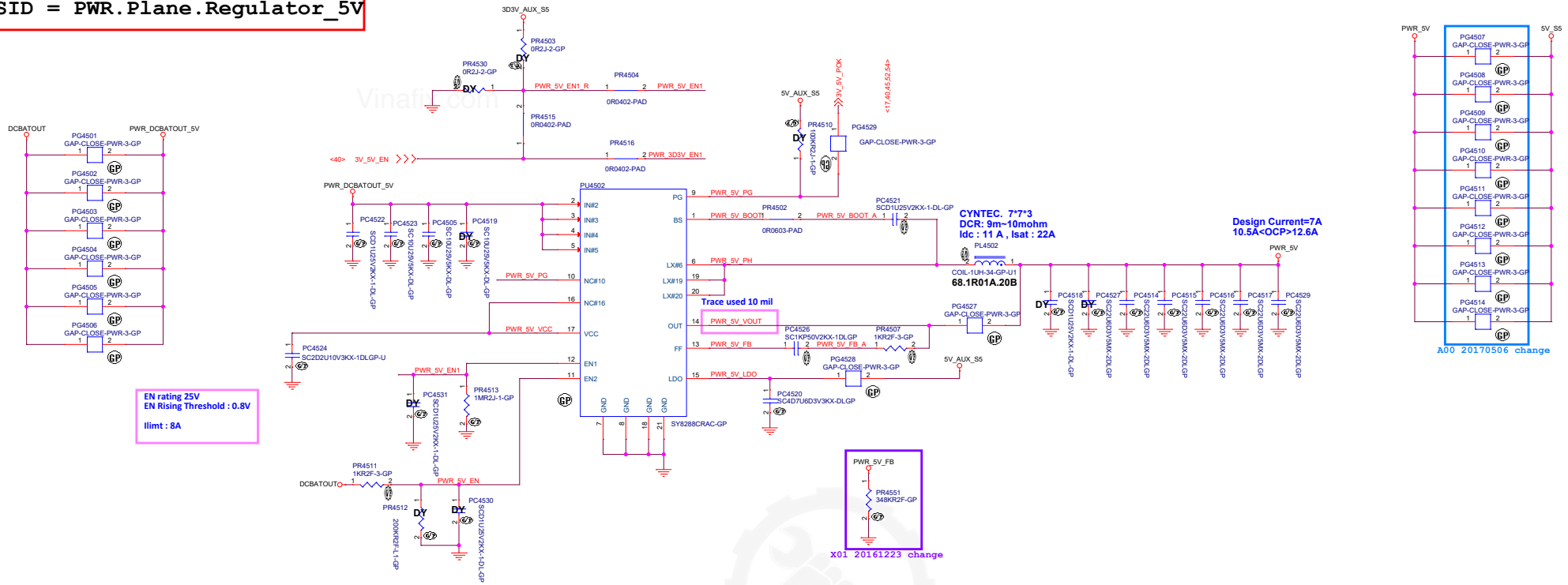
Title: Charger

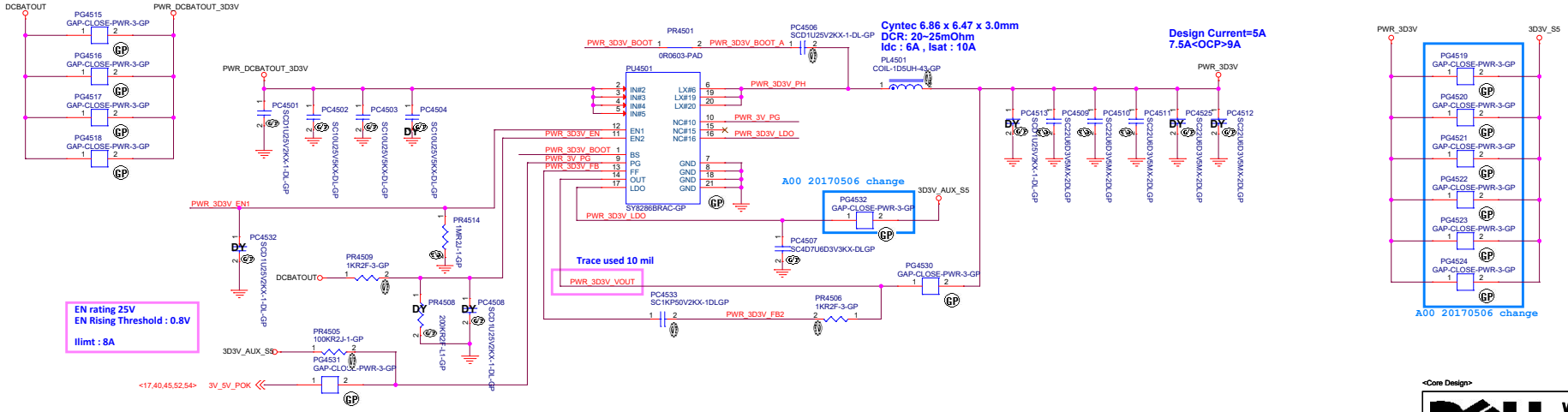
Size	Document Number	Rev
A1	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 44 of 55

SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V



<Core Design>

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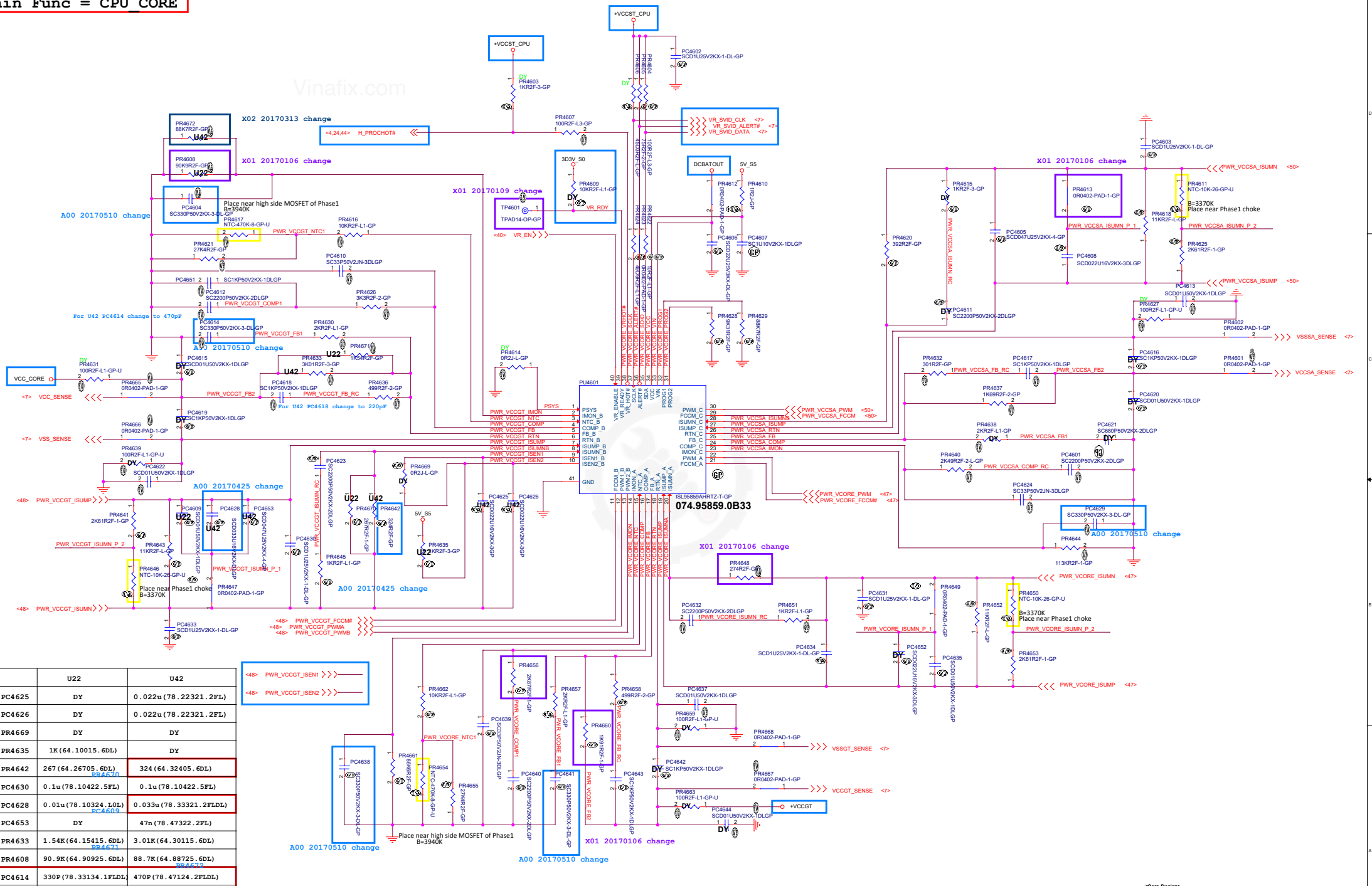
Title: (Reserved)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 45 of 106

Main Func = CPU_CORE



	U22	U42
PC4625	DY	0.022u(78.22321.2FL)
PC4626	DY	0.022u(78.22321.2FL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	267(64.26705.6DL)	324(64.32405.6DL)
PC4630	0.1u(78.10422.5FL)	0.1u(78.10422.5FL)
PC4628	0.01u(78.10324.L0L)	0.033u(78.33321.2FLDL)
PC4653	DY	47n(78.47322.2FL)
PR4633	1.54K(64.15415.6DL)	3.01K(64.30115.6DL)
PR4608	90.9K(64.90925.6DL)	88.7K(64.88725.6DL)
PC4614	330P(78.33134.1FLDL)	470P(78.47124.2FLDL)
PC4618	1000P(78.10224.2FLDL)	220P(78.22124.2FLDL)

<Core Design>

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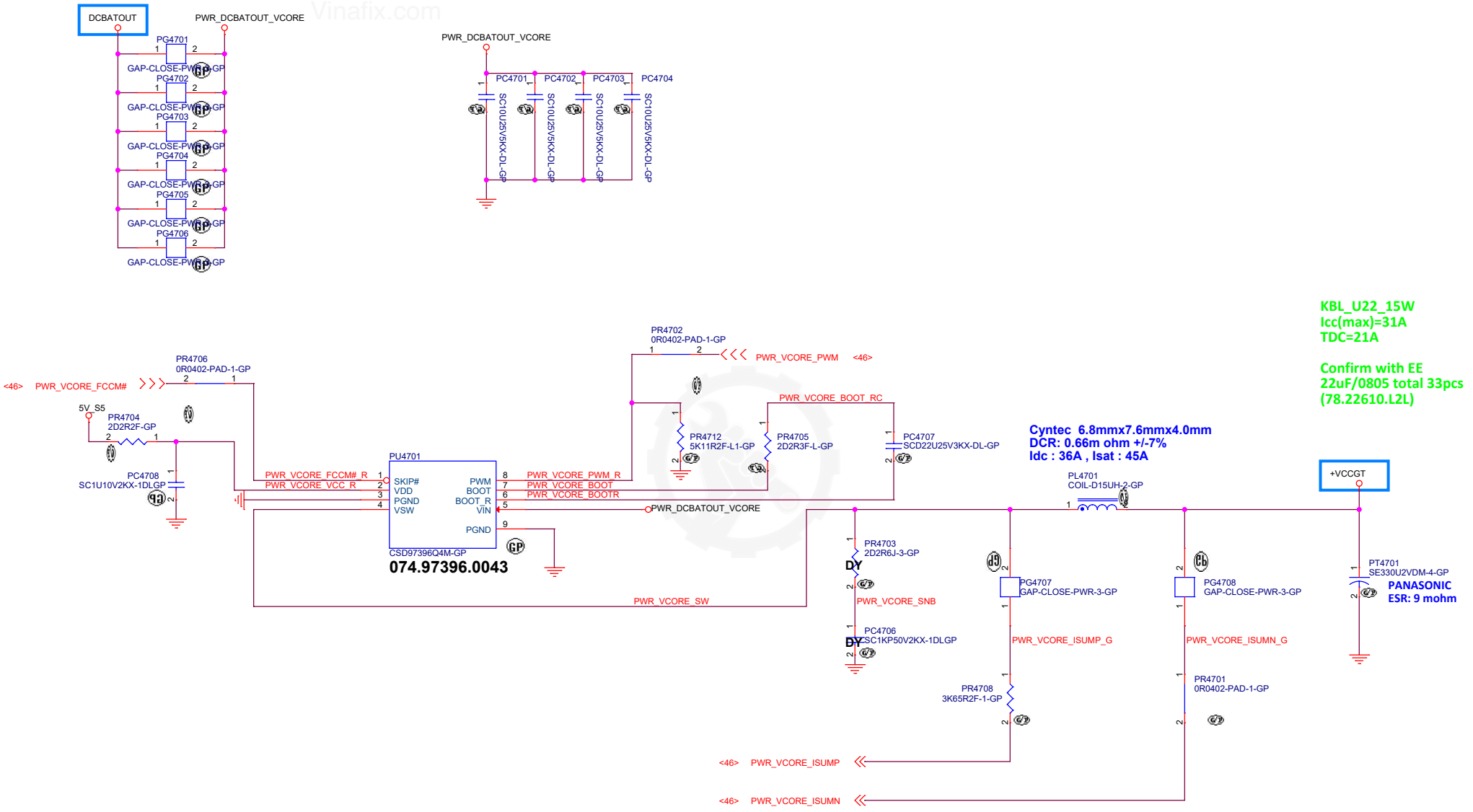
Title: NCP81208MN_CPU_VCORE(1/3)

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 46 of 106

Main Func = CPU_CORE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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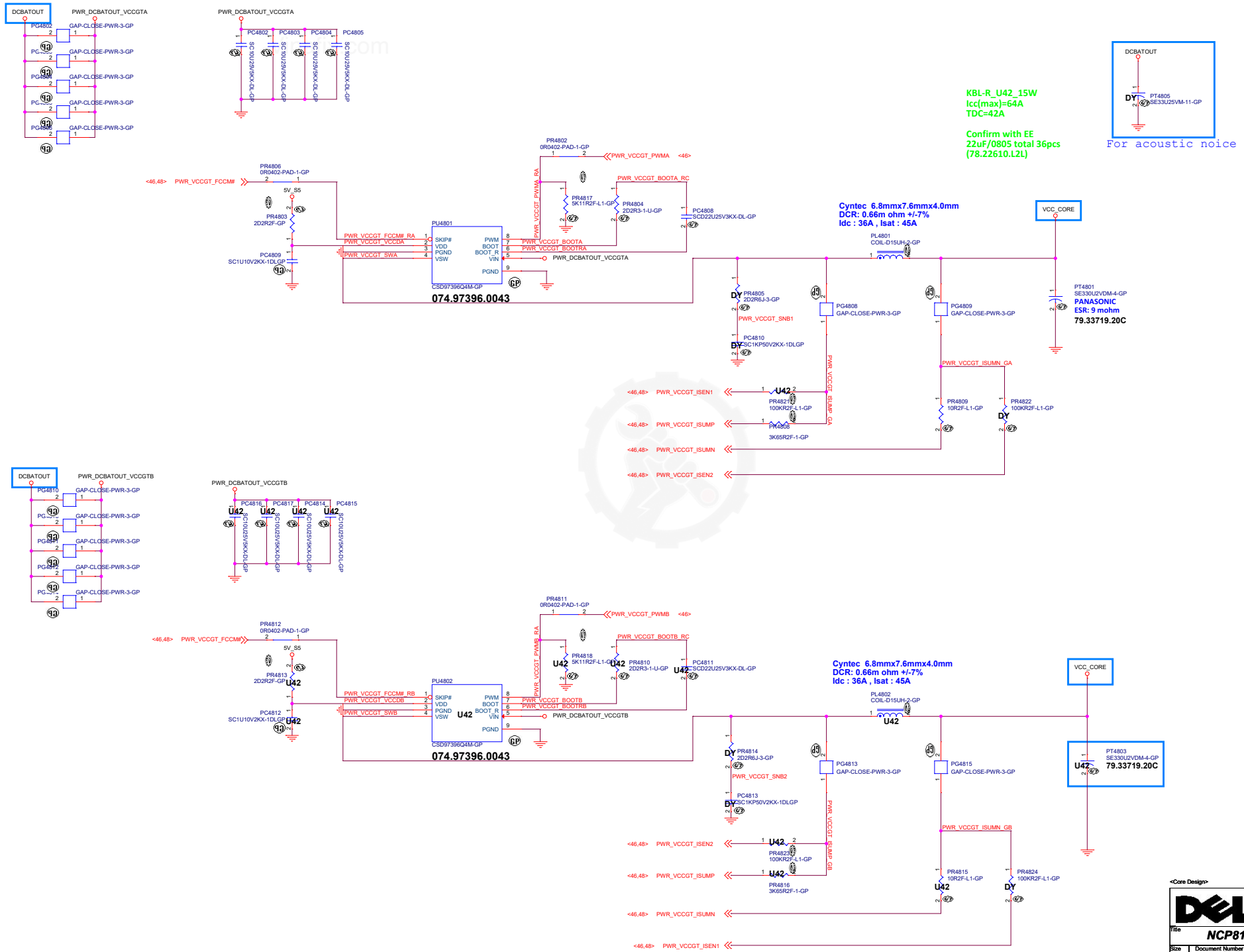
Title	NCP81382MN_CPU_VCORE(2/3)	
Size: A3	Document Number: Kyloren 15" KBL-U	Rev: A00
Date: Tuesday, June 20, 2017	Sheet 47 of 106	

Main Func = CPU_CORE



<Core Design>

Wistron Corporation
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Title	NCP81382MN_CPU_VCCGT(3/3)	
Size A2	Document Number Kyloren 15" KBL-U	Rev A00
Date: Tuesday, June 20, 2017	Sheet 48 of 106	

<Core Design>

Wistron Corporation
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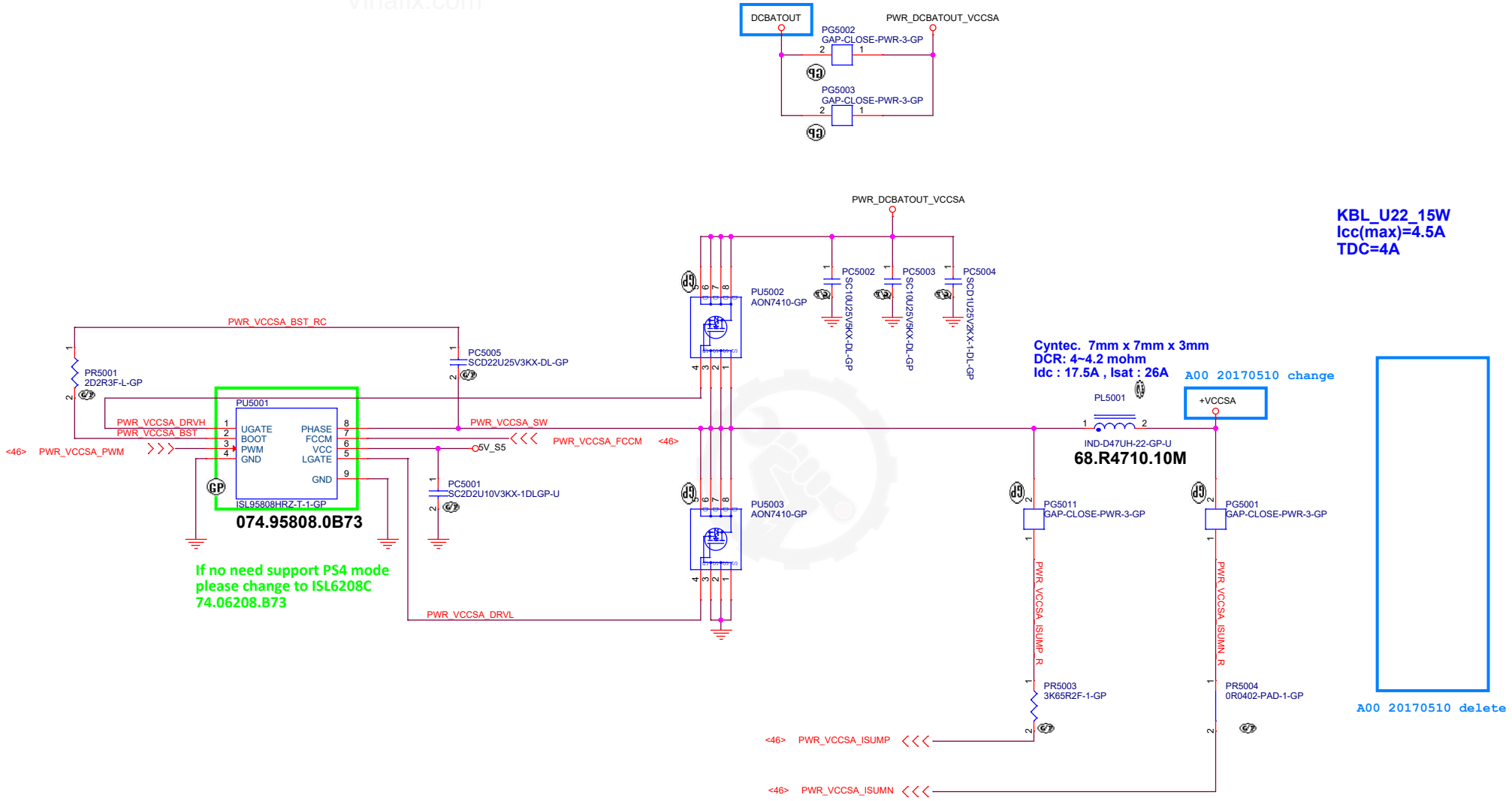
Title: NCP81210MN_CPU_VCCGTUS

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 49 of 106

Main Func = CPU_CORE



<Core Design>

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Title: VCCSA

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

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SSID = PWR.Plane.Regulator_1D2V/0D6V

SY8288RAC for 1D2V

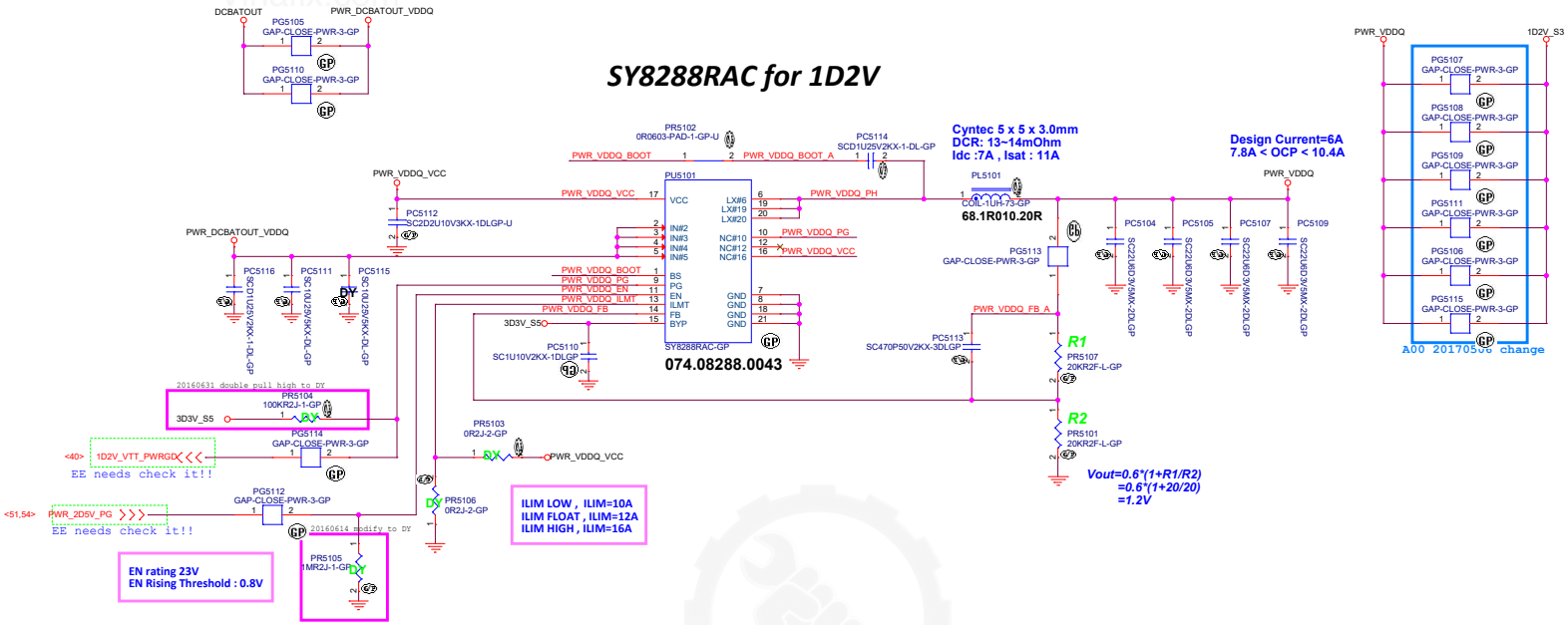
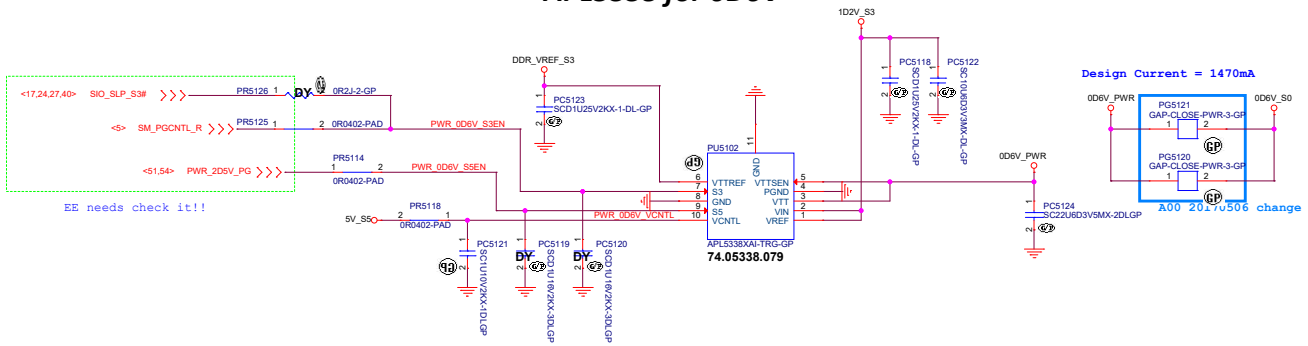


Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

APL5338 for 0D6V



<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

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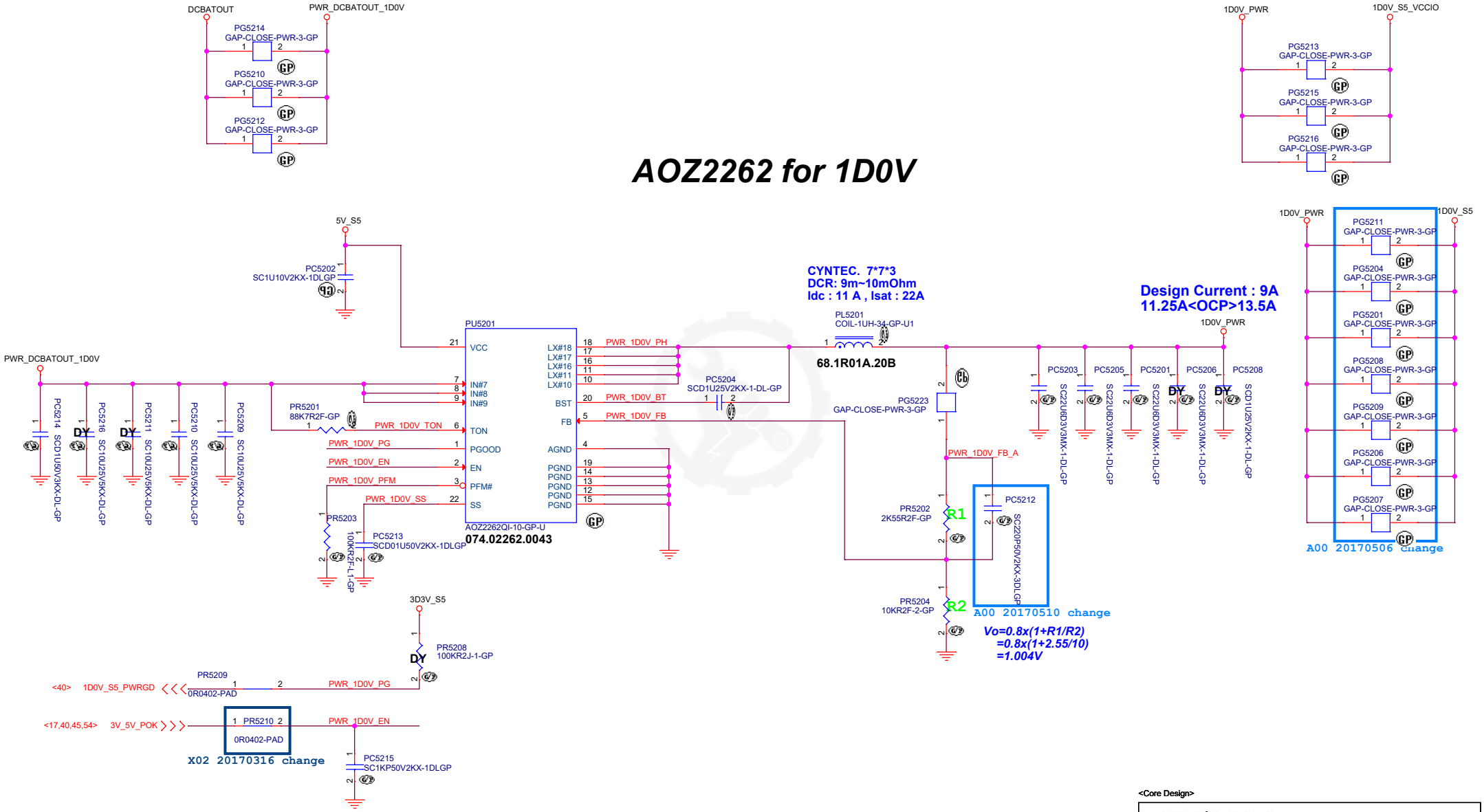
SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V



<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 52 of 106

SSID = PWR.Plane.Regulator_VCCIO/VCCPRIM_CORE

<Core Design>

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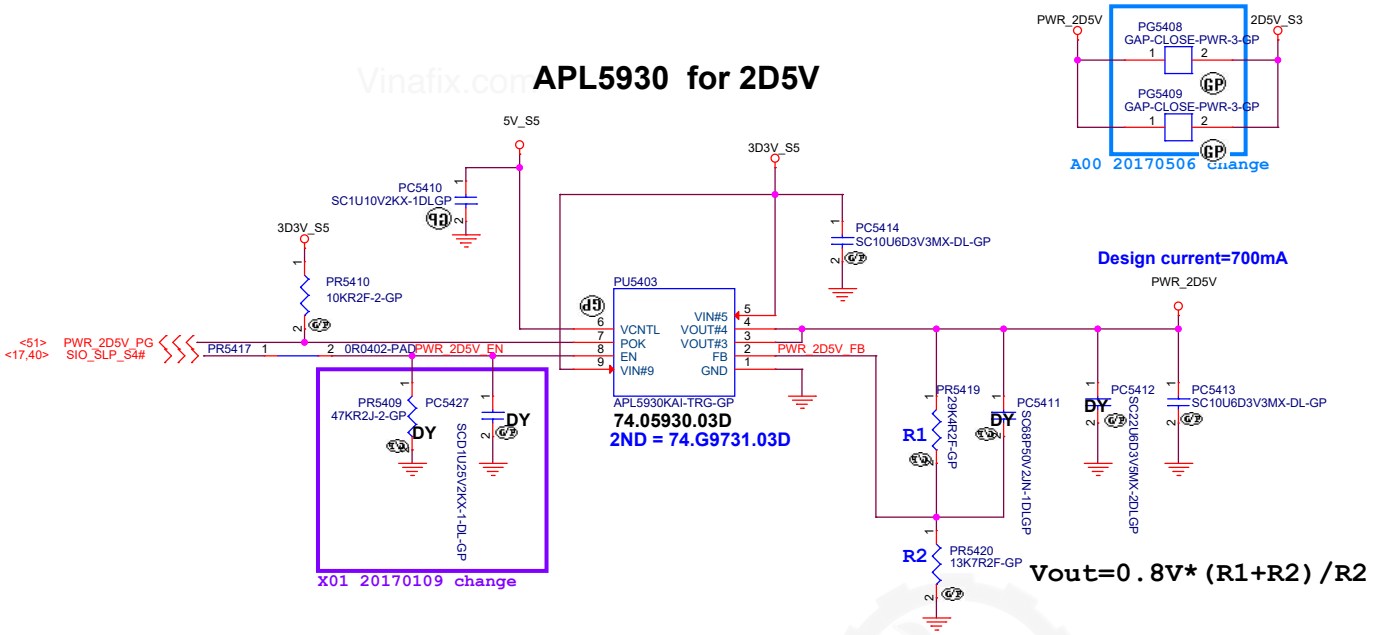
Title
(Reserved)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

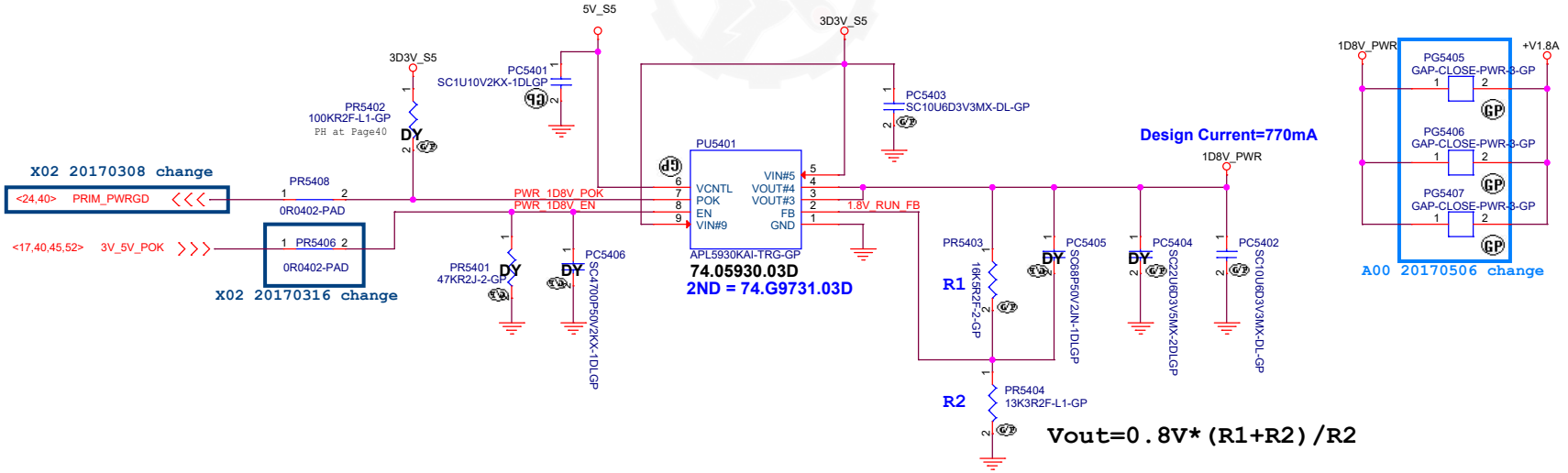
Date: Tuesday, June 20, 2017 Sheet 53 of 106

Main Func = 2D5V/ 1D8V

APL5930 for 2D5V



APL5930 for 1D8V_S5



<Core Design>

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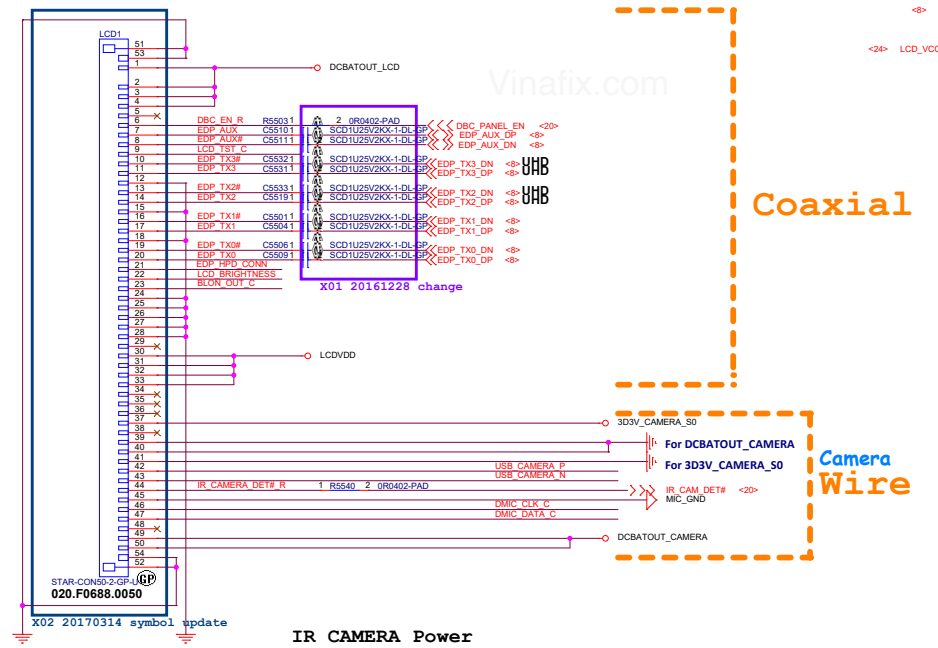
Title: *(Reserved)*

Size	Document Number	Rev
A3	*Kyloren 15" KBL-U*	*A00*

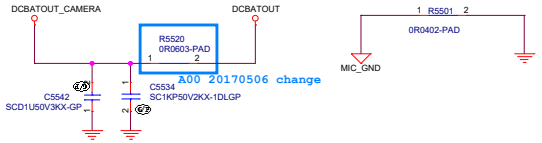
Date: Tuesday, June 20, 2017 Sheet 54 of 106

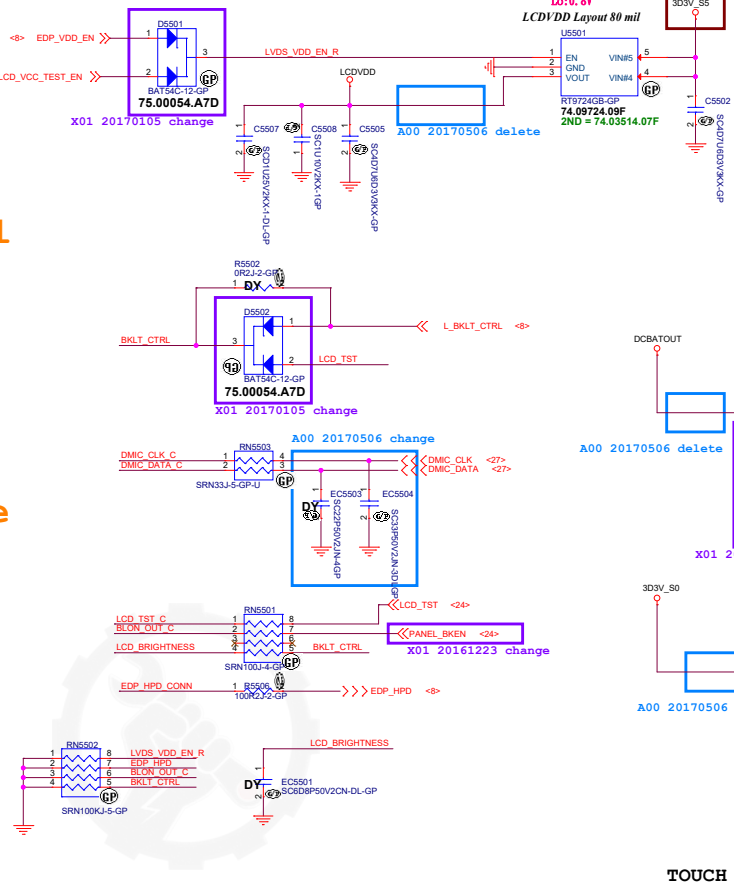
Main Func = LCD

Panel / Camera/ DMIC

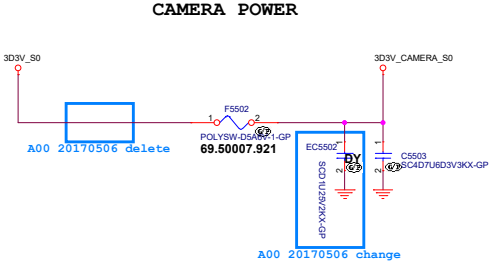


IR CAMERA Power

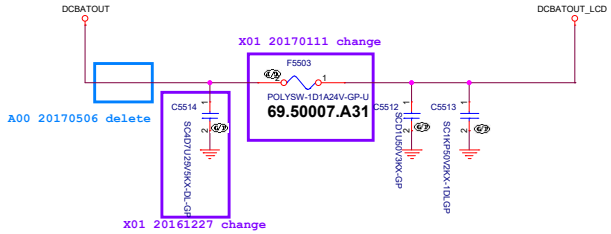




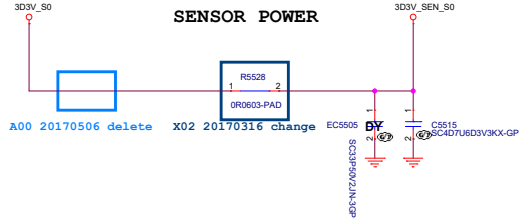
CAMERA POWER



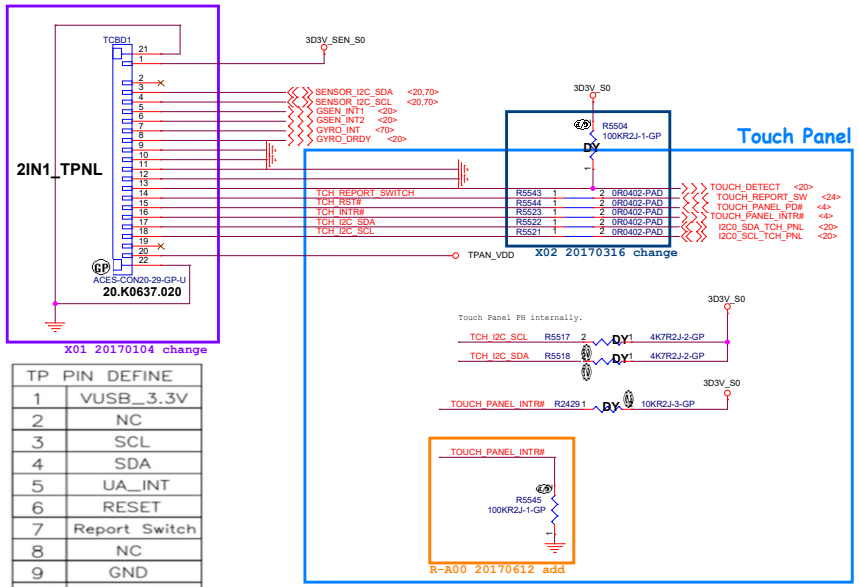
INVERTER POWER



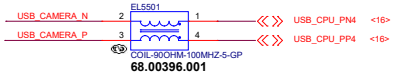
SENSOR POWER

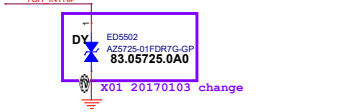


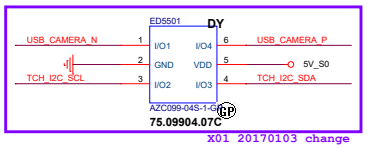
Sensor/ Touch Panel



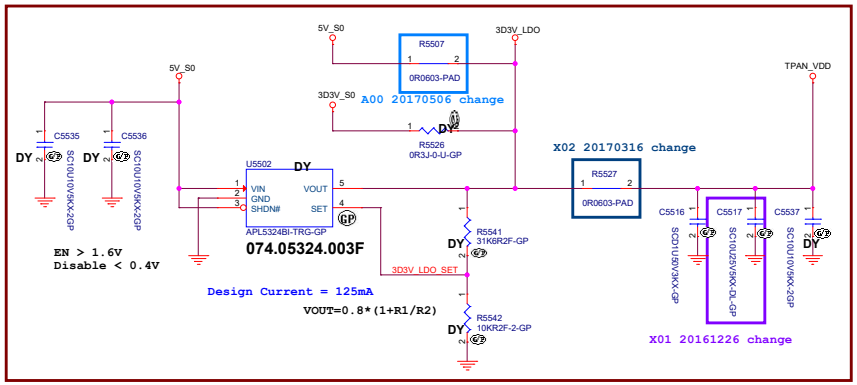
TP	PIN DEFINE
1	VUSB_3.3V
2	NC
3	SCL
4	SDA
5	UA_INT
6	RESET
7	Report Switch
8	NC
9	GND
10	GND







TOUCH PANEL POWER



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 55 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 56 of 106

Main Func = HDMI

X01 20161228 change

A00 20170506 change

X01 20161228 change

X02 20170302 change

X02 20170313 change

X01 20161228 change

X01 20170105 change

X01 20170104 change

HDMI CONN

Close to U5701

<Core Design>

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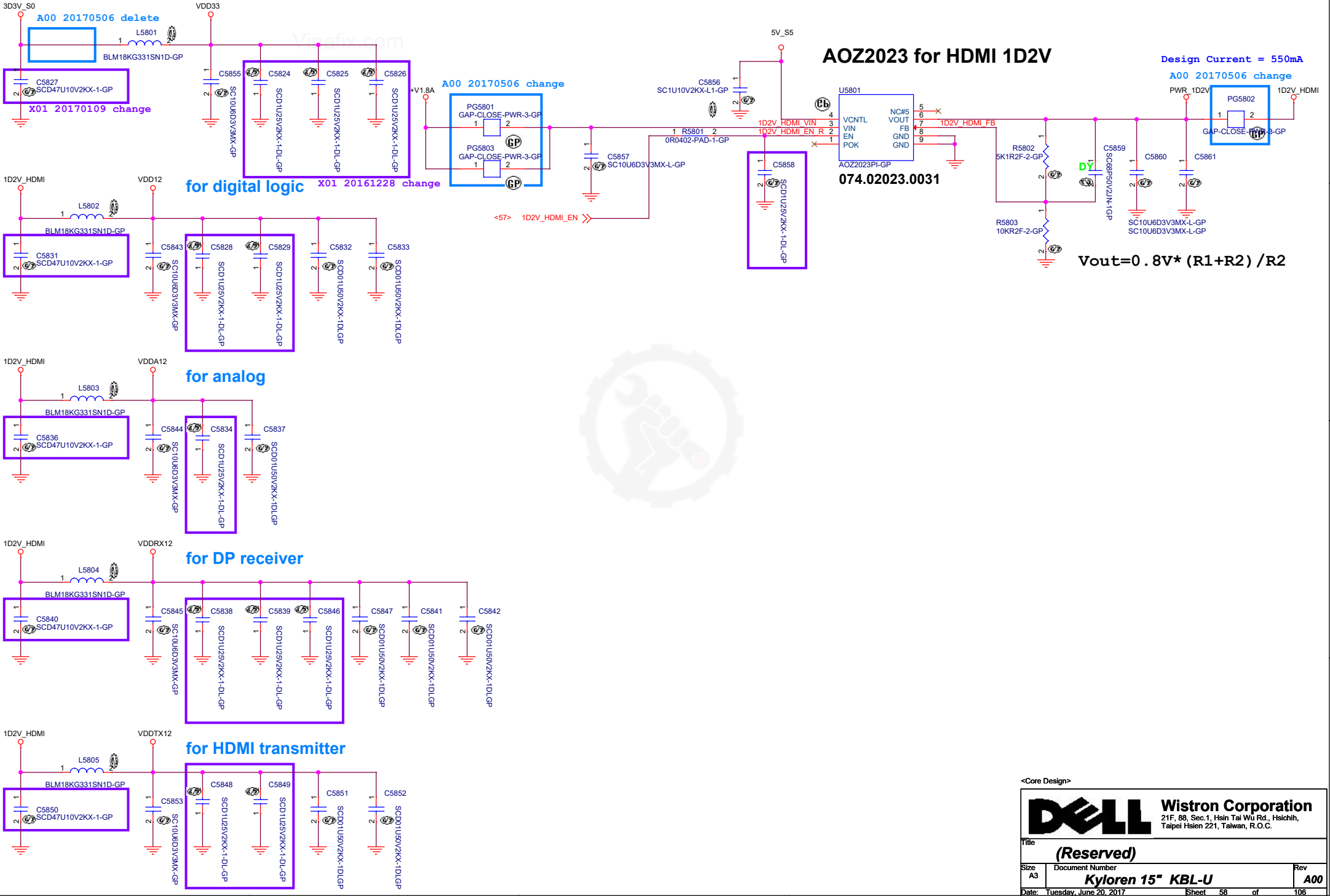
Title	HDMI
Size: A2	Document Number: Kyloren 15" KBL-U
Rev	A00
Date: Tuesday, June 20, 2017	Sheet 57 of 106

Main Func = HDMI



<Core Design>

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Title	(Reserved)	
Size A3	Document Number: Kyloren 15" KBL-U	Rev: A00
Date: Tuesday, June 20, 2017	Sheet 58 of 106	

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<Core Design>

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Title: *(Reserved)*

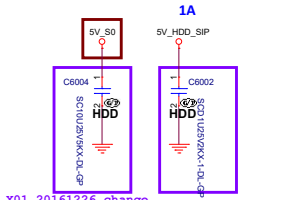
Size	Document Number	Rev
A3	*Kyloren 15" KBL-U*	*A00*

Date: Tuesday, June 20, 2017 Sheet 59 of 106

Main Func = HDD

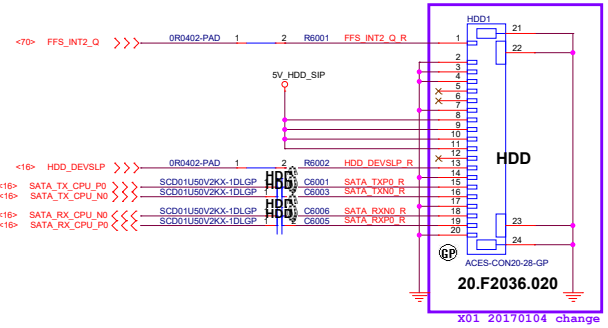
SATA HDD Connector

A00 20170506 change

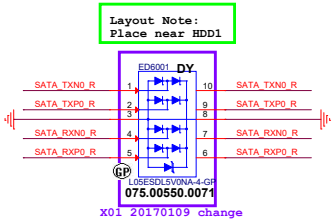


X01 20161226 change

X01 20161228 change



X01 20170104 change



X01 20170109 change

Main Func = ODD

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF_HDD/ODD

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 60 of 106

Main Func = WLAN

<Core Design>

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Title

NGFF_WLAN CONN

Size	Document Number	Rev
A3	*Kyloren 15" KBL-U*	*A00*

Date: Tuesday, June 20, 2017 Sheet 61 of 106

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	*Kyloren 15" KBL-U*	*A00*

Date: Tuesday, June 20, 2017 Sheet 62 of 106

SSD M.2

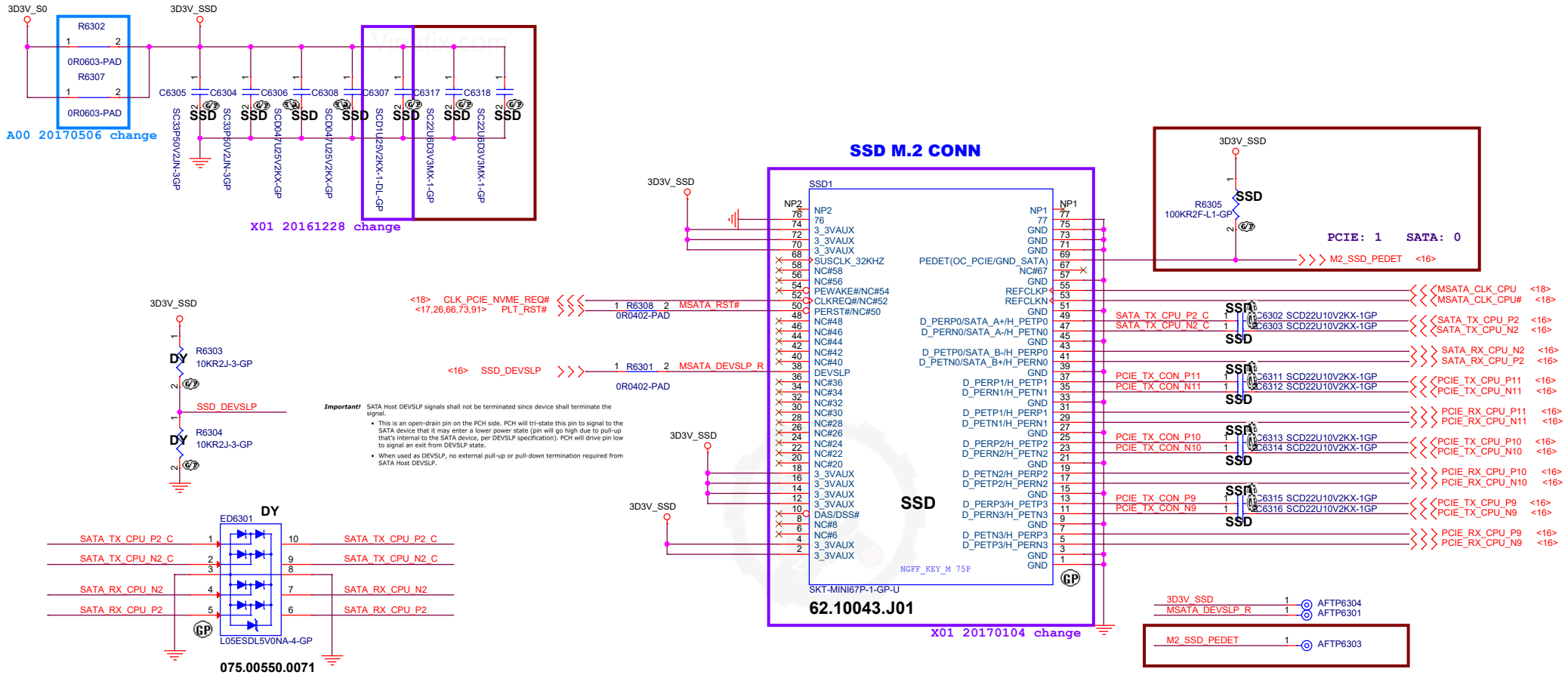


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

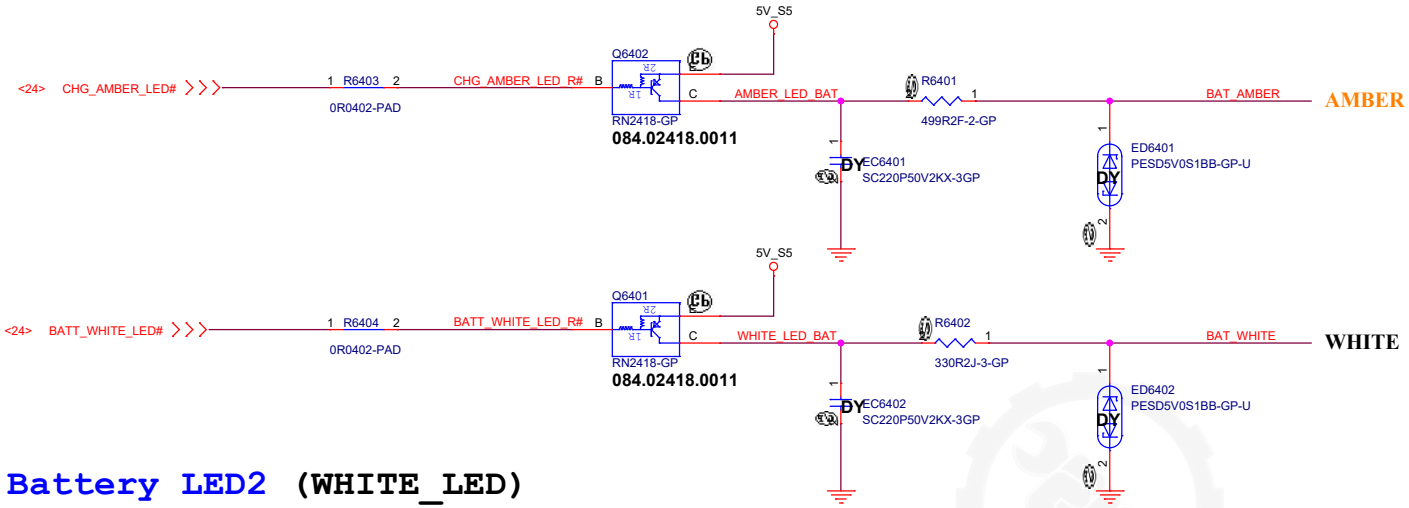
1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

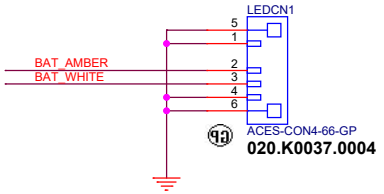
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Main Func = Power BTN

Battery LED1 (AMBER_LED)

Low actived from KBC GPIO

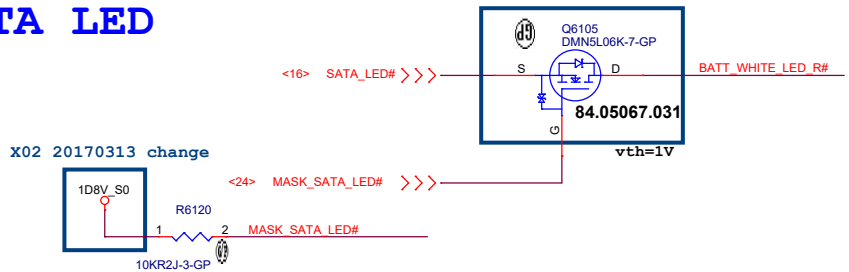




Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

SATA LED



<Core Design>

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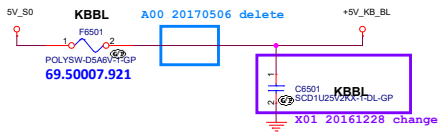
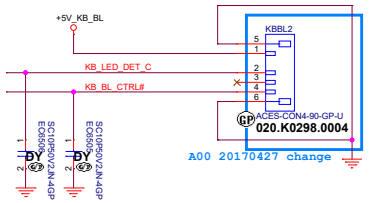
Taipei Hsien 221, Taiwan, R.O.C.

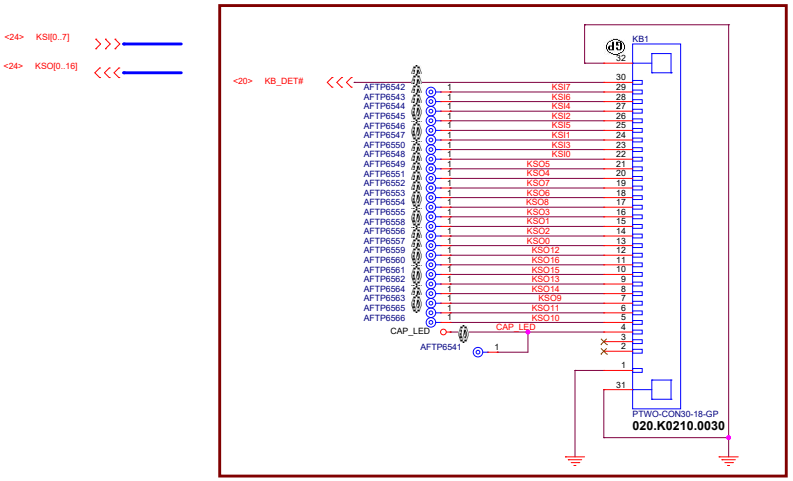
Title	LED Board&Power Button	
Size A3	Document Number Kyloren 15" KBL-U	Rev A00
Date: Tuesday, June 20, 2017	Sheet 64 of 106	

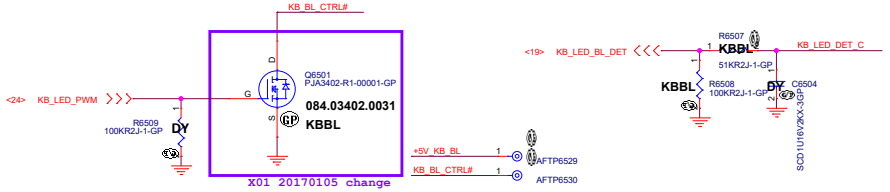
Main Func = Keyboard

KB Backlight Power Consumption: 285mA max.

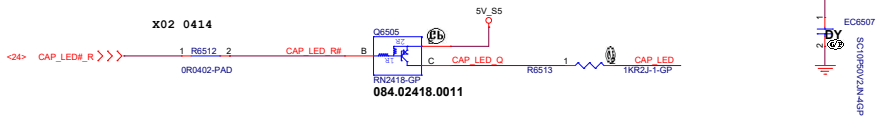




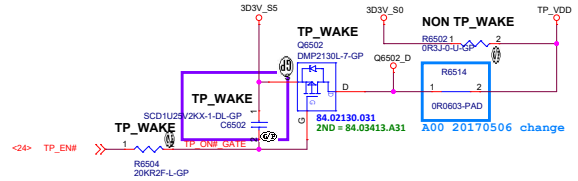




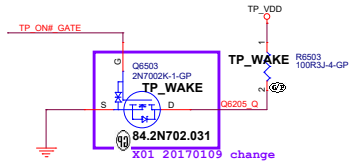
CAP LED Control
LOW actived from KBC GPIO



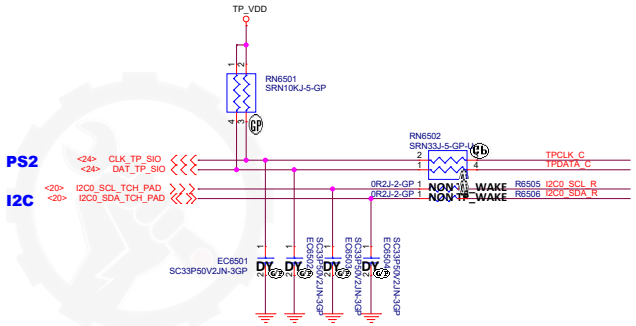
Main Func = TPAD

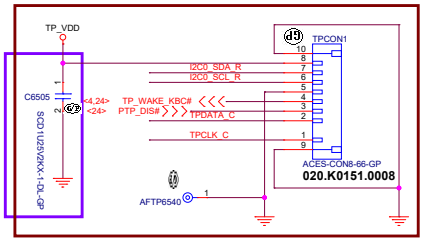


TP_VDD Discharge Circuit



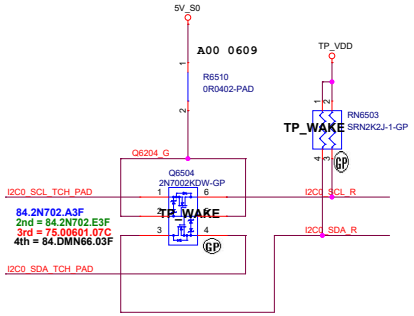
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

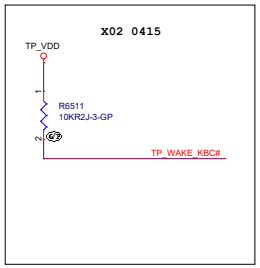




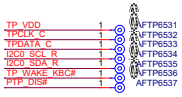
Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

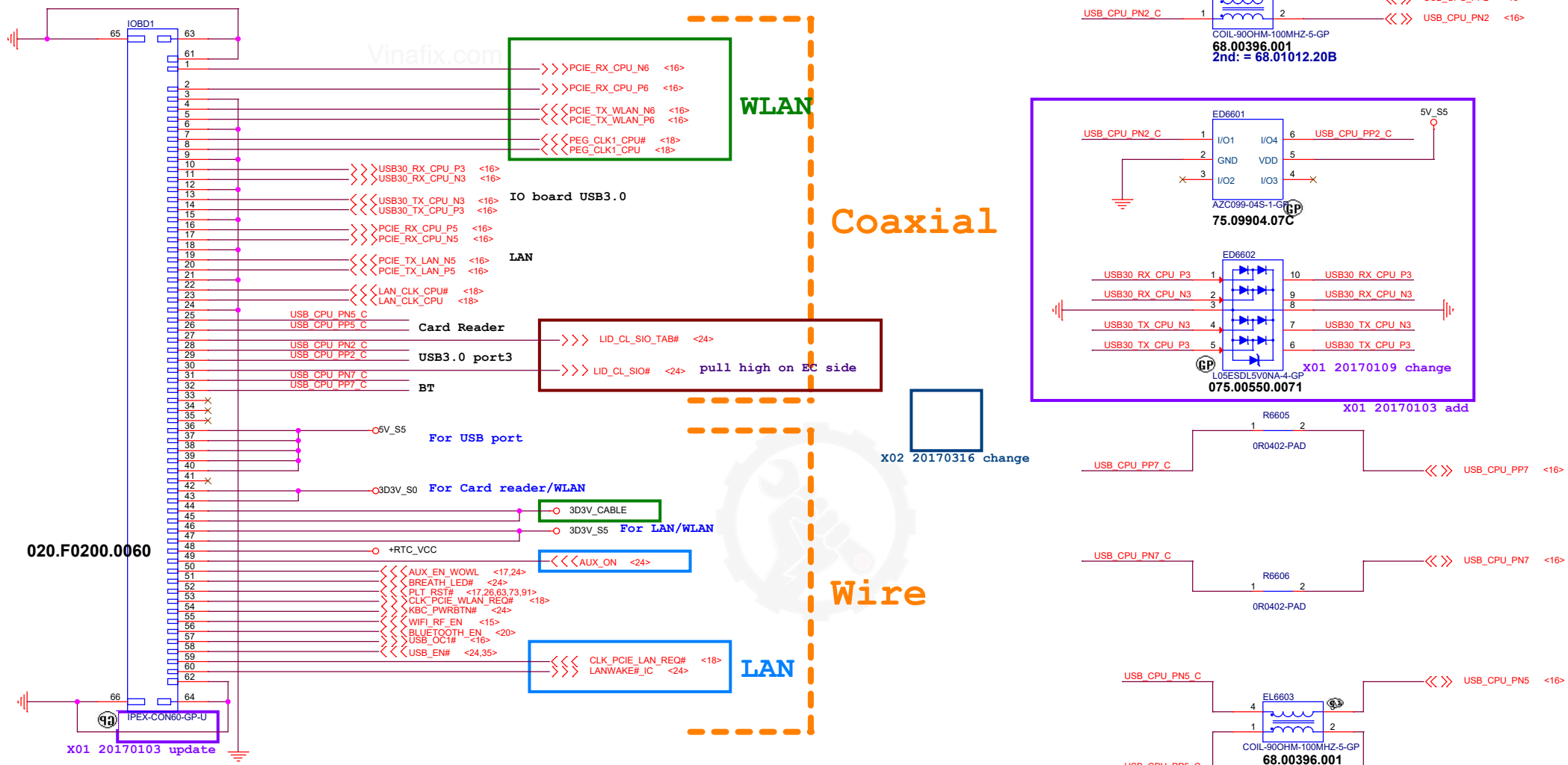


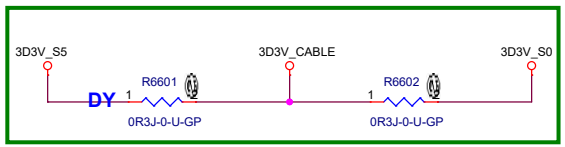
<Core Design>

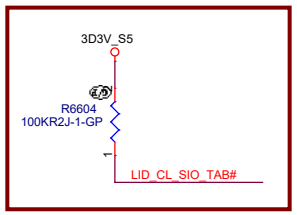
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad
Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00
Date: Tuesday, June 20, 2017 | Sheet 65 of 106

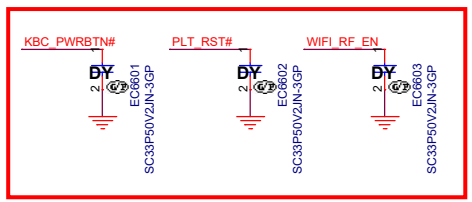
Main Func = IO Connector

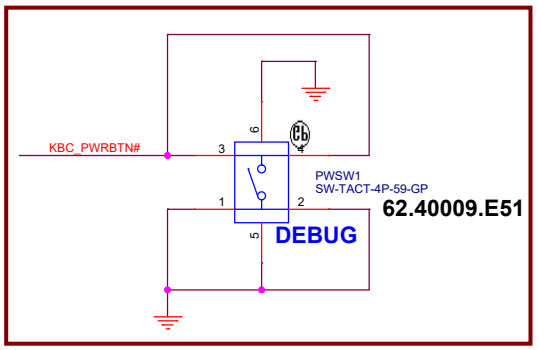






EMI Reserve , 20141118





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

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<Core Design>

Wistron Corporation
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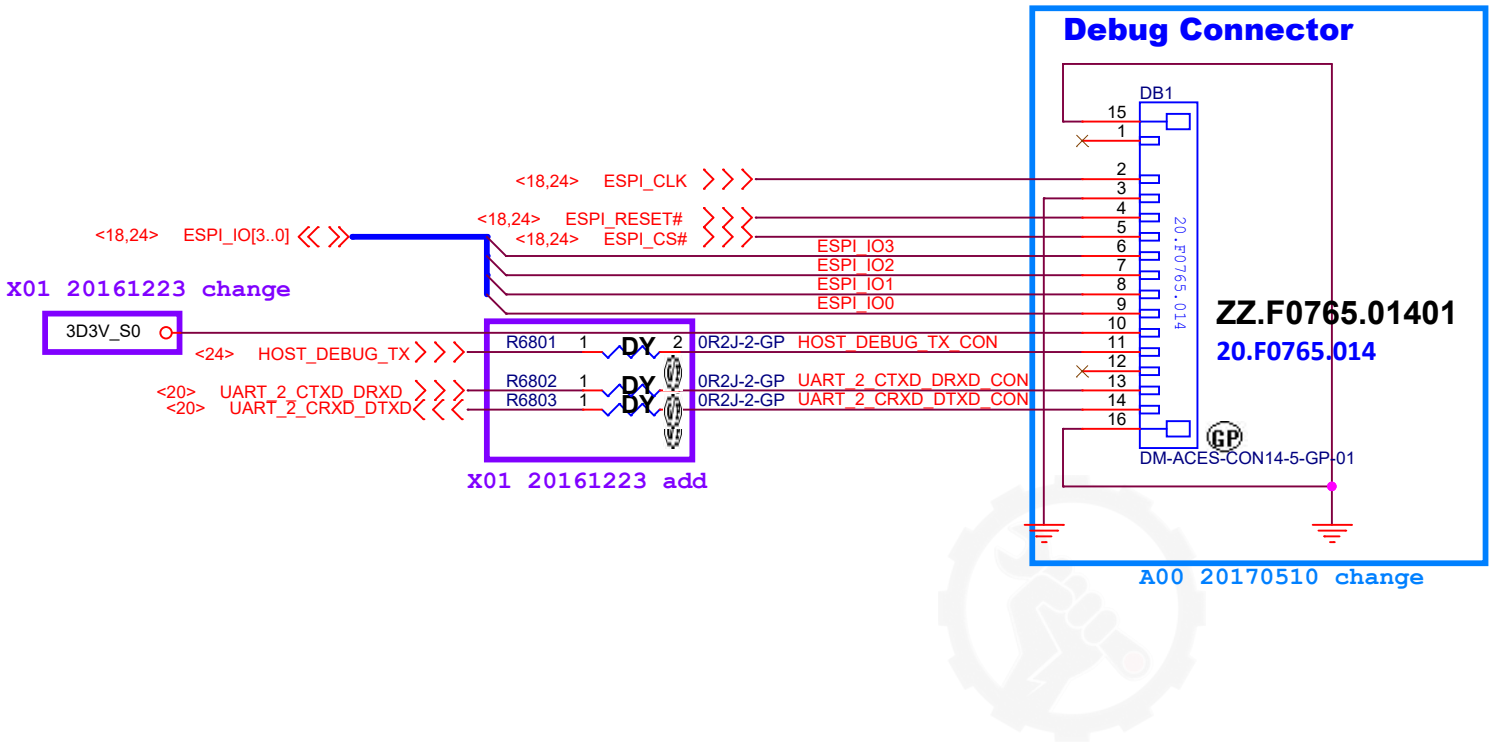
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Kyloren 15" KBL-U* | Rev: *A00*

Date: Tuesday, June 20, 2017 | Sheet 67 of 106

Main Func = Debug



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Dubug connector*	
Size A4	Document Number *Kyloren 15" KBL-U*	Rev *A00*
Date: Tuesday, June 20, 2017	Sheet 68 of 106	

<Core Design>

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Title

Reserved

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

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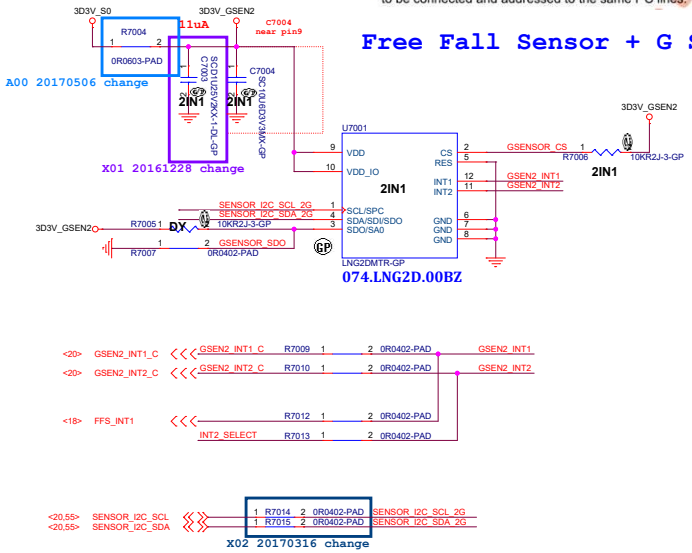
Main Func = Free Fall Sensor

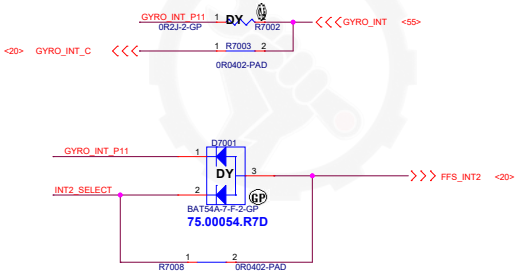
LID sensor

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor

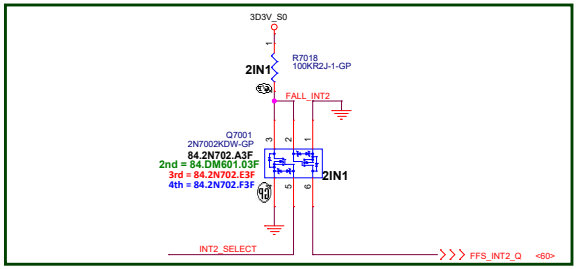


combine G



Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 70 of 106

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<Core Design>

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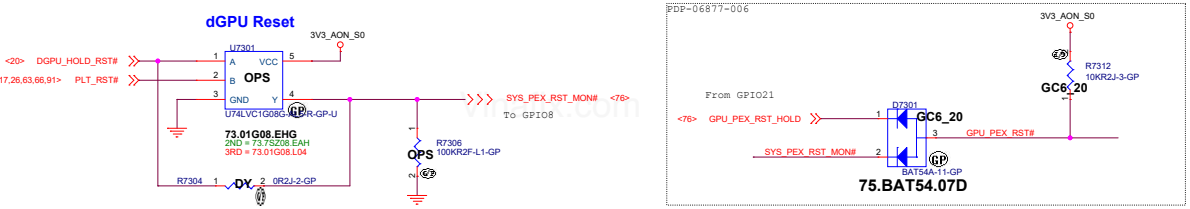
Title

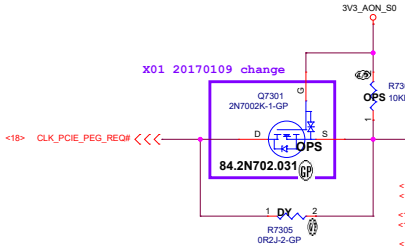
USB3.0 PORT

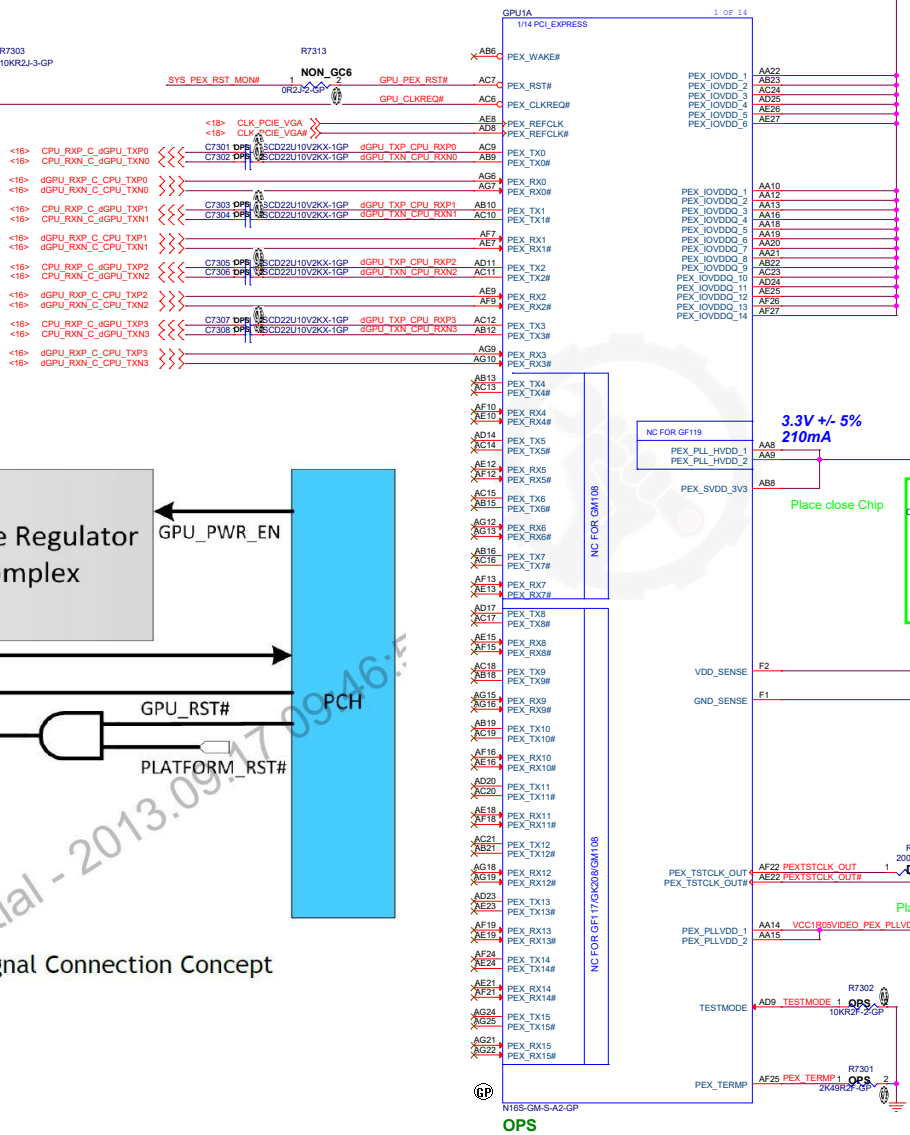
Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 72 of 106

Main Func = dGPU







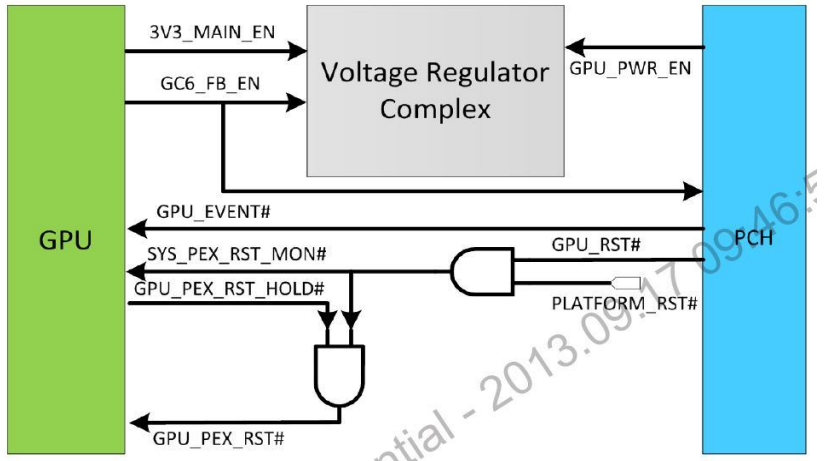


Figure 18-11. GC6 2.0 High-level Signal Connection Concept

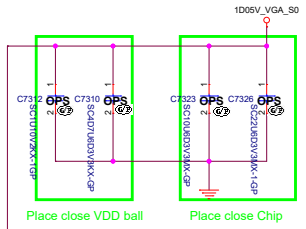
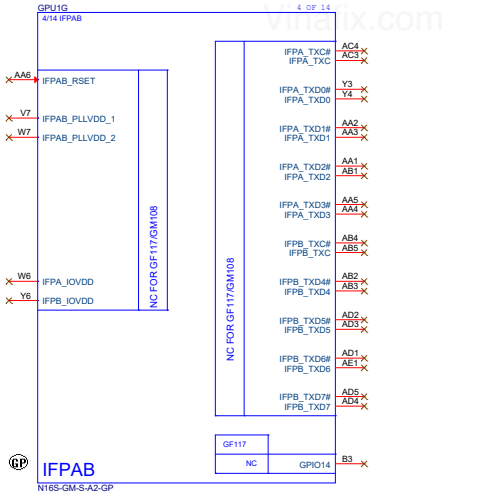
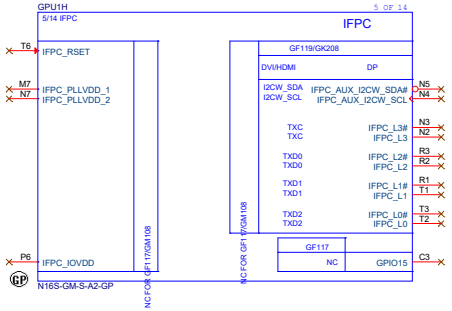


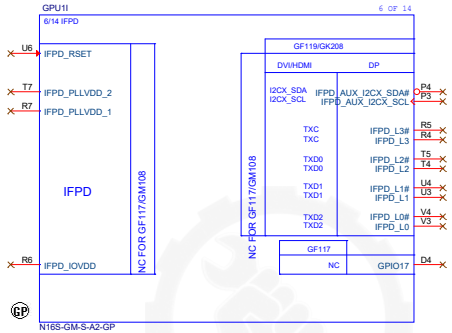
Table 3-16. PEX_IOVVD/Q Power Rail Combined

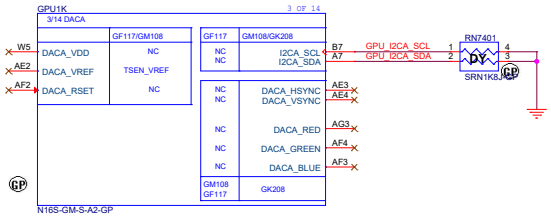
GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

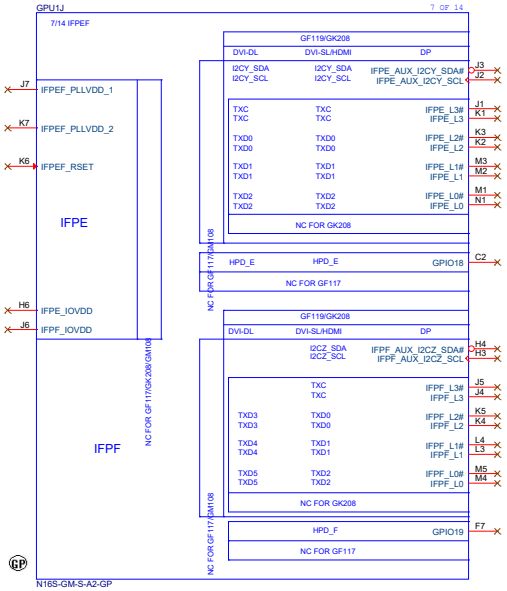
Main Func = dGPU











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Title: GPU(2/5)DIGITALOUT

Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 74 of 106

Main Func = dGPU

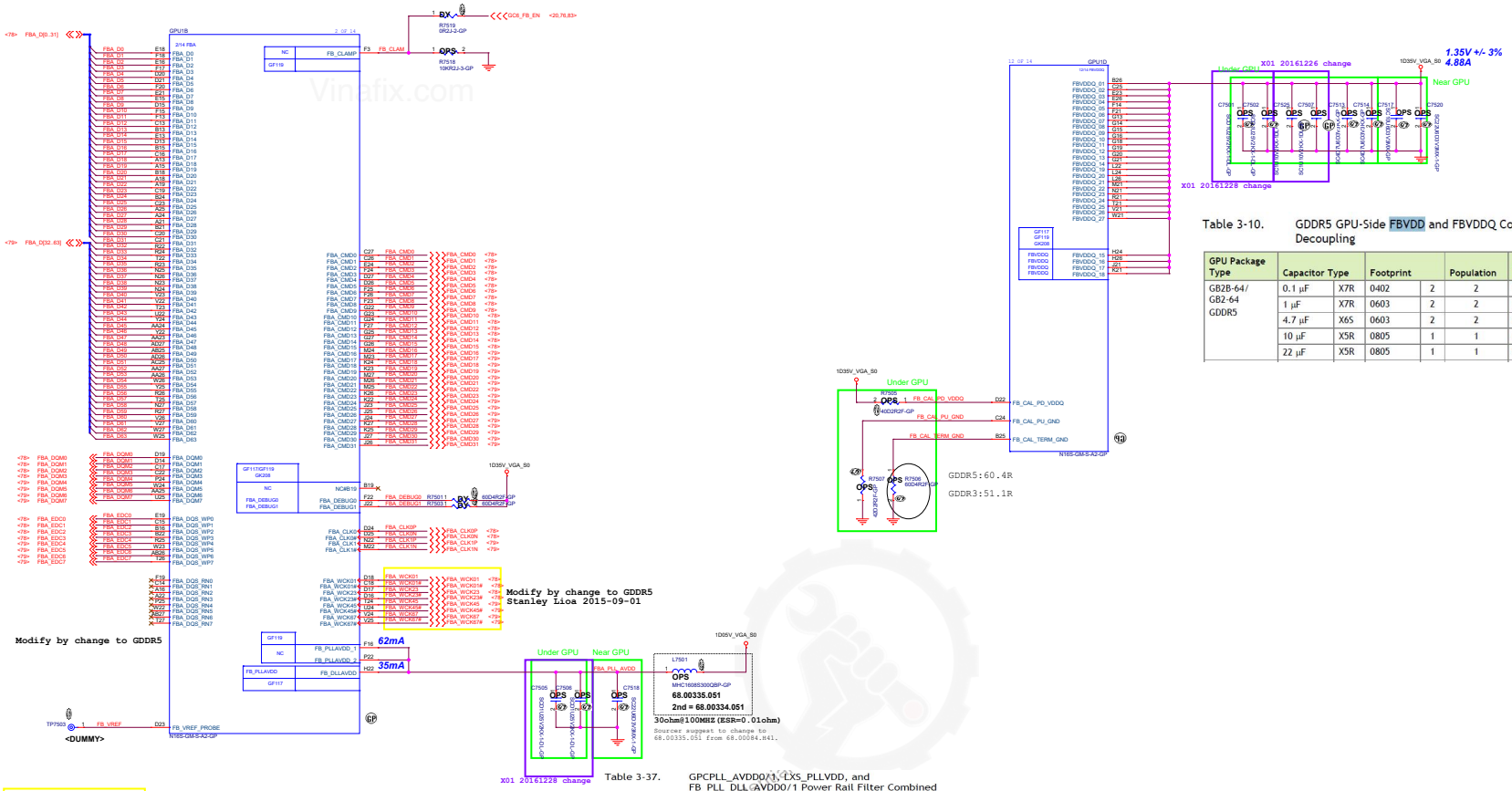


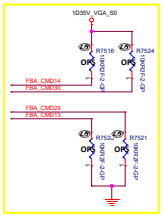
Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint	Population		Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

Table 3-37. GPCPLL_AVDD0/1, LXS_PLLVDD, and FB_PLL_DLL_AVDD0/1 Power Rail Filter Combined

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB3B-256	GPCPLL_AVDD0/1 + LXS_PLLVDD + FB_PLL_DLL_AVDD0/1	0.1 µF	X7R	0402	5	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5



<Core Design>

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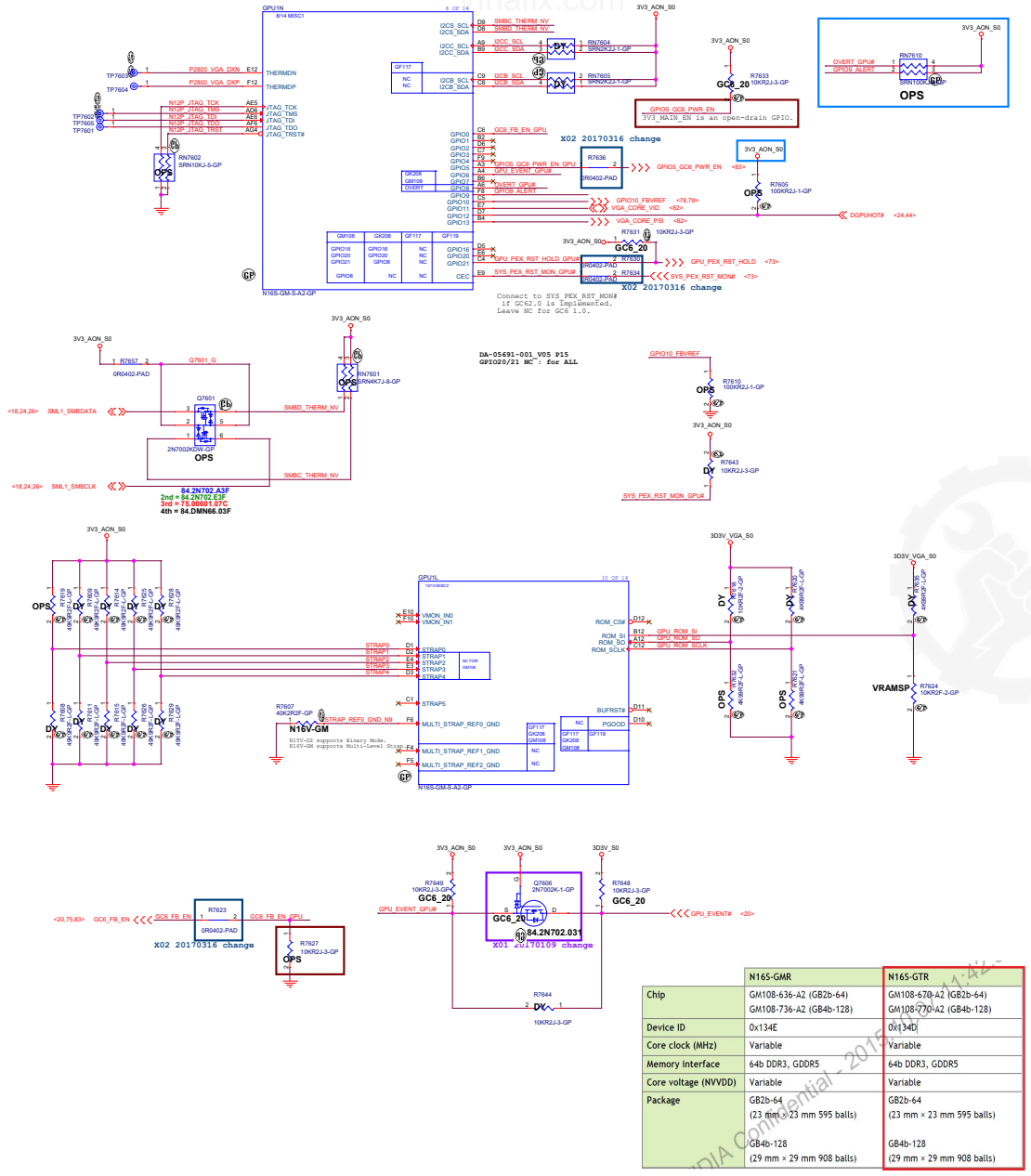
Title: GPU(3/5)VRAM/F

Size: A1 | Document Number: Kyloren 15" KBL-U | Rev: A00

Date: Tuesday, June 20, 2017 | Sheet 75 of 105

Main Func = dGPU



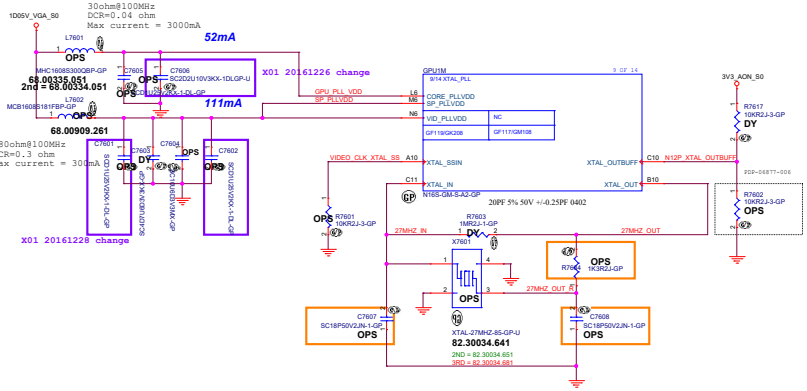


Table 12. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		128Mx32	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
		512Mx16	Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready.
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready

Note: For H16V-GMR1 and N16S-LG/-GMR/-GTR, the maximum allowable memory case temperature is 85 °C.

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND.			
STRAP2	Do not stuff.			
STRAP3				
STRAP4				

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

4.99K	64.49915.6DL
10K	64.10025.L0L
15K	64.15025.6DL
20K	64.20025.6DL
24.9K	64.24925.6DL
30.1K	64.30125.6DL
34.8K	64.34825.6DL
45.3K	64.45325.6DL

	N16S-GMR	N16S-GTR
Chip	GM108-636-A2 (GB2b-64) GM108-736-A2 (GB4b-128)	GM108-670-A2 (GB2b-64) GM108-770-A2 (GB4b-128)
Device ID	0x134E	0x134D
Core clock (MHz)	Variable	Variable
Memory Interface	64b DDR3, GDDR5	64b DDR3, GDDR5
Core voltage (NVVDD)	Variable	Variable
Package	GB2b-64 (23 mm × 23 mm 595 balls) GB4b-128 (29 mm × 29 mm 908 balls)	GB2b-64 (23 mm × 23 mm 595 balls) GB4b-128 (29 mm × 29 mm 908 balls)

STRAP PIN MODE TABLE

PIN NAME	GK208: MULTI-LEVEL bit [3:0]	GF117: BINARY STRAPS
STRAP0	USER[3:0]	RAM_CFG[0]
STRAP1	3GIO_PADCFG_ADR[3:0]	RAM_CFG[1]
STRAP2	PCI_DEVID[3:0]	RAM_CFG[2]
STRAP3	SOR[3:0]_EXPOSED	RAM_CFG[3]
STRAP4	RESERVED, PCIE_SPEED_CHANGE_GNE3, PCIE_MAX_SPEED, DP_PLL_VDD_33V	PCIE_MAX_SPEED
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, PCIDEVID[5], PEX_PLL_EN_TERM	SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]	SUB_VENDOR
ROM_SO	FB[1], FB[0], SMB_ALT_ADDR, VGA_DEVICE	VGA_DEVICE

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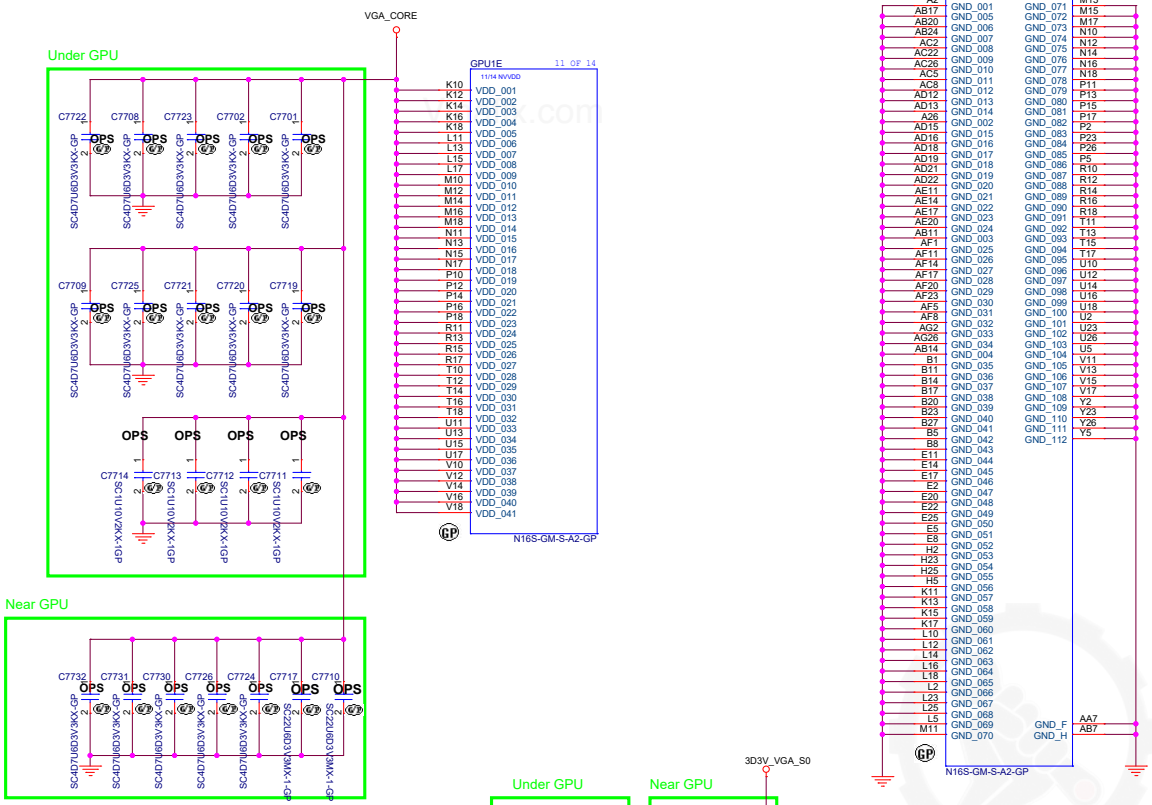
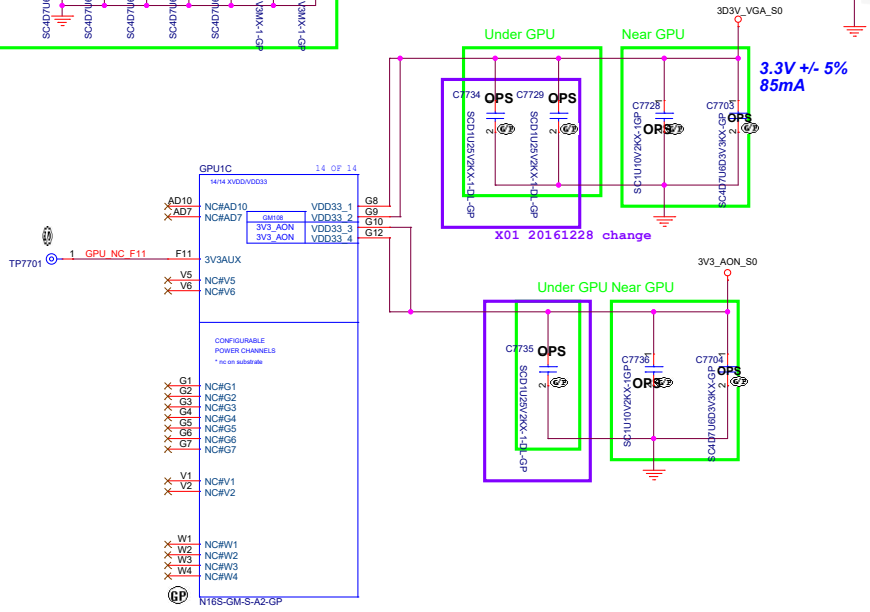
Title: GPU(4/5)GPIO/STRAP

Size	Document Number	Rev
Custom	Kyloren 15" KBL-U	A00
Date: Tuesday, June 20, 2017	Sheet 76 of 106	

Main Func = dGPU





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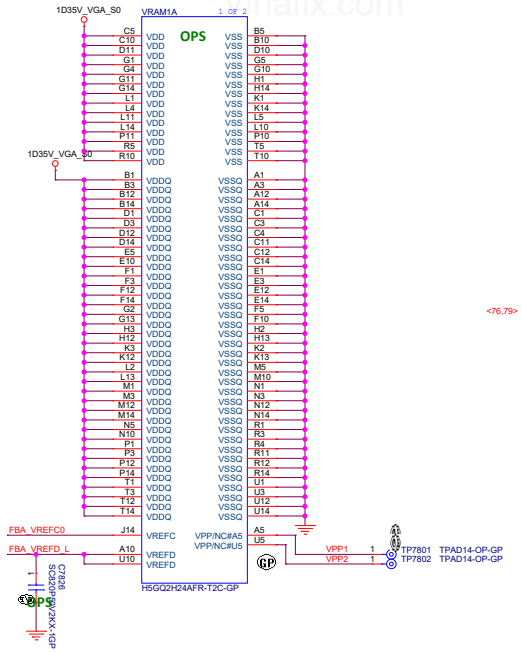
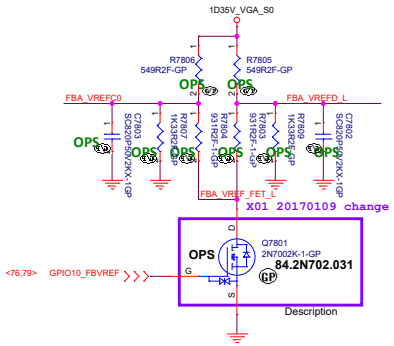
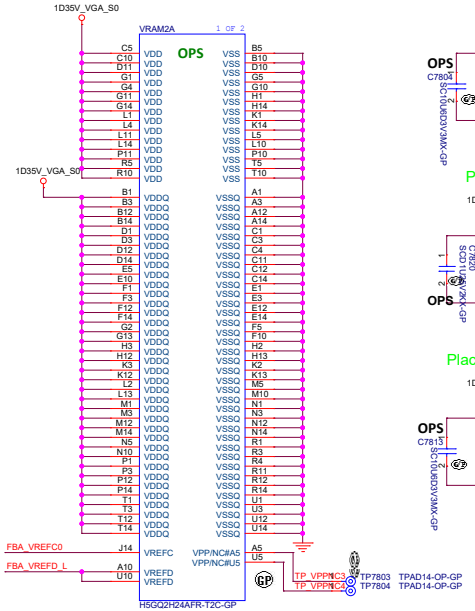


Frame Buffer Patition A-Lower Half

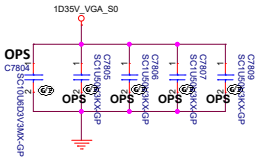


FBVREF Termination

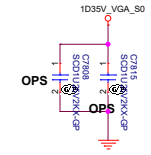
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



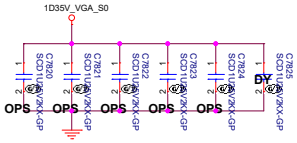
Place close VDD ball



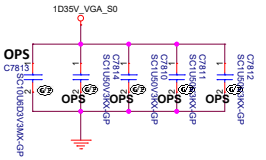
Place close VDD ball



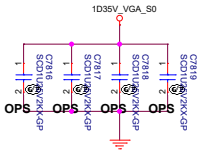
Place close VDD ball



Place close VDDQ ball



Place close VDDQ ball



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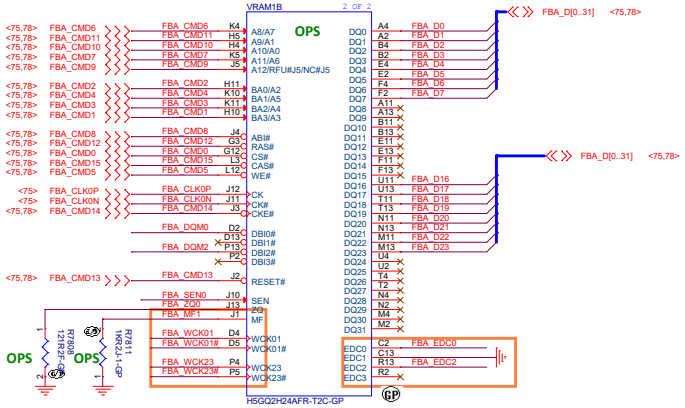

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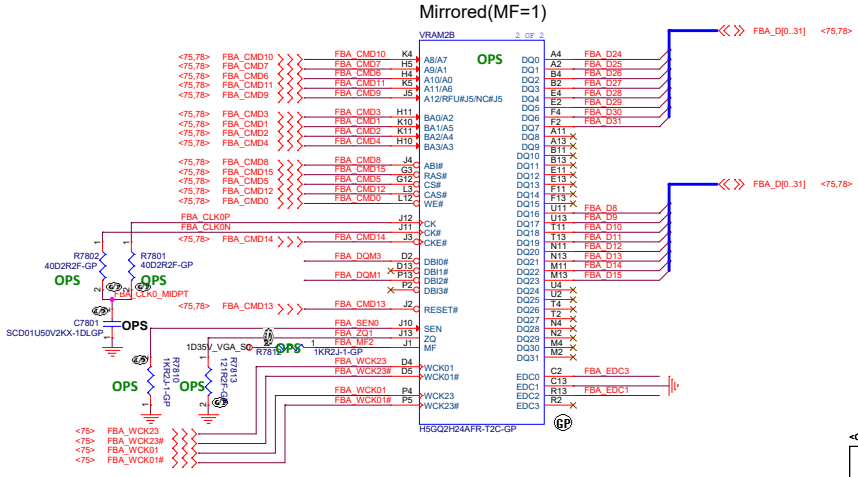

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Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

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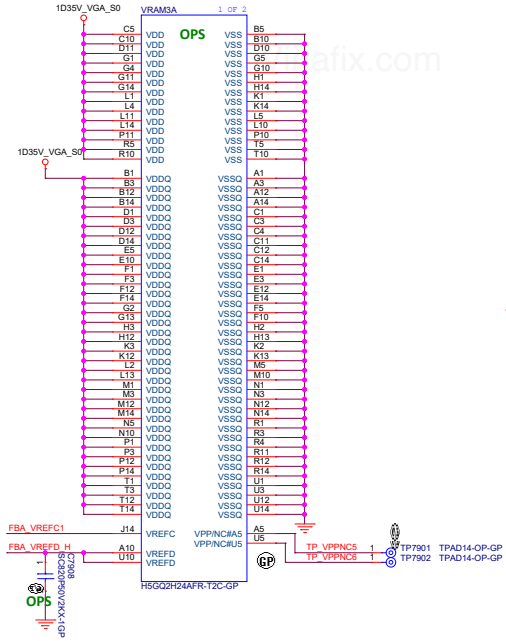
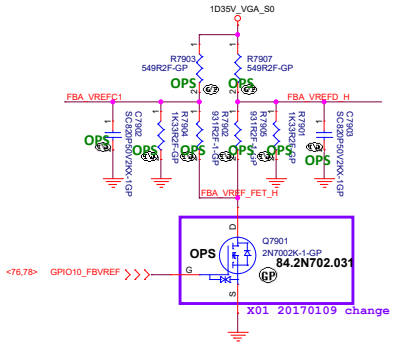
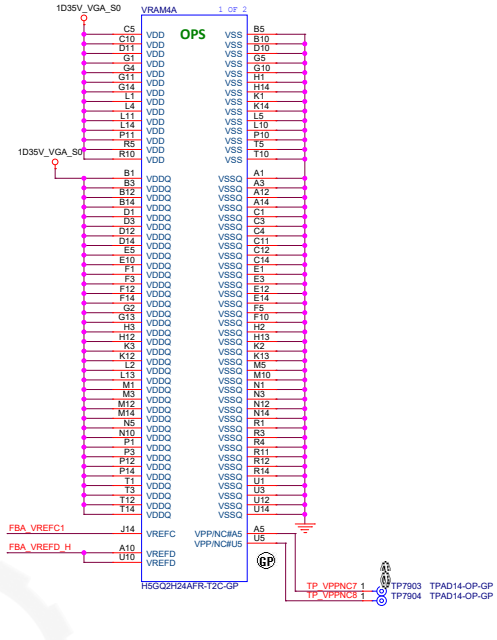


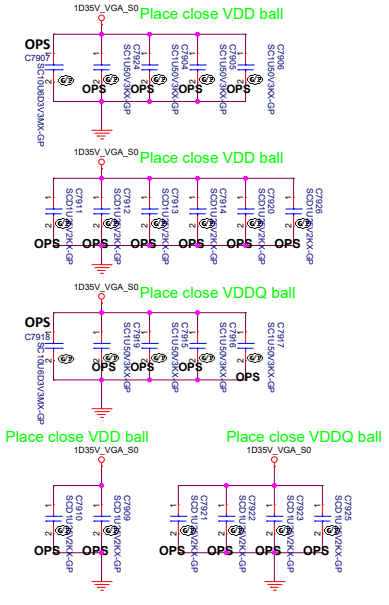
Frame Buffer Patition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





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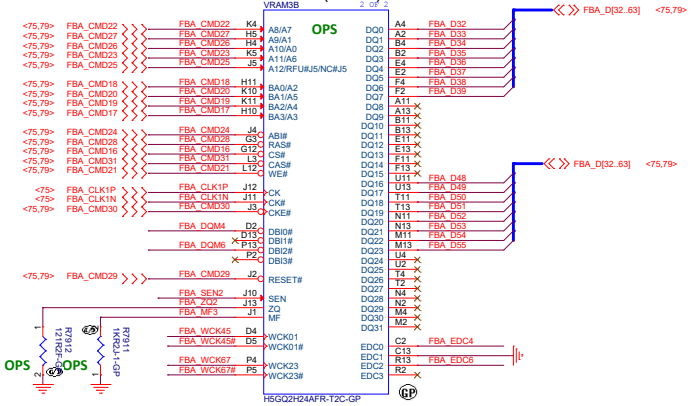

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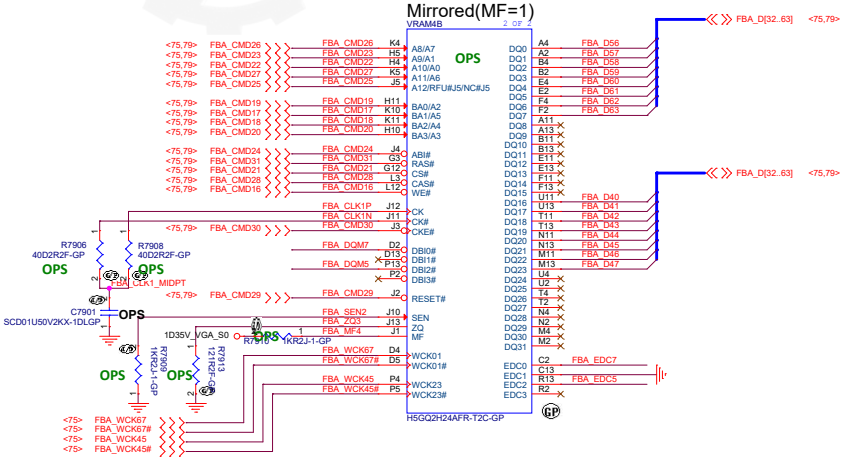

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 79 of 106

Main Func = dGPU

<Core Design>

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Title: GPU(5/5)PWR/GND

Size	Document Number	Rev
Custom	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 80 of 106

Main Func = dGPU

<Core Design>

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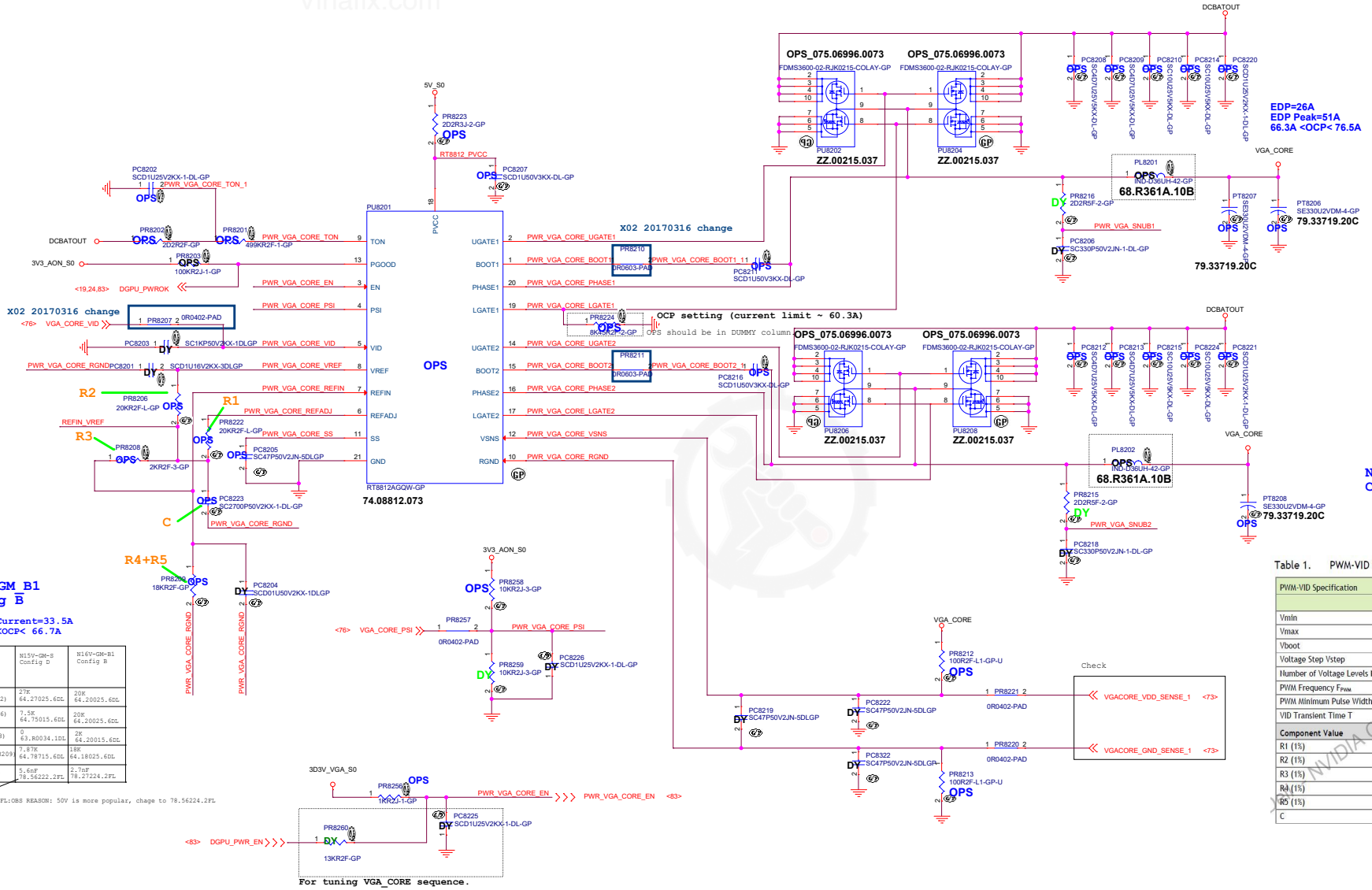
Title: *GPU-VRAM1,2 (1/4)*

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 81 of 106

Main Func = dGFX_CORE



Component value	N15V-GM-S Config D	N16V-GM-B1 Config B
R1 (PR8222)	27K 64.27025.6DL	20K 64.20025.6DL
R2 (PR8206)	7.5K 64.75015.6DL	20K 64.20025.6DL
R3 (PR8208)	0 63.R0034.1DL	2K 64.20015.6DL
R4+R5 (PR8209)	7.87K 64.78715.6DL	18K 64.18025.6DL
C (PC8223)	5.6nF 78.56222.2FL	2.7nF 78.27224.2FL

78.56222.2FL:OBS REASON: 50V is more popular, chage to 78.56224.2FL

Table 1. PWM-VID Spec and Component Values

PWM-VID Specification		Config A	Config B
Vmin	V	0.6	0.6
Vmax	V	1.2	1.2
Vboot	V	0.875	0.9
Voltage Step Vstep	mV	6.25	6.25
Number of Voltage Levels N	level	96	96
PWM Frequency F_{PWM}	MHz	1.125	1.125
PWM Minimum Pulse Width T_{SWIN}	ns	9.26	9.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KΩ	39	20
R2 (1%)	KΩ	39	20
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

<Core Design>

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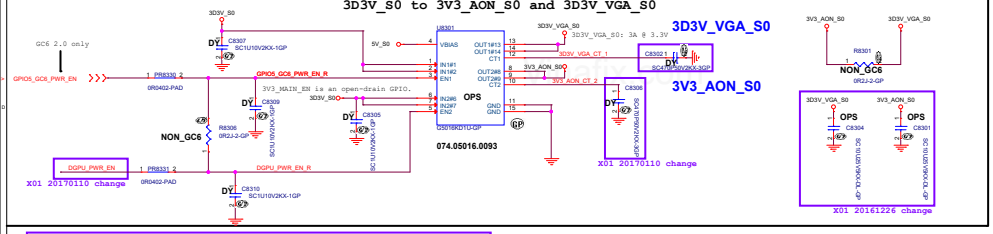
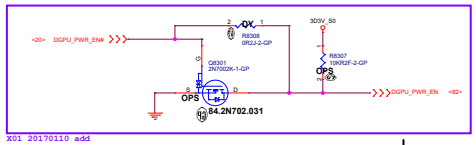
Title: RT8812_VGACORE
Size: A2 | Document Number: Kyloren 15" KBL-U | Rev: A00
Date: Tuesday, June 20, 2017 | Sheet 82 of 106

Main Func = dGPU

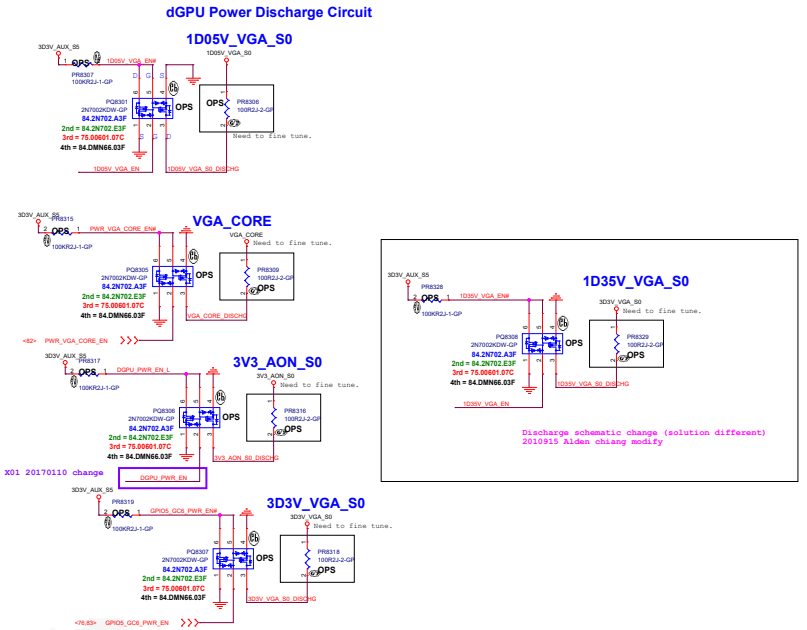
[DG-07158-001 Rev03]Power up sequence:
3.3V ==> NVVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> FBVDD/Q (1.35V)

3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0

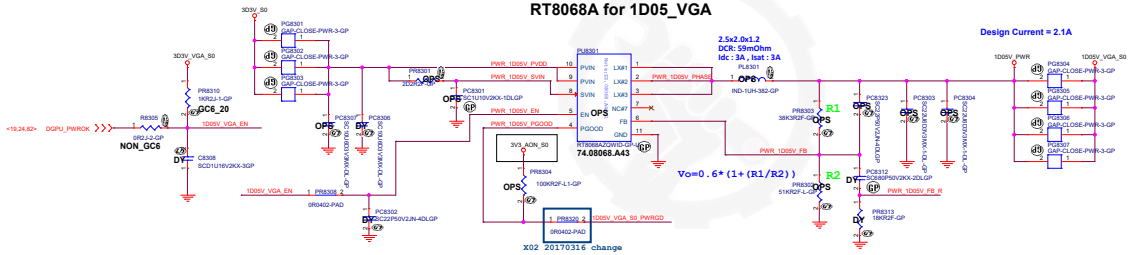




dGPU Power Discharge Circuit

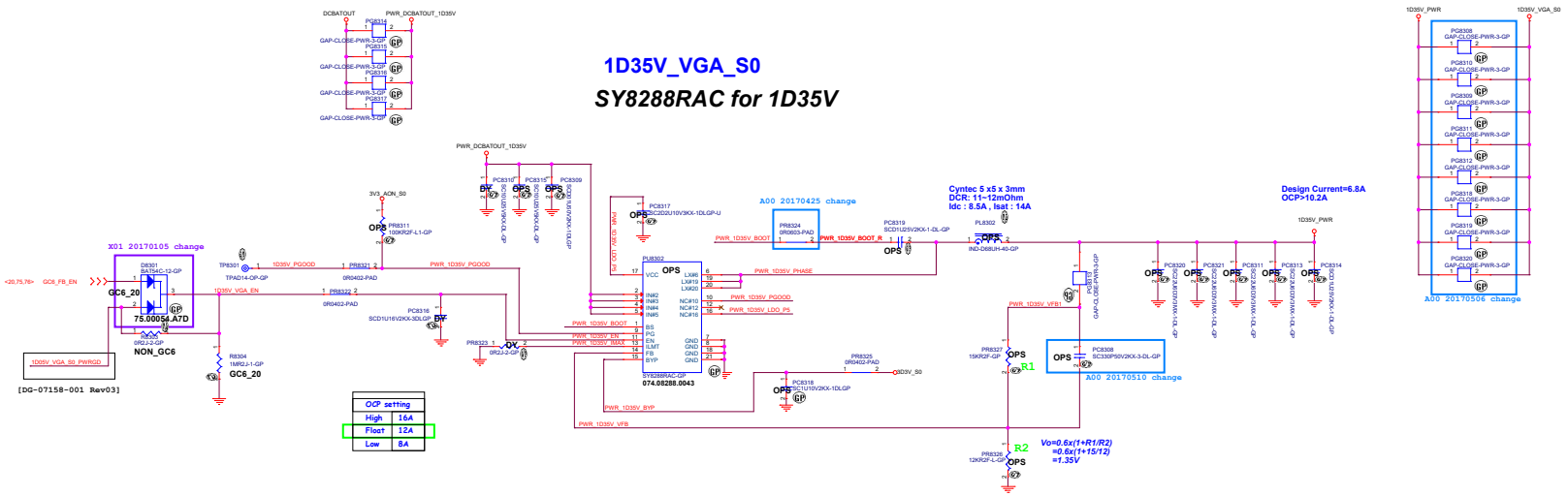


RT8068A for 1D05_VGA



1D35V_VGA_S0

SY8288RAC for 1D35V



OCP setting	
High	16A
Float	12A
Low	8A

<Core Design>

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Title: DISCRETE VGA POWER

Size	Document Number	Rev
A1	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 | Sheet 83 of 105

Main Func = dGPU

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

Date: Tuesday, June 20, 2017 Sheet 84 of 106

Main Func = dGFX_CORE

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU CORE

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

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Main Func = dGPU

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Title

GPU Discrete Power

Size	Document Number	Rev
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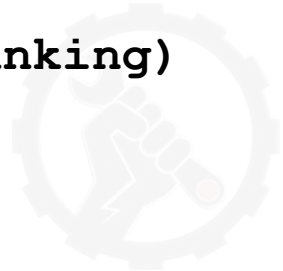

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Main Func = UnusedParts

SPR1 SPRING-171-GP 34.4YW18.001 DY
SPR2 SPRING-171-GP 34.4YW18.001 DY
SPR3 SPRING-171-GP 34.4YW18.001 DY
SPR4 SPRING-63-GP 34.4Y806.001 DY

X01 20170104 change

ZZ.00PAD.7F1

H2 HOLE335R178-GP ZZ.00PAD.7F1
H4 HOLE335R178-GP ZZ.00PAD.7F1
H7 HOLE335R178-GP ZZ.00PAD.7F1
H8 HOLE335R178-GP ZZ.00PAD.7F1
H1 HOLE335R178-GP ZZ.00PAD.7F1
H11 HOLE335R178-GP ZZ.00PAD.7F1
H12 HOLE335R178-GP ZZ.00PAD.7F1
H14 HOLE335R178-GP ZZ.00PAD.7F1
H3 HOLE335R178-GP ZZ.00PAD.7F1
H5 HOLE335R178-GP ZZ.00PAD.7F1
H6 HOLE335R178-GP ZZ.00PAD.7F1

Type-C

HS2 STF217R115H101-2-GP 434.04X0C.1001

3D3V_S0 — A00 20170506 change
5V_S0
3D3V_S5
5V_S5

SSID = EMI

Mind the voltage rating of the caps.

AUD_AGND
DCBATOUT

X01 20170103 change

3D3V_S0 — A00 20170506 change
3D3V_S5
+DC_IN
5V_S5
5V_S0 — A00 20170506 change
1D2V_S3 — X01 20161230B change

EMI reserve , 20141118
VCC_CORE
+VCCGT
+VCCSA

SSID = RF

1D2V_S3 — X01 20161230B change
DCBATOUT
1D2V_S3 — X01 20161230B change

+SDC_IN
VGA_CORE
VCC_CORE
+VCCSA
+VCCIO

X01 20161230B change

For GPU

Mind the voltage rating of the caps.
DCBATOUT

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Title: UNUSED PARTS/EMI Capacitors
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Title: *Reserved*

Size: A3 | Document Number: *Kyloren 15" KBL-U* | Rev: *A00*

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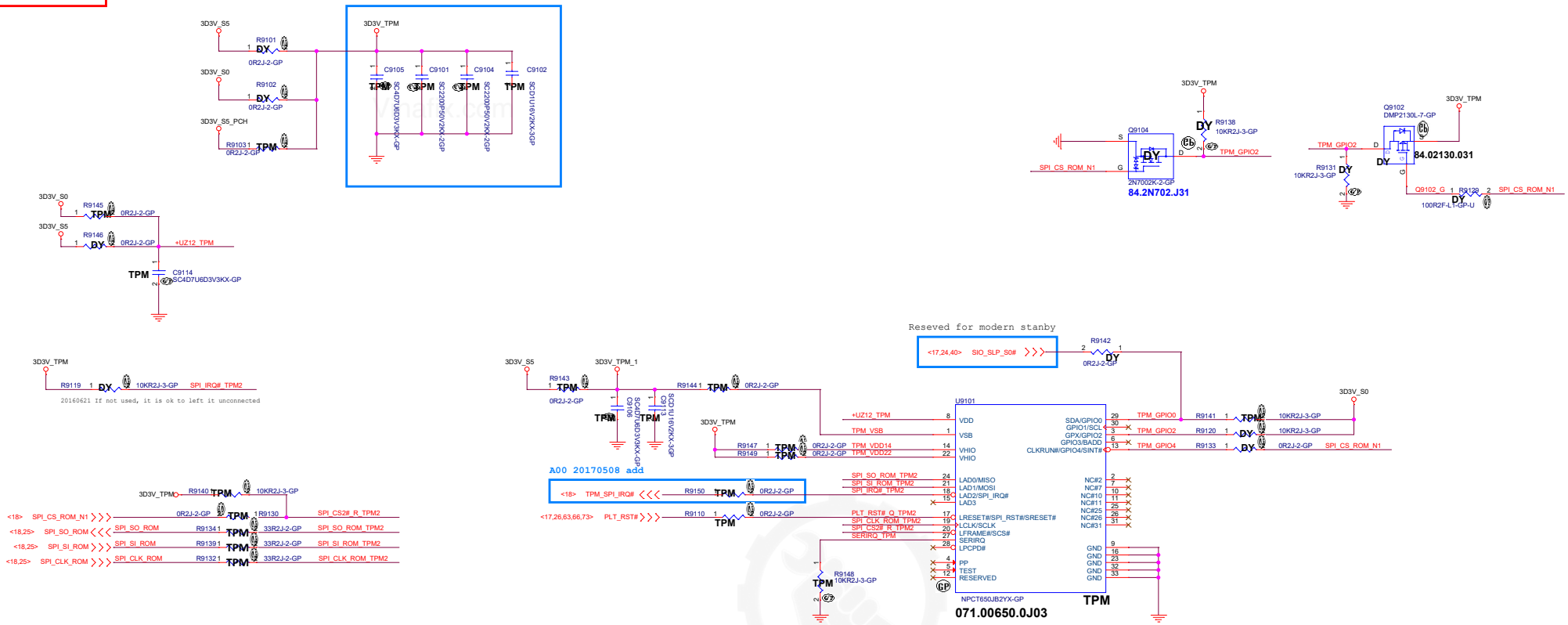
SSID = TPM



<Core Design>

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Title	TPM2.0	
Size A2	Document Number: Kyloren 15" KBL-U	Rev: A00
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Main Func = Finger Print

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Title: *Finger Print*

Size: A3 | Document Number: *Kyloren 15" KBL-U* | Rev: *A00*

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(Blanking)

<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Kyloren 15" KBL-U*	*A00*

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Kyloren 15" KBL-U*	*A00*

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Kyloren 15" KBL-U*	*A00*

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Title: *(Reserved)*

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Title: *LVDS_Switch*

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

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Title: CRT_Switch

Size	Document Number	Rev
A3	Kyloren 15" KBL-U	A00

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Main Func = Debug

<Core Design>

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Title: CPU_XDP;PCH_XDP

Size	Document Number	Rev
A2	Kyloren 15" KBL-U	A00

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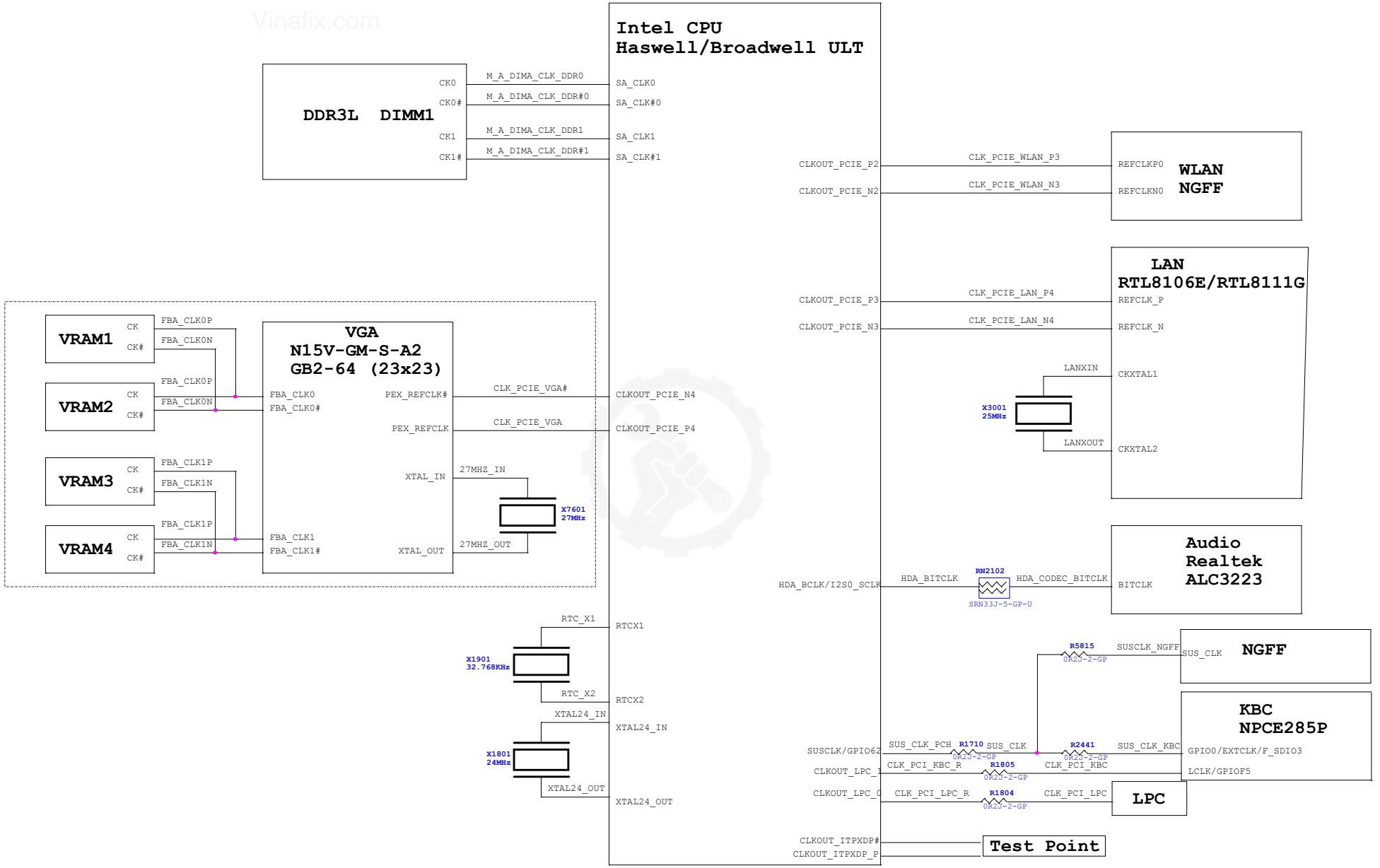
CLK Block Diagram



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CLK Block Diagram
Size: A2
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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: Change History

Size	Document Number	Rev
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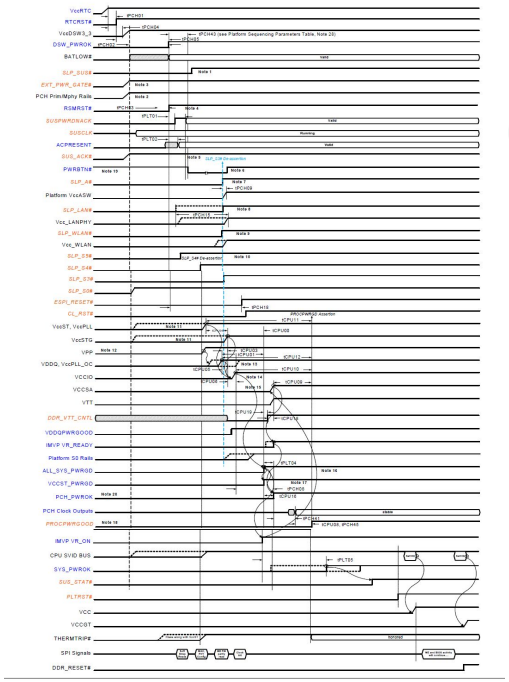
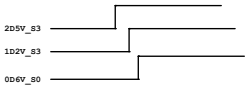
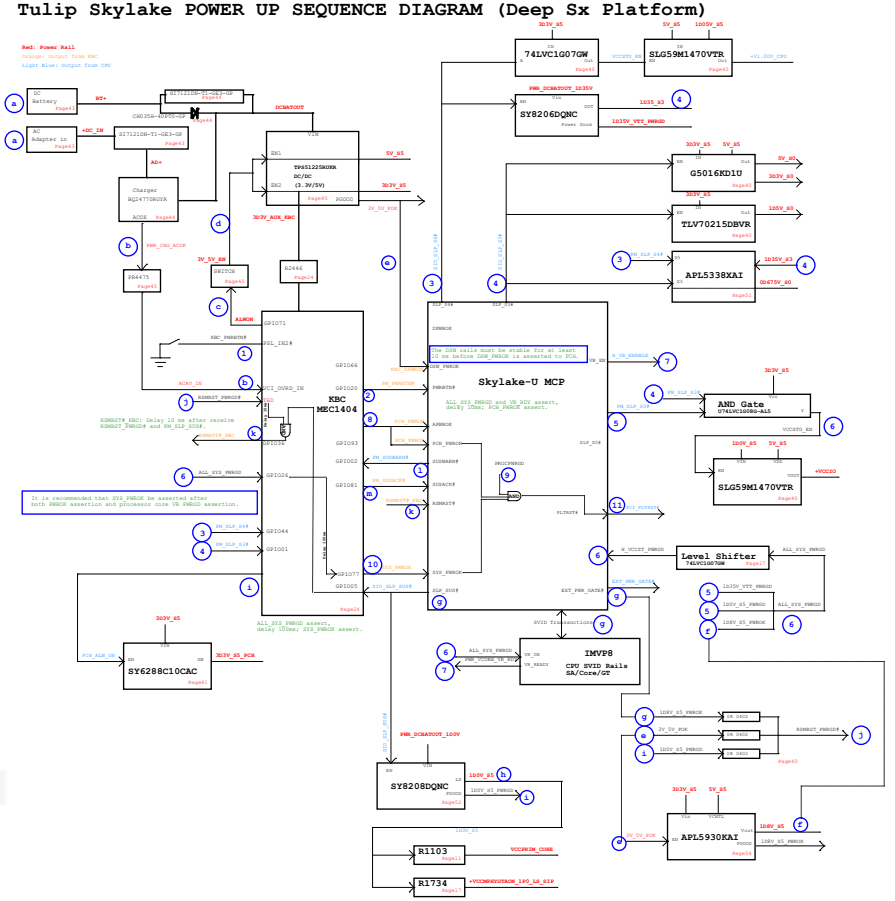
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



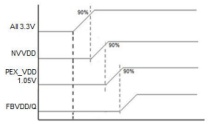
For DDR4 power sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:
- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

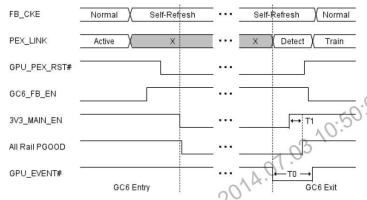
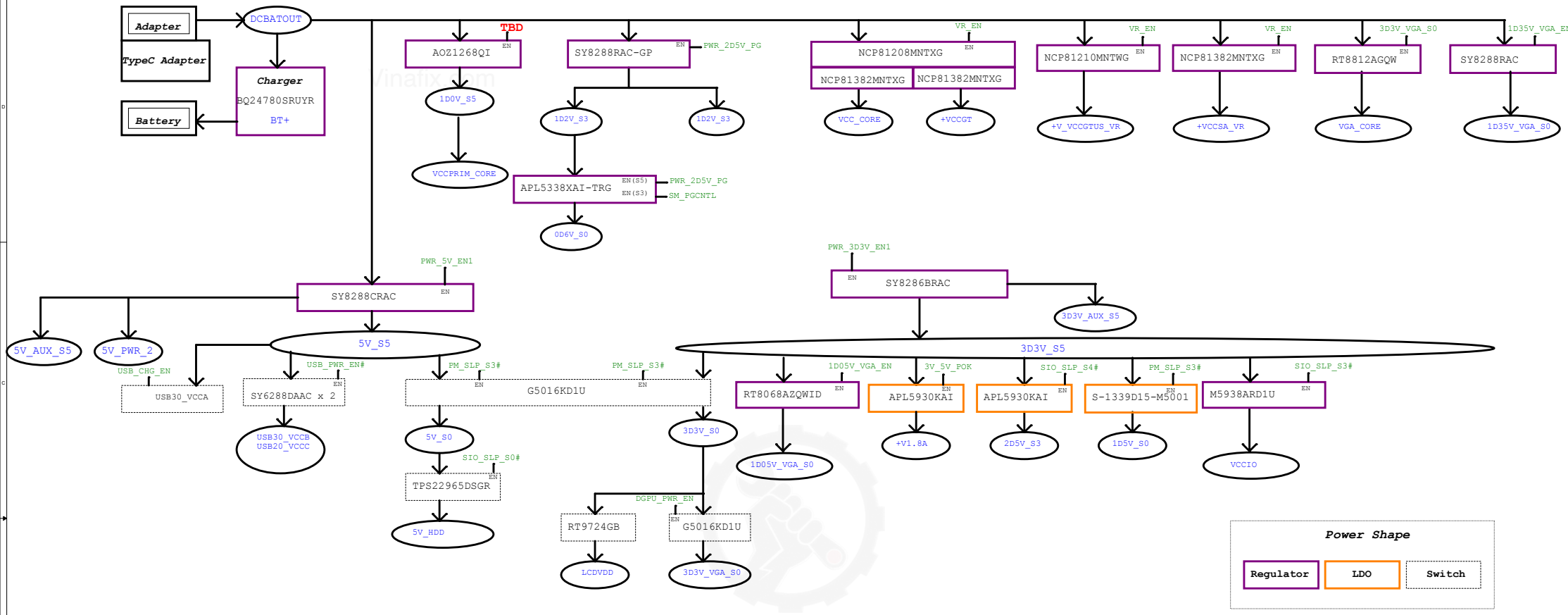


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.



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Title: Power Block Diagram

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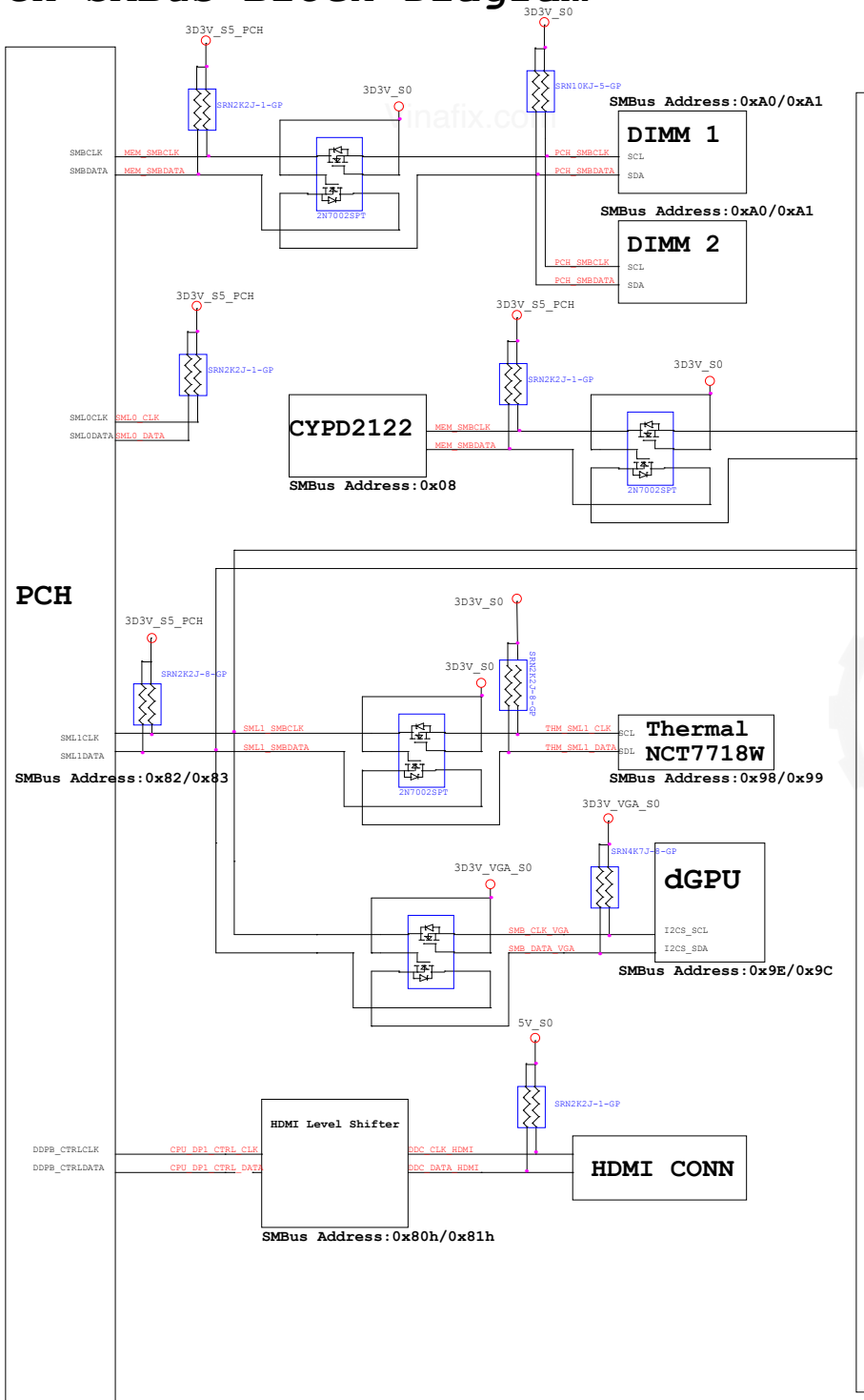
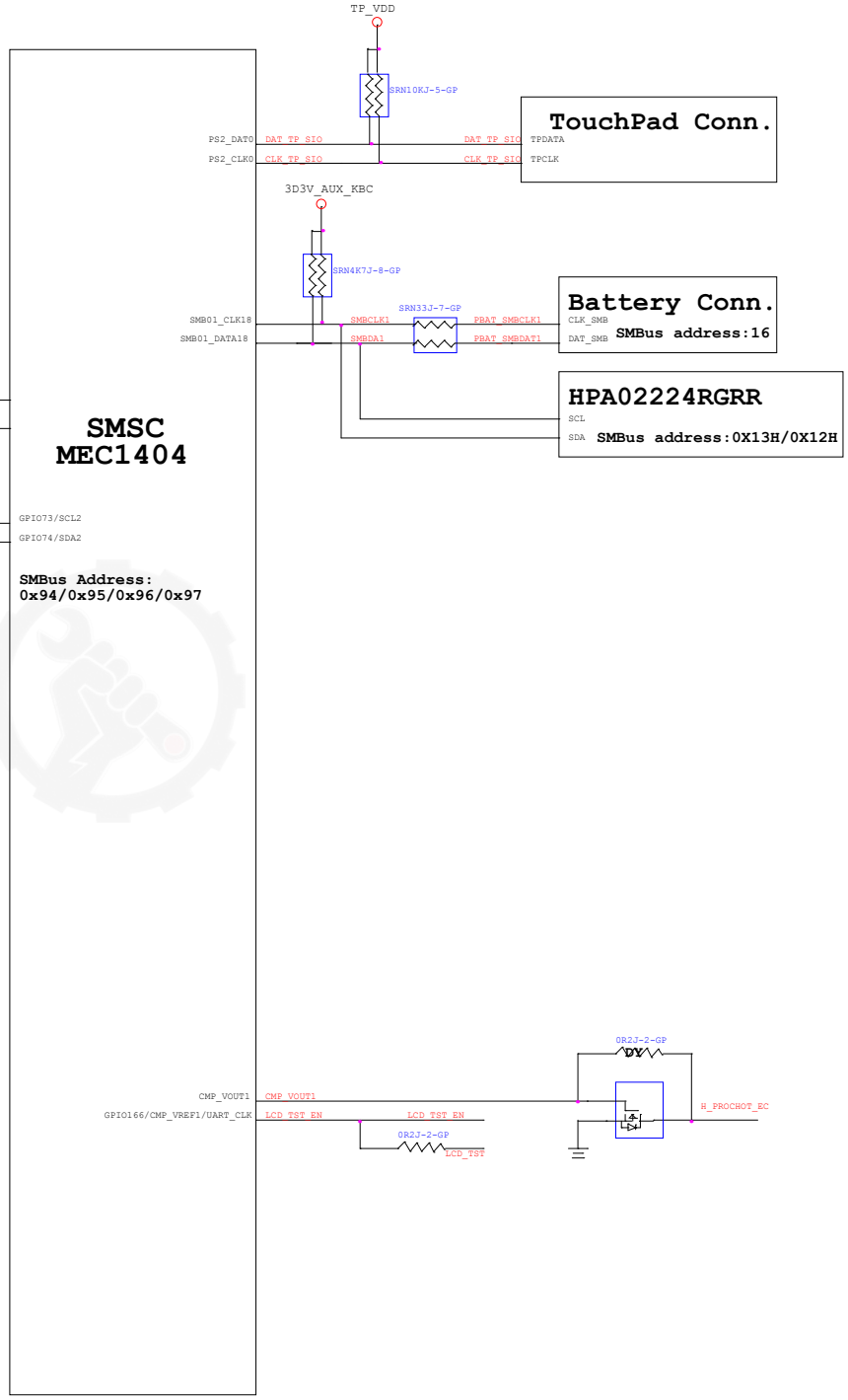
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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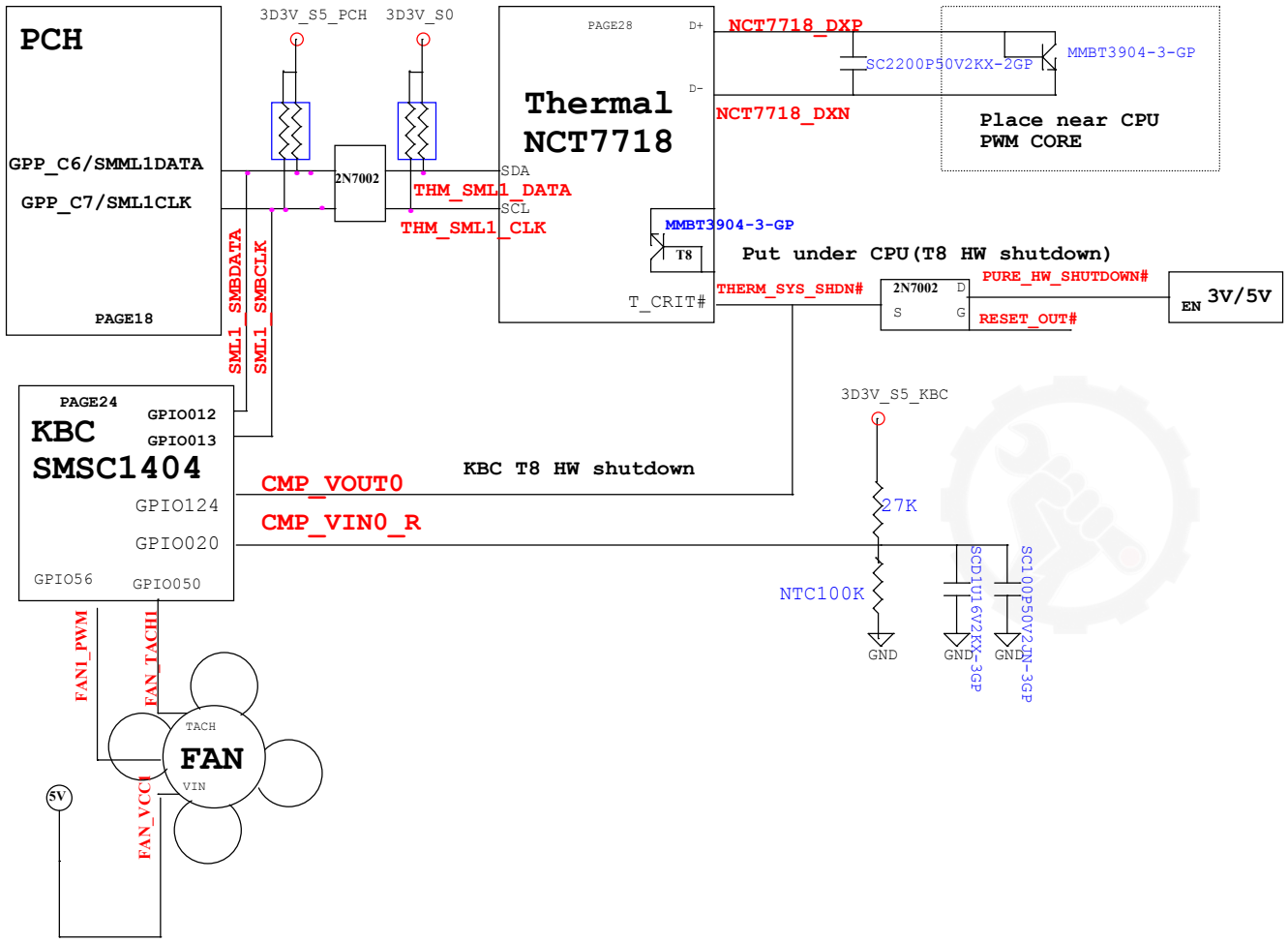
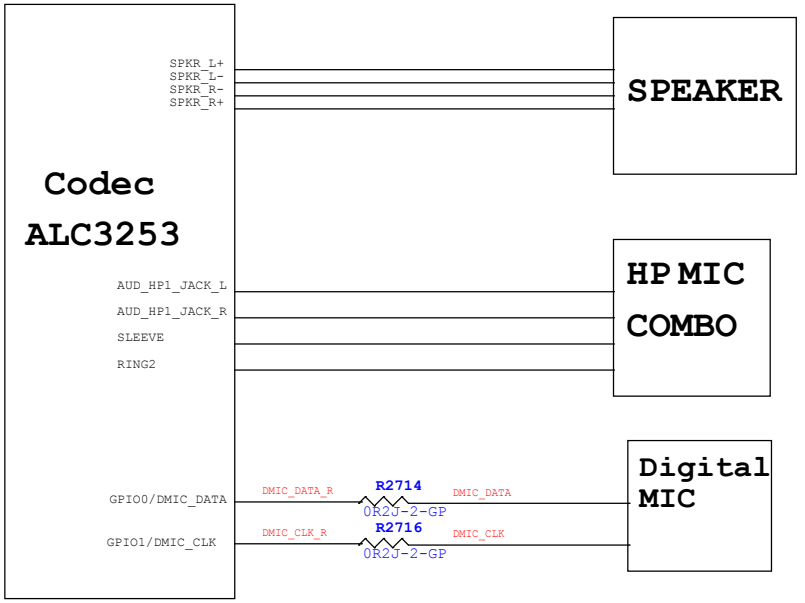
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title

SIP connector

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