Ratchet-1 WHL SVT Logic Schematics

RT1WL-3
VER 3.12
April/1/2019

BASE LOGIC :
Ratchet-1 WHL SIT Logic Schematic Ver 2.18

Lenovo

Project Name : Ratchet-1	Title : TITLE PAGE
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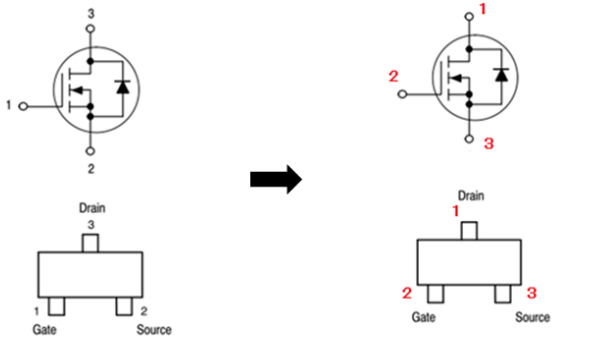
EC HISTORY

RT1IL-3
(Base Logic : Ratchet-1 WHL SIT Logic Schematic Ver. 2.18)

VER.3.00 2019/02/18 APPLIED Ratchet-1 SVT EC001,EC002
VER.3.01 2019/02/19 APPLIED Ratchet-1 SVT EC003
VER.3.02 2019/02/20 APPLIED Ratchet-1 SVT EC004,EC005
VER.3.03 2019/02/21 APPLIED Ratchet-1 SVT EC006,EC007,EC008,EC009,EC010
VER.3.04 2019/02/22 APPLIED Ratchet-1 SVT EC011
VER.3.05 2019/02/25 APPLIED Ratchet-1 SVT EC012,EC013
VER.3.06 2019/02/27 APPLIED Ratchet-1 SVT EC014,EC015
VER.3.07 2019/03/04 APPLIED Ratchet-1 SVT EC016,EC017,EC018
VER.3.08 2019/03/13 APPLIED Ratchet-1 SVT EC019,EC020
VER.3.09 2019/03/14 APPLIED Ratchet-1 SVT EC021
VER.3.10 2019/03/15 APPLIED Ratchet-1 SVT EC022,EC023
VER.3.11 2019/03/20 APPLIED Ratchet-1 SVT EC024
VER.3.12 2019/04/01 APPLIED Ratchet-1 SVT EC025,EC026,EC027

LCFC 3Pin Symbol rule
Orcad Symbol & PCB Footprint pin assignment

Use common rule, Top side is Pin1, not follow original datasheet definition to avoid confusion with different vender definition. Below is an example.



part supplier pin assignment

LCFC common pin assignment

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC -55 to 125degC	+/-30ppm/degC +/-30ppm/degC	NPO C0G
-55 to 125degC -55 to 105degC -55 to 85degC	+/-15% +/-22% +/-15%	X7R X6S X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.1pF +/-0.25pF +/-0.5pF	B C D
+/-5% +/-10% +/-20% +80/-20%	J K M Z

TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

LOGIC

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Project Name : Ratchet-1	Title : EC HISTORY
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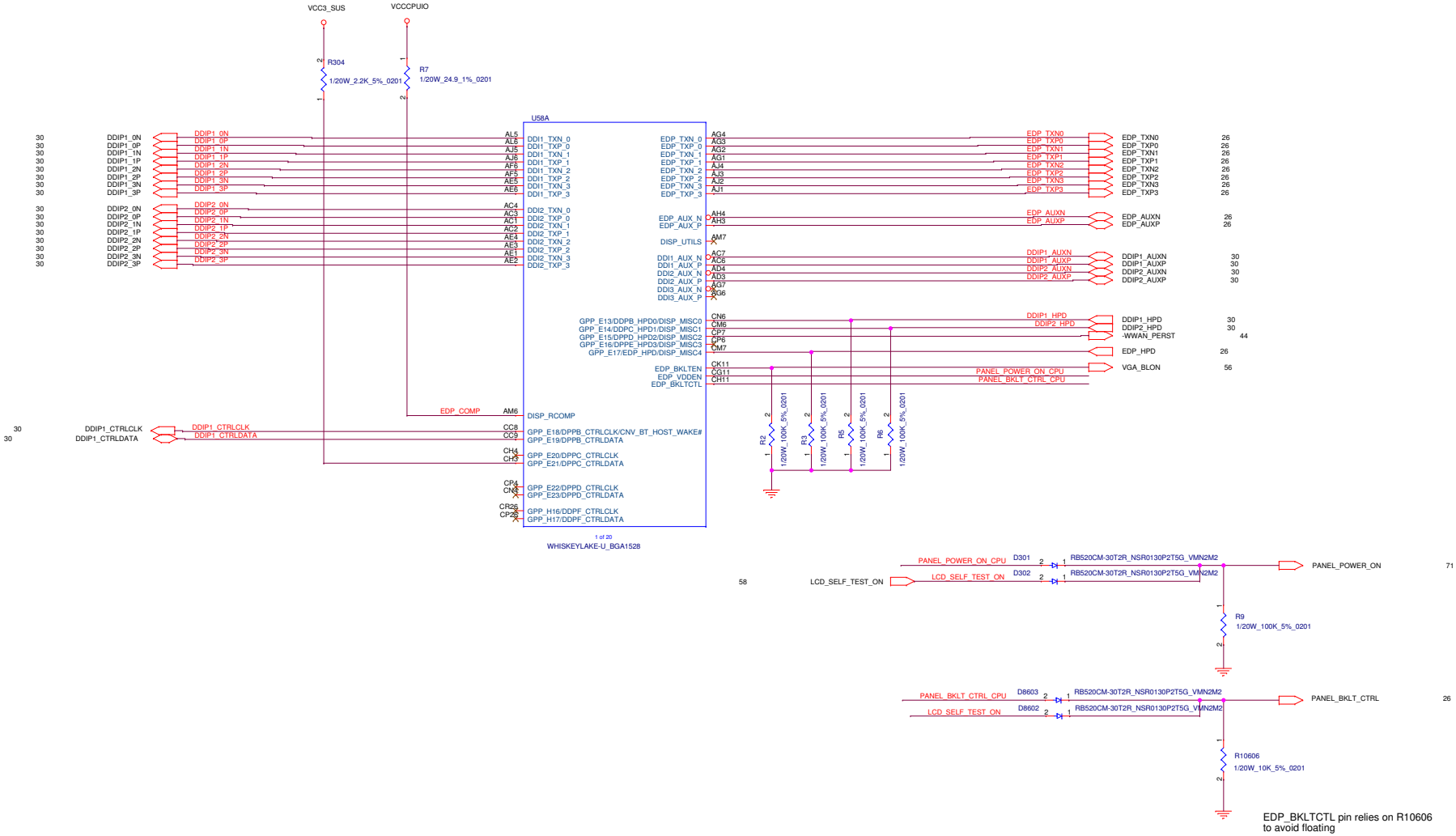
TABLE : Functional Strap

GPP_E19/DDPB_CTRLDATA(DISPLAY PORT B DETECTED)	
GPP_E21/DDPC_CTRLDATA(DISPLAY PORT C DETECTED)	
GPP_E23/DDPD_CTRLDATA(DISPLAY PORT D DETECTED)	
HIGH	**ENABLE**
LOW	**DISABLE**



EDP_BKLTCTL pin relies on R10606 to avoid floating

Project Name : Ratchet-1	Title : CPU(1/16) : DDI/EDP	
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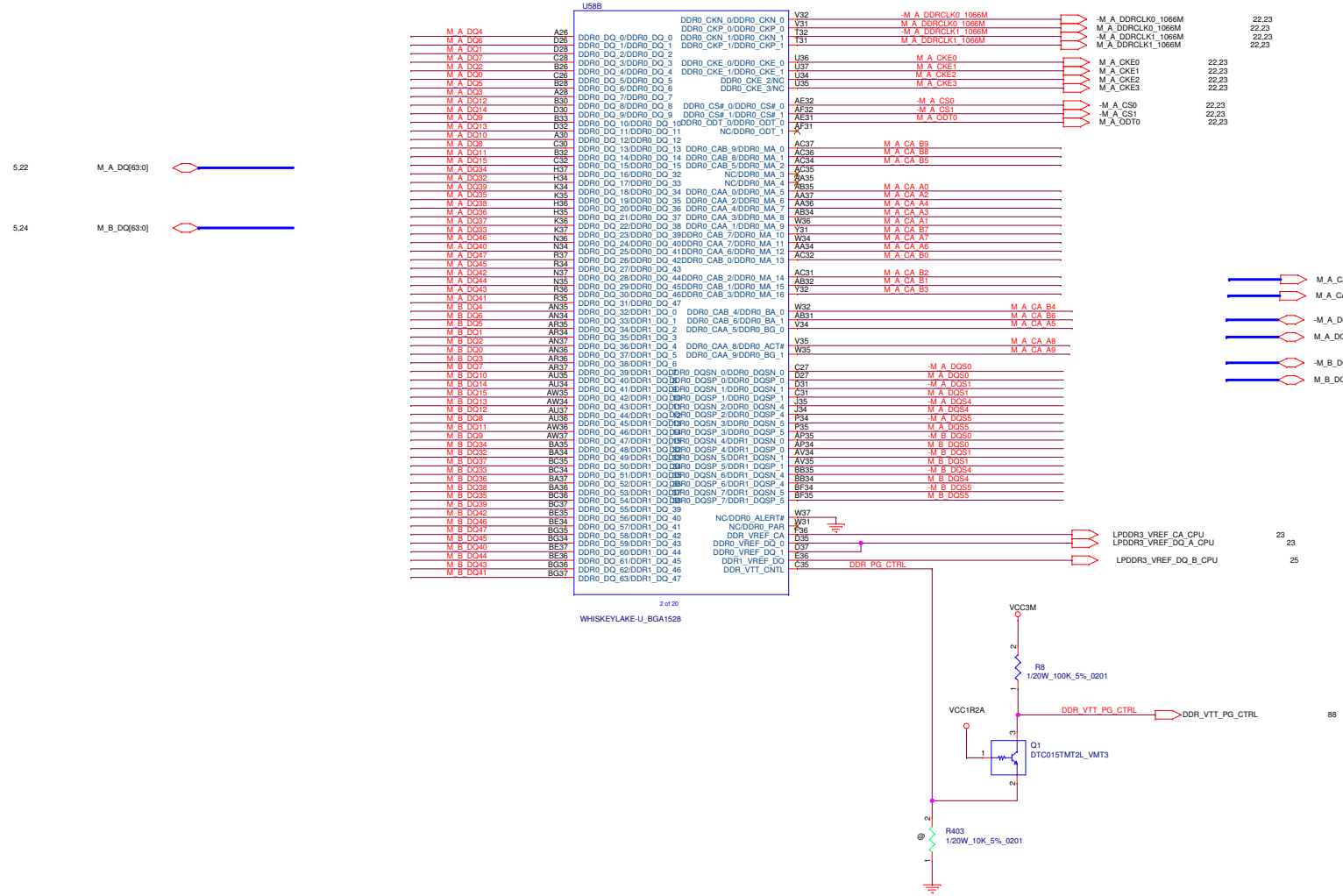

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Project Name : Ratchet-1		Title : CPU(2/16) : DDR (1/2)	
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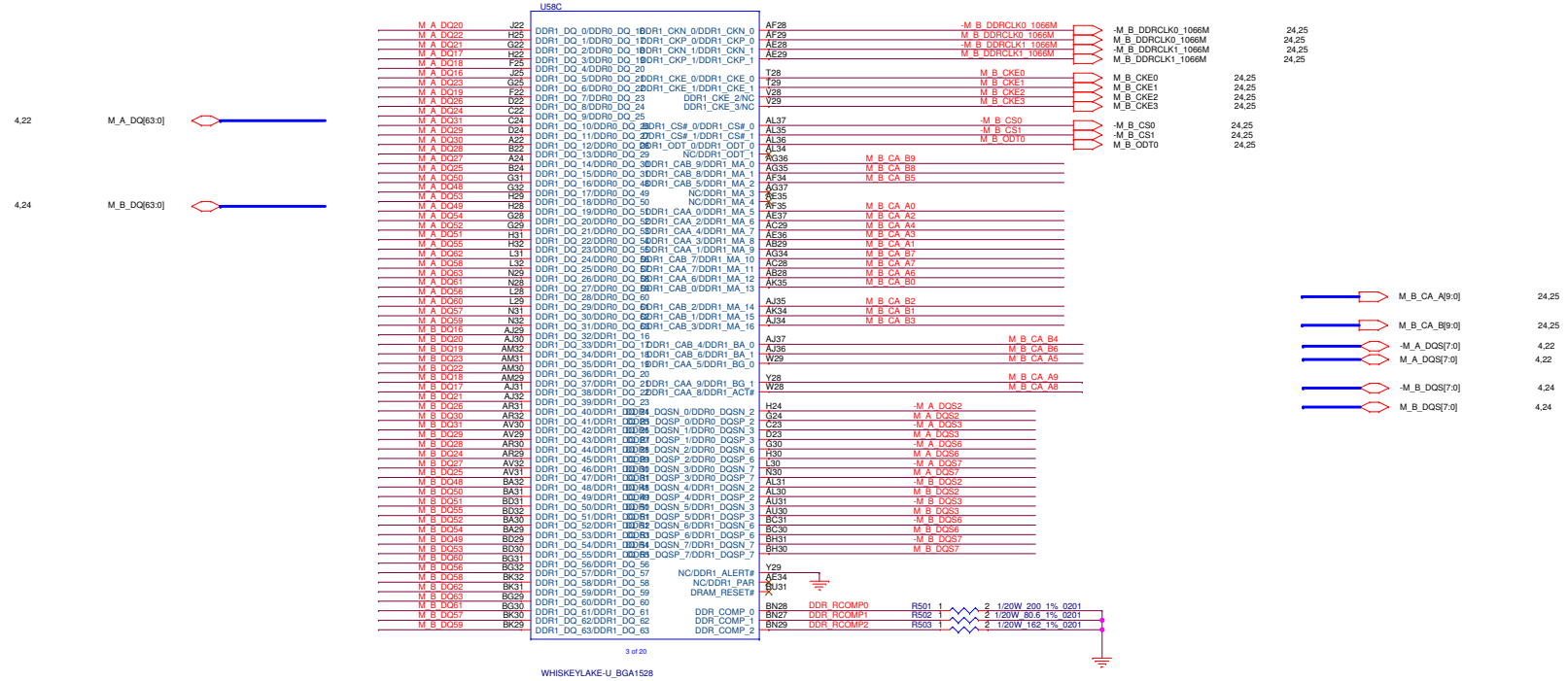

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Project Name : Ratchet-1		Title : CPU(3/16) : DDR (2/2)	
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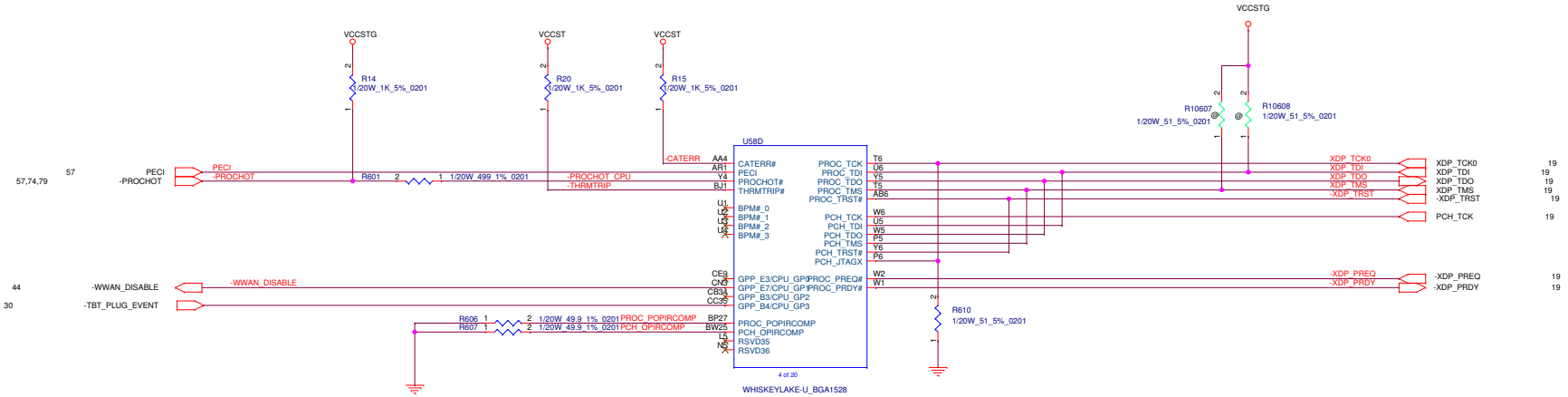

Lenovo			
Project Name : Ratchet-1		Title : CPU(4/16) : MISC/JTAG	
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TABLE : Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Disable (Default)
LOW	Enable

← LOGIC

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT#	
HIGH	Enable Intel(R) DCI-OOB
LOW	Disable Intel(R) DCI-OOB (Default)

← LOGIC

TABLE : Functional Strap

GPP_C2/SMLALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

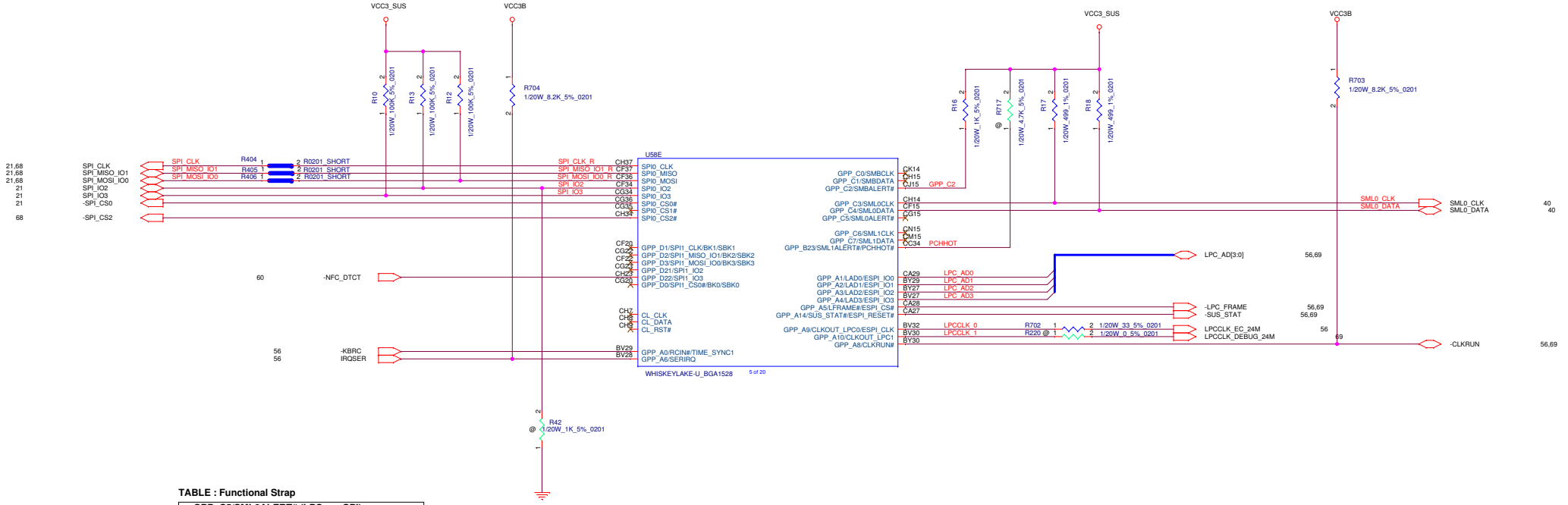

TABLE : Functional Strap

GPP_C5/SML0ALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

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Project Name : Ratchet-1	Title : CPU(5/16) : LPC/SPI/SMBUS/C-LINK
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TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

LOGIC

TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI(Default)

LOGIC

TABLE : Functional Strap

GPP_F6/CNV_RGI_DT(M.2 CNVi Mode Select)	
HIGH	Integrated CNVi Disabled
LOW	Integrated CNVi Enabled

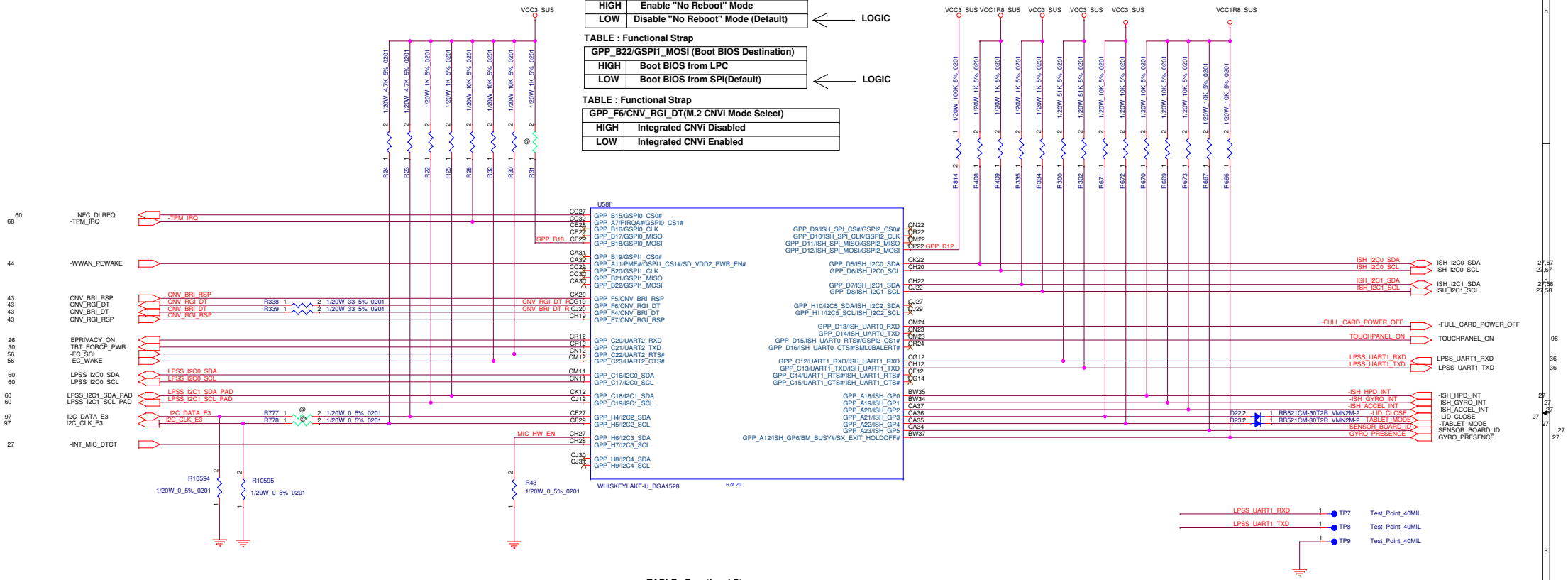

TABLE : Functional Strap

GPP_D12(JTAG ODT Disable)	
HIGH	JTAG ODT Enable (Default)
LOW	JTAG ODT Disable

LOGIC

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Project Name : Ratchet-1		Title : CPU(6/16) : LPSS/ISH	
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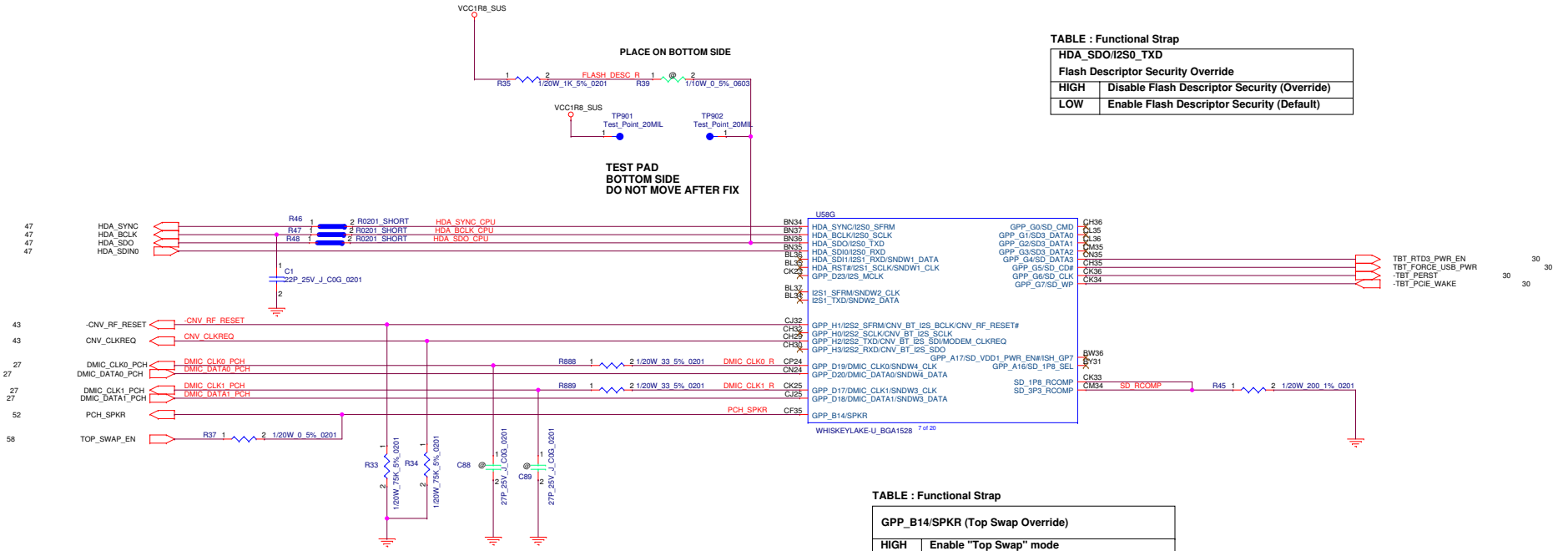

TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

← LOGIC

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Project Name : Ratchet-1	Title : CPU(7/16) : AUDIO/SDXC
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Flexible I/O Configuration

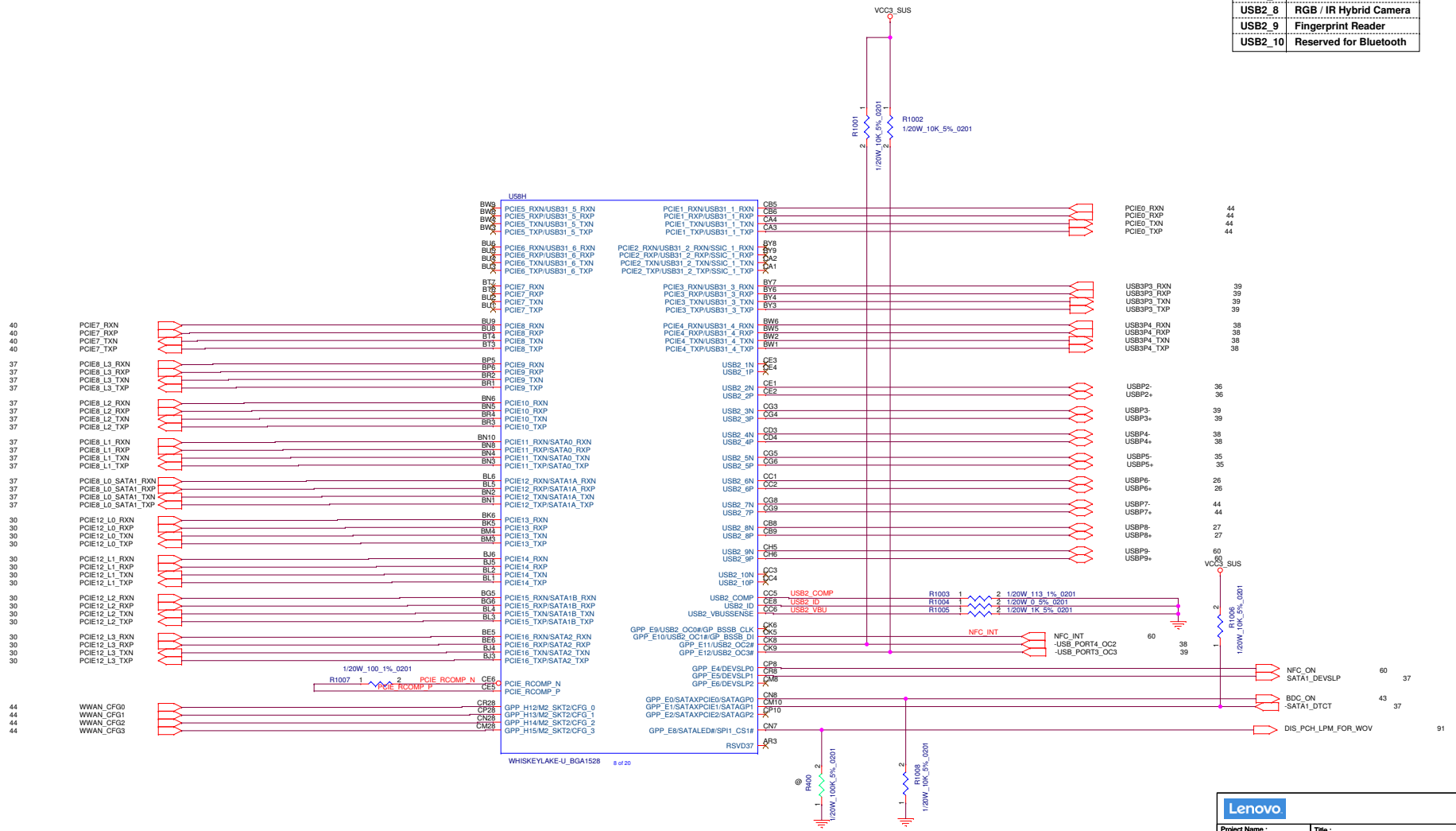
HSIO Port	High Speed Signals	PCI Device	PCI Function	HSIO Configuration	Descriptor for PCIe	Net Name	PCI Device	PCI Function
Port 1	USB3 1 / PCIE 1	1Ch	0h	PCIE 1	4x1 LaneReversal Disabled	PCIE0	1Ch	0h
Port 2	USB3 2 / PCIE 2		1h	PCIE 2		PCIE1		1h
Port 3	USB3 3 / PCIE 3		2h	USB3 3		USB3P3		
Port 4	USB3 4 / PCIE 4		3h	USB3 4		USB3P4		
Port 5	USB3 5 / PCIE 5	1Ch	4h	PCIE 5	4x1 LaneReversal Disabled	N/A		
Port 6	USB3 6 / PCIE 6		5h	PCIE 6		N/A		
Port 7	PCIE 7 (GbE)		6h	PCIE 7		N/A		
Port 8	PCIE 8 (GbE)		7h	PCIE 8 (GbE)		PCIE7	1Fh	6h
Port 9	PCIE 9 (GbE)	1Dh	0h	PCIE 9 (x4)	1x4 LaneReversal Enabled	PCIE8_L3	1Dh	0h
Port 10	PCIE 10		1h	PCIE 10(x4)		PCIE8_L2		
Port 11	PCIE 11 / SATA 0		2h	PCIE 11(x4)		PCIE8_L1		
Port 12	PCIE 12 / SATA 1A		3h	GPIO STRAP		PCIE8_L0_SATA1		
Port 13	PCIE 13 (GbE)	1Dh	4h	PCIE 13(x4)	1x4 LaneReversal Disabled	PCIE12_L0	1Dh	4h
Port 14	PCIE 14 (GbE)		5h	PCIE 14(x4)		PCIE12_L1		
Port 15	PCIE 15 / SATA 1B		6h	PCIE 15(x4)		PCIE12_L2		
Port 16	PCIE 16 / SATA 2		7h	PCIE 16(x4)		PCIE12_L3		

PCIe Port Assignment	
PCIE 1	WWAN
PCIE 2	N/A
PCIE 3	(USB3_3)
PCIE 4	(USB3_4)
PCIE 5	N/A
PCIE 6	N/A
PCIE 7	N/A
PCIE 8	GBE
PCIE 9 (x4)	NVMe SSD
PCIE 13 (x4)	Alpine Ridge-DP

SATA Port Assignment	
SATA 0	(PCIE11)
SATA 1A	SATA SSD
SATA 1B	(PCIE15)
SATA 2	(PCIE16)

USB 3.1 Port Assignment	
USB3_1	(PCIE1)
USB3_2	(PCIE2)
USB3_3	Type-A Port (AOU)
USB3_4	Type-A Port (DCI)
USB3_5	(PCIE5)
USB3_6	(PCIE6)

USB 2.0 Port Assignment	
USB2_1	(Reserved)
USB2_2	Type-C Port A
USB2_3	Type-A Port (AOU)
USB2_4	Type-A Port (DCI)
USB2_5	Type-C Port B (DOCK)
USB2_6	Touch Panel
USB2_7	WWAN Card
USB2_8	RGB / IR Hybrid Camera
USB2_9	Fingerprint Reader
USB2_10	Reserved for Bluetooth



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Project Name : Ratchet-1	Title : CPU(8/16) : PCIE/USB/SATA
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TABLE : Functional Strap

GPP_H23(eSPI Flash Sharing Mode)	
HIGH	Enable SAFS
LOW	Enable MAFS(Default)

← LOGIC

TABLE : Functional Strap

GPP_H21 (XTAL Frequency Select)	
HIGH	24MHz XTAL selected
LOW	38.4MHz XTAL frequency selected (Default)

← LOGIC

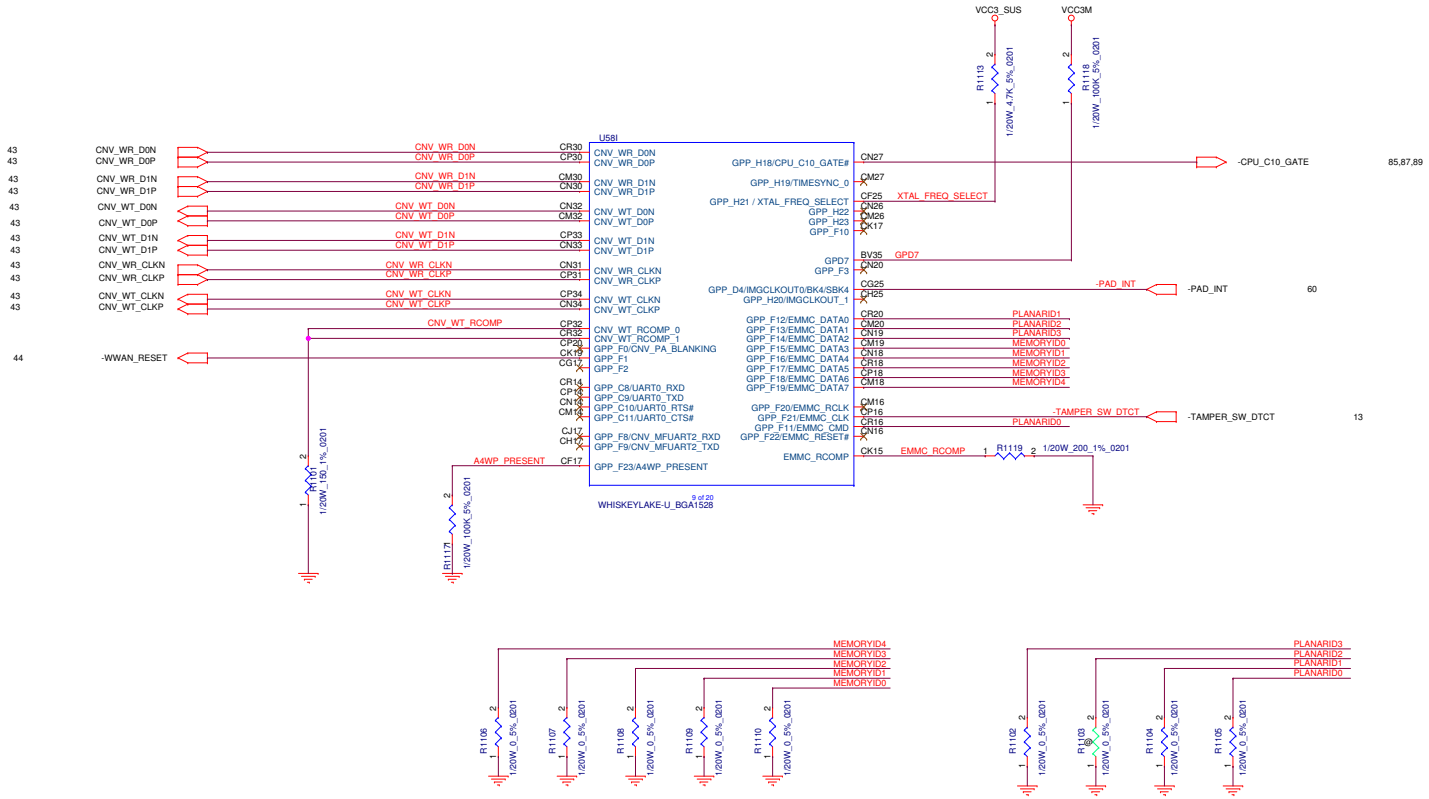

TABLE:

MEMORYID[4:0]	U170,U171,U172,U173			Capacity
00h (00000b)	Samsung	K4E6E304EC-EGCG	16Gbit DDP	8GB
01h (00001b)		K4EBE304EC-EGCG	32Gbit QDP	16GB
02h (00010b)	SK hynix	H9CCNNNBJTALAR-NVD	16Gbit DDP	8GB
03h (00011b)		H9CCNNNCLGALAR-NVD	32Gbit QDP	16GB
04h (00100b)	Samsung	K4E6E304EB-EGCG	16Gbit DDP	8GB
05h (00101b)		K4EBE304EB-EGCG	32Gbit QDP	16GB
06h (00110b)		K4E6E304ED-EGCG	16Gbit DDP	8GB
07h (00111b)		K4EBE304ED-EGCG	32Gbit QDP	16GB
08h (01000b)	Nanya	NT6CL512T32AM-H0	16Gbit DDP	8GB

TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R1102	R1103	R1104	R1105
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3:0]
EVT	0000B
FVT	0001B
ME SIT	0010B
SIT	0011B
SVT	0100B

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Project Name : Ratchet-1	Title : CPU(9/16) : CSI-2/EMMC/CNVI
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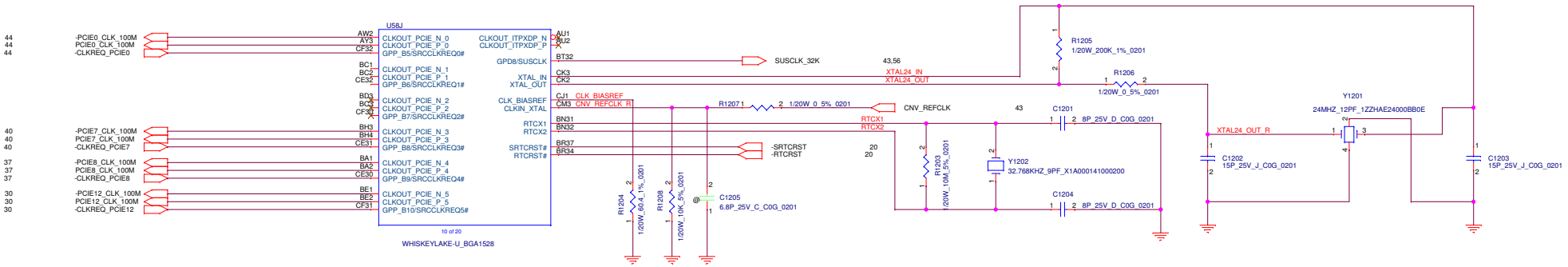

TABLE of Y1202		
Vendor	P/N	LCFC P/N
EPSON	X1A000141000200	SJ10000IX00
TXC	9H03280012	SJ10000J900
KDS	1TJF090DJ1A000B	SJ100069400

TABLE of Y1201		
Vendor	P/N	LCFC P/N
KDS	1ZZHAE24000BB0E	SJ10000TG00
TXC	8Y24080004	SJ10000TN00

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Project Name : Ratchet-1	Title : CPU(10/16) : CLOCK SIGNALS
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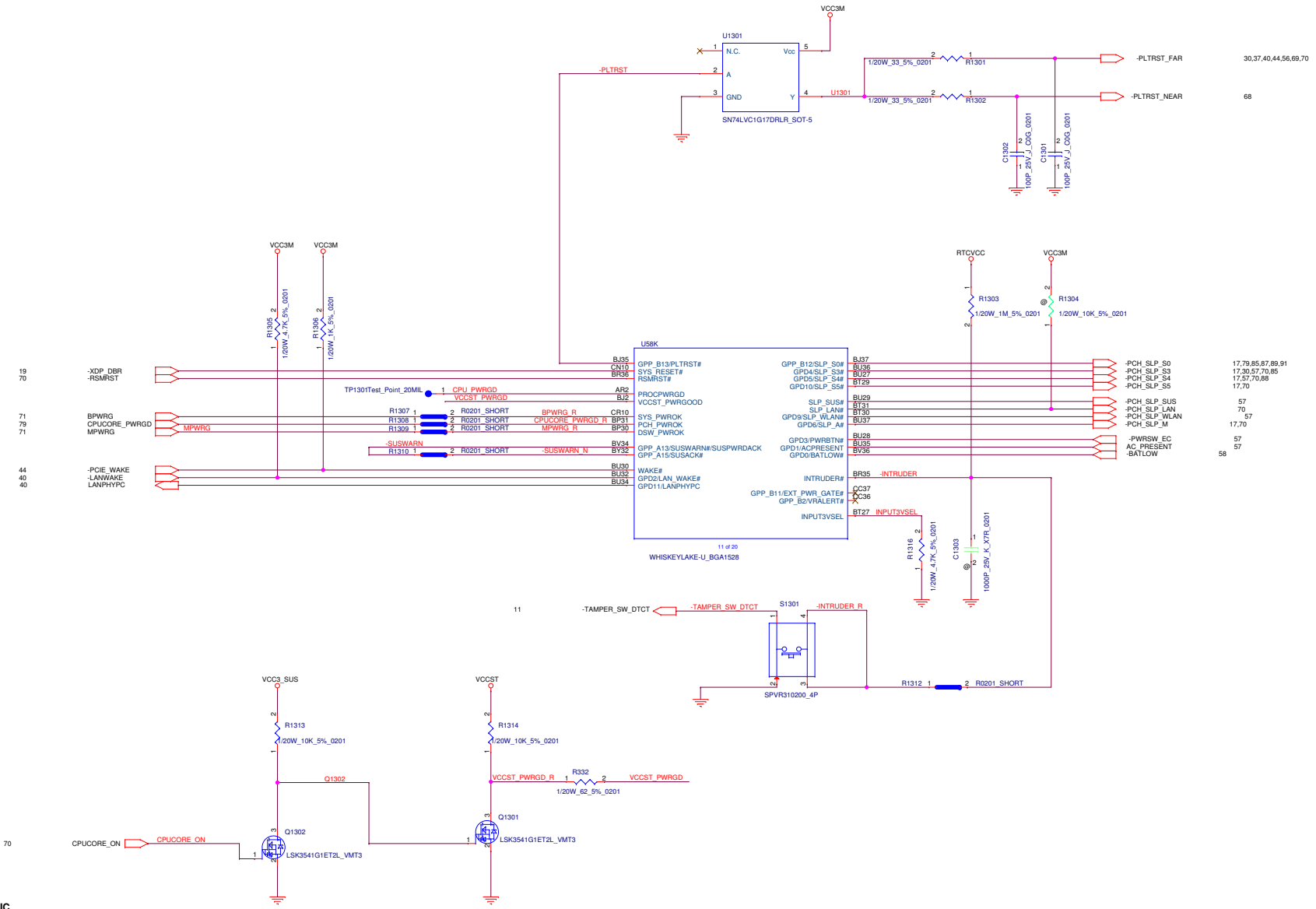

TABLE : Functional Strap

INPUT3VSEL (3.0V Select)	
HIGH	3.3V supply is 3.0V +/- 5%
LOW	3.3V supply is 3.3V +/- 5%

← LOGIC

Project Name : Ratchet-1	Title : CPU(11/16) : SYSTEM PM
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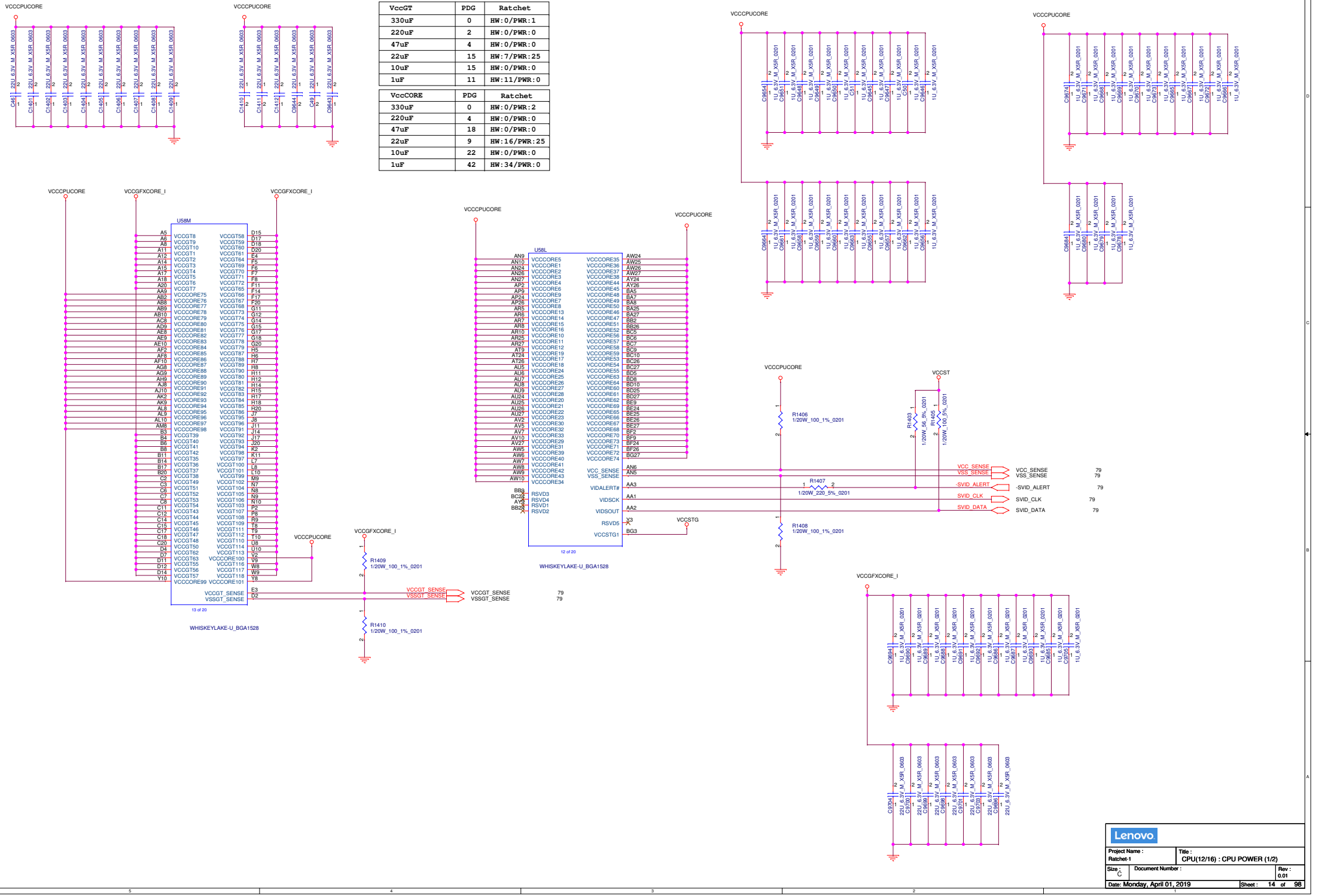
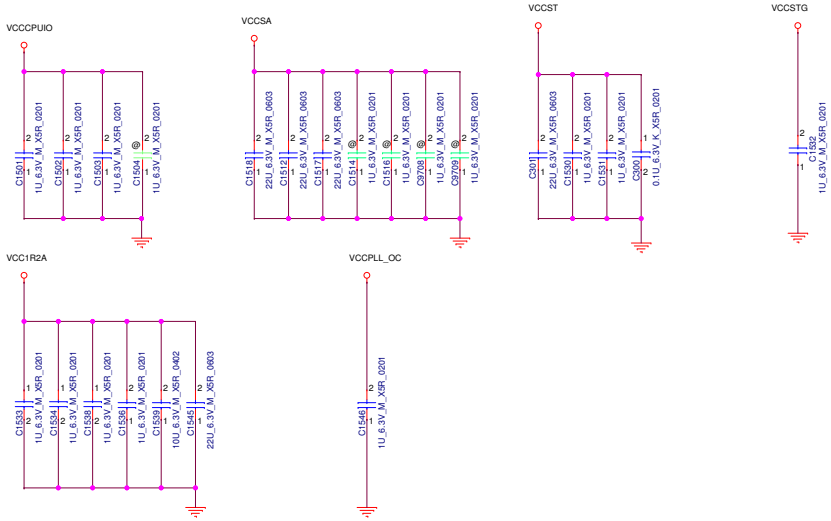
VccGT	PDG	Ratchet
330uF	0	HW:0/PWR:1
220uF	2	HW:0/PWR:0
47uF	4	HW:0/PWR:0
22uF	15	HW:7/PWR:25
10uF	15	HW:0/PWR:0
1uF	11	HW:11/PWR:0

VccCORE	PDG	Ratchet
330uF	0	HW:0/PWR:2
220uF	4	HW:0/PWR:0
47uF	18	HW:0/PWR:0
22uF	9	HW:16/PWR:25
10uF	22	HW:0/PWR:0
1uF	42	HW:34/PWR:0





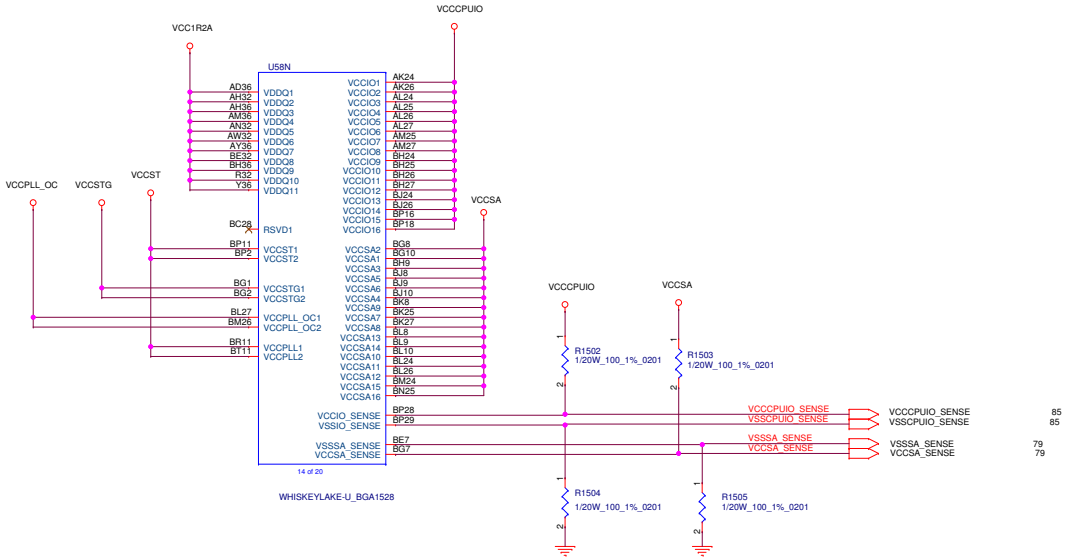
VccSA	PDG	Ratchet
47uF	2	HW:0/PWR:0
22uF	0	HW:3/PWR:6
10uF	13	HW:0/PWR:0
1uF	0	HW:0/PWR:0

VDDQ	PDG	Ratchet
47uF	0	HW:0/PWR:0
22uF	1	HW:1/PWR:5
10uF	9	HW:1/PWR:0/MEM:12
1uF	4	HW:4/PWR:0/MEM:36
0.1uF	0	HW:0/PWR:1
0.01uF	0	HW:0/PWR:1
2200pF	0	HW:0/PWR:1

VccIO	PDG	Ratchet
47uF	0	HW:0/PWR:0
22uF	0	HW:0/PWR:4
10uF	6	HW:0/PWR:0
1uF	4	HW:3/PWR:0
0.1uF	0	HW:0/PWR:1

VccPLL/VCCST	PDG	Ratchet
22uF	0	HW:1/PWR:0
1uF	1	HW:2/PWR:0
0.1uF	1	HW:1/PWR:1

VccPLL_OC	PDG	Ratchet
1uF	1	HW:1/PWR:0



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Project Name : Ratchet-1	Title : CPU(13/16) : CPU POWER (2/2)
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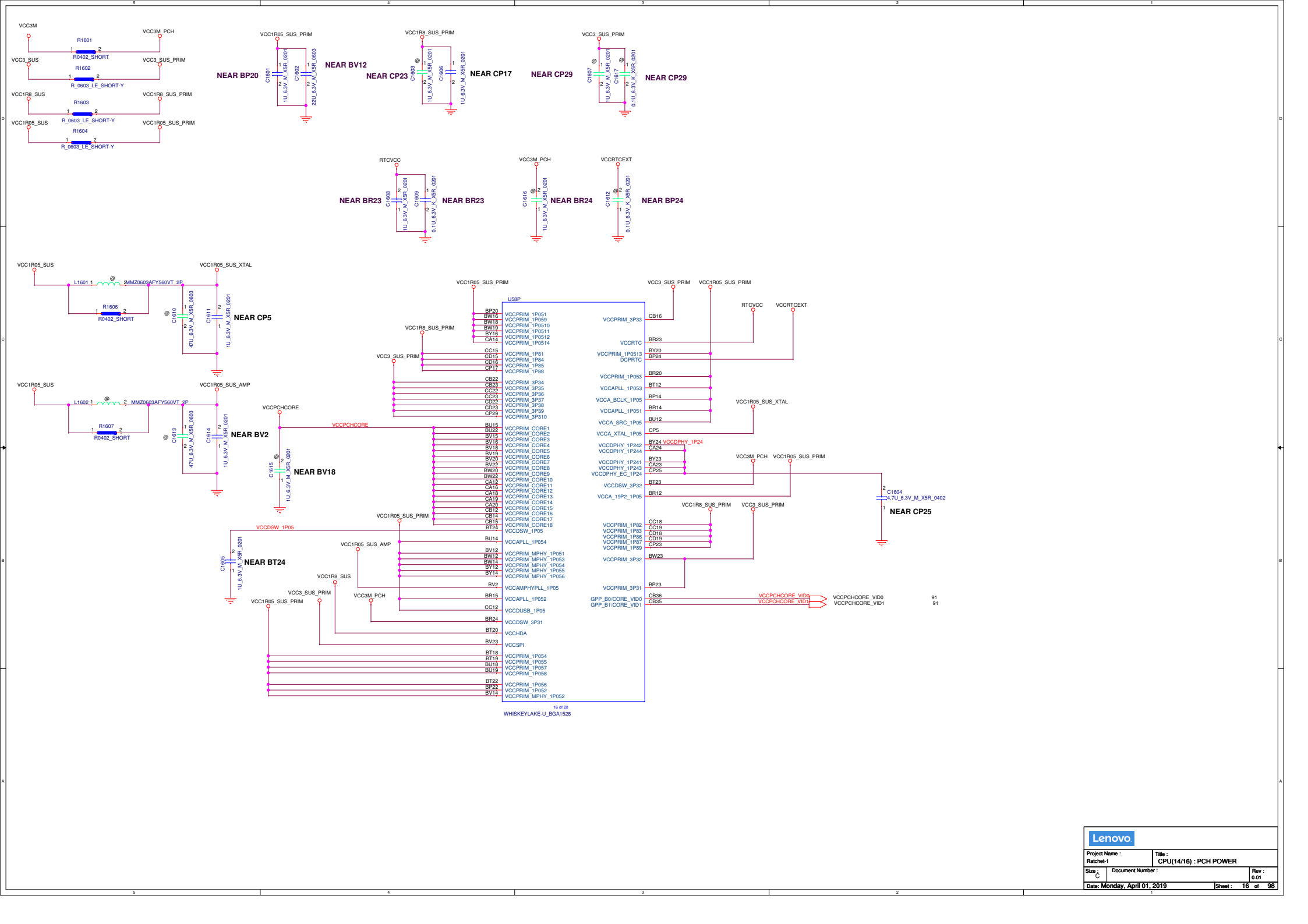

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Project Name : Ratchet-1	Title : CPU(14/16) : PCH POWER
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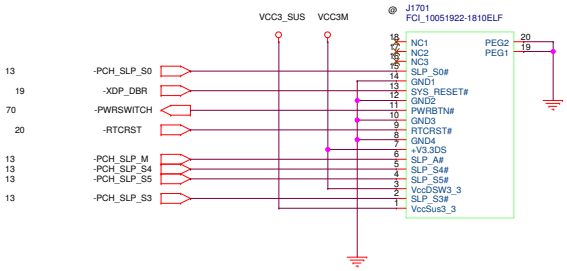
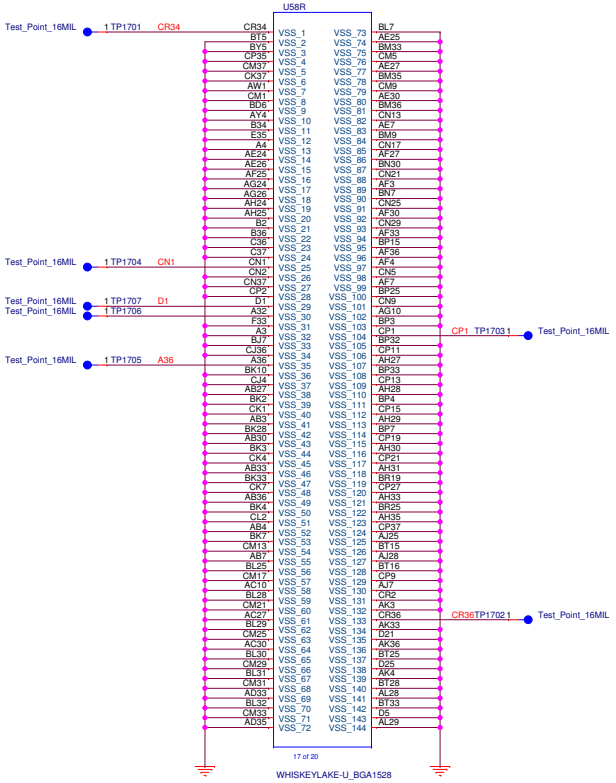
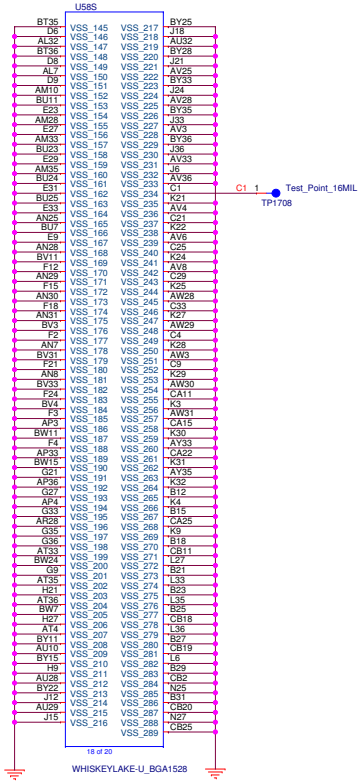
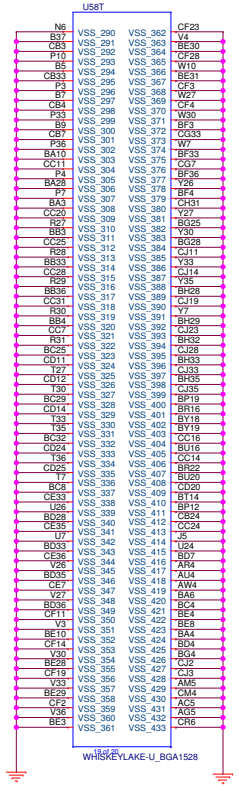
APS/PETS Interface









Project Name : Ratchet-1	Title : CPU(15/16) : GND
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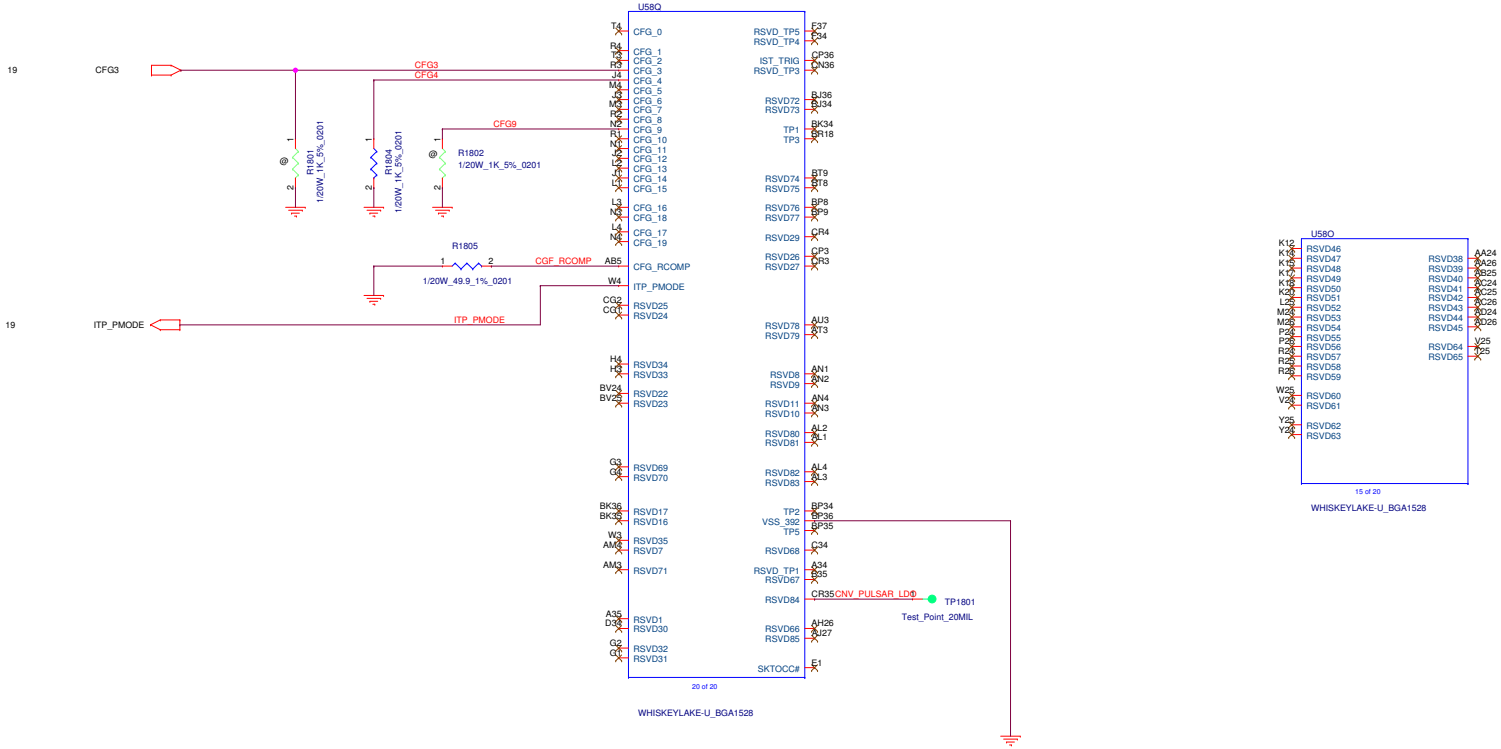
TABLE

CFG0: Stall Reset Sequence after PCU PLL Lock untill de-asserted **1:No Stall** **0: Stall**
CFG3: MSR Privacy Bit Feature **1: MSR (C80h) bit[0] setting** **0: MSR (C80h) bit[0] overridden**
CFG4: eDP Enable **1:Disabled** **0:Enabled**
CFG9: SVID Bus Communication **1:Enabled** **0:Disabled**



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Project Name : Ratchet-1	Title : CPU(16/16) : CFG/RESERVED
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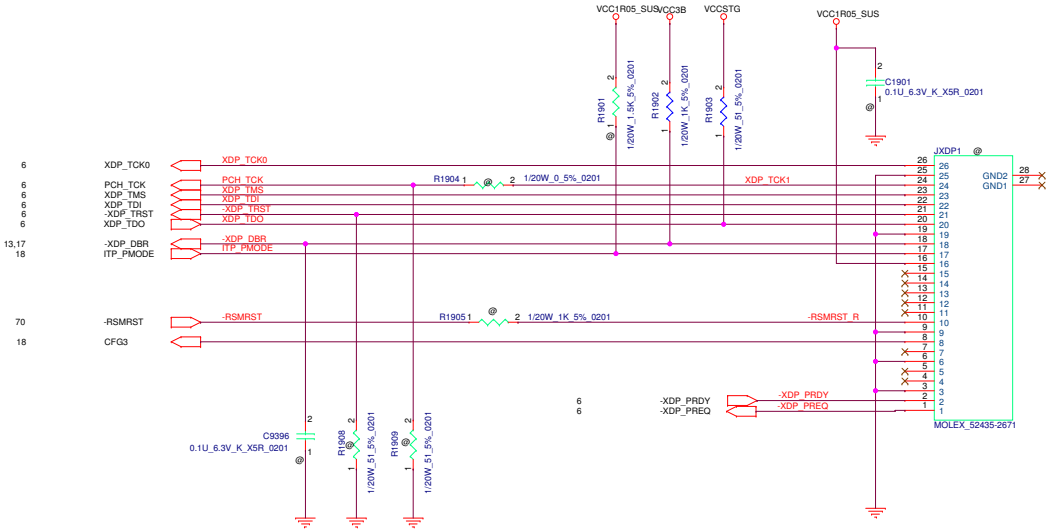

TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 6	R10607	ASM	NO_ASM
	R10608	ASM	NO_ASM
Page 7	R42	ASM	NO_ASM
Page 18	R1801	ASM	NO_ASM
Page 19	JXDP1	ASM	NO_ASM
	C1901	ASM	NO_ASM
	R1903	ASM	ASM
	R1902	ASM	ASM
	R1901	ASM	NO_ASM
	R1905	ASM	NO_ASM
	R1904	ASM	NO_ASM

LOGIC

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Project Name : Ratchet-1	Title : XDP CONNECTOR
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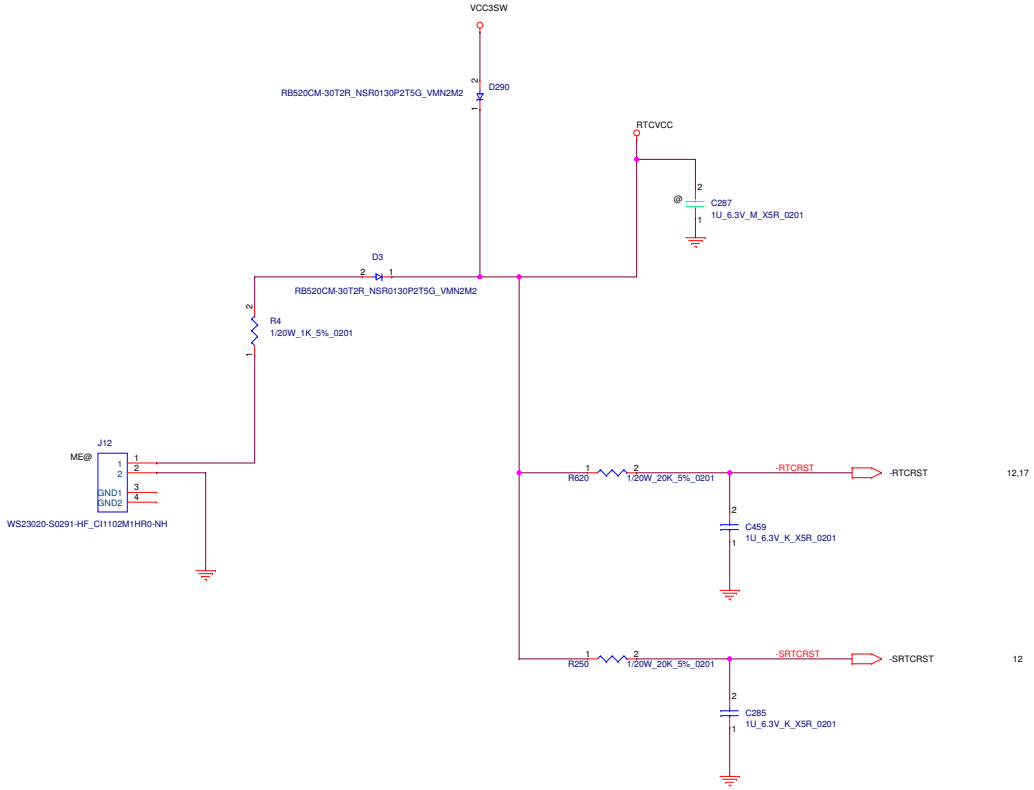
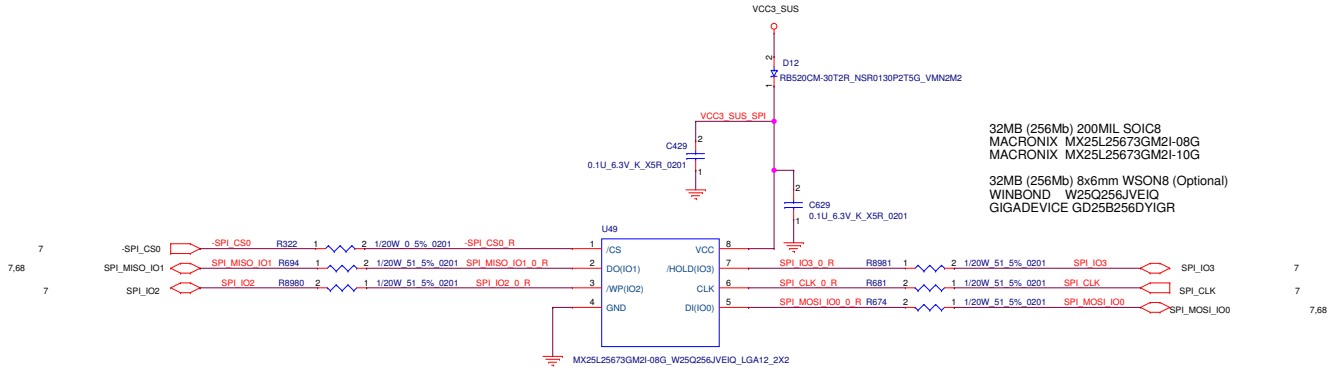


Project Name : Ratchet-1	Title : RTC BATTERY	
Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 20 of 98	



32MB (256Mb) 200MIL SOIC8
MACRONIX MX25L25673GM2I-08G
MACRONIX MX25L25673GM2I-10G

32MB (256Mb) 8x6mm WSON8 (Optional)
WINBOND W25Q256JVEIQ
GIGADEVICE GD25B256DYIGR

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	D12.1	GND	GND	2
3	CS#	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

Project Name : Ratchet-1		Title : SPI FLASH	
Size : C	Document Number :		Rev : 0.01
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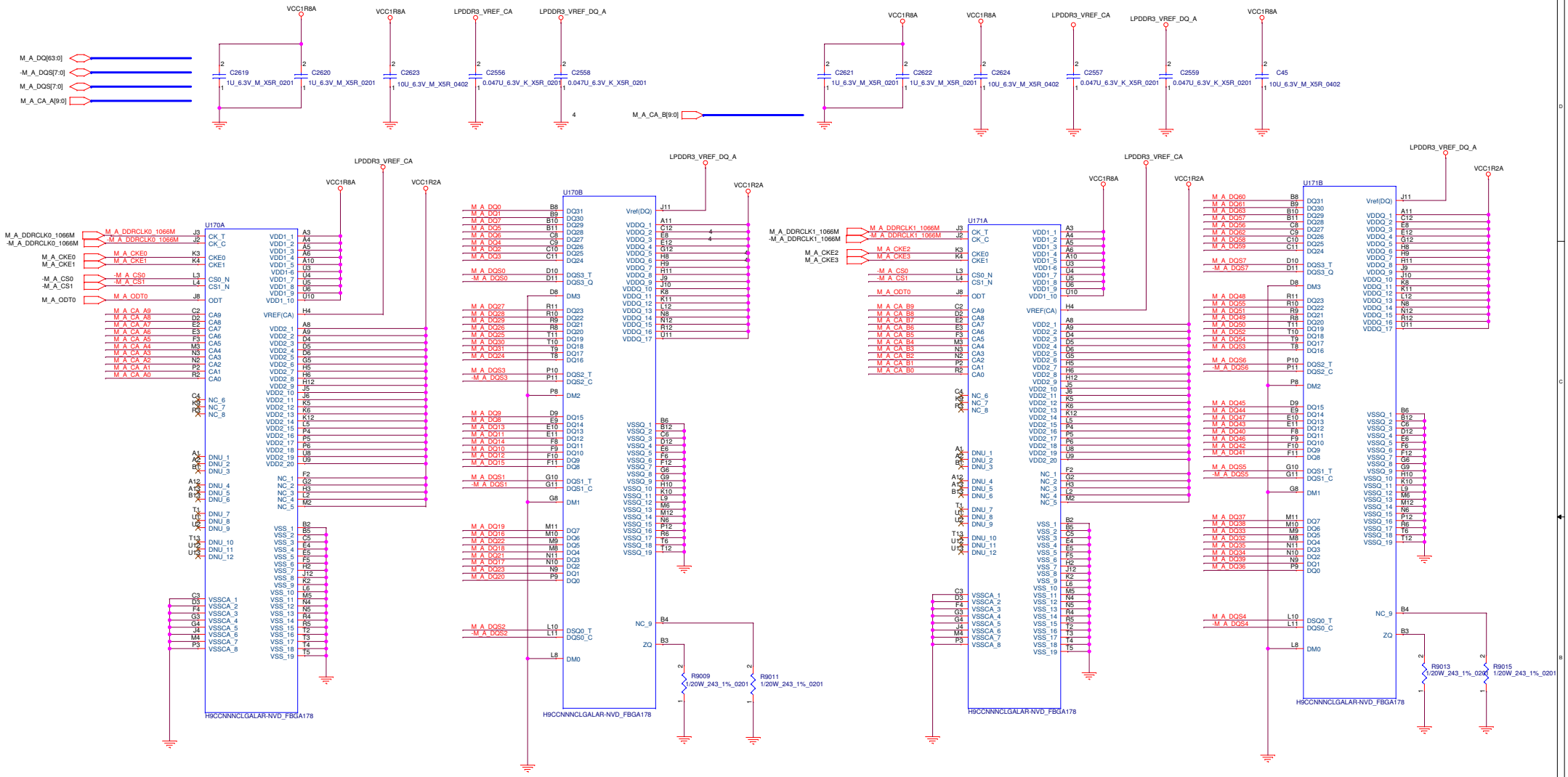

TABLE: LPDDR3 SDRAM Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Configuration	ZQ0/ZQ	ZQ1/NC	Dual Ch
Samsung	16Gb	K4E6E304EB-EGCG	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
		K4E6E304ED-EGCG	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
	32Gb	K4EBE304EB-EGCG	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
		K4EBE304ED-EGCG	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
SK hynix	16Gb	H9CCNNNBJTALAR-NVD	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
	32Gb	H9CCNNNCLGALAR-NVD	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
Nanya	16Gb	NT6CL512T32AM-H0	10.5 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB

Lenovo

Project Name : Ratchet-1	Title : LPDDR3 BASE MEMORY CH-A (1/2)
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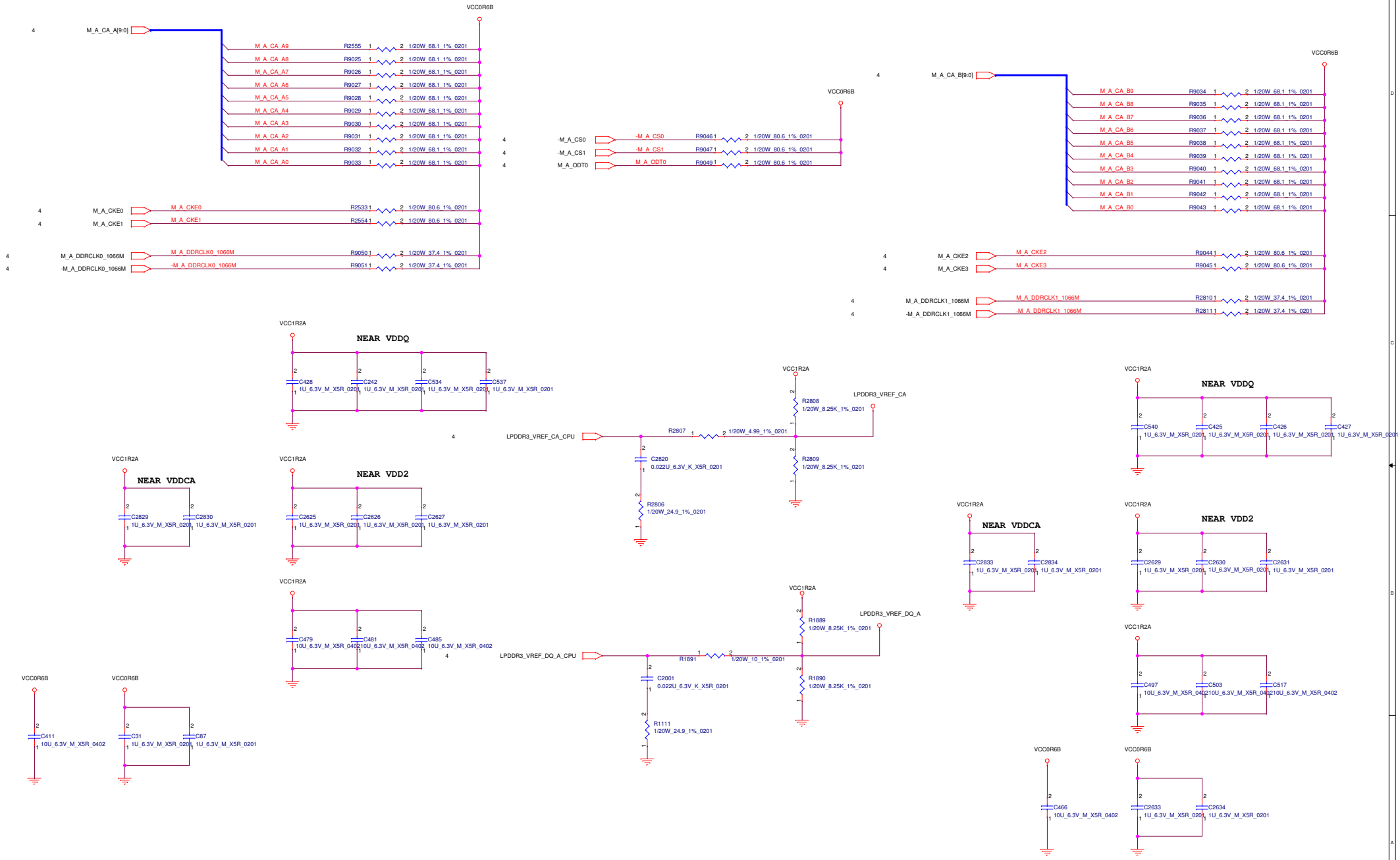

Lenovo		
Project Name : Ratchet-1	Title : LPDDR3 BASE MEMORY CH-A (2/2)	
Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 23 of 98	

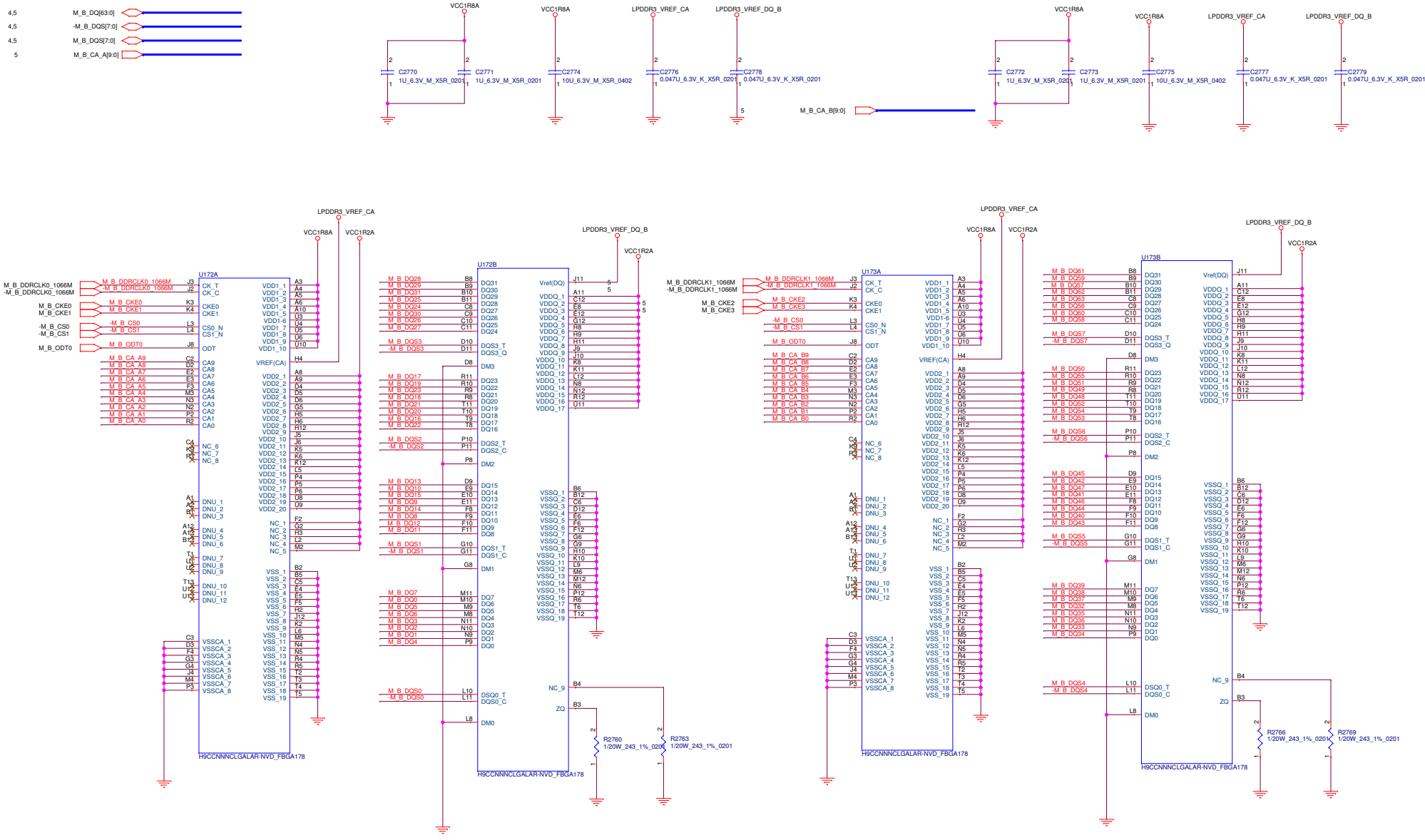

TABLE: LPDDR3 SDRAM Source

Supplier	Capacity	Supplier's P/N	Package Size		Die	Configuration	ZQ0/ZQ	ZQ1/NC	Dual Ch
Samsung	16Gb	K4E6E304EB-EGCG	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
		K4E6E304ED-EGCG	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
	32Gb	K4EBE304EB-EGCG	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
		K4EBE304ED-EGCG	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
SK hynix	16Gb	H9CCNNNBJTALAR-NVD	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
	32Gb	H9CCNNNCLGALAR-NVD	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
Nanya	16Gb	NT6CL512T32AM-H0	10.5 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB

Lenovo

Project Name : Ratchet-1	Title : LPDDR3 BASE MEMORY CH-B (1/2)
Size : C	Document Number :
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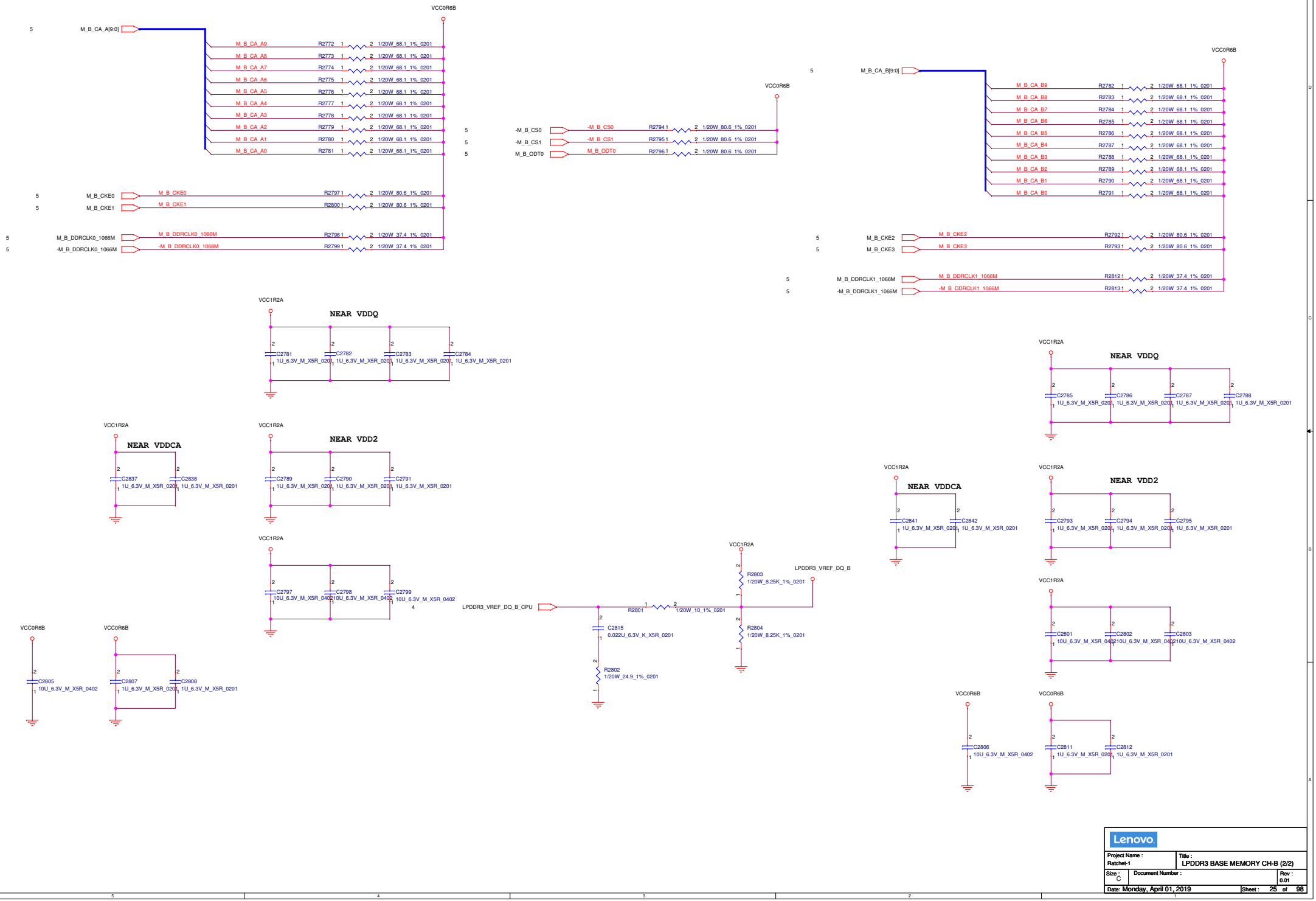
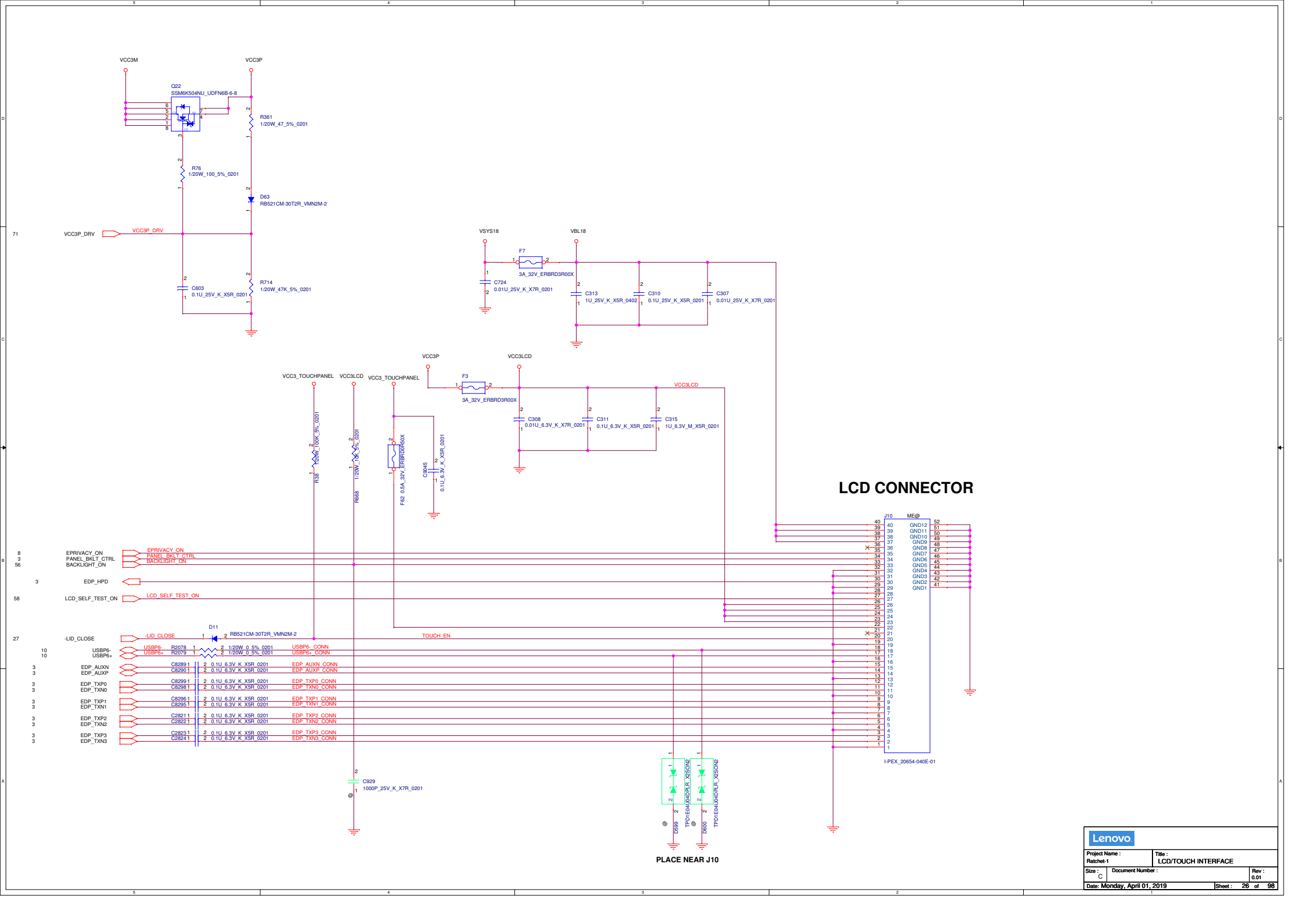


Lenovo

Project Name : Ratchet-1	Title : LPDDR3 BASE MEMORY CH-B (2/2)
Size : C	Document Number :
Date: Monday, April 01, 2019	Sheet : 25 of 98



Project Name : Ratchet-1	Title : LCD/TOUCH INTERFACE
Size : C	Document Number :
Date: Monday, April 01, 2019	Rev : 0.01
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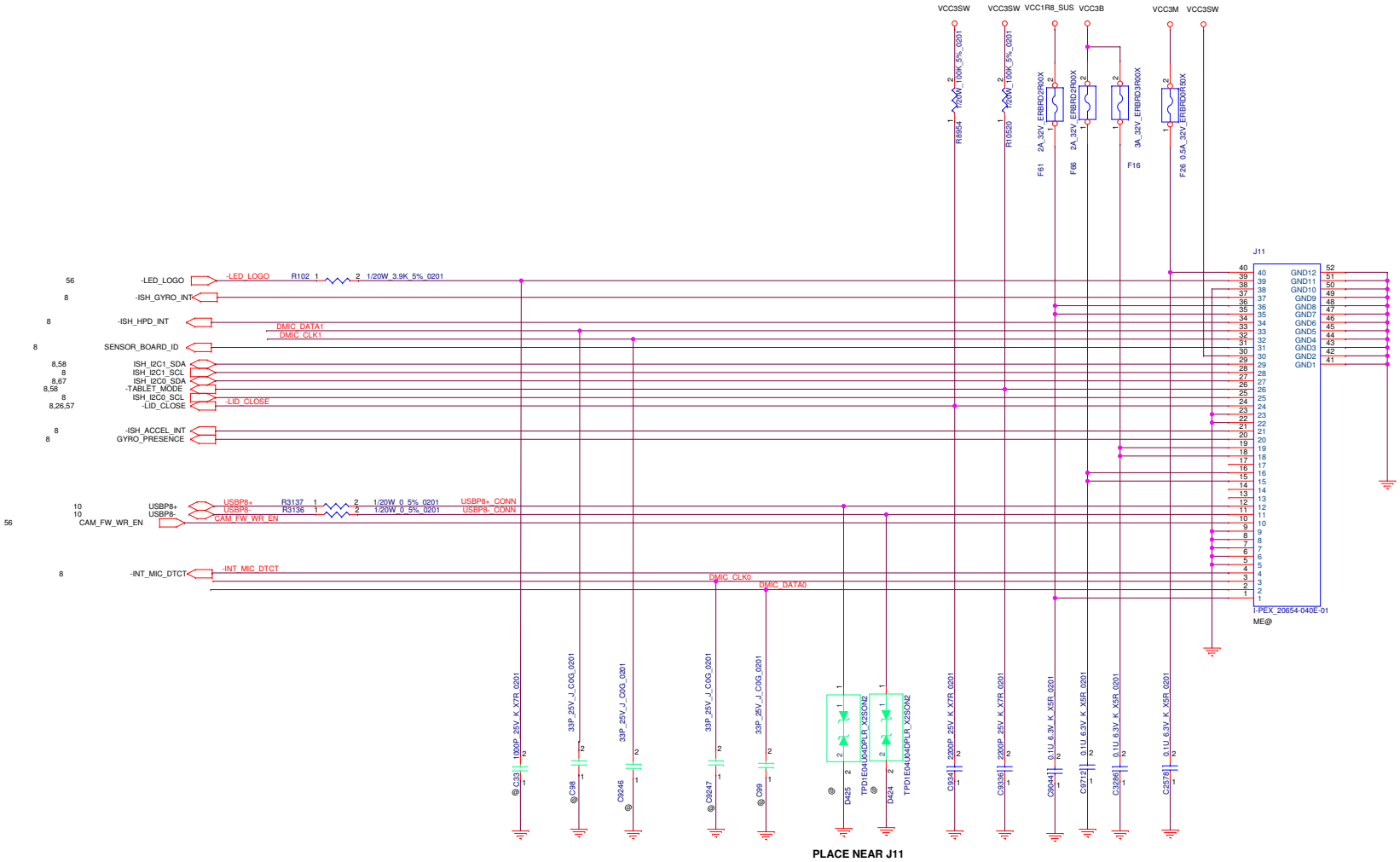
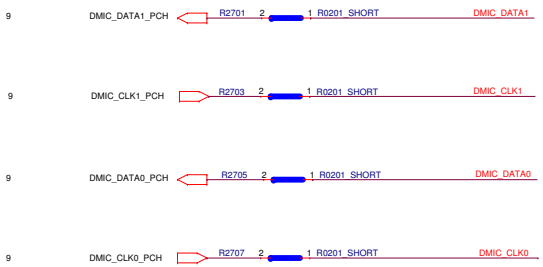


PLACE NEAR J11



Lenovo

Project Name : Ratchet-1	Title : LID/CAMERA/MIC/SENSOR INTERFACE
Size : C	Document Number :
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Project Name : Ratchet-1	Title : BLANK	
Size : C	Document Number :	Rev : 0.01
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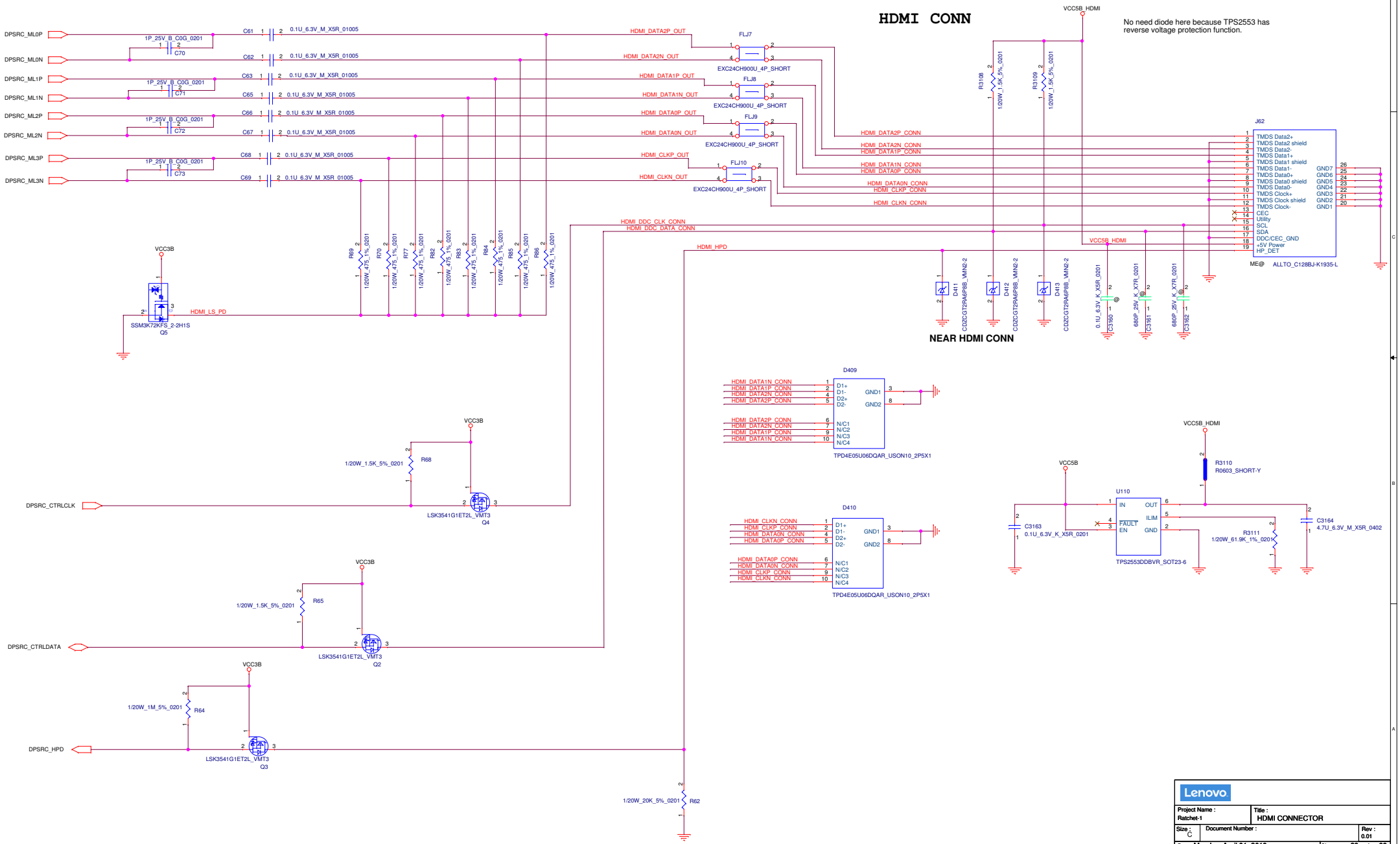
HDMI CONN



Lenovo		
Project Name : Ratchet-1	Title : HDMI CONNECTOR	
Size : C	Document Number :	Rev : 0.01
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I2C from PD for Alpine Ridge should be pulled-up to VCC3_SUS to prevent leakge when VCC3_SUS=OFF and VCC3M=ON

I2C_DATA_TBT R3043 2.2K 5% 0201
I2C_CLK_TBT R3045 2.2K 5% 0201
TBT_RTD3_PWR_EN R92 10K 5% 0201
VCC3_SUS

-TBT_PLUG_EVENT R3048 10K 5% 0201
TBT_SRC0_CFG1 R3051 10K 5% 0201
-TBT_PCIE_WAKE R181 10K 5% 0201

TABLE U2
Nexperia 74AUP1G08GS
TI SN74AUP1G08DSF2

R3156 2.2K 5% 0201
R3157 2.2K 5% 0201
R2908 10K 5% 0201

U182A

PCIE12_L0_TXP / PCIE12_L0_TXN
PCIE12_L1_TXP / PCIE12_L1_TXN
PCIE12_L2_TXP / PCIE12_L2_TXN
PCIE12_L3_TXP / PCIE12_L3_TXN
PCIE12_CLK_100M / -PCIE12_CLK_100M / -CLKREQ_PCIE12
0.22U 6.3V M X5R 01005

PCIE_RX0_P/N
PCIE_RX1_P/N
PCIE_RX2_P/N
PCIE_RX3_P/N
PCIE_REFCLK_100_IN_P/N
PCIE_CLKREQ_N
PCIE GEN3

PCIE_TX0_P/N
PCIE_TX1_P/N
PCIE_TX2_P/N
PCIE_TX3_P/N
PERST_N
PCIE_RBIAS
R29091 3.01K 1% 0201

PCIE12_L0_RXP_C C29101 / PCIE12_L0_RXN_C C29111
PCIE12_L1_RXP_C C29121 / PCIE12_L1_RXN_C C29131
PCIE12_L2_RXP_C C29141 / PCIE12_L2_RXN_C C29151
PCIE12_L3_RXP_C C29161 / PCIE12_L3_RXN_C C29171
0.22U 6.3V M X5R 01005

PCIE12_L0_RXP / PCIE12_L0_RXN
PCIE12_L1_RXP / PCIE12_L1_RXN
PCIE12_L2_RXP / PCIE12_L2_RXN
PCIE12_L3_RXP / PCIE12_L3_RXN

-TBT_PERST_AR
SN74AUP1G08DSF2_SON-6
U2
C100 0.1U 6.3V K X5R 0201
-PLTRST_FAR
-TBT_PERST
R182 10K 5% 0201
Test_Point_20MIL
TP10

AND LOGIC

DDIP1_0P / DDIP1_0N
DDIP1_1P / DDIP1_1N
DDIP1_2P / DDIP1_2N
DDIP1_3P / DDIP1_3N
DDIP1_AUXP / DDIP1_AUXN
DDIP1_HPD
DDIP1_CTRLCLK / DDIP1_CTRLDATA
0.1U 6.3V M X5R 01005

DPSNK0_ML0_P/N
DPSNK0_ML1_P/N
DPSNK0_ML2_P/N
DPSNK0_ML3_P/N
DPSNK0_AUX_P/N
DPSNK0_HPD
DPSNK0_DDC_CLK / DPSNK0_DDC_DATA
SINK PORT 0

DPSRC_ML0_P/N
DPSRC_ML1_P/N
DPSRC_ML2_P/N
DPSRC_ML3_P/N
DPSRC_AUX_P/N
DPSRC_HPD
DPSRC_RBIAS
R2923 14K 1% 0201
SOURCE PORT 0

DPSRC_ML0P / DPSRC_ML0N
DPSRC_ML1P / DPSRC_ML1N
DPSRC_ML2P / DPSRC_ML2N
DPSRC_ML3P / DPSRC_ML3N
DPSRC_HPD

DDIP2_0P / DDIP2_0N
DDIP2_1P / DDIP2_1N
DDIP2_2P / DDIP2_2N
DDIP2_3P / DDIP2_3N
DDIP2_AUXP / DDIP2_AUXN
DDIP2_HPD
0.1U 6.3V M X5R 01005

DPSNK1_ML0_P/N
DPSNK1_ML1_P/N
DPSNK1_ML2_P/N
DPSNK1_ML3_P/N
DPSNK1_AUX_P/N
DPSNK1_HPD
DPSNK1_DDC_CLK / DPSNK1_DDC_DATA
DPSNK_RBIAS
SINK PORT 1

GPIO_0 ... GPIO_8
TBT_TMU_CLK_OUT
TBT_SRC0_CFG1
LC GPIO

POC_GPIO_0 ... POC_GPIO_6
-BATLOW_TBT
-PCH_SLP_S3_TBT
D415 / D416 RB521CM-30T2R VMN2M-2
POC GPIO

TEST_EN
TEST_PWR_GOOD
RESET_N
R2927 100_5% 0201
R2928 100_5% 0201
-TBT_RESET
Misc

I2C_DATA_TBT
I2C_CLK_TBT
-TBT_EE_WP
-TBT_PCIE_WAKE
-TBT_PLUG_EVENT
DPSRC_CTRLDATA
DPSRC_CTRLCLK
-TBT_I2C_INT
TBT_FORCE_USB_PWR
TBT_FORCE_PWR
-BATLOW
-PCH_SLP_S3
TBT_RTD3_PWR_EN
R179 10K 5% 0201
D14 / D15 RB521CM-30T2R VMN2M-2
-TBT_RESET_EC
-TBT_RESET_PD

VCC3_TBT_LC

R2920 14K 1% 0201
R2932 10K 5% 0201
R2933 10K 5% 0201
R2934 10K 5% 0201
R2935 10K 5% 0201
R2921 4.75K 0.5% 0201
TDI / TMS / TCK / TDO / RBIAS / RSENSE
MISC

XTAL_25_IN / XTAL_25_OUT
TBT_XTAL_25_IN
TBT_XTAL_25_OUT

EE_DI / EE_DO / EE_CS_N / EE_CLK
TBT_EE_DI / TBT_EE_DO / -TBT_EE_CS / TBT_EE_CLK

AND LOGIC

TBTA_RX2P / TBTA_RX2N
TBTA_TX2P / TBTA_TX2N
TBTA_TX1P / TBTA_TX1N
TBTA_RX1P / TBTA_RX1N
TBTA_AUXP / TBTA_AUXN
TBTA_LSTX / TBTA_LSRX / TBTA_HPD
PA_RX1_P/N
PA_TX1_P/N
PA_TX0_P/N
PA_RX0_P/N
PA_DPSRC_AUX_P/N
PA_USB2_D_P/N
PA_LSTX / PA_LSRX / PA_DPSRC_HPD
PA_USB2_RBIAS
R2922 499_1% 0201
Port A

PB_RX1_P/N
PB_TX1_P/N
PB_TX0_P/N
PB_RX0_P/N
PB_DPSRC_AUX_P/N
PB_USB2_D_P/N
PB_LSTX / PB_LSRX / PB_DPSRC_HPD
PB_USB2_RBIAS
R2929 21/20W_499_1% 0201
PORT B

TBTB_RX2P / TBTB_RX2N
TBTB_TX2P / TBTB_TX2N
TBTB_TX1P / TBTB_TX1N
TBTB_RX1P / TBTB_RX1N
TBTB_AUXP / TBTB_AUXN
TBTB_LSTX / TBTB_LSRX / TBTB_HPD

TBT PORTS
POC

THERMDA_1 / THERMDA_2
PCIE_ATEST
TEST_EDM
FUSE_VQPS_64 / FUSE_VQPS_128
MONDC_CIO_0 / MONDC_CIO_1
MONDC_SVR
ATEST_P / ATEST_N
USB2_ATEST
MONDC_DPSNK_0 / MONDC_DPSNK_1
MONDC_DPSRC
JHL6540 SLLSM C1_FC-CSP337
DEBUG

R2945 1M 5% 0201
R2946 1M 5% 0201
R2947 100K 5% 0201
R101 100K 5% 0201
R3069 100K 5% 0201
R3112 100K 5% 0201
R2948 100K 5% 0201
R2949 1M 5% 0201
R2950 1M 5% 0201

R2936 0_5% 0201
Y7 25MHZ_18PF_7R25080003
C3012 27P_25V_J_C0G_0201
C3013 27P_25V_J_C0G_0201

25MHz 18pF 30ppm 2016
TXC 7R25080003
KDS 1ZZHAE25000CC0F
EPSON Q22FA1280056000

TBT_RTD3_PWR_EN R303 10K 5% 0201
TBT_TMU_CLK_OUT R2924 100K 5% 0201
TBT_FORCE_USB_PWR R2925 10K 5% 0201
TBT_FORCE_PWR R3052 100K 5% 0201
-BATLOW_TBT R3053 100K 5% 0201
-PCH_SLP_S3_TBT R3054 10K 5% 0201
-TBT_EE_WP R9888 10K 5% 0201

Lenovo
Project Name : Ratchet-1
Title : ALPINE RIDGE (1/2)
Size : C
Document Number :
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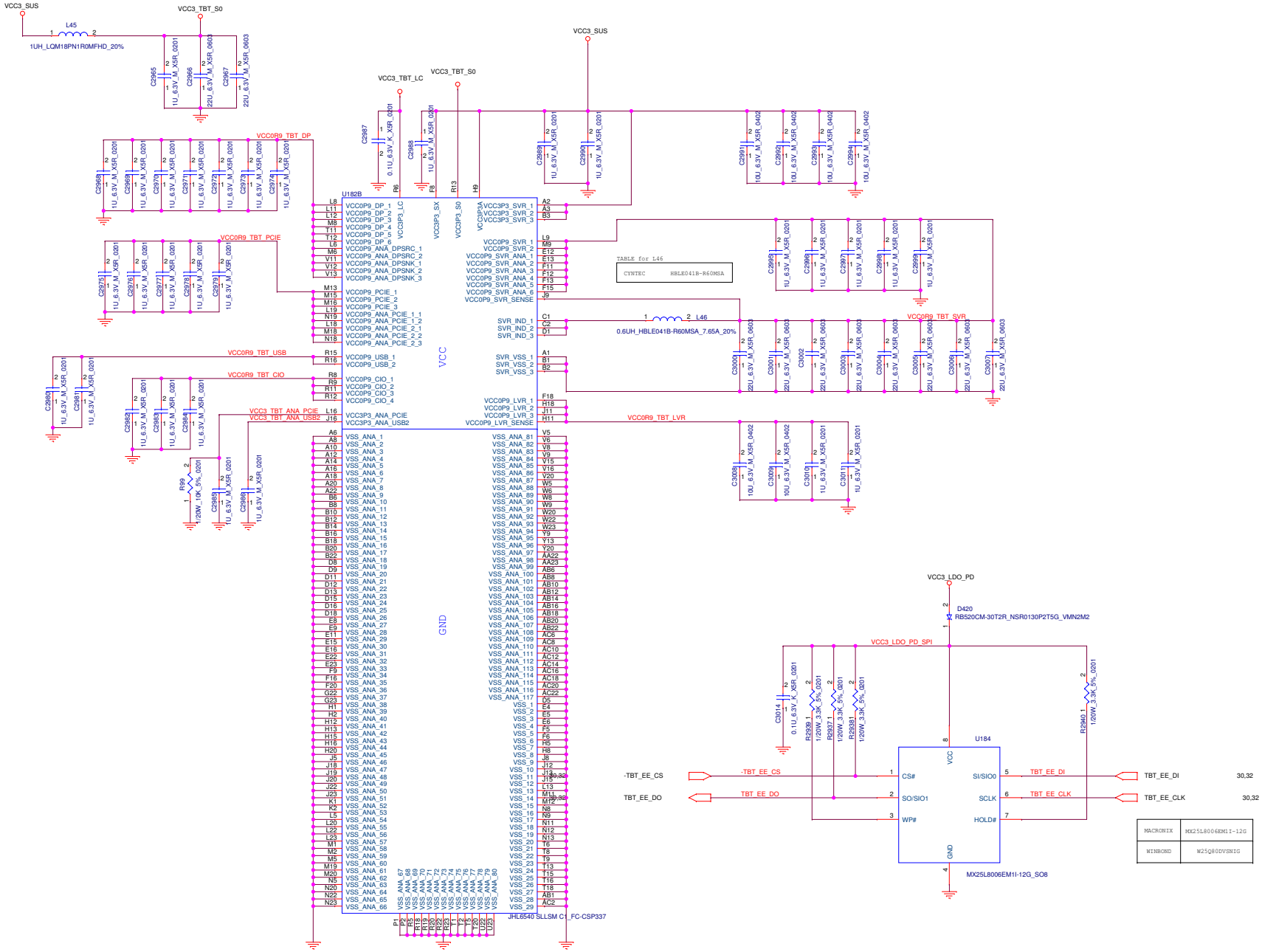

Project Name : Ratchet-1	Title : ALPINE RIDGE (2/2)
Size : C	Document Number :
Date: Monday, April 01, 2019	Rev : 0.01
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TABLE I2C Addressing

I2C1(to EC)	TBTA PORT	0x23
	TBTB PORT	0x27
I2C2(to AR)	TBTA PORT	0x38
	TBTB PORT	0x3F

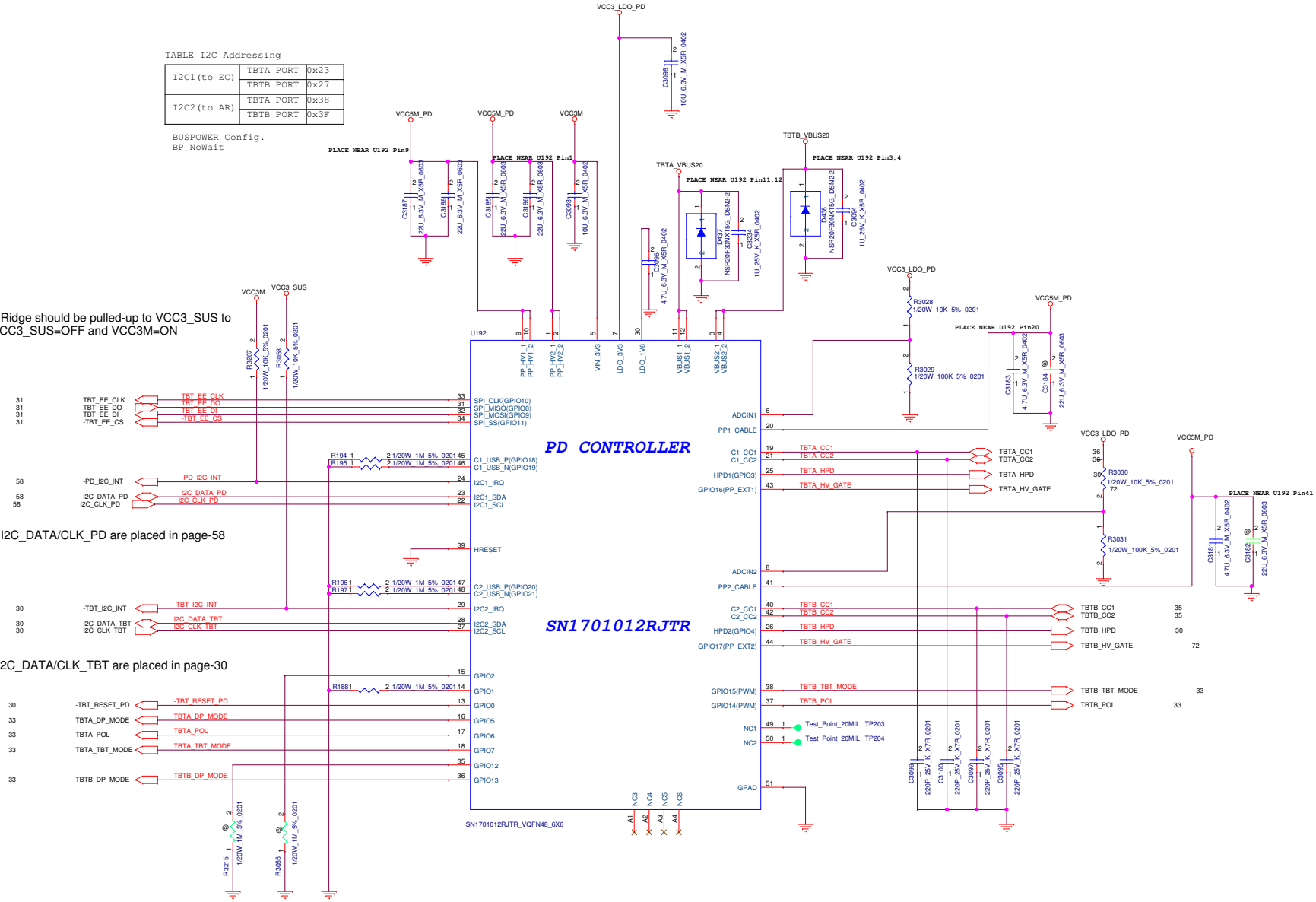
BUSPOWER Config.
BP_NoWait

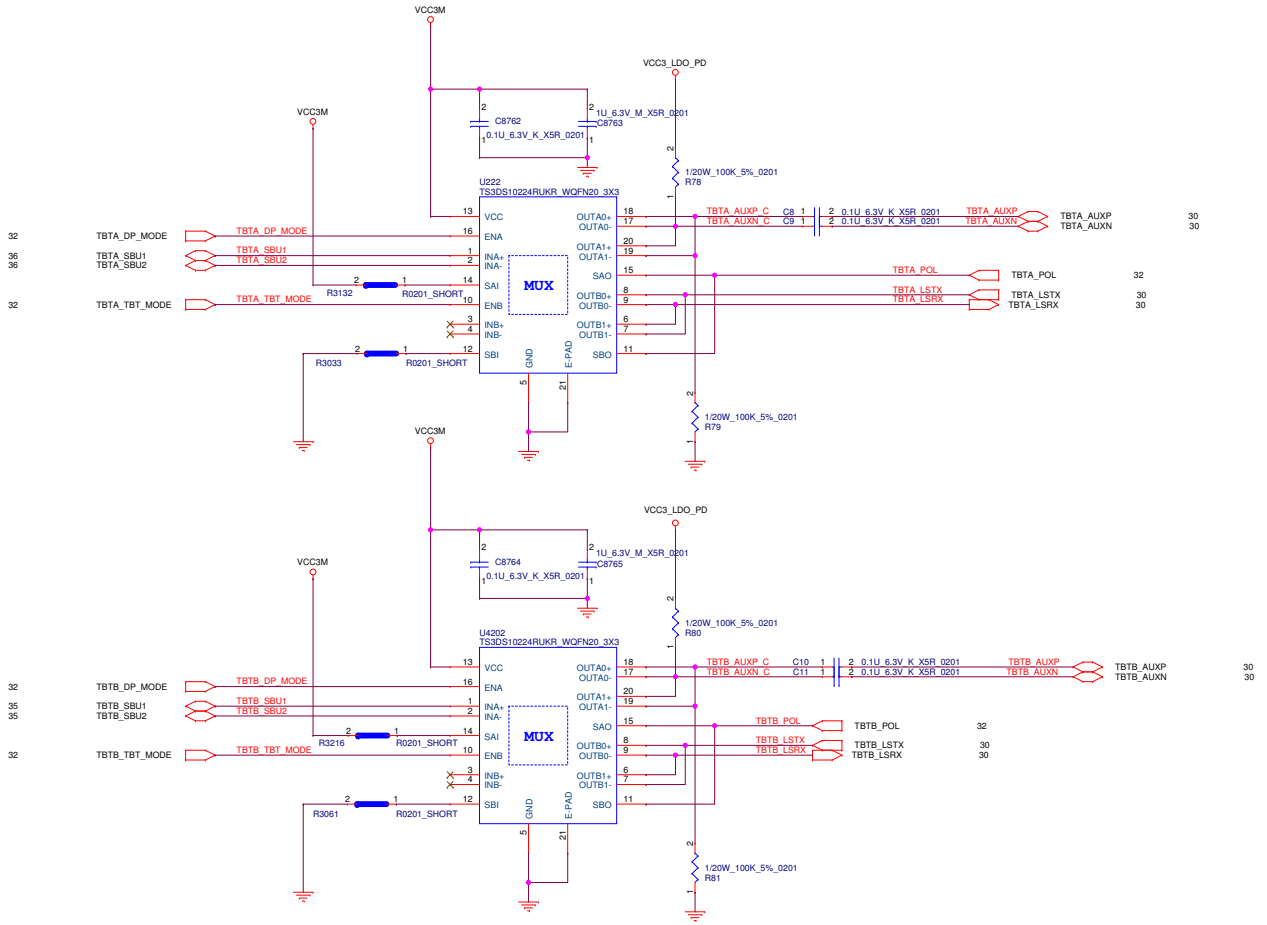
I2C from PD for Alpine Ridge should be pulled-up to VCC3_SUS to prevent leakge when VCC3_SUS=OFF and VCC3M=ON

Pull-up resisters for I2C_DATA/CLK_PD are placed in page-58

Pull-up resisters for I2C_DATA/CLK_TBT are placed in page-30

GPIO2/12 can be floating when unused.





Lenovo	
Project Name : Ratchet-1	Title : USB PD DEMUX
Size : C	Document Number :
Rev : 0.01	
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Lenovo		
Project Name : Ratchet-1	Title : BLANK	
Size : C	Document Number :	Rev : 0.01
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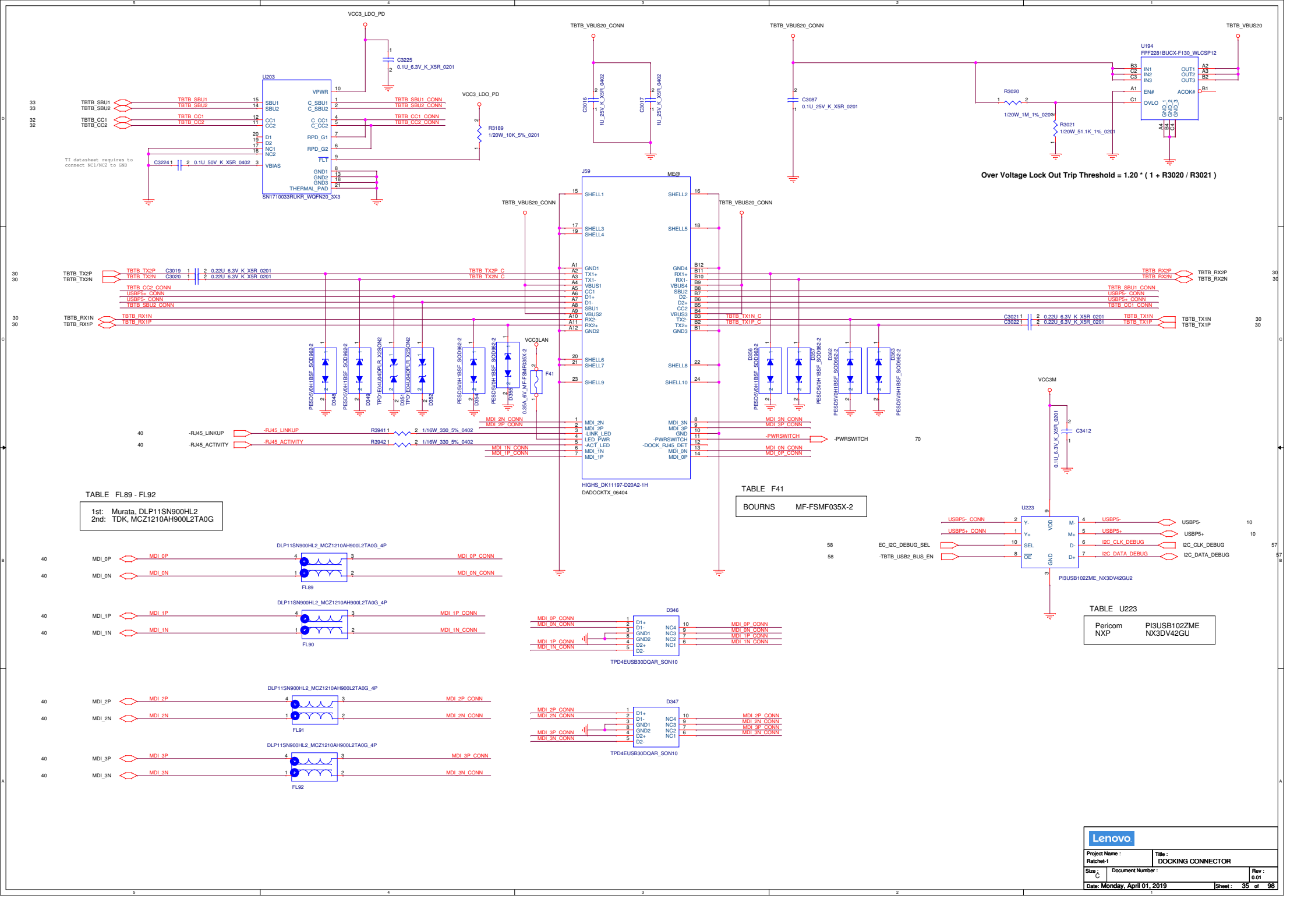
VCC3_LDO_PD
U203
SN1710033RUKR_WQFN20_3X3
TI datasheet requires to connect NC1/NC2 to GND
TBTB_VBUS20_CONN
U194
FPF2281BUCX-F130_WLCSP12
Over Voltage Lock Out Trip Threshold = 1.20 * (1 + R3020 / R3021)
J59
HIGHS_DK11197-D20A2-1H
DADOCKTX_06404
VCC3LAN
VCC3M
TABLE FL89 - FL92
1st: Murata, DLP11SN900HL2
2nd: TDK, MCZ1210AH900L2TA0G
TABLE F41
BOURNS MF-FSMF035X-2
TABLE U223
Pericom PI3USB102ZME
NXP NX3DV42GU
PI3USB102ZME_NX3DV42GU2
TPD4EUSB30DQAR_SON10
Lenovo
Project Name : Ratchet-1
Title : DOCKING CONNECTOR
Size : C
Document Number :
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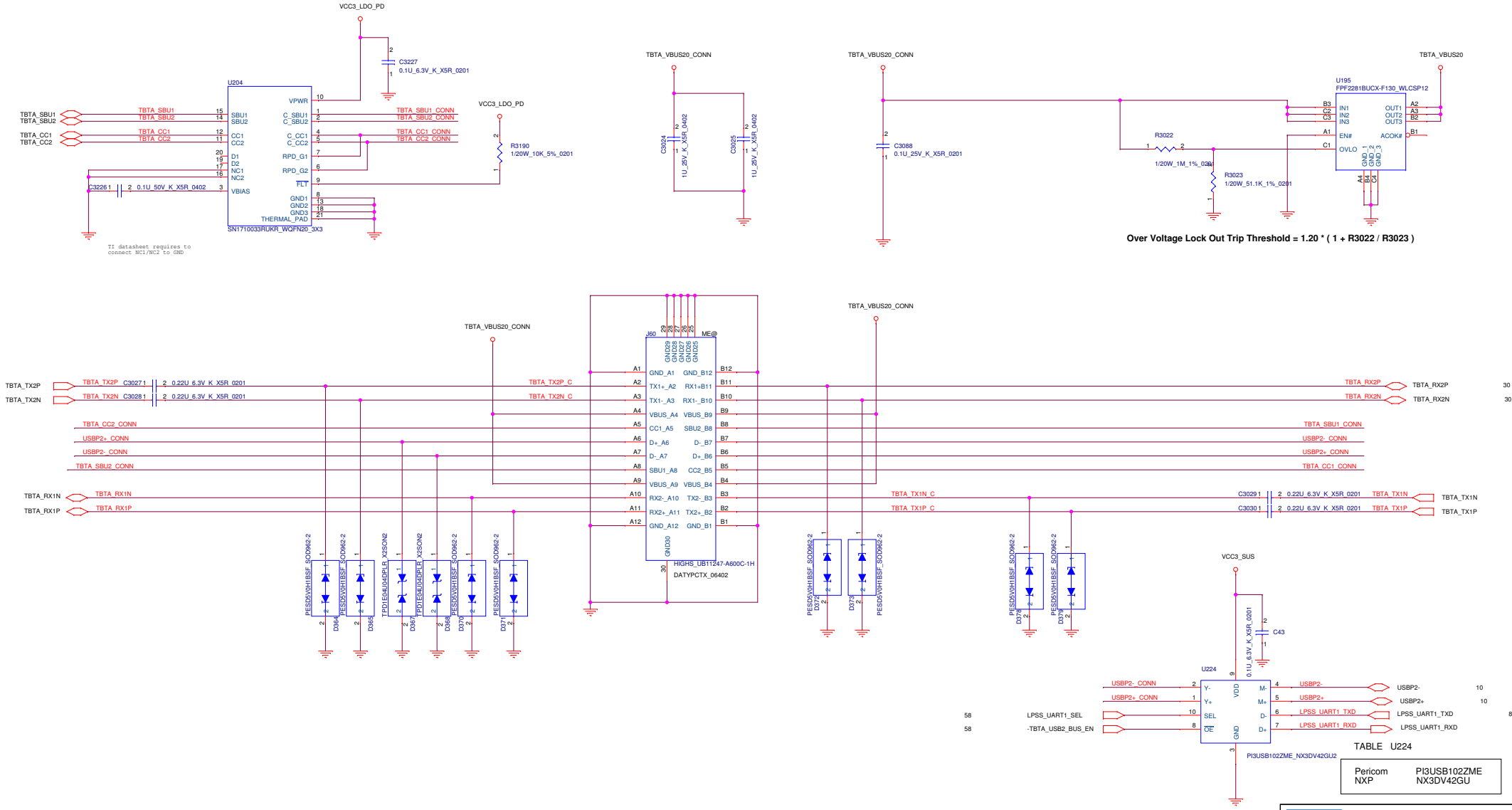

Lenovo

Project Name : Ratchet-1	Title : THUNDERBOLT CONNECTOR
Size : C	Document Number :
Date: Monday, April 01, 2019	Rev : 0.01
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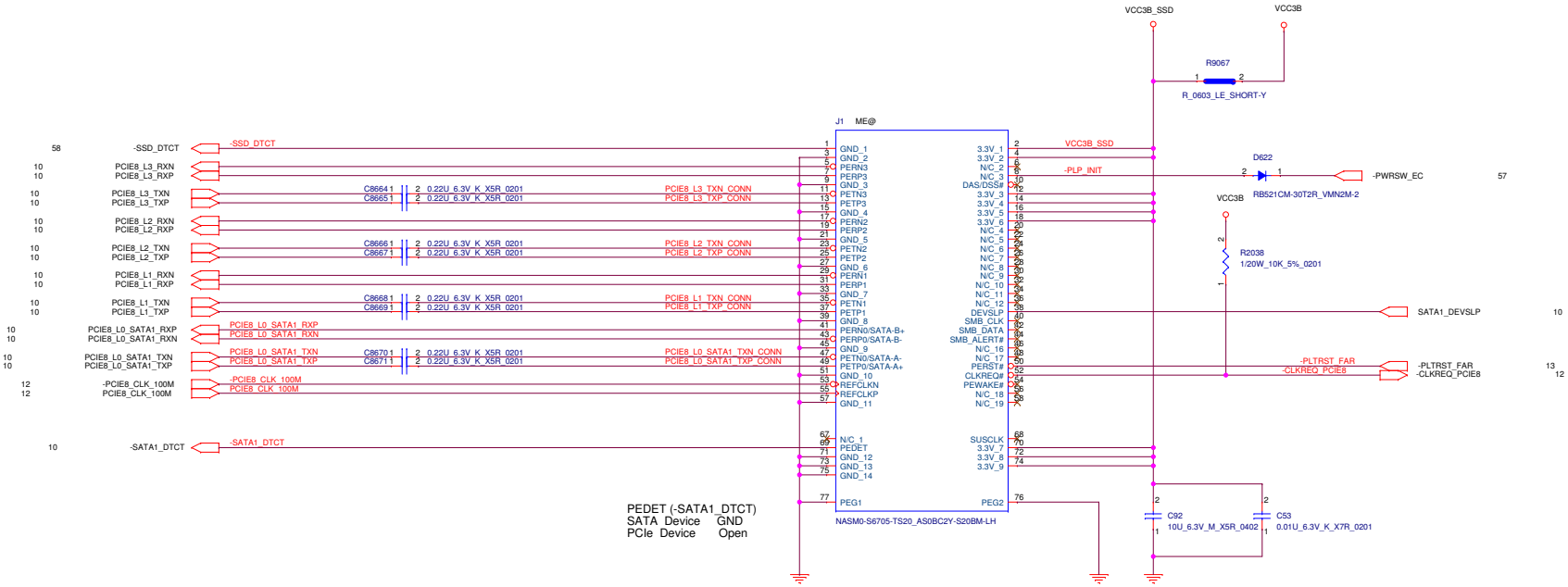
M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.00mm Connector



Project Name : Ratchet-1	Title : M.2 SOCKET 3 MODULE I/F
Size : C	Document Number :
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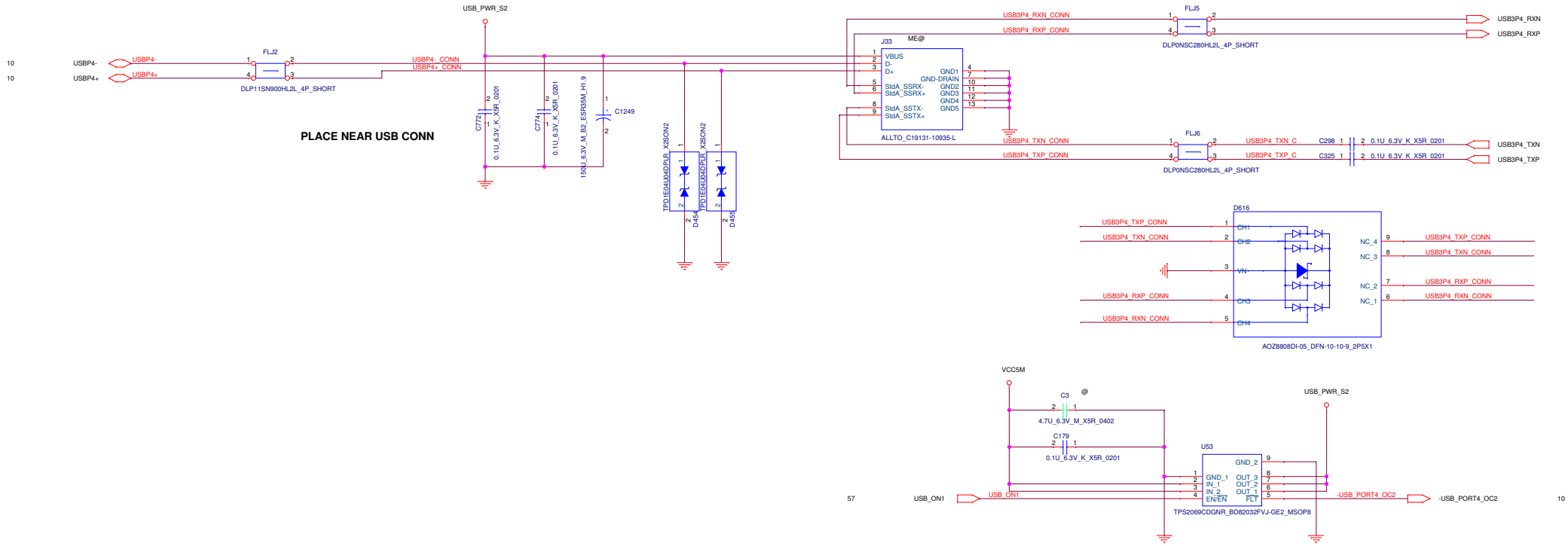
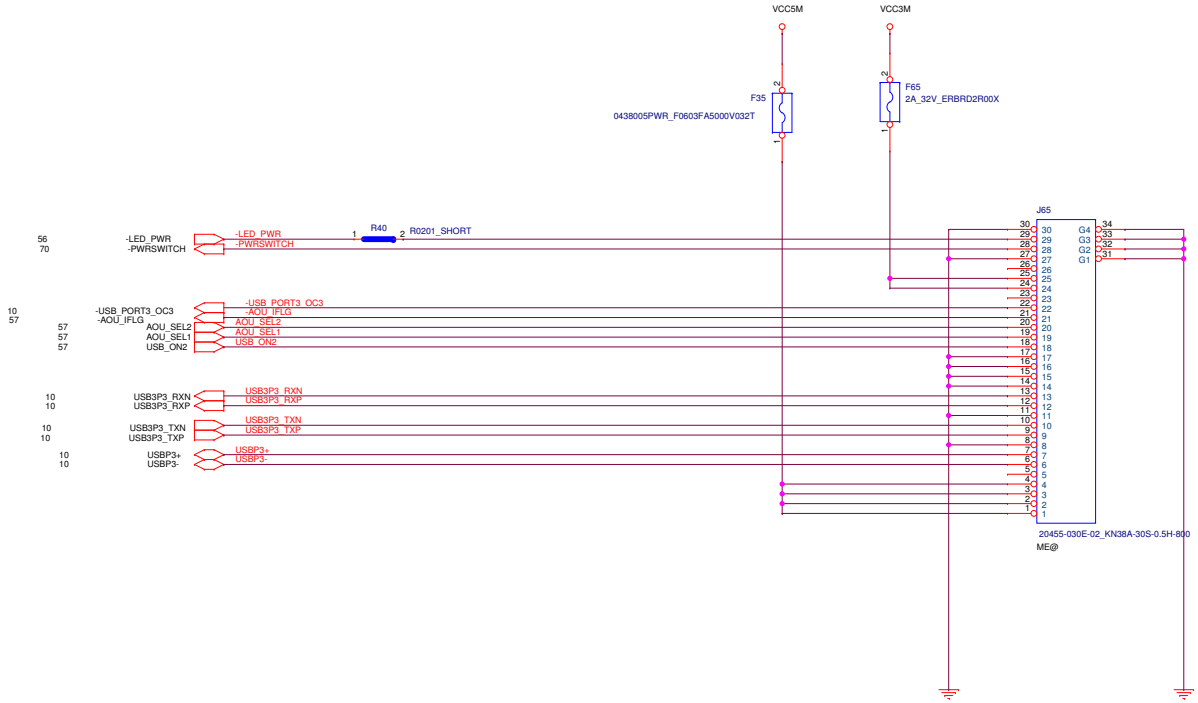
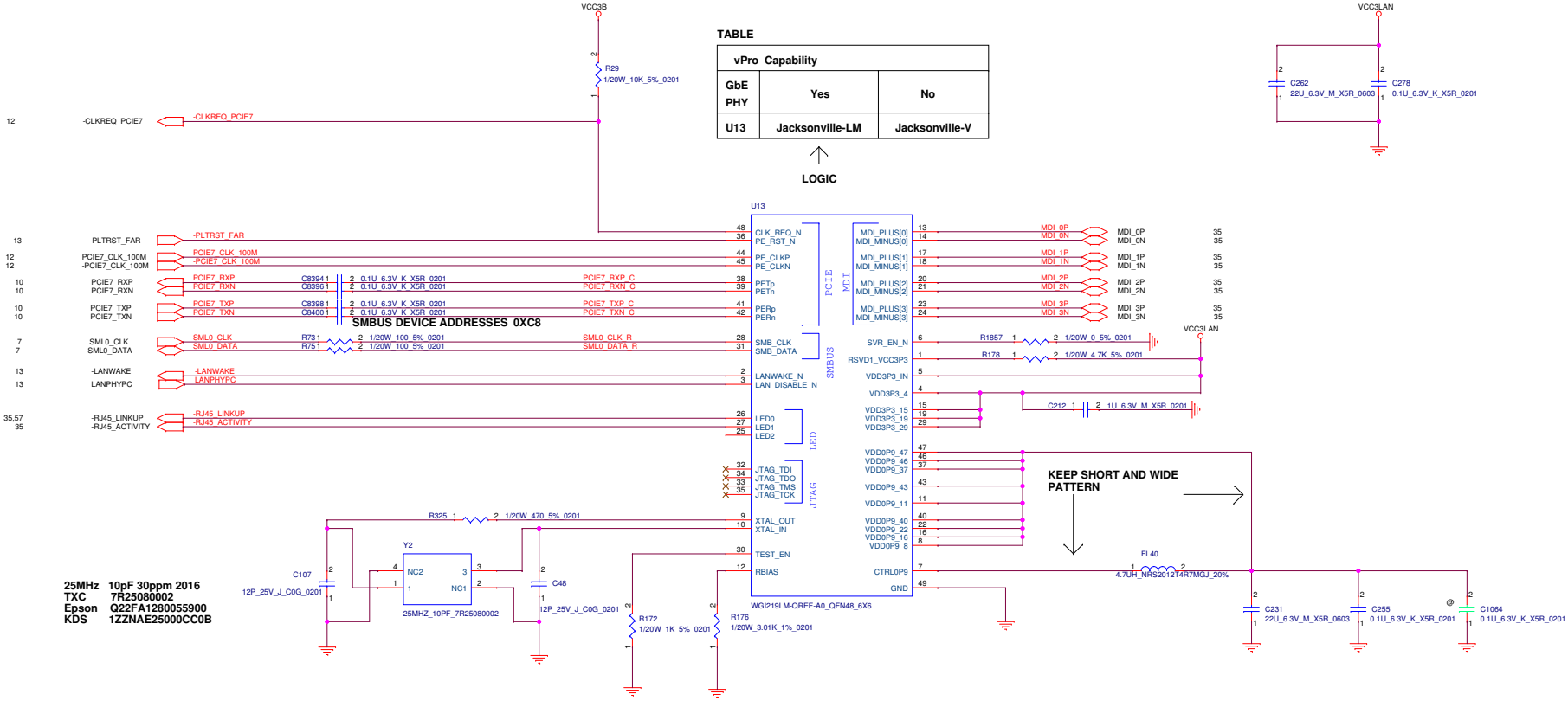
Date: Monday, April 01, 2019	Sheet : 37 of 98



Project Name : Ratchet-1	Title : USB TYPE-A CONNECTOR
Size : C	Document Number :
Rev : 0.01	
Date: Monday, April 01, 2019	Sheet : 38 of 98



Project Name : Ratchet-1	Title : USB TYPE-A SUBCARD INTERFAC
Size : C	Document Number :
Rev : 0.01	
Date: Monday, April 01, 2019	Sheet : 39 of 98



Project Name : Ratchet-1	Title : GBE JACKSONVILLE
Size : C	Document Number :
Date: Monday, April 01, 2019	Rev : 0.01
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Project Name : Ratchet-1	Title : BLANK
Size : C	Document Number :
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Date: Monday, April 01, 2019	Sheet : 41 of 98

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Project Name : Ratchet-1	Title : BLANK
Size : C	Document Number :
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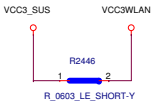
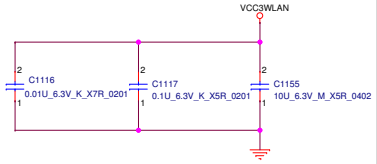
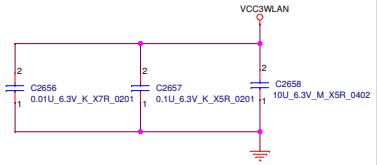
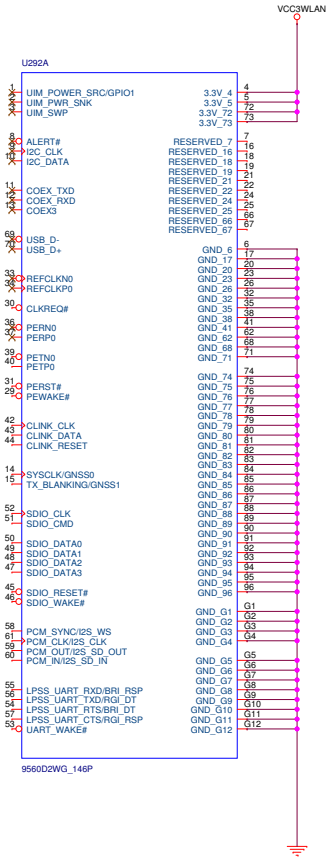
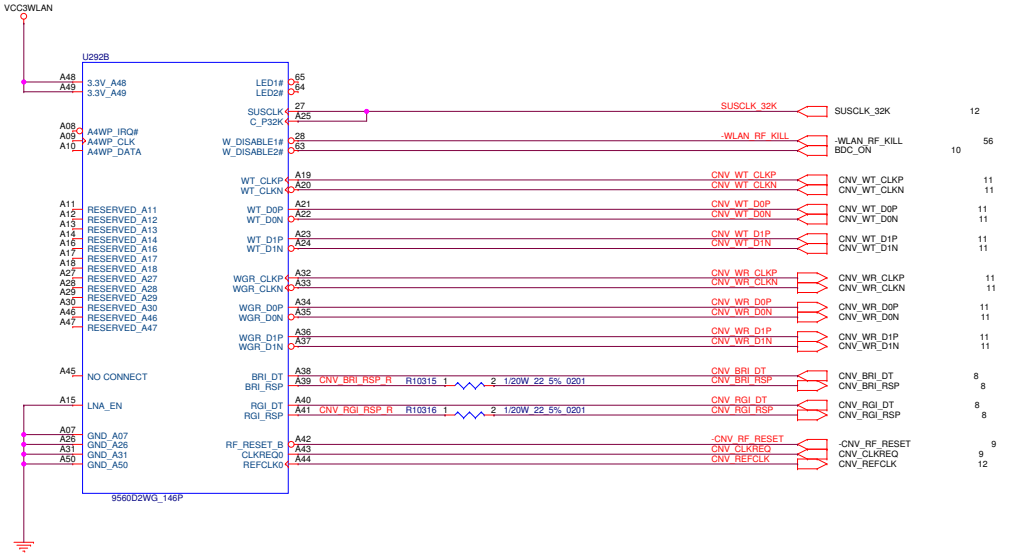
M.2 Type 1216 Module for WLAN / Bluetooth











Lenovo			
Project Name : Ratchet-1		Title : M.2 TYPE 1216 MODULE	
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M.2 Socket 2 (Key-B) for 3042 S3 WWAN

H=2.00mm Connector

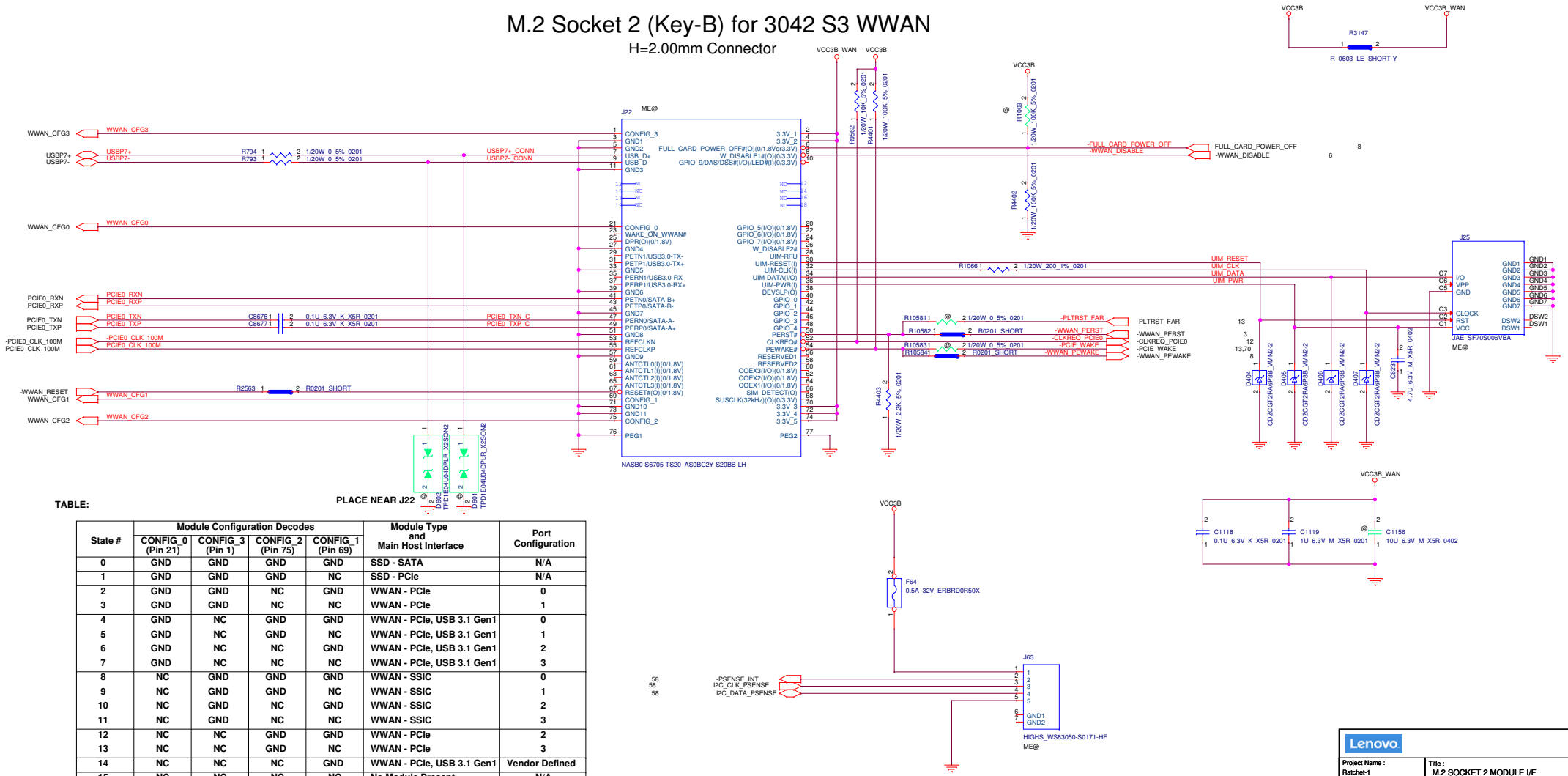

TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A

Project Name : Ratchet-1	Title : M.2 SOCKET 2 MODULE I/F
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Project Name : Ratchet-1	Title : BLANK	
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Project Name : Ratchet-1	Title : BLANK
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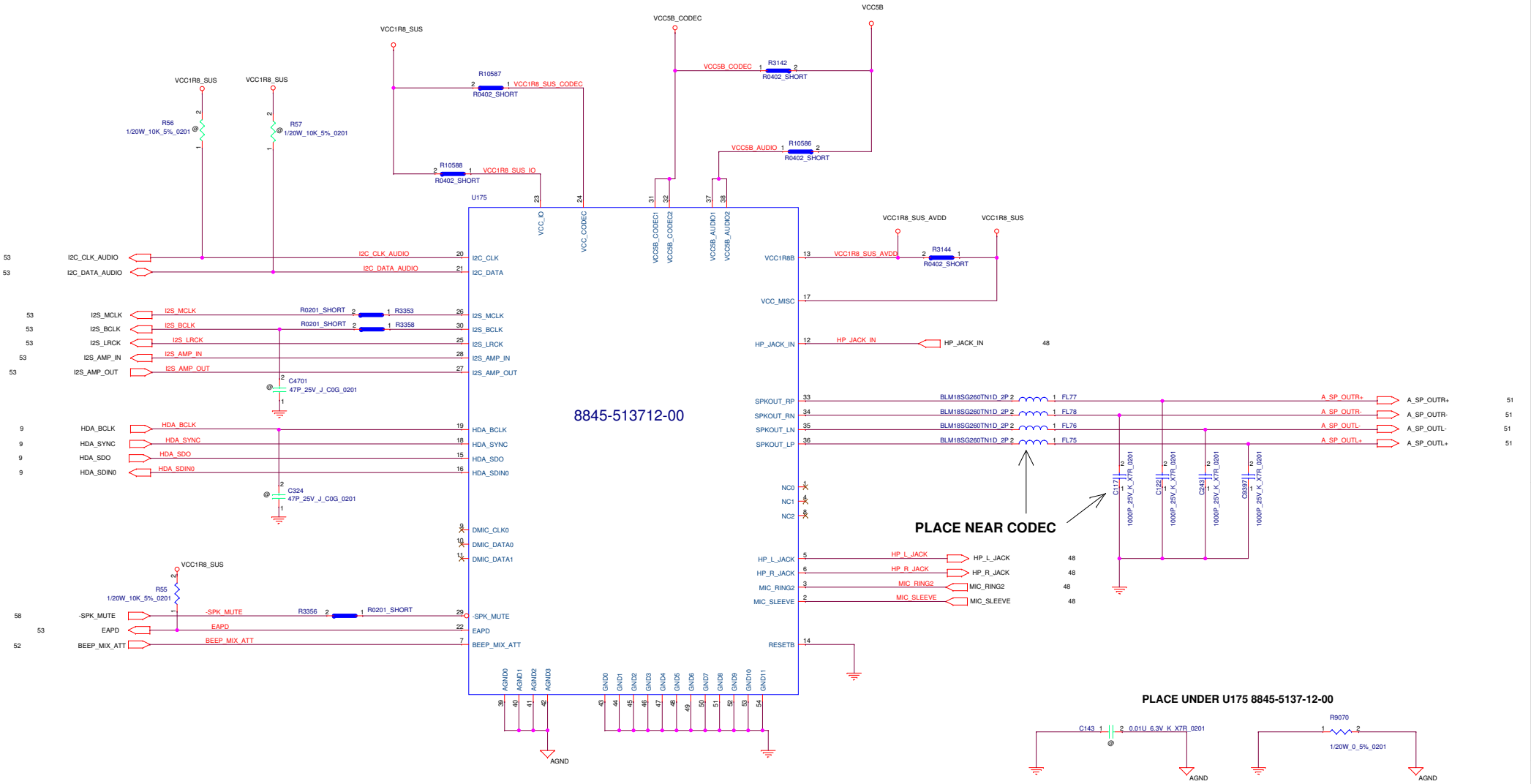
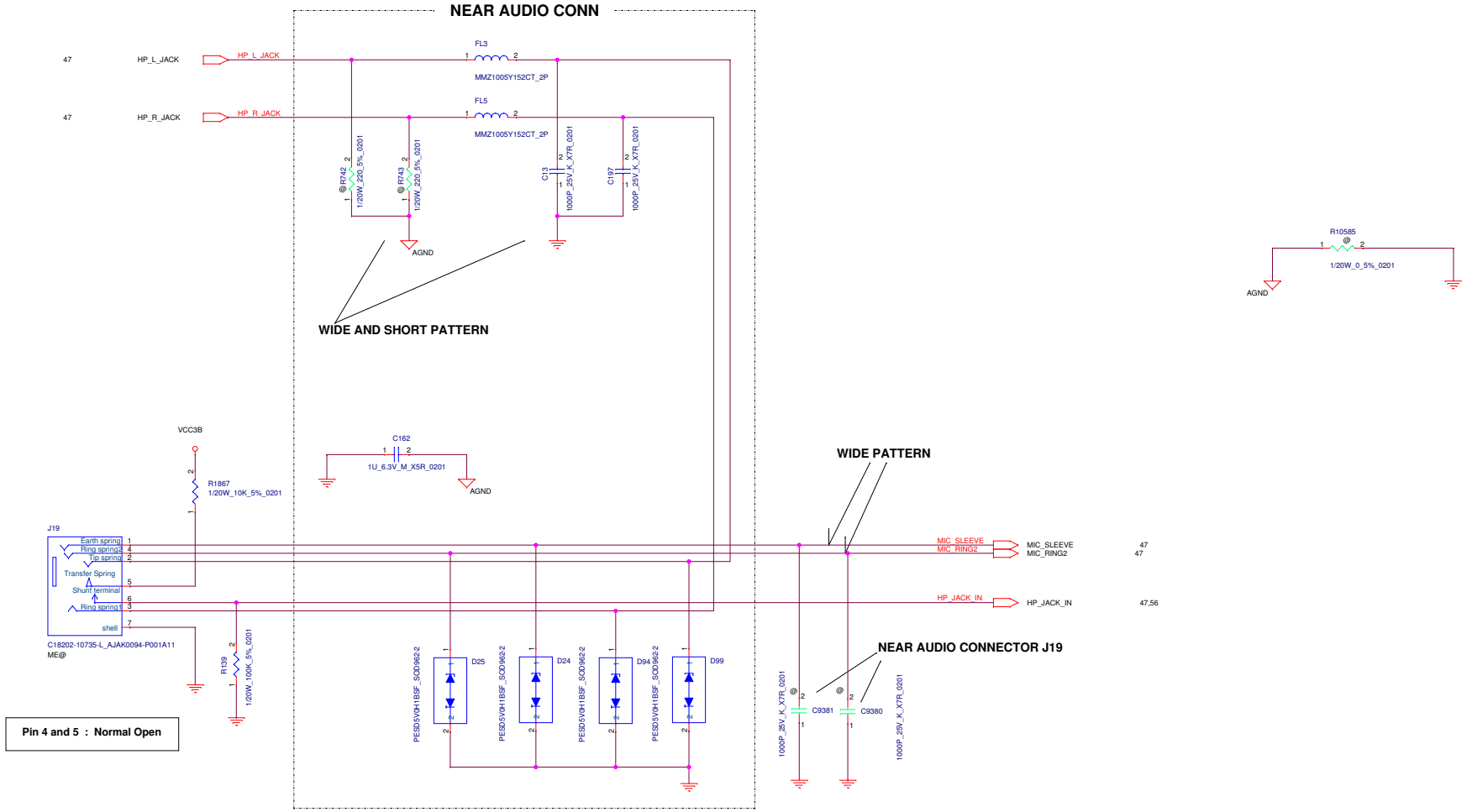


Lenovo			
Project Name : Ratchet-1		Title : AUDIO SIP (ALC3286)	
Size :	Document Number :		Rev : 0.01
Date: Monday, April 01, 2019		Sheet : 47 of 98	



Project Name : Ratchet-1	Title : AUDIO CONNECTOR
Size : C	Document Number :
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Project Name : Ratchet-1	Title : BLANK
Size : C	Document Number :
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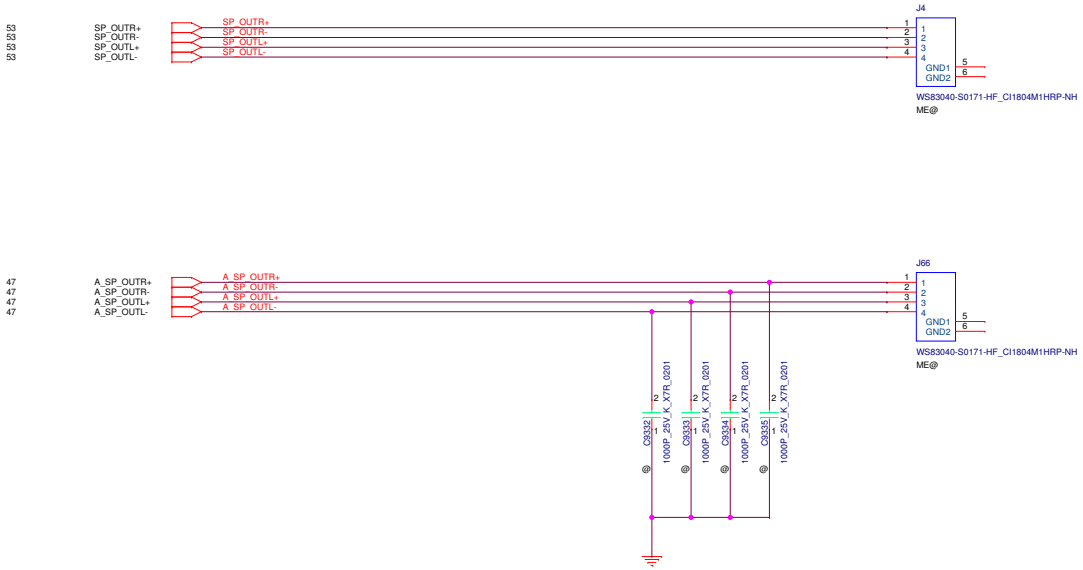
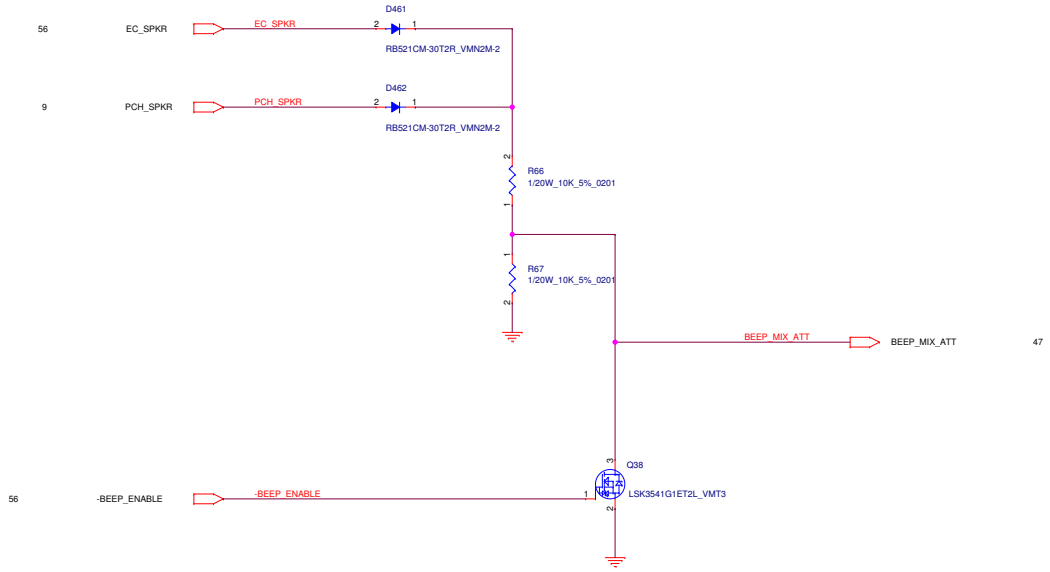
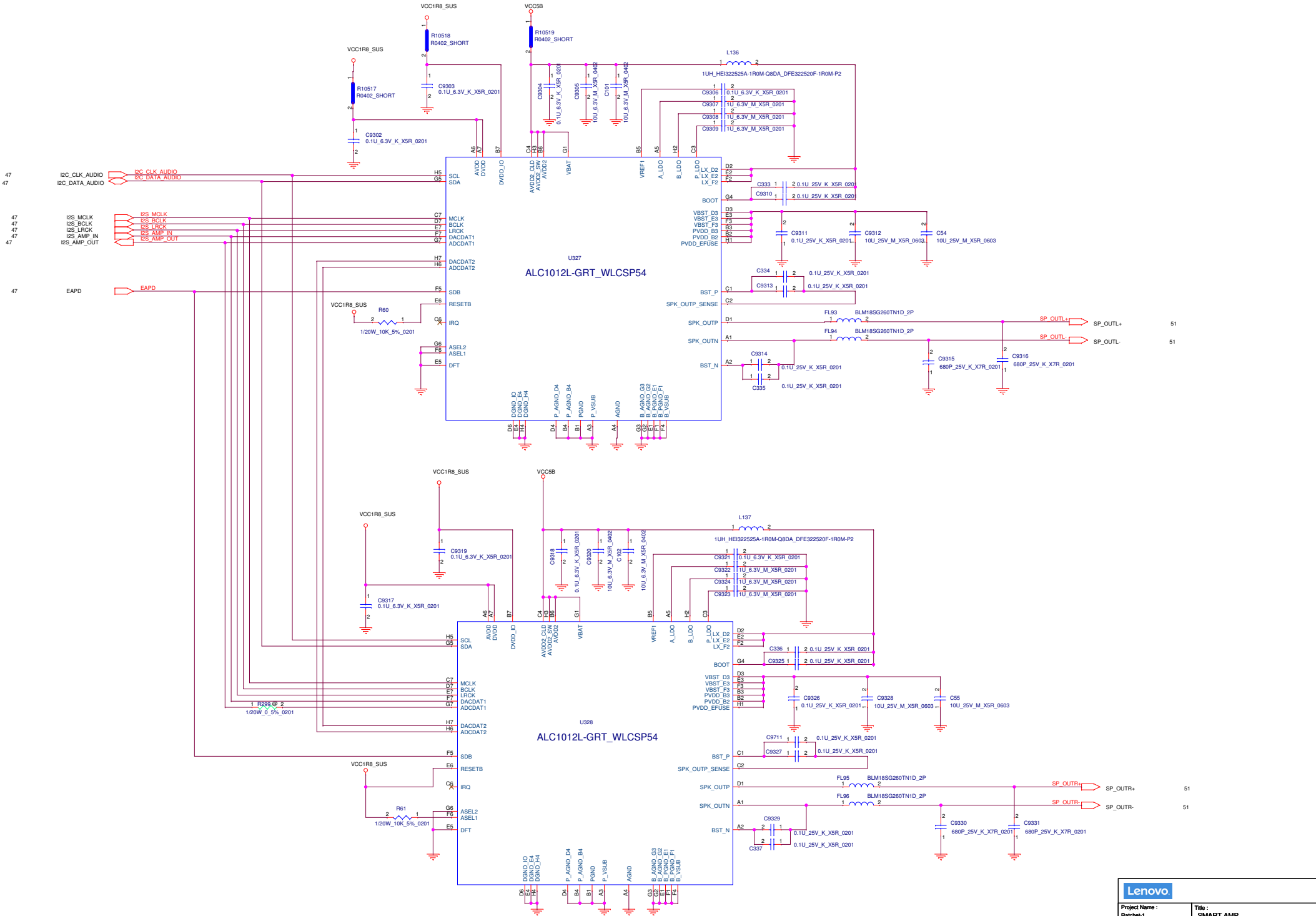
Project Name : Ratchet-1	Title : BLANK	
Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 50 of 98	



Lenovo		
Project Name : Ratchet-1	Title : AUDIO SPEAKER	
Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 51 of 98	



Lenovo			
Project Name : Ratchet-1		Title : AUDIO BEEP	
Size : C	Document Number :		Rev : 0.01
Date: Monday, April 01, 2019		Sheet : 52 of 98	



Project Name : Ratchet-1	Title : SMART AMP	
Size : C	Document Number :	Rev : 0.01
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Project Name : Ratchet-1	Title : BLANK
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Project Name : Ratchet-1	Title : BLANK	
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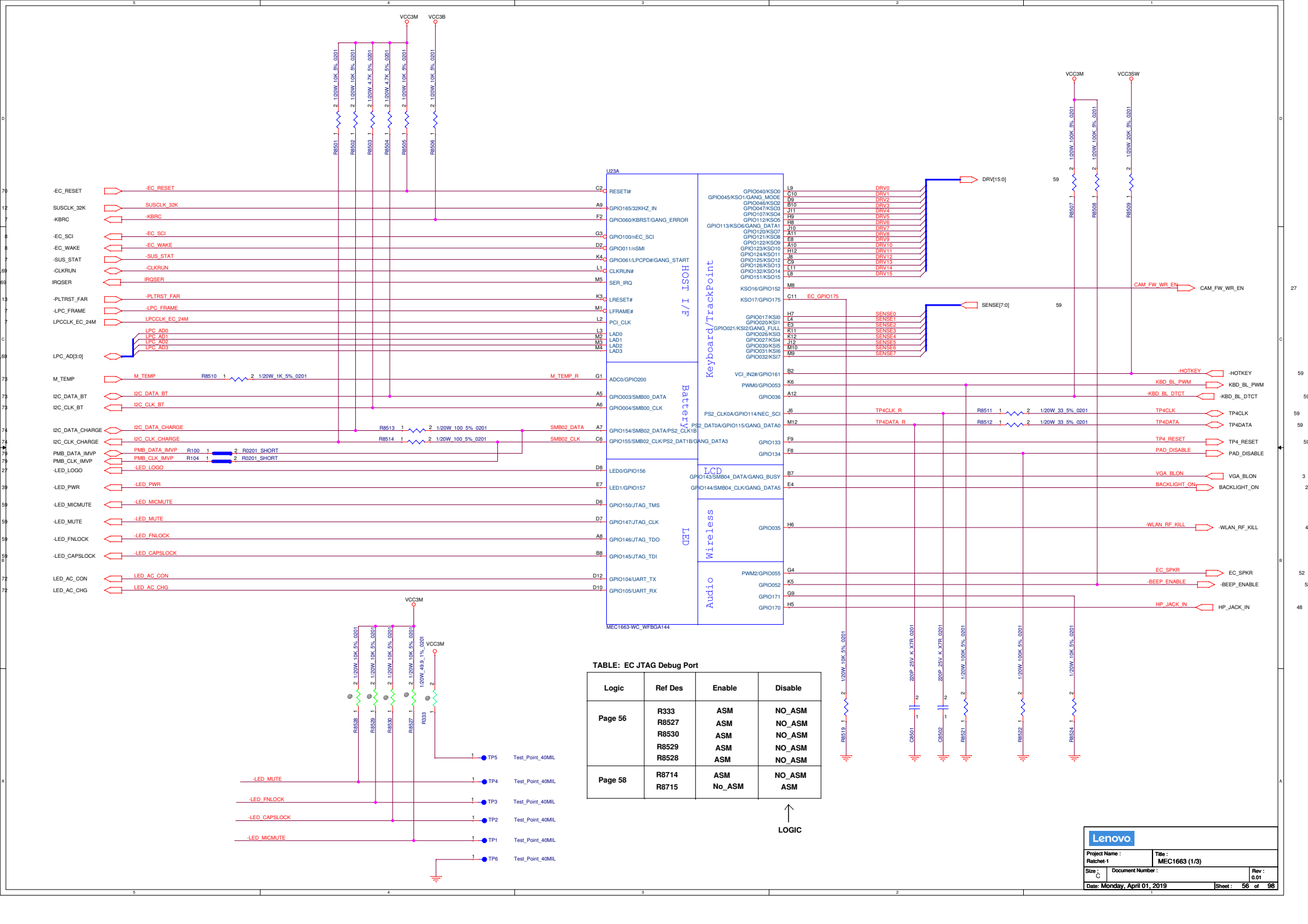

TABLE: EC JTAG Debug Port

Logic	Ref Des	Enable	Disable
Page 56	R333	ASM	NO_ASM
	R8527	ASM	NO_ASM
	R8530	ASM	NO_ASM
	R8529	ASM	NO_ASM
	R8528	ASM	NO_ASM
Page 58	R8714	ASM	NO_ASM
	R8715	No_ASM	ASM

LOGIC

Project Name : Ratchet-1		Title : MEC1663 (1/3)	
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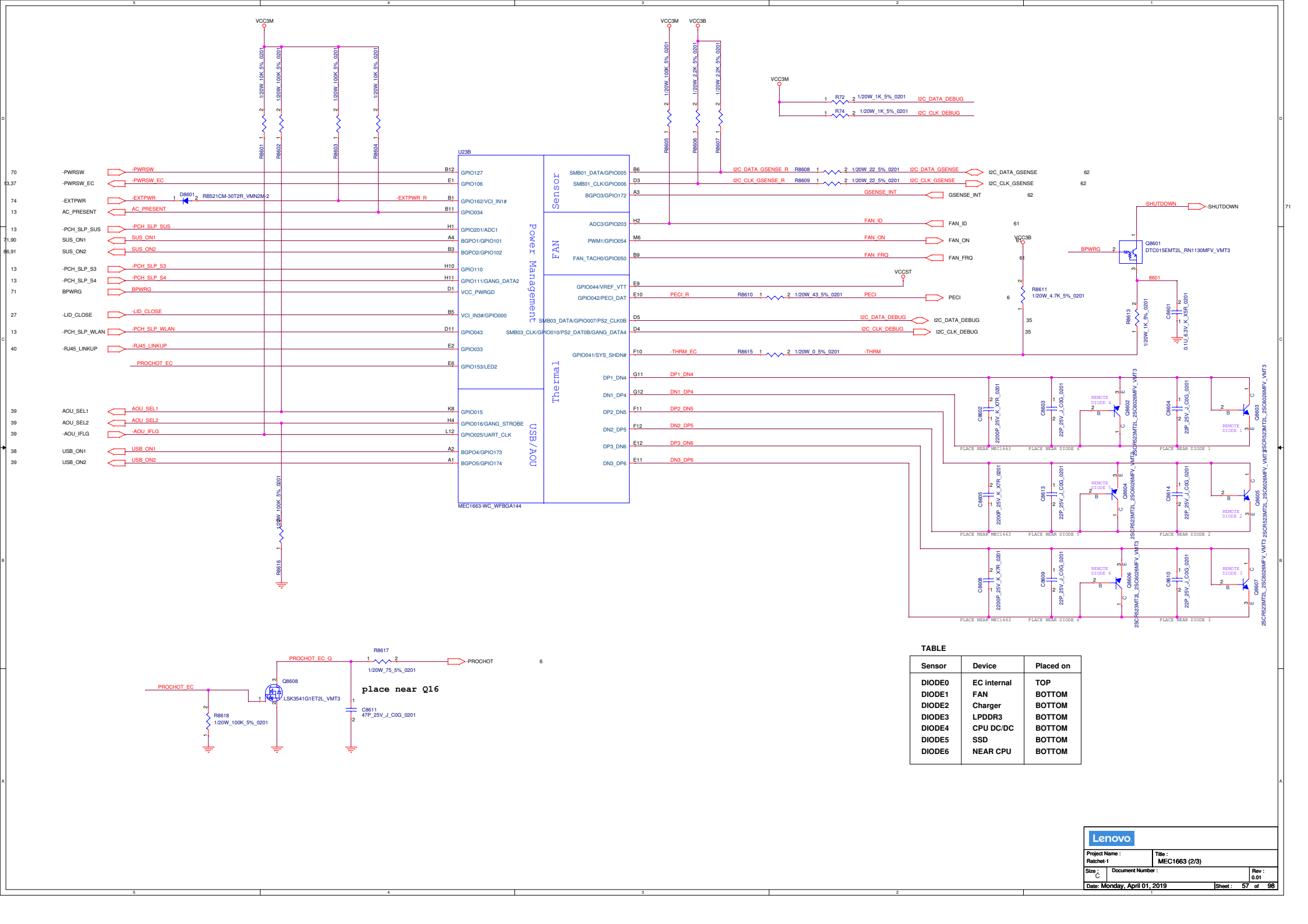

TABLE

Sensor	Device	Placed on
DIODE0	EC internal	TOP
DIODE1	FAN	BOTTOM
DIODE2	Charger	BOTTOM
DIODE3	LPDDR3	BOTTOM
DIODE4	CPU DC/DC	BOTTOM
DIODE5	SSD	BOTTOM
DIODE6	NEAR CPU	BOTTOM

Project Name : Ratchet-1	Title : MEC1663 (2/3)	
Size : C	Document Number :	Rev : 0.01
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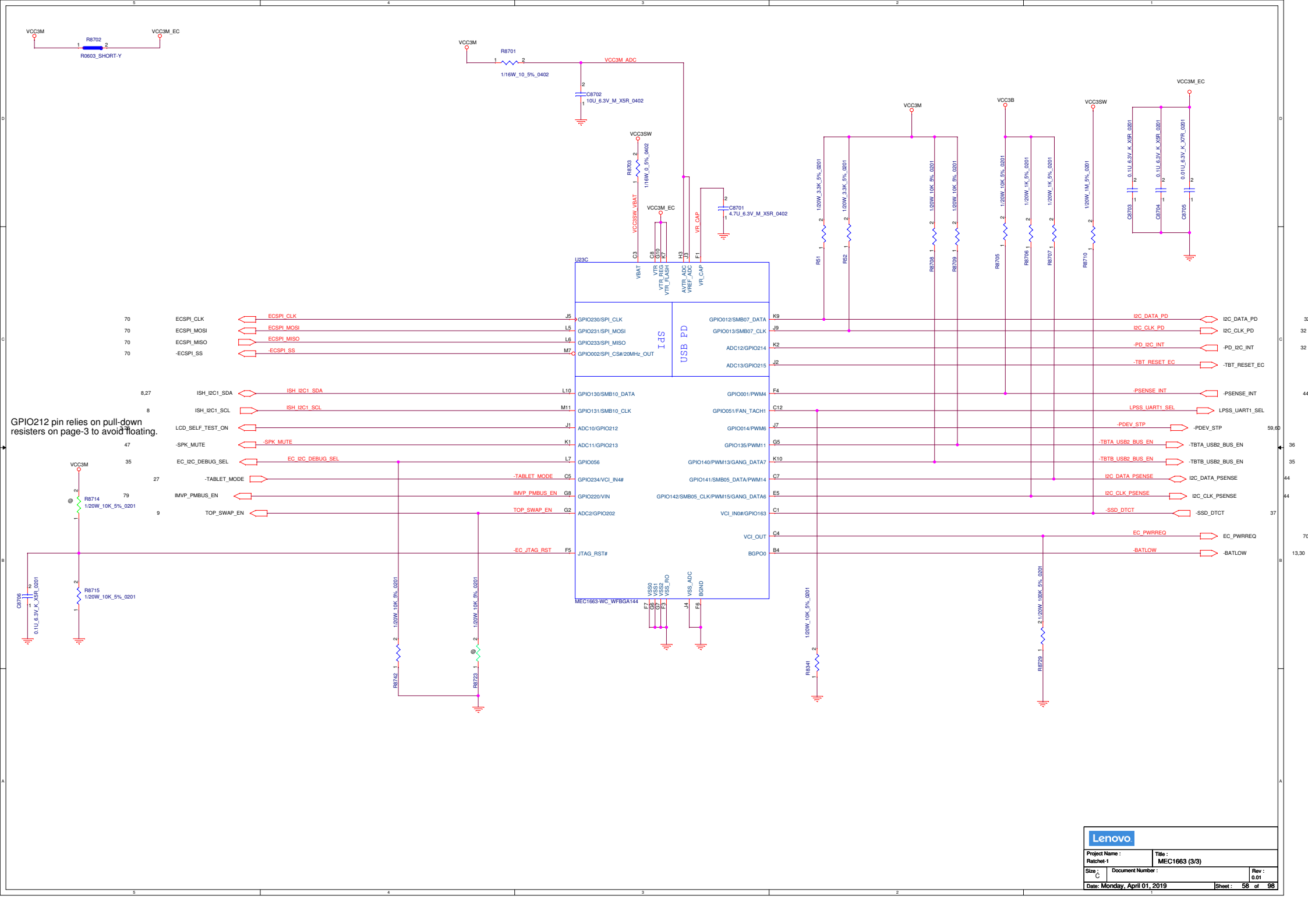

GPIO212 pin relies on pull-down resisters on page-3 to avoid floating.

Project Name : Ratchet-1	Title : MEC1663 (3/3)
Size : C	Document Number :
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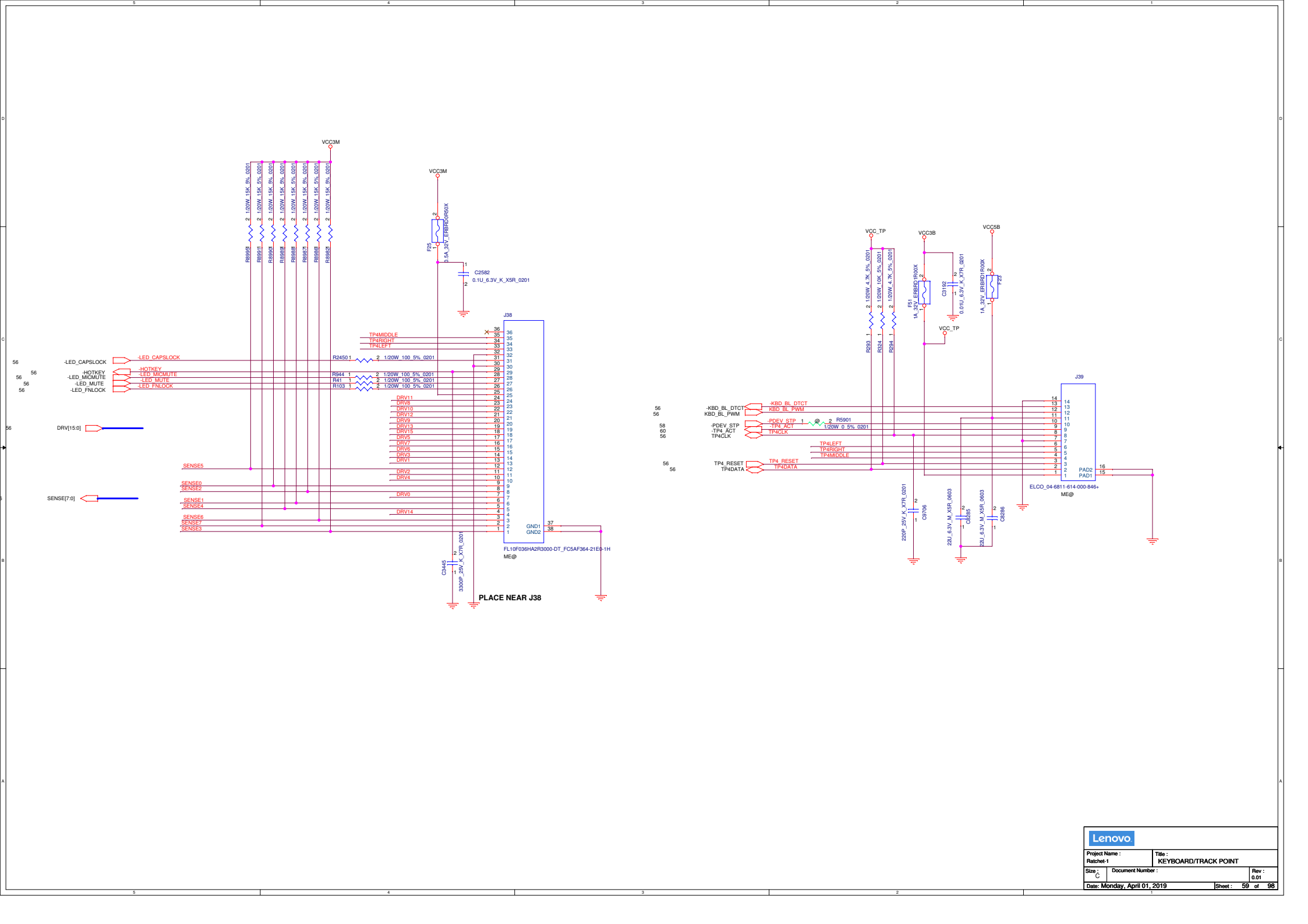

Lenovo		
Project Name : Ratchet-1	Title : KEYBOARD/TRACK POINT	
Size : C	Document Number :	Rev : 0.01
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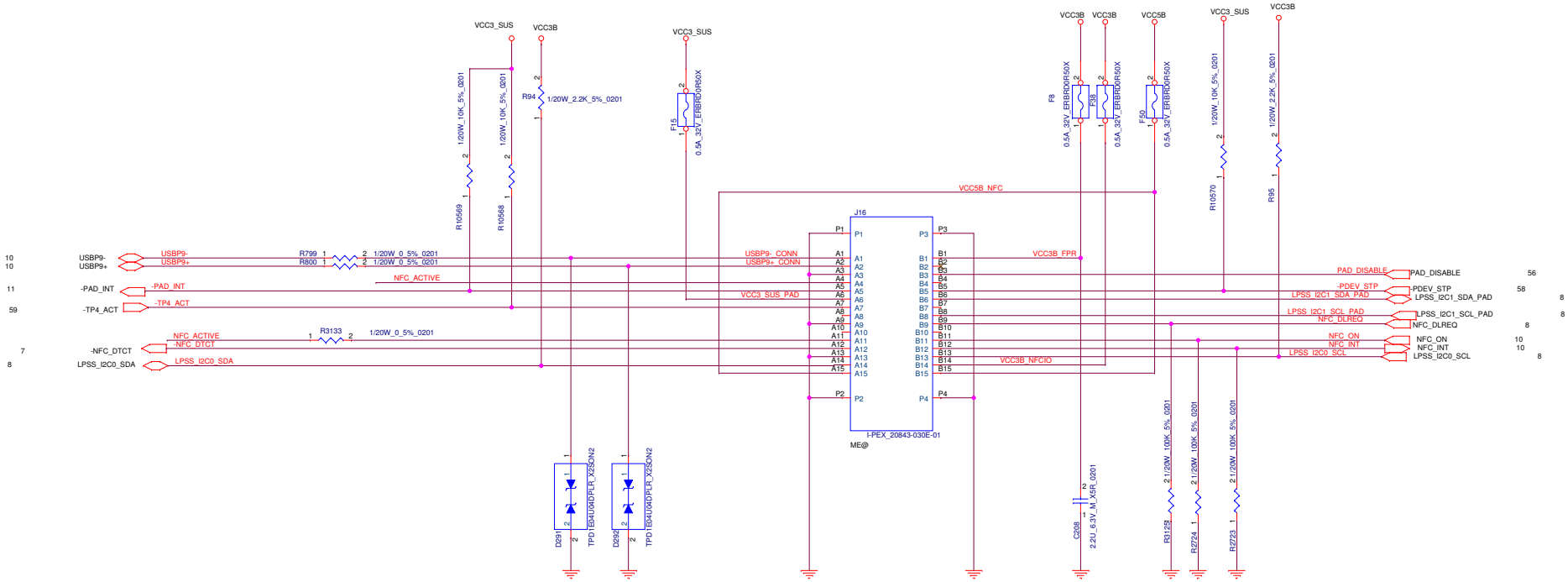

PLACE NEAR J16

Lenovo	
Project Name : Ratchet-1	Title : TOUCH PAD/NFC/FPR
Size : C	Document Number :
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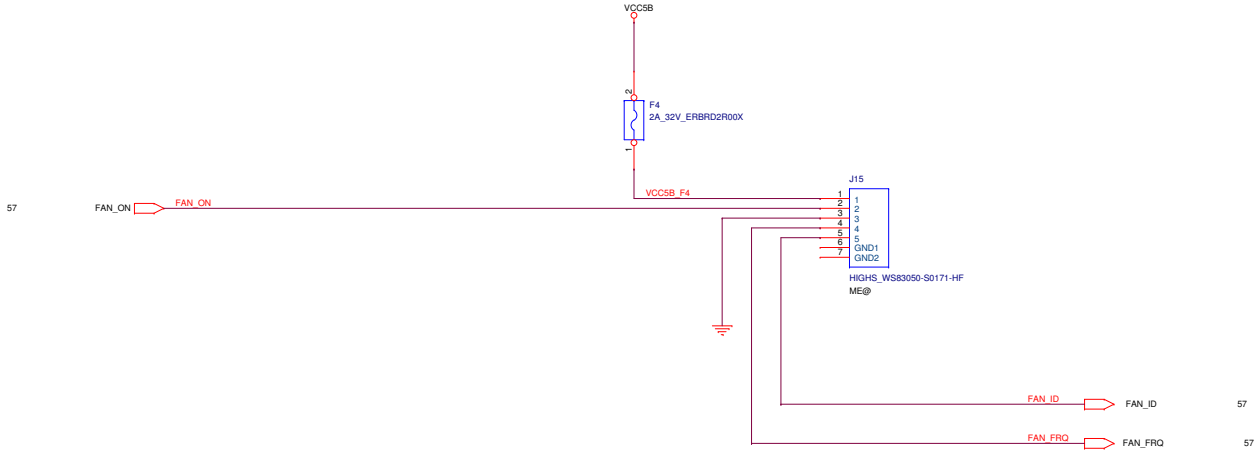

Project Name : Ratchet-1	Title : FAN CONNECTOR
Size : C	Document Number :
Rev : 0.01	
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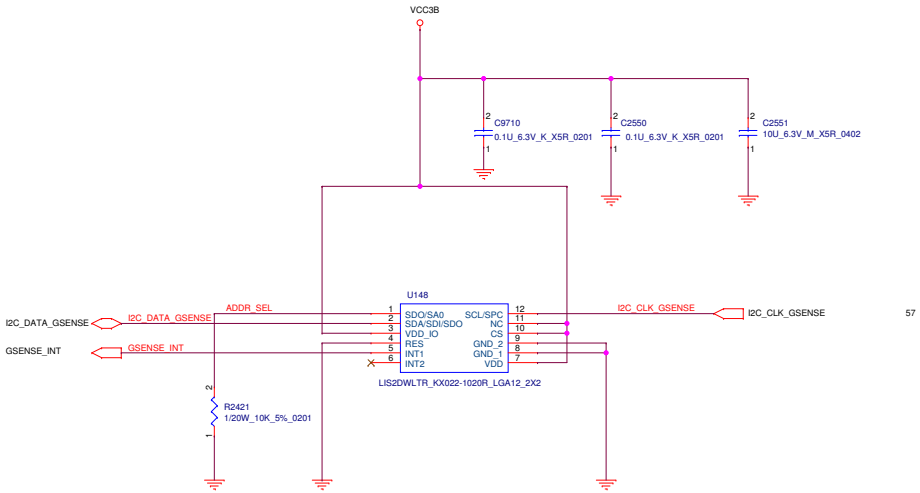
TABLE : G-Sensor Power

HDD Support	**VCC3M**
SSD Only	**VCC3B**

TABLE

P/N	ADDR_SEL	Address
LIS2DWL	**H** **L**	**32h (W) & 33h (R)** **30h (W) & 31h (R)**
KX022-1020	**H** **L**	**3Eh (W) & 3Fh (R)** **3Ch (W) & 3Dh (R)**



I2C_DATA_GSENSE		57
GSENSE_INT		57
I2C_CLK_GSENSE		57

Project Name : Ratchet-1	Title : APS G-SENSOR	
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Project Name : Ratchet-1	Title : BLANK	
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Project Name : Ratchet-1	Title : BLANK	
Size : C	Document Number :	Rev : 0.01
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Project Name : Ratchet-1	Title : BLANK	
Size : C	Document Number :	Rev : 0.01
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Project Name : Ratchet-1	Title : BLANK	
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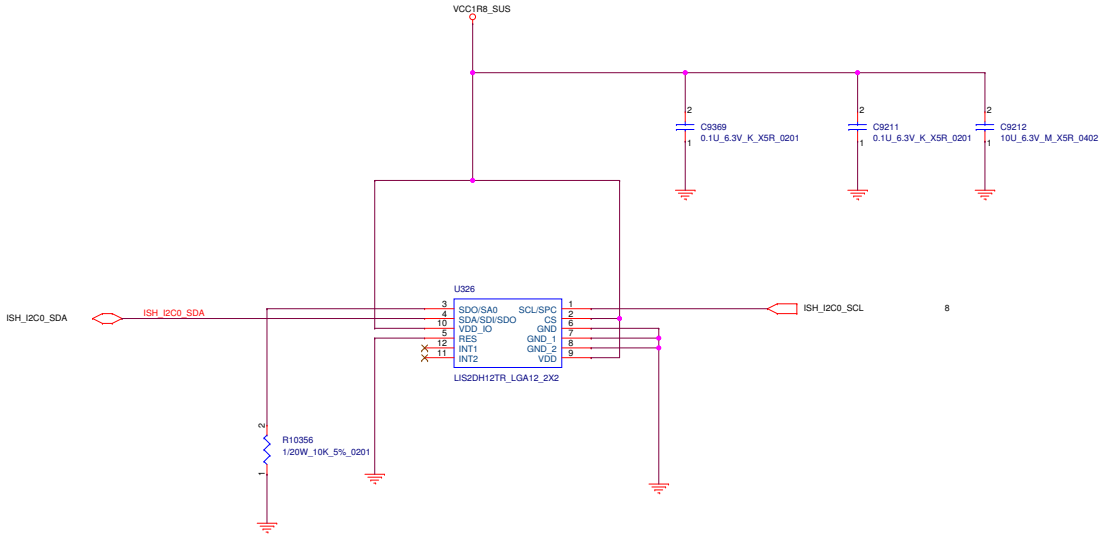
TABLE

P/N	ADDR_SEL	Address
LIS2DH12TR	H	31h (W) & 30h (R)
	L	33h (W) & 32h (R)



Lenovo			
Project Name : Ratchet-1		Title : ISH ACCELEROMETER	
Size : C	Document Number :		Rev : 0.01
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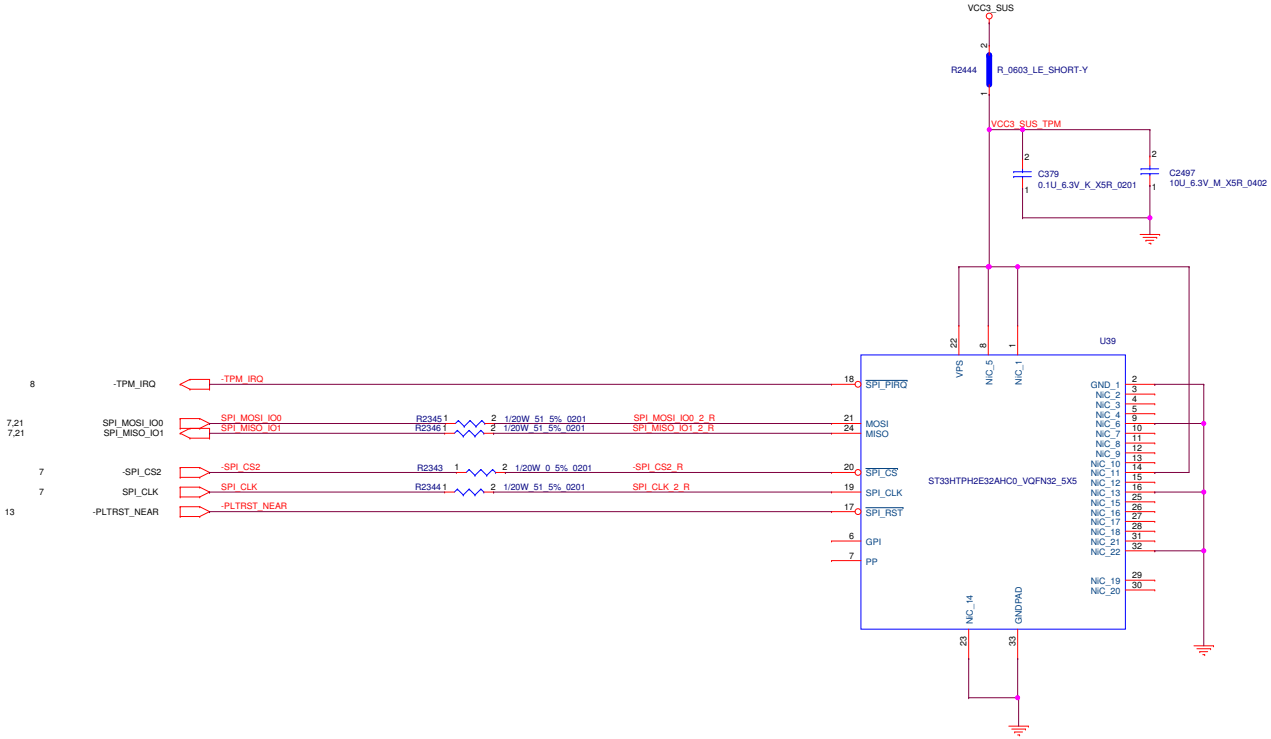

TABLE

Pin No	TCG PTP Spec Rev.01.03.v22	ST Micro ST33HTPH2E32AHC0	Nuvoton NPCT750LABYX
1	VDD/VSB	NC	VSB
2	GND	GND	NC
3	GPIO	NC	NC
4	GPIO	NC	PP/GPIO6
5	NC	NC	NC
6	VNC/GPIO/I2C_PIRQ#	GPIO	GPIO3
7	GPIO/VDD	PP	NC
8	VDD	NC	VHIO
9	GND	NC	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO/I2C_PIRQ#	NC	GPIO4
14	VDD	NC	NC
15	NC	NC	NC
16	GND	NC	GND
17	SPI_RST#	SPI_RST#	PLTRST#
18	SPI_PIRQ#/I2C_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2
19	SPI_CLK	SPI_CLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5
21	MOSI	MOSI	MOSI/GPIO7
22	VDD	VPS	VHIO
23	GND	NC	GND
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	VNC/GPIO	NC	NC
28	VNC/GPIO	NC	NC
29	SDA	NC	SDA/GPIO0
30	SCL	NC	SCL/GPIO1
31	VNC	NC	NC
32	GND	NC	NC

Lenovo

Project Name : Ratchet-1	Title : DISCRETE TPM 2.0
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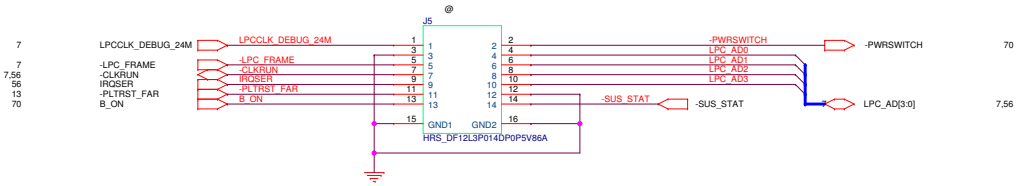
TABLE

REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

LOGIC



Project Name : Ratchet-1	Title : LPC DEBUG PORT
Size : C	Document Number :
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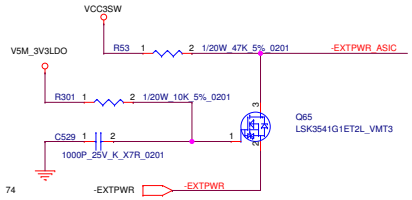

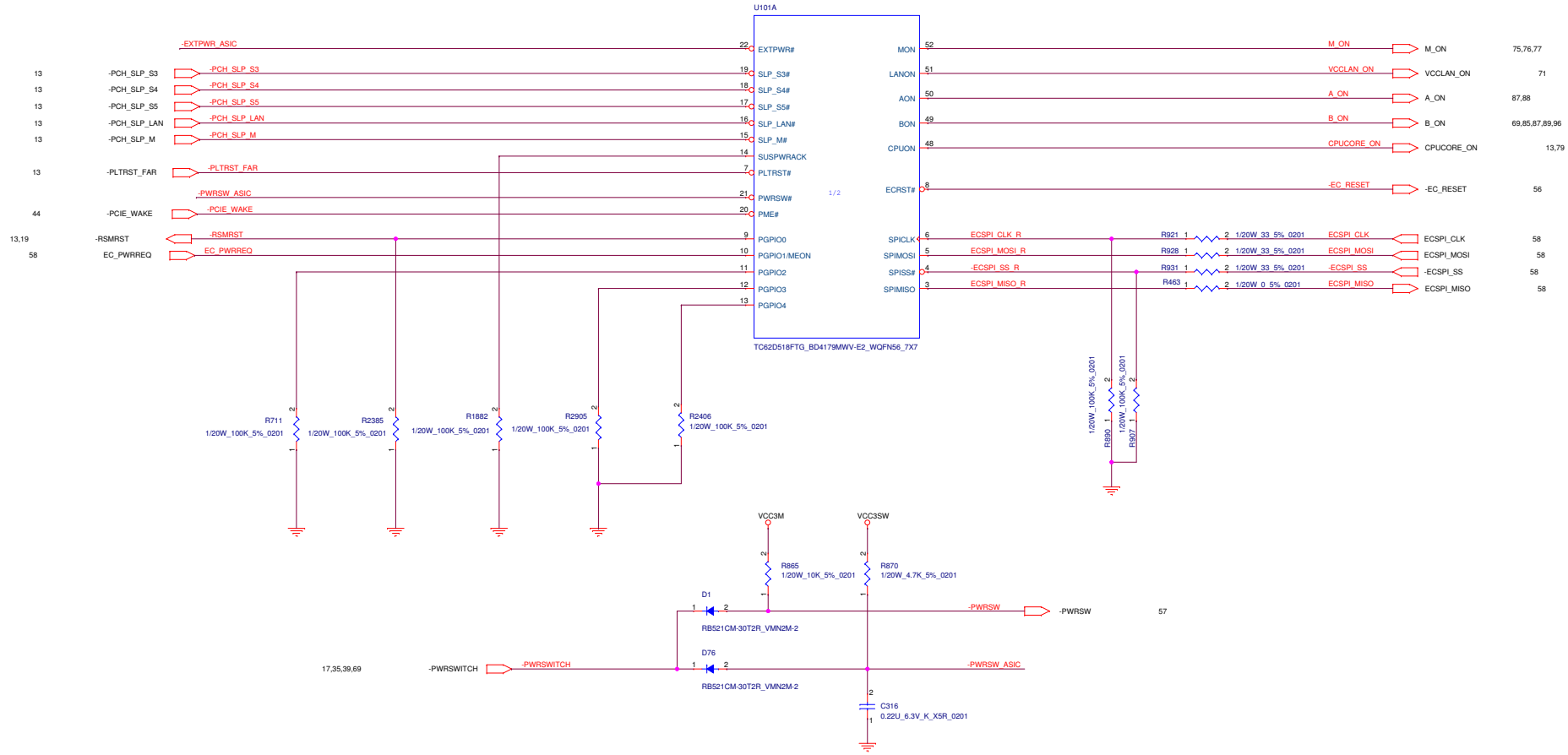

Lenovo		
Project Name : Ratchet-1	Title : THINK ENGINE-3 (1/2)	
Size :	Document Number :	Rev : 0.01
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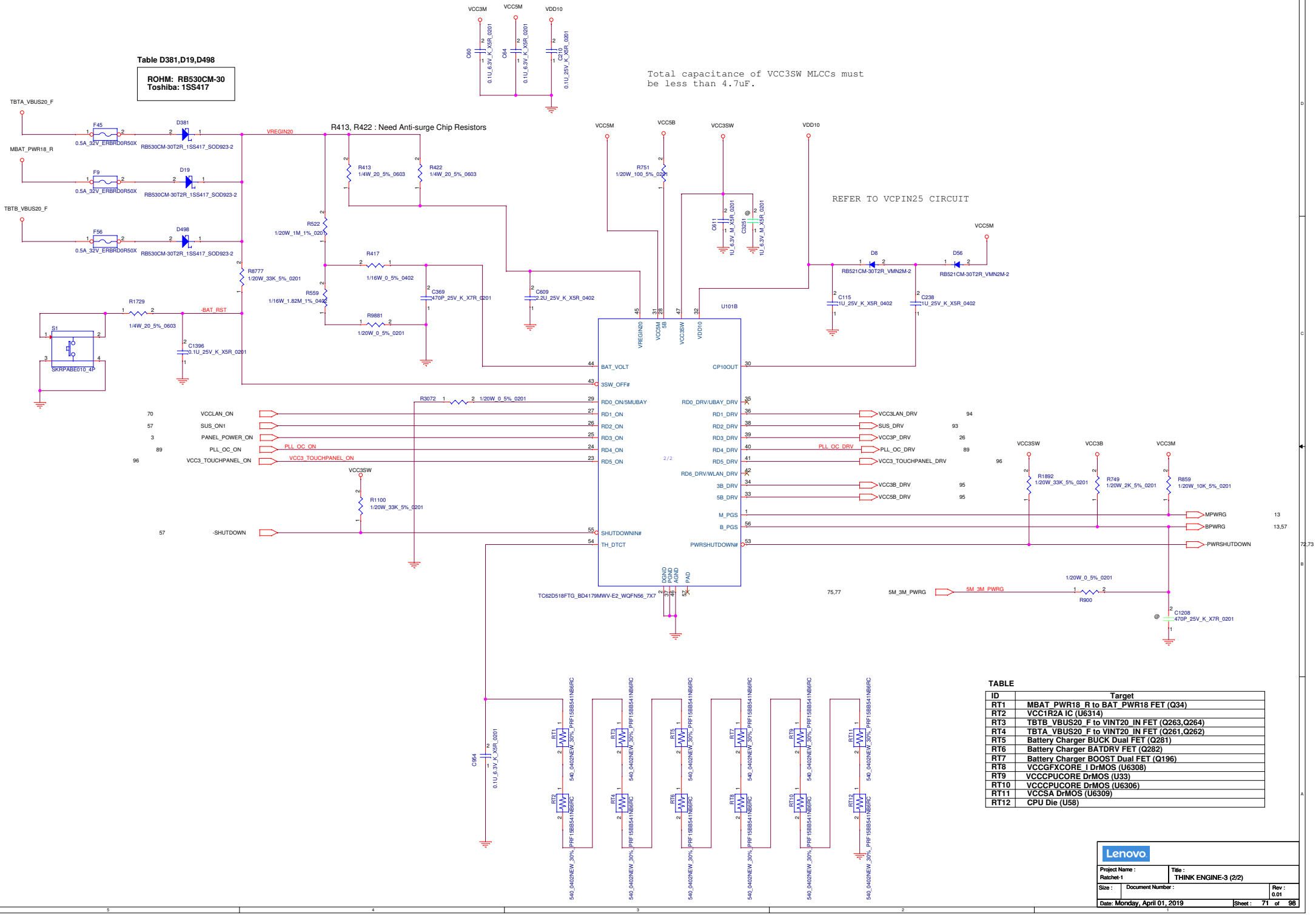

TABLE	
ID	Target
RT1	MBAT_PWR18_R to BAT_PWR18 FET (Q34)
RT2	VCC1R2A IC (U6314)
RT3	TBTB_VBUS20_F to VINT20_IN FET (Q263,Q264)
RT4	TBTA_VBUS20_F to VINT20_IN FET (Q261,Q262)
RT5	Battery Charger BUCK Dual FET (Q281)
RT6	Battery Charger BATDRV FET (Q282)
RT7	Battery Charger BOOST Dual FET (Q196)
RT8	VCCGFXCORE_I DrMOS (U6308)
RT9	VCCCPUCORE DrMOS (U33)
RT10	VCCCPUCORE DrMOS (U6306)
RT11	VCCSA DrMOS (U6309)
RT12	CPU Die (U58)

Lenovo

Project Name : Ratchet-1	Title : THINK ENGINE-3 (2/2)
Size :	Document Number : Rev : 0.01
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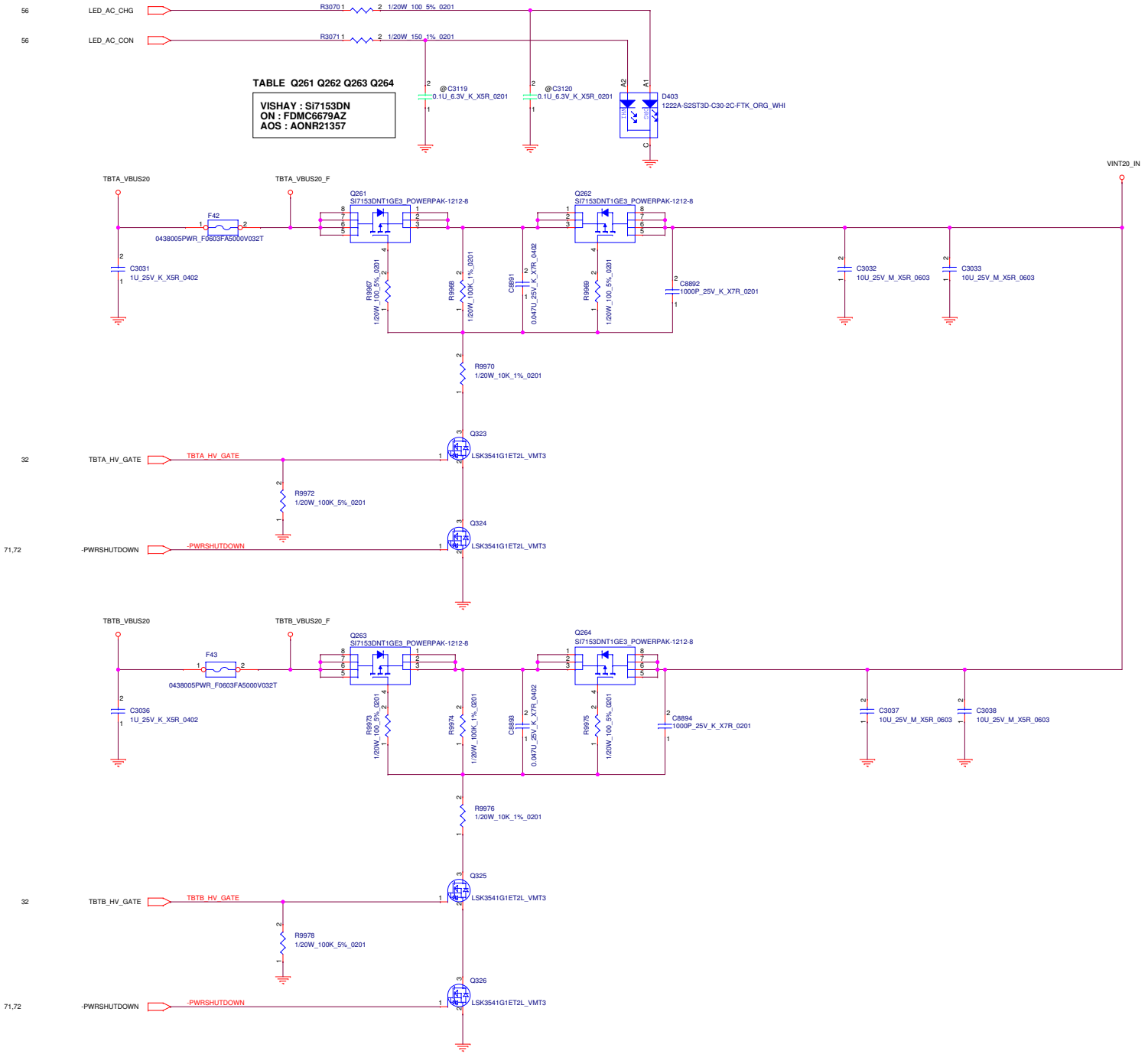

Lenovo			
Project Name : Ratchet-1		Title : DC-IN	
Size : C	Document Number :		Rev : 0.01
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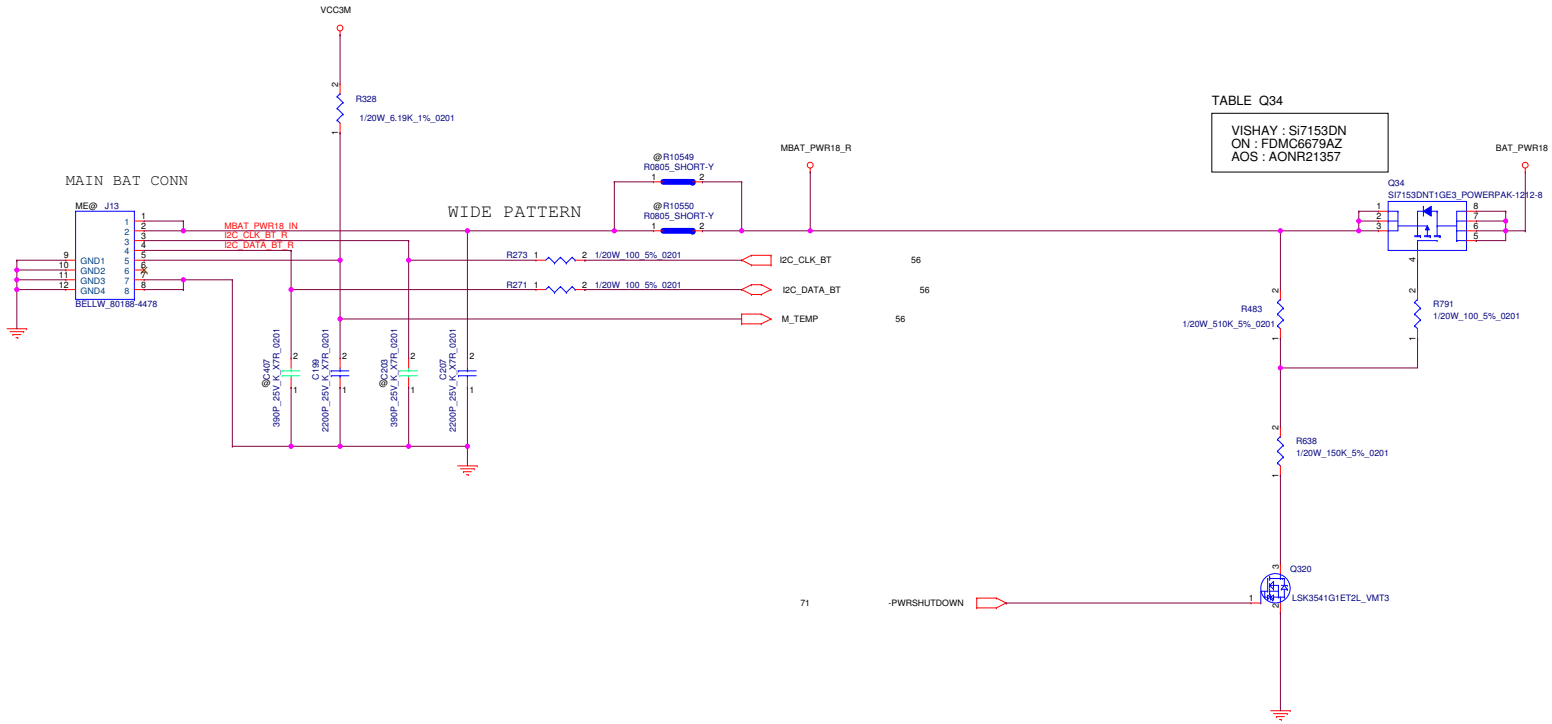

Lenovo		
Project Name : Ratchet-1	Title : BATTERY INPUT	
Size : C	Document Number :	Rev : 0.01
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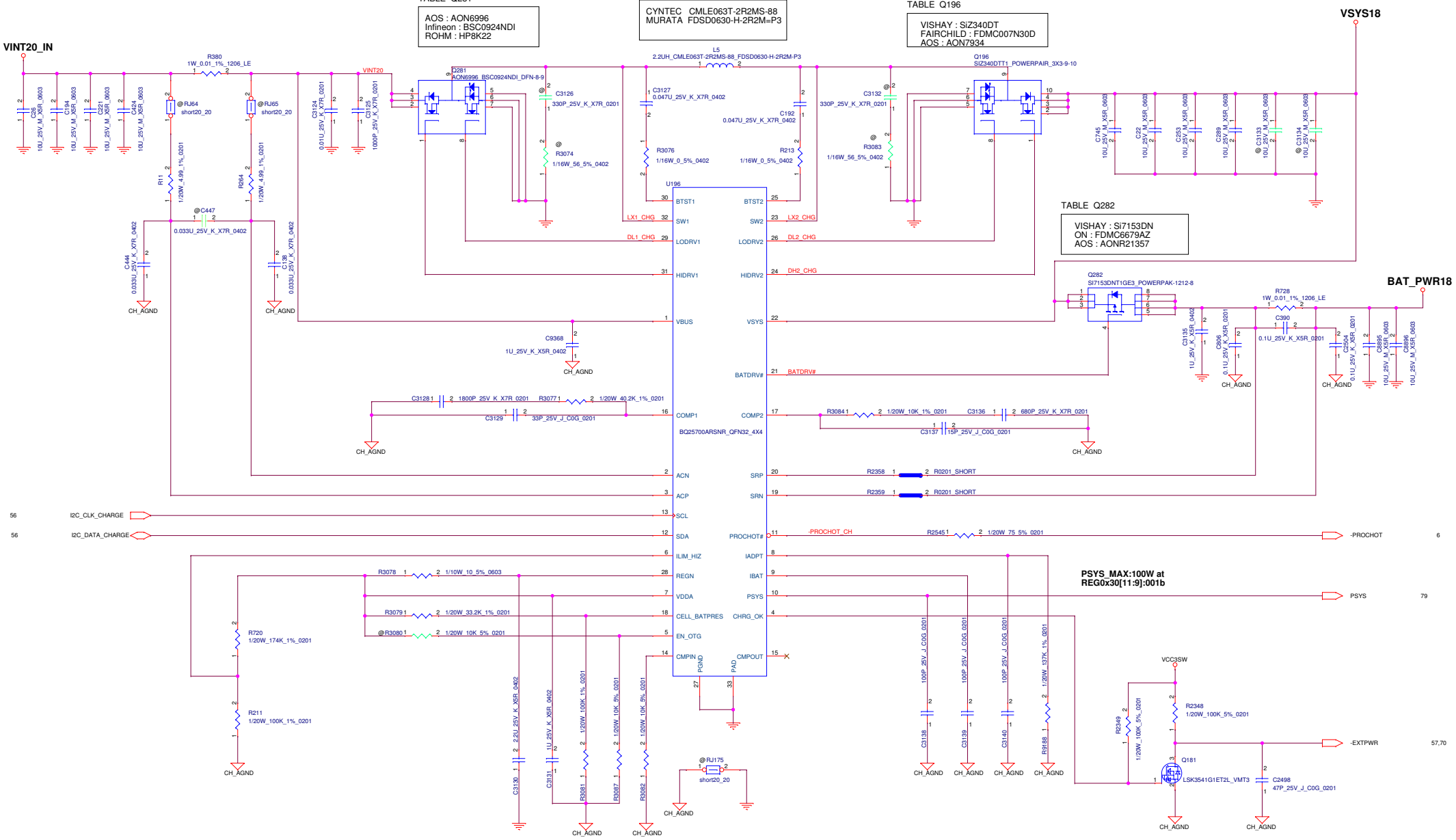

TABLE : ILIM_HIZ

IDPM	V (ILIM)	
500mA	1.2V	
1.0A	1.4V	
1.5A	1.6V	
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

← LOGIC

TABLE : CELL_BATPRES

# of CELL	V (CELL_PRES)	R3079
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

← LOGIC

TABLE

Inductor	R(IADP)	fsw@POR
1.0uH	93kohm	800kHz
2.2uH	137kohm	800kHz
3.3uH	169kohm	800kHz

← LOGIC

Project Name : Ratchet-1	Title : BATTERY CHARGER (BQ25700A)
Size :	Document Number : Rev : 0.01
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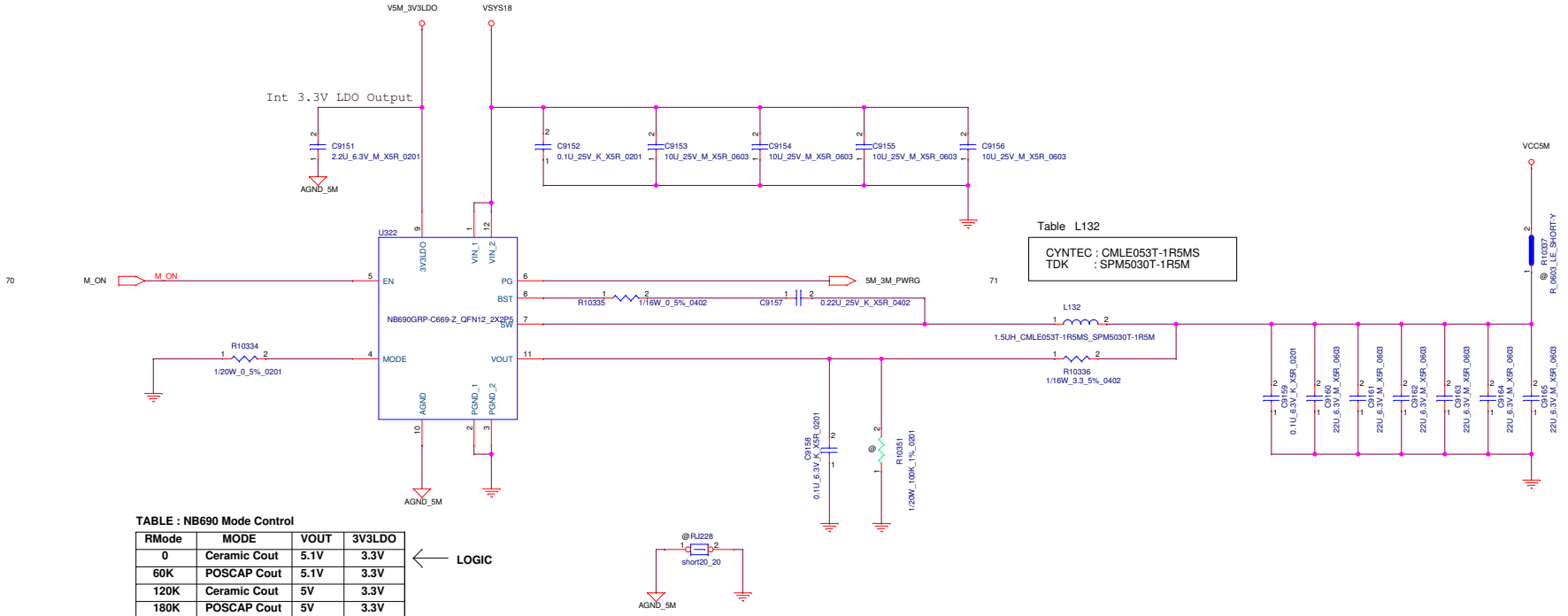

Table L132

CYNTEC :	CMLE053T-1R5MS
TDK :	SPM5030T-1R5M

TABLE : NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

← LOGIC

Lenovo			
Project Name : Ratchet-1		Title : DC/DC VCC5M (NB690)	
Size : C	Document Number :		Rev : 0.01
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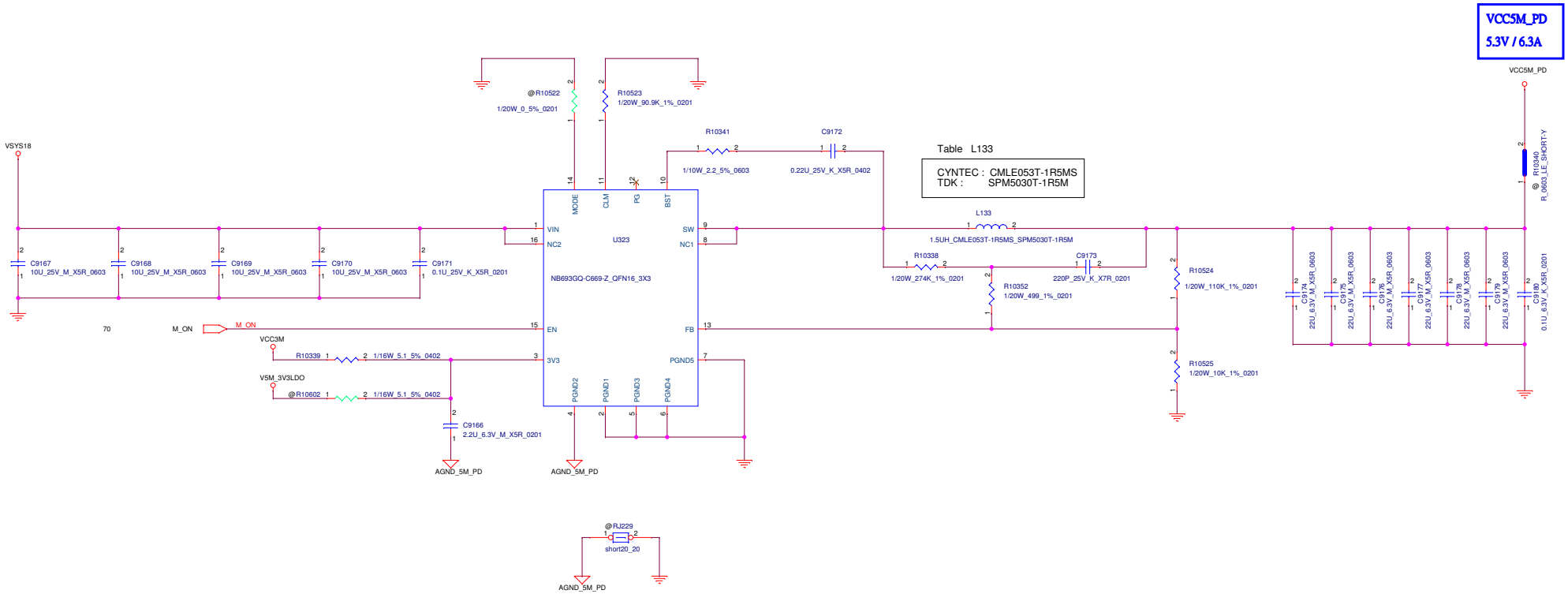

Lenovo		
Project Name : Ratchet-1	Title : DC/DC VCC5M_PD (NB690)	
Size : C	Document Number :	Rev : 0.01
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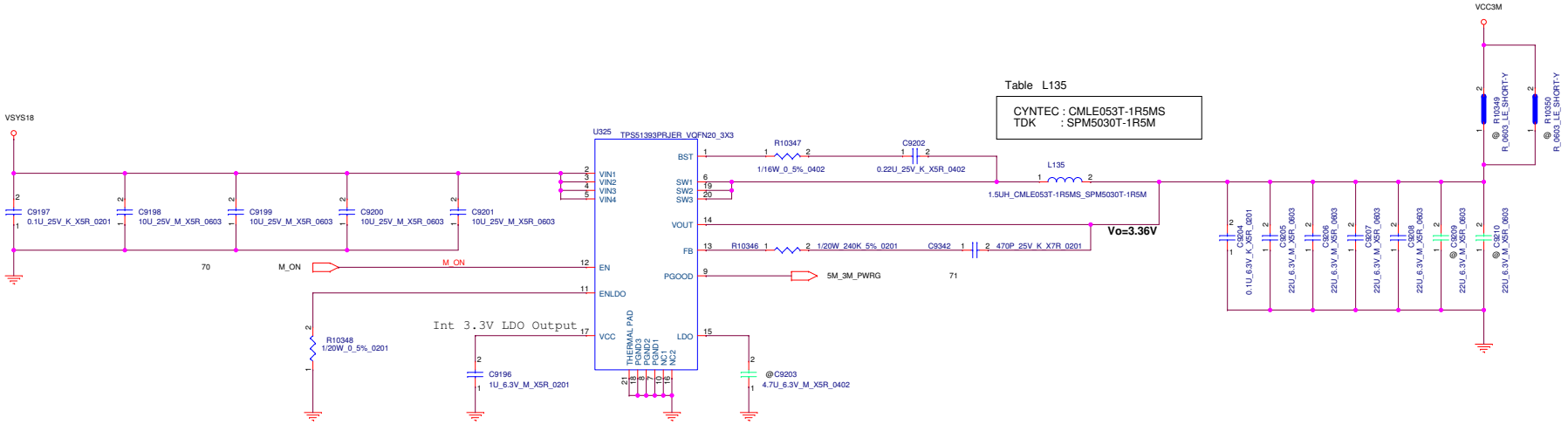

Table L135

CYNTEC	CMLE053T-1R5MS
TDK	SPM5030T-1R5M

Lenovo			
Project Name : Ratchet-1		Title : DC/DC VCC3M (NB690)	
Size : C	Document Number :		Rev : 0.01
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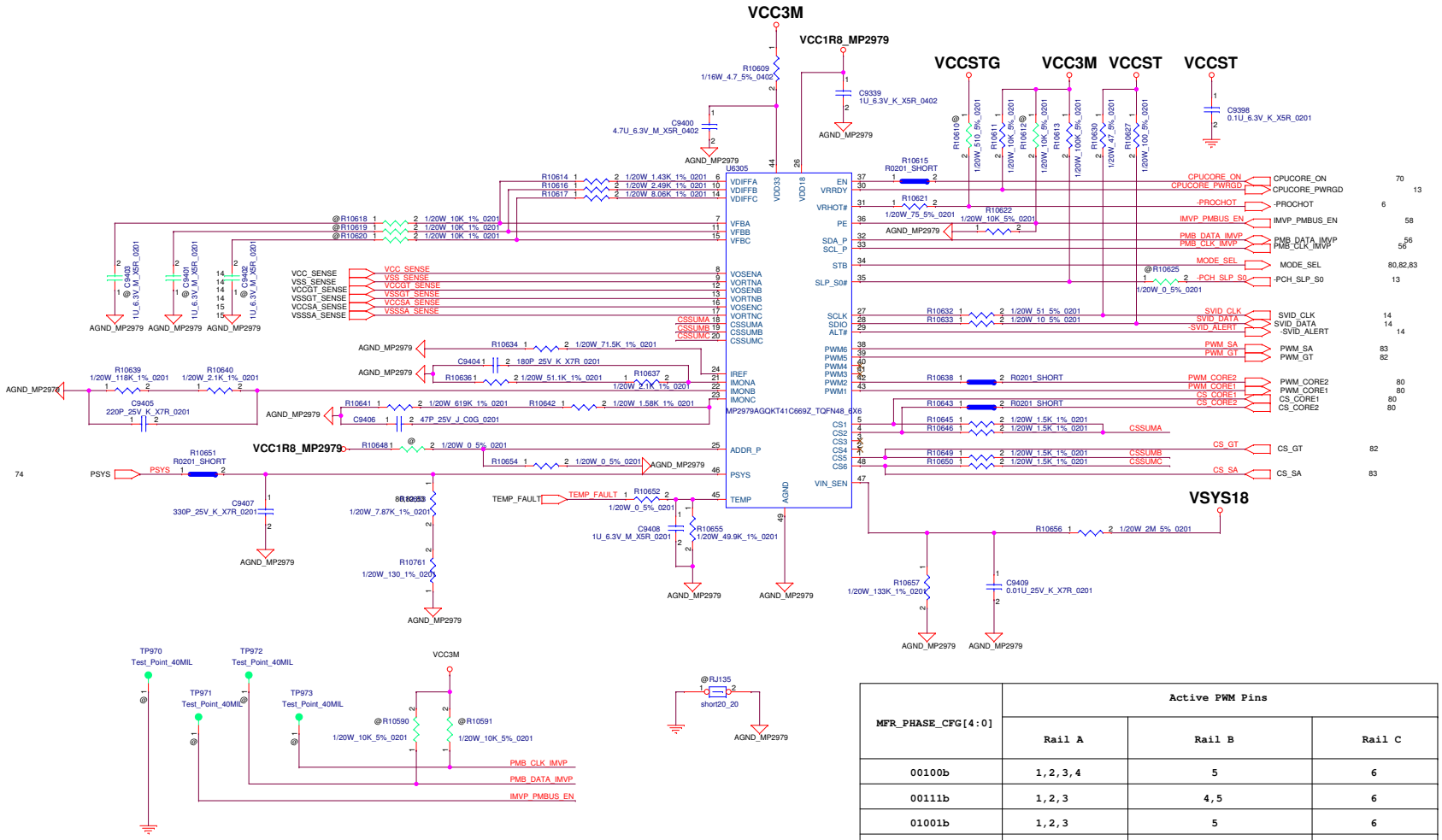
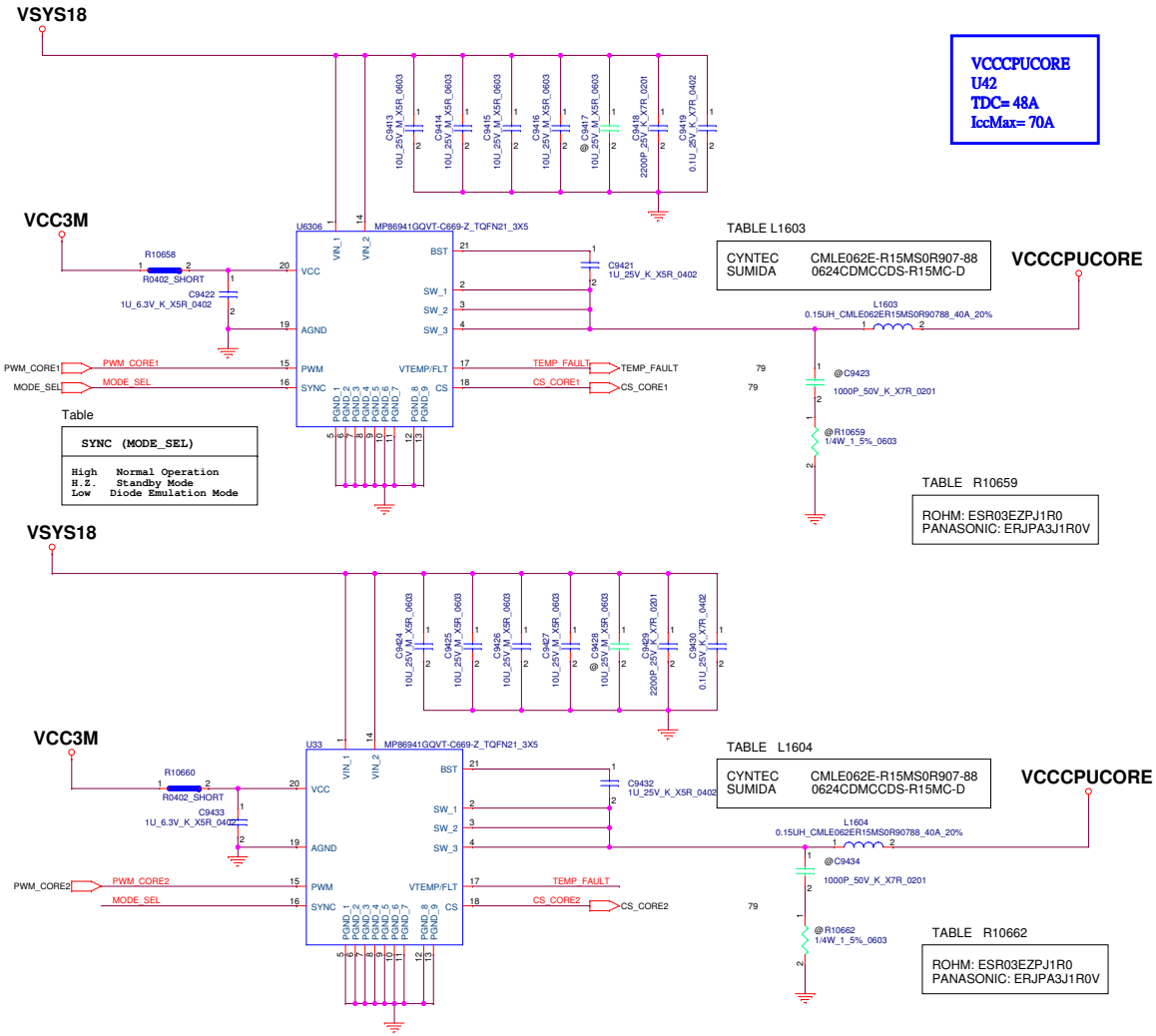
Project Name : Ratchet-1	Title : BLANK	
Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 78 of 98	



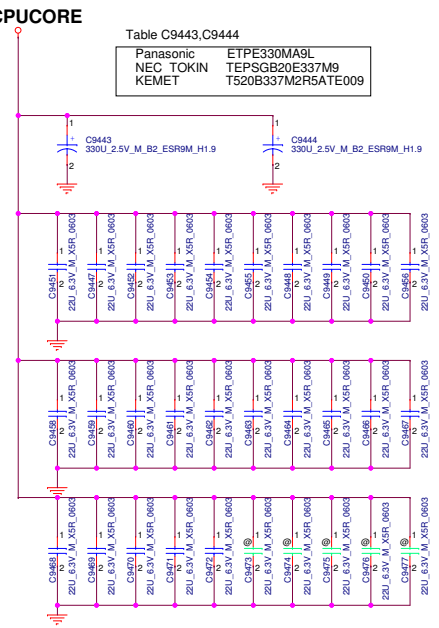
MFR_PHASE_CFG[4:0]	Active PWM Pins		
	Rail A	Rail B	Rail C
00100b	1,2,3,4	5	6
00111b	1,2,3	4,5	6
01001b	1,2,3	5	6
01100b	1,2	4,5	6
01110b	1,2	5	6
10001b	1	5	6

← LOGIC

Project Name : Ratchet-1	Title : DC/DC IMVP8 (MP2979AGQKT)
Size : C	Document Number :
Rev : 0.01	
Date: Monday, April 01, 2019	Sheet : 79 of 98



2pcs 330uF + 25pcs for WHL U42 VCCCPUCORE



Lenovo			
Project Name : Ratchet-1		Title : DC/DC VCCCPUCORE (MP86941 X 2)	
Size :	Document Number :		Rev : 0.01
Date: Monday, April 01, 2019		Sheet : 80 of 98	

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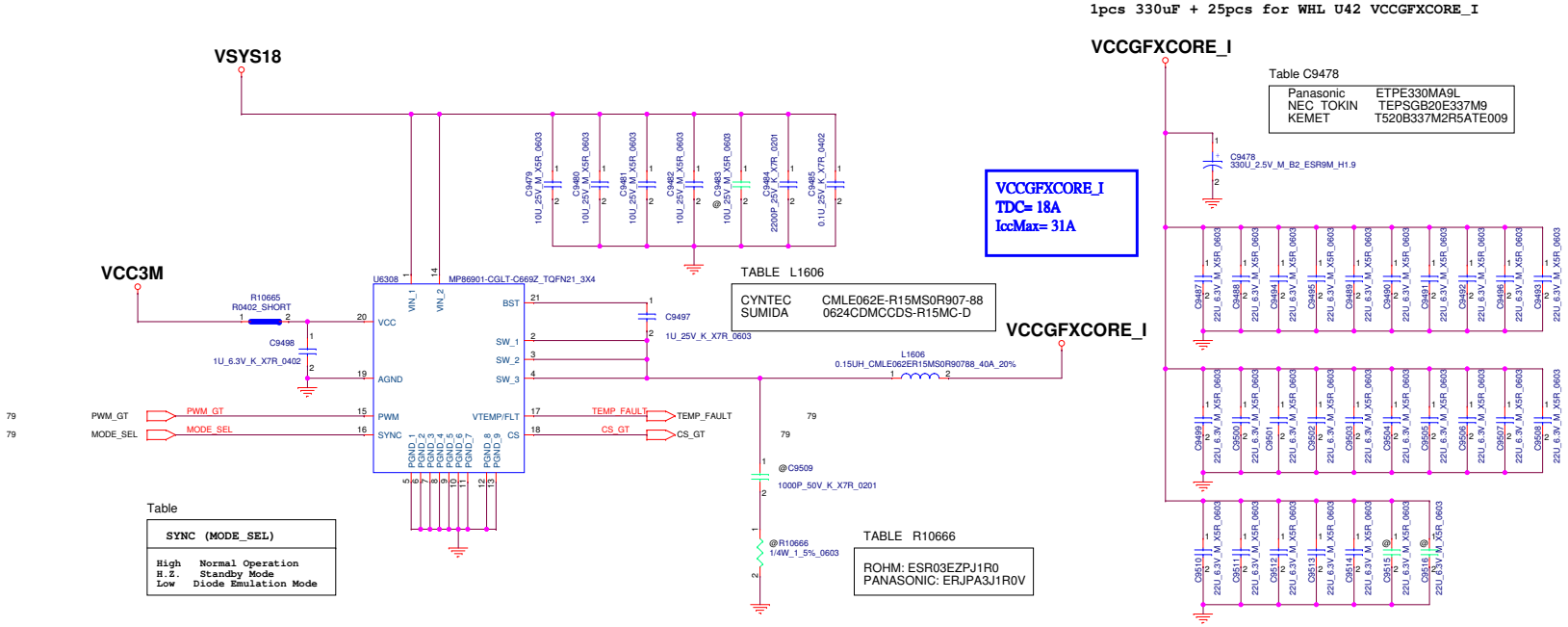
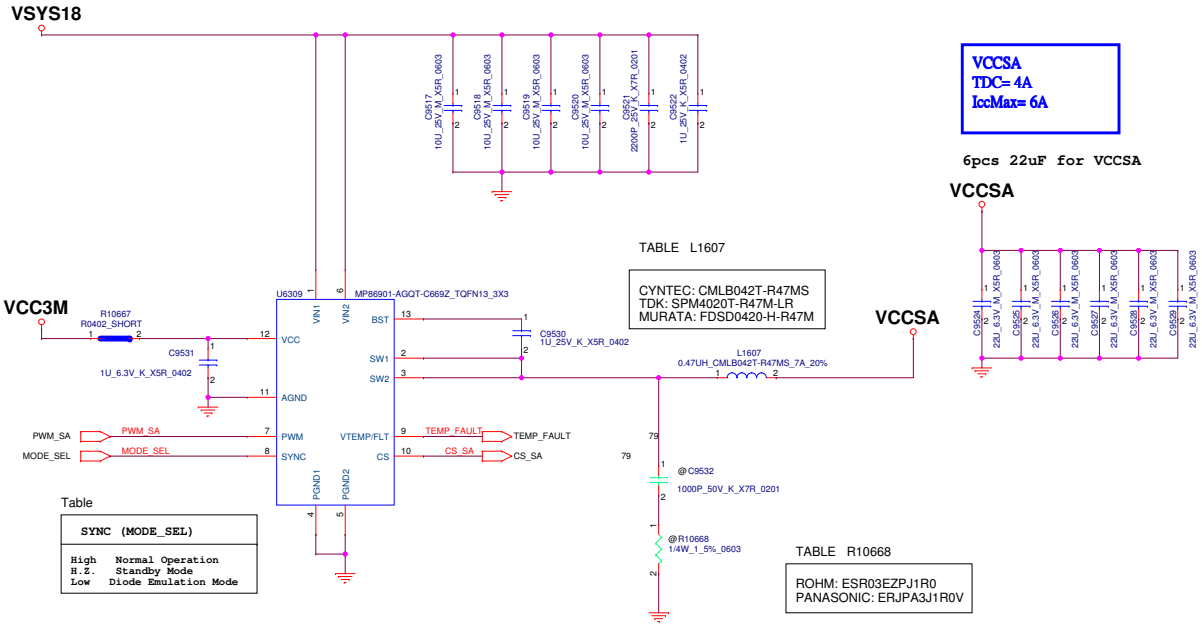
Project Name : Ratchet-1	Title : BLANK	
Size :	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 81 of 98	



Project Name : Ratchet-1	Title : DC/DC VCCGFXCORE_I (MP86901C)
Size :	Document Number : / Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 82 of 98



Project Name : Ratchet-1	Title : DC/DC VCCSA (MP86901A)
Size :	Document Number : Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 83 of 98

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Project Name : Ratchet-1	Title : BLANK	
Size :	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 84 of 98	

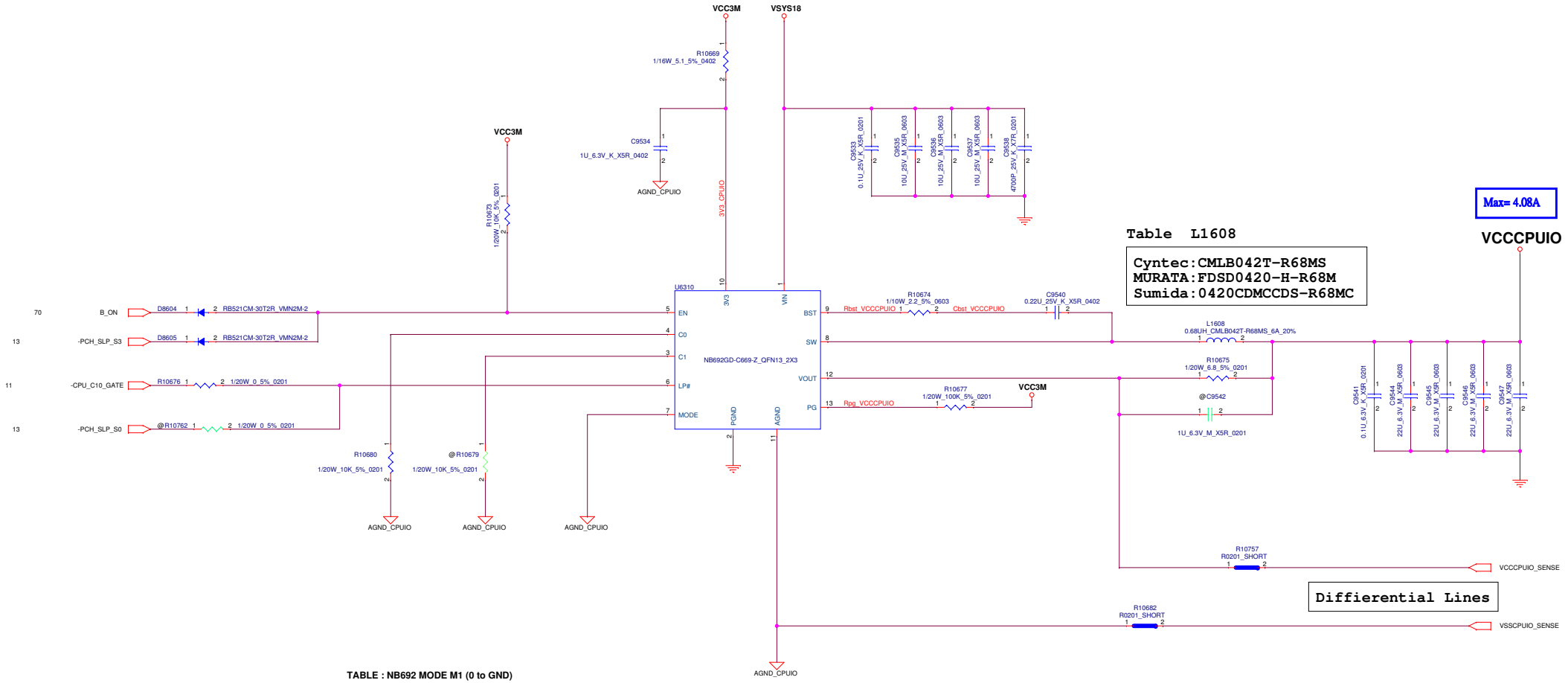

TABLE : NB692 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	← SLP_S0#
1	0	0	0.850V	
1	0	1	0.875V	
1	1	0	0.950V	← LOGIC
1	1	1	0.975V	

Project Name : Ratchet-1	Title : DC/DC VCCCPUIO(NB692)
Size :	Document Number : Rev : 0.01
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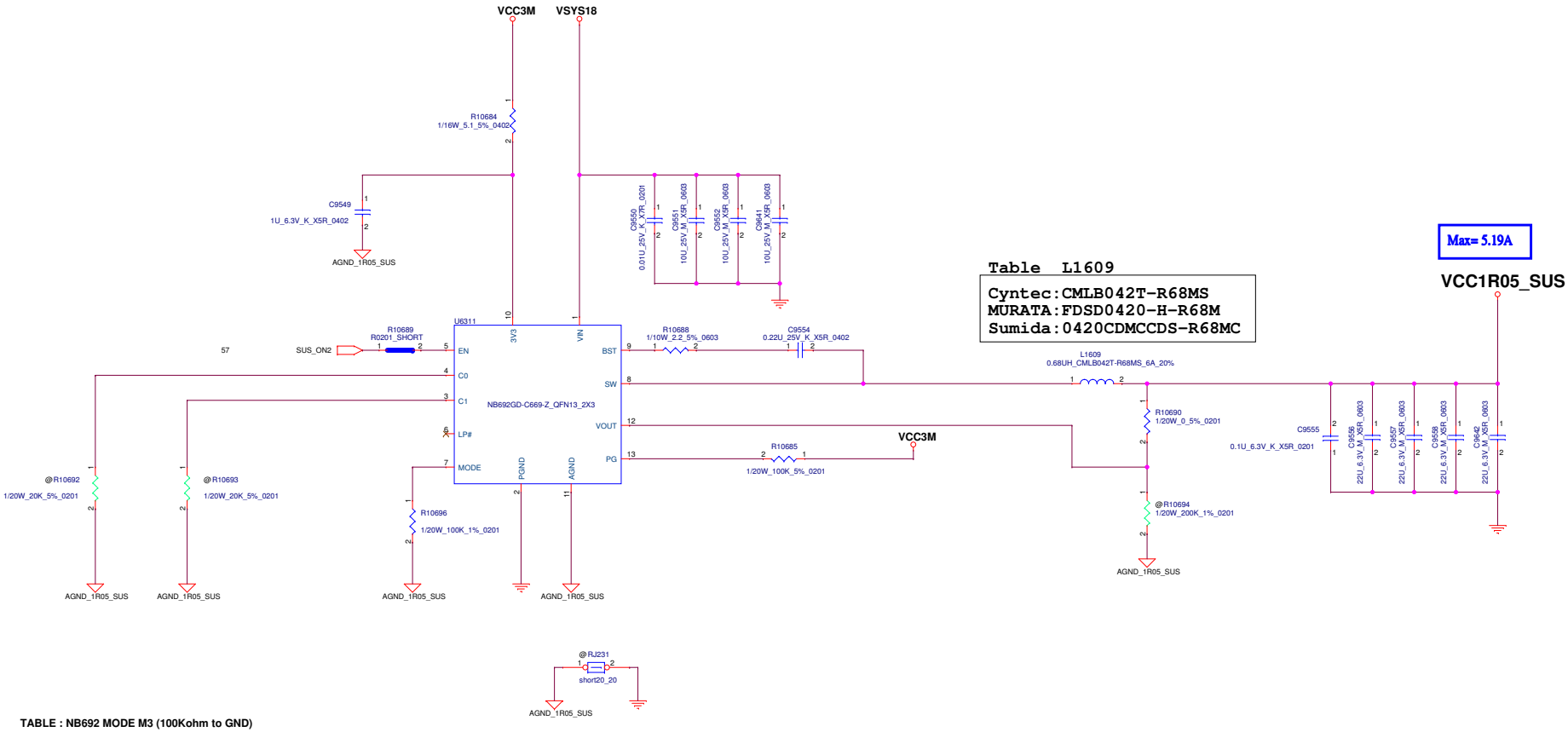


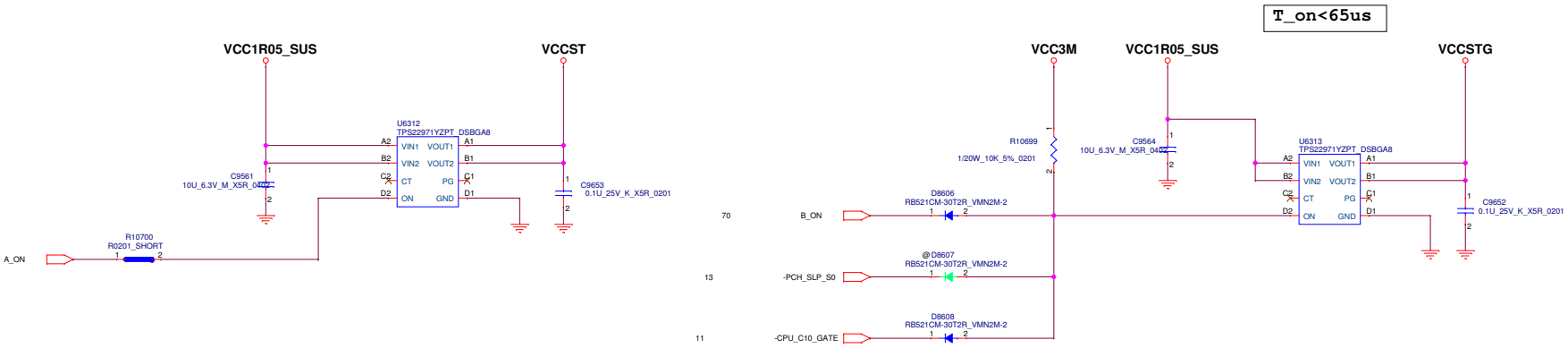
Table L1609

Cyntec:CMLB042T-R68MS
MURATA:FDSD0420-H-R68M
Sumida:0420CDMCCDS-R68MC

TABLE : NB692 MODE M3 (100Kohm to GND)

LP#	C1	C0	VOUT(V)	
0	X	X	0V	
1	0	0	0.8V	
1	0	1	0.95V	
1	1	0	1V	
1	1	1	1.05V	← Default Value

Project Name : Ratchet-1	Title : DC/DC VCC1R05_SUS (NB692)	
Size :	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 86 of 98	



Project Name : Ratchet-1	Title : LOAD SW VCCST & VCCSTG
Size :	Document Number : Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 87 of 98

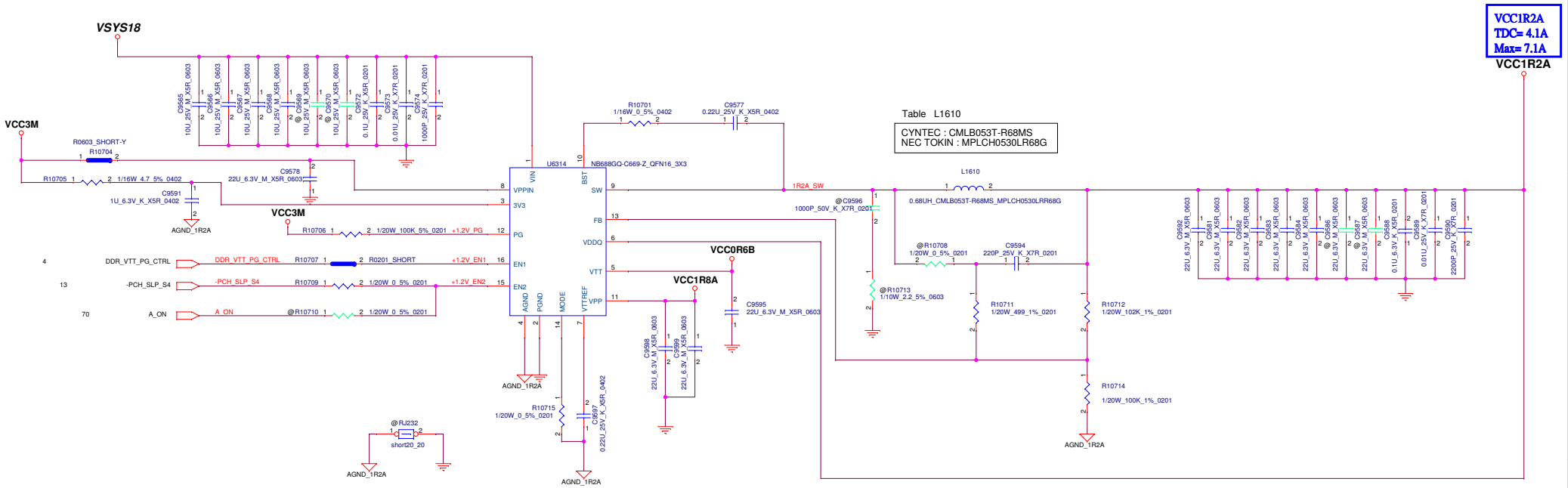


TABLE NB688BGQ:EN1/EN2

State	EN1	EN2	VDDQ	VTTREF	VTT	VPP
S0	High	High	ON	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)	ON
S4/S5	Low	Low	OFF	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF	OFF

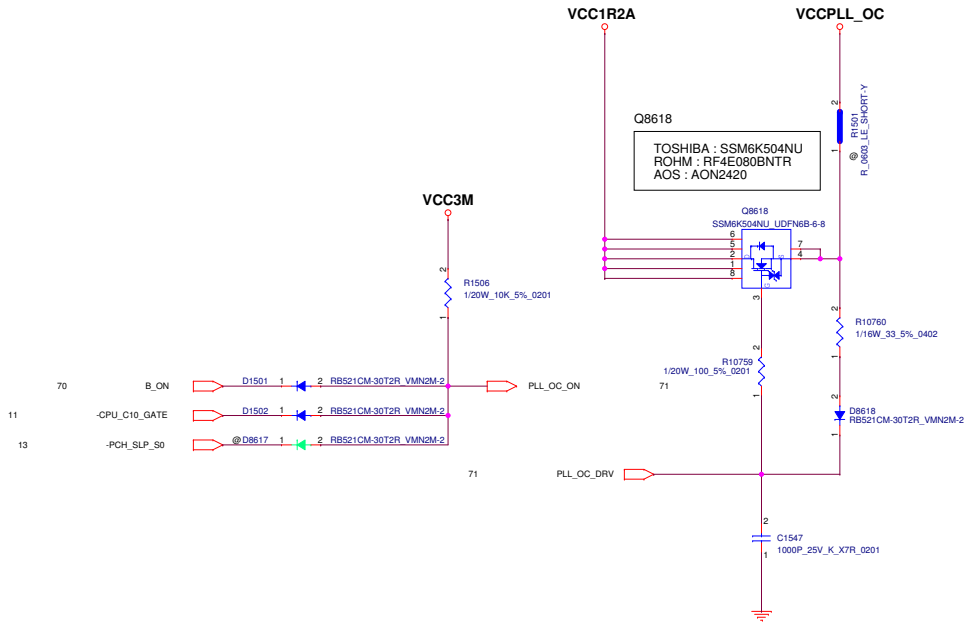
TABLE NB688BGQ:MODE

State	USM	Fs	Resistor to GND
M1	NO	700KHz	0
M2	YES	700KHz	90K
M3	NO	500KHz	150K
M4	YES	500KHz	>230K or Float

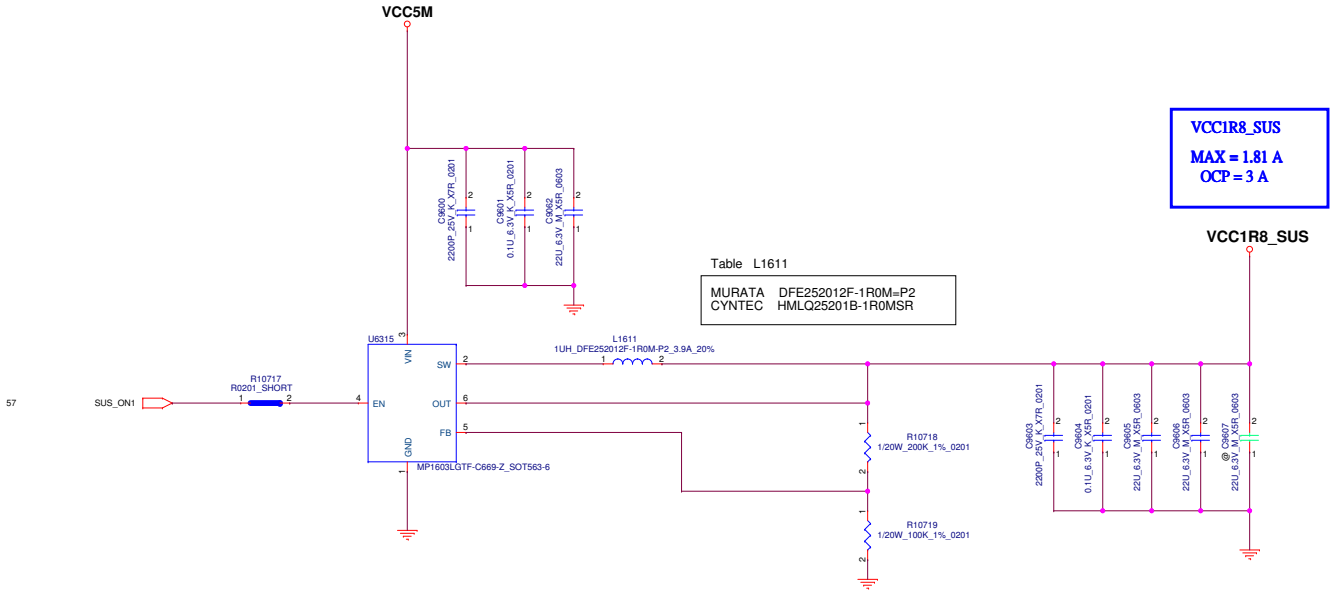
← LOGIC

Lenovo

Project Name : Ratchet-1	Title : DC/DC VCC1R2A/0R6B/1R8A(NB688)
Size :	Document Number : Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 88 of 98



Project Name : Ratchet-1	Title : LOAD SW VCCPLL_OC
Size : C	Document Number :
Date: Monday, April 01, 2019	Sheet : 89 of 98



Project Name : Ratchet-1	Title : DC/DC VCC1R8_SUS (MP1603L)
Size : C	Document Number :
Date: Monday, April 01, 2019	Sheet : 90 of 98
	Rev : 0.01

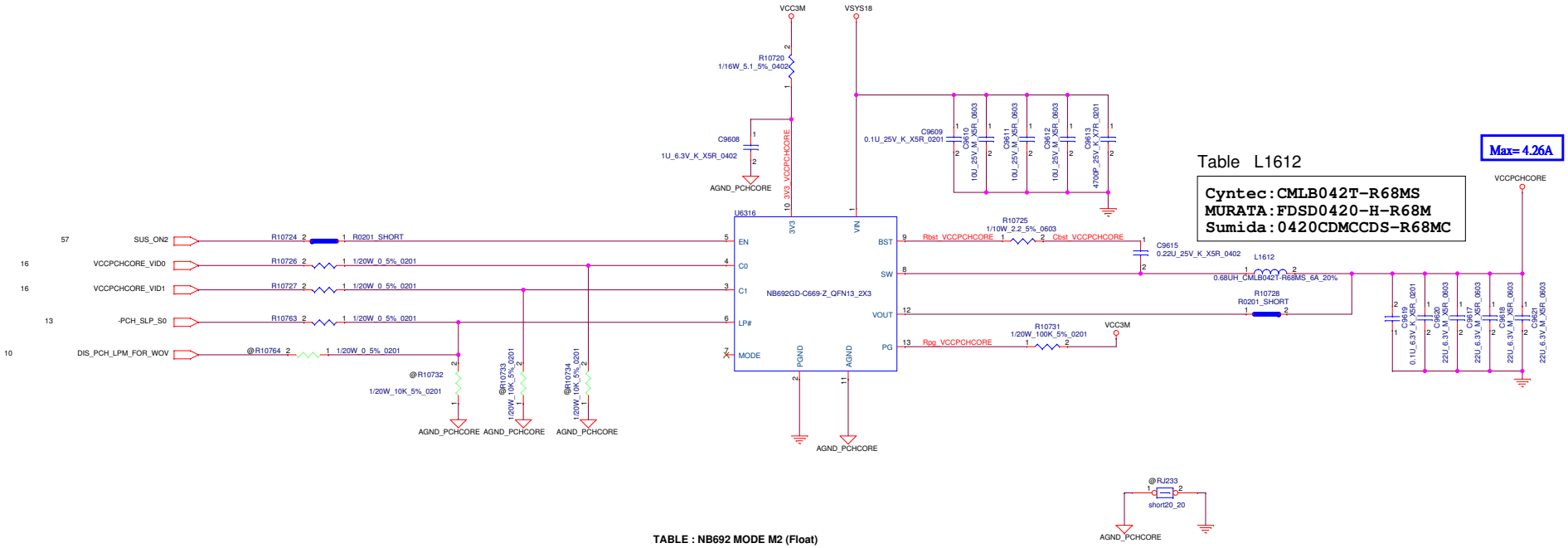


Table L1612

Cyntec:CMLB042T-R68MS
MURATA:FDSD0420-H-R68M
Sumida:0420CDMCCDS-R68MC

Max= 4.26A

TABLE : NB692 MODE M2 (Float)

LP#	C1	C0	VOUT	
0	X	X	0.75V	← SLP_S0#
1	0	0	0.90V	
1	0	1	0.95V	
1	1	0	1.00V	
1	1	1	1.05V	← DEFAULT

Lenovo

Project Name : Ratchet-1	Title : DC/DC VCCPCHCORE(NB692)
Size : C	Document Number :
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Project Name : Ratchet-1	Title : BLANK
Size : C	Document Number :
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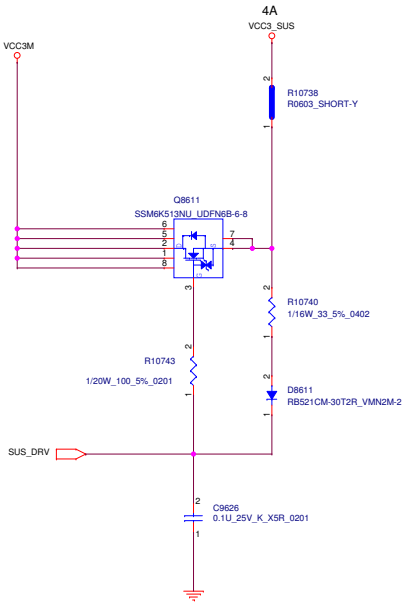
Q8611

TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD : FDMA8878



Project Name : Ratchet-1	Title : LOAD SW PCH SUS	
Size :	Document Number :	Rev : 0.01
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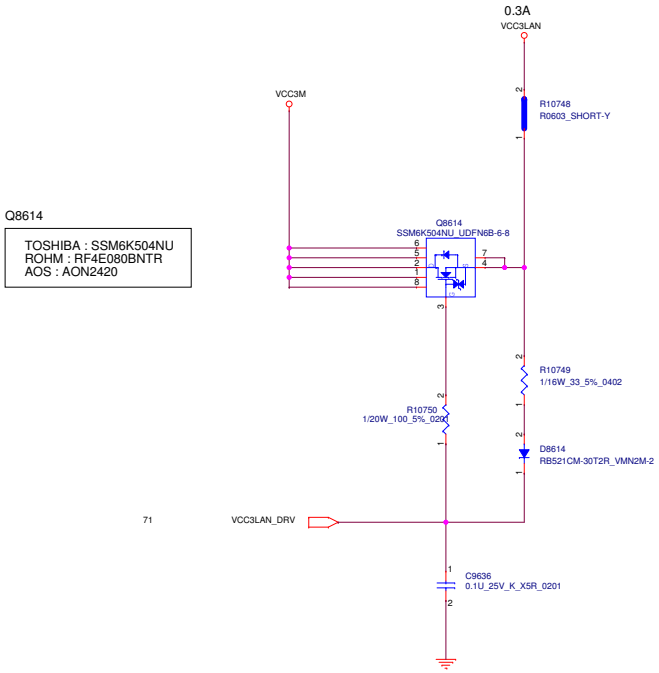


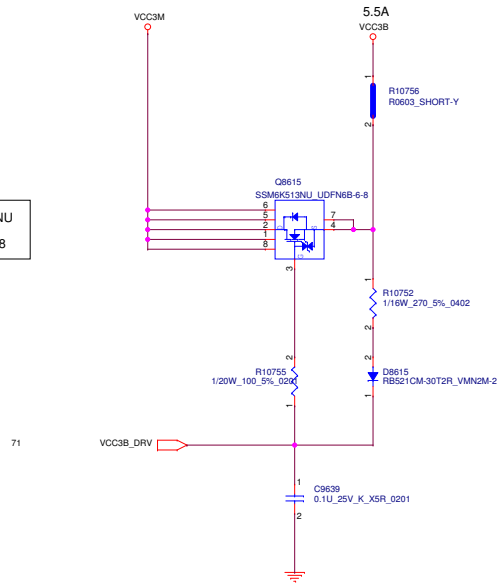
Q8614

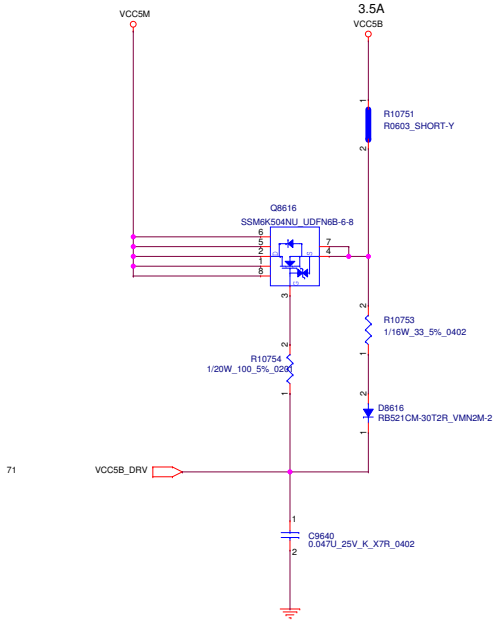
TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420

Project Name : Ratchet-1		Title : LOAD SW LAN	
Size :	Document Number :		Rev : 0.01
Date: Monday, April 01, 2019		Sheet : 94 of 98	

Q8615

TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD : FDMA8878

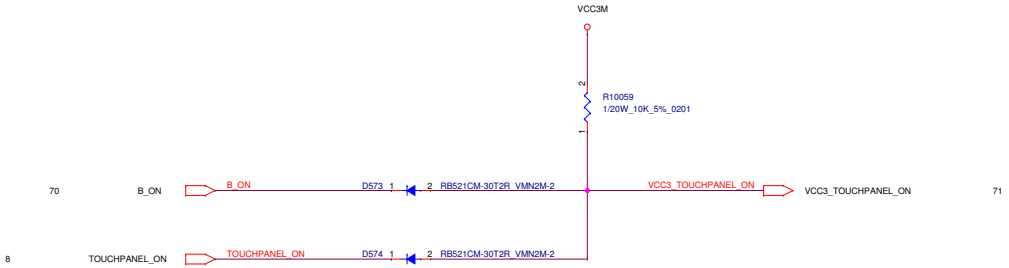


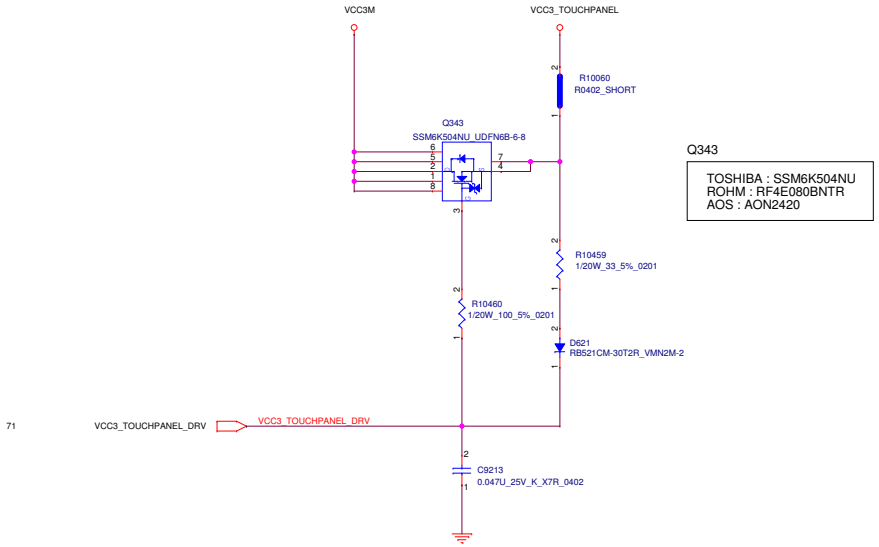


Q8616

TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420

Lenovo		
Project Name : Ratchet-1	Title : LOAD SW B	
Size :	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 95 of 98	

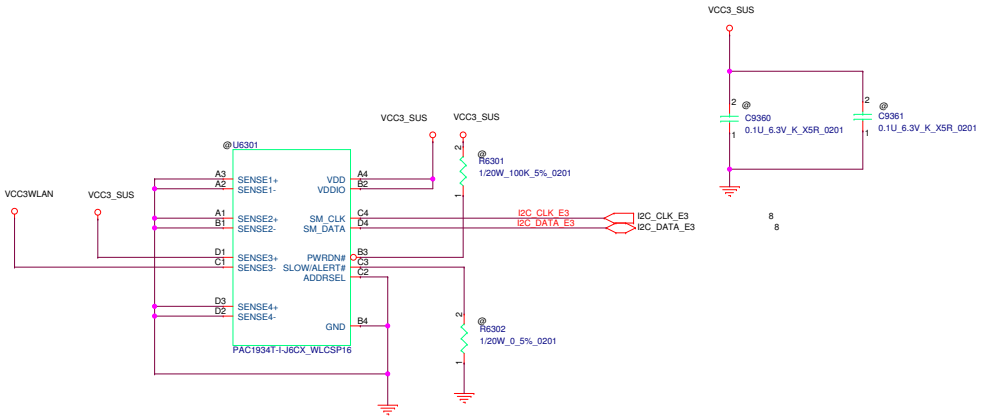




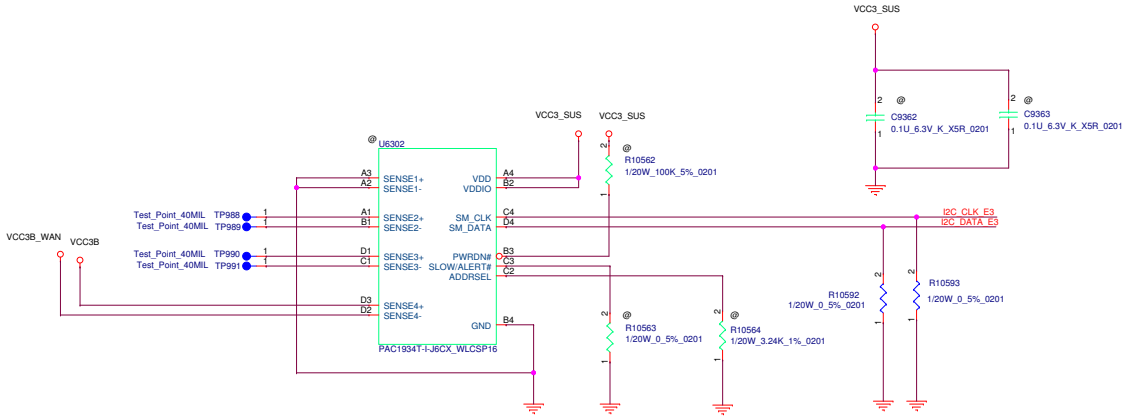
Q343

TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420

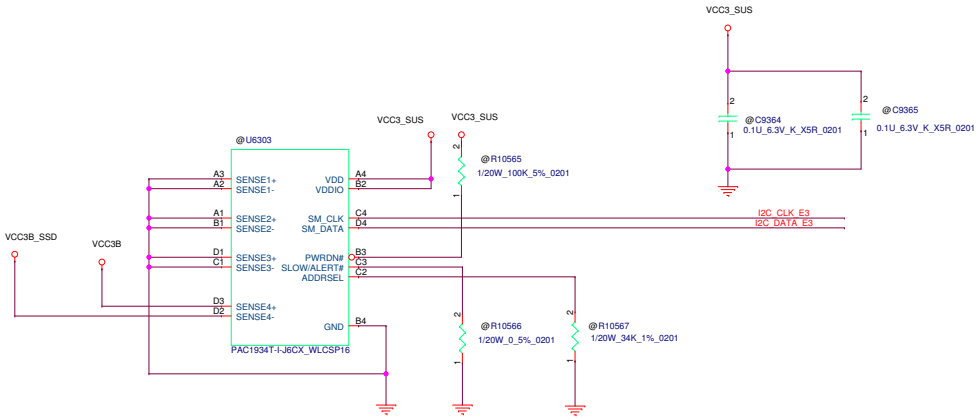
Project Name : Ratchet-1	Title : LOAD SW TOUCH PANEL
Size : C	Document Number :
Rev : 0.49	
Date: Monday, April 01, 2019	Sheet : 96 of 98



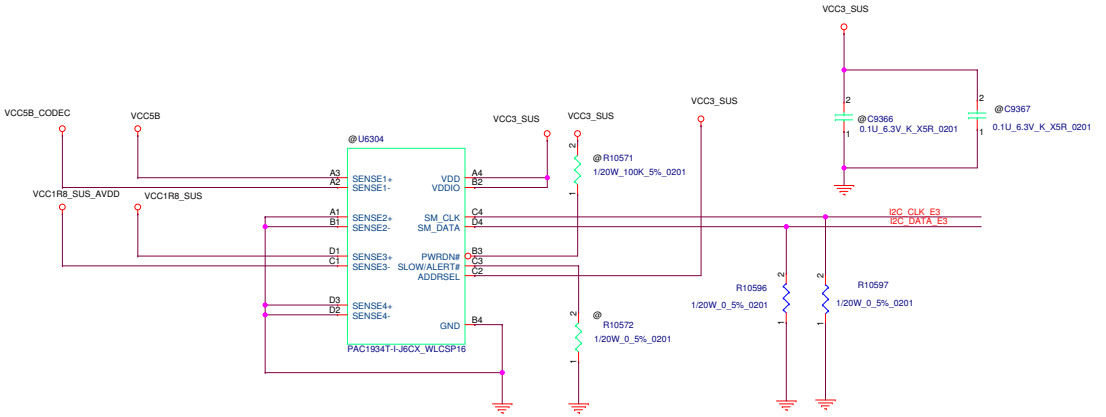
For WLAN I2C Address:0010_000(ADDRSEL=0 (Tie to GND))



For WWAN I2C Address:0010_101(ADDRSEL=3,240)

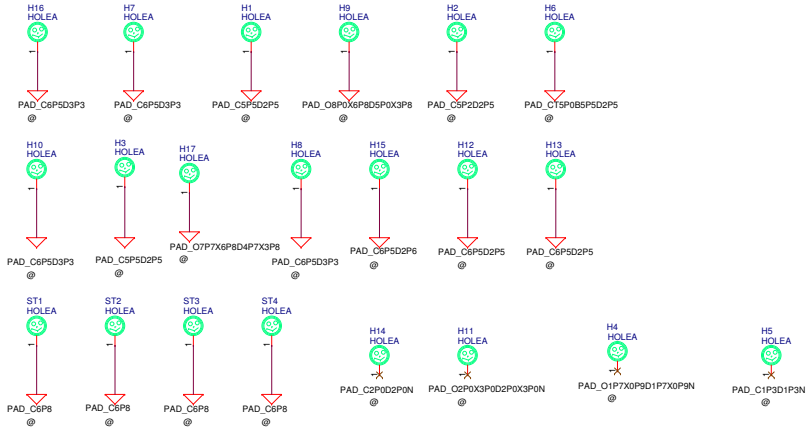


For Storage I2C Address:0011_010(ADDRSEL=34,000)

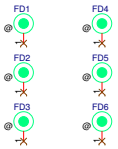


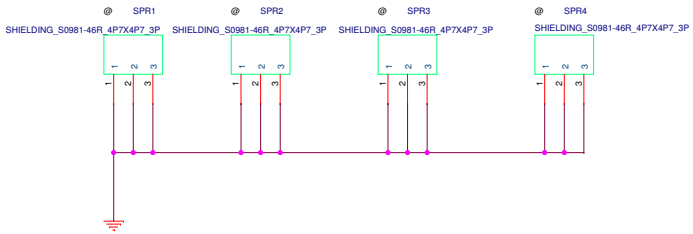
For Audio I2C Address:0011_111(ADDRSEL=Tied to VDD)

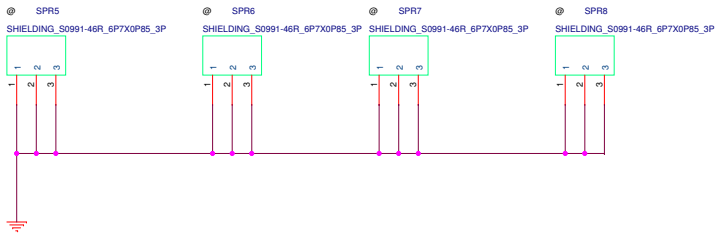
Lenovo		
Project Name : Ratchet-1	Title : ENERGY ESTIMATION ENGINE	
Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019	Sheet : 97 of 98	



FID
Board Area



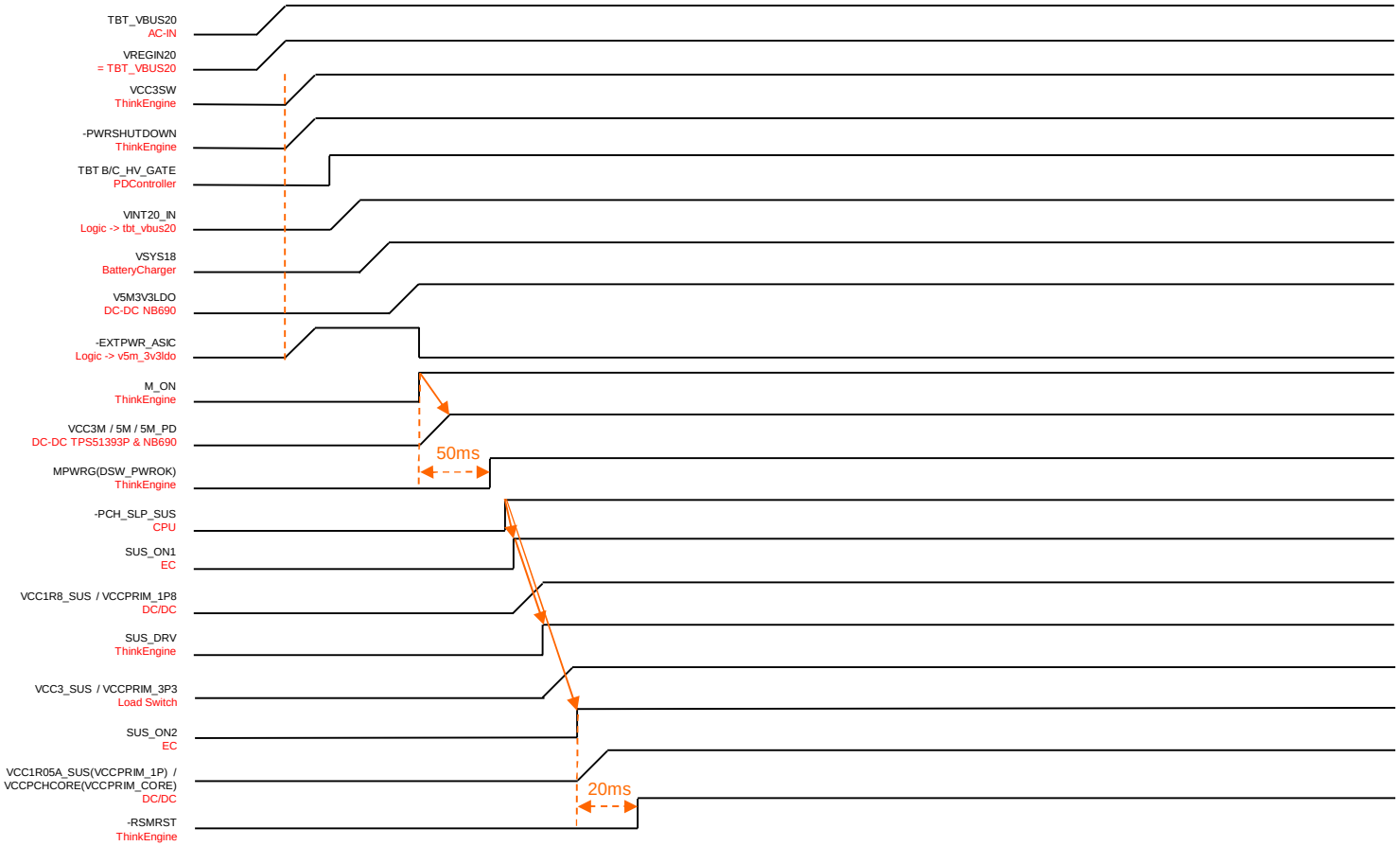




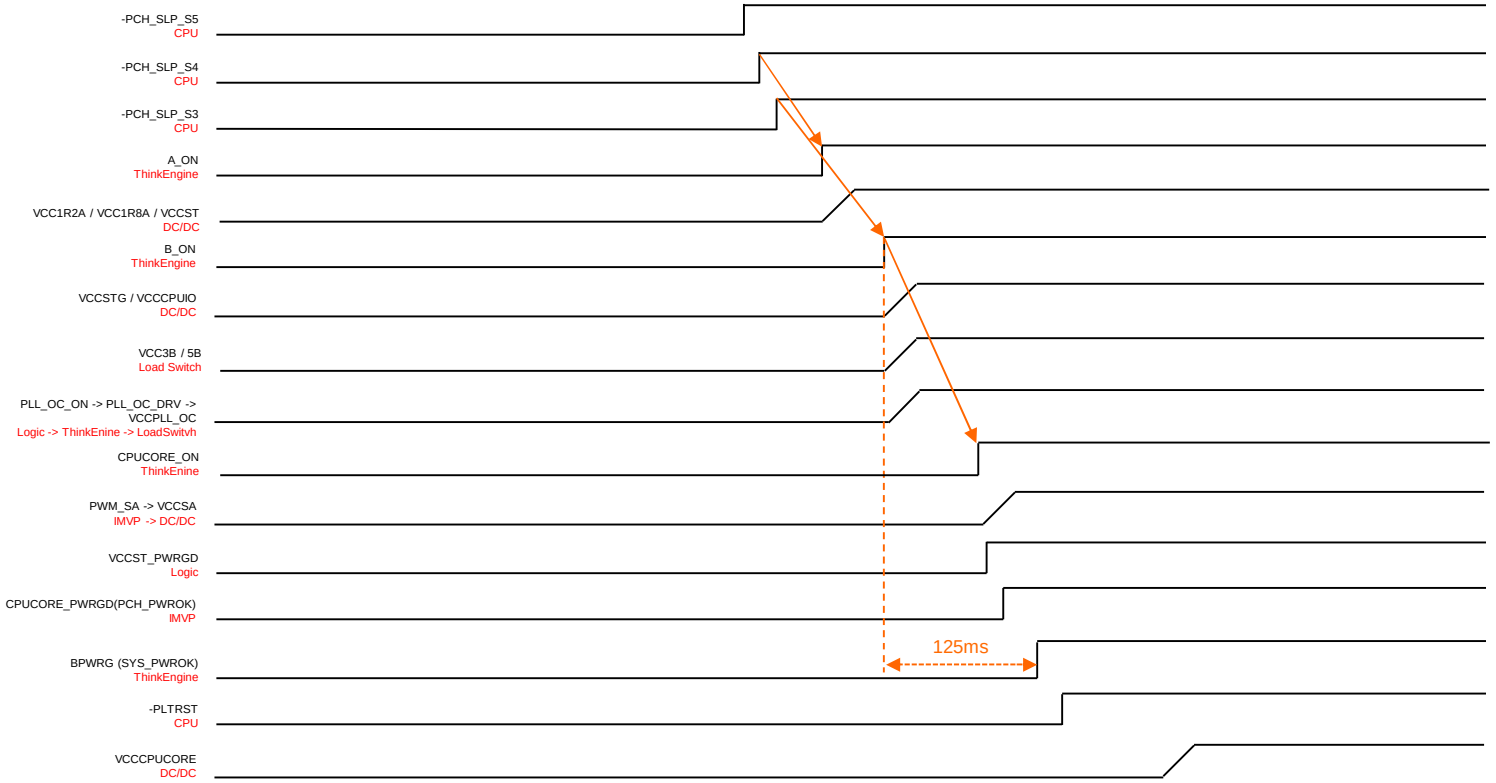
Lenovo

Project Name : Ratchet-1	Title : PTH FOR SCREW HOLES
Size : C	Document Number :
Rev : 0.01	
Date: Monday, April 01, 2019	Sheet : 98 of 98

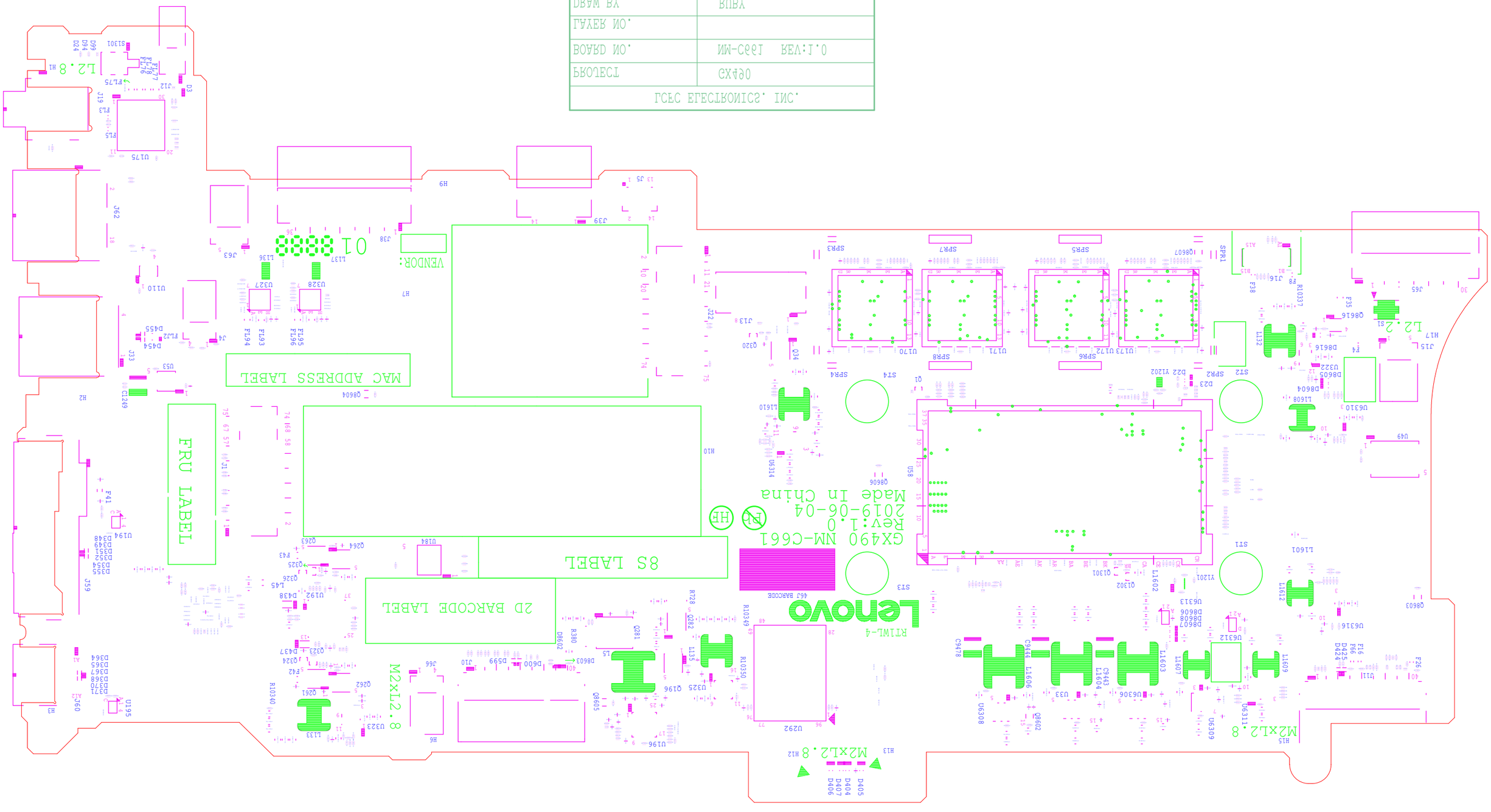
Ratchet Power up Sequence - cold boot with Type-C (Thunderbolt)

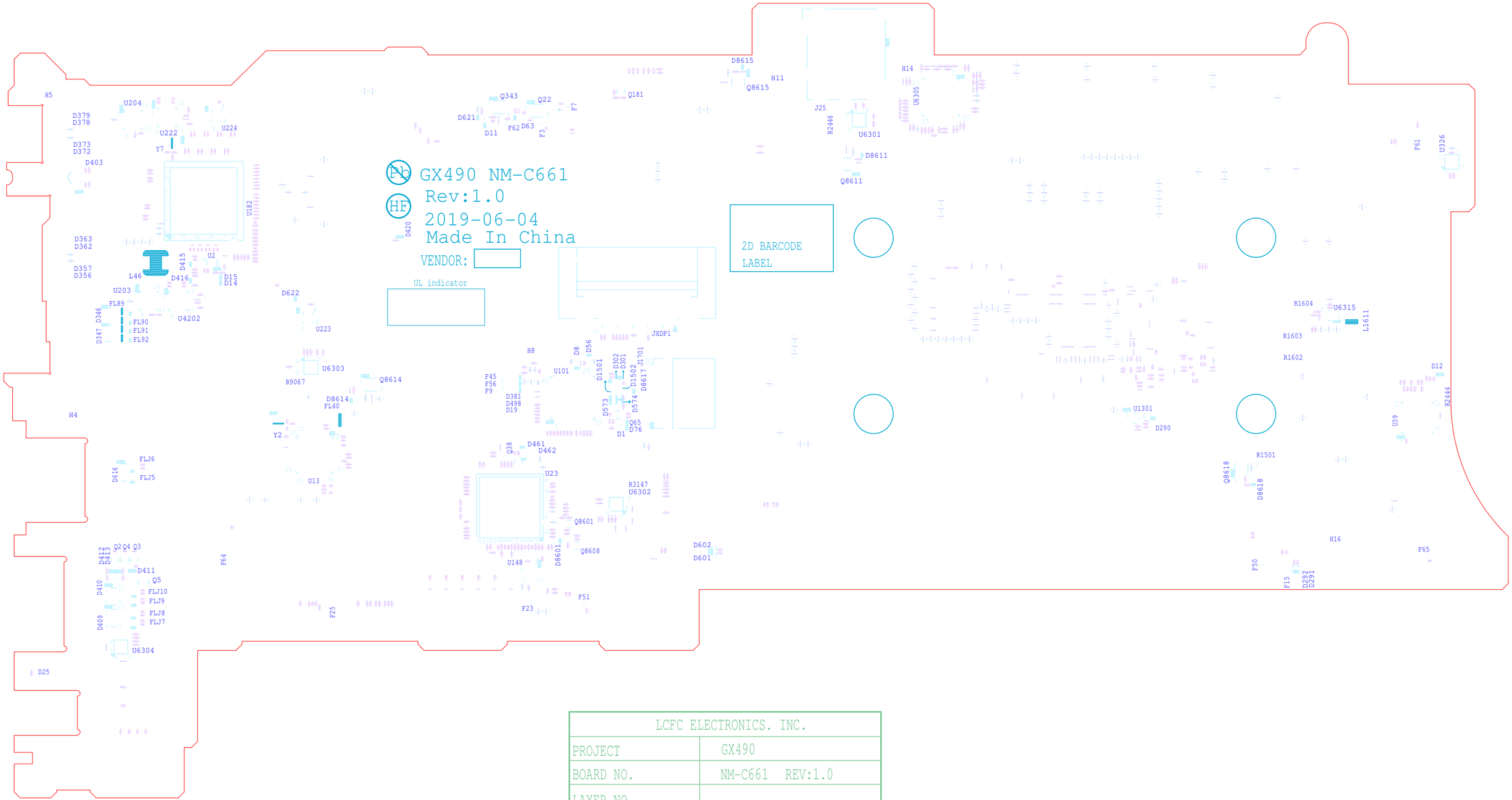


Ratchet Power up Sequence - cold boot with Type-C (Thunderbolt)



LCFC ELECTRONICS, INC.	
PROJECT	GX490
BOARD NO.	NM-C661 REV:1.0
LAYER NO.	
DRAM BY	KUBX
Issued Date	2019-06-04
Security level	Confidential
Description of change	2019-06-04





LCFC ELECTRONICS. INC.	
PROJECT	GX490
BOARD NO.	NM-C661 REV:1.0
LAYER NO.	
DRAW BY	RUBY
Issued Date	2019-06-04
Security level	Confidential
Decipherment date	2020-06-04