PCH_CPU GPIO

		Default ok	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
N501	GPIO_00	GPI	GPI	CIO_PLUG_EVENT		EXT PU 3.3K	+3VS
	GPIO_01	GPI	GPI	EXT_SMI#	INT PU 20K (As TACH)	EXT PU 10K	+3VS
	GPIO_02	GPI	Native	PCI_INTE#		EXT PU 10K	+3VS
	GPIO_03	GPI	GPI	SATA_ODD_DA#		EXT PU 10K	+3VS
	GPIO_04	GPI	GPI	PCB_ID0		EXT PD 10K	+3VS
	GPIO_05	GPI	GPI	PCB_ID1		EXT PD 10K	+3VS
	GPIO_06	GPI	GPI	THDS_HIMI_HPD	INT PU 20K (As TACH)	Ext PU 10K	+3VS
	GPIO_07	GPI	GPI		INT PU 20K (As TACH)	Ext PU 10K	+3VS
	GPIO_08	GPO	GPO	PCH_GPIO8	INT PU 20K (RSMRST#-L)		+3VSUS
	GPIO_09	Native	GPI	USB_OC#5(EXT_SCI#)		EXT PU 10K	+3VSUS
	GPIO_10	Native	Native	USB_OC#6		EXT PU 10K	+3VSUS
	GPIO_11	Native	GPI	CPAD_INT		EXT PU 10K	+3VSUS
	GPIO_12	Native	Native	LAN_PHY_PWR_CTRL(NC)			+3VSUS
N501	GPIO_13	GPI	Native				+3VSUS
	GPIO_14	Native	Native	USB_OC#7		EXT PU 10K	+3VSUS
	GPIO_15	GPO	GPO	WLAN_BT_LED		EXT PU 1K	+3VSUS
	GPIO_16	GPI	GPI	SATA_DEVSLP_B (NC)		EXT PU 10K	+3VS
	GPIO_17	GPI	GPI	DGPU_PWROK	INT PU 20K (As TACH)	EXT PD 1M EXT PU 1K	+3VSG
	GPIO_18	Native	Native	CLK_REQ1#		EXT PU 10K	+3VSUS
	GPIO_19	GPI	GPI	SATA1GP (BIOS Boot)	INT PU 20K		+3VS
	GPIO_20	Native	Native	CLK_REQ2#	INT PU 20K(AS SMI#)	EXT PU 10K	+3VS
	GPIO_21	GPI	GPI	SATA_DEVSLP_B (NC)		Ext PU 10K	+3VS
	GPIO_22	GPI	GPO	WLAN_LED		Ext PU 10K	+3VS
	GPIO_23	Native	Native	PCH_DEQ#1(NC)	INT PU 20K		+3VS
	GPIO_24	GPO	GPO	SMBUS_SEL (NC)			+3VSUS
	GPIO_25	Native	Native	CLK_REQ3#		EXT PU 10K	+3VS
	GPIO_26	Native	Native	CLK_REQ4# (NC)		EXT PU 10K	+3VSUS
	GPIO_27	GPI	GPI	DSW_WAKE#	INT PU 20K		+VCCPDSW
N501	GPIO_28	GPO	GPO	WLAN_ON#		EXT PU 10K ok	+3VSUS
N501	GPIO_29	GPI	Native?	SLP_WLAN#			+VCCPDSW
	GPIO_30	Native	Native	ME_SusPwrDnAck_R		EXT PU 10K	+3VSUS
	GPIO_31	GPI	Native	ME_AC_PRESENT_PCH	INT PU 20K	EXT PU 100K	+VCCPDSW
	GPIO_32	Native	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS
	GPIO_33	GPO	Native	HDA_DOCK_RST# (NC)	INT PU(PLTRST#-L)		+3VS
	GPIO_34	GPI	GPI	STP_PCI# (NC)		EXT PU 10K	+3VS
	GPIO_35	GPO	GPO	SATA_PWR_EN#1_R	INT PU(AS SMI#)		+3VS
	GPIO_36	GPI	GPI	SATA_ODD_PRSNT#_R	INT PU 20K (PLTRST#-L)	EXT PU 200K	+3VS
	GPIO_37	GPI	GPI	PDI_OVRVLTG	INT PU 20K (PLTRST#-L)	EXT PD 100K	+3VS
	GPIO_38	GPI	GPI	SPKR_MUTE (NC)		EXT PU 10K	+3VS
	GPIO_39	GPI	GPI	SATA_ZPD_DET (NC)		EXT PU 10K	+3VS
N501	GPIO_40	GPO	GPO	GPIO_3_FORCE_PWR		EXT PU 10K	+3VSUS
	GPIO_41	GPI	GPI	DIMM_SEL0		EXT PU 10K	+3VSUS
	GPIO_42	GPI	GPI	DIMM_SEL1		EXT PU 10K	+3VSUS
	GPIO_43	GPI	GPI	DIMM_SEL2		EXT PU 10K	+3VSUS
	GPIO_44	Native	Native	CLK_REQ5#	INT PU 20K (RSMRST#-L)	EXT PU 10K	+3VSUS
	GPIO_45	Native	Native	CLK_REQ6#		EXT PU 10K	+3VSUS
	GPIO_46	Native	Native	CLK_REQ7#	INT PU 20K (RSMRST#-L)	EXT PU 10K	+3VSUS
	GPIO_47	Native	Native	CLK_PEGA_REQ#		EXT PU 10K	+3VSUS
N501	GPIO_48	GPI	GPI	DGPU_FB_CLAMP_GPIO		EXT PD 10K	+3VS
	GPIO_49	GPI	GPI	PCIE_TERM_REF#_R (NC)		EXT PU 10K	+3VS
	GPIO_50	GPI	GPO	GPU_RST#		EXT PD 10K	+5VS
	GPIO_51	GPO	GPO	SPI_CS1# (NC) (BIOS Boot)	INT PU 20K (RSMRST#-L)		+3VS
	GPIO_52	GPI	GPO	STP_PCI# (NC)		EXT PU 10K	+3VS
N501	GPIO_53	GPO	GPO	GPU_EVENT#	INT PU 20K (RSMRST#-L)	EXT PU 100K	+3VSG
	GPIO_54	GPI	GPO	DGPU_PWR_EN#		EXT PD 1K	+5VS
	GPIO_55	GPO	Native	STP_A16GVR	INT PU 20K (RSMRST#-L)		+3VS
	GPIO_56	Native	Native	CLK_PEGB_REQ# (NC)		EXT PU 10K	+3VSUS
	GPIO_57	GPI	GPO	BT_ON		EXT PD 100K	+3VSUS
	GPIO_58	Native	Native	SML1_CLK		EXT PU 2.2K	+3VSUS
	GPIO_59	Native	Native	USB_OC#0		EXT PU 10K	+3VSUS
	GPIO_60	Native	GPO	DRAMRST_PCH		EXT PU 2.2K	+3VSUS
	GPIO_61	Native	Native	PM_SUS_STAT#			+3VSUS
	GPIO_62	Native	Native	SUS_CLK#	INT PU (RSMRST#-L)		+3VSUS
	GPIO_63	Native	Native	SLP_S5#			+3VSUS
	GPIO_64	Native	Native	CLK_CPU1 (NC)	INT PU 20K (PWROK+L)		+3VS
	GPIO_65	Native	Native	CLK_CPU1 (NC)	INT PU 20K (PWROK+L)		+3VS
	GPIO_66	Native	Native	CLK_CPU2 (NC)	INT PU 20K (PWROK+L)		+3VS
	GPIO_67	Native	Native	CLK_CPU3#0 (NC)	INT PU 20K (PWROK+L)		+3VS
N501	GPIO_68	GPI	GPO	SATA_ZPD_PWRDT (NC)	INT PU 20K (As TACH)		+3VS
	GPIO_69	GPI	GPI	GPIO69 (NC)	INT PU 20K (As TACH)	EXT PU 10K	+3VS
	GPIO_70	Native	Native	GPIO70 (NC)	INT PU 20K (As TACH)	EXT PU 10K	+3VS
	GPIO_71	Native	Native	GPIO71 (NC)	INT PU 20K (As TACH)	EXT PU 10K	+3VS
N501	GPIO_72	Native	Native	TBT_BATLOW#		EXT PU 10K	+VCCPDSW
	GPIO_73	Native	Native	CLK_REQ0#		EXT PU 10K	+3VSUS
	GPIO_74	Native	Native	PCHHOT#		EXT PU 10K	+3VSUS
	GPIO_75	Native	Native	SML1_DAT	INT PU (RSMRST#-L)	EXT PU 2.2K	+3VSUS

CKI

EC IT8585 GPIO

EC GPIO	Use As	Signal Name	CKD
GPA0	O	PWR_LED#	
GPA1	OD	CHG_LED#	
GPA2	OD	CHG_FULL_LED#	
GPA3	O	AOAC_WLANLED	(Default: Low)
GPA4	ALT	FAN1_PWM	
GPA5	ALT	FAN0_PWM	
GPA6	ALT	KB_LED_PWM	(Default: Low)
GPA7	O	OS_LED#	(Default: Low)
GPB0	I	AC_IN_OC#	
GPB1	I	LIS_SW#	
GPB2	OD	PM_BATLOW# (EXT PU 10Kohm, +3VA_DSW)	
GPB3	I	PWR_SW#	
GPB4	O	PS_ON	
GPB5	O	A20GATE	
GPB6	OD	RCIN#	
GPB7		3VA_ALW	(Power pin)
GPC0	O	AOAC_WLANON/FM_EXTTS#0	(Default: Low)
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	O	PM_PWRBTN#	
GPC4		DGPU_FB_CLAMP_REQ#_EC	
GPC5	I	PM_SUSC#	
GPC6	I	BAT1_IN_OC#	
GPC7	I	RFON_SW#	
GPD0	I	TP	
GPD1	OD	CAP_LED#	
GPD2	O	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	O	OP_SD#	
GPD6	ALT	FAN0_TACH	
GPD7	ALT	FAN1_TACH	
GPE0	O	SUSB_EC#	
GPE1	O	SUSC_EC#	
GPE2	O	1.35V_ON	
GPE3	OD	PCH_GPIO27#	
GPE4		TP	
GPE5	I	PM_SUSB#	(Default: Low)
GPE6	I	ME_AC_PRESENT	
GPE7	ALT	Exp_Gate/P4G#	/WLAN_WAKE#_EC
GPF0	O	5VSUS_ON	
GPF1	O	3VSUS_ON	
GPF2	ALT	SMB0_CLK	
GPF3	ALT	SMB0_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	ALT	PECI_EC	
GPF7	O	PCH_SPI_OV	
GPG0	O	DGPU_LIMIT	
GPG1	O	PM_SUSACK#	
GPG2	O	PWRLIMIT#_EC	(Default: Low)
GPG3	SPI	EC_SCE#_PCH	
GPG4	SPI	EC_SI_PCH	
GPG5	SPI	EC_SO_PCH	
GPG6	O	USB30_5VBUS	(Default: Low)
GPG7	SPI	EC_SCK_PCH	
GPH0	O	PM_CLKRUN#	
GPH1	OD	THRO_CPU#	
GPH2	O	LCD_BACKOFF#	
GPH3	O	PM_RSMRST#	
GPH4	O	DPWROK_EC	
GPH5	O	PM_PWROK	
GPH6	O	PM_SYSPWROK	
GPH7		TP	
GPI0	I	PCH_SLPSUS#	(Ext PU +3VA_EC)
GPI1	I	+3VSUS_PWRGD	
GPI2	I	ALL_SYSTEM_PWRGD	
GPI3	I	CORE_PWRGD	
GPI4	I	5VSUS_PWRGD/3VA_DSW_PWRGD	(DEEP S3)
GPI5	I	ME_SusPwrDnAck	(Ext PD 100K)
GPI6	I	A/D_Max_Power	(Ext PD 100K)
GPI7	ALT	MB_MAX_POWER	(Ext PD 100K)
GPJ0		TP	
GPJ1	O	3VADSW_ON	
GPJ2	O	PL_REF_EC	(Default: Low)
GPJ3		TP	
GPJ4		TP	
GPJ5	O	DRAMRST_EC	
GPJ6		DGPU_FB_CLAMP	
GPJ7	O	USB_CHARGE_ON#	

Design IP Source: N56JZ

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
SO-DIMM A(0)	A0h	
ON-BOARD MEM B		
EC Master (SMB1)	**SMBus Address**	
SM-Bus Device		
VGA Thermal Sensor	9Eh	
CPU Thermal Sensor	90h	
DIMM Thermal sensor	9Ah	

DDR3L@1.35V only
1 DPC DDR3L 1600 MTs
2 DPC DDR3L 1333 MTs

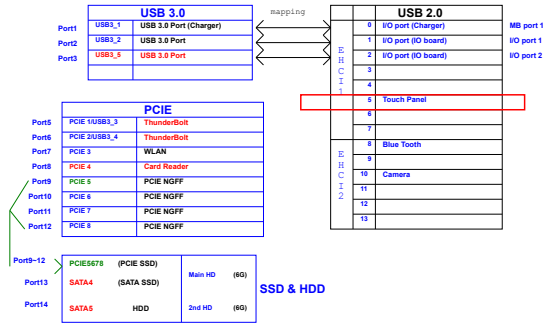
CPU(Haswell) rPGA 947
PCH(Lynx Point) BGA695

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

VID / DID

N15P-GX	
ALC668	
RTS5226-GR	



* There are three USB3.0 I/O port in HM86 sku, port5 can be configured as USB3.0 I/O port

Mobile Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
QM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 PCIe* Port 1	USB 3.0 Port 4 PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 PCIe* Port 1	SATA 6Gb/s Port 5 PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 PCIe* Port 1	USB 3.0 Port 4 PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 PCIe* Port 1	SATA 6Gb/s Port 5 PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 PCIe* Port 1	USB 3.0 Port 4 PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 PCIe* Port 1	SATA 6Gb/s Port 5 PCIe* Port 2	SATA 6Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA

NOTES:
1. Ports listed with NA are not available and are disabled.

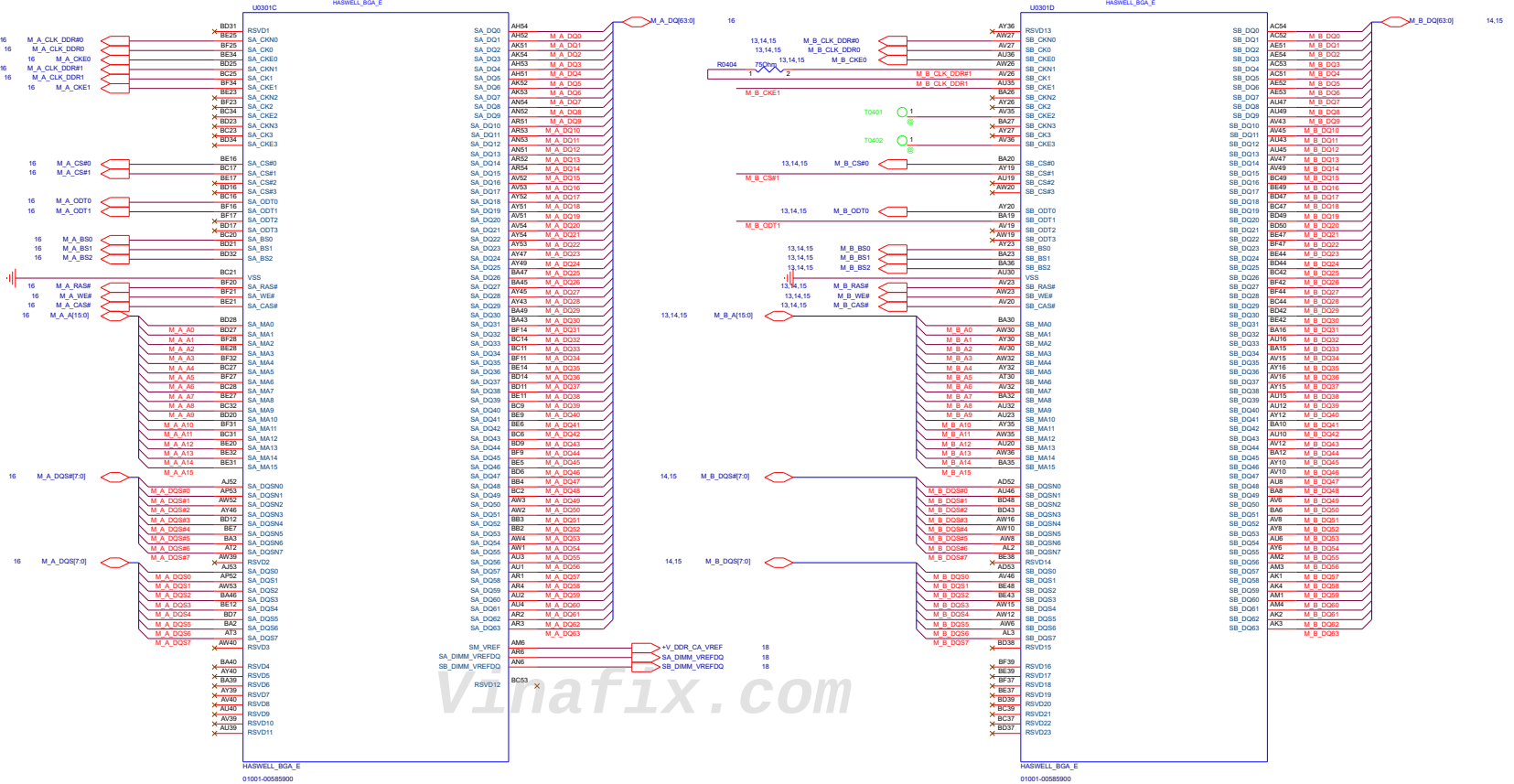
USB 3.0 xHCI Highlights

- Port mapping restrictions removed
  - USB 3.0 signals can now be paired with any of USB2.0 signal 0-7 or 8-13
  - Custom mapping through ACPI table/BIOS
  - Default mapping USB 3.0 1-6 to USB 2.0 0-5 ports

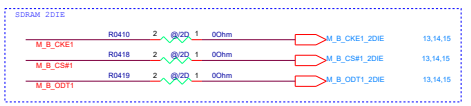
USB 2.0 Signal	USB 3.0 Signal
0	1
⋮	2
7	3
8	4
⋮	5
13	6

- Better USB 2.0 performance than EHCI
- Windows* 8 will include a native inbox xHCI driver

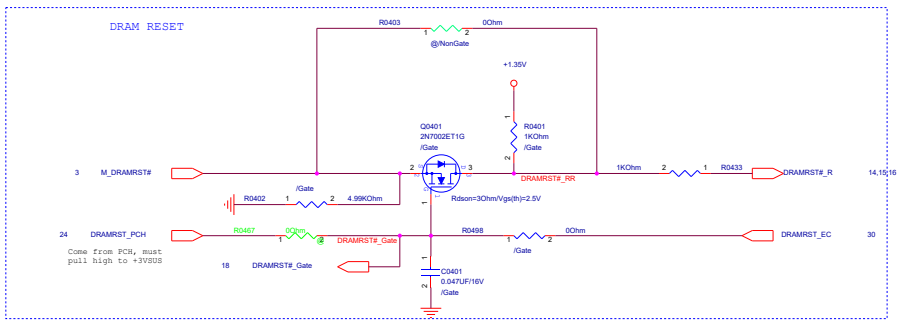
ASUSTeK COMPUTER INC. NB1	Title : System Setting	
	Engineer: RD1/EE1	
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 10, 2015	Sheet 2 of 58	



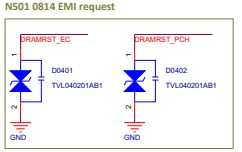
	Mount	Unmount
intel ds3	R0403	Q0401 R0401 R0498 R0402
asus ds3	Q0401 R0401 R0498 R0402	R0403



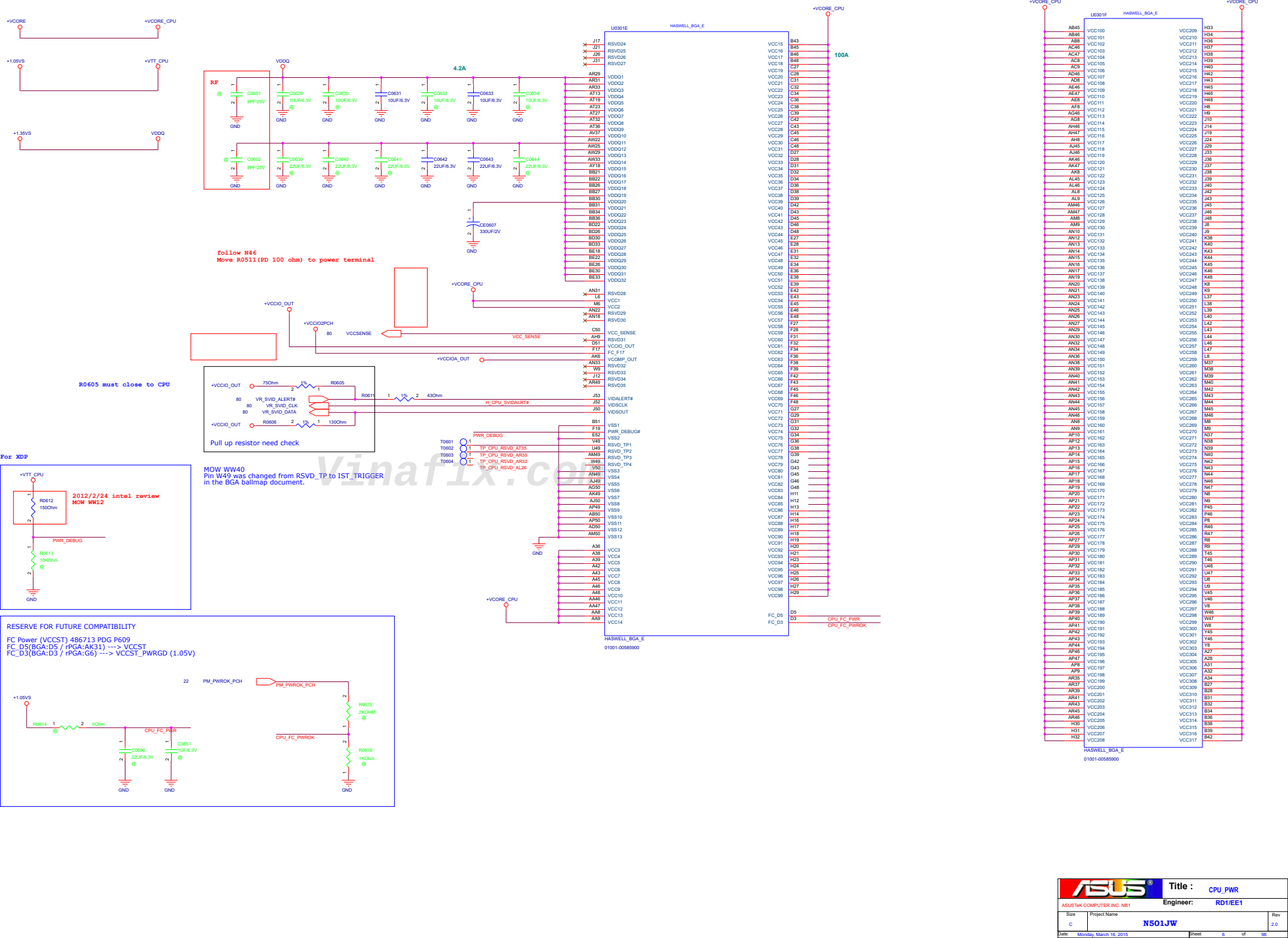
farad : BOM



N501 0814 EMI request



ASUSTeK COMPUTER INC. NB1	Title :	CPU_DDR3L
	Engineer:	RD1/EE1
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 4 of 98	



ASUSTeK COMPUTER INC. NB1	Title :	CPU_PWR	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 6 of 98		

remove XDP

ASUSTeK COMPUTER INC. NB3	Title : CPU_XDP	
	Engineer: RD1/EE1	
Size: B	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 7 of 98	

Title : NB_****

Engineer: RD1/EE1

ASUSTeK COMPUTER INC. NB3

Size	Project Name	Rev
A	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 8 of 98

Title : NB_****

Engineer: RD1/EE1

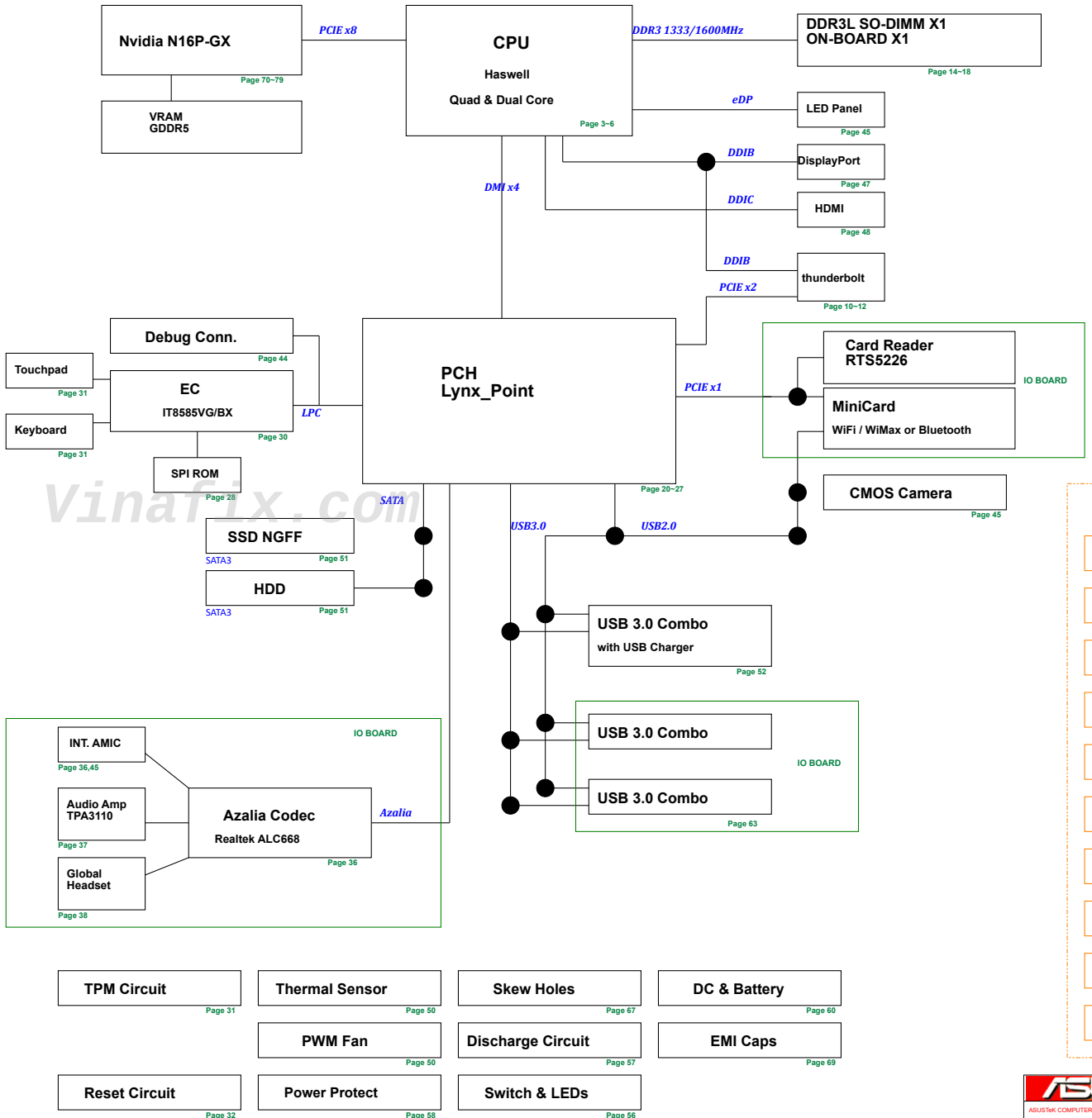
ASUSTeK COMPUTER INC. NB3

Size	Project Name	Rev
A	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 9 of 98

N501JW Block Diagram

Shark Bay Platform



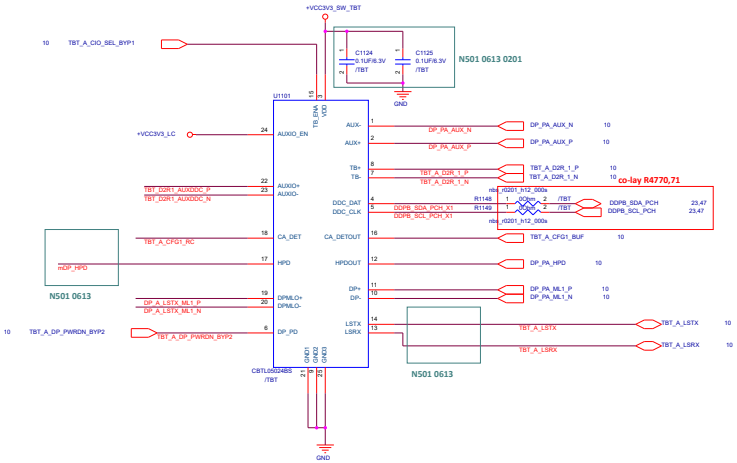
ASUSTeK COMPUTER INC. NB3

Title : Block Diagram

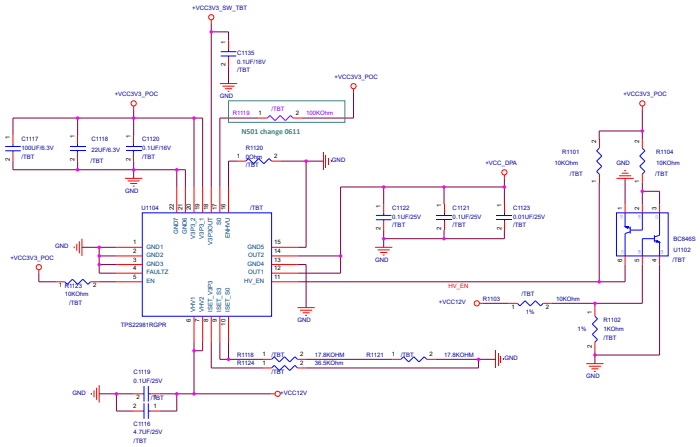
Engineer: RD1/EE1

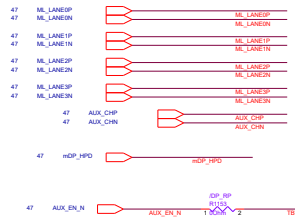
Size: C | Project Name: N501JW | Rev: 2.0

Date: Monday, March 16, 2015 | Sheet 1 of 98

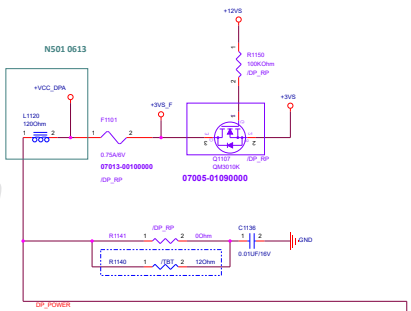


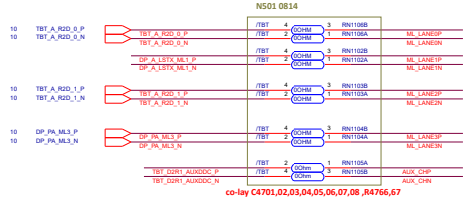
Thunderbolt Multi Level output power

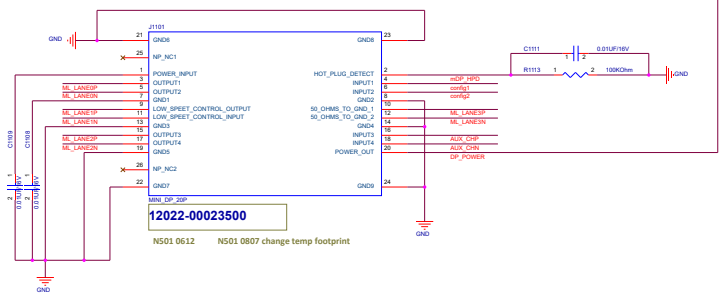




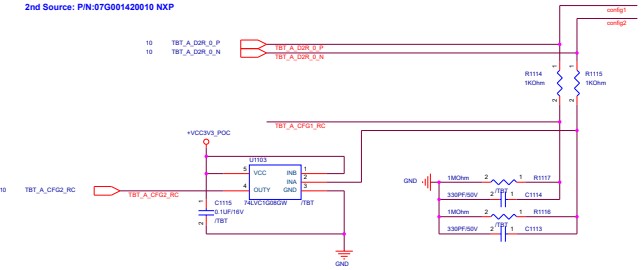
Display Port repeter colay







2nd Source: P/N:07G001420010 NXP



Title :	BDW-LP TBT_CON
ASUSTeK COMPUTER INC. NB1	Engineer: RD1/EE1
Size: Custom	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 11 of 98

FDI Disable	DG - 486713_486713_Shark_Bay_Mobile_PDG_Rev1_0.p190	
Signal	**Enable**	**Disable**
FDI_TXN[0:1] FDI_TXP[0:1]		Can float on CPU
FDI_RXP[0:1] FDI_RXN[0:1]		Can float on PCH
FDI_CSYNC	Connect to Processor and PCH	
FDI_INT	Connect to Processor and PCH	
FDI_RCOMP FDI_RSET	Connect to +1.8VS through 7.5 KΩ resistor Connect to +1.8VS	Float Float

	Mount	Unmount
intel ds3	R0347 R0348 R0349 R0342 R0343 C0310	R0334 R0337 R0351 R0341
asus ds3	R0334 R0337 R0342 R0343 C0310	R0347 R0348 R0349 R0341

ALL_SYSTEM_PWRGD in page58 has been pulled up to +3VS
if mounting R0340, leakage carefully

farad : BOM

farad mini displayport 07/17

R0303 close to CPU
PEG_COMP's trace length < 400mils

eDP_RCOMP's trace length < 100mils

eDP disable/Enable
CFG[4]:
Enable: Mount R0503, R0303=1K
Disable: un-mount R0503, R0303=1/0ohm

connected 43pF close to the SMSV

EMC RESERVED

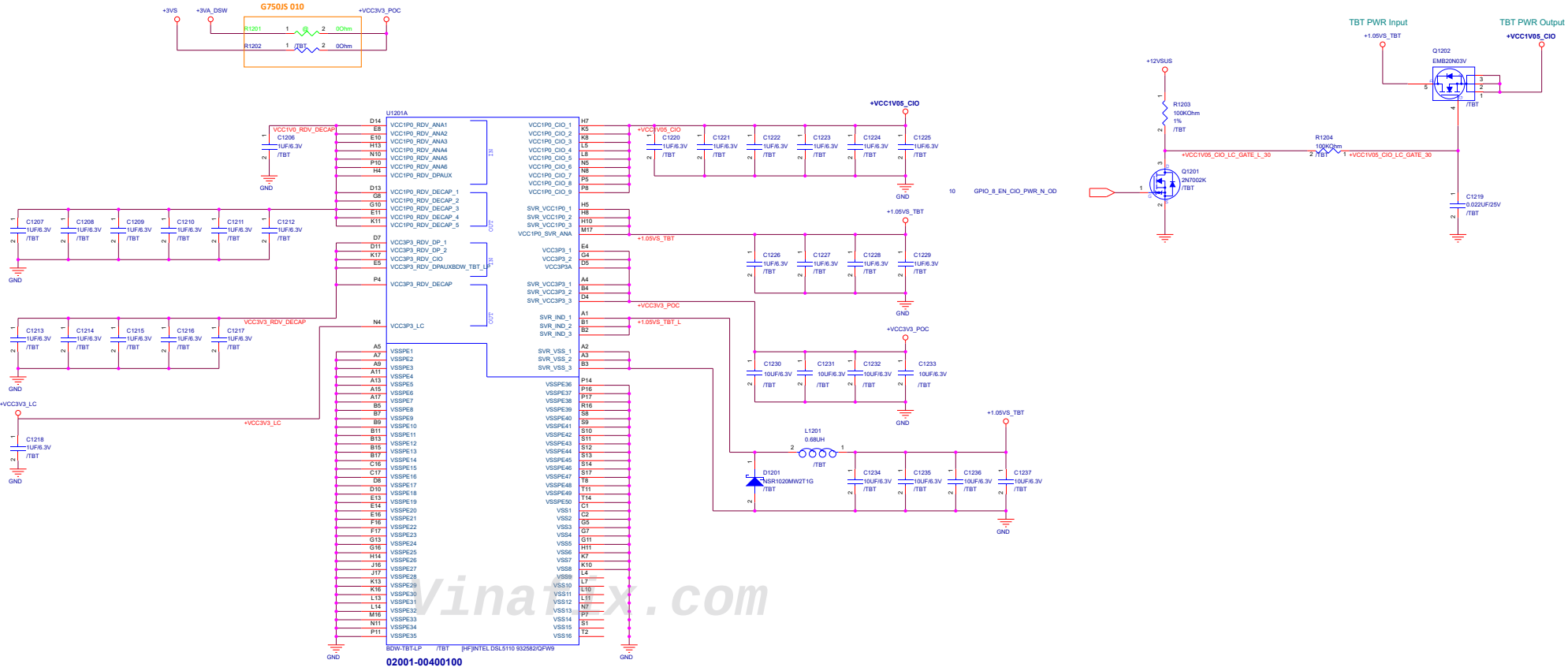
CSC Request

Boundary Scan TP(CPU)

For JTAG

NS01JW

Title :	CPU_SM&PEG,FDI,eDP,DDI
Engineer:	RD1/EE1
Size: Custom	Project Name:
Date: Monday, March 19, 2012	Sheet 1 of 58



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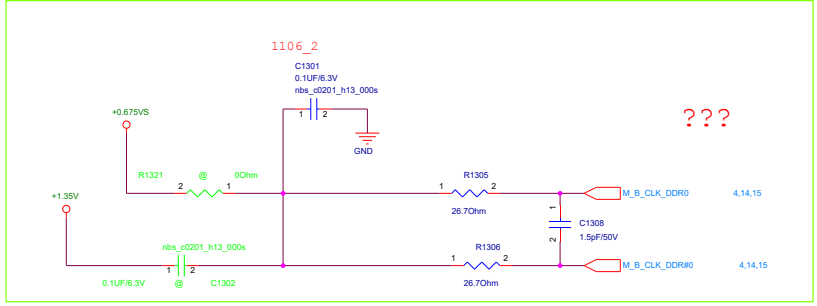
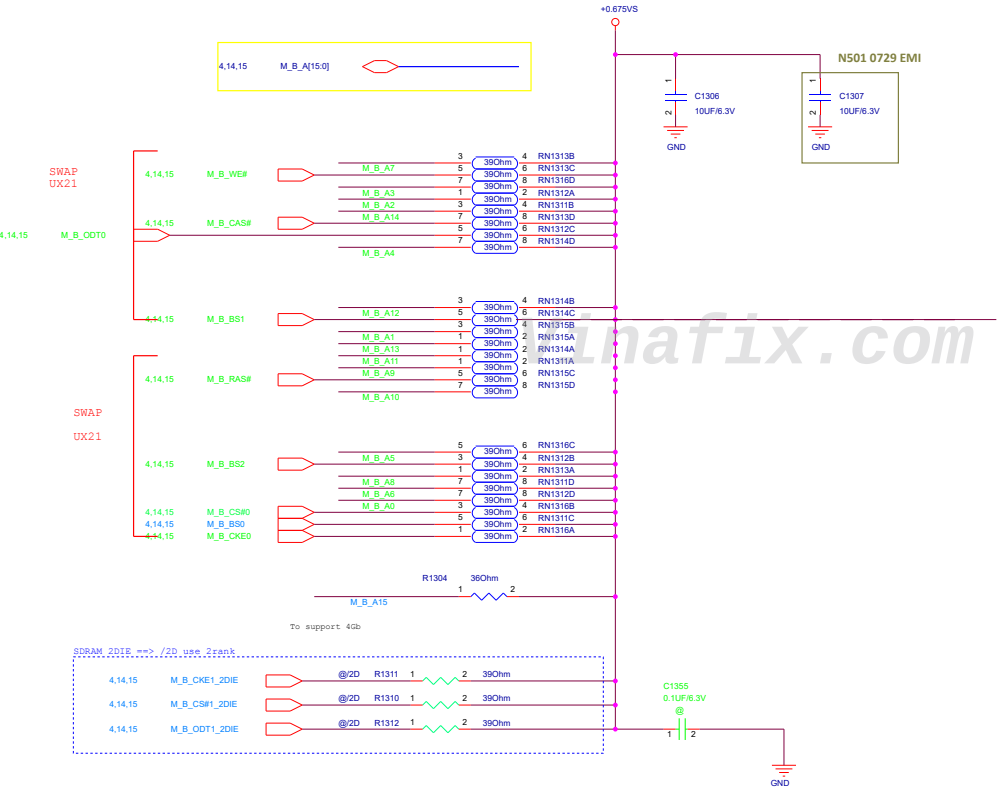
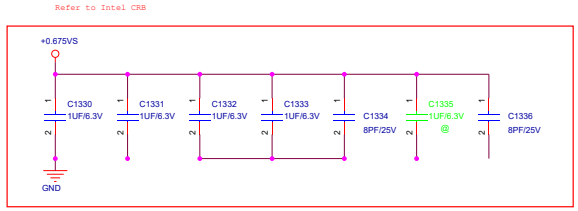
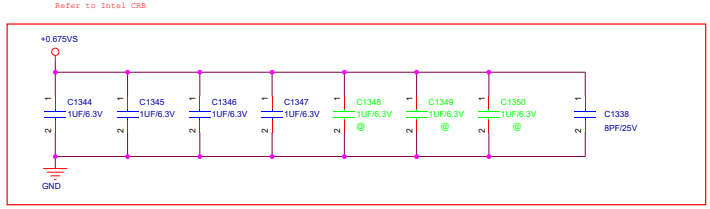
ASUSTeK COMPUTER INC. NB1	Title :	BDW-LP TBT_PWR
	Engineer:	RD1/EE1
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 12 of 98	

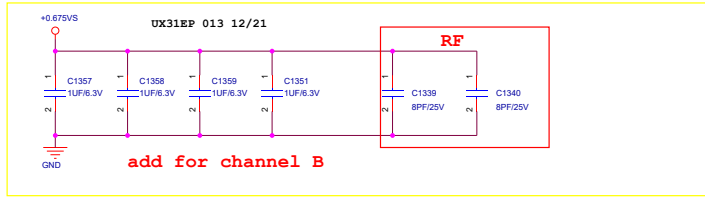


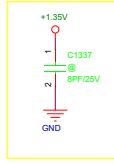






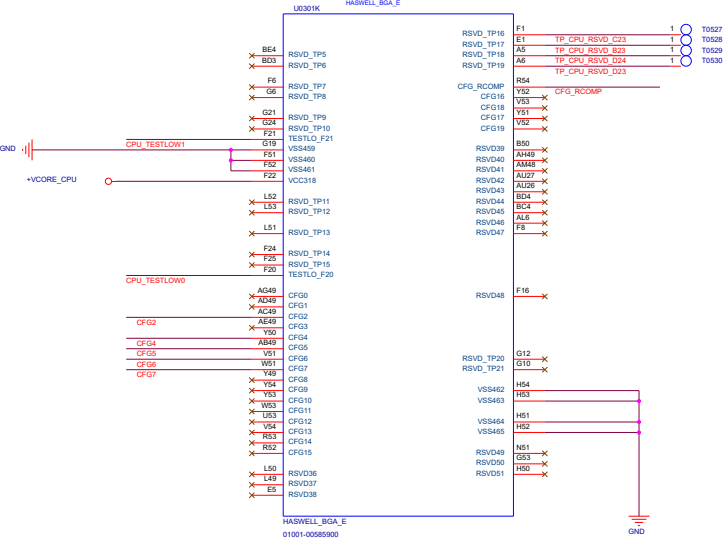
ER-001

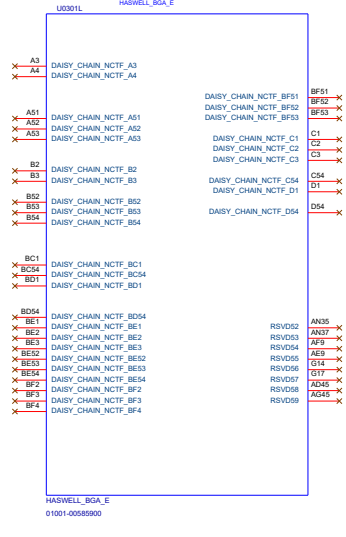


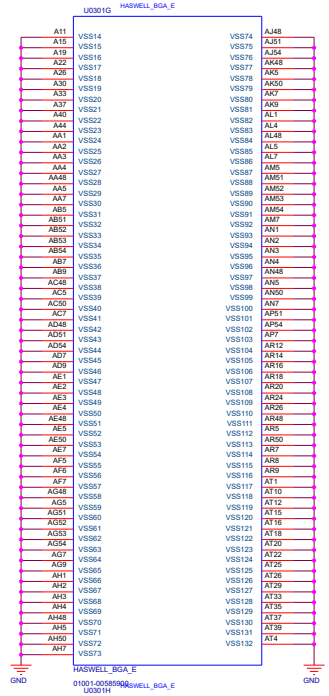


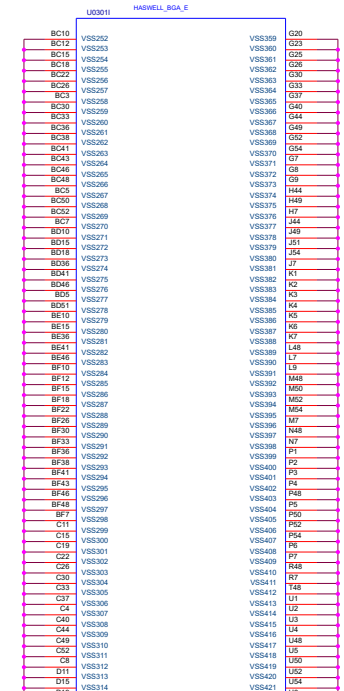
ER-022

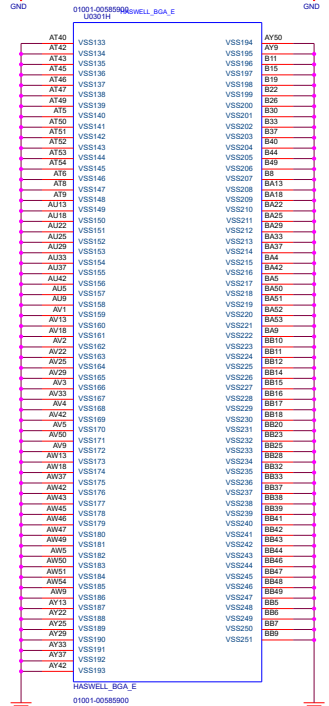
ASUSTeK COMPUTER INC.	Title :	DDR3_TERMINATION
	Engineer:	RD1/EE1
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 13 of 98	











VSS_SENSE → VSSSENSE 80

follow N46
Move R0511(PD 100 ohm) to power terminal

CFG Straps for Processor

ref : 487246_487246_MBL_HSW_EDS_Vol_I_Rev1_0v1 p 74

CFG[1:0]: Reserved configuration lane.

A test point may be placed on the board for these lanes.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.

- 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

CFG[3]: MSR Privacy Bit Feature

— 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting
— 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

CFG[4]: Display Port Presence Strap

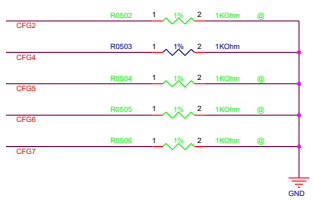
- 1 : (Default) Disable; No Physical Display Port attached to Embedded Display Port
- 0 : Enable; An external Display Port device is connected to the Embeded Display port

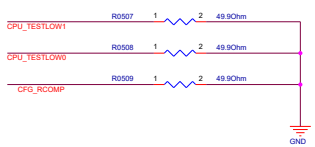
CFG[6:5]: PCIE Port Bifurcation Straps

— 00 = 1 x8, 2 x4 PCI Express*
— 01 = reserved
— 10 = 2 x8 PCI Express*
— 11 = 1 x16 PCI Express*

CFG[19:7]: Reserved configuration lanes.

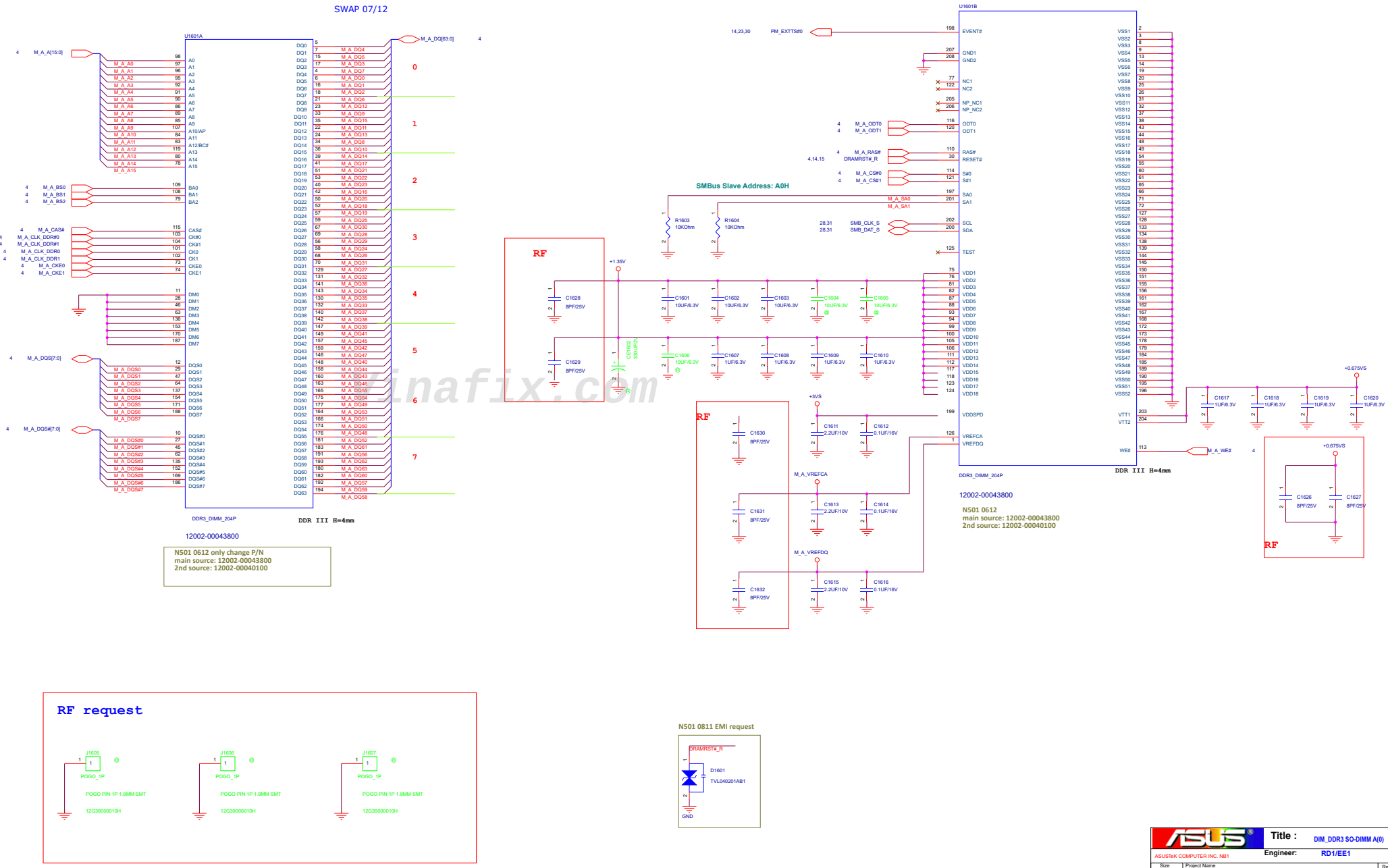
A test point may be placed on the board for these lands





ASUSTeK COMPUTER INC. NB1	Title : CPU_CFG,RSVD,GND	
	Engineer: RD1/EE1	
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 5 of 98	

SODIMM CHA-DIMM0



RF request

N501 0811 EMI request

ASUSTeK COMPUTER INC. NB1	Title :	DIM_DDR3 SO-DIMM A(0)
	Engineer:	RD1/EE1
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 16 of 98	

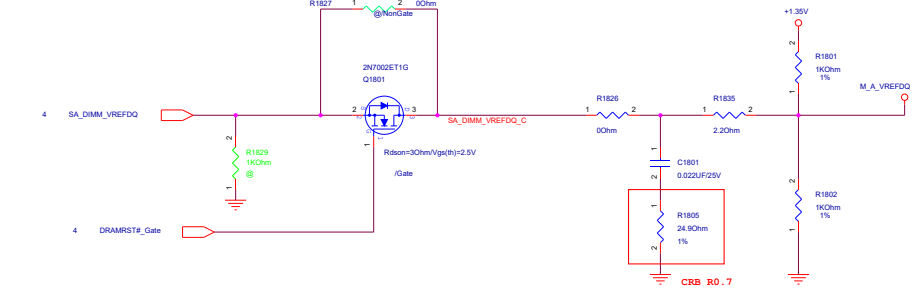
Title : DIM_DDR3 SO-DIMM B(0)

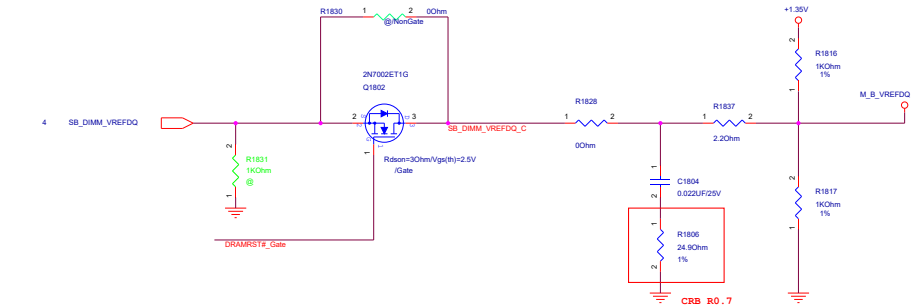
ASUSTeK COMPUTER INC. NB1

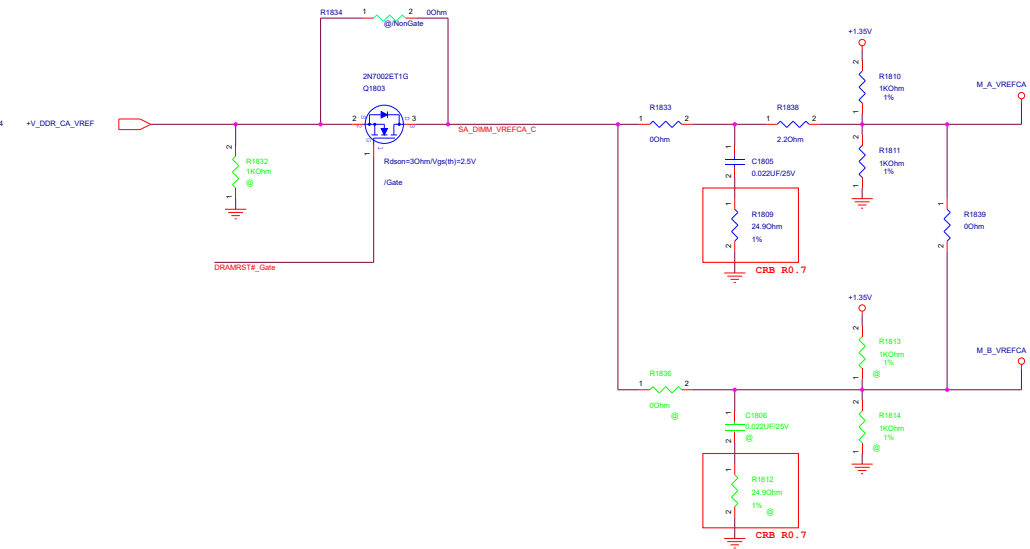
Engineer: RD1/EE1

Size	Project Name	Rev
C	N501JW	2.0

Date:	Monday, March 16, 2015	Sheet	17	of	98







ASUSTeK COMPUTER INC. NB1	Title :	DIM_CA/DQ Voltage	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 18 of 98		

Place close to C1105~C1114

Default BDW-LP TBT FW: TXP/TXN ; RXP/RXN SWAP

N501 0613 0201

N501 0613 0201

N501 0605 0201 co-lay

BDW-LP TBT Flash Memory

Thunderbolt repeter colay
c4715,16,20,21,22,23,24,25
c4709,10

X1101: 25MHZ +/-30ppm/10pF (3225)
1st: P/N:07G010272501 TXC/7V25000011
2nd: P/N:07G0190952500 HOSONIC/E3FB25

07G010272501

Flash Memory

JTAG

Debug Purpose

BDW-LP TBT New Function

BDW-LP TBT SLP_S3#

BDW-LP TBT Force PWR

BDW-LP TBT BATLOW#

02001-00400100

1st: 02001-00400100
2nd:02001-00400000

G750JS 011

PCH_R2506 3.3Kohm Pull High +3Vs

To PCH GPIO that supports SMI

Low pulse

Title :	BDW-LP TBT_IC
ASUSTeK COMPUTER INC. NB1	Engineer: RD1/EE1
Size: C	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 10 of 98

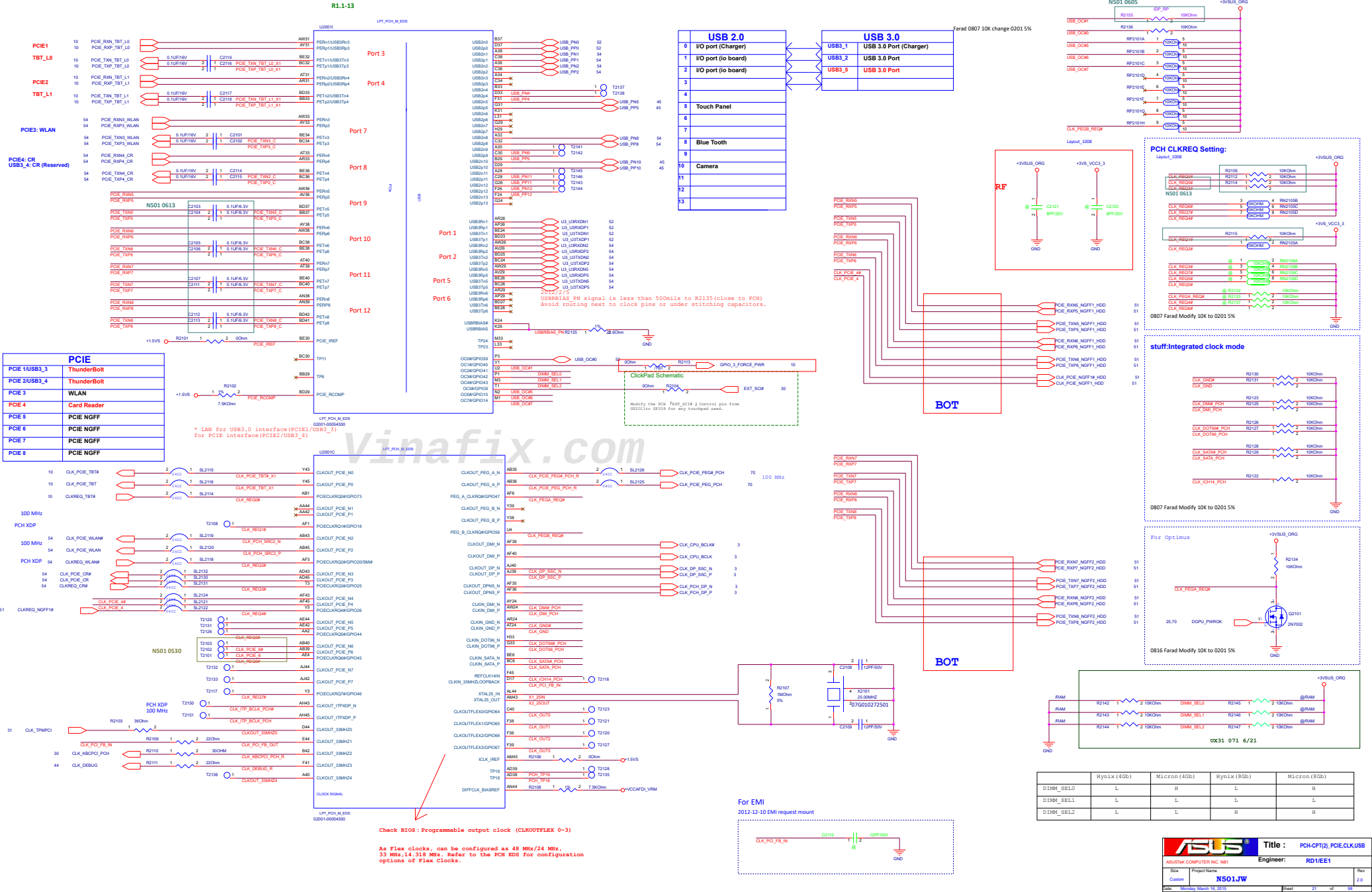
Title : *****

Engineer: RD1/EE1

ASUSTeK COMPUTER INC. NB3

Size	Project Name	Rev
C	N501JW	2.0

Date:	Monday, March 16, 2015	Sheet	19	of	98

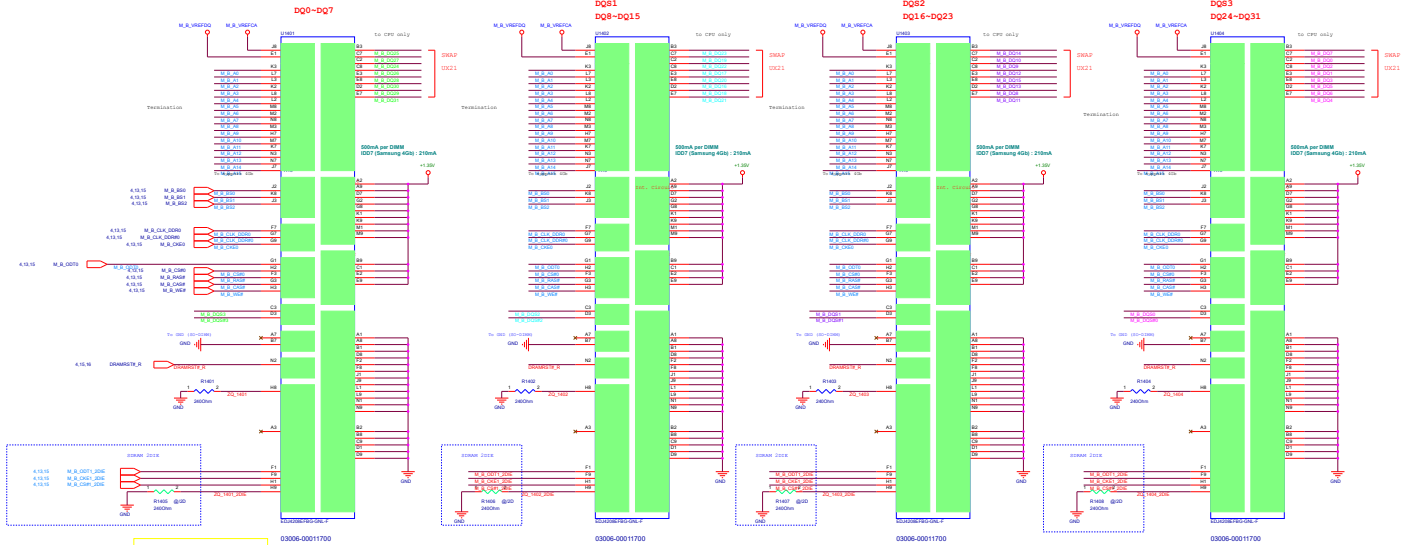


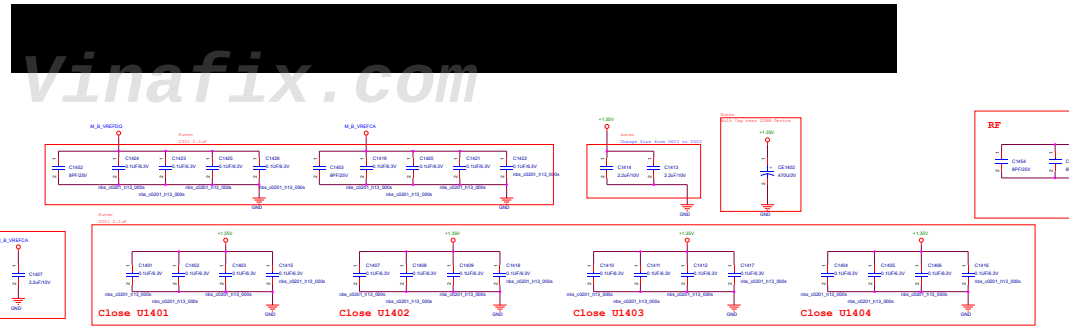
PCIE	
PCIE 1/USB3_3	ThunderBolt
PCIE 2/USB3_4	ThunderBolt
PCIE 3	WLAN
PCIE 4	Card Reader
PCIE 5	PCIE NGFF
PCIE 6	PCIE NGFF
PCIE 7	PCIE NGFF
PCIE 8	PCIE NGFF

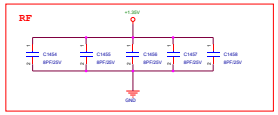
	Hynix(4Gb)	Micron(4Gb)	Hynix(8Gb)	Micron(8Gb)
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	L	L	L
DIMM_SEL2	L	L	H	H

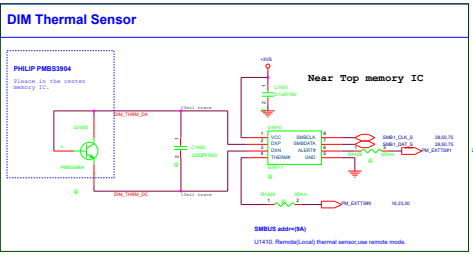
Title :	PCH-CPT(2)_PCIE,CLK,USB
Engineer:	RD1/EE1
Size	Custom
Project Name	N501JW
Rev	2.0
Date:	Monday, March 16, 2015
Sheet	21 of 98

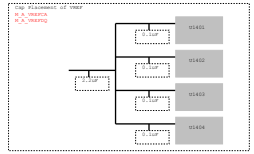
ASUSTeK COMPUTER INC. NB1

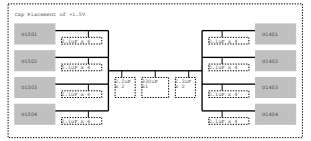




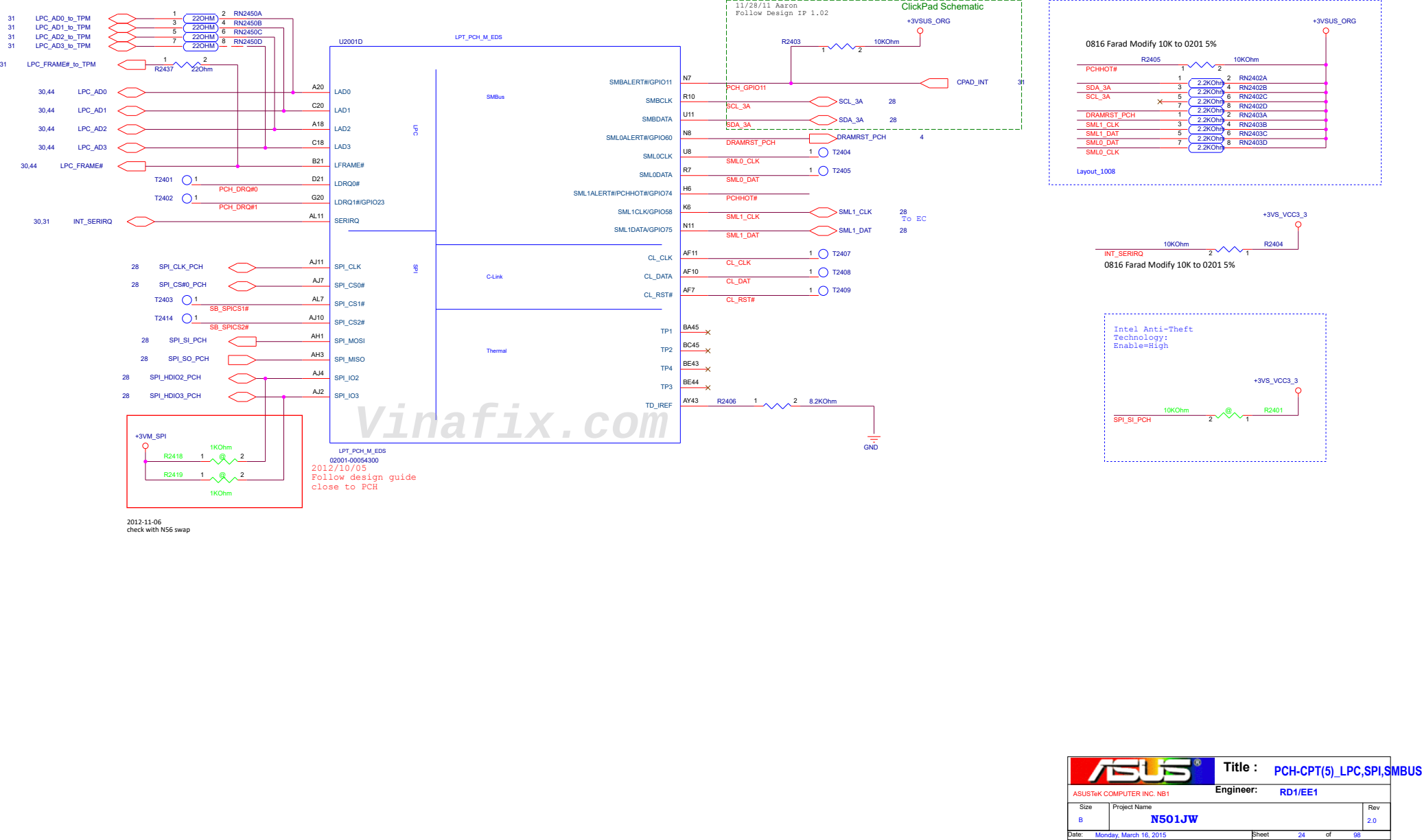








ASUSTeK COMPUTER INC.	Title :	DDR3_ON-BOARD_A	
	Engineer:	RD1/EE1	
Size: D	Project Name: N501JW		Rev: 0.0
Date: Monday, March 18, 2013	Sheet: 14 of 66		



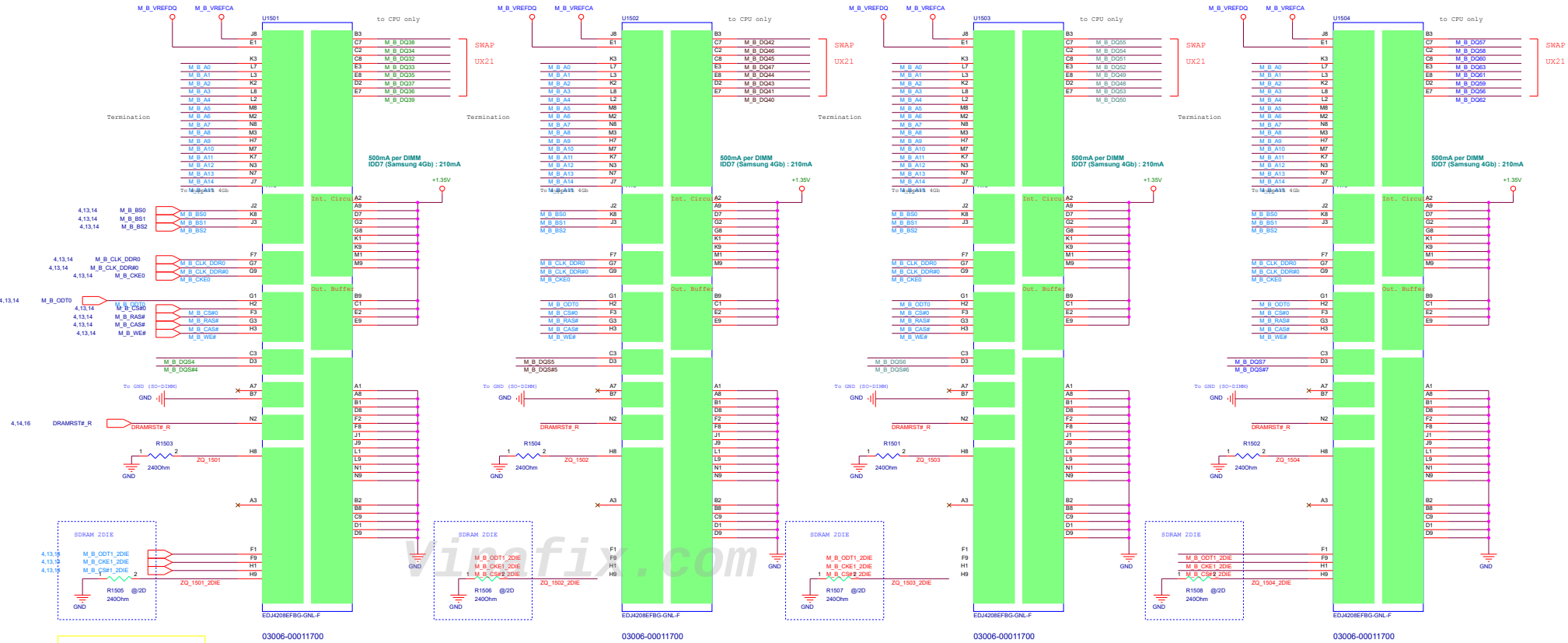
ASUSTeK COMPUTER INC. NB1	Title :	PCH-CPT(5)_LPC,SPI,SMBUS	
	Engineer:	RD1/EE1	
Size: B	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 24 of 98		

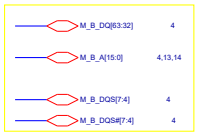
DQS4
DQ32~DQ39

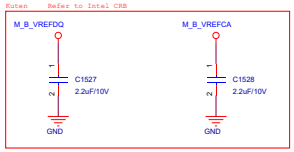
DQS5
DQ40~DQ47

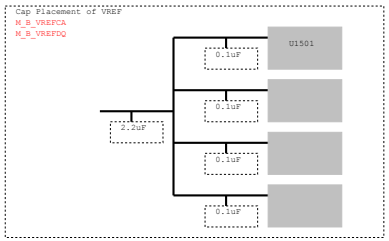
DQS6
DQ48~DQ55

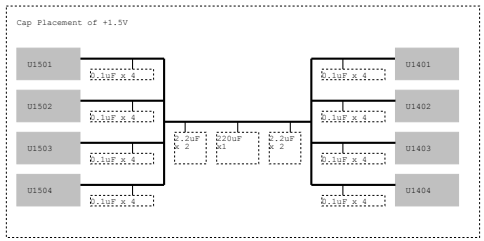
DQS7
DQ56~DQ63

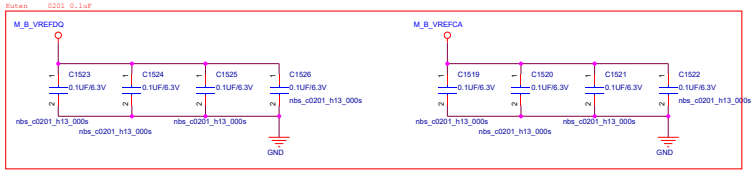


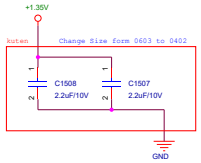


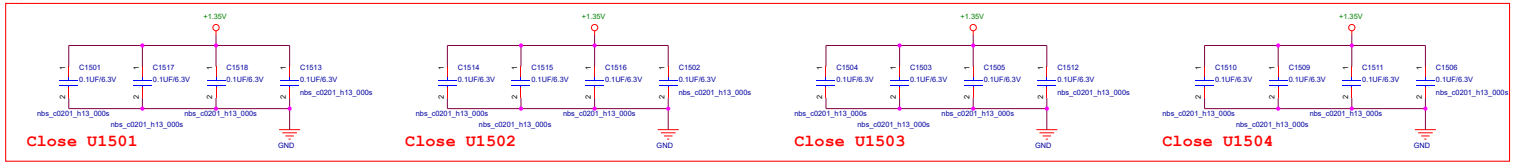












ASUSTeK COMPUTER INC.	Title :	DDR3_ON-BOARD_B	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 15 of 98		

For PCH debug with XDP,
NO STUFF all series paths
for GPIO usage

G750JS 011

G55VW R1.0 0804
From Thunderbolt

10 CIO_PLUG_EVENT R2524 0Ohm /TBT
nbs_r0201_h12_000s

+3VS_VCC3_3

R2506 1% 3.3KOhm S_GPIO

N501 0530

30 EXT_SMI#

T2508 TMDS_HDMI_HPD
T2509 USB3_SMI#
T2540 PCH_GPIO8
T2510 LAN_PHY_PWR_EN

56 WLAN_BT_LED R2517 0Ohm

PCH XDP

21,70 DGPU_PWROK

R1.1-4

56 WLAN_LED

2012/3/2

30 PCH_GPIO27# R2546 0Ohm

54 DSW_WAKE#

54 WLAN_ON# R2508 0Ohm

2012/3/1

PCH XDP
PCH XDP
PCH XDP

GC6_2.0

75,77 DGPU_FB_CLAMP_GPIO R2561 /GC6 20 0Ohm

GND R2525 100KOhm

PCH XDP

54 BT_ON

T2541 SATA_ODD_PWRGT

10KOhm R2531 GPIO69
+3VS_VCC3_3 10KOhm R2529 GPIO70
10KOhm R2530 GPIO71

Any GPIO that is configured as GPI (inputs)
and is unused must be terminated to their reference
voltage through a weak pull-up resistor (8.2 k -10 k).

0815 Farad Modify 10K to 0201 5%

U2001F LPT_PCH_M_EDS

AT8	BMBUSY#/GPIO0
F13	TACH1/GPIO1
A14	TACH2/GPIO6
G15	TACH3/GPIO7
Y1	GPIO8
K13	LAN_PHY_PWR_CTRL/GPIO12
AB11	GPIO15
AN2	SATA4GP/GPIO16
C14	TACH0/GPIO17
BB4	SCLOCK/GPIO22
Y10	GPIO24
R11	GPIO27
AD11	GPIO28
AN6	GPIO34
AP1	GPIO35/NMI#
AT3	SATA2GP/GPIO36
AK1	SATA3GP/GPIO37
AT7	SLOAD/GPIO38
AM3	SDATAOUT0/GPIO39
AN4	SDATAOUT1/GPIO48
AK3	SATA5GP/GPIO49
U12	GPIO57
C16	TACH4/GPIO68
D13	TACH5/GPIO69
G13	TACH6/GPIO70
H15	TACH7/GPIO71

CPU/Misc

TP14	AN10	A20GATE 30
PECI	AY1	T2503 PECI
RCIN#	AT6	RCIN# RCIN# 30
PROCPWRGD	AV3	H_CPUPWRGD H_CPUPWRGD 3
THRMTRIP#	AV1	R2512 390Ohm H_THRMTRIP# 3
PLTRST_PROC#	AU4	PM_THRMTRIP# PCH_PLTRST_CPU 3
VSS5	N10	

GPIO

VSS6	A2
VSS7	A41
VSS8	A43
VSS9	A44
VSS10	B1
VSS11	B2
VSS12	B44
VSS13	B45
VSS14	BA1
VSS15	BC1
VSS16	BD1
VSS17	BD2
VSS18	BD44
VSS19	BD45
VSS20	BE2
VSS21	BE3
VSS22	D1
VSS23	E1
VSS24	E45
VSS25	A4

NCTF

BE41	VSS1
BE5	VSS2
C45	VSS3
A5	VSS4

GND

LPT_PCH_M_EDS
02001-00054300

2012/10/8
Intel feedback for GPIO27 isolation

+3VA_EC

N501 0618

(EC) (PCH)

PCH_GPIO27# DSW_WAKE#

Q2501 2N7002ET1G @

For 2014 CPU

486713 PDG P616
THRMTRIP# buffer for 2014 Processor is open-drain
Need PH 470 ~1K to PCH 1.05VS

+VTT_PCH_VCC

R2539 @ 1KOhm

PM_THRMTRIP#

2012/12/28
For EMI request

H_CPUPWRGD

C2501 0.01UF/16V @

GND

DMI & FDI Termination Voltage	
NV_CLE	LOW : Set to Vss
	HIGH : Set to Vcc

CRB

+3VSUS_ORG

R2526 1KOhm WLAN_BT_LED
R2527 @ 10KOhm USB20_SEL
R2532 @ 10KOhm LAN_PHY_PWR_EN

+3VS_VCC3_3

R2528 10KOhm TMDS_HDMI_HPD
R2515 10KOhm STP_PCI#
R2540 10KOhm WLAN_LED
R2541 10KOhm CRIT_TEMP_REP#_R
R2537 10KOhm EXT_SMI#
R2538 10KOhm USB3_SMI#
R2523 @NO_GC6 10KOhm TEST_SET_UP
R2518 10KOhm MFG_MODE
R2513 10KOhm SATA_DET#4_R

R1.1-4

GC6_2.0

R1.1-X

R2510 1MOhm DGPU_PWROK
R2535 @ 10KOhm SATA_PWR_EN#1_R

GND

+3VSUS_ORG

R2536 10KOhm PLL_ODVR_EN
R2534 @ 1KOhm

GPIO28(On-Die PLL VR):
High:Enable (default), Low:Disable

GND

+VCCPDSW

R2533 @ 10KOhm LAN_PHY_PWR_EN
R2511 10KOhm DSW_WAKE#
R2514 @ 10KOhm

GND

+3VS_VCC3_3

R2519 10KOhm GFX_CRB_DET
R2521 @ 10KOhm

GND

0815 Farad Modify 1K & 10K to 0201 5%

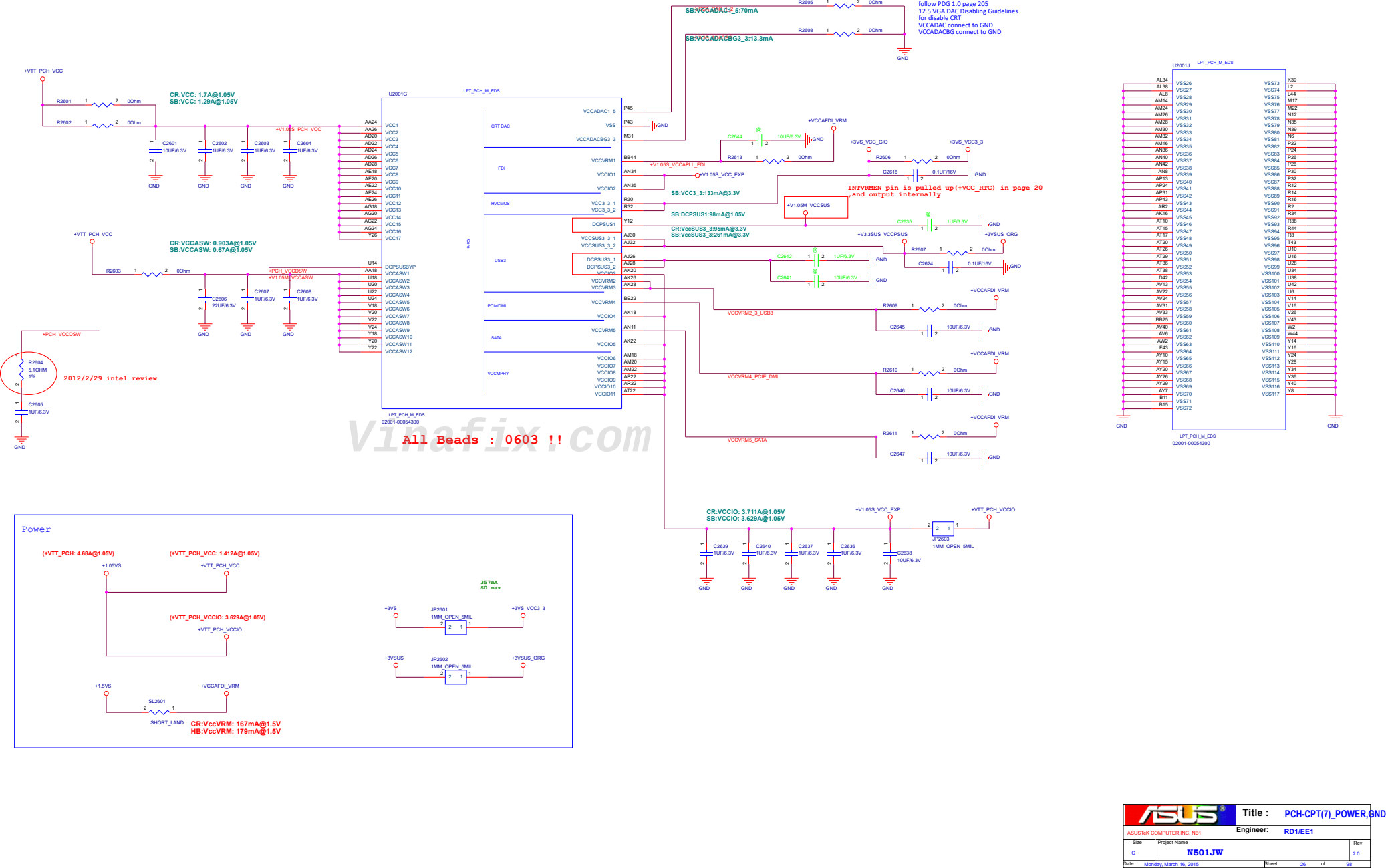
+3VS_VCC3_3

R2509 200KOhm SATA_ODD_PRSNT#_R
R2545 @ 200KOhm FDI_OVRVLTG
R2520 100KOhm

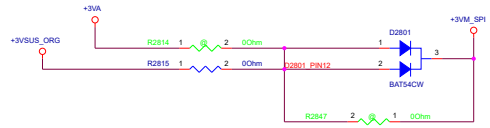
FDI&DMI Termination Voltage Override

GND

ASUSTeK COMPUTER INC. NB1	Title :	PCH-CPT(6)_GPIO,MISC	
	Engineer:	RD1/EE1	
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 25 of 98		


follow PDG 1.0 page 205
12.5 VGA DAC Disabling Guidelines
for disable CRT
VCCADAC connect to GND
VCCADACBG connect to GND
SB:VCCADAC1_5:70mA
SB:VCCADACBG3_3:13.3mA
CR:VCC: 1.7A@1.05V
SB:VCC: 1.29A@1.05V
CR:VCCASW: 0.903A@1.05V
SB:VCCASW: 0.67A@1.05V
2012/2/29 intel review
INTVRMEN pin is pulled up(+VCC_RTC) in page 20
and output internally
SB:VCC3_3:133mA@3.3V
SB:DCPSUS1:98mA@1.05V
CR:VccSUS3_3:95mA@3.3V
SB:VccSUS3_3:261mA@3.3V
CR:VCCIO: 3.711A@1.05V
SB:VCCIO: 3.629A@1.05V
All Beads : 0603 !!
Power
(+VTT_PCH: 4.68A@1.05V)
(+VTT_PCH_VCC: 1.412A@1.05V)
(+VTT_PCH_VCCIO: 3.629A@1.05V)
357mA
SO max
CR:VccVRM: 167mA@1.5V
HB:VccVRM: 179mA@1.5V
Title : PCH-CPT(7)_POWER,GND
ASUSTeK COMPUTER INC. NB1
Engineer: RD1/EE1
Project Name N501JW
Monday, March 16, 2015

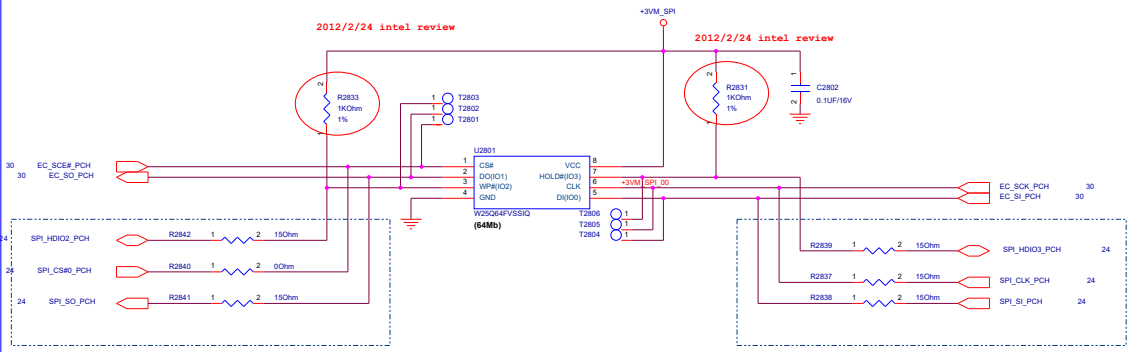
SPI Power



SPI

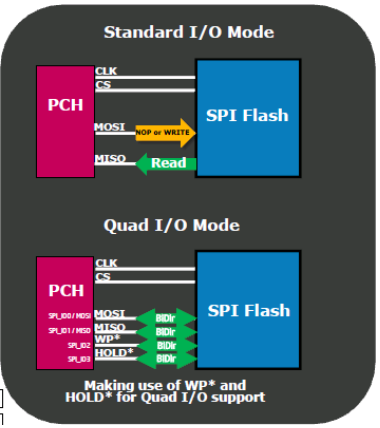
Main: 05006-00010500 (fixed quad bit)

second: ?

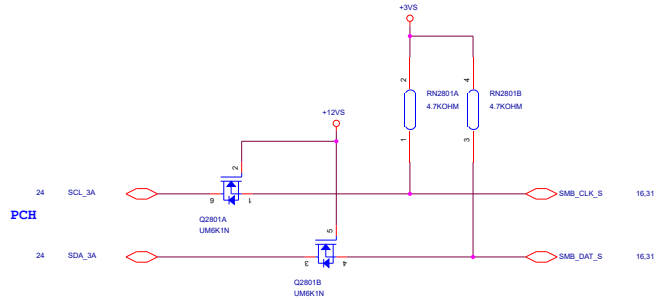


8585 built in eFlash(128k)

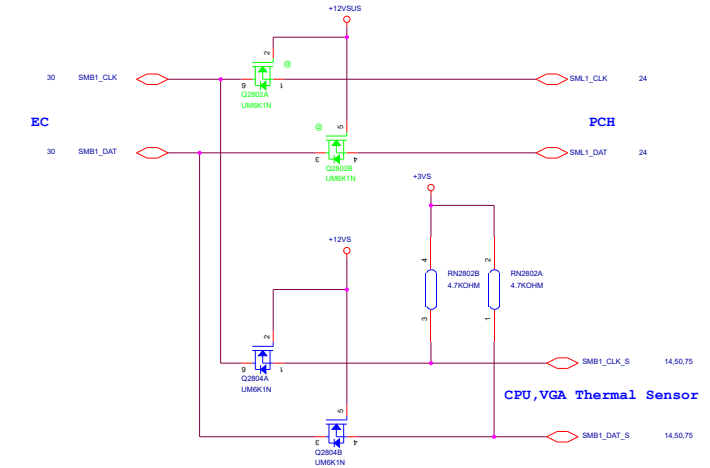
Shark Bay support Quad I/O Mode
EC 8521



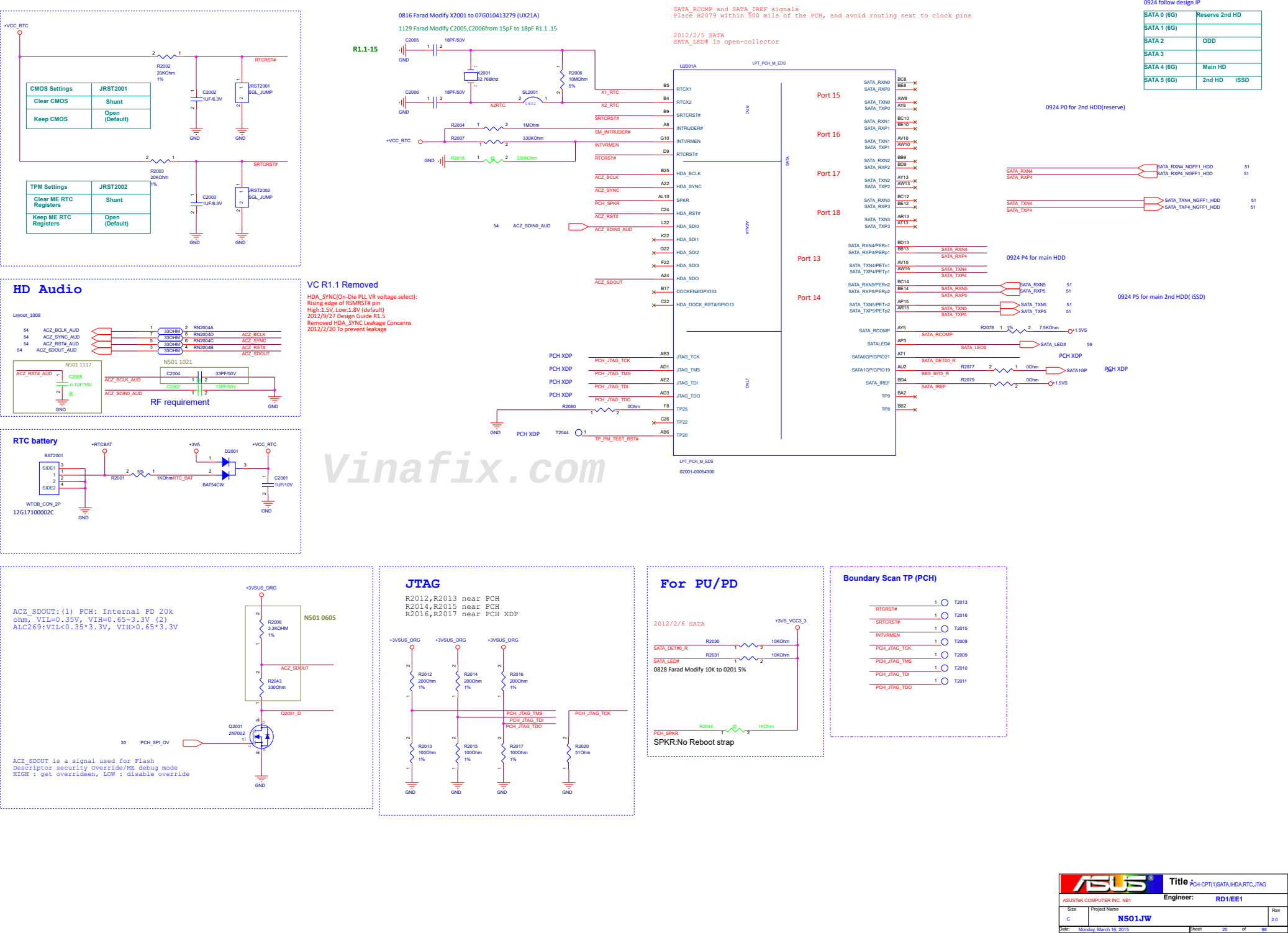
SMBus Interface



System Management Interface



ASUSTeK COMPUTER INC. NB1	Title : PCH-SPI ROM,OTH	
	Engineer: RD1/EE1	
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 28 of 98	


+VCC_RTC
R2002 20KOhm 1%
RTCRST#
C2002 1UF/6.3V
JRST2001 SGL_JUMP
GND
CMOS Settings | JRST2001
Clear CMOS | Shunt
Keep CMOS | Open (Default)
R2003 20KOhm 1%
SRTCRST#
C2003 1UF/6.3V
JRST2002 SGL_JUMP
TPM Settings | JRST2002
Clear ME RTC Registers | Shunt
Keep ME RTC Registers | Open (Default)
0816 Farad Modify X2001 to 07G010413279 (UX21A)
1129 Farad Modify C2005,C2006from 15pF to 18pF R1.1 .15
R1.1-15
C2005 18PF/50V
C2006 18PF/50V
X2001 32.768khz
SL2001 0402
R2006 10MOhm 5%
X1_RTC
X2_RTC
X2RTC
R2004 1MOhm
R2007 330KOhm
R2018 330KOhm
SM_INTRUDER#
INTVRMEN
RTCRST#
SRTCRST#
SATA_RCOMP and SATA_IREF signals
Place R2079 within 500 mils of the PCH, and avoid routing next to clock pins
2012/2/5 SATA
SATA_LED# is open-collector
U2001A
LPT_PCH_M_EDS
RTC
SATA
AZALIA
JTAG
RTCX1
RTCX2
SRTCRST#
INTRUDER#
INTVRMEN
RTCRST#
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDI2
HDA_SDI3
HDA_SDO
DOCKEN#/GPIO33
HDA_DOCK_RST#/GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TP25
TP22
TP20
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
ACZ_SDIN0_AUD
PCH_SPKR
PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
TP_PM_TEST_RST#
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3
SATA_RXN4/PERn1
SATA_RXP4/PERp1
SATA_TXN4/PETn1
SATA_TXP4/PETp1
SATA_RXN5/PERn2
SATA_RXP5/PERp2
SATA_TXN5/PETn2
SATA_TXP5/PETp2
SATA_RCOMP
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_IREF
Port 15
Port 16
Port 17
Port 18
Port 13
Port 14
0924 follow design IP
SATA 0 (6G) | Reserve 2nd HD
SATA 1 (6G) |
SATA 2 | ODD
SATA 3 |
SATA 4 (6G) | Main HD
SATA 5 (6G) | 2nd HD iSSD
0924 P0 for 2nd HDD(reserve)
SATA_RXN4_NGFF1_HDD
SATA_RXP4_NGFF1_HDD
SATA_TXN4_NGFF1_HDD
SATA_TXP4_NGFF1_HDD
0924 P4 for main HDD
0924 P5 for main 2nd HDD(iSSD)
R2078 7.5KOhm
R2077 0Ohm
R2079 0Ohm
1.5VS
SATA_DET#0_R
BBS_BIT0_R
PCH XDP
SATA1GP
HD Audio
Layout_1008
ACZ_BCLK_AUD
ACZ_SYNC_AUD
ACZ_RST#_AUD
ACZ_SDOUT_AUD
RN2004A 33OHM
RN2004D
RN2004C
RN2004B
N501 1117
C2008 0.1UF/16V
N501 1021
C2004 33PF/50V
C2007 15PF/50V
RF requirement
VC R1.1 Removed
HDA_SYNC(On-Die PLL VR voltage select):
Rising edge of RSMRST# pin
High:1.5V, Low:1.8V (default)
2012/9/27 Design Guide R1.5
Removed HDA_SYNC Leakage Concerns
2012/2/20 To prevent leakage
RTC battery
+RTCBAT
+3VA
+VCC_RTC
BAT2001
SIDE1
SIDE2
WTOB_CON_2P
12G17100002C
R2001 5K 1KOhm
RTC_BAT
D2001 BAT54CW
C2001 1UF/10V
ACZ_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V (2) ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V
+3VSUS_ORG
R2008 3.3KOHM 1%
N501 0605
ACZ_SDOUT
R2043 330Ohm
Q2001_D
Q2001 2N7002
30 PCH_SPI_OV
ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override
JTAG
R2012,R2013 near PCH
R2014,R2015 near PCH
R2016,R2017 near PCH XDP
R2012 200Ohm 1%
R2014 200Ohm 1%
R2016 200Ohm 1%
R2013 100Ohm 1%
R2015 100Ohm 1%
R2017 100Ohm 1%
R2020 51Ohm
For PU/PD
2012/2/6 SATA
+3VS_VCC3_3
R2030 10KOhm
R2031 10KOhm
0828 Farad Modify 10K to 0201 5%
R2044 1KOhm
SPKR:No Reboot strap
Boundary Scan TP (PCH)
T2013
T2016
T2015
T2008
T2009
T2010
T2011
Vinafix.com
Title : PCH-CPT(1)SATA,IHDA,RTC,JTAG
ASUSTeK COMPUTER INC. NB1
Engineer: RD1/EE1
Size C
Project Name N501JW
Rev 2.0
Date: Monday, March 16, 2015
Sheet 20 of 98

Title : PCH-XDP

ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

Size	Project Name	Rev
A	N501JW	2.0

Date: Monday, March 16, 2015

Sheet 29 of 98

DMI_IREF and DMI_RCOMP signals
Avoid routing next to clock pins or noisy signals

FDI_IREF and FDI_RCOMP signals
Avoid routing next to clock pins or noisy signals

Note

SUSACK#:
SUSACK# and SUSWARN# can be tied together
if EC does not want to involve in handshake
mechanism for the Deep Sleep state entry and exit.

APWROK:
For platform not supporting iAMT
it can be connected to PWROK.

SUSPWRDNACK (PCH to EC):
This pin requires a pull-up to +3VSUS.
Platforms are not expected to use this
signal when the PCH's Deep S4/S5 feature is used.

SUSWARN# (PCH to EC):
This pin aserts low when PCH is planning
to enter the DeepEx power state and remove
Suspend power(using SLP_SUS#)

Entry Into Deep S4/S5
A combination of condition is required for entry into Deep S4/S5
All of the following must be met:
-Intel ME in Moff.
-AND either a or b(EDS R0.7v1 p.186).

R2212 can be removed in MP
if XDP no used

ASW Power well stable for at least 1ms
before platform logic asserts APWROK

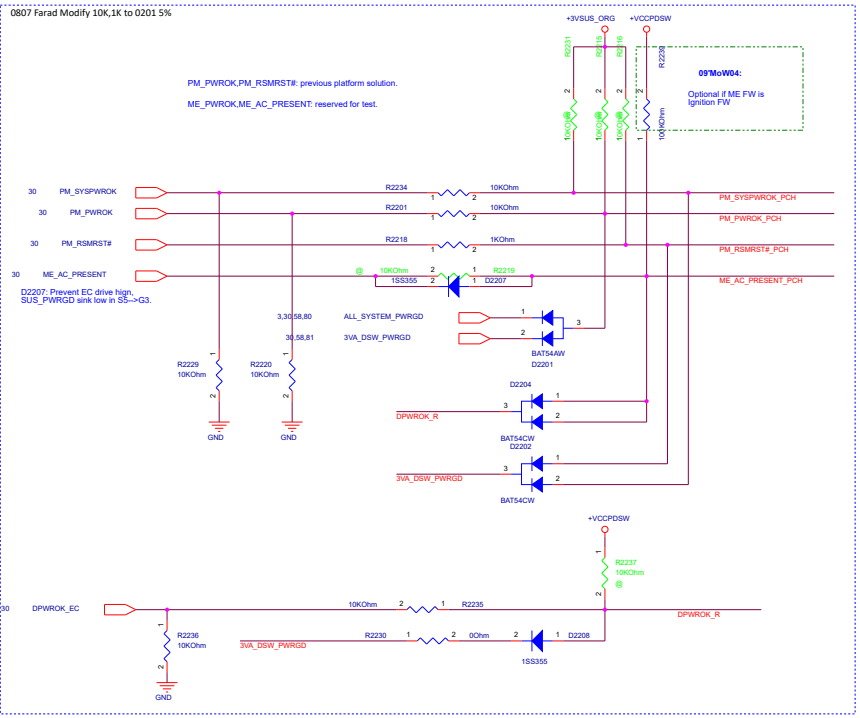
SL2214 Use:
With AMT unstuff,Without AMT stuff

N501 0530

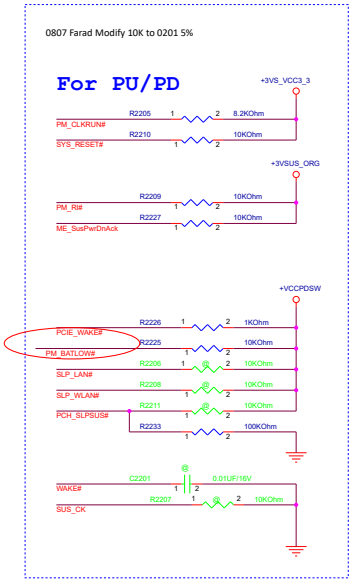
2012/3/2

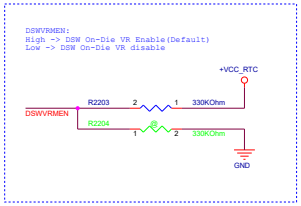
2012/3/1

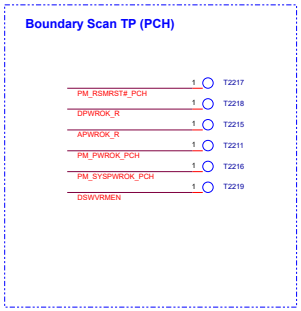
N501 0811 EMI request



Power failure solution (S0-->G3,S5-->G3):

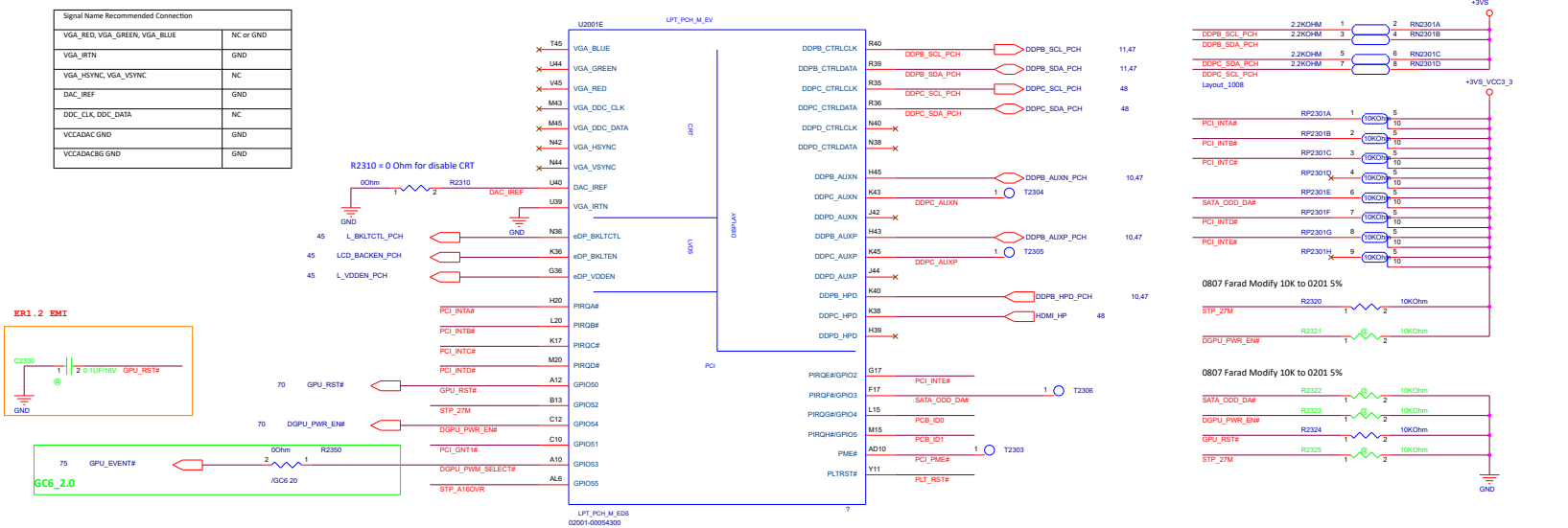




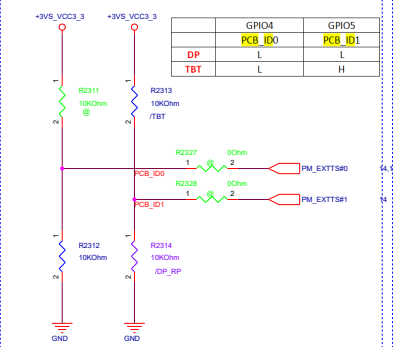


ASUSTeK COMPUTER INC. NB1	Title :	PCH-CPT(3)_FDI,DMI,SYS PWR	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 22 of 98		

Signal Name Recommended Connection	
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC GND	GND
VCCADACBG GND	GND



PCB ID



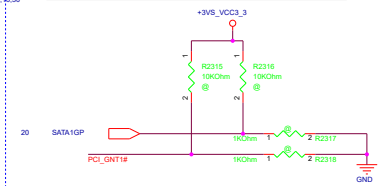
	GPIO4	GPIO5
	PCB_ID0	PCB_ID1
DP	L	L
TBT	L	H

0807 Farad Modify 10K to 0201 5%

Boot BIOS Strap : GNT1#, SATA1GP

Boot BIOS Strap ,Sampled on rising edge of PWROK.
Default PU 20K OHM

GNT1#(BBS1)	SATA1GP(BBS0)	Boot BIOS Location
0	1	Reserved
1	0	- - -
1	1	SPI (PCH)
0	0	LPC

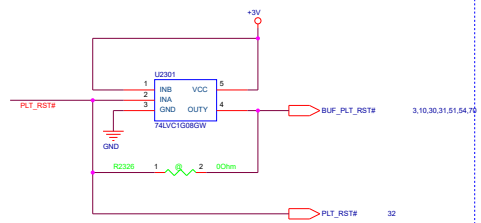


0807 Farad Modify 10K,1K to 0201 5%

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

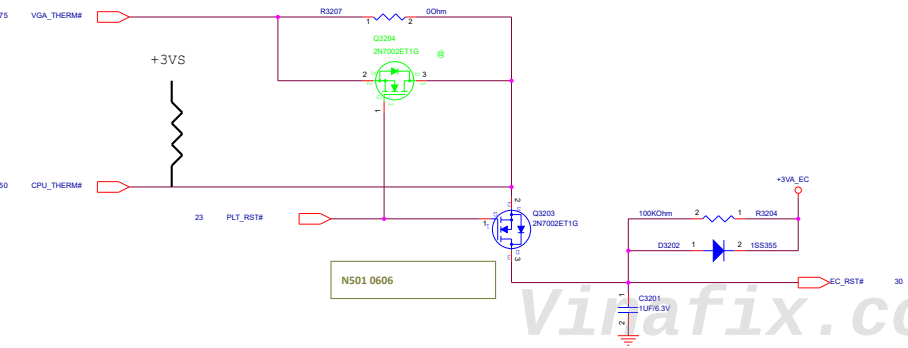
0807 Farad Modify 1K to 0201 5%



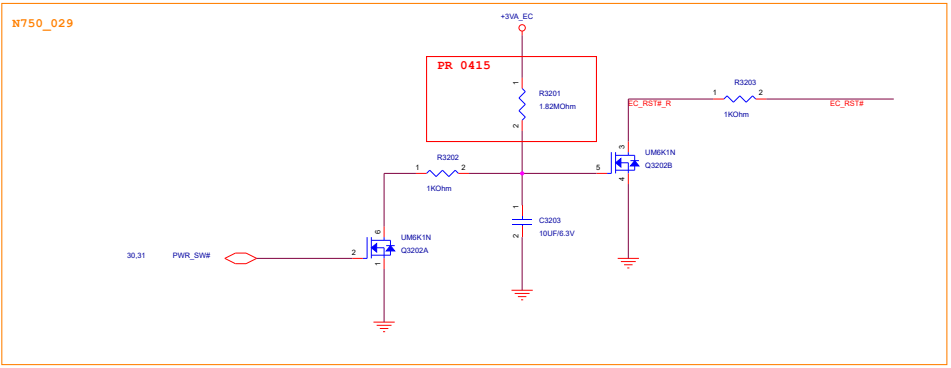
Title :	PCH-CPT(4)_CRT,eDP,PCI,DP
Engineer:	RD1/EE1
ASUSTeK COMPUTER INC. NB1	
Size: C	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 23 of 98

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.

Reset Circuit



battery embedded (press pwr_sw 10sec, then reset ec)



ASUSTeK COMPUTER INC. NB1	Title : RST_Reset Circuit	
	Engineer: RD1/EE1	
Size: B	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 32 of 98	

Title : LAN-RTL8112G-CG

Engineer:

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom		2.0

Date:	Monday, March 16, 2015	Sheet	33	of	98

Title : LAN RJ45

ASUSTeK COMPUTER INC. NB4

Engineer: RD1/EE1

Size	Project Name	Rev
B	N501JW	2.0

Date: Monday, March 16, 2015

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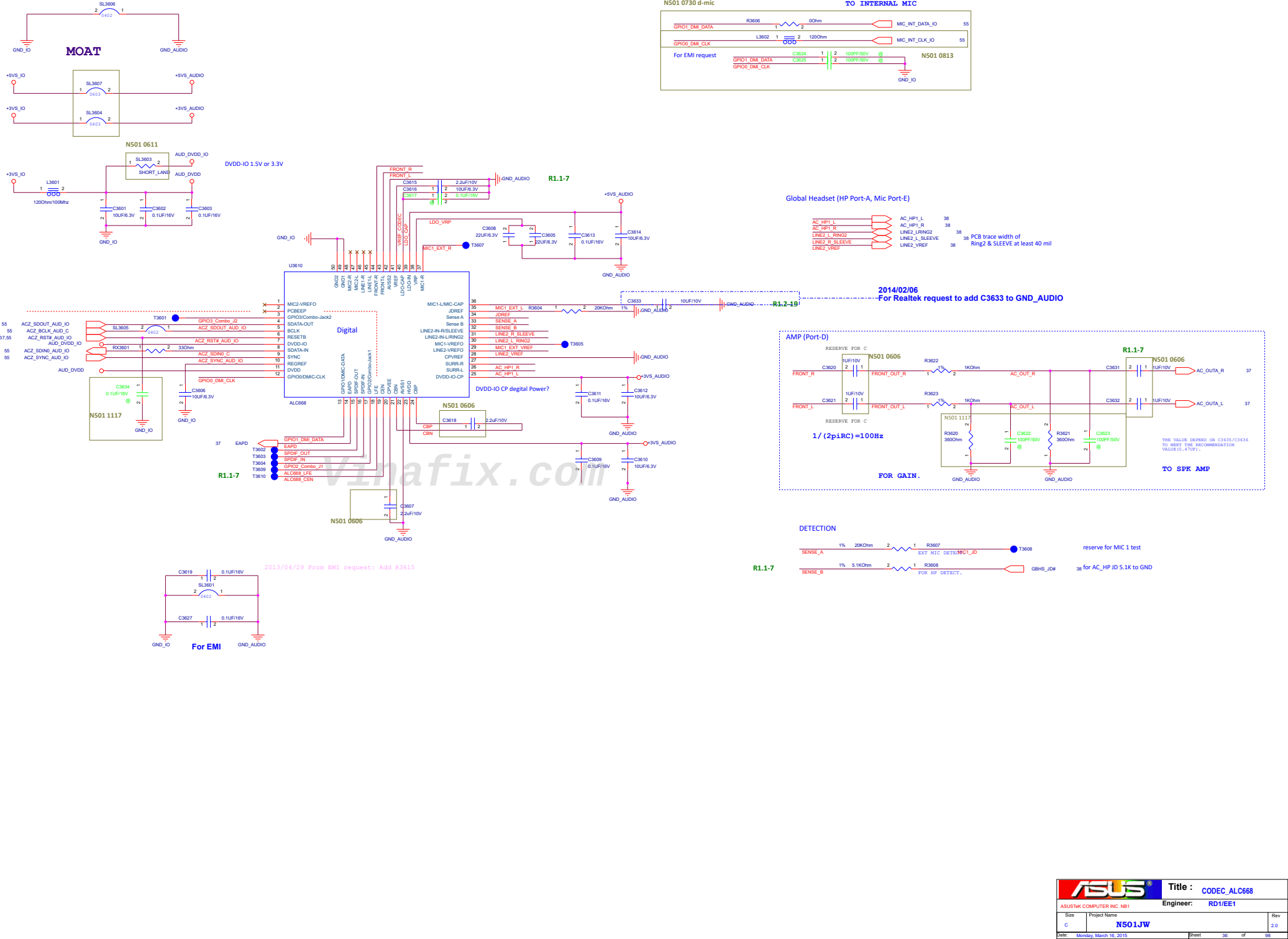
Title : LAN_*****

ASUSTeK COMPUTER INC. NB3

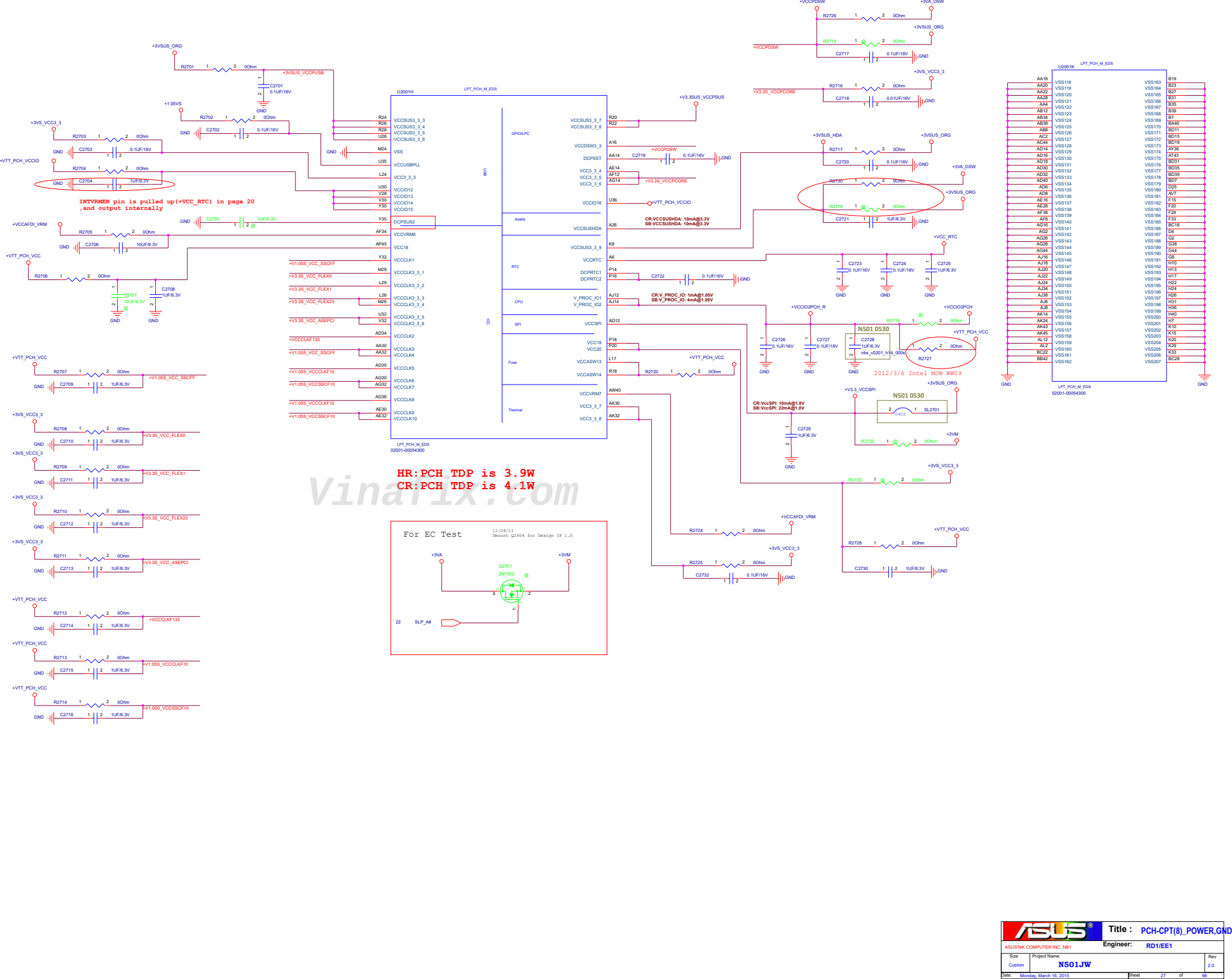
Engineer: RD1/EE1

Size	Project Name	Rev
C	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 35 of 98

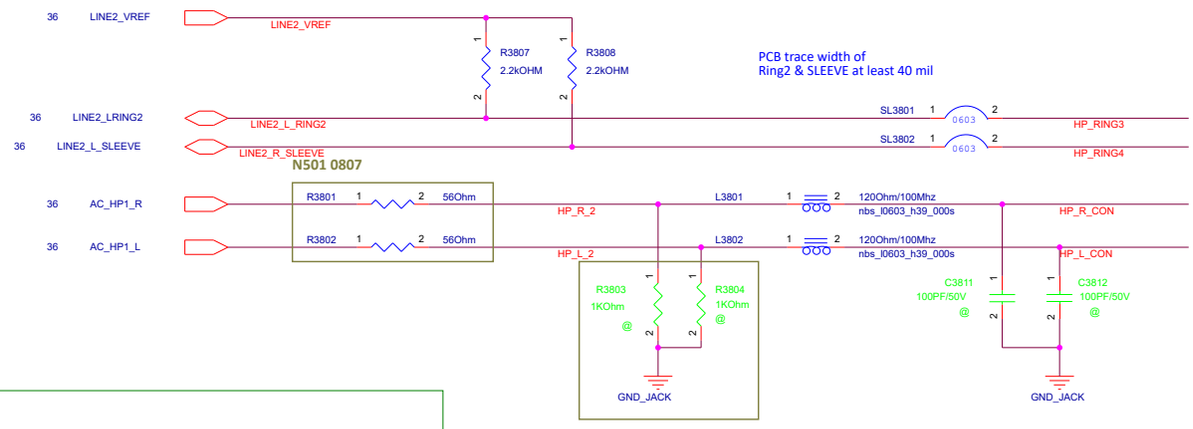


Title :	CODEC_ALC668
Engineer:	RD1/EE1
ASUSTeK COMPUTER INC. NB1	
Size: C	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 36 of 98



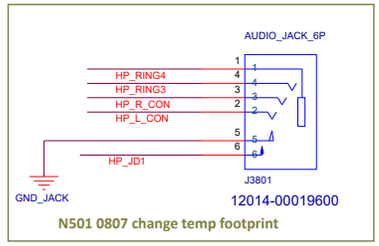
Title :	PCH-CPT(8)_POWER,GND
ASUSTeK COMPUTER INC. NB1	Engineer: RD1/EE1
Size: Custom	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 27 of 98

Global Headset (HP Port-A, Mic Port-E)



N501 0611 normal open

N501 0611 normal open

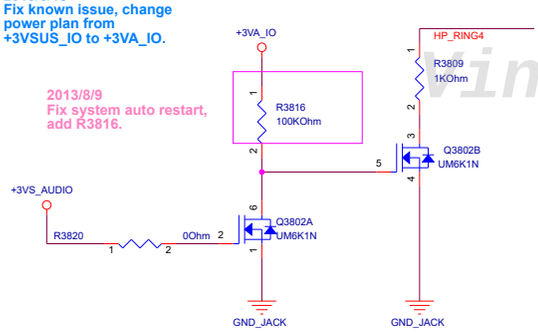


N501 0807 change temp footprint

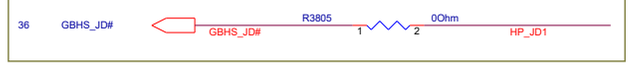
R1.1-X

2013/6/18
Fix known issue, change power plan from +3VSUS_IO to +3VA_IO.

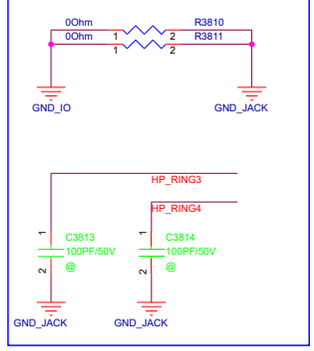
2013/8/9
Fix system auto restart, add R3816.



N501 0611 normal open



For EMI 01/14/13



2013/04/29 From EMI request: Change GND_audio to GND_JACK.

ASUSTeK COMPUTER INC. NB1	Title : Aud_HP Jack, MIC		
	Engineer: RD1/EE1		
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 38 of 98		

Note

Only 3V Torlence

GPB[3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPI [0 :7]
GPJ[0:7]

farad : BOM

For EMI 09/24/12

For EMI 12/13/12

Close U3001

Power

RF

N501 0811

N501 0808 EMI request

N501 0811 EMI request

R1.1-4

2012/10/8
Intel feedback

R1.1-X for usb charge disable

R1.1-1

ER need modify

IT8585VG/BX
02041-00140800
nbs_bga_128p_nonhdi_002

N501 0611 EMI

Colay 8585

PU/PD

for load code

ClickPad Schematic

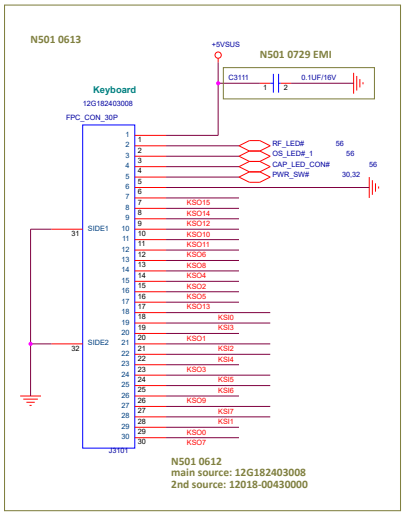
11/08/11
1. Add CHG_LED# Pull- high R3044 @
2. Add CHG_FULL_LED# Pull- high R3043 @

Title :	KBC_IT8585_C
Engineer:	RD1/EE1
ASUSTeK COMPUTER INC. NB1	
Size: C	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 30 of 98

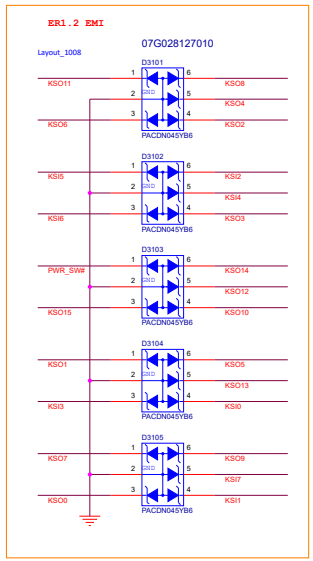
ASUSTeK COMPUTER INC. NB3	Title : iSSD_SANDISK	
	Engineer: RD1/EE1	
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 40 of 98	

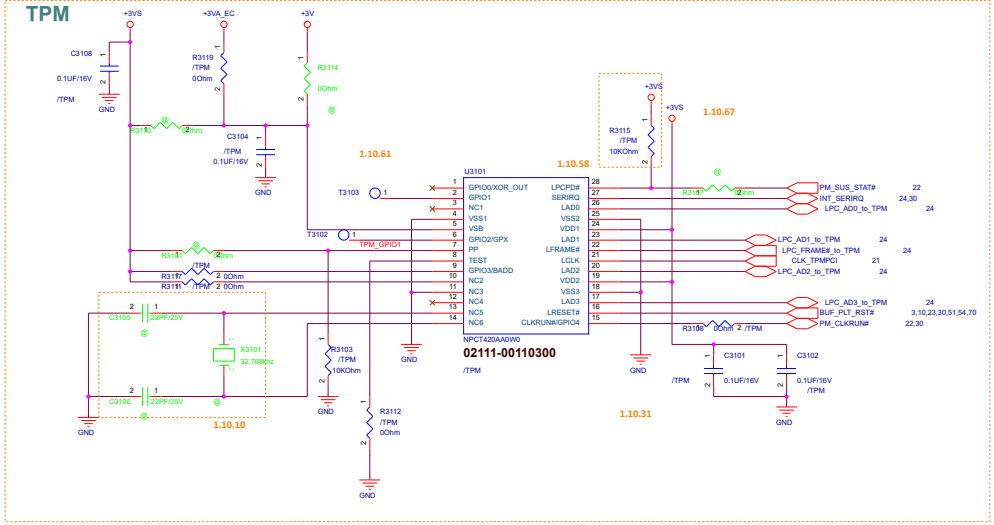
Keyboard Connector

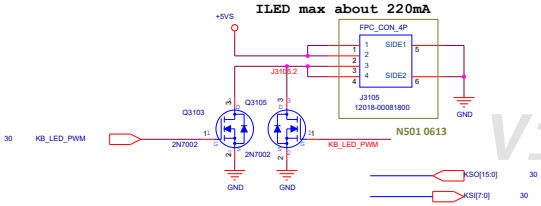
1st : 07G028021011 (EOL)
2nd : 07G028127010 (now)
2nd : 07G028162010

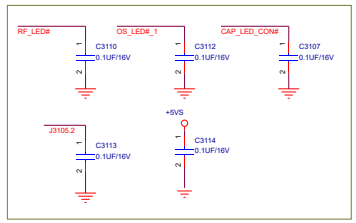


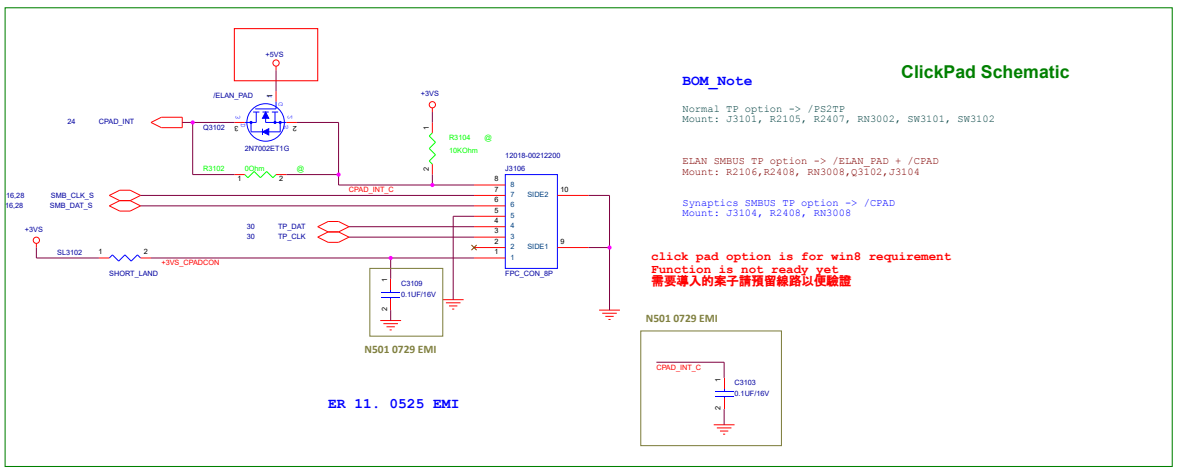
Reserved for EMI











BOM_Note

Normal TP option -> /PS2TP
Mount: J3101, R2105, R2407, RN3002, SW3101, SW3102

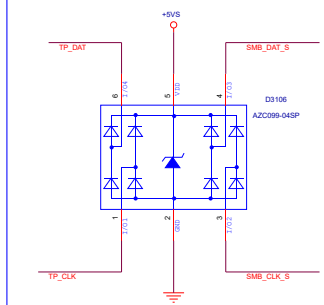
ELAN SMBUS TP option -> /ELAN_PAD + /CPAD
Mount: R2106,R2408, RN3008,Q3102,J3104

Synaptics SMBUS TP option -> /CPAD
Mount: J3104, R2408, RN3008

ClickPad Schematic

click pad option is for win8 requirement
Function is not ready yet
需要導入的案子請預留線路以便驗證

Reserved for EMI



ASUSTeK COMPUTER INC. NB1	Title :	KBC_KB & TP	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 31 of 98		

Title : CB_*****

ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

Size	Project Name	Rev
A	N501JW	2.0

Date: Monday, March 16, 2015

Sheet 41 of 98

Title : CB_*****

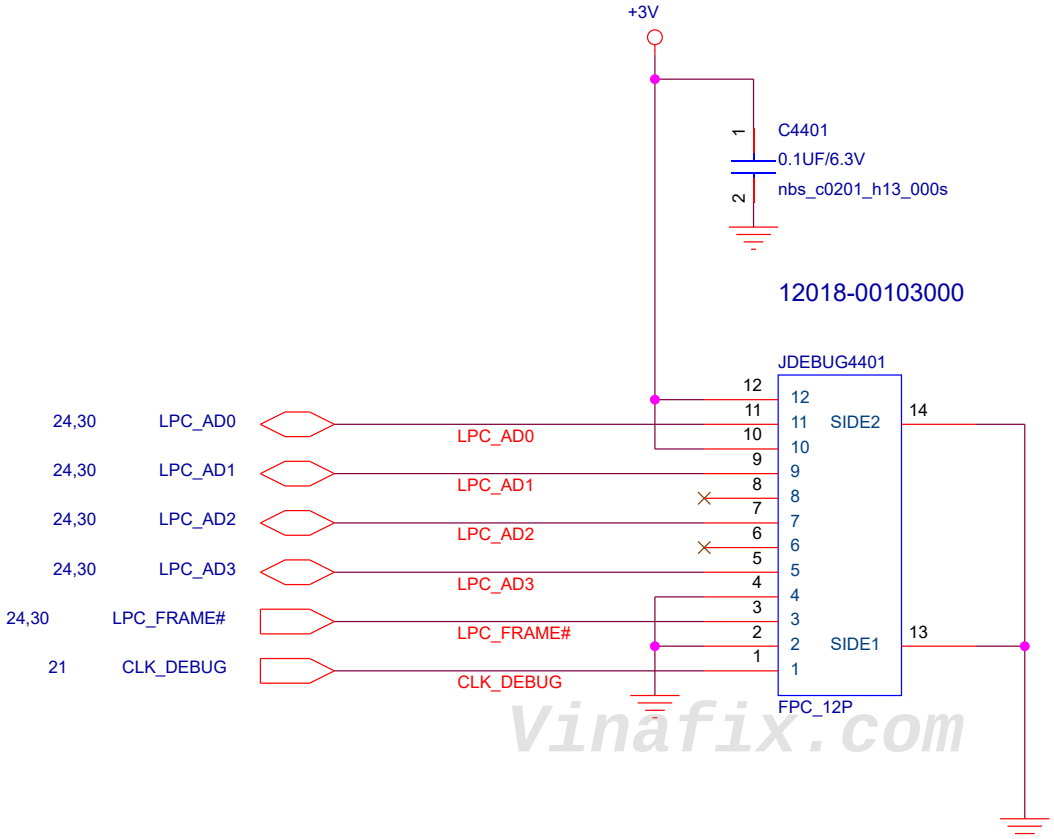
ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

Size	Project Name	Rev
A	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 43 of 98

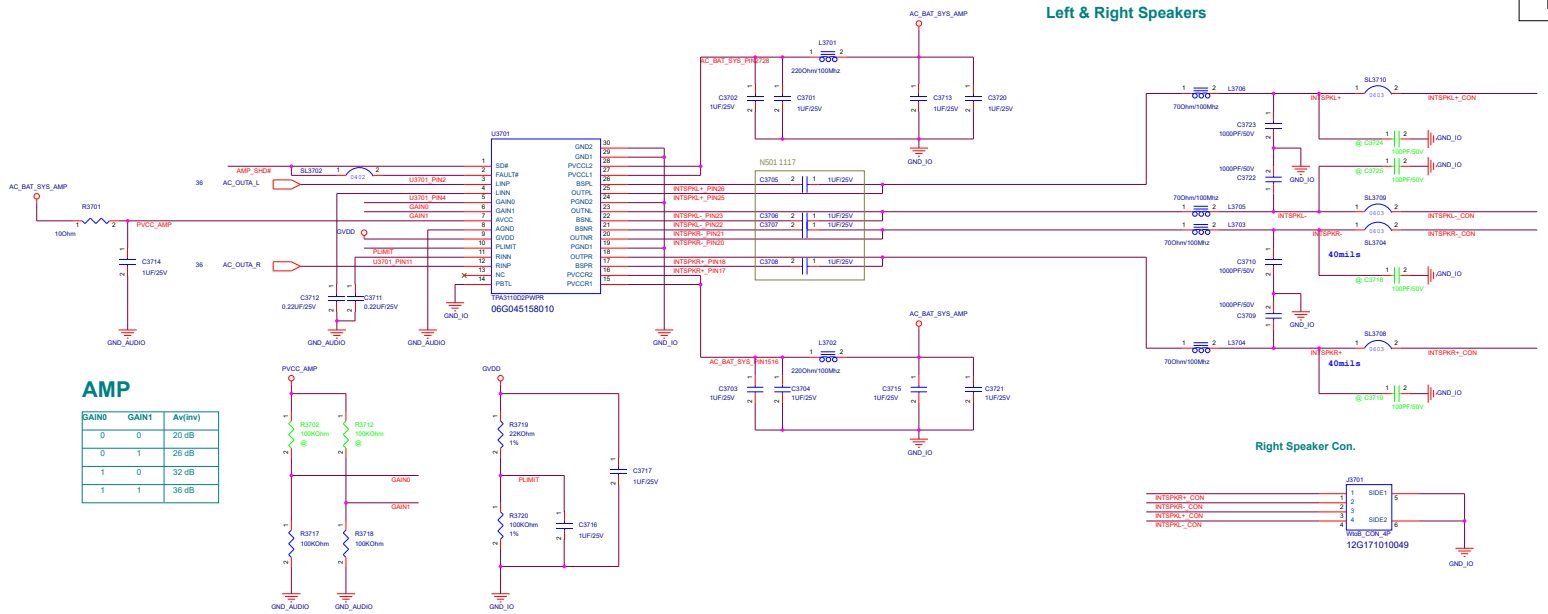
LPC Debug Port



Debug Connector Pool :
12G183401225 FPC CON 12P 0.5MM,R/A,SMTACES/88511-1241
躺式(掀)(X,Y,Z)10.2,5.8,2 nbfpc12p202hdraace
12G183401226 FPC CON 12P 0.5MM,R/A,SMTP-TWO/196210-12041
躺式(掀)(X,Y,Z)10.4,5.25,2 nbfpc12p202hdraace
12G183301208 FPC CON 12P,0.5mm,S/T,SMTACES/87152-12071
抽屜式(X,Y,Z) 10.4,6.3,1.9 nbs_fpc_12p_002c

ASUSTeK COMPUTER INC. NB3	Title : DEBUG_LPC	
	Engineer: RD1/EE1	
Size: A	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 44 of 98	

Left & Right Speakers



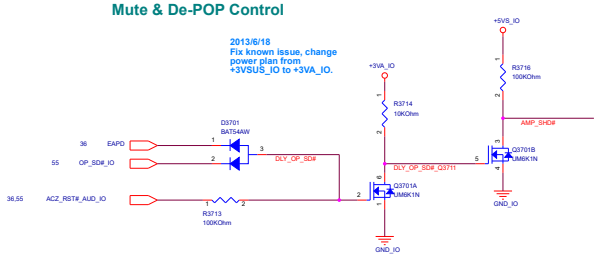
AMP

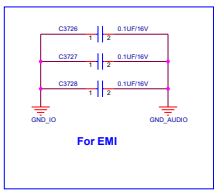
GAIN0	GAIN1	Av(inv)
0	0	20 dB
0	1	26 dB
1	0	32 dB
1	1	36 dB

Right Speaker Con.

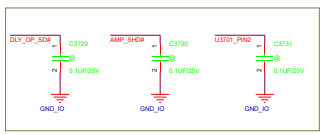
Mute & De-POP Control

2013/6/18
Fix known issue, change power plan from +3VSUS_IO to +3VA_IO.



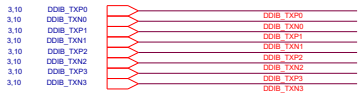


N501 1119



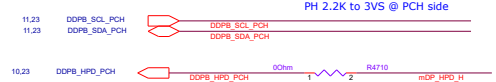
Title :	Aud_Spk,Woofer,MIC
Engineer:	RD1/EE1
ASUSTeK COMPUTER INC. NB1	
Size: Custom	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 37 of 98

DP from DDI Port B



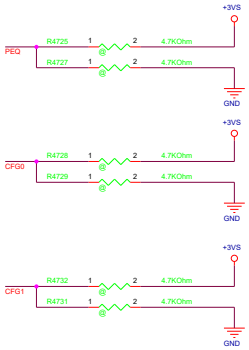
N501 0605 0201 co-lay

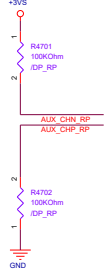
PH 2.2K to 3VS @ PCH side



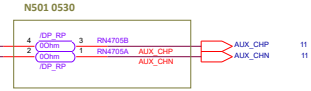
Note reversed source/drain connection on DDC_CLK isolation pass gate.

Follow Shark Bay PDG 1.0 P149
Figure 7-10. DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit

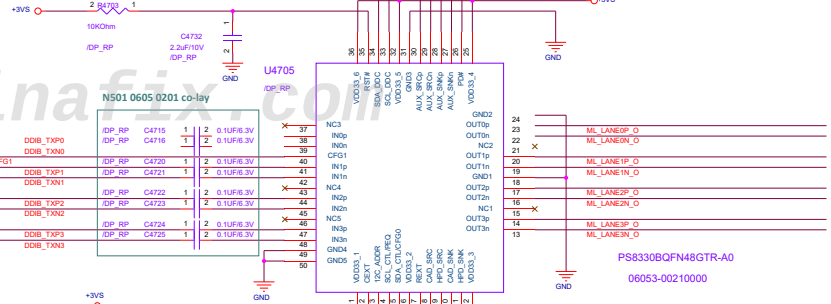




N501 0530

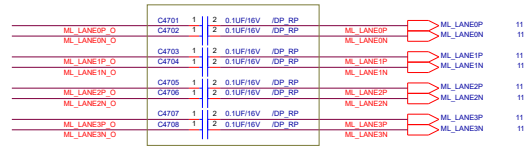


co-lay

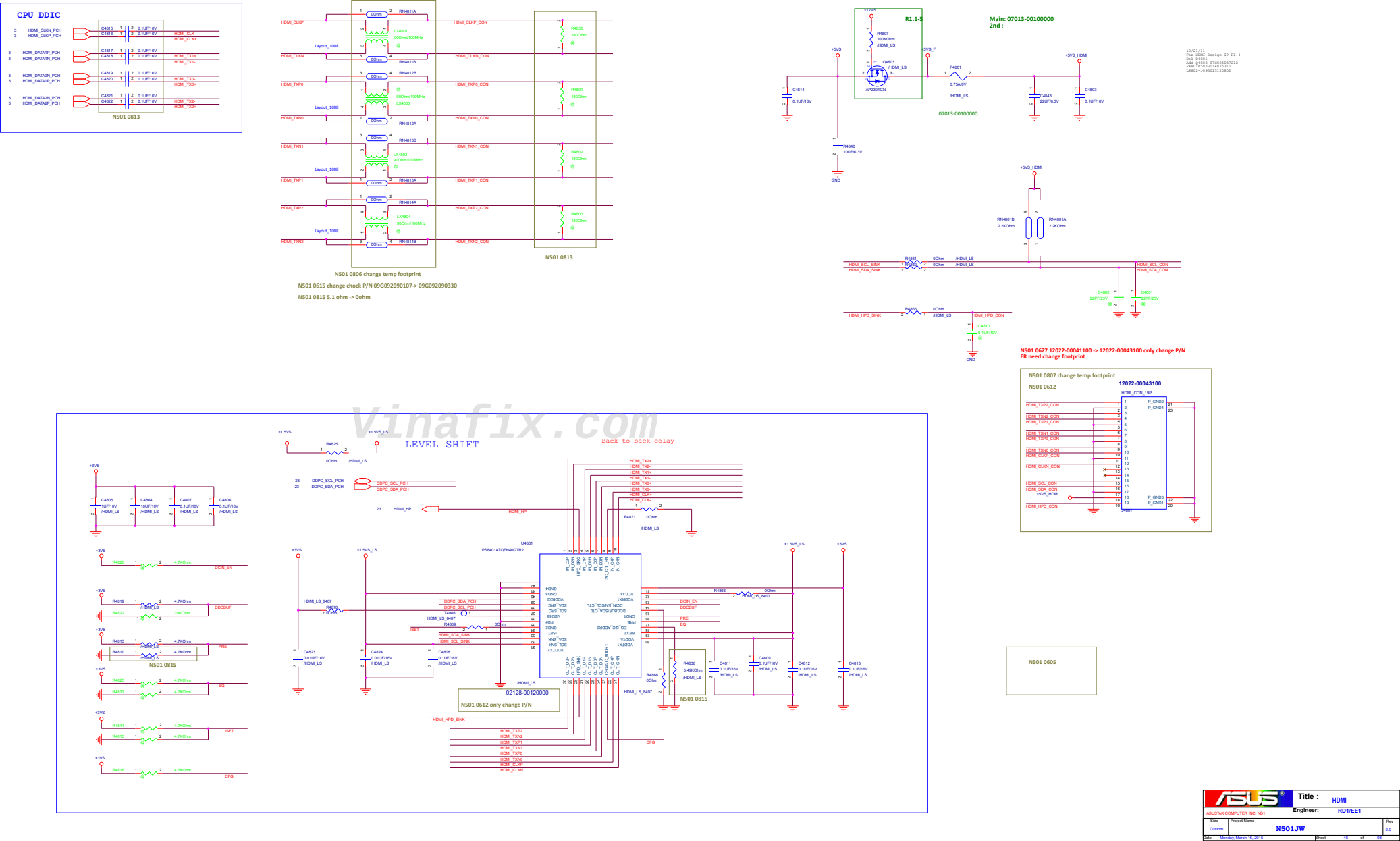


N501 0530

N501 0814



Title :	CRT_DP
Engineer:	RD1/EE1
ASUSTeK COMPUTER INC. NB3	
Size: Custom	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 47 of 98


CPU DDIC
HDMI_CLKN_PCH
HDMI_CLKP_PCH
HDMI_DATA1P_PCH
HDMI_DATA1N_PCH
HDMI_DATA0N_PCH
HDMI_DATA0P_PCH
HDMI_DATA2N_PCH
HDMI_DATA2P_PCH
0.1UF/16V
HDMI_CLK-
HDMI_CLK+
HDMI_TX1+
HDMI_TX1-
HDMI_TX0-
HDMI_TX0+
HDMI_TX2-
HDMI_TX2+
N501 0813
RN4811A
RN4811B
RN4812B
RN4812A
RN4813B
RN4813A
RN4814A
RN4814B
LX4801
LX4802
LX4803
LX4804
90Ohm/100MHz
0Ohm
HDMI_CLKP
HDMI_CLKN
HDMI_TXP0
HDMI_TXN0
HDMI_TXN1
HDMI_TXP1
HDMI_TXP2
HDMI_TXN2
HDMI_CLKP_CON
HDMI_CLKN_CON
HDMI_TXP0_CON
HDMI_TXN0_CON
HDMI_TXN1_CON
HDMI_TXP1_CON
HDMI_TXP2_CON
HDMI_TXN2_CON
R4800
R4801
R4802
R4803
180Ohm
Layout_1008
N501 0806 change temp footprint
N501 0615 change chock P/N 09G092090107-> 09G092090330
N501 0815 5.1 ohm -> 0ohm
Main: 07013-00100000
2nd :
R1.1-5
+5VS
+5VS_F
+5VS_HDMI
R4807
100KOhm
/HDMI_LS
Q4803
AP2304GN
F4801
0.75A/6V
C4814
C4843
22UF/6.3V
C4803
0.1UF/16V
R4640
10UF/6.3V
GND
07013-00100000
12/21/11
For HDMI Design IP R1.4
Del Q4801
Add Q4803 2700050472212
P4801=2679014675203
L4802=2696013120802
+5VS_HDMI
RN4801B
2.2KOhm
RN4801A
2.2KOhm
R4681
R4685
HDMI_SCL_SINK
HDMI_SDA_SINK
HDMI_HPD_SINK
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_HPD_CON
C4802
22PF/25V
C4801
C4810
0.1UF/10V
N501 0627 12022-00041100 -> 12022-00043100 only change P/N
ER need change footprint
N501 0807 change temp footprint
N501 0612
12022-00043100
HDMI_CON_19P
P4801
P_GND2
P_GND4
P_GND3
P_GND1
HDMI_TXP2_CON
HDMI_TXN2_CON
HDMI_TXP1_CON
HDMI_TXN1_CON
HDMI_TXP0_CON
HDMI_TXN0_CON
HDMI_CLKP_CON
HDMI_CLKN_CON
HDMI_SCL_CON
HDMI_SDA_CON
+5VS_HDMI
HDMI_HPD_CON
Vinafix.com
LEVEL SHIFT
Back to back colay
+1.5VS
+1.5VS_LS
+3VS
R4825
0Ohm
/HDMI_LS
C4805
10UF/10V
C4804
10UF/10V
C4807
0.1UF/16V
C4806
0.1UF/16V
DDPC_SCL_PCH
DDPC_SDA_PCH
HDMI_HP
R4871
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_CLK+
HDMI_CLK-
U4801
PS8401ATQFN40GTR2
R4820
4.7KOhm
DCIN_EN
R4819
R4822
10KOhm
DDCBUF
R4813
R4810
PRE
R4823
R4811
EQ
R4814
R4815
ISET
R4816
CFG
N501 0815
HDMI_LS_8407
R4870
2.49KOhm
R4869
C4823
0.01UF/16V
C4824
C4808
0.1UF/16V
R4866
R4838
5.49KOhm
C4811
C4609
C4812
C4813
02128-00120000
N501 0612 only change P/N
N501 0605
ASUSTeK COMPUTER INC. NB1
Title : HDMI
Engineer: RD1/EE1
Size: Custom
Project Name: N501JW
Rev: 2.0
Date: Monday, March 16, 2015
Sheet 48 of 98

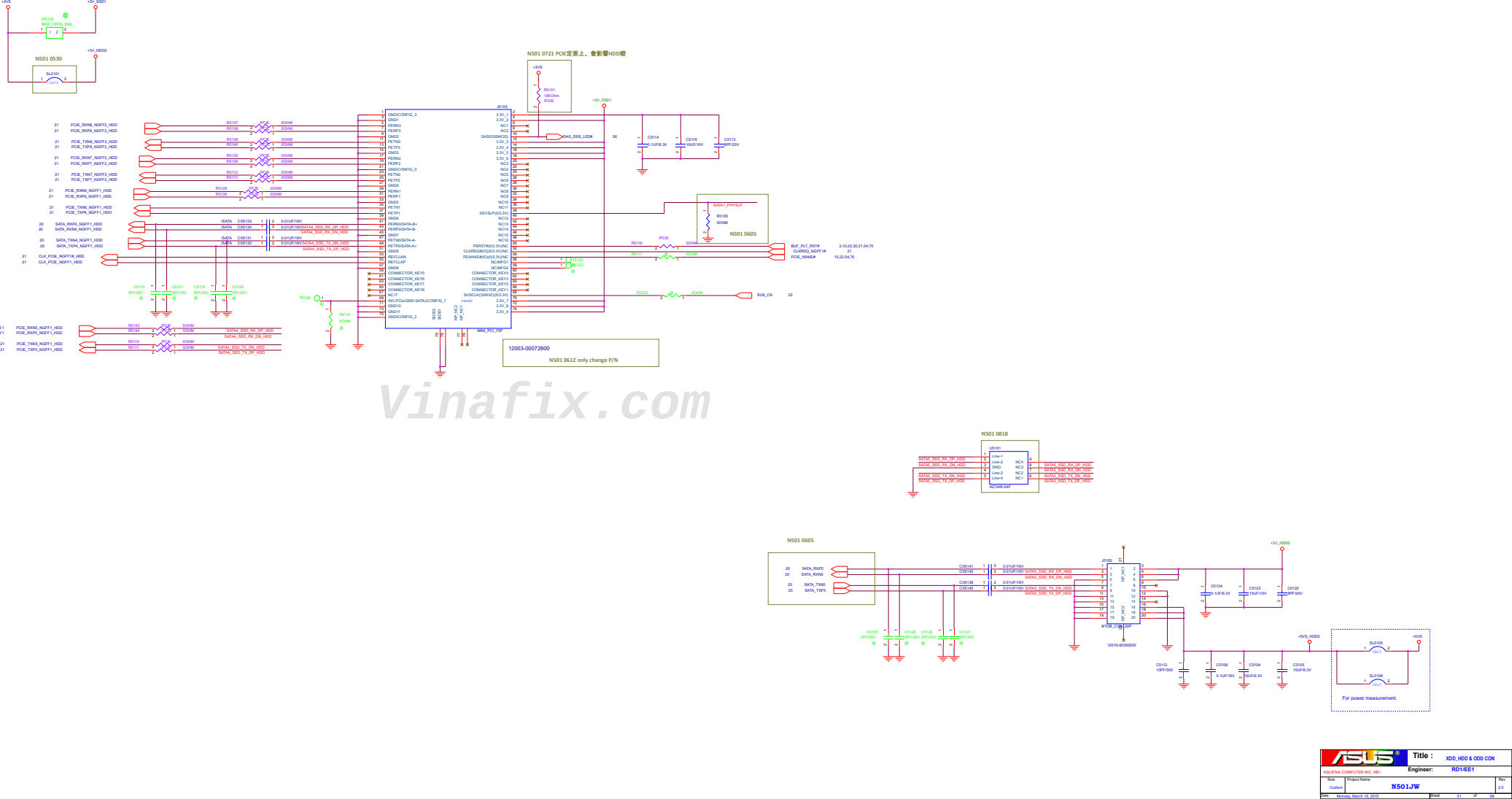
Title : TV_****

ASUSTeK COMPUTER INC. NB3

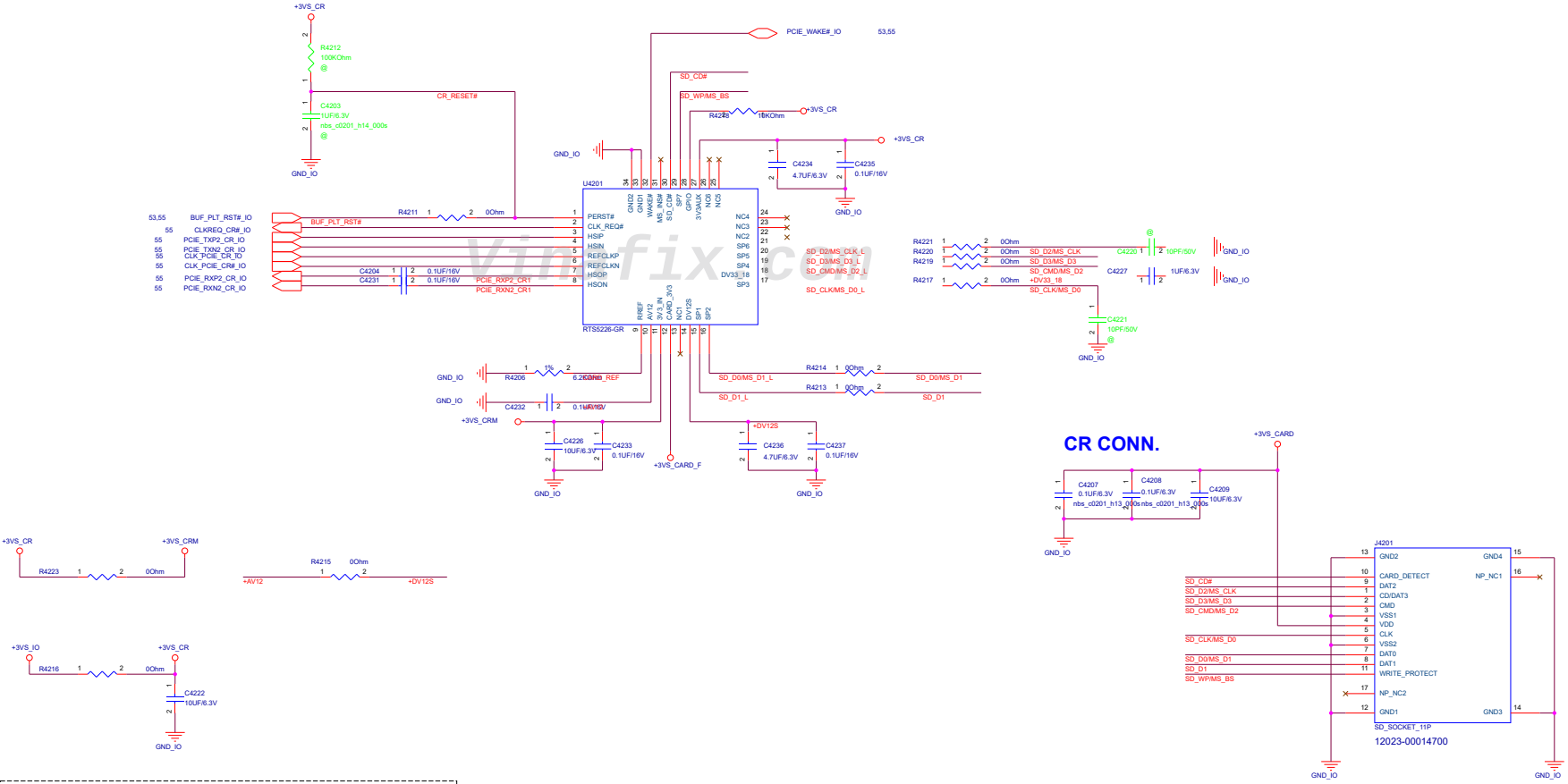
Engineer: RD1/EE1

Size	Project Name	Rev
B	N501JW	2.0

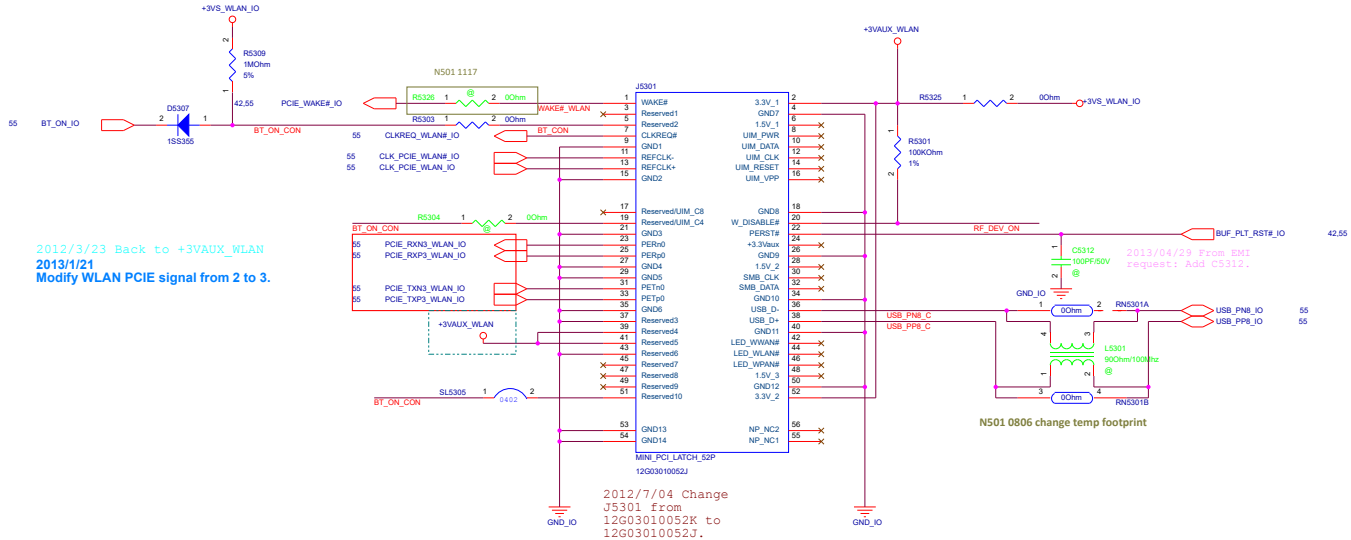
Date:	Monday, March 16, 2015	Sheet	49	of	98

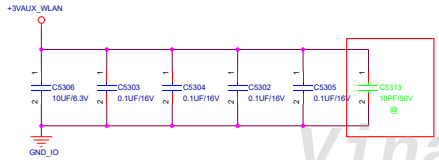


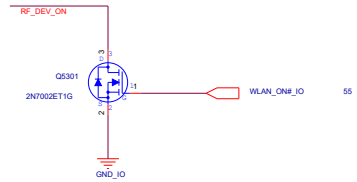
Title :	XDD_HDD & ODD CON
Engineer:	RD1/EE1
ASUSTeK COMPUTER INC. NB1	
Size: Custom	Project Name: N501JW
Rev: 2.0	
Date: Monday, March 16, 2015	Sheet 51 of 98

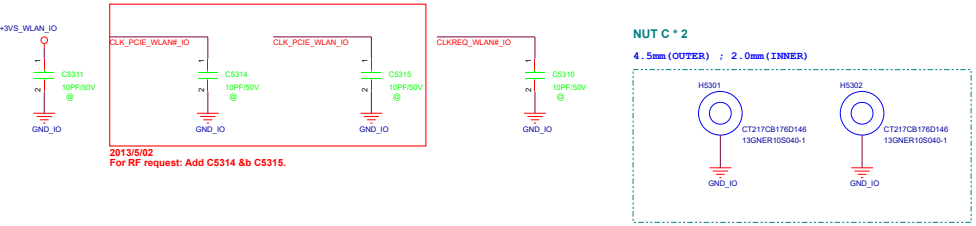


ASUSTeK COMPUTER INC. NB1	Title : Card Reader-RTS5226	
	Engineer: RD1/EE1	
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 42 of 98	





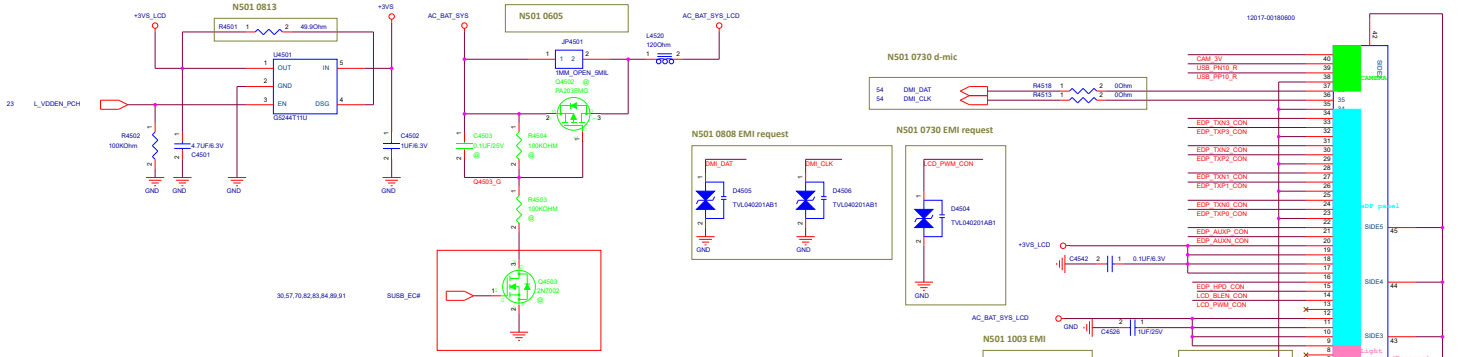




ASUSTeK COMPUTER INC. NB1	Title : MINICARD(WLAN)		
	Engineer: RD1/EE1		
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 53 of 98		

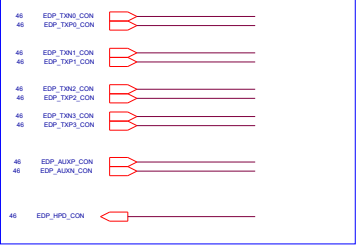
LCD Power switch

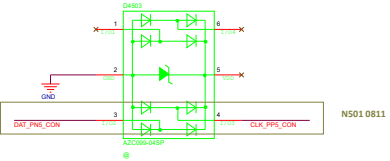
1st: 12017-00180600
2nd: 12017-00181400



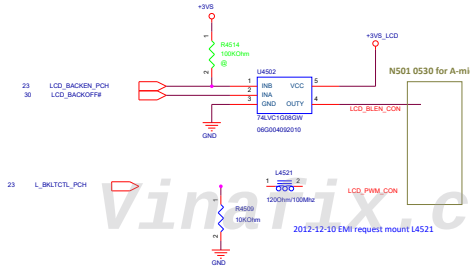
eDP from CPU

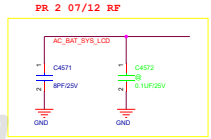
0919 Farad Modify 0.1u to 0201
1212 Farad Modify 0.1u to 0402

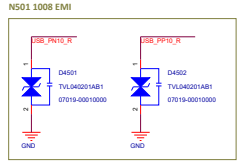




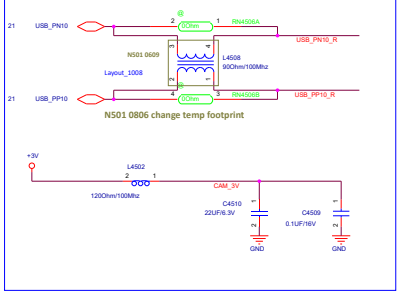
2012-12-13 EMI request mount D4503



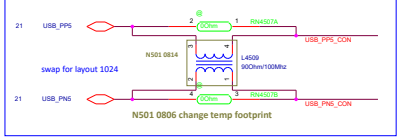


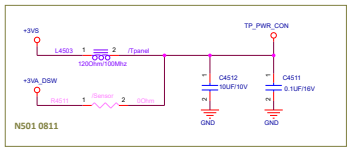


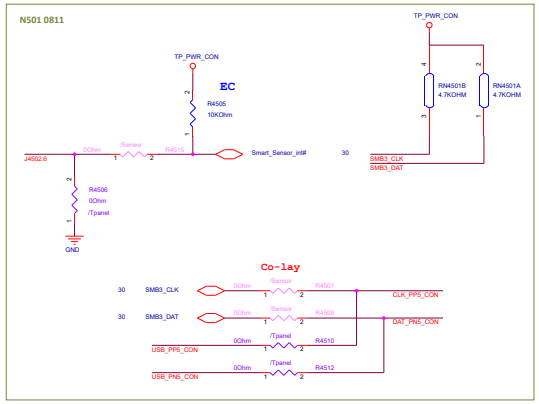
Camera module



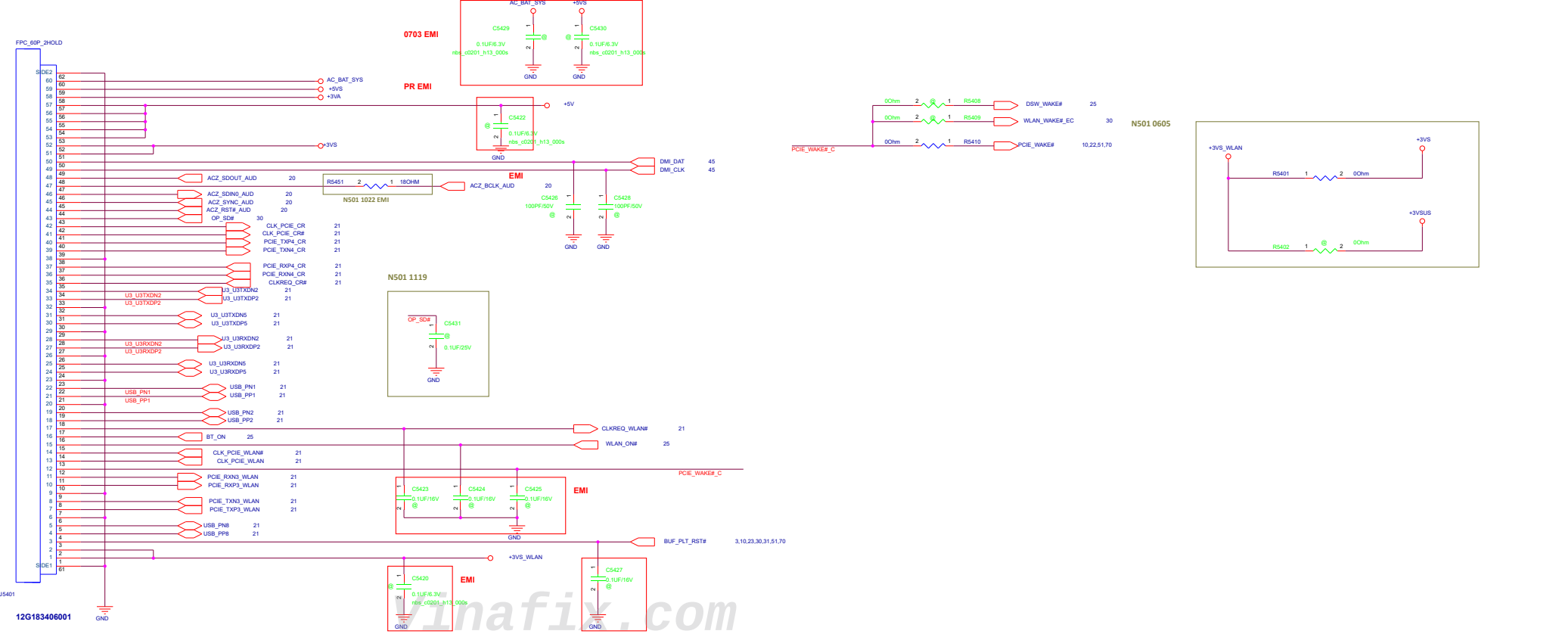
Touch Panel for S500 touch solution



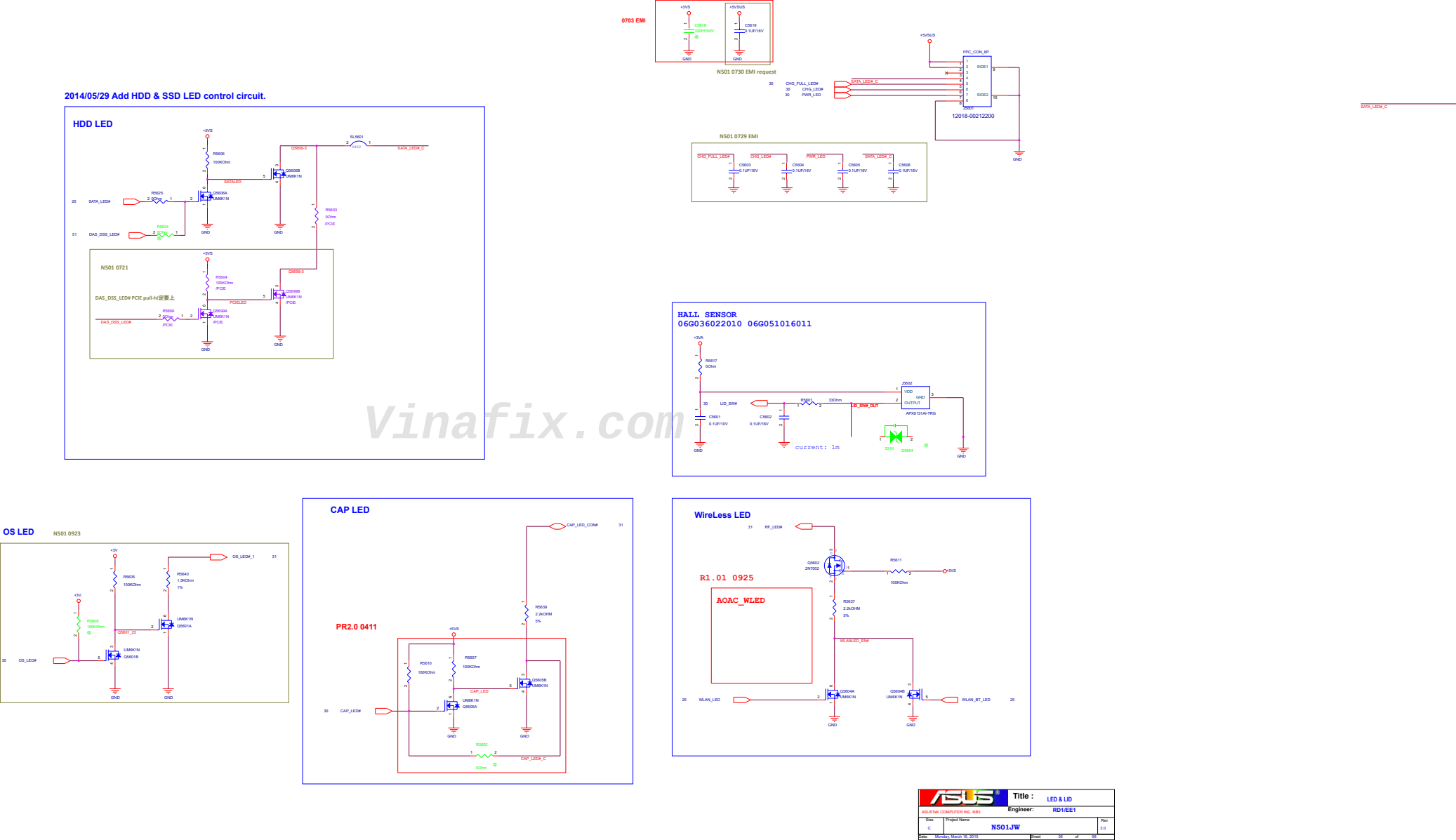


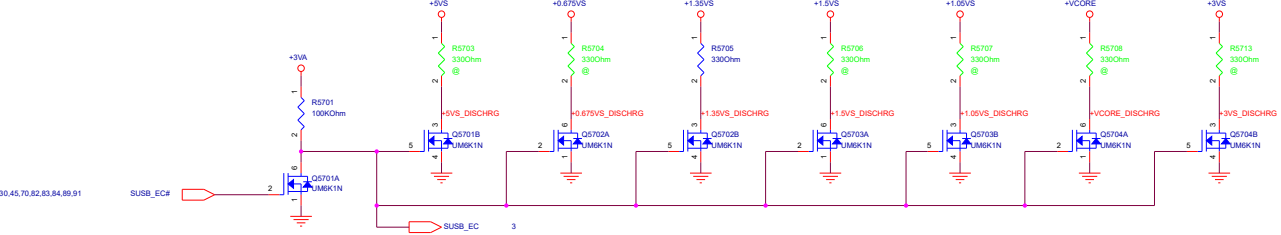


ASUSTeK COMPUTER INC. NB1	Title :	CRT_eDP	
	Engineer:	RD1/EE1	
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 45 of 98		

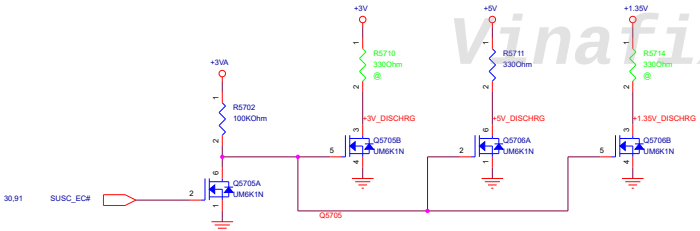


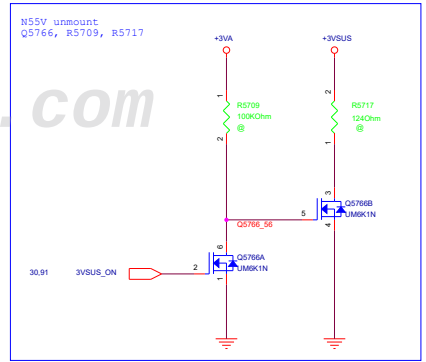
ASUSTeK COMPUTER INC	Title :	USB3_*****
	Engineer:	RD1/EE1
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 54 of 98	

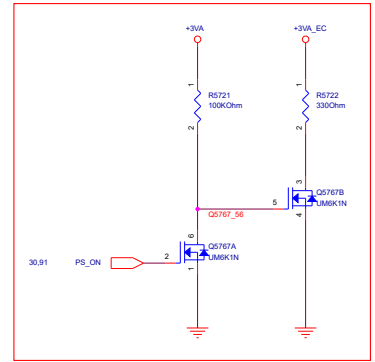

0703 EMI
+3VS
+5VSUS
C5618
680PF/50V
C5619
0.1UF/16V
GND
N501 0730 EMI request
30 CHG_FULL_LED#
30 CHG_LED#
30 PWR_LED
SATA_LED#_C
FPC_CON_8P
SIDE1
SIDE2
12018-00212200
N501 0729 EMI
CHG_FULL_LED#
CHG_LED#
PWR_LED
SATA_LED#_C
C5603 0.1UF/16V
C5604 0.1UF/16V
C5605 0.1UF/16V
C5606 0.1UF/16V
2014/05/29 Add HDD & SSD LED control circuit.
HDD LED
+5VS
R5608 100KOhm
Q5608B UMBK1N
Q5608A UMBK1N
SATALED
SATA_LED#
R5625 100R
R5624 100R
DAS_DSS_LED#
SL5601
SATA_LED#_C
Q5608-3
R5603 0Ohm /PCIE
N501 0721
DAS_DSS_LED# PCIE pull-hi定置上
R5604 100KOhm /PCIE
Q5699B UMBK1N /PCIE
Q5699A UMBK1N /PCIE
PCIELED
R5699 100R /PCIE
Q5699-3
HALL SENSOR
06G036022010 06G051016011
+3VA
R5617 0Ohm
LID_SW#
R5601 33Ohm
LED_SW#_OUT
C5601 0.1UF/16V
C5602 0.1UF/16V
J5602
VDD
GND
OUTPUT
APX9131AI-TRG
current: 1m
331K
C5604
OS LED
N501 0923
+3V
R5605 100KOhm
R5640 1.5KOhm 1%
R5606 100KOhm
Q5601_23
Q5601A UMBK1N
Q5601B UMBK1N
OS_LED#_1
OS_LED#
CAP LED
PR2.0 0411
CAP_LED_CON#
R5639 2.2KOHM 5%
R5610 100KOhm
R5607 100KOhm
Q5605B UMBK1N
Q5605A UMBK1N
CAP_LED
CAP_LED#
R5602 0Ohm
CAP_LED#_C
WireLess LED
R1.01 0925
AOAC_WLED
RF_LED#
Q5602 2N7002
R5611 100KOhm
R5637 2.2KOHM 5%
WLANLED_EN#
WLAN_LED
Q5604A UMBK1N
Q5604B UMBK1N
WLAN_BT_LED
SATA_LED#_C
Title : LED & LID
ASUSTeK COMPUTER INC. NB3
Engineer: RD1/EE1
Size: C
Project Name: N501JW
Rev: 2.0
Date: Monday, March 16, 2015
Sheet 58 of 98



follow n46
For +3VA_EC discharge circuit

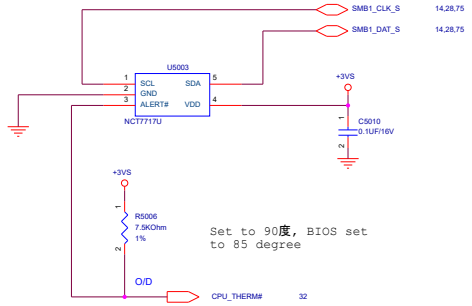






ASUSTeK COMPUTER INC. NB1	Title : DSG_Discharge	
	Engineer: RD1/EE1	
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 57 of 98	

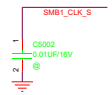
CPU Thermal Sensor



SMBUS address=10010000 (90)

Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

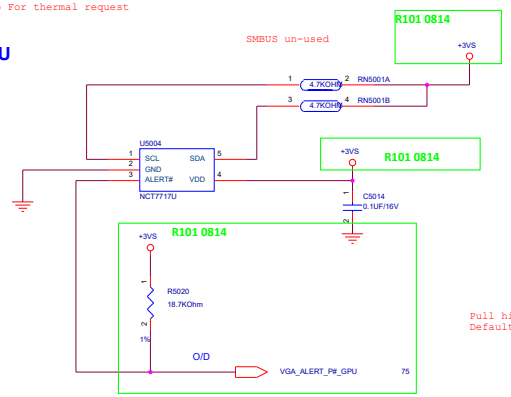
Reserve for
powr noise



2012/12/25 For thermal request

For GPU

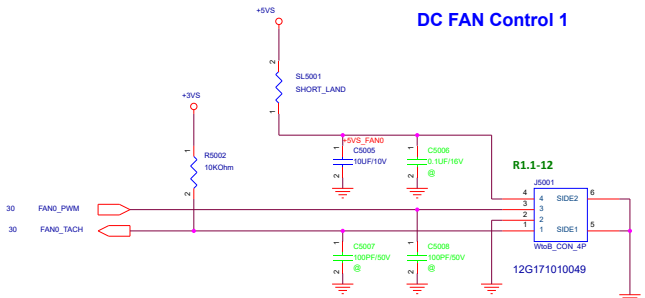
SMBUS un-used



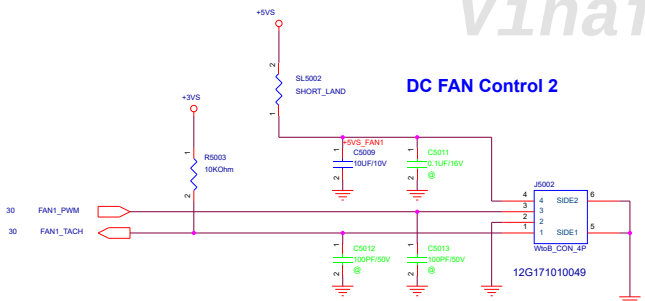
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Pull high in R7527
Default 18.7kohm => 110 deg.(need to tune)

DC FAN Control 1

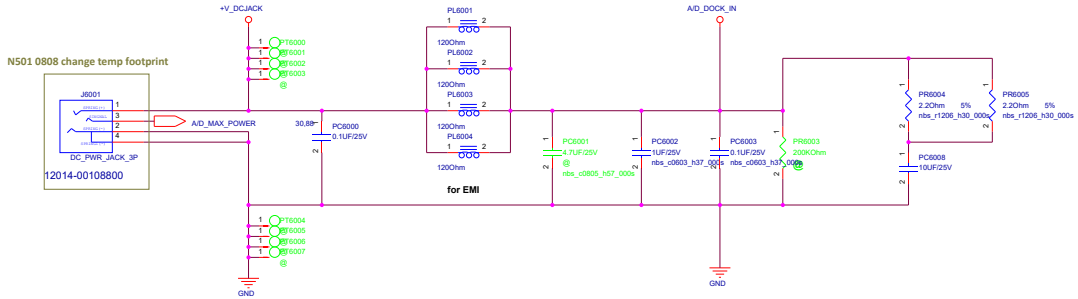


DC FAN Control 2

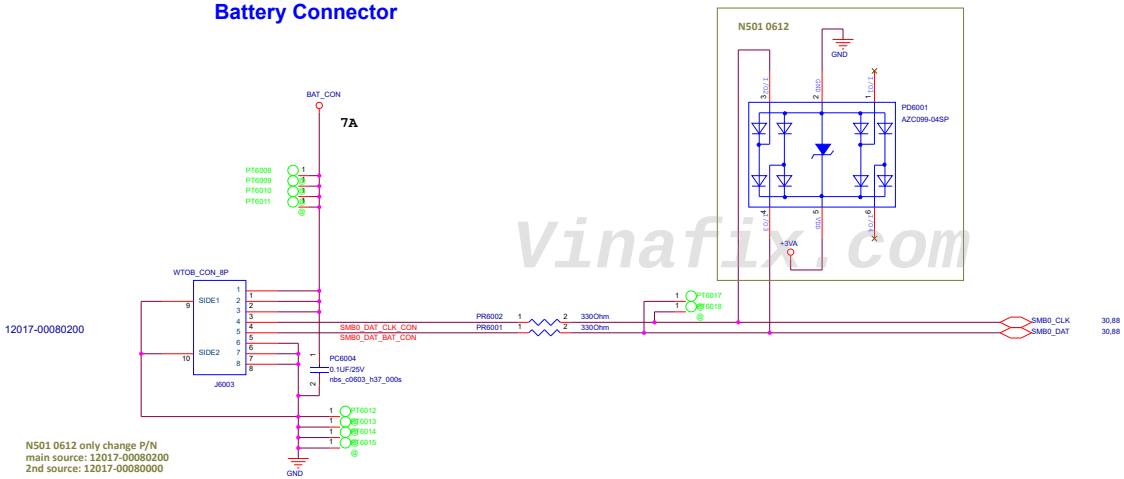


ASUSTeK COMPUTER INC. NB1	Title : FAN_Thermal Sensor & Fan		
	Engineer: RD1/EE1		
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 50 of 98		

DC-IN Connector



Battery Connector



ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer:		
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 60 of 98		

Title : BT_Bluetooth

ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

Size	Project Name	Rev
A	N501JW	2.0

USB3.0 EMI-Protection

12/10/25
L5201, L5202,L5203, L5204
09G092090400

N501 0806 change temp footprint

LS201 90Ohm @
LS202 90Ohm @

21 U3_U3RXDP1
21 U3_U3RXDN1
21 U3_U3TXDP1
21 U3_U3TXDN1

CS201 2 1 0.1UF/16V
CS202 2 1 0.1UF/16V

0Ohm RNS201B
0Ohm RNS201A
0Ohm RNS202B
0Ohm RNS202A

U3_U3RXDP1_R
U3_U3RXDN1_R
U3_U3TXDP1_R
U3_U3TXDN1_R

N501 0806 change temp footprint

From PCH

USB2.0 EMI-Protection

0Ohm RNS205A @
90Ohm/100Mhz LS205
0Ohm RNS205B @

USB_PN0_C
USB_PP0_C
USB_U0-
USB_U0+

2012-12-10 EMI request mount
N501 0806 change temp footprint

DS202 AZC099-04SP @
+5VSUS

USB3.0_Port 0

RF

+5VSUS
CS206 0.1UF/16V
US201 GL887
NEW
R5203 0Ohm @
OC# USB_OC#0 21
LIM_SEL1 LIM_SEL0
P5V DM_UP DP_UP ILIM_SEL[2]
GND3 GND2 GND1 LIM_SEL[1] LIM_SEL[0] ALARM
VBUS_OUT DM_DOWN DP_DOWN BC_CON
P3W_EN CHG_MOD[2] CHG_MOD[1] CHG_MOD[0]
21 USB_PN0
21 USB_PP0
ILIM_SEL2
USB_PN0_C
USB_PP0_C
06016-00810000
30,81 5VSUS_ON
30 USB30_5VSUS
R5204 0Ohm
CHG_MOD2
CHG_MOD1
CHG_MOD0

06016-00300000 TPS2543RTER
06016-00510000 TPS2546RTER
06016-00810000 TPS2544RTER <-

N501 0812
LS207 80Ohm/100Mhz
+5V_USB1
CS208 100UF/6.3V
CS205 0.1UF/16V
CS203 8PF/25V
GND

USB3.0_Port 0
N501 0808 change temp footprint
N501 0612
+5V_USB1
USB_U0-
USB_U0+
U3_U3RXDN1_R
U3_U3RXDP1_R
U3_U3TXDN1_R
U3_U3TXDP1_R
JS201
VBUS D- D+ GND STDA_SSRX- STDA_SSRX+ GND_DRAIN STDA_SSTX- STDA_SSTX+ P_GND1 P_GND3 P_GND4 P_GND2
USB_CON_9P
12013-00040700

USB Charge Circuit (For PORT 0)

N501 0604

30 USB_CHARGE_ON#
30 USB_BC1.2_OFF#
SI402
SL5201
CHG_MOD2
CHG_MOD0
CHG_MOD1
+5VSUS
RS206 10KOhm
RS215 10KOhm
RS212 10KOhm
RS214 20KOhm
ILIM_SEL2
ILIM_SEL1
ILIM_SEL0

Reserve for 2013 platform BC1.2 charger disable

USB3.0/USB 2.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

US203 AZ1045-04F @
U3_U3TXDP1_R
U3_U3TXDN1_R
U3_U3RXDP1_R
U3_U3RXDN1_R
GND

RF request

J5203 POGO_1P @
POGO PIN 1P 1.8MM SMT
12G3900001 0H

ASUSTeK COMPUTER INC. NB1	Title :	USB Charger
	Engineer:	RD1/EE1
Size: D	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 52 of 98	

Title : I/O board(1-1)_CR_RTS5139

ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

Size	Project Name	Rev
C	N501JW	2.0

Date:	Monday, March 16, 2015	Sheet	62	of	98

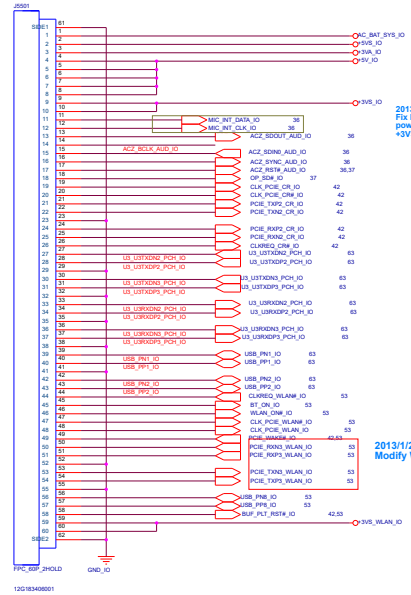
Title : I/O board LED

ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

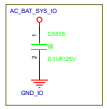
Size	Project Name	Rev
A	N501JW	2.0

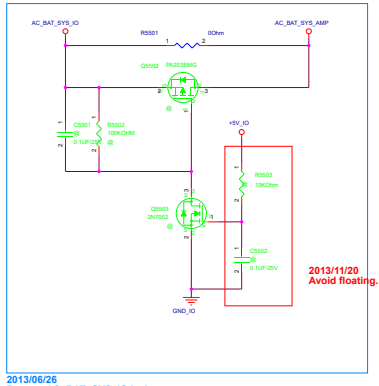
Date:	Monday, March 16, 2015	Sheet	64	of	98



2013/6/18
Fix known issue, change power plan from +3VSUS_IO to +3VA_IO.

N501 1119

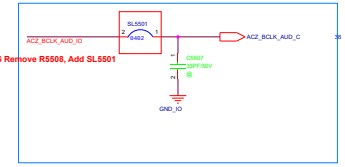




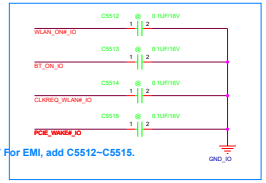
2013/11/20
Avoid floating.

2013/06/26
Prevent AC_BAT_SYS_IO leakage current.

2013/1/21
Modify WLAN PCIE signal from 2 to 3.



2012/07/16 Remove R5508, Add SL5501



2012/07/17 For EMI, add C5512~C5515.
靠近J5501

ASUSTeK COMPUTER INC. NB1	Title :	IO Con. to MB	
	Engineer:	RD1/EE1	
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 55 of 66		

ASUSTeK COMPUTER INC. NB3	Title :	I/O board PWR key	
	Engineer:	RD1/EE1	
Size: B	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 66 of 98		

A

H6702 8
1 2
2D_D94
GND GND

N501 1009 EMS 2D BAR CODE AREA

U6701
EMS_2D_BARCODE
U6703
EMS_2D_BARCODE

N501 0814 spring for EMI

U6702
SMD132X93_S16
GND

E NUT

H6724 CT217CB63D47 13GN7K10M340-1 GND
H6725 CT217CB63D47 13GN7K10M340-1 GND
H6726 CT217CB63D47 13GN7K10M340-1 GND
H6727 CT217CB63D47 13GN7K10M340-1 GND

N501 0807

12 H6701 C315D94 GND
12 H6703 C315D94 GND

N501 0813

H6745 CT197CB128D98 13020-01540000 GND
H6746 CT197CB128D98 13020-01540000 GND

RF request

11

J6701 POGO_1P POGO PIN 1P 1.8MM SMT 12G39000010H
J6702 POGO_1P POGO PIN 1P 1.8MM SMT 12G39000010H
J6703 SMD197X197_NP G46VW LED PAD temp_TX15671_0004
J6704 POGO_1P POGO PIN 1P 1.8MM SMT 12G39000010H
J6705 POGO_1P POGO PIN 1P 1.8MM SMT 12G39000010H

N501 0806

B CPU

RCT240X240CBID146 H6709 2 GND
RCT240X240CBID146 H6710 1 GND
RCT240X240CBID146 H6711 4 GND
RCT240X240CBID146 H6712 3 GND

N501 0806

H6704 6
2D_D94
GND GND

N501 0612

HDD B to B NUT

H6739 13GNMU10M010-1 CT256BID146 GND
H6740 13GNMU10M010-1 CT256BID146 GND

N501 0806

G
H
5
H6720 3D_D110_D83_D165
GND

C GPU NUT

H6713 CT217CB176D146 13GNER10S040-1 nb_nut_ct217bid146_h59_lf2 GND
H6714 CT217CB176D146 13GNER10S040-1 nb_nut_ct217bid146_h59_lf2 GND
H6744 CT217CB176D146 13GNER10S040-1 nb_nut_ct217bid146_h59_lf2 GND

I

9 H6721 CT315CRBI114D94 s07912 GND
9 H6722 CT315CRBI114D94 s07912 GND
10 H6723 2D_D94_DO107X94 GND GND

N501 0612

H6741 CT217CB176D146 13GNER10S040-1 nb_nut_ct217bid146_h59_lf2 GND
H6742 CT217CB176D146 13GNER10S040-1 nb_nut_ct217bid146_h59_lf2 GND

TOP NUT

H6743 CT217CB176D146 13GNER10S040-1 nb_nut_ct217bid146_h59_lf2 GND

N501 0930

H6747 CT217CB176D146 13GNER10S040-1 GND
H6748 CT217CB176D146 13GNER10S040-1 GND
H6749 CT217CB176D146 13GNER10S040-1 GND
H6750 CT217CB176D146 13GNER10S040-1 GND

D FAN NUT

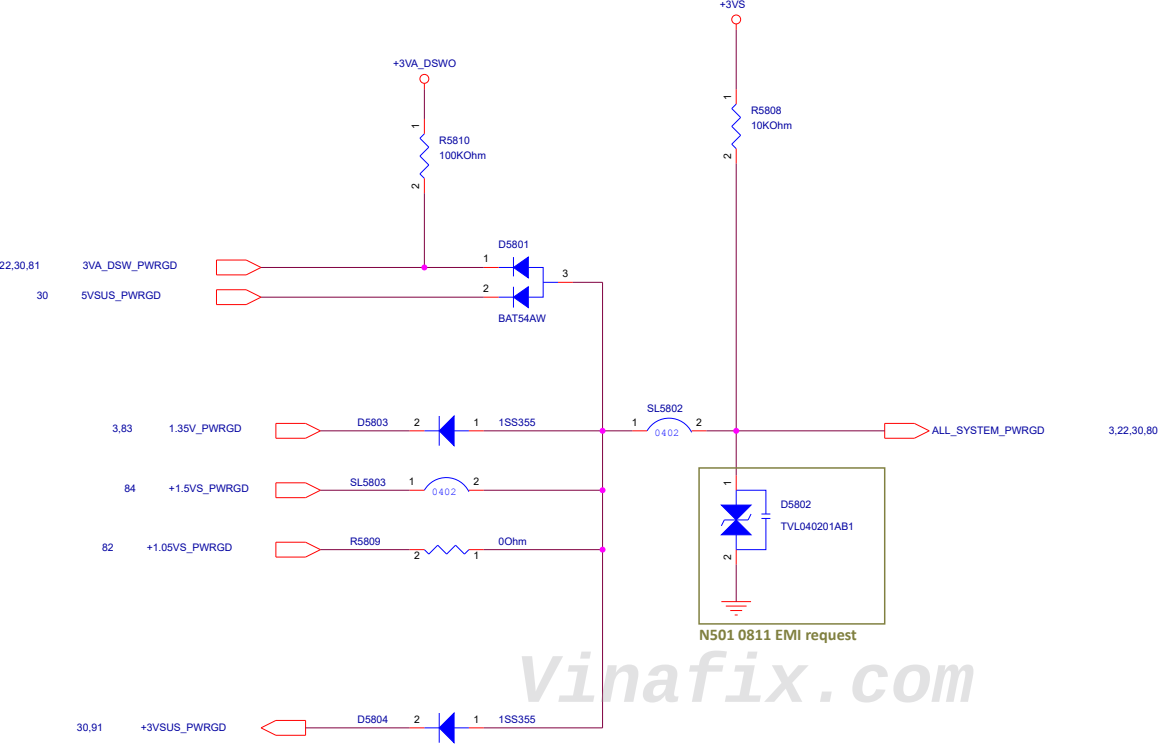
H6715 CT217CB176D146 GND
H6716 CT217CB176D146 GND
H6717 CT217CB176D146 GND
13GNER10S040-1 nb_nut_ct217bid146_h59_lf2
13GNER10S040-1 nb_nut_ct217bid146_h59_lf2
13GNER10S040-1 nb_nut_ct217bid146_h59_lf2

N501 0929

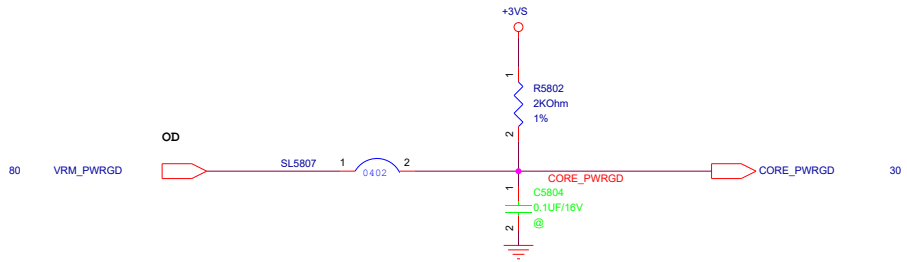
F SSD NUT

H6718 CT217CB315ID146 13020-00780900 GND

ASUSTeK COMPUTER INC. NB3	Title : I/O board FUNC key	
	Engineer: RD1/EE1	
Size: B	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 67 of 98	

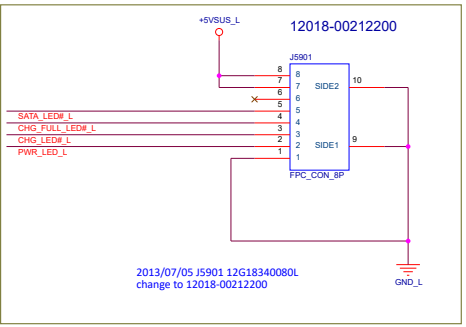


N501 0606



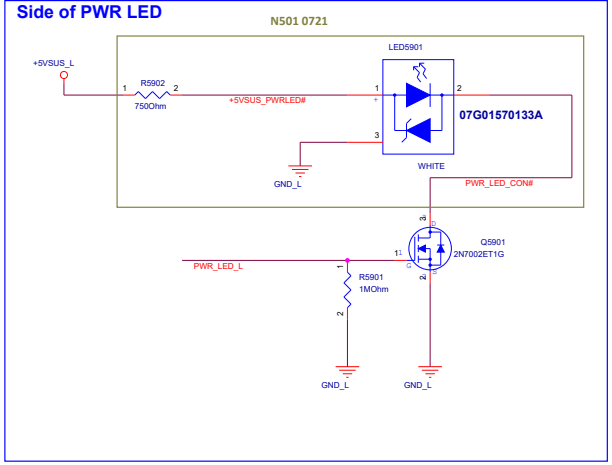
ASUSTeK COMPUTER INC. NB1	Title : Power Protect		
	Engineer: RD1/EE1		
Size: B	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 58 of 98		

N501 0603

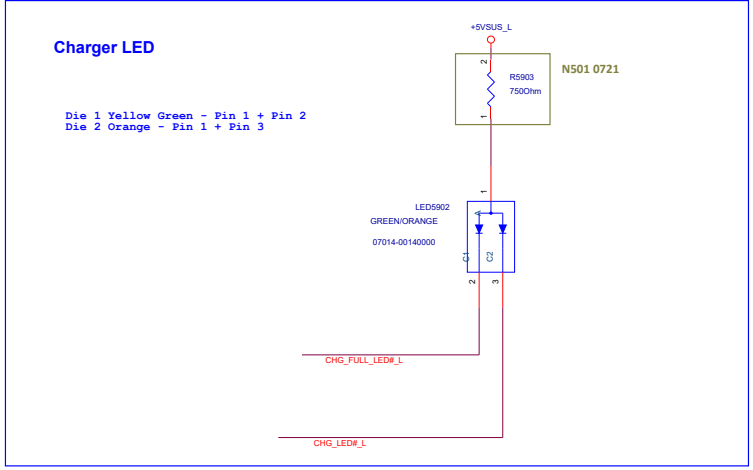


Side of PWR LED

N501 0721

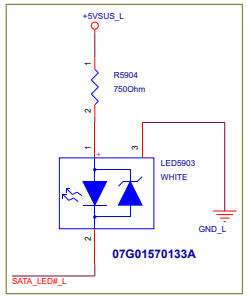


Charger LED



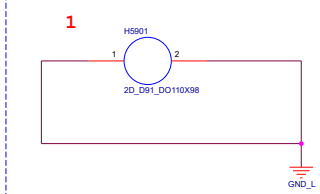
HDD LED

N501 0721



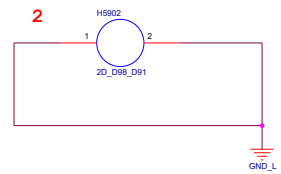
Screw Hole A

1.6 mm tooling hold
2.3mm(inner);5mm(outer)



Screw Hole B

1.6mm tooling hold
2.3mm(inner);5mm(outer)



ASUSTeK COMPUTER INC. NB3	Title : I/O_Main board Conn.	
	Engineer: RD1/EE1	
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 59 of 98	

Title : OTH_for test only

ASUSTeK COMPUTER INC. NB3

Engineer: RD1/EE1

Size	Project Name	Rev
A	N501JW	2.0

Date: Monday, March 16, 2015

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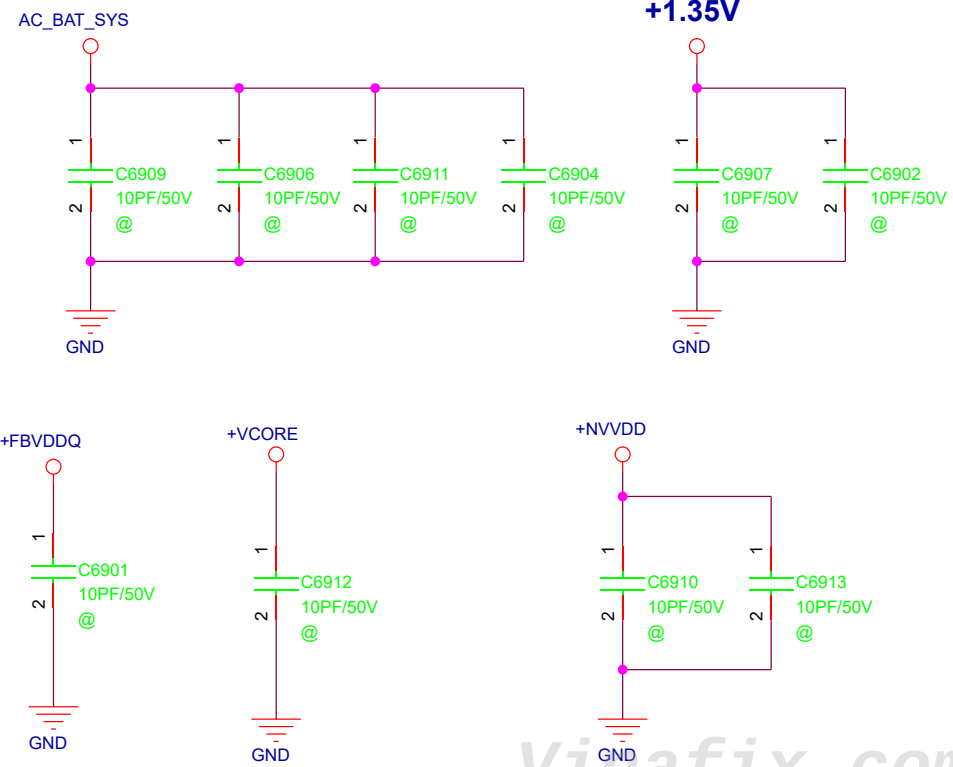
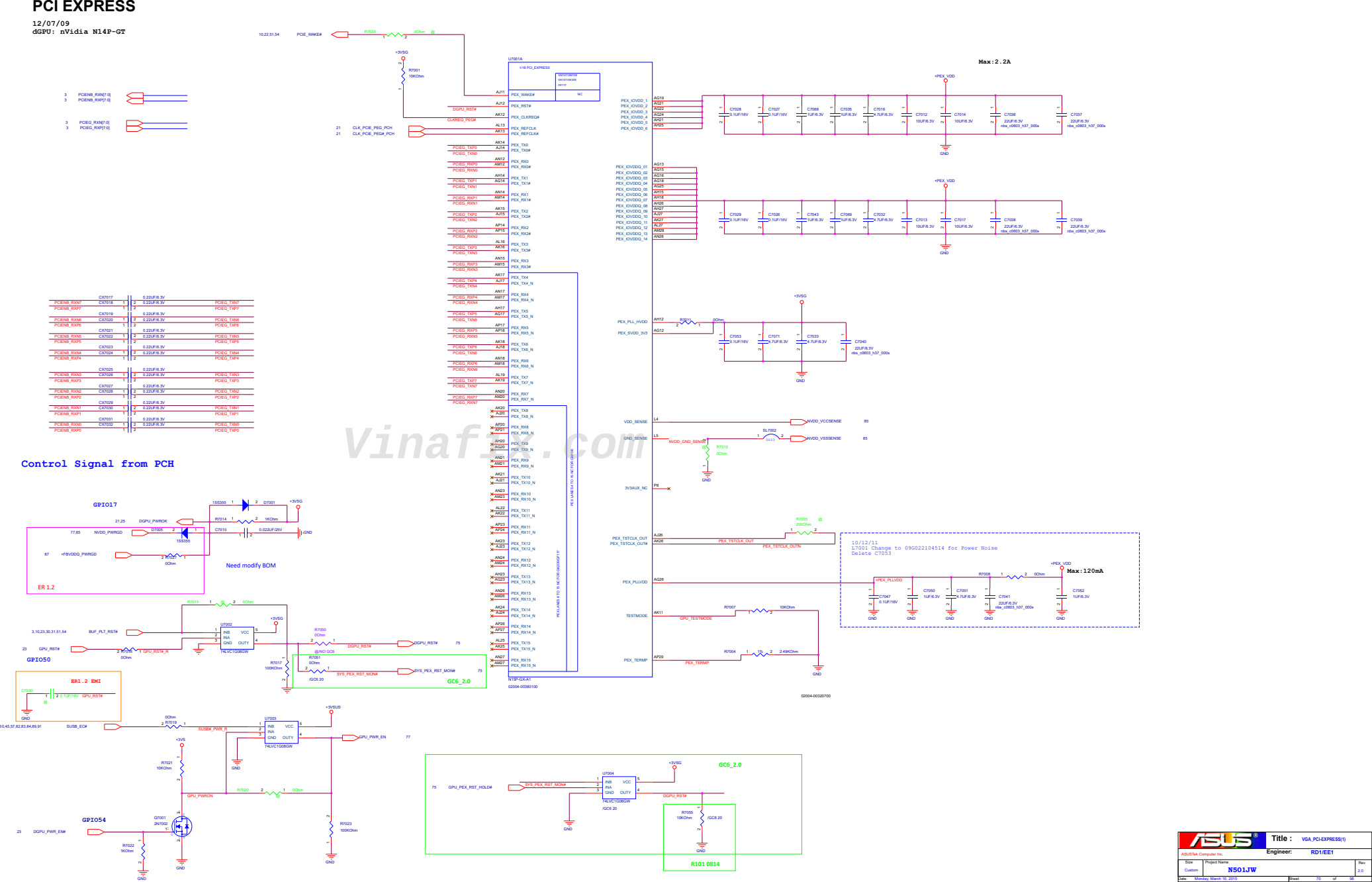


ASUSTeK COMPUTER INC. NB3	Title : OTH_EMI Caps		
	Engineer: RD1/EE1		
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 69 of 98		

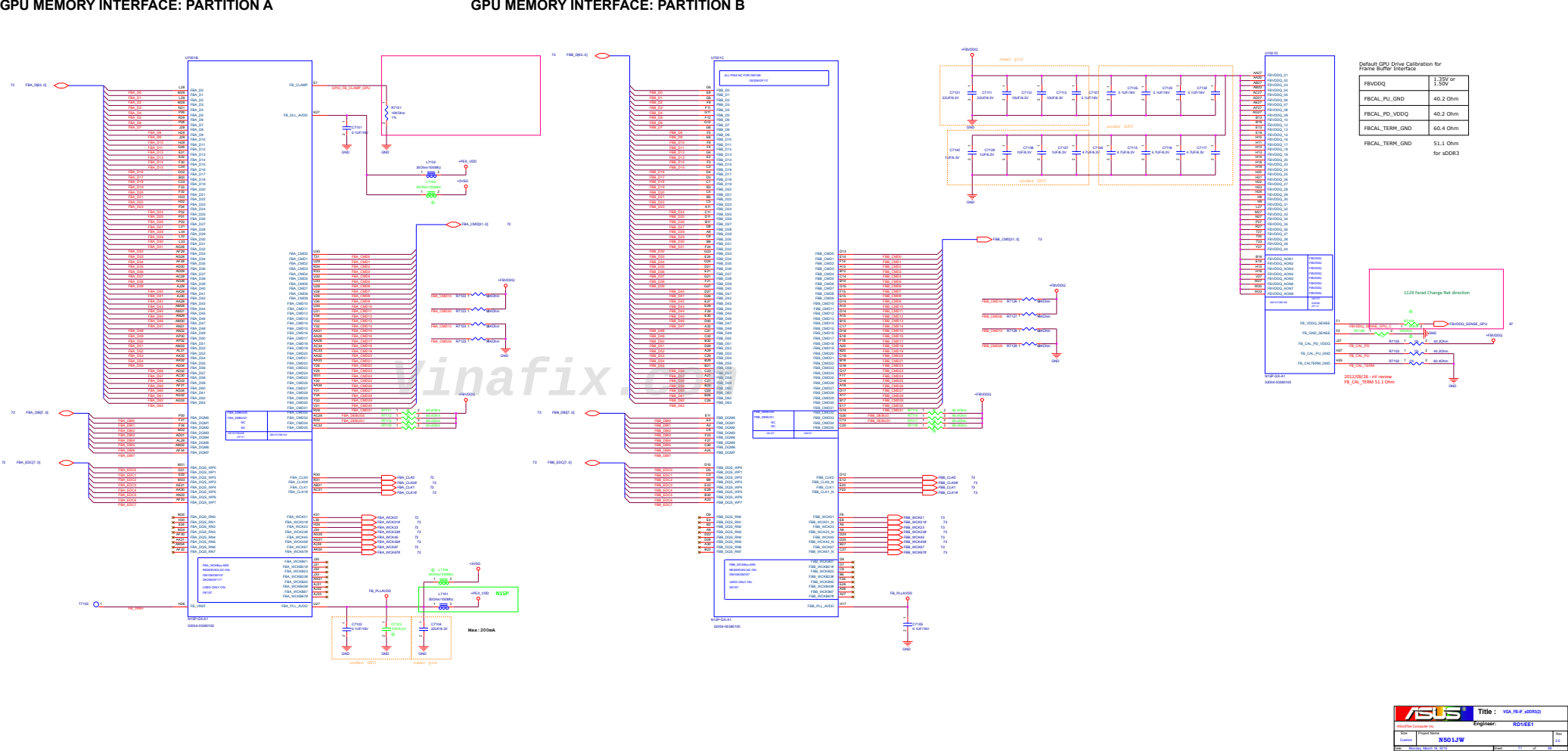
PCI EXPRESS

12/07/09

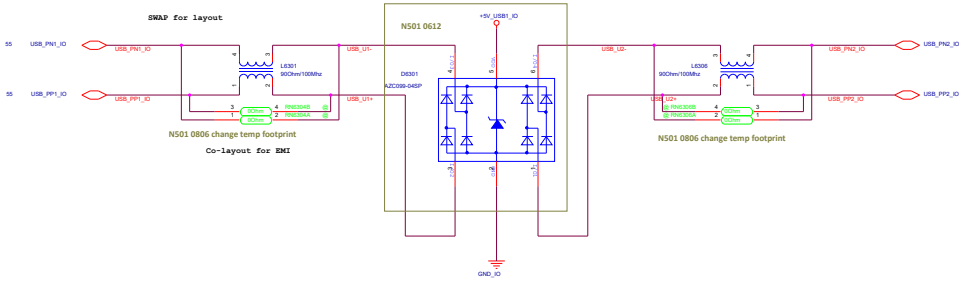
dGPU: nVidia N14P-GT



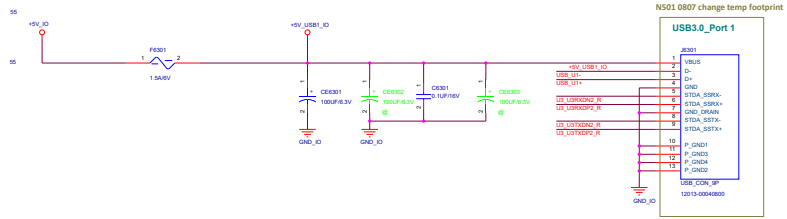
Title :	VGA_PCI-EXPRESS(1)
Engineer:	RD1/EE1
Size	Custom
Project Name	N501JW
Rev	2.0
Date:	Monday, March 16, 2015
Sheet	70 of 98


GPU MEMORY INTERFACE: PARTITION A
GPU MEMORY INTERFACE: PARTITION B
Default GPU Drive Calibration for Frame Buffer Interface
FBVDDQ 1.35V or 1.50V
FBCAL_PU_GND 40.2 Ohm
FBCAL_PD_VDDQ 40.2 Ohm
FBCAL_TERM_GND 60.4 Ohm
FBCAL_TERM_GND 51.1 Ohm for sDDR3
1129 Farad Change Net direction
2012/09/26 : HV review
FB_CAL_TERM 51.1 Ohm
Max: 200mA
Title : VGA_FB-F_sDDR3(2)
Engineer: RD1/EE1
N501JW
Vinafix.com

USB 2.0 EMI / ESD-Protection

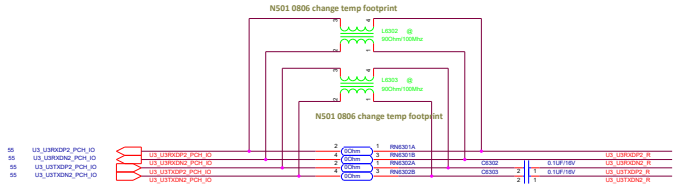


USB 3.0 port1

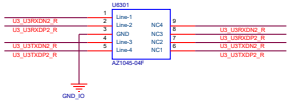


2013/6/25 Change U3 connector from 12013-00012400 to 12013-00046200.

USB3.0 EMI-Protection



USB3.0 ESD-Protection

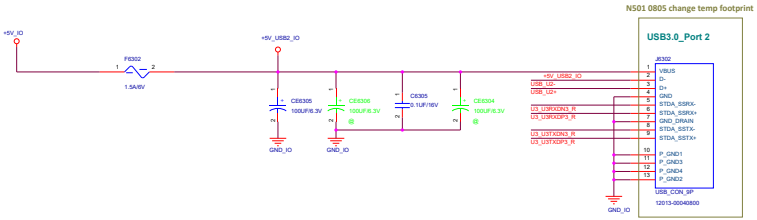


Follow N71Ja Design
1st : 07G028076030
ESD PROTECTION AZ1045-04F

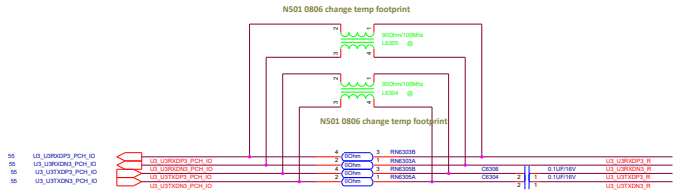
2nd : 07G028171010
ESD PROTECTION IP4292CZ10-TB

走線請直接由 U5501 穿過至零件另一側之對應 pin 勿成分枝狀走線

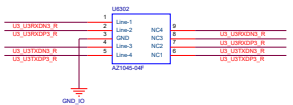
USB 3.0 port2



USB3.0 EMI-Protection



USB3.0 ESD-Protection



Follow N71Ja Design
1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028171010
ESD PROTECTION IP4292CZ10-TB

走線請直接由 U5502 穿過至零件另一側之對應 pin 勿成分枝狀走線

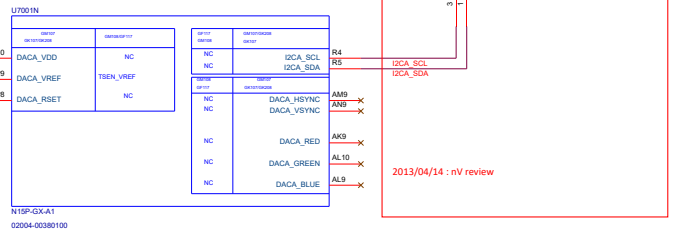
ASUSTeK COMPUTER INC. NB1	Title :	USB3.0(2ports)
	Engineer:	RD1/EE1
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 63 of 68	

DG-06246-001_v04 DG9.6 p170
DAC interface not used
Leave DACA_VDD floating
All Other pin (DACA_VREF,DACA_RSET) NC

DG-06246-001_v02 DG10.2.1 p168
Unused I2C should be soft grounded or
PU 3.3V via 2.2kOhm

CRT DAC_A

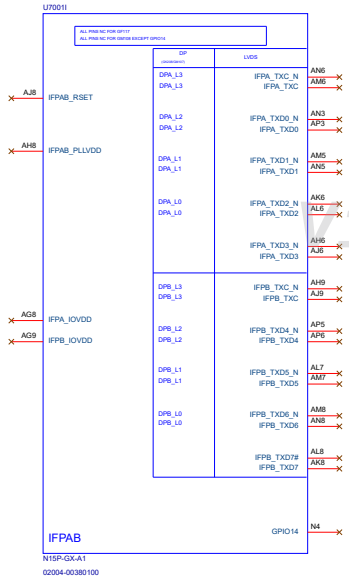
2013/04/14 : nV review
no stuff resistor



DG-06246-001_v04 DG8.6 p162
Float IFPxy_IOCDD/IFPxy_PLLVDD
Other pin NC

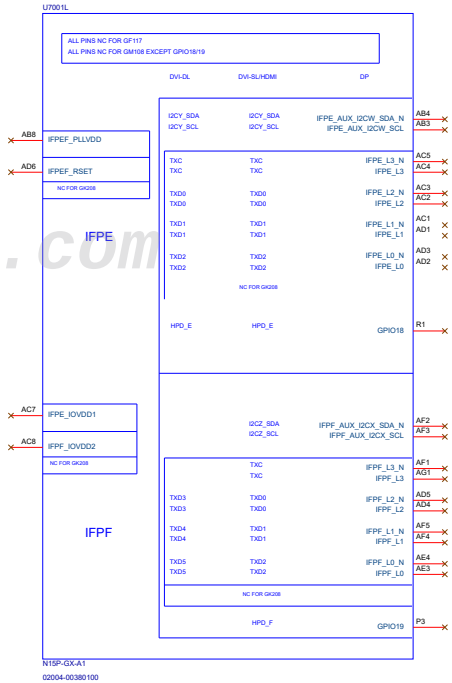
LVDS IFPA/B

2013/04/14 : nV review
no stuff resistor

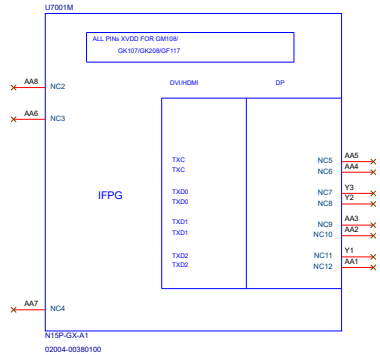


2013/04/14 : nV review
no stuff resistor

LVDS IFPE/F



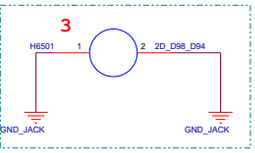
LVDS IFPG



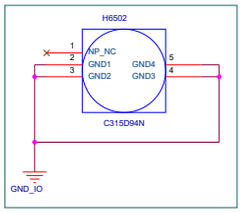
ASUSTek Computer Inc.	Title :	VGA_CRT/LVDS(5)
	Engineer:	RD1/EE1
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 74 of 98	

Screw Hole A * 2

6.0mm(OUTER) ; 2.4mm(INNER)



N501 0812

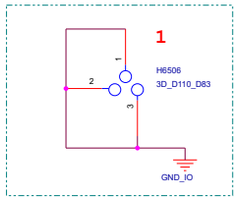


NUT C * 2

4.5mm(OUTER) ; 2.0mm(INNER)

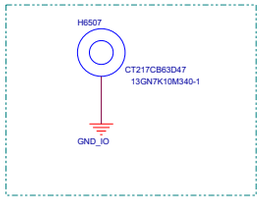
Screw Hole D & E * 1

4.3m(outer) ; 2.5mm(INNER)

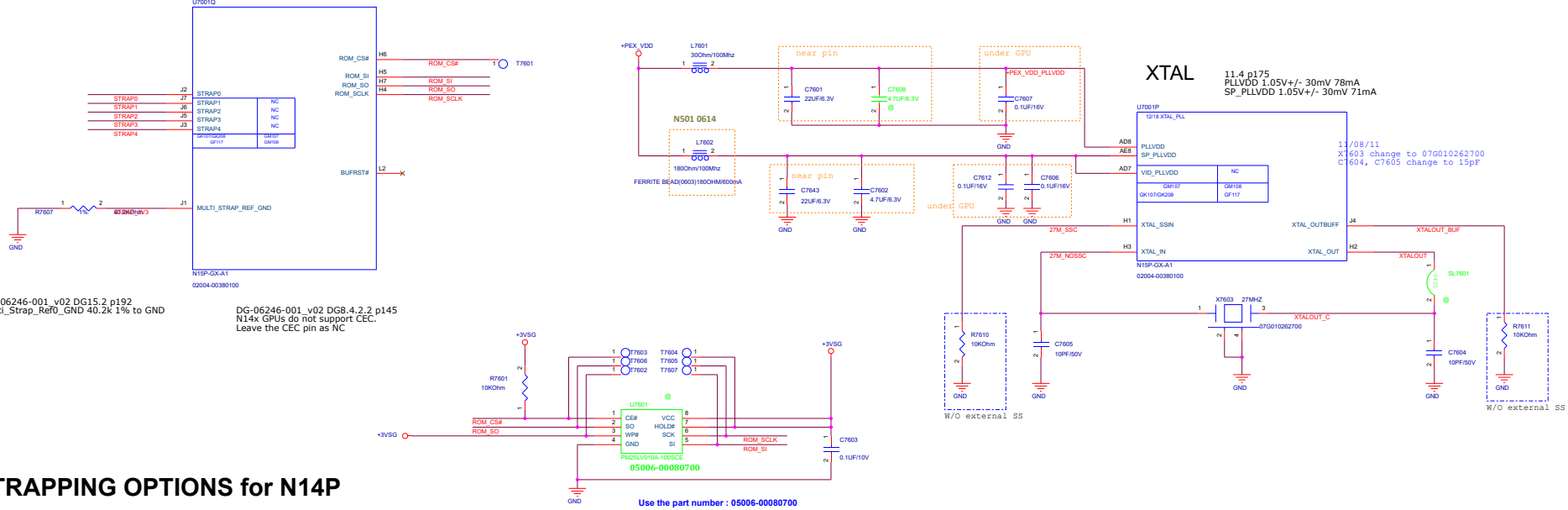


Screw Hole F * 1

5.0mm(OUTER) ; 2.0mm(INNER)



ASUSTeK COMPUTER INC. NB1	Title : ME_Screw Hole & Nut	
	Engineer: RD1/EE1	
Size: C	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 65 of 98	

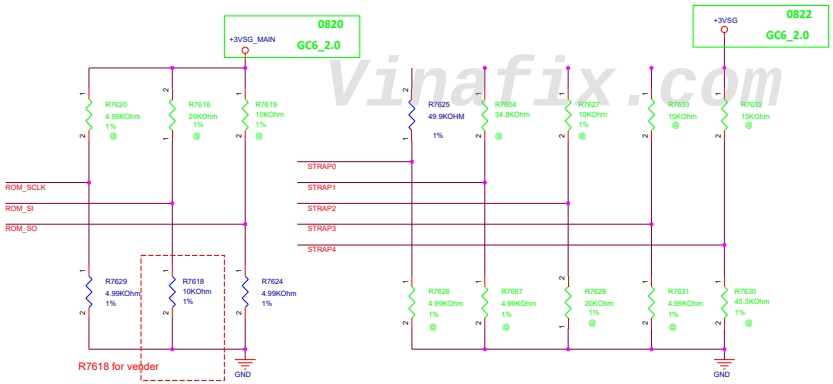


DG-06246-001_v02 DG15.2 p192
Multi_Strap_Ref0_GND 40.2k 1% to GND

DG-06246-001_v02 DG8.4.2.2 p145
N14x GPUs do not support CEC.
Leave the CEC pin as NC

STRAPPING OPTIONS for N14P

2012/09/28 nV review



DG-06246-001_v03 DG15.6 p201
STRAP DESCRIPTIONS

PCI_DEVID = 0x0FE4

ROM_SCLK	PCI_DEVID[4]=	SUB_VENDER = 0	PCI_DEVID[5]=	PEX_PLL_EN_TERN = 0	0010 => PD 15K
ROM_SI	RAM_CFG[3] = X	RAM_CFG[3] = X	RAM_CFG[3] = X	RAM_CFG[3] = X	
ROM_SO	FB[1] = 1	FB[0] = 0	SMBUS_ALT_ADDR = 0	VGA_DEVICE = 1	1000 => PU 4.99K
STRAP0	USER[3] = 1	USER[2] = 1	USER[1] = 1	USER[0] = 1	use EDID 1111 => PU 45.3K
STRAP1	3GIO_PADCFG[3] = 0	3GIO_PADCFG[2] = 0	3GIO_PADCFG[1] = 0	3GIO_PADCFG[0] = 0	Gen 3 support 0000 =>PD 4.99K
STRAP2	PCI_DEVID[3]=	PCI_DEVID[2]=	PCI_DEVID[1]=	PCI_DEVID[0]=	0100 => PD 24.9K
STRAP3	SOR[3]_EXPOSED = 0	SOR[2]_EXPOSED = 0	SOR[1]_EXPOSED = 0	SOR[0]_EXPOSED = 0	0000 => PD 4.99K
STRAP4	Reservd	PCIE_SPEED _CHANGE_GEN3 = 1	PCIE_MAX_SPEED = 1	DP_PLL_VDD33V = 1	0111 => PD 45.3K

Table 113

	PU	PD
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

4.99K 10G212499114030
10K 10G212100214030
15K 10G212150214030
24.9K 10G212249214030

N501 R7618

VRAM	2G	03008-00020900	GDDR5 64M*32-0.3 1.5V FBGA170	HYNIX/H5GC2H24BFR-T2C	PD-10K	0001	0x1
		03008-00020500	GDDR5 64M*32-0.3 1.5V FBGA170	SAMSUNG/K4G20325FD-FC03	PD-4.99K	0000	0x0
	4G	03008-00030100	GDDR5 128M*32-0.3 1.5V FBGA170	HYNIX/H5GC4H24MFR-T2C	PD-15K	0010	0x2
		03008-00030400	GDDR5 128M*32-0.3 1.5V FBGA170	ELPIDA/EDW4032BABG-60-F	PD-24.9K	0100	0x4

ASUSTek Computer Inc.

Title : VGA_XTAL/STRAPPING(7)
Engineer: RD1/EE1
Size: C
Project Name: N501JW
Rev: 2.0
Date: Monday, March 16, 2015
Sheet 76 of 98

Title : *****

ASUSTeK COMPUTER INC. NB4

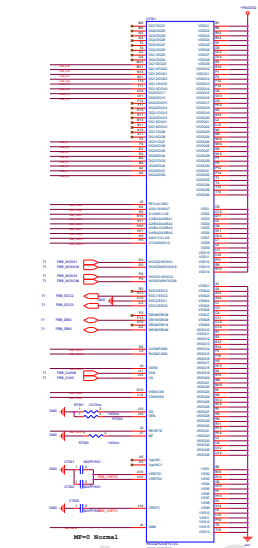
Engineer: RD1/EE1

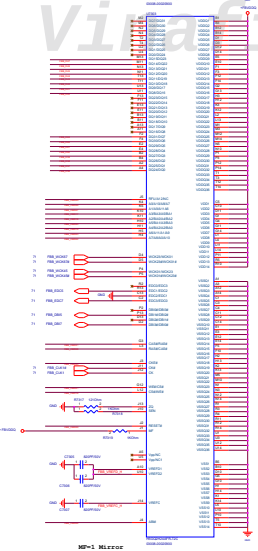
Size	Project Name	Rev
C	N501JW	2.0

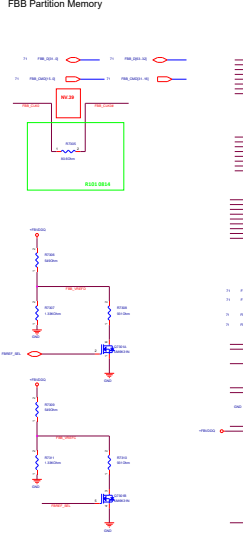
Date:	Monday, March 16, 2015	Sheet	79	of	98

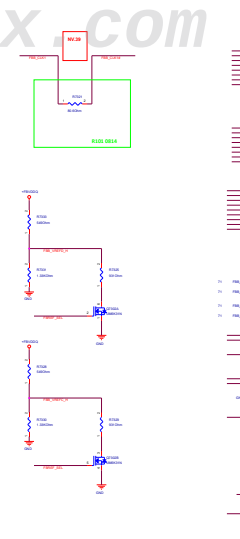
FBB Partition Memory

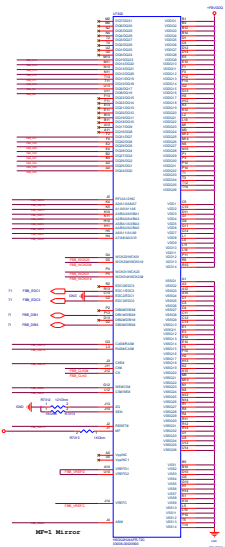
VRAM 03G15174J110 GDDR5 64M*32
SAMSUNG/K4G20325FC-HC04

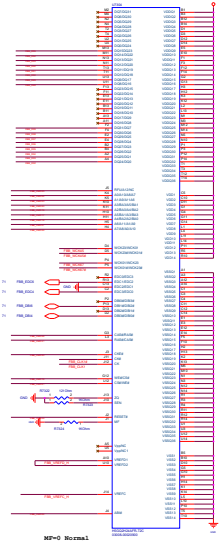




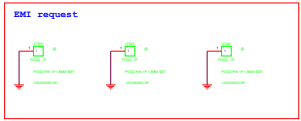




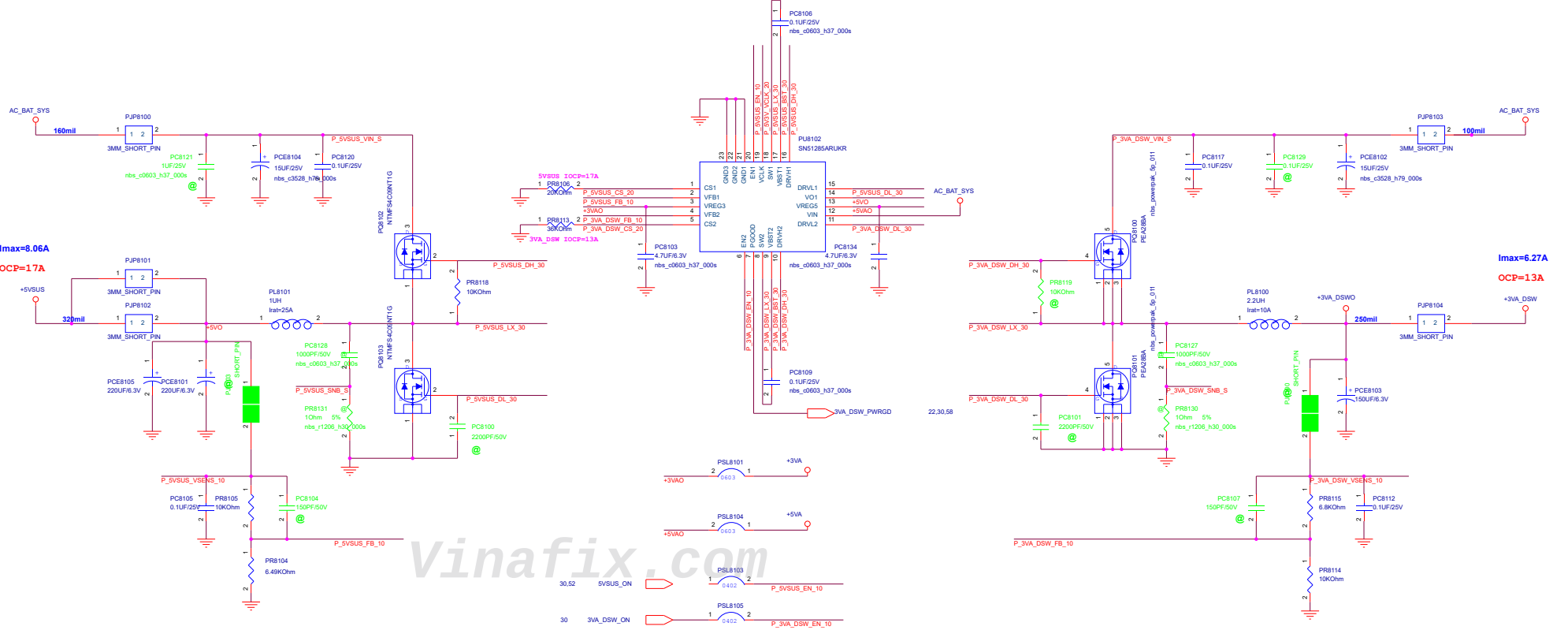


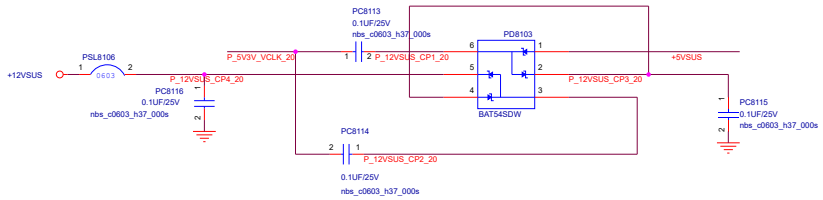


EMI request

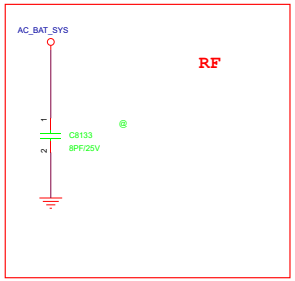


Title :	VGA VRAM DI_II
Engineer:	REV:1.0/1
Project Name	N550JV





請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



Adaptor Mode (VR12.6 non CS & VR12.5)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Adaptor Mode (VR12.6 with CS)

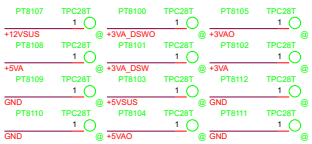
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	1	-	-	1	-	1
3VADSW_ON	1	1	-	-	1	-	1
3VSUS_ON	1	1	-	-	0	-	0
5VSUS_ON	1	1	-	-	1	-	1
1.2V_ON	1	1	-	-	0	-	0
SUSC_EC#	1	1	-	-	0	-	0
SUSB_EC#	1	1	-	-	0	-	0

Battery Mode (VR12.6 non CS & VR12.5)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

Battery Mode (VR12.6 with CS)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	1	-	-	0	0	1
3VADSW_ON	1	1	-	-	0	0	0
3VSUS_ON	1	1	-	-	0	0	0
5VSUS_ON	1	1	-	-	0	0	1
1.2V_ON	1	1	-	-	0	0	0
SUSC_EC#	1	1	-	-	0	0	0
SUSB_EC#	1	1	-	-	0	0	0



<variant_name>

ASUSTeK COMPUTER INC. NB

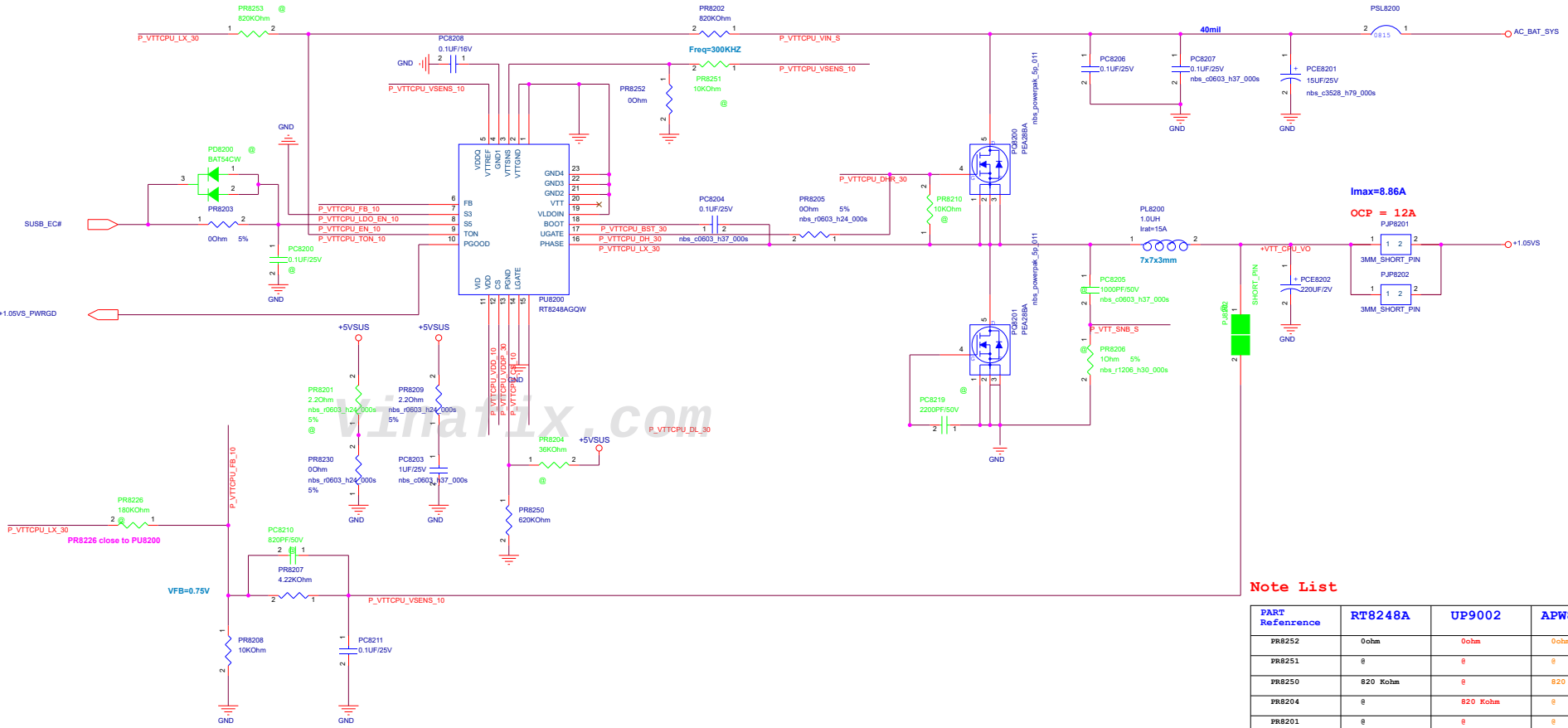
Title : POWER_SYSTEM

Engineer: RD1/EE1

Size	Project Name	Rev
Custom	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 61 of 98

+VTT_PCH & dGPU POWER SUPPLY



Note List

PART Refenrence	RT8248A	UP9002	APW8868
PR8252	0ohm	0ohm	0ohm
PR8251	@	@	@
PR8250	820 Kohm	@	820 Kohm
PR8204	@	820 Kohm	@
PR8201	@	@	@
PC8201	0ohm	0ohm	0ohm
PR8250	OCP自行設定	@	@
PR8204 <Variant Name>	@	OCP自行設定	OCP自行設定

PT8207 TPC28T +VTT_CPU_VO
PT8208 TPC28T +VTT_CPU_VO
PT8206 TPC28T GND
PT8211 TPC28T GND
PT8201 TPC28T +1.05VS
PT8202 TPC28T +1.05VS
PT8203 TPC28T +1.05VS
PT8205 TPC28T GND

ASUSTeK COMPUTER INC. NB

Title : SB 1.05VS

Engineer: RD1/EE1

Size: Custom | Project Name: N501JW | Rev: 2.0

Date: Monday, March 16, 2015 | Sheet 82 of 98

MEMORY(4.88A) & CPU(4.2A) POWER SUPPLY

S3/S0 / S5 / S5

30 1.35V_ON — PR8379 5% @ — 0Ohm — PR8378 0Ohm 5% — P_1V35_S5_10

22,30 PM_SUSC# — PR8380 5% — 0Ohm

PD8300 BAT54CTB @ — PC8300 0.1UF/25V @ — GND

S0 / S3/S5 / S3/S5

30,45,57,70,82,84,89,91 SUSB_EC# — PR8300 39KOHM — P_1V35_S3_10

PD8301 BAT54CTB — PC8301 1UF/6.3V — GND

S3 And S5 Truth Table

State	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Low	Hi	On
S4/S5	Low	Low	Off (Discharge)

State	VTTREF	VTT
S0	On	On
S3	On	Off(Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)

+0.675VS — 40mil — PC8306 10UF/6.3V nbs_c0805_h57_000s — PC8307 10UF/6.3V nbs_c0805_h57_000s — GND

Freq=300KHZ — PR8351 10KOhm — P_1V35_VSENS_10 — PR8352 0Ohm — PC8308 0.1UF/16V

+1.35VS — 40mil — PJP8300 — P_1V35_VIN_S — PC8304 0.1UF/25V nbs_c0603_h37_000s — PC8303 0.1UF/25V nbs_c0603_h37_000s — PCE8325 15UF/25V nbs_c3528_h79_000s — 60mil — PSL8301 0815 — AC_BAT_SYS

PR8353 820KOhm @ — P_1V35_LX_30 — Freq=300KHZ — PR8318 820KOhm — P_1V35_VIN_S — 1.35V_PWRGD

PU8300 RT8248AGQW: VDDQ VTTREF GND1 VTTGND VTTSNS VTTGND GND4 GND3 GND2 VTT VLDOIN BOOT UGATE PHASE FB S3 S5 TON PGOOD VID VDD CS PGND LGATE

P_1V35_FB_10 — P_1V35_S3_10 — P_1V35_S5_10 — P_1V35_TON_10 — P_1V35_VLDOIN_30 — P_1V35_BST_30 — P_1V35_DH_30 — P_1V35_LX_30 — P_1V35_DHR_30 — P_1V35_DL_30

PC8309 0.1UF/25V — PR8307 0Ohm 5% — nbs_c0603_h24_000s — PC8310 1UF/25V nbs_c0603_h37_000s — PR8321 10KOhm

PQ8300 PEA288A — PQ8301 PEA288A — nbs_powerpak_5p_011

PL8301 1.0UH Irat=15A — 7x7x3mm — +1.35VO — Imax=9.08A — OCP=12A — +1.35V

PJP8302 — PJP8303 — 3MM_SHORT_PIN — 360mil

PJ8301 SHORT_PIN — PCE8300 470U/2V

+1.35V — PC8335 0.1UF/16V — PC8336 1UF/6.3V

+5VSUS — PR8309 2.2Ohm nbs_r0603_h24_000s 5% — PR8310 2.2Ohm nbs_r0603_h24_000s 5% — PR8312 56KOhm — PR8330 0Ohm nbs_r0603_h24_000s 5% — PC8313 1UF/25V nbs_c0603_h37_000s — PR8350 620KOhm

P_1V35_VDD_10 — P_1V35_VDDP_30 — P_1V35_CS_10

PC8311 1000PF/50V @ — PC8314 1000PF/50V @

PR8301 432KOhm — P_1V35_LX_30 — 0.75V — PR8314 10KOhm — PR8313 8.2KOhm 10G212820114030 — PC8315 0.1UF/16V

PR8315 10OHM — PSL8302 0402 — P_1V35_RESENS_10 — P_1V35_FBJP_10 — PJ8303 SHORT_PIN@ — +1.35V

RF — +1.35V — C8332 8PF/25V @ — C8333 8PF/25V @ — GND

Note List

PART Refenrence	RT8248A	UP9002	APW8868
PR8352	0ohm	0ohm	0ohm
PR8351	@	@	@
PR8350	820 Kohm	@	820 Kohm
PR8312	@	820 Kohm	@
PR8309	@	@	@
PC8312	0ohm	0ohm	0ohm
PR8350	OCP自行設定	@	@
PR8312	@	OCP自行設定	OCP自行設定

<Variant Name>

ASUSTeK COMPUTER INC. NB — Title : SB DDRL — Engineer: RD1/EE1

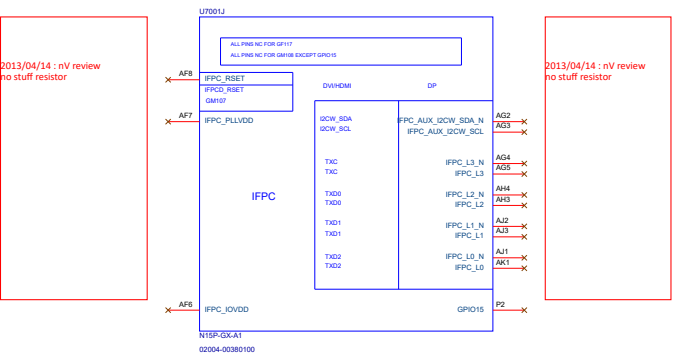
Size: C — Project Name: N501JW — Rev: 2.0

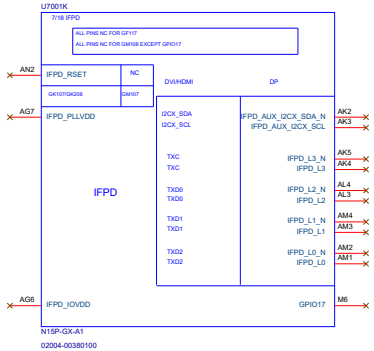
Date: Monday, March 16, 2015 — Sheet 83 of 96

DG-06246-001_v02 p157 DG8.6
IPF not used
IFPxy_IOCDD/IFPxy_PLLVDD 10K PD
Other pin NC

DP(link C)

DVI(link D)





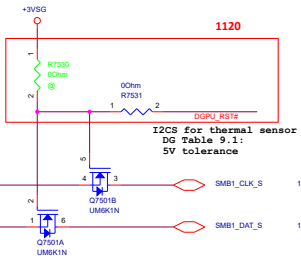
DG-06246-001_v03 p186 Table 114

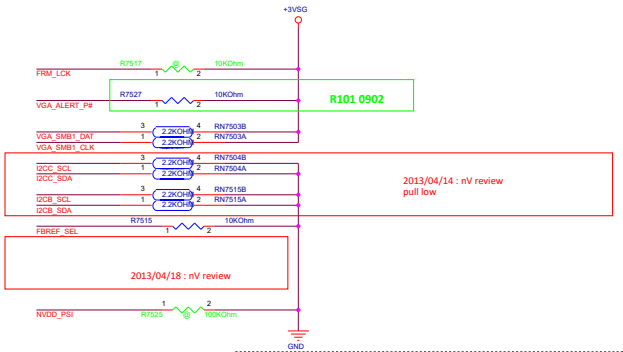
GPIO ASSIGNMENTS

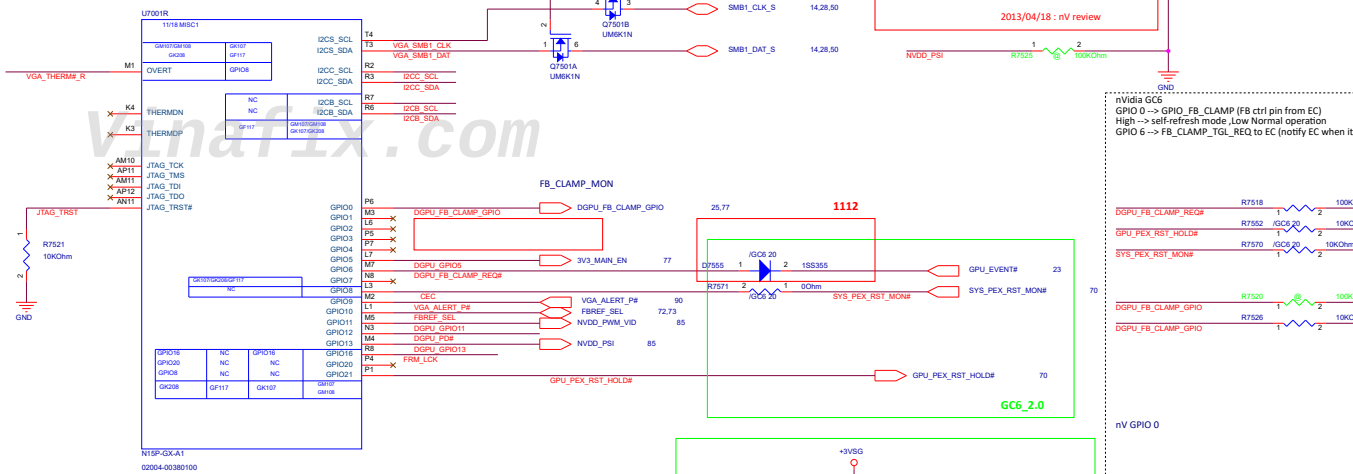
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	FB_CLAMP_MON
1	OUT	N/A	MEM_VDD_CTL
2	OUT	HIGH	LCD_BL_PWM
3	OUT	HIGH	LCD_VCC_EN
4	OUT	HIGH	LCD_BL_EN
5	N/A	N/A	Reserved
6	OUT	N/A	FB_CLAMP_TGL_REQ
7	OUT	N/A	3D Vision L/R signal
8	I/O	LOW	OVER THERMAL
9	I/O	LOW	THERMAL ALERT
10	OUT	N/A	MEM_VREF_CTL
11	OUT	N/A	PWM_VID
12	IN	N/A	AC DETECT
13	OUT	N/A	PSI Phase Shedding
14	IN	N/A	IFPAB HOTPLUG
15	IN	N/A	IFPC HOTPLUG (HDMI)
16	OUT	N/A	FRM_LCK JT Frame Lock signal
17	IN	N/A	IFPD HOTPLUG
18	IN	N/A	IFPE HOTPLUG
19	IN	N/A	IFPF or IPFB(DP) HOTPLUG
20	N/A	N/A	Reserved
21	N/A	N/A	Reserved

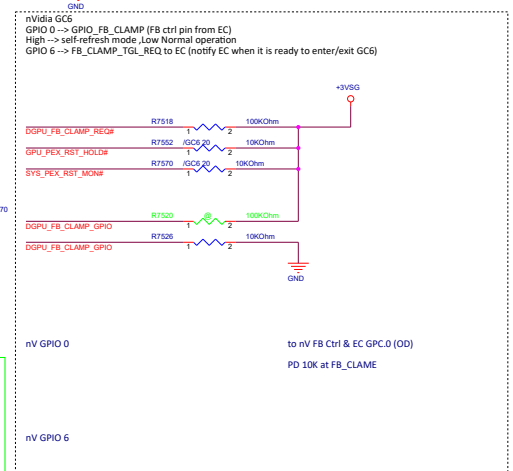
GPIO, TEMP SENSOR, JTAG

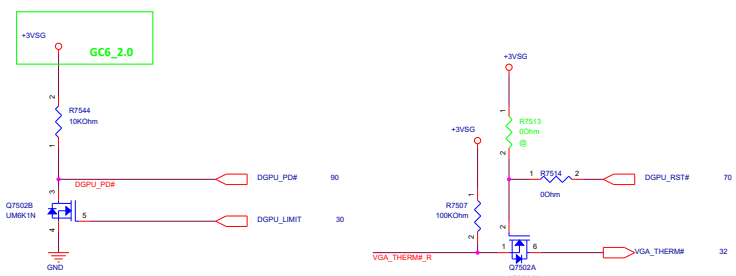
N14X : I2C ADDRESS: 0x9Eh

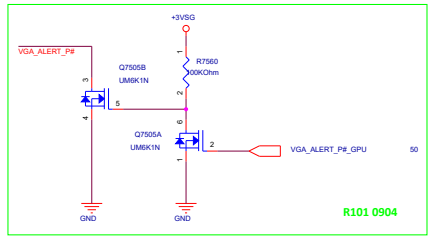






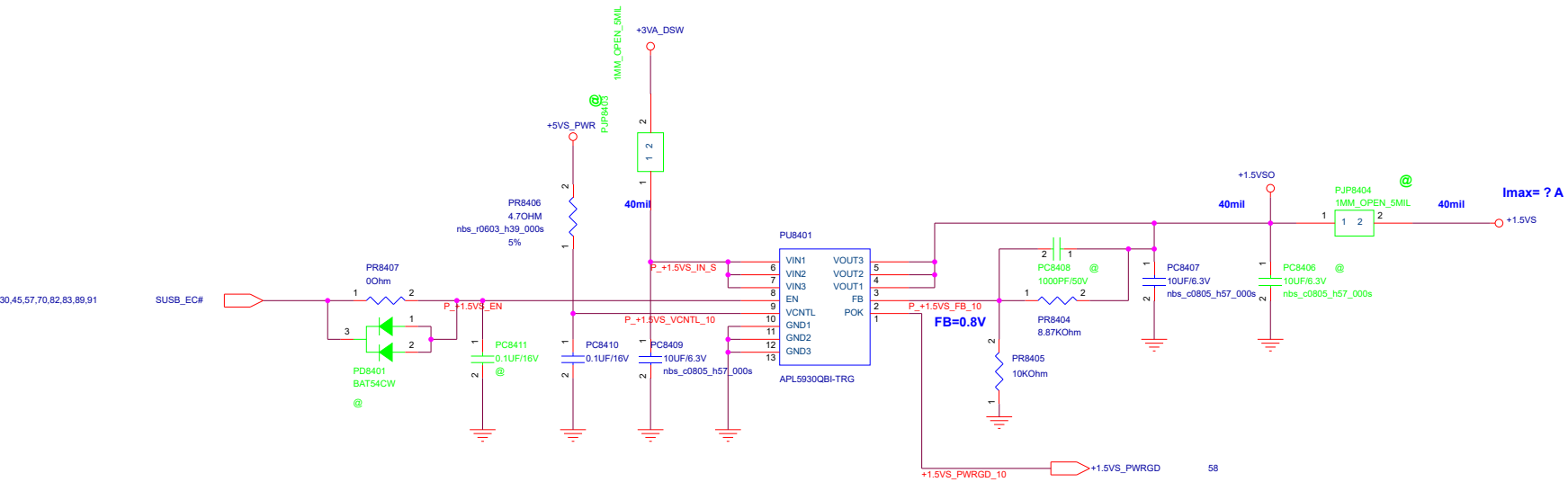






ASUSTeK Computer Inc.	Title : VGA_GPIO/DVI/DP(6)		
	Engineer: RD1/EE1		
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet: 75	of: 98	

+1.5VS POWER SUPPLY FOR PCH

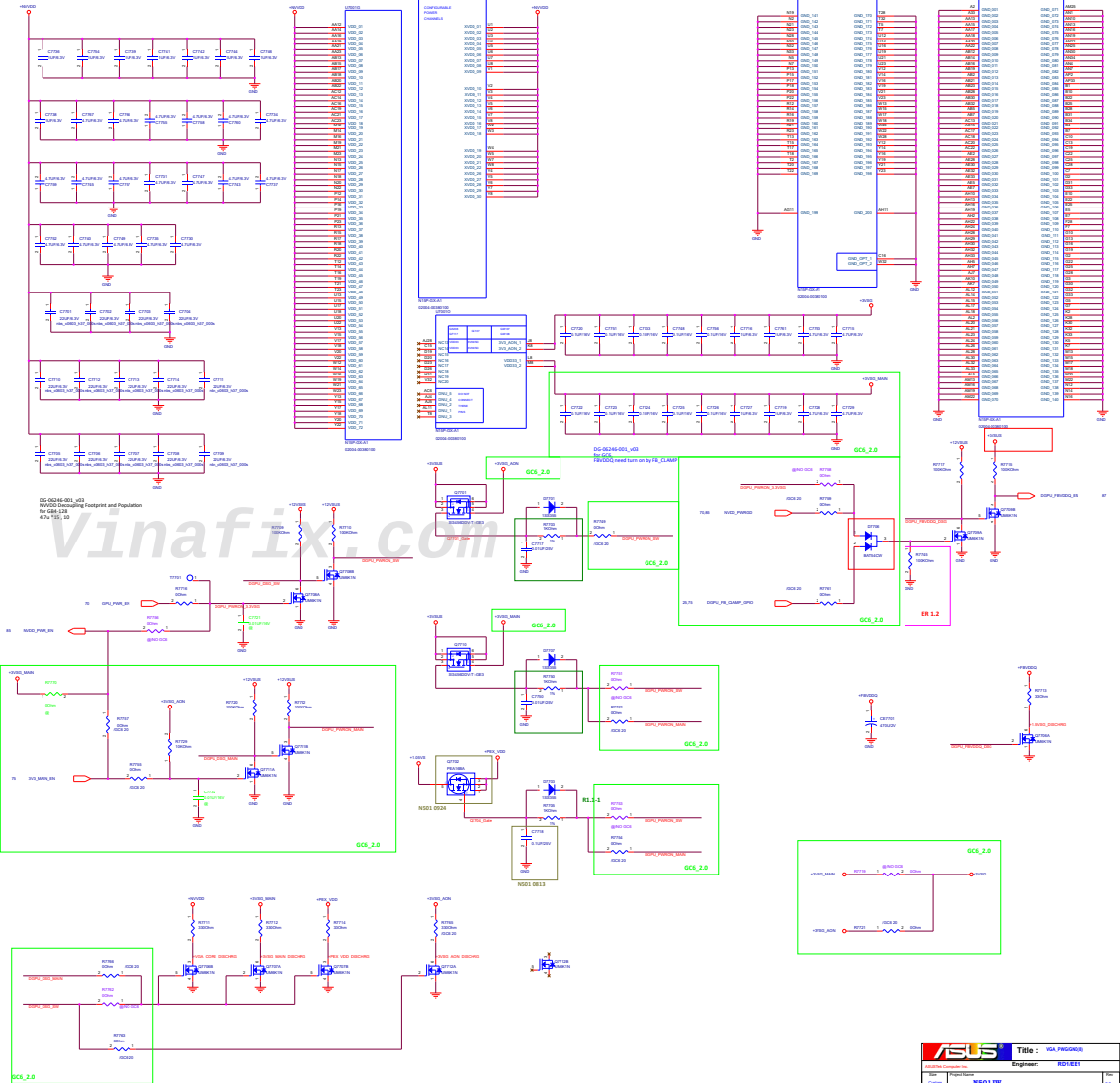


Vout	1.05V	1.2V	1.5V
PR8404	3.16K	5.11K	8.87K
PR8405	10K	10K	10K

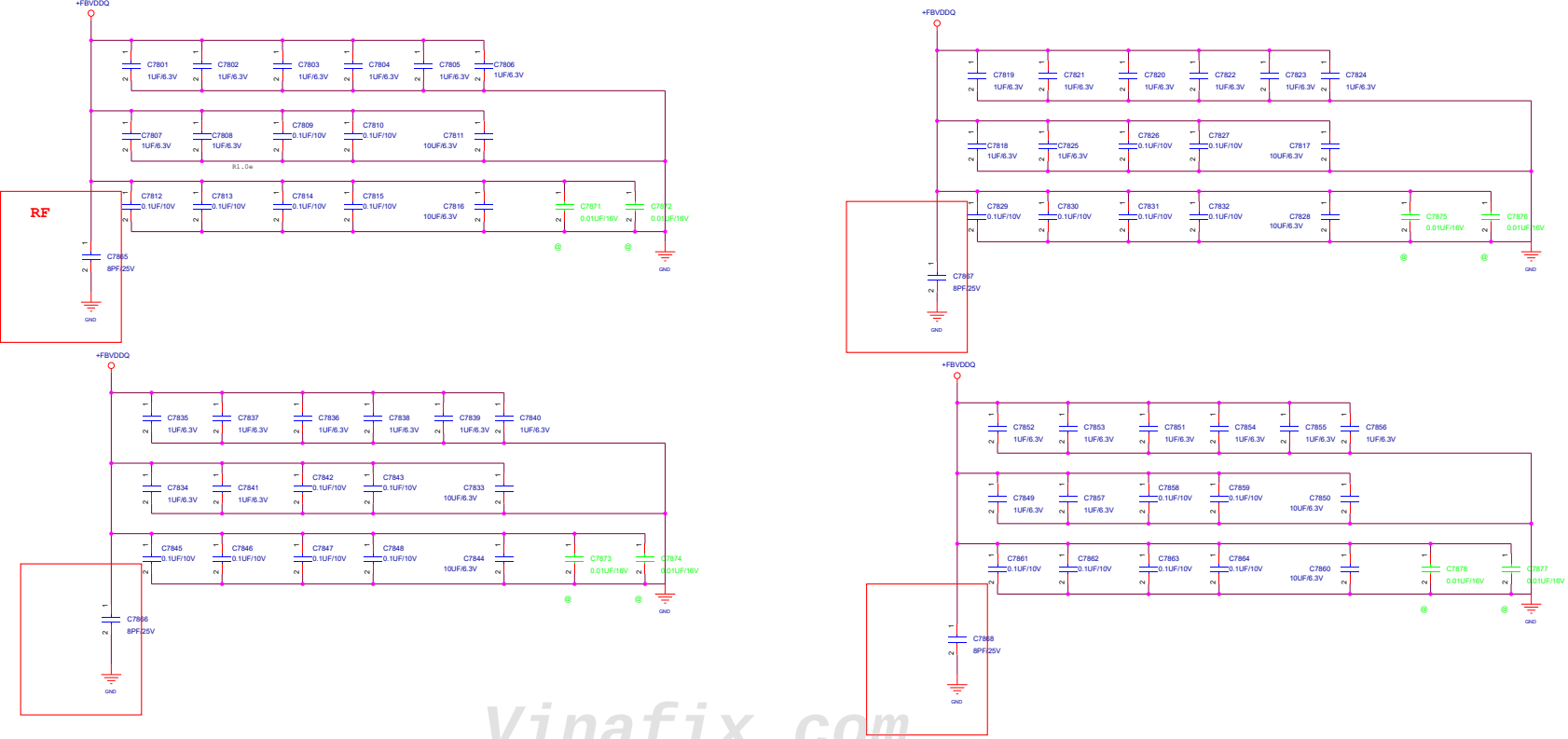
ASUSTeK COMPUTER INC.	Title :	PW_+1.5VS_PCH
	Engineer:	RD1/EE1
Size: B	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 84 of 98	

NVVDD POWER AND DECOUPLING

NVVDD GROUND



Title :	VGA_PWG(NDE)
Engineer:	RDI/EE1
Size	Project Name
Custom	NS01JW
Date: Monday, March 16, 2015	Sheet 17 of 66

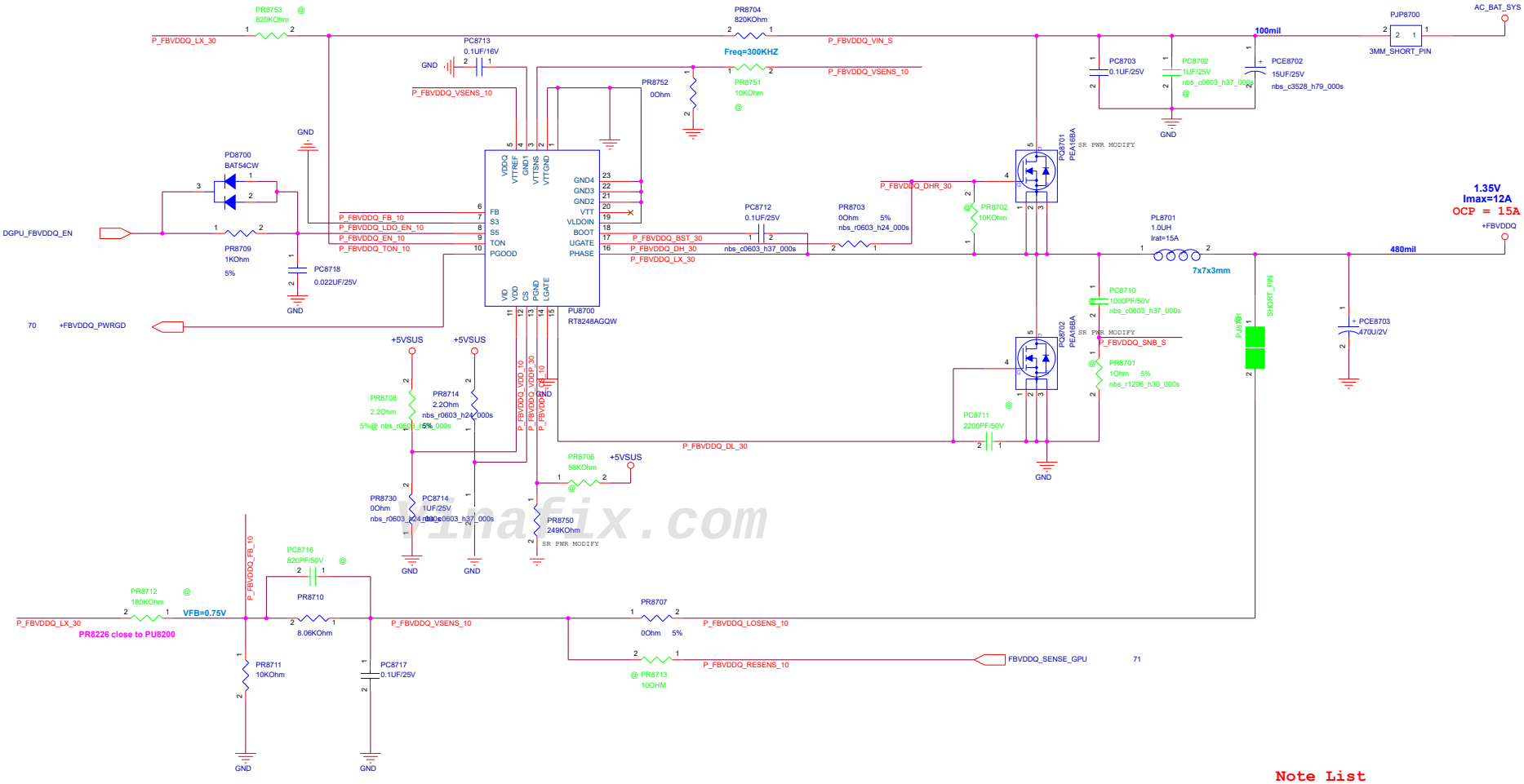


ASUSTeK COMPUTER INC. NB4	Title :	VRAM CAP
	Engineer:	RD1/EE1
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 78 of 98	

<Variant Name>

ASUSTeK COMPUTER INC.	Title : Black light	
	Engineer: RD1/EE1	
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 86 of 98	

VRAM POWER SUPPLY

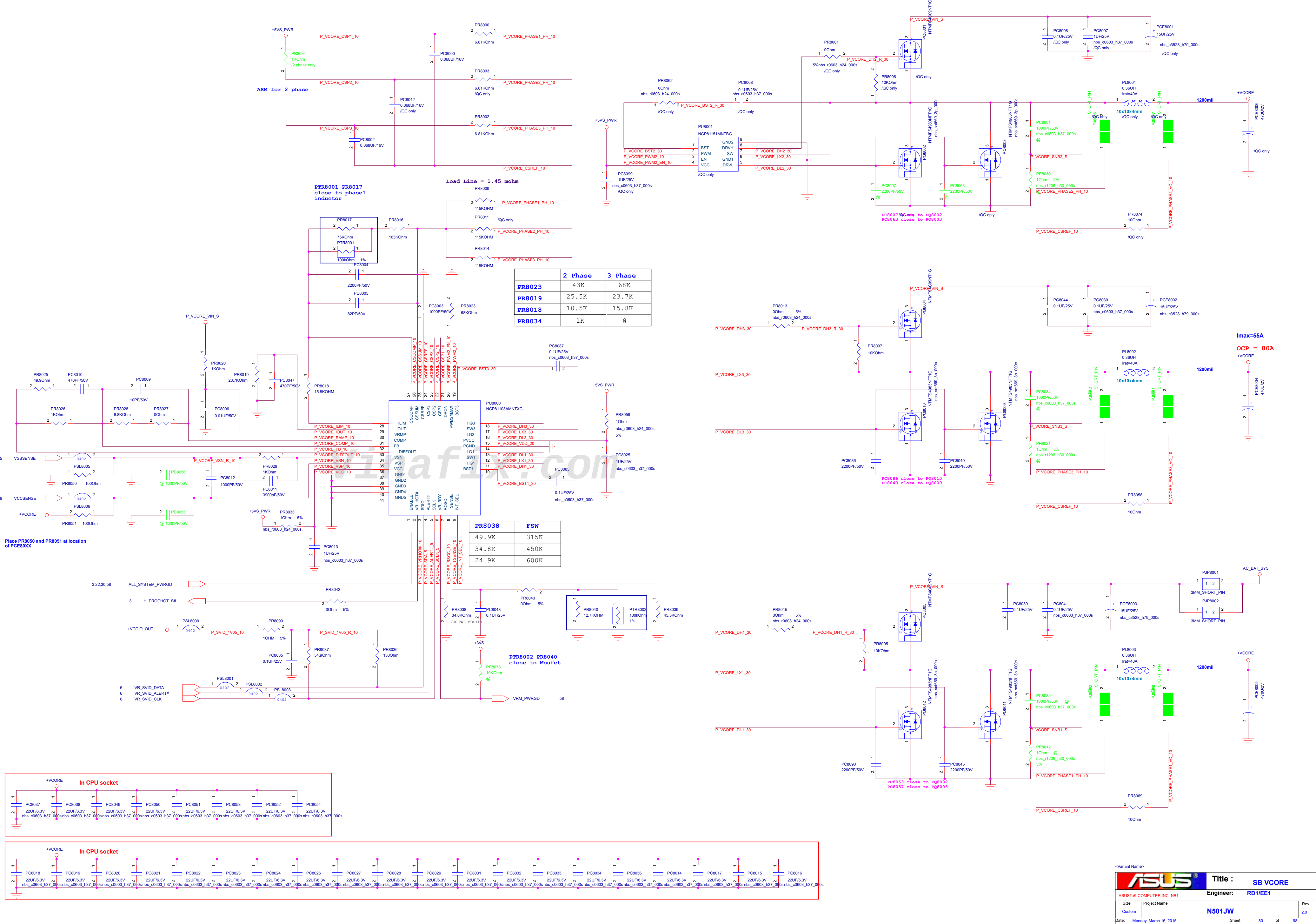


Note List

PART Refenrence	RT8248A	UP9002	APW8868
PR8752	0ohm	0ohm	0ohm
PR8751	@	@	@
PR8704	820 Kohm	@	820 Kohm
PR8706	@	820 Kohm	@
PR8708	@	@	@
PC8702	0ohm	0ohm	0ohm
PR8750	OCP自行設定	@	@
PR8706	@	OCP自行設定	OCP自行設定

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : SB FBVDDQ	
	Engineer: RD1/EE1	
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 87 of 98	



	2 Phase	3 Phase
PR8023	43K	68K
PR8019	25.5K	23.7K
PR8018	10.5K	15.8K
PR8034	1K	@

PR8038	FSW
49.9K	315K
34.8K	450K
24.9K	600K

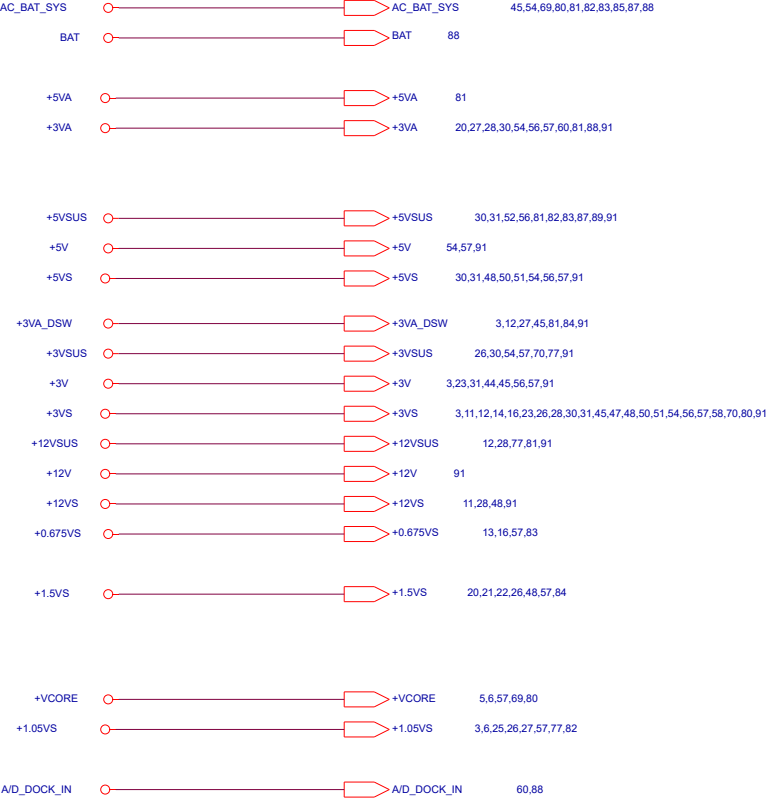
FBA Partition Memory (1 of 2)

GDD5 MODE SELECTION

MODE	MF	ESC1	ESC2
x32	0	VDDQ	VDDQ
x32	1	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

VRAM 03G15174J110 GDDR5 64M*32
SAMSUNG/K4G20325FC-HC04

FBA Partition Memory (2 of 2)



ASUSTeK COMPUTER INC. NB8

Title : POWER_SIGNAL

Engineer: RD1/EE1

Size	Project Name	Rev
Custom	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 93 of 98

1224 1. change on board memory on b channel
2. change EC to BGA type
1224_2 3. change key board and lan remove
1226 4. ngff sata colay
1226_2 5. modify p45
1227 6. change to DDR5
7. change to DDR5 part number
8. Add Memory down GPIO select pin
0108 9. Change small keyboard
10. Change TPanel to usb5
11. add sata ngff susck pin & desleep pin
0110 12. add HDMI level shift ic
13. change mem clk termination pull cap low
0115 14. change mem x8 to x16
15. HDD colay NGFF2 for raid sku
0121 16. change CPU cap 0805 to 0603 22uf
17. modify p54 IO board pin define
0123 18. DDR3L change to 512x8
0124 19. change pwr to 0124
0125 20. add TPM & del HDD
0130 21. add DP repeater IC
0204 22. Change HDMI level shift IC
0207 23. add p54 AOAC
0219 24. Change pwr 0207
25. add lid switch &wlan led p56
0220 26. add cap & pwr led p56
0222 27. P47,48 OOHM 4r8p change to 0201
0227 28. change EC footprint NBS_BGA_128P_NONHDI_002
0304 29. layout swap 0303/0304
30.remove speaker to IO board
0305 31.change pin define IO board p.54
0307 32.change led board add mic
33.layout swap otherswap0306
0308 34. RF request
0311 35. Change pwr 0307
0312 36. Change pwr 0312
0318 37.layout swap 0318
0318_2 38. change pwr to 0318
39. add DP repeter DC cap
0319 40. RF request
0321 41. change to n46 r2.0
0326 42. link fbvddq_pwrgd
0403 43.remove HDMI EMI res
44.remove CCD int for EC team request
45.remove CE0606 CAP
46.remove CE7702 CAP
47.add p59 LED MIC IO board
0411 48.add EDP repeater
0412 49.swap0411 for layout request
0416 50.modify nvidia request
51.modify RF0410 request
0418 52.modify nvidia request test point
53.add VGA thermal sensor
0422 54.change keyboard con
56.add aux co-lay res p.46,47
0424 57.change pwr 0424 and add backlight IC
58.del p58 +1.2VS_PWRGD &P_1VS8_PWRGD
0503 59.remove LED board p59
60.change keyboard con part number
0506 61.del battery con bat_in_oc# pin for inside
0507 62.modify aux co-lay res p.46,47
0508 63.modify strap res for nvidia
64.modify touch pad pin reverse
65.link vram commad 16
0516 66.add +3vs p.30
67.remove jp p.6 +vtt_cpu
68.modify TPM
0520 69.change i2c level shift IC
70.modify led follow ux31LA
0521 71.add short line p.21 for DP ssc CLK
0524 72.change pwr to 0524
0528 73.del sl2123 sl2124 for dp ssc
0529 74.change screw hole
0603 75.update pwr 0603
0606 76.update battery con
0610 77.update +3vs_lcd to +3vs
0617 78.del tp power 2pin to lpin
0618 79.change io board pin50 3vsus to 3va
0619 80.change DEBUG connector
0627 81.change subsystem id
0701 82.change connector for ME
83.change PWR to 0701
84.debug pin change
0702 85.change EC part number & c7811 10uf 0805 to 0603
0703 86.swap keyboard for layout
87.add cap & res for EMI request
0808 88.modify EC short pin to GND(PIN K5) , battery in pull low, EDP repetor HPD modify ,AUX_N/P pull 10k
0808_2 89.UPdate GC62.0 schematic
0812 90.SDD unmount 10k pull low, nvdivia GC6 20 power plan
91.EDP AUX repetor add cap
0816 92.XVDD pu nvdd
0819 93.ADD NGFF PCIE solution, layout swap request , pwr change to 0819,
0822 94.change power plan for nvidia request
0826 95.modify power schematic to 0826
0827 96.modify power schematic to 0827
0916/0918 97.C1308 mount , nvdd pwrok pull to 3vsg_main , modify res to 36 ohm p21.13
0925 98.EDP RP HPD modify p46
0930 99.power modify to 0927
1007 101.power modify to 1007
1009 102.update screw hole
1016 103.TP panel add pltrst# pin
1017 104.Change BL enable schematic
Change keyboard BL pin define
add ALS_INT# pin
1112 105.add diode for nv request
EDP repter power plane change to +3vs_rp
1113 106.NGFF change to pice x4 for 2280
Q7001 change part number
1119 107.update pwr to 1119
update IO schematic
1120 108.For NV request
1122 109.Modify repter HPD signal to pull high
change Touch pad pin define
1125 110.update pwr to 1125 p.80,88
1128 110.update pwr to 1128 p88
1129 112.update pwr to 1129 p85
1202 113.remove HDMI PCH trace for 4k2k
1205 114.add pad for EMI request p73

R1.2

1209 115.power modify p.80,81,88

Rev	Date	Description
R1.0	2012/10/31	Initial
R1.1	2013/08/14	1. change thermal sensor power plan to 3vs for nvidia request 2. change vram clk series res to 80 OHM for nvidia spec 3. GPU_PEX_RST request pull low
	2013/08/20	4. change power plan for nv request 0819
	2013/08/22	5. change power plan for nv request 0822
	2013/09/04	6. modify vga_alert_p# p.75
	2013/09/25	7. remove EC GPA3 AOAC_WLED and p.56 , change to FAN1_PWM
R1.2	2014/02/07	8. Add cap C3633 for realtek request 9. ER 1.2 for nvidia sequence and EDP modify
	2014/02/11	10.update power controller IC p80~p91 11.R2110 change 30ohm for EA measure 12.R4810,R4813 mount 4.7k
	2014/02/12	13.update power0212 P.87 14.add 0ohm co-lay for RF requet p.45
	2014/02/13	15.del 0ohm co-lay for RF requet p.45 16.add pogoping for RF p.67
	2014/02/19	17.add pc8335,pc8336
	2014/02/20	18.add c4572 for RF p.45
	2014/02/21	19. ER 1.2 for nvidia sequence add diode d7005, mount r7027 , mount pr8520
	2014/02/24	20. RN4811,12,13,14 change to 5.1ohm R4810, mount 4.7k for EA measure
	2014/02/25	21. add screw hold , modify power p82,87,92
R2.0	2014/04/11	22. Mount Q5605 for cap led issue.
	2014/04/15	23. R3201 change to 1.8OHM for led issue 24. change CPU PCH VGA part number
	2014/04/16	25. power modify p.81,88
	2014/04/17	26. power modify p.90 27.LED board modify
	2014/04/18	28.LED board screw hold
	2014/04/22	29.add chock for RF request p.46
	2014/04/24	29.chock pin swap p.46
N501 R0.1	2014/05/20	1. Update PWR Circuit P.80 2. Update SATA connector and Circuit. P51 3. Update KB connector and Pin define(Small to Big)-Follow G751. P31
	2014/05/29	1. Update P.45 eDP connector pin define. Move Light sensor signal from Pin 36 & 37 to Pin 6 & 7. Add DMIC Signal to Pin 36 &37. 2. Add SSD LED control circuit. P.56

ASUSTeK COMPUTER INC. NB8

Title : *****

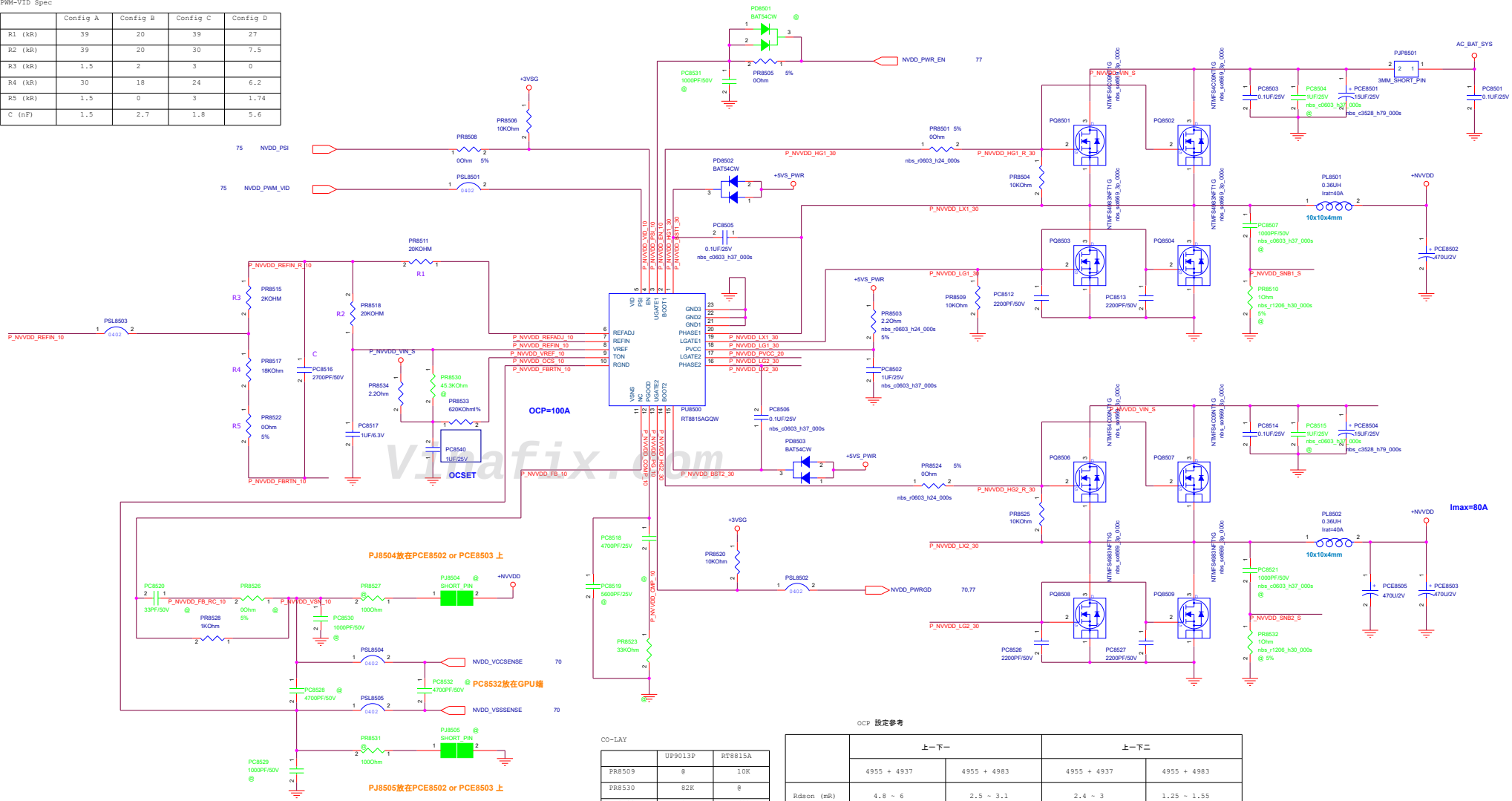
Engineer: RD1/EE1

Size	Project Name	Rev
Custom	N501JW	2.0

Date: Monday, March 16, 2015 Sheet 94 of 98

PWM-VID Spec

	Config A	Config B	Config C	Config D
R1 (kR)	39	20	39	27
R2 (kR)	39	20	30	7.5
R3 (kR)	1.5	2	3	0
R4 (kR)	30	18	24	6.2
R5 (kR)	1.5	0	3	1.74
C (nF)	1.5	2.7	1.8	5.6



CO-LAY

	UP9013P	RT8815A
PR8509	@	10K
PR8530	82K	@
PR8533	0	620K
PR8534	@	2.2
PR8535	150K	1UF
PC8518	4700P	@
PR8523	33K	@

OCP 設定參考

	上一下一		上一下二	
	4955 + 4937	4955 + 4983	4955 + 4937	4955 + 4983
Rdson (mR)	4.8 ~ 6	2.5 ~ 3.1	2.4 ~ 3	1.25 ~ 1.55
R1 (kR)	11	30	30	82
R2 (kR)	20	51	51	150
OCP (理論)	67 ~ 53	80 ~ 65	83 ~ 67	96 ~ 77
OCP (測量)	66 ~ 52	80 ~ 67	83 ~ 69	96 ~ 80

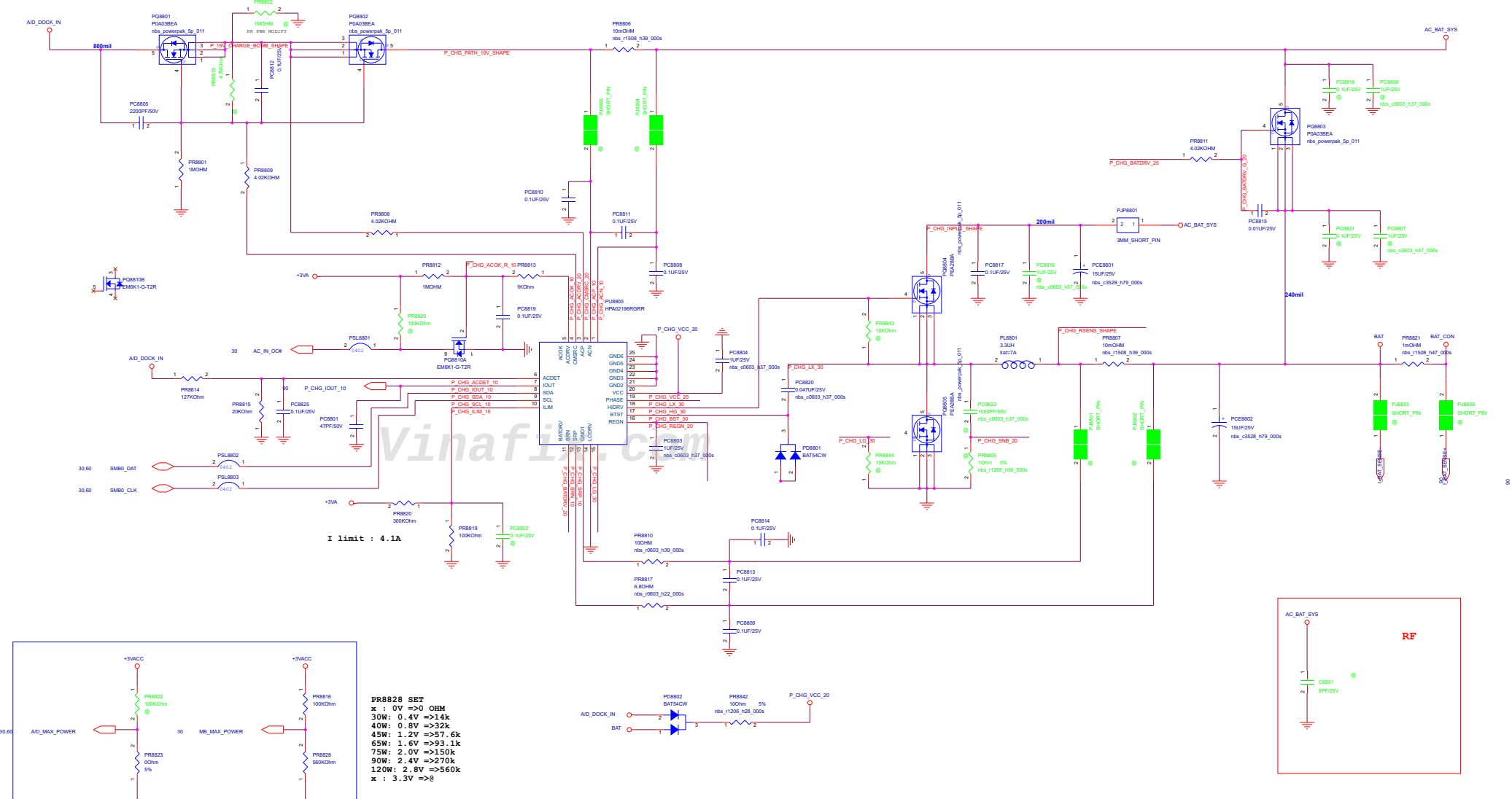
ASUSTek Computer Inc.

Title : NVDD

Engineer: RD1/EE1

Size: Custom | Project Name: N501JW | Rev: 2.0

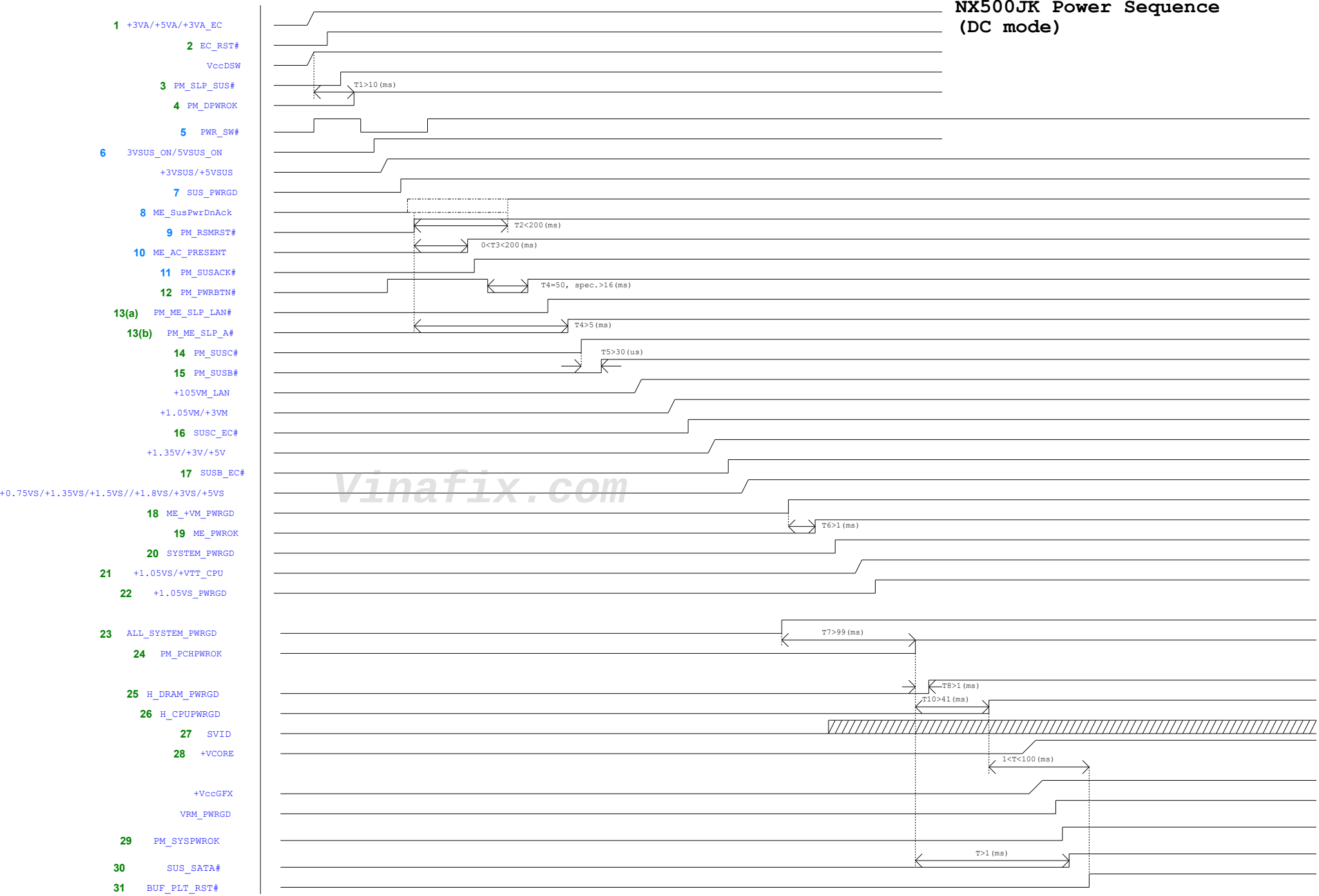
Date: Monday, March 16, 2015 | Sheet 85 of 98



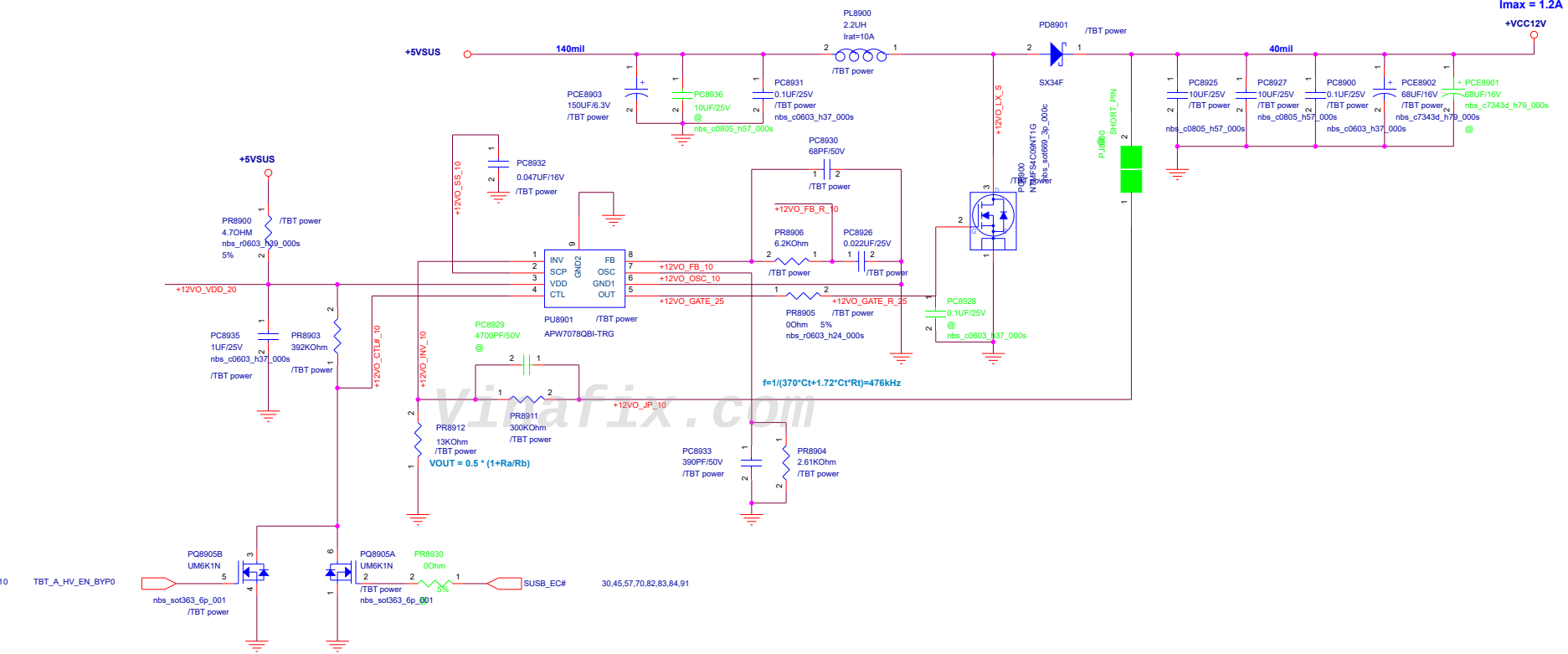
	45W	65W	90W	120W	150W	180W
PR8806	10m	10m	10m	10m	10m	5m
	40.9W	60.1W	85.3W	112.5W	145.5W	175.9W

DC-IN Mode

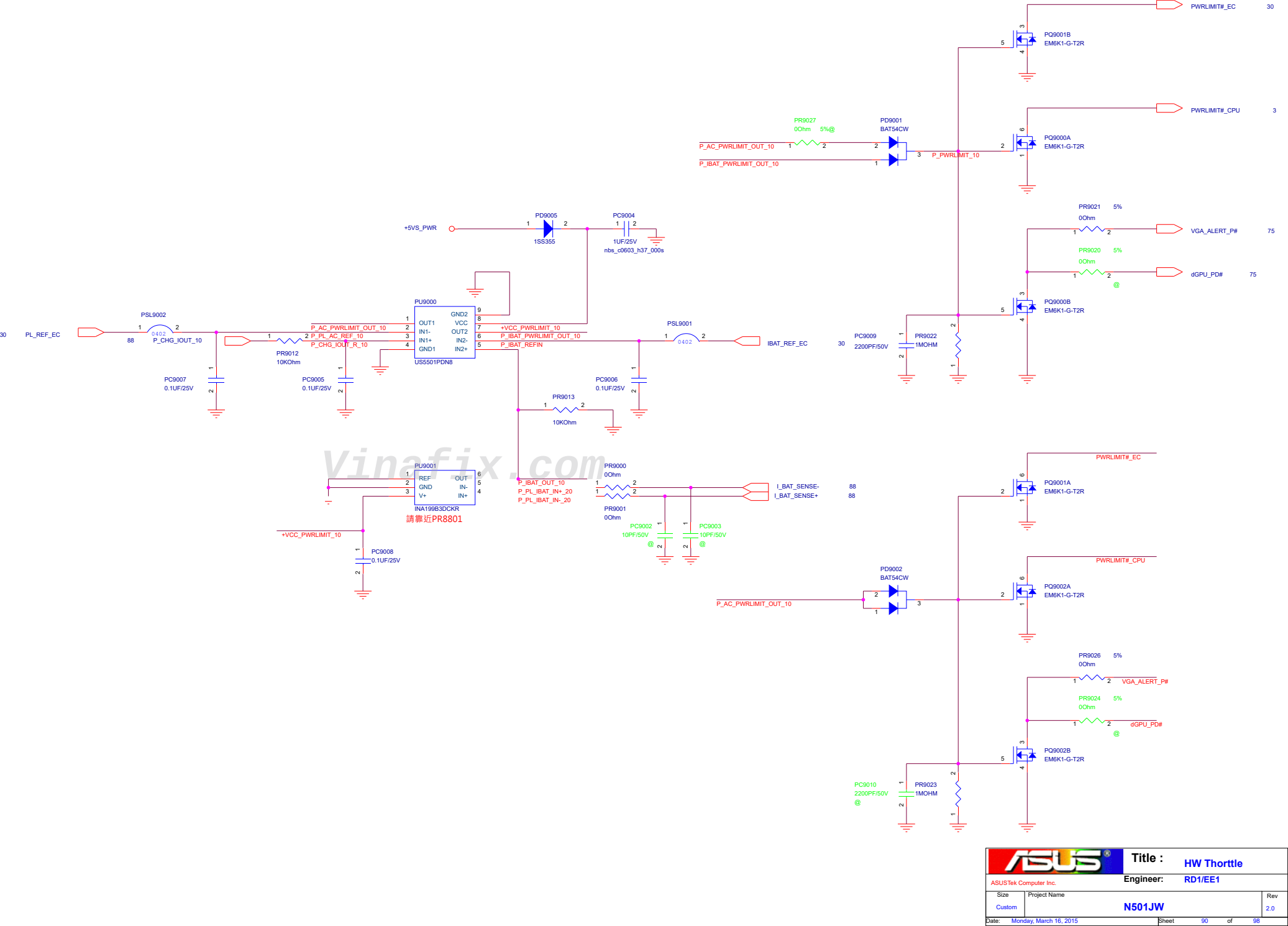
NX500JK Power Sequence (DC mode)



ASUSTeK COMPUTER INC. NB8	Title :	Power Sequence(DC mode)	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 98 of 98		

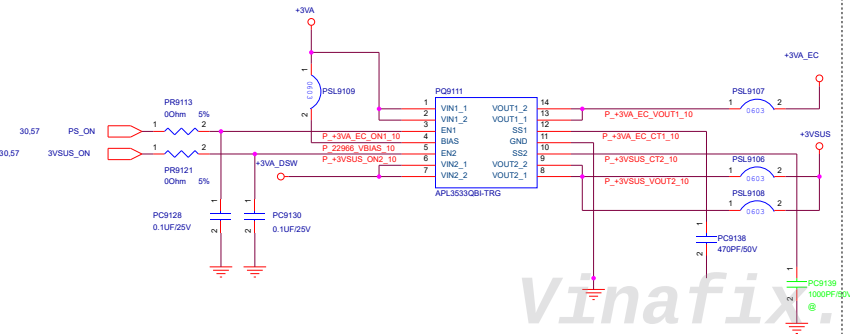


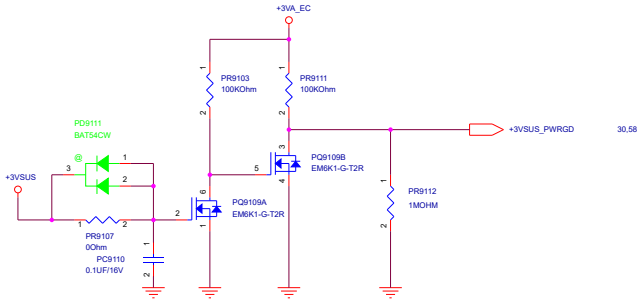
ASUSTeK COMPUTER INC. NB1	Title : TBT		
	Engineer:		
Size: Custom	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 89 of 98		



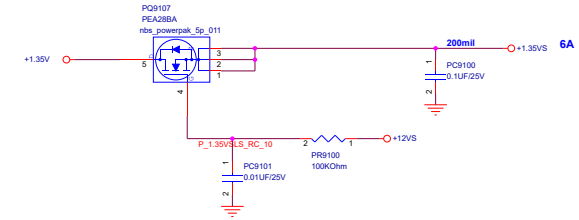
ASUSTek Computer Inc.	Title :	HW Thorttle
	Engineer:	RD1/EE1
Size: Custom	Project Name:	N501JW
		Rev: 2.0
Date: Monday, March 16, 2015	Sheet	90 of 98

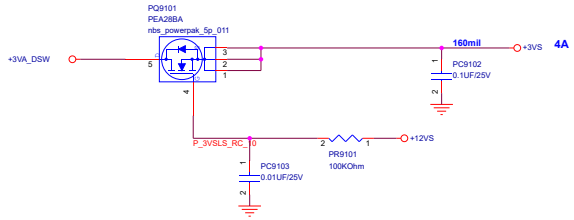
3VSUS POWER



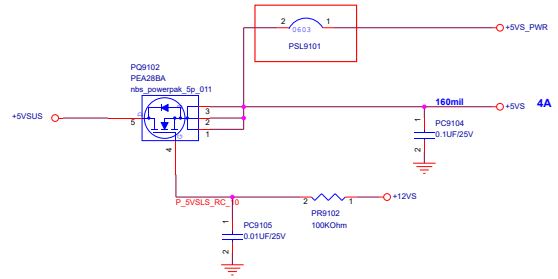


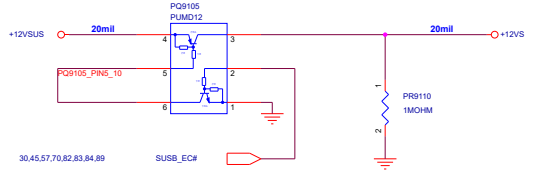
SUSB#_PWR POWER



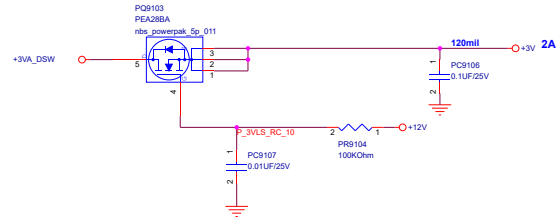


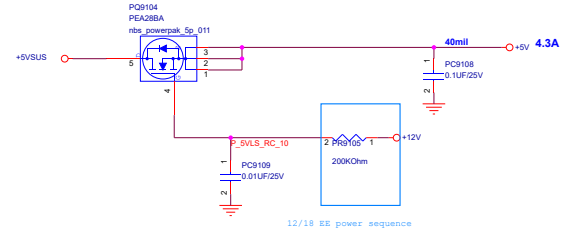
PSL9101 請擺在 PQ9102 旁邊

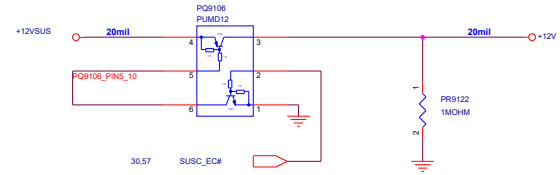




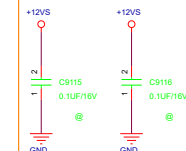
SUSC#_PWR POWER





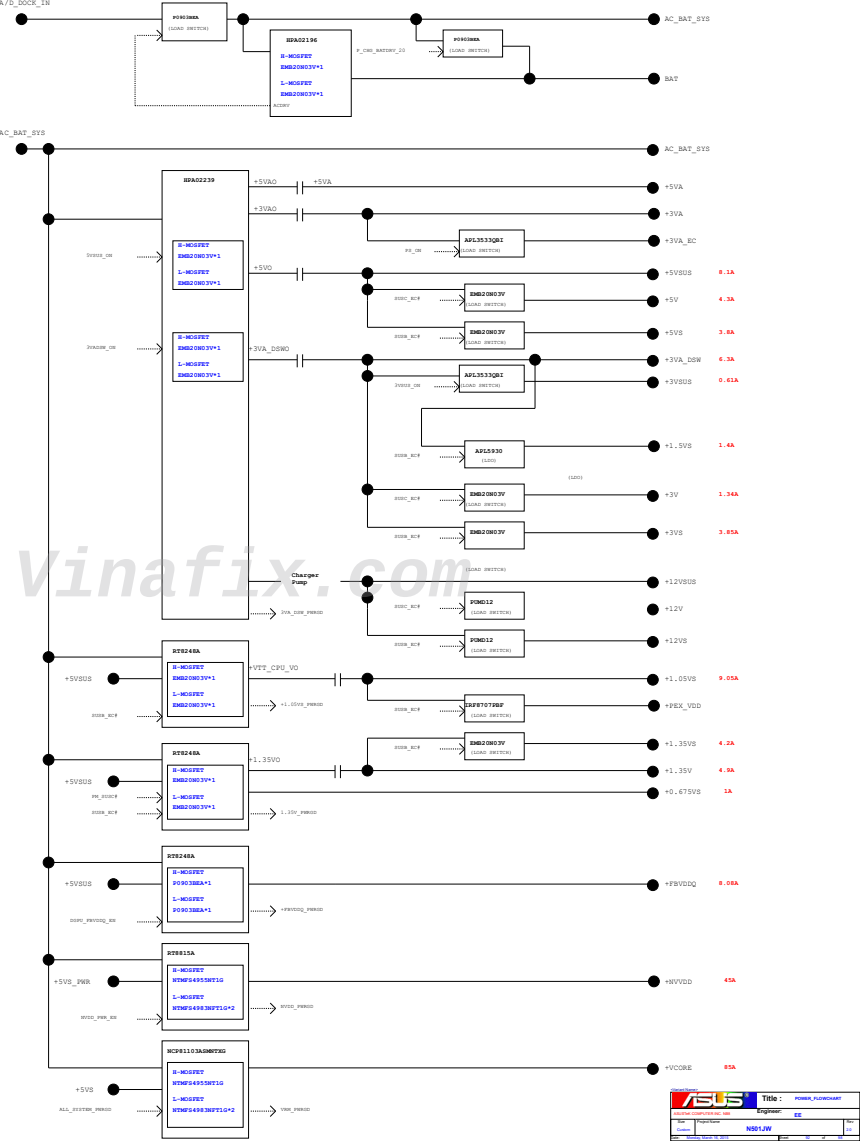


ER1.2 EMI



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : SB LOAD SW	
	Engineer: RD1/EE1	
Size: Custom	Project Name: N501JW	Rev: 2.0
Date: Monday, March 16, 2015	Sheet 91 of 98	


A/D_DOCK_IN
P0903MEA
(LOAD SWITCH)
HPA02196
N-MOSFET
EMB20N03V*1
L-MOSFET
EMB20N03V*1
ACDRV
P_CHG_BATDRV_G
P0903MEA
(LOAD SWITCH)
AC_BAT_SYS
BAT
AC_BAT_SYS
AC_BAT_SYS
HPA02239
+5VAO
+5VA
+5VA
+3VAO
+3VA
+3VA
APL3533QBI
(LOAD SWITCH)
PS_ON
+3VA_EC
5VSUS_ON
N-MOSFET
EMB20N03V*1
L-MOSFET
EMB20N03V*1
+5VSO
+5VSUS
8.1A
SUSC_EC#
EMB20N03V
(LOAD SWITCH)
+5V
4.3A
SUSB_EC#
EMB20N03V
(LOAD SWITCH)
+5VS
3.8A
3VAGSW_ON
N-MOSFET
EMB20N03V*1
L-MOSFET
EMB20N03V*1
+3VA_DSWO
+3VA_DSW
6.3A
APL3533QBI
(LOAD SWITCH)
3VSUS_ON
+3VSUS
0.61A
APL5930
(LDO)
SUSB_EC#
+1.5VS
1.4A
(LDO)
SUSC_EC#
EMB20N03V
(LOAD SWITCH)
+3V
1.34A
SUSB_EC#
EMB20N03V
(LOAD SWITCH)
+3VS
3.85A
Charger
Pump
(LOAD SWITCH)
+12VSUS
PGND12
(LOAD SWITCH)
SUSC_EC#
+12V
PGND12
(LOAD SWITCH)
SUSB_EC#
+12VS
3VA_S5W_PWRGD
RT8248A
+5VSUS
N-MOSFET
EMB20N03V*1
L-MOSFET
EMB20N03V*1
+VTT_CPU_VO
+1.05VS
9.05A
SUSB_EC#
+1.05VS_PWRGD
IRF8707TRPBF
(LOAD SWITCH)
SUSB_EC#
+PEX_VDD
RT8248A
+5VSUS
N-MOSFET
EMB20N03V*1
L-MOSFET
EMB20N03V*1
+1.35VO
SUSB_EC#
EMB20N03V
(LOAD SWITCH)
+1.35VS
4.2A
PM_SUSC#
SUSB_EC#
+1.35V_PWRGD
+1.35V
4.9A
+0.675VS
1A
RT8248A
+5VSUS
N-MOSFET
P0903MEA*1
L-MOSFET
P0903MEA*1
+FBVDDQ
8.08A
DDPU_FBVDDQ_EN
+FBVDDQ_PWRGD
RT8815A
+5VS_PWR
N-MOSFET
NTMFS4955NT1G
L-MOSFET
NTMFS4983NFT1G*2
+NVVDD
45A
NVDD_PWR_EN
NVDD_PWRGD
NCP81103AMNTXG
+5VS
N-MOSFET
NTMFS4955NT1G
L-MOSFET
NTMFS4983NFT1G*2
+VCORE
85A
ALL_SYSTEM_PWRGD
VRM_PWRGD
Title :
POWER_FLOWCHART
Engineer:
EE
Project Name
N501JW
Monday, March 31, 2014

Rev	Date	Description
X1.0	2014/04/23	initial
X1.1	2014/06/27	1. change c4801 12022-00041100 -> 12022-00043100 only change P/N EN need change footprint
	2014/06/30	2. change Y1201 02001-00900000 -> 02001-00400100 only change P/N
	2014/07/14	3. page23 add PCH_ID for DP sku & TBT sku
	2014/07/21	4. page54 change HDD LED logic & stuff DAZ_DSS_LED# pull-hi for PCH SSD
	2014/07/21	5. page59 change LED P/N follow pool & change 330 ohm -> 750ohm for ME request
	2014/07/29	6. page61 change J4502 footprint follow EN tool 7. page48 change J4801 footprint
	2014/07/30	8. change Rl3706, Rl3704, RL2707, RL3402, RJ415 0ohm->0.1u/16V(C3724, C3727, C3728, C3627, C3619) for EMI request 9. stuff C5403, C5404, C5405, C5419, C3103, C3109, C3110, C3111, C3112, C3107, 10. add 0.1u/16V DATA_LANE 0 (C25494) to Ground EMI request 11. add 0.1u/16V +5V(C3114) to Ground EMI request 12. add 0.1u/16V DATA_LANE 1 (C25495) to CK514 C5513 for A-dic 13. del C3606 cap for ACS_RCLK_AUD_C 14. add KSO on LCD_PWM_CON(R4804) for EMI request 15. change s stuff "C4473 5P->0.1u on KSP_KPD_CON for EMI request
	2014/08/04	16. update power schematic _0801 (PR8038 & PR8750)
	2014/08/05	17. change temp footpint for test

P/N	old footprint	new footprint	location
12013-00040700	nbs_usb_9p_049	nbs_u_usb_9p_019	J5201
12013-00040800	nbs_usb_9p_050	nbs_u_usb_9p_020	J6301 J6302
12022-00023500	nbs_u_mini_dp_20p_003	nbs_u_mini_dp_20p_004	J1101
12022-00043100	nbs_u_hdmi_19p_003	nbs_u_hdmi_19p_011	J4801
12014-00019600	nbs_u_audio_jack_6p_013	nbs_u_audio_jack_6p_017	J3801
-	-	-	-

2014/08/06	18. change choke temp footpint for test 19. change RN temp footpint for test 20. change screw hole(H704, H709, H710, H4711, H6712, H6718, H6720) 21. page20 stuff C2004 10PF->33PF on ACS_RCLK_AUD for EMI request 22. page54 change C5419 100PF->0.1uF on +5VDUS for EMI request
2014/08/07	23. change R3801 & R3802 18ohm -> 56ohm on AC_HP1_R & AC_HP1_L for meet EA audio test 24. change screw hole(H4701, H6702)

P/N	old footprint	new footprint	Location
12013-00040700	nbs_usb_9p_049	nbs_u_usb_9p_021	J5201
12013-00040800	nbs_usb_9p_050	nbs_u_usb_9p_022	J6301 J6302
12022-00023500	nbs_u_mini_dp_20p_003	nbs_u_mini_dp_20p_005	J1101
12022-00043100	nbs_u_hdmi_19p_003	nbs_u_hdmi_19p_012	J4801
12014-00019600	nbs_u_audio_jack_6p_013	nbs_u_audio_jack_6p_018	J3801
12014-00108800	nbs_u_dc_pwr_jack_3p_007	nbs_u_dc_pwr_jack_3p_008	J6001

2014/08/09	25. add s stuff KSO D4505 & D4506 on SMI_DAT & SMI_CLK for EMI request 26. change C5334 43P->KSO(SO362) on H_PROCHOT_S# R1 for EMI request 27. change C3010 0.01uF->0.1uF on PWR_SRC for EMI request 28. add KSO SO401 on CHARGRT_EC for EMI request 29. add KSO SO402 on CHARGRT_Gate for EMI request 30. change C5303 1000pF->KSO (SO383) on H_CHARGRT# for EMI request 31. change C1421 0.1uF->KSO (SO401) on CHARGRT_R for EMI request 32. add KSO SO401 on CHARGRT_EC for EMI request 33. add KSO SO402 on CHARGRT_Gate for EMI request 34. change C5302 1000pF->KSO (SO383) on H_CHARGRT# for EMI request 35. change C1421 0.1uF->KSO (SO401) on CHARGRT_R for EMI request 36. add KSO SO403 on PSYS for EMI request 37. change C5280 1000pF->KSO (SO393) on H_CHAR_PERIOD for EMI request 38. change C5405 0.1uF->KSO (SO402) on ALL_SYSTEM_PWROD for EMI request 39. add KSO SO404 on SM_CHARGPWROK for EMI Request 40. change C5235 0.01uF->KSO (SO385) on A_CPUPWRGD_R for EMI request 41. change C5019 1000pF->KSO (SO351) on EC_RST# for EMI request
2014/08/12	42. change 07G001007200(HDL) -> 07G001007100 SI2307 SI2308 SI202 DI803 DI804 D7001 DI805 DI806 D7002 D7703 D7713 PCH603 DI807 43. MI002.1 change net GND-VRP 44. change 09G012080007(HDL) -> 09G012080301 LI2207
	45. change Q4501->0ohm(M4515) on Smart_Sensor_int# 46. add M4701 EMI ID MAX CODE AREA 47. del M3002 0ohm for THRO_CPU#
2014/08/13	48. change R4501 49.9 ohm->220 ohm to meet eDP sequence 49. change R3411 0 ohm->120 ohm @mds(13603) on HDI_INT_CLK_ID for EMI request 50. change C4915-C4922 0.1u C402->C201 for HDMI 51. change C4923-C4930 0.1u C403->C202 C4923-C4931 for HDMI 52. change option 0/PCIE -> /PCIE 53. del Q7504 R7519 R3080 R3081 R3072 R7107 R7740 U7501 SC4 1.0 & add test point T3002 T3003 54. add R6740 & R6748 follow DDF 55. change R6705 & R6706 follow DDF
	56. change 07G001007200(HDL) -> 07G001007100 SI1301 57. change C7718 0.01uF->0.1uF on Q7704_Gate to meet HV sequence
2014/08/14	58. RN4701-RN4704 0ohm->0.1u(C4701-C4708) for DP 59. RN01103 RN1106 0402->0402 for co-lay 60. change SO402 for CHARGRT_Gate-> CHARGRT_PCH for EMI request 61. add stuff C4623 C4624 0.01u on LCD_BLEN_CON & KSP_KPD_CON 62. unstuff C4623 C4624 0.1u on LCD_BLEN_CON & KSP_KPD_CON
2014/08/15	63. del M6705 & M6706 follow DDF 64. RN4611-RN4614 5.1ohm->0ohm & Swap 65. stuff R4810 for HDMI 2.5dB pre-emphasis 66. change R4838 4.99K ohm -> 5.49K ohm for HDMI Heat
2014/08/18	stuff SI101 07G020076200 for XDD EDS stuff C3010 1UH3225M41000 on PWR_SRC_SW_R1 FOR EMI stuff C3010 1UH3225M41J90 on PWR_SRC for EMI stuff SO401 07G19-00010000 on CHARGRT_EC FOR EMI stuff SO402 07G19-00010000 on CHARGRT_PCH FOR EMI stuff SO001 07G19-00010000 on EC_RST# FOR EMI stuff SO403 07G19-00010000 on PSYS_PCH FOR EMI stuff SO402 07G19-00010000 on ALL_SYSTEM_PWROD FOR EMI stuff SI401 07G19-00010000 on CHARGRT_R FOR EMI stuff SO304 07G19-00010000 on SM_CHARGPWROK FOR EMI stuff SO383 07G19-00010000 on H_CHARGRT# FOR EMI stuff SO351 07G19-00010000 on H_CPUPWRGD_R
2014/09/23	page21 change RN2104A (RN1DK) -> R2105 R2112 R2114 R2115 (10K/0402) page21 change CLK_REQ2# pull-hi to +3VDUS (R6) page21 change CLK_REQ1# pull-hi to +3VS VTC1_3 page30 del V3001 2 add GS_LED# for NB LED page54 del R5408 R5409 & add R5405 R5406 & change logic for KB LED page59 change LED P/N follow pool & change 330 ohm -> 750ohm change R4844 R4849 R4845 R4871 optional 0/PCH# LS 8201->HDMI LS 8407 change s stuff 100PF(C3424) -> KSO(SO401) on ACS_RST#_AUD_1G for EMI
2014/09/24	change power mos on +PEX_VDD 07G005503210 -> 07G05-A0570000 for power RD request
2014/09/29	page47 change R6718 13020-00500100 -> 13020-00790900 on XDD Nut for ME request
2014/09/30	page47 add R6747 R6748 R6749 R6750 nut(13DNKN108040-1) for CPU
2014/10/03	change (C4546) 0.1UF/6.3V -> KSO 07G19-00010000 (D4507) on LCD_BLEN_CON for EMI request change (C4613) 0.1UF/16V -> KSO 07G19-00010000 (D4601) on KSP_KPD_CON for EMI request
2014/10/08	stuff D4501 & D4502 KSO on CMOS GEN for EMI request
2014/10/09	add D4703 EMI_ID_MARCOON for EMI
after MP 0/0	
2014/10/13	change D4501 D4502 KSO 07G02K011010 ->07G19-00010000 on camera GEN for EMI request change R4501 0ohm -> MBAD 029001230010 on ACS_RCLK_AUD for EMI request unstuff C5307 33PF/50V on ACS_RCLK_AUD_C change C2004 33PF -> 27PF on ACS_RCLK_AUD for EMI request
2014/10/14	change M5451 footprint
2014/10/22	change M5451 MBAD 029001230131 -> 18 ohm on ACS_RCLK_AUD for EMI request change C2004 27PF -> 33PF on ACS_RCLK_AUD for EMI request

X2.0	2014/11/17	add 0.1u/16V(C2008) on ACS_RST#_AUD for EMI change KSO(SO401) -> 0.1u/16V(C3424) on ACS_RST#_AUD_1G for EMI change R4501 0ohm -> MBAD 029001230131 on ACS_RCLK_AUD for EMI change R3620 & R3621 523 ohm -> 360 ohm on speak AC_OUT_L & AC_OUT_R for 金属音 add & unstuff M5326 0ohm for HWRST_MLAB to fix BB08异常
	2014/11/19	add 0.1/25V(C5314) on AC_BAT_SYS_ID for EMI add 0.1/25V(C5739) on ACS_OP_RST for EMI add 0.1/25V(C5740) on ACS_OP_ID for EMI add 0.1/25V(C5731) on G5731 PIN2 for EMI add 0.1/25V(C5431) on OP_SUS for EMI
	2015/03/14	change audio jack footprint nbs_u_audio_jack_6p_018 -> nbs_u_audio_jack_6p_013

Title :	Revision History		
Engineer:	RD1/EE1		
Size	Project Name		Rev
Custom	N501JW		2.0
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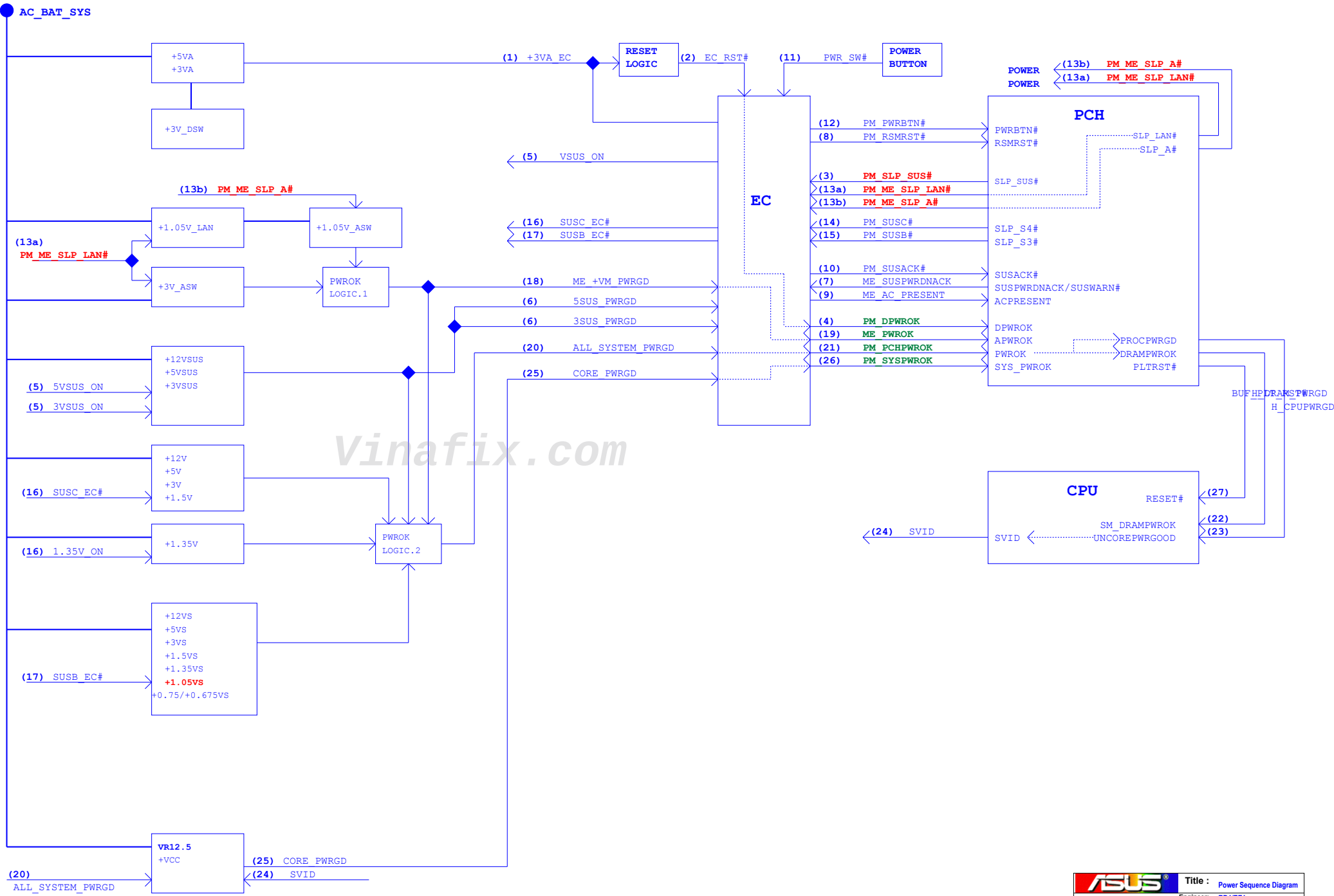
AC-IN Mode

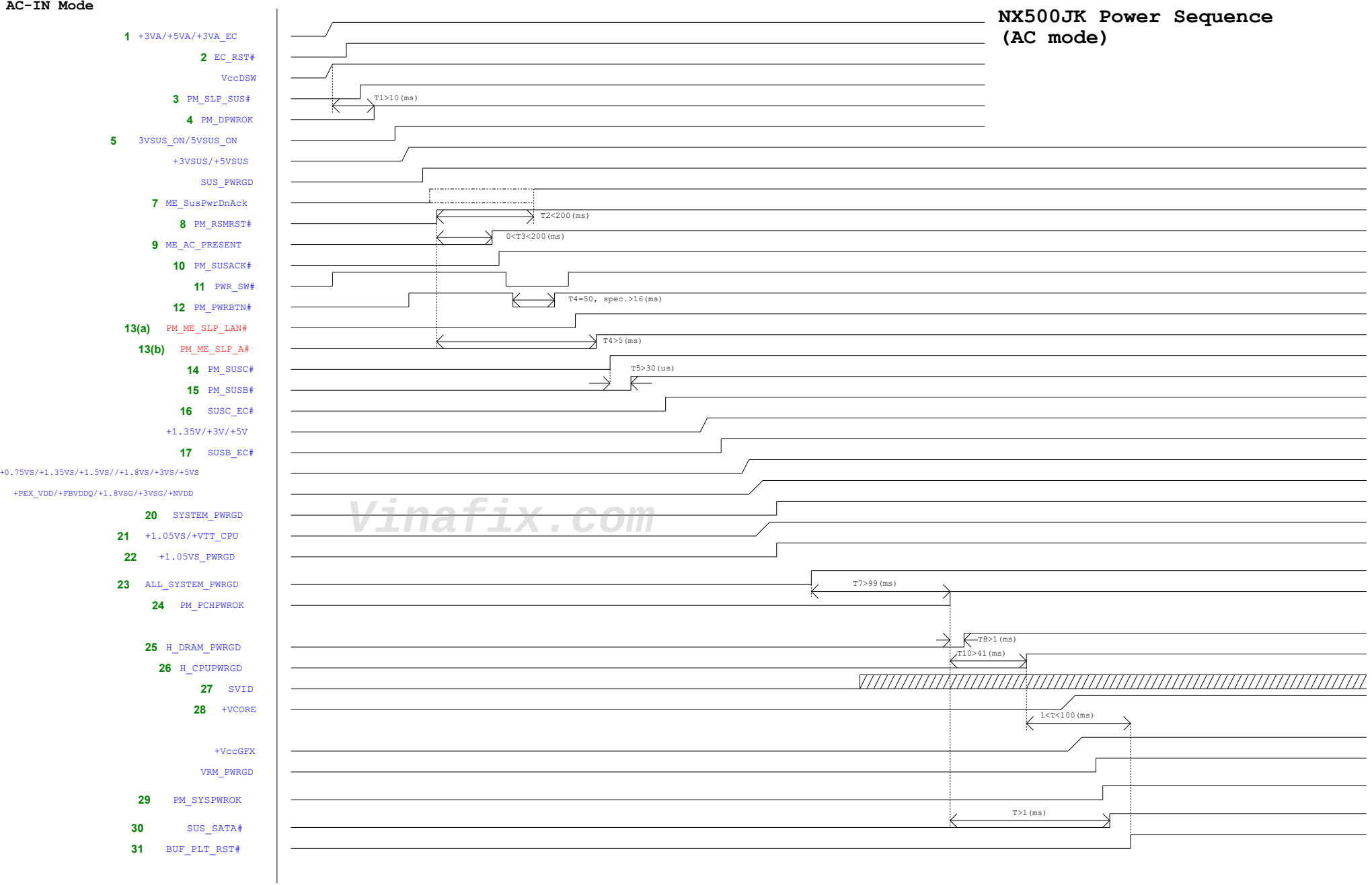
NX500JK Power On Sequence Diagram R1.0



ASUSTeK COMPUTER INC.	Title :	Power Sequence Diagram	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 96 of 98		

NX500JK Power Sequence (AC mode)

AC-IN Mode



ASUSTeK COMPUTER INC. NB8	Title :	Power Sequence(AC mode)	
	Engineer:	RD1/EE1	
Size: C	Project Name: N501JW		Rev: 2.0
Date: Monday, March 16, 2015	Sheet 97 of 98		